CALICE-UK Report to the PPARC Oversight Committee

March 14, 2006

1 Introduction

The CALICE collaboration is a worldwide effort to study calorimetry for the International Linear Collider (ILC). The collaboration is described in more detail in Section 2 below.

UK involvement in CALICE started in 2002. The PPRP granted seedcorn funds for five groups in December of that year to join the collaboration, with funding covering the period from January 2003 to March 2005. The UK contribution was in readout electronics, DAQ software and preparations for data analysis of the proposed beam tests of pre-prototype calorimeters.

In February 2005, seven UK groups then returned to the PPRP for further funding to complete the ongoing programme of beam tests as well as start several longer-term R&D programmes. The latter were intended to allow the UK groups to make significant contributions to the ILC detector TDRs which are due in 2009. Due to financial constraints, the proposed programme was cut by a small amount and, more significantly, was delayed by between 6 and 12 months as a condition of approval.

The ongoing beam test programme, Workpackage 1 (WP1), was approved as a continuation of the existing programme, again from seedcorn funds, and funding covers the period from April 2005 to March 2009.

The four longer-term programmes cover various aspects of calorimetry. Workpackage 2 involves R&D into DAQ systems for the calorimeter, where the aim is for a triggerless, commercial ("backplaneless") readout system off-detector. Workpackage 3 is studying a novel electromagnetic calorimeter design based on monolithic active pixel sensors (MAPS) to form a tungsten-silicon sampling calorimeter. Workpackage 4 is studying various aspects of the mechanical and thermal issues of building a high performance calorimeter of the type proposed. Workpackage 5 covers the software aspects, including modelling of alternative calorimeter designs, global detector performance and physics reach studies. All four of these workpackages are funded from October 2005 to March 2009.

The UK CALICE groups were also part of the successful EUDET infrastructure bid to the EU, which was approved in January 2006. This gives the UK funding to produce a DAQ system for reading out future calorimeter prototypes also being produced within the EUDET framework. This closely ties in with the work of WP2.

The individual workpackages are described in more detail in Sections 3 to 7. The Annexes contain the schedule and milestones for each workpackage. The financial and risk tables are supplied separately.

2 Status of CALICE

The CALICE collaboration is undertaking a major programme of R&D into calorimetry for the ILC. It now has 190 members from 32 institutes worldwide and is by far the largest group studying calorimetry for the ILC. It is also the only collaboration within the ILC community studying both electromagnetic (ECAL) and hadronic (HCAL) calorimeters in an integrated way.

The collaboration intends to test pre-prototypes of an ECAL along with at least two types of HCAL in electron and hadron beams over the next two years. The CALICE programme also covers simulation studies incorporating the results of these tests, all directed towards the design of an ILC calorimeter optimised for both performance and cost. In addition, the collaboration serves as an umbrella organisation for longer-term ILC calorimeter projects where developments can be tested together.

The CALICE ECAL pre-prototype is a silicon-tungsten sampling calorimeter and consists of 30 layers of silicon wafers interspersed between tungsten sheets. Each wafer layer contains a 3×3 array of silicon wafers, each containing 36 $1 \times 1\,\mathrm{cm}^2$ diode pads. There are around 10,000 channels in total occupying a volume of approximately $(18\,\mathrm{cm})^3$. The ECAL is mainly a collaboration between the French and UK groups, with the former responsible for the mechanics and silicon detectors and the latter for the readout electronics. The ECAL assembly is currently paced by the silicon wafer production; around 1/3 of the silicon wafers have been manufactured. There have been problems with wafer production throughout 2005 but the next delivery is expected this month. The schedule is for 2/3 of all 30 layers to be completed by May 2006 and the final 1/3 by July 2006.

The analogue HCAL (AHCAL) is a sampling calorimeter with 40 layers of steel absorber sheets instrumented with scintillator tiles. The total volume is approximately $(1\,\mathrm{m})^3$. The tiles are of varying sizes, with the highest granularity central region using $3 \times 3\,\mathrm{cm}^2$ tiles, increasing to $12 \times 12\,\mathrm{cm}^2$ for the outermost tiles. As the name implies, the readout will be analogue, with the off-detector electronics being common to the ECAL. The AHCAL has around 8,000 channels in total. It is a collaboration of many small European institutions but is lead by a large DESY group. Currently, eight layers have been assembled and it is scheduled to be completed by June 2006. It is complemented by a "tail-catcher", TCMT, consisting of 96 cm of iron instrumented with 16 layers of 5 mm $\times$ 5 cm scintillator strips, which will tag leakage and detect muons.

The digital HCAL (DHCAL) is a binary readout sampling calorimeter. The sensitive layers will be mainly resistive plate chambers (RPC) although for some of the tests, one or more layers may be replaced with gas electron multiplier (GEM) detectors. The RPC (or GEM) pads will be $1 \times 1\,\mathrm{cm}^2$, giving 380,000 channels, each reading one bit. Both the RPC and GEM developments are being done by US groups. As one of the main aims of the beam tests is to compare the performance of these HCAL options, the same absorber structure and tail catcher as for the AHCAL will be used, so as to eliminate any spurious differences which might otherwise arise. Hence, the DHCAL is also around $(1\,\mathrm{m})^3$ in volume. The DHCAL is being developed by US groups, who are currently applying for funds for the production of readout electronics (common to RPC and GEM). Assuming funding is secured, the DHCAL should then be completed early in 2007.

The first 14 layers of the ECAL were exposed to a low energy (up to 6 GeV) electron test beam at DESY in January and February 2005. This was a technical commissioning run to provide a first look at the ECAL performance. When enough of the remaining layers are available, it will move back onto the beam line at DESY to take data with full shower containment. This run is expected to last from April to June 2006.

The TCMT took data with one of its 16 layers during February 2006 in a hadron beam at FNAL, using 120 GeV protons and 16 GeV pions. This was again a technical commissioning run and around 1M events were collected. The run has now ended as the beam line has shutdown for several months. The TCMT may take further data before being shipped to CERN later in the year.

In July 2006, the ECAL, AHCAL and TCMT will move to CERN for tests in the North

Area H6 beam line. This will start with ECAL-only electron beams and AHCAL-only hadron beams up to around 100 GeV during July and August, respectively. Combined tests of all three systems in hadron beams will then take place in October. The aim is to collect around 100M events with a large variety of energies, types and angles of incidence.

Early in 2007, the ECAL and TCMT will move to FNAL to take hadron beam data with the DHCAL. The AHCAL will also be moved to take some runs in order to cross check the results against the CERN beam data. These tests are expected to continue throughout 2007 and it is hoped that another data sample of a similar or larger size will result.

3 WP1: Beam Test Programme

This workpackage has the highest degree of interaction with, and dependence on, non-UK groups. The beam test programme is outlined above. All the groups in CALICE are contributing to the beam test data taking and analysis although the UK groups have positioned themselves to be at the forefront of this work. The coming six months will be dominated by preparations for, and participation in, the main test beam runs of the CALICE pre-prototypes at DESY and CERN.

3.1 Task 1.1: Support for beam tests

The first PPRP seedcorn award funded the production of readout electronics for the ECAL and an online computing system for the whole experiment. Fabrication and purchase of the hardware for both of these items was completed within the period of that grant. Nine custom-designed CALICE Readout Cards (CRC)[1] were designed and fabricated by RAL/EID, each of which can read out 1728 channels. A total of six are needed for the ECAL. The computing system is based on standard PCs with commercial PCI-VME bus adapter cards. However, the UK-designed electronics has since been adopted by the AHCAL and TCMT for their readout systems. Hence a further seven CRCs have been produced through RAL during 2005, funded by non-UK groups. Delivery of these boards is almost complete. All other hardware for the DESY beam tests in mid 2006 is now in hand.

For the CERN beam tests later in 2006, commercial TDCs and ADCs for reading the CERN beam line tracking chambers and Čerenkov PID detectors, respectively, will be needed and these will be purchased by the UK.

There is still ongoing work to the firmware (at Imperial, Manchester and UCL) for the CRCs and to the software (at Imperial) for the online system. For the former, the main change needed is to fully use the large 8 MByte buffers on the CRCs; this will be needed for the CERN beam tests when the spill structure means the system will trigger during a spill, buffer the data on board and only read out after the spill. For the software, the remaining work is now in handling and reading multiple crates, implementing the various calibration runs needed for system tests and tuning the performance of the overall system. The target is to read out events at an average rate of 100Hz and some work will be needed to achieve this with the full system.

3.2 Task 1.2: DESY test beam

In December 2004 the first 10 layers of the ECAL pre-prototype, in which an area of $12 \times 18\,\mathrm{cm}^2$ in each layer was instrumented, were calibrated using around 1M cosmic muon events taken in Paris. Then in January-February 2005 the prototype, by then extended to 14 instrumented layers ($\sim 7.2X_0$), was moved to DESY for tests in an electron beam. All the UK groups contributed significantly to these activities, commissioning the off-detector electronics and DAQ system as

[1] M.Warren, "A 96 Channel, 16 Bit, 500kHz ADC and Bus LVDS-Based VME Readout System for the CALICE Electromagnetic Calorimeter," presented at IEEE/NSS04, Rome, October 2004.

well as running shifts. This run was highly successful, with around 20M events and some 250 GB of data being recorded. Electron beams of energies 1-6 GeV were fired at the detector at normal incidence and at angles of 10°, 20° and 30°. The detector was moved so that the beam was fired into each silicon wafer, and at various points near to the inter-wafer gaps.

The UK groups have played the leading rôle in the analysis of these data, and in presenting them at international meetings. Fig. 1 shows the signals recorded in a typical cell during the cosmic run. A clear separation between signal and noise is seen. In Fig. 1 we also show the distribution of the signal (peak of the Landau distribution above pedestal in ADC counts) and the signal/noise ratio for all 2160 pads calibrated. We note that the signal is uniform from pad to pad within $\sim 3\%$, and that the signal/noise ratio is narrowly peaked around an acceptable value of 8.2.

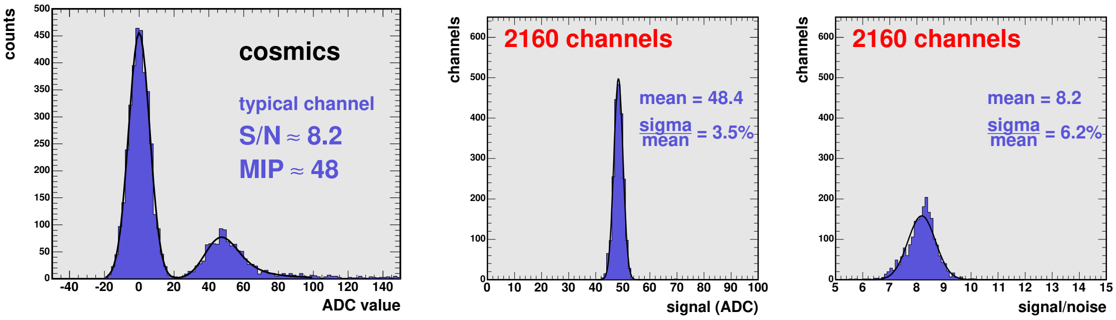

Figure 1: *Left: ADC distribution for a typical channel recorded during cosmic calibration; centre: Distribution of signal peak position for all channels; right: Distribution of signal/noise for all channels.*

Although the early 2005 ECAL run was largely an engineering and commissioning run, the data have been of significant use in establishing data analysis procedures, and in beginning the process of validation of the simulation tools. This work has largely been pioneered in Cambridge. A CALICE-UK member was chosen by the Collaboration to present these first results at two ILC workshops in 2005[2]. For example, using the data in which the normal incidence beam impinged on the detector close to the edge of a wafer, the response across the inter-wafer gaps can be studied. Using upstream drift chambers, the ~ 13 mm wide beam can be used to perform a position scan, yielding the results shown in Fig. 2. The wafers in the prototype are aligned in y, but staggered in x, leading to a broader but shallower drop in response in the latter case. Such results will be important in validating the simulation in preparation for optimising the design of a full scale detector.

The existing data have also revealed significant features of the Geant4 Monte Carlo simulation. In order to achieve a reasonable agreement between data and Monte Carlo, it was necessary to make two changes to the simulation:

- A detailed simulation of material upstream of the detector was required, including four drift chambers, four scintillator planes and 10 m of air, amounting to $> 10\% X_0$, in order to account for preshowering before the calorimeter. This simulation was provided by the RHUL group as their first contribution to CALICE.

[2]G.Mavromanolakis, CALICE *Si/W ECAL prototype - first test beam results* LCWS05, Stanford (March 2005) `http://www.hep.ph.ic.ac.uk/calice/others/050318lcws05/mavromanolakis.pdf`; G.Mavromanolakis, CALICE *Silicon Tungsten Electromagnetic Calorimeter* ECFA ILC Workshop, Vienna (November 2005) `http://www.hep.ph.ic.ac.uk/calice/others/051114vienna/mavromanolakis.pdf`.

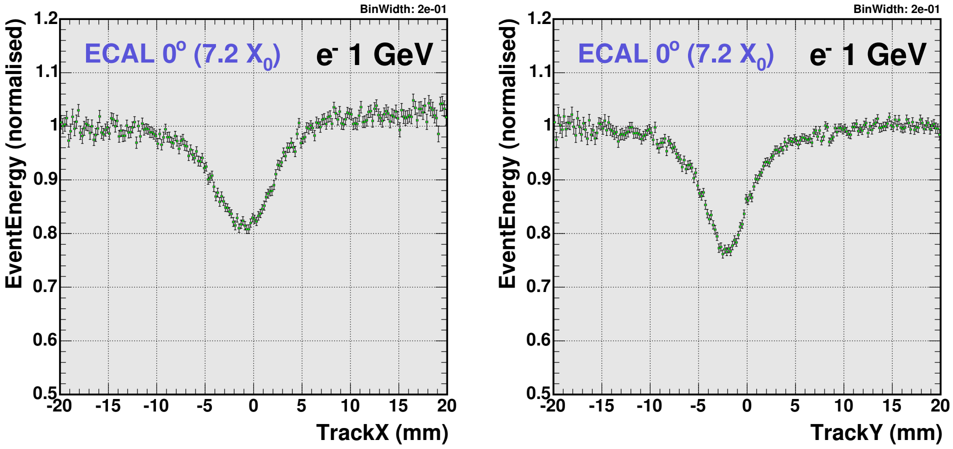

Figure 2: *ECAL response to 1 GeV electrons as a function of beam position close to an inter-wafer gap.*

- When using Geant4 version 7.1, it was found that the predictions of the simulation were dependent on the tracking (range) cutoff, and that a very low cutoff of ~ 200 nm was required in order to fit the data. Under these conditions the simulation was prohibitively slow[3]. The Geant4 authors have now addressed this issue, and the results of Geant4 version 8.0 are much more satisfactory.

For example, in Fig. 3 we show some typical comparisons between data and Geant4 simulation, for 1 GeV electrons at normal incidence. The improvement in agreement for Geant4 version 8.0 in terms of both normalisation and shape is evident.

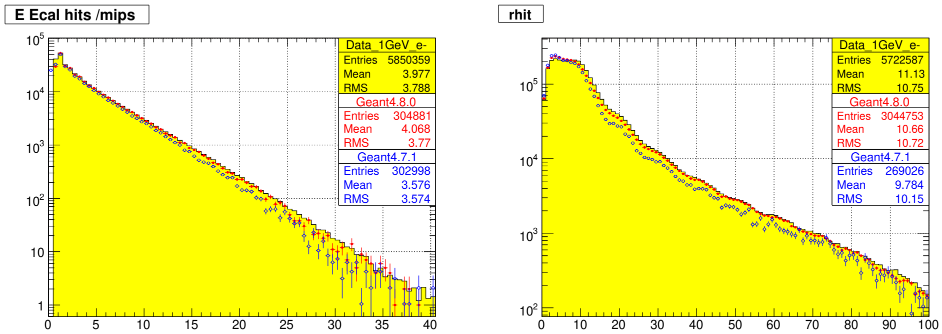

Figure 3: *Left: hit energies (in units of MIPs); right: radial distance of hits from the shower barycentre (in mm). The solid histogram shows data, the filled symbols represent Geant4 version 8.0 and the open symbols version 7.1, all normalised to the same number of events.*

A further round of electron beam tests at DESY is planned for April-June 2006. The ECAL will be more complete than in 2005, and will be integrated with those AHCAL planes which are ready. As well as provising valuable data on low energy electrons, this will be an important dry run for the major test beam campaign at CERN. Much of the commissioning, of hardware, of the DAQ and online software, of run procedures such monitoring, and of the offline software, can

[3] D.R. Ward, *Data/MC comparisons* ECFA ILC Workshop, Vienna (November 2005) `http://www.hep.ph.ic.ac.uk/calice/others/051114vienna/Ward.pdf`.

be carried out at DESY. Active discussions are currently taking place about the organisation of the test beam work, in which the UK groups have played a leading rôle. As one example, the Cambridge group has been setting up monitoring tools to allow rapid checks of data during the future test beam runs, starting at DESY. The UK groups intend to provide a strong presence in the test beam running at DESY, with emphasis on the DAQ and short-term monitoring and data checking.

With the appointment of three new PPARC-funded RAs, and the participation of the RHUL group, the effort in the UK on data analysis is starting to increase rapidly. For example, detailed studies of position and angular resolution are under way in Imperial, of digitization effects associated with the electronics and DAQ at UCL, and resolution studies at Birmingham.

3.3 Task 1.3: CERN test beam

Installation of the ECAL at CERN is anticipated for the end of June 2006. Approximately two weeks of high energy electron running with the ECAL are provisionally scheduled for July-August, followed by stand-alone tests of the AHCAL in August, and the main combined ECAL-AHCAL-TCMT data taking in October 2006. The UK groups are planning to continue their strong contribution in the test beam running when the equipment is moved to CERN, building on the expertise gained at DESY.

The major task of understanding the combined data and comparing with simulations will then be able to begin. The UK groups, because of their knowledge of the DAQ system, and their track record in data analysis and simulation already, are in a prime position to take the lead in this effort. We intend that the UK should maintain its leading rôle in understanding the CALICE data and in validating the Monte Carlo tools.

3.4 Task 1.4: FNAL test beam

The TCMT has already taken some test data at the Fermilab MTBF beam. In early 2007 the ECAL will move to Fermilab for combined hadron beam tests with the DHCAL. It is likely that the AHCAL will also take data at Fermilab to assist comparison between the CERN data and the DHCAL data. The detailed schedule at Fermilab is still unclear, but we anticipate significant data taking throughout 2007.

4 WP2: DAQ Studies

This workpackage consists of five separate tasks, which are to a greater or lesser degree interrelated. Compared with the original PPRP proposal, Tasks 2.1 to 2.4 were delayed by around six months while the Task 2.5 was delayed but also had its funding reduced.

However, the work on DAQ has been enhanced by additional funding gained from the European Union as part of the EUDET project.[4] A sum of about 330 keuro was awarded to UK universities to provide the DAQ system for upcoming EUDET technical prototypes, i.e. a part of the calorimeter which can be scaled up to the final detector, for the ECAL, the HCAL and forward calorimeter, FCAL. This has substantially enhanced our programme, replenishing (and more) the cuts incurred from the PPRP. The task dedicated to building an off-detector receiver, Task 2.5, which was reduced in scope, has essentially been extended with the extra source of funding. We will therefore fabricate more equipment to have a fully functional DAQ system to read out the EUDET technical prototypes and provide support up to the end of 2009 for this during testing both in the laboratory and in test-beam, if necessary.

[4]M. Wing, "Calorimeter data acquisition R&D", presented at EUDET Kick-off Meeting, DESY, Hamburg, February 2006, http://www.hep.ucl.ac.uk/lc/calice/DAQ/Meetings/EUDET_060215/wing.pdf

In collaboration with the French groups, we have settled on a design for the EUDET technical prototype and hence the requirements of our DAQ system. We can therefore now start with full confidence on designing our readout card as described in Task 2.5. This also fits to the original proposal where much of the work on DAQ intended for the first six months was book work and pre-design ideas. We therefore expect rapid progress on all tasks in the next six months as detailed below.

4.1 Task 2.1: Readout of prototype VFE ASICs

The current version of the VFE ASIC chip is being used to read out the existing CALICE ECAL pre-prototype. This chip does not meet the requirements for the ILC ECAL and the development of the design is an ongoing project in LAL/Orsay. The LAL group expect to have a new version of the ASIC developed for each of the next few years. The work we intend to do must therefore follow the pace of ASIC development and is dictated by this.

The next ASIC version will be ready in mid 2006 and it is intended that it be tested at CERN in beam in the current ECAL pre-prototype by replacing the ASIC version currently in use. This new ASIC will have power pulsing and may have an ADC with properties consistent with those required in the final ILC ECAL. This ASIC version can be read out with the current UK DAQ system for the ECAL pre-prototype. These additional features will be accommodated by changes to the firmware at Imperial. These modifications will be relatively simple if the analogue output is used, i.e. the ADC output is bypassed. However, the full test of the ASIC, using the on-ASIC ADC, will require more firmware effort and so will be done later in the run.

Further ASIC versions will be fabricated around the middle of 2007 and 2008. These should incorporate all features expected of the ILC ASIC. Initial tests of these chips will be done at Imperial and will require a simple PCB to read out multiple chips. This will give us valuable experience with these chips and enable us to feedback any design problems so that modifications can be made before the final ASIC design is produced for the EUDET technical prototype.

4.2 Task 2.2: Study of data paths over 1.5 m slab

As the EUDET technical prototype is now envisaged, a 1.5 m PCB which holds the silicon wafers and ASIC readout electronics (a "slab") will be needed. A functioning version of a slab will be built and Task 2.2 feeds in very important information to this design. Current designs propose having smaller PCBs stitched together to form a 1.5 m PCB as such a long board will be very difficult to manufacture. Although the French groups intend to have all data reduction done in the ASIC, a copper readout along the slab will still be challenging, with issues such as power dissipation, transmission across stitches and combining data paths from different ASICs. These developments have changed the scope somewhat due to the resources acquired to build the EUDET technical prototype. However, we will be providing vital input to the final design.

Initial studies on shorter PCBs were always planned as part of this project, but they have now taken on more importance rather than just as preliminary tests. Designs for the short PCBs have started and calculations of data rates and power dissipation are also well underway. A conceptual design is shown in Fig. 4.

However, it should be said that the method of stitching PCBs together is currently undefined and untested. In addition, a high degree of data suppression in the ASIC may not be necessary or desirable. Therefore our initial plan of investigating much higher rates along the PCB and the design of a 1.5 m board are still valid and will be pursued at Cambridge after the initial short-PCB studies.

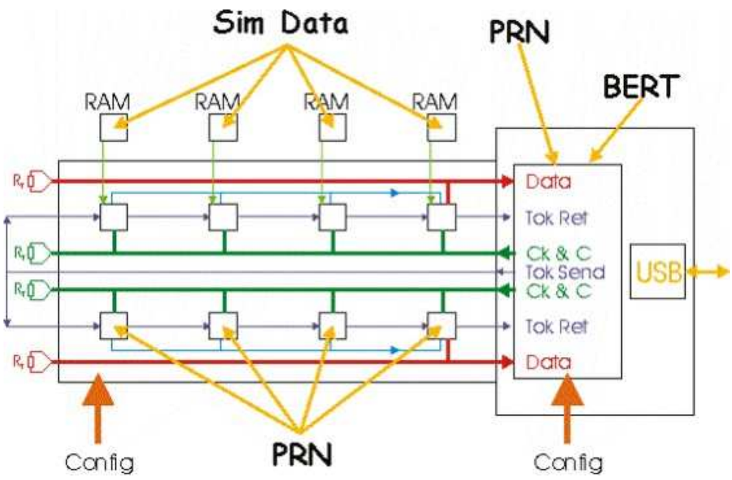

Figure 4: *Conceptual design of a short PCB to test efficiency of data transmission.*

4.3 Task 2.3: Connection from on-detector to the off-detector receiver

In this task we will set up test systems to validate the effectiveness of high-rate switching. This will allow us to design a future DAQ system which can cope with any foreseen data rates or, if a large amount of data reduction is done on-detector, use high-speed network systems to transmit data from more of the detector along a fibre and to fewer off-detector receivers. Both a conventional switching system is considered and also an optical network using an optical ("layer-1") switch.

Work has started in earnest on setting up a conventional 10 Gbit networking test bench. Throughputs have been measured at Manchester using different motherboards and the PCI-X standard with rates up to 6 Gbit/s achieved. Studies[5] on PCI-X are in the process of being adapted to investigate the performance of the more recent technology, PCI-Express. The optical network studies are not due to start until 2007.

4.4 Task 2.4: Transport of configuration, clock and control data

This task deals with communication from the off-detector receiver to the detector itself. One aspect considers the stability of FPGAs mounted at the edge of the detector slabs whilst the other investigates the sending of clock and control signals with commercial components all timed into the accelerator clock.

At UCL, a literature survey of the response of various FPGAs to radiation and rates of single event upsets has started. In general, it was thought that we should use the same FPGA (new and powerful) for all our studies, but depending on the outcome of this survey, this may not be the case for this task whereas for the off-detector receiver it will not be affected by such issues and so can be the most powerful available to suit our needs. The environment around the FPGA is being determined to assess the single event upset rate. This will be done using Monte Carlo simulations of the particle density around the FPGA. This would have been more advanced if we could have hired the UCL RA earlier.

The clock and control aspect of this task is just starting. It will benefit from much of the hardware development in Task 2.2 and UCL will incorporate aspects of the clock and control

[5] R.Hughes-Jones, P.Clarke and S.Dallison, "Performance of Gigabit and 10 Gigabit Ethernet NICs with Server Quality Motherboards," Grid Edition of Future Generation Computer Systems Volume 21, Issue 4, April 2005 p 469-488.

design into the test PCB. There will be close collaboration between the two groups, Cambridge and UCL, with the test PCB shared between the two.

4.5 Task 2.5: Prototype off-detector receiver

As stated previously, the extra funding from the EU has enhanced this task. The proposal to the PPRP was essentially based around producing PCI cards which would be used on the test bench. However, we will now provide a certain number (funded by the EU grant) for the EUDET technical prototypes. To be able to decide the exact functionality of the PCI card, we needed to know the specifications of the EUDET technical prototypes. The ECAL will have $\mathcal{O}(10^4)$ cells, which will mean that our design can easily cope with the expected data volume. The HCAL will be similar to the ECAL in numbers of channels while the FCAL will have a much smaller number. The Cambridge, RHUL and UCL groups propose a card which is flexible, can act as both a data receiver and transmitter, send configuration, clock and control signals, perform data reduction and handle high speed and volume. A sketch of such a card is shown in Fig. 5. It should also be flexible enough to read out the MAPS design, with the higher data

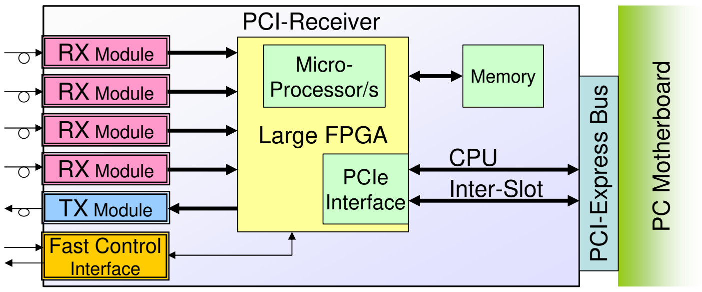

Figure 5: *Conceptual design of a customised PCI card.*

rates expected, as it is planned that these will be tested in the EUDET prototype, probably replacing a wafer layer.

Similar cards are available on the commercial market, however we do not know if they are flexible enough. For Task 2.3, Manchester bought a card which has a similar functionality. We will also consider other companies and buy a similar card for this task. This will help us assess the limitations of these cards and also specify in more detail the functionality. Work is also starting on the power of data reduction via clustering at this stage of the reconstruction before going to an event builder. Ideas of the functionality and more detailed design studies have now started with significant progress expected in the next six months.

5 WP3: MAPS studies

As one of the more expensive workpackages, these studies were delayed by around 12 months compared to the February 2005 proposal in order to fit within the PPARC cost envelope, although the scope of the workpackage was not reduced. The delay means these studies are currently at an early stage.

The baseline electromagnetic calorimeter design being considered within CALICE is a tungsten-silicon sampling calorimeter, where the sensitive silicon layers consist of diode pads. The pad size is assumed to be somewhere between 3×3 and $10 \times 10\,\mathrm{mm}^2$. This is much larger than the average distance between charged particles in an electromagnetic shower at high energies, where particle densities are around $100/\mathrm{mm}^2$. The diode pads also have to be sensitive to single particles (MIPs) for hadron track-shower matching in the hadronic calorimeter. This requires the analogue signal from each diode pad to be digitised to at least 10 to 14 bits, depending on pad size.

The MAPS concept is to replace the sensitive layers with MAPS detectors rather than diode pad detectors. The MAPS would incorporate much of the readout electronics and buffering directly on the sensor, removing the need for the external ASIC used in the diode pad case. The pixel size of the MAPS would be chosen to be small enough so that the chance of more than one particle passing through each pixel is small. This would allow binary readout of each pixel. Given a particle density of $100/\text{mm}^2$, it is clear the pixels have to be significantly smaller than the diode pads, namely of order $0.1 \times 0.1\,\text{mm}^2$. The data from each pixel will be buffered on the sensor during the ILC bunch train and read out in the long dead time between bunches.

5.1 Task 3.1: Sensor production and testing

The work within this workpackage so far[6] has concerned understanding the basic parameters of a MAPS calorimeter. There are three main strands:

1. The physical implementation and design of the MAPS sensors are being studied by RAL/EID. This work gives information on the physical size of the readout circuitry, in particular the buffer memories. Fig. 6 shows some layouts of various designs of memory cells and their sizes. To store the required data over an ILC bunch train, the memory cells define a minimum area and so set constraints on the pixel sizes. This work will build towards an actual sensor design; two rounds of sensors will be fabricated to test their performance over the next three years. In these first two rounds, the sensors would be designed in a $0.35\,\mu$m CMOS technology to minimise costs. Once the design is validated, finer feature technologies like 0.18 or $0.13\,\mu$m could be used longer-term, especially for a final ILC detector production. These technologies would be widely available at that stage, even for stitched sensors. They would allow denser designs and/or additional functionality.

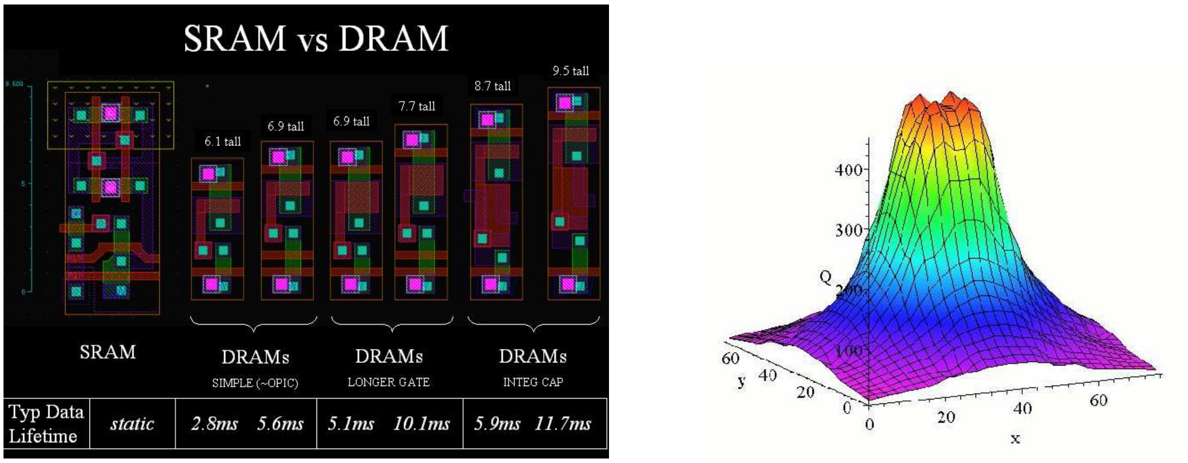

Figure 6: *Left: Possible MAPS memory designs and sizes. Right: Charge diffusion with the epitaxial layer for a point source energy deposit. The axis units are μm.*

2. The sensors are being modelled in a detailed device simulation in RAL/PPD. This gives information on properties such as the diffusion of charge within the epitaxial layer and hence the amount of charge detected per pixel. This is turn gives estimates of the efficiency

[6] See `http://www.hep.ph.imperial.ac.uk/calice/mapsMeetings/meetings.html`

and crosstalk of the pixels given a binary threshold. Fig. 6 shows the simulated charge diffusion within the epitaxial layer. The measurable results from these simulations will be tested against the real sensors when they are produced.

3. The calorimeter is being modelled in a physics simulation to estimate the global performance of a MAPS calorimeter compared to the baseline silicon diode version. This study, by the Birmingham and Imperial groups, will look at several aspects such as the electromagnetic shower energy and position resolutions, where a significant issue is the potential non-linearity introduced when multiple particles hit a pixel. Longer term, studies of the impact of a MAPS calorimeter on particle flow algorithms will be performed, as this is the main physics performance indicator for ILC calorimetry. The simulation will be compared and tuned to agree with the measurements and sensor simulations described above. These studies should allow an optimised MAPS calorimeter to be designed by the time of the ILC detector TDRs. (See also Sec. 7.3.)

In summary, progress on both the electronics design and sensor simulation has been good, with the sensor parameter space being narrowed significantly. The physics simulations have proceeded less rapidly, since the main effort for this will be from the RAs at Imperial and Birmingham, who have only been recruited recently.

The major milestones before the next Oversight Committee meeting are two reviews. The Preliminary Design Review at the end of April 2006 is intended to firm up the design concepts after the feasibility study and allow realistic sensor design to start. The Interim Design Review in August 2006 is a mid-way review to check on the progress of the sensor design.

6 WP4: Mechanical and Thermal Studies

Workpackage 4 deals with the mechanical and thermal aspects of the ECAL design and Manchester is responsible for the whole of this workpackage. This package was cut down heavily from our original proposal: we had planned to work on prototyping automated assembly techniques for reliably locating pads to the required precision, gluing them, and verifying the connections. However the PPRP decided this was premature at this stage of the project, and our budget in both manpower and funding was severely trimmed.

We hope to return to design of assembly procedures when the time is ripe for them, and meanwhile we still have two very significant avenues of investigation – studies of conducting glues and thermal simulation of the calorimeter slabs and associated electronics.

In addition to the glue studies and thermal simulations outlined below, Manchester personnel will begin to work on mechanical designs for the ECAL endcap calorimeter as part of the ILC detector concept studies. This is made possibly by the recruitment of Dr David Bailey to the project, who provides a significant increase in the Manchester academic involvement. There is currently little or no effort dedicated to this part of the calorimeter design and our preliminary discussions and expressions of interest have been very warmly received by the collaboration, who had been aware that this was a shortcoming in the overall programme which needed addressing.

Taking responsibility for a large detector component at this time will position the UK to contribute to the mechanical design section of the detector TDRs and, in due course, to be well placed to take on construction of all or part of the ECAL endcaps. If there is good progress here, we may well come to the Oversight Committee with a request to use our working allowance to boost the effort in this area.

6.1 Task 4.1: Thermal studies

The final ILC detector slabs holding the silicon wafers cannot have conventional active cooling installed along their length without compromising the performance of the calorimeter. The maximum operating temperature of the slabs imposes stringent upper limits on the power consumption of the front end electronics. It is, therefore, crucial to understand the thermal environment of the detector – not least because high temperature increases the electronic noise, but also because of the effect it may have on mechanical stability of the slabs. Thermal simulations will define the envelope within which the detector can operate, and will ultimately define the maximum power per readout channel.

Thermal simulations of individual slabs are now being carried out in Manchester using the FlexPDE package. Fig. 7 shows an example of the first results of these simulations. The models will be refined using engineering drawings of the modules provided by our French collaborators. Early results indicate that in the present design there will be a temperature difference of 14° C across the slab: the LAL/Orsay ASIC designers are evaluating whether this would seriously affect the electronics performance.

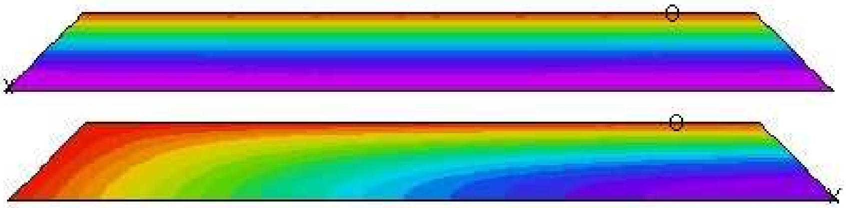

Figure 7: *Example heat distribution of a simulated detector module for two different cooling scenarios. Top: Cooling only at the top face. Bottom: Cooling at both the top and left faces.*

Ideas for using binary cooling for the detector slabs are also under consideration. This technique uses evaporative cooling to remove heat. This method has the advantage of not requiring a large temperature drop through the cooling circuit and therefore reduces dangers from condensation.

6.2 Task 4.2: Glue studies

The current design of the ECAL uses conductive glue to attach the silicon diode pads to the thin PCB carrying the front-end ASICs. This glue provides both the mechanical and electrical contact between the silicon and the PCB. It is thus of crucial importance to understand the long-term effects of temperature and environment on the glue properties since, at the ILC, detector slabs may be inaccessible for long periods of time. Other detectors using conducting glue have experienced problems of various types, and we need to understand fully the possibilities for loss of contact and the physics that drives them.

An environmental chamber at Manchester has now been commissioned and measurements are underway. Fig. 8 shows measurements being made on Epo-Tek E4110, the glue currently used by CALICE. The resistance of the glue increases as expected with temperature but clearly fails to return to its previous value when cooled. More information is clearly of great impostance, and these studies are ongoing.

Recently, other issues connected with gluing silicon diodes have been identified. The dark current measured on recently glued wafers has shown a large increase immediately after gluing. Depending on the manufacturer of the wafer, the dark currents slowly recover to those of the unglued silicon over periods ranging from a few days to months. The reason for this is not currently understood, but it is assumed to be due to the interaction of the glue with the passivation

Figure 8: *Measurements of the resistance of conductive glue underway at Manchester. The green line shows the temperature variation inside the envionmental chamber, the red line the resistance of the glued structure.*

layer on the wafer. This is a major problem as, even if the diodes recover fully, the delay caused by waiting for the currents to return to normal will seriously impact assembly time.

These problems will be investigated at Manchester using, in the first instance, test-pads from the wafers made in the Czech Republic. Ideally these tests would be carried out on a production wafer. However, due to the wafer production problems mentioned in Sec. 2, all wafers are currently required for the prototype calorimeter so detailed investigations will be delayed until sufficient wafers are available.

7 WP5: Physics and Simulation

The simulation and physics work package is now starting to produce results. New RAs have taken up project posts at Birmingham, Imperial and UCL and are contributing to all aspects of the project software. There are new Ph.D. students taking part in the project at Imperial and RHUL. In addition, a new RA has started at Cambridge in a University-funded post, mainly to work on global detector design studies. Regular meetings have been taking place since October 2005, with notes from these and related software information maintained on our project web pages[7].

The R&D work being carried out in the UK is part of the larger international effort to optimise both the design of the detector and the development of algorithms for event reconstruction. Overall detector design (WP5.2) is based on three detector concept studies, LDC, SiD and GLD. These are intended to be fully global in their participation, but in practise they are dominated by separate regions (Europe, North America, Asia, respectively). The natural starting point for the UK work is in LDC, the successor to the TESLA detector of which the CALICE ECAL was a major component. The design optimisation process depends on results obtained from both single particle studies and physics analyses benchmarks. The development of simple, robust physics analyses (WP5.4) requires the use of a complete event reconstruction package, including an energy flow algorithm. Since the original proposal of January 2005, a first version of such a package has been developed (outside the UK) based on the Marlin/LCIO framework. This allows WP5.4 to proceed in parallel with UK effort towards developing more performant energy flow algorithms (WP5.1). Finally, at the lowest level in the programme, WP5.3 will support

[7]CALICE UK Simulation and Physics web pages, `http://www.ep.ph.bham.ac.uk/exp/CALICE/sim/`.

simulations to be used in other WPs for the development of DAQ (WP2), MAPS sensors (WP3) and mechanical design aspects (WP4).

The progress already made in all four tasks of the project outlined in the CALICE proposal, both within the UK and in the wider international context, is summarised below.

7.1 Task 5.1: Energy Flow algorithms

The release of the Marlin package in August 2005 helps our task considerably as it has allowed the development of a physics analysis for detector optimisation to start, decoupled from our efforts for particle flow and particle resolution studies. It also serves as a basis for development of new algorithms within the UK, a first example of which (PandoraPFA[8]) is being presented at LCWS06. In terms of reconstruction within calorimeters themselves, the Minimal Spanning Tree algorithm developed at Cambridge for calorimeter clustering, gNIKI[9], has now been made publically available to the ILC community in the form of a Marlin processor, and can therefore be easily studied by others.

7.2 Task 5.2: Global detector design

Energy resolution studies have been carried out by several people from both the RHUL and Cambridge groups, investigating the relative performance to single photons, electrons and pions in detector models derived from the original TESLA detector. The resolution for single photons in the latest baseline LDC model, LDC01 (with a 30 layer ECAL), was found to be $\Delta E/E = 14.4\%/\sqrt(E(\mathrm{GeV})) + 0.5\%$, while that for single electrons (above 5 GeV) was $\Delta E/E = 16.3\%/\sqrt(E(\mathrm{GeV})) + 0.3\%$. Studies using the earlier LDC00 model (40 layer ECAL) were found to have a $\sim 4\%$ (absolute) smaller statistical term and approximately double the constant term. Details of the studies performed in the UK are included as part of the LDC Detector Outline Document, being presented at LCWS06 this month, and on the project web pages.

7.3 Task 5.3: Workpackage support

Work on implementing a more complete simulation of the MAPS sensors in `Mokka` for the LDC01 model is in progress, in line with our plans. The very large number of sensors in the detector ($\sim 10^{12}$) presents some technical difficulties concerning assigning unique identifiers to each active sensor, and we are considering the relative merits and implications of several alternative implementations. The Birmingham group had already carried out a study of single particle enery resolution using MAPS sensors in the SiD detector using the `Geant4`-based `slic` Monte Carlo[10]. An illustration of this implementation is given in Fig. 9. Relative performance in terms of energy resolution and linearity of response were also studied for various pixel pitches.

7.4 Task 5.4: Physics studies

Physics studies using the ZHH process ($Z \to e^+e^-$ or $Z \to \mu^+\mu^-$) with $m_H = 120\,\mathrm{GeV}$ at $\sqrt{s} = 500\,\mathrm{GeV}$ are underway at RHUL. This process allows the Higgs self-coupling to be determined and serves as a convenient benchmark for particle flow algorithms and calorimeter cluster reconstruction, owing to the multi-jet nature of the final state. Samples of signal and Standard

[8] PandoraPFA, M.Thomson, `http://indico.cern.ch/contributionDisplay.py?contribId=83&sessionId=10&confId=568`

[9] gNIKI, G.Mavromanolakis, `http://www.hep.phy.cam.ac.uk/gmavroma/calice/gNIKI`.

[10] N.Watson, Talk at CALICE meeting, DESY, Oct 2005, `http://www.hep.ph.ic.ac.uk/calice/calice/051012desy/watsona.ppt`.

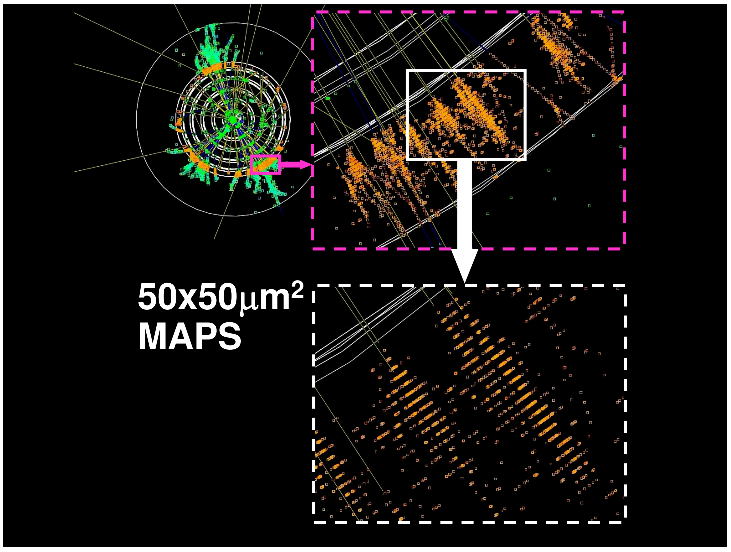

Figure 9: *Example SiD event illustrating granularity of MAPS pixel implementation in* `slic`*, showing the "tracking" aspects of the calorimeter which are needed for particle flow algorithms.*

Model background events have been simulated using `Mokka` with both LDC00 and LDC01 detector models and reconstructed within Marlin. Separation of signal from dominant background is achieved using a mass difference metric in a cut-based analysis, and fits are made to reconstructed mass peaks for Z and H. It is noted that there are differences in the efficiency of e.g. the track finding algorithm when applied to LDC01 and LDC00 simulations, which indicates the difficulty of trying to separate intrinsic detector performance from that of the algorithms used.

Fig. 10 shows the example of the $Z \to \mu^+\mu^-$ channel. A slightly increased width in the

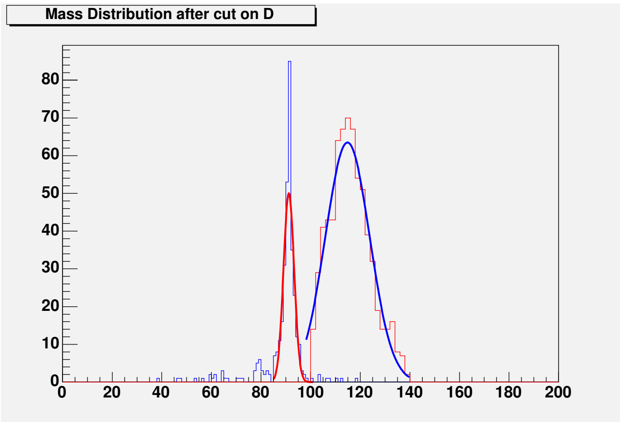

Figure 10: *Example of reconstructed Z and H masses in ZHH process, ($Z \to \mu^+\mu^-$, $H \to$ jets), using the LDC01 detector concept in* `Mokka`*. The fitted widths of the Z and Higgs peaks are 2.1 GeV and 9.0 GeV, respectively, the latter being dominated by experimental resolution.*

reconstructed Z mass in the $Z \to \mu^+\mu^-$ channel is observed in LDC01, an expected consequence of the reduction in the number of TPC layers. A refinement of the analysis in which the high energy charged leptons are explicitly identified and excluded from the jet finding process has recently been implemented. This significantly ($\sim 30\%$) improves the reconstructed Z mass resolution but introduces a few GeV bias in the reconstructed Higgs mass, which is currently under investigation.

8 Summary

The CALICE programme is about to enter an exciting period, with a much more complete ECAL in the beam at DESY, followed by combined beam tests at CERN of the ECAL and AHCAL later in 2006. The UK contribution to this is organised through WP1. Although the beam tests are later than assumed in the original schedule, the UK contributions in the electronics and DAQ have been tested quite thoroughly and are close to being completed.

The workpackages other than WP1 have only started in October 2005 and so are all at a preliminary stage, with no significant problems identified yet.

Annex A: Workpackage Details

Annex A1: Workpackage 1

Responsible institutes

Birmingham, Cambridge, Imperial, RHUL and UCL are the responsible institutes, with D.R.Ward (Cambridge) being the workpackage manager.

Schedule

Workpackage 1	FY05/06				FY06/07				FY07/08				FY08/09			
	1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4
Task 1.1: Support for beam tests																
Complete board firmware	=	=	=	=	=											
Optimise DAQ software	=	=	=	=	=	=	=									
Upgrade DAQ for HCALs				=	=	=	=	=								
Task 1.2: DESY test beam																
Understand beam line	=	=	=	=												
Generate MC samples	=	=	=	=	=	=										
Test beam running					=											
Tune detector simulation	=	=	=	=	=	=										
Data/MC comparisons	=	=	=	=	=	=	=									
Publish results							=	=								
Task 1.3: CERN test beam																
Compare hadron MCs		=	=	=	=	=	=	=								
Understand beam line					=	=										
Generate MC samples					=	=	=	=								
Test beam running						=	=									
Data/MC comparisons						=	=	=	=							
Publish results									=	=						
Task 1.4: FNAL test beam																
Understand beam line							=	=	=	=						
Generate MC samples							=	=	=	=	=	=				
Test beam running								=	=	=	=					
Data/MC comparisons								=	=	=	=	=	=			
Publish results													=	=	=	=

Milestones

Milestone	Scheduled Date	Within Grant Period (months)	Comment
Completion of data-taking at the DESY ECAL-only beam test	End Jun 06	15	Before next OsC meeting
Completion of data-taking at the CERN ECAL and AHCAL beam test	End Oct 06	19	
Completion of data-taking at the FNAL ECAL and AHCAL/DHCAL beam test	End Dec 07	33	

Deliverables

The main UK deliverables are:
Operating hardware, firmware and software for the data acquisition system for the ECAL, AHCAL and TCMT detectors.
Major contribution to publication of beam test results from all three data-taking periods.

Annex A2: Workpackage 2

Responsible institutes

Cambridge, Imperial, Manchester, RHUL and UCL are the responsible institutes, with M.Wing (UCL) being the workpackage manager.

Schedule

Workpackage 2	FY05/06		FY06/07				FY07/08				FY08/09			
	3	4	1	2	3	4	1	2	3	4	1	2	3	4
Task 2.1: Readout of prototype VFE ASICs														
ASIC tests using existing electronics					=	=								
Design and layout of PCB						=	=	=			=			
Write test PCB firmware						=	=	=			=			
Readout ASICs in bulk								=	=	=		=	=	=
Task 2.2: Study of data paths over 1.5 m slab														
Preliminary design studies and preparation	=	=	=	=	=									
Short board fabrication and tests					=	=	=	=	=	=				
Long board fabrication and tests										=	=	=	=	=
Task 2.3: Connection from on-detector to the off-detector receiver														
Study of technologies and test criteria	=	=	=	=										
Set up and operate 10 Gbit test-bench				=	=	=								
Examine traffic flow performance						=	=	=	=	=				
Link Test for optical network								=	=	=				
Explore switching performance										=	=	=	=	=
Task 2.4: Transport of configuration, clock and control data														
Radiation tolerance and SEU rates	=	=	=	=										
Test system on high-speed network		=	=	=	=	=	=							
Evaluate the clocking requirements					=	=	=	=						
Build network for testing trigger timing								=	=	=				
Extend to 10000 link test system										=	=	=	=	=
Task 2.5: Prototype off-detector receiver														
Investigation of latest PCI technology	=	=	=											
Design and build PCI card			=	=	=									
Test PCI card					=	=	=							
Fabricate PCI cards and setup test system							=	=	=					
Efficiency and volume of data transfer									=	=	=	=	=	=

Milestones

Milestone	Scheduled Date	Within Grant Period (months)	Comment
Task 2.1: Readout of prototype VFE ASICs			
Complete build and programming of board to read 2007 production ASIC chips	End Sep 07	24	
Complete build and programming of board to read 2008 production ASIC chips	End Jun 08	33	
Task 2.2: Study of data paths over 1.5 m slab			
Complete build of short, 0.5 m, board for data transfer tests	End Dec 06	15	
Complete build of long, 1.5 m, board for data transfer tests	End Dec 07	27	
Task 2.3: Connection from on-detector to the off-detector receiver			
Setup of 10 Gbit networking test bench	End Mar 07	18	
Setup optical networking test bench	End Dec 07	27	
Task 2.4: Transport of configuration, clock and control data			
Complete test system for reprogramming FPGAs	End Dec 06	15	
Complete test bench for method of synchronising clock and control data	End Dec 07	27	
Task 2.5: Prototype off-detector receiver			
Build and test prototype PCI card	End Dec 06	15	
Fabrication of final PCI cards and setup of test system	End Jun 07	21	

Deliverables

The main deliverables are:
Provide readout board for testing prototype ASIC chips.
Produce a functional pre-prototype of a PCI off-detector receiver card.
Write one or more linear collider notes on results of data acquisition workpackage.
Position UK groups to be in clear lead in the area of DAQ so as to later write chapter on data acquisition for calorimeter for the TDR.

Annex A3: Workpackage 3

Responsible institutes

Birmingham, Imperial, RAL/EID and RAL/PPD are the responsible institutes, with P.D.Dauncey (Imperial) being the workpackage manager and R.Turchetta (RAL/EID) the workpackage lead engineer.

Schedule

Workpackage 3	FY05/06		FY06/07				FY07/08				FY08/09			
	3	4	1	2	3	4	1	2	3	4	1	2	3	4
Task 3.1: Sensor production and testing														
Initial feasibility study of options	=	=	=											
First sensor design			=	=	=									
First sensor fabrication						=	=							
Basic functional tests							=							
Detailed bench tests								=	=	=				
Second sensor design								=	=					
Second sensor fabrication										=	=			
Basic functional tests											=			
Detailed bench tests											=	=	=	=
Beam test PCB design and fabrication									=	=	=	=		
Beam test													=	=

Milestones

Milestone	Scheduled Date	Within Grant Period (months)	Comment
Preliminary Design Review	End Apr 06	7	Before next OsC meeting
Interim Design Review	End Aug 06	11	Before next OsC meeting
Interim Design Review	End Dec 06	15	
First fabrication round completed	End Apr 07	19	
Interim Design Review	End Sep 07	24	
Final Design Review	End Dec 07	27	
Second fabrication round completed	End Apr 08	31	
Beam test started	End Oct 08	37	

Deliverables

The main deliverables are:
Evaluation of whether MAPS are a viable option for silicon-tungsten ILC ECAL.
If the concept is proved valid, then a working MAPS pre-prototype for the ECAL application.

Annex A4: Workpackage 4

Responsible institutes

Manchester is the responsible institute, with D.Bailey (Manchester) being the workpackage manager.

Schedule

Workpackage 4	FY05/06		FY06/07				FY07/08				FY08/09			
	3	4	1	2	3	4	1	2	3	4	1	2	3	4
Task 4.1: Thermal studies														
Chip measurements		=	=	=										
Thermal simulation				=	=	=								
Thermal measurements						=	=	=	=	=				
Thermal design							=	=	=	=				
Cooling system									=	=	=	=	=	=
Task 4.2: Glue studies														
Review current knowledge		=	=	=										
Studies of ageing					=	=	=	=						

Milestones

Milestone	Scheduled Date	Within Grant Period (months)	Comment
Task 4.1: Thermal studies			
Measured thermal outputs of readout chips	End Sep 06	12	Around next OsC meeting
Thermal simulation of realistic detector configuration	End Mar 07	18	
Task 4.2: Glue studies			
Literature search of existing glues	End Sep 06	12	Around next OsC meeting

Deliverables

The main deliverables are:
A report on cooling system issues and possibilities, to be used as input for the design of the detector.
A report validating the glue and gluing techniques to be used.

Annex A5: Workpackage 5

Responsible institutes

Birmingham, Cambridge, Imperial, RHUL and UCL are the responsible institutes, with N.K.Watson (Birmingham) being the workpackage manager.

Schedule

Workpackage 5	FY05/06		FY06/07				FY07/08				FY08/09			
	3	4	1	2	3	4	1	2	3	4	1	2	3	4
Task 5.1: Energy Flow algorithms														
Resolution/algorithm brainstorming	=	=	=	=										
Tool definitions		=	=											
Evaluation of existing codes			=	=										
Algorithm implementation				=	=	=								
Physics benchmark results						=	=							
Algorithm development							=	=	=	=	=	=	=	=
Task 5.2: Global detector design														
Performance, single particles (LDC)	=	=	=	=										
Performance, physics benchmark (LDC)			=	=	=									
Other detector concepts					=	=	=							
Further physics benchmarks								=	=	=				
Detector parameter variation					=	=	=	=	=	=	=	=		
Optimisation for each concept				=	=	=	=	=	=	=	=	=	=	=
Task 5.3: Workpackage support														
DAQ local clustering				=	=	=								
Mechanical imperfections							=		=	=				
MAPS into `Mokka`	=	=	=											
MAPS sensor variation studies			=	=	=	=								
MAPS test beam										=	=	=	=	=
Task 5.4: Physics studies														
Survey existing analyses/benchmarks	=													
Implement first analysis		=	=	=										
Develop alternative analysis benchmark					=	=	=	=						
Hadronic modelling sensitivity				=	=	=	=	=	=	=	=	=	=	=

Milestones

Milestone	Scheduled Date	Within Grant Period (months)	Comment
Task 5.1: Energy Flow algorithms			
Comparison of existing energy flow algorithms	End Jun 06	9	Before next OsC meeting
Physics benchmark results	End Mar 07	18	
Task 5.2: Global detector design			
Initial results from single particle studies	End Mar 06	6	Before next OsC meeting
First physics benchmark of detector concept	End Sep 06	12	Around next OsC meeting
Task 5.3: Workpackage support			
MAPS implemented in Mokka	End May 06	8	Before next OsC meeting
First results from mechanical imperfection simulations	End Dec 07	27	
Simulations for MAPS test beam	End Mar 08	30	
Task 5.4: Physics studies			
Present status at regional ILC software workshop	End Apr 06	7	Before next OsC meeting
Generic physics analysis implemented	End Sep 06	12	Around next OsC meeting
Alternative physics benchmark available for global detector optimisation	End Sep 07	24	
Report summarising hadronic modelling studies	End Jun 08	33	

Deliverables

The main deliverables are:
Code for generic energy flow algorithm.
Significant contributions to detector CDRs and LoIs, positioning the UK to contribute strongly to the TDR.
Positions of responsibility in global LC software activity.
Report on simulations for Workpackages 2, 3 and 4.
Framework for physics analysis benchmarking of detector designs.