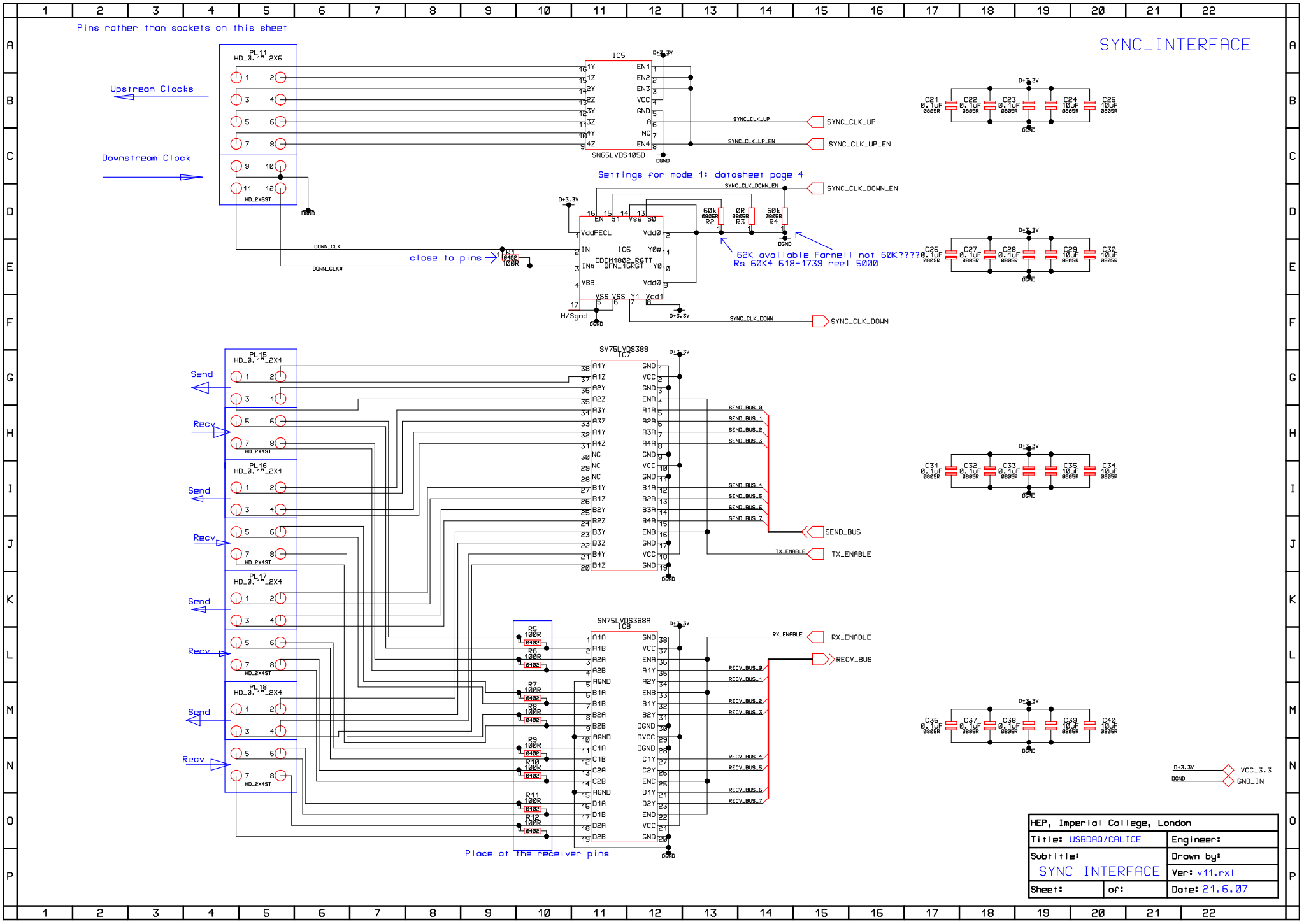

SYNC_INTERFACE
Pins rather than sockets on this sheet
Upstream Clocks
Downstream Clock
PL11
HD_0.1"_2X6
HD_2X6ST
IC5
SN65LVDS105D
SYNC_CLK_UP
SYNC_CLK_UP_EN
Settings for mode 1: datasheet page 4
SYNC_CLK_DOWN_EN
SYNC_CLK_DOWN
IC6
CDCM1802_RGTT
QFN_16RGT
close to pins
DOWN_CLK
DOWN_CLK#
62K available Farnell not 60K????
Rs 60K4 618-1739 reel 5000
PL15
PL16
PL17
PL18
HD_0.1"_2X4
HD_2X4ST
Send
Recv
SV75LVDS389
IC7
SEND_BUS
TX_ENABLE
SN75LVDS388A
IC8
RX_ENABLE
RECV_BUS
Place at the receiver pins
VCC_3.3
GND_IN
HEP, Imperial College, London
Title: USBDAQ/CALICE
Engineer:
Subtitle:
SYNC INTERFACE
Drawn by:
Ver: v11.rxl
Sheet:
of:
Date: 21.6.07