Pins rather than sockets on this sheet

SYNC_INTERFACE

Upstream Clocks

Downstream Clock

PL11 HD_0.1"_2X6

HD_2X6ST

DGND

IC5 SN65LVDS105D

D+3.3V

SYNC_CLK_UP

SYNC_CLK_UP_EN

SYNC_CLK_UP

SYNC_CLK_UP_EN

C21 0.1UF 0805R

C22 0.1UF 0805R

C23 0.1UF 0805R

C24 10UF 0805R

C25 10UF 0805R

Settings for mode 1: datasheet page 4

SYNC_CLK_DOWN_EN

SYNC_CLK_DOWN_EN

60k 0805R R2

0R 0805R R3

60k 0805R R4

DOWN_CLK

DOWN_CLK#

close to pins

R1 0402 100R

IC6 CDCM1802_RGTT QFN_16RGT

52K available Farnell not 50K???? Rs 60K4 618-1739 reel 5000

C26 0.1UF 0805R

C27 0.1UF 0805R

C28 0.1UF 0805R

C29 10UF 0805R

C30 10UF 0805R

H/Sgnd

SYNC_CLK_DOWN

SYNC_CLK_DOWN

PL15 HD_0.1"_2X4

PL16 HD_0.1"_2X4

PL17 HD_0.1"_2X4

PL18 HD_0.1"_2X4

HD_2X4ST

Send

Recv

IC7 SV75LVDS389

SEND_BUS_0

SEND_BUS_1

SEND_BUS_2

SEND_BUS_3

SEND_BUS_4

SEND_BUS_5

SEND_BUS_6

SEND_BUS_7

SEND_BUS

TX_ENABLE

TX_ENABLE

C31 0.1UF 0805R

C32 0.1UF 0805R

C33 0.1UF 0805R

C35 10UF 0805R

C34 10UF 0805R

IC8 SN75LVDS388A

R5 100R 0402

R6 100R 0402

R7 100R 0402

R8 100R 0402

R9 100R 0402

R10 100R 0402

R11 100R 0402

R12 100R 0402

RX_ENABLE

RX_ENABLE

RECV_BUS

RECV_BUS_0

RECV_BUS_1

RECV_BUS_2

RECV_BUS_3

RECV_BUS_4

RECV_BUS_5

RECV_BUS_6

RECV_BUS_7

Place at the receiver pins

C36 0.1UF 0805R

C37 0.1UF 0805R

C38 0.1UF 0805R

C39 10UF 0805R

C40 10UF 0805R

D+3.3V VCC_3.3

DGND GND_IN

HEP, Imperial College, London		
Title: USBDAQ/CALICE		Engineer:
Subtitle: SYNC INTERFACE		Drawn by:
		Ver: v12b4.rx1
Sheet:	of:	Date: 3.7.07