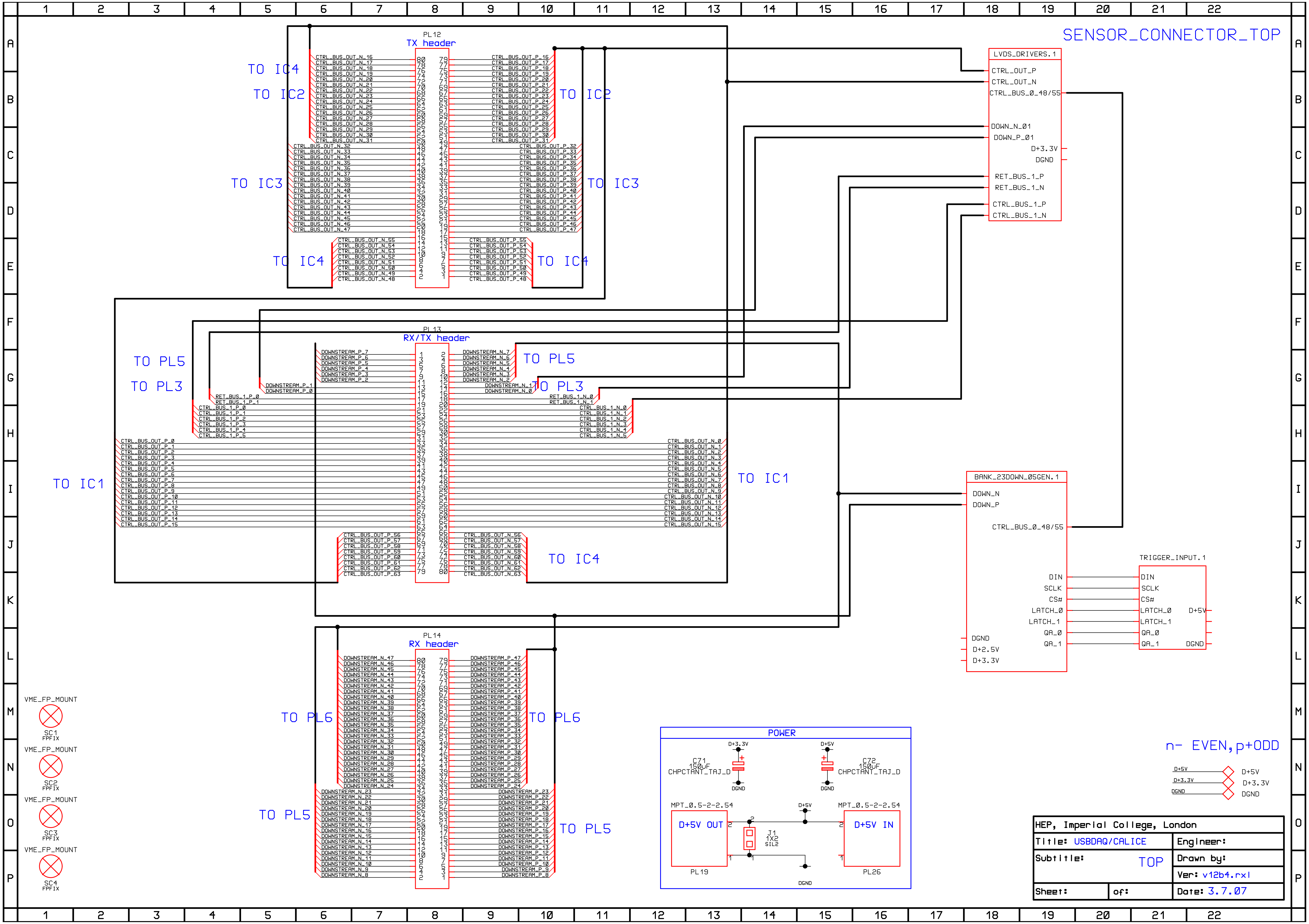
SENSOR_CONNECTOR_TOP



PL12
TX header
TO IC4
TO IC2
TO IC3
TO IC4
CTRL_BUS_OUT_N_16 … CTRL_BUS_OUT_N_31
CTRL_BUS_OUT_P_16 … CTRL_BUS_OUT_P_31
CTRL_BUS_OUT_N_32 … CTRL_BUS_OUT_N_47
CTRL_BUS_OUT_P_32 … CTRL_BUS_OUT_P_47
CTRL_BUS_OUT_N_48 … CTRL_BUS_OUT_N_55
CTRL_BUS_OUT_P_48 … CTRL_BUS_OUT_P_55
PL13
RX/TX header
TO PL5
TO PL3
TO IC1
DOWNSTREAM_P_0 … DOWNSTREAM_P_7
DOWNSTREAM_N_0 … DOWNSTREAM_N_7
RET_BUS_1_P_0
RET_BUS_1_P_1
RET_BUS_1_N_0
RET_BUS_1_N_1
CTRL_BUS_1_P_0 … CTRL_BUS_1_P_5
CTRL_BUS_1_N_0 … CTRL_BUS_1_N_5
CTRL_BUS_OUT_P_0 … CTRL_BUS_OUT_P_15
CTRL_BUS_OUT_N_0 … CTRL_BUS_OUT_N_15
CTRL_BUS_OUT_P_56 … CTRL_BUS_OUT_P_63
CTRL_BUS_OUT_N_56 … CTRL_BUS_OUT_N_63
PL14
RX header
TO PL6
TO PL5
DOWNSTREAM_N_8 … DOWNSTREAM_N_47
DOWNSTREAM_P_8 … DOWNSTREAM_P_47
LVDS_DRIVERS.1
CTRL_OUT_P
CTRL_OUT_N
CTRL_BUS_0_48/55
DOWN_N_01
DOWN_P_01
D+3.3V
DGND
RET_BUS_1_P
RET_BUS_1_N
CTRL_BUS_1_P
CTRL_BUS_1_N
BANK_23DOWN_05GEN.1
DOWN_N
DOWN_P
CTRL_BUS_0_48/55
DIN
SCLK
CS#
LATCH_0
LATCH_1
QA_0
QA_1
DGND
D+2.5V
D+3.3V
TRIGGER_INPUT.1
DIN
SCLK
CS#
LATCH_0
LATCH_1
QA_0
QA_1
D+5V
DGND
VME_FP_MOUNT
SC1
FPFIX
VME_FP_MOUNT
SC2
FPFIX
VME_FP_MOUNT
SC3
FPFIX
VME_FP_MOUNT
SC4
FPFIX
POWER
D+3.3V
D+5V
C71
150uF
CHPCTANT_TAJ_D
C72
150uF
CHPCTANT_TAJ_D
DGND
DGND
MPT_0.5-2-2.54
MPT_0.5-2-2.54
D+5V OUT
D+5V IN
D+5V
J1
1X2
SIL2
PL19
PL26
DGND
n- EVEN,p+ODD
D+5V
D+3.3V
DGND

HEP, Imperial College, London
Title: USBDAQ/CALICE
Engineer:
Subtitle: TOP
Drawn by:
Ver: v12b4.rxl
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Date: 3.7.07