CALICE ECAL Readout Electronics: VFE-PCB Interface Specification

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1 Introduction

The prototype calorimeter will consist of 30 layers of silicon diodes. Each layer comprises a 3×3 array of silicon diode wafers, each containing a 6×6 array of diodes. Each diode needs to be read out and so corresponds to a channel. Hence, each wafer contains 36 channels, each layer contains $36 \times 9 = 324$ channels and the whole prototype is $324 \times 30 = 9720$ channels.

The silicon wafers will be mounted onto one very-front-end card (VFE-PCB). Each VFE-PCB can hold up to 6 wafers in a 2×3 array. Each layer will therefore consist of one VFE-PCB fully-populated with 6 wafers and one VFE-PCB half-populated with 3 wafers in a 1×3 array. Because the VFE-PCBs will be physically mounted with their orientation alternating in each layer between top and bottom side facing forwards, then the 3 wafers in the half-populated VFE-PCB will be alternating between the two possible 1×3 arrays. Hence, there will be 3 different flavours of VFE-PCB; fully-populated, left half-populated and right half-populated. There are 60 VFE-PCB's in total, 30 fully-populated, 15 left half-populated and 15 right half-populated, with each layer containing one fully-populated and one half-populated VFE-PCB.

The wafers will be read out using VFE FLC_PHY2 chips, each reading 18 channels. Hence, there will be six or twelve VFE chips per VFE-PCB. The 18 channels are multiplexed onto a single output line per VFE chip. The VFE chip will also accept a calibration signal which is used to inject a pulse at the chip input.

The interface to the readout elecronics is the connector on the VFE-PCB which supplies the driving signals for the VFE-PCB and takes the output signals. The power for the VFE-PCB is supplied separately.

2 Signals

The readout electronics will have an independent ground from the VFE-PCB's. Hence, all signals on the PCB connector which provide the interface to the readout electronics are differential. The connector shield will be grounded at the VFE-PCB end (? Is this correct? Is it also grounded at the readout board end?).

Table 1 lists the numbers and types of signals to and from a fully-populated VFE-PCB. Notes:

1. All LVDS signals will have the standard +1.2 V quiescent level.
2. Each of the shift register output signals are the AND of those from six of the VFE chips on the VFE-PCB. For half-populated VFE-PCBs, only one of these output signals will be used.

Signal (Name)	I/O	Type	Specification	Number	Pins	Notes
Sample-and-hold (HOLD)	I	Digital	Bus LVDS	1	2	1
Shift register reset (RESET)	I	Digital	Bus LVDS	1	2	1
Shift register input (SRIN)	I	Digital	Bus LVDS	1	2	1
Shift register multiplex clock (CLOCK)	I	Digital	Bus LVDS	1	2	1
Shift register output (SROUTn)	O	Digital	(Bus?) LVDS	2?	4?	1,2
VFE-PCB identification (IDn?)	O	Digital	(Bus?) LVDS	6?	12?	1
Channel signal output (OUTPUTn)	O	Analogue	Diff. $0 \pm 1.25\,\mathrm{V}$	12	24	3,4,5
Calibration timing strobe (TCALIBn)	I	Digital	Bus LVDS	2	4	1,6
Calibration group select (ENABLEn)	I	Digital	Bus LVDS	6	12	1,6
Calibration signal level (VCALIB)	I	Analogue	Diff. $0 \pm 1.25\,\mathrm{V}$	1	2	7
Total				33?	66?	

Table 1: Signals to ("I") and from ("O") the VFE-PCB. NEEDS CHECK ON SROUT AND ID VALUE.

3. The range of the channel signal output depends on the termination. The above $\pm 1.25\,\mathrm{V}$ range assumes $100\,\Omega$ termination within the readout electronics.

4. The twelve channel signal outputs each correspond to the output of one VFE ship. For half-populated VFE-PCBs, only six of these channel signal outputs will be used.

5. The channel signal output must be digitised with a 10 bit signal range, but with 4 bits precision at the low end, rising to 10 bits precision at the high end. Hence, 14 bits dynamic range, 10 bits precision is needed.

6. The calibration group select value sets which group of channels to calibrate. The 18 channels per VFE chip are divided into six groups of three channels each. These six groups can be selected bitwise; the same group is tested simultaneously on all VFE chips. The two calibration timing strobe signals allow a selection of the two banks of VFE chips corresponding to half-populated boards.

7. The same calibration voltage is used for all VFE chips on the board. The calibration signal level dynamic range and precision must be at least at good as that for the channel signal output.

3 Timing

The time-dependent signals are shown in Fig. 1; the calibration group select lines, calibration signal level lines and VFE-PCB identification lines are constant during data capture and transfer.

Notes:

1. The calibration timing strobe is only present if calibrating.

2. The timing between the start of the sequence (given by the rising edge of the trigger input) or, if calibrating, the rising edge of the calibration timing strobe, to the sample-and-hold must be accurately adjustable to $\leq$ 10ns.

3. The shift register input must overlap with the first shift register clock. It should go down before the first ADC channel is sampled.

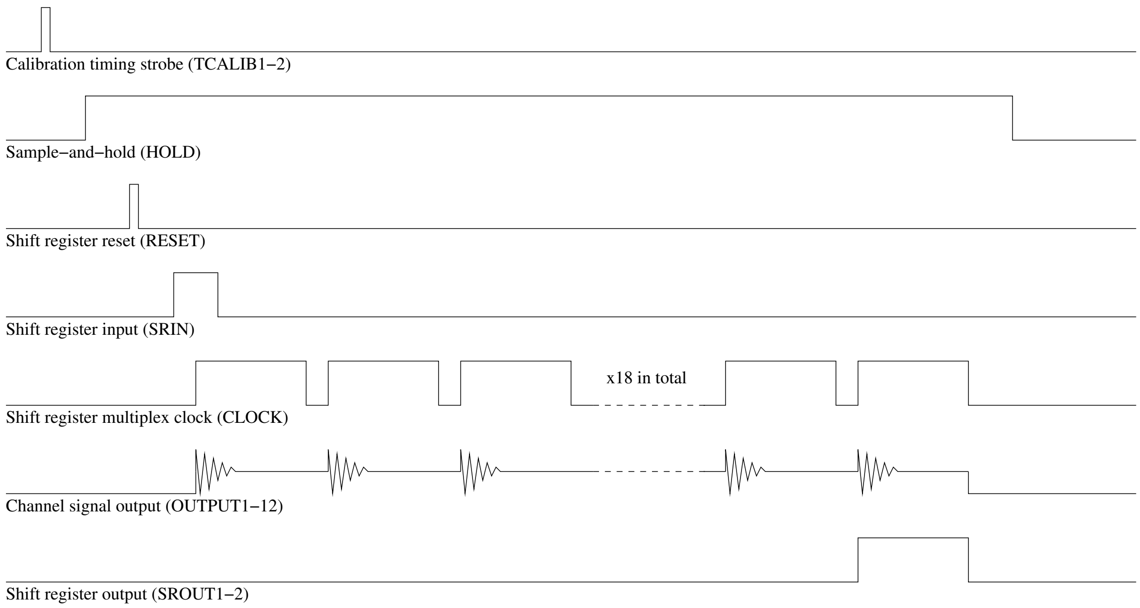

Figure 1: Time-dependent signals to and from the VFE-PCB. The calibration group select, signal level and board identification signals are constant throughout this sequence and so are not shown.

4. The shift register clock speed must be $\leq$ 5MHz.

4 Connectors and cables

The physical thickness of the VFE-PCB and connector cannot exceed 8mm due to space contraints. The connector will be the same 68-pin SCSI as will be used at the readout electronics end.

Each readout board will handle up to eight cables of fully-populated VFE-PCBs, i.e. $8 \times 12 \times 18 = 1728$ channels. There will be 16 connectors per board in 8 pairs. Each pair can be used for one fully-populated VFE-PCB cable or two half-populated VFE-PCB cables, one left-handed and one right-handed.

The cable should be twisted pair and around 2m long. There are no radiation-hard requirements but the cable should meet CERN/DESY specifications for safety.

Table 2 lists the signals on the VFE-PCB connector for the three types of VFE-PCB.

Connector Pair	VFE-PCB Signal		
	Fully-populated	Left Half-populated	Right Half-populated
35,1	OUTPUT1+,−	OUTPUT1+,−	Floating????
36,2	OUTPUT7+,−	Floating????	OUTPUT7+,−
37,3	Floating	Floating	Floating
38,4	OUTPUT2+,−	OUTPUT2+,−	Floating????
39,5	OUTPUT8+,−	Floating????	OUTPUT8+,−
40,6	HOLD+,−	HOLD+,−	HOLD+,−
41,7	VCALIB+,−	VCALIB+,−	VCALIB+,−
42,8	SRIN+,−	SRIN+,−	SRIN+,−
43,9	RESET+,−	RESET+,−	RESET+,−
44,10	ENABLE1+,−	ENABLE1+,−	ENABLE1+,−
45,11	ENABLE2+,−	ENABLE2+,−	ENABLE2+,−
46,12	ENABLE3+,−	ENABLE3+,−	ENABLE3+,−
47,13	CLOCK+,−	CLOCK+,−	CLOCK+,−
48,14	OUTPUT3+,−	OUTPUT3+,−	Floating????
49,15	OUTPUT9+,−	Floating????	OUTPUT9+,−
50,16	ENABLE4+,−	ENABLE4+,−	ENABLE4+,−
51,17	ENABLE5+,−	ENABLE5+,−	ENABLE5+,−
52,18	ENABLE6+,−	ENABLE6+,−	ENABLE6+,−
53,19	Floating	Floating	Floating
54,20	OUTPUT4+,−	OUTPUT4+,−	Floating????
55,21	OUTPUT10+,−	Floating????	OUTPUT10+,−
56,22	Floating	Floating	Floating
57,23	Floating	Floating	Floating
58,24	Floating	Floating	Floating
59,25	TCALIB1+,−	TCALIB1+,−	Floating????
60,26	TCALIB2+,−	Floating????	TCALIB2+,−
61,27	Floating	Floating	Floating
62,28	Floating	Floating	Floating
63,29	Floating	Floating	Floating
64,30	OUTPUT5+,−	OUTPUT5+,−	Floating????
65,31	OUTPUT11+,−	Floating????	OUTPUT11+,−
66,32	Floating	Floating	Floating
67,33	OUTPUT6+,−	OUTPUT6+,−	Floating????
68,34	OUTPUT12+,−	Floating????	OUTPUT12+,−

Table 2: Signals on VFE-PCB connector. NEEDS SROUT AND BOAD ID ADDED.