CALICE ECAL Readout Electronics: Project Specification

November 19, 2002

1 Introduction

The CALICE collaboration plans to test a prototype tungsten-silicon electromagnetic calorimeter (ECAL) with a beam in 2004/5. The prototype will have around 10000 channels and the UK hopes to provide the readout electronics and data acquisition for this experiment. There will also be a hadronic calorimeter (HCAL) prototype and, although the UK is not funding any electronics, it would be useful if the ECAL readout electronics could also be used for the HCAL. In this case, the non-UK groups involved would pay for the extra boards needed.

The prototype calorimeter will consist of 30 layers of silicon diodes. Each layer comprises a 3×3 array of silicon diode wafers and the three silicon wafers in a row in each layer will be mounted on PCB's which route the diode signals to the very front end (VFE) chips which provide amplification and shaping. Each layer therefore consists of three such VFE-PCB's.

The system will be triggered using external logic based on fast scintillator detectors in the beam line. This trigger will be supplied to the readout electronics via lemo cables, presumably at NIM levels.

The diodes, VFE chips, VFE-PCB's and their power supplies, as well as the beam trigger and its logic, will be provide by non-UK groups, while the UK will need to provide all the readout electronics downstream and the data acquisition (DAQ) system to read it out. All signals from each VFE-PCB are assumed to be routed through a single connector. This will provide the well-defined interface between the two parts of the electronics. The UK will provide any cables needed from this connector.

2 Overview of proposed readout system

An overview of the proposed ECAL system is shown in Fig. 1. The system has the cables from the VFE-PCB's connecting directly to 9U VME boards, with all the necessary readout electronics on these boards. The system could run in several modes: triggered, with readout for each event before allowing the next trigger to occur; semi-buffered, where only minimal verification information is read out for each event; and fully buffered where events are accumulated with no intervention before readout. The trigger would be controlled by one of the readout boards which would also distribute the trigger across the backplane. No data reduction is done in hardware, so all 9720 channels are read out for each trigger.

The basic unit of the readout is based on the 90 VFE-PCB's. These each hold 108 channels which are multiplexed onto 6 lines. Each 9U board can take 16 input connectors, so this gives 6 readout boards, each handling the signals from 16 VFE-PCB's.

A further board may be required for testing the readout boards during the prototype and production phases. This test board will send and receive the signals to and from a single readout board using the same cables as the VFE-PCBs.

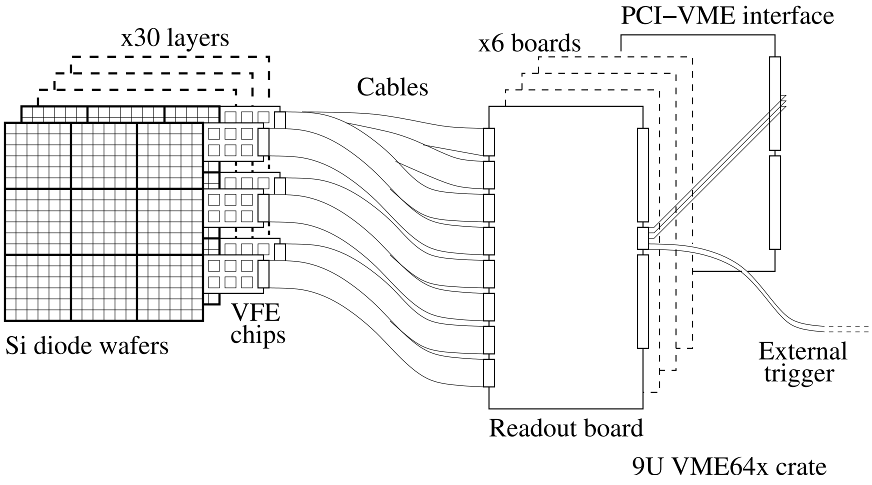

Figure 1: Overview of the proposed ECAL readout system.

3 Cost

We assume that we will build 2 prototypes of the readout boards and for production, we need 6 readout boards plus 3 spares. The test board will be produced during prototyping and no production of this is needed. A simple NIM-LVDS converter board for the trigger signals is also needed.

In addition to the purpose built boards, the system also needs commercially available infrastructure, namely, a PCI/VME interface card, a high-end PC, some disk storage and a VME crate and power supplies.

All the following prices include VAT. A VME-PCI8026 PCI/VME interface card set, including a 2m cable, is quoted by National Instruments at £3889. Note, we may use an SBS VME-PCI fibre channel, Model 618, as this can have the PC outside the radiation area; the cost is assumed to be similar. A dual Pentium-IV, 2 GHz, 2 Gbytes memory PC, with screen and keyboard, is quoted by Compusys at £3680. For disk, a 1.4 Tbytes array spread over 12 IDE disks with RAID 5 redundancy and a SCSI interface, recently bought by the UCL group, was £8k. CMS have VME64x crates available for £5600.

Therefore, an estimated costing of the readout electronics is:

- Non-recurring design costs; for all electronics = £5k.
- Readout boards; £6100 per board $\times$ 11 boards = £67k.
- Test board; £1000 per board = £1k.
- NIM-LVDS board; £1000 per board = £1k.
- Cables; £150 per cable $\times$ 100 cables = £15k.
- PC and disk; £4k for the PC, £8k for 1.4 Tbytes of disk = £12k.
- VME interfaces; £4k for PCI-VME interface = £4k.
- 9U VME64x crate and power supplies; £6k per crate = £6k.

All values given are in FY02/03 prices and include VAT, so the total cost of the equipment for the project is therefore FY02/03 £111k.

4 Schedule

Task	Date of completion
Readout electronics CDR	October 2002
Prototype readout board design completed	January 2003
Readout electronics PDR	February 2003
Prototype readout board layout completed	March 2003
Prototype readout board fabrication completed	April 2003
Prototype readout board and prototype VFE-PCB tests	July 2003
Prototype readout board testing completed	September 2003
Production readout board redesign completed	October 2003
Readout electronics FDR	November 2003
Production readout board layout completed	November 2003
Production readout board fabrication completed	December 2003
Production readout board testing completed	March 2004

Table 1: Schedule for the readout electronics.

Table 1 shows the schedule for the readout electronics. The system needs to be ready for a beam test in mid 2004. It therefore needs to be completed by the end of March 2004. Fabrication, testing and data acquisition software development of the full system is likely to require around 6 months, which sets the end of the readout board prototype phase to be September 2003. Therefore, the time to January 2003 will be used to complete the specification and design of the readout boards. Full specification prototype fabrication of these will take place by April 2003 and prototype testing will take place over summer 2003.

Hence, prototype costs will be incurred in FY02/03 and FY03/04, while all production costs will be incurred in FY03/04. The prototype costs in FY02/03 will be for half the NRE (£2k), the PC (£4k), the VME crate (£6k) and components for the two prototype readout boards (£7k) giving a total of £19k in FY02/03. The remaining infrastructure and board production costs, totalling FY02/03 £92k, will all be incurred in FY03/04.

5 Effort

The readout electronics is estimated to require around 37 months of engineering effort in total. We estimate that 30 months of engineering effort will be required for the design of the readout board; this breaks down as 15 months for the FE FPGA, 6 months for the data handling part of the BE FPGA, 6 months for the trigger part of the BE FPGA and 3 months for the FE component schematics. In addition, 3 months total will be needed for layout and fabrication of the two rounds of the readout board and 2 months for JTAG testing of the board. The final 2 months is for the design and layout of the test board and NIM-LVDS converter board.

There is a total of 18 months engineering effort available within the Universities over FY02/03 and FY03/04; 3 months from Manchester (Dave Mercer), 10 months from Imperial (Dave Price and Osman Zorba) and 5 months from UCL (Martin Postranecky and Matt Warren). Currently, Manchester are working on the data handling part of the BE FPGA, Imperial on the FE FPGA and UCL on the trigger part of the BE FPGA. UCL will design the test and NIM-LVDS boards and they will be laid out at Imperial.

Assuming the project is approved in December 2002, then effort from RAL ID would be required to complete the system. They have used 1 month in preparations for the proposal. The project engineer will work full-time for the remaining 4 months of FY02/03 and for 10 months in FY03/04. It is clear that this engineer would need to cover all aspects of the project as all are short of effort at present. Some rearrangement of tasks between groups might also be useful at this stage. Additional technical effort of 2 months from the RAL drawing office for the layout and fabrication in FY02/03 and 1 month in FY03/04 would also be needed. There will also be 1 month of JTAG preparation and tests in FY02/03 and 1 month in FY03/04. This gives a total of 20 months of RAL ID effort.

Test software for the boards will mainly be provided by the University groups.