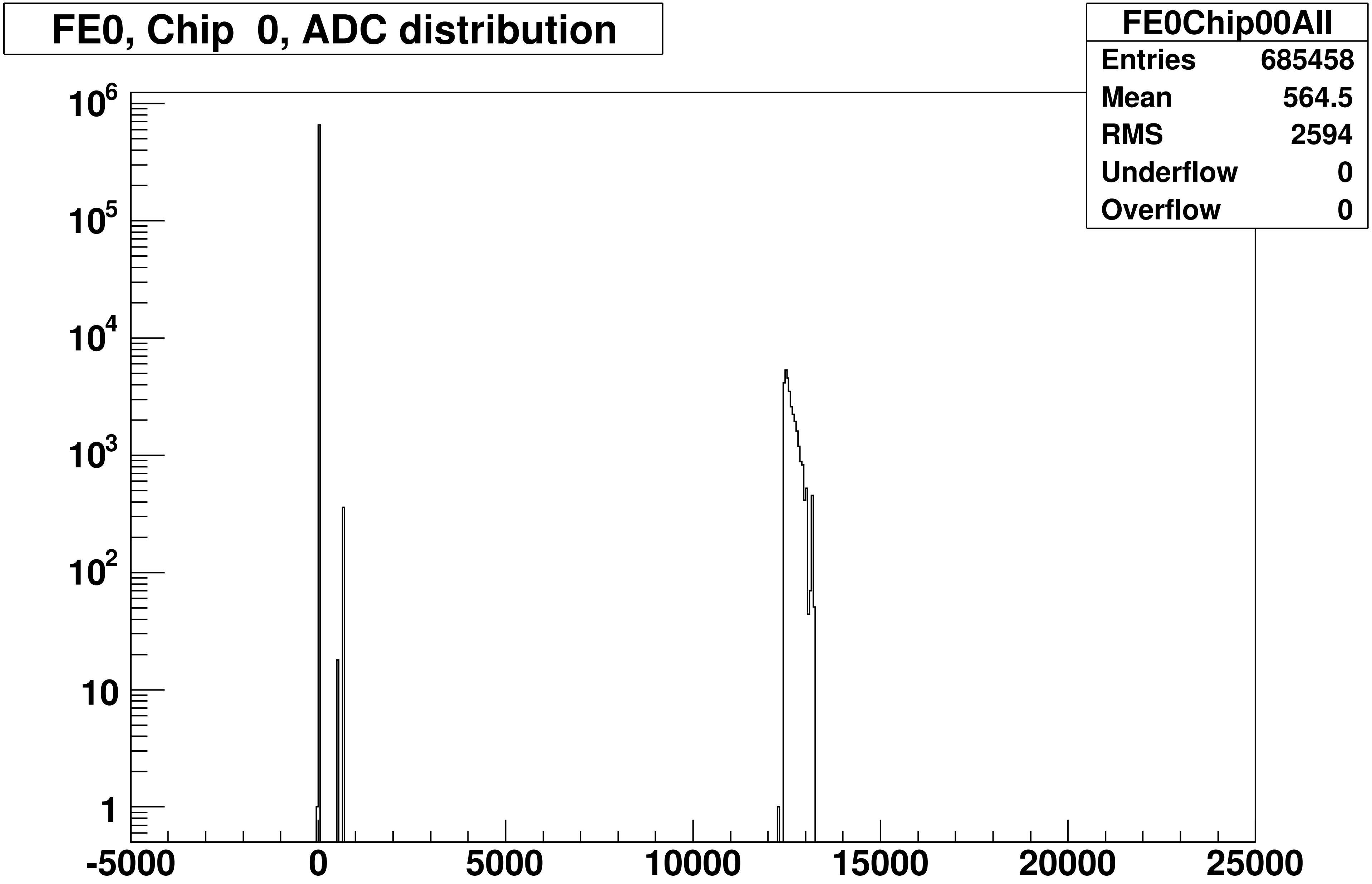
FE0, Chip 0, ADC distribution
FE0Chip00All
Entries 685458
Mean 564.5
RMS 2594
Underflow 0
Overflow 0
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10^3
10^2
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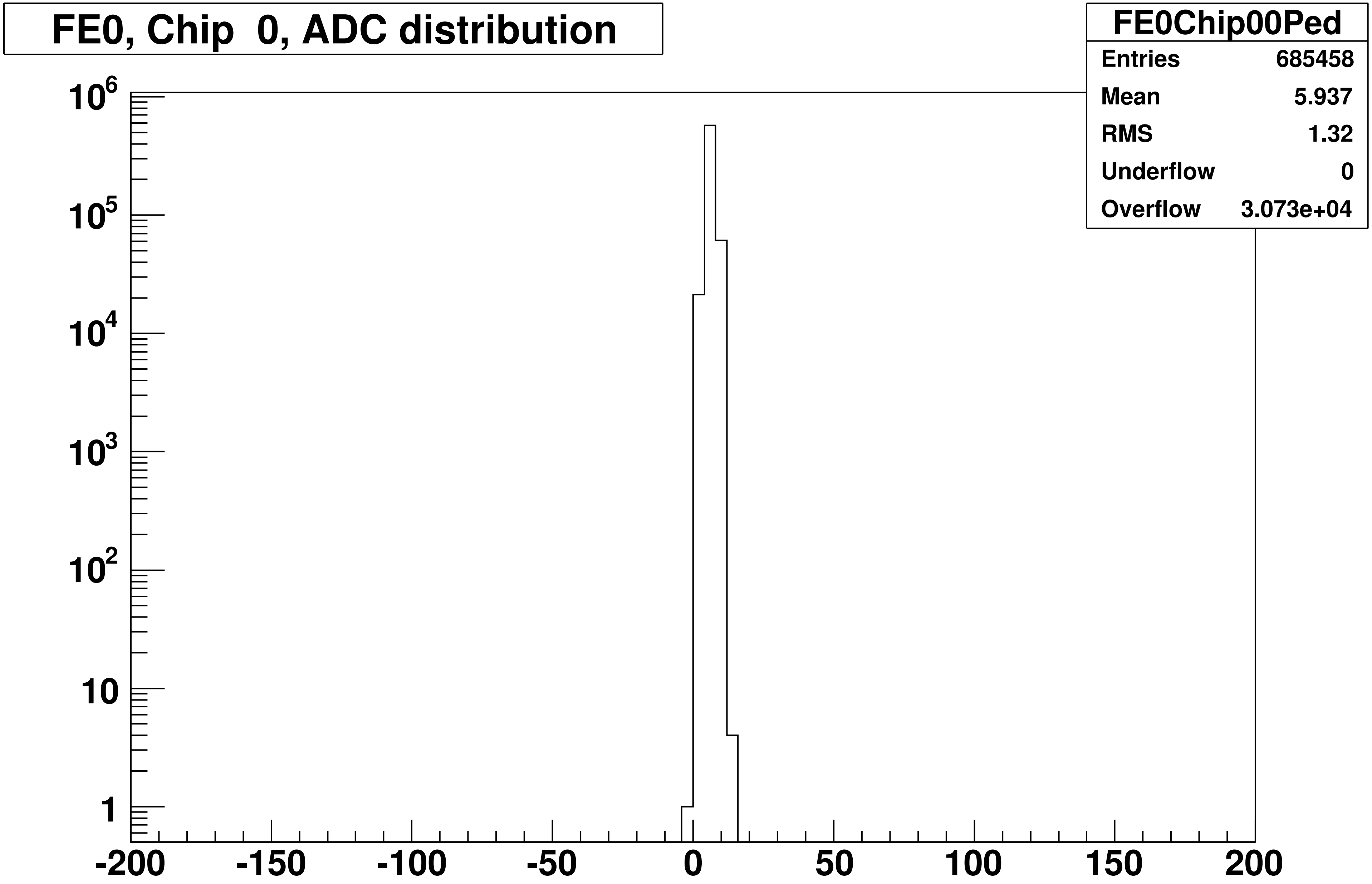

FE0, Chip 0, ADC distribution
FE0Chip00Ped
Entries 685458
Mean 5.937
RMS 1.32
Underflow 0
Overflow 3.073e+04
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10^3
10^2
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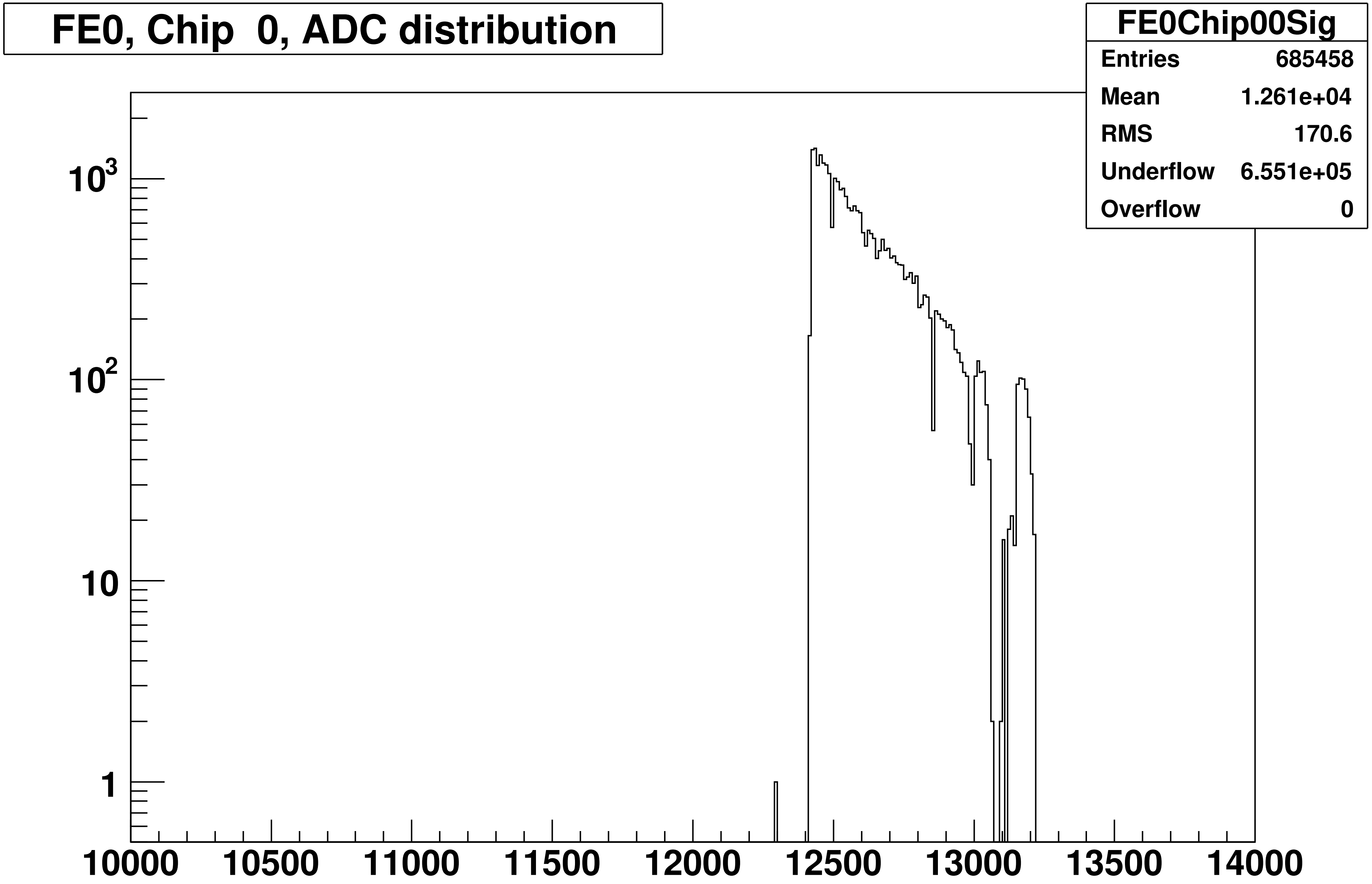
150
200



FE0, Chip 0, ADC distribution
FE0Chip00Sig
Entries 685458
Mean 1.261e+04
RMS 170.6
Underflow 6.551e+05
Overflow 0
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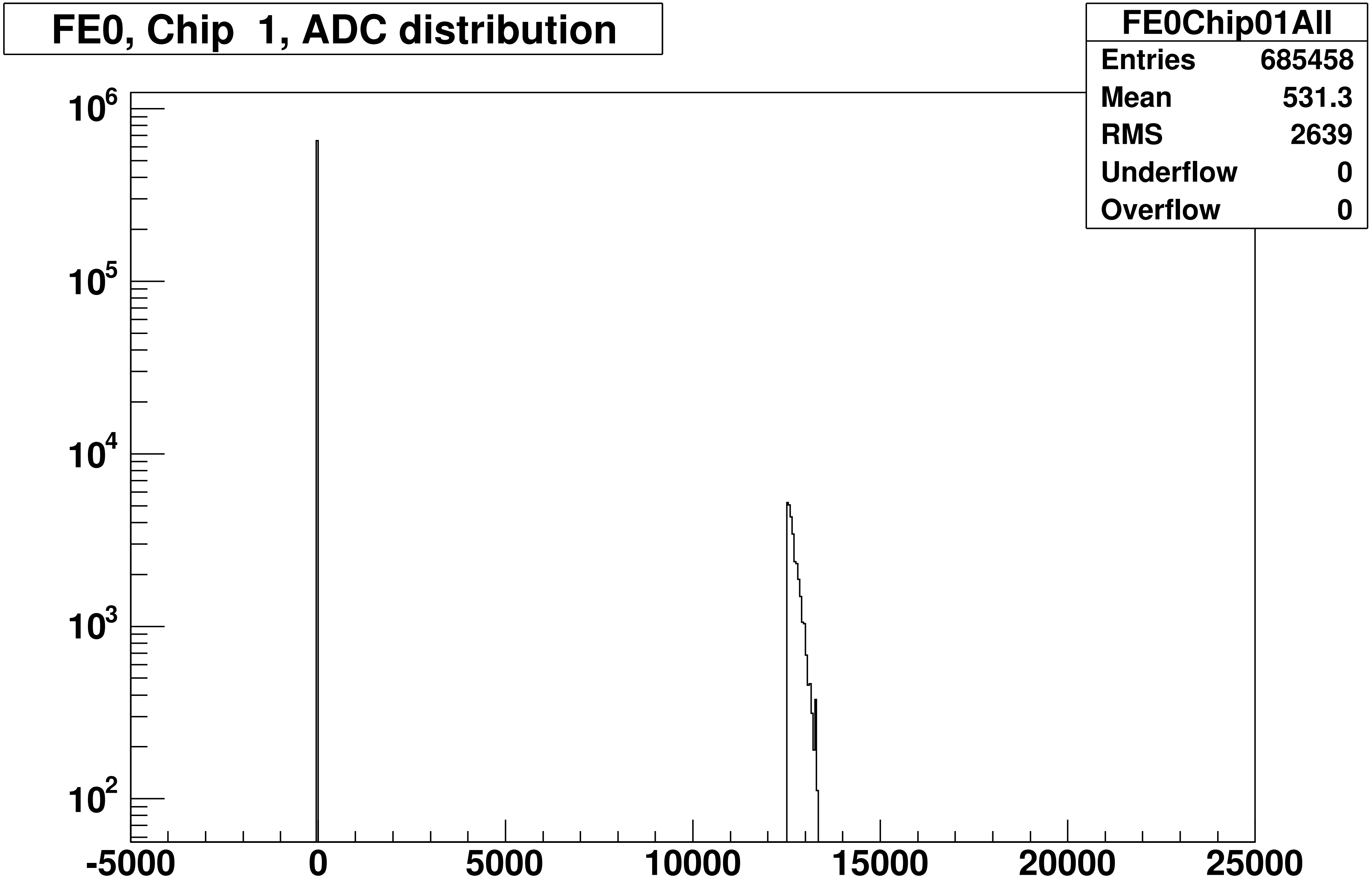
FE0, Chip 1, ADC distribution
FE0Chip01All
Entries 685458
Mean 531.3
RMS 2639
Underflow 0
Overflow 0
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10^4
10^3
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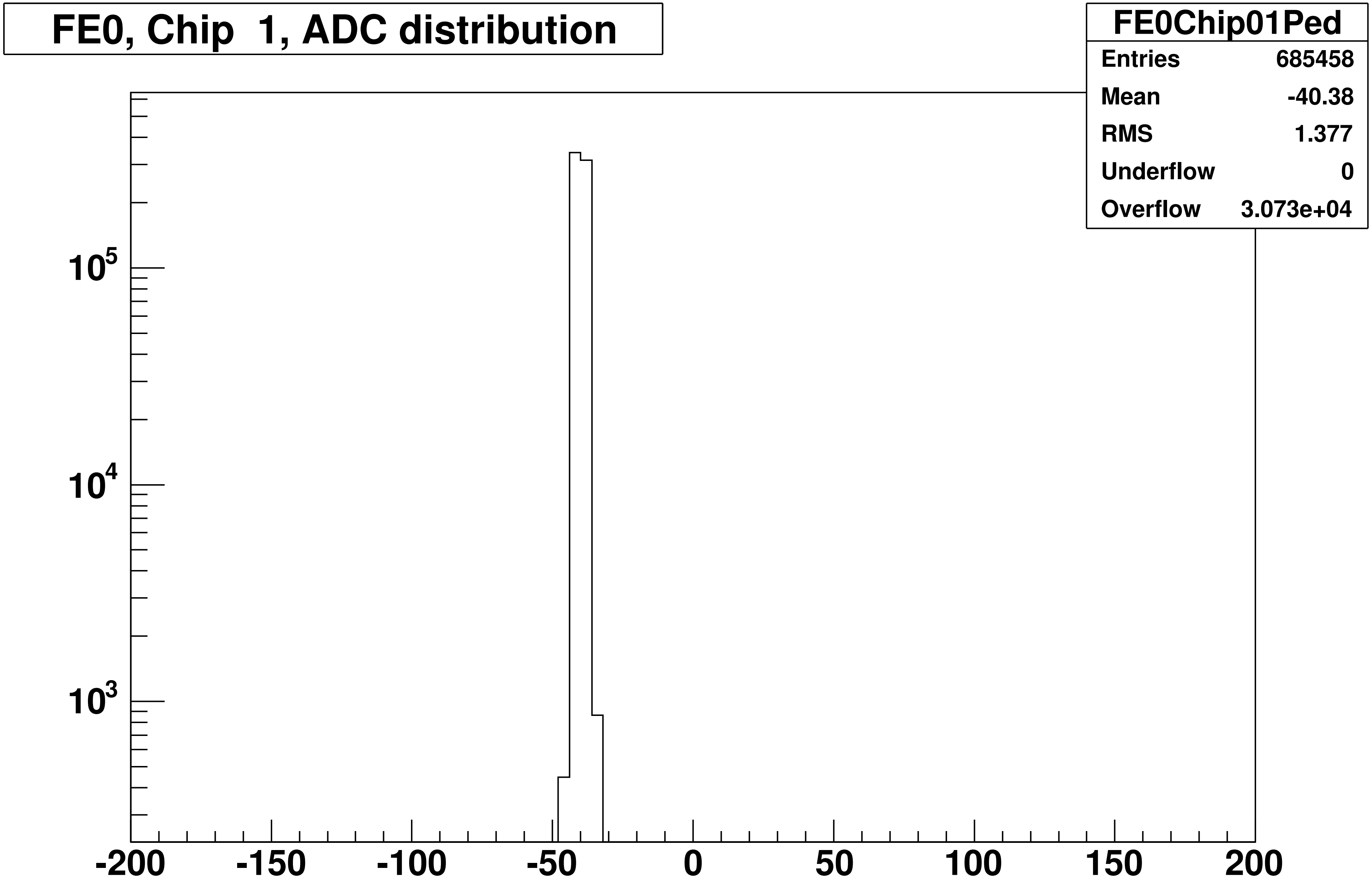
FE0, Chip 1, ADC distribution
FE0Chip01Ped
Entries 685458
Mean -40.38
RMS 1.377
Underflow 0
Overflow 3.073e+04
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10^4
10^3
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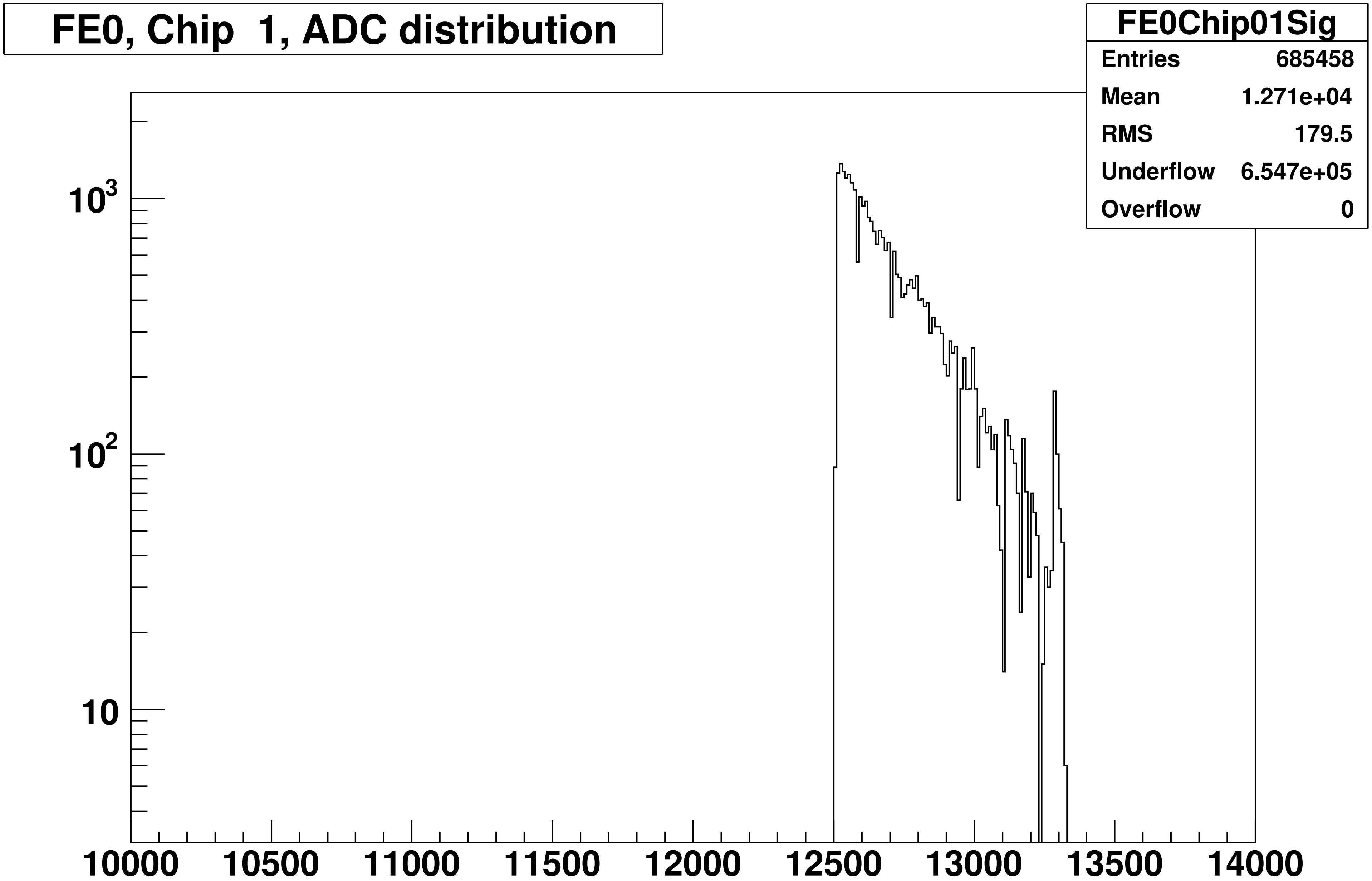

FE0, Chip 1, ADC distribution
FE0Chip01Sig
Entries 685458
Mean 1.271e+04
RMS 179.5
Underflow 6.547e+05
Overflow 0
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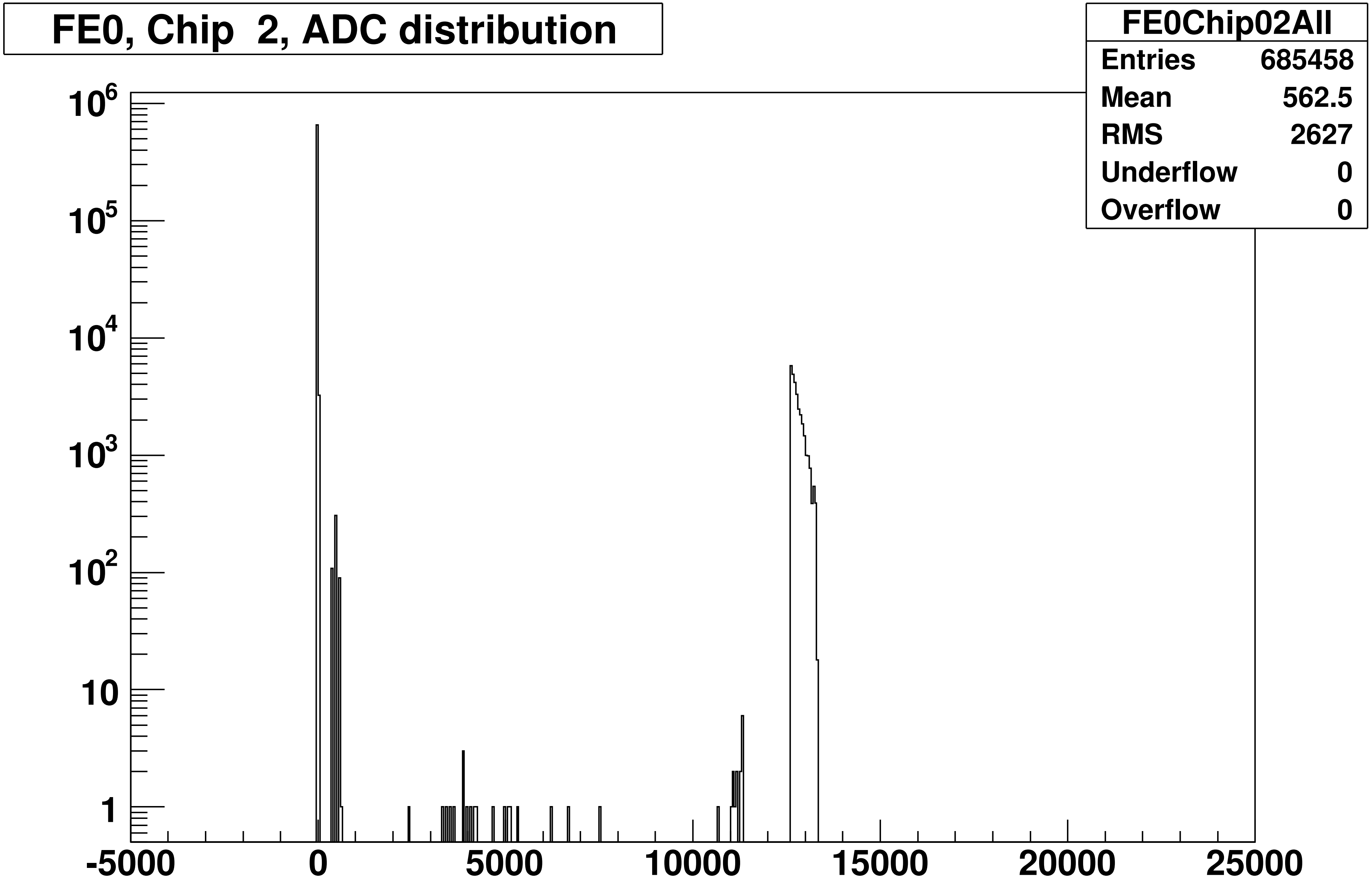
FE0, Chip 2, ADC distribution
FE0Chip02All
Entries 685458
Mean 562.5
RMS 2627
Underflow 0
Overflow 0
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10^4
10^3
10^2
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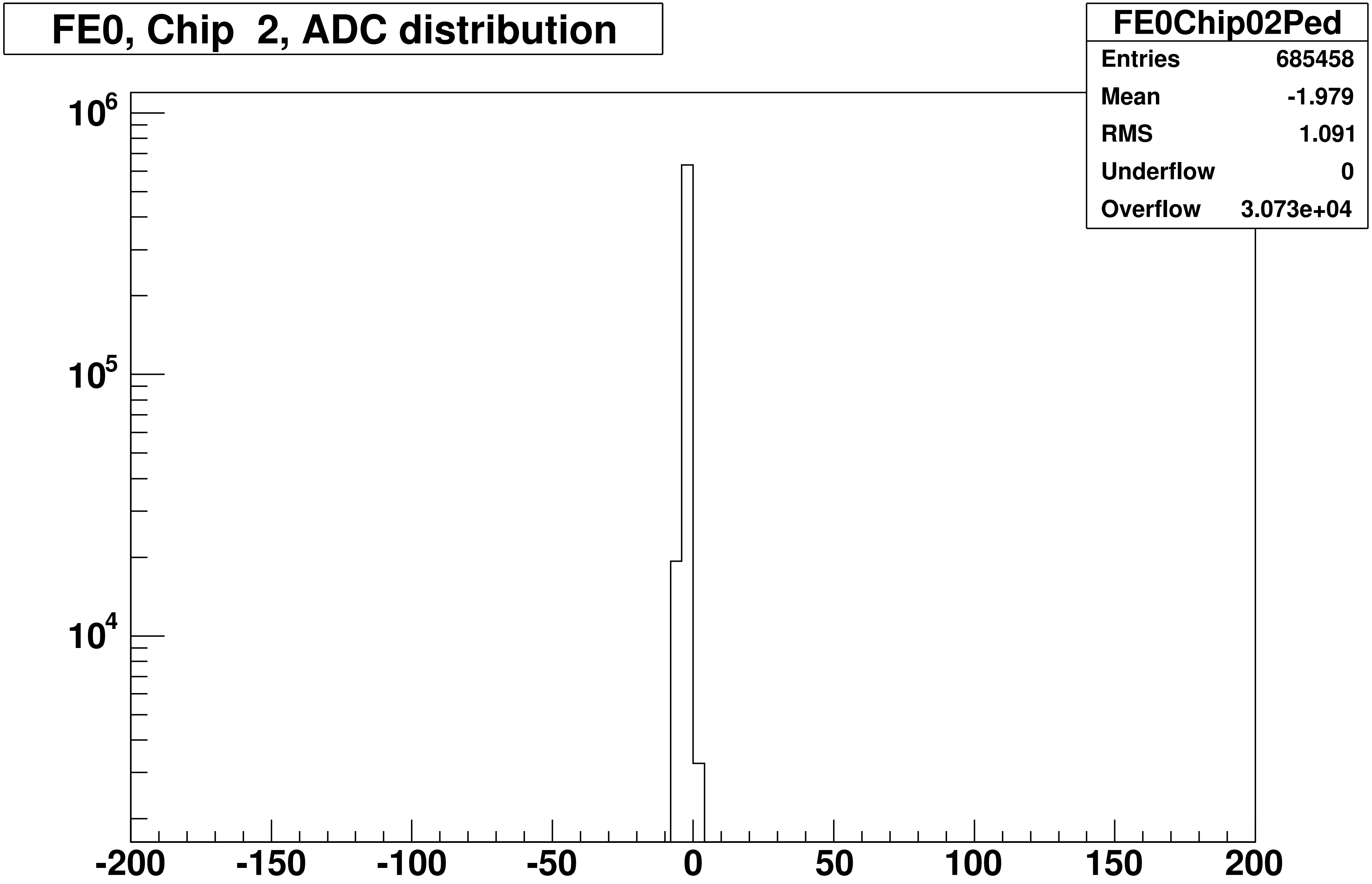
FE0, Chip 2, ADC distribution
FE0Chip02Ped
Entries 685458
Mean -1.979
RMS 1.091
Underflow 0
Overflow 3.073e+04
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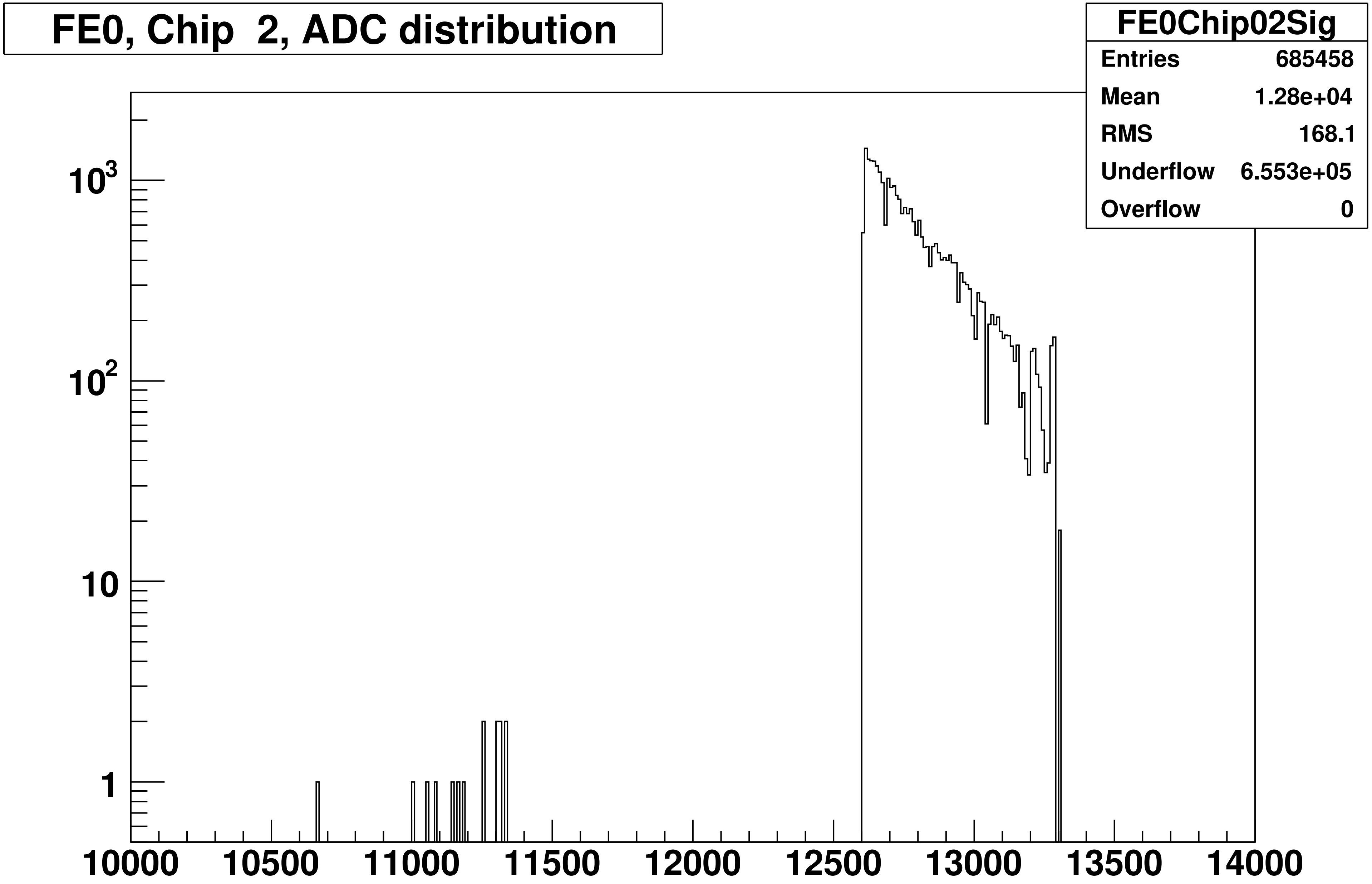
FE0, Chip 2, ADC distribution
FE0Chip02Sig
Entries 685458
Mean 1.28e+04
RMS 168.1
Underflow 6.553e+05
Overflow 0
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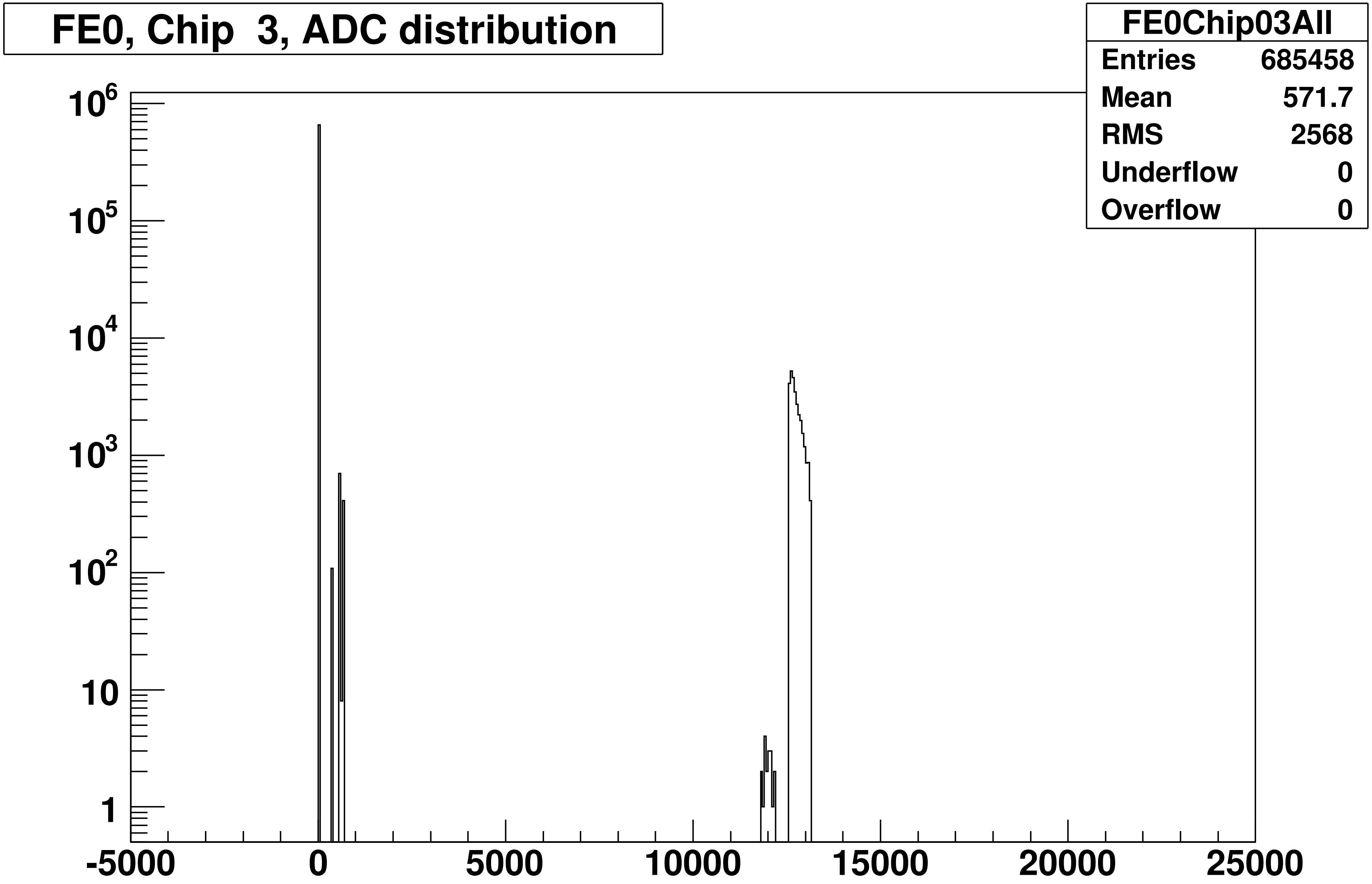
FE0, Chip 3, ADC distribution
FE0Chip03All
Entries 685458
Mean 571.7
RMS 2568
Underflow 0
Overflow 0
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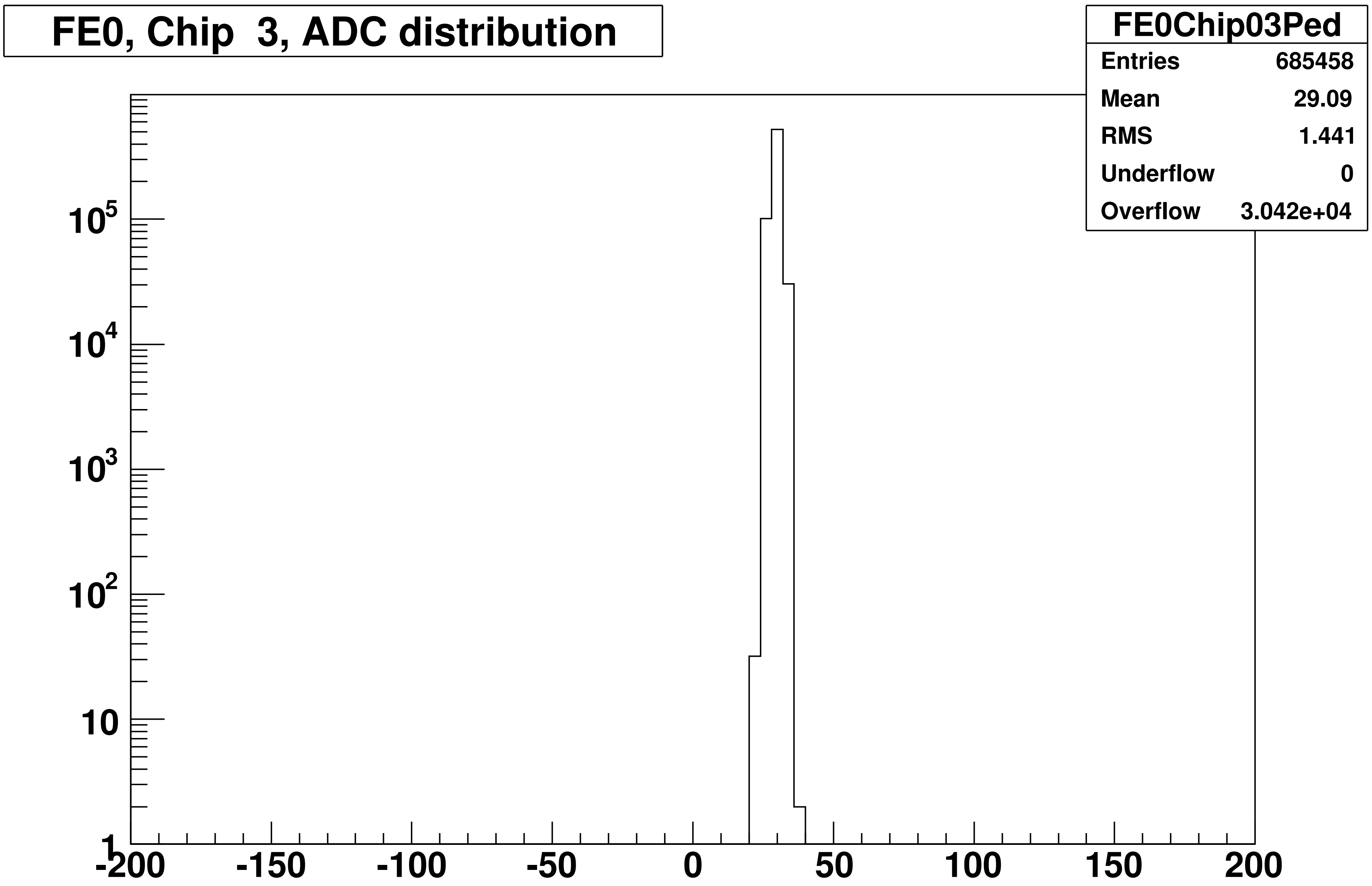
FE0, Chip 3, ADC distribution
FE0Chip03Ped
Entries 685458
Mean 29.09
RMS 1.441
Underflow 0
Overflow 3.042e+04
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10^3
10^2
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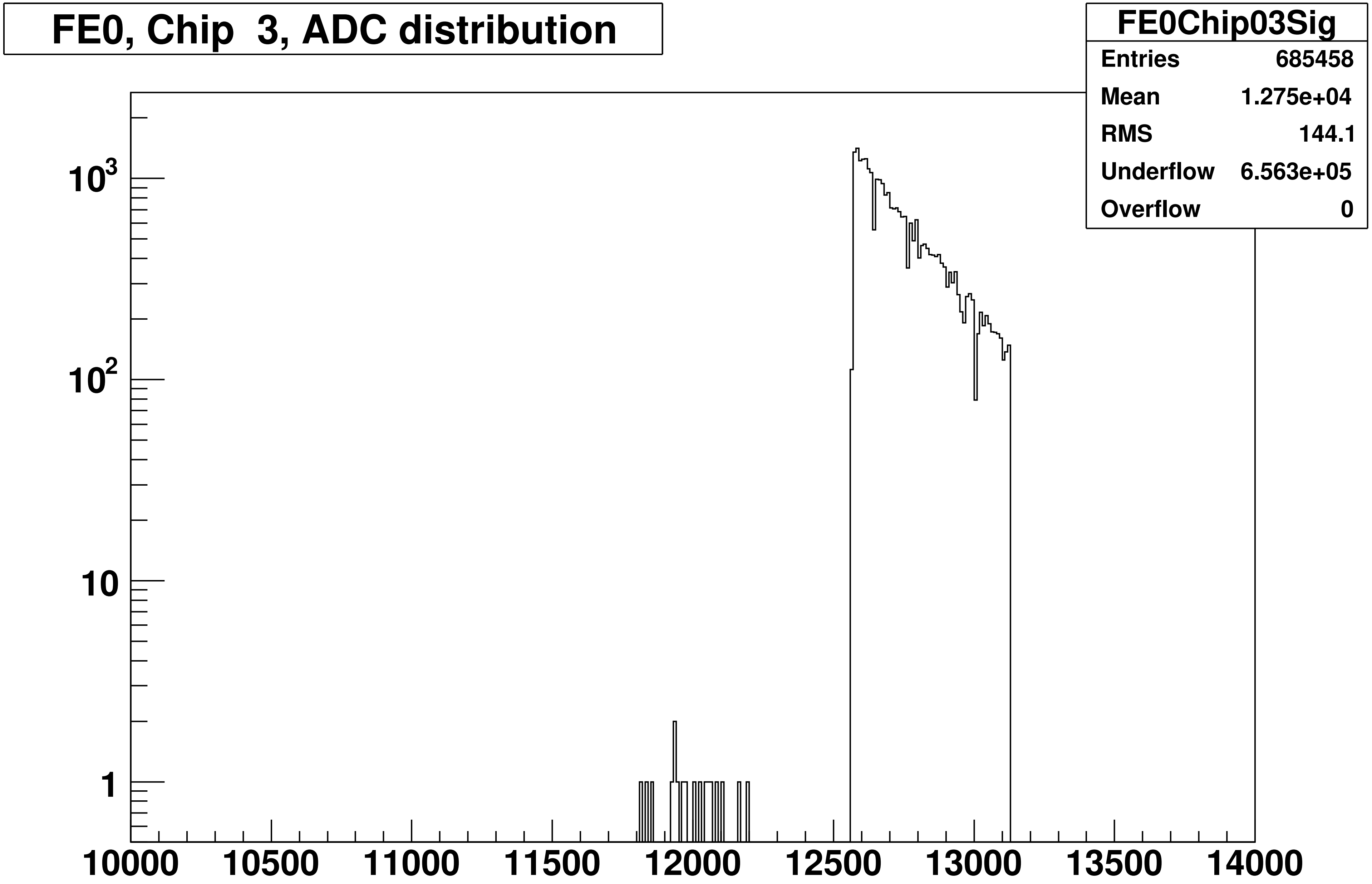

FE0, Chip 3, ADC distribution
FE0Chip03Sig
Entries 685458
Mean 1.275e+04
RMS 144.1
Underflow 6.563e+05
Overflow 0
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10^2
10
1
10000
10500
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11500
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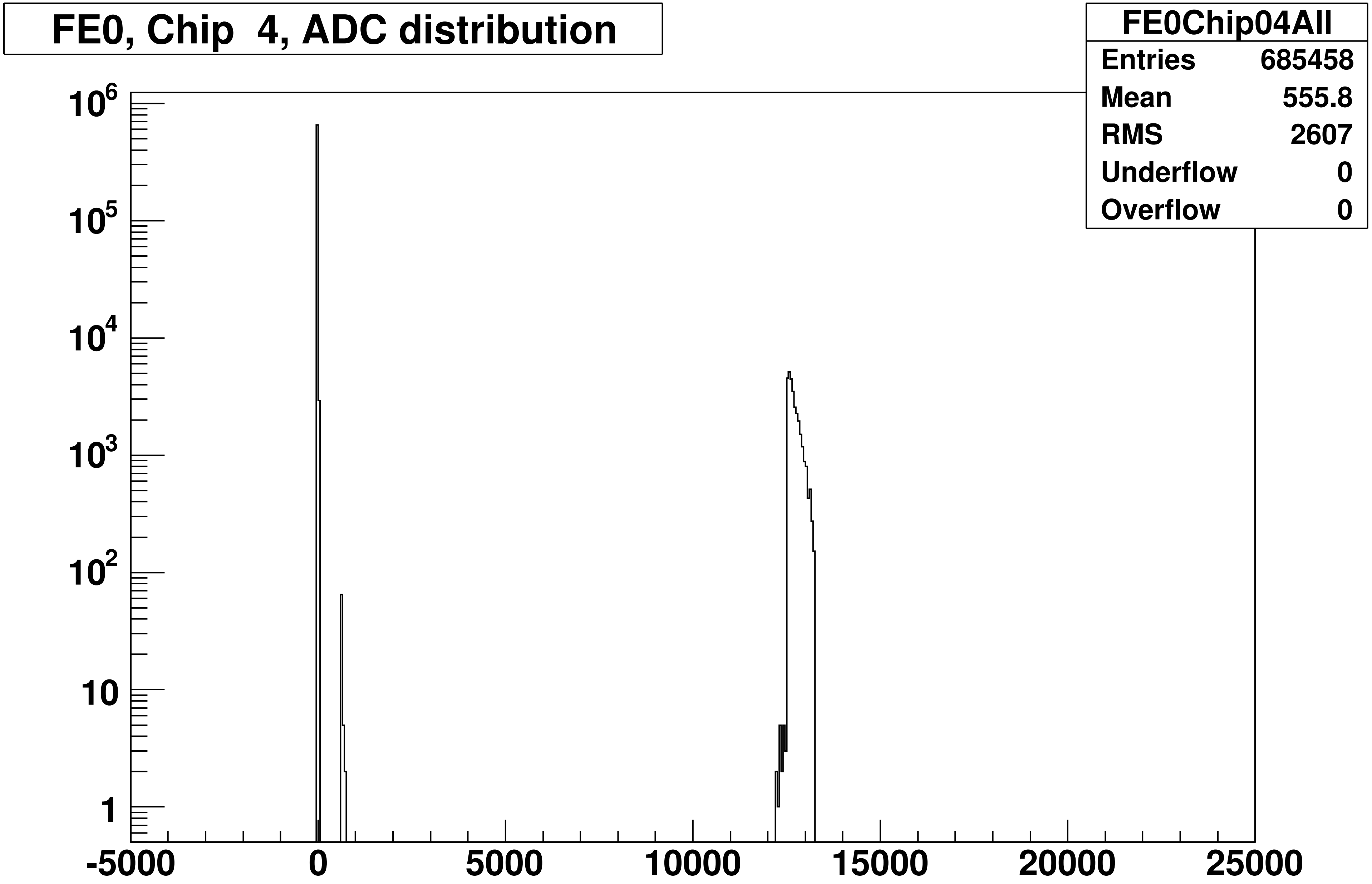
FE0, Chip 4, ADC distribution
FE0Chip04All
Entries 685458
Mean 555.8
RMS 2607
Underflow 0
Overflow 0
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10^4
10^3
10^2
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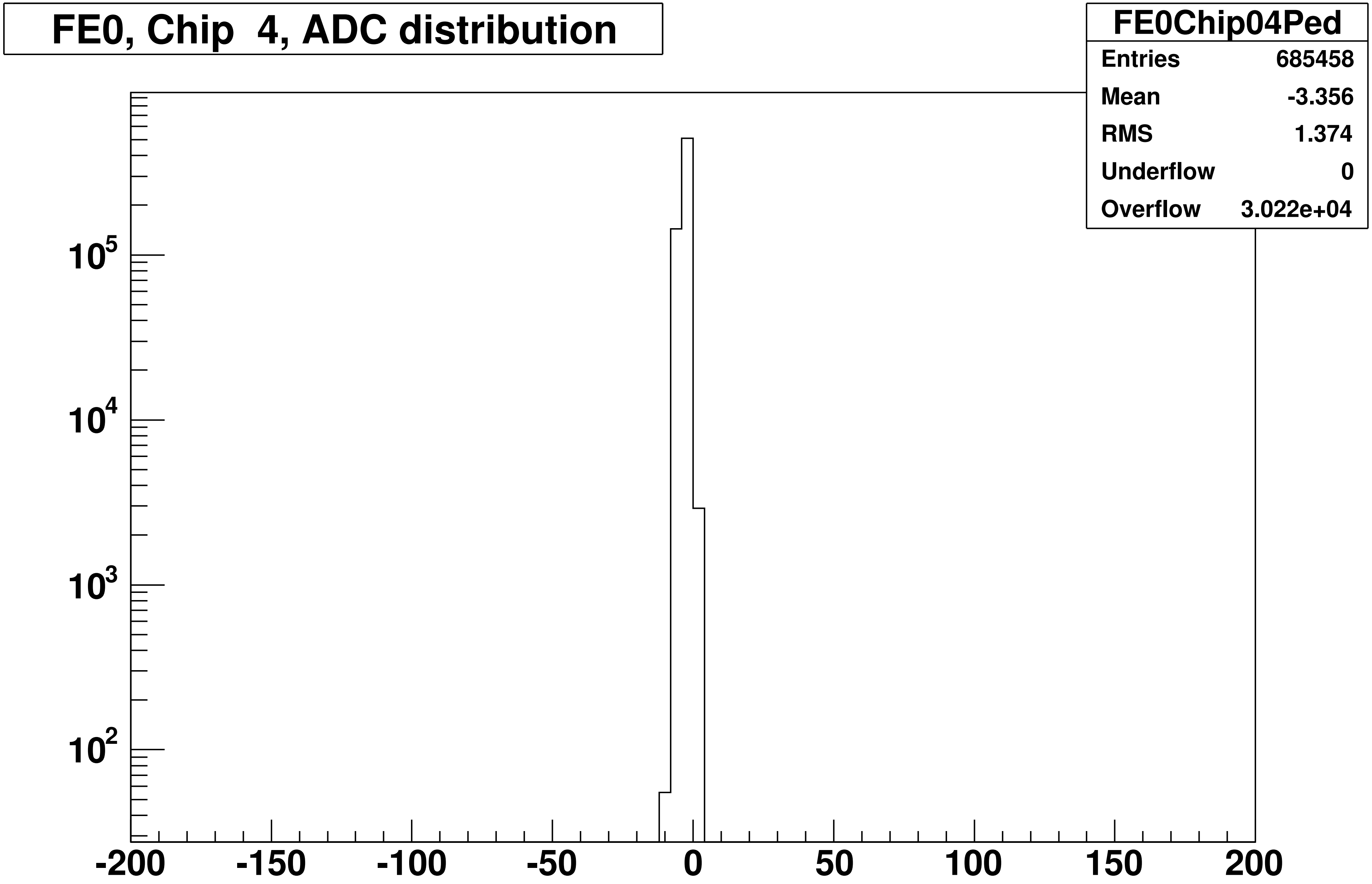
FE0, Chip 4, ADC distribution
FE0Chip04Ped
Entries 685458
Mean -3.356
RMS 1.374
Underflow 0
Overflow 3.022e+04
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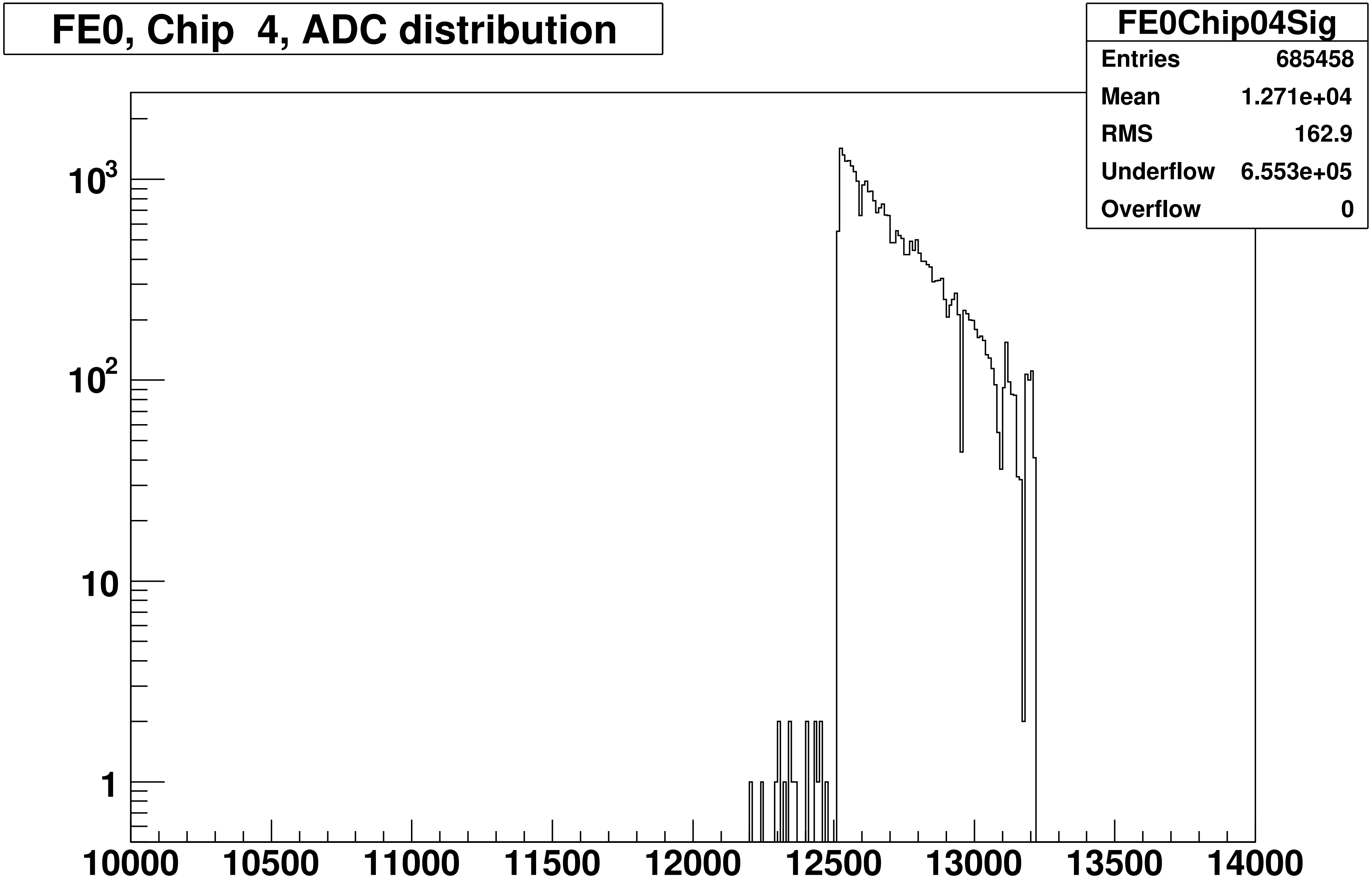

FE0, Chip 4, ADC distribution
FE0Chip04Sig
Entries 685458
Mean 1.271e+04
RMS 162.9
Underflow 6.553e+05
Overflow 0
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10^2
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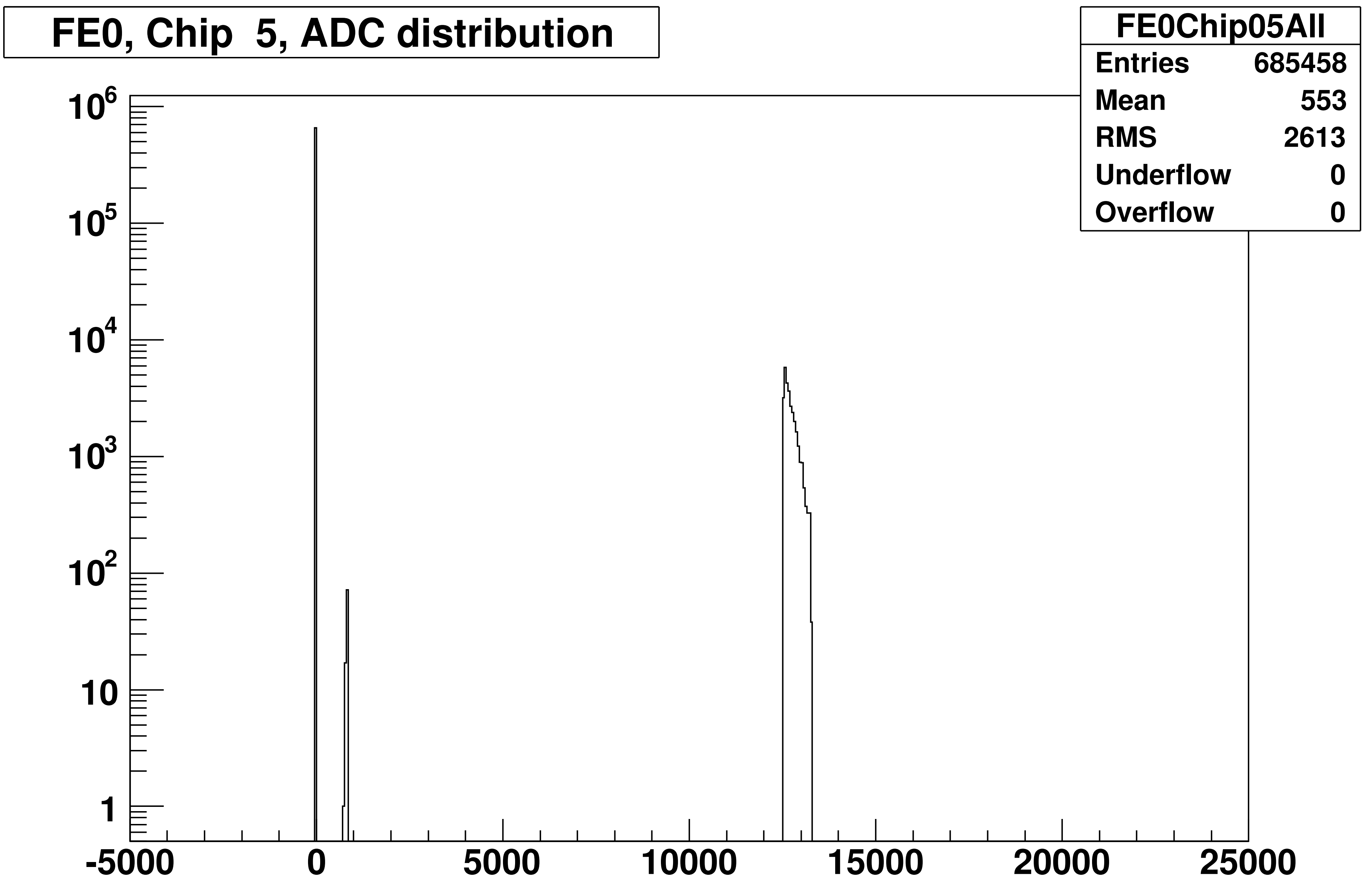
FE0, Chip 5, ADC distribution
FE0Chip05All
Entries 685458
Mean 553
RMS 2613
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
1
-5000
0
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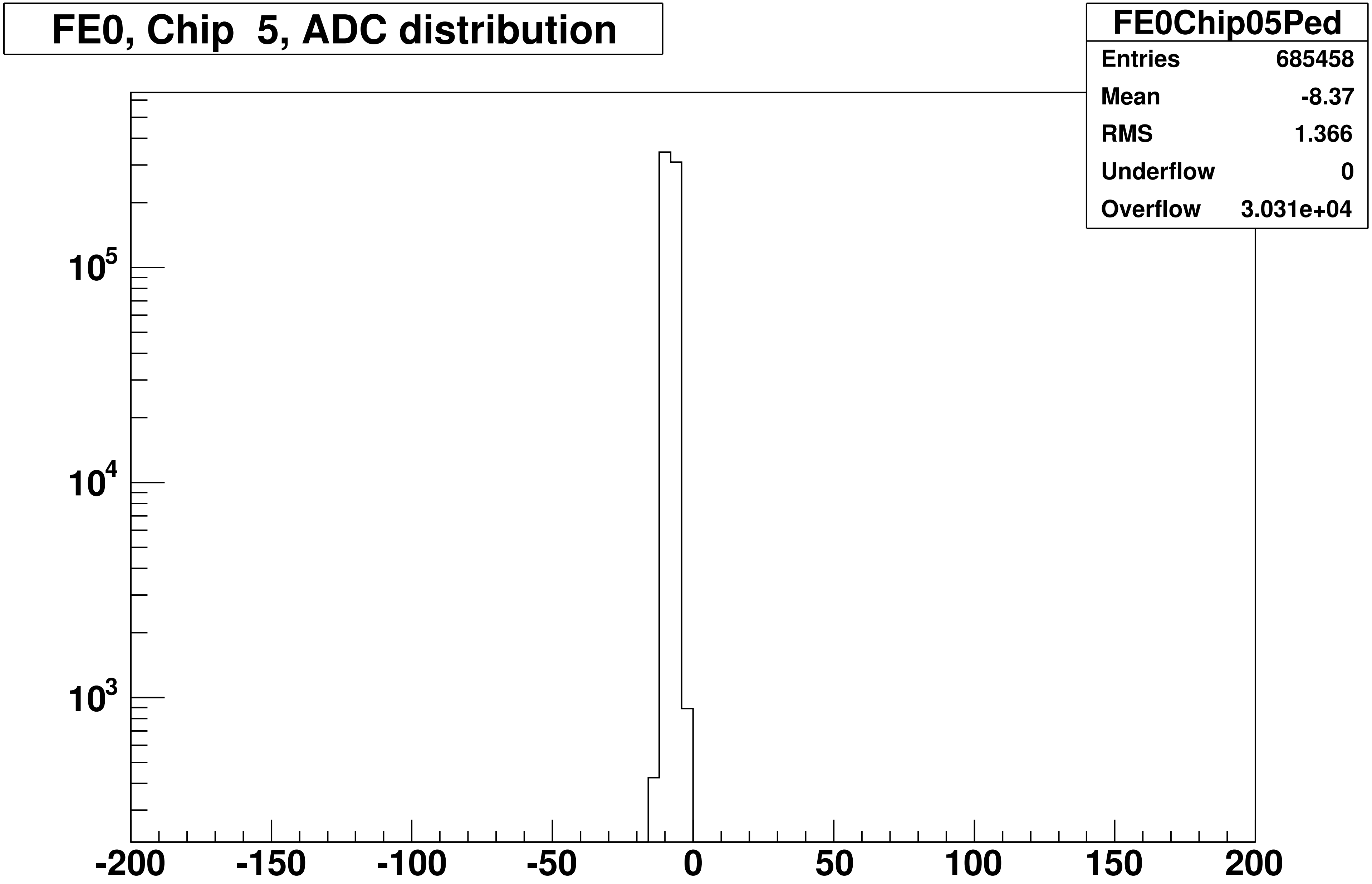
FE0, Chip 5, ADC distribution
FE0Chip05Ped
Entries 685458
Mean -8.37
RMS 1.366
Underflow 0
Overflow 3.031e+04
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10^4
10^3
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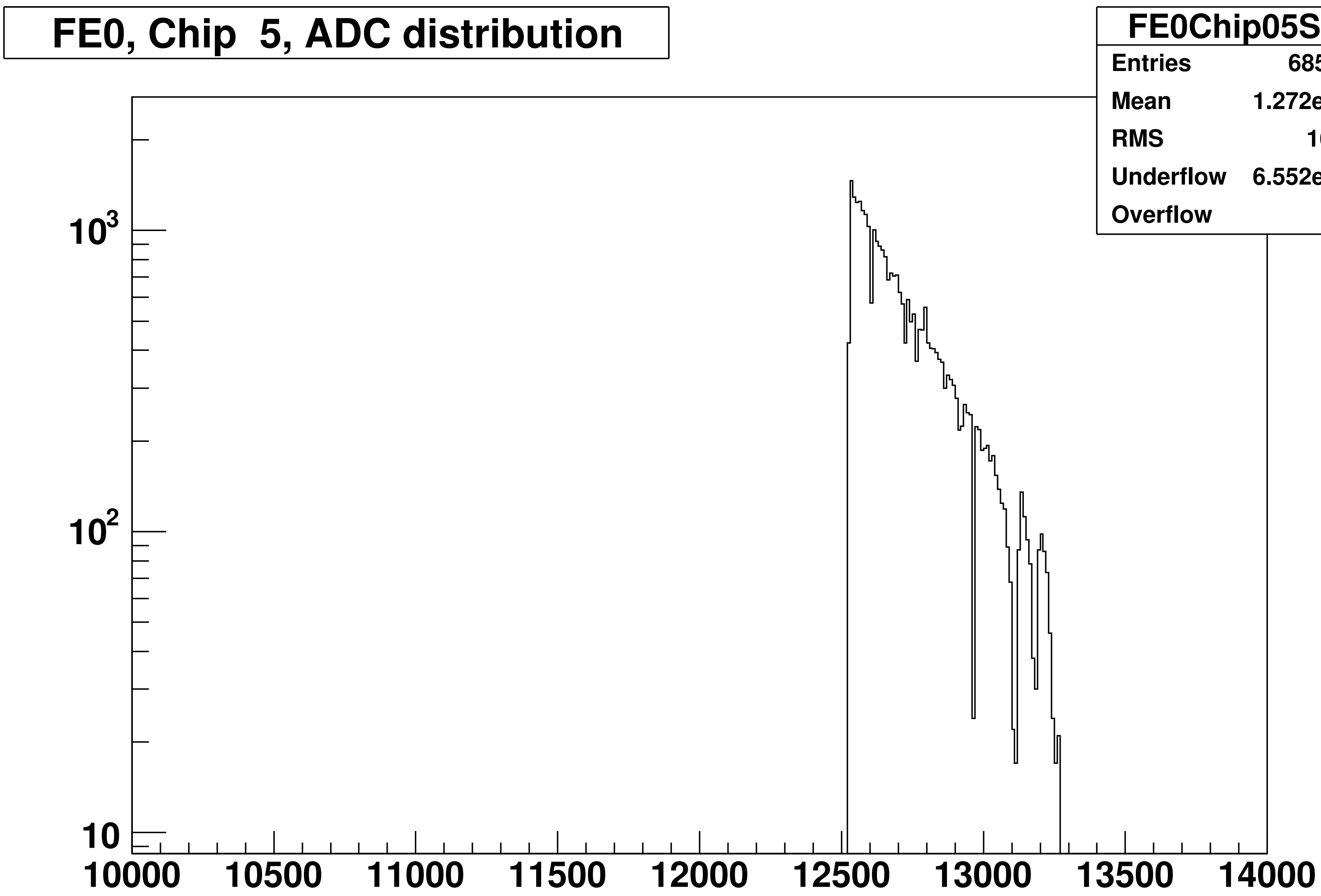

FE0, Chip 5, ADC distribution
FE0Chip05Sig
Entries 685458
Mean 1.272e+04
RMS 165.7
Underflow 6.552e+05
Overflow 0
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10^2
10
10000
10500
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11500
12000
12500
13000
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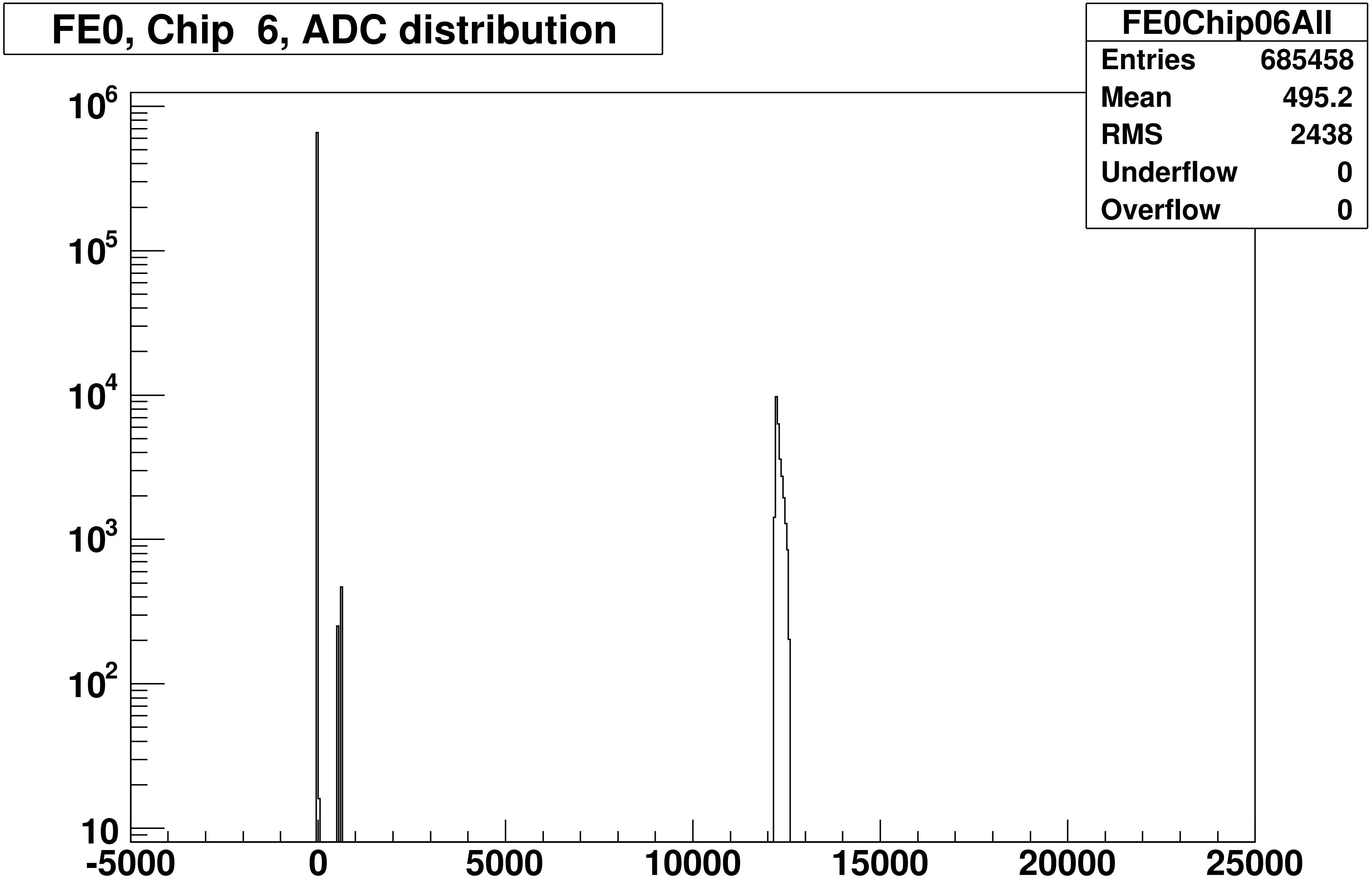
FE0, Chip 6, ADC distribution
FE0Chip06All
Entries 685458
Mean 495.2
RMS 2438
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
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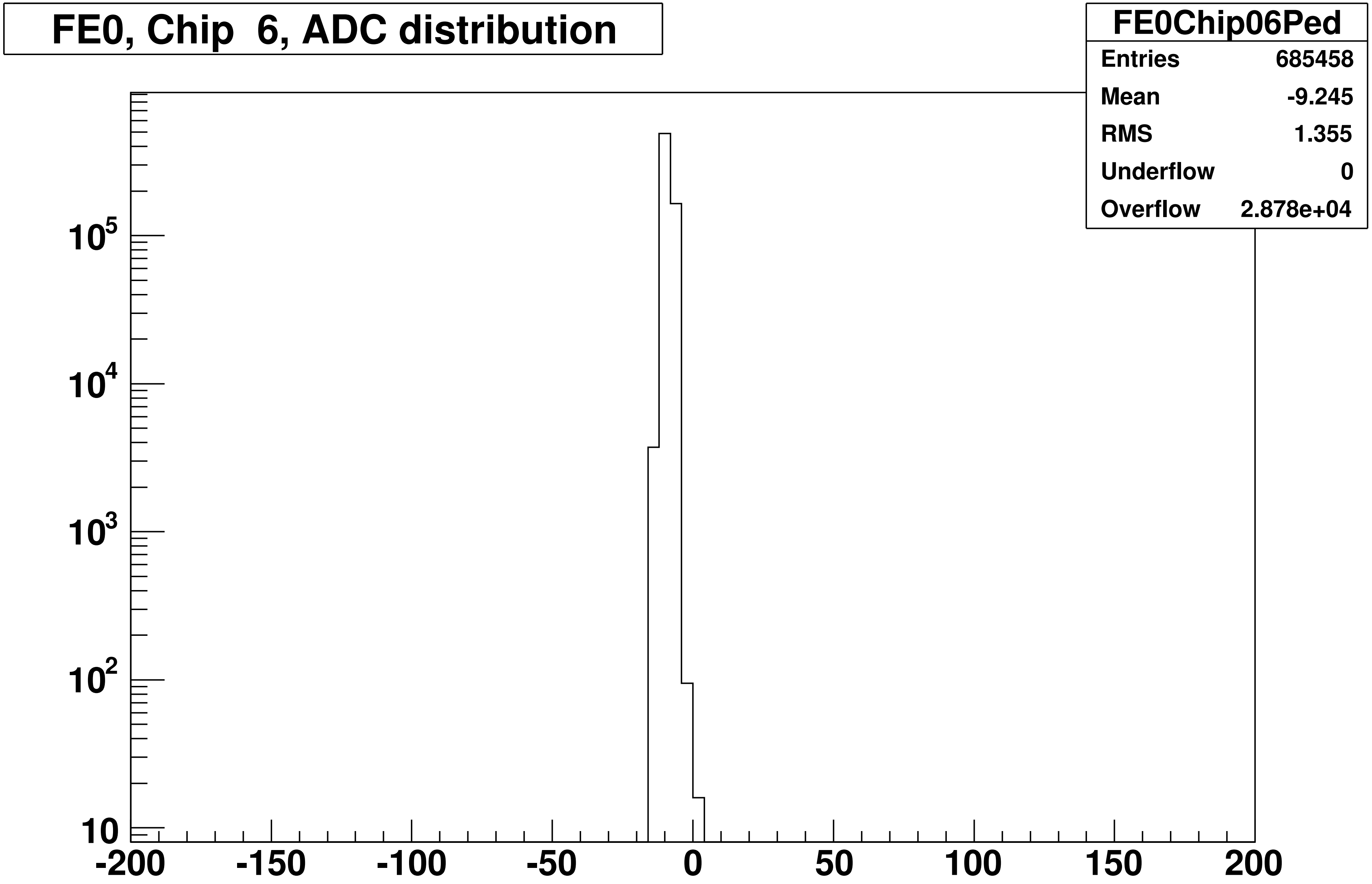
-5000
0
5000
10000
15000
20000
25000


FE0, Chip 6, ADC distribution
FE0Chip06Ped
Entries 685458
Mean -9.245
RMS 1.355
Underflow 0
Overflow 2.878e+04
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10^4
10^5
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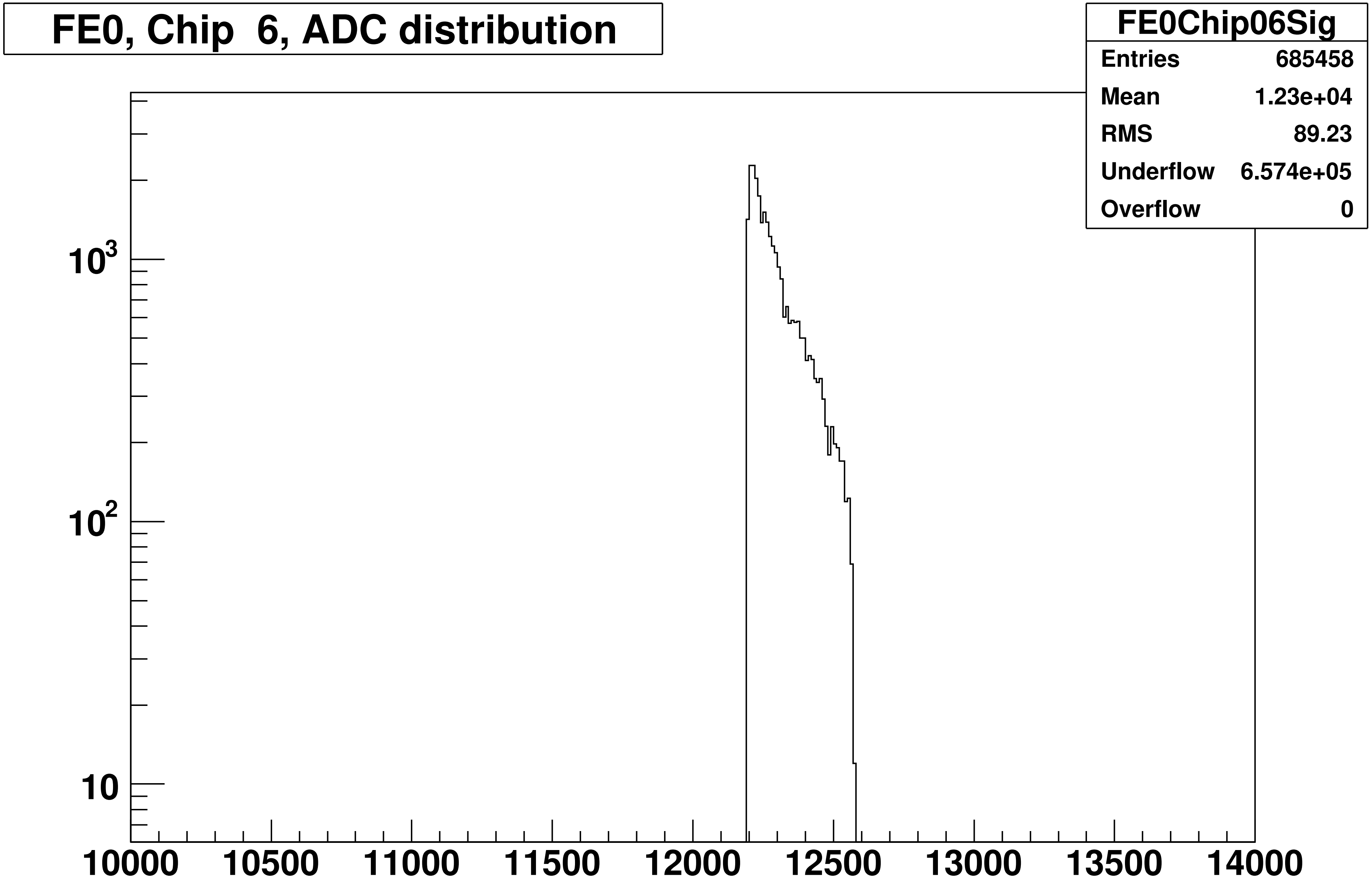
150
200


FE0, Chip 6, ADC distribution
FE0Chip06Sig
Entries 685458
Mean 1.23e+04
RMS 89.23
Underflow 6.574e+05
Overflow 0
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10^2
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11500
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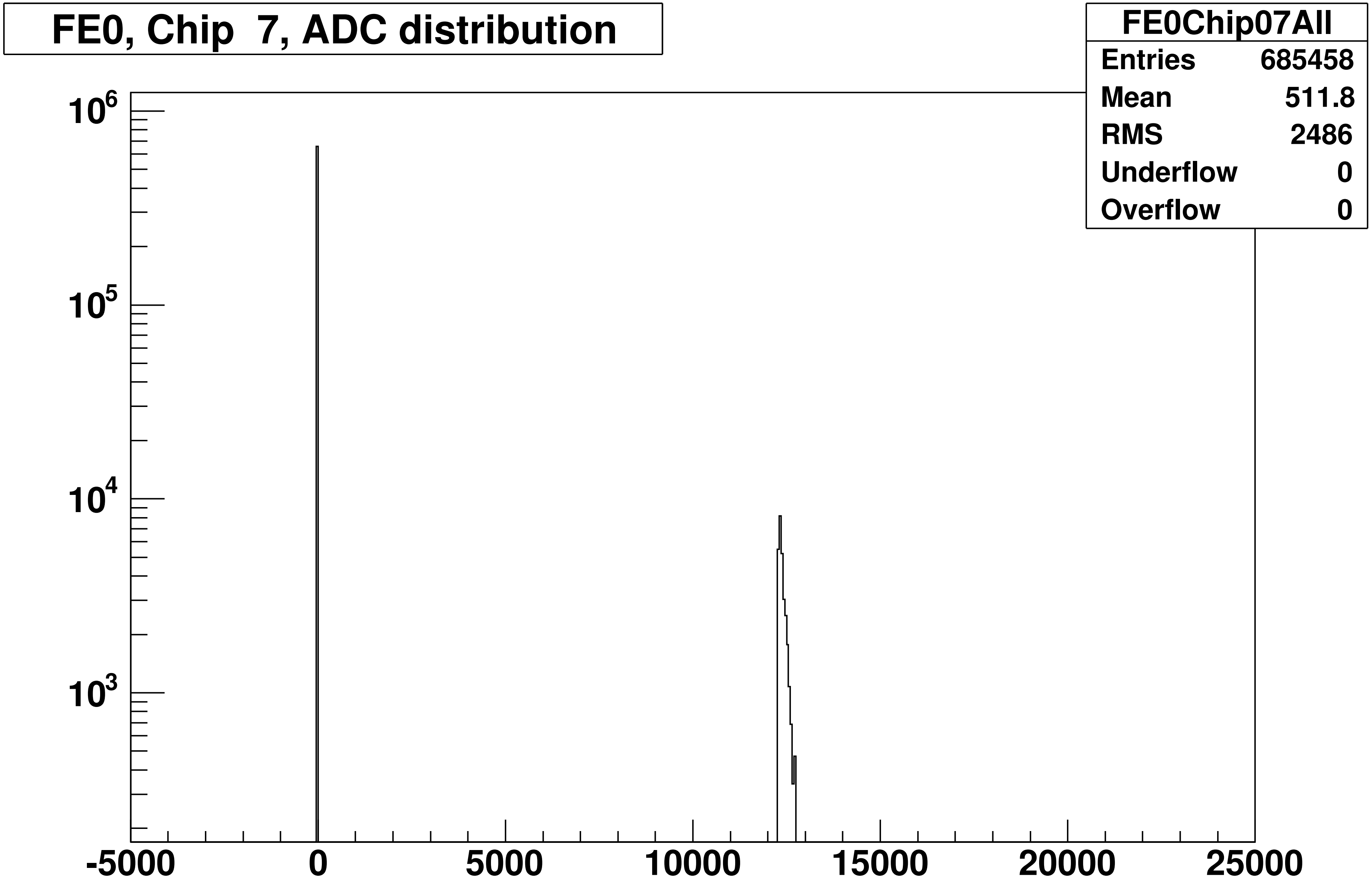
FE0, Chip 7, ADC distribution
FE0Chip07All
Entries 685458
Mean 511.8
RMS 2486
Underflow 0
Overflow 0
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10^4
10^3
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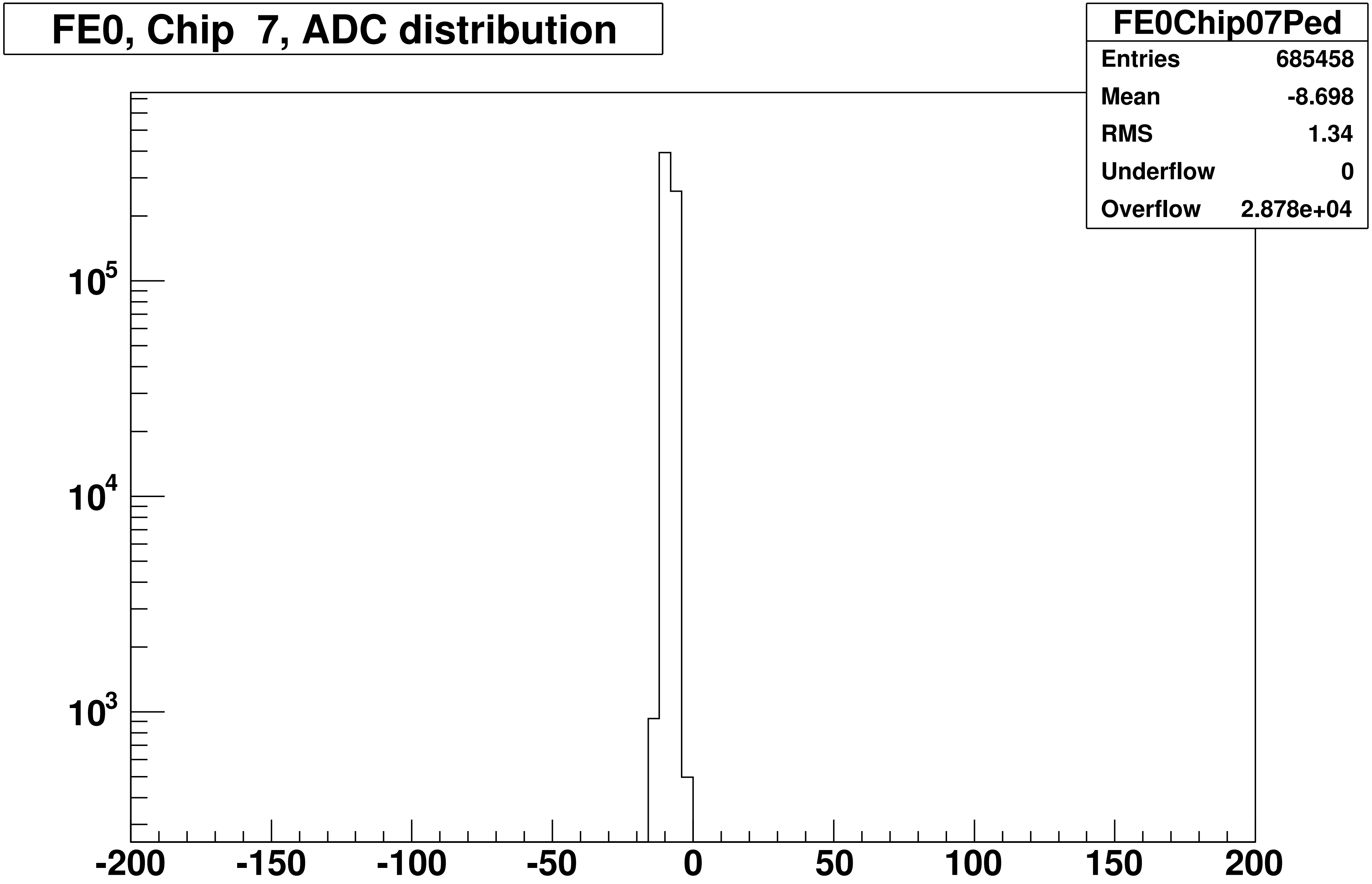
FE0, Chip 7, ADC distribution
FE0Chip07Ped
Entries 685458
Mean -8.698
RMS 1.34
Underflow 0
Overflow 2.878e+04
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10^4
10^3
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-100
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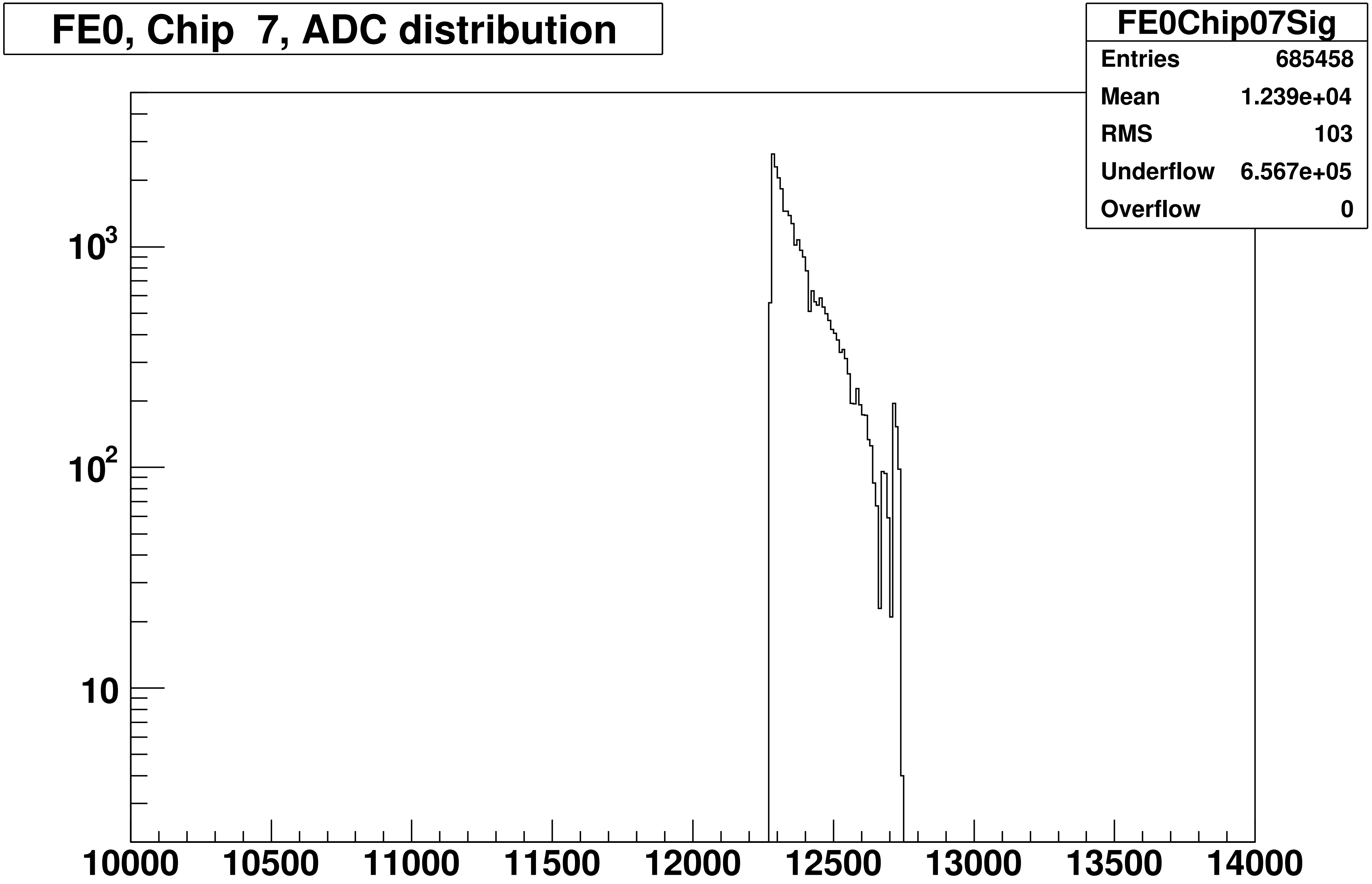
150
200


FE0, Chip 7, ADC distribution
FE0Chip07Sig
Entries 685458
Mean 1.239e+04
RMS 103
Underflow 6.567e+05
Overflow 0
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10^2
10
10000
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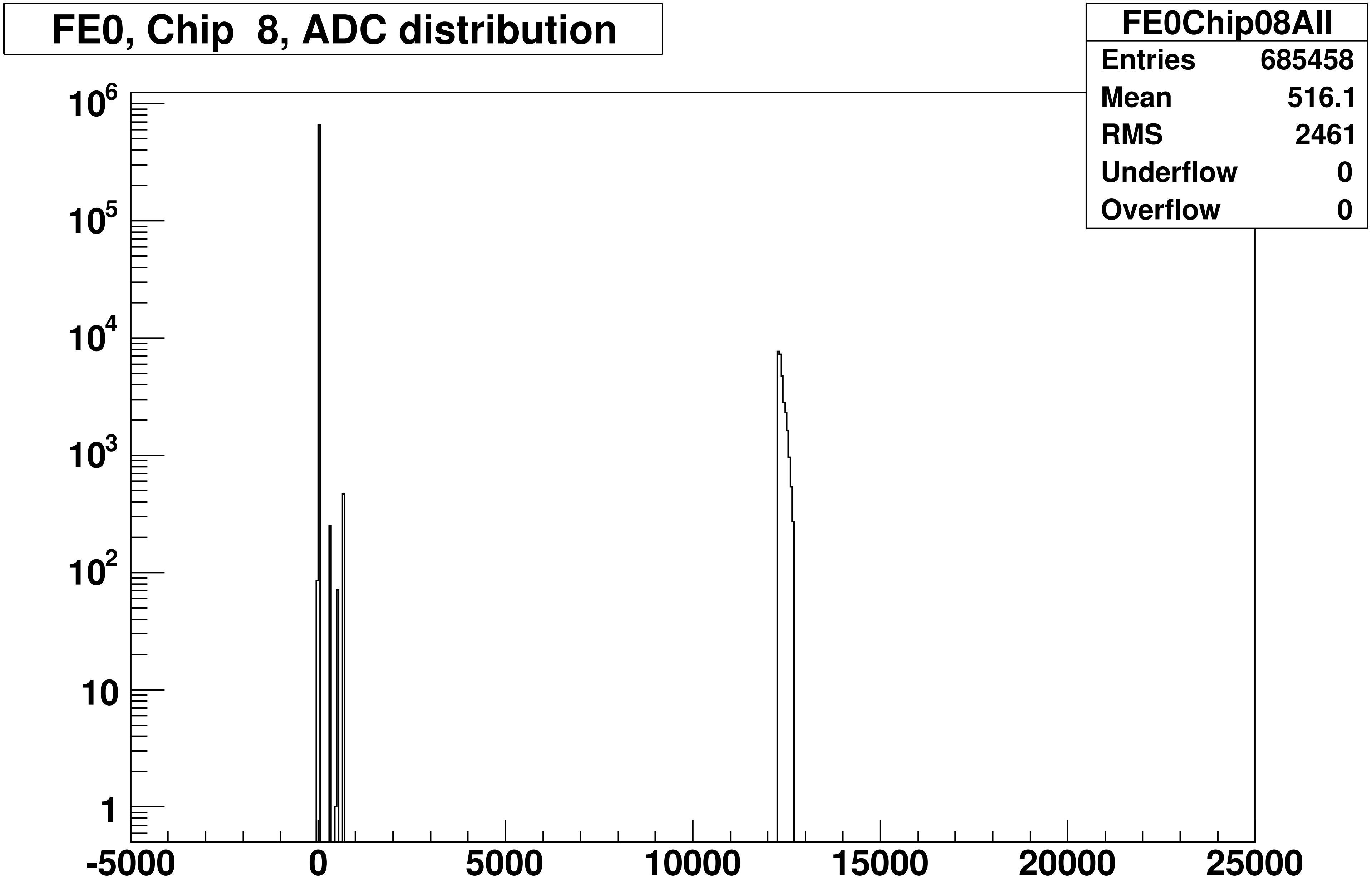

FE0, Chip 8, ADC distribution
FE0Chip08All
Entries 685458
Mean 516.1
RMS 2461
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
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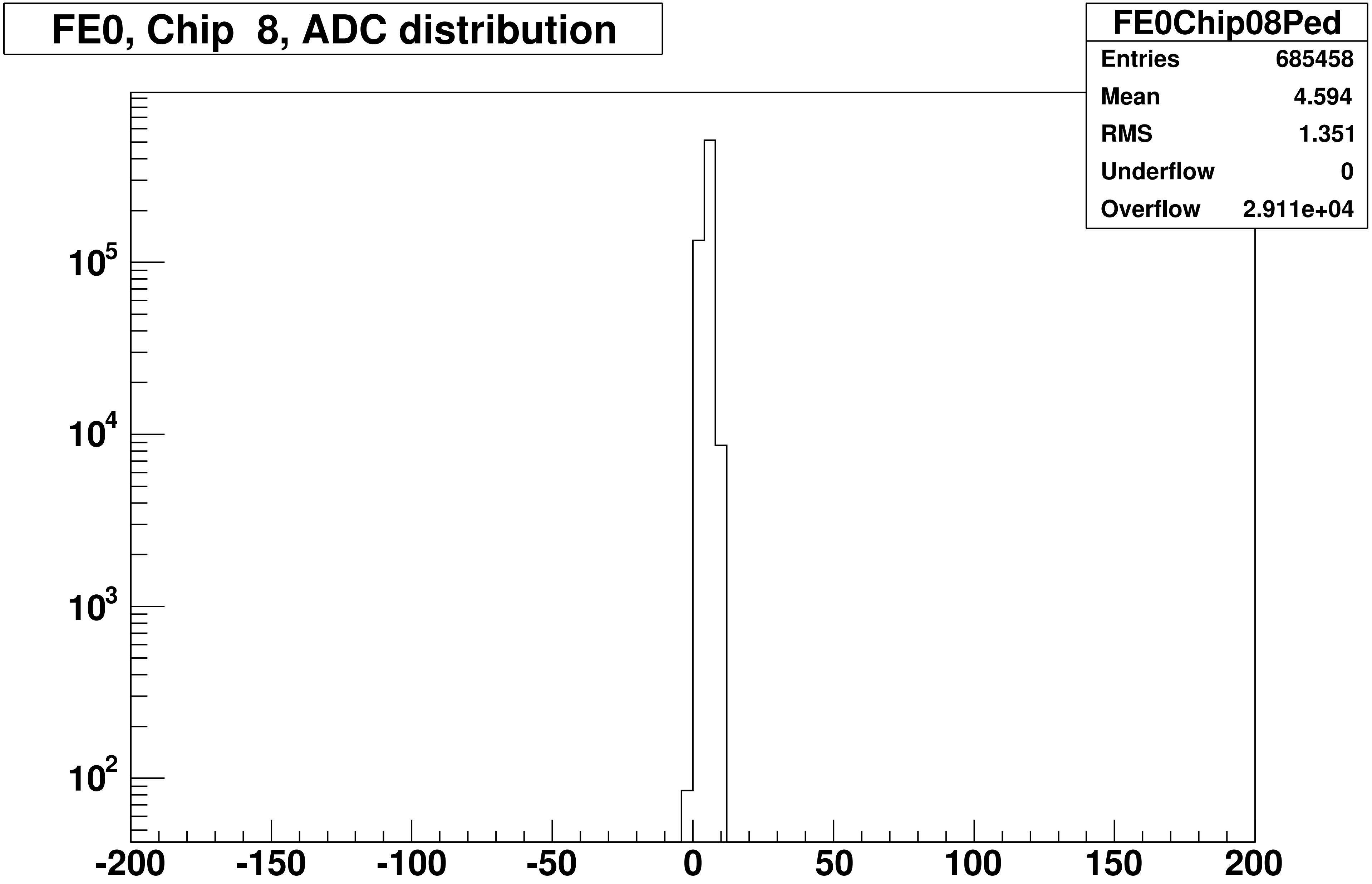
FE0, Chip 8, ADC distribution
FE0Chip08Ped
Entries 685458
Mean 4.594
RMS 1.351
Underflow 0
Overflow 2.911e+04
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10^4
10^3
10^2
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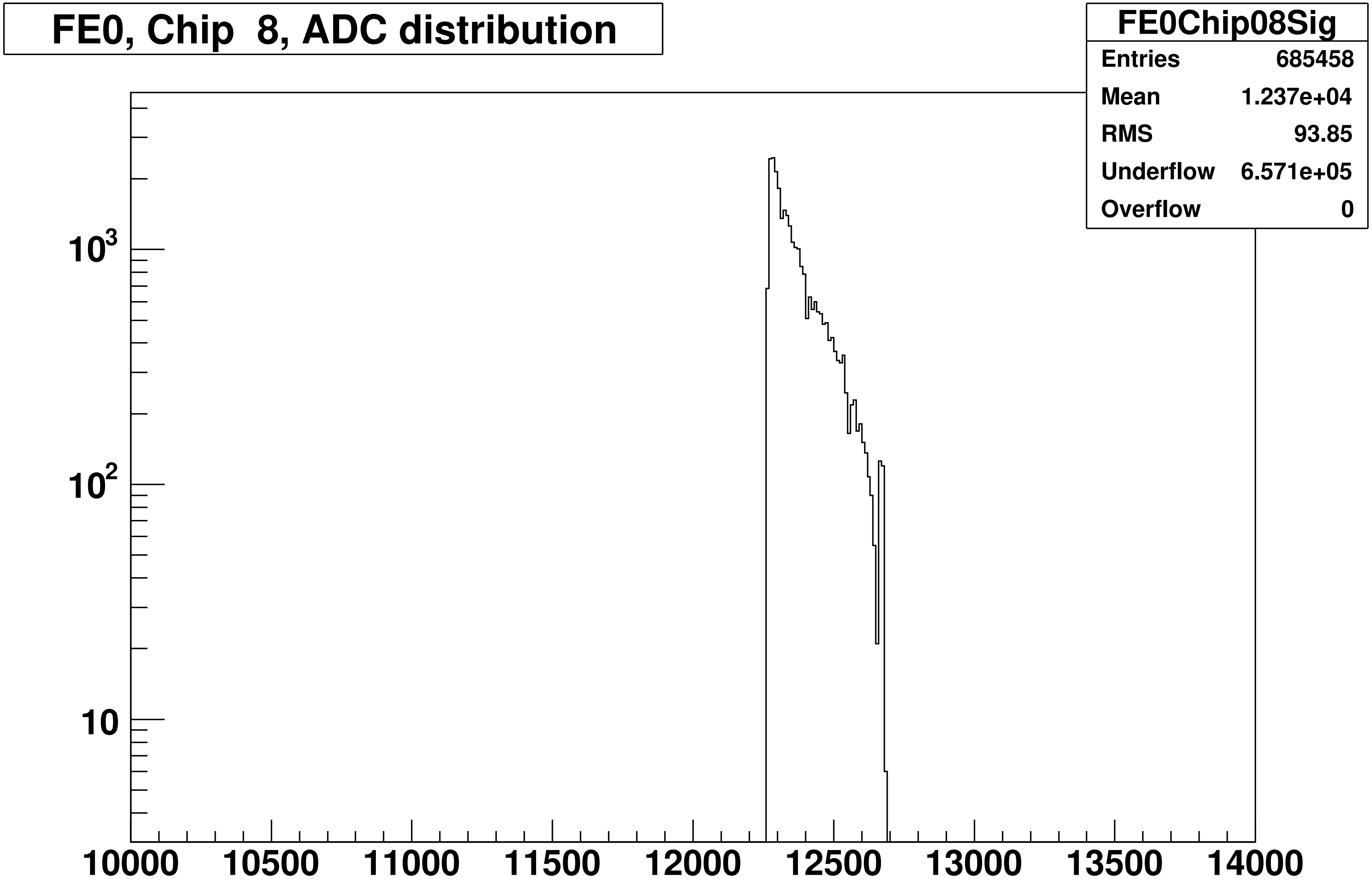

FE0, Chip 8, ADC distribution
FE0Chip08Sig
Entries 685458
Mean 1.237e+04
RMS 93.85
Underflow 6.571e+05
Overflow 0
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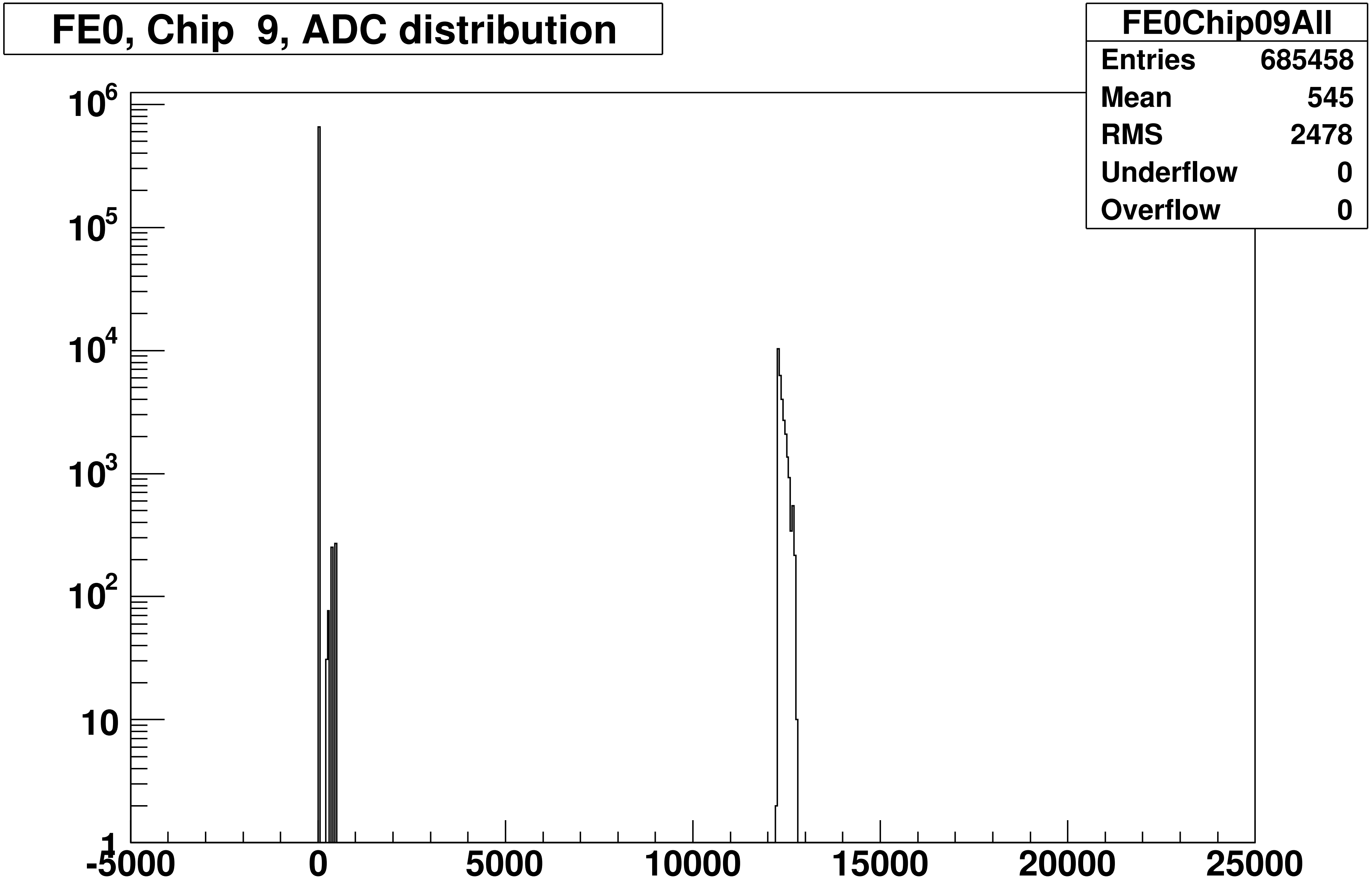
FE0, Chip 9, ADC distribution
FE0Chip09All
Entries 685458
Mean 545
RMS 2478
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
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0
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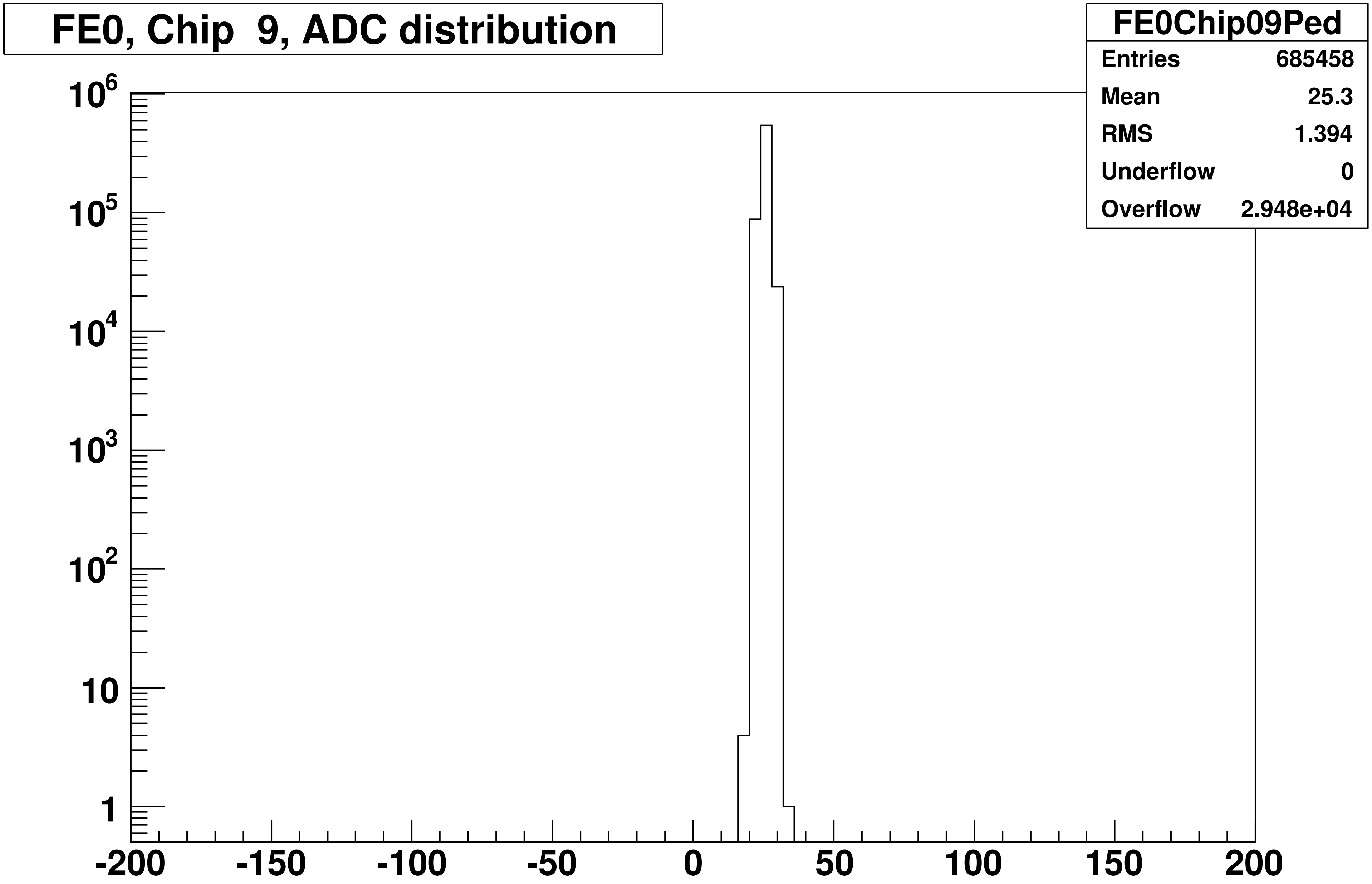
20000
25000



FE0, Chip 9, ADC distribution
FE0Chip09Ped
Entries 685458
Mean 25.3
RMS 1.394
Underflow 0
Overflow 2.948e+04
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10^5
10^4
10^3
10^2
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1
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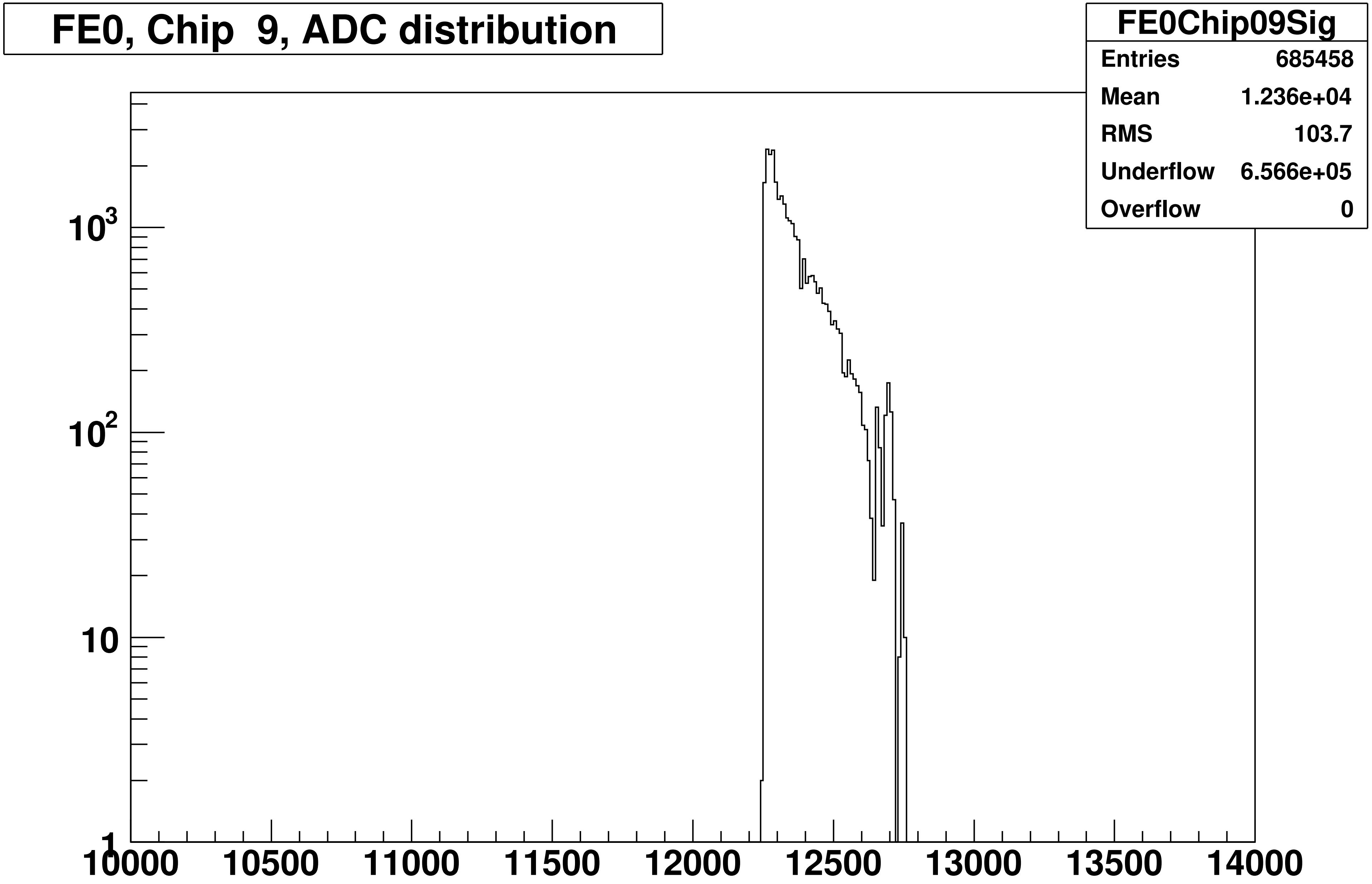
FE0, Chip 9, ADC distribution
FE0Chip09Sig
Entries 685458
Mean 1.236e+04
RMS 103.7
Underflow 6.566e+05
Overflow 0
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10^2
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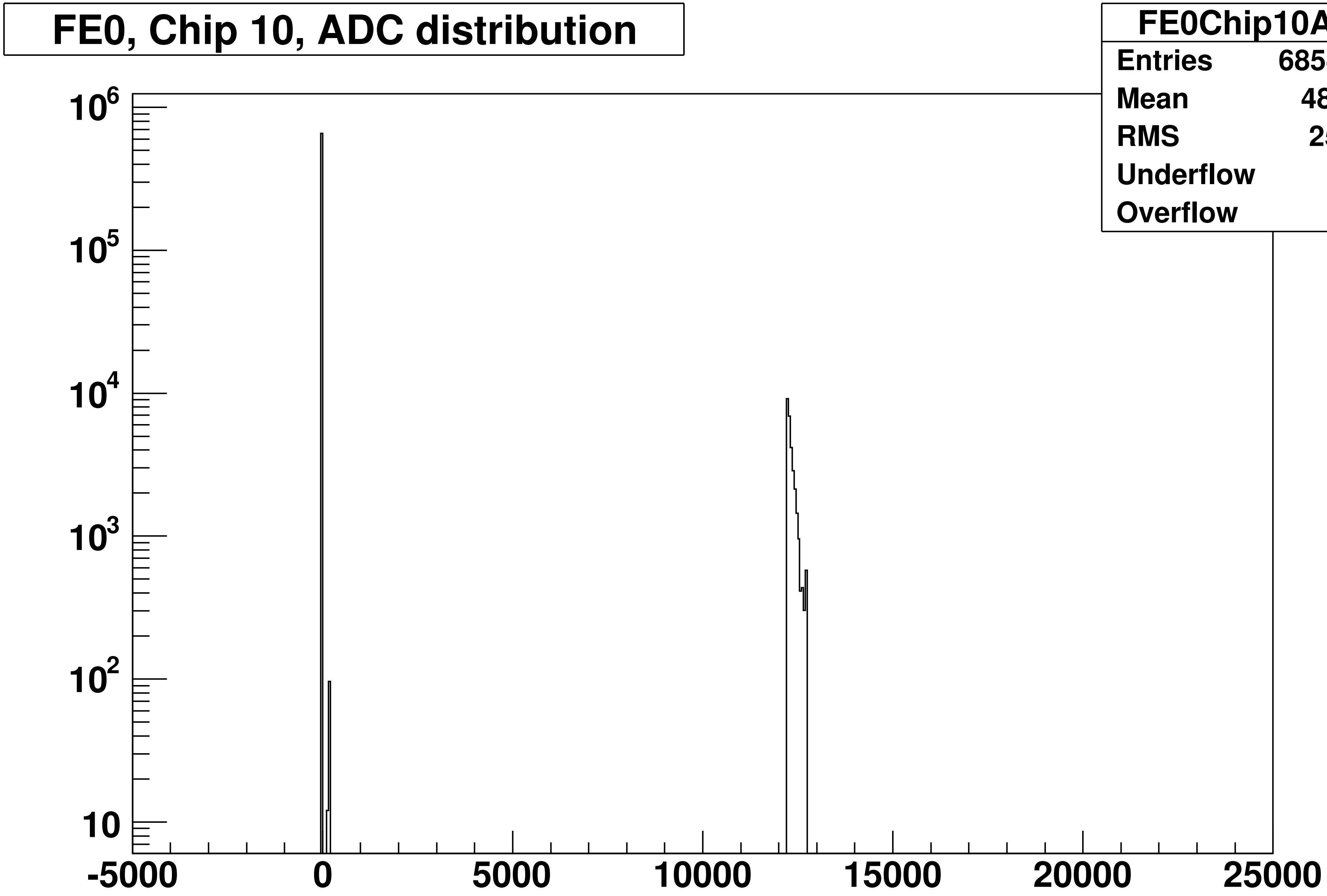

FE0, Chip 10, ADC distribution
FE0Chip10All
Entries 685458
Mean 489.3
RMS 2505
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
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-5000
0
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10000
15000
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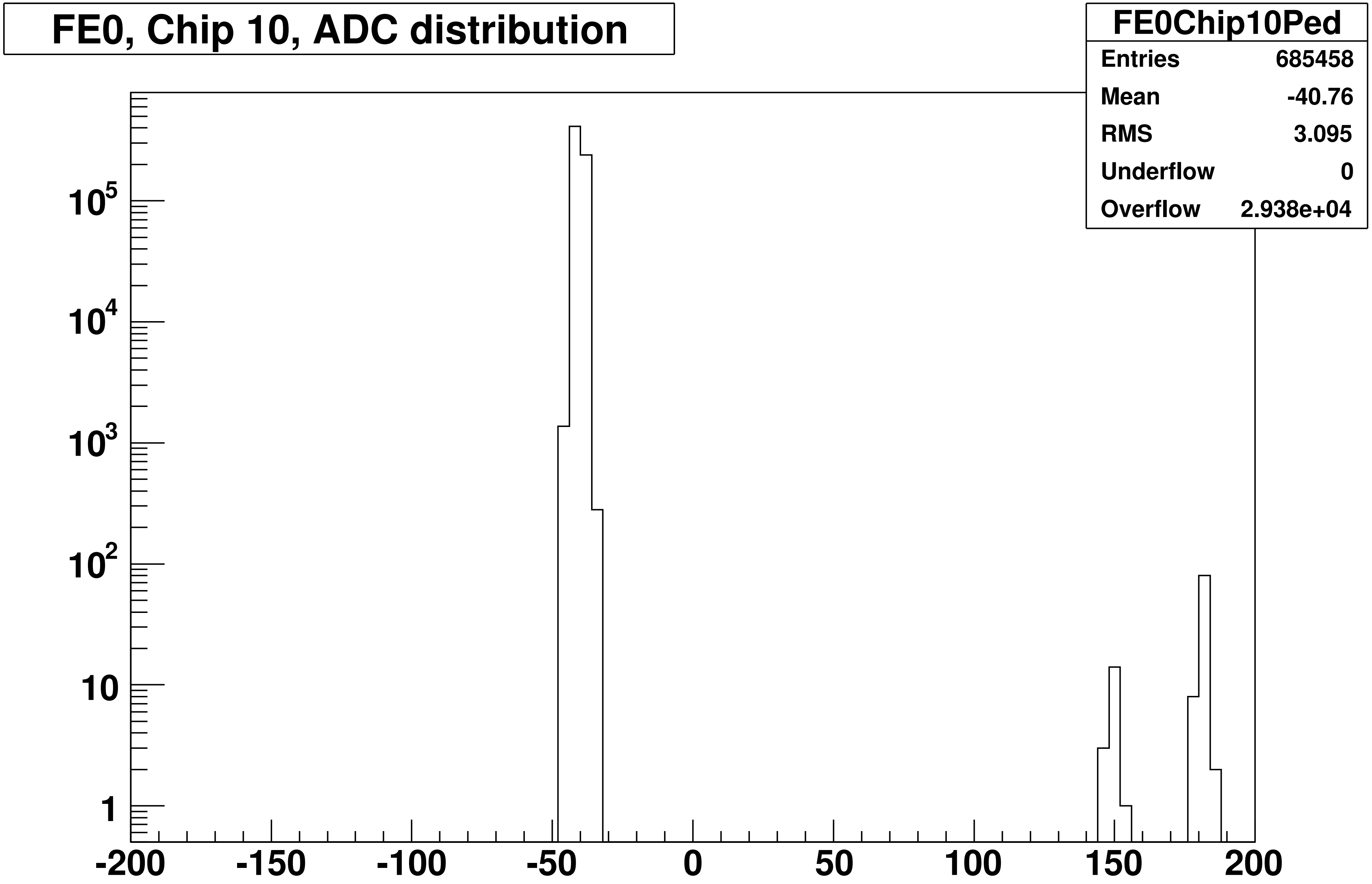

FE0, Chip 10, ADC distribution
FE0Chip10Ped
Entries 685458
Mean -40.76
RMS 3.095
Underflow 0
Overflow 2.938e+04
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10^3
10^2
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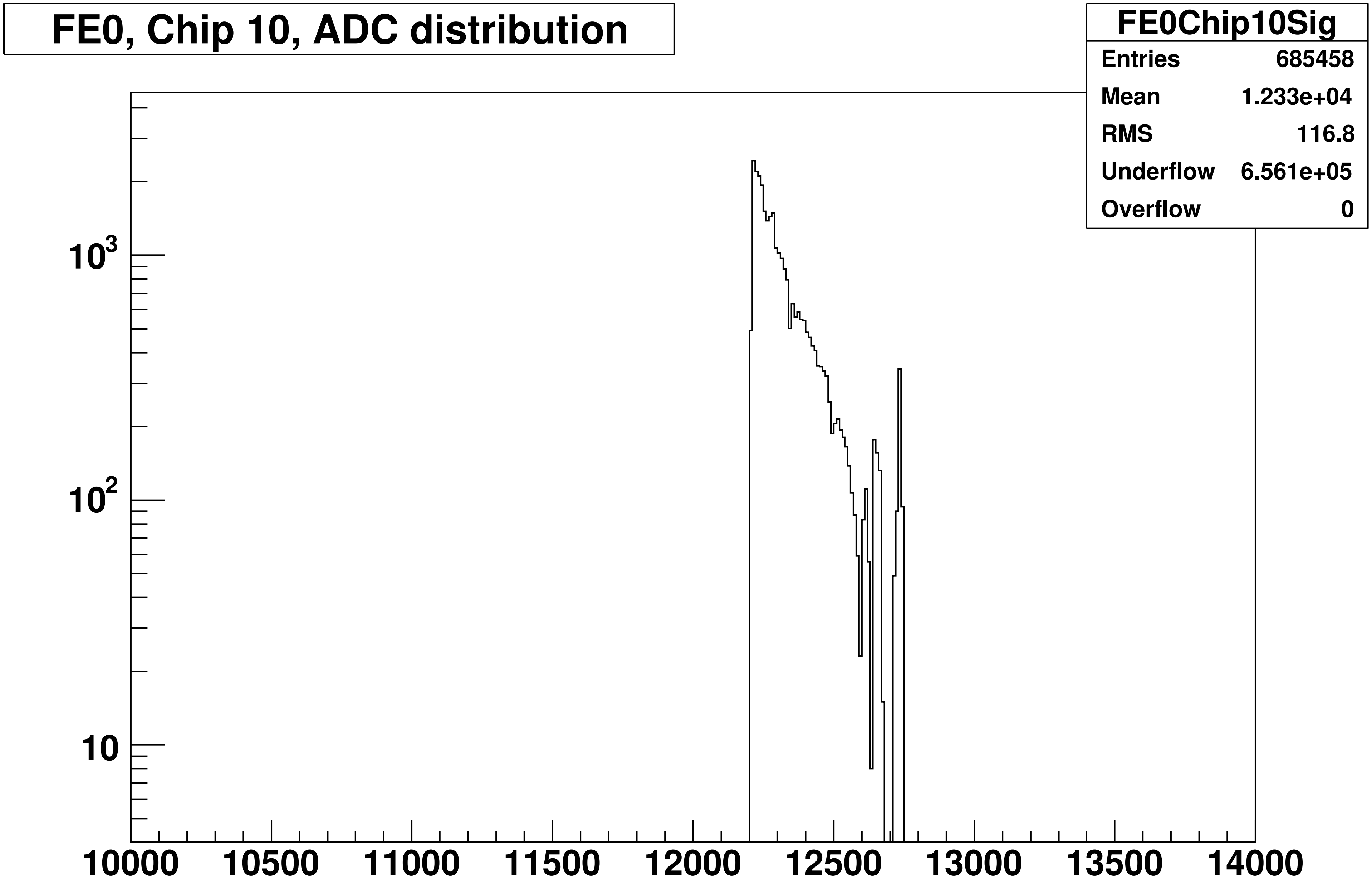
150
200



FE0, Chip 10, ADC distribution
FE0Chip10Sig
Entries 685458
Mean 1.233e+04
RMS 116.8
Underflow 6.561e+05
Overflow 0
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10^2
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10000
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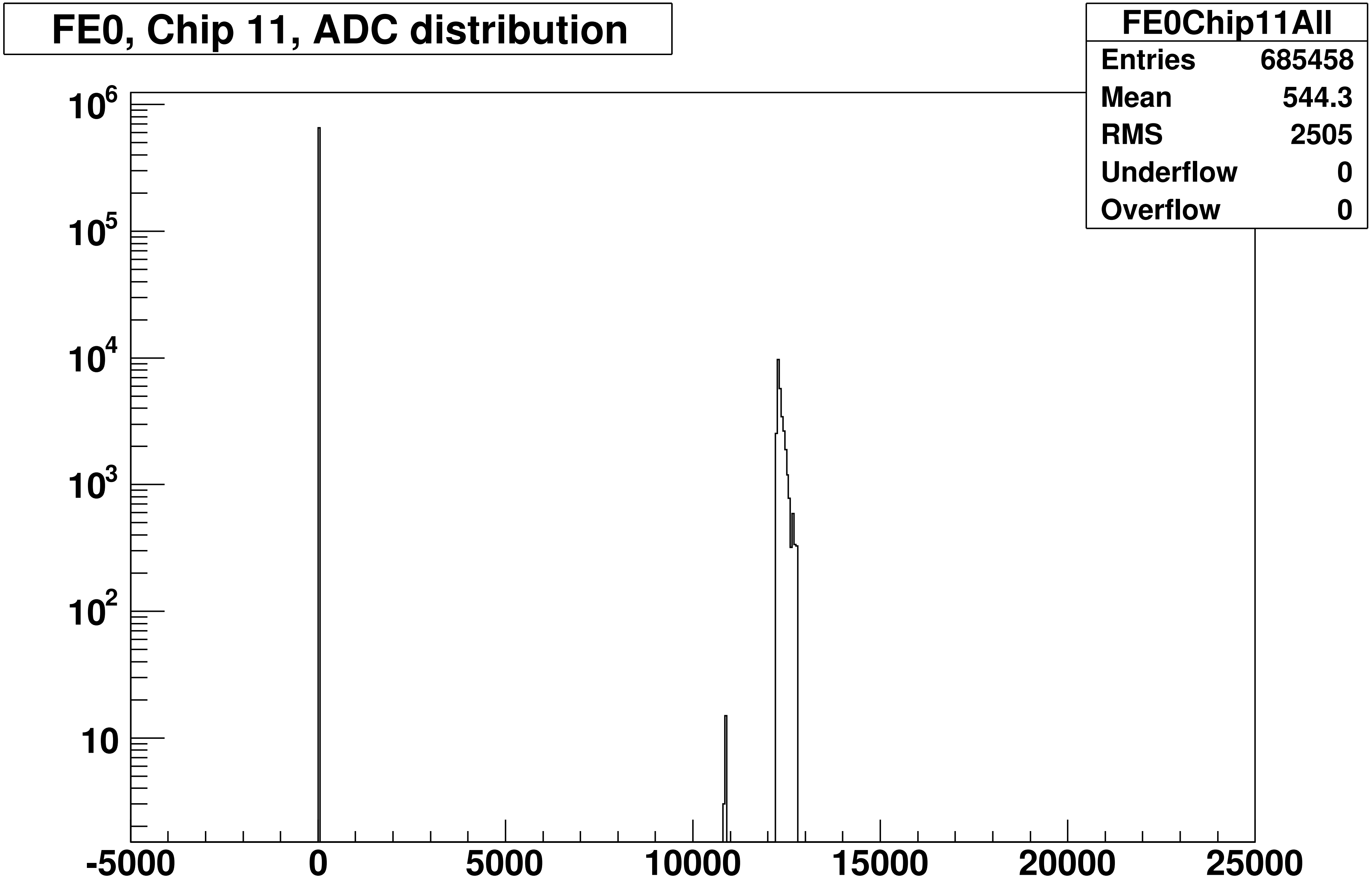
FE0, Chip 11, ADC distribution
FE0Chip11All
Entries 685458
Mean 544.3
RMS 2505
Underflow 0
Overflow 0
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10^3
10^4
10^5
10^6
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0
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10000
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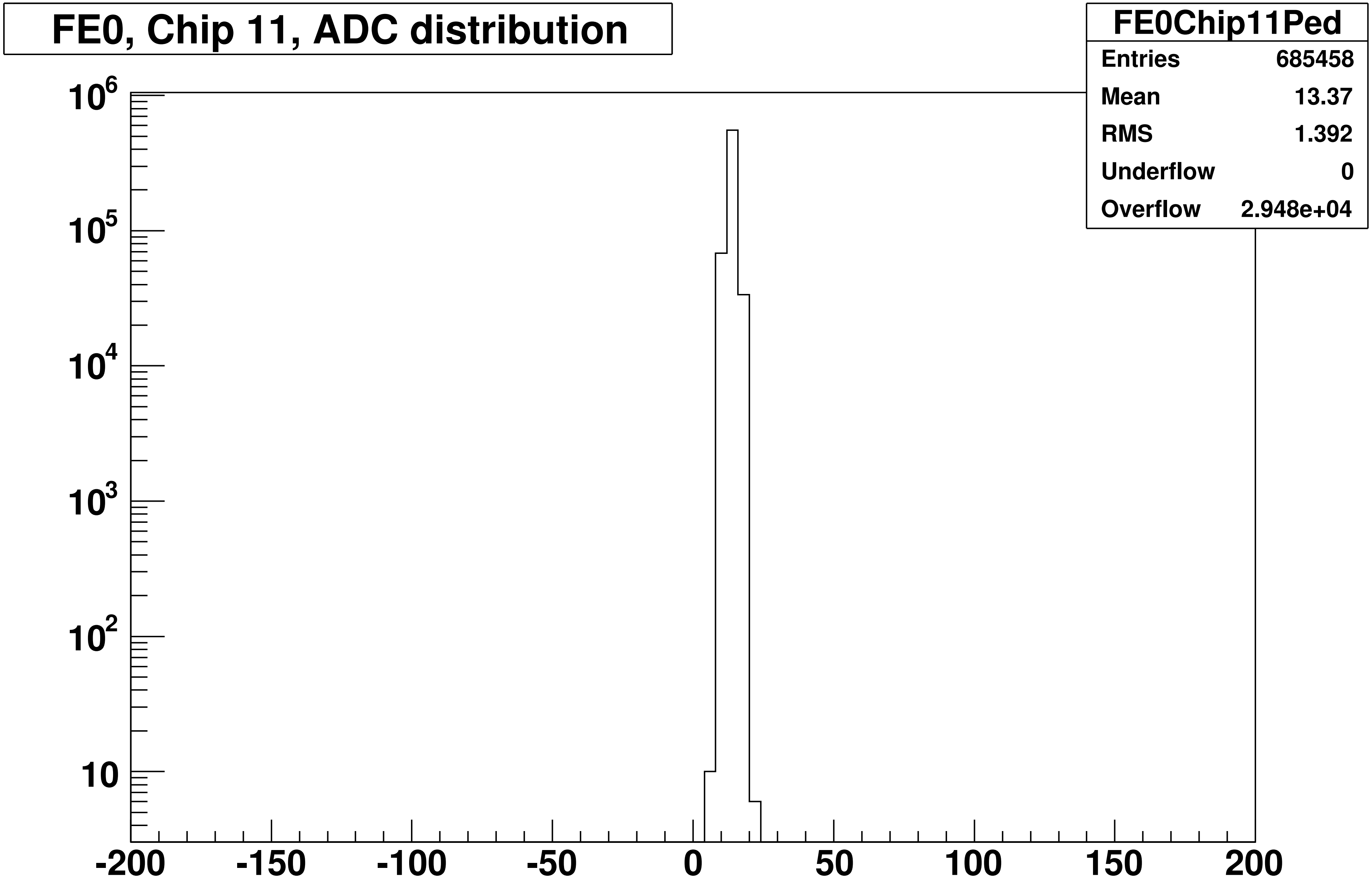
FE0, Chip 11, ADC distribution
FE0Chip11Ped
Entries 685458
Mean 13.37
RMS 1.392
Underflow 0
Overflow 2.948e+04
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10^4
10^5
10^6
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-100
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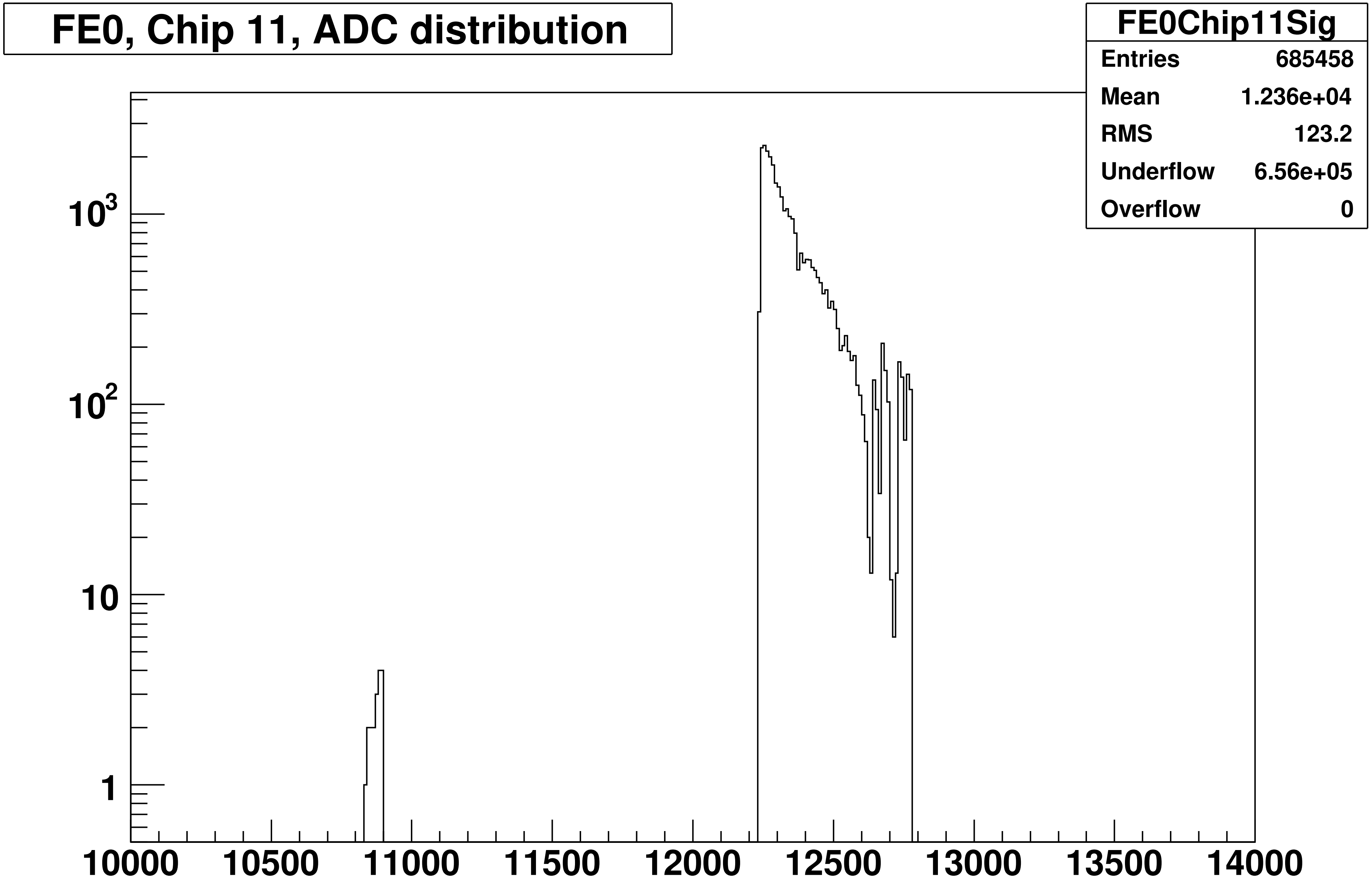
0
50
100
150
200


FE0, Chip 11, ADC distribution
FE0Chip11Sig
Entries 685458
Mean 1.236e+04
RMS 123.2
Underflow 6.56e+05
Overflow 0
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10^2
10
1
10000
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11500
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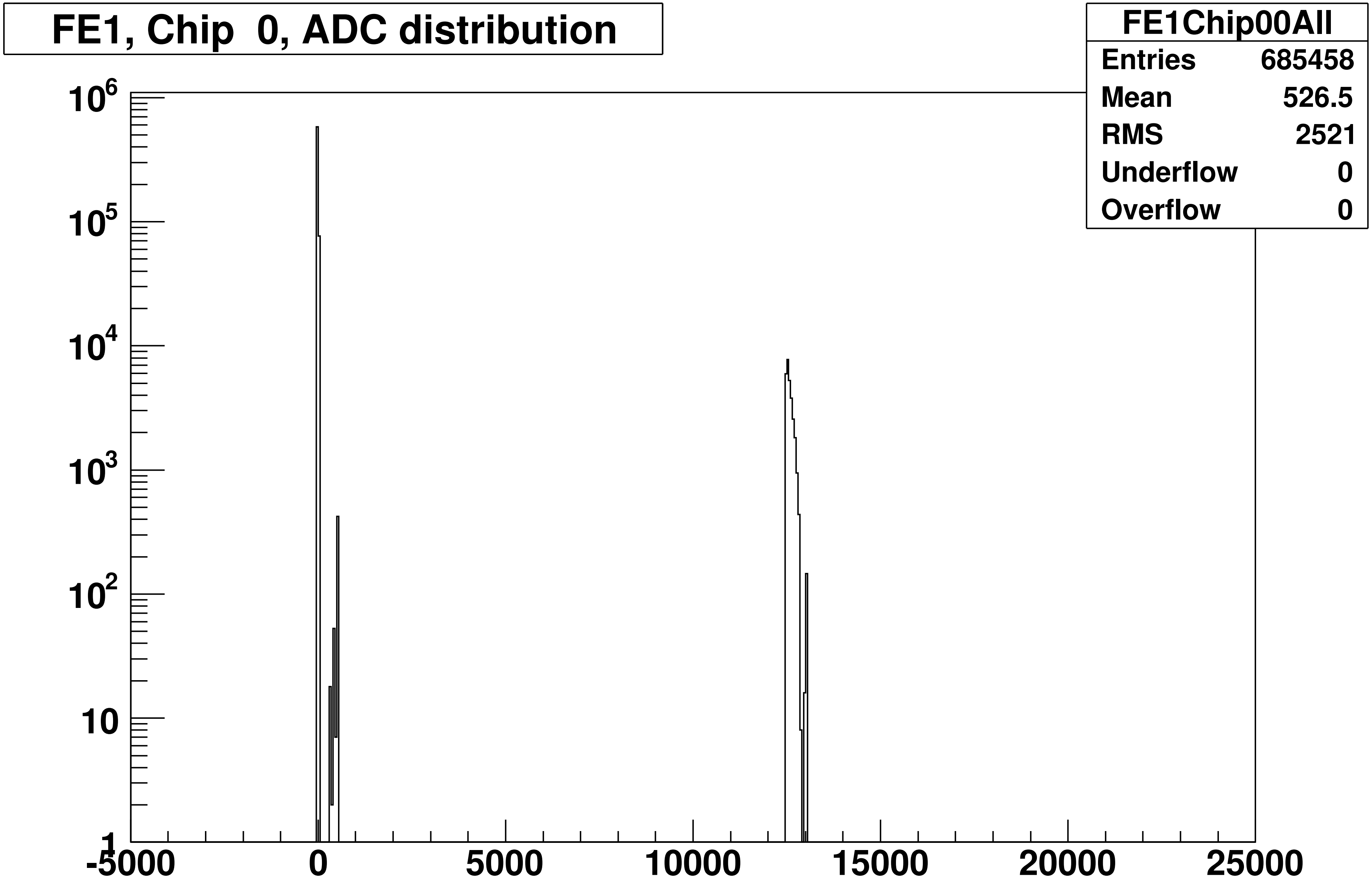
FE1, Chip 0, ADC distribution
FE1Chip00All
Entries 685458
Mean 526.5
RMS 2521
Underflow 0
Overflow 0
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10^4
10^3
10^2
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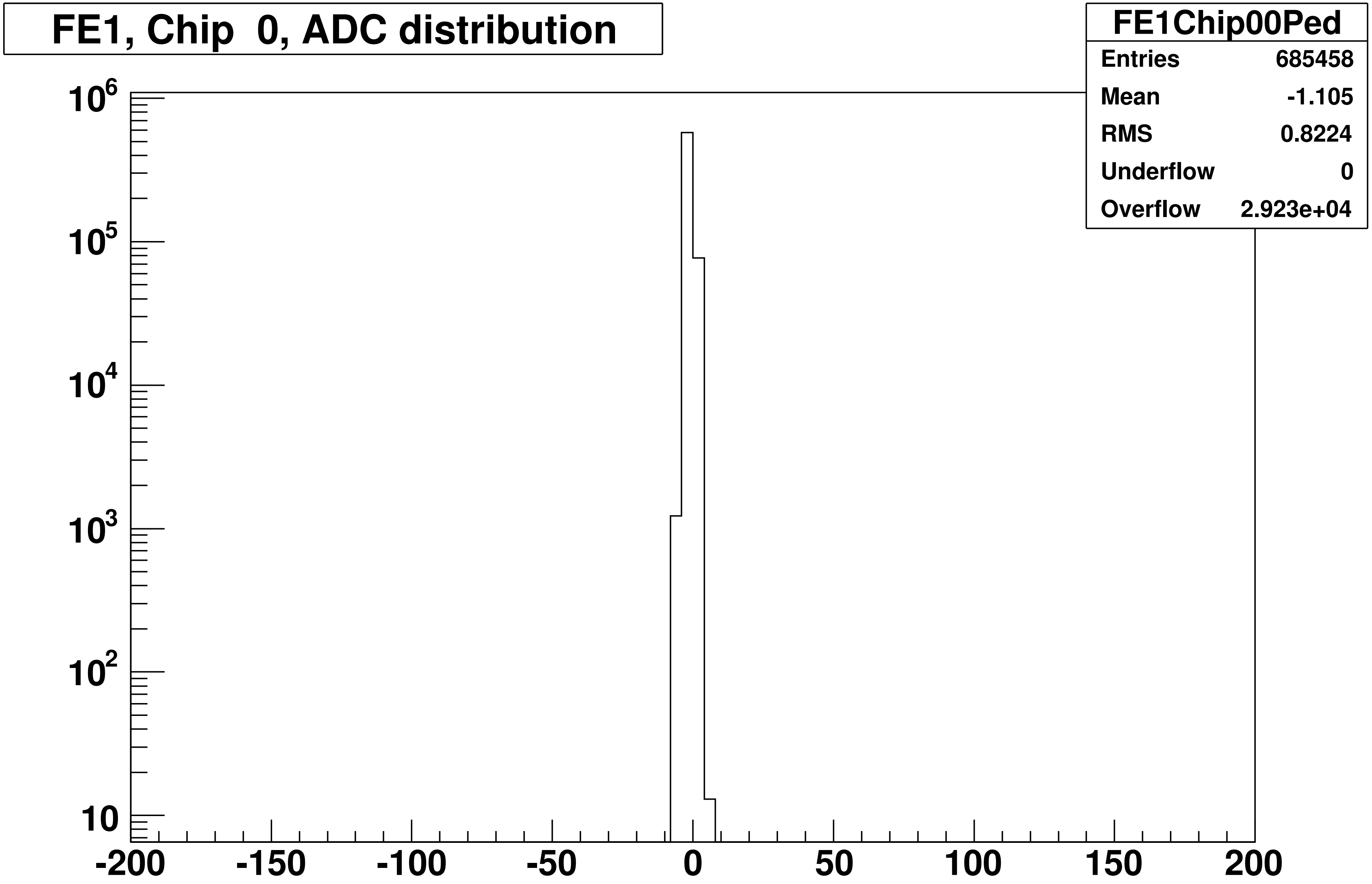
FE1, Chip 0, ADC distribution
FE1Chip00Ped
Entries 685458
Mean -1.105
RMS 0.8224
Underflow 0
Overflow 2.923e+04
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10^4
10^3
10^2
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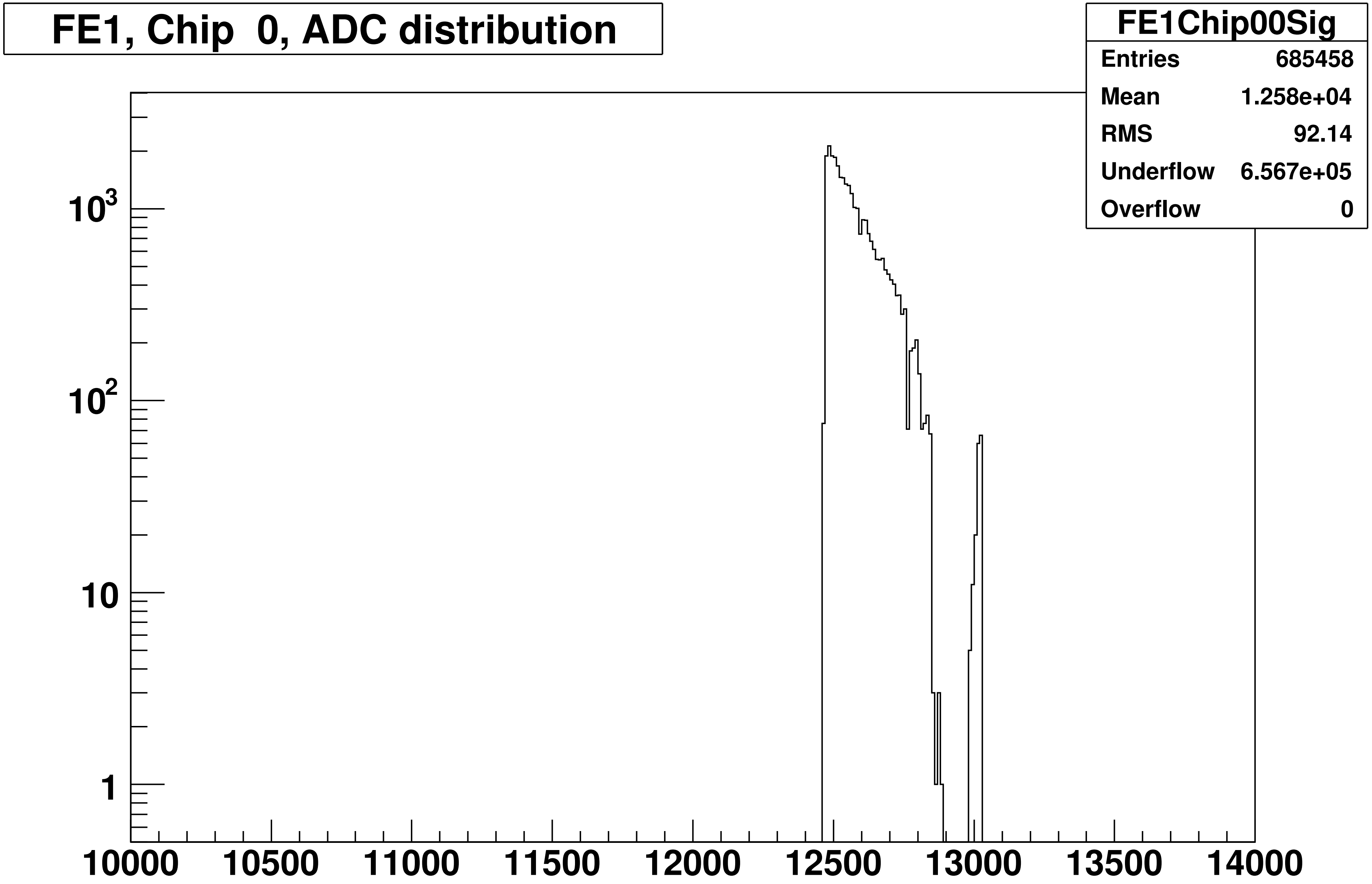
50
100
150
200


FE1, Chip 0, ADC distribution
FE1Chip00Sig
Entries 685458
Mean 1.258e+04
RMS 92.14
Underflow 6.567e+05
Overflow 0
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10^2
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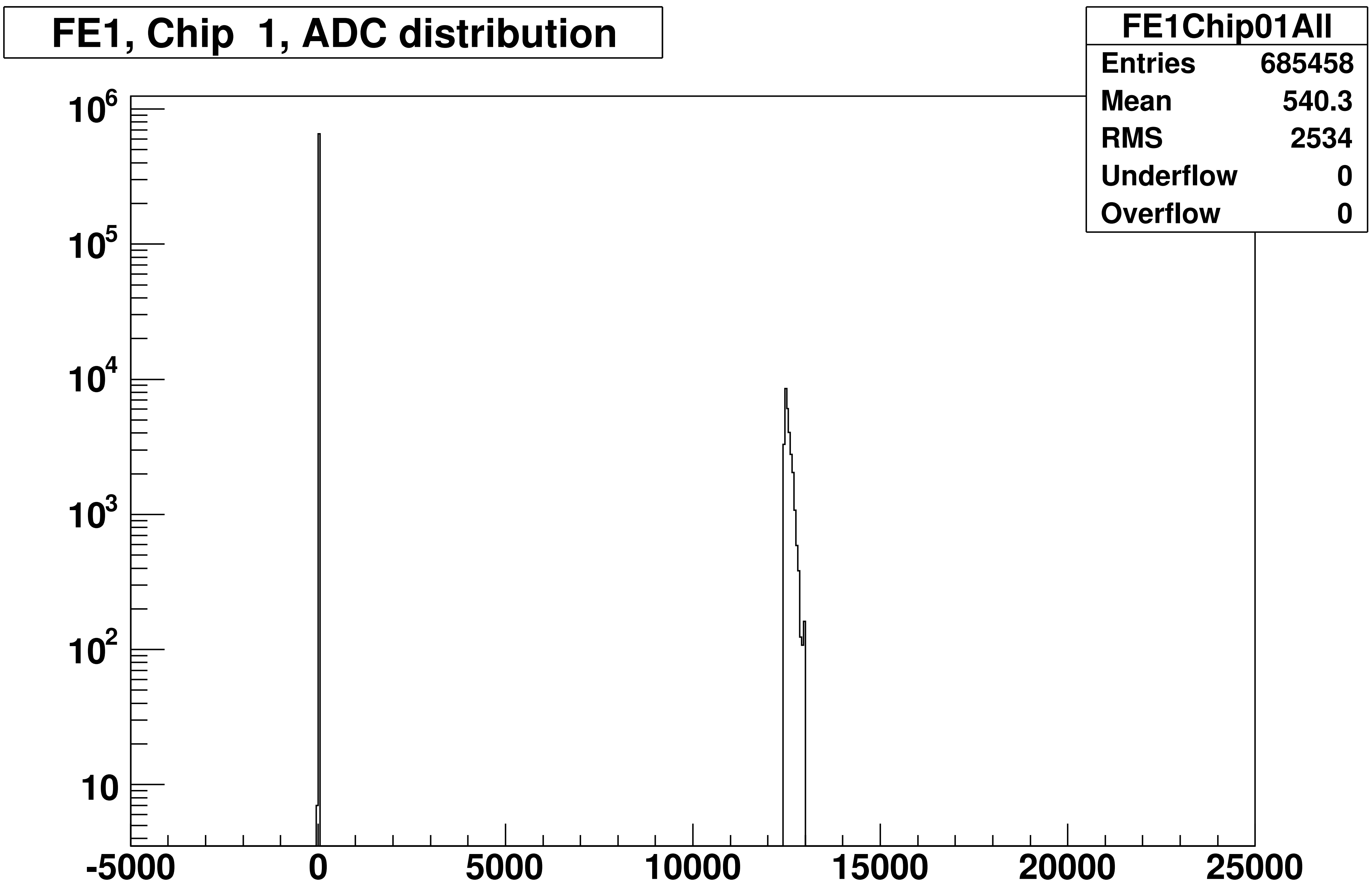
FE1, Chip 1, ADC distribution
FE1Chip01All
Entries 685458
Mean 540.3
RMS 2534
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
-5000
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5000
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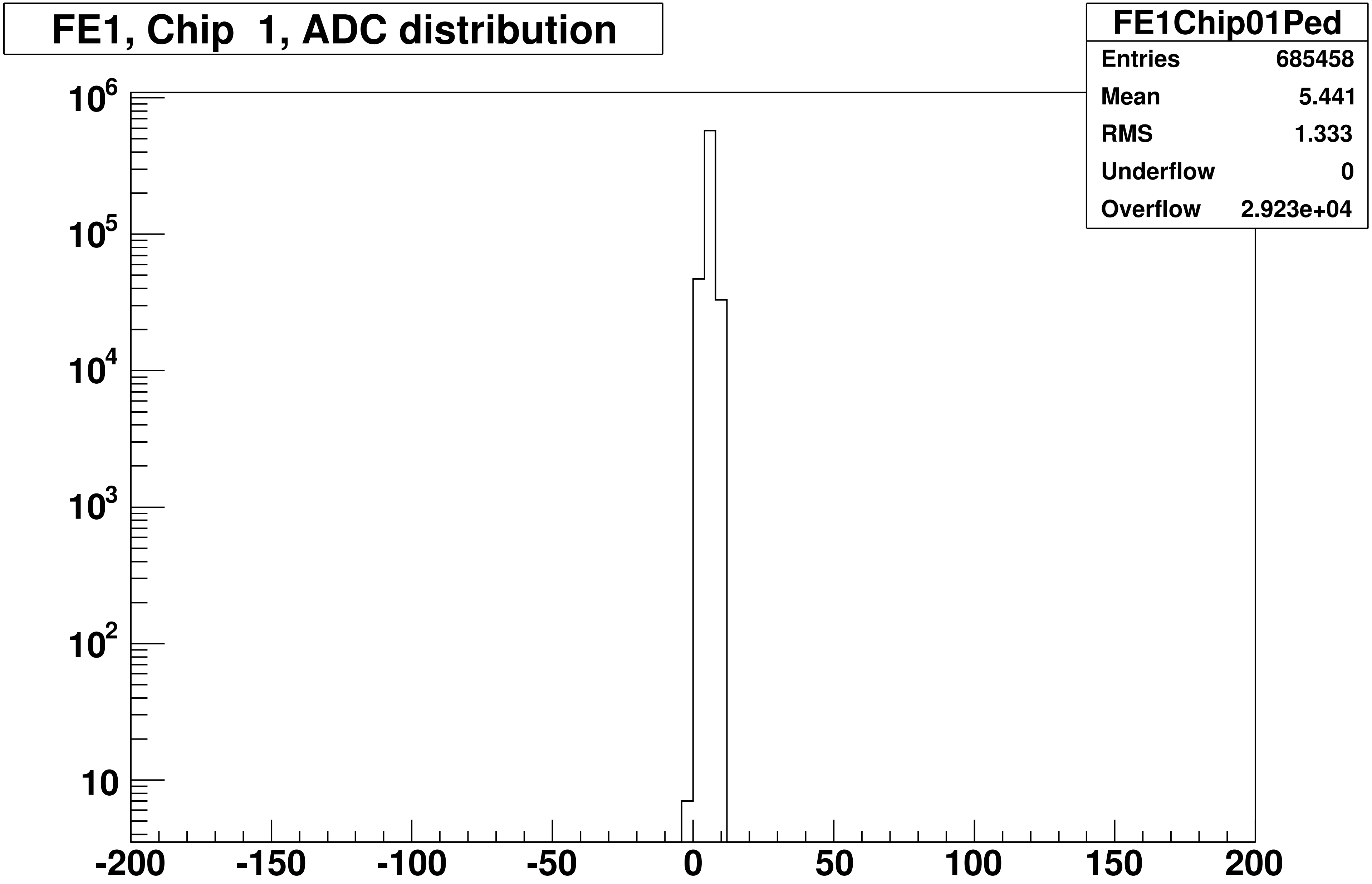
25000


FE1, Chip 1, ADC distribution
FE1Chip01Ped
Entries 685458
Mean 5.441
RMS 1.333
Underflow 0
Overflow 2.923e+04
10^6
10^5
10^4
10^3
10^2
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-200
-150
-100
-50
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150
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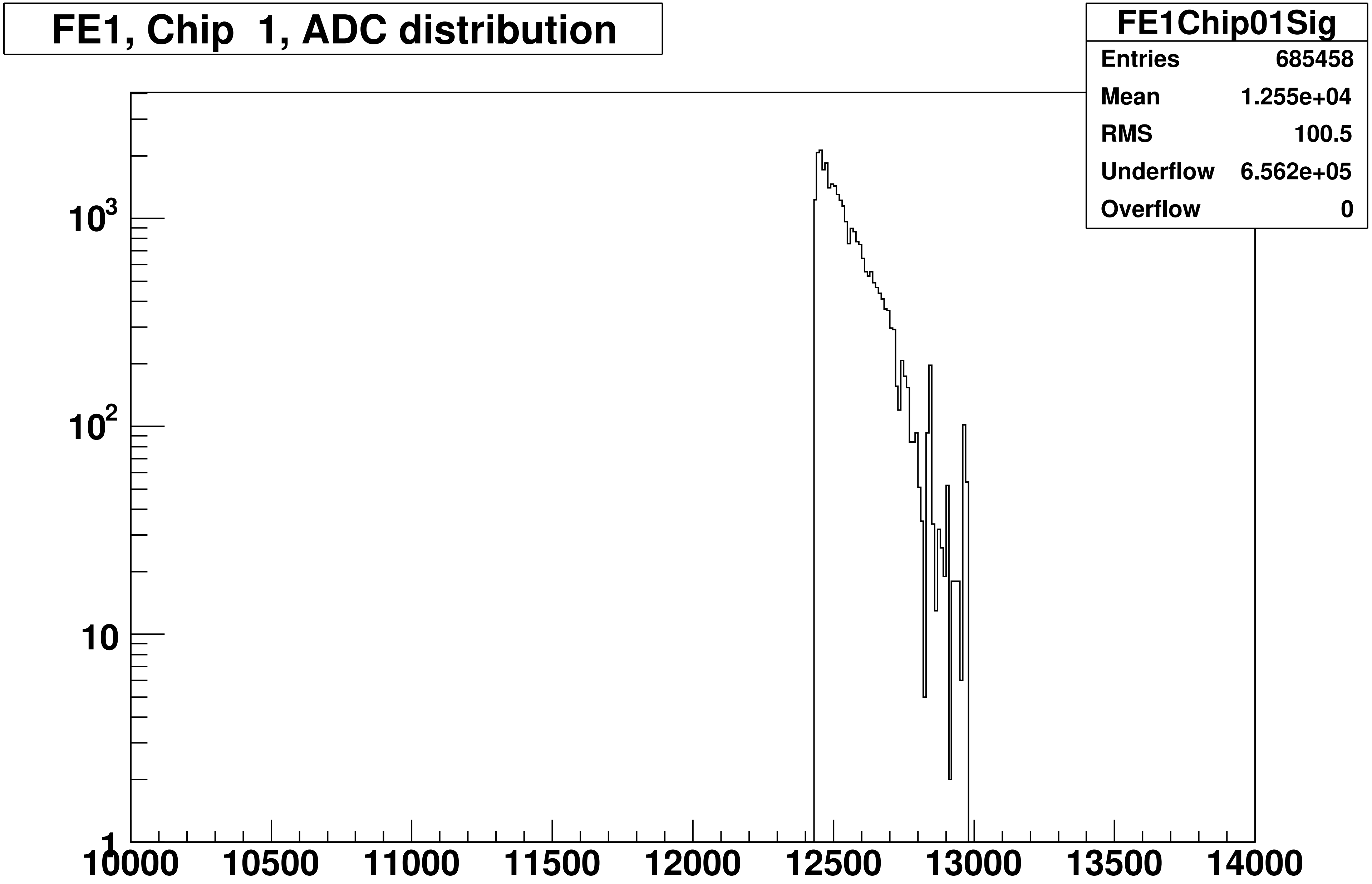
FE1, Chip 1, ADC distribution
FE1Chip01Sig
Entries 685458
Mean 1.255e+04
RMS 100.5
Underflow 6.562e+05
Overflow 0
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10^2
10
1
10000
10500
11000
11500
12000
12500
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13500
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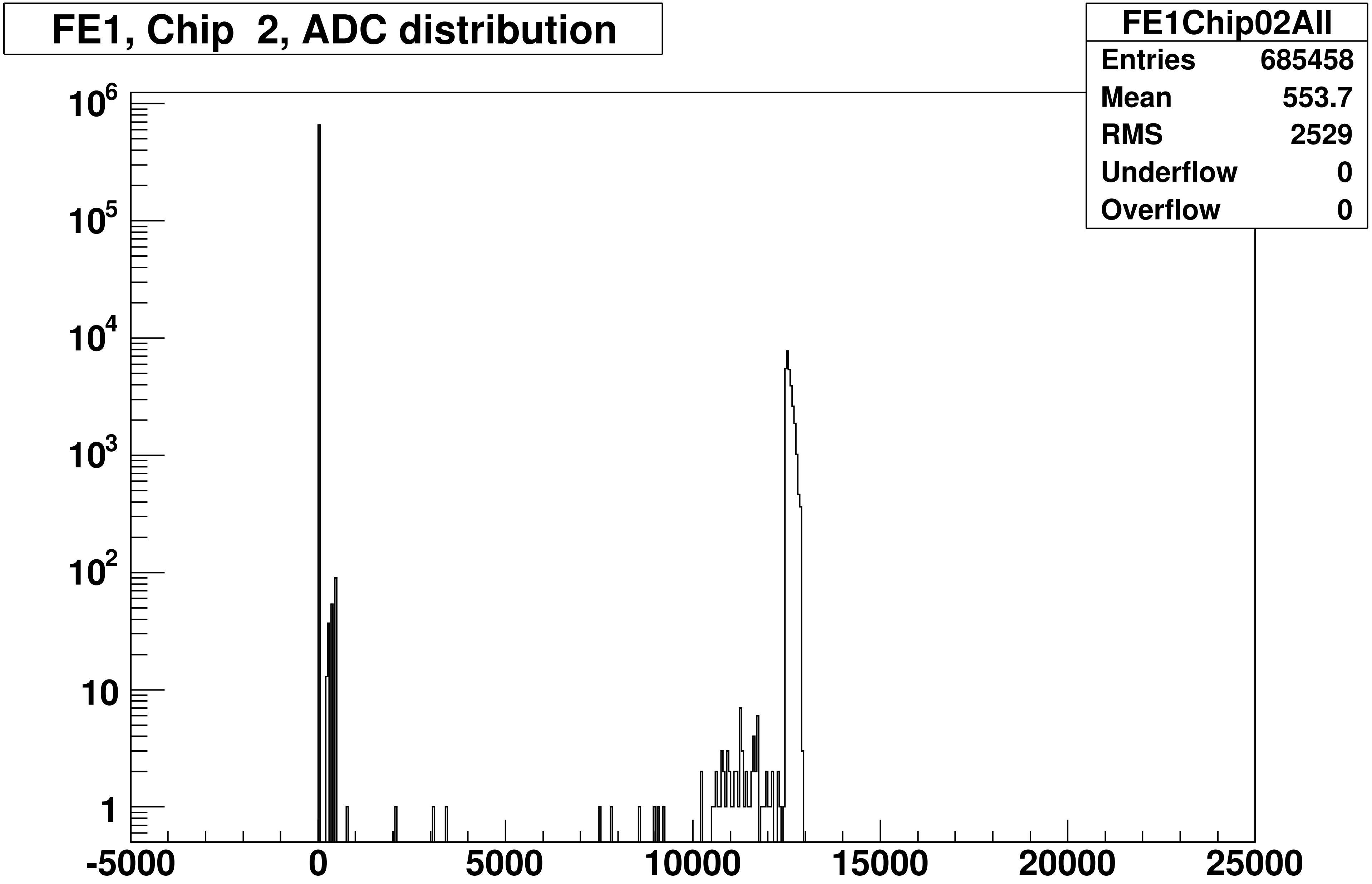

FE1, Chip 2, ADC distribution
FE1Chip02All
Entries 685458
Mean 553.7
RMS 2529
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
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10000
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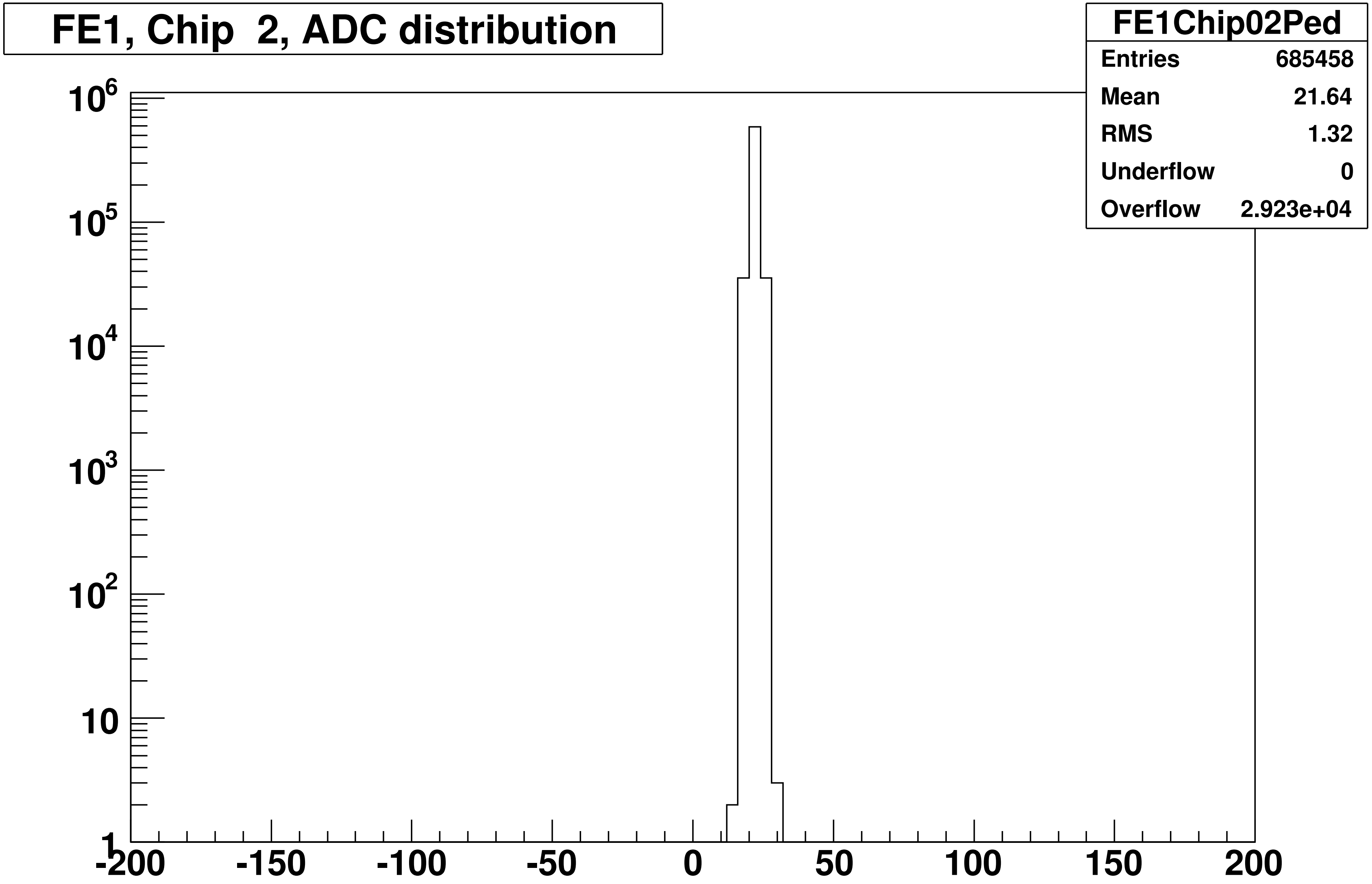
FE1, Chip 2, ADC distribution
FE1Chip02Ped
Entries 685458
Mean 21.64
RMS 1.32
Underflow 0
Overflow 2.923e+04
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10^5
10^4
10^3
10^2
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1
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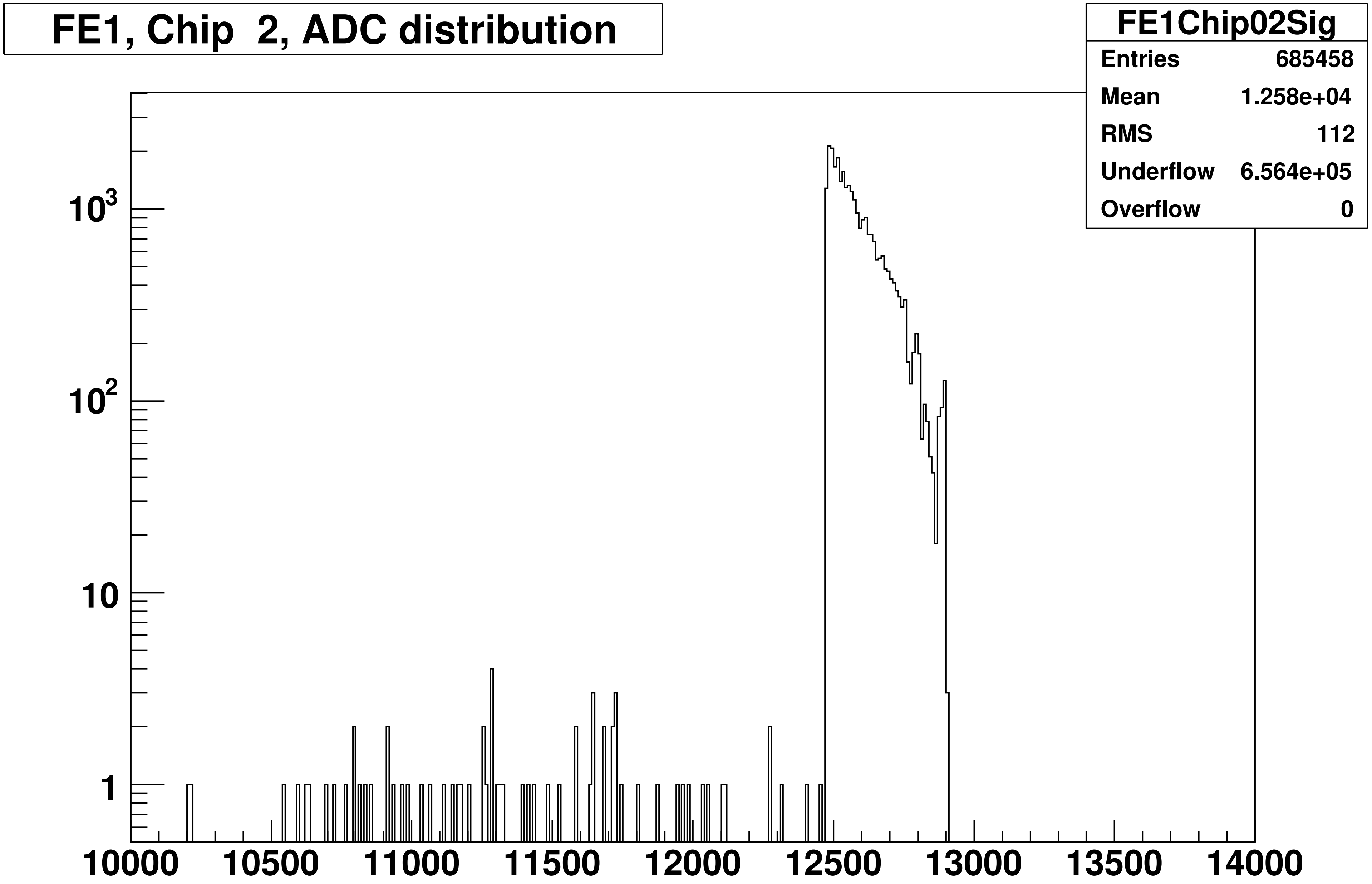

FE1, Chip 2, ADC distribution
FE1Chip02Sig
Entries 685458
Mean 1.258e+04
RMS 112
Underflow 6.564e+05
Overflow 0
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10^2
10
1
10000
10500
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11500
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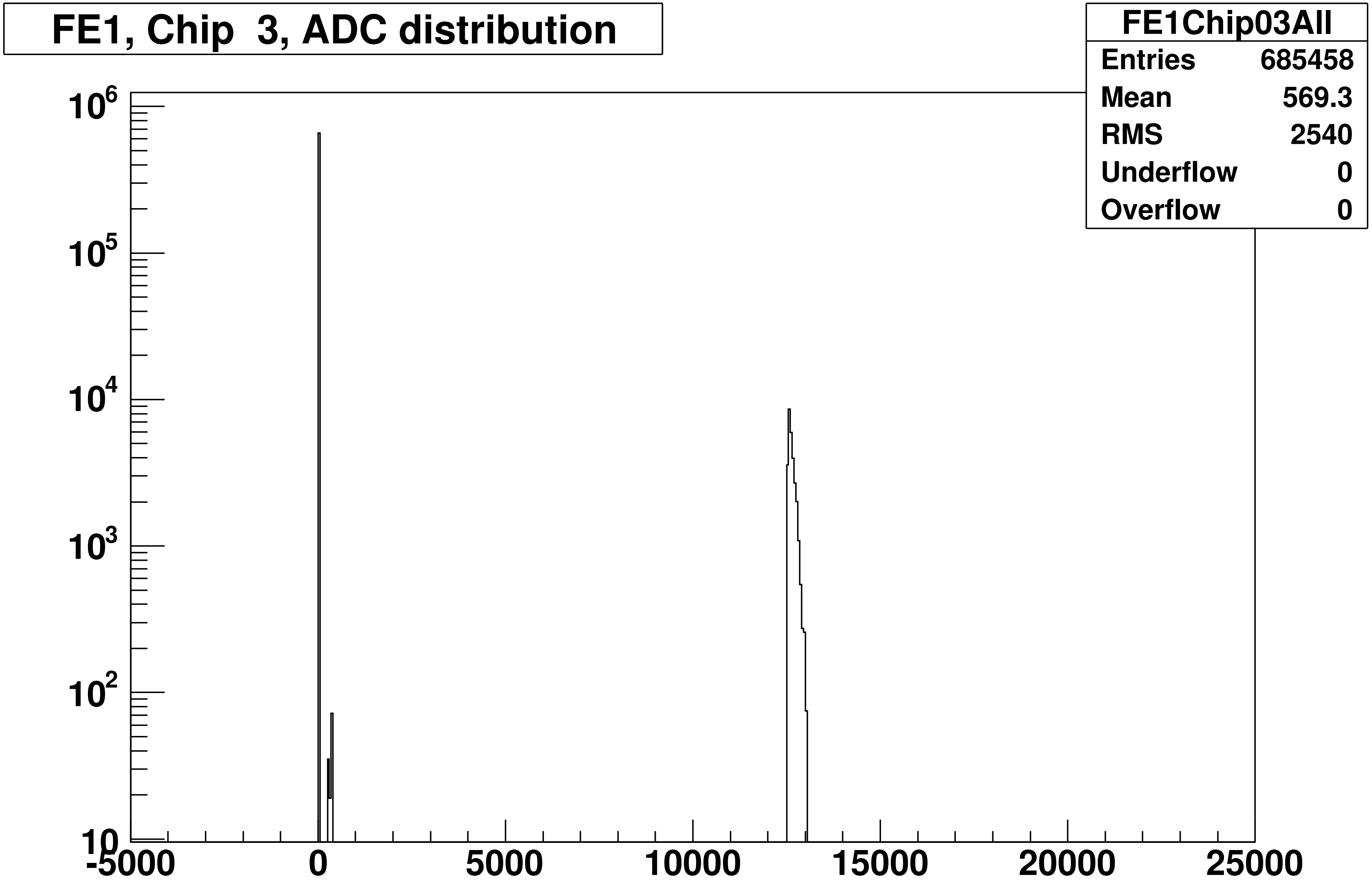
FE1, Chip 3, ADC distribution
FE1Chip03All
Entries 685458
Mean 569.3
RMS 2540
Underflow 0
Overflow 0
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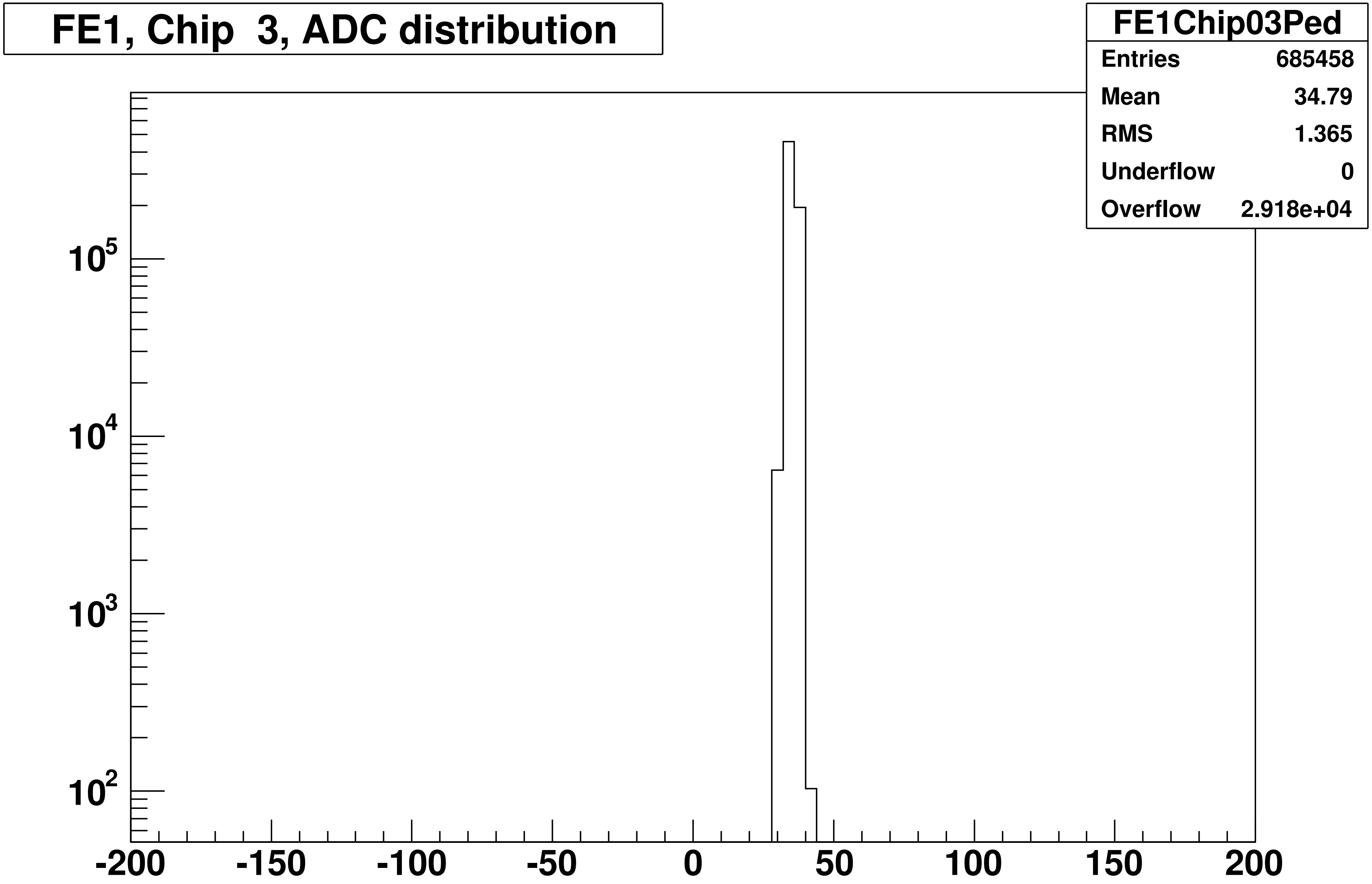
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000



FE1, Chip 3, ADC distribution
FE1Chip03Ped
Entries 685458
Mean 34.79
RMS 1.365
Underflow 0
Overflow 2.918e+04
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10^4
10^3
10^2
-200
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-100
-50
0
50
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150
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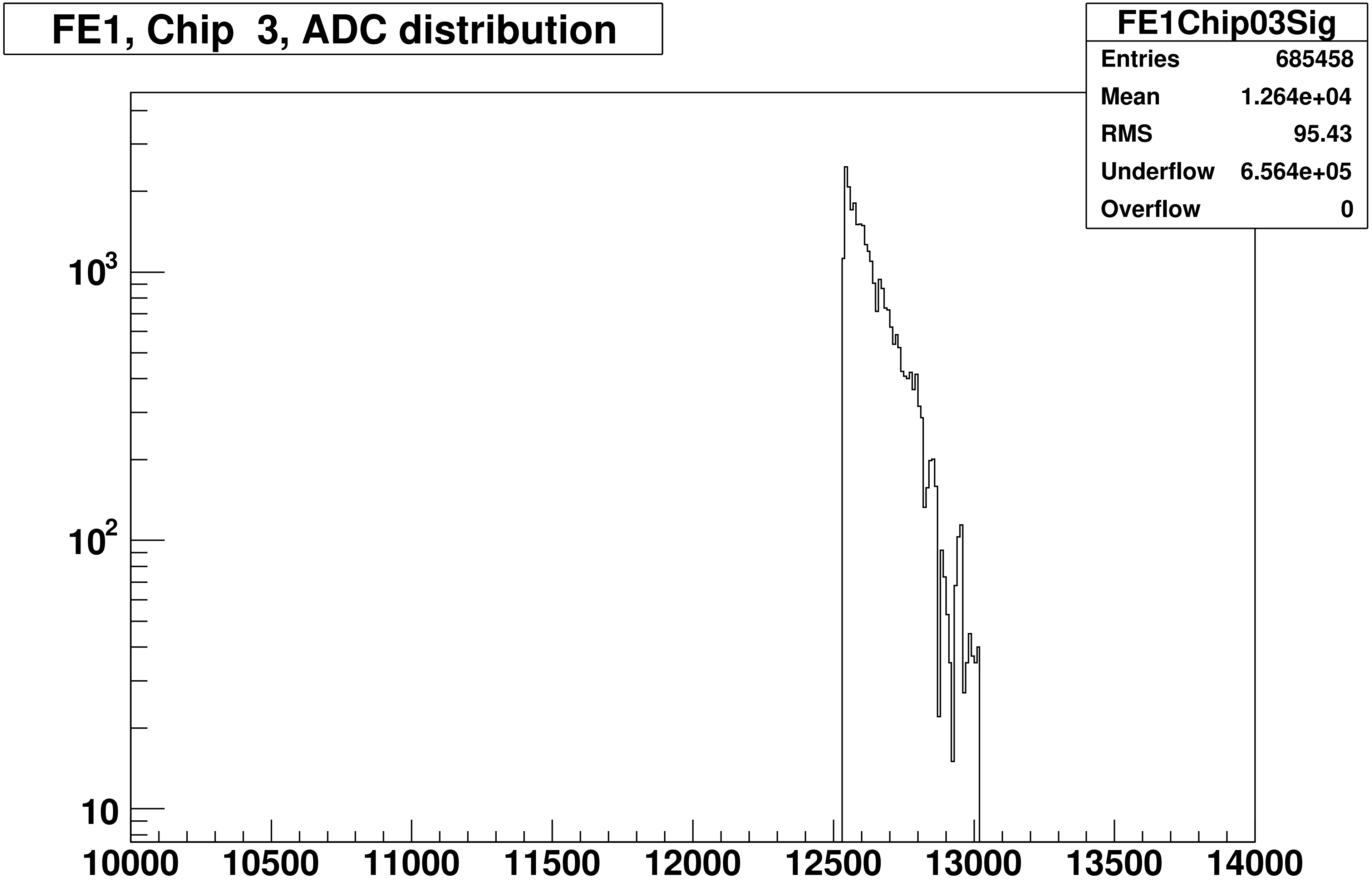

FE1, Chip 3, ADC distribution
FE1Chip03Sig
Entries 685458
Mean 1.264e+04
RMS 95.43
Underflow 6.564e+05
Overflow 0
10^3
10^2
10
10000
10500
11000
11500
12000
12500
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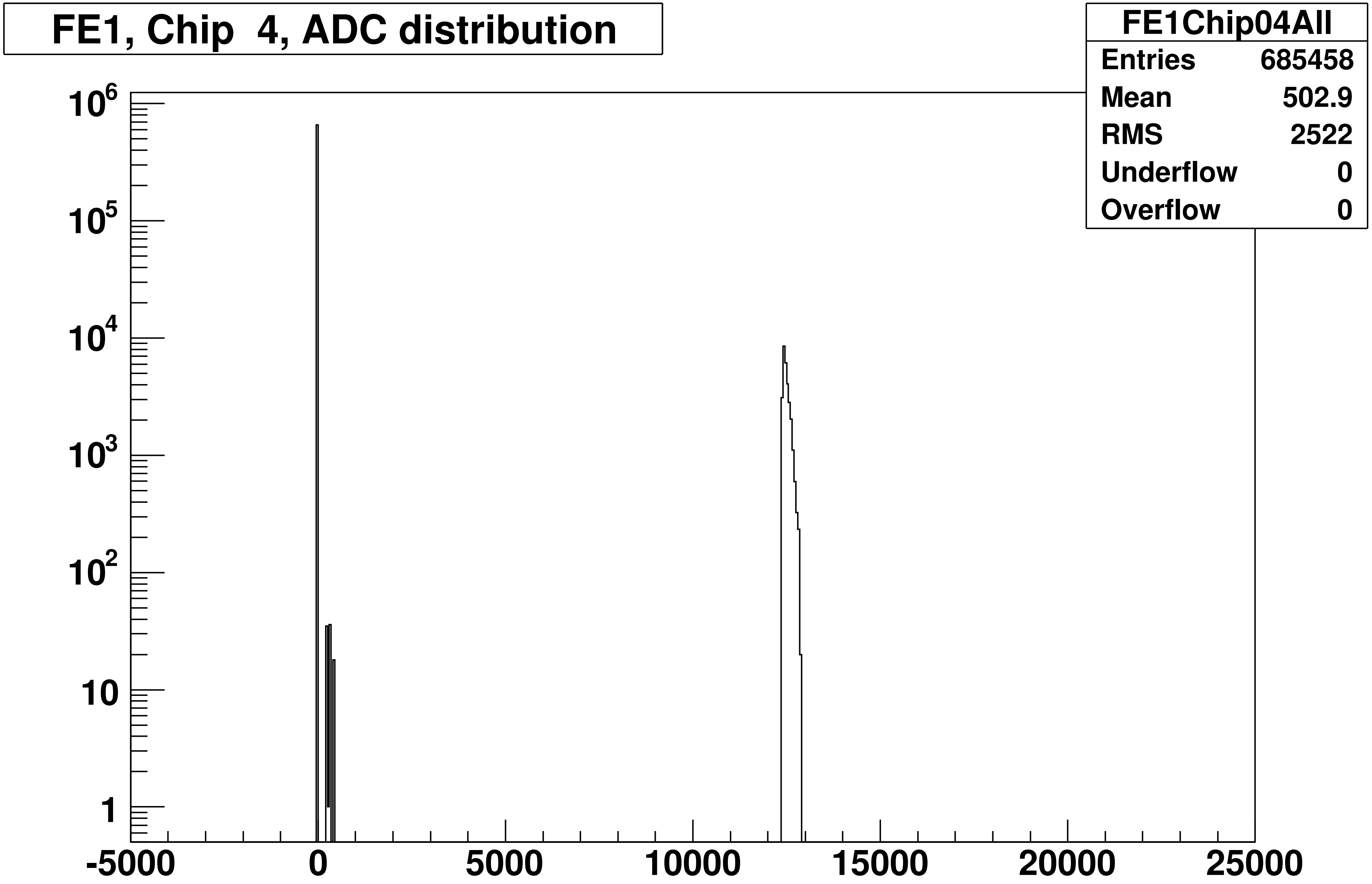
FE1, Chip 4, ADC distribution
FE1Chip04All
Entries 685458
Mean 502.9
RMS 2522
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
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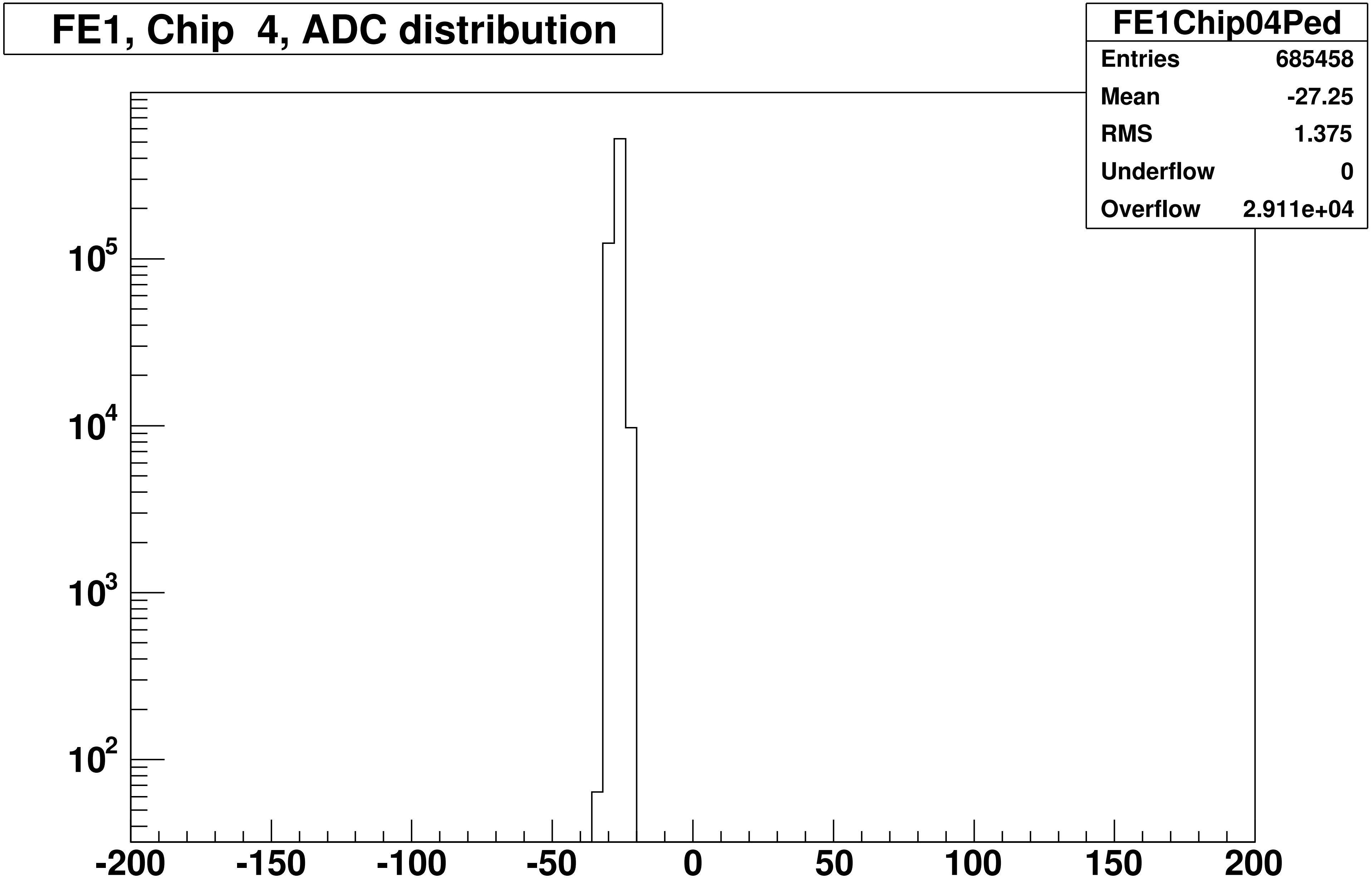
10000
15000
20000
25000


FE1, Chip 4, ADC distribution
FE1Chip04Ped
Entries 685458
Mean -27.25
RMS 1.375
Underflow 0
Overflow 2.911e+04
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10^4
10^3
10^2
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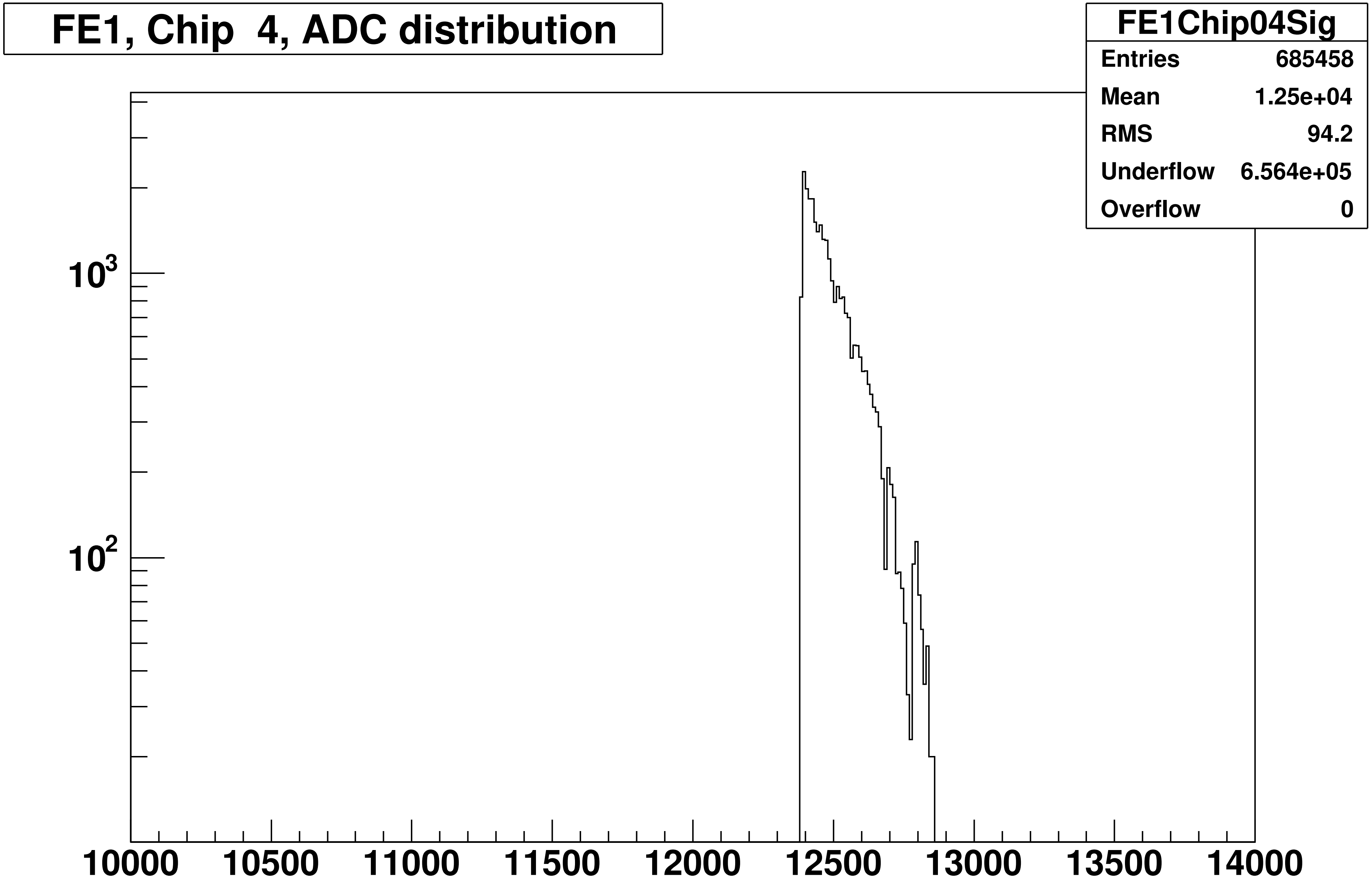
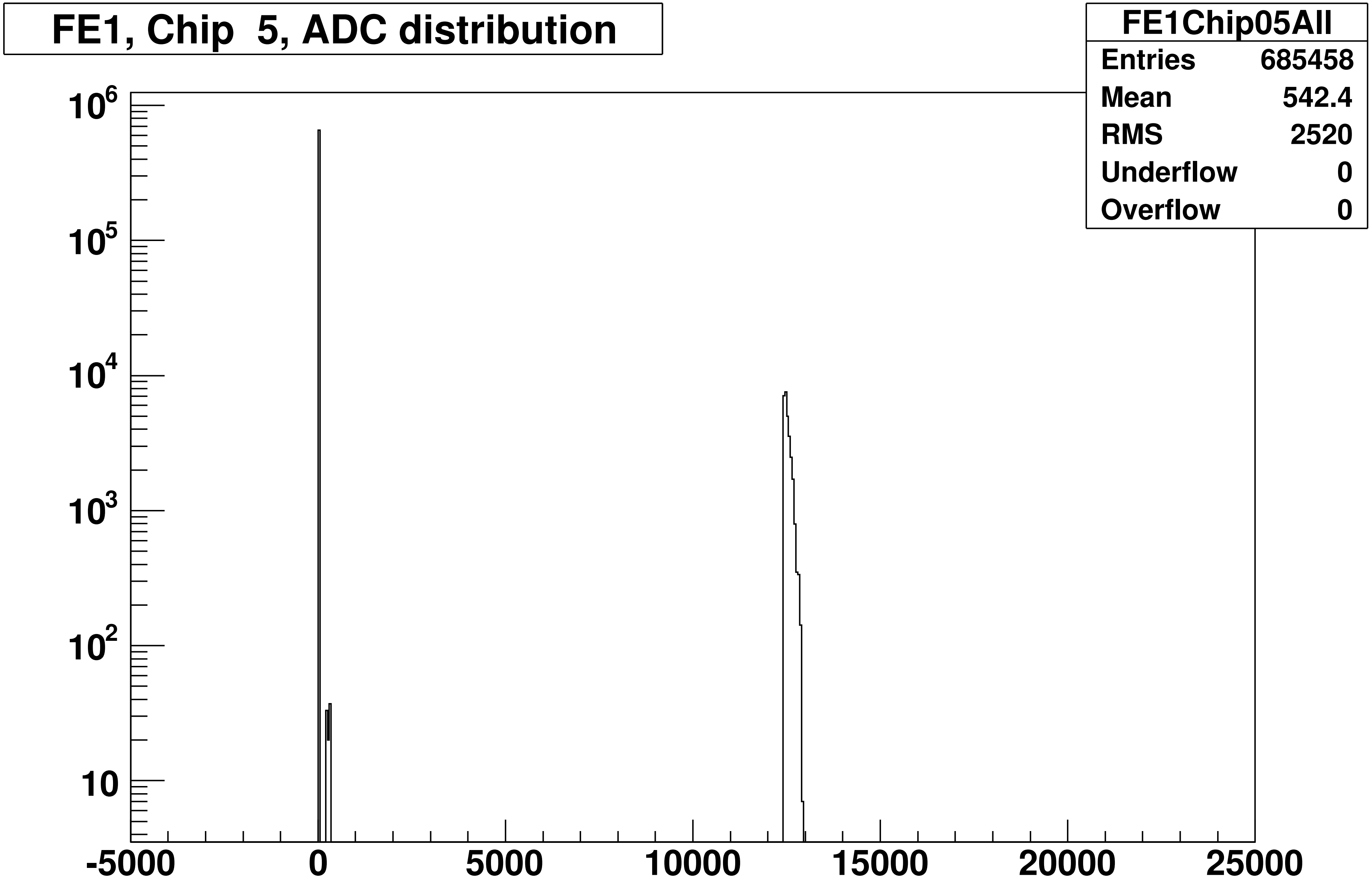
150
200


FE1, Chip 4, ADC distribution
FE1Chip04Sig
Entries 685458
Mean 1.25e+04
RMS 94.2
Underflow 6.564e+05
Overflow 0
10^3
10^2
10000
10500
11000
11500
12000
12500
13000
13500
14000


FE1, Chip 5, ADC distribution
FE1Chip05All
Entries 685458
Mean 542.4
RMS 2520
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
-5000
0
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10000
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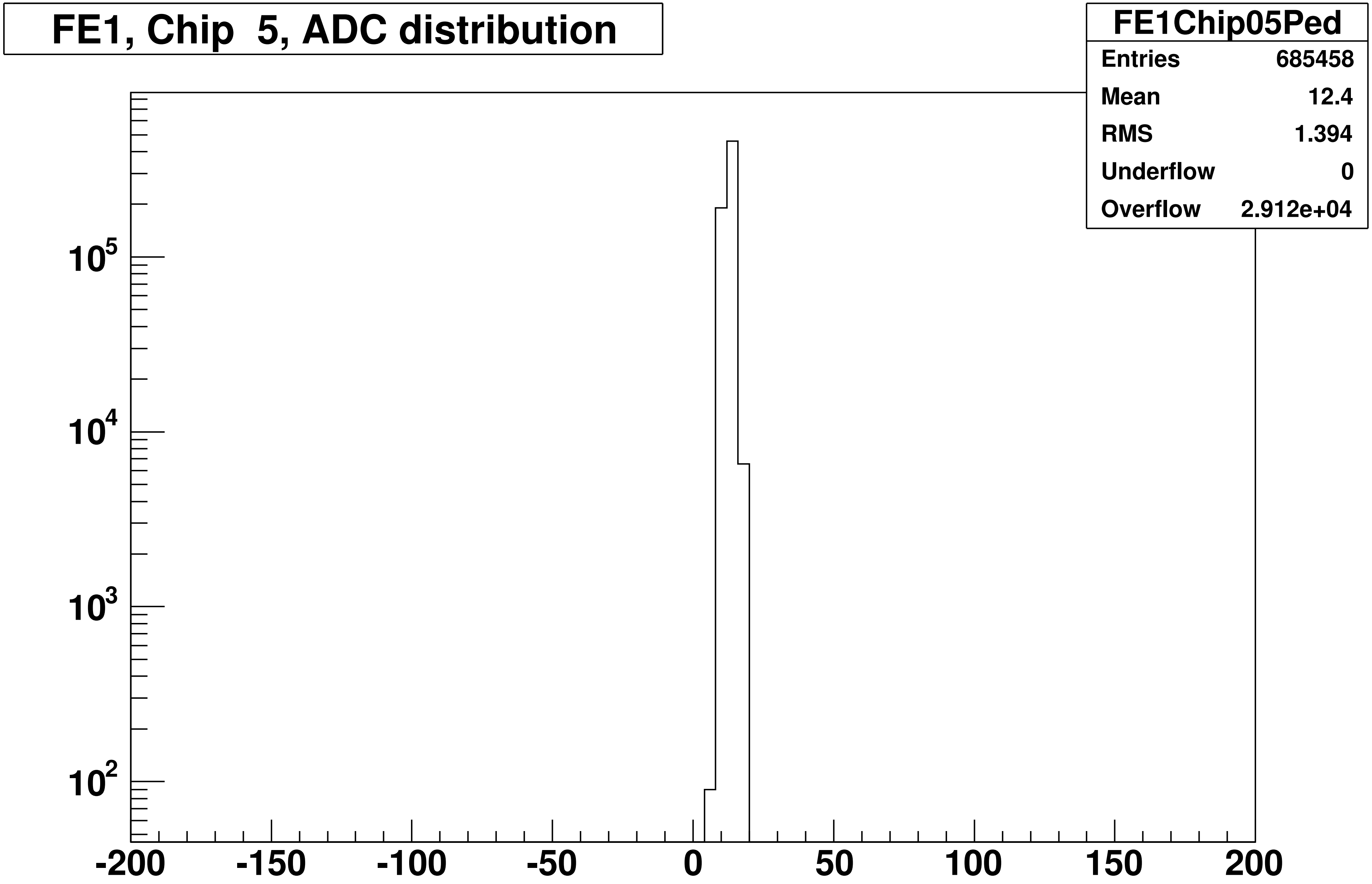
25000


FE1, Chip 5, ADC distribution
FE1Chip05Ped
Entries 685458
Mean 12.4
RMS 1.394
Underflow 0
Overflow 2.912e+04
10^5
10^4
10^3
10^2
-200
-150
-100
-50
0
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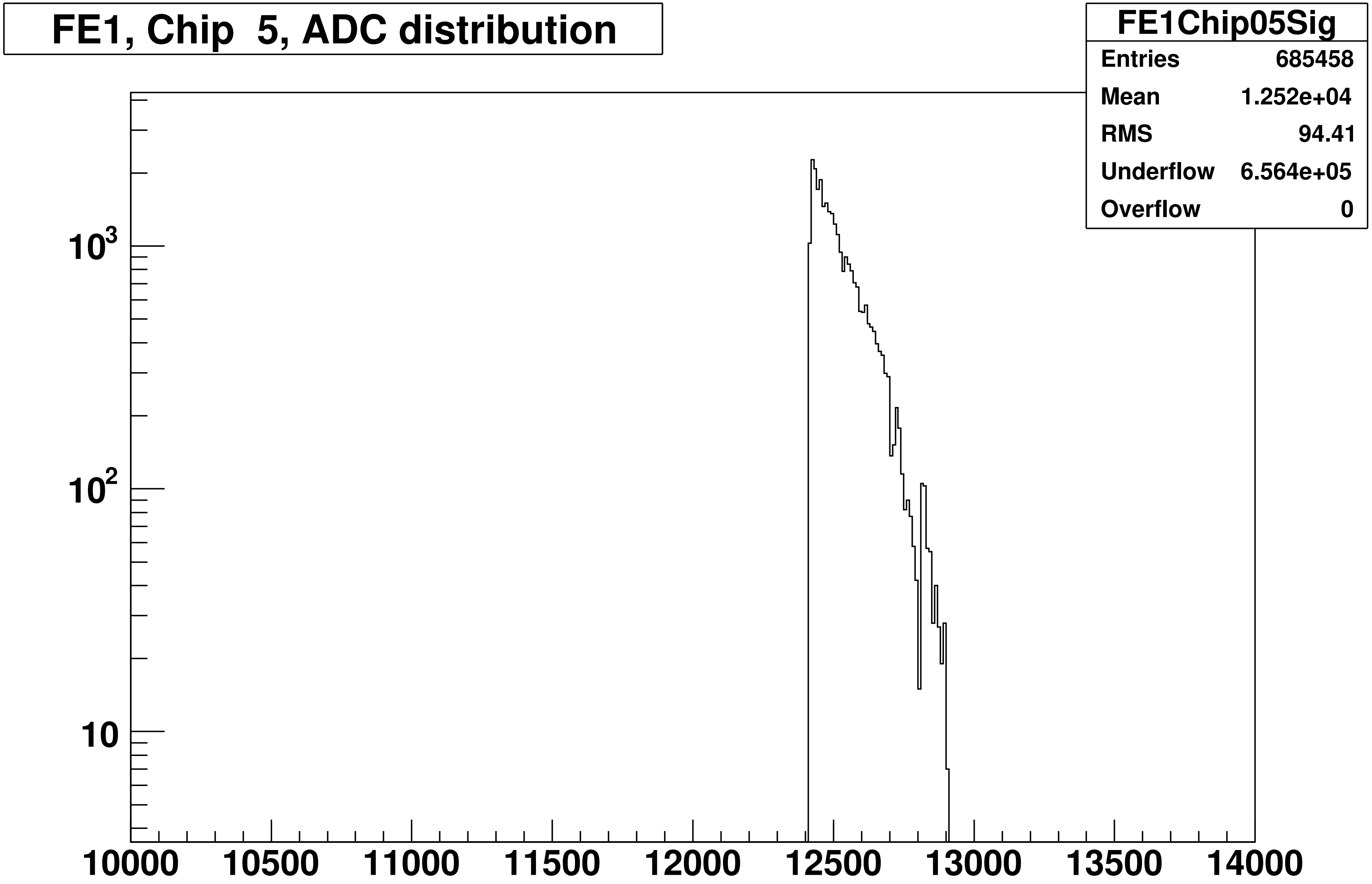
100
150
200


FE1, Chip 5, ADC distribution
FE1Chip05Sig
Entries 685458
Mean 1.252e+04
RMS 94.41
Underflow 6.564e+05
Overflow 0
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10^2
10
10000
10500
11000
11500
12000
12500
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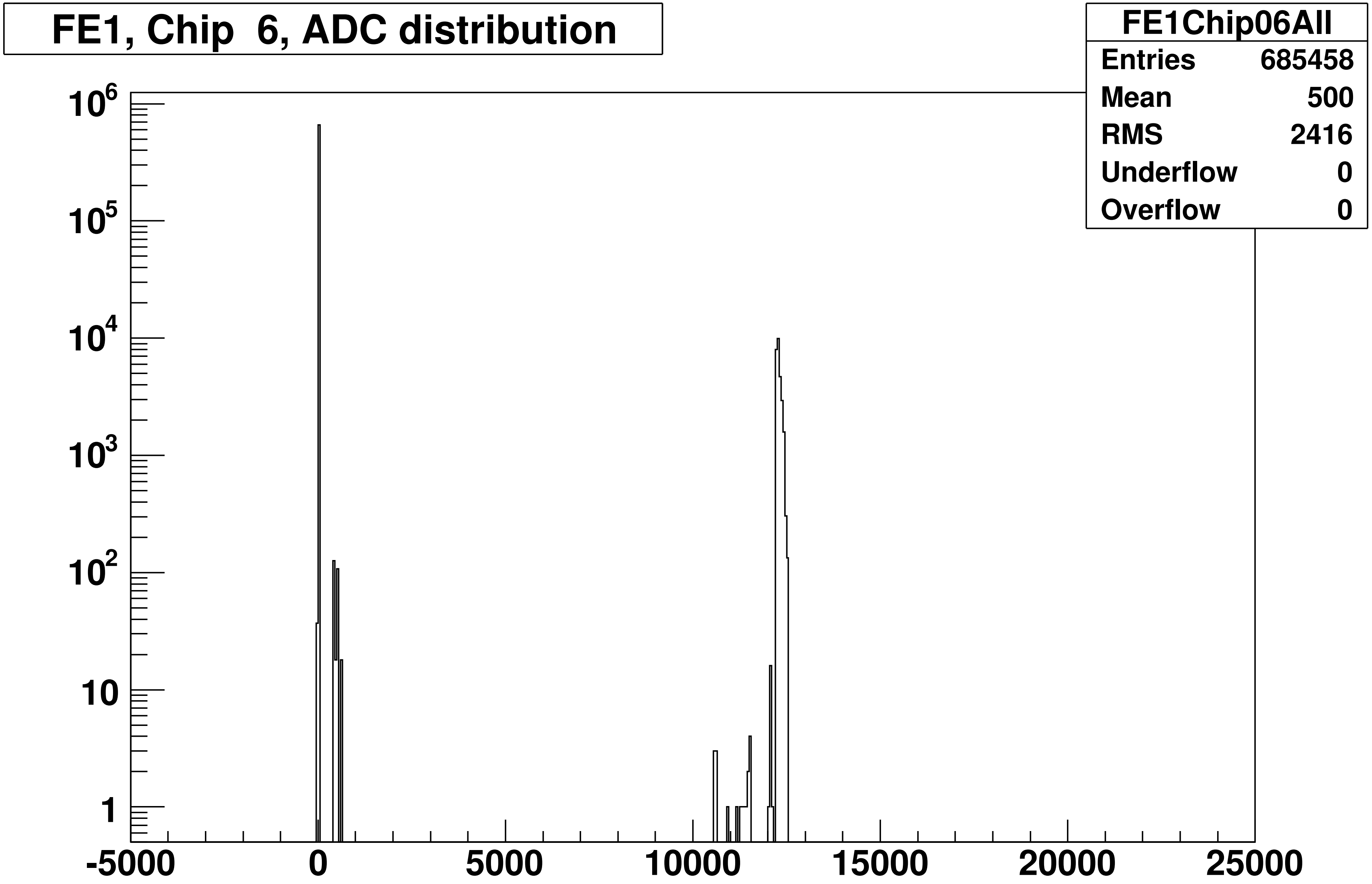
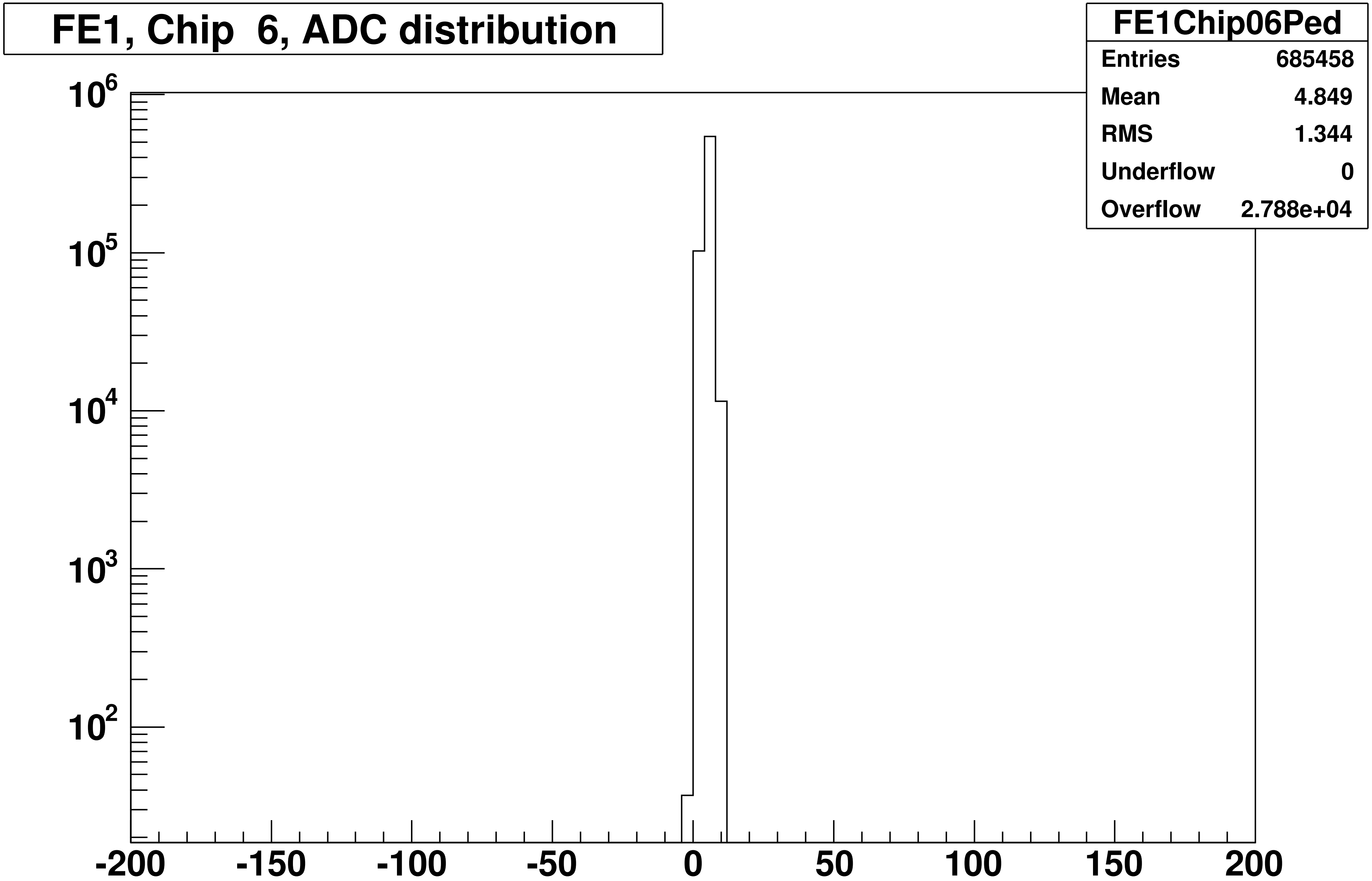
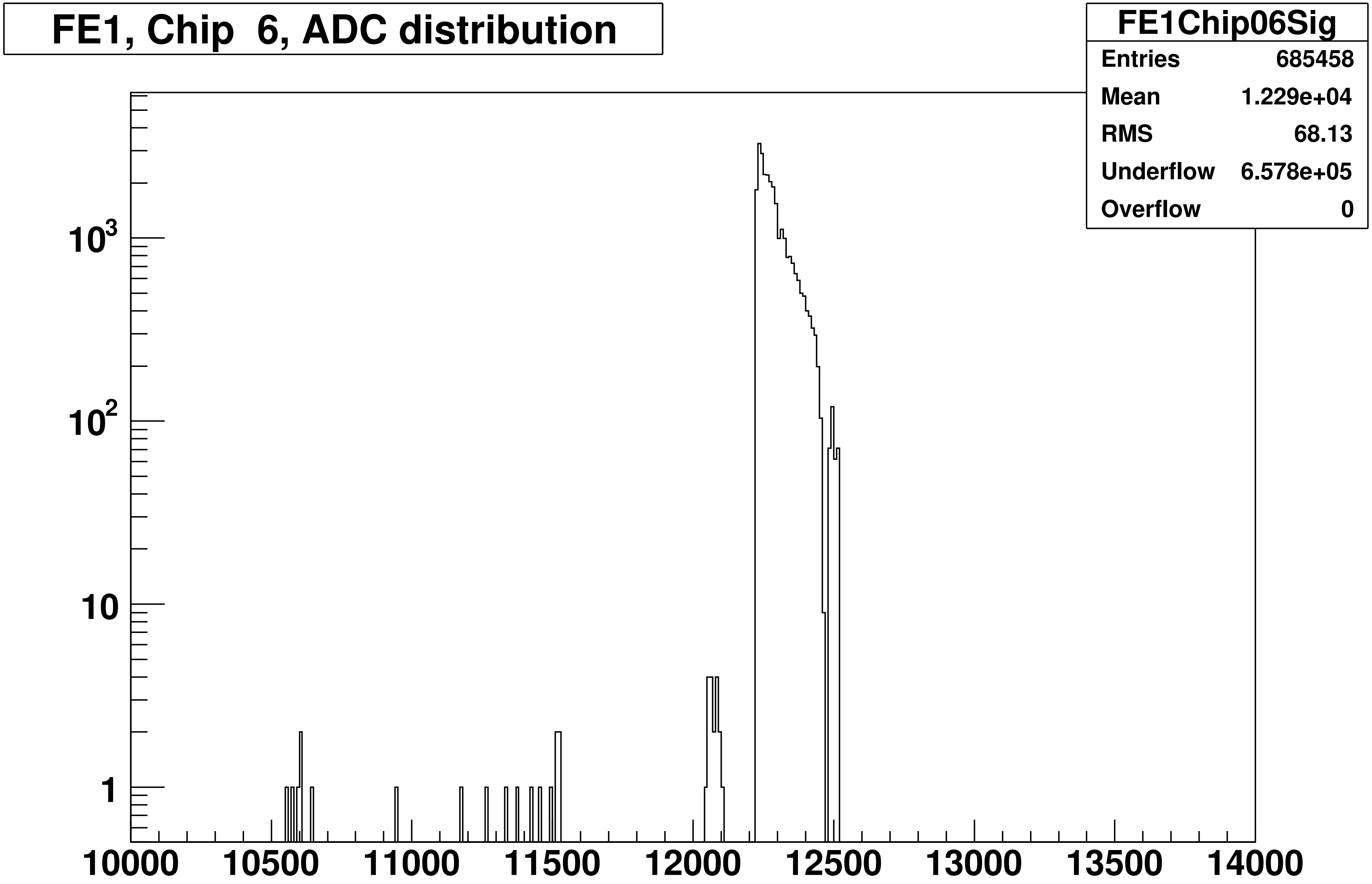
14000


FE1, Chip 6, ADC distribution
FE1Chip06All
Entries 685458
Mean 500
RMS 2416
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE1, Chip 6, ADC distribution
FE1Chip06Ped
Entries 685458
Mean 4.849
RMS 1.344
Underflow 0
Overflow 2.788e+04
10^6
10^5
10^4
10^3
10^2
-200
-150
-100
-50
0
50
100
150
200


FE1, Chip 6, ADC distribution
FE1Chip06Sig
Entries 685458
Mean 1.229e+04
RMS 68.13
Underflow 6.578e+05
Overflow 0
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10^2
10
1
10000
10500
11000
11500
12000
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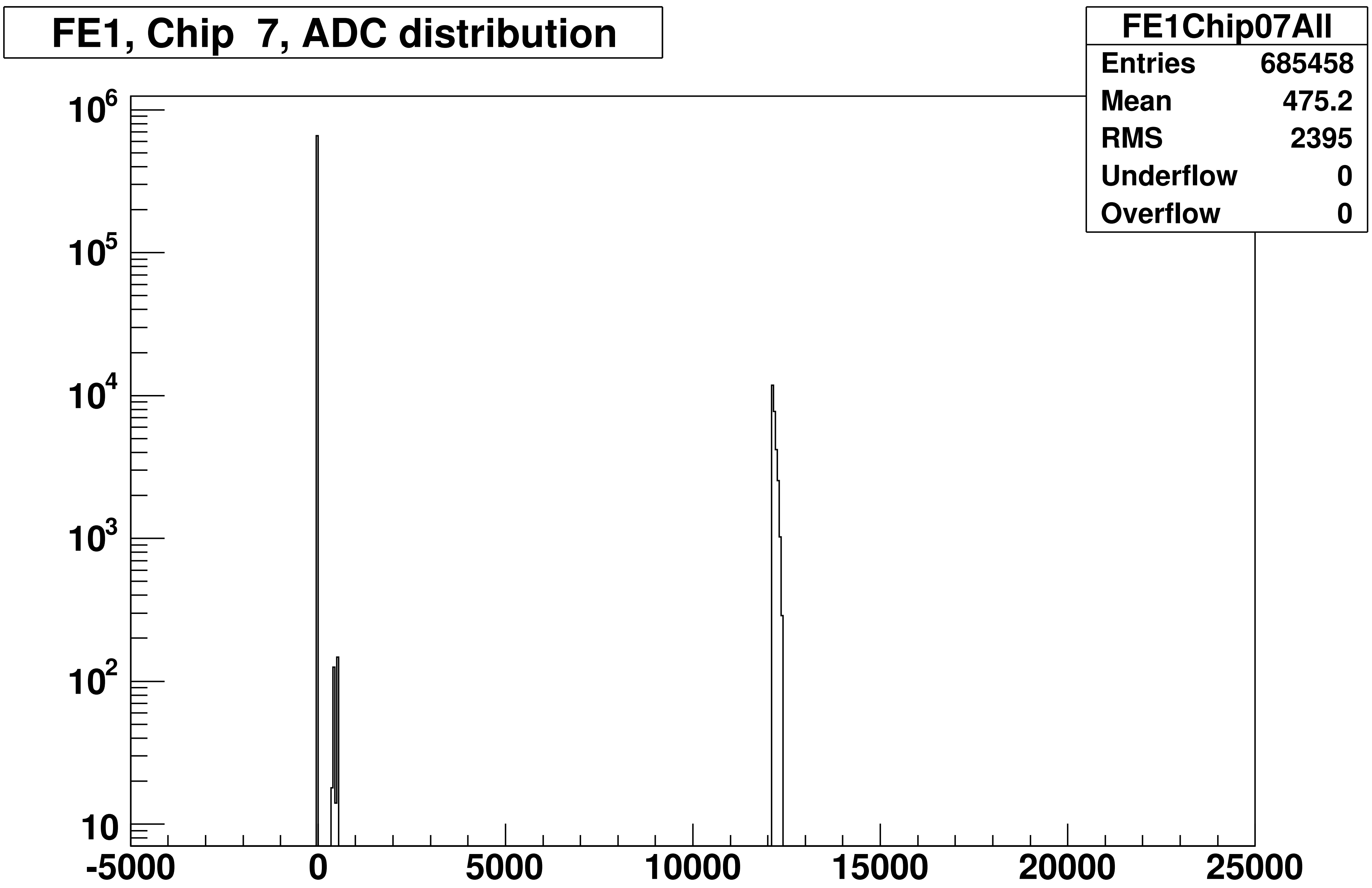
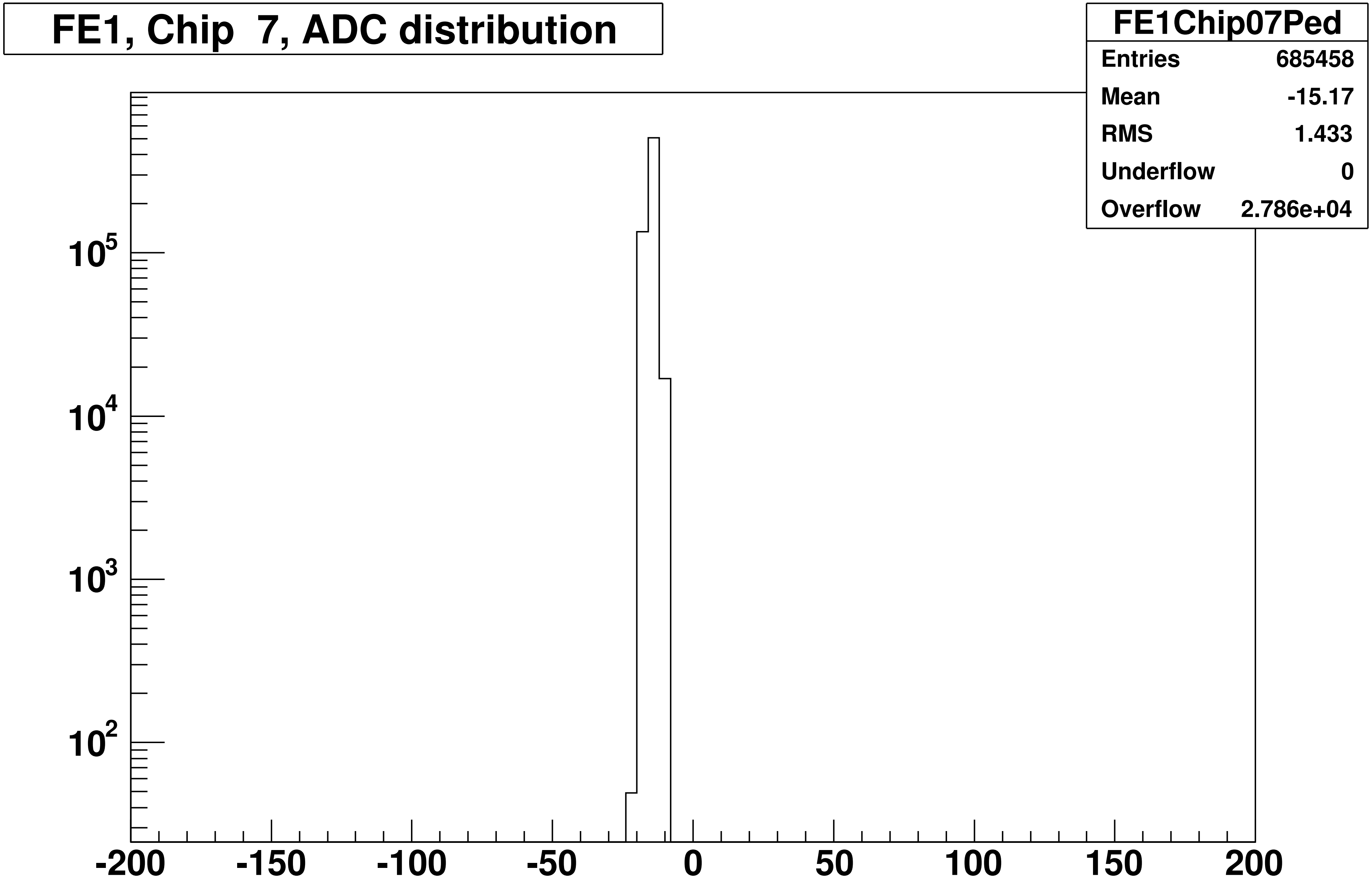
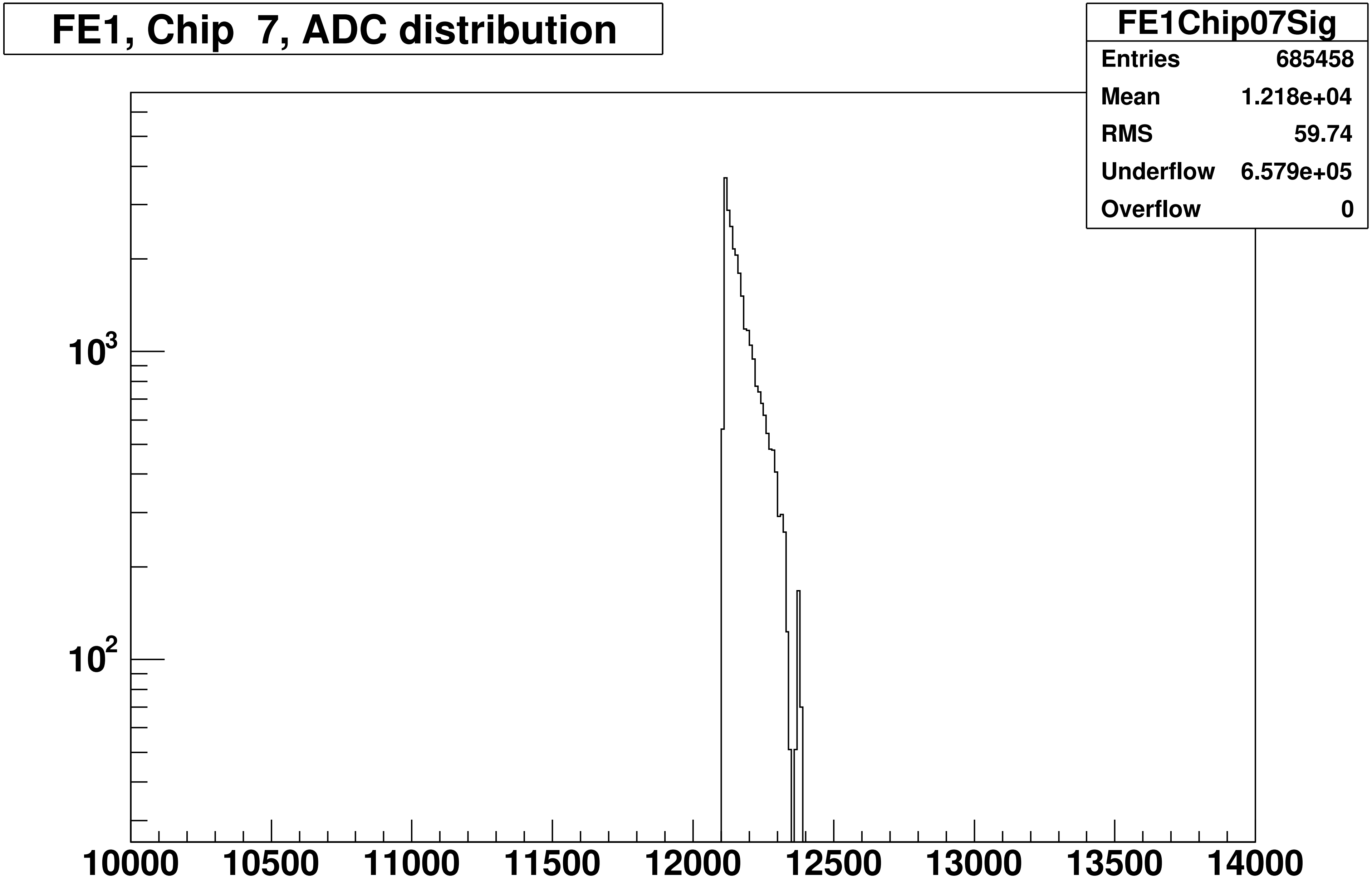

FE1, Chip 7, ADC distribution
FE1Chip07All
Entries 685458
Mean 475.2
RMS 2395
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000



FE1, Chip 7, ADC distribution
FE1Chip07Ped
Entries 685458
Mean -15.17
RMS 1.433
Underflow 0
Overflow 2.786e+04
10^5
10^4
10^3
10^2
-200
-150
-100
-50
0
50
100
150
200


FE1, Chip 7, ADC distribution
FE1Chip07Sig
Entries 685458
Mean 1.218e+04
RMS 59.74
Underflow 6.579e+05
Overflow 0
10^3
10^2
10000
10500
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11500
12000
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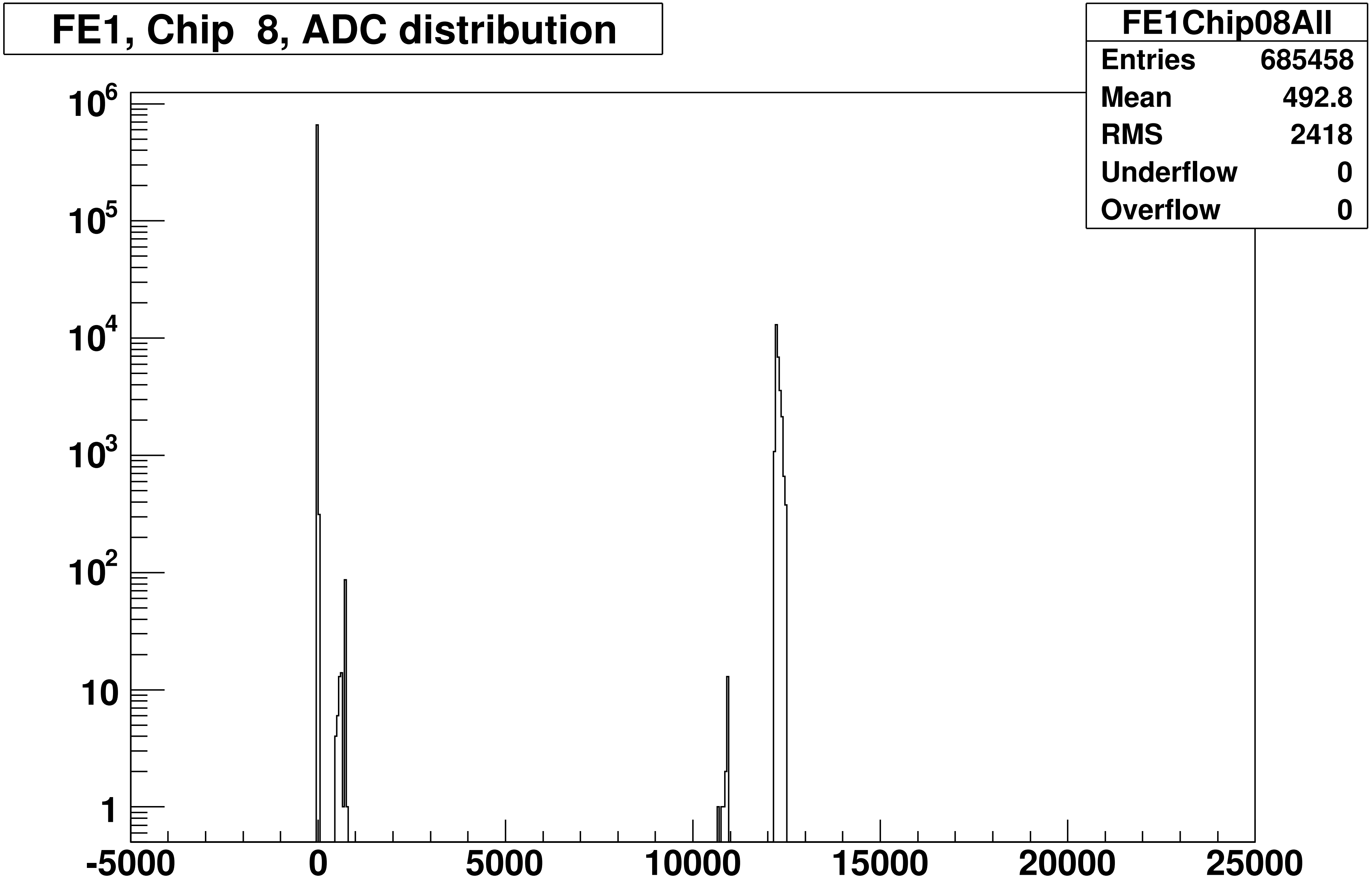
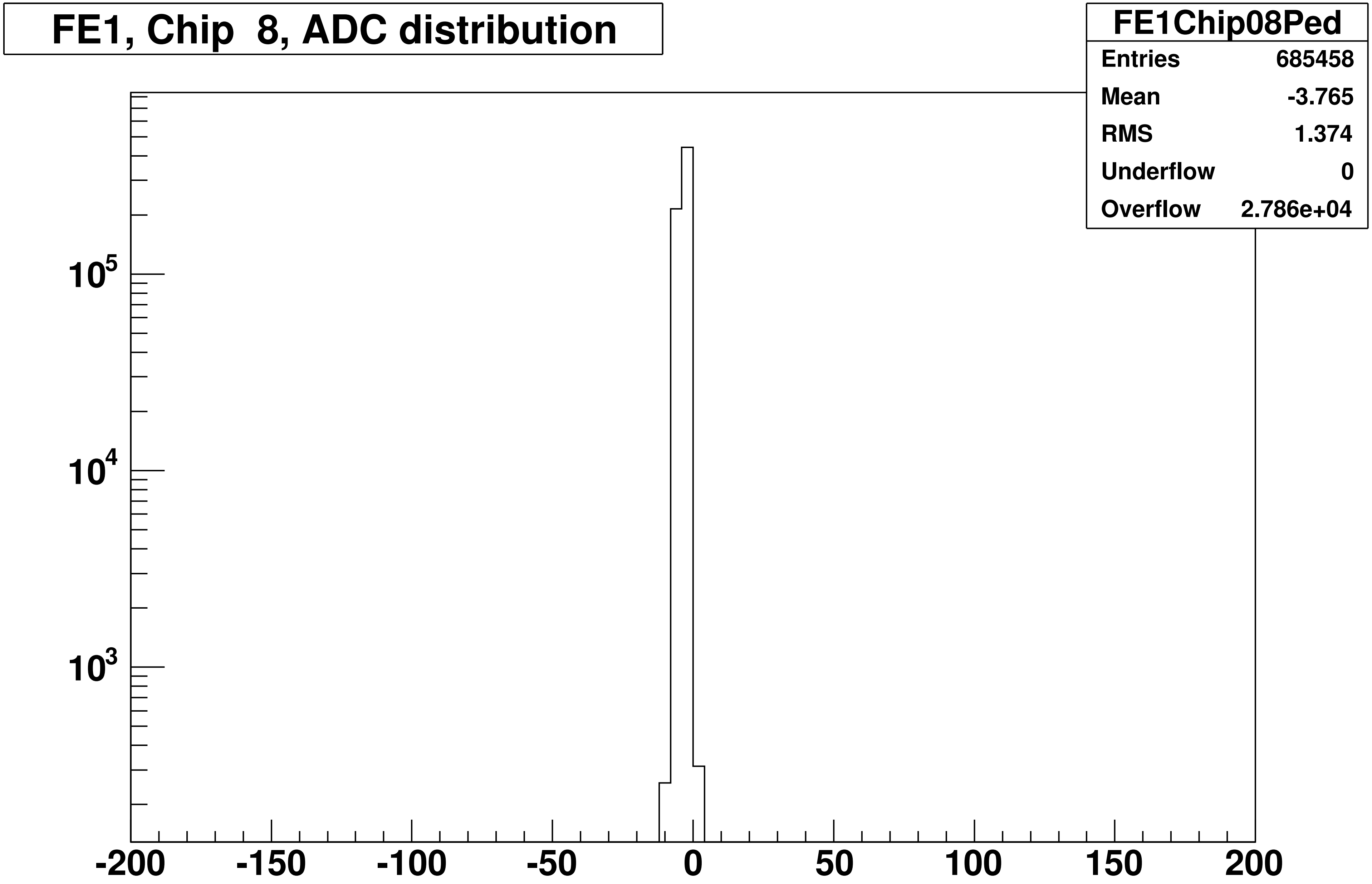
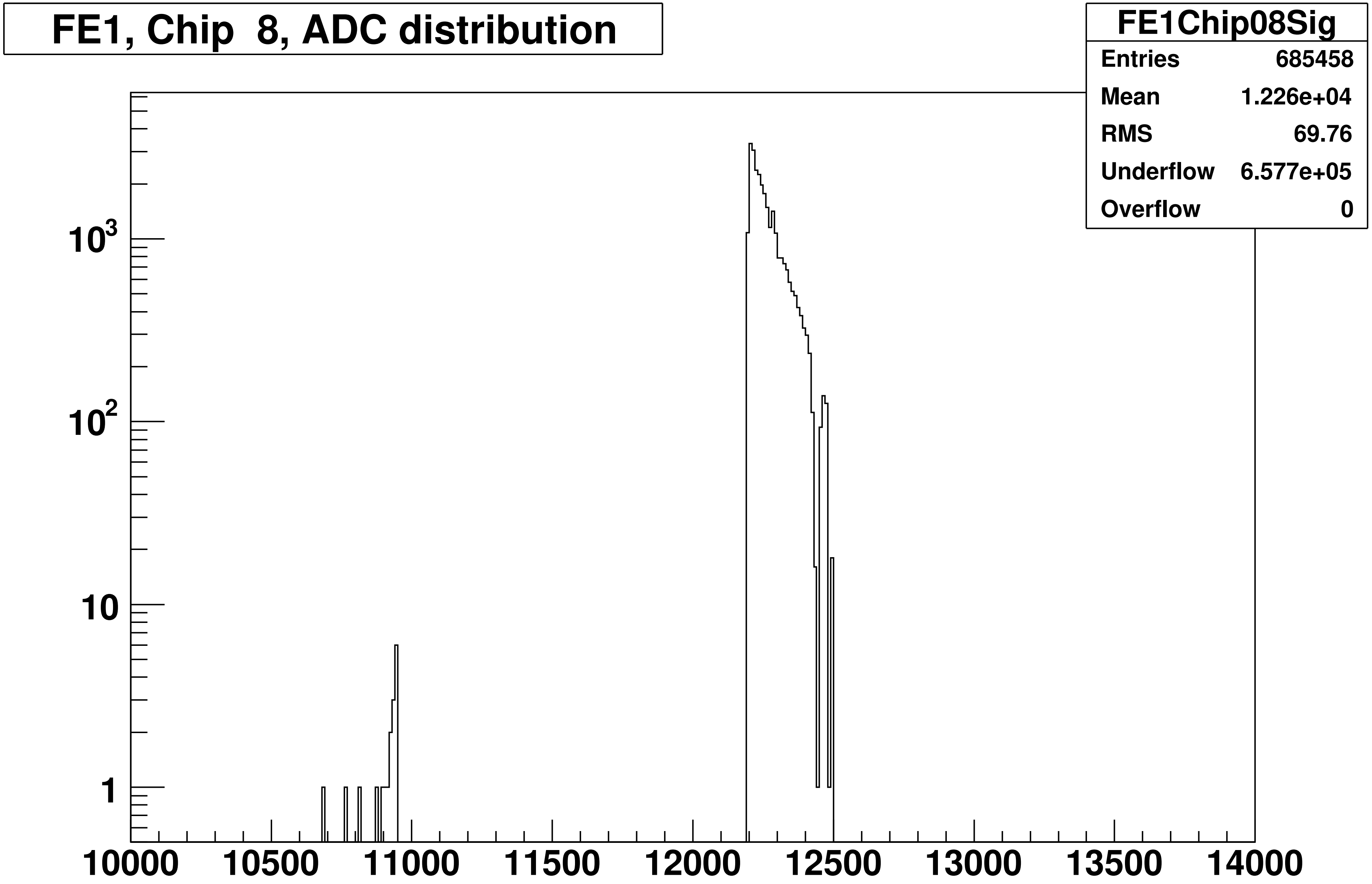
13500
14000

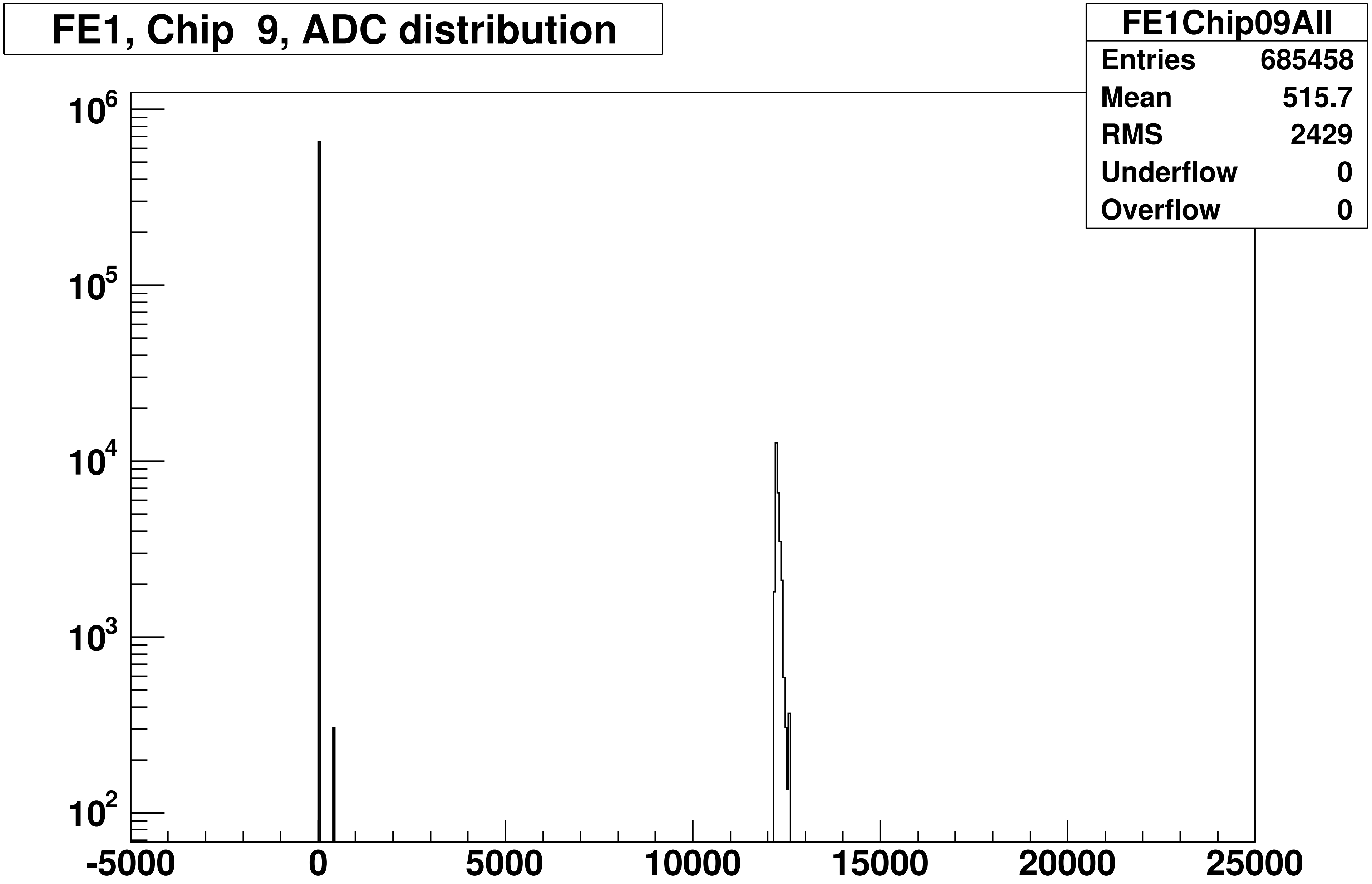

FE1, Chip 8, ADC distribution
FE1Chip08All
Entries 685458
Mean 492.8
RMS 2418
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



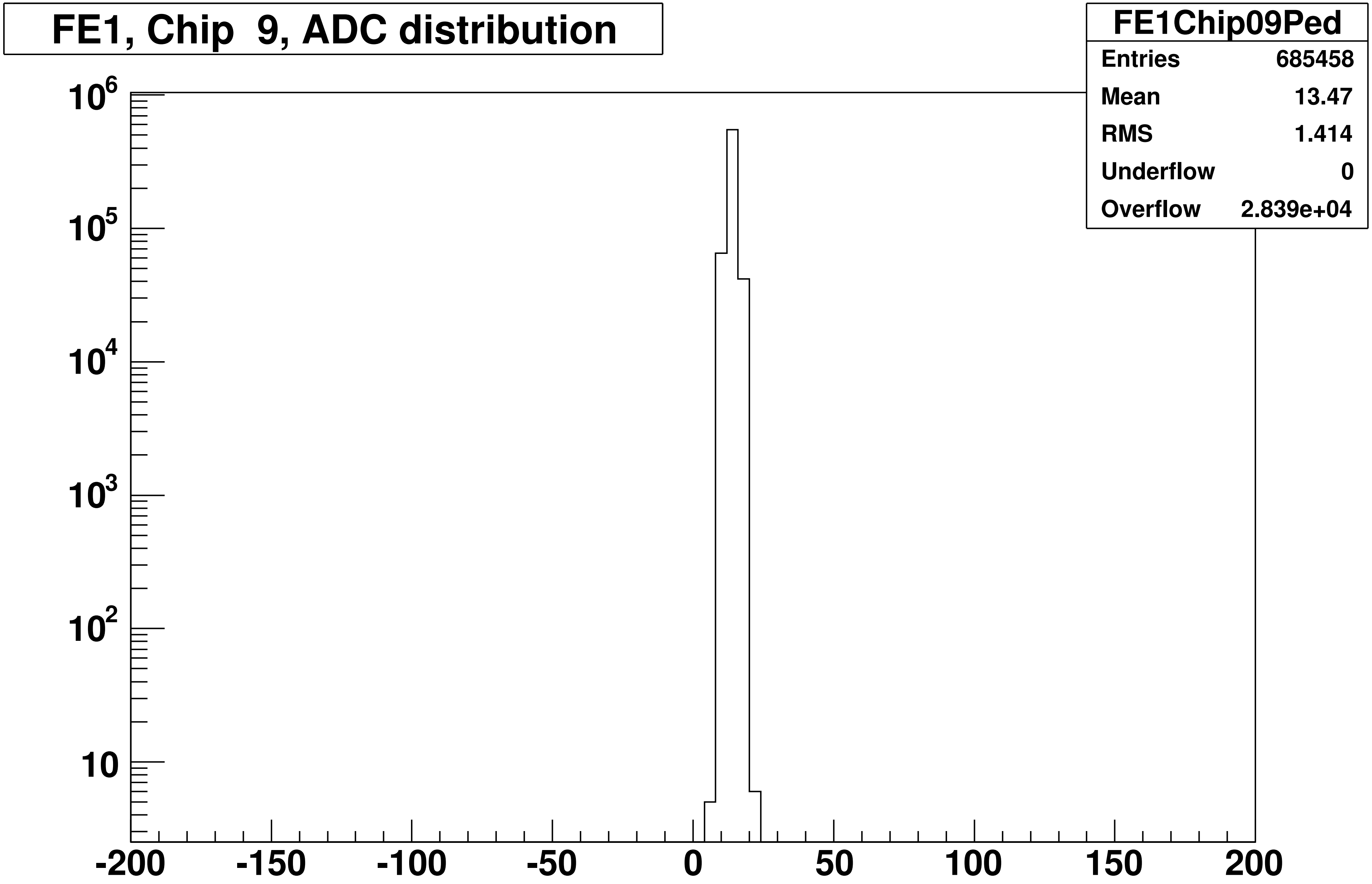
FE1, Chip 8, ADC distribution
FE1Chip08Ped
Entries 685458
Mean -3.765
RMS 1.374
Underflow 0
Overflow 2.786e+04
10^5
10^4
10^3
-200 -150 -100 -50 0 50 100 150 200



FE1, Chip 8, ADC distribution
FE1Chip08Sig
Entries 685458
Mean 1.226e+04
RMS 69.76
Underflow 6.577e+05
Overflow 0
10^3
10^2
10
1
10000
10500
11000
11500
12000
12500
13000
13500
14000



FE1, Chip 9, ADC distribution
FE1Chip09All
Entries 685458
Mean 515.7
RMS 2429
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000



FE1, Chip 9, ADC distribution
FE1Chip09Ped
Entries 685458
Mean 13.47
RMS 1.414
Underflow 0
Overflow 2.839e+04
10^6
10^5
10^4
10^3
10^2
10
-200
-150
-100
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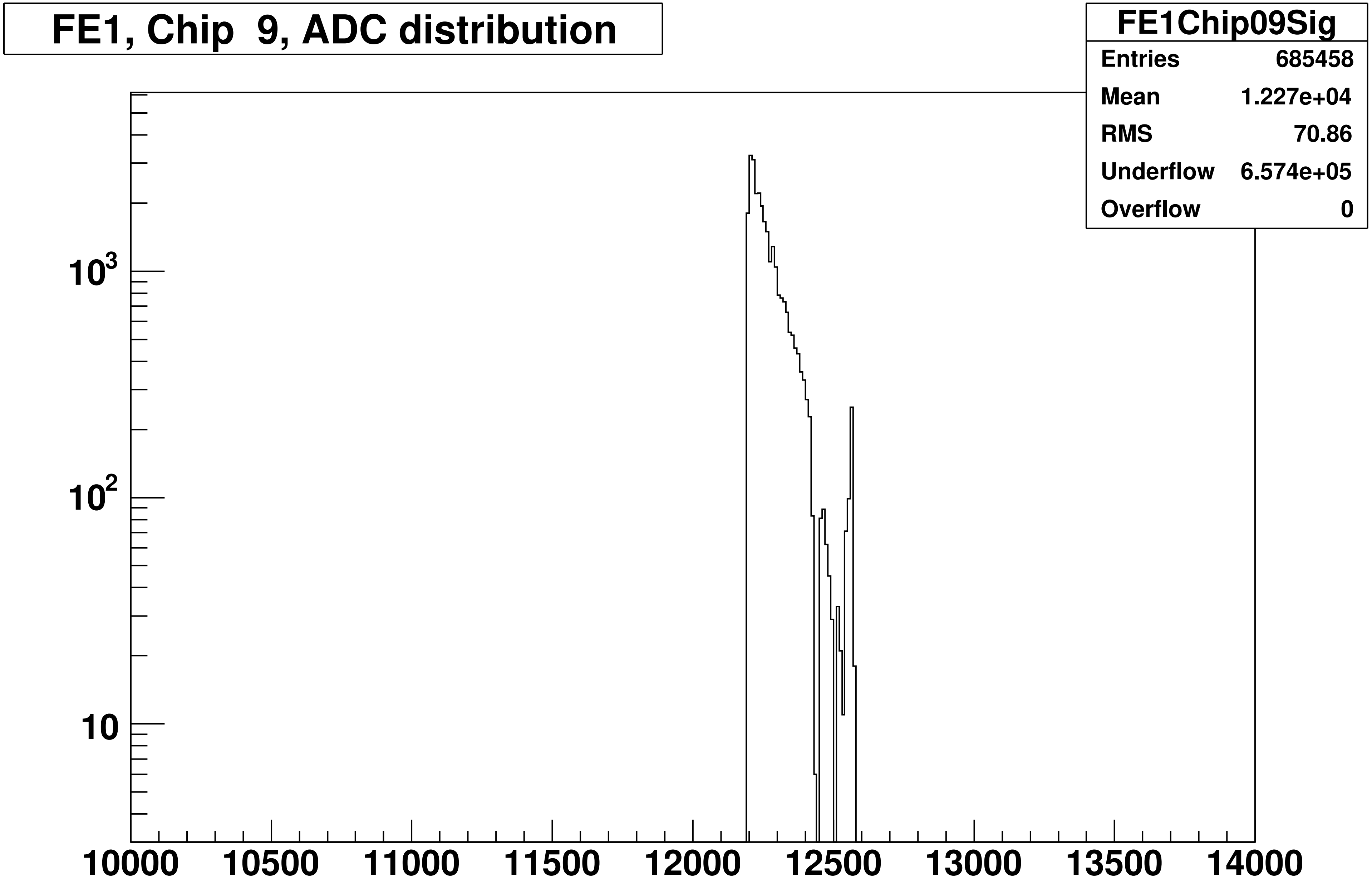
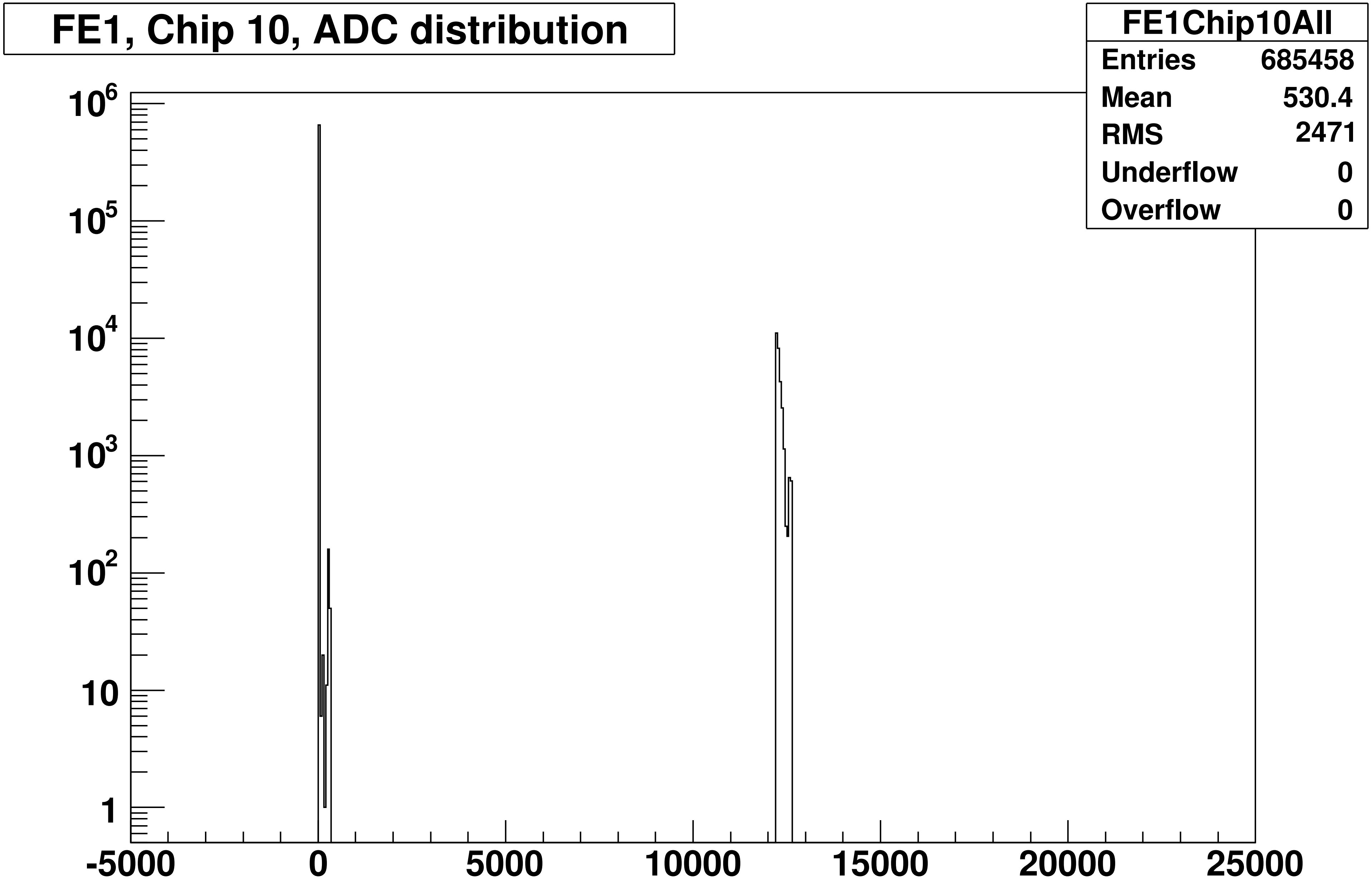
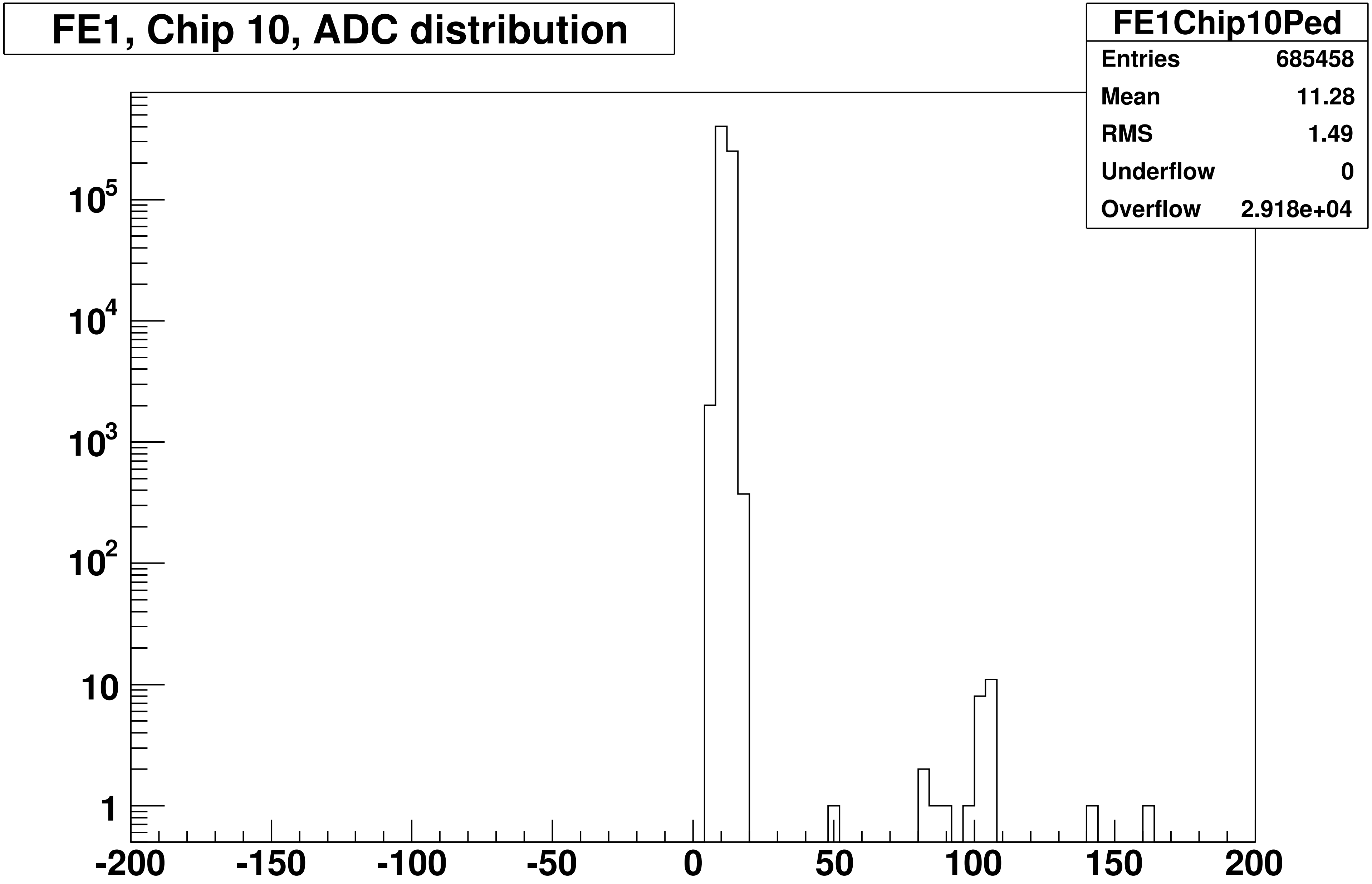
100
150
200


FE1, Chip 9, ADC distribution
FE1Chip09Sig
Entries 685458
Mean 1.227e+04
RMS 70.86
Underflow 6.574e+05
Overflow 0
10^3
10^2
10
10000
10500
11000
11500
12000
12500
13000
13500
14000



FE1, Chip 10, ADC distribution
FE1Chip10All
Entries 685458
Mean 530.4
RMS 2471
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE1, Chip 10, ADC distribution
FE1Chip10Ped
Entries 685458
Mean 11.28
RMS 1.49
Underflow 0
Overflow 2.918e+04
-200
-150
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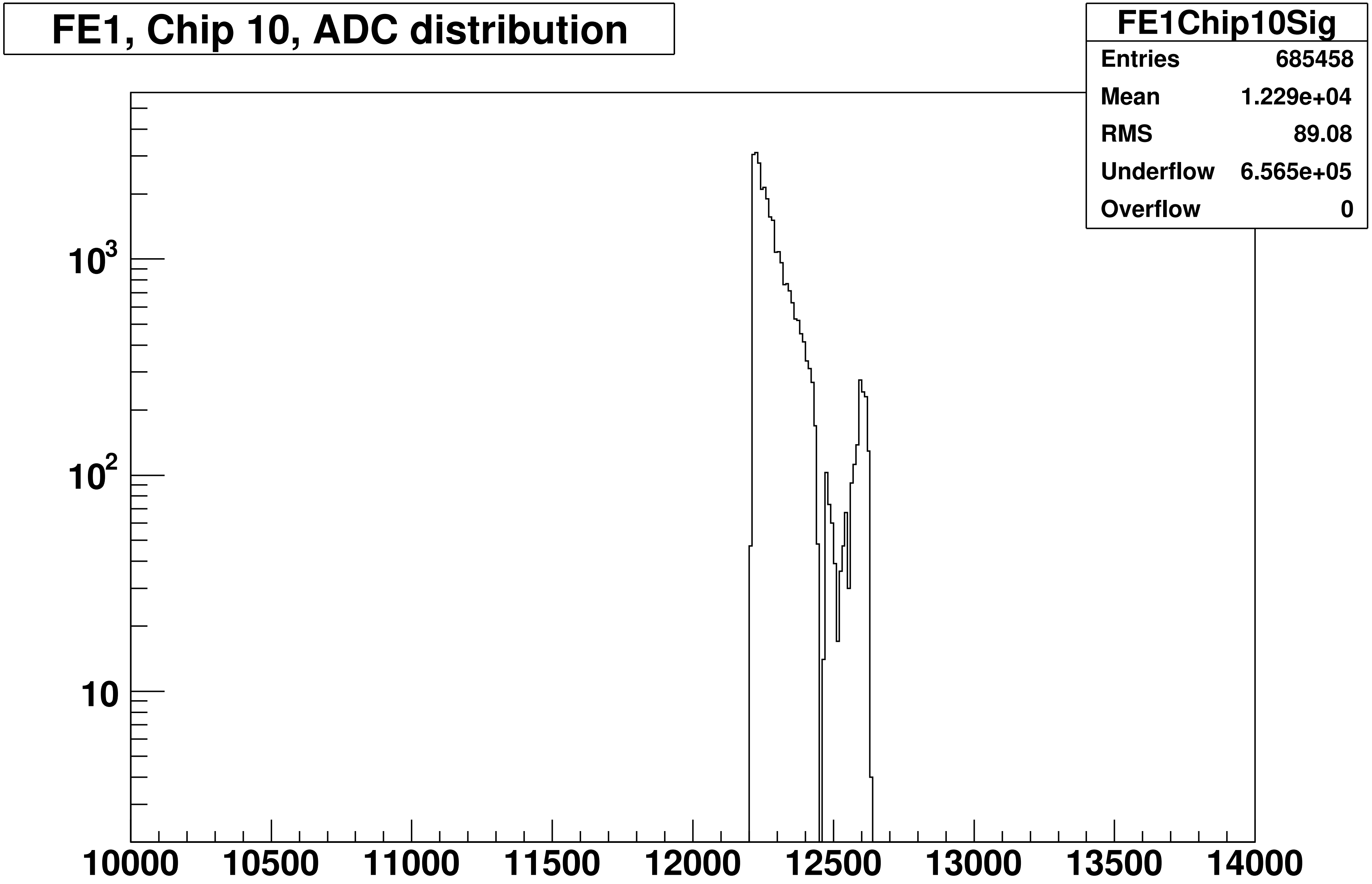
10^3
10^4
10^5


FE1, Chip 10, ADC distribution
FE1Chip10Sig
Entries 685458
Mean 1.229e+04
RMS 89.08
Underflow 6.565e+05
Overflow 0
10
10^2
10^3
10000
10500
11000
11500
12000
12500
13000
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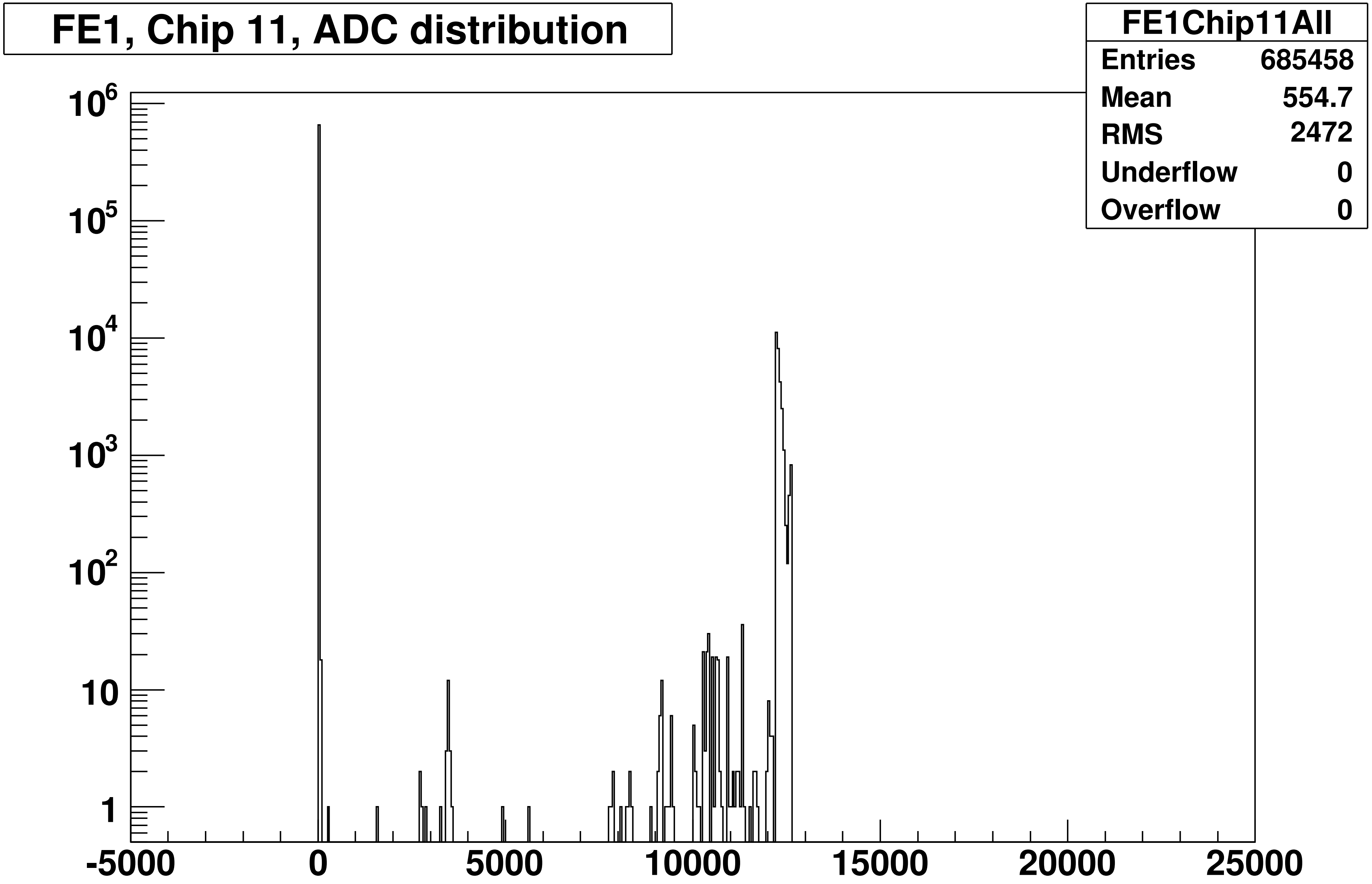
14000


FE1, Chip 11, ADC distribution
FE1Chip11All
Entries 685458
Mean 554.7
RMS 2472
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
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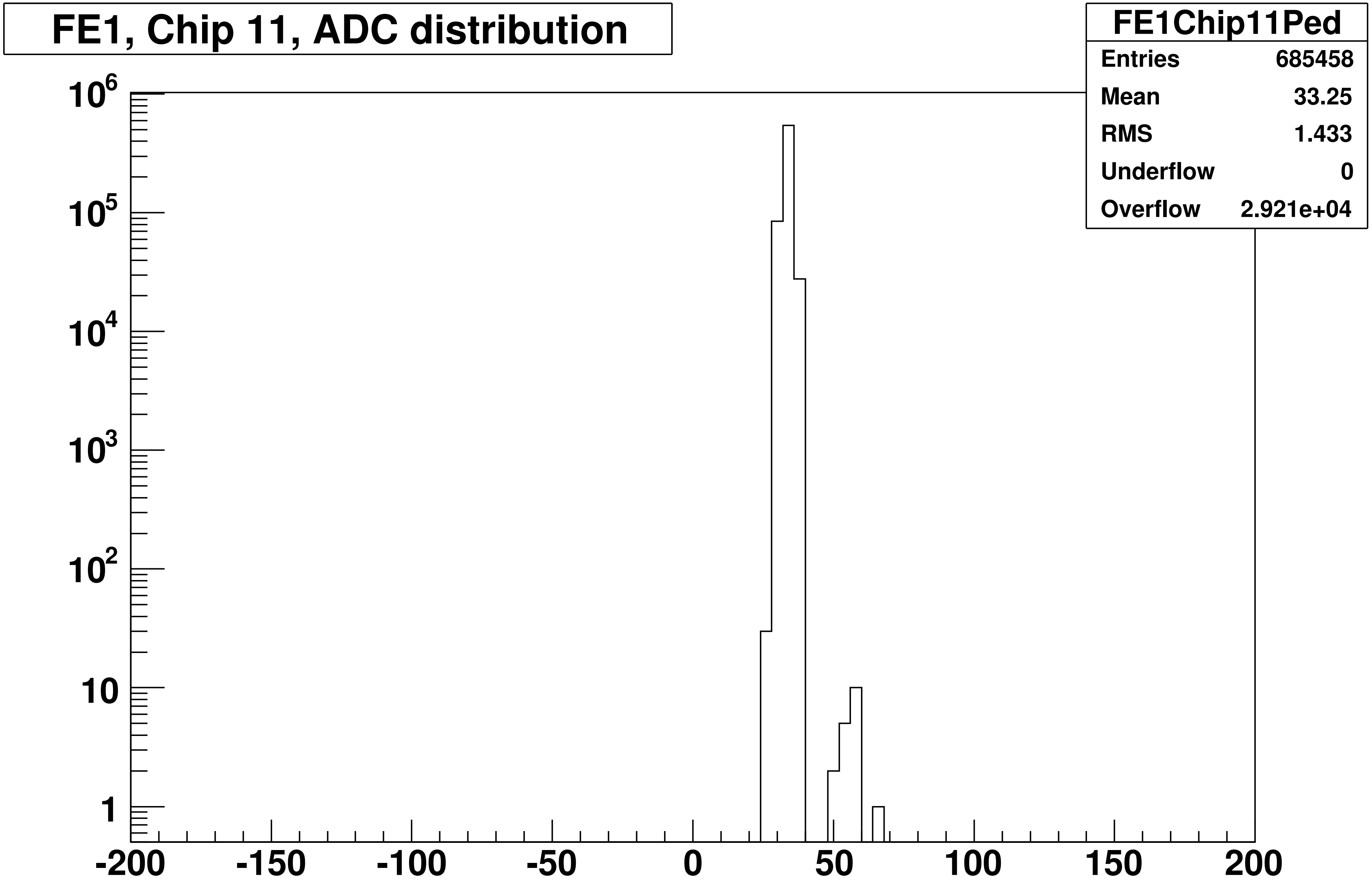
10000
15000
20000
25000


FE1, Chip 11, ADC distribution
FE1Chip11Ped
Entries 685458
Mean 33.25
RMS 1.433
Underflow 0
Overflow 2.921e+04
10^6
10^5
10^4
10^3
10^2
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1
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0
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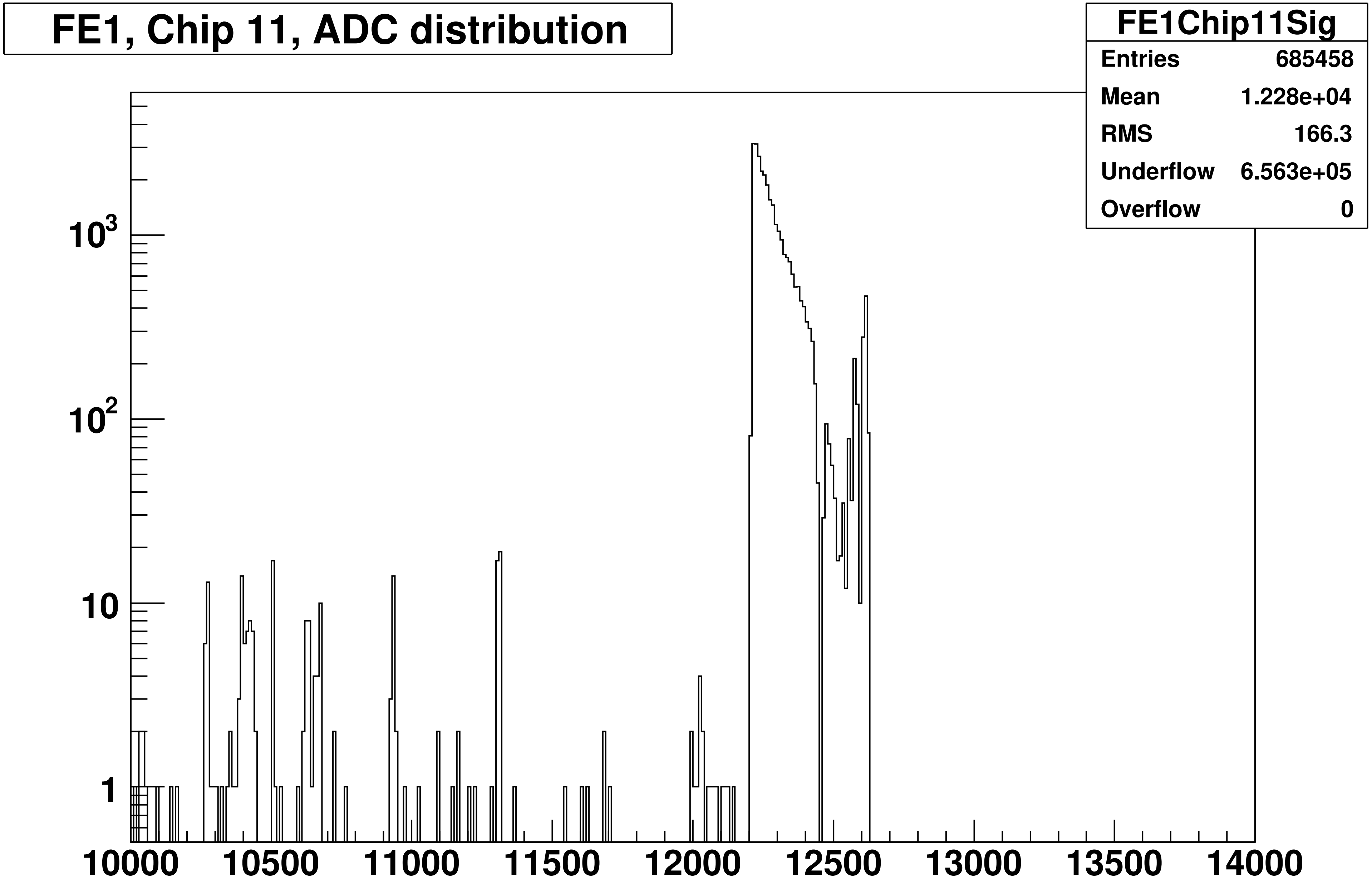
100
150
200


FE1, Chip 11, ADC distribution
FE1Chip11Sig
Entries 685458
Mean 1.228e+04
RMS 166.3
Underflow 6.563e+05
Overflow 0
10^3
10^2
10
1
10000
10500
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11500
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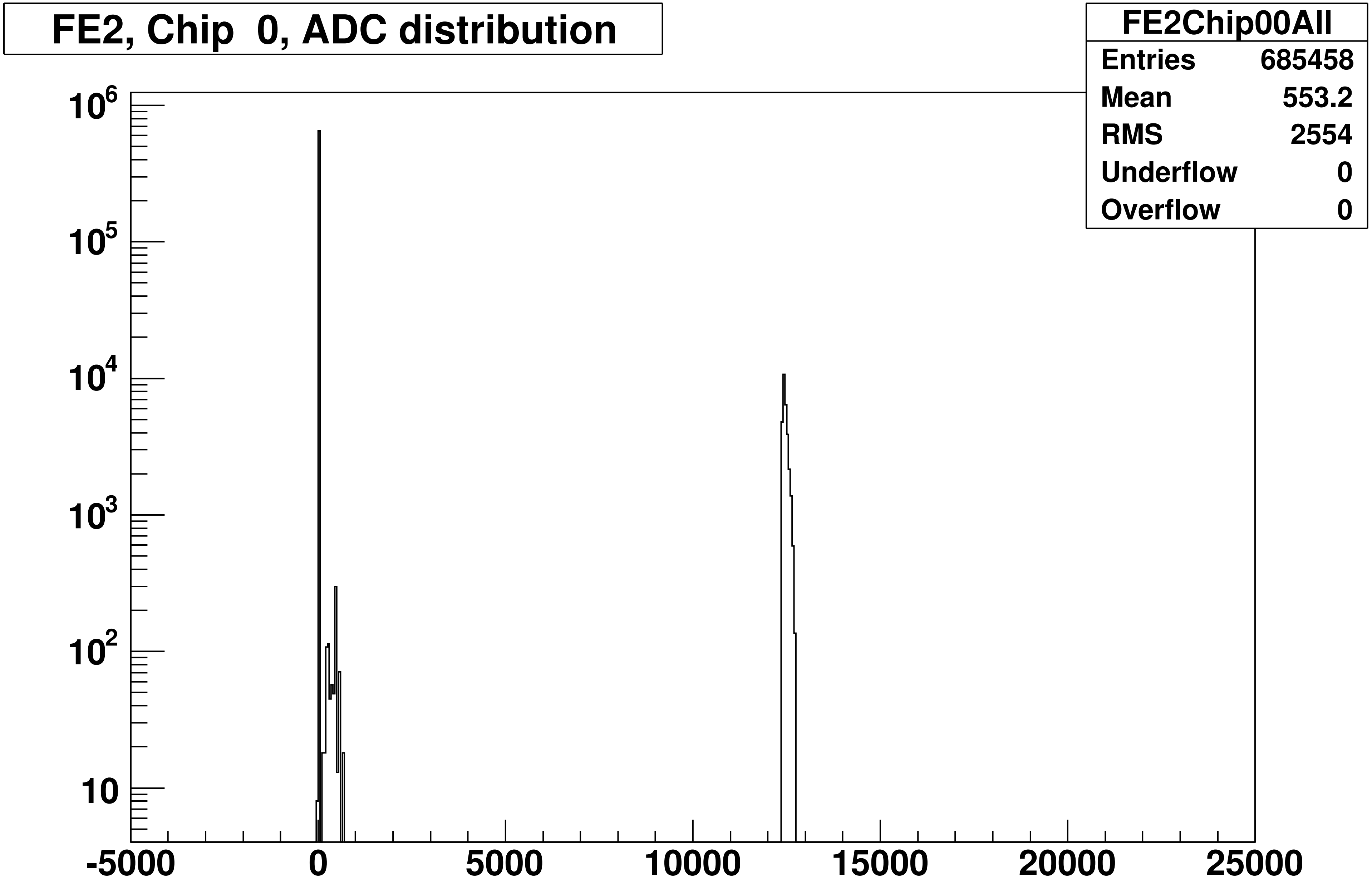
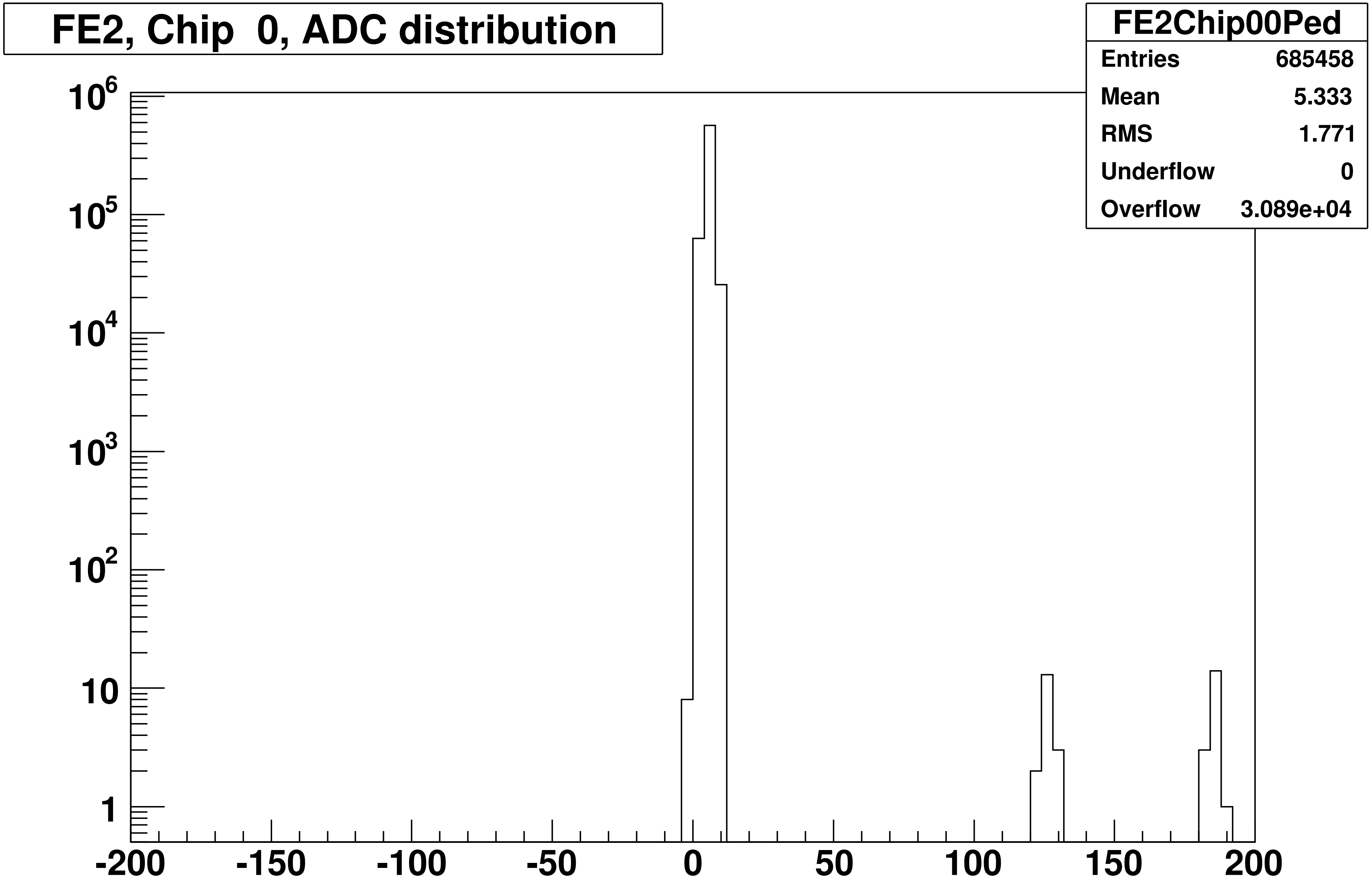

FE2, Chip 0, ADC distribution
FE2Chip00All
Entries 685458
Mean 553.2
RMS 2554
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE2, Chip 0, ADC distribution
FE2Chip00Ped
Entries 685458
Mean 5.333
RMS 1.771
Underflow 0
Overflow 3.089e+04
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10^5
10^4
10^3
10^2
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1
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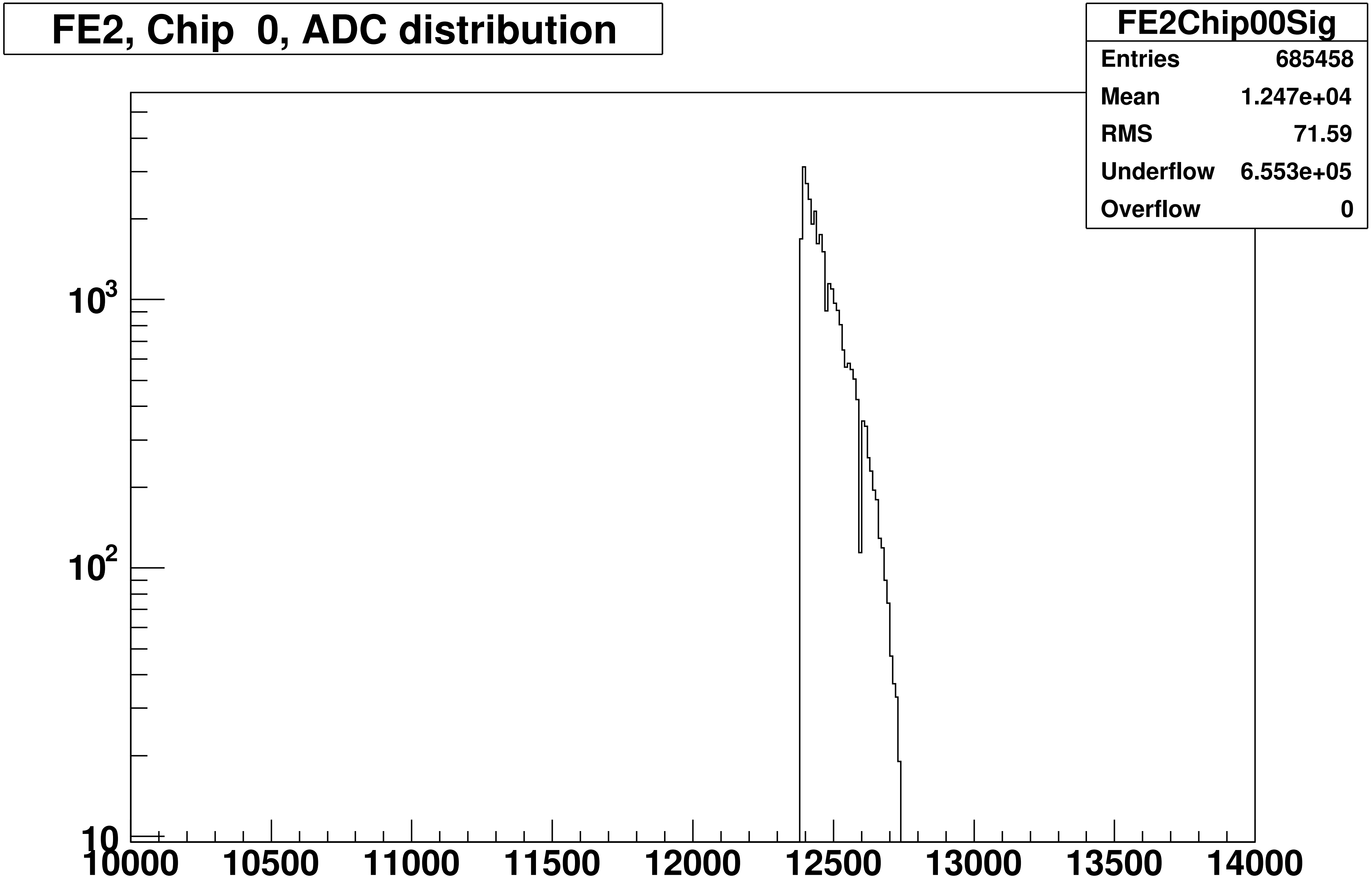
150
200


FE2, Chip 0, ADC distribution
FE2Chip00Sig
Entries 685458
Mean 1.247e+04
RMS 71.59
Underflow 6.553e+05
Overflow 0
10^3
10^2
10
10000
10500
11000
11500
12000
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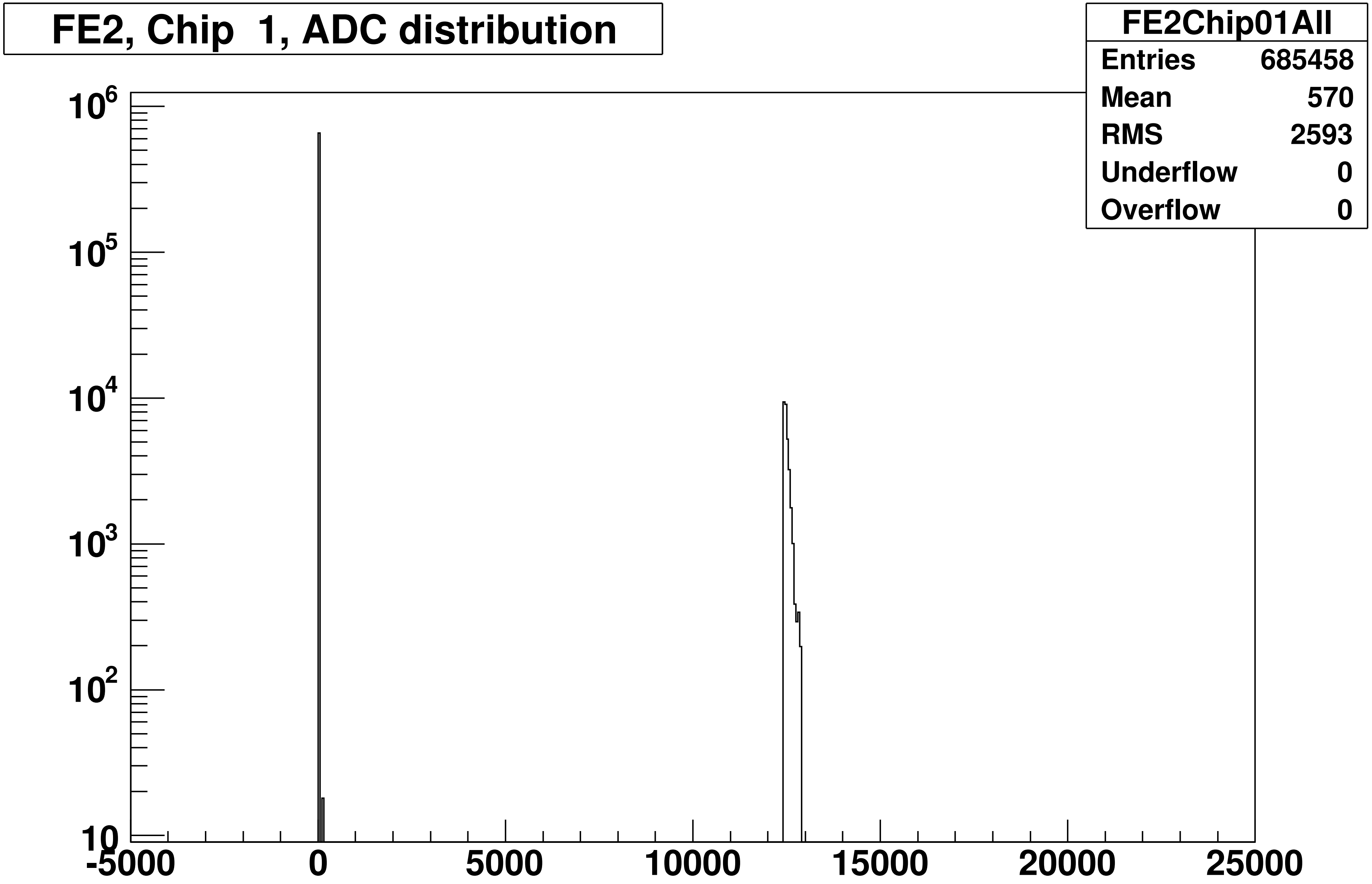
13000
13500
14000



FE2, Chip 1, ADC distribution
FE2Chip01All
Entries 685458
Mean 570
RMS 2593
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
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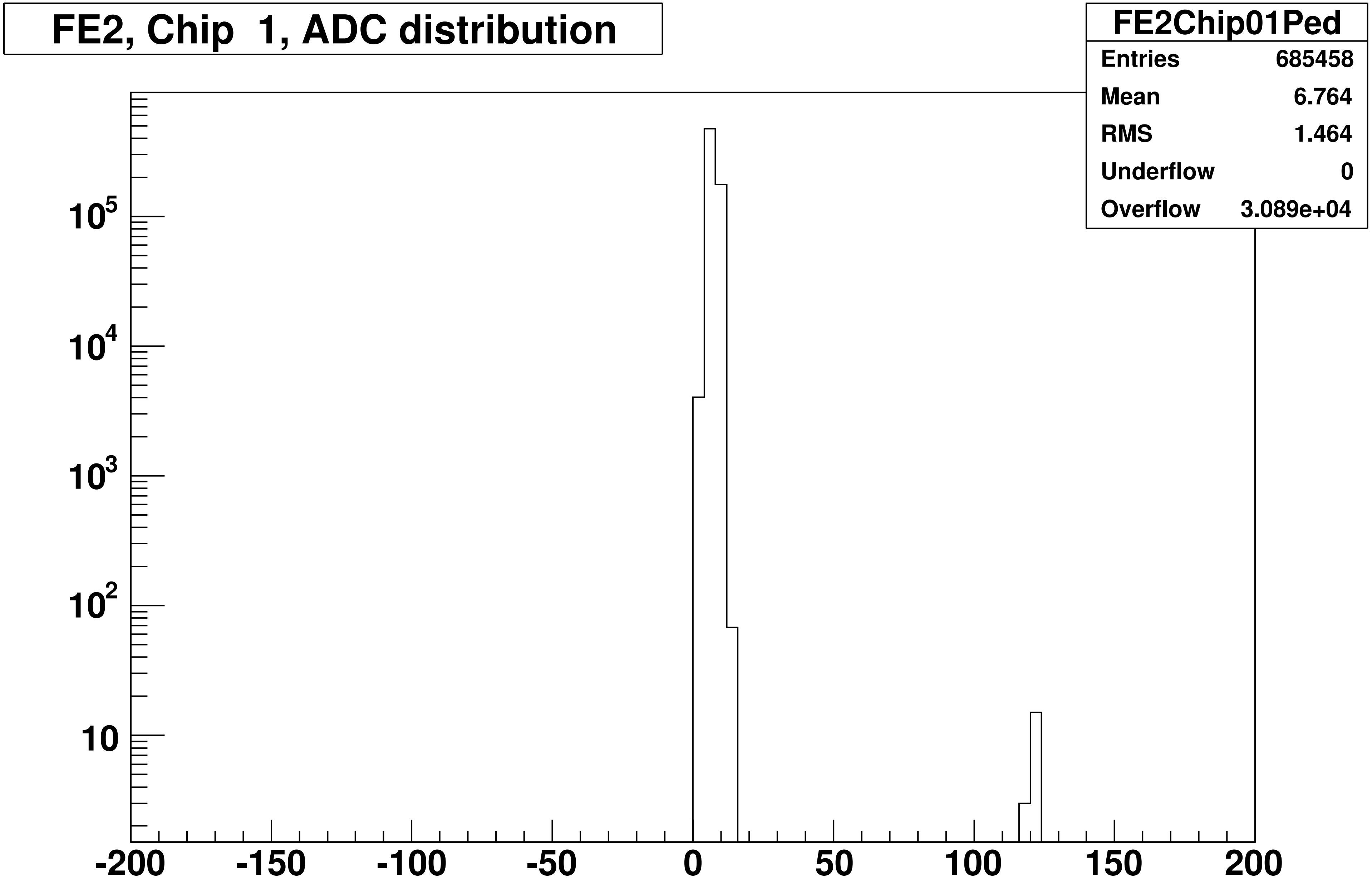
20000
25000


FE2, Chip 1, ADC distribution
FE2Chip01Ped
Entries 685458
Mean 6.764
RMS 1.464
Underflow 0
Overflow 3.089e+04
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10^4
10^3
10^2
10
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-150
-100
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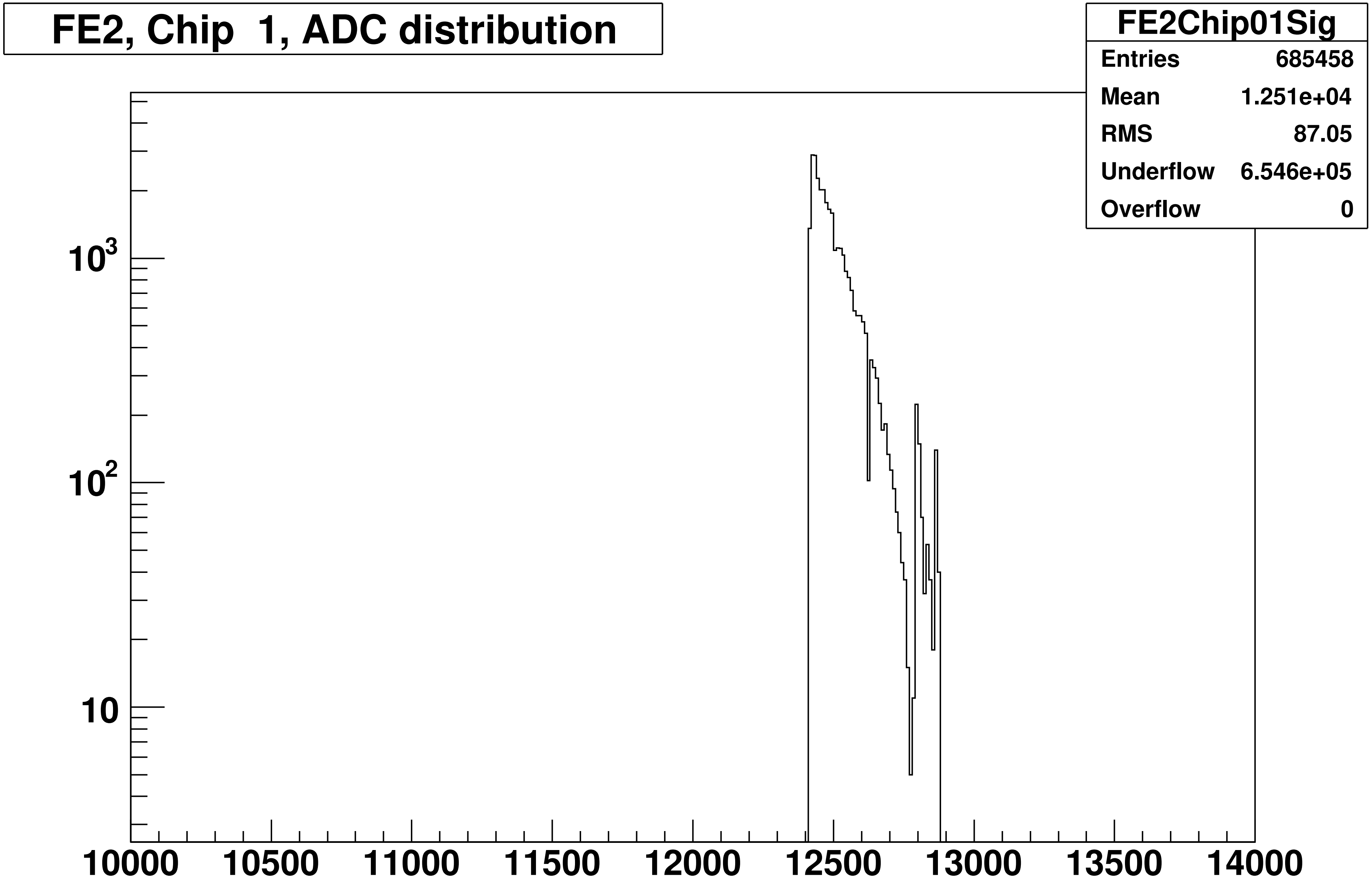
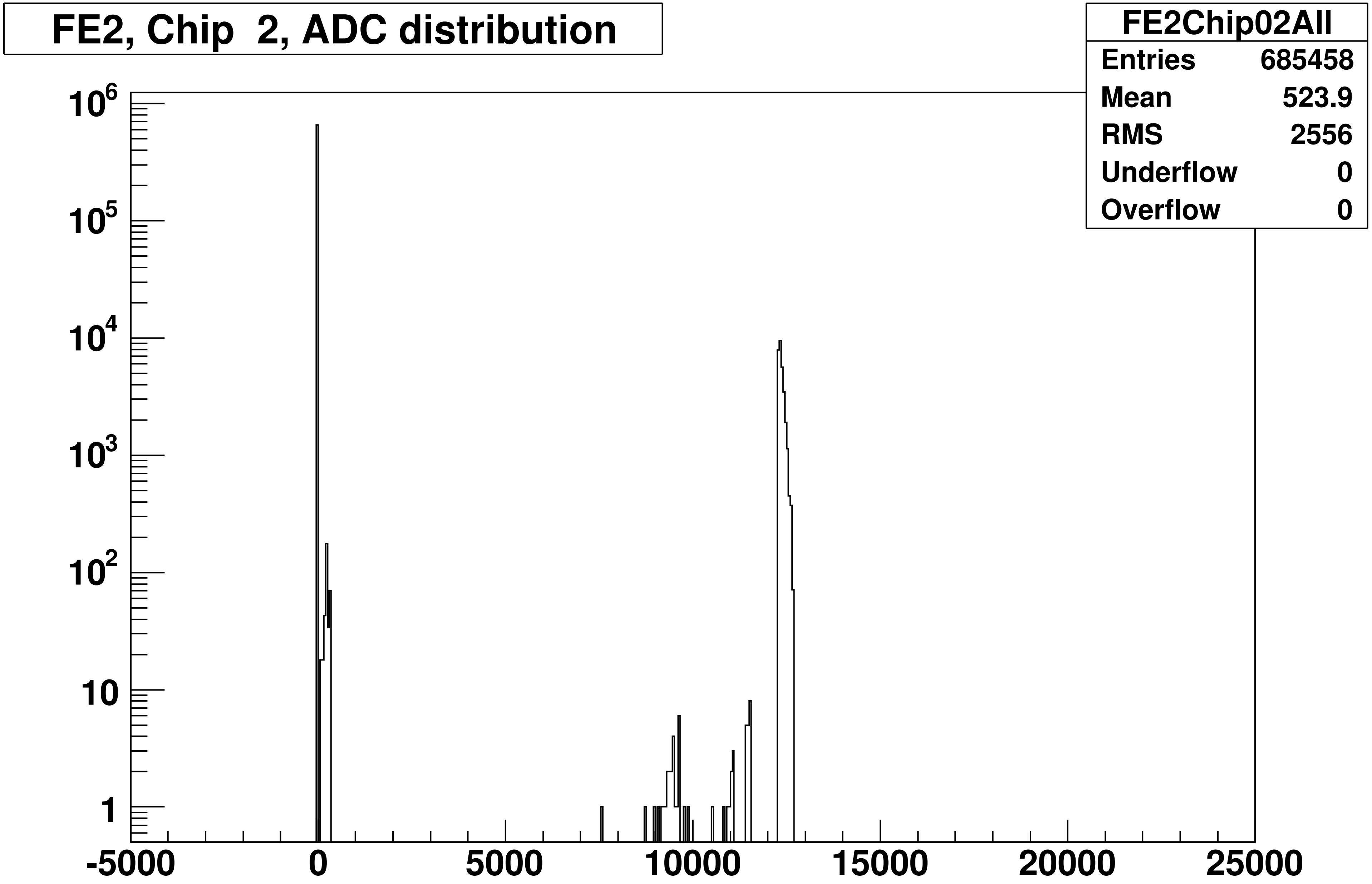
50
100
150
200


FE2, Chip 1, ADC distribution
FE2Chip01Sig
Entries 685458
Mean 1.251e+04
RMS 87.05
Underflow 6.546e+05
Overflow 0
10
10^2
10^3
10000
10500
11000
11500
12000
12500
13000
13500
14000


FE2, Chip 2, ADC distribution
FE2Chip02All
Entries 685458
Mean 523.9
RMS 2556
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
1
-5000
0
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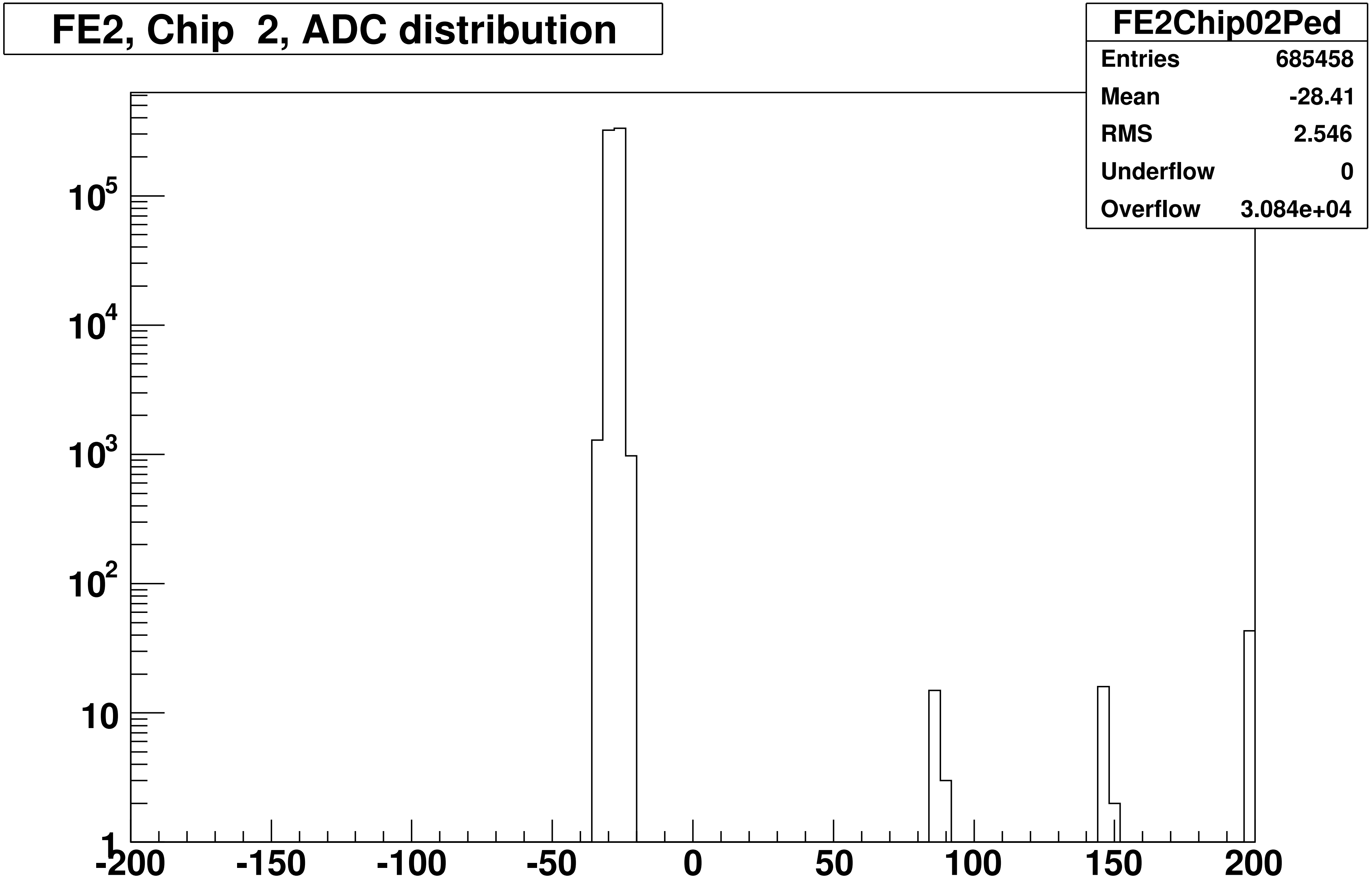
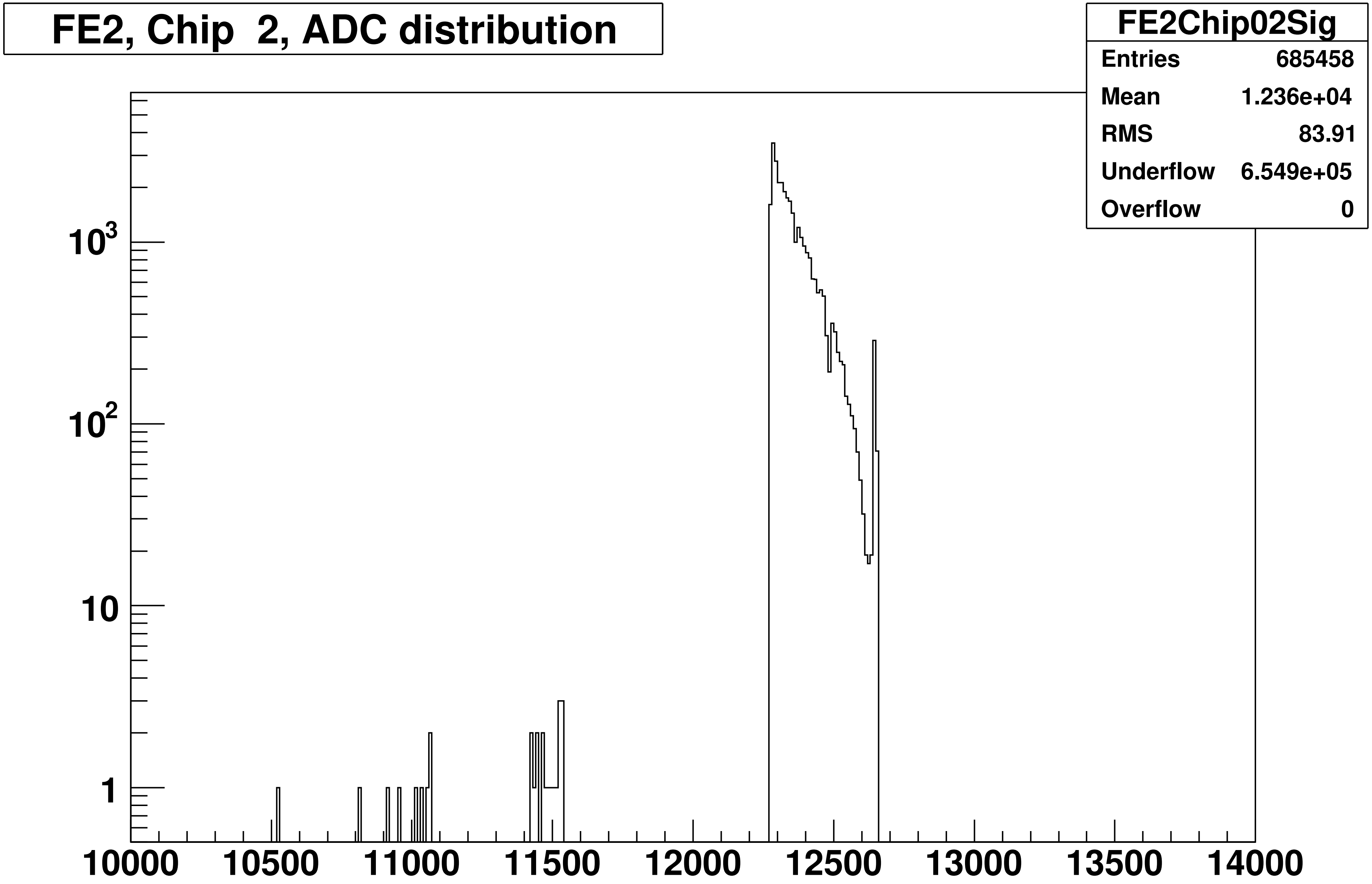
10000
15000
20000
25000


FE2, Chip 2, ADC distribution
FE2Chip02Ped
Entries 685458
Mean -28.41
RMS 2.546
Underflow 0
Overflow 3.084e+04
1
10
10^2
10^3
10^4
10^5
-200
-150
-100
-50
0
50
100
150
200


FE2, Chip 2, ADC distribution
FE2Chip02Sig
Entries 685458
Mean 1.236e+04
RMS 83.91
Underflow 6.549e+05
Overflow 0
10^3
10^2
10
1
10000
10500
11000
11500
12000
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13500
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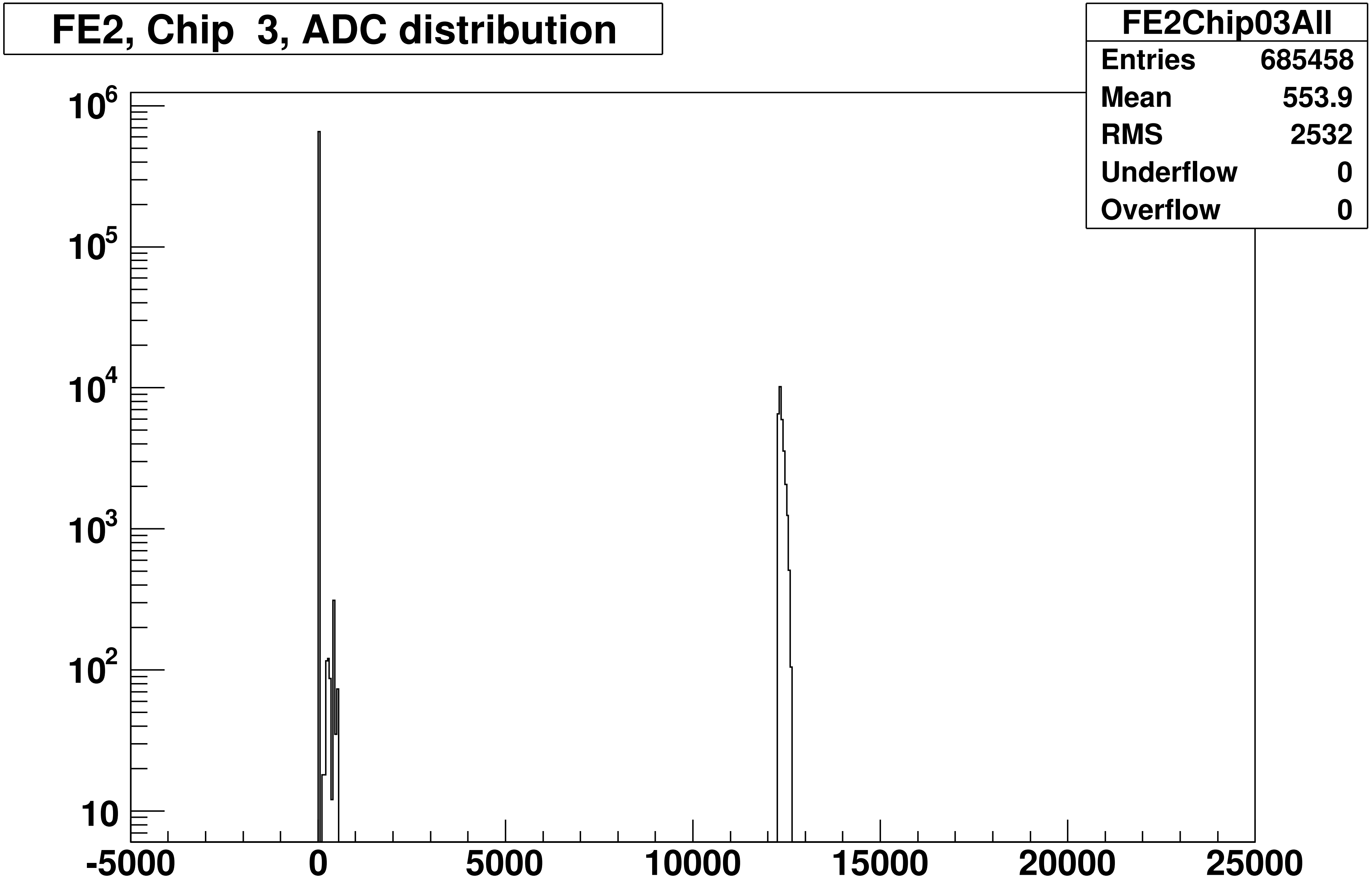
FE2, Chip 3, ADC distribution
FE2Chip03All
Entries 685458
Mean 553.9
RMS 2532
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
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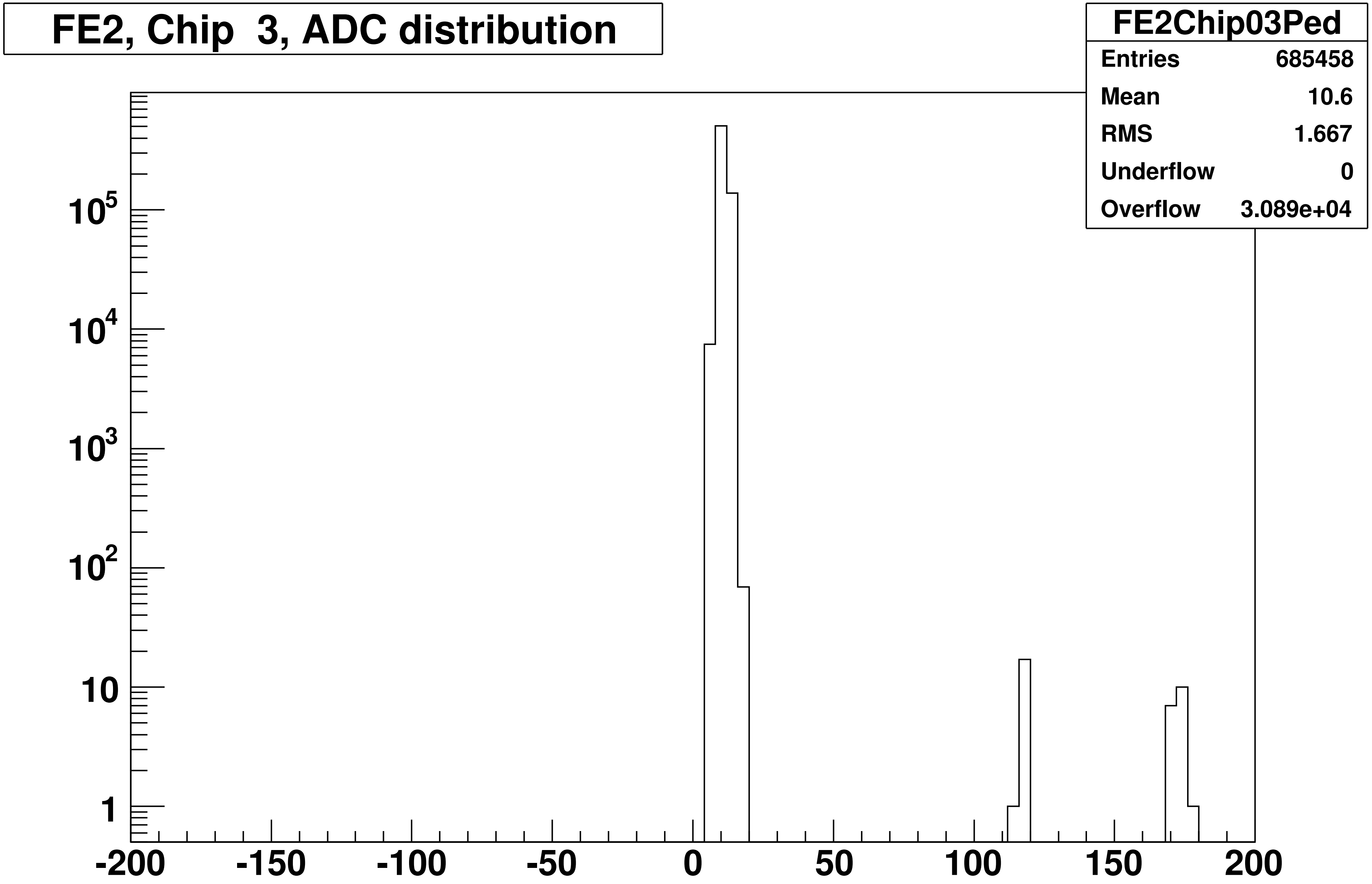
FE2, Chip 3, ADC distribution
FE2Chip03Ped
Entries 685458
Mean 10.6
RMS 1.667
Underflow 0
Overflow 3.089e+04
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10^4
10^3
10^2
10
1
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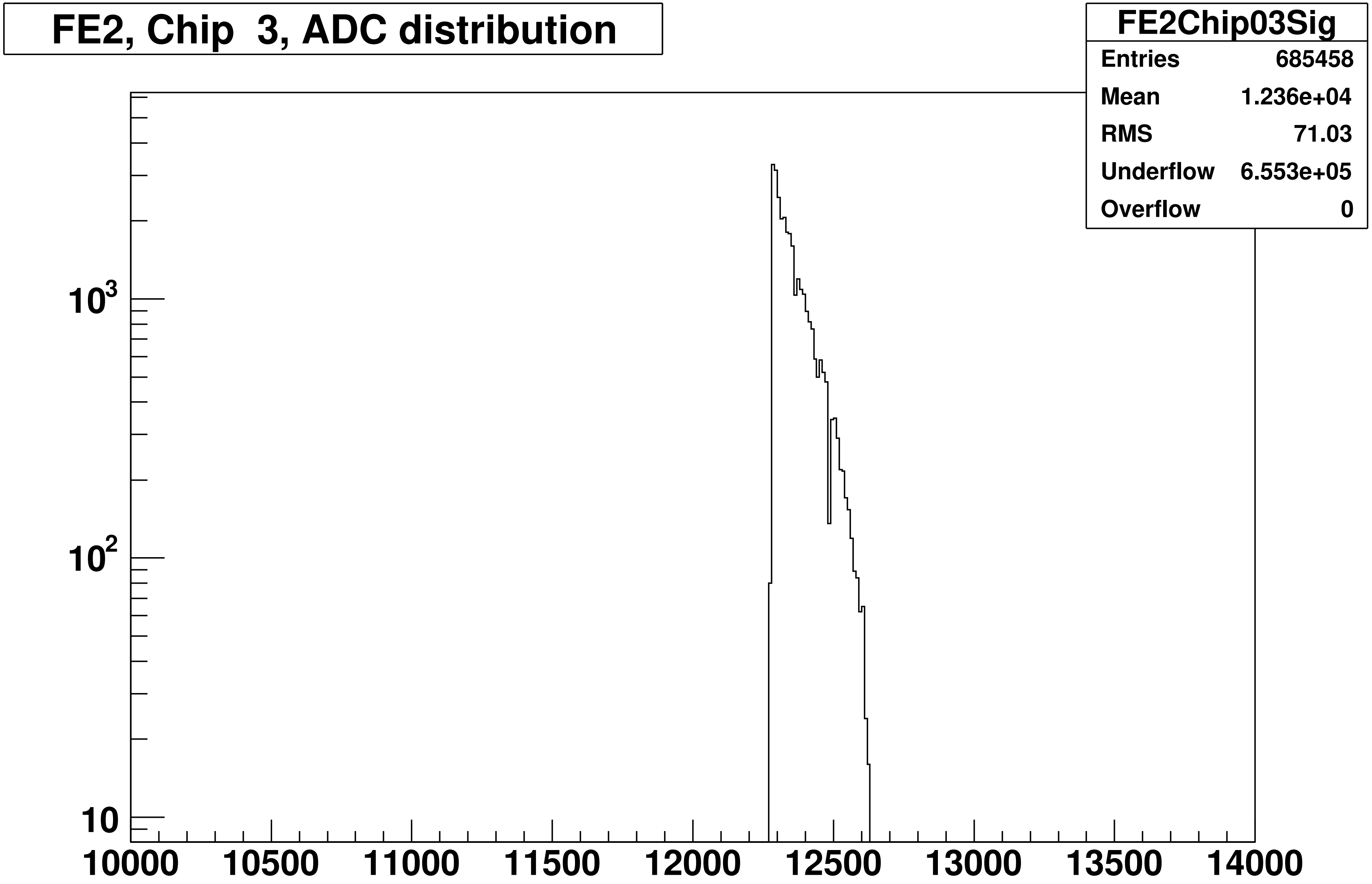
FE2, Chip 3, ADC distribution
FE2Chip03Sig
Entries 685458
Mean 1.236e+04
RMS 71.03
Underflow 6.553e+05
Overflow 0
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10^2
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10000
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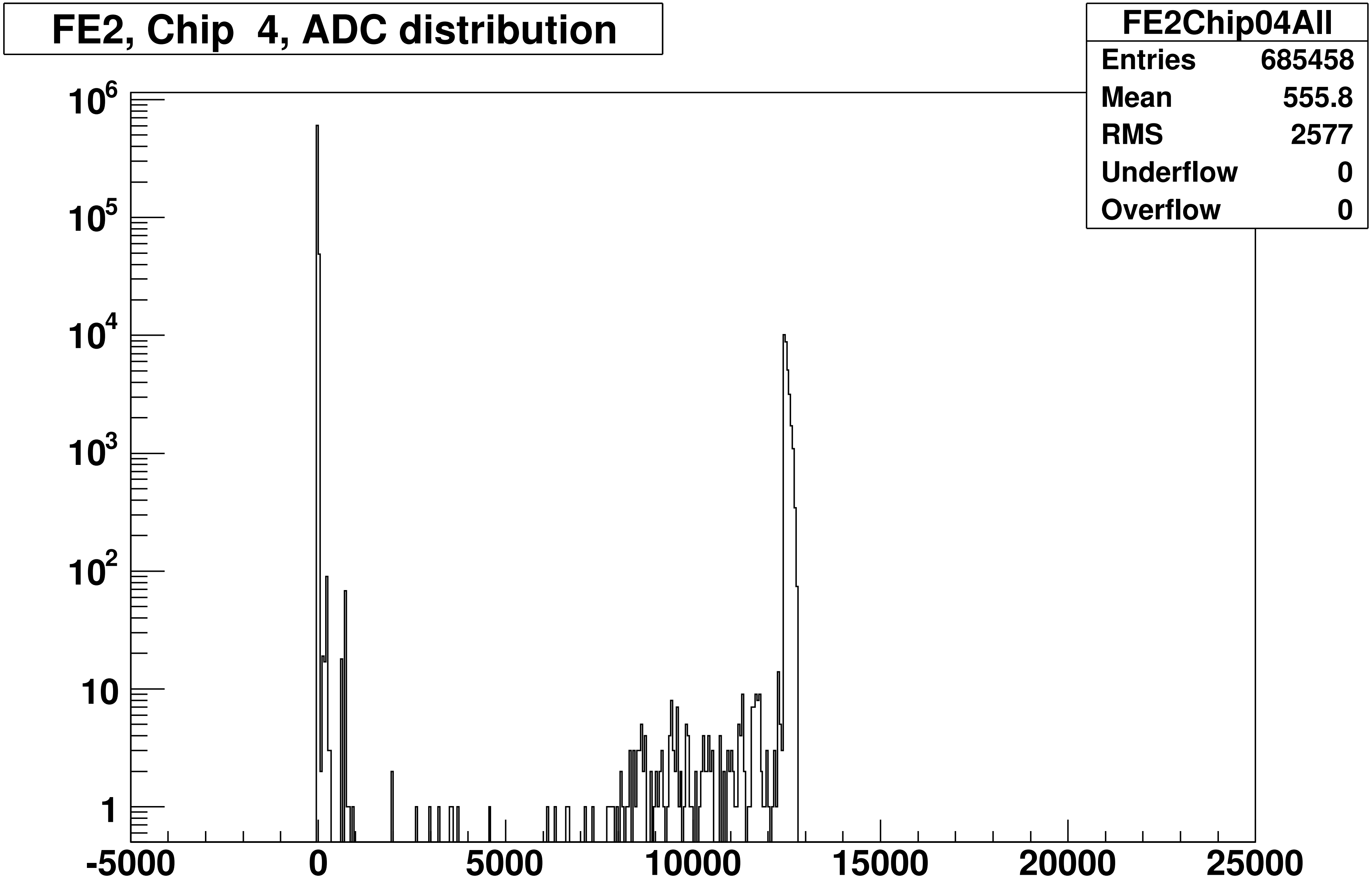

FE2, Chip 4, ADC distribution
FE2Chip04All
Entries 685458
Mean 555.8
RMS 2577
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
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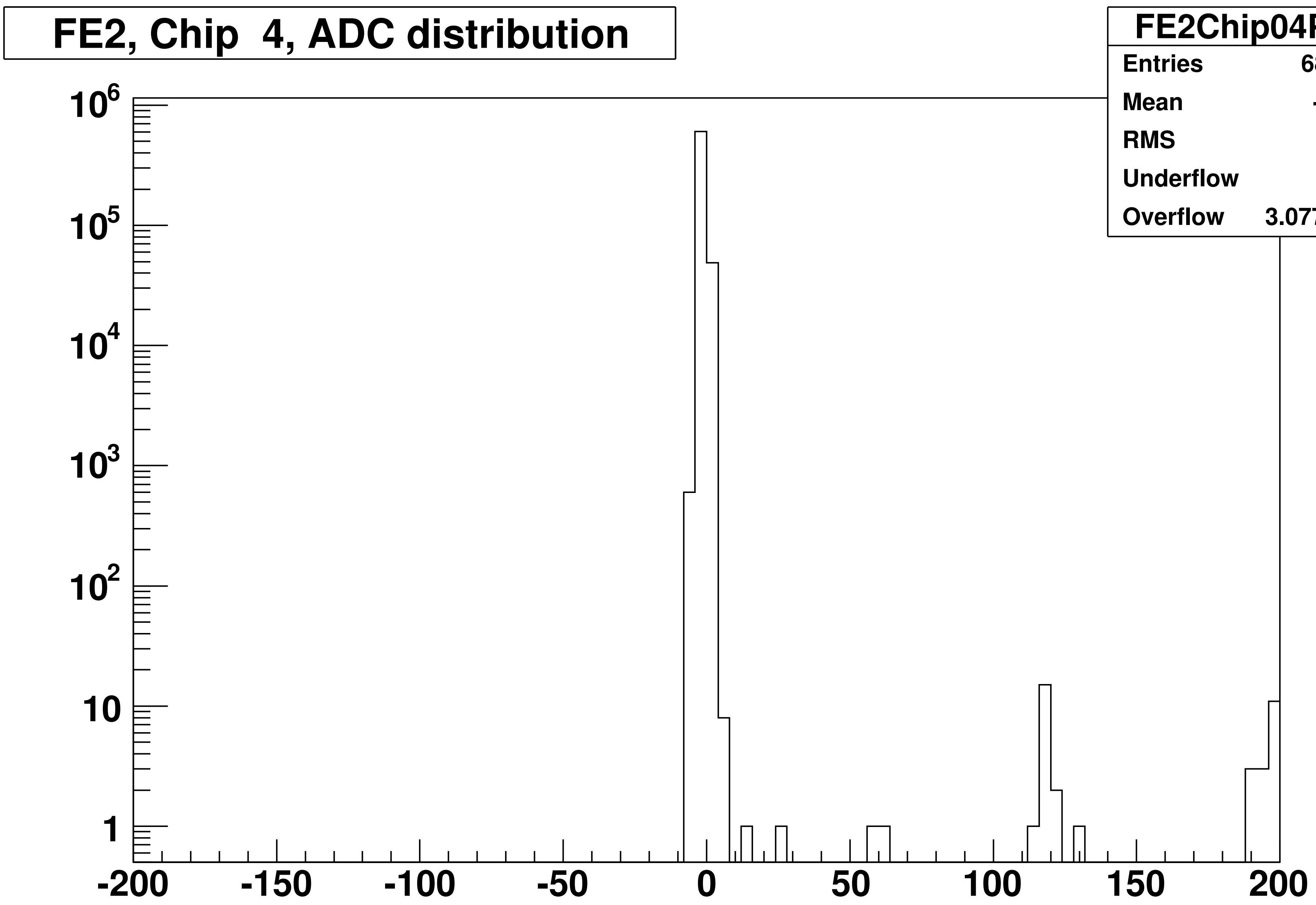

FE2, Chip 4, ADC distribution
FE2Chip04Ped
Entries 685458
Mean -1.102
RMS 1.374
Underflow 0
Overflow 3.077e+04
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10^5
10^4
10^3
10^2
10
1
-200
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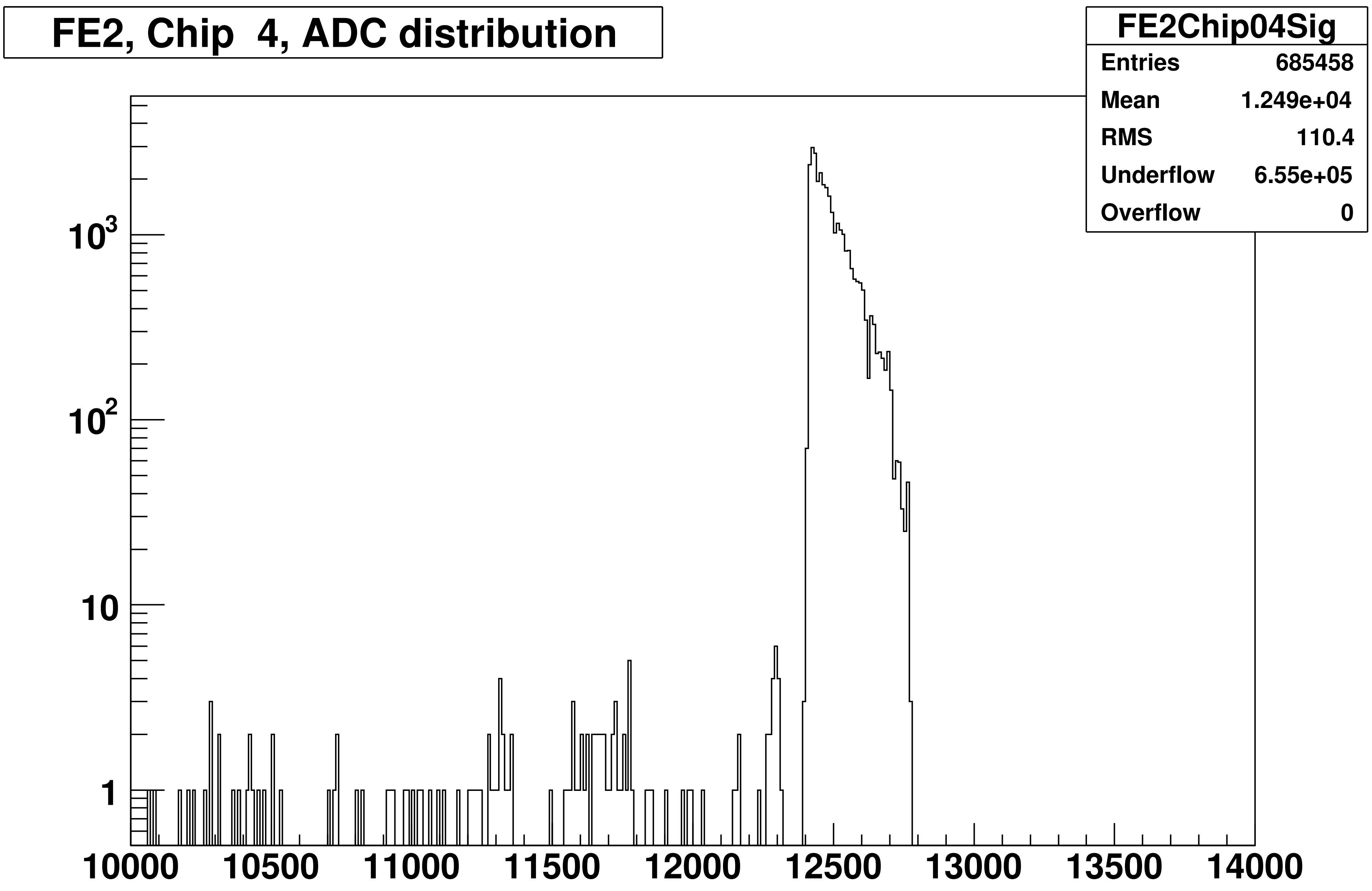
FE2, Chip 4, ADC distribution
FE2Chip04Sig
Entries 685458
Mean 1.249e+04
RMS 110.4
Underflow 6.55e+05
Overflow 0
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10^2
10
1
10000
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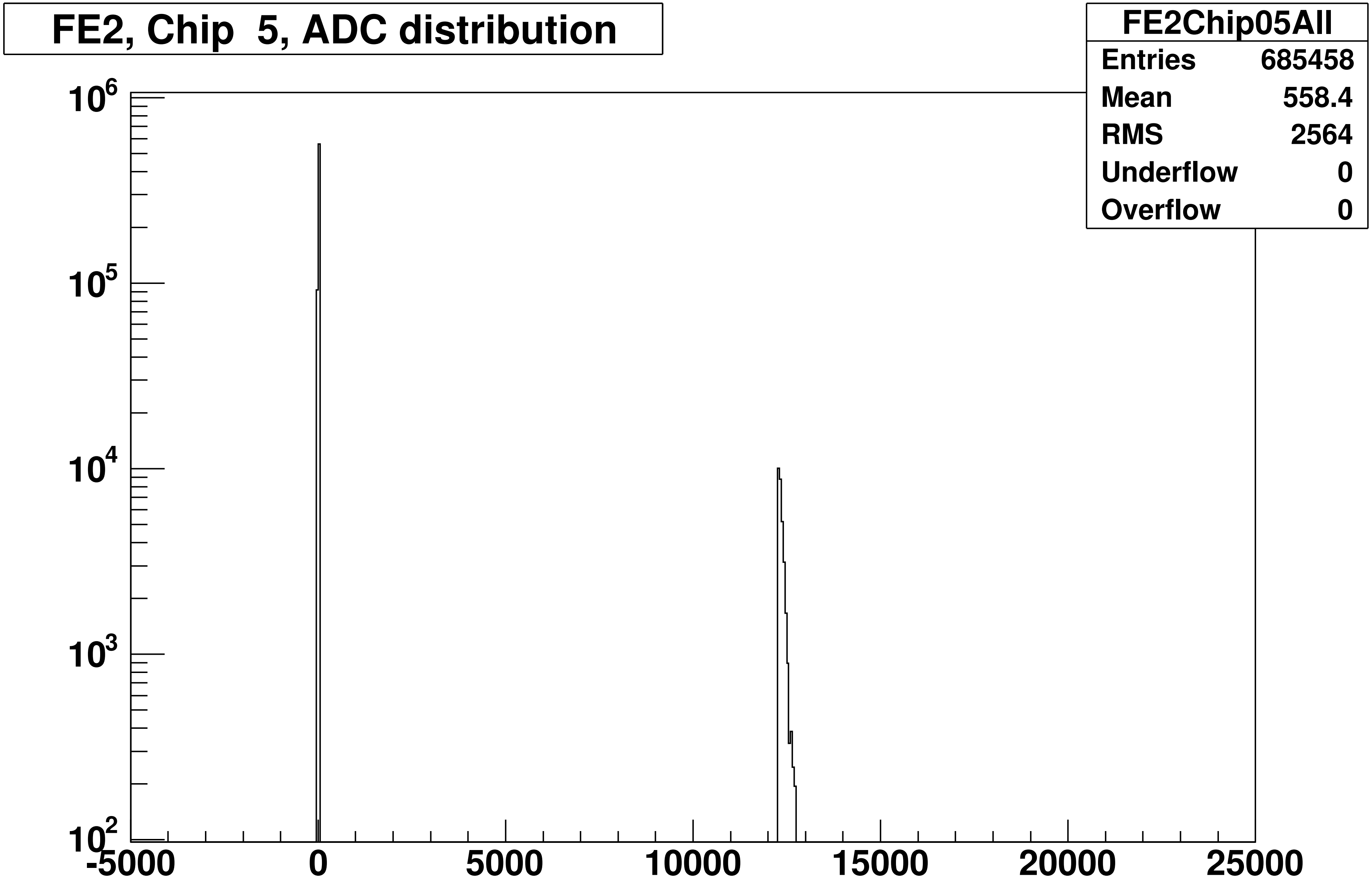

FE2, Chip 5, ADC distribution
FE2Chip05All
Entries 685458
Mean 558.4
RMS 2564
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
-5000
0
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10000
15000
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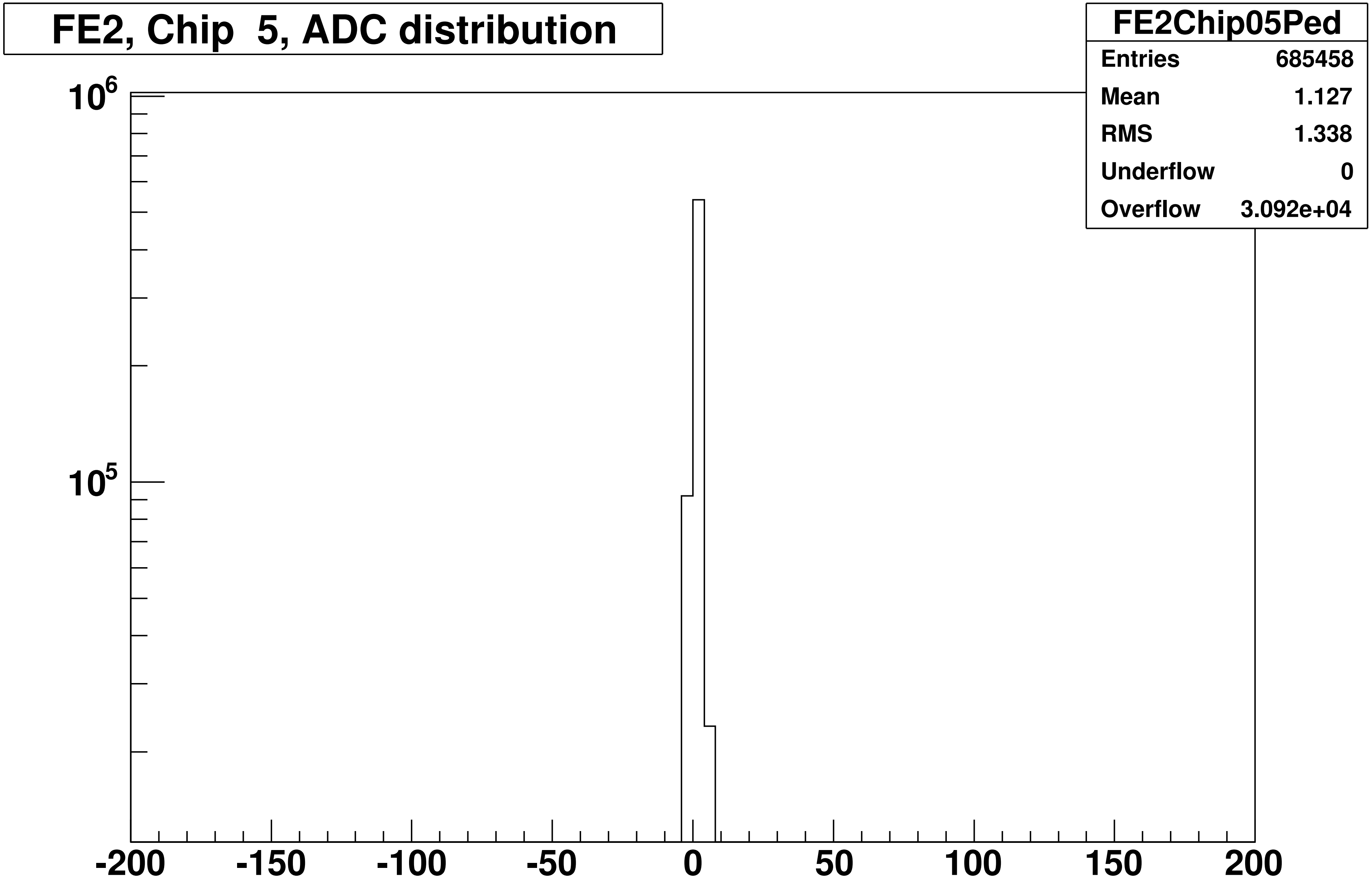
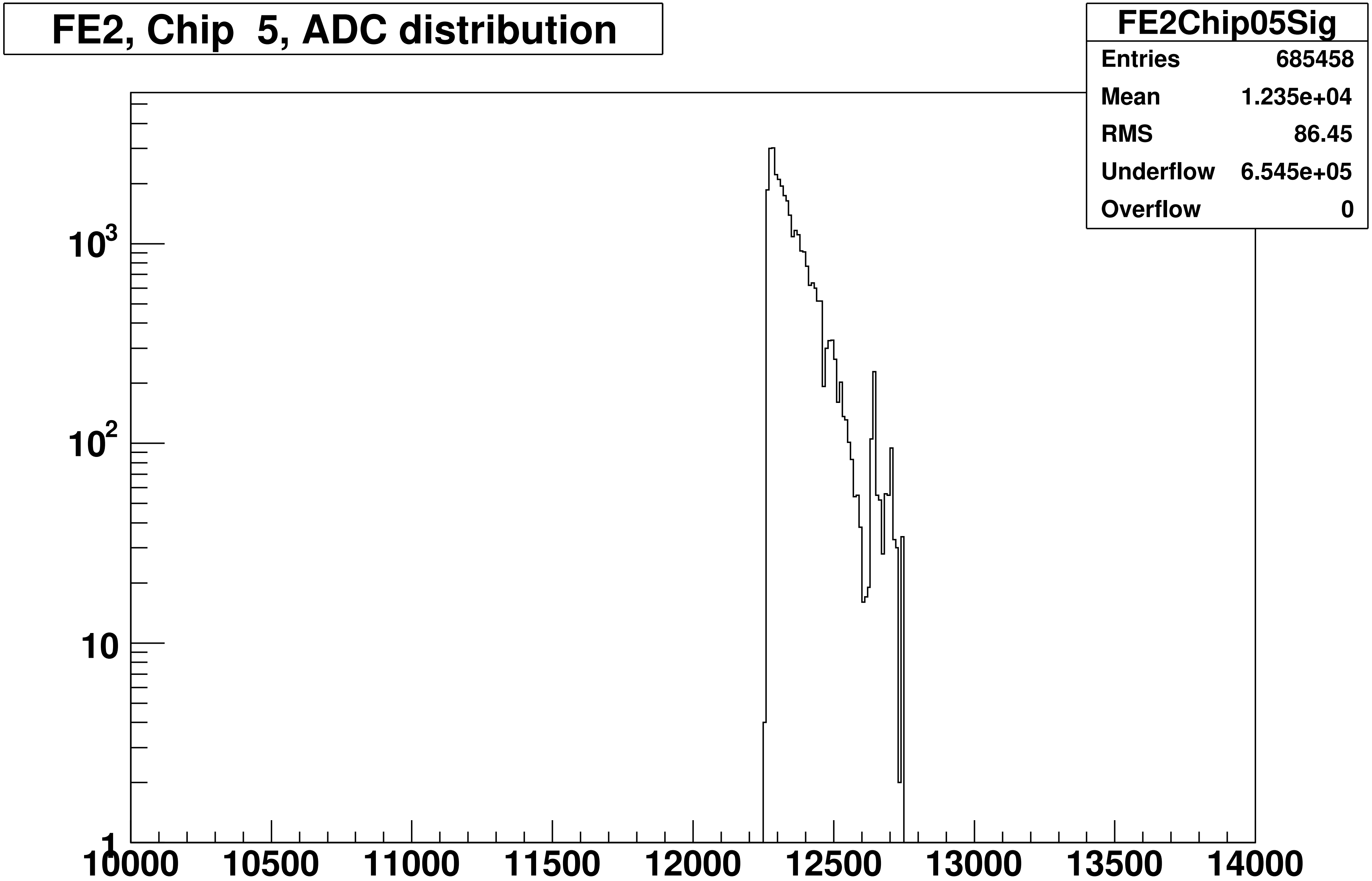

FE2, Chip 5, ADC distribution
FE2Chip05Ped
Entries 685458
Mean 1.127
RMS 1.338
Underflow 0
Overflow 3.092e+04
10^6
10^5
-200
-150
-100
-50
0
50
100
150
200


FE2, Chip 5, ADC distribution
FE2Chip05Sig
Entries 685458
Mean 1.235e+04
RMS 86.45
Underflow 6.545e+05
Overflow 0
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10^2
10
1
10000
10500
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11500
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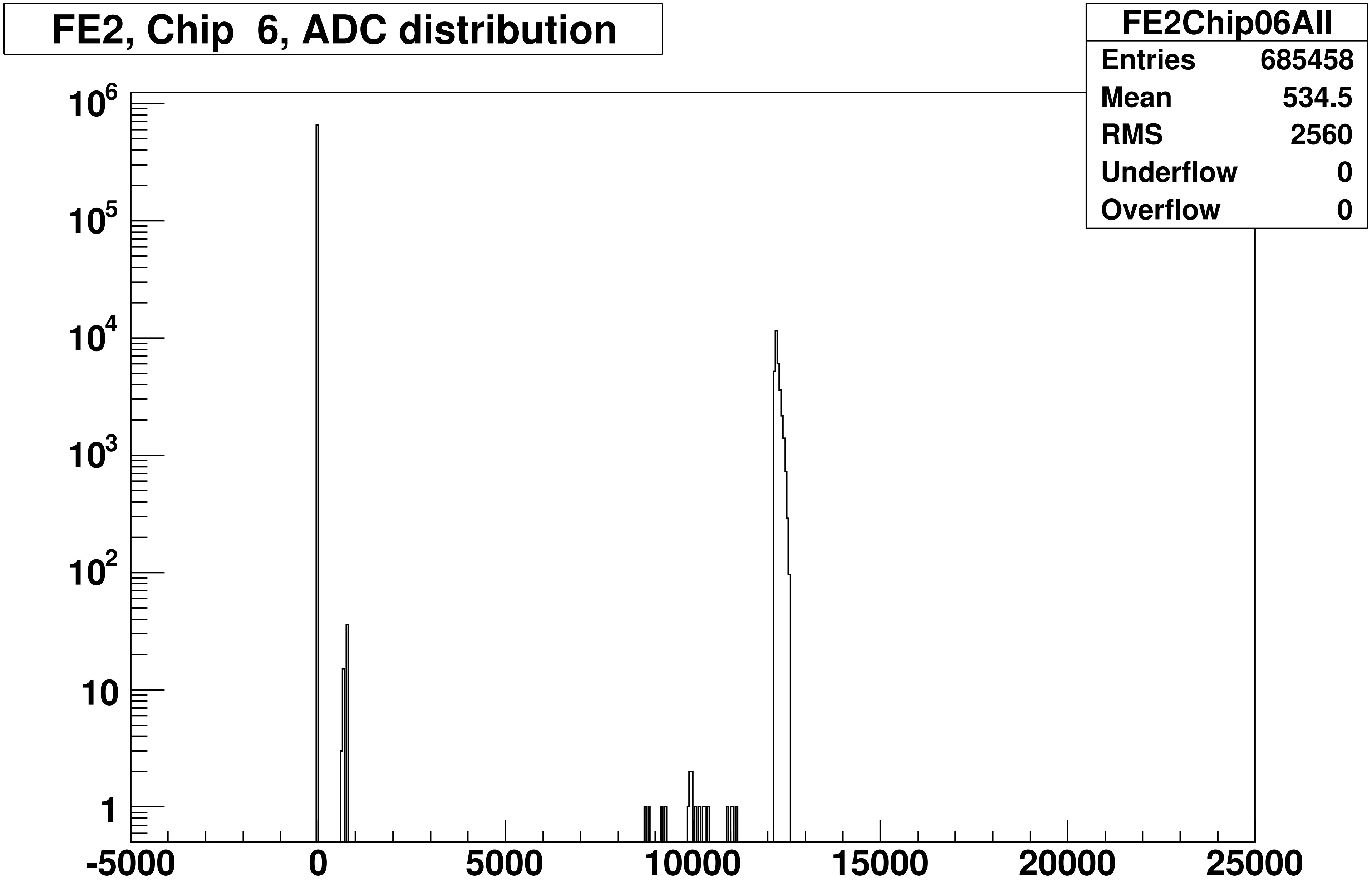

FE2, Chip 6, ADC distribution
FE2Chip06All
Entries 685458
Mean 534.5
RMS 2560
Underflow 0
Overflow 0
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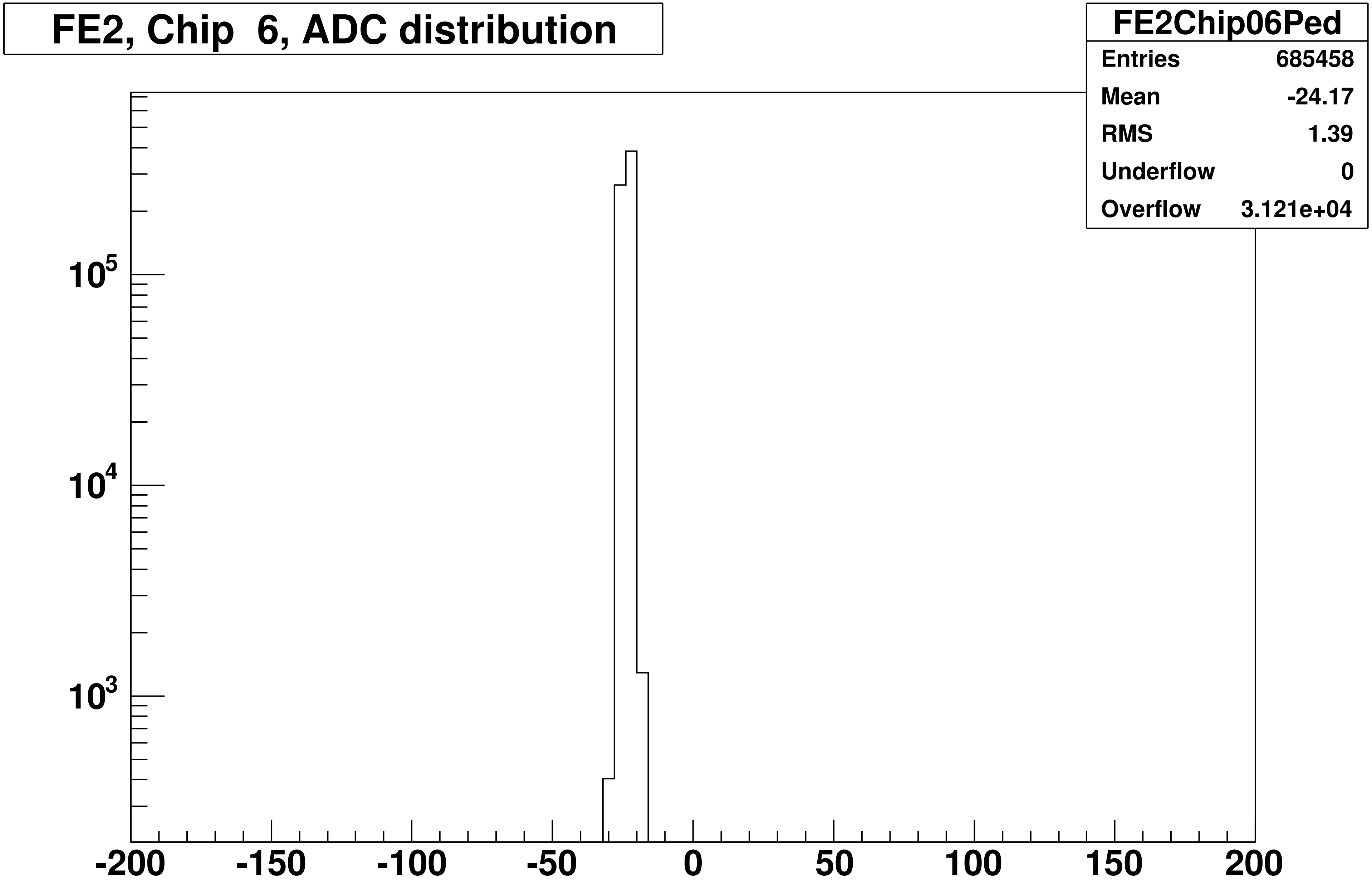
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE2, Chip 6, ADC distribution
FE2Chip06Ped
Entries 685458
Mean -24.17
RMS 1.39
Underflow 0
Overflow 3.121e+04
10^5
10^4
10^3
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-100
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0
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150
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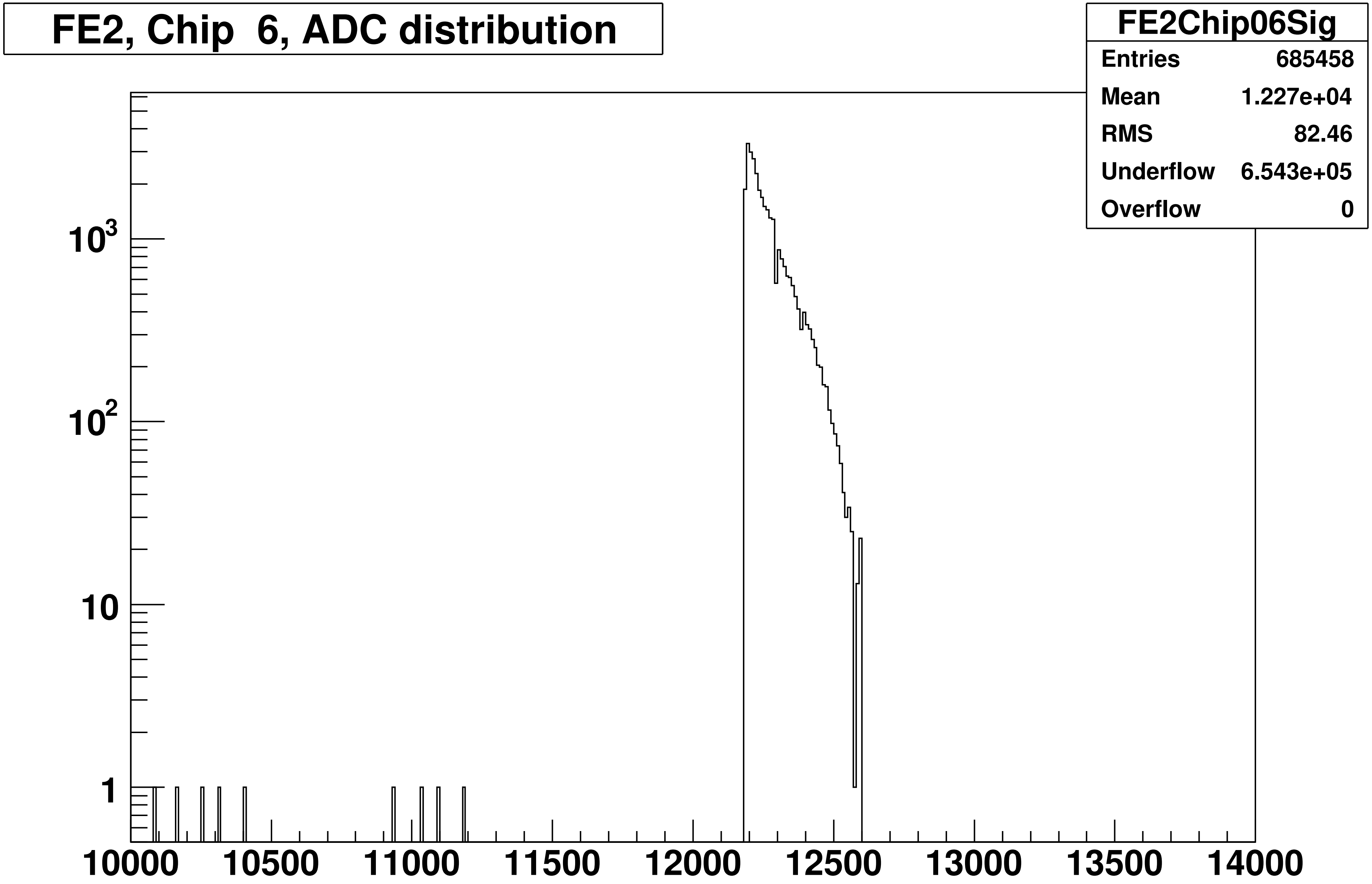
FE2, Chip 6, ADC distribution
FE2Chip06Sig
Entries 685458
Mean 1.227e+04
RMS 82.46
Underflow 6.543e+05
Overflow 0
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10^2
10
1
10000
10500
11000
11500
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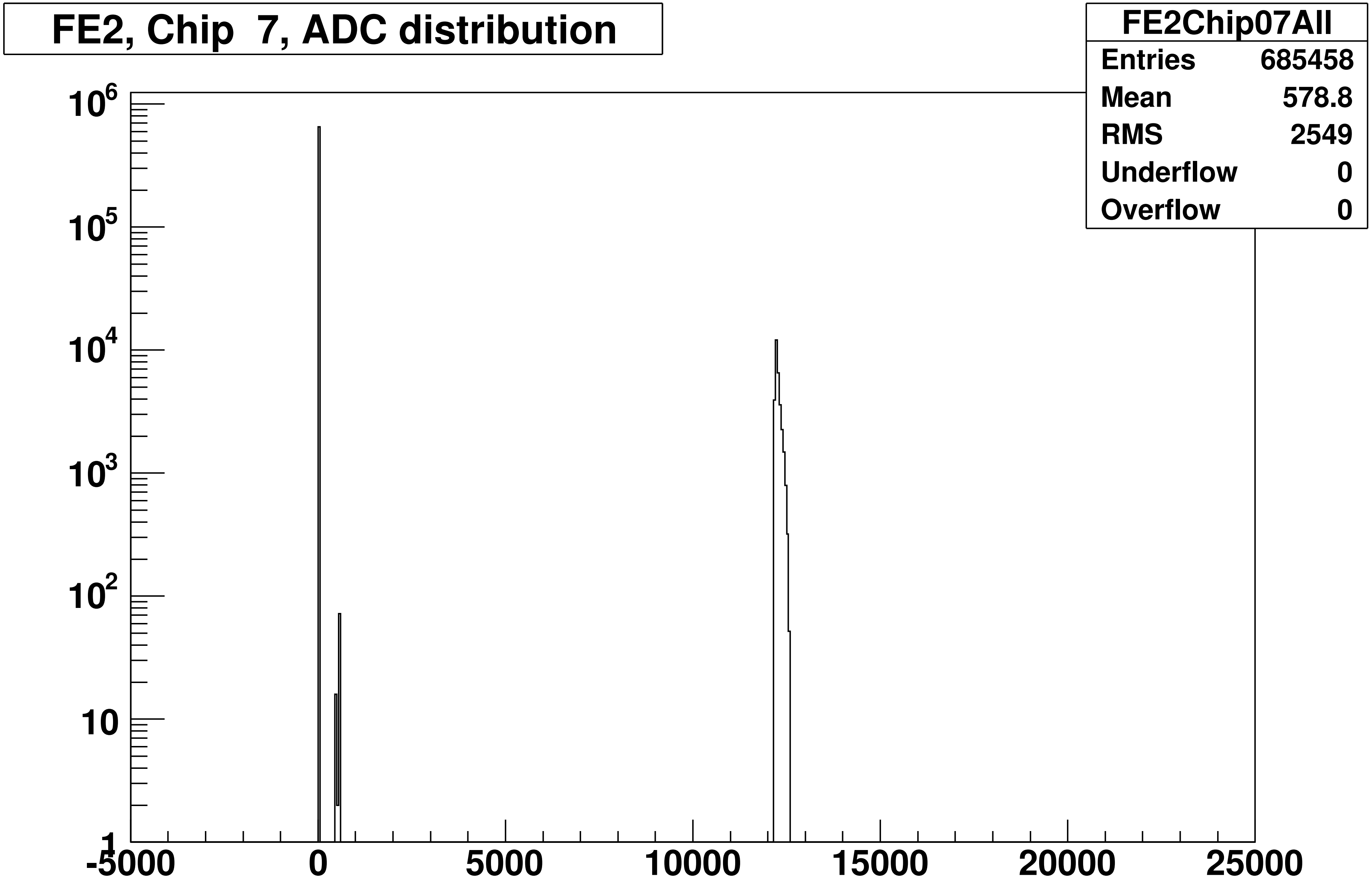
12500
13000
13500
14000



FE2, Chip 7, ADC distribution
FE2Chip07All
Entries 685458
Mean 578.8
RMS 2549
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
1
-5000
0
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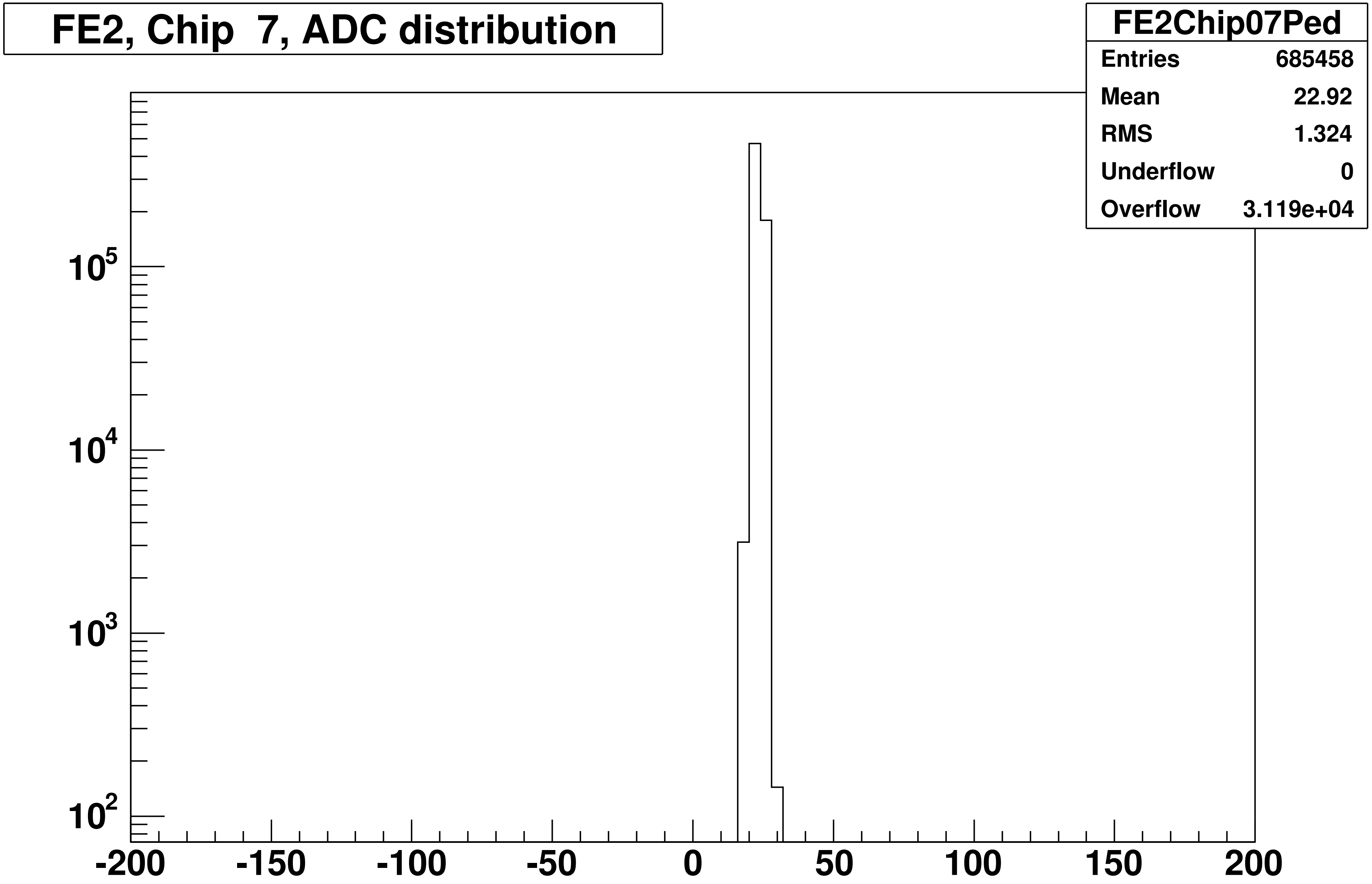
10000
15000
20000
25000


FE2, Chip 7, ADC distribution
FE2Chip07Ped
Entries 685458
Mean 22.92
RMS 1.324
Underflow 0
Overflow 3.119e+04
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10^4
10^3
10^2
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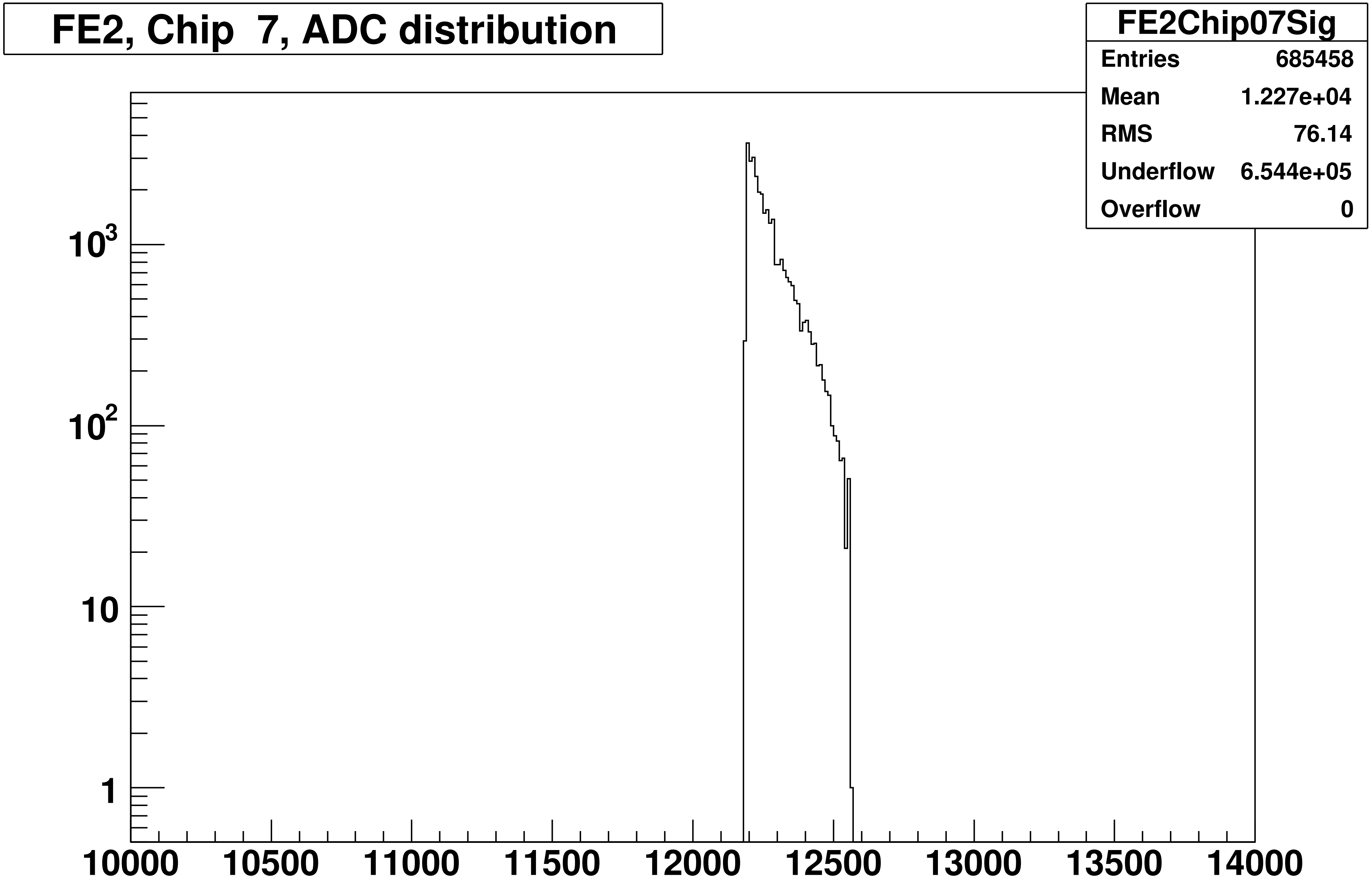
-150
-100
-50
0
50
100
150
200



FE2, Chip 7, ADC distribution
FE2Chip07Sig
Entries 685458
Mean 1.227e+04
RMS 76.14
Underflow 6.544e+05
Overflow 0
10^3
10^2
10
1
10000
10500
11000
11500
12000
12500
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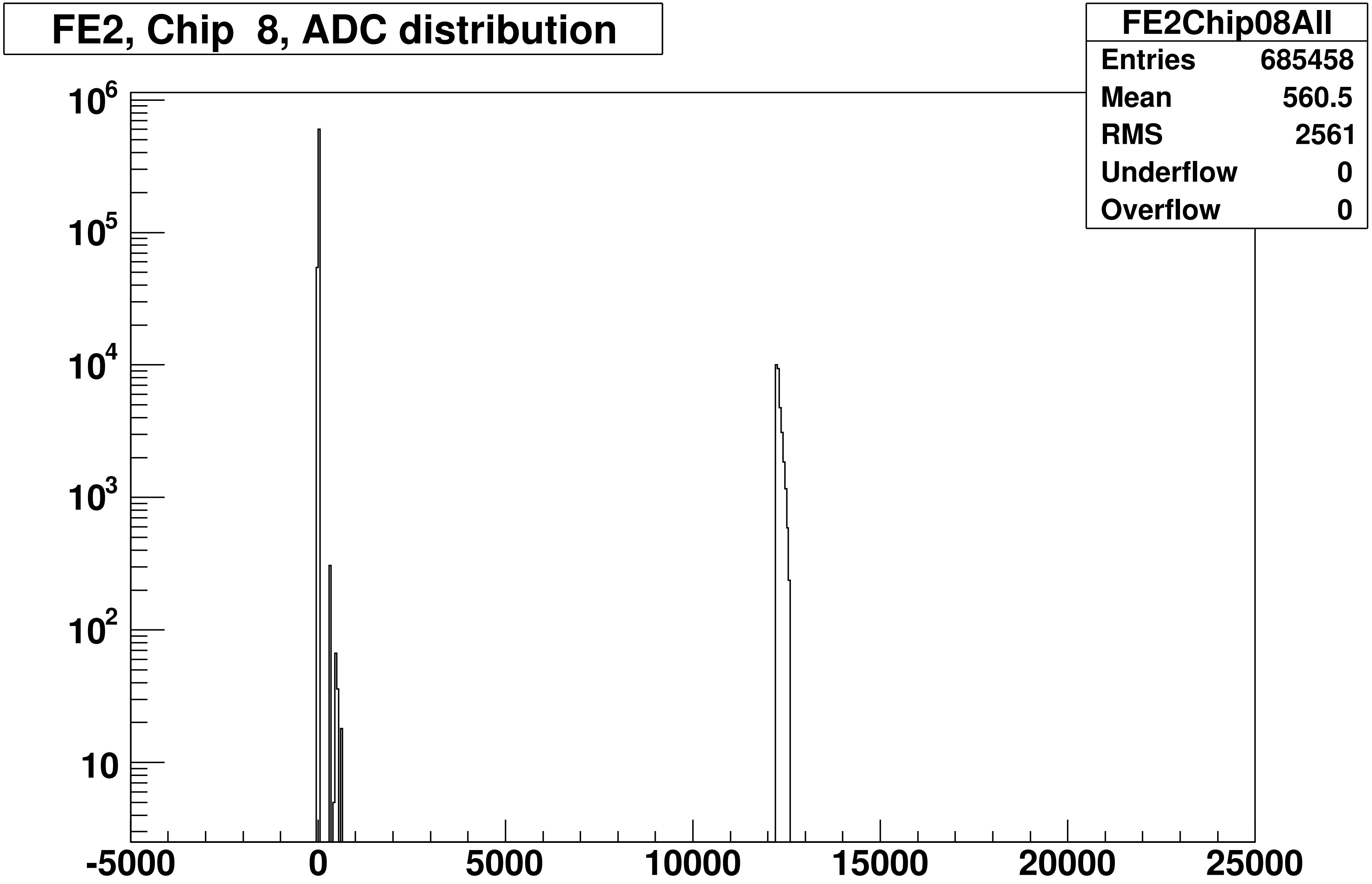

FE2, Chip 8, ADC distribution
FE2Chip08All
Entries 685458
Mean 560.5
RMS 2561
Underflow 0
Overflow 0
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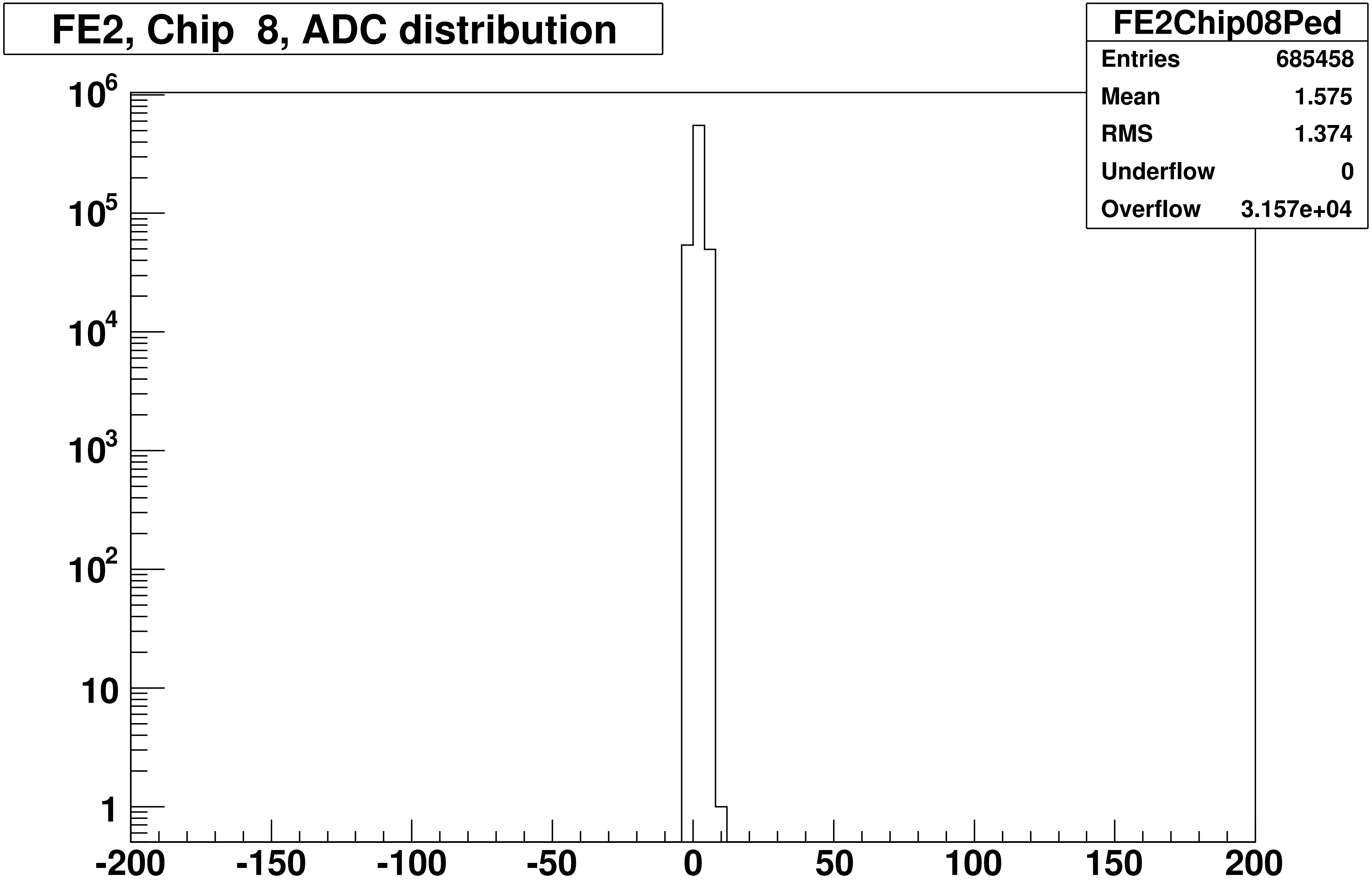
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000



FE2, Chip 8, ADC distribution
FE2Chip08Ped
Entries 685458
Mean 1.575
RMS 1.374
Underflow 0
Overflow 3.157e+04
10^6
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
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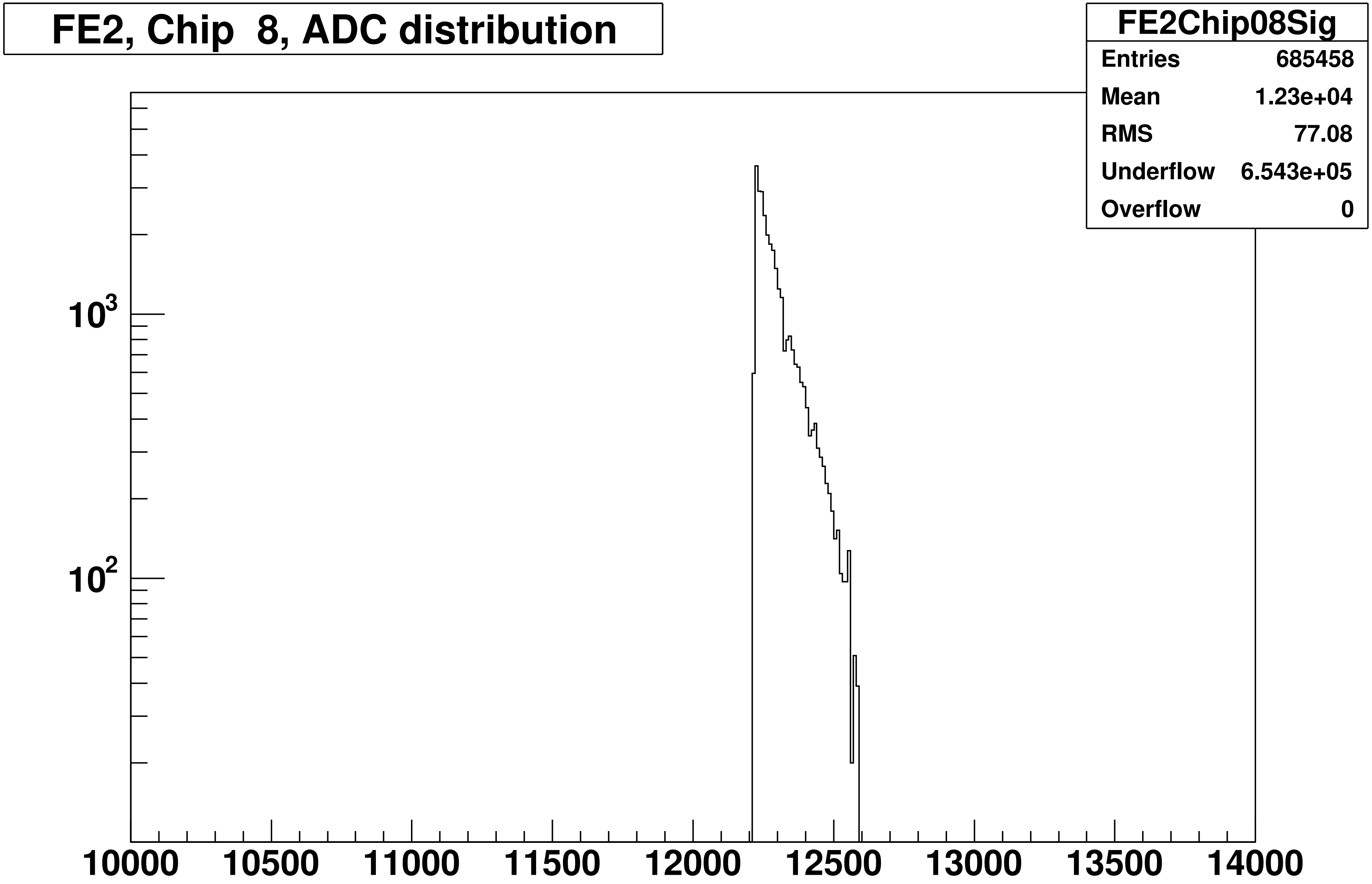
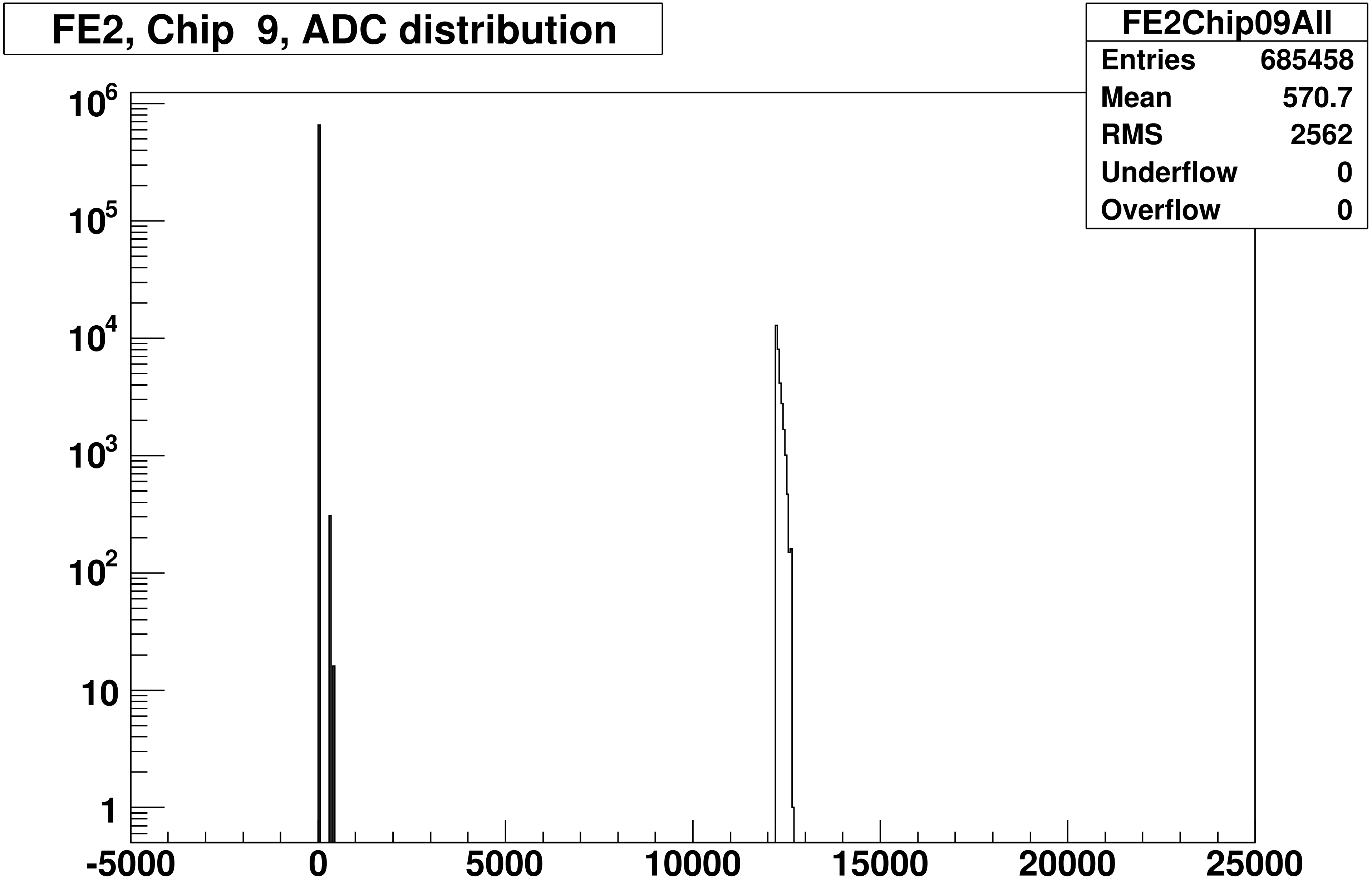


FE2, Chip 8, ADC distribution
FE2Chip08Sig
Entries 685458
Mean 1.23e+04
RMS 77.08
Underflow 6.543e+05
Overflow 0
10^3
10^2
10000
10500
11000
11500
12000
12500
13000
13500
14000



FE2, Chip 9, ADC distribution
FE2Chip09All
Entries 685458
Mean 570.7
RMS 2562
Underflow 0
Overflow 0
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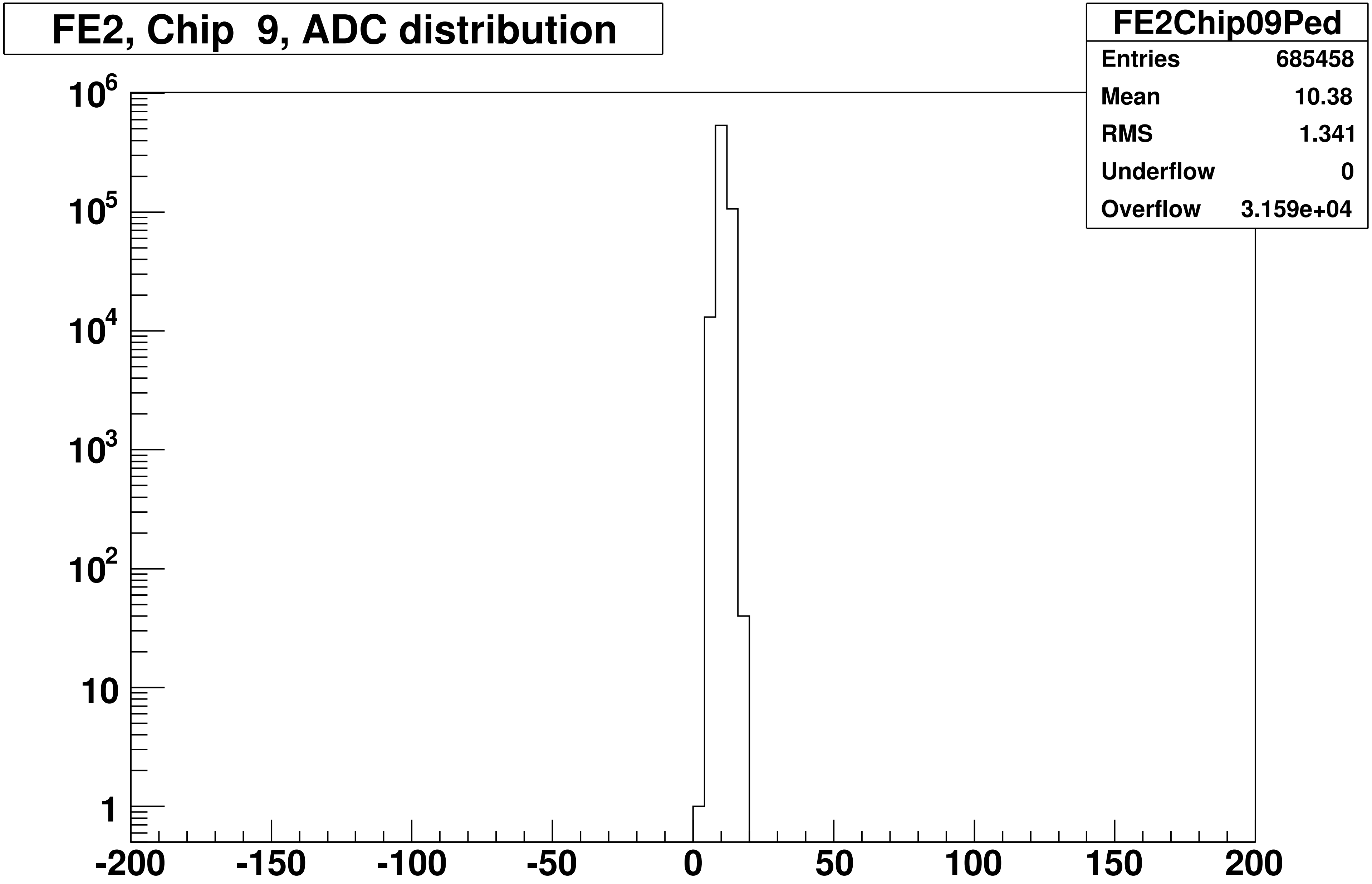
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE2, Chip 9, ADC distribution
FE2Chip09Ped
Entries 685458
Mean 10.38
RMS 1.341
Underflow 0
Overflow 3.159e+04
10^6
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
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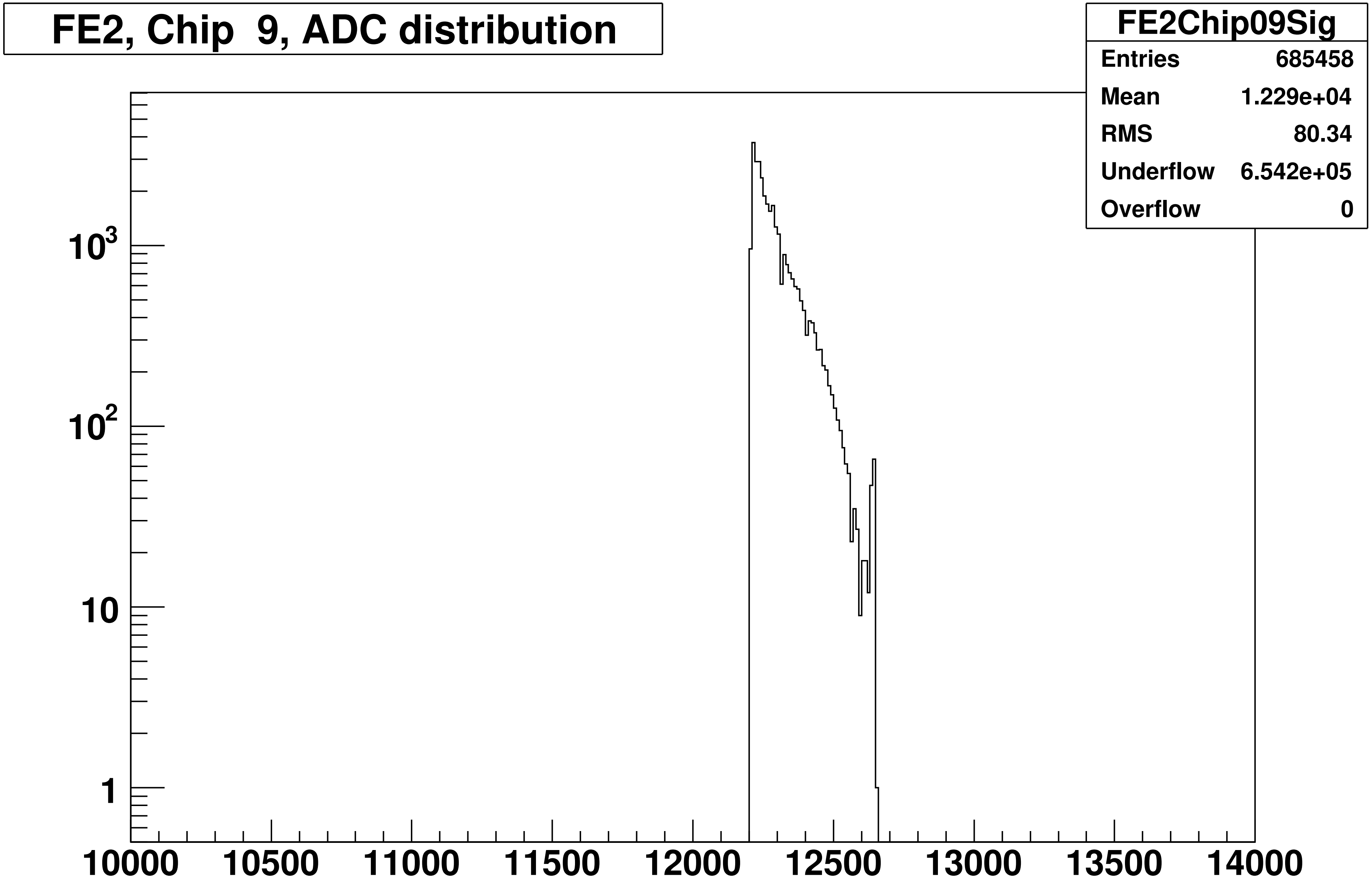
0
50
100
150
200


FE2, Chip 9, ADC distribution
FE2Chip09Sig
Entries 685458
Mean 1.229e+04
RMS 80.34
Underflow 6.542e+05
Overflow 0
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10^2
10
1
10000
10500
11000
11500
12000
12500
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13500
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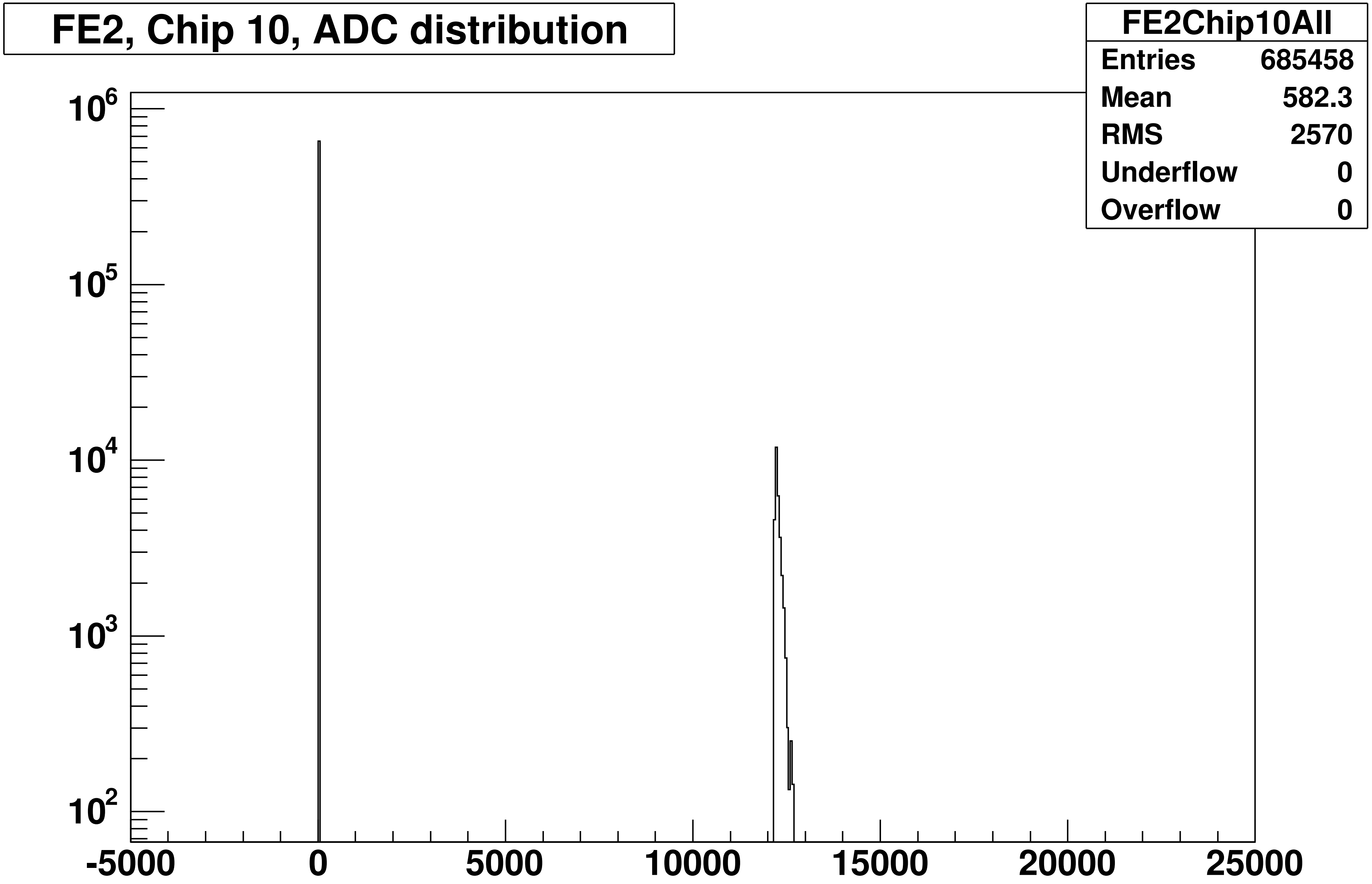
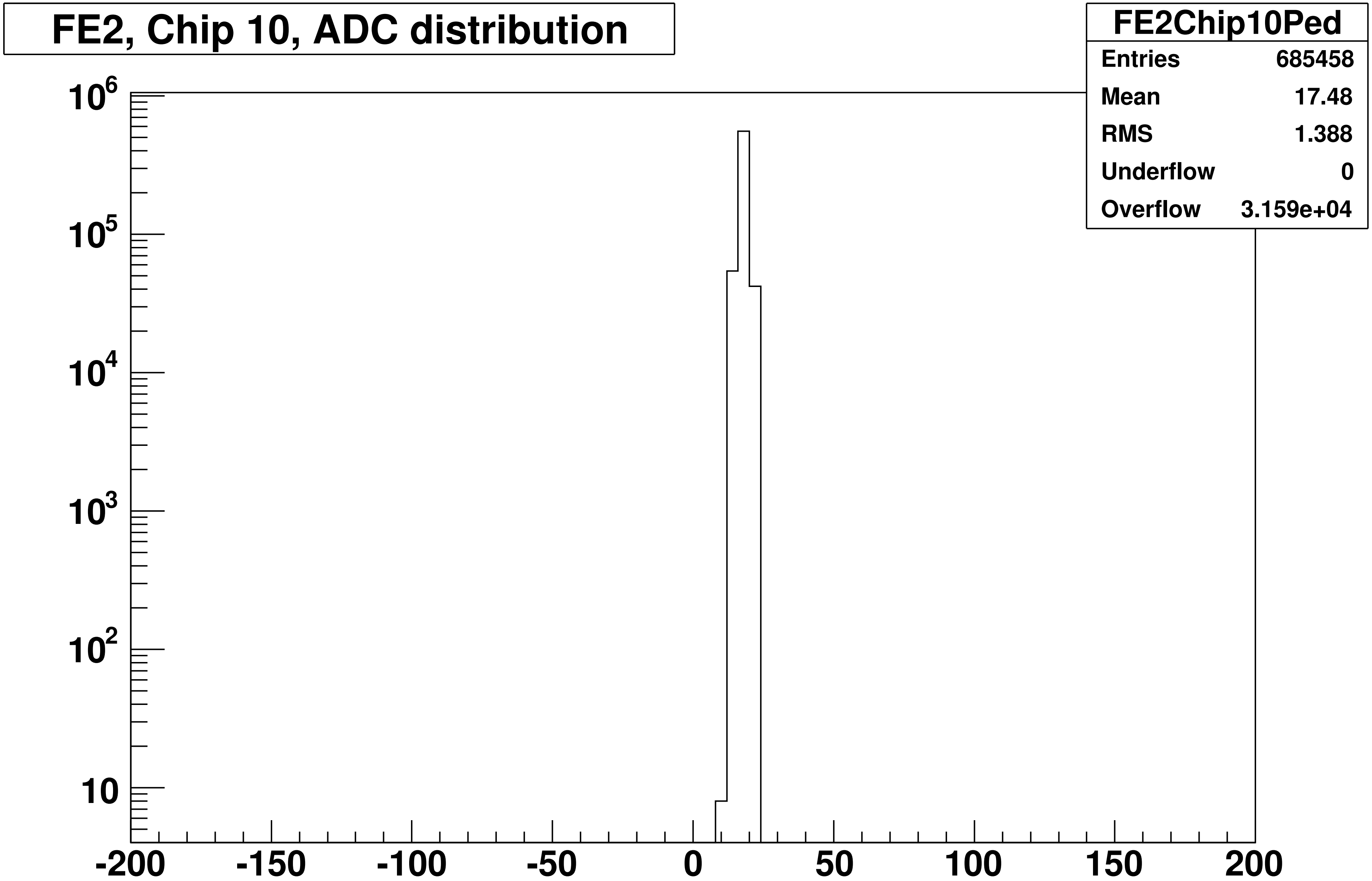

FE2, Chip 10, ADC distribution
FE2Chip10All
Entries 685458
Mean 582.3
RMS 2570
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000


FE2, Chip 10, ADC distribution
FE2Chip10Ped
Entries 685458
Mean 17.48
RMS 1.388
Underflow 0
Overflow 3.159e+04
10^6
10^5
10^4
10^3
10^2
10
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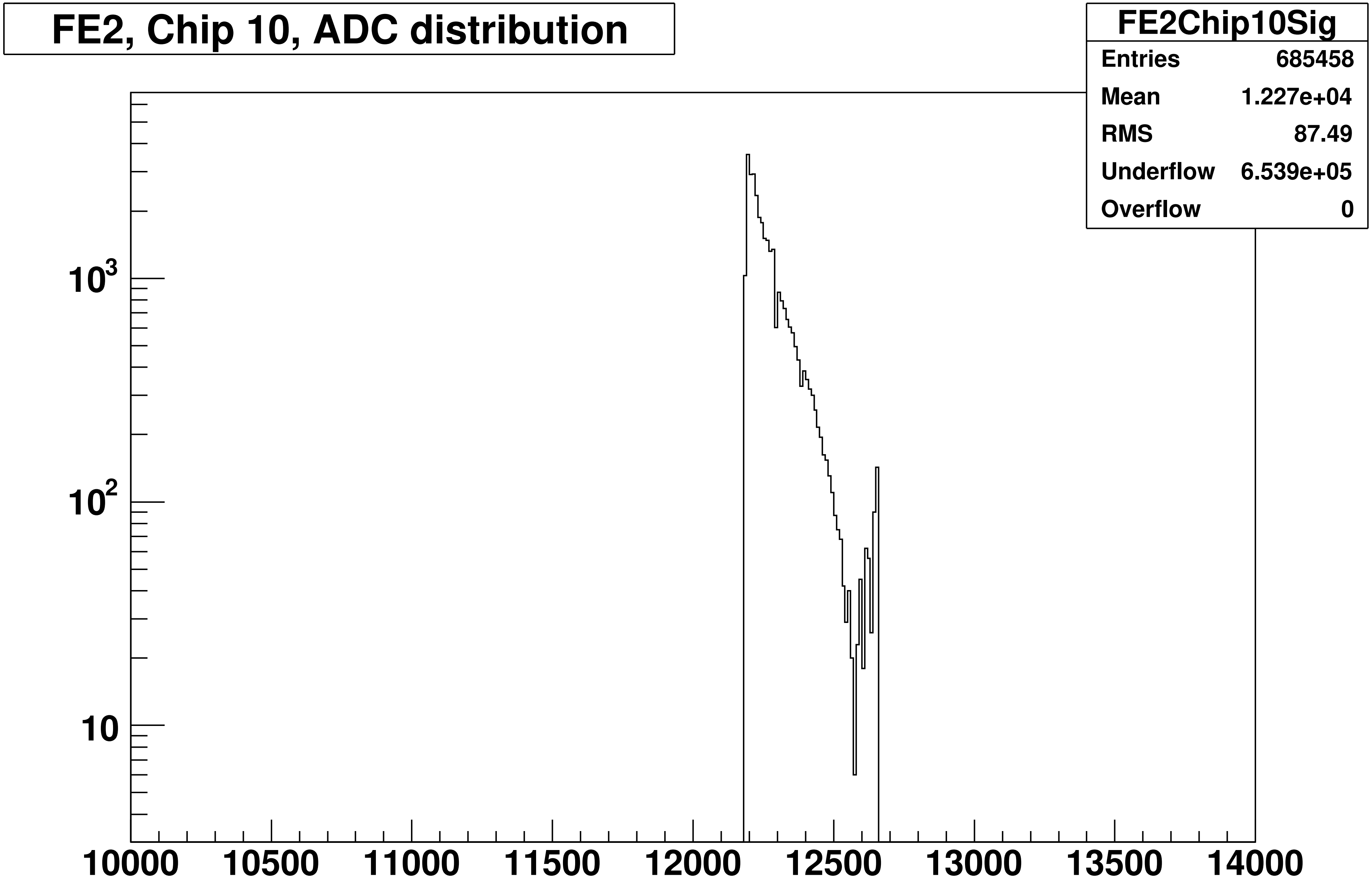
100
150
200


FE2, Chip 10, ADC distribution
FE2Chip10Sig
Entries 685458
Mean 1.227e+04
RMS 87.49
Underflow 6.539e+05
Overflow 0
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10^2
10
10000
10500
11000
11500
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12500
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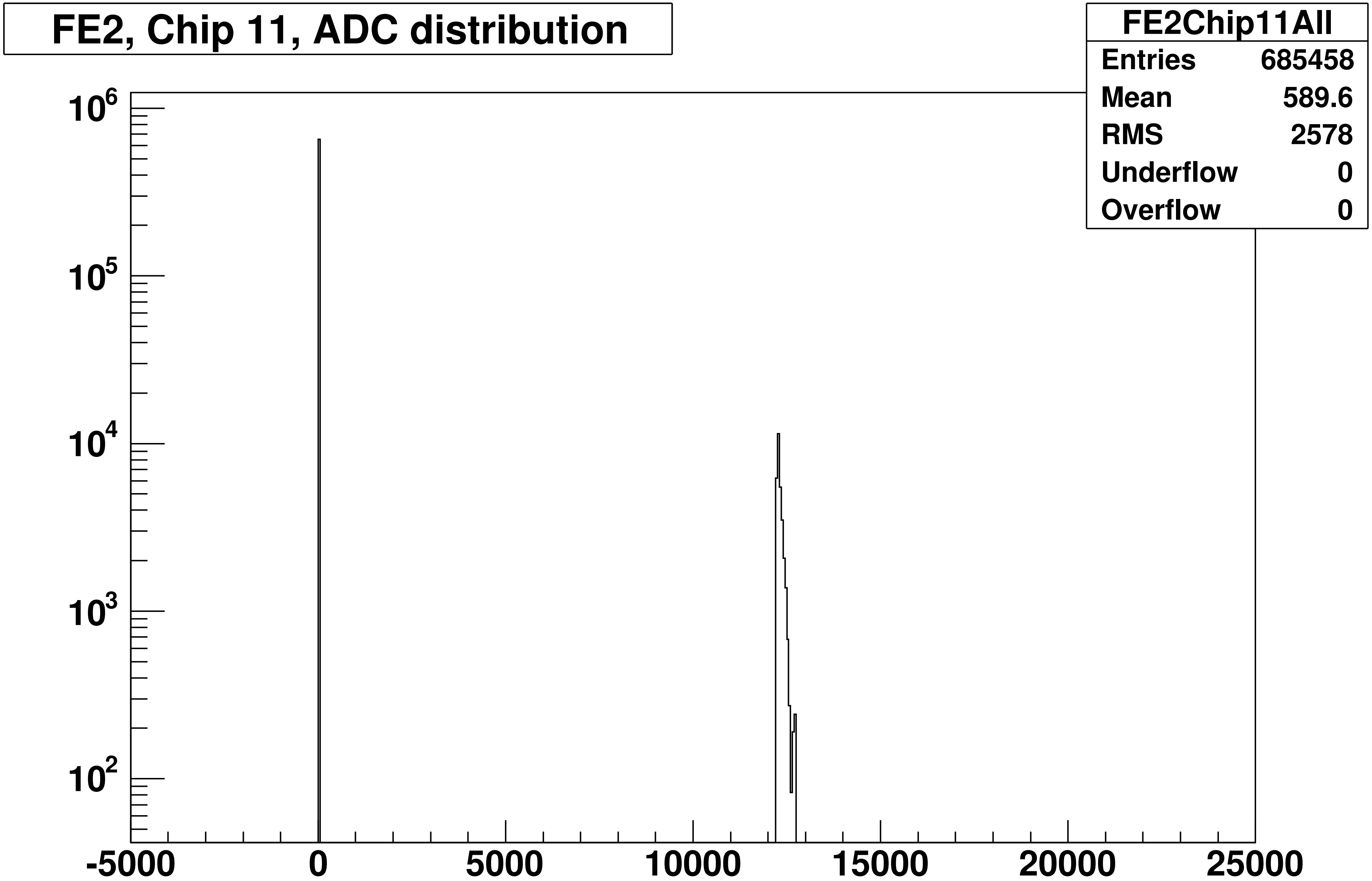

FE2, Chip 11, ADC distribution
FE2Chip11All
Entries 685458
Mean 589.6
RMS 2578
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
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15000
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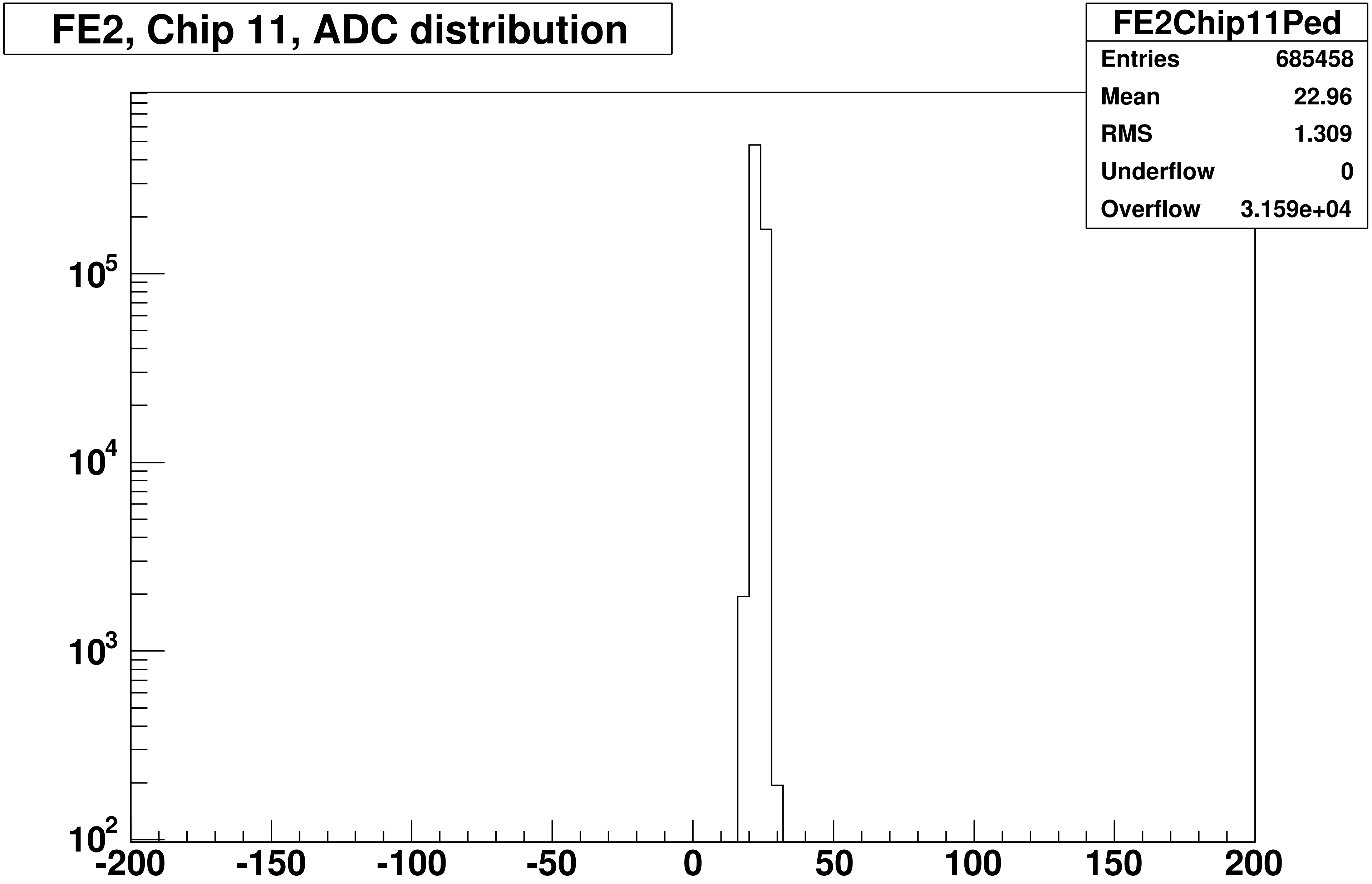

FE2, Chip 11, ADC distribution
FE2Chip11Ped
Entries 685458
Mean 22.96
RMS 1.309
Underflow 0
Overflow 3.159e+04
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10^4
10^3
10^2
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-100
-50
0
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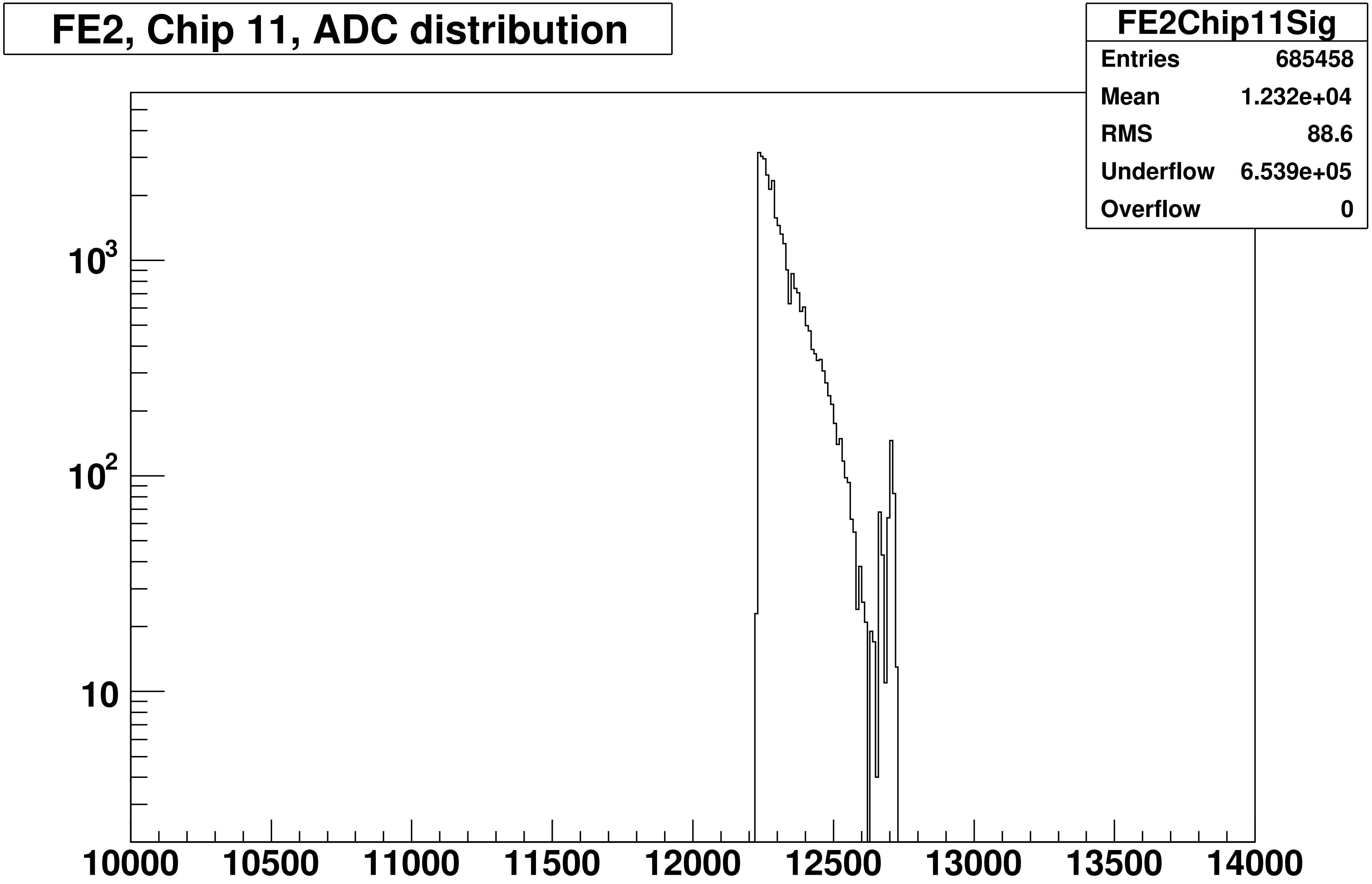
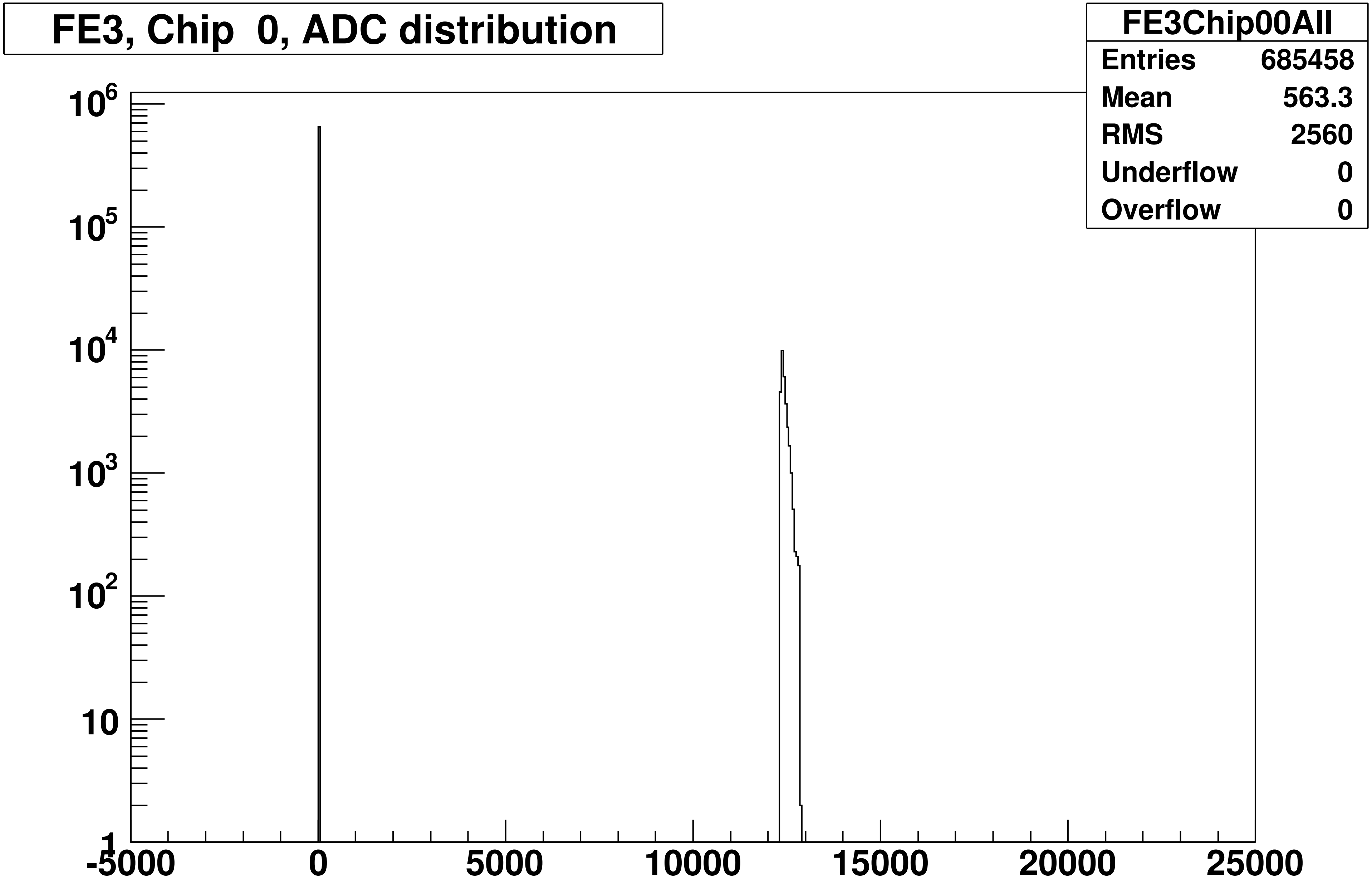
100
150
200


FE2, Chip 11, ADC distribution
FE2Chip11Sig
Entries 685458
Mean 1.232e+04
RMS 88.6
Underflow 6.539e+05
Overflow 0
10
10^2
10^3
10000
10500
11000
11500
12000
12500
13000
13500
14000


FE3, Chip 0, ADC distribution
FE3Chip00All
Entries 685458
Mean 563.3
RMS 2560
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
1
-5000
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10000
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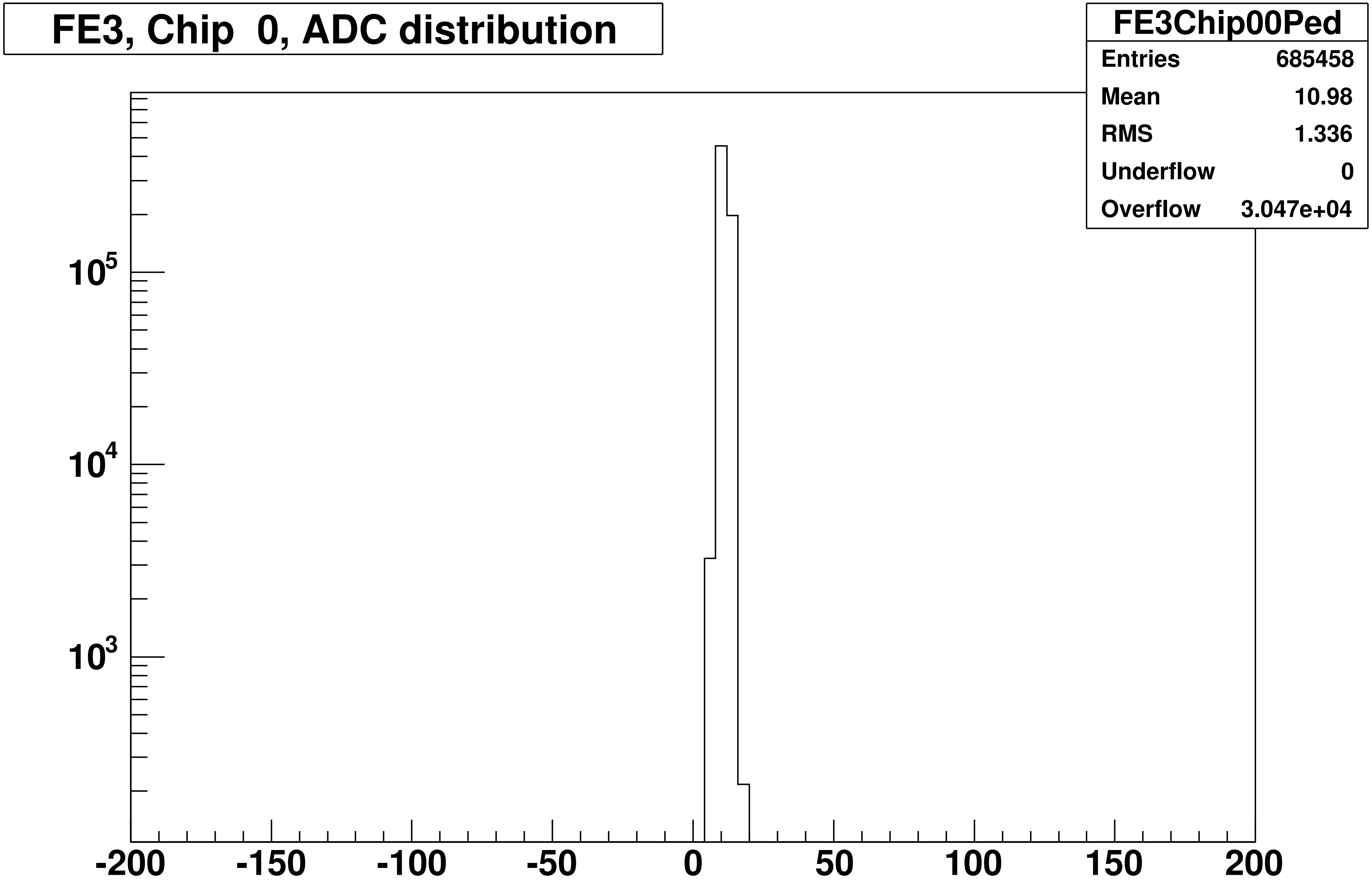
20000
25000


FE3, Chip 0, ADC distribution
FE3Chip00Ped
Entries 685458
Mean 10.98
RMS 1.336
Underflow 0
Overflow 3.047e+04
10^5
10^4
10^3
-200
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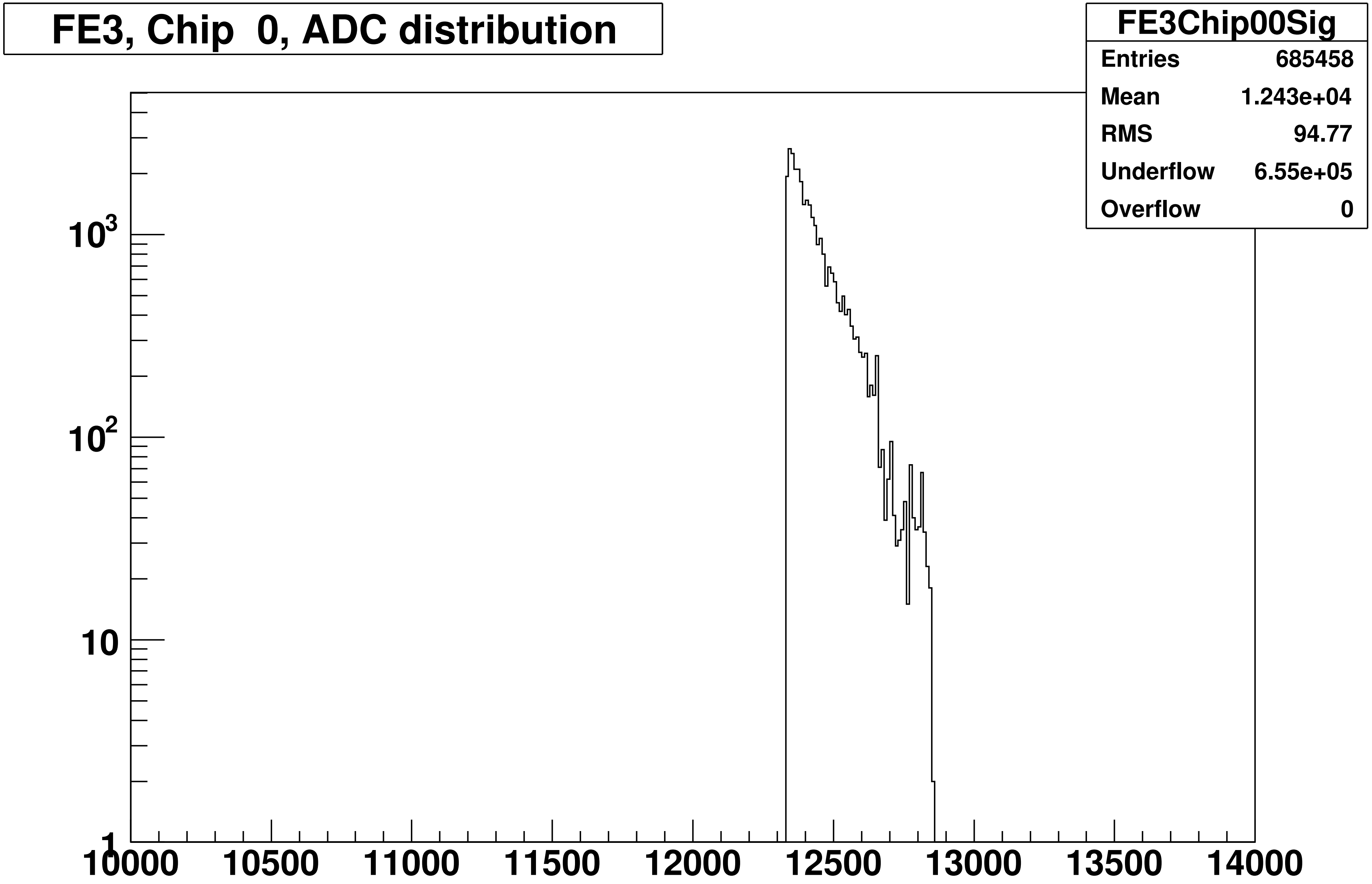
-100
-50
0
50
100
150
200


FE3, Chip 0, ADC distribution
FE3Chip00Sig
Entries 685458
Mean 1.243e+04
RMS 94.77
Underflow 6.55e+05
Overflow 0
10^3
10^2
10
1
10000
10500
11000
11500
12000
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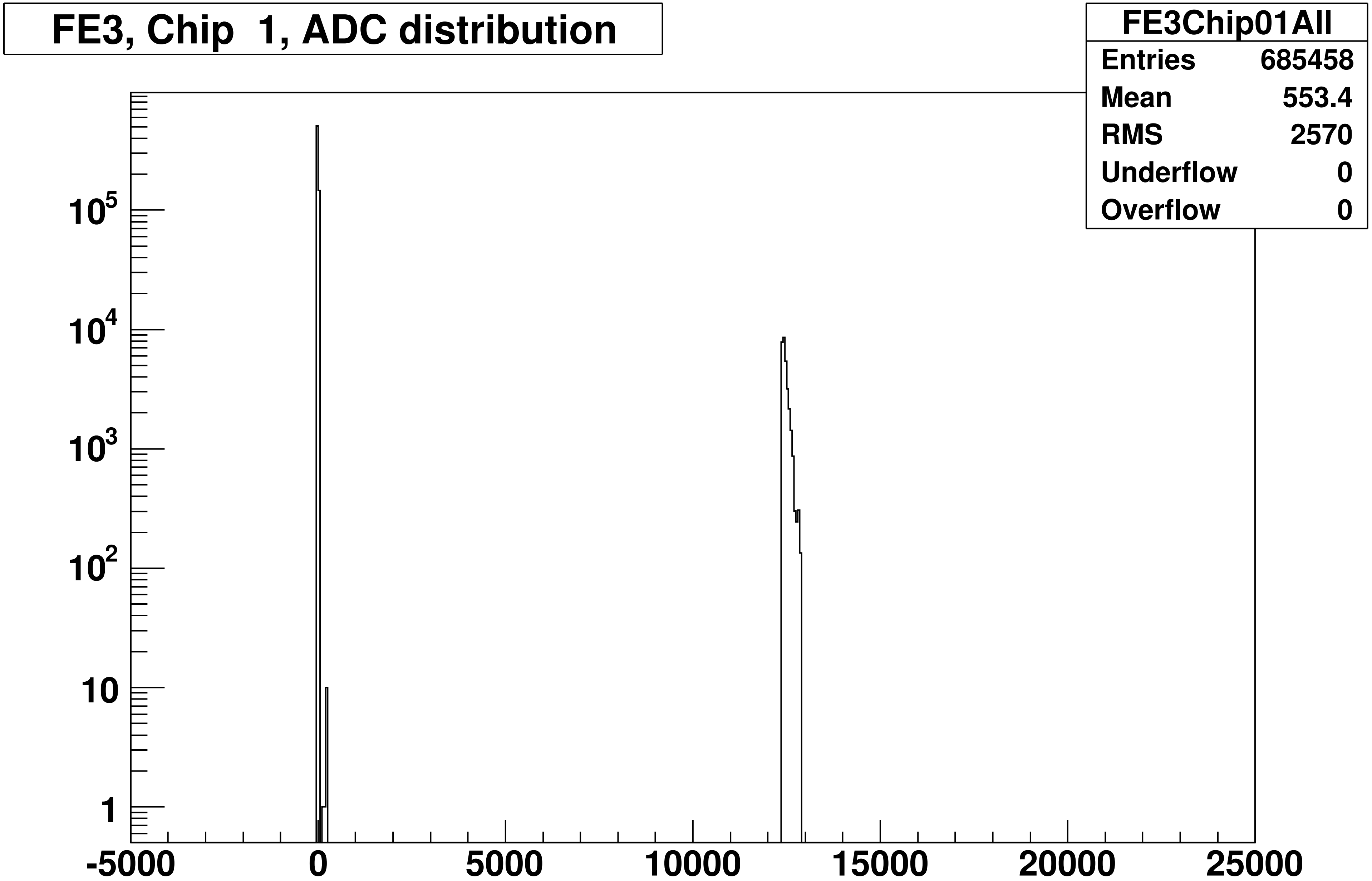
13000
13500
14000


FE3, Chip 1, ADC distribution
FE3Chip01All
Entries 685458
Mean 553.4
RMS 2570
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
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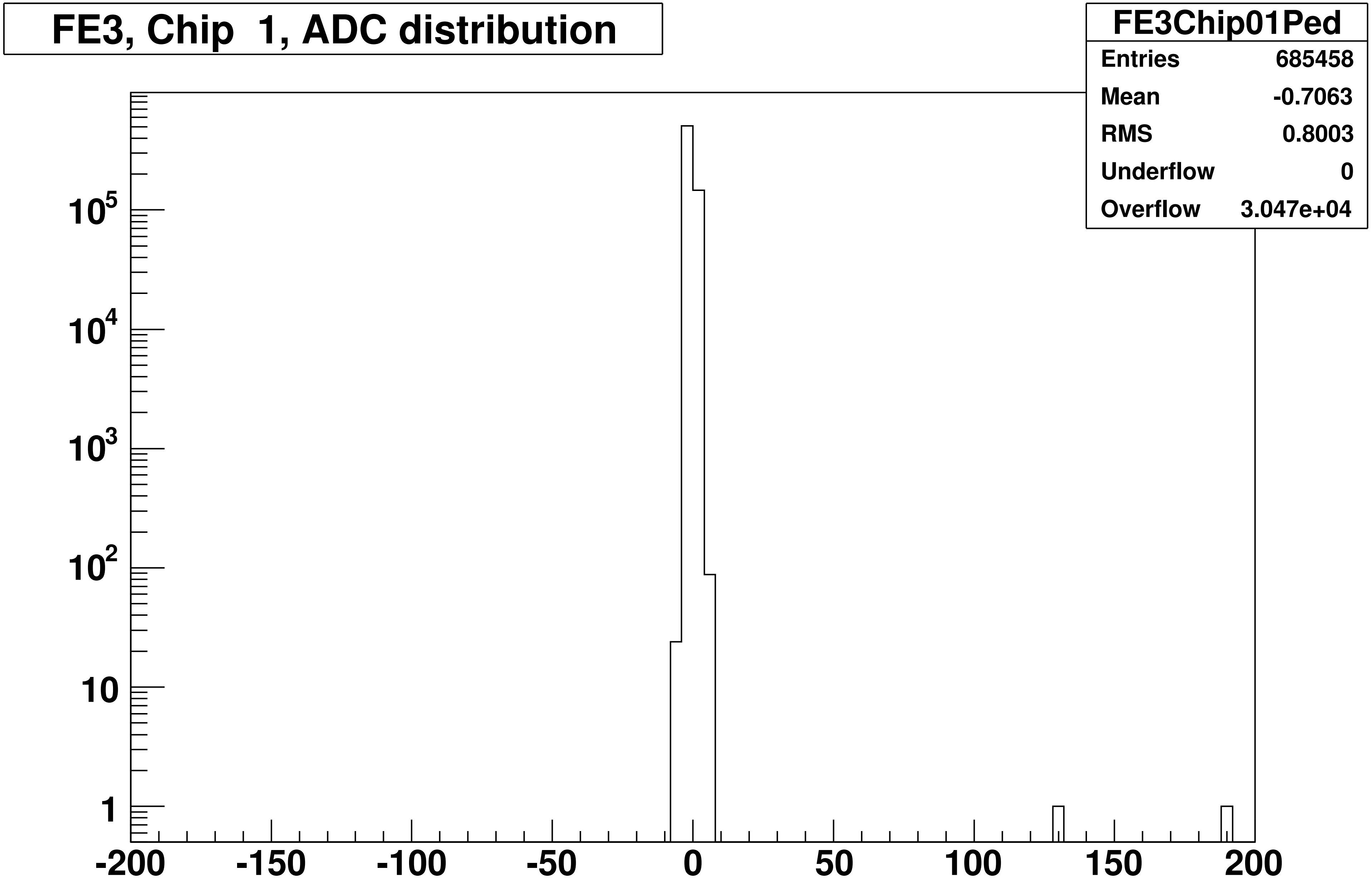
10000
15000
20000
25000


FE3, Chip 1, ADC distribution
FE3Chip01Ped
Entries 685458
Mean -0.7063
RMS 0.8003
Underflow 0
Overflow 3.047e+04
10^5
10^4
10^3
10^2
10
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-200
-150
-100
-50
0
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150
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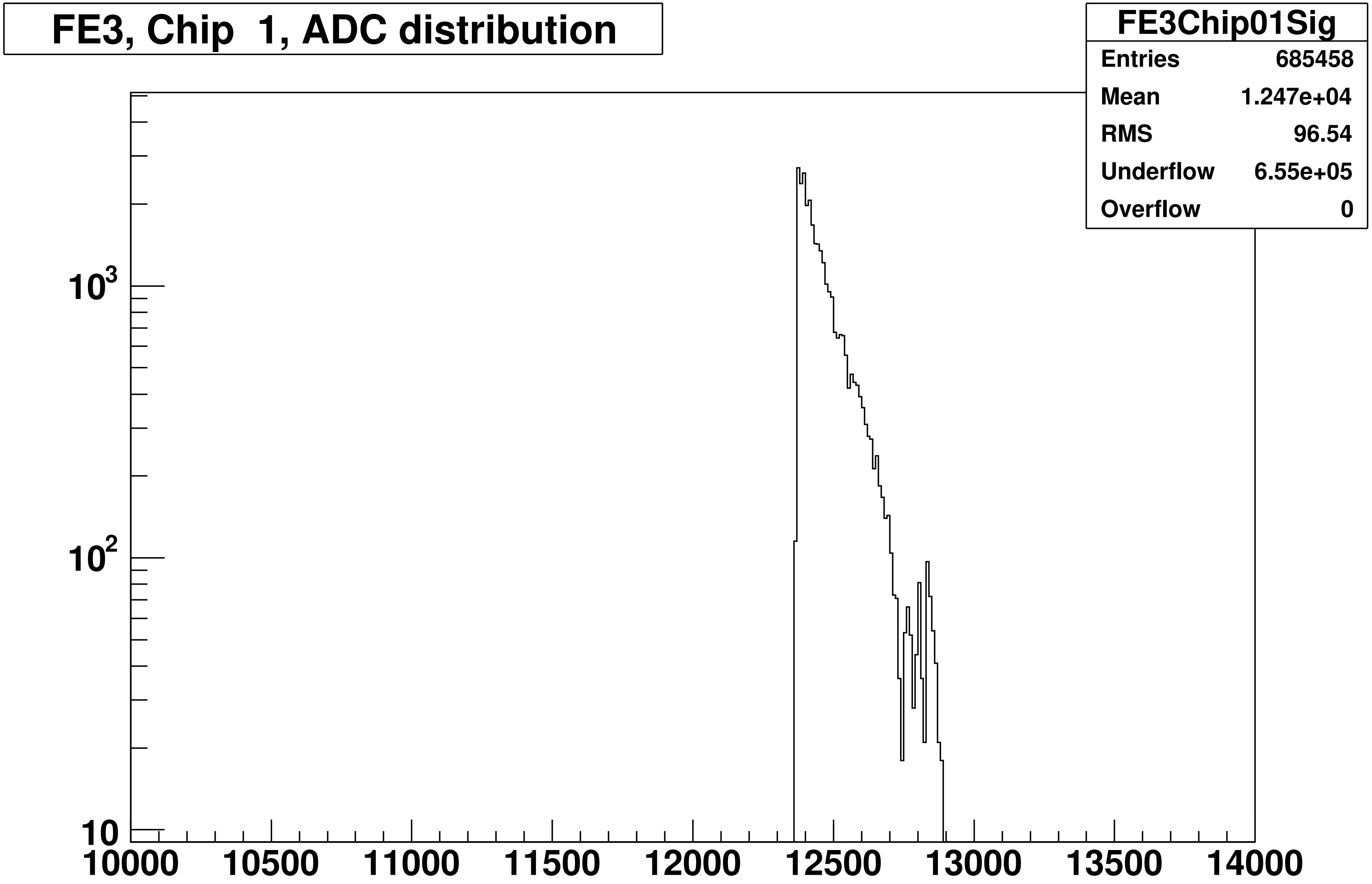

FE3, Chip 1, ADC distribution
FE3Chip01Sig
Entries 685458
Mean 1.247e+04
RMS 96.54
Underflow 6.55e+05
Overflow 0
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10^2
10^3
10000
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11000
11500
12000
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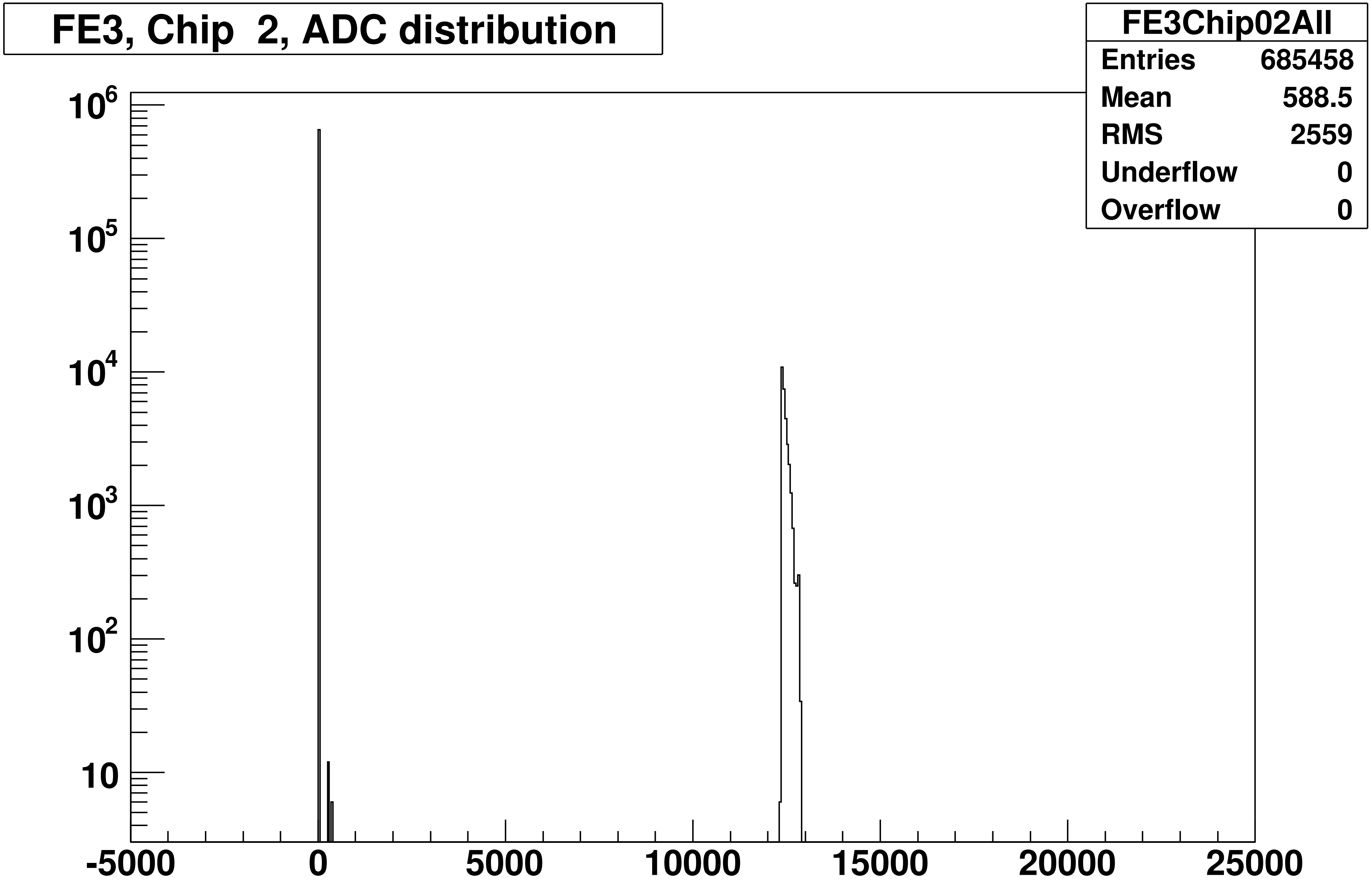

FE3, Chip 2, ADC distribution
FE3Chip02All
Entries 685458
Mean 588.5
RMS 2559
Underflow 0
Overflow 0
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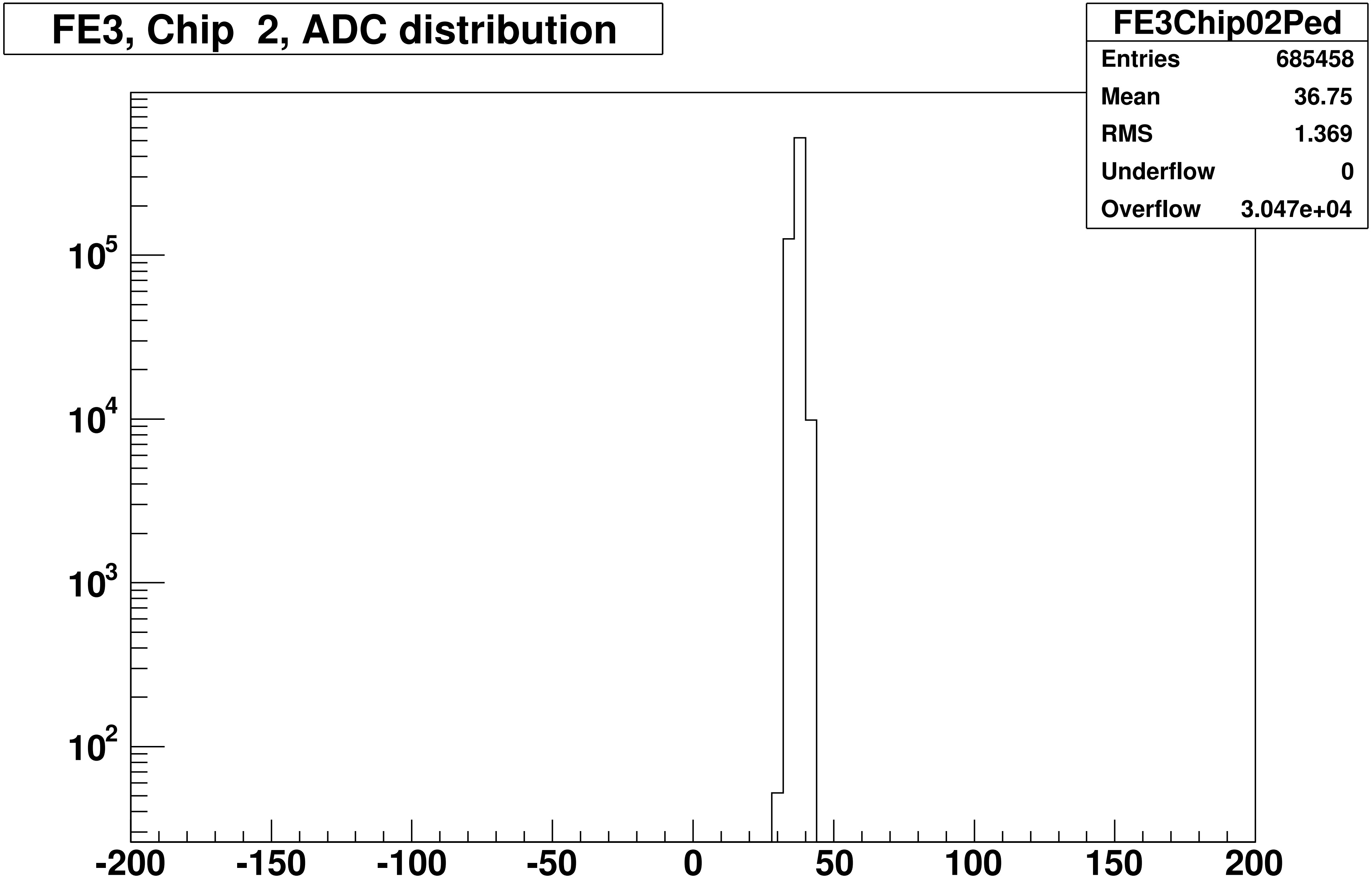
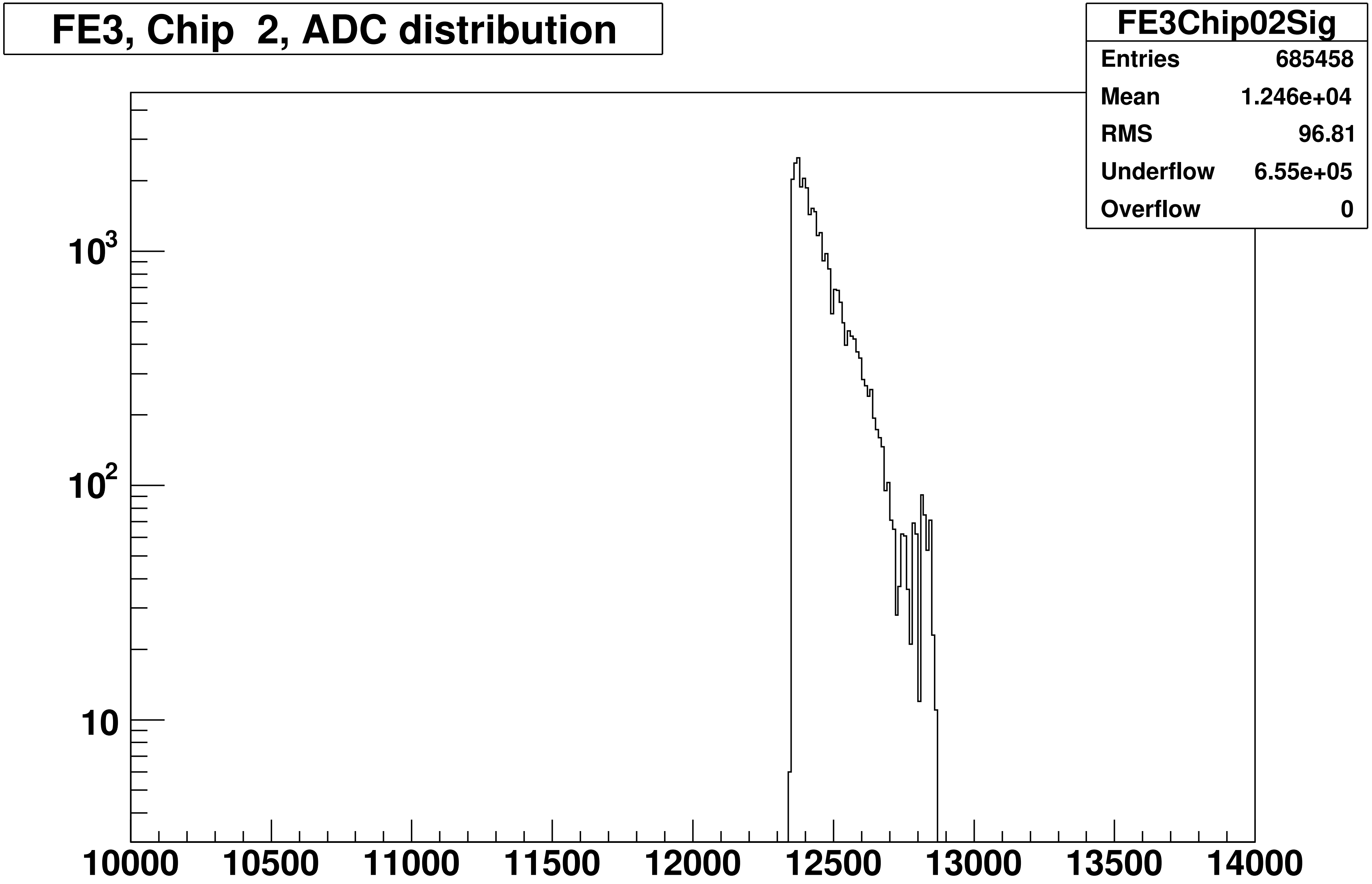
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE3, Chip 2, ADC distribution
FE3Chip02Ped
Entries 685458
Mean 36.75
RMS 1.369
Underflow 0
Overflow 3.047e+04
10^5
10^4
10^3
10^2
-200
-150
-100
-50
0
50
100
150
200



FE3, Chip 2, ADC distribution
FE3Chip02Sig
Entries 685458
Mean 1.246e+04
RMS 96.81
Underflow 6.55e+05
Overflow 0
10
10^2
10^3
10000
10500
11000
11500
12000
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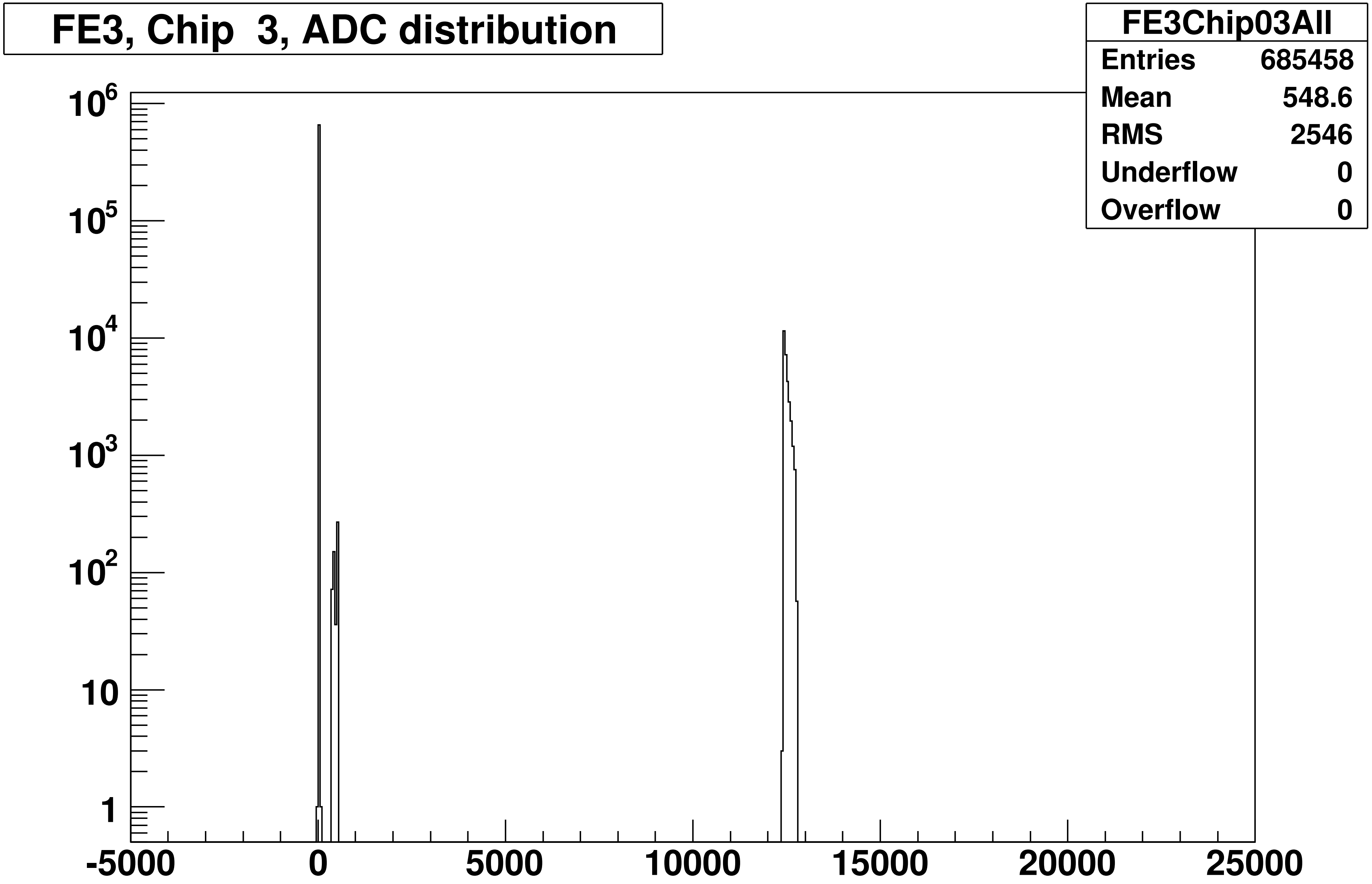

FE3, Chip 3, ADC distribution
FE3Chip03All
Entries 685458
Mean 548.6
RMS 2546
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
1
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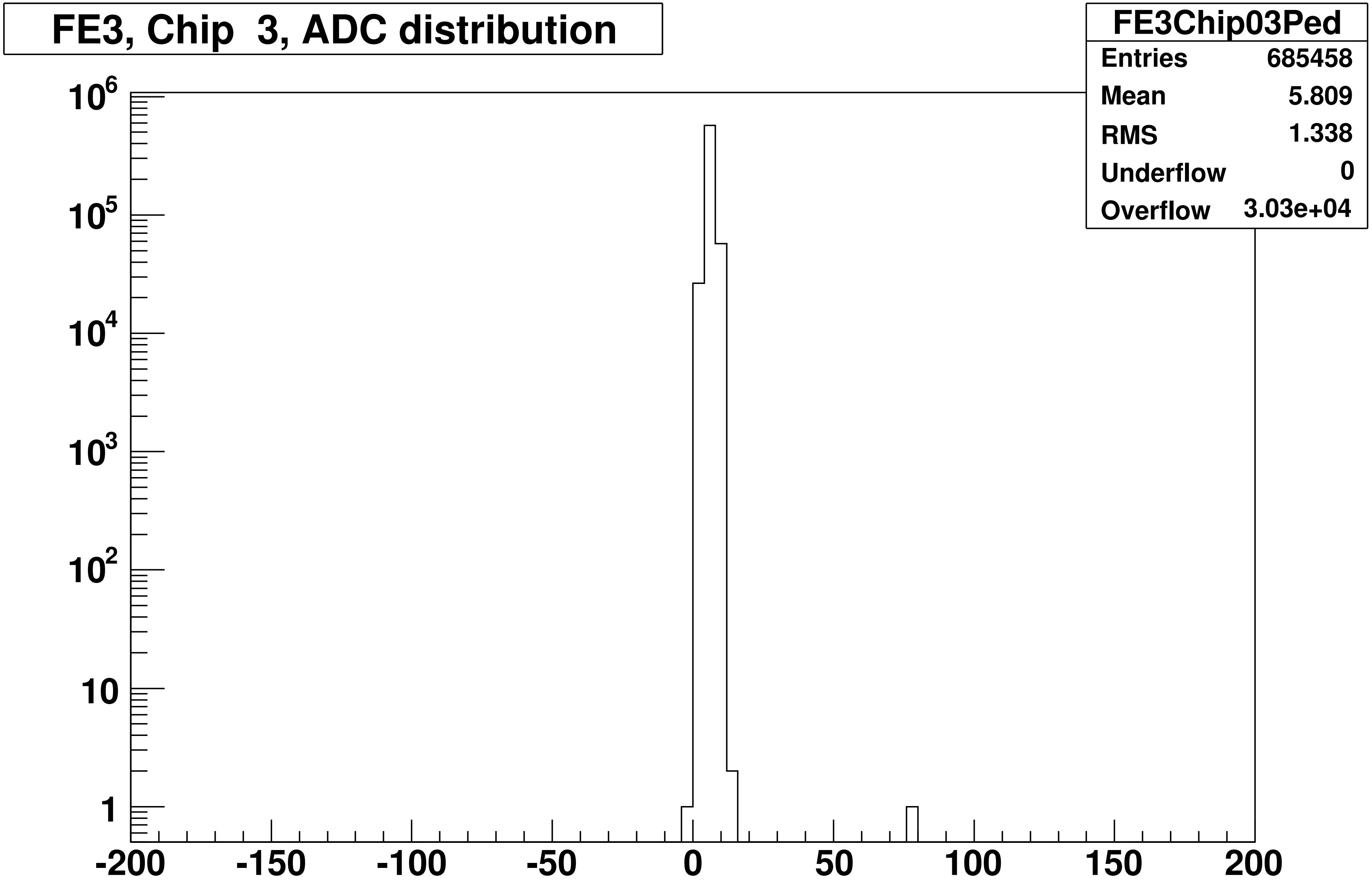
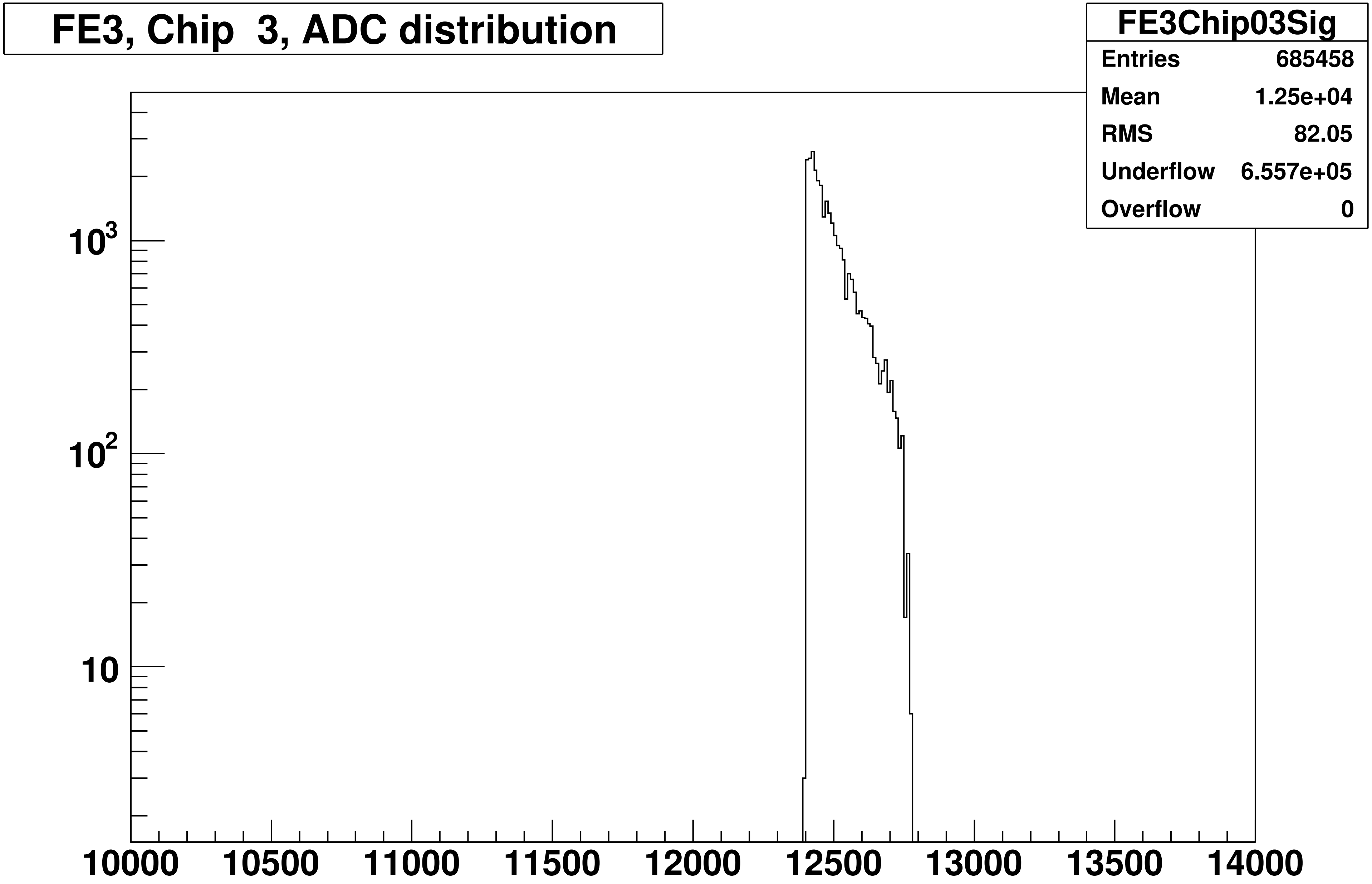
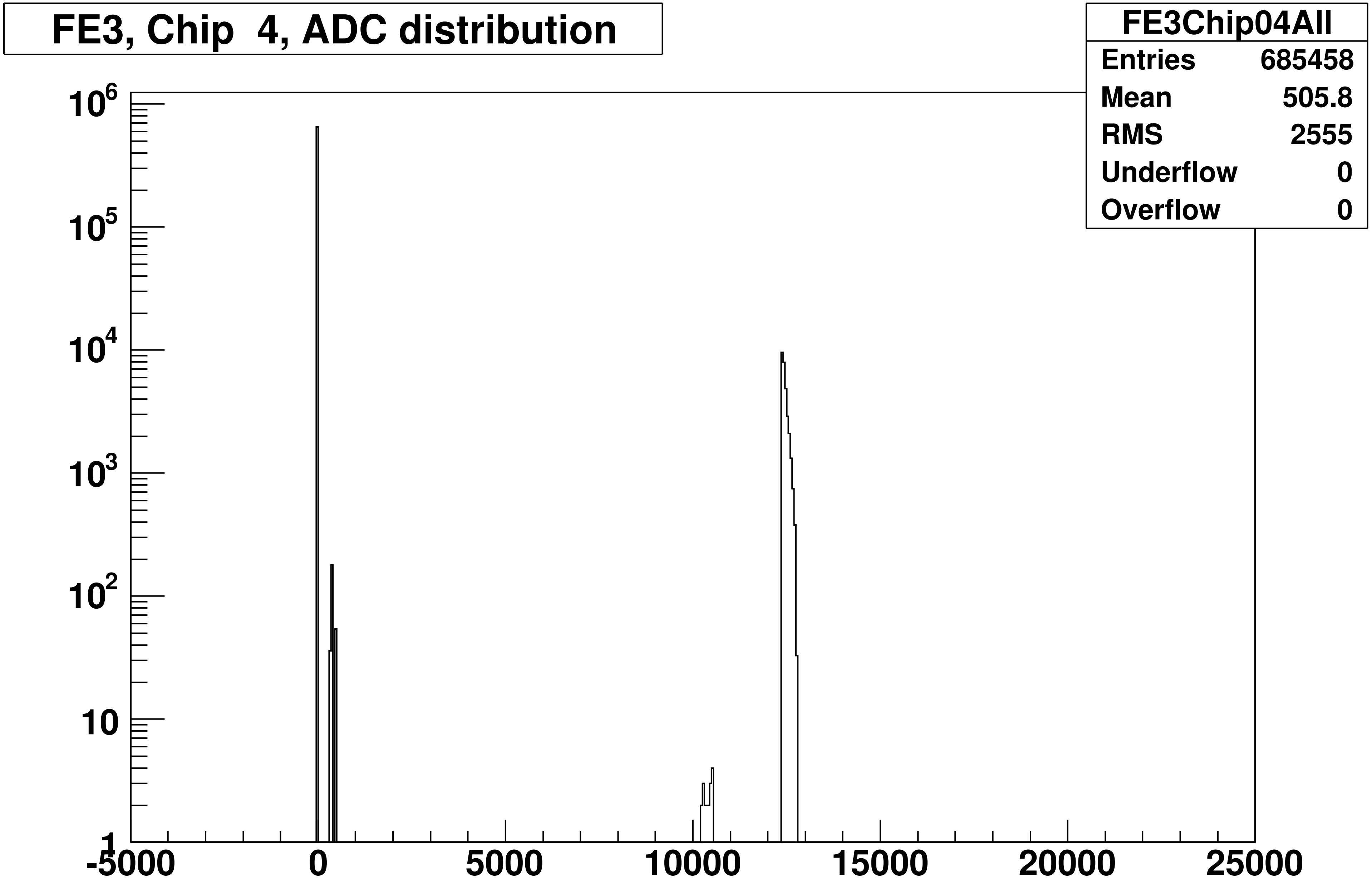
5000
10000
15000
20000
25000



FE3, Chip 3, ADC distribution
FE3Chip03Ped
Entries 685458
Mean 5.809
RMS 1.338
Underflow 0
Overflow 3.03e+04
10^6
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
200


FE3, Chip 3, ADC distribution
FE3Chip03Sig
Entries 685458
Mean 1.25e+04
RMS 82.05
Underflow 6.557e+05
Overflow 0
10^3
10^2
10
10000
10500
11000
11500
12000
12500
13000
13500
14000


FE3, Chip 4, ADC distribution
FE3Chip04All
Entries 685458
Mean 505.8
RMS 2555
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
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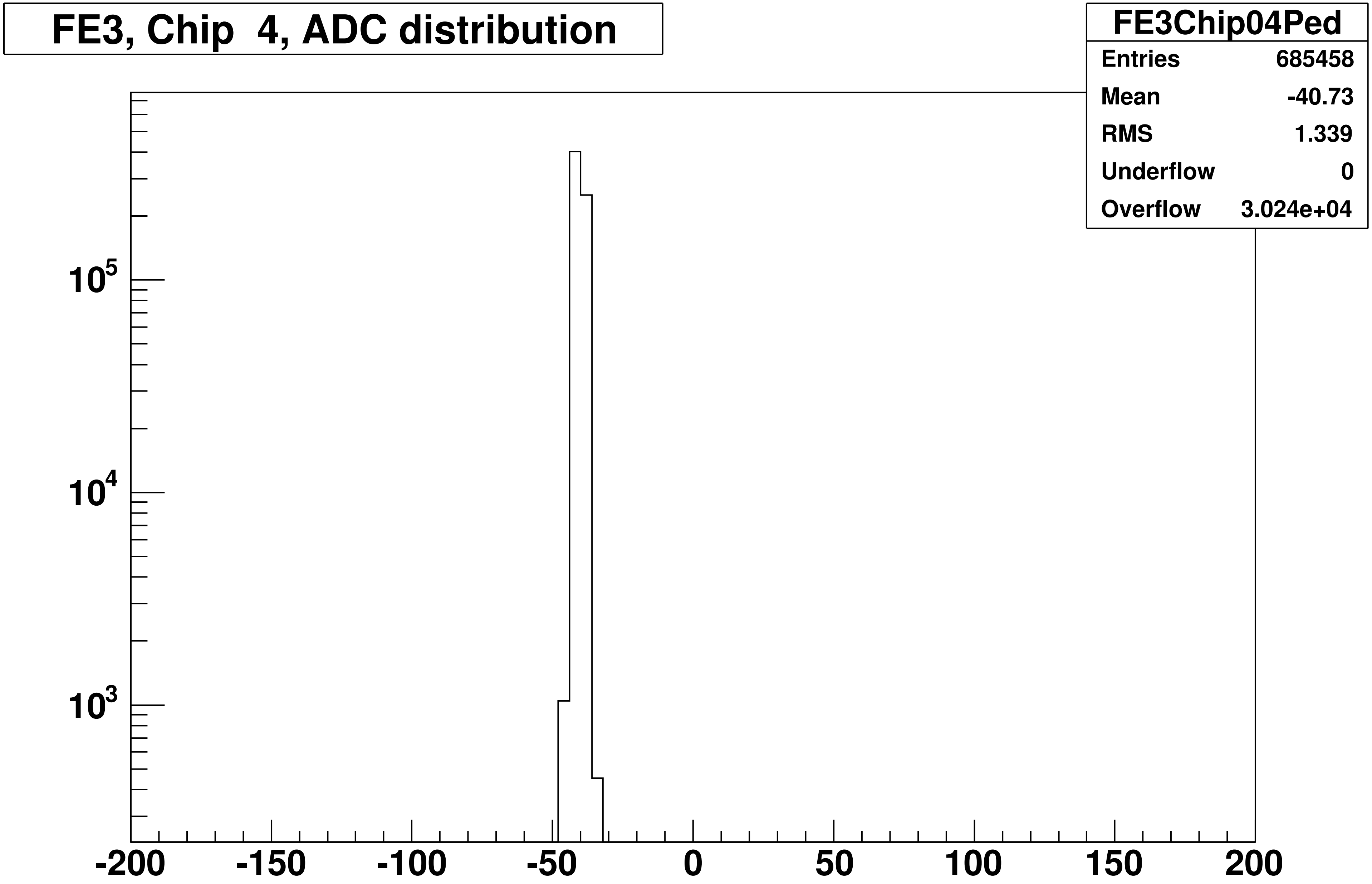
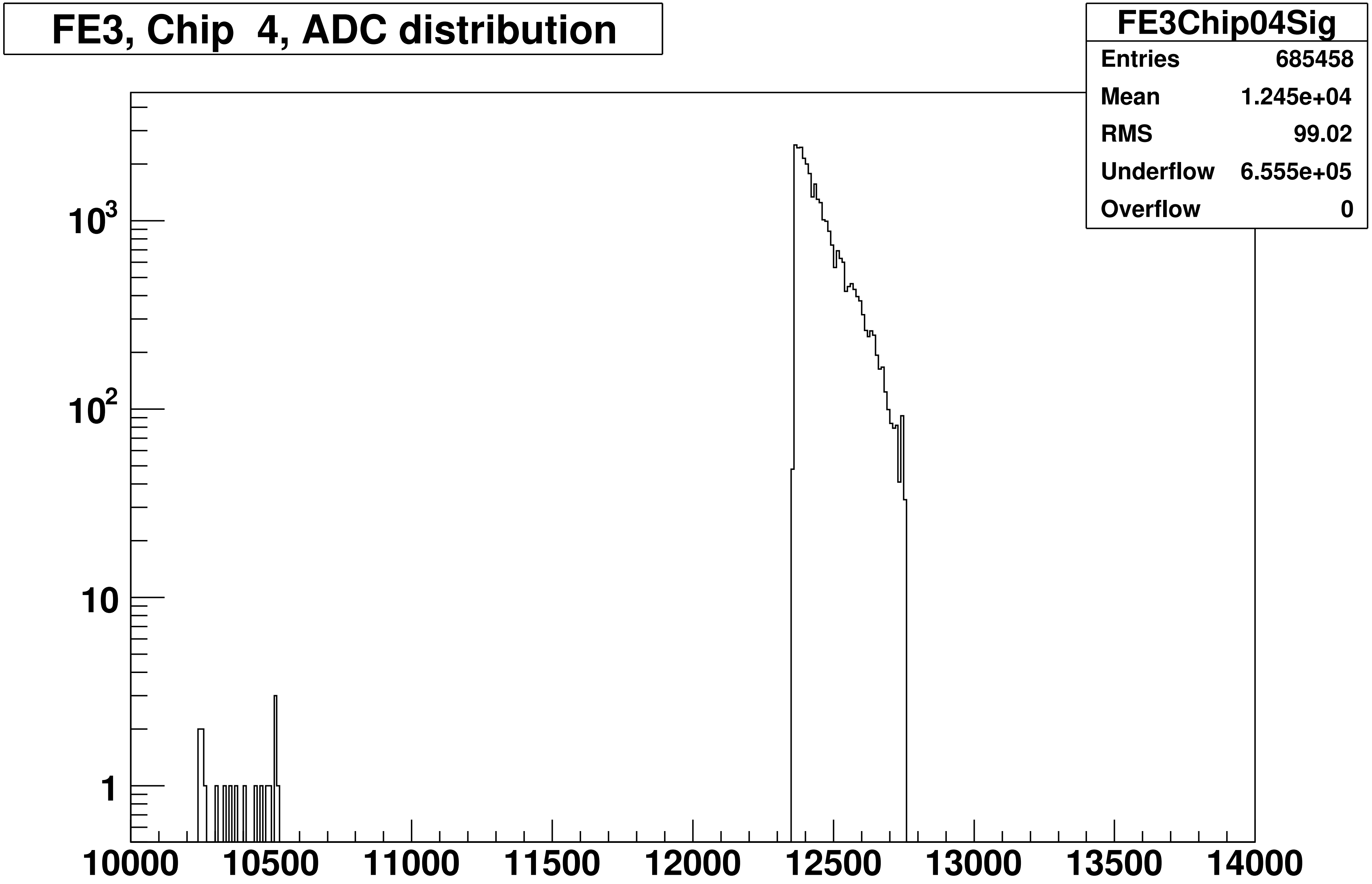


FE3, Chip 4, ADC distribution
FE3Chip04Ped
Entries 685458
Mean -40.73
RMS 1.339
Underflow 0
Overflow 3.024e+04
10^5
10^4
10^3
-200 -150 -100 -50 0 50 100 150 200


FE3, Chip 4, ADC distribution
FE3Chip04Sig
Entries 685458
Mean 1.245e+04
RMS 99.02
Underflow 6.555e+05
Overflow 0
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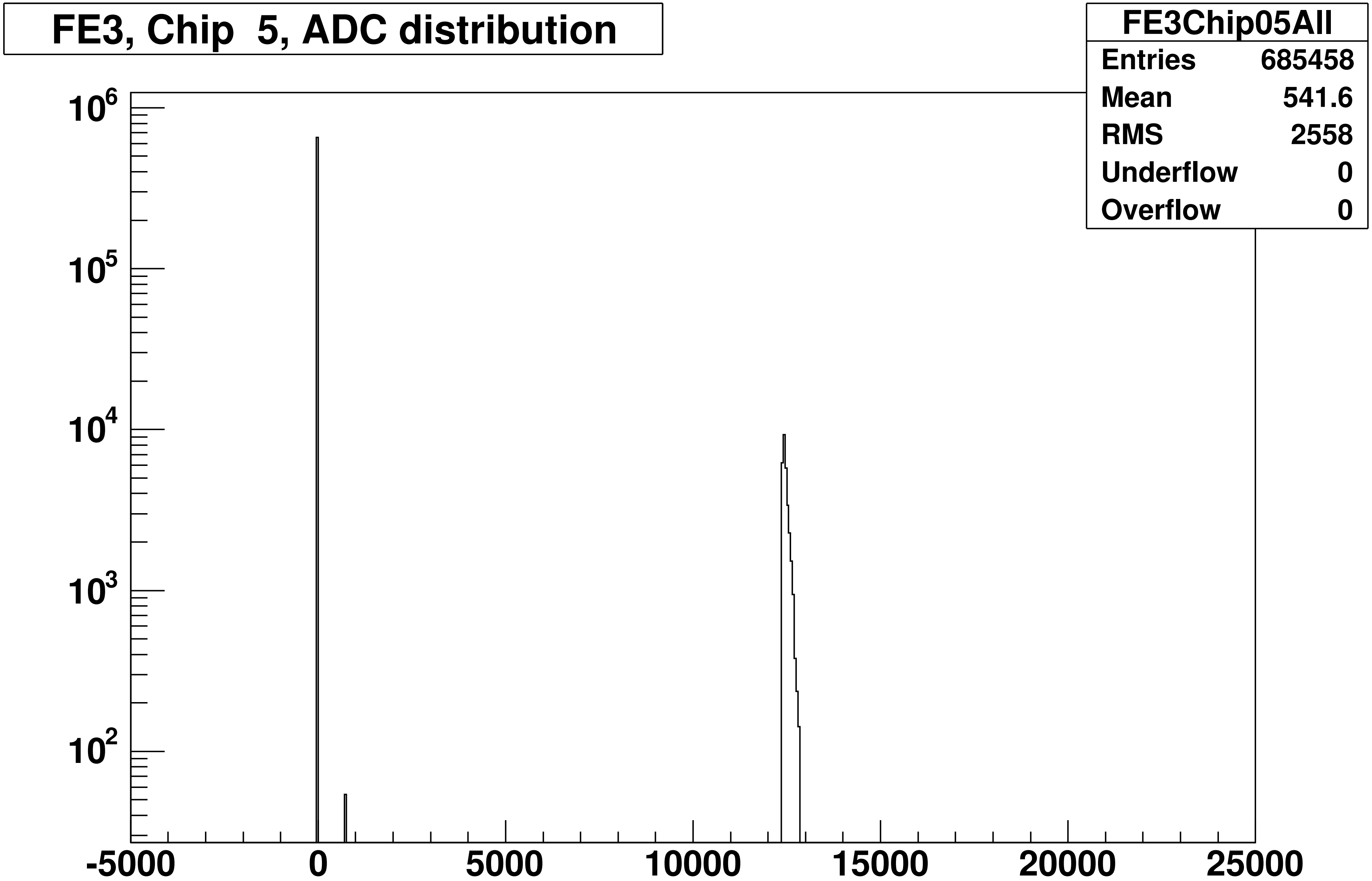
FE3, Chip 5, ADC distribution
FE3Chip05All
Entries 685458
Mean 541.6
RMS 2558
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
-5000
0
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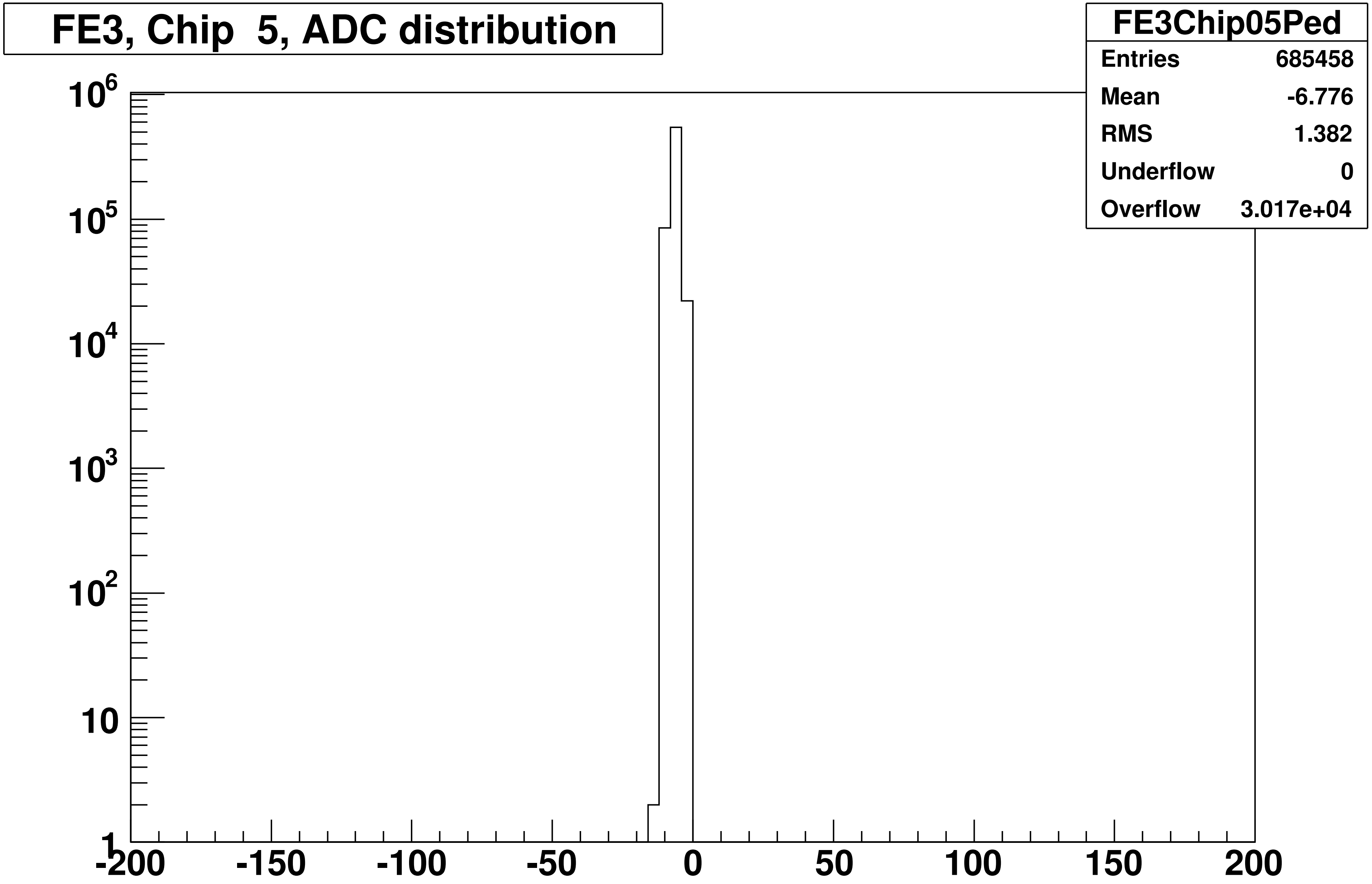
10000
15000
20000
25000



FE3, Chip 5, ADC distribution
FE3Chip05Ped
Entries 685458
Mean -6.776
RMS 1.382
Underflow 0
Overflow 3.017e+04
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10^5
10^4
10^3
10^2
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150
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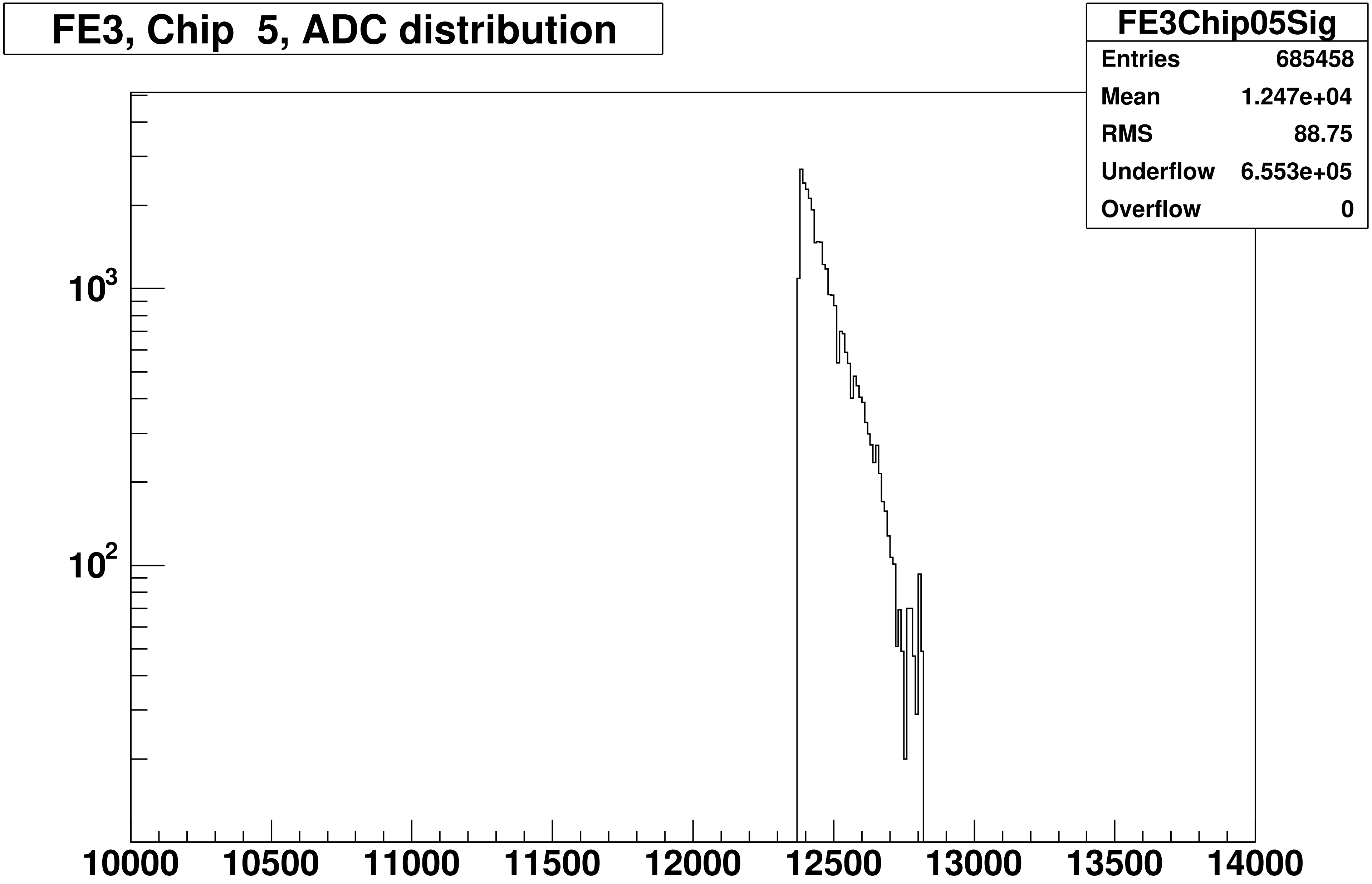
FE3, Chip 5, ADC distribution
FE3Chip05Sig
Entries 685458
Mean 1.247e+04
RMS 88.75
Underflow 6.553e+05
Overflow 0
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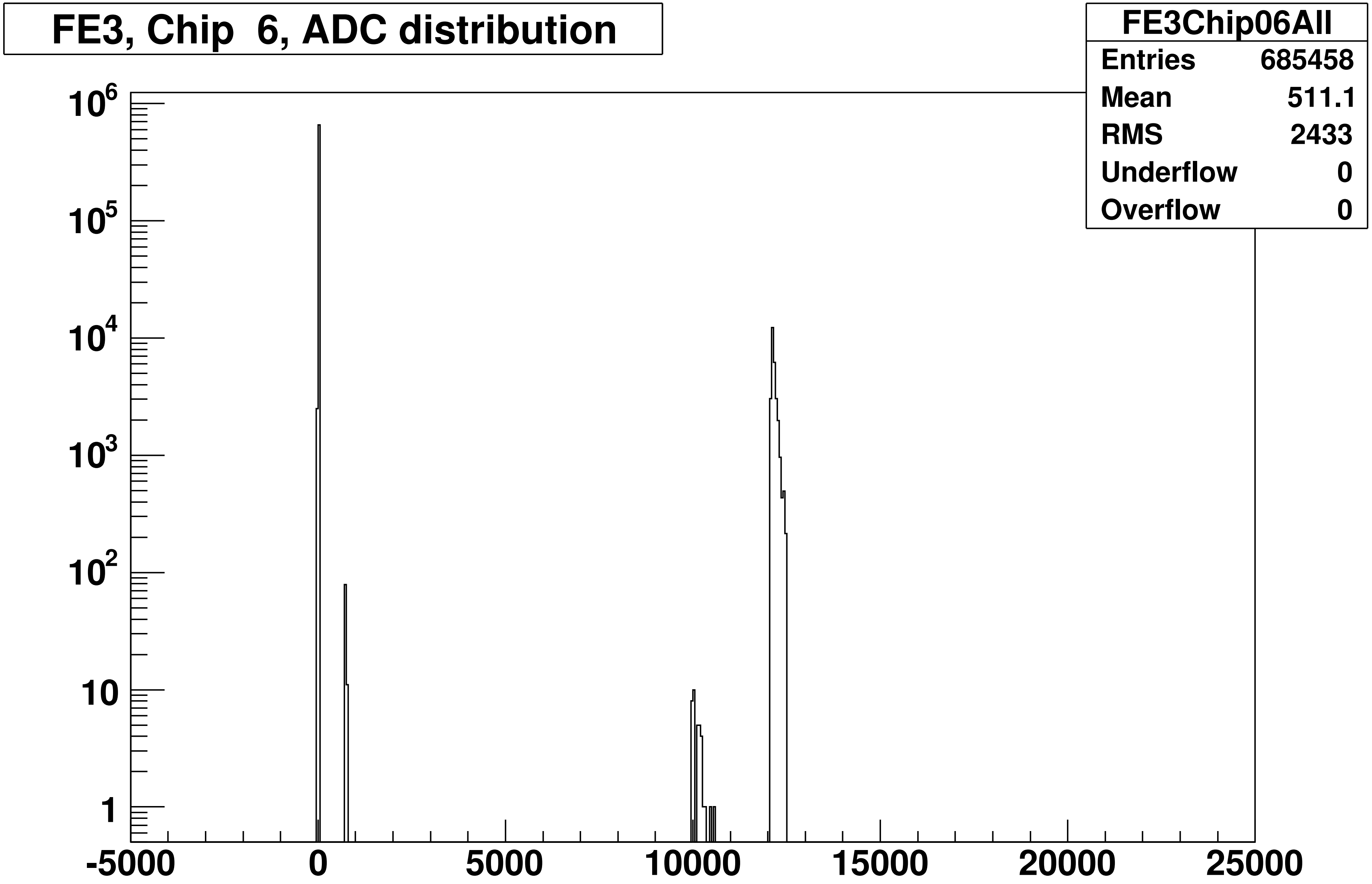

FE3, Chip 6, ADC distribution
FE3Chip06All
Entries 685458
Mean 511.1
RMS 2433
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
1
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0
5000
10000
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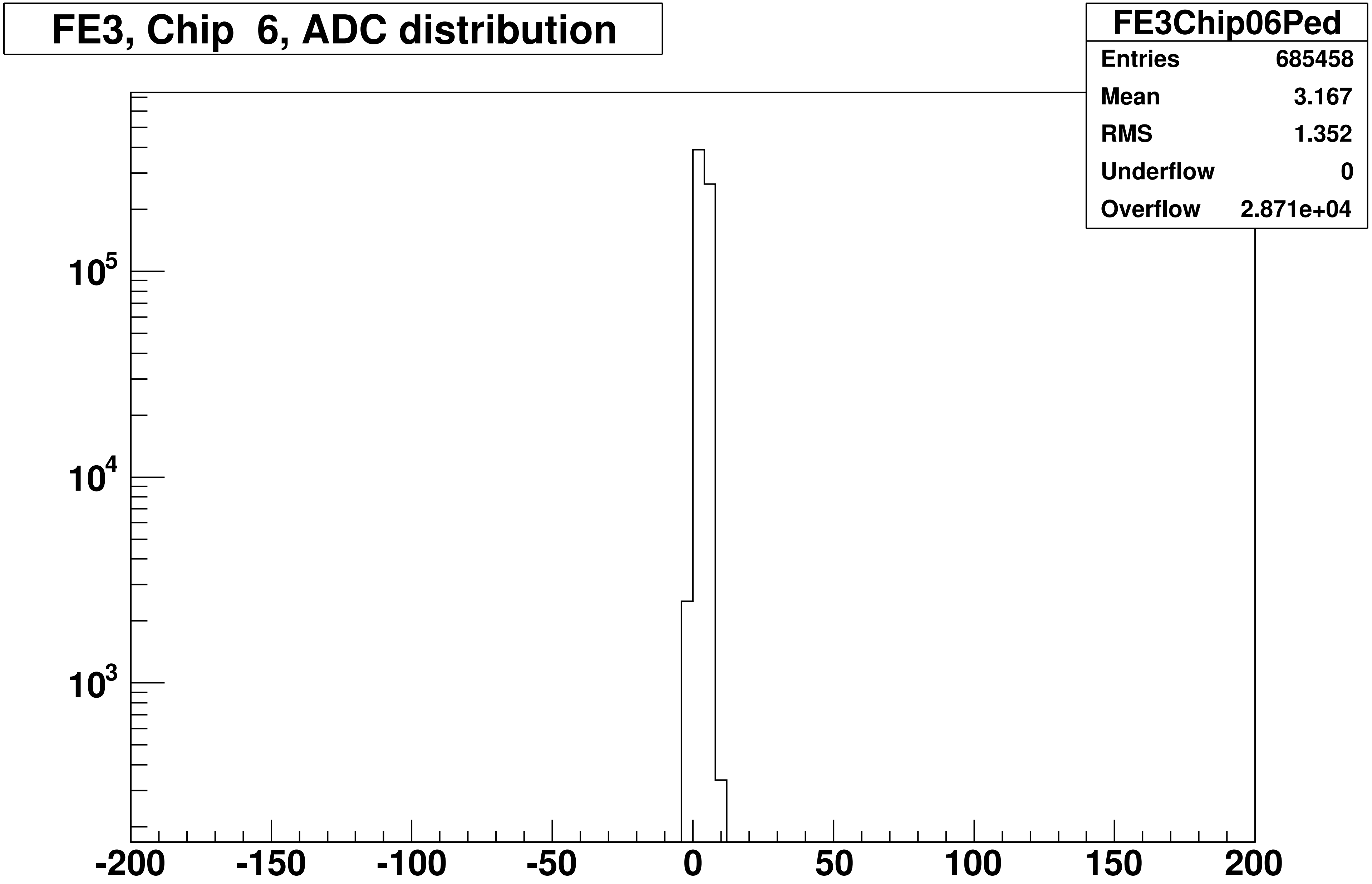
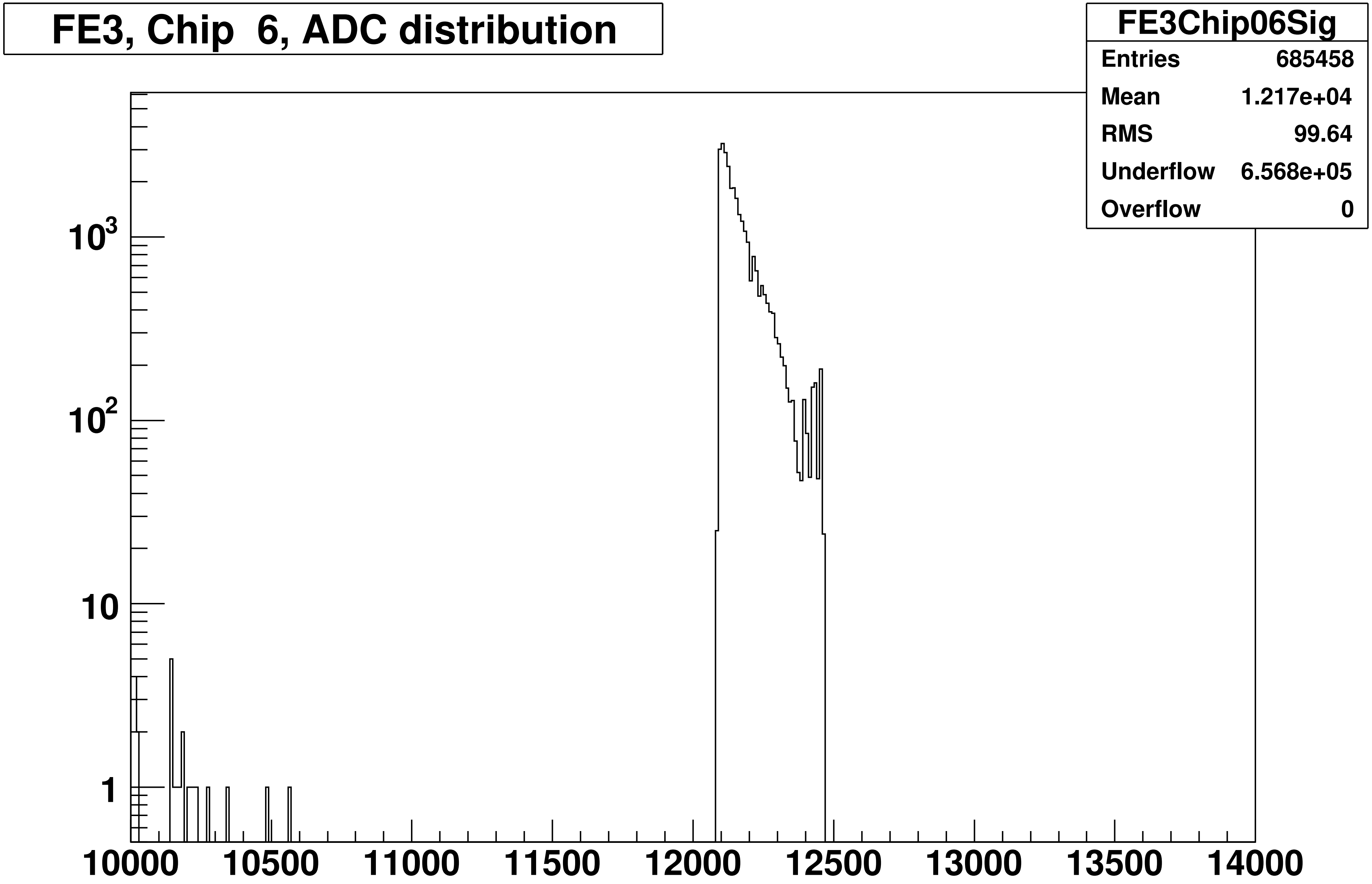
25000



FE3, Chip 6, ADC distribution
FE3Chip06Ped
Entries 685458
Mean 3.167
RMS 1.352
Underflow 0
Overflow 2.871e+04
10^5
10^4
10^3
-200
-150
-100
-50
0
50
100
150
200



FE3, Chip 6, ADC distribution
FE3Chip06Sig
Entries 685458
Mean 1.217e+04
RMS 99.64
Underflow 6.568e+05
Overflow 0
10^3
10^2
10
1
10000
10500
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11500
12000
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13500
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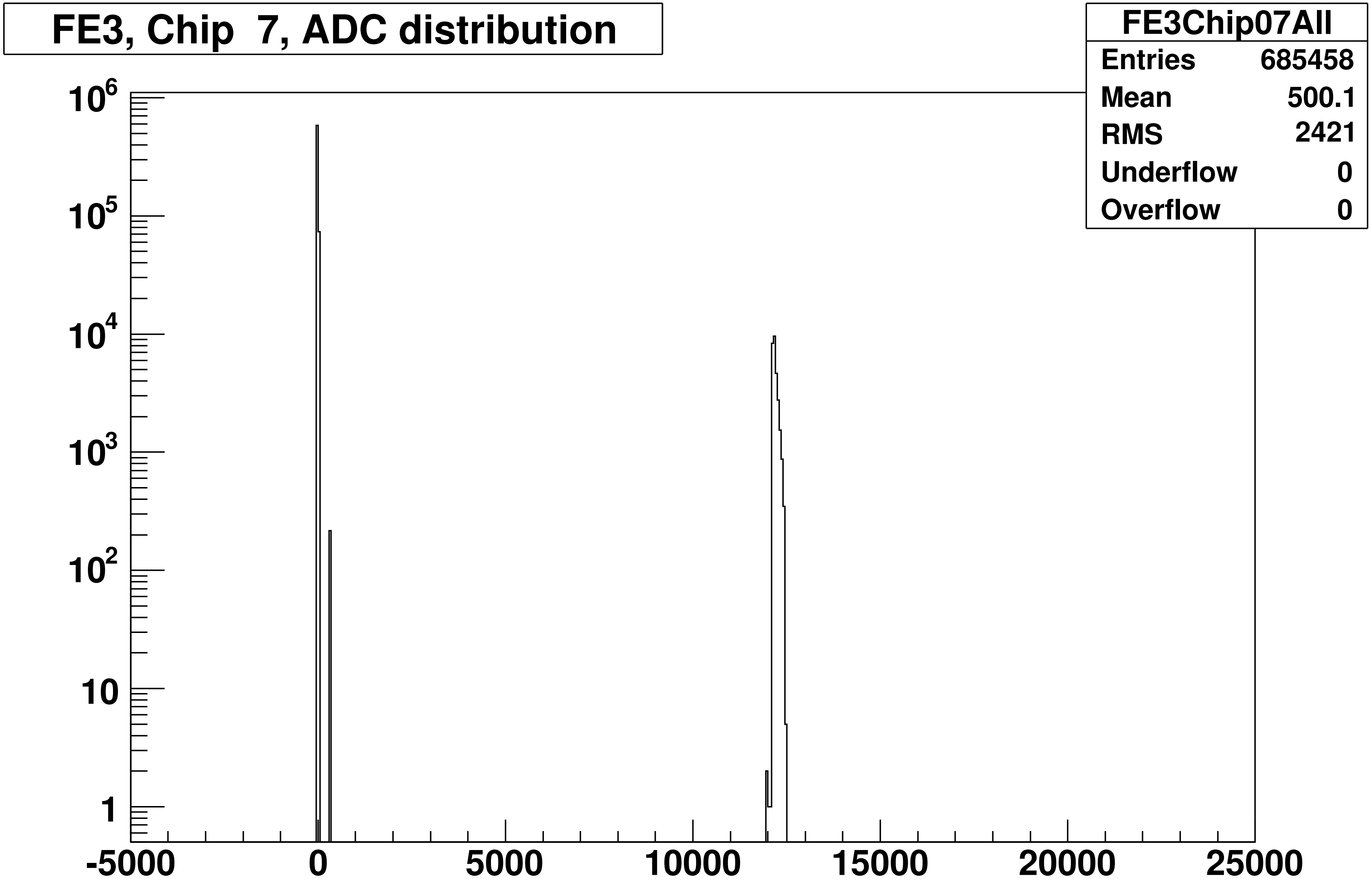

FE3, Chip 7, ADC distribution
FE3Chip07All
Entries 685458
Mean 500.1
RMS 2421
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
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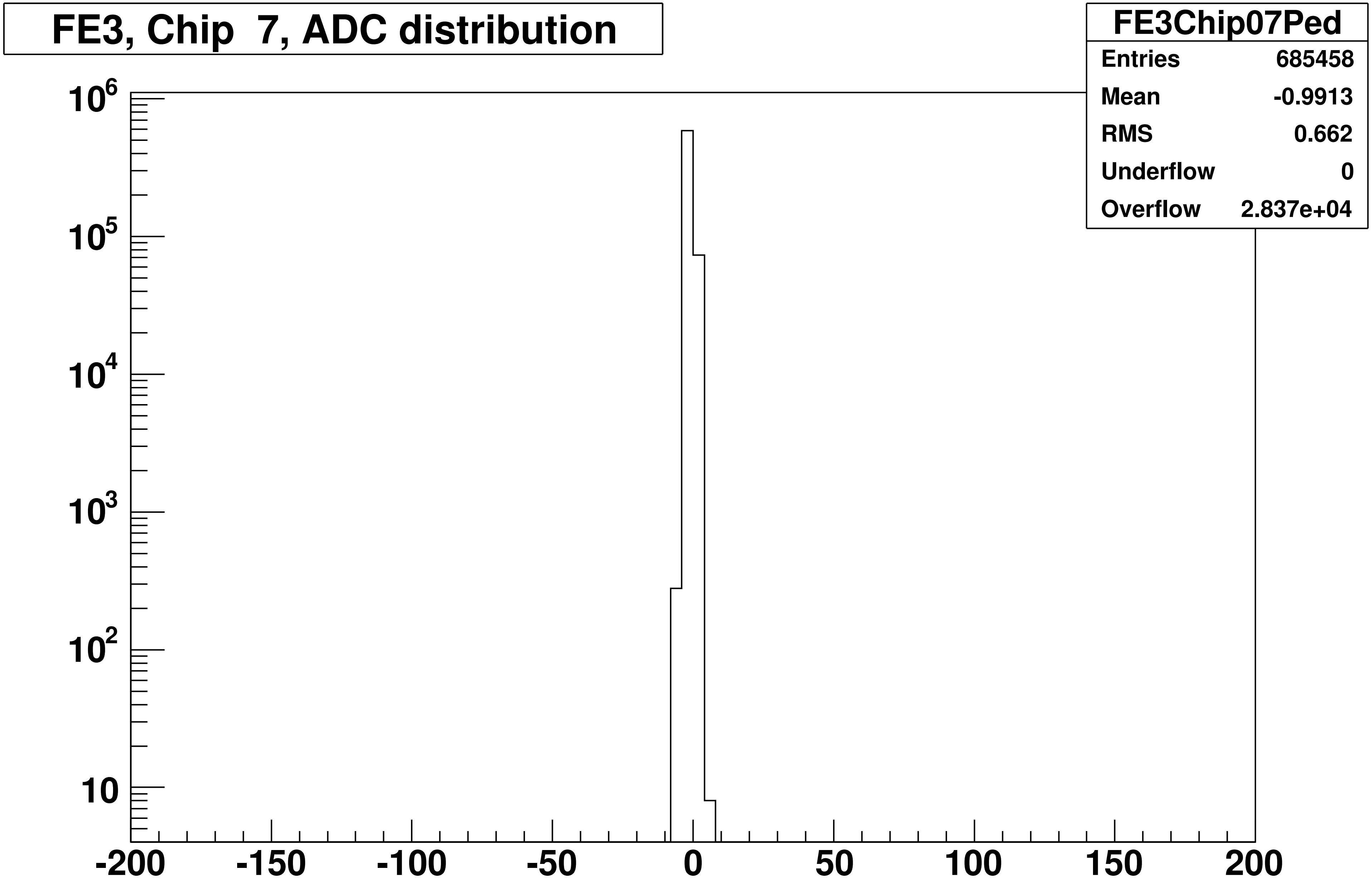
25000



FE3, Chip 7, ADC distribution
FE3Chip07Ped
Entries 685458
Mean -0.9913
RMS 0.662
Underflow 0
Overflow 2.837e+04
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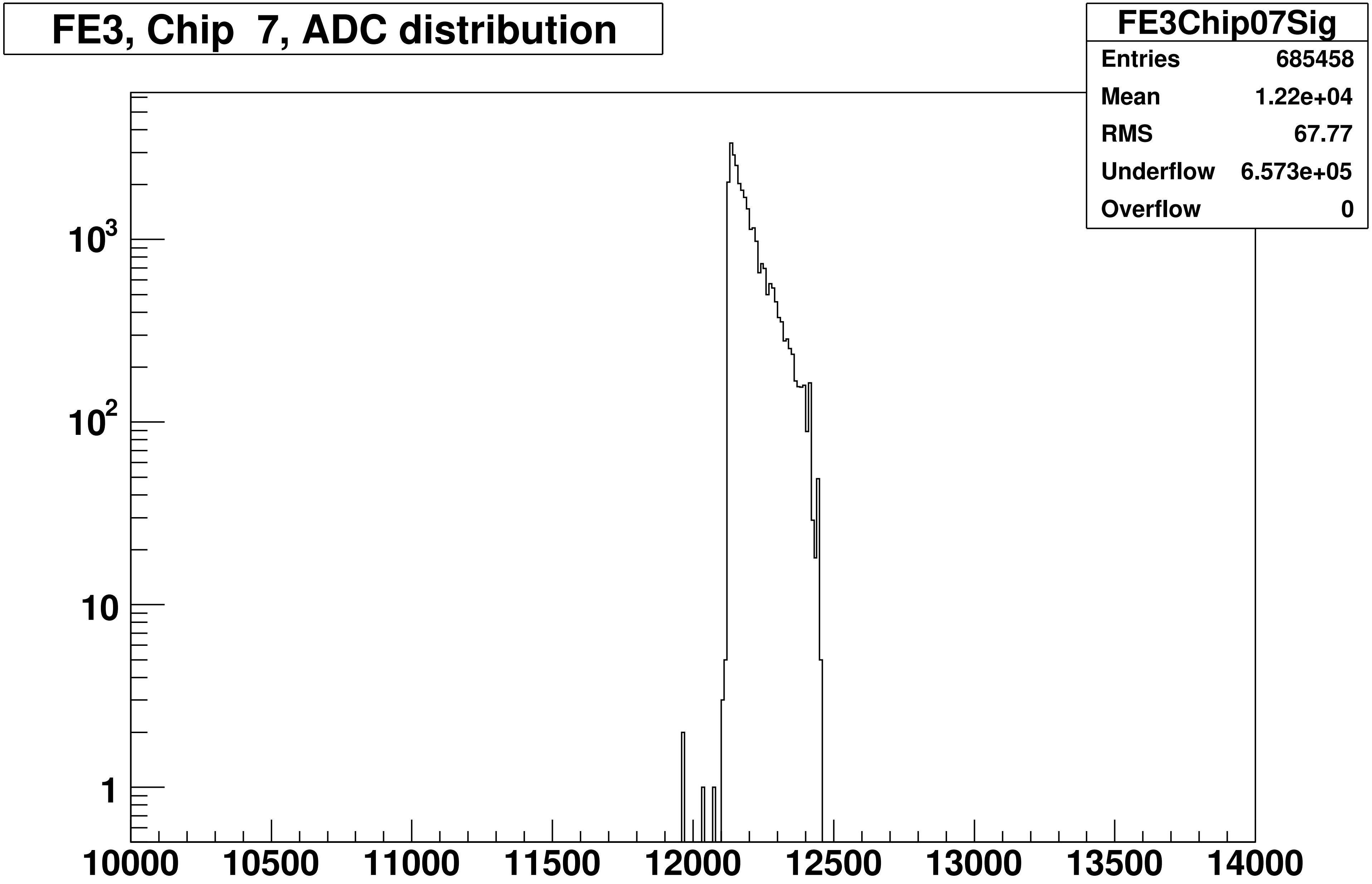
10^5
10^4
10^3
10^2
10
-200
-150
-100
-50
0
50
100
150
200


FE3, Chip 7, ADC distribution
FE3Chip07Sig
Entries 685458
Mean 1.22e+04
RMS 67.77
Underflow 6.573e+05
Overflow 0
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10
10^2
10^3
10000
10500
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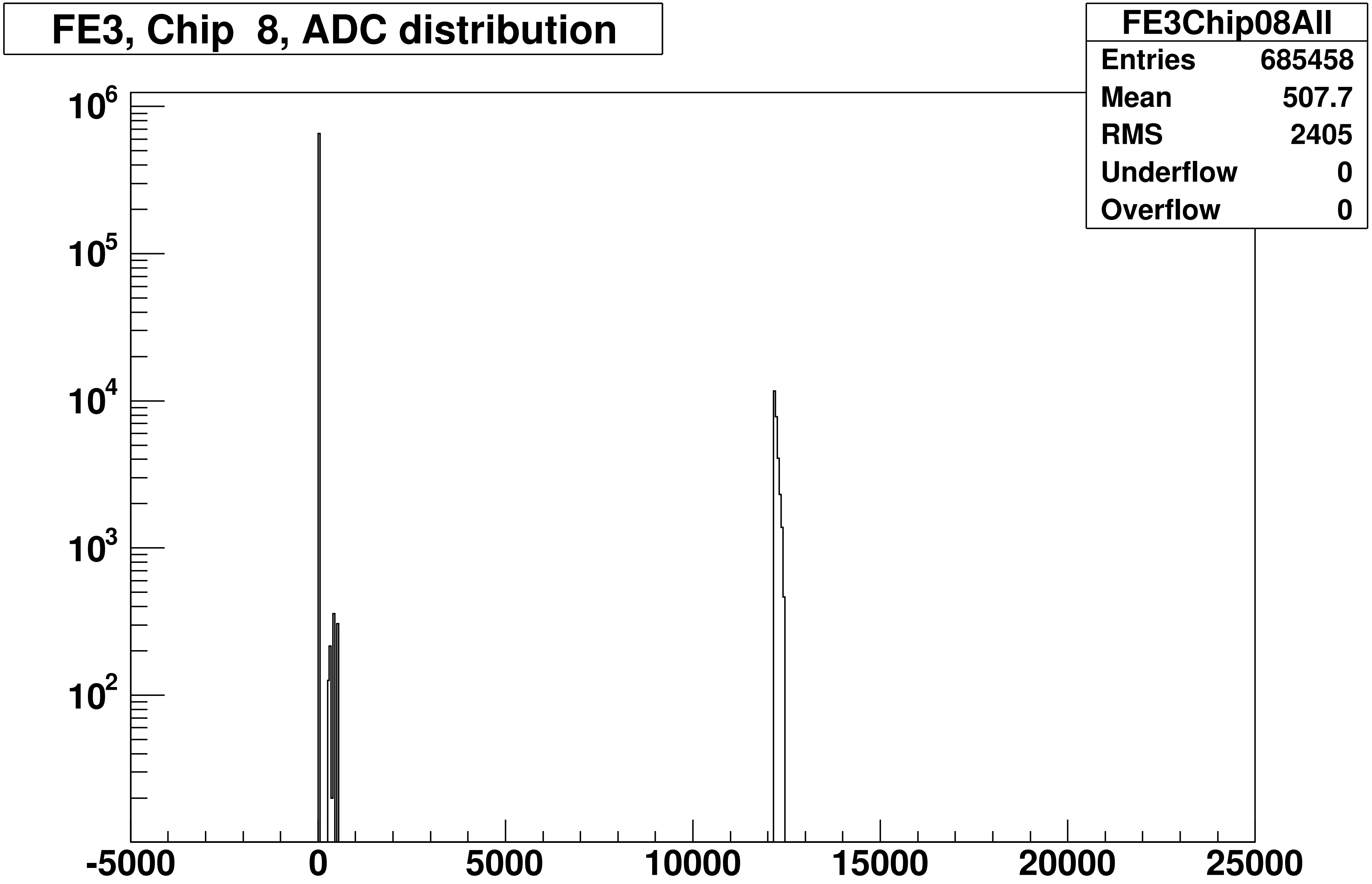
11500
12000
12500
13000
13500
14000


FE3, Chip 8, ADC distribution
FE3Chip08All
Entries 685458
Mean 507.7
RMS 2405
Underflow 0
Overflow 0
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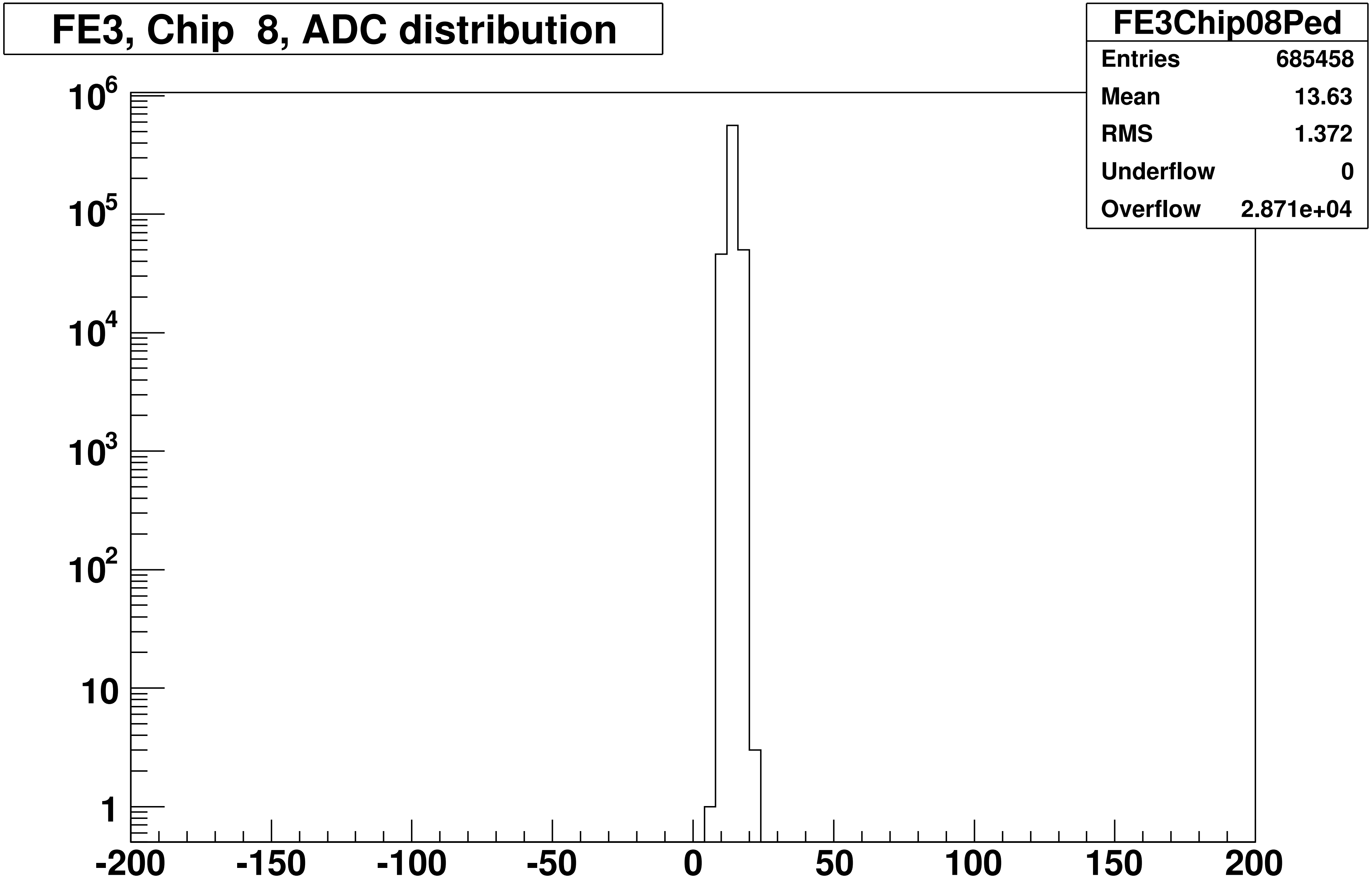
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000


FE3, Chip 8, ADC distribution
FE3Chip08Ped
Entries 685458
Mean 13.63
RMS 1.372
Underflow 0
Overflow 2.871e+04
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10^5
10^4
10^3
10^2
10
1
-200
-150
-100
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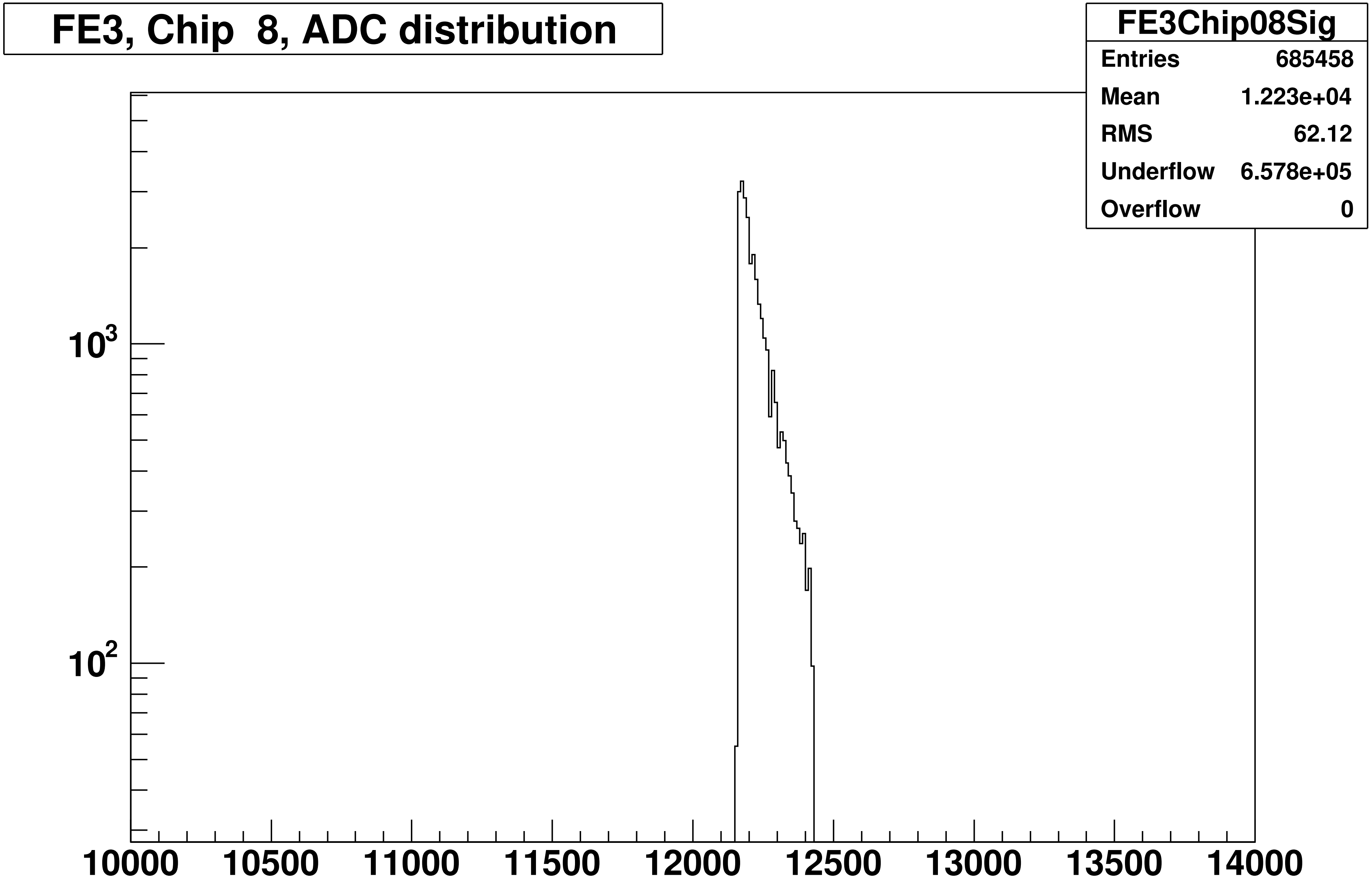
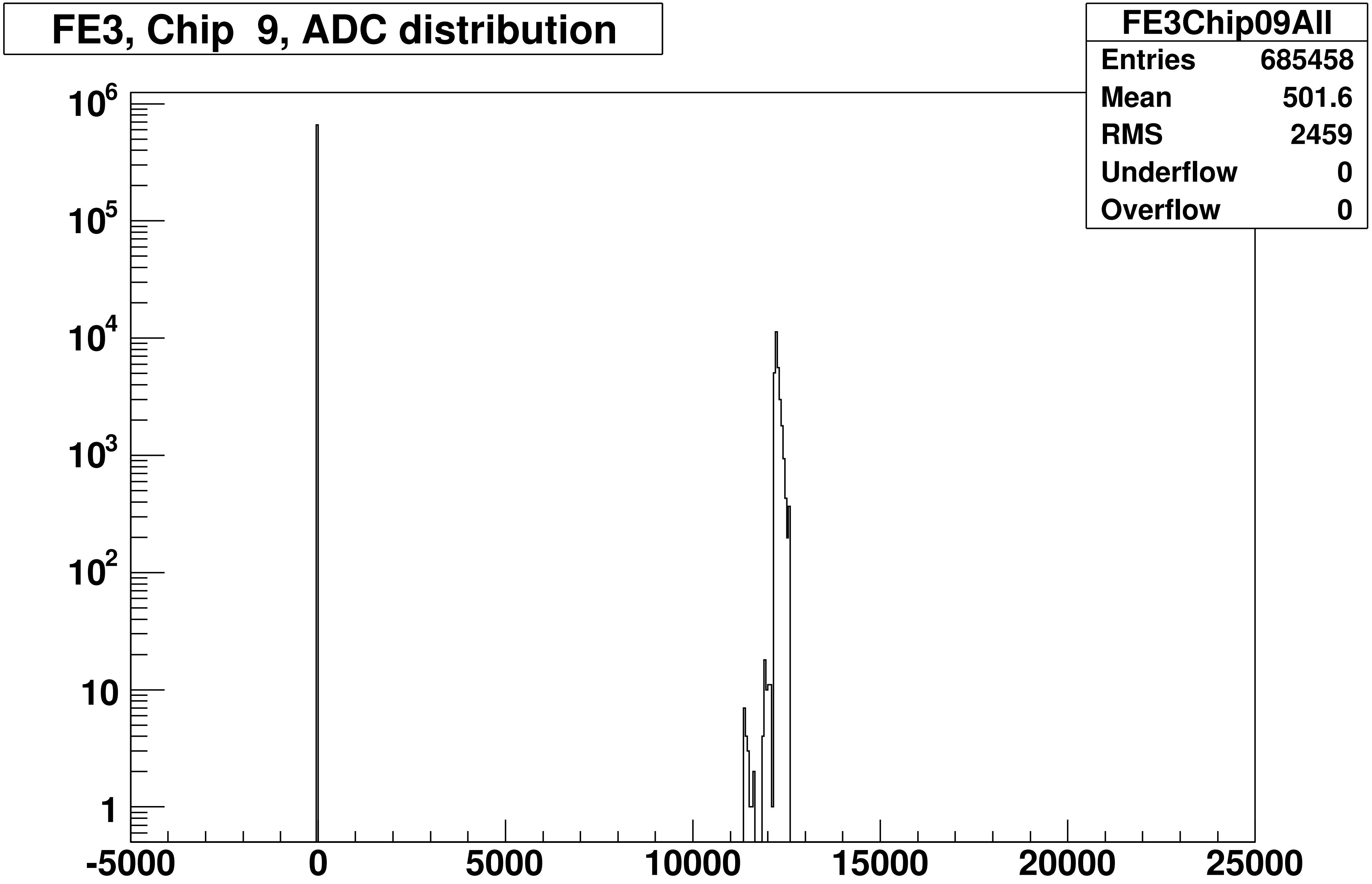
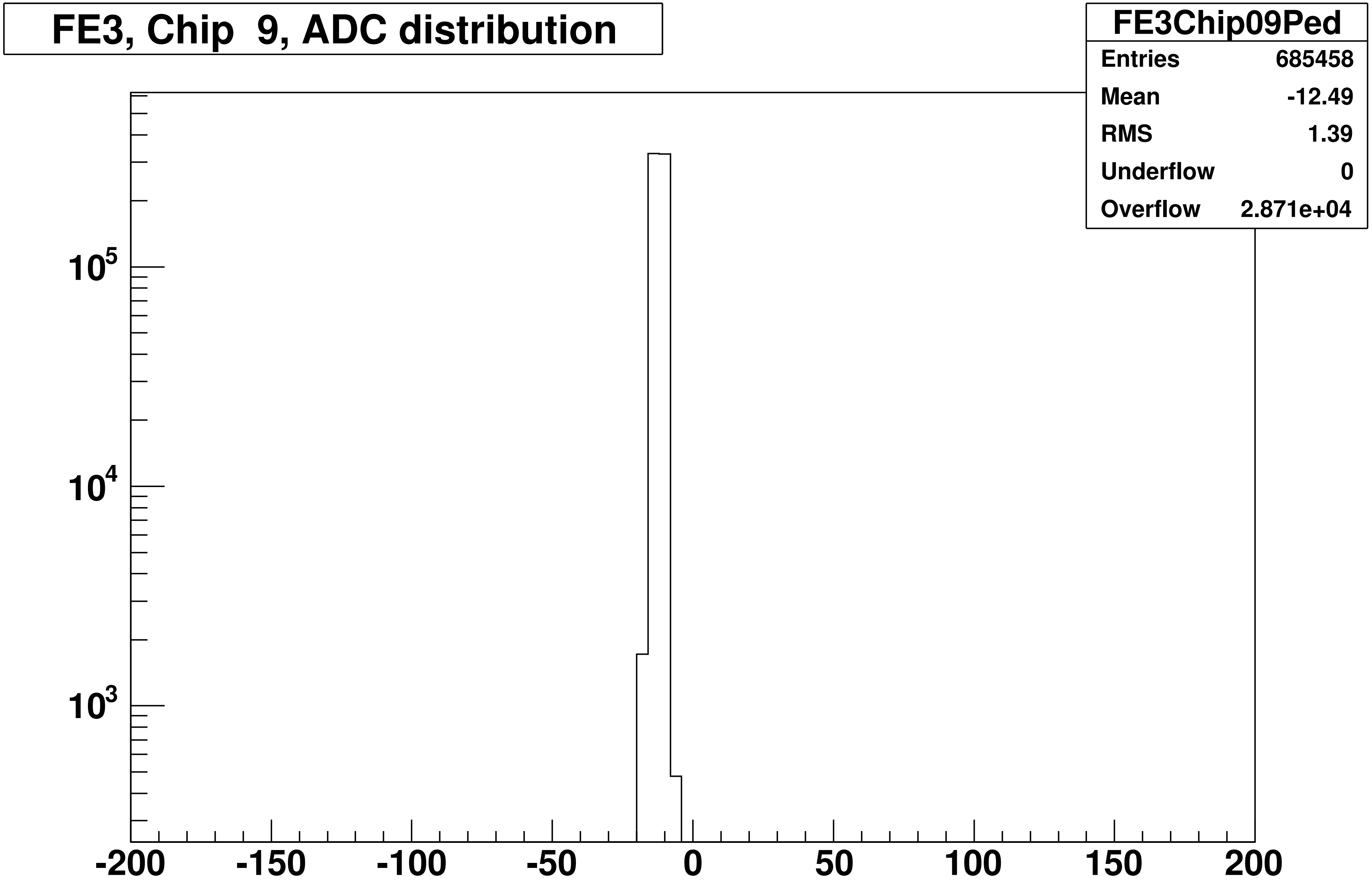
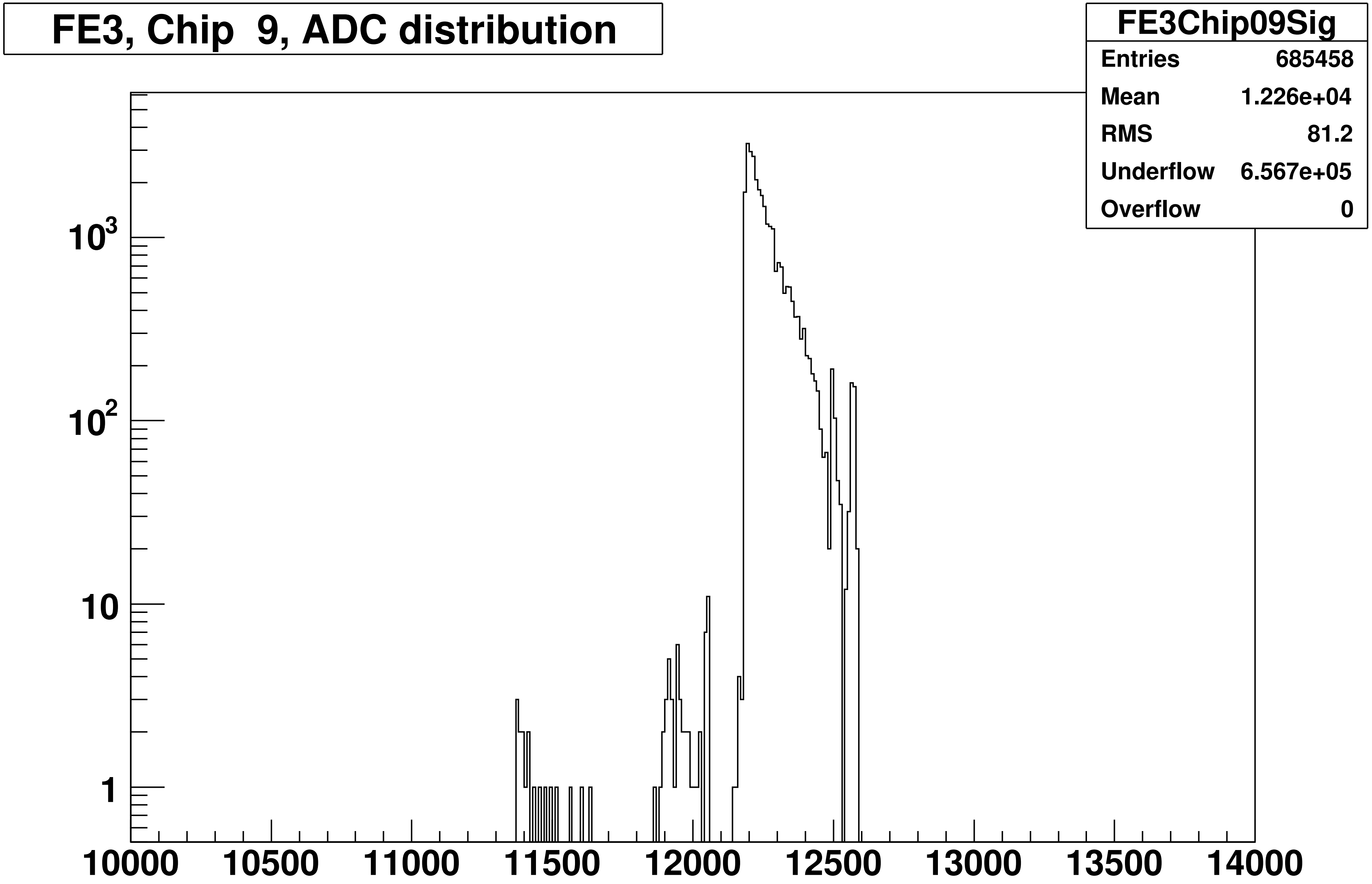
0
50
100
150
200


FE3, Chip 8, ADC distribution
FE3Chip08Sig
Entries 685458
Mean 1.223e+04
RMS 62.12
Underflow 6.578e+05
Overflow 0
10^3
10^2
10000
10500
11000
11500
12000
12500
13000
13500
14000

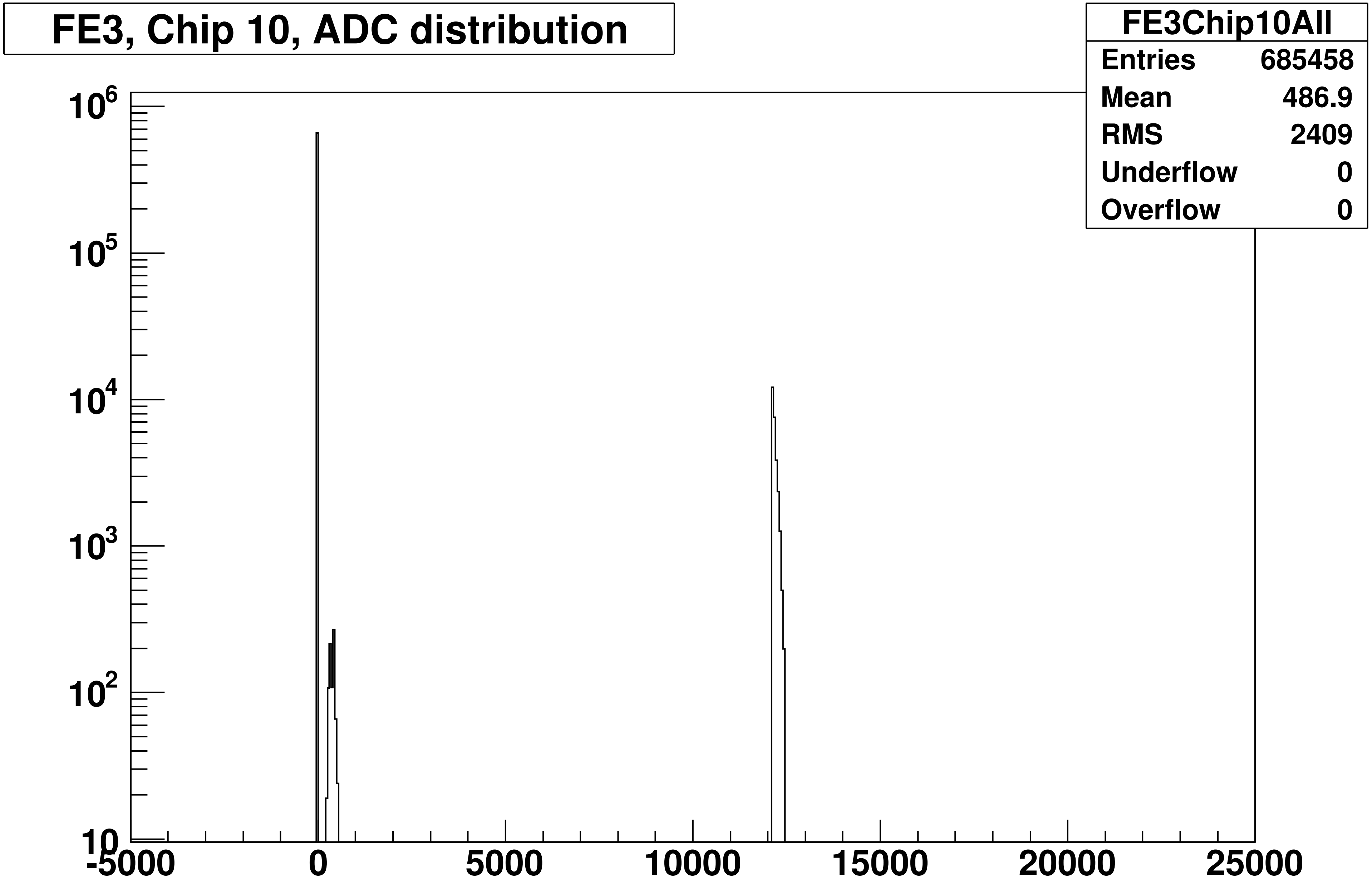


FE3, Chip 9, ADC distribution
FE3Chip09All
Entries 685458
Mean 501.6
RMS 2459
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE3, Chip 9, ADC distribution
FE3Chip09Ped
Entries 685458
Mean -12.49
RMS 1.39
Underflow 0
Overflow 2.871e+04
10^5
10^4
10^3
-200
-150
-100
-50
0
50
100
150
200



FE3, Chip 9, ADC distribution
FE3Chip09Sig
Entries 685458
Mean 1.226e+04
RMS 81.2
Underflow 6.567e+05
Overflow 0
10^3
10^2
10
1
10000
10500
11000
11500
12000
12500
13000
13500
14000


FE3, Chip 10, ADC distribution
FE3Chip10All
Entries 685458
Mean 486.9
RMS 2409
Underflow 0
Overflow 0
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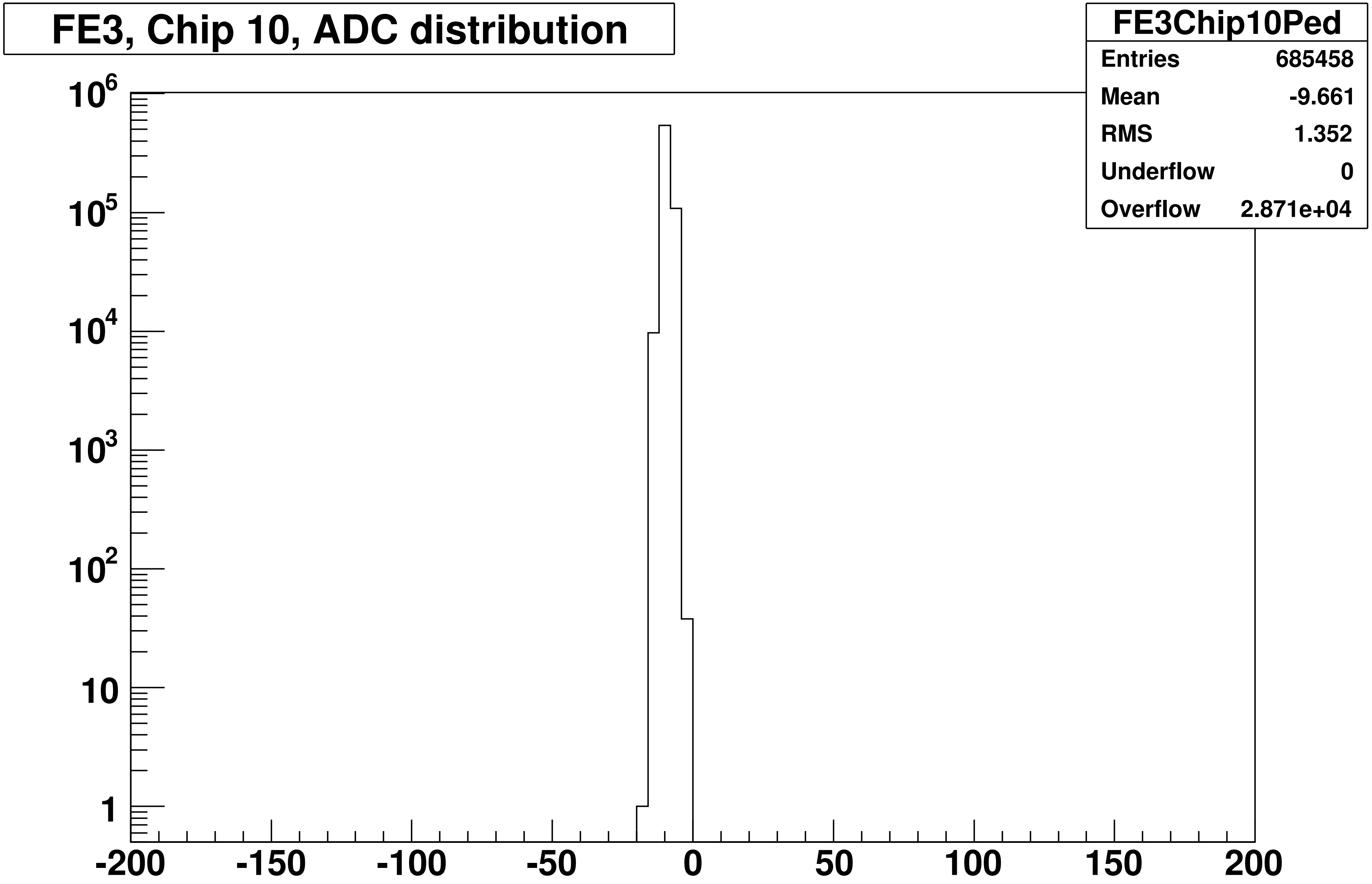
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE3, Chip 10, ADC distribution
FE3Chip10Ped
Entries 685458
Mean -9.661
RMS 1.352
Underflow 0
Overflow 2.871e+04
10^6
10^5
10^4
10^3
10^2
10
1
-200
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-100
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0
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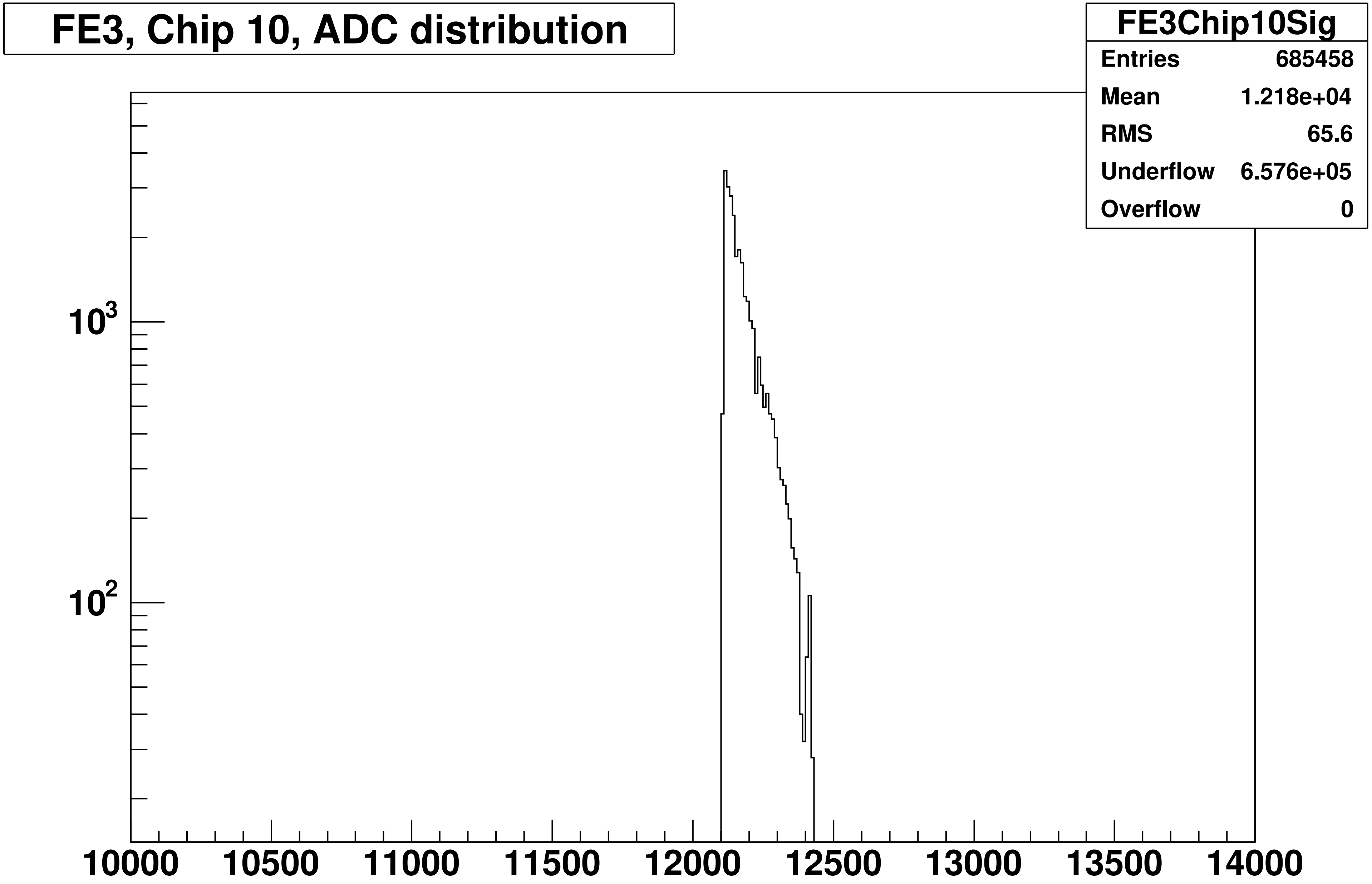
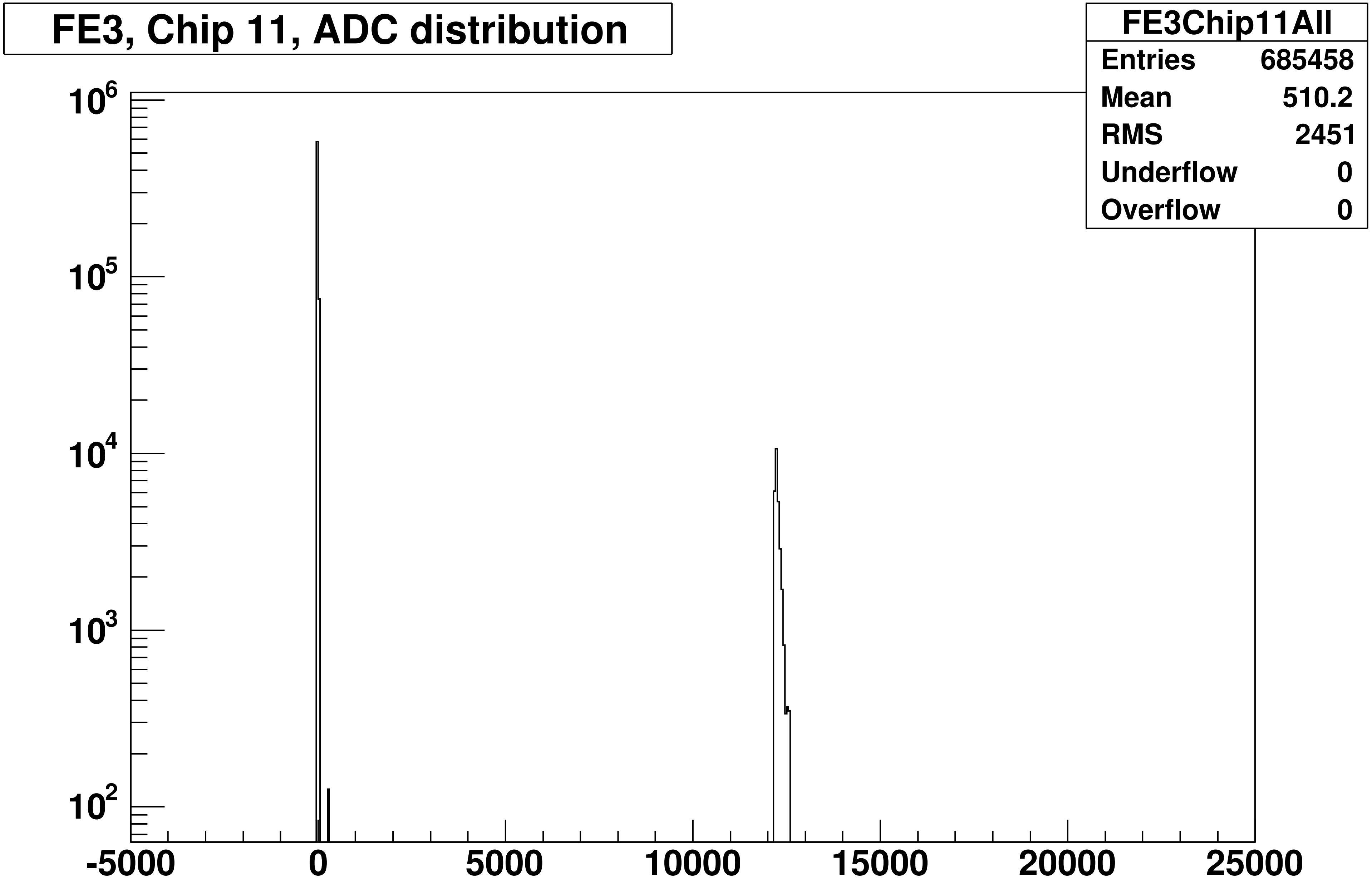
100
150
200


FE3, Chip 10, ADC distribution
FE3Chip10Sig
Entries 685458
Mean 1.218e+04
RMS 65.6
Underflow 6.576e+05
Overflow 0
10^3
10^2
10000
10500
11000
11500
12000
12500
13000
13500
14000



FE3, Chip 11, ADC distribution
FE3Chip11All
Entries 685458
Mean 510.2
RMS 2451
Underflow 0
Overflow 0
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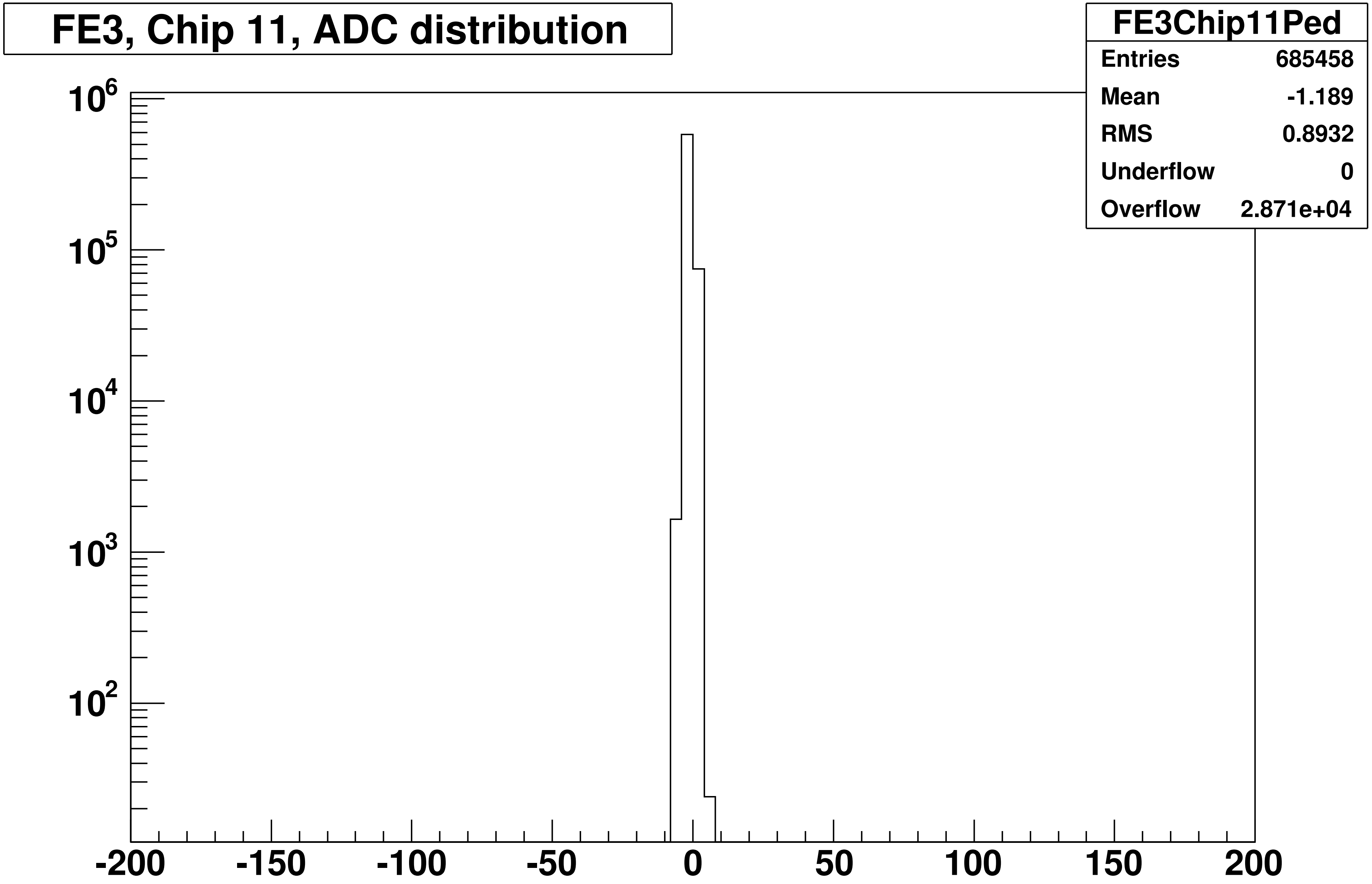
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000


FE3, Chip 11, ADC distribution
FE3Chip11Ped
Entries 685458
Mean -1.189
RMS 0.8932
Underflow 0
Overflow 2.871e+04
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10^5
10^4
10^3
10^2
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-100
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0
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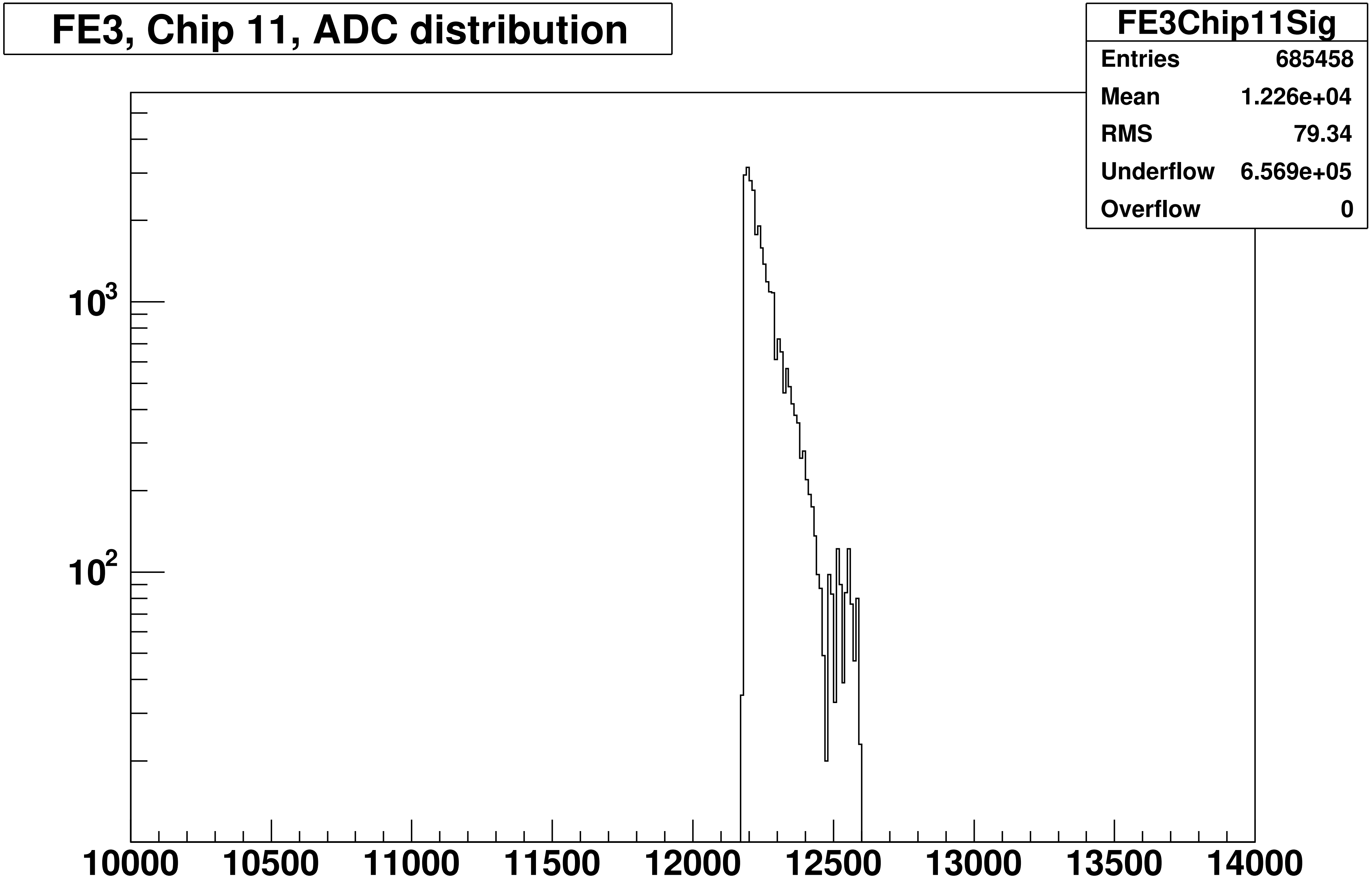
100
150
200



FE3, Chip 11, ADC distribution
FE3Chip11Sig
Entries 685458
Mean 1.226e+04
RMS 79.34
Underflow 6.569e+05
Overflow 0
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10^2
10000
10500
11000
11500
12000
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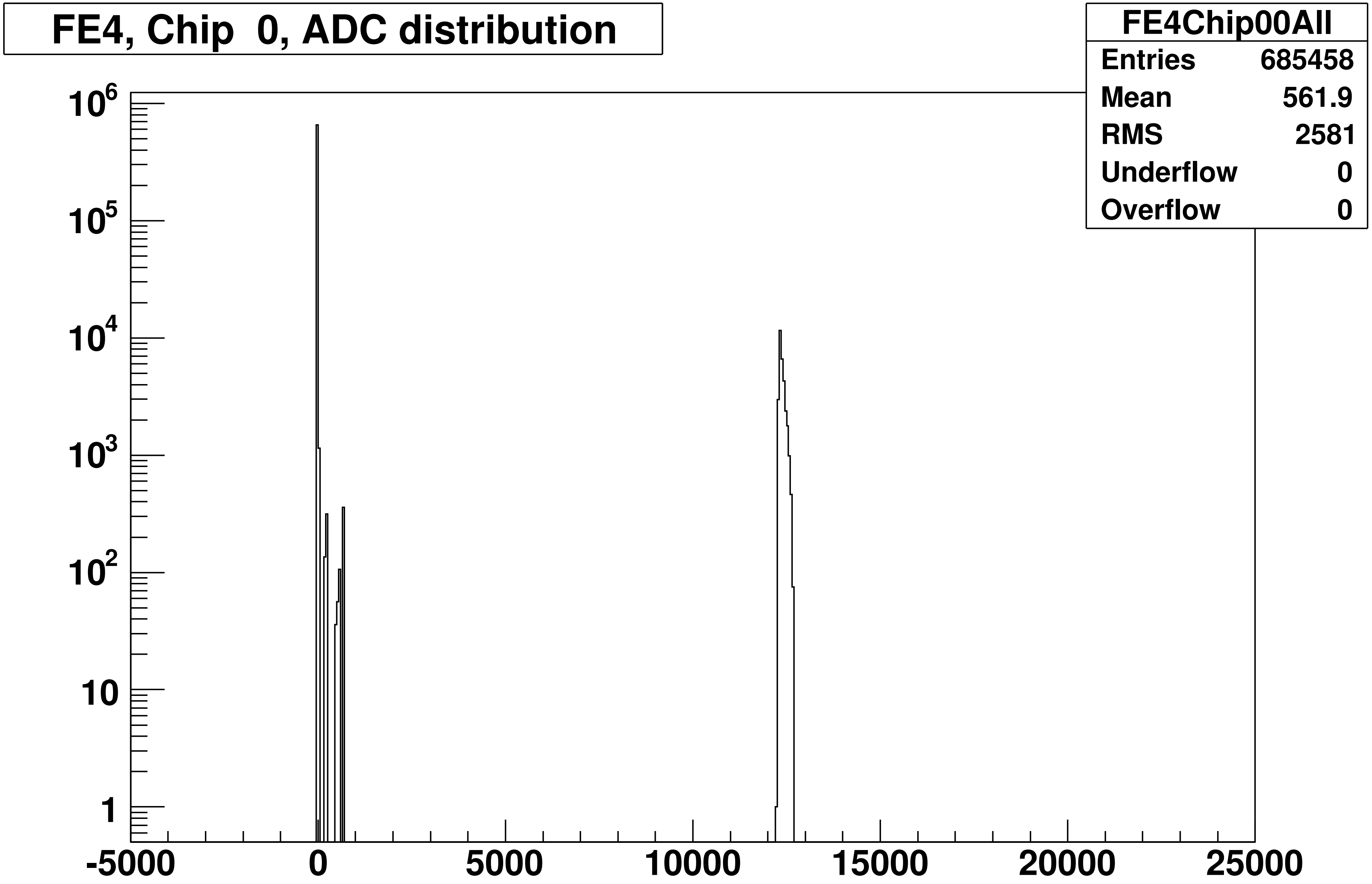
FE4, Chip 0, ADC distribution
FE4Chip00All
Entries 685458
Mean 561.9
RMS 2581
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
1
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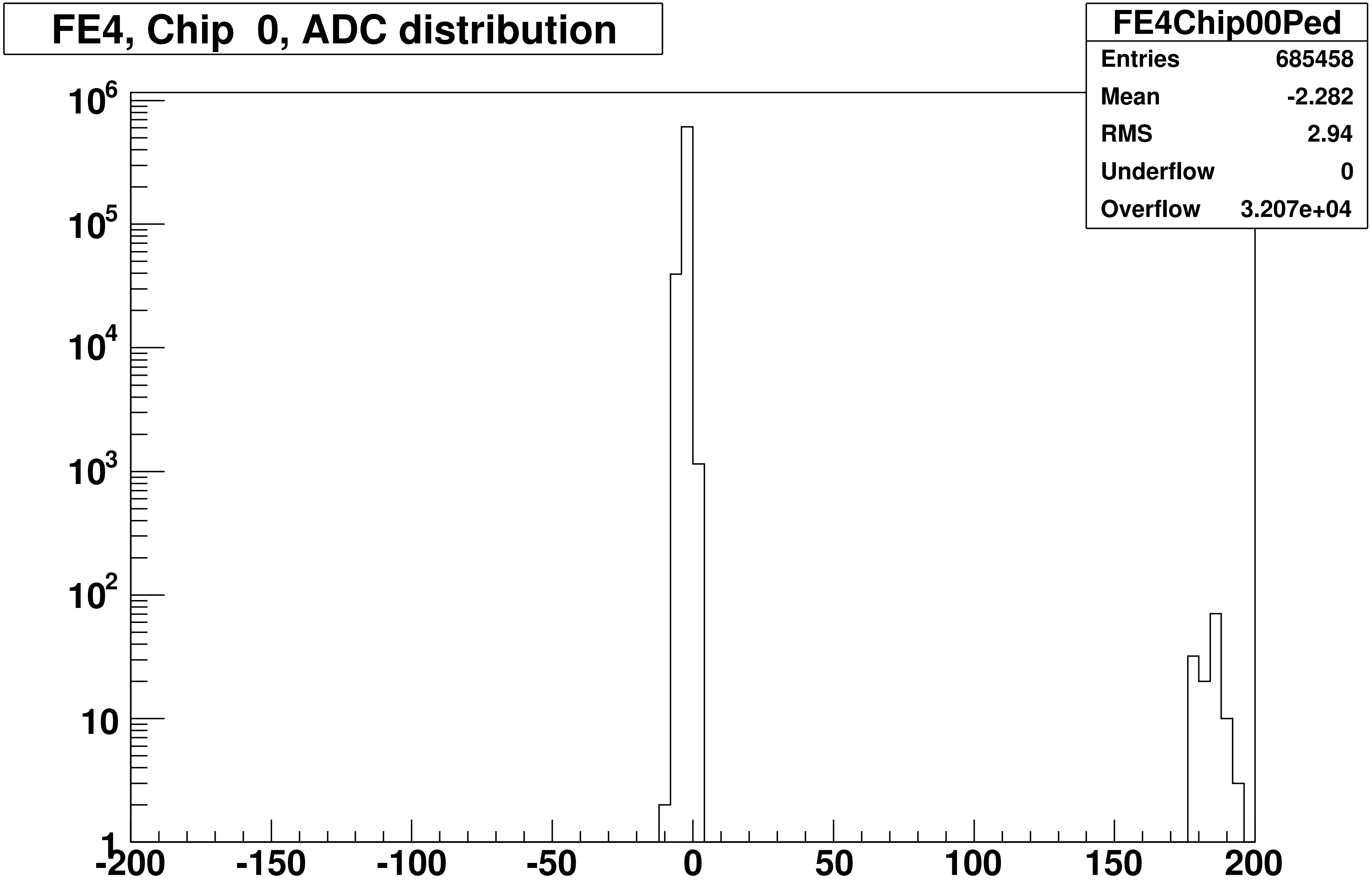
0
5000
10000
15000
20000
25000



FE4, Chip 0, ADC distribution
FE4Chip00Ped
Entries 685458
Mean -2.282
RMS 2.94
Underflow 0
Overflow 3.207e+04
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10^5
10^4
10^3
10^2
10
1
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-100
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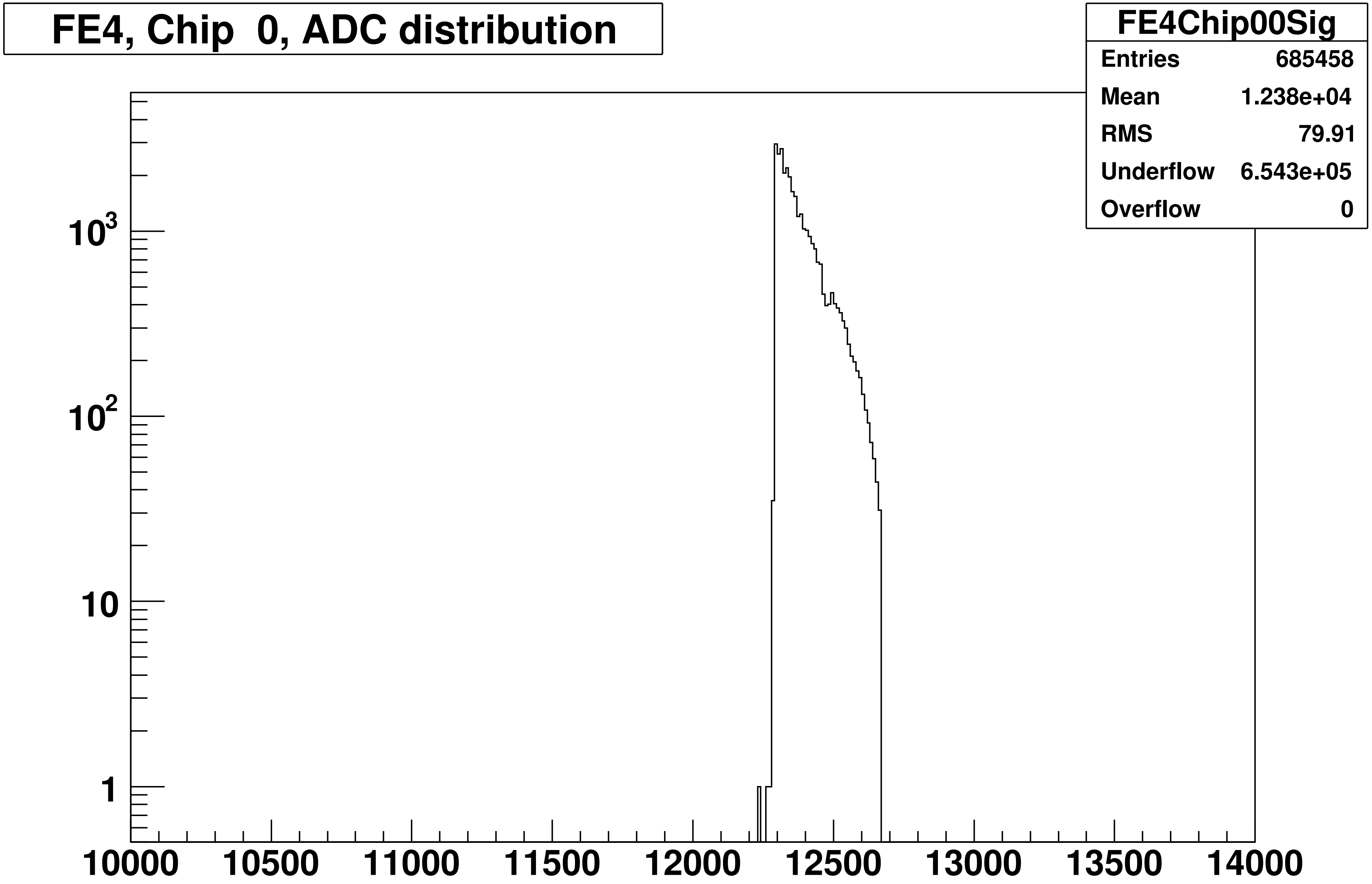
0
50
100
150
200


FE4, Chip 0, ADC distribution
FE4Chip00Sig
Entries 685458
Mean 1.238e+04
RMS 79.91
Underflow 6.543e+05
Overflow 0
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10^2
10
1
10000
10500
11000
11500
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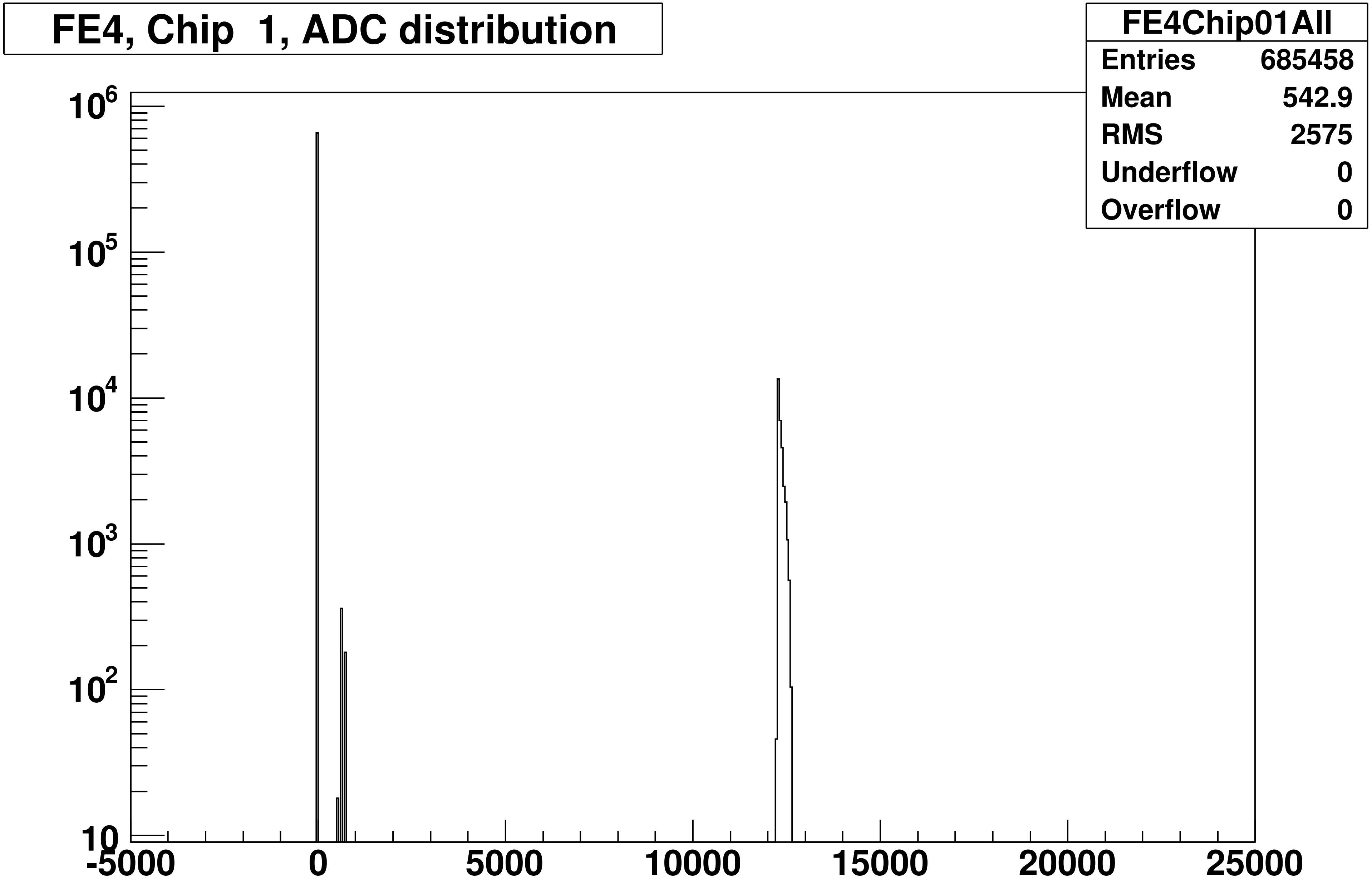
14000


FE4, Chip 1, ADC distribution
FE4Chip01All
Entries 685458
Mean 542.9
RMS 2575
Underflow 0
Overflow 0
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10^2
10^3
10^4
10^5
10^6
-5000
0
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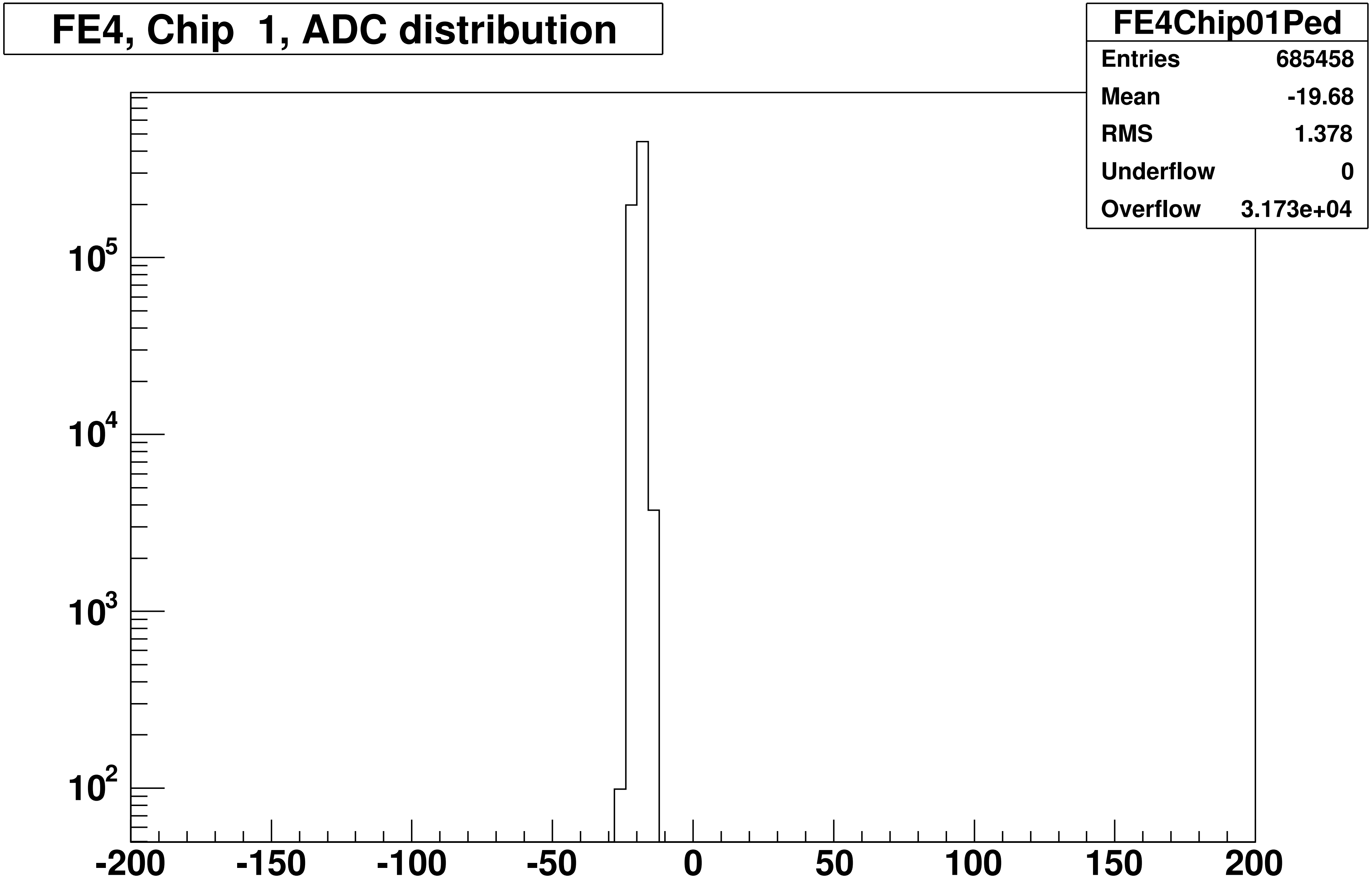
10000
15000
20000
25000



FE4, Chip 1, ADC distribution
FE4Chip01Ped
Entries 685458
Mean -19.68
RMS 1.378
Underflow 0
Overflow 3.173e+04
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10^4
10^3
10^2
-200
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-100
-50
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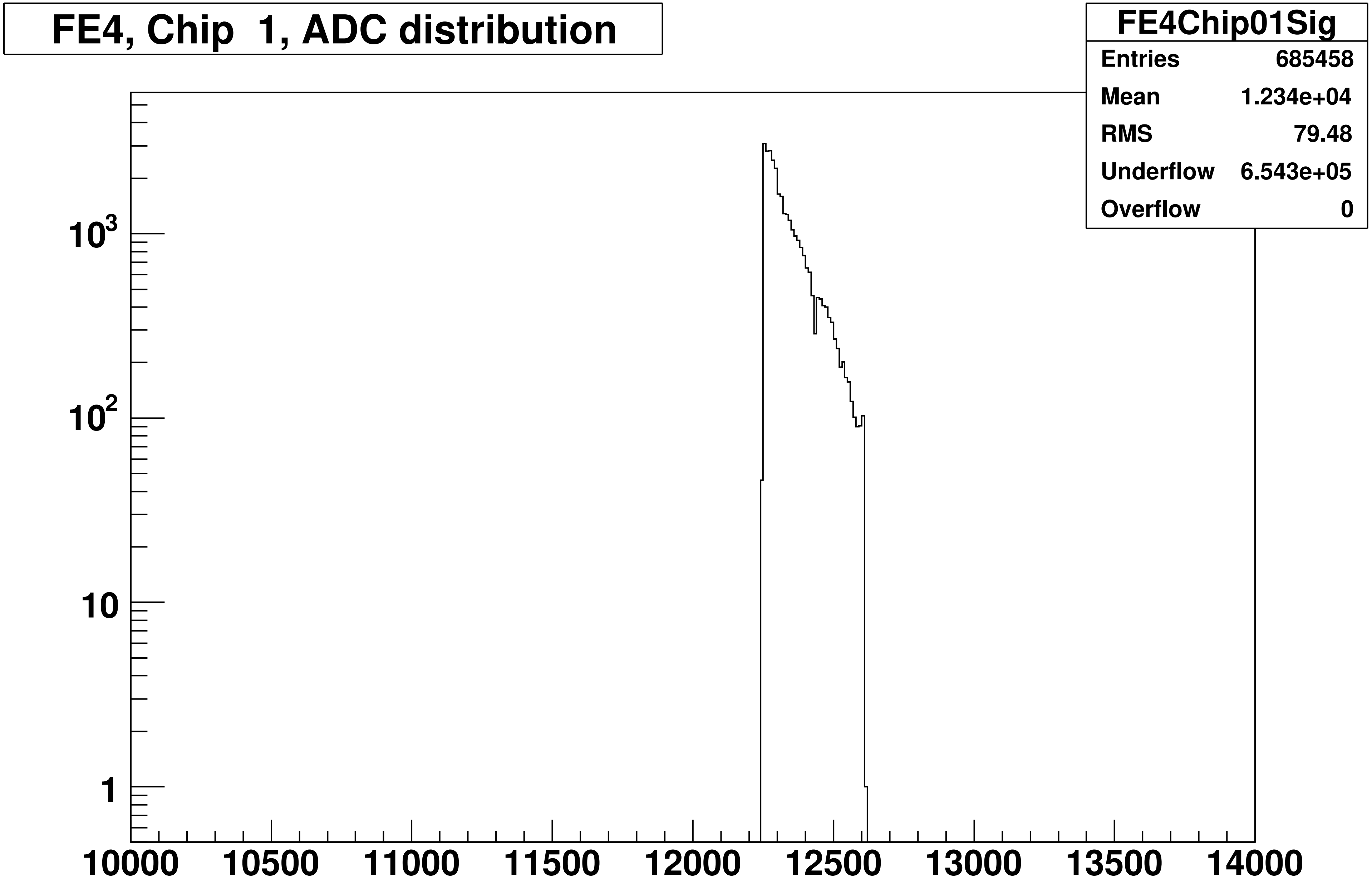
100
150
200


FE4, Chip 1, ADC distribution
FE4Chip01Sig
Entries 685458
Mean 1.234e+04
RMS 79.48
Underflow 6.543e+05
Overflow 0
10^3
10^2
10
1
10000
10500
11000
11500
12000
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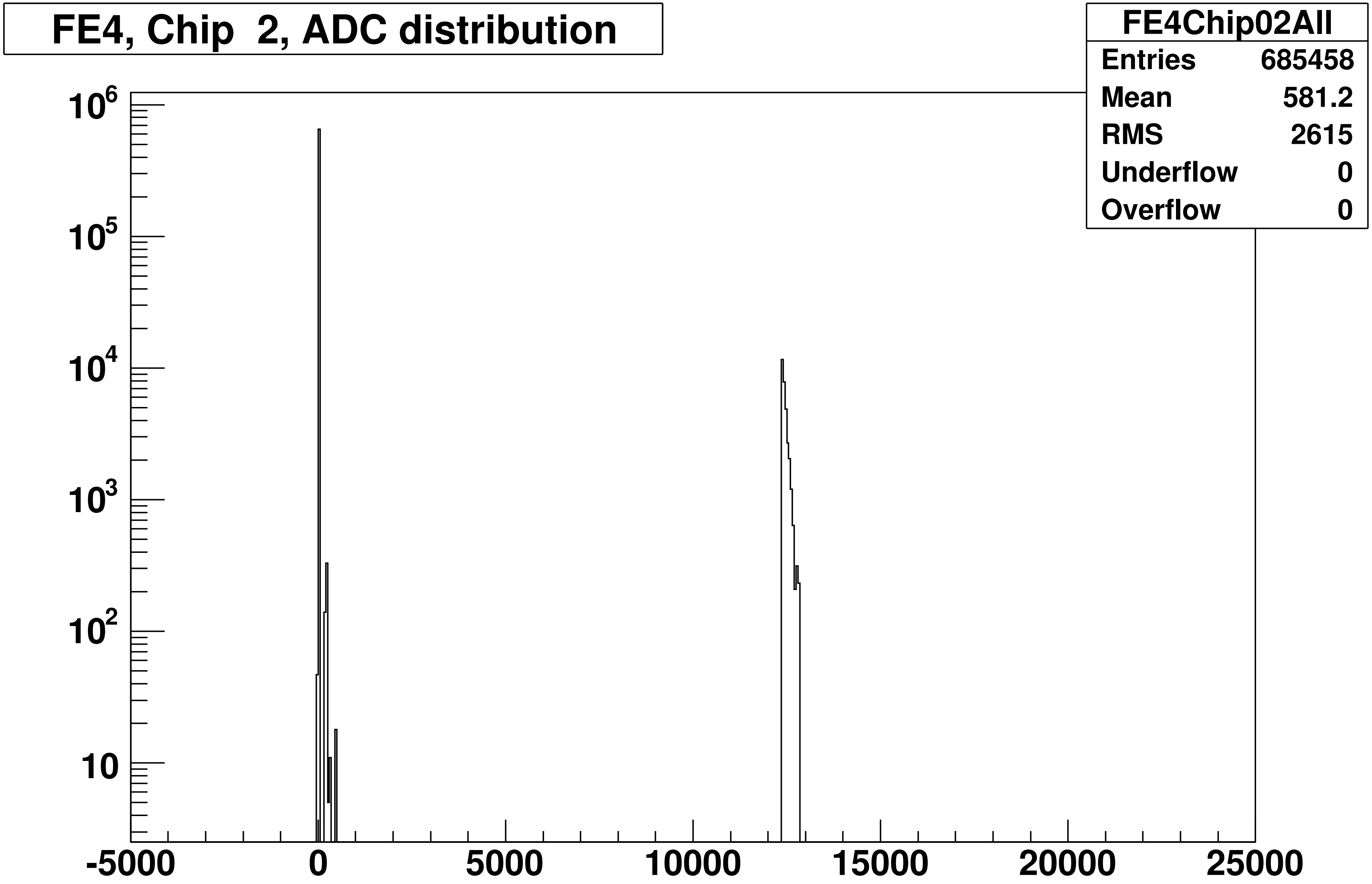
13000
13500
14000


FE4, Chip 2, ADC distribution
FE4Chip02All
Entries 685458
Mean 581.2
RMS 2615
Underflow 0
Overflow 0
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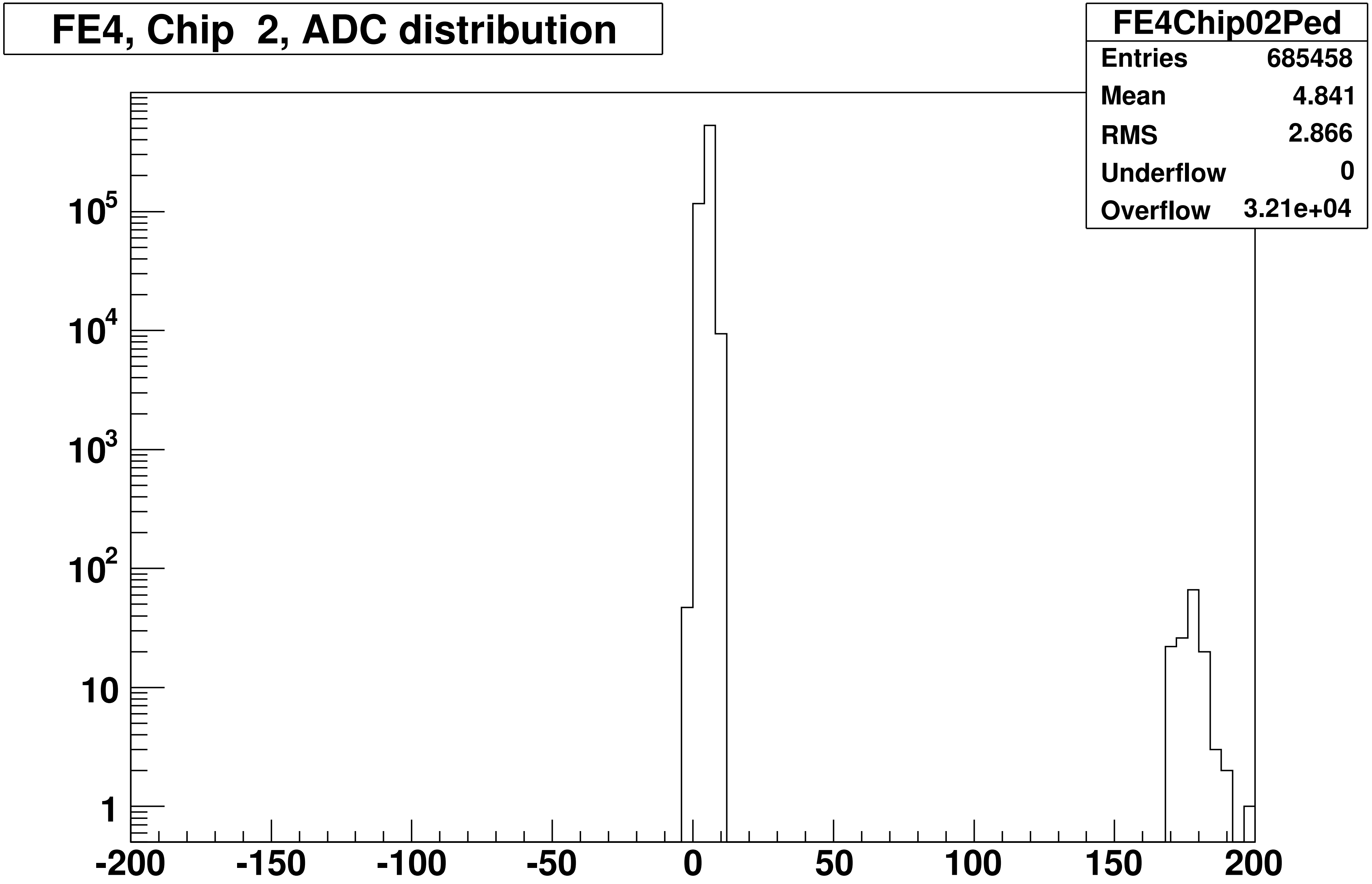
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000



FE4, Chip 2, ADC distribution
FE4Chip02Ped
Entries 685458
Mean 4.841
RMS 2.866
Underflow 0
Overflow 3.21e+04
10^5
10^4
10^3
10^2
10
1
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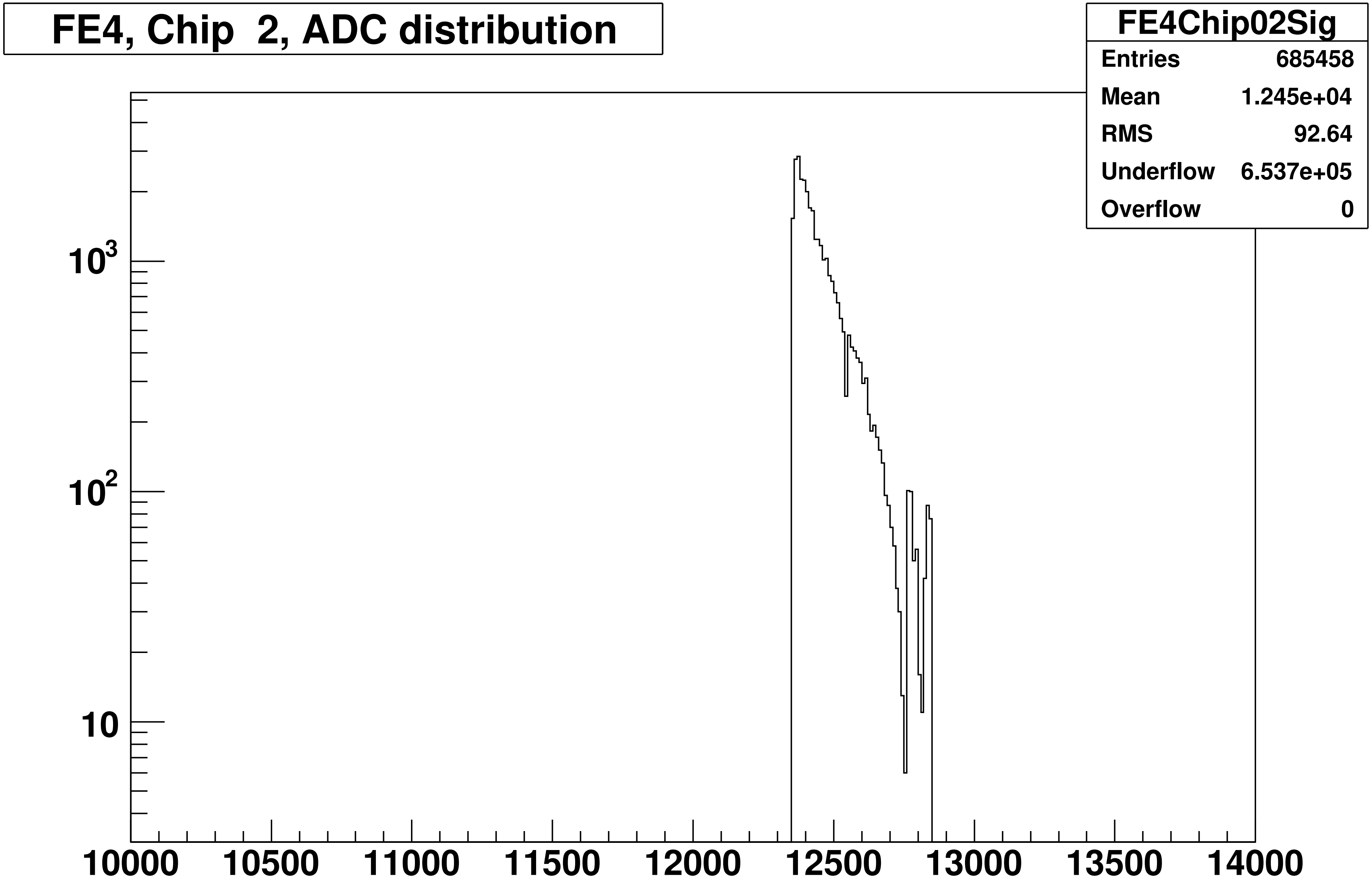
-150
-100
-50
0
50
100
150
200


FE4, Chip 2, ADC distribution
FE4Chip02Sig
Entries 685458
Mean 1.245e+04
RMS 92.64
Underflow 6.537e+05
Overflow 0
10^3
10^2
10
10000
10500
11000
11500
12000
12500
13000
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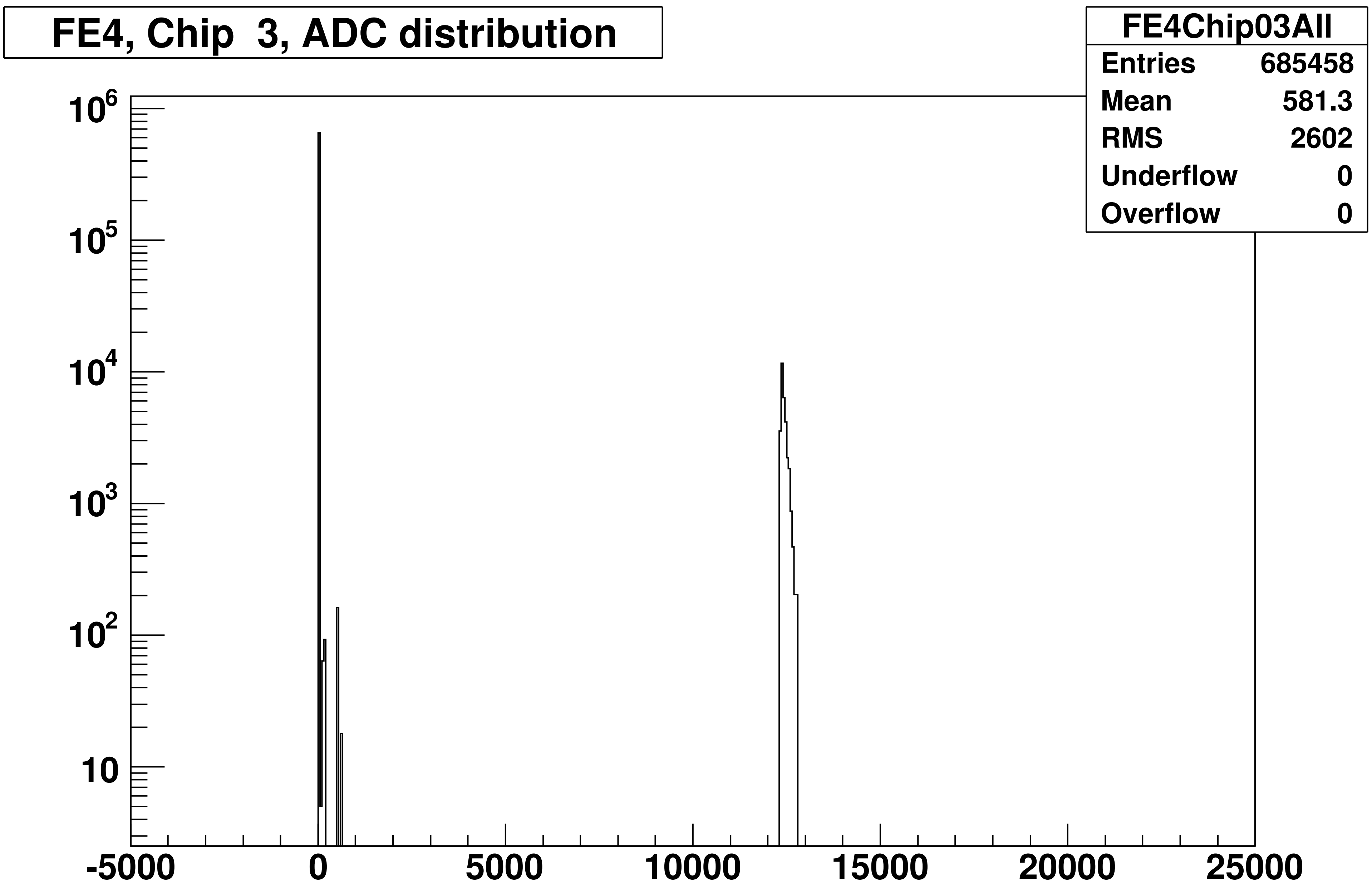
14000


FE4, Chip 3, ADC distribution
FE4Chip03All
Entries 685458
Mean 581.3
RMS 2602
Underflow 0
Overflow 0
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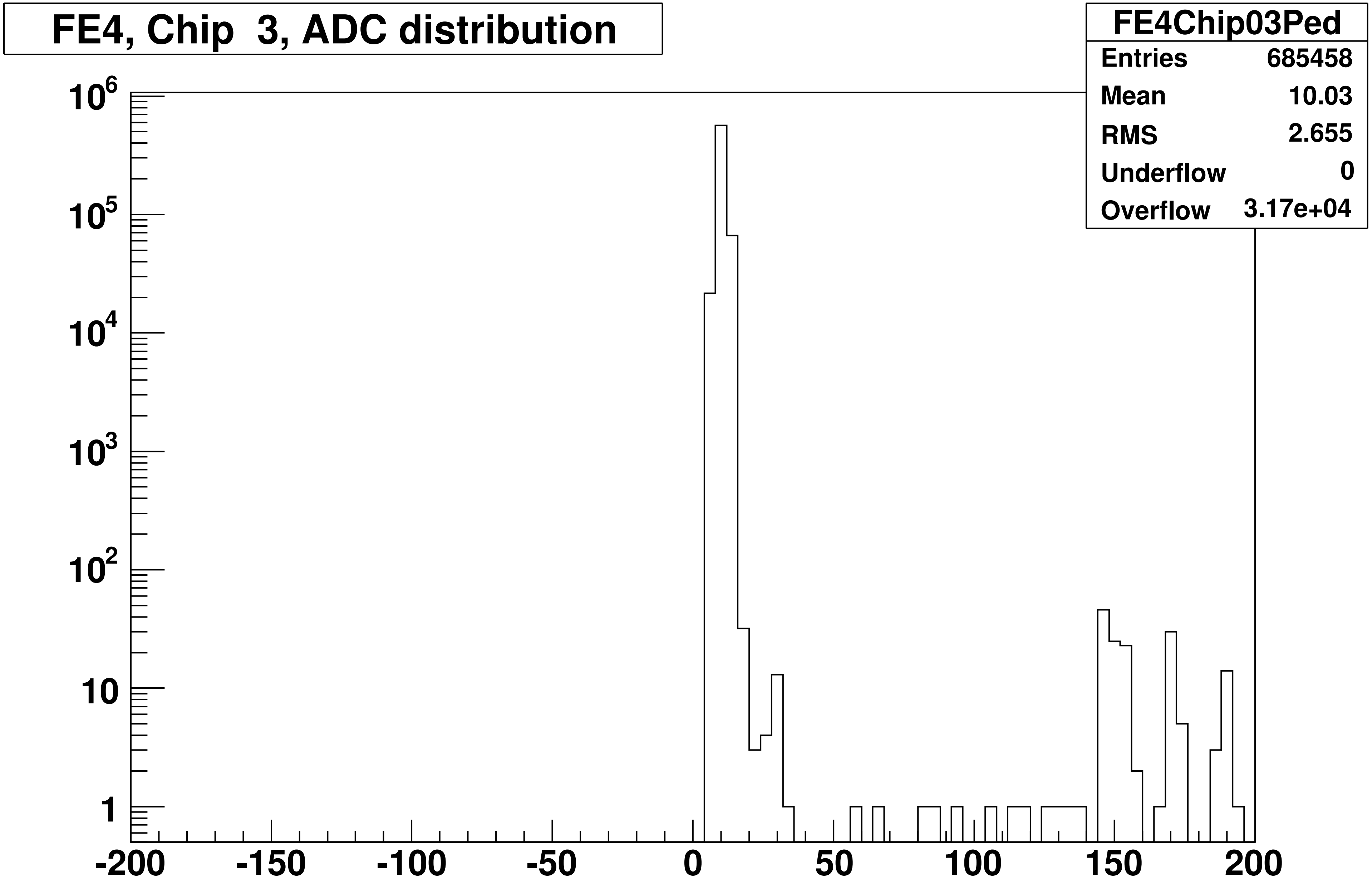
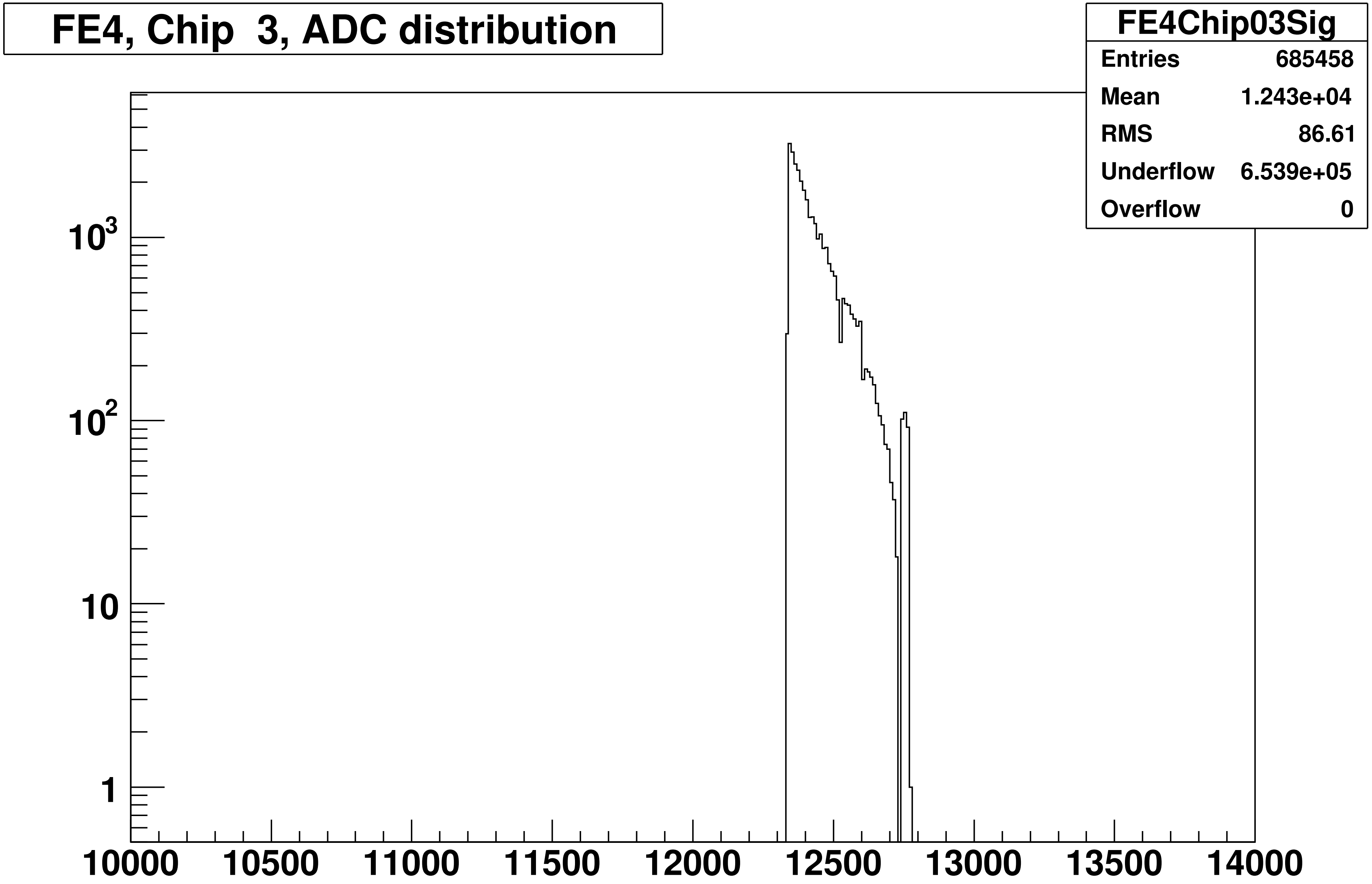
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE4, Chip 3, ADC distribution
FE4Chip03Ped
Entries 685458
Mean 10.03
RMS 2.655
Underflow 0
Overflow 3.17e+04
10^6
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
200



FE4, Chip 3, ADC distribution
FE4Chip03Sig
Entries 685458
Mean 1.243e+04
RMS 86.61
Underflow 6.539e+05
Overflow 0
10^3
10^2
10
1
10000
10500
11000
11500
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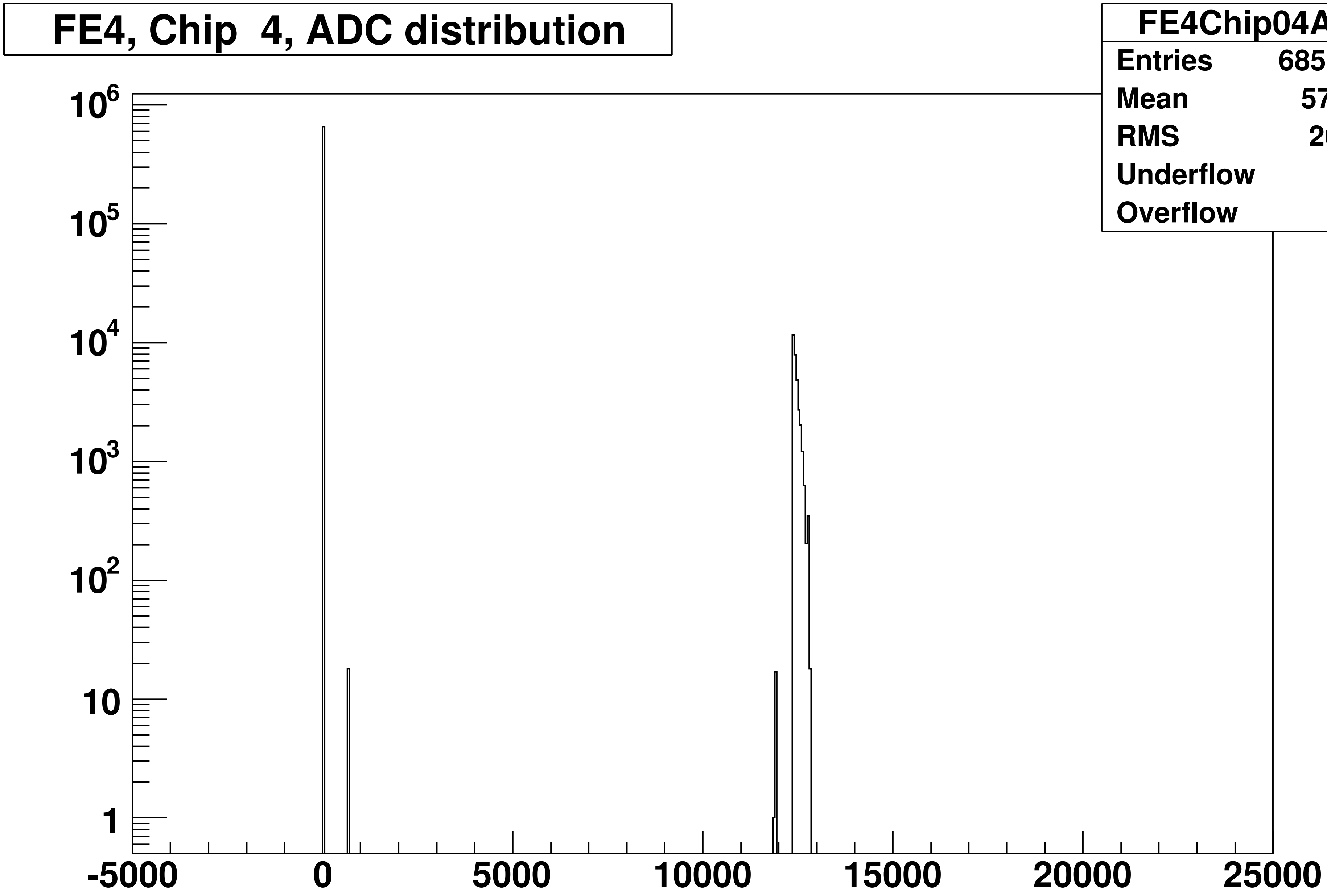
13500
14000



FE4, Chip 4, ADC distribution
FE4Chip04All
Entries 685458
Mean 579.6
RMS 2608
Underflow 0
Overflow 0
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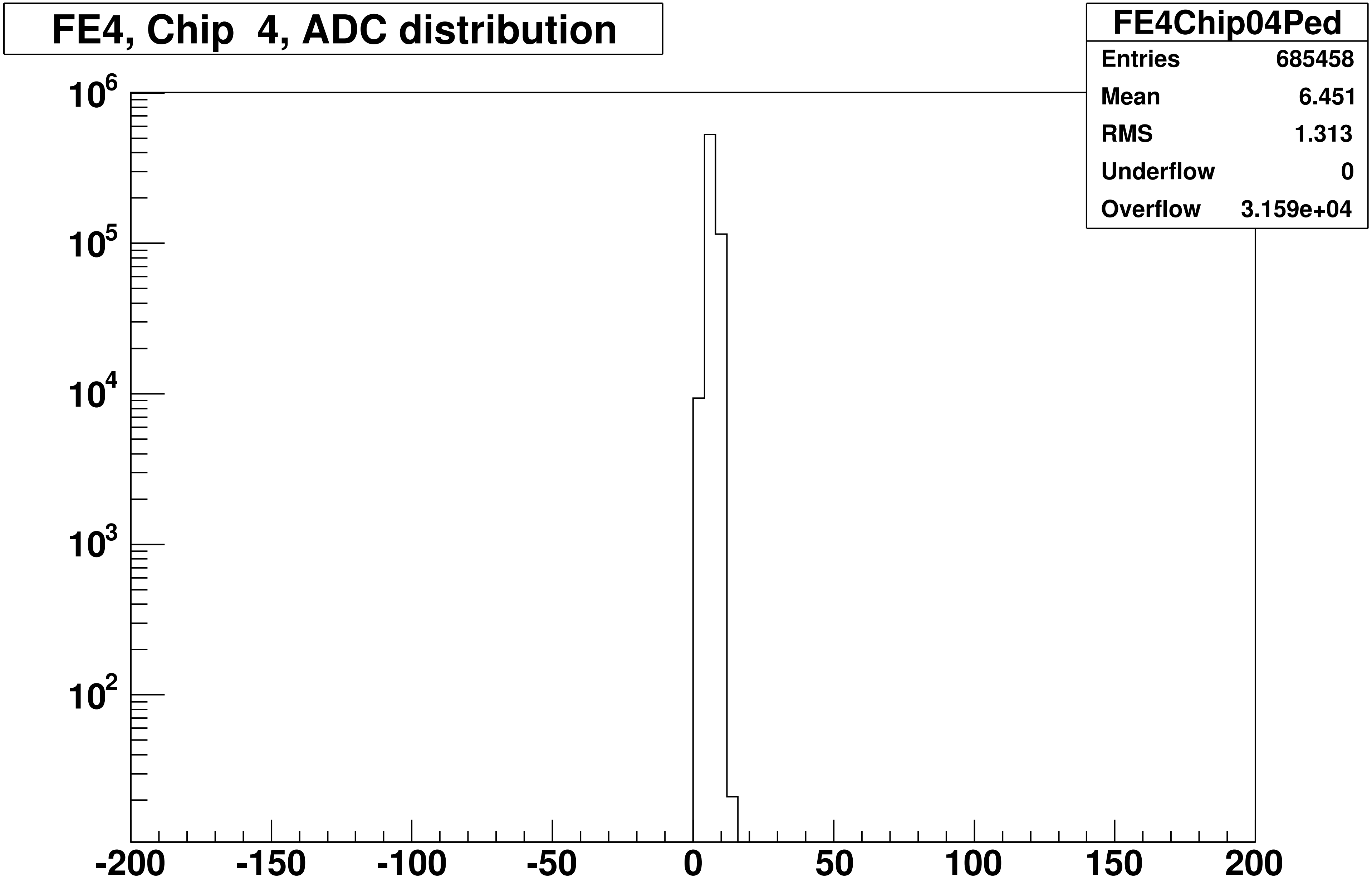
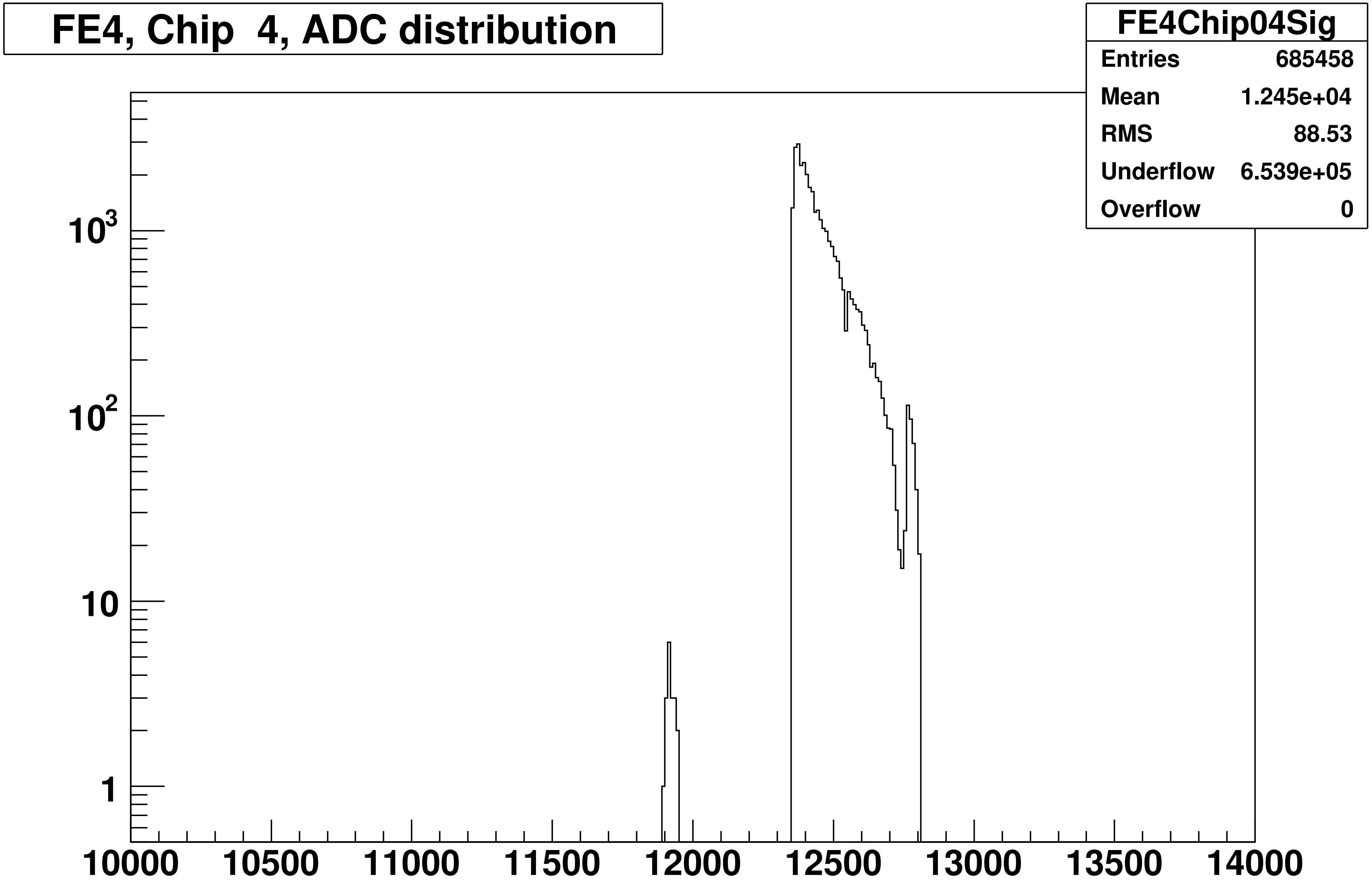
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE4, Chip 4, ADC distribution
FE4Chip04Ped
Entries 685458
Mean 6.451
RMS 1.313
Underflow 0
Overflow 3.159e+04
10^6
10^5
10^4
10^3
10^2
-200
-150
-100
-50
0
50
100
150
200



FE4, Chip 4, ADC distribution
FE4Chip04Sig
Entries 685458
Mean 1.245e+04
RMS 88.53
Underflow 6.539e+05
Overflow 0
10^3
10^2
10
1
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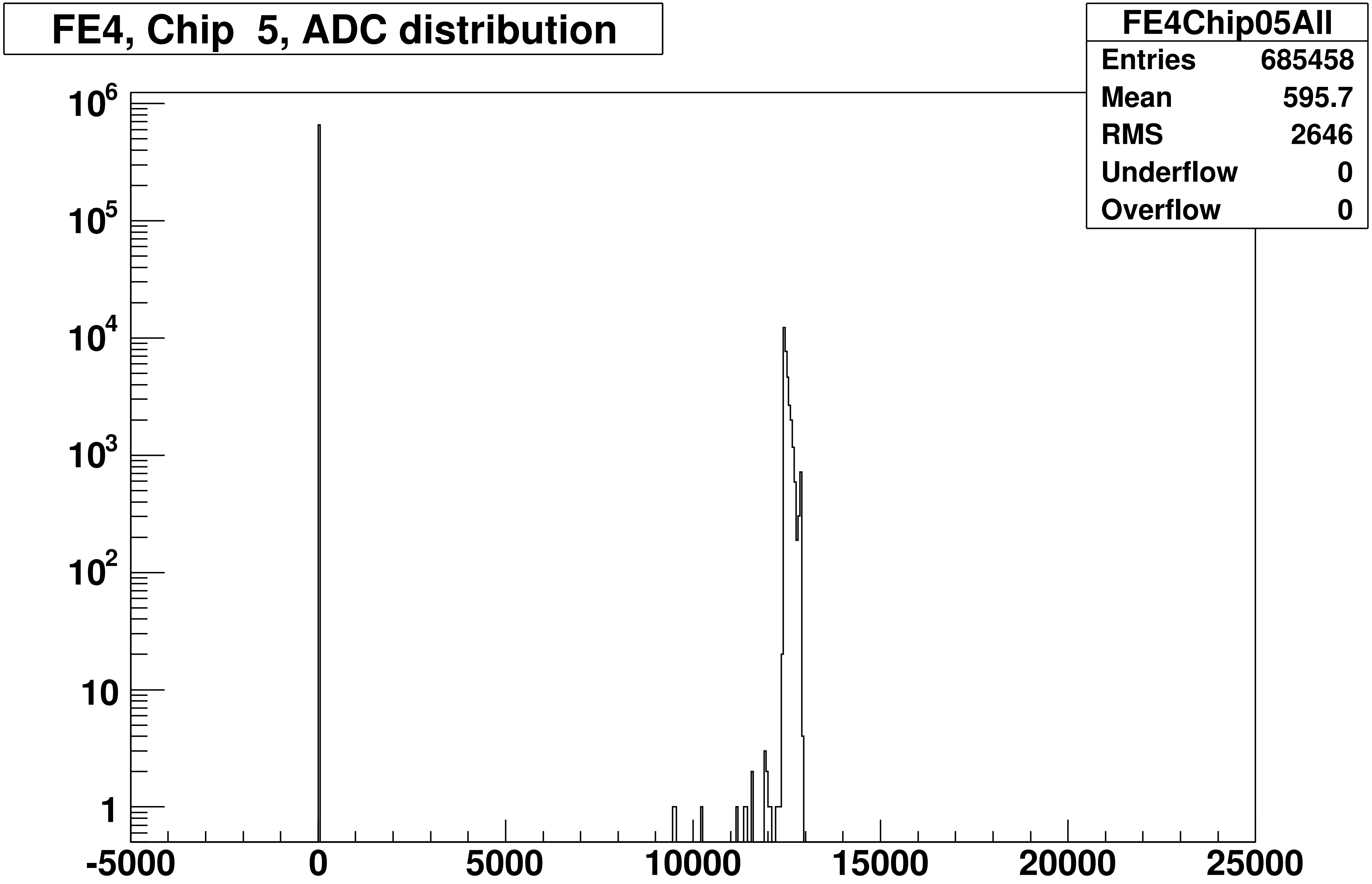

FE4, Chip 5, ADC distribution
FE4Chip05All
Entries 685458
Mean 595.7
RMS 2646
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
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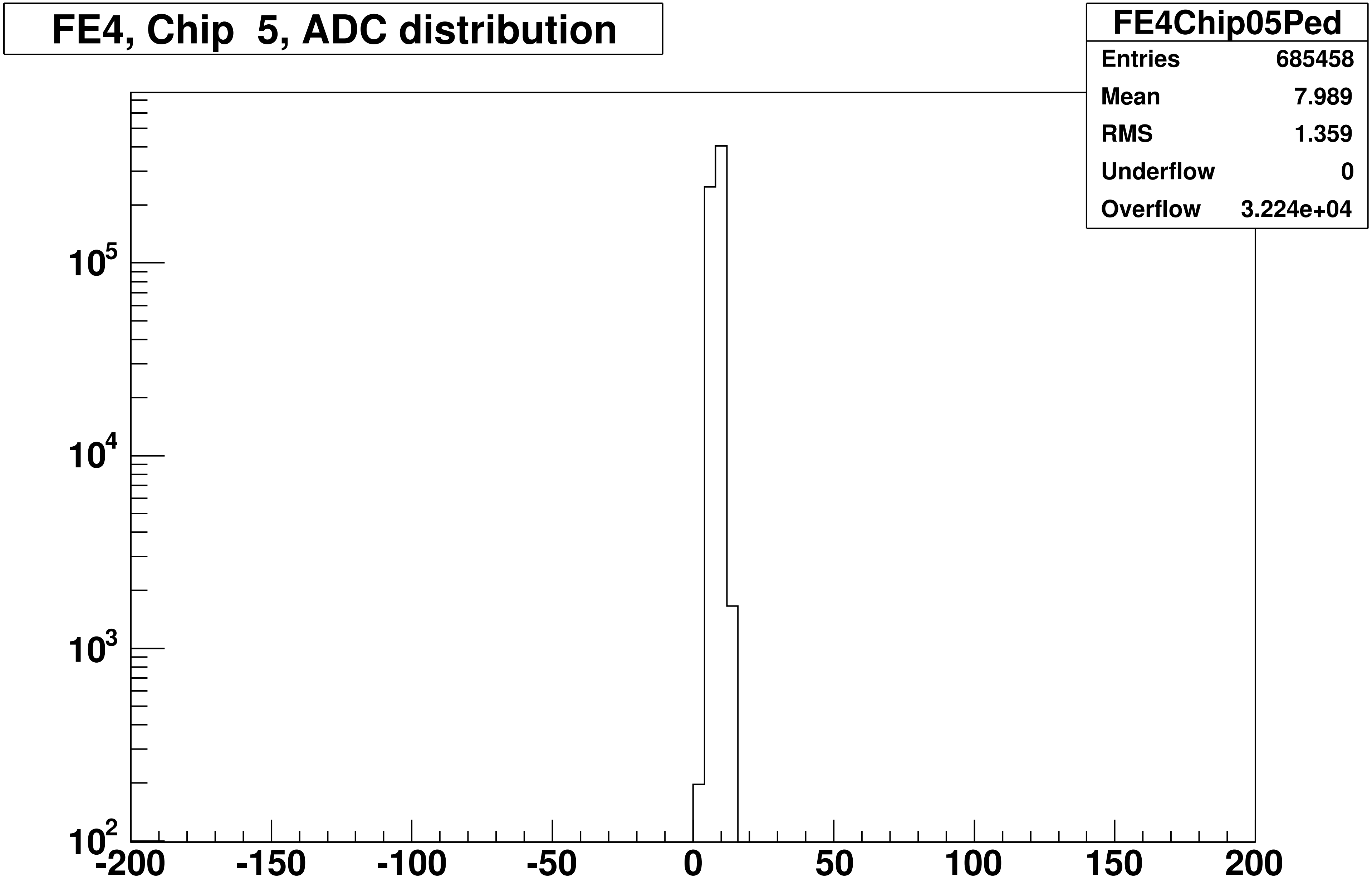

FE4, Chip 5, ADC distribution
FE4Chip05Ped
Entries 685458
Mean 7.989
RMS 1.359
Underflow 0
Overflow 3.224e+04
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10^4
10^3
10^2
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-150
-100
-50
0
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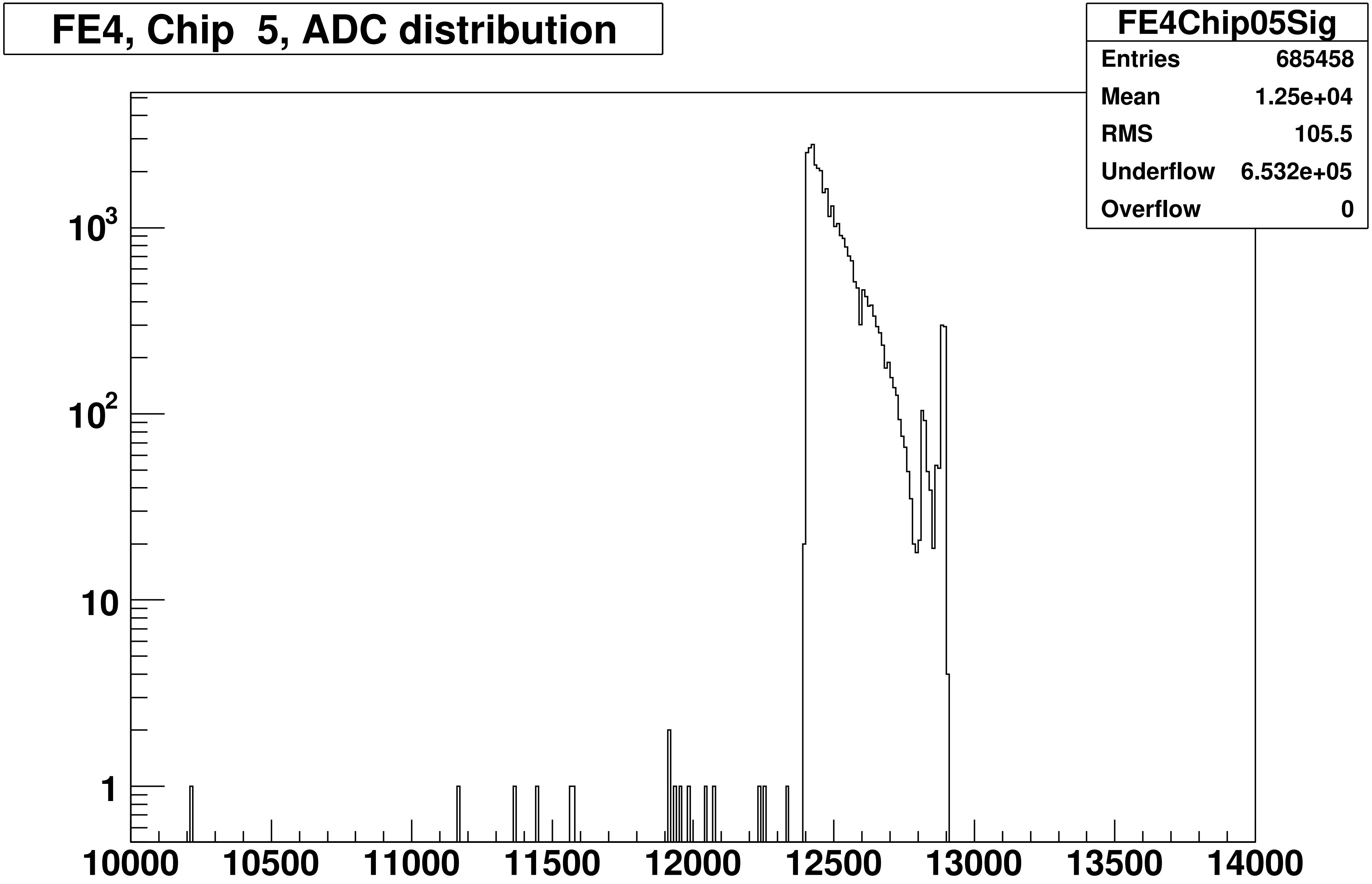
100
150
200



FE4, Chip 5, ADC distribution
FE4Chip05Sig
Entries 685458
Mean 1.25e+04
RMS 105.5
Underflow 6.532e+05
Overflow 0
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10^2
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1
10000
10500
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11500
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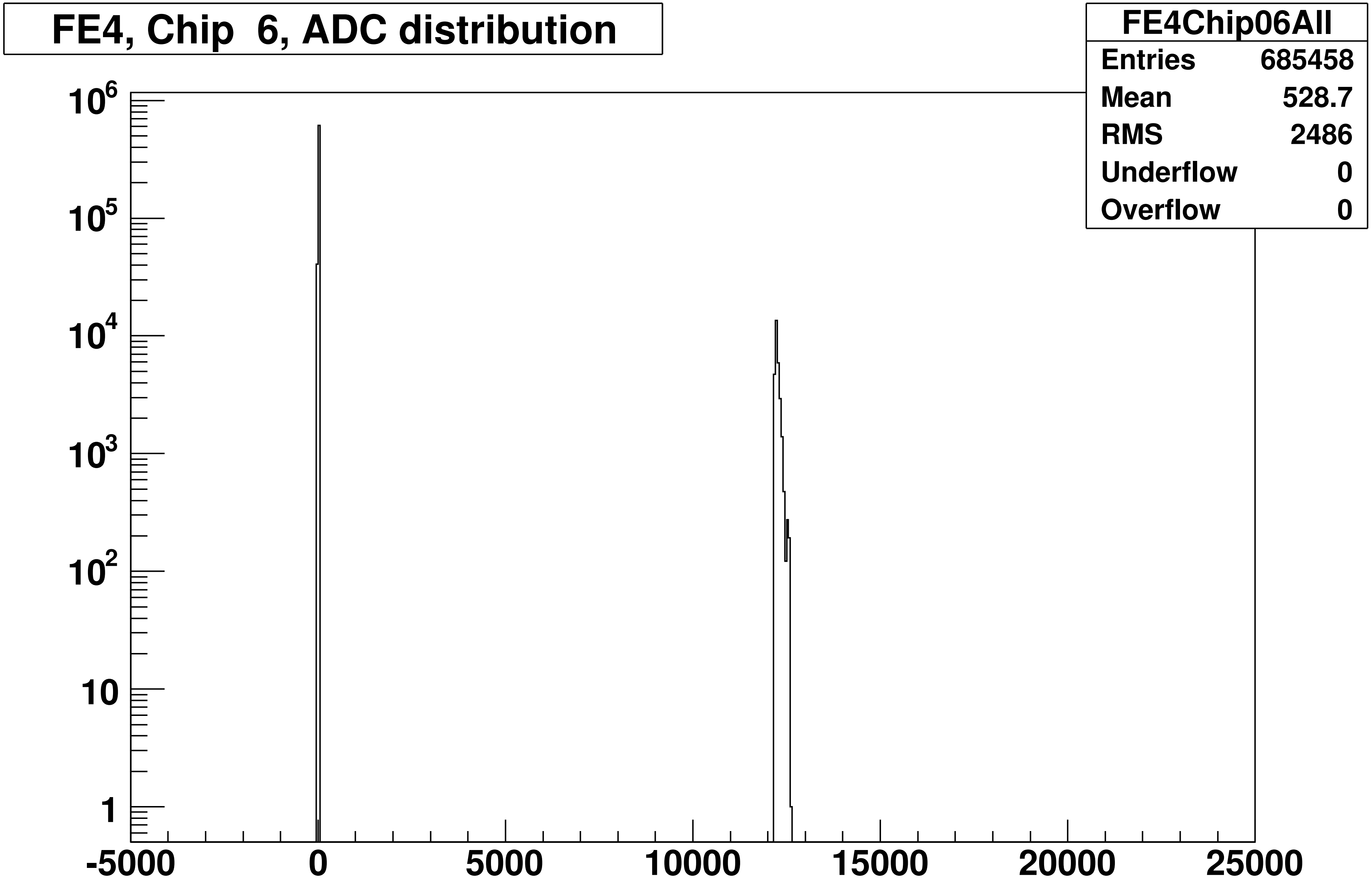
FE4, Chip 6, ADC distribution
FE4Chip06All
Entries 685458
Mean 528.7
RMS 2486
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
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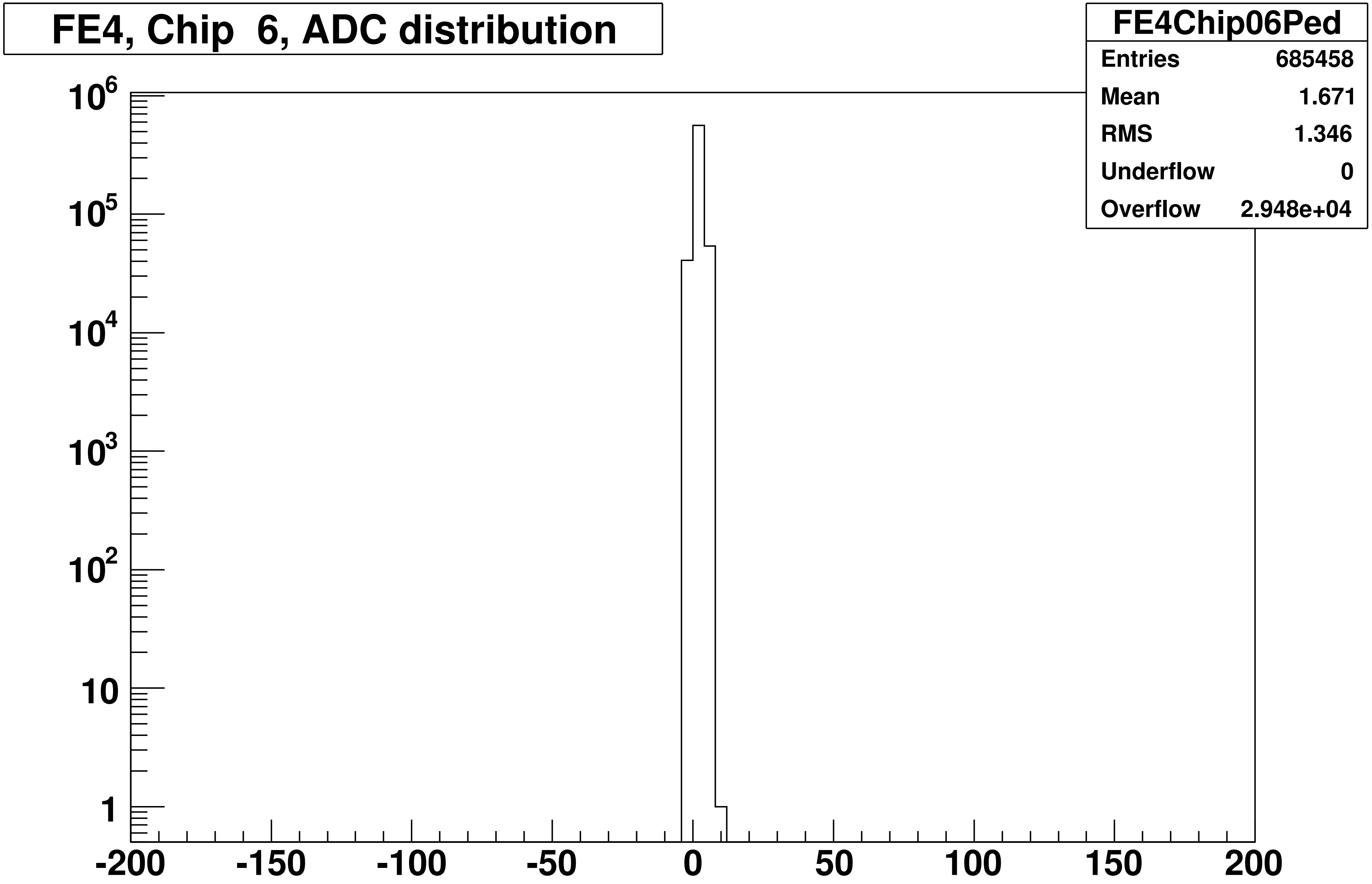
FE4, Chip 6, ADC distribution
FE4Chip06Ped
Entries 685458
Mean 1.671
RMS 1.346
Underflow 0
Overflow 2.948e+04
10^6
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
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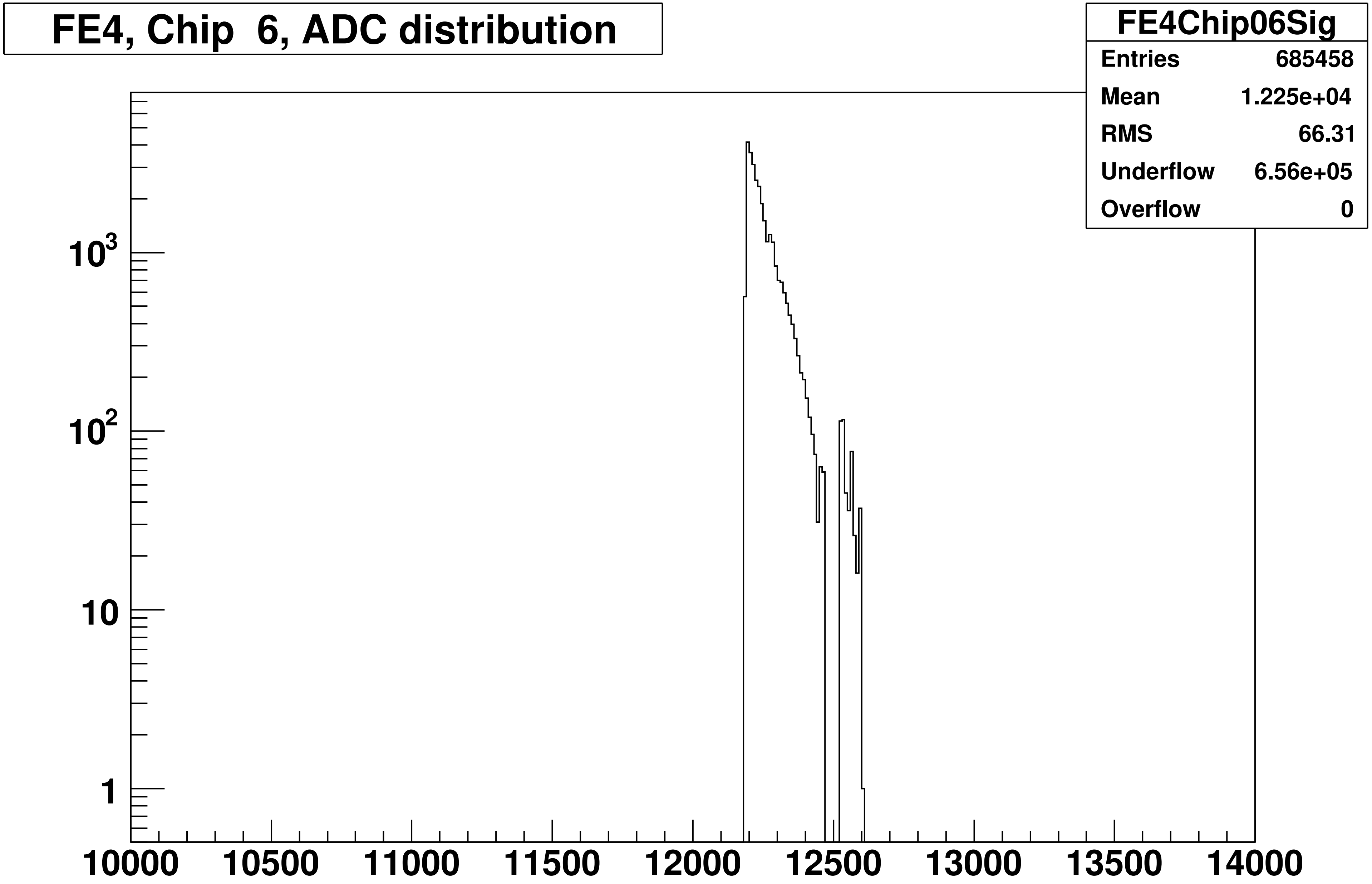
100
150
200



FE4, Chip 6, ADC distribution
FE4Chip06Sig
Entries 685458
Mean 1.225e+04
RMS 66.31
Underflow 6.56e+05
Overflow 0
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10^2
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1
10000
10500
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11500
12000
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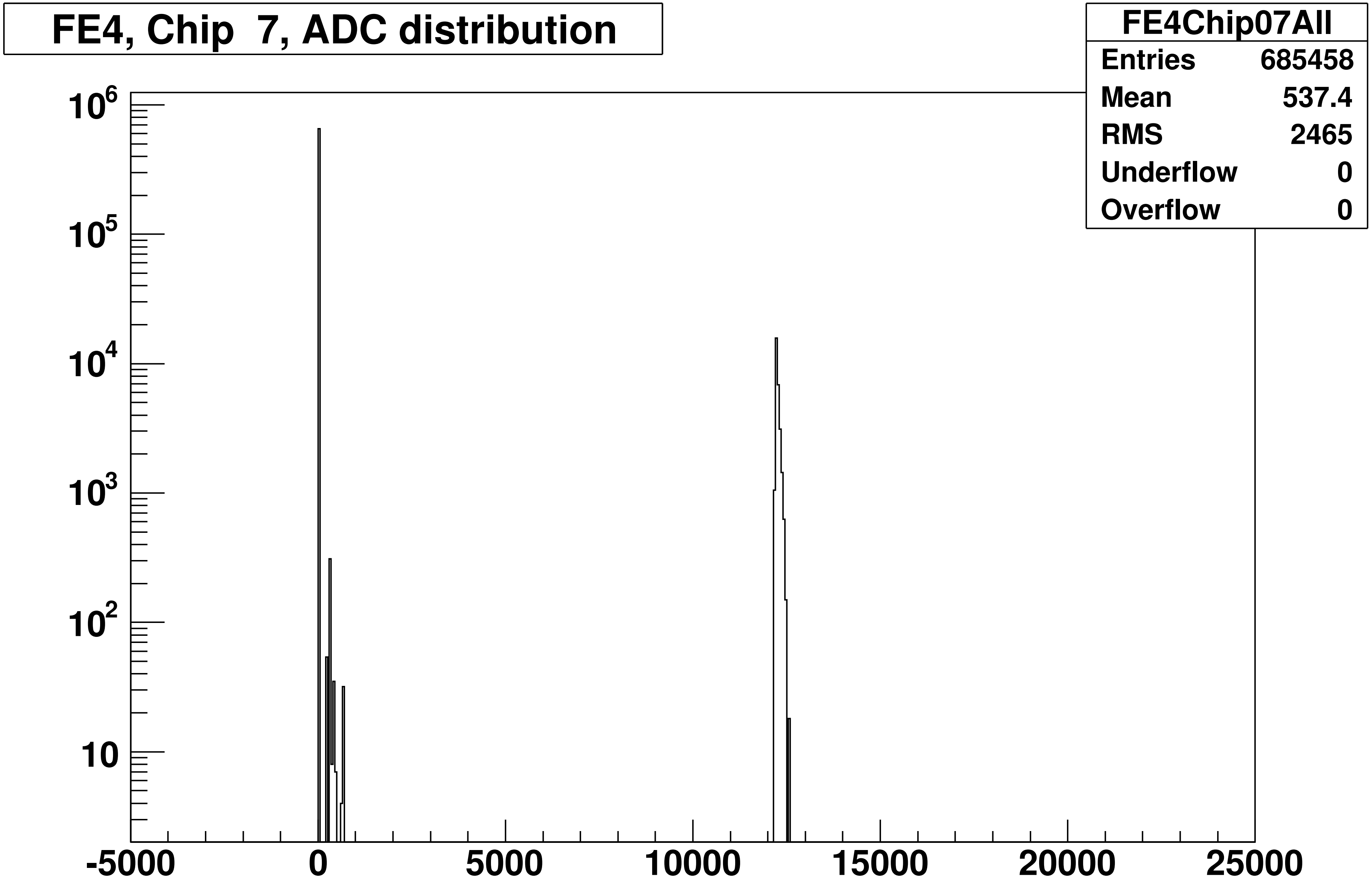
FE4, Chip 7, ADC distribution
FE4Chip07All
Entries 685458
Mean 537.4
RMS 2465
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
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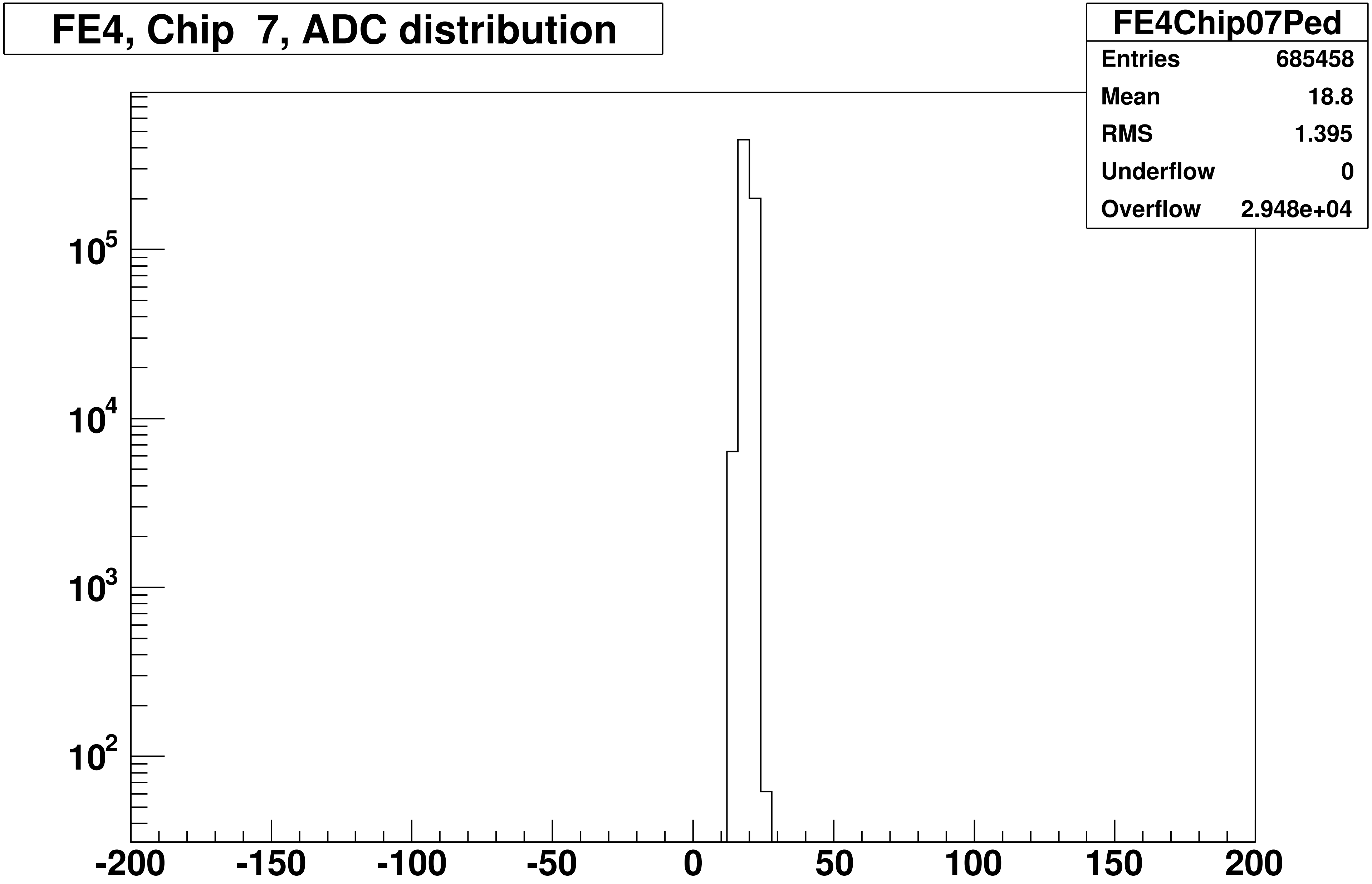
20000
25000



FE4, Chip 7, ADC distribution
FE4Chip07Ped
Entries 685458
Mean 18.8
RMS 1.395
Underflow 0
Overflow 2.948e+04
10^5
10^4
10^3
10^2
-200
-150
-100
-50
0
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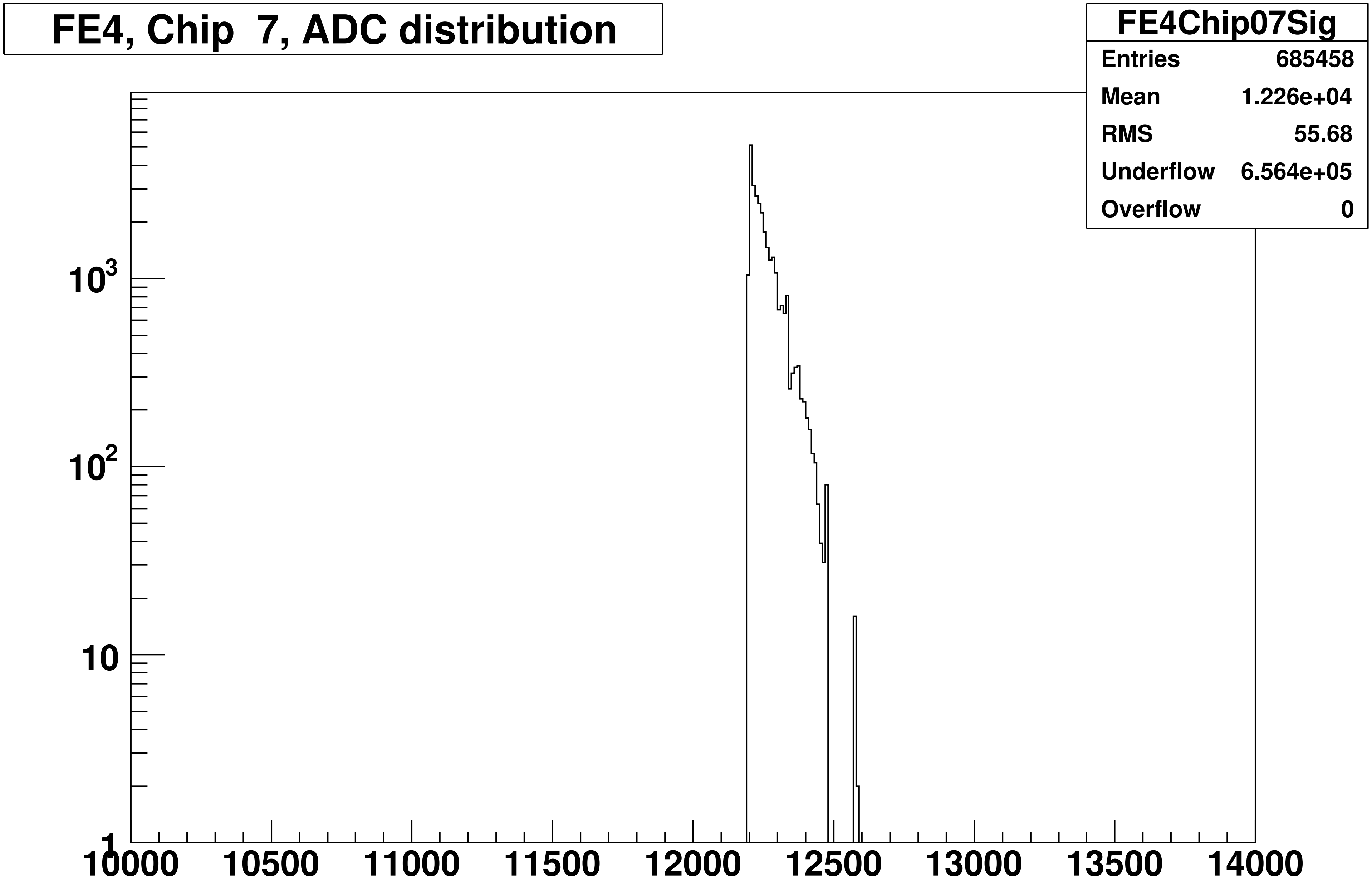
100
150
200



FE4, Chip 7, ADC distribution
FE4Chip07Sig
Entries 685458
Mean 1.226e+04
RMS 55.68
Underflow 6.564e+05
Overflow 0
10^3
10^2
10
1
10000
10500
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11500
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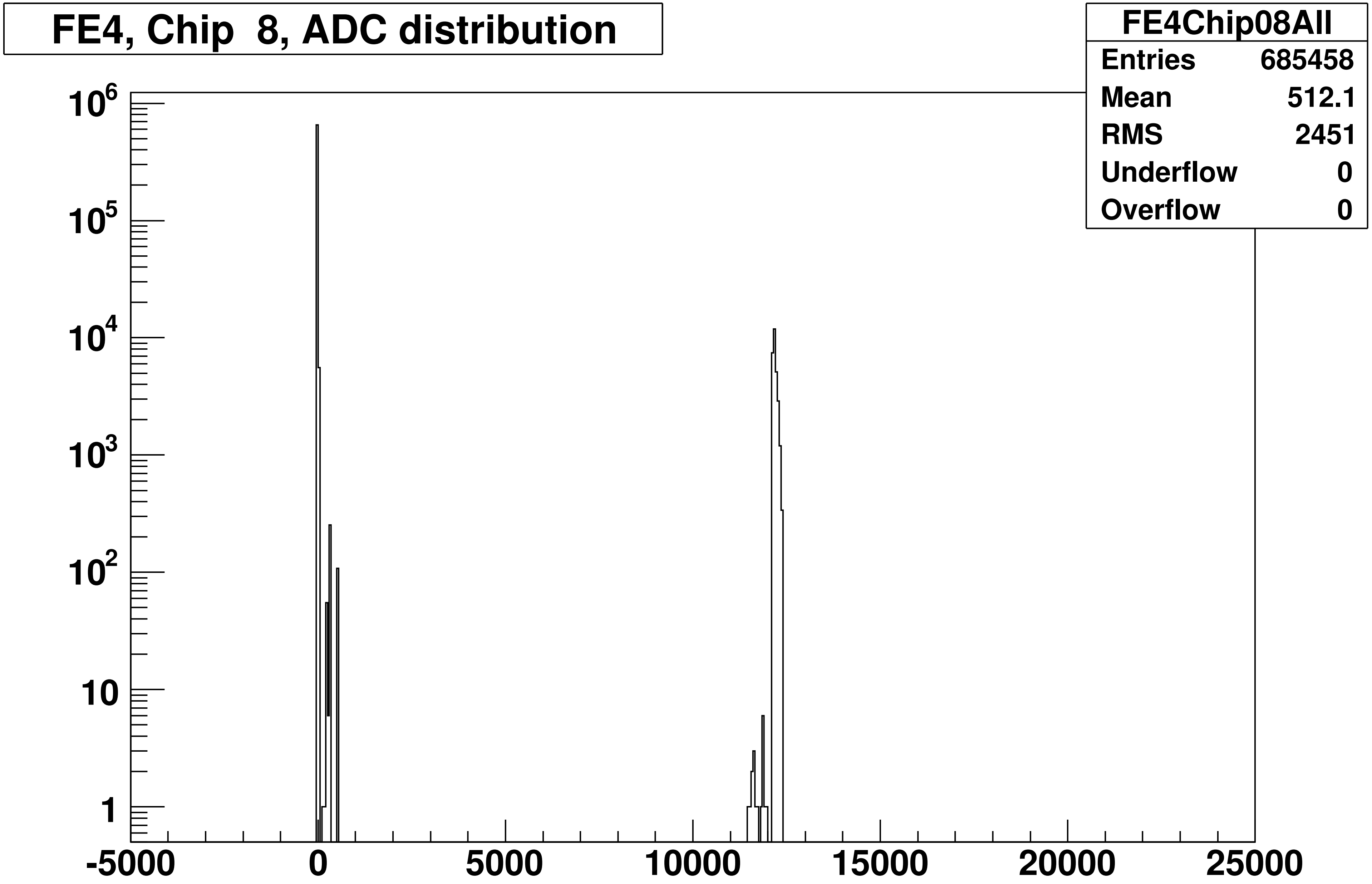
13500
14000


FE4, Chip 8, ADC distribution
FE4Chip08All
Entries 685458
Mean 512.1
RMS 2451
Underflow 0
Overflow 0
10^6
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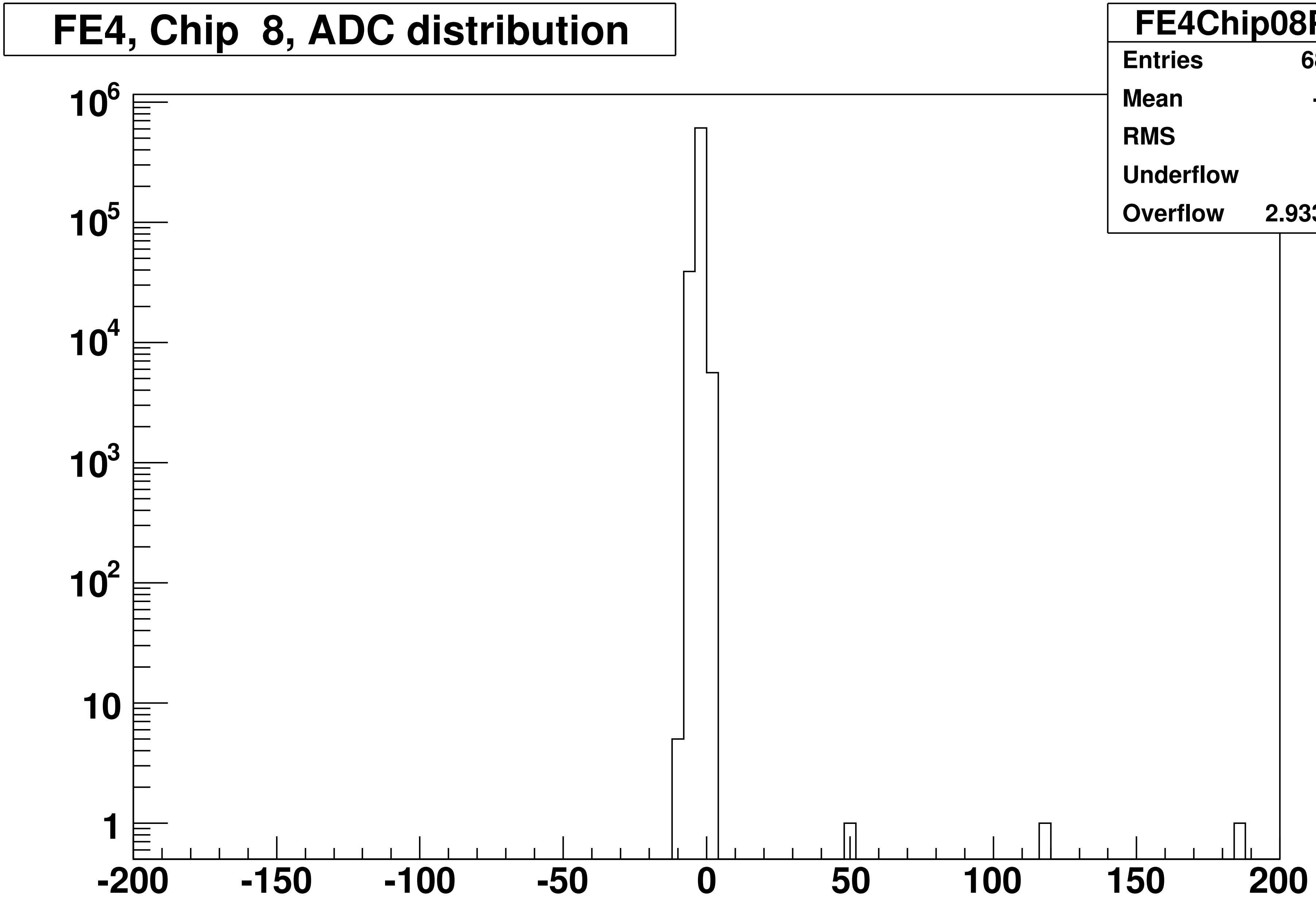
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE4, Chip 8, ADC distribution
FE4Chip08Ped
Entries 685458
Mean -2.343
RMS 1.247
Underflow 0
Overflow 2.933e+04
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10^5
10^4
10^3
10^2
10
1
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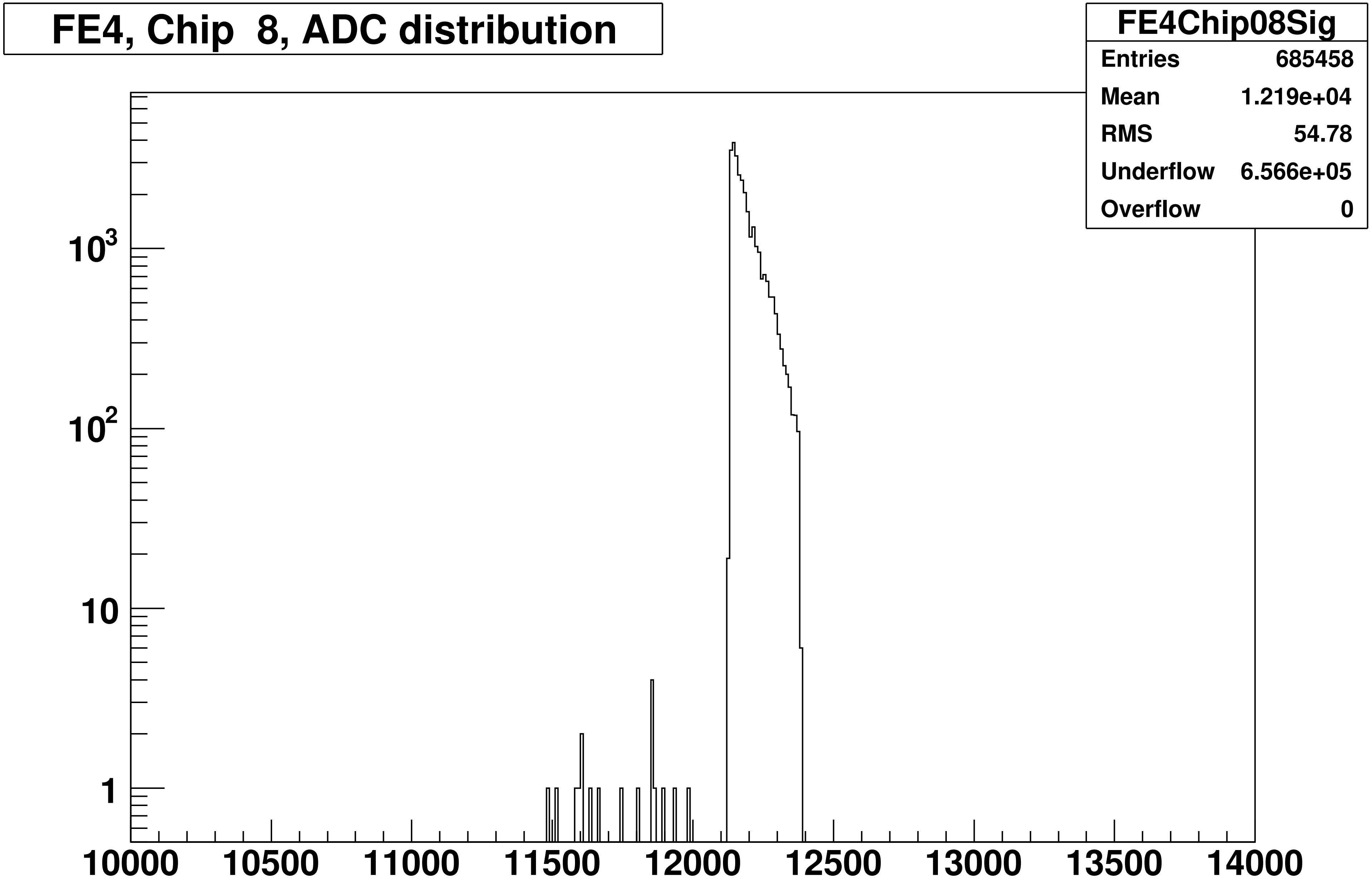
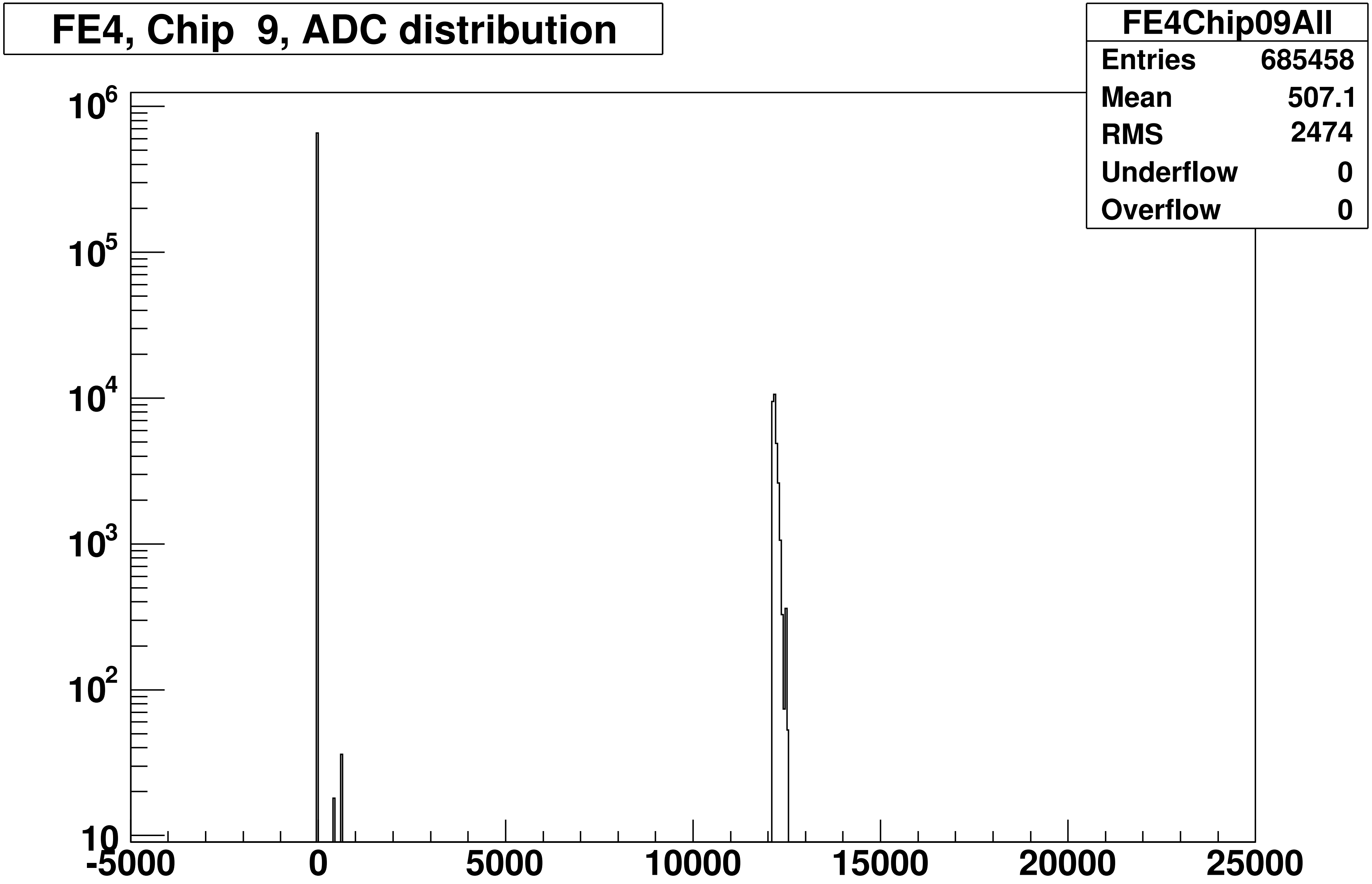
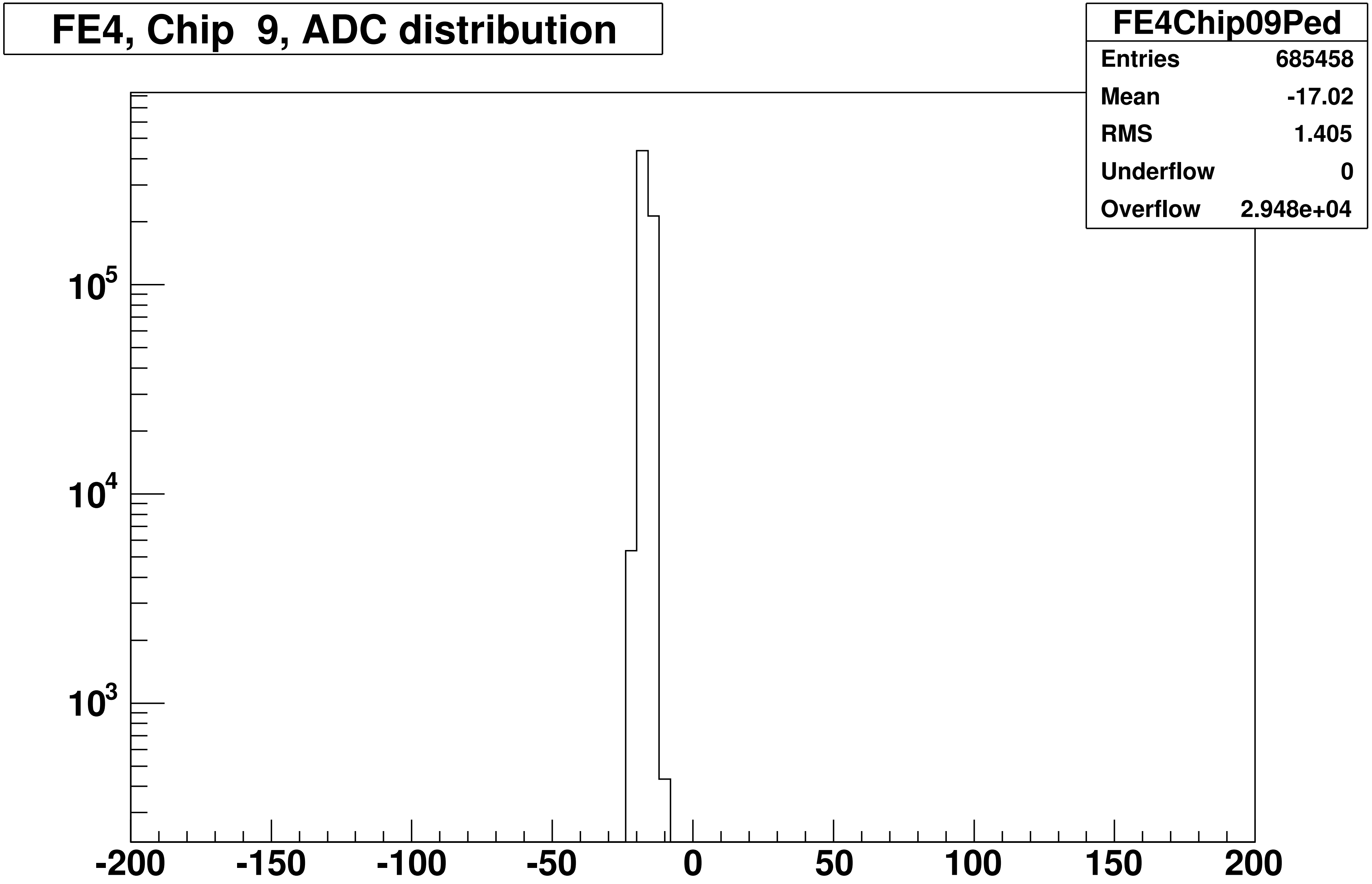
-150
-100
-50
0
50
100
150
200



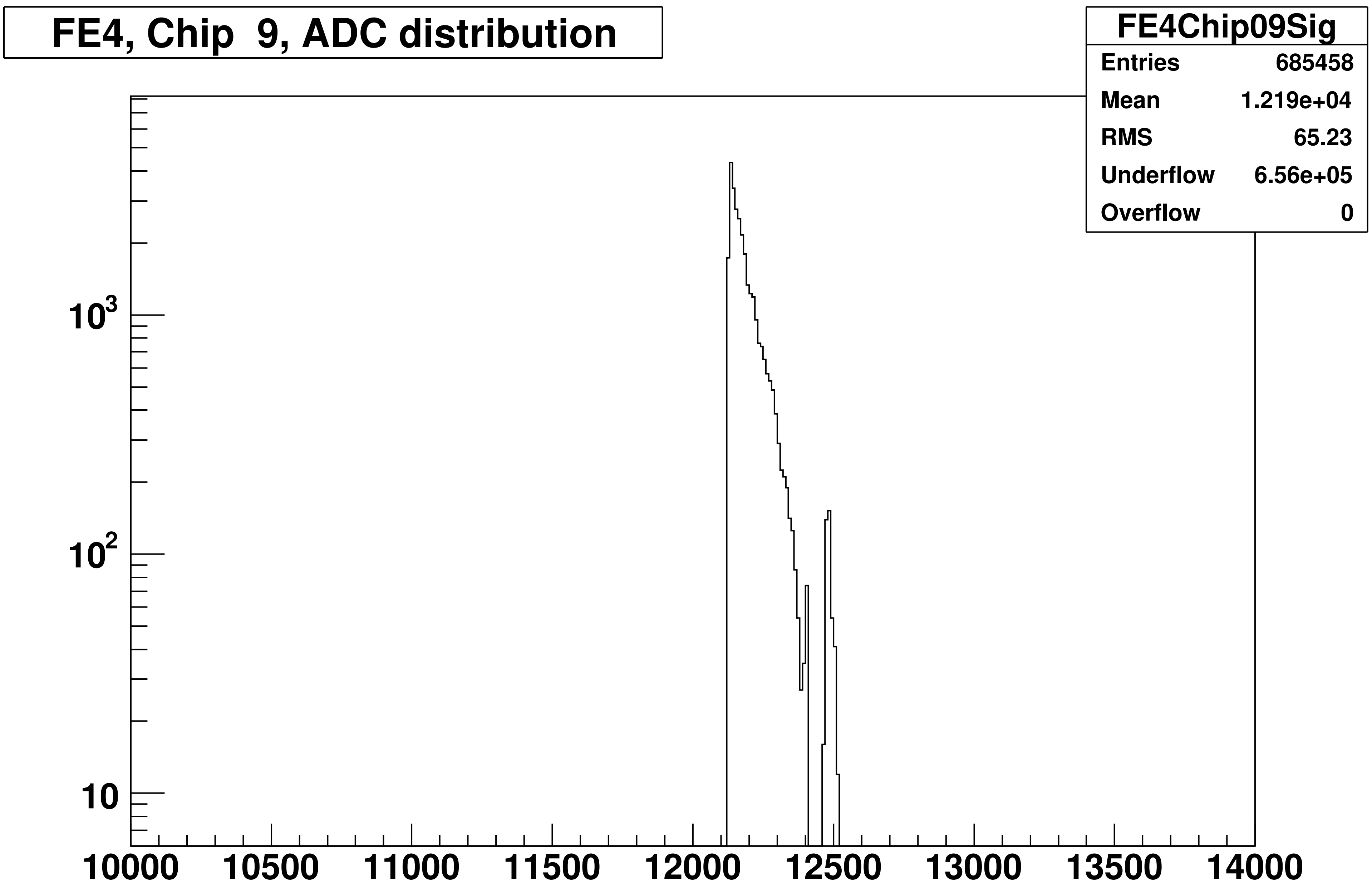
FE4, Chip 8, ADC distribution
FE4Chip08Sig
Entries 685458
Mean 1.219e+04
RMS 54.78
Underflow 6.566e+05
Overflow 0
10^3
10^2
10
1
10000
10500
11000
11500
12000
12500
13000
13500
14000

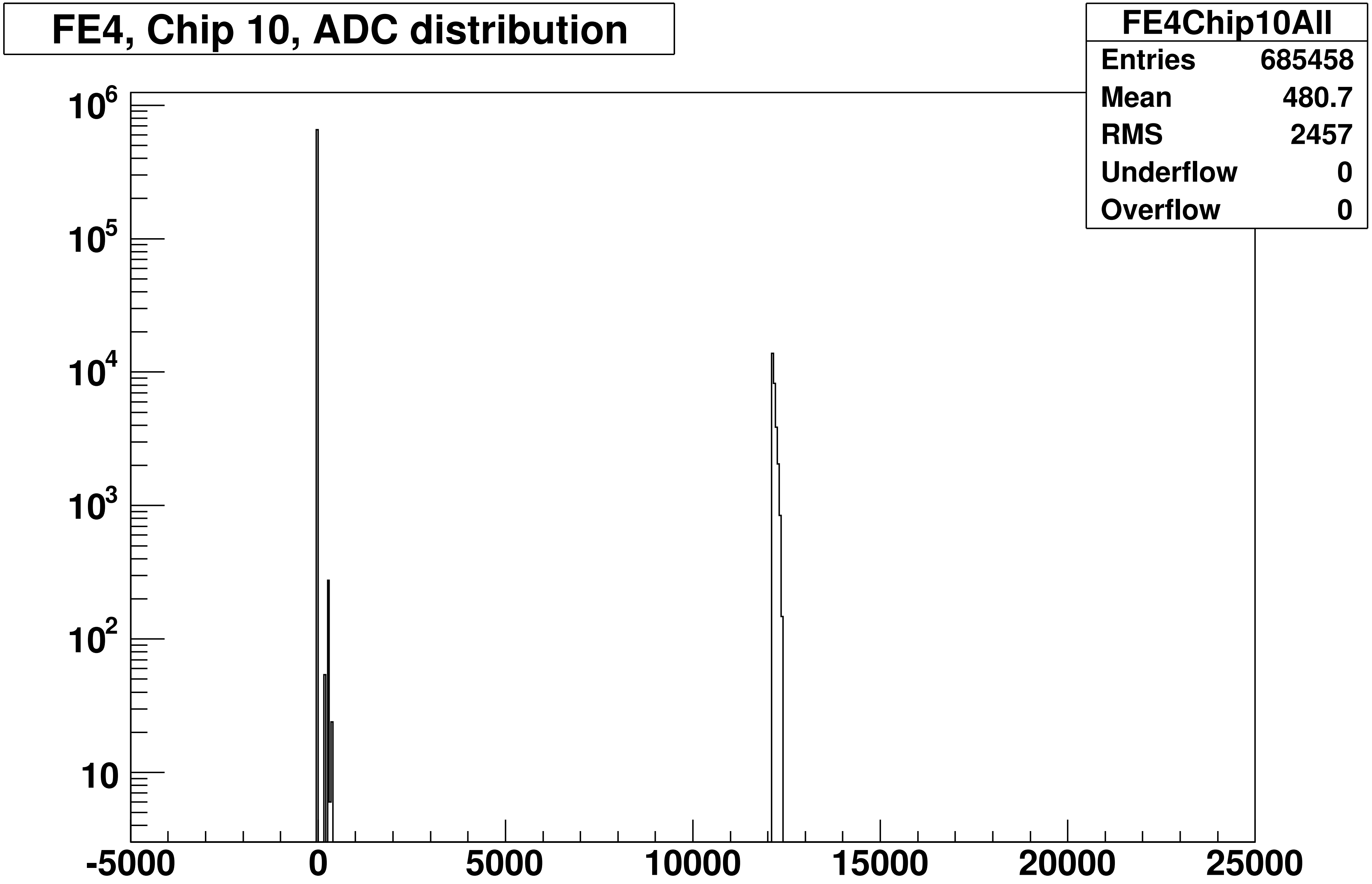


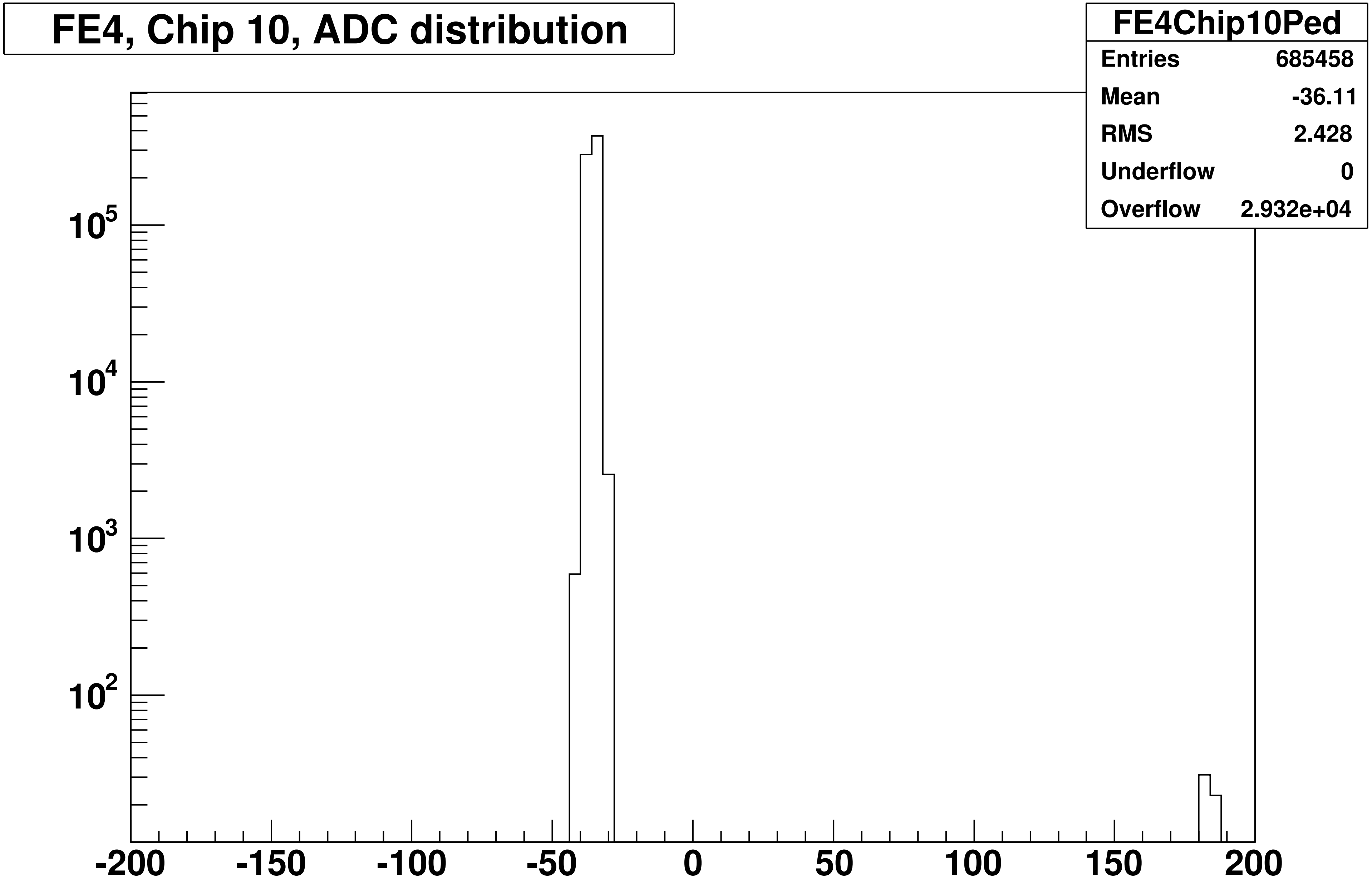
FE4, Chip 9, ADC distribution
FE4Chip09All
Entries 685458
Mean 507.1
RMS 2474
Underflow 0
Overflow 0
10
10^2
10^3
10^4
10^5
10^6
-5000
0
5000
10000
15000
20000
25000

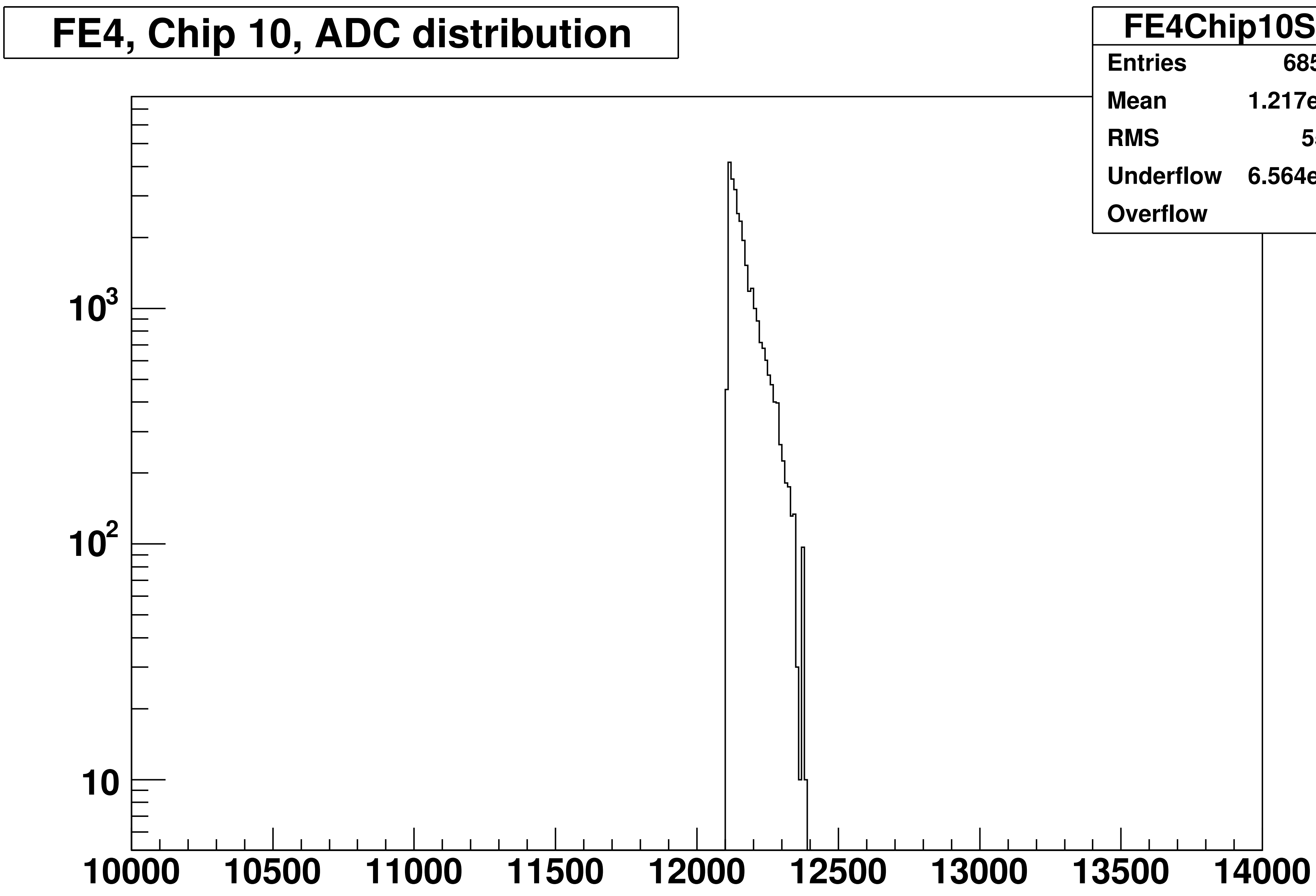


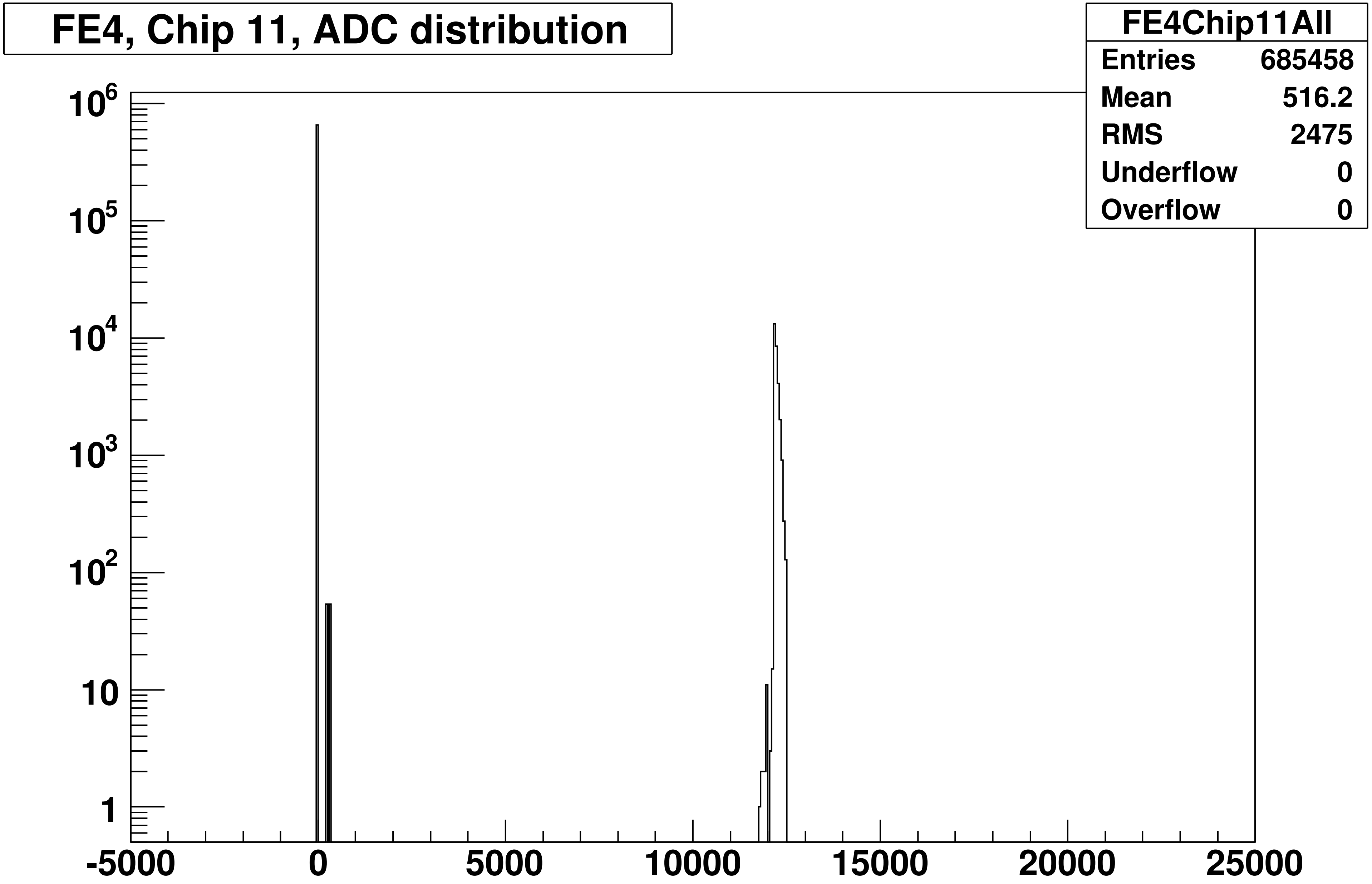
FE4, Chip 9, ADC distribution
FE4Chip09Ped
Entries 685458
Mean -17.02
RMS 1.405
Underflow 0
Overflow 2.948e+04
10^5
10^4
10^3
-200
-150
-100
-50
0
50
100
150
200

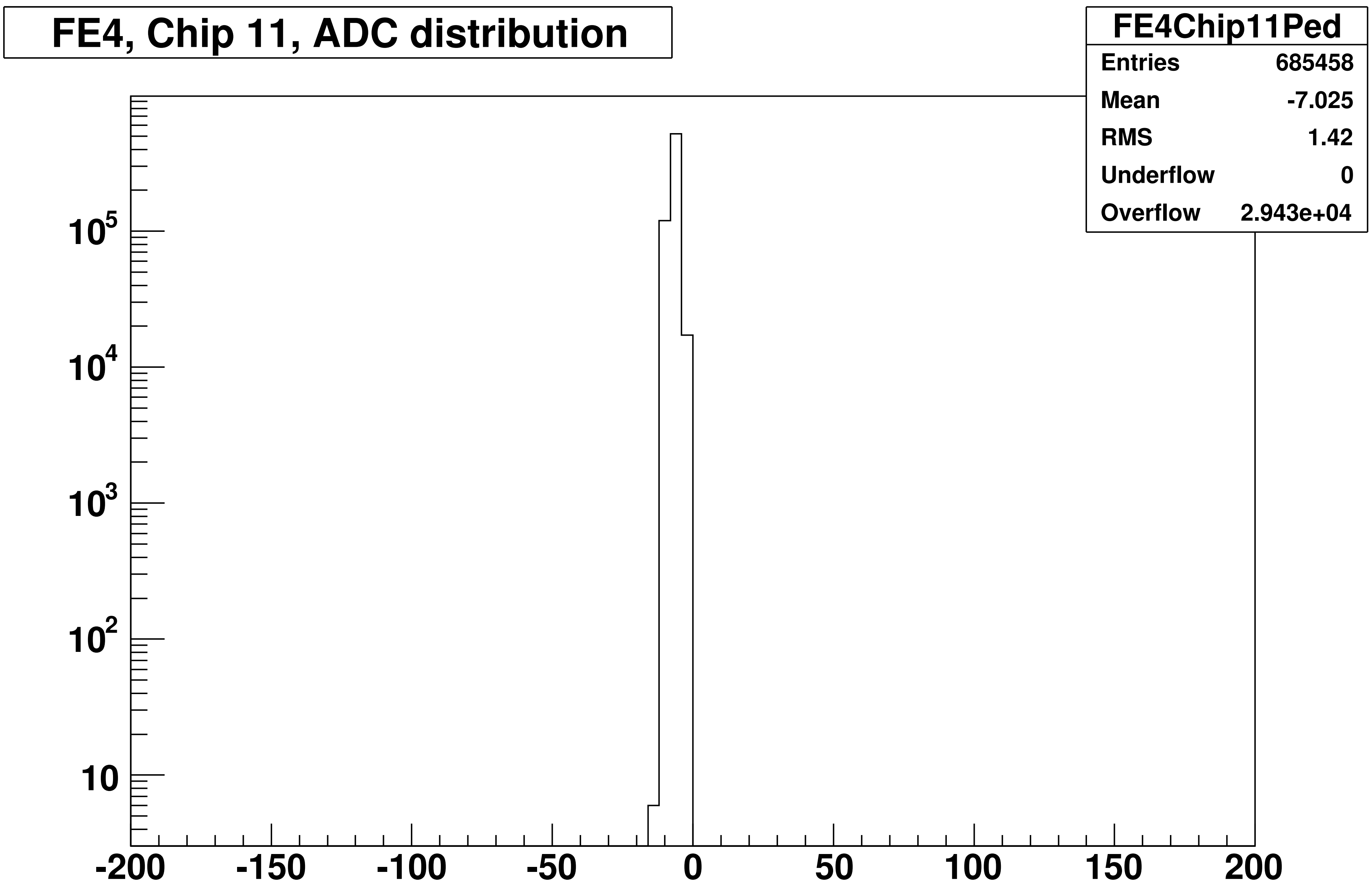

FE4, Chip 9, ADC distribution
FE4Chip09Sig
Entries 685458
Mean 1.219e+04
RMS 65.23
Underflow 6.56e+05
Overflow 0
10^3
10^2
10
10000
10500
11000
11500
12000
12500
13000
13500
14000


FE4, Chip 10, ADC distribution
FE4Chip10All
Entries 685458
Mean 480.7
RMS 2457
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE4, Chip 10, ADC distribution
FE4Chip10Ped
Entries 685458
Mean -36.11
RMS 2.428
Underflow 0
Overflow 2.932e+04
10^5
10^4
10^3
10^2
-200
-150
-100
-50
0
50
100
150
200


FE4, Chip 10, ADC distribution
FE4Chip10Sig
Entries 685458
Mean 1.217e+04
RMS 55.04
Underflow 6.564e+05
Overflow 0
10
10^2
10^3
10000
10500
11000
11500
12000
12500
13000
13500
14000


FE4, Chip 11, ADC distribution
FE4Chip11All
Entries 685458
Mean 516.2
RMS 2475
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE4, Chip 11, ADC distribution
FE4Chip11Ped
Entries 685458
Mean -7.025
RMS 1.42
Underflow 0
Overflow 2.943e+04
10^5
10^4
10^3
10^2
10
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0
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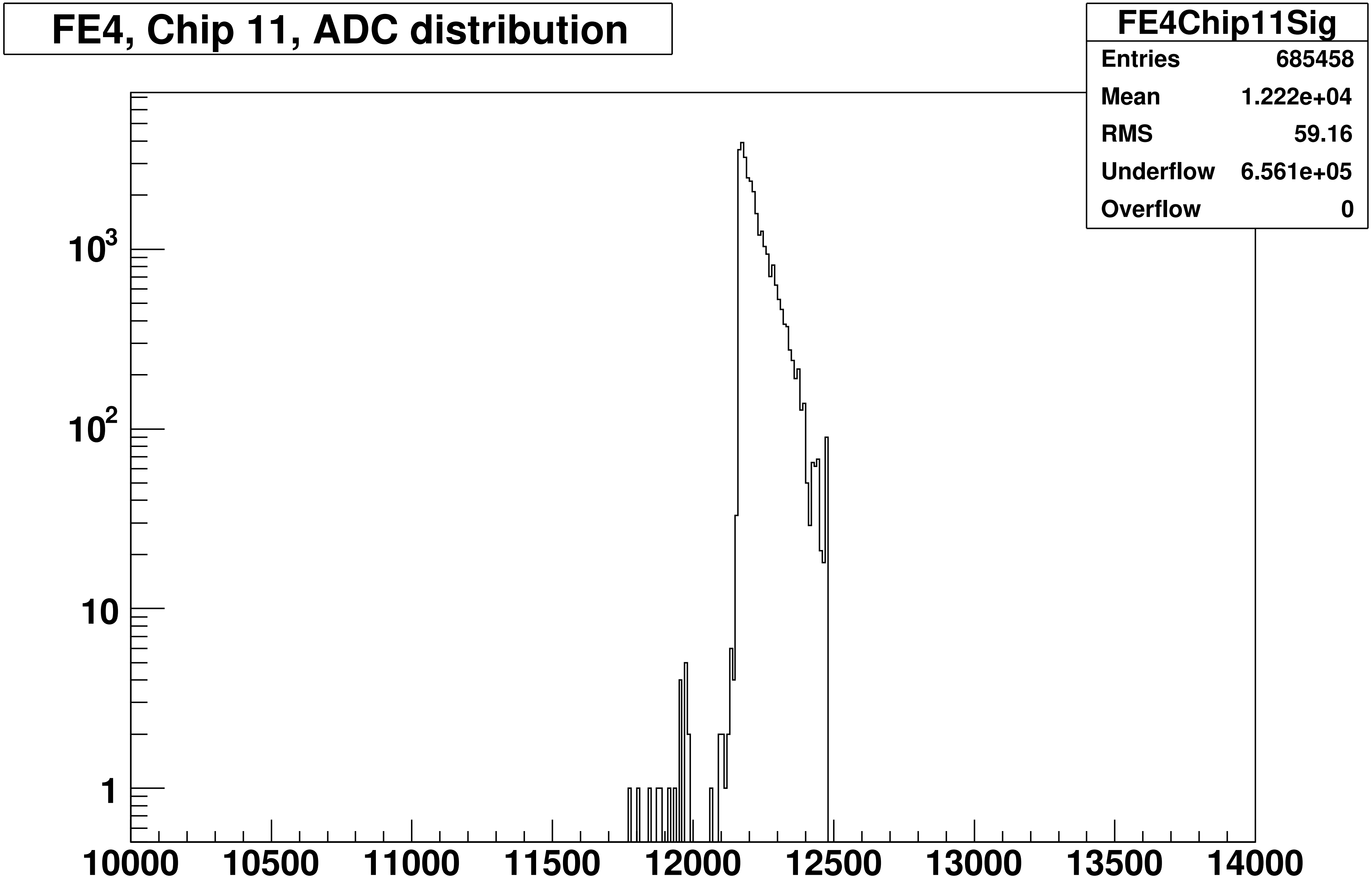
100
150
200


FE4, Chip 11, ADC distribution
FE4Chip11Sig
Entries 685458
Mean 1.222e+04
RMS 59.16
Underflow 6.561e+05
Overflow 0
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10^2
10
1
10000
10500
11000
11500
12000
12500
13000
13500
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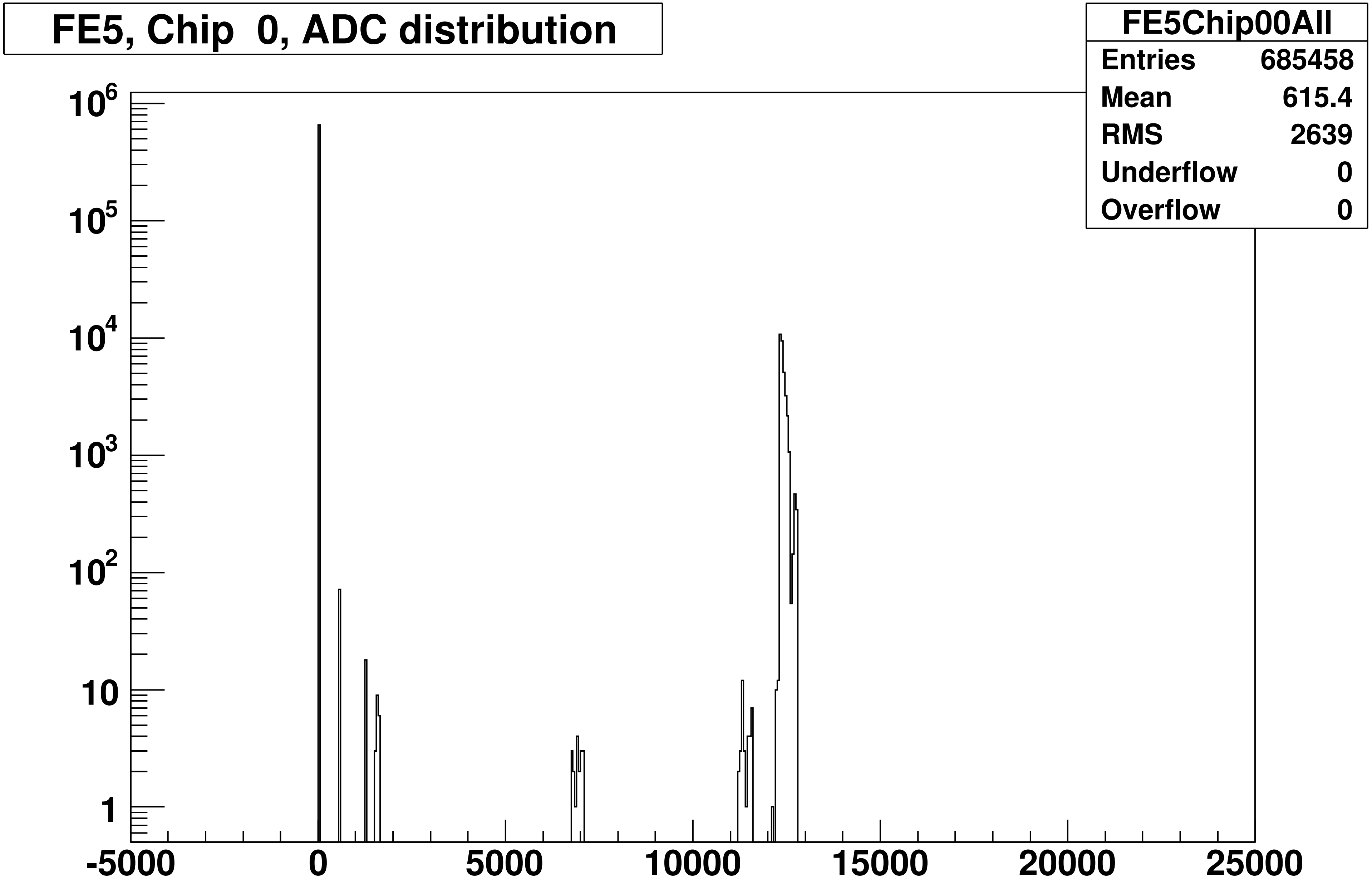
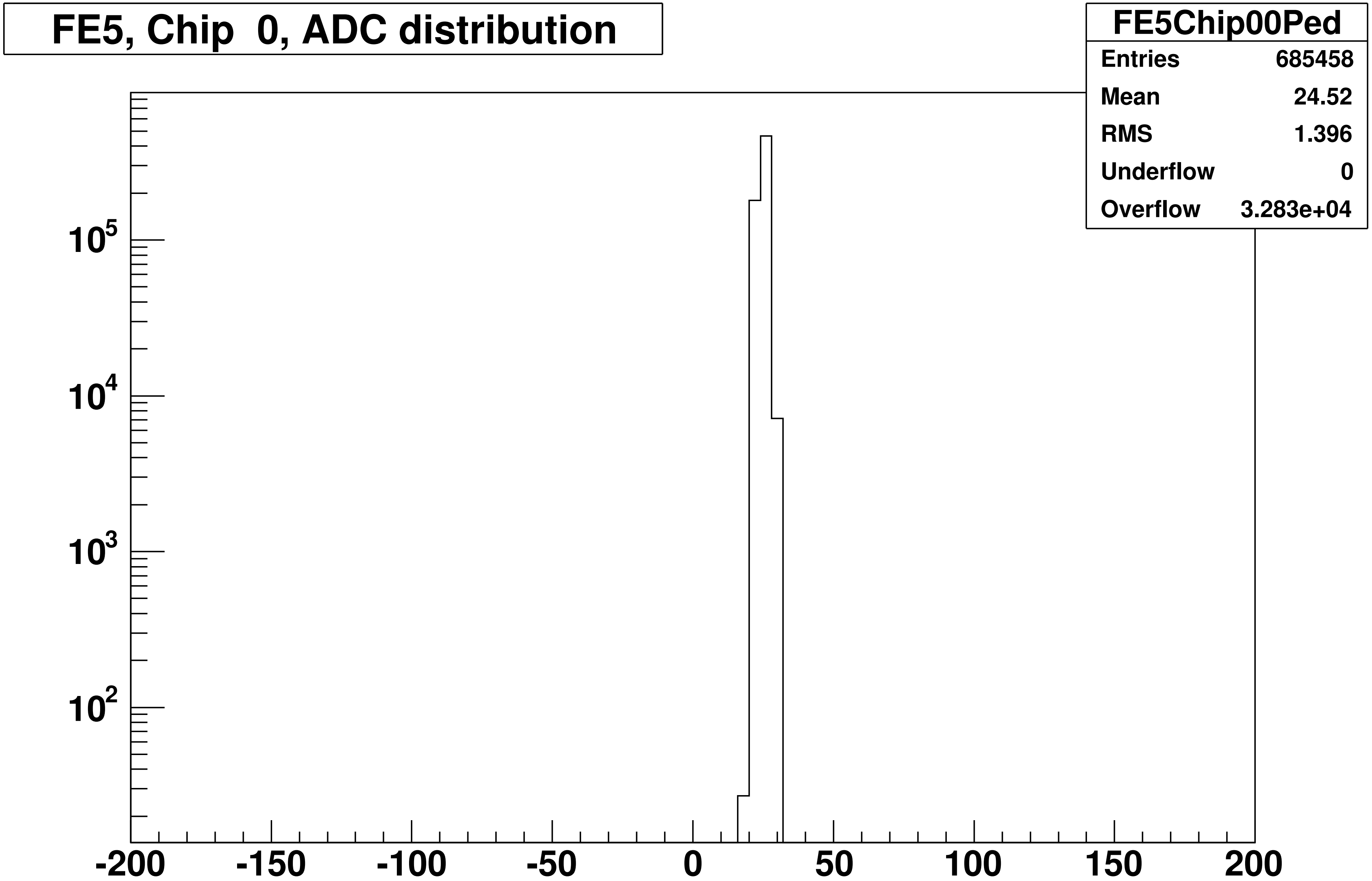
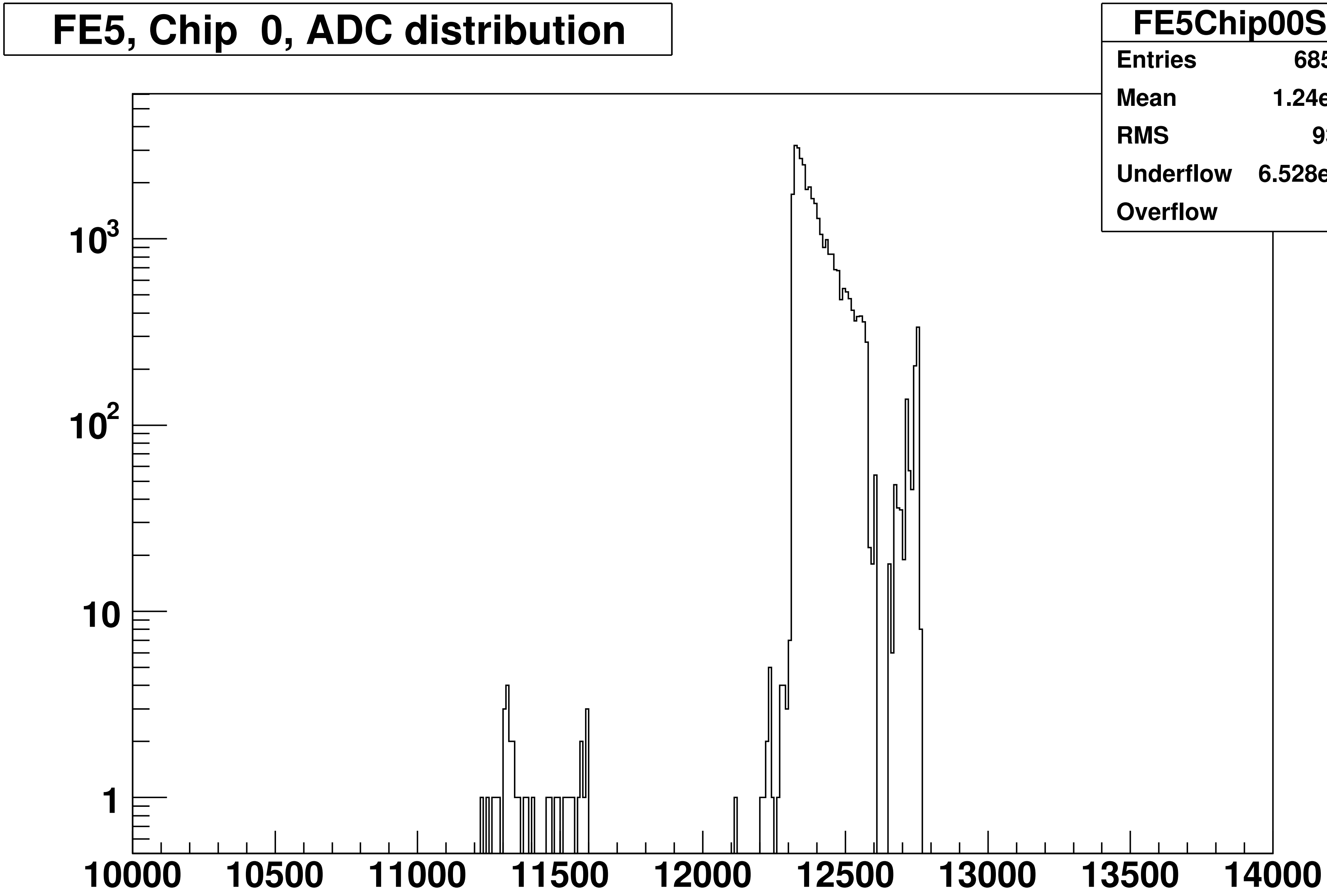
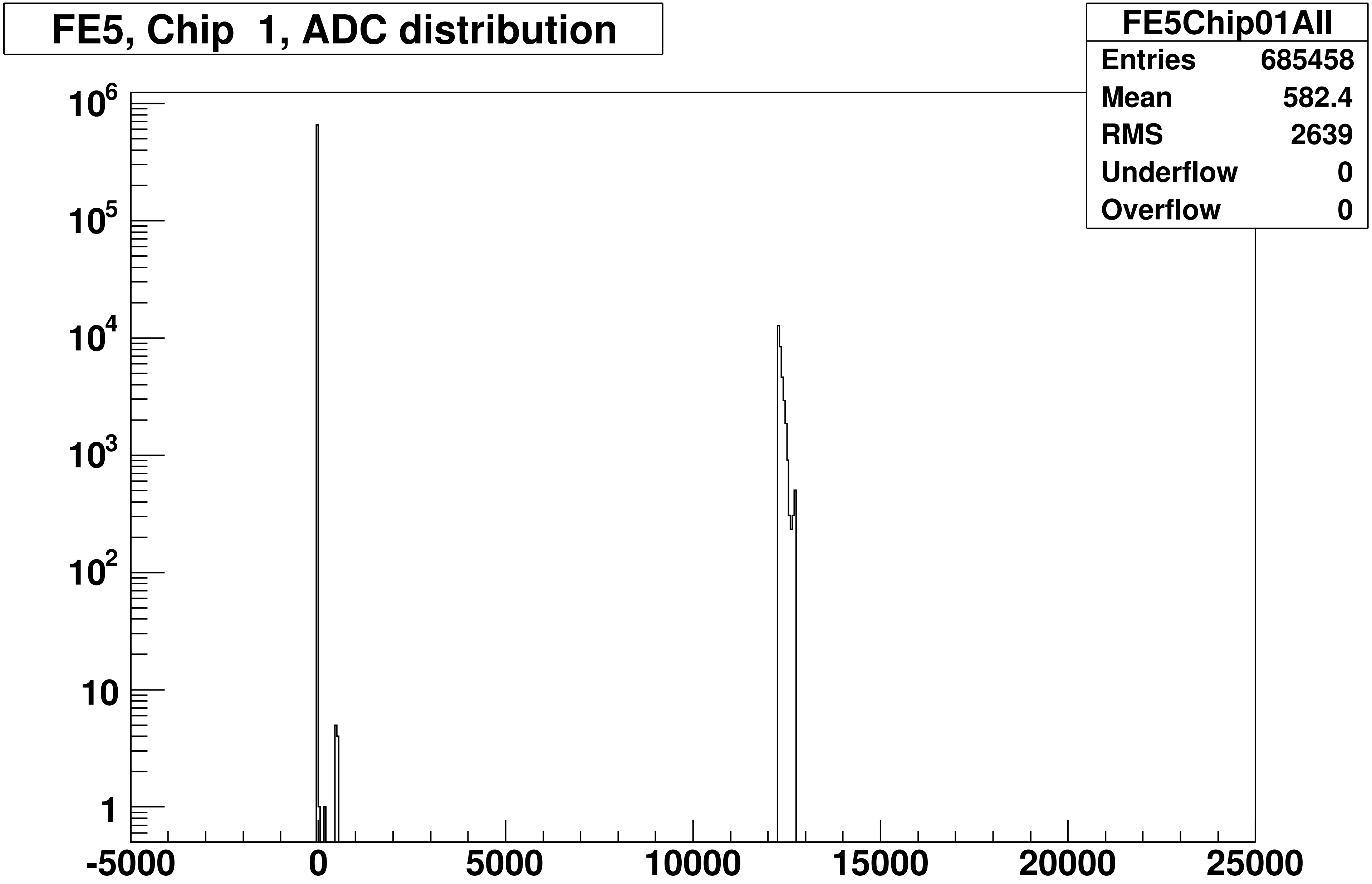
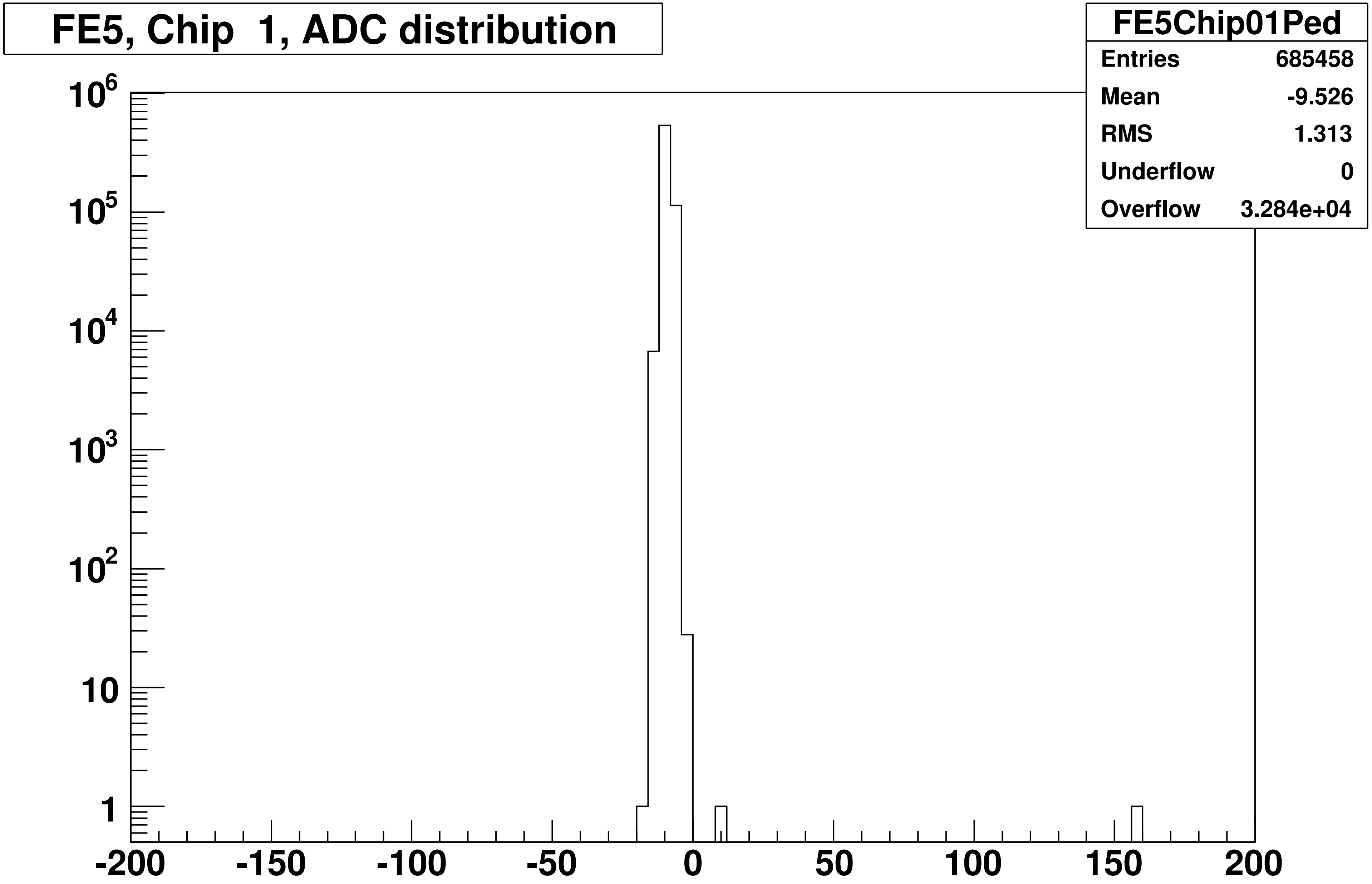

FE5, Chip 0, ADC distribution
FE5Chip00All
Entries 685458
Mean 615.4
RMS 2639
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE5, Chip 0, ADC distribution
FE5Chip00Ped
Entries 685458
Mean 24.52
RMS 1.396
Underflow 0
Overflow 3.283e+04
10^5
10^4
10^3
10^2
-200
-150
-100
-50
0
50
100
150
200


FE5, Chip 0, ADC distribution
FE5Chip00Sig
Entries 685458
Mean 1.24e+04
RMS 93.87
Underflow 6.528e+05
Overflow 0
10^3
10^2
10
1
10000
10500
11000
11500
12000
12500
13000
13500
14000



FE5, Chip 1, ADC distribution
FE5Chip01All
Entries 685458
Mean 582.4
RMS 2639
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE5, Chip 1, ADC distribution
FE5Chip01Ped
Entries 685458
Mean -9.526
RMS 1.313
Underflow 0
Overflow 3.284e+04
10^6
10^5
10^4
10^3
10^2
10
1
-200
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-100
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0
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150
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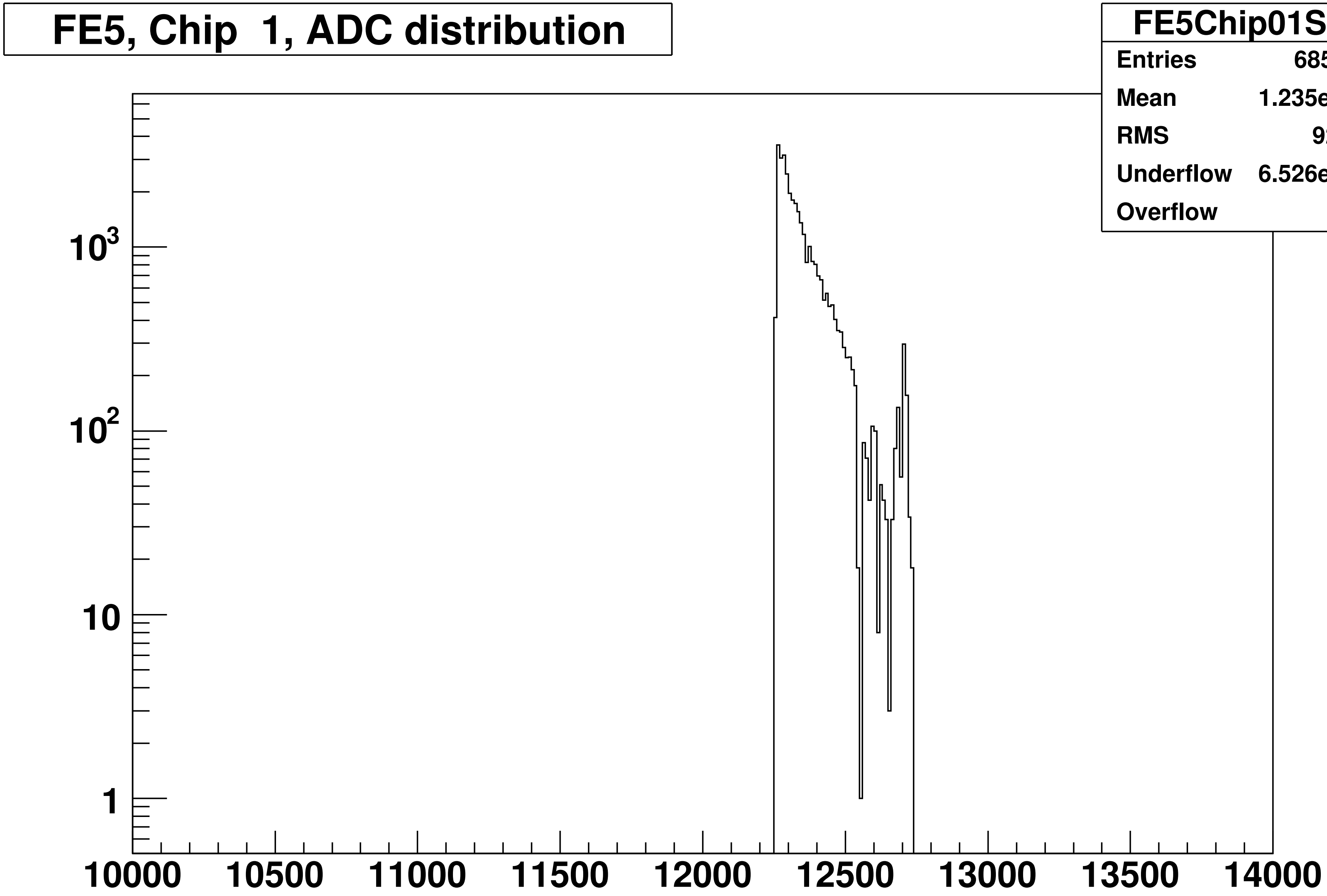
FE5, Chip 1, ADC distribution
FE5Chip01Sig
Entries 685458
Mean 1.235e+04
RMS 92.75
Underflow 6.526e+05
Overflow 0
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10^2
10
1
10000
10500
11000
11500
12000
12500
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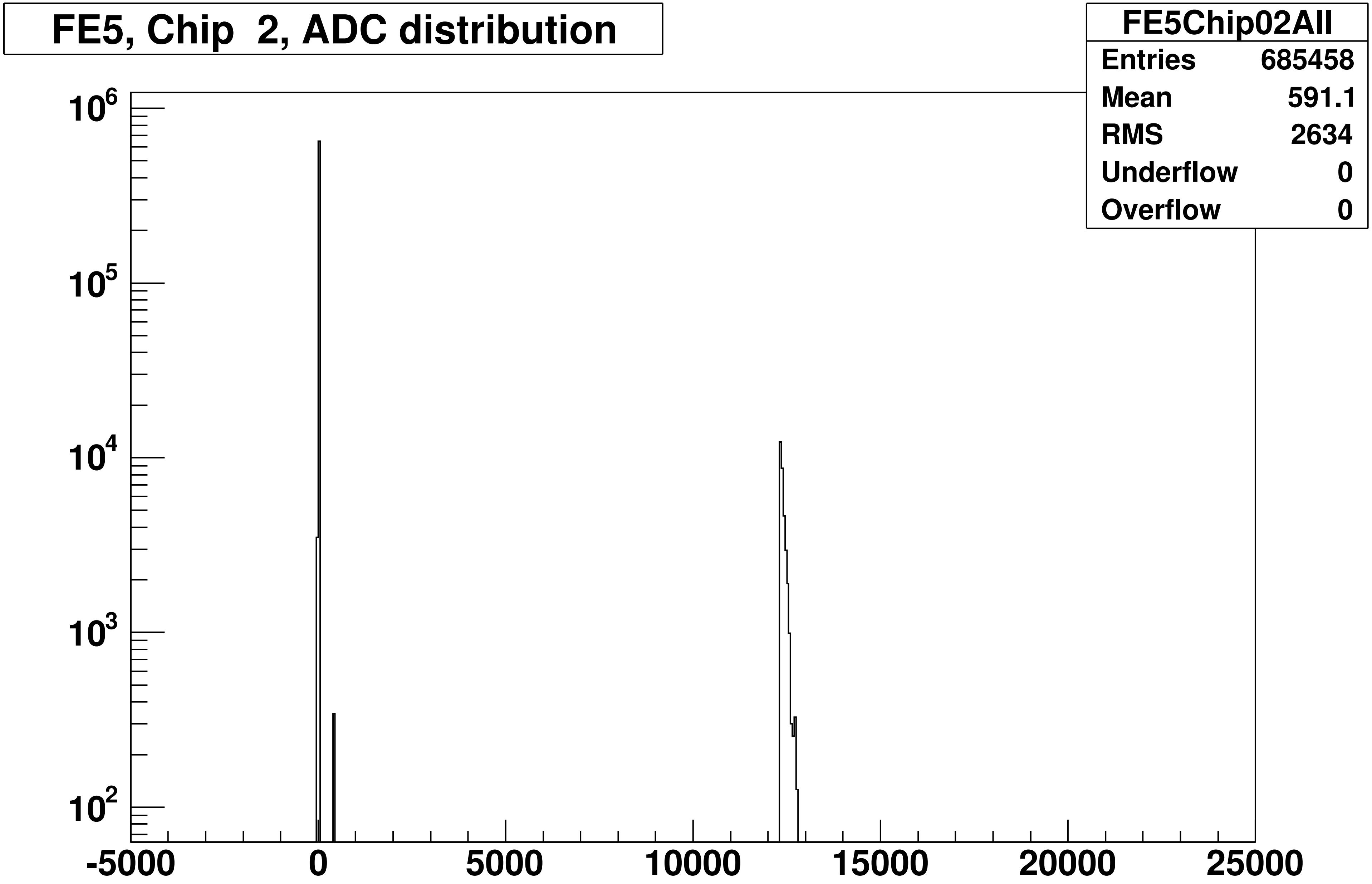
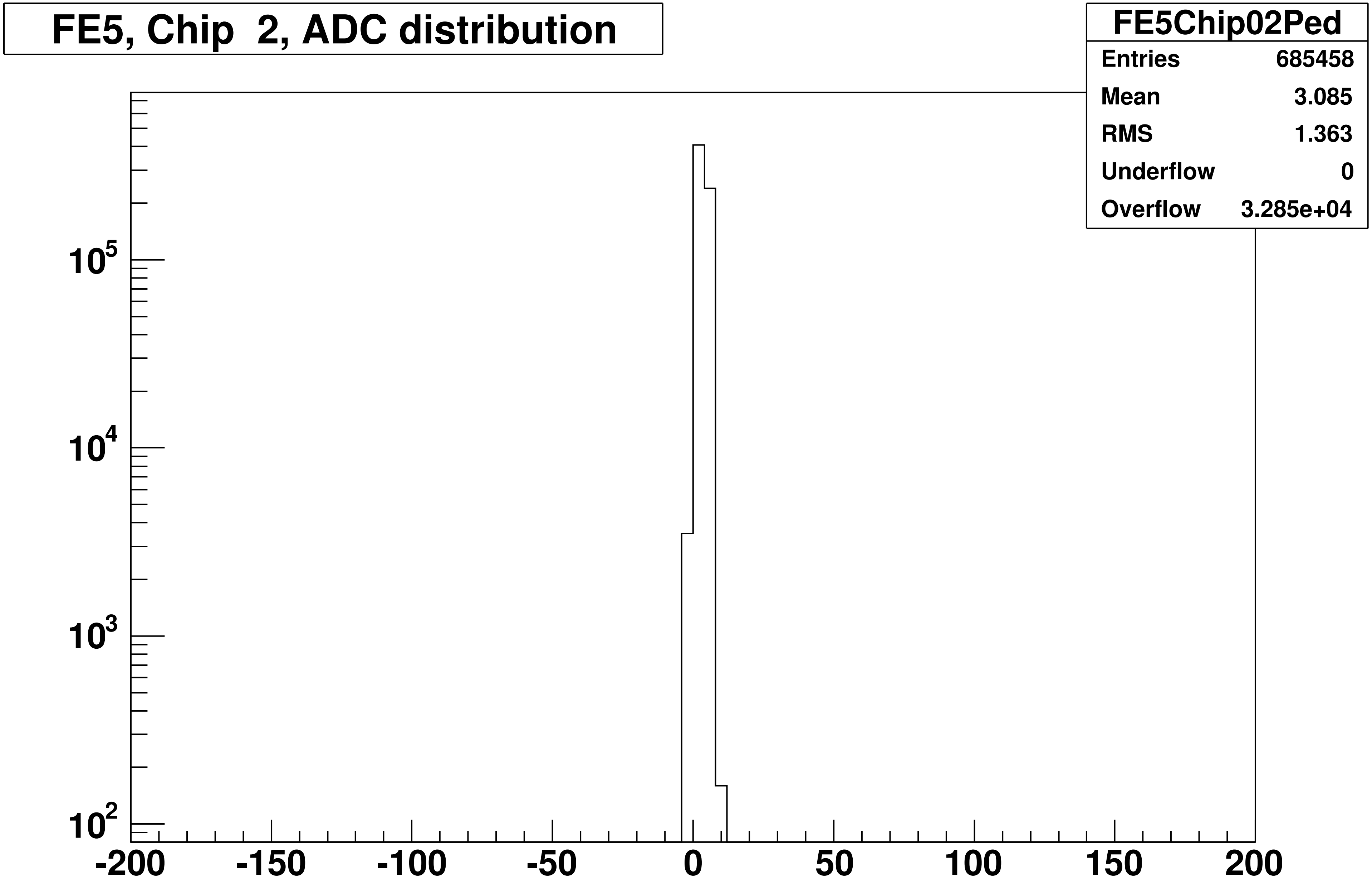
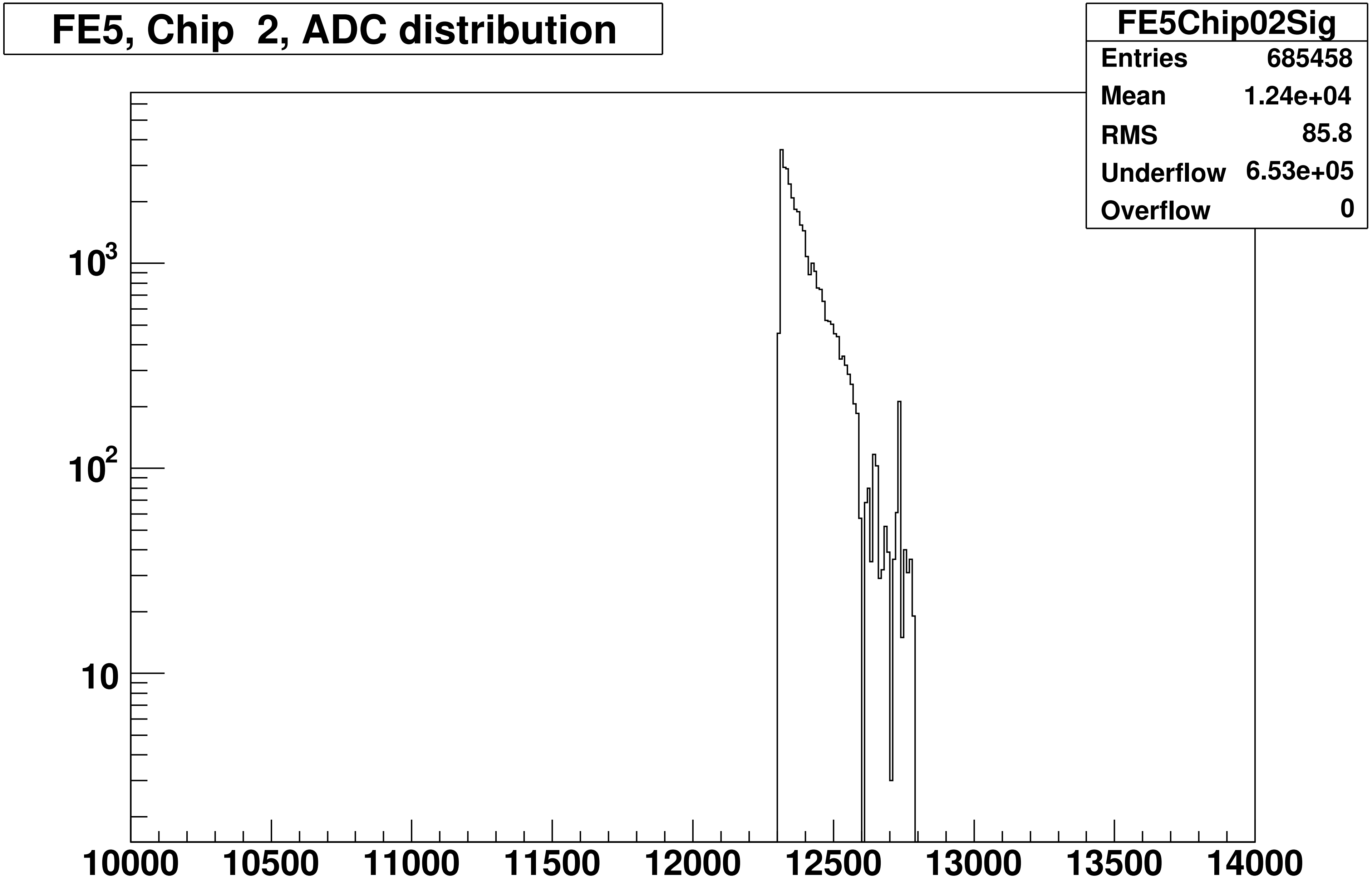
13500
14000


FE5, Chip 2, ADC distribution
FE5Chip02All
Entries 685458
Mean 591.1
RMS 2634
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000



FE5, Chip 2, ADC distribution
FE5Chip02Ped
Entries 685458
Mean 3.085
RMS 1.363
Underflow 0
Overflow 3.285e+04
10^5
10^4
10^3
10^2
-200
-150
-100
-50
0
50
100
150
200


FE5, Chip 2, ADC distribution
FE5Chip02Sig
Entries 685458
Mean 1.24e+04
RMS 85.8
Underflow 6.53e+05
Overflow 0
10^3
10^2
10
10000
10500
11000
11500
12000
12500
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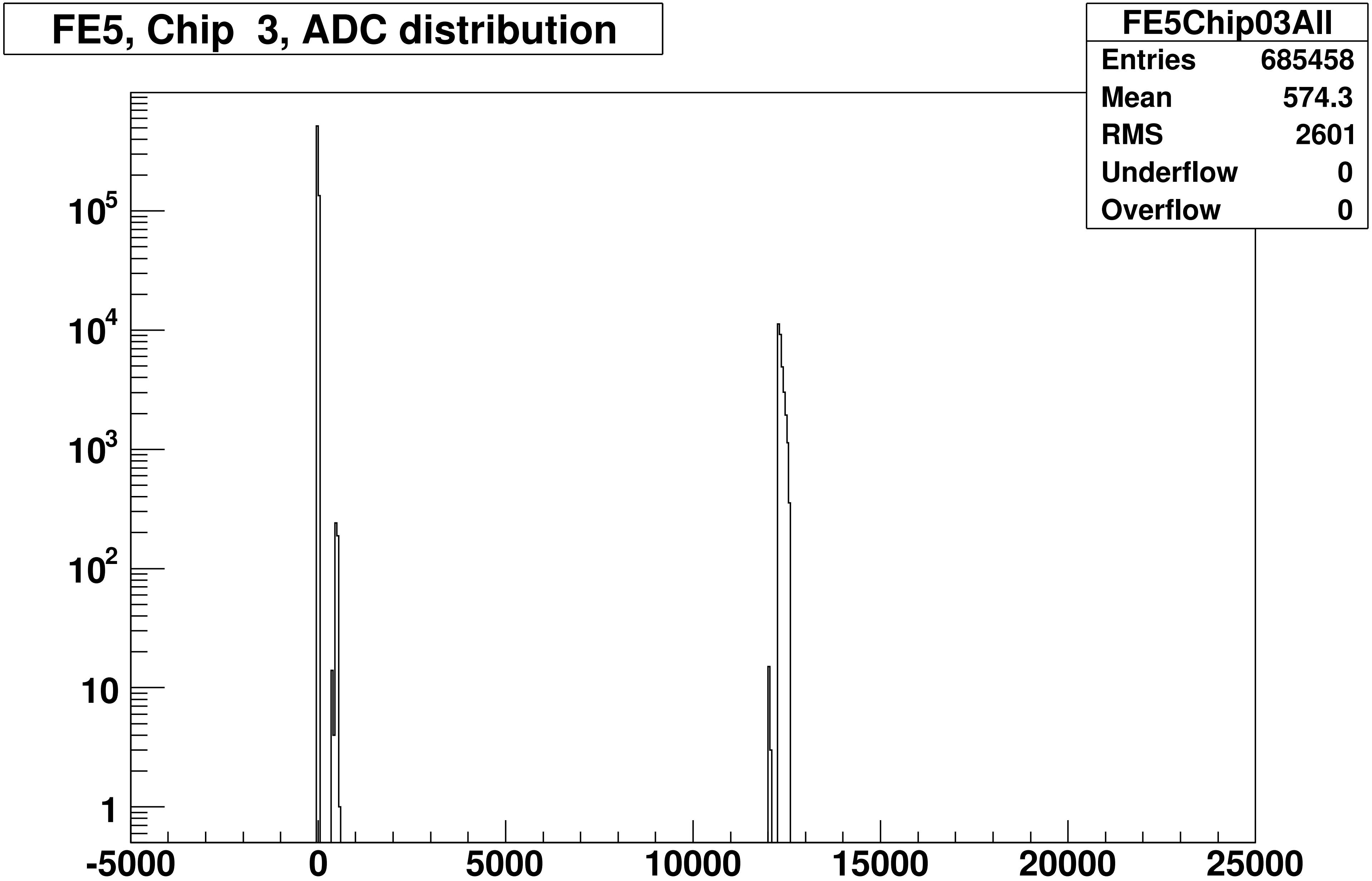
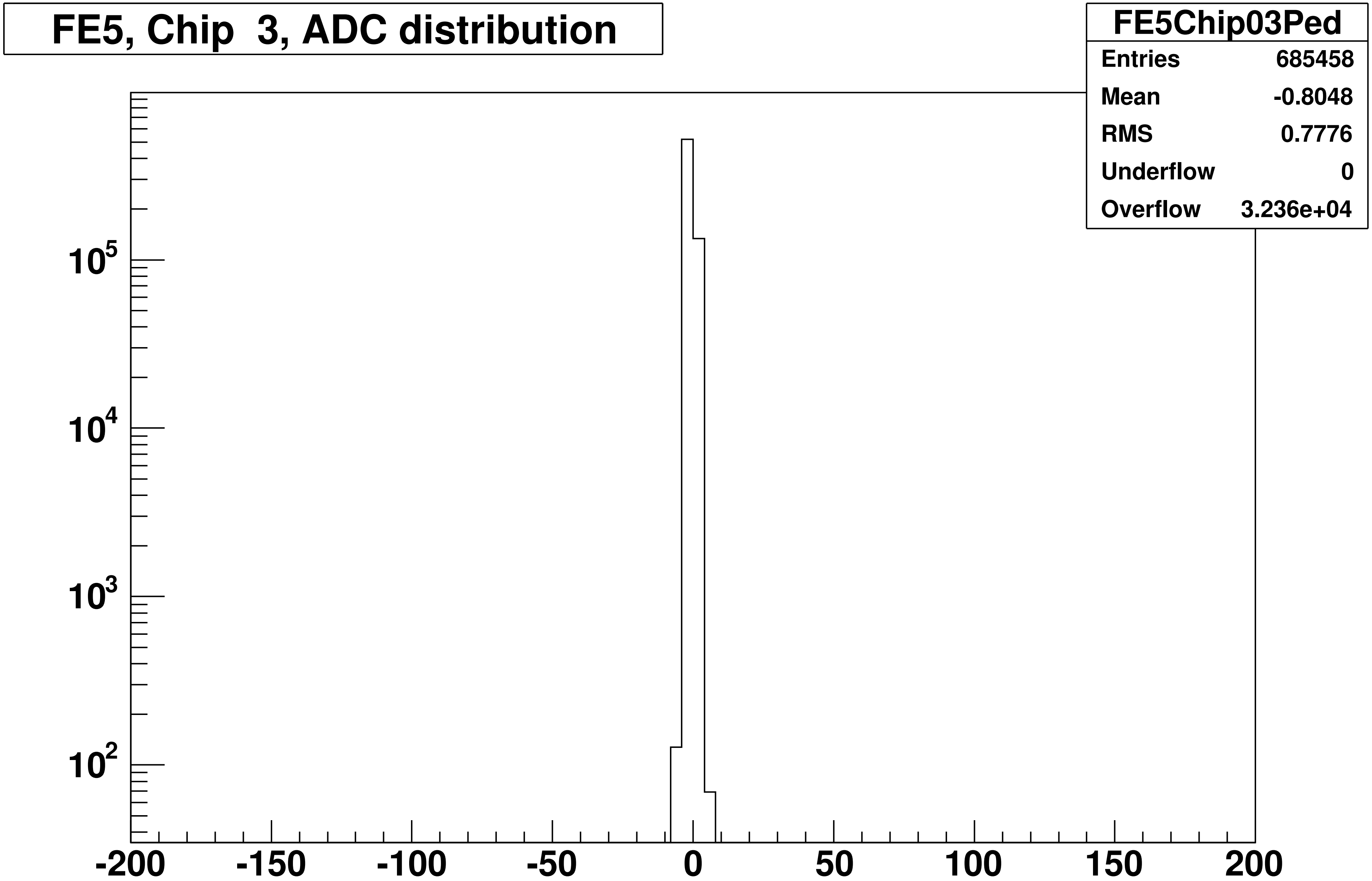
13500
14000


FE5, Chip 3, ADC distribution
FE5Chip03All
Entries 685458
Mean 574.3
RMS 2601
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE5, Chip 3, ADC distribution
FE5Chip03Ped
Entries 685458
Mean -0.8048
RMS 0.7776
Underflow 0
Overflow 3.236e+04
10^5
10^4
10^3
10^2
-200
-150
-100
-50
0
50
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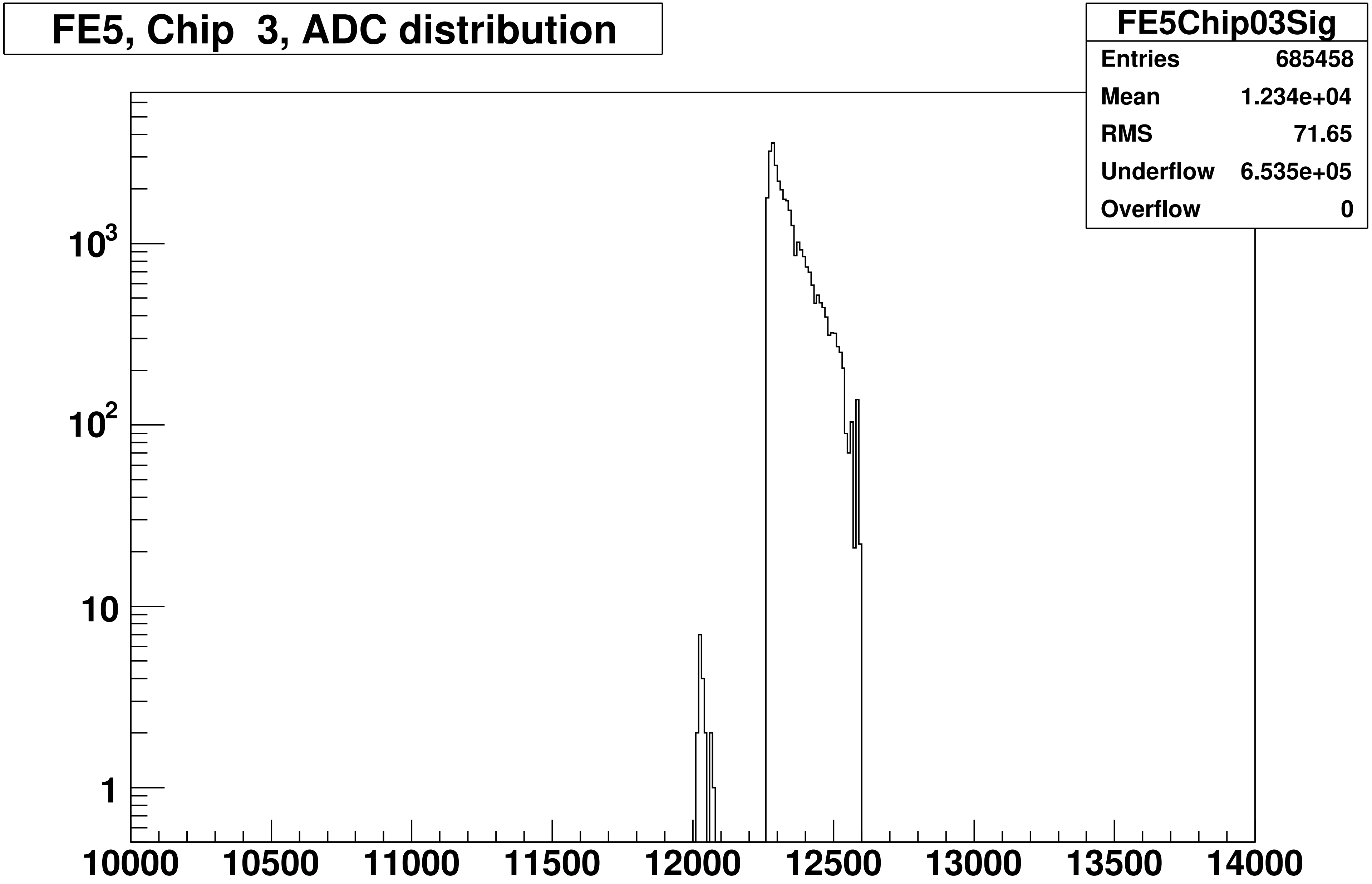
150
200



FE5, Chip 3, ADC distribution
FE5Chip03Sig
Entries 685458
Mean 1.234e+04
RMS 71.65
Underflow 6.535e+05
Overflow 0
10^3
10^2
10
1
10000
10500
11000
11500
12000
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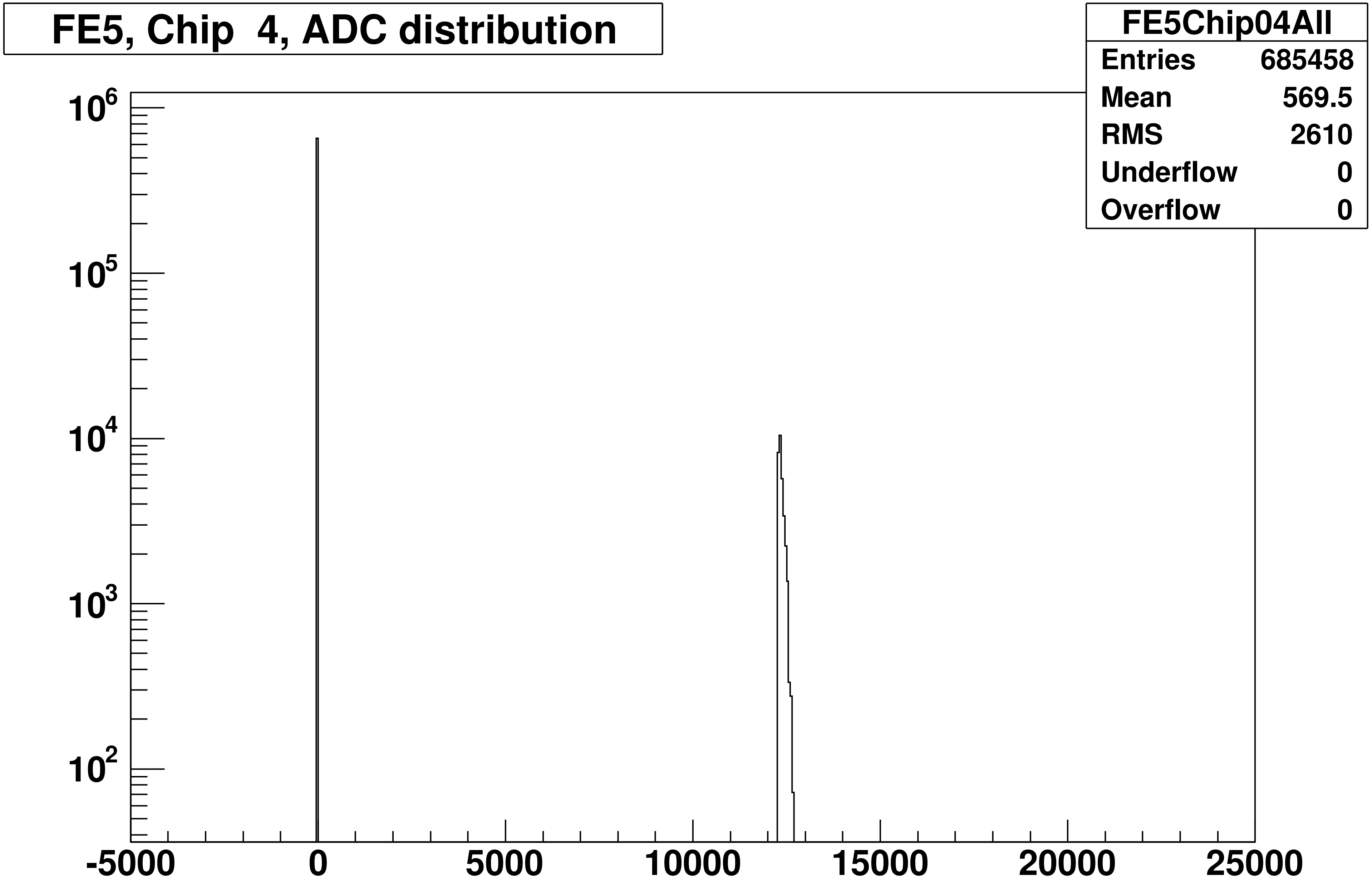
13000
13500
14000


FE5, Chip 4, ADC distribution
FE5Chip04All
Entries 685458
Mean 569.5
RMS 2610
Underflow 0
Overflow 0
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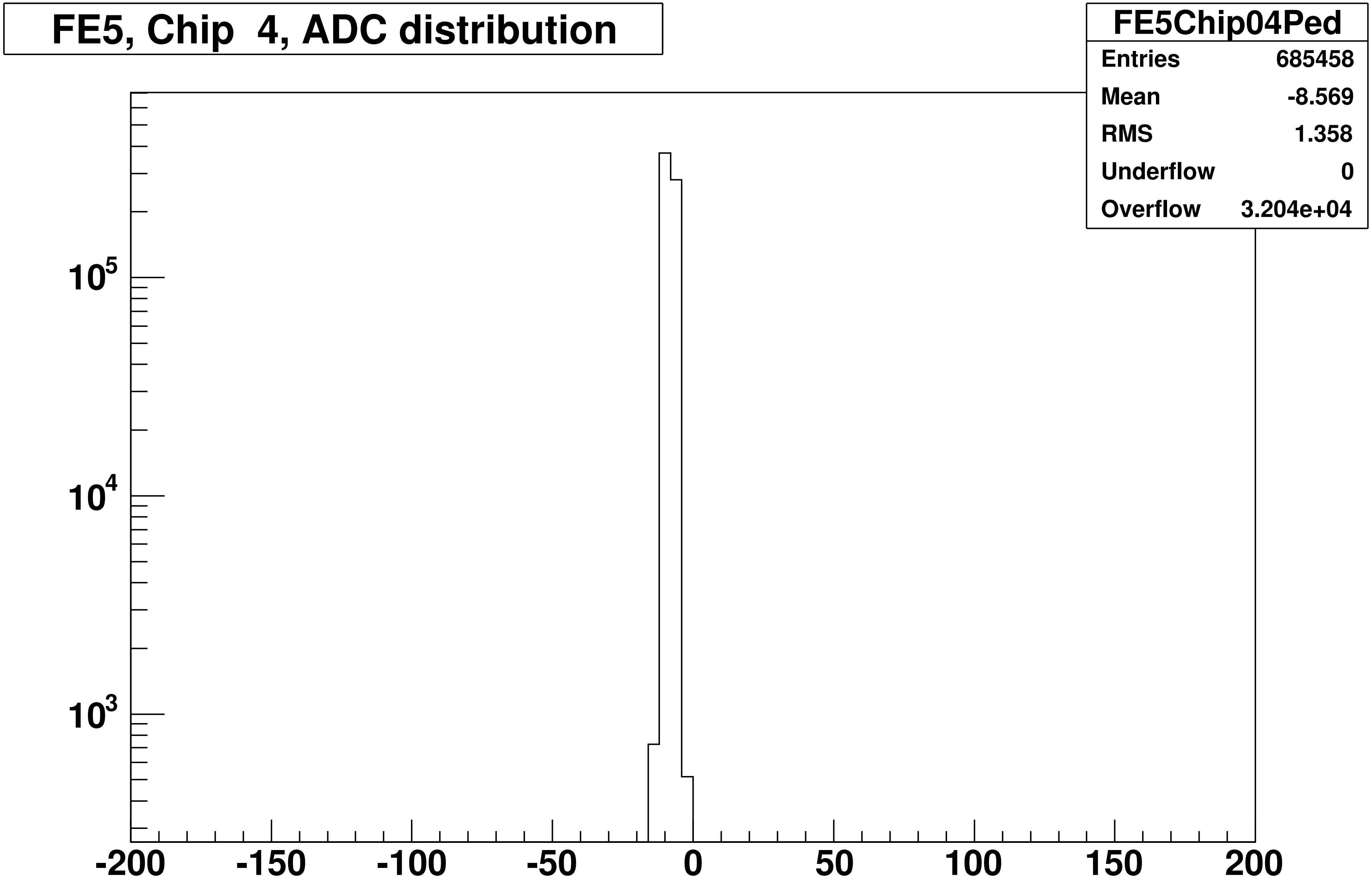
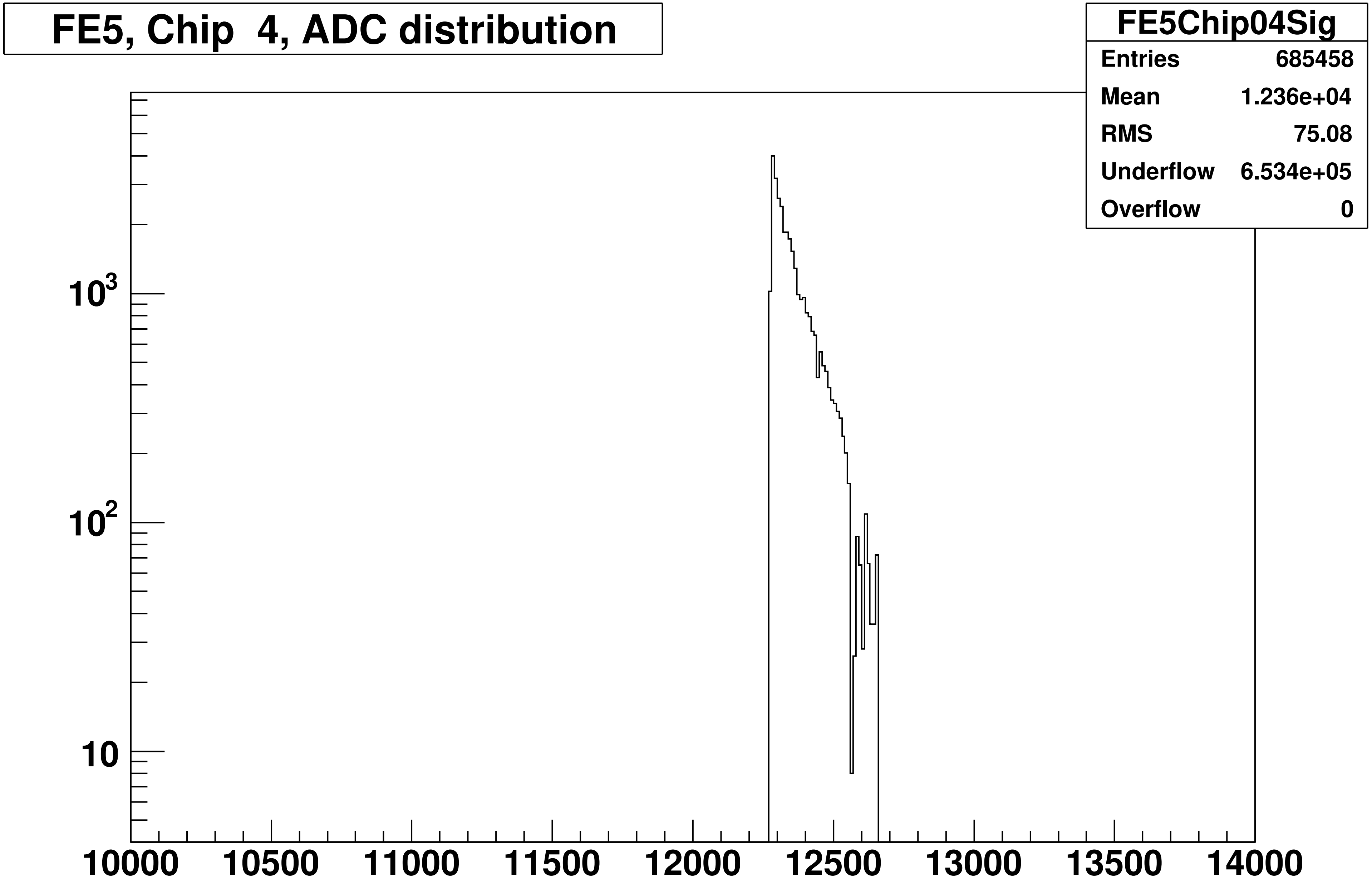
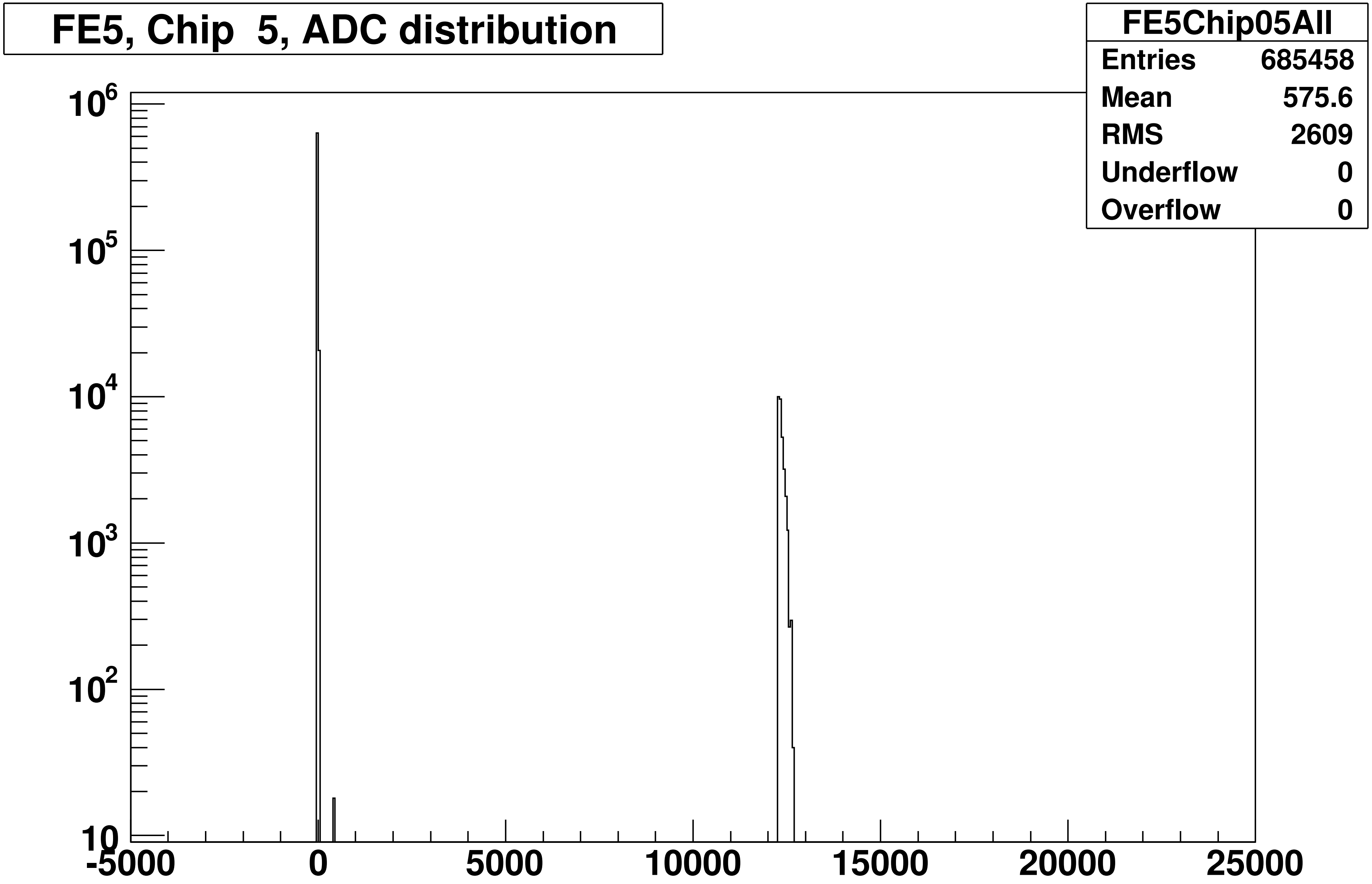
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000


FE5, Chip 4, ADC distribution
FE5Chip04Ped
Entries 685458
Mean -8.569
RMS 1.358
Underflow 0
Overflow 3.204e+04
10^5
10^4
10^3
-200
-150
-100
-50
0
50
100
150
200



FE5, Chip 4, ADC distribution
FE5Chip04Sig
Entries 685458
Mean 1.236e+04
RMS 75.08
Underflow 6.534e+05
Overflow 0
10
10^2
10^3
10000
10500
11000
11500
12000
12500
13000
13500
14000


FE5, Chip 5, ADC distribution
FE5Chip05All
Entries 685458
Mean 575.6
RMS 2609
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
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-5000
0
5000
10000
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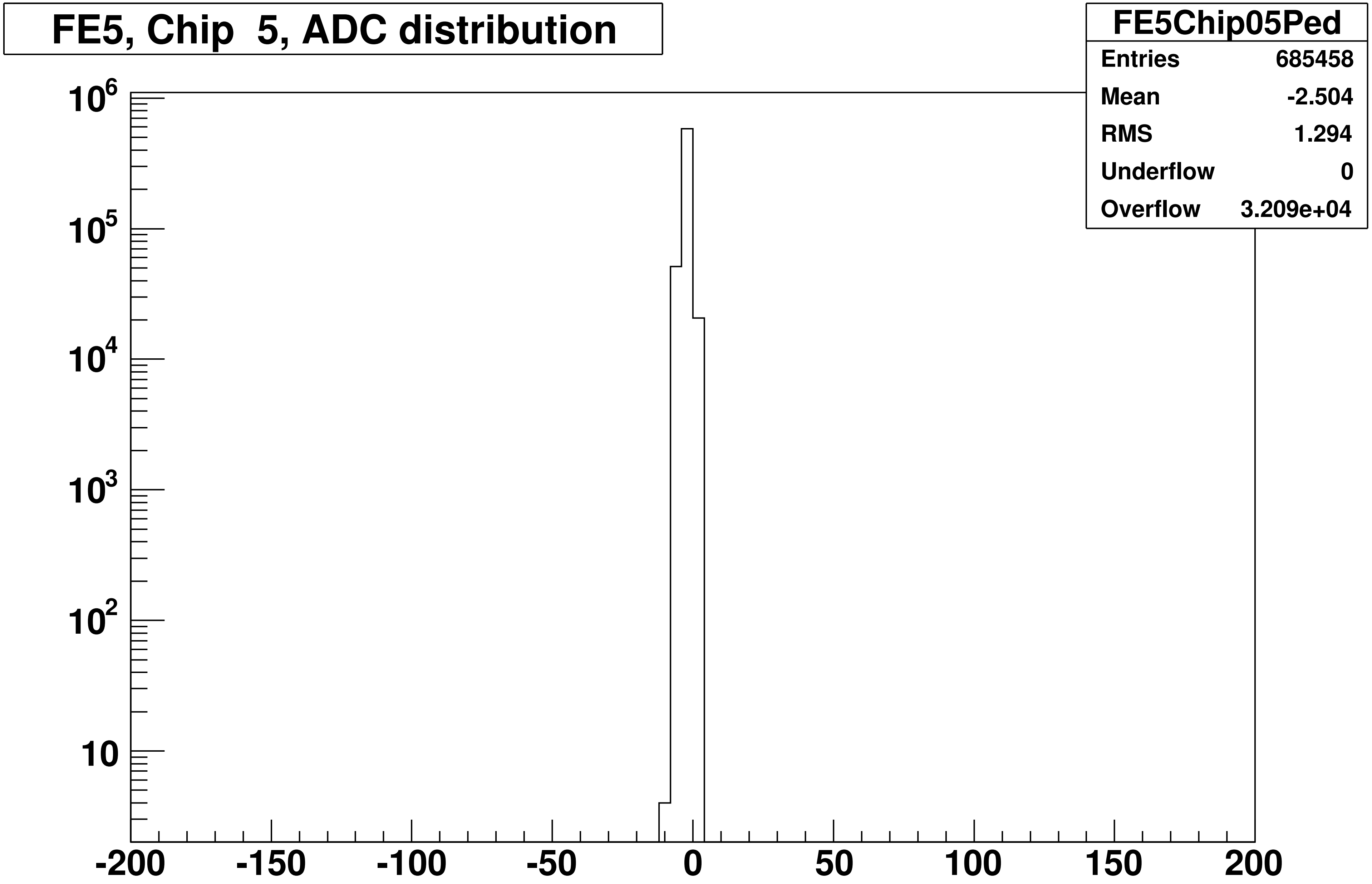
20000
25000


FE5, Chip 5, ADC distribution
FE5Chip05Ped
Entries 685458
Mean -2.504
RMS 1.294
Underflow 0
Overflow 3.209e+04
10^6
10^5
10^4
10^3
10^2
10
-200
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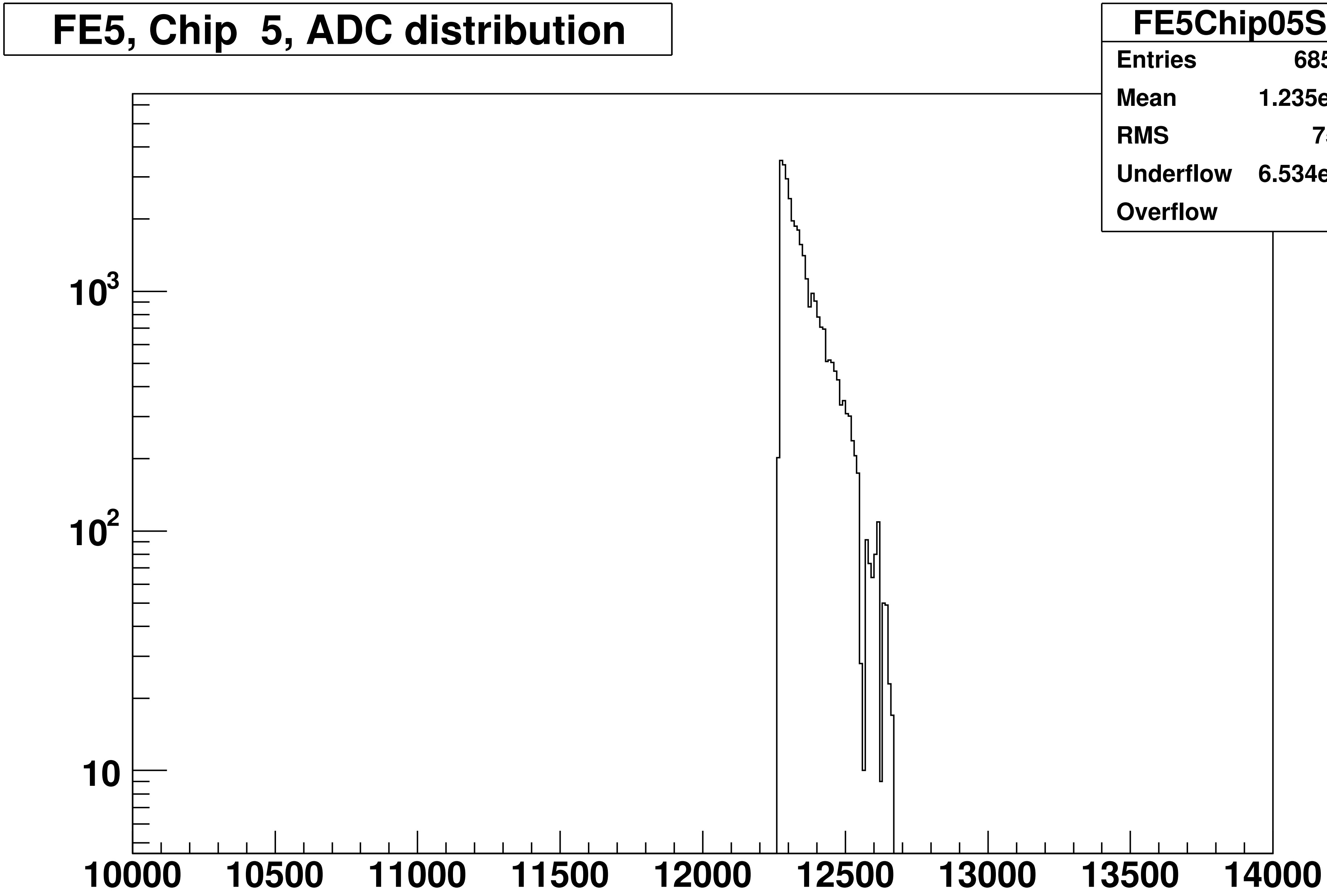
-100
-50
0
50
100
150
200



FE5, Chip 5, ADC distribution
FE5Chip05Sig
Entries 685458
Mean 1.235e+04
RMS 75.46
Underflow 6.534e+05
Overflow 0
10^3
10^2
10
10000
10500
11000
11500
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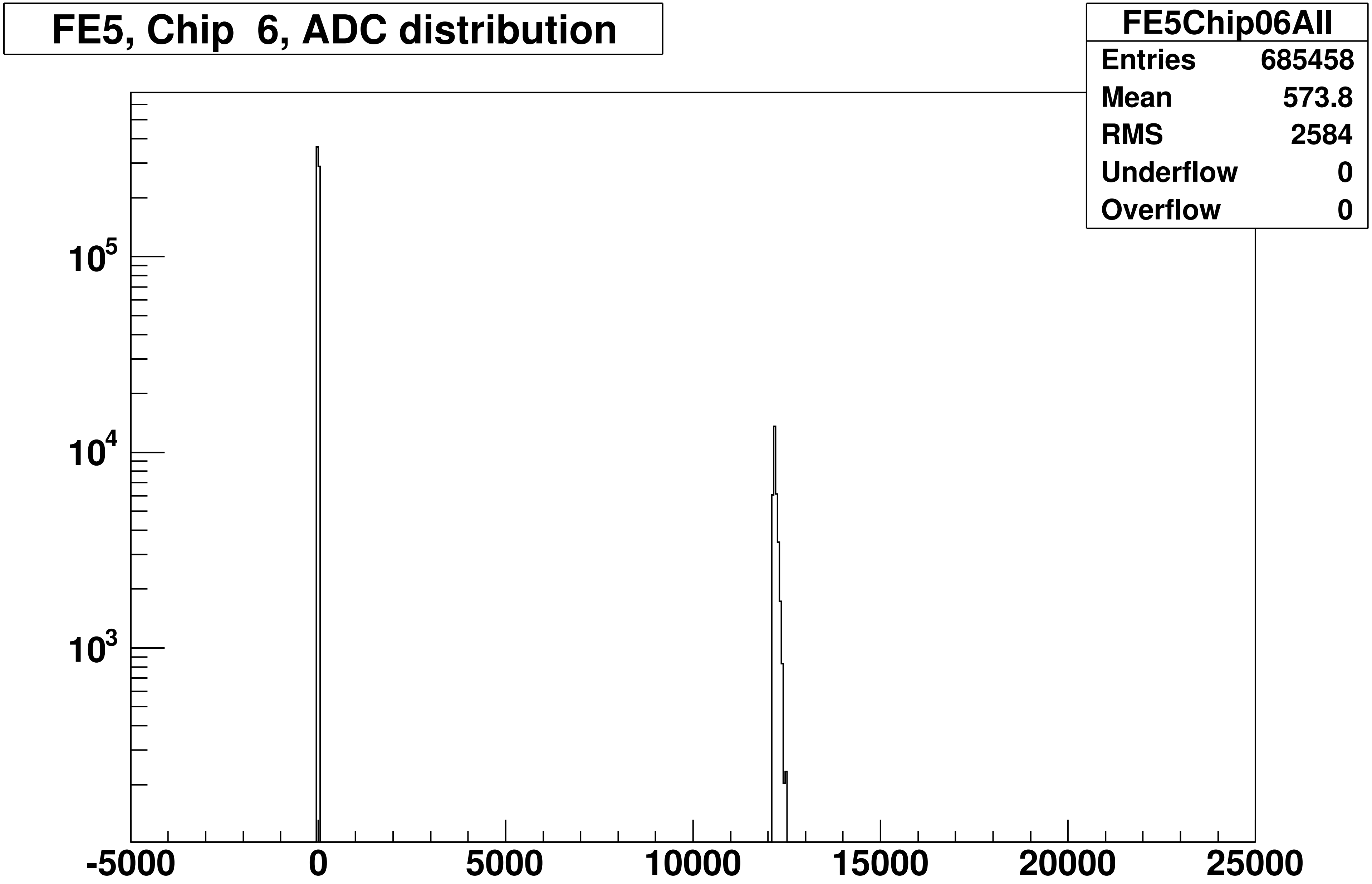
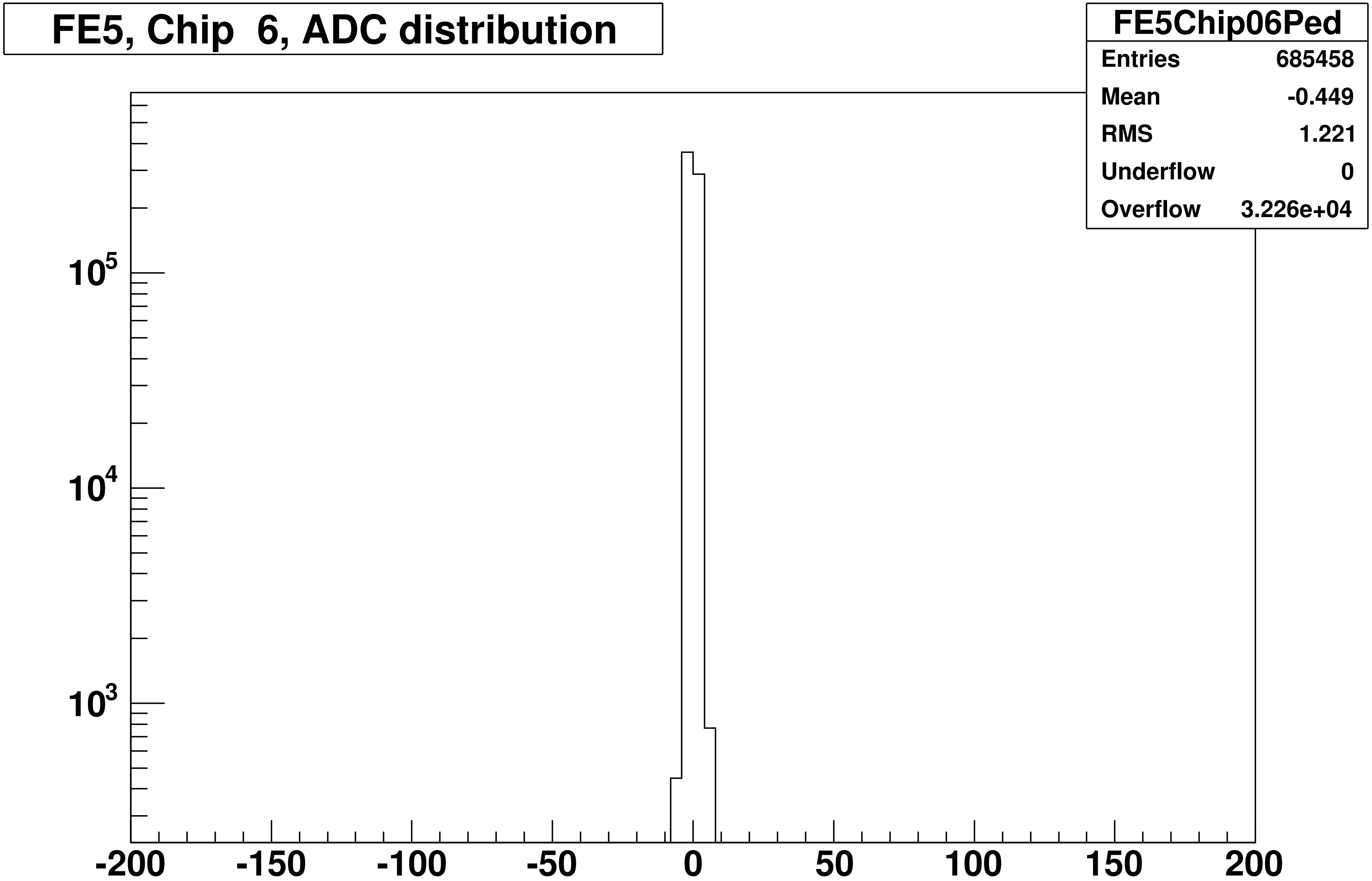
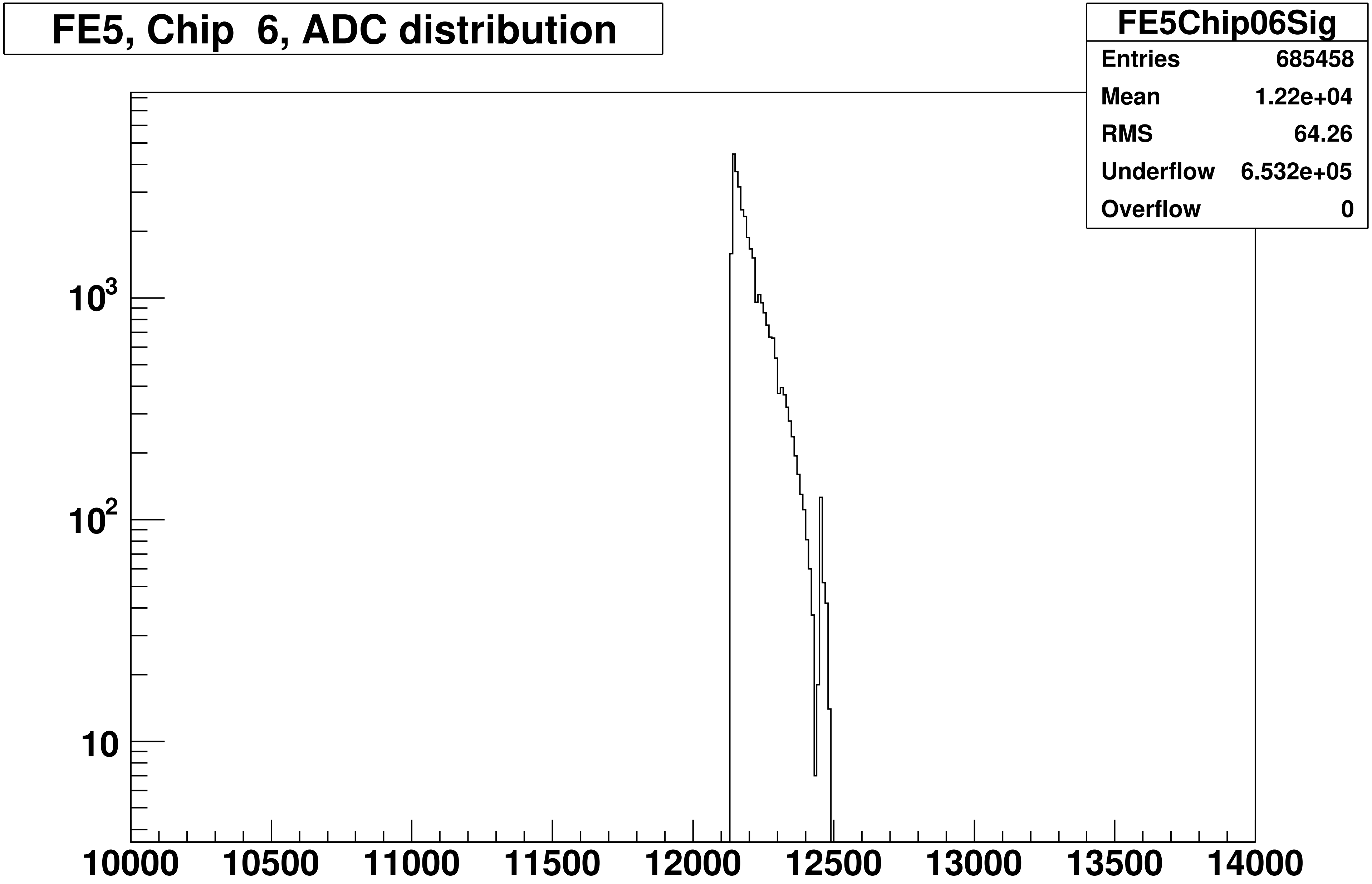


FE5, Chip 6, ADC distribution
FE5Chip06All
Entries 685458
Mean 573.8
RMS 2584
Underflow 0
Overflow 0
10^5
10^4
10^3
-5000
0
5000
10000
15000
20000
25000



FE5, Chip 6, ADC distribution
FE5Chip06Ped
Entries 685458
Mean -0.449
RMS 1.221
Underflow 0
Overflow 3.226e+04
10^5
10^4
10^3
-200
-150
-100
-50
0
50
100
150
200



FE5, Chip 6, ADC distribution
FE5Chip06Sig
Entries 685458
Mean 1.22e+04
RMS 64.26
Underflow 6.532e+05
Overflow 0
10^3
10^2
10
10000
10500
11000
11500
12000
12500
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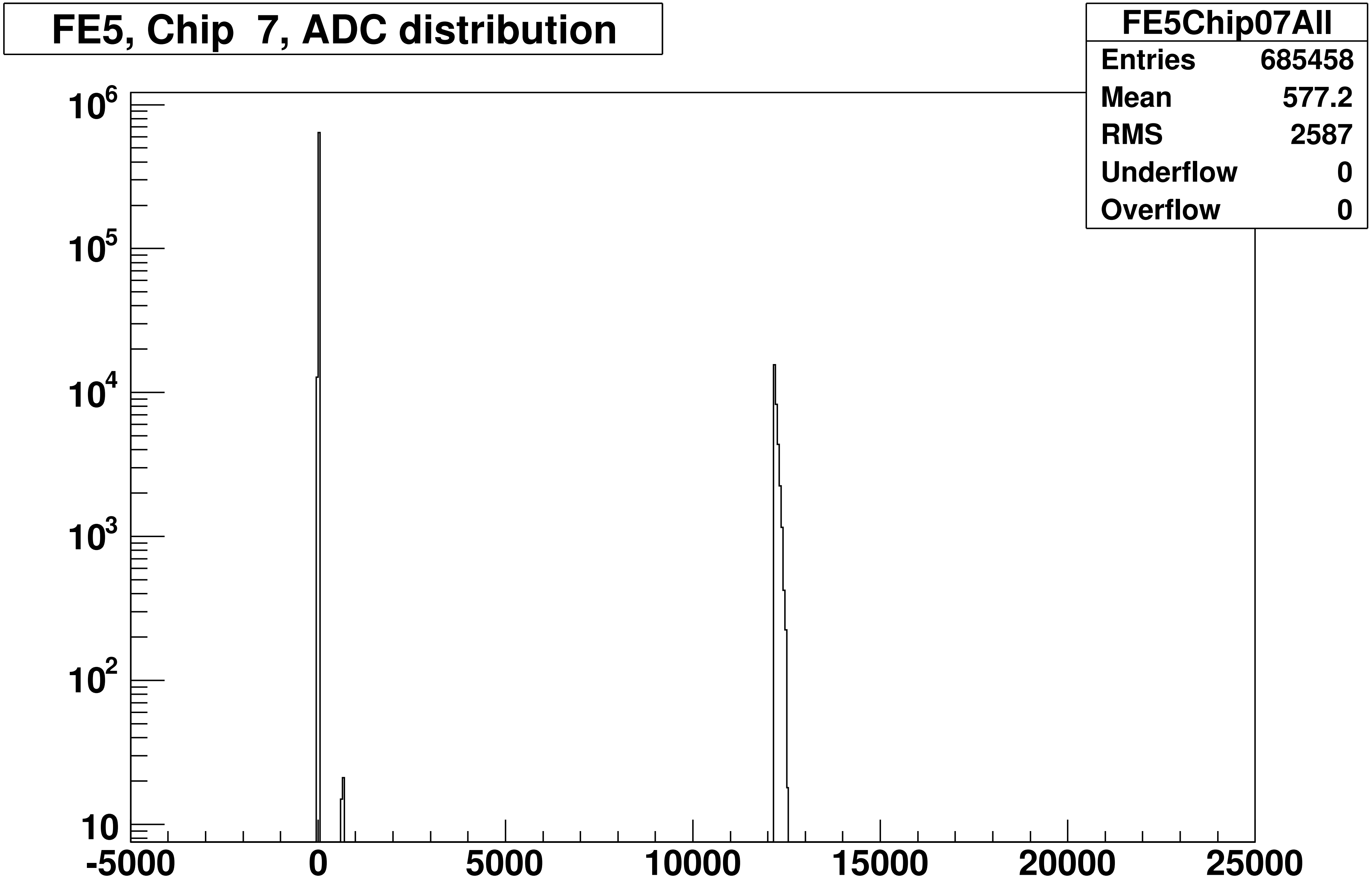
14000


FE5, Chip 7, ADC distribution
FE5Chip07All
Entries 685458
Mean 577.2
RMS 2587
Underflow 0
Overflow 0
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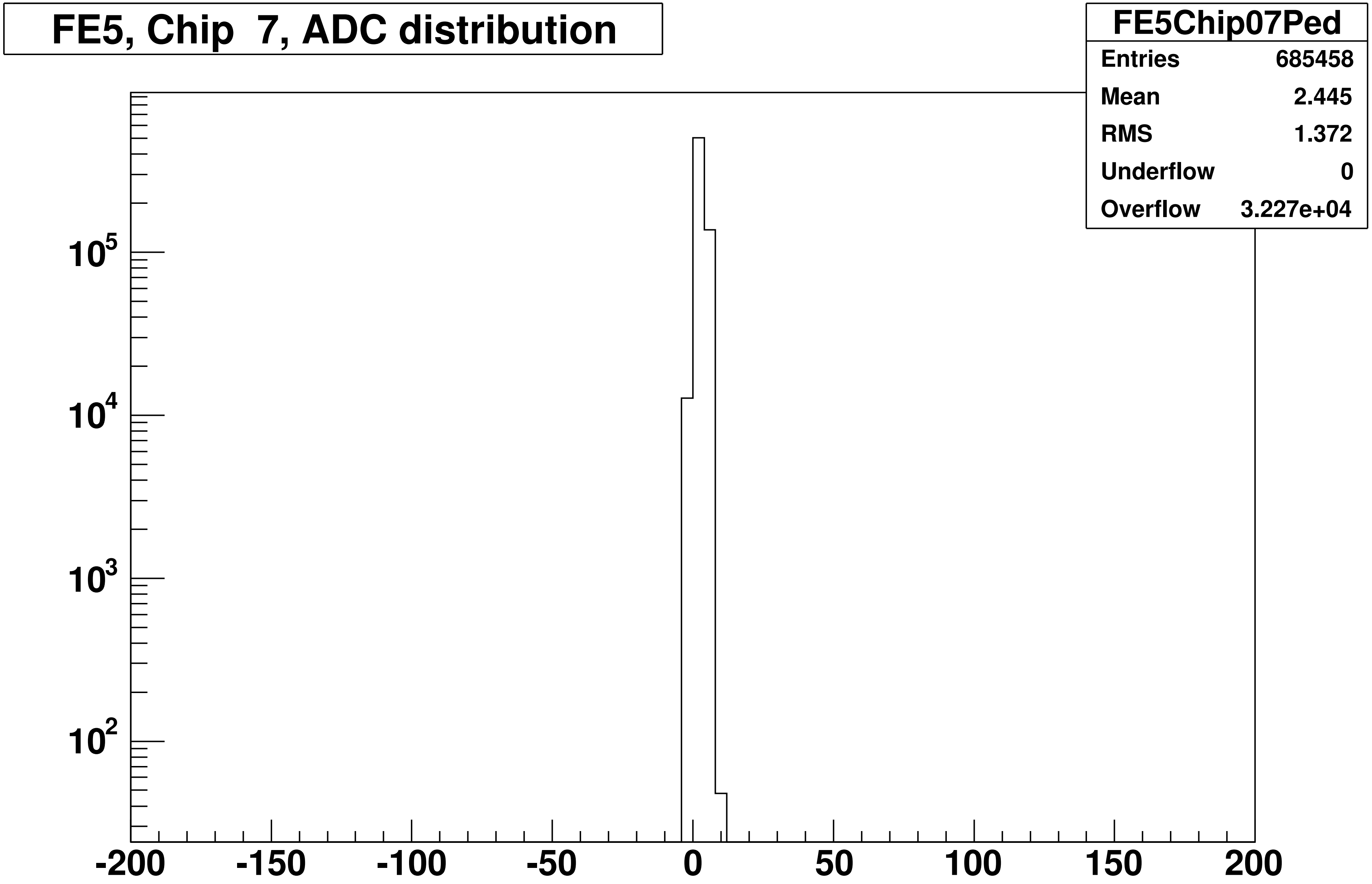
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000



FE5, Chip 7, ADC distribution
FE5Chip07Ped
Entries 685458
Mean 2.445
RMS 1.372
Underflow 0
Overflow 3.227e+04
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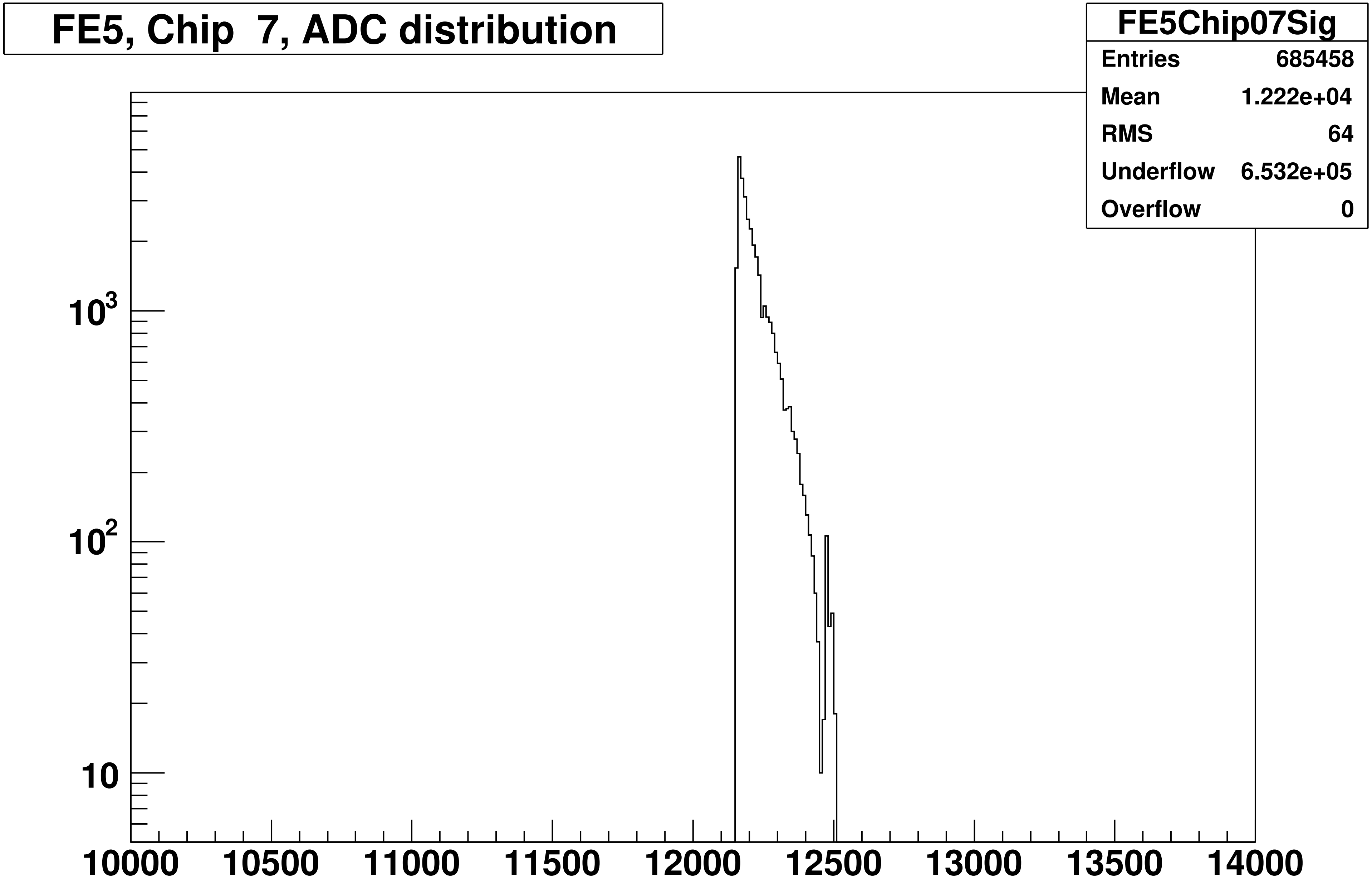
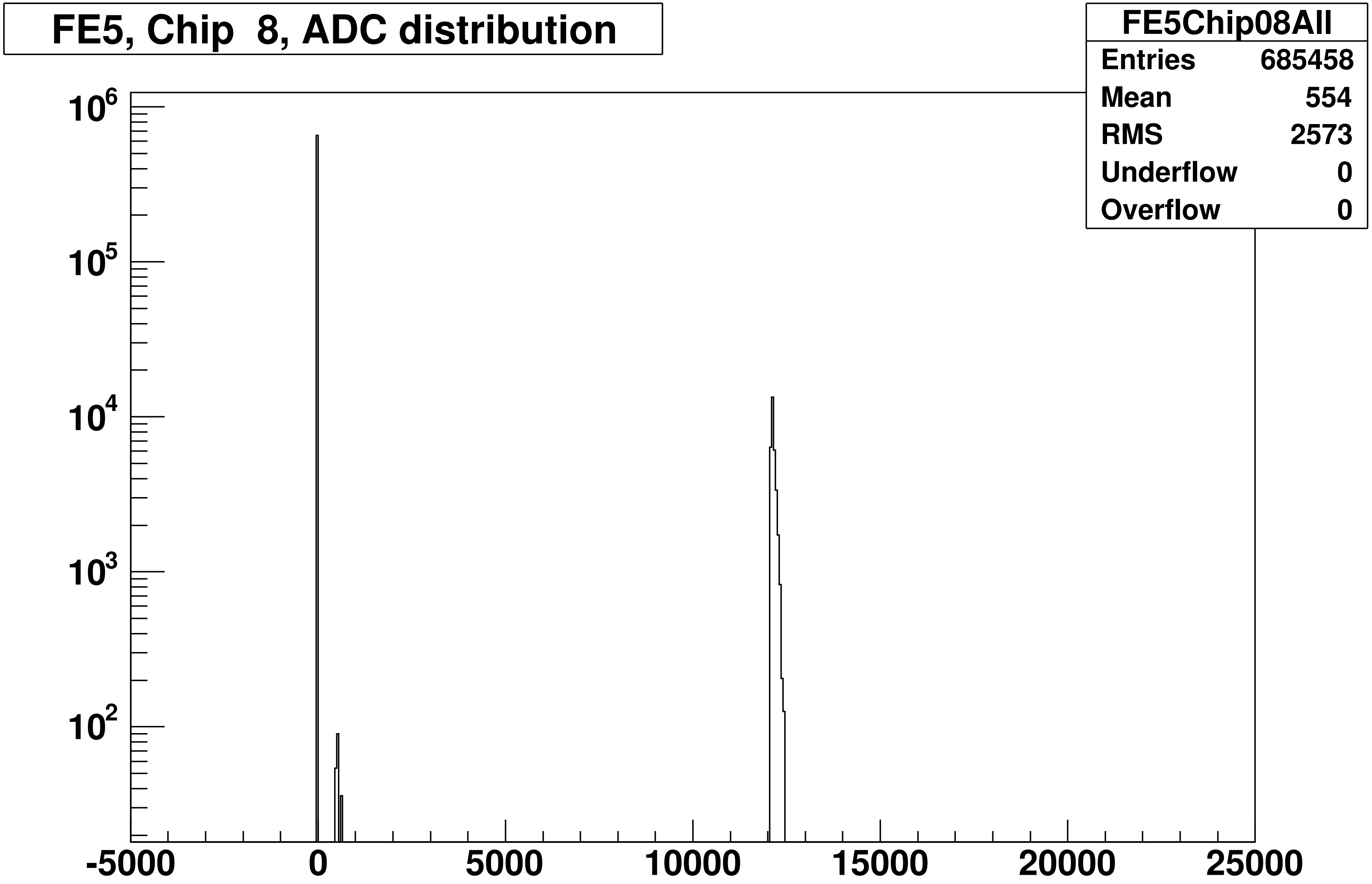
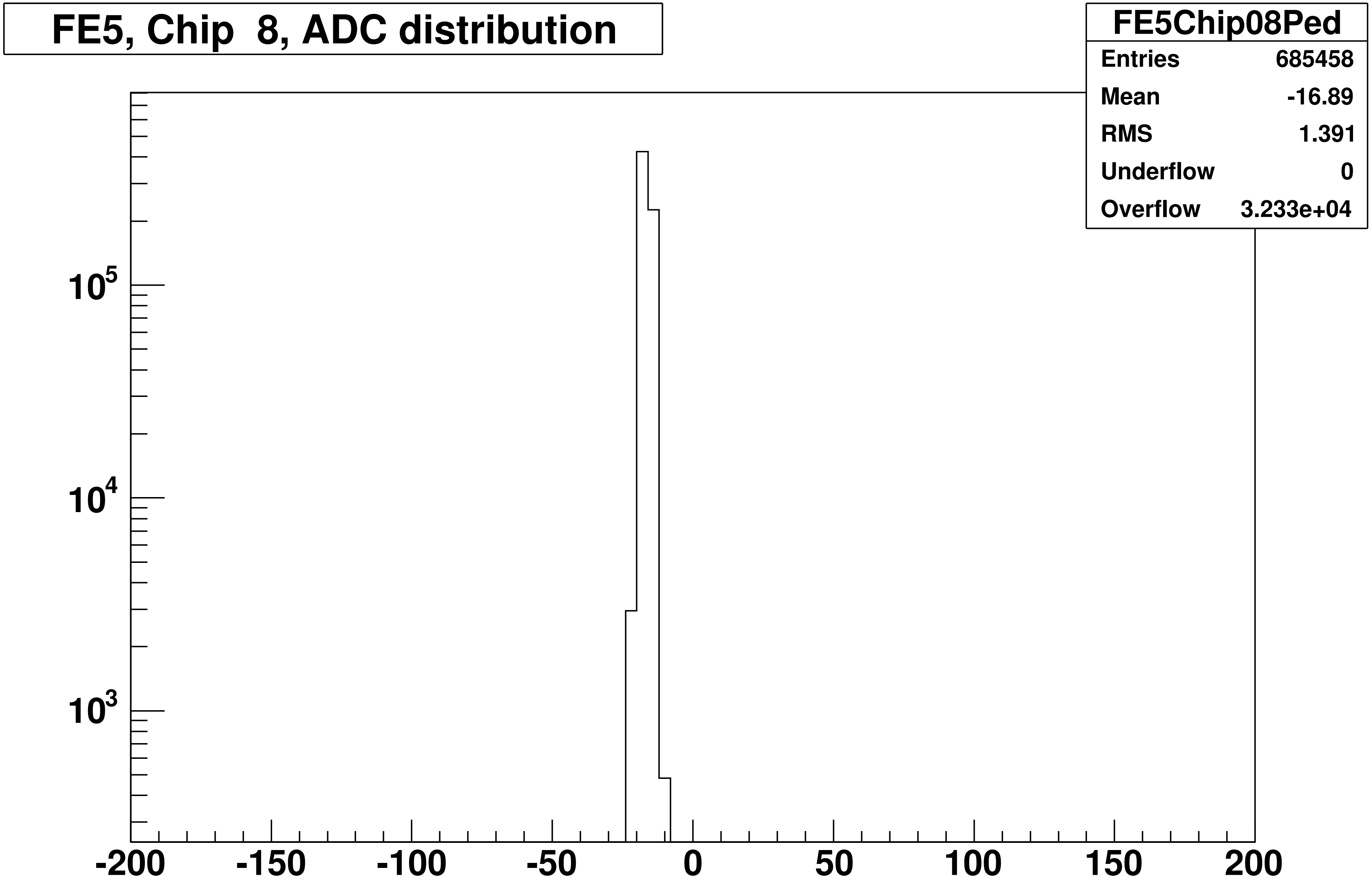
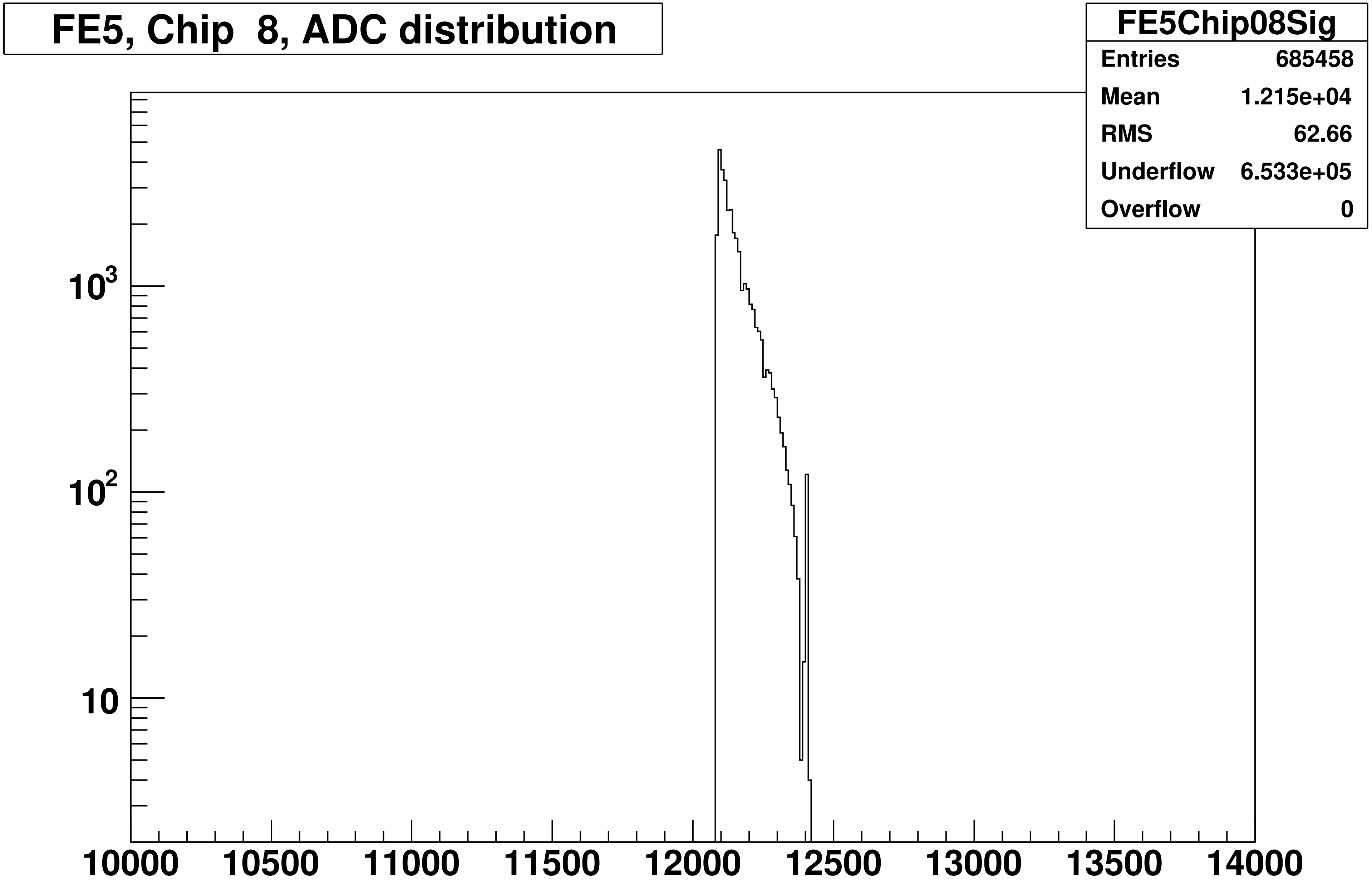
10^4
10^3
10^2
-200
-150
-100
-50
0
50
100
150
200



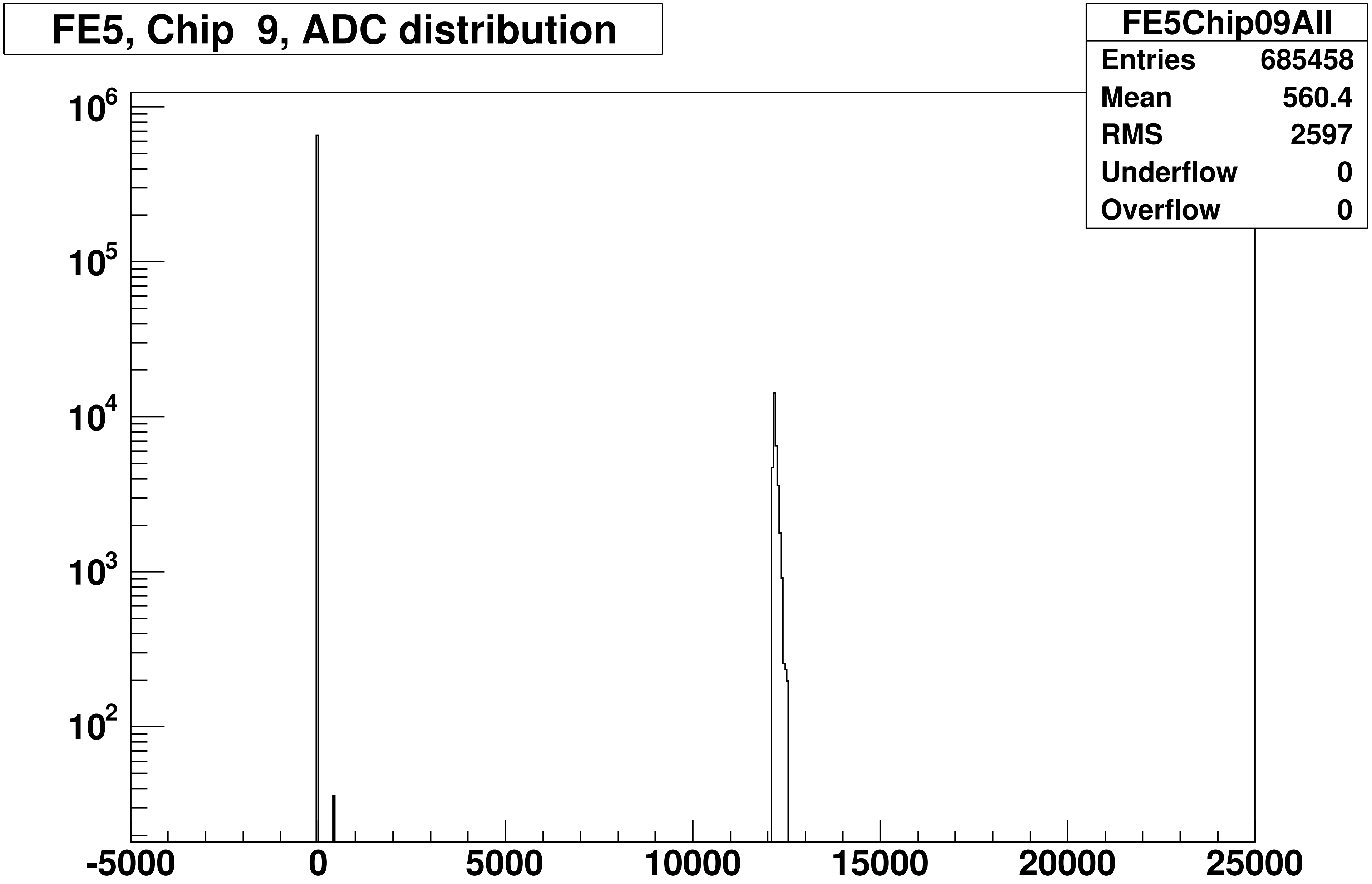
FE5, Chip 7, ADC distribution
FE5Chip07Sig
Entries 685458
Mean 1.222e+04
RMS 64
Underflow 6.532e+05
Overflow 0
10^3
10^2
10
10000
10500
11000
11500
12000
12500
13000
13500
14000

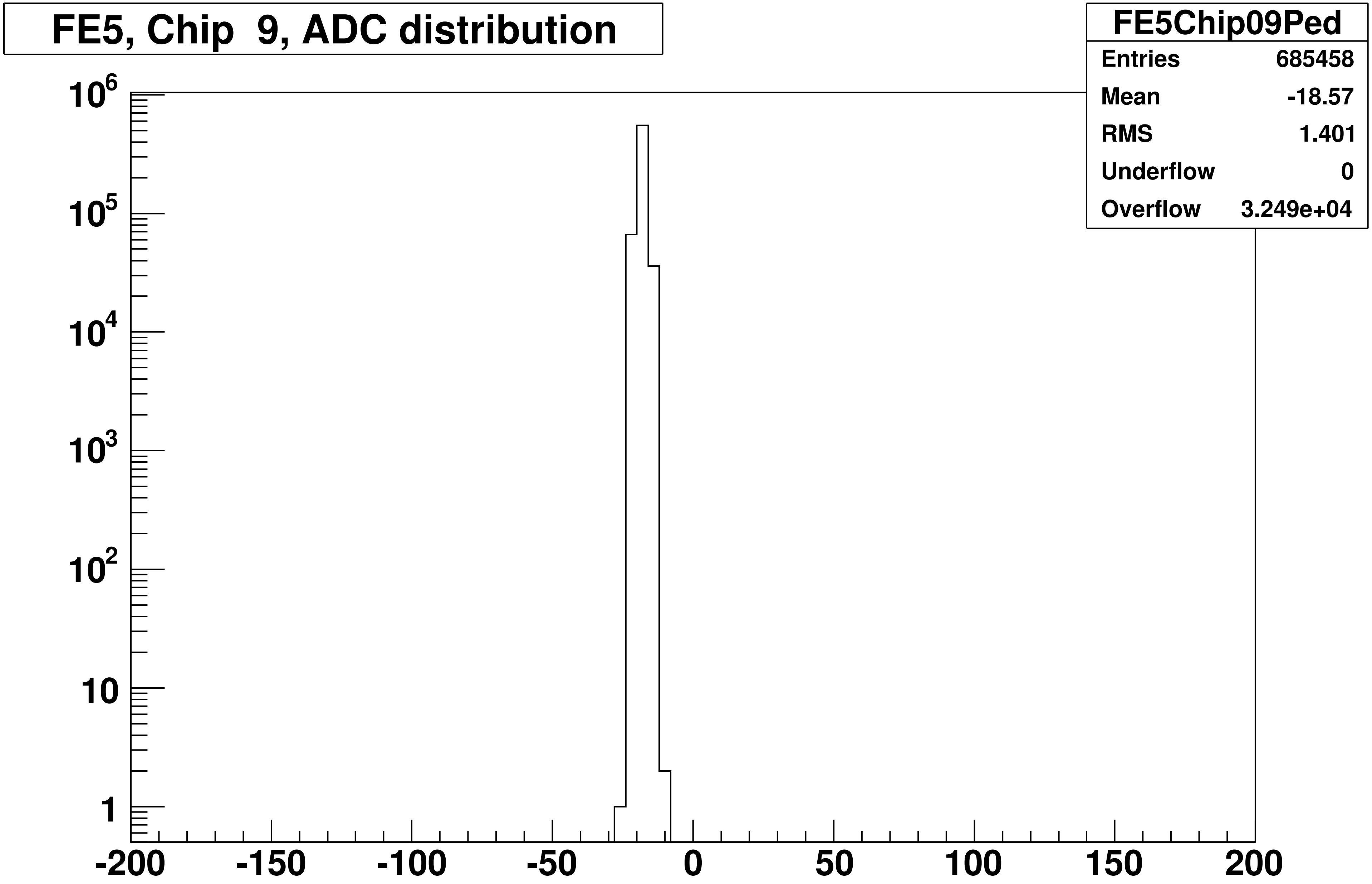

FE5, Chip 8, ADC distribution
FE5Chip08All
Entries 685458
Mean 554
RMS 2573
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000


FE5, Chip 8, ADC distribution
FE5Chip08Ped
Entries 685458
Mean -16.89
RMS 1.391
Underflow 0
Overflow 3.233e+04
10^5
10^4
10^3
-200 -150 -100 -50 0 50 100 150 200



FE5, Chip 8, ADC distribution
FE5Chip08Sig
Entries 685458
Mean 1.215e+04
RMS 62.66
Underflow 6.533e+05
Overflow 0
10^3
10^2
10
10000
10500
11000
11500
12000
12500
13000
13500
14000


FE5, Chip 9, ADC distribution
FE5Chip09All
Entries 685458
Mean 560.4
RMS 2597
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000


FE5, Chip 9, ADC distribution
FE5Chip09Ped
Entries 685458
Mean -18.57
RMS 1.401
Underflow 0
Overflow 3.249e+04
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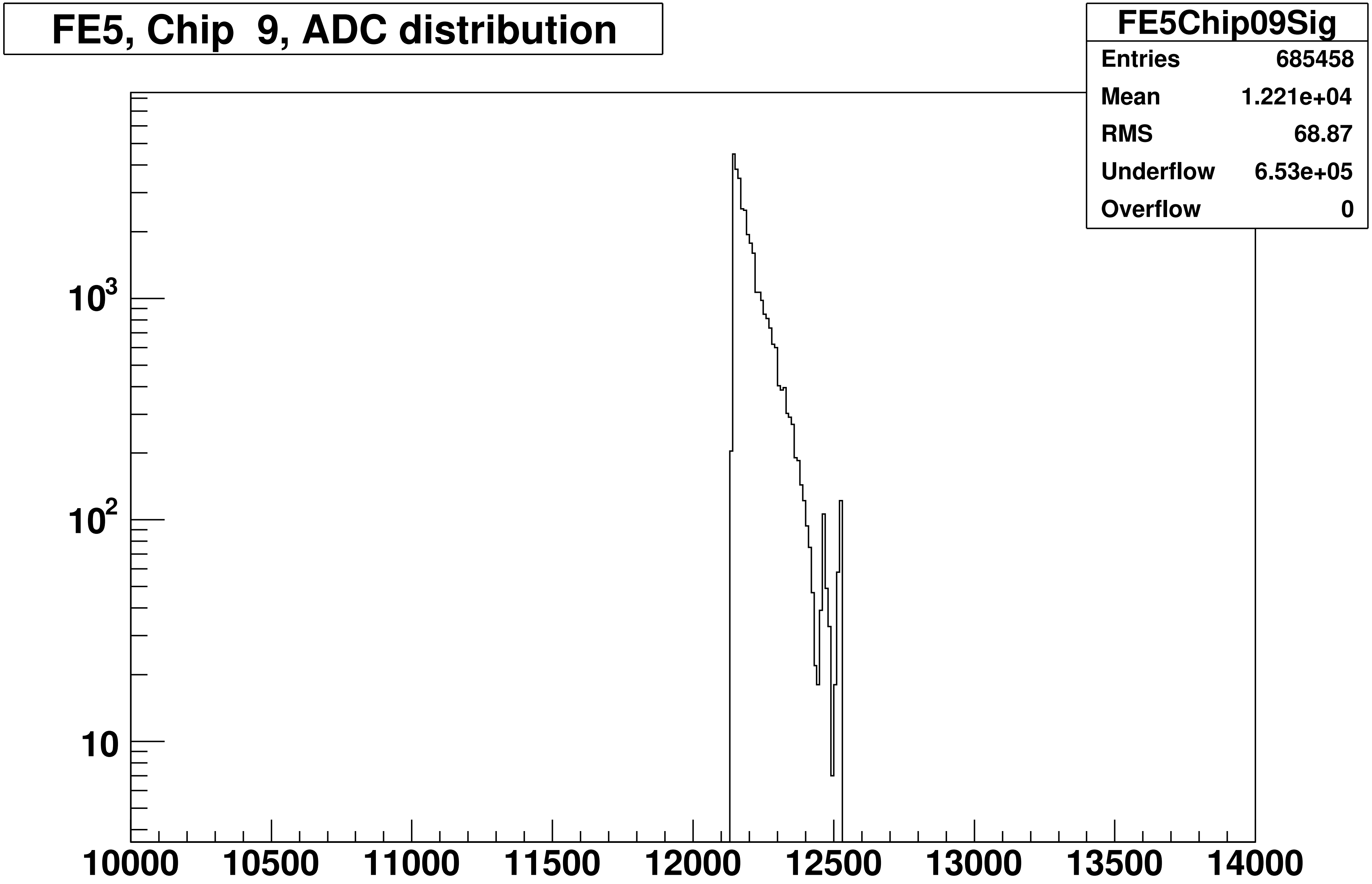
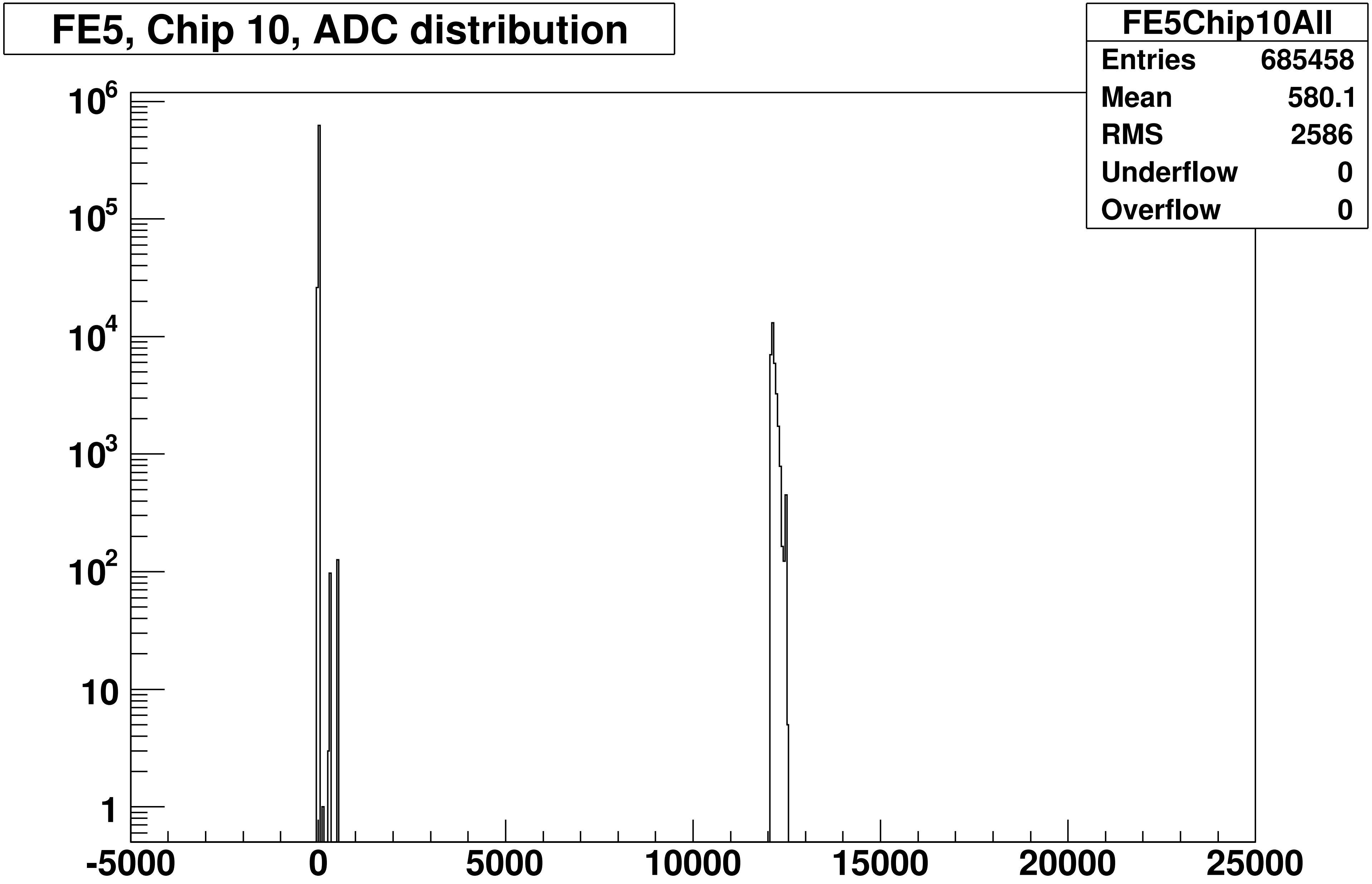
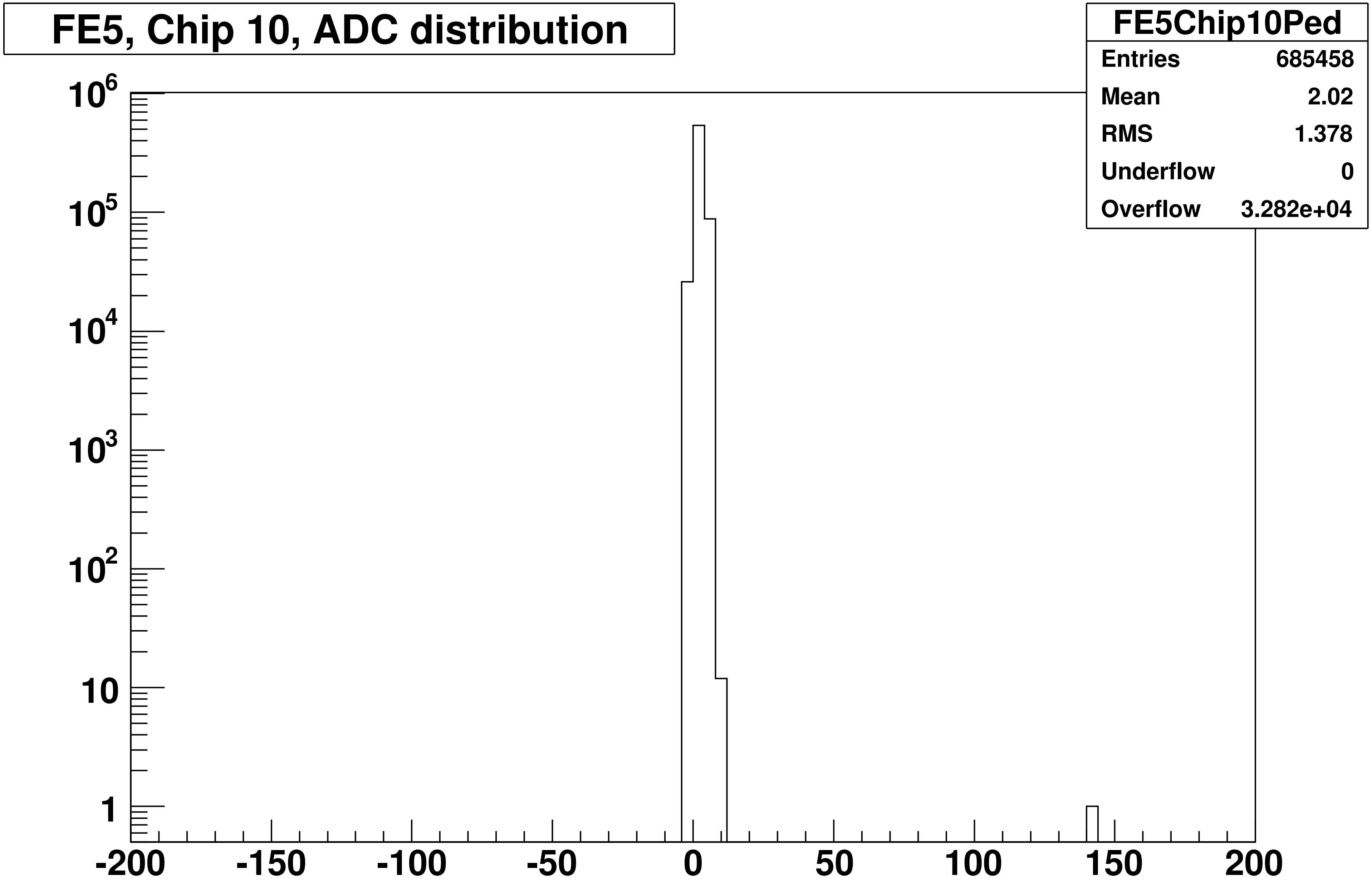
10^5
10^4
10^3
10^2
10
1
-200 -150 -100 -50 0 50 100 150 200

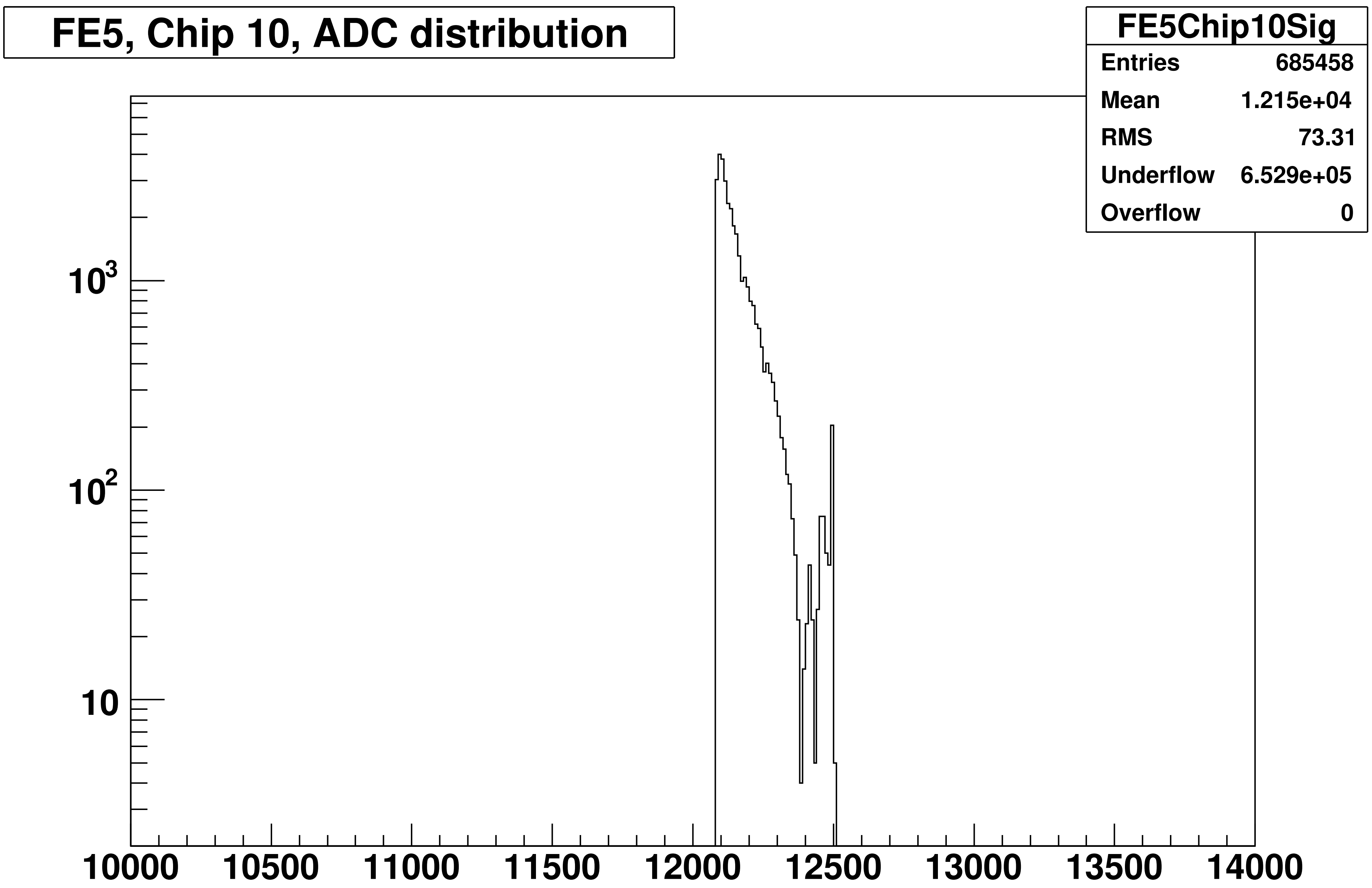


FE5, Chip 9, ADC distribution
FE5Chip09Sig
Entries 685458
Mean 1.221e+04
RMS 68.87
Underflow 6.53e+05
Overflow 0
10^3
10^2
10
10000
10500
11000
11500
12000
12500
13000
13500
14000

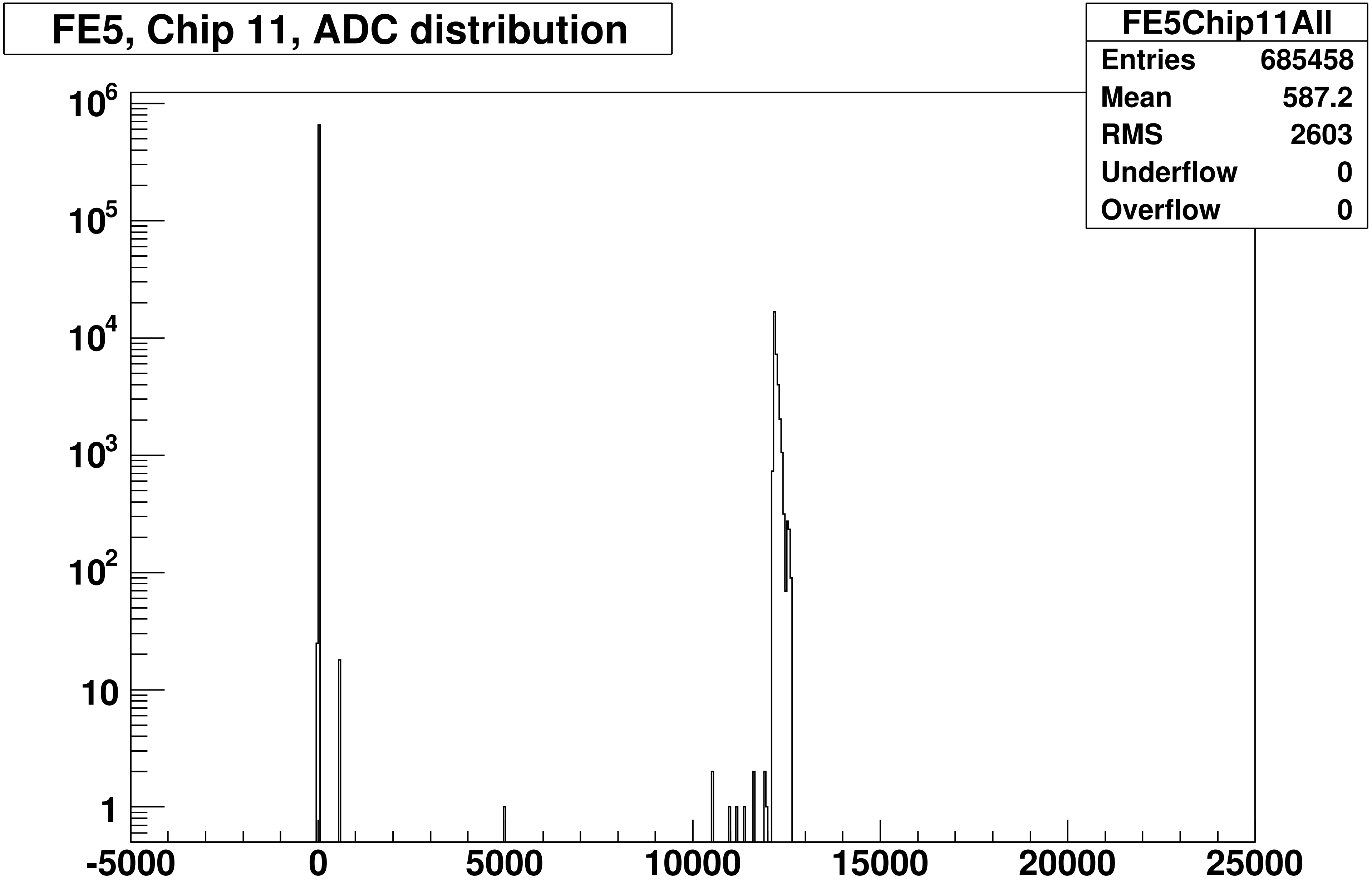

FE5, Chip 10, ADC distribution
FE5Chip10All
Entries 685458
Mean 580.1
RMS 2586
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



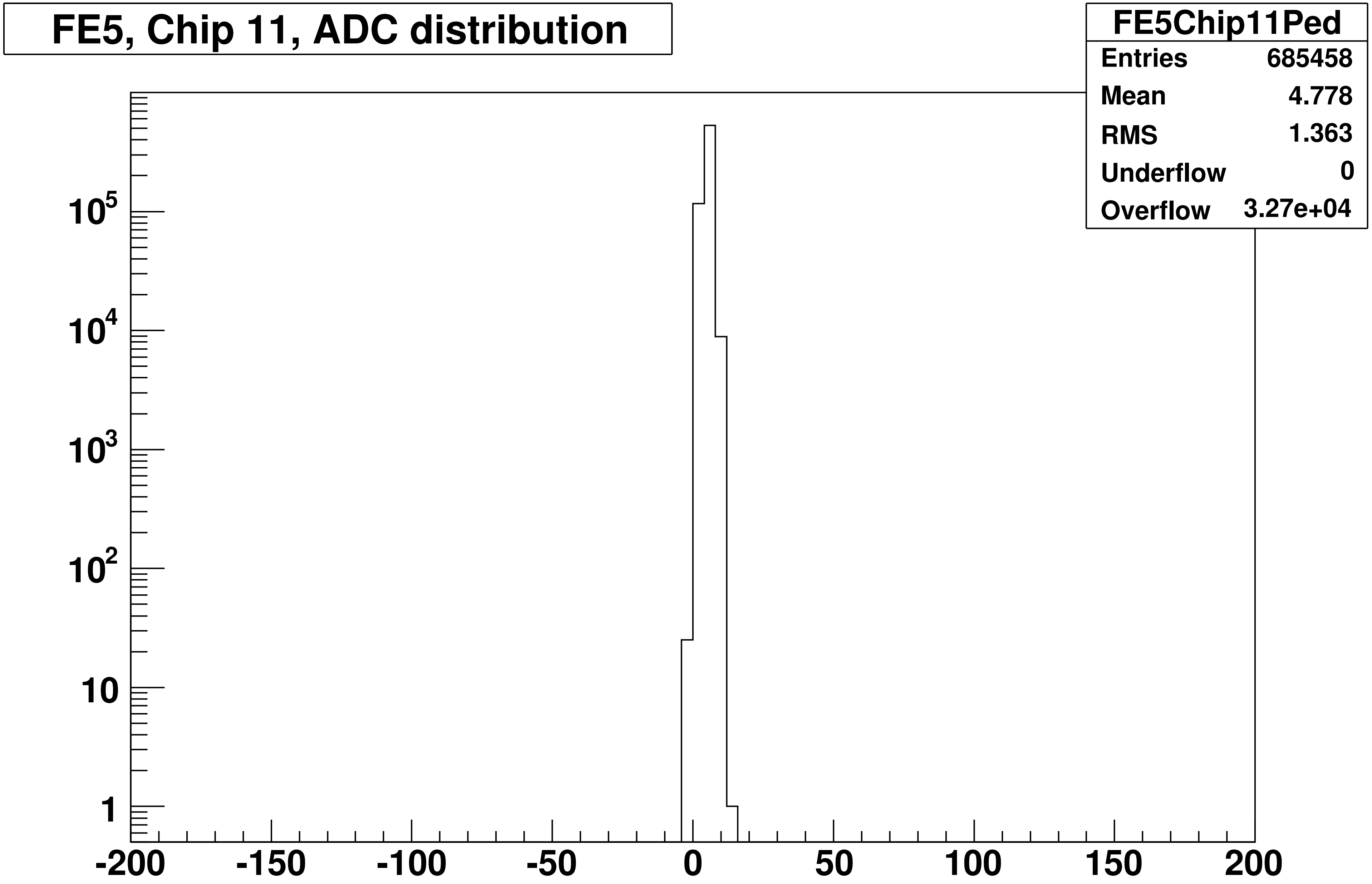
FE5, Chip 10, ADC distribution
FE5Chip10Ped
Entries 685458
Mean 2.02
RMS 1.378
Underflow 0
Overflow 3.282e+04
10^6
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
200

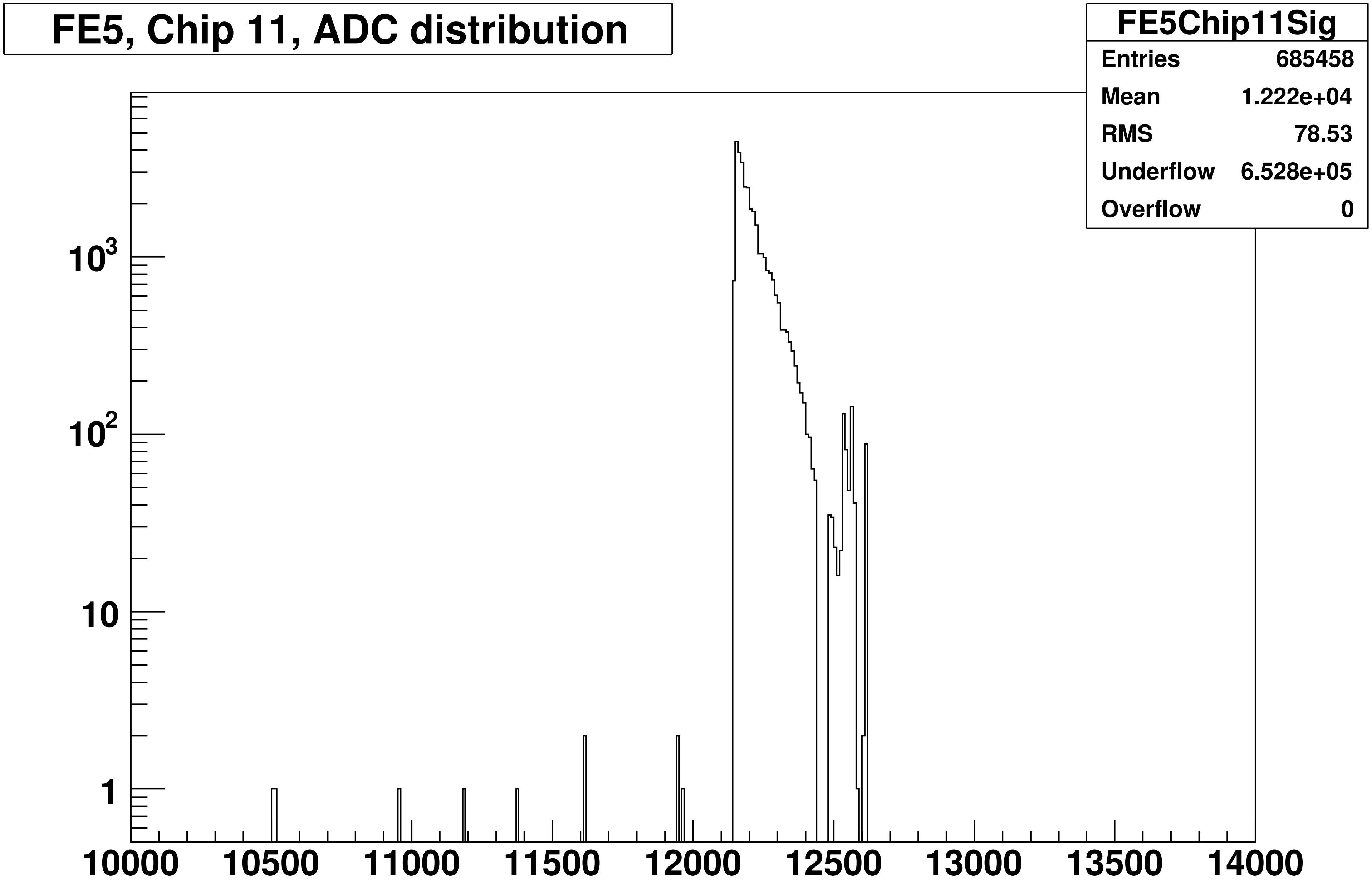


FE5, Chip 10, ADC distribution
FE5Chip10Sig
Entries 685458
Mean 1.215e+04
RMS 73.31
Underflow 6.529e+05
Overflow 0
10^3
10^2
10
10000
10500
11000
11500
12000
12500
13000
13500
14000



FE5, Chip 11, ADC distribution
FE5Chip11All
Entries 685458
Mean 587.2
RMS 2603
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE5, Chip 11, ADC distribution
FE5Chip11Ped
Entries 685458
Mean 4.778
RMS 1.363
Underflow 0
Overflow 3.27e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
200


FE5, Chip 11, ADC distribution
FE5Chip11Sig
Entries 685458
Mean 1.222e+04
RMS 78.53
Underflow 6.528e+05
Overflow 0
10^3
10^2
10
1
10000
10500
11000
11500
12000
12500
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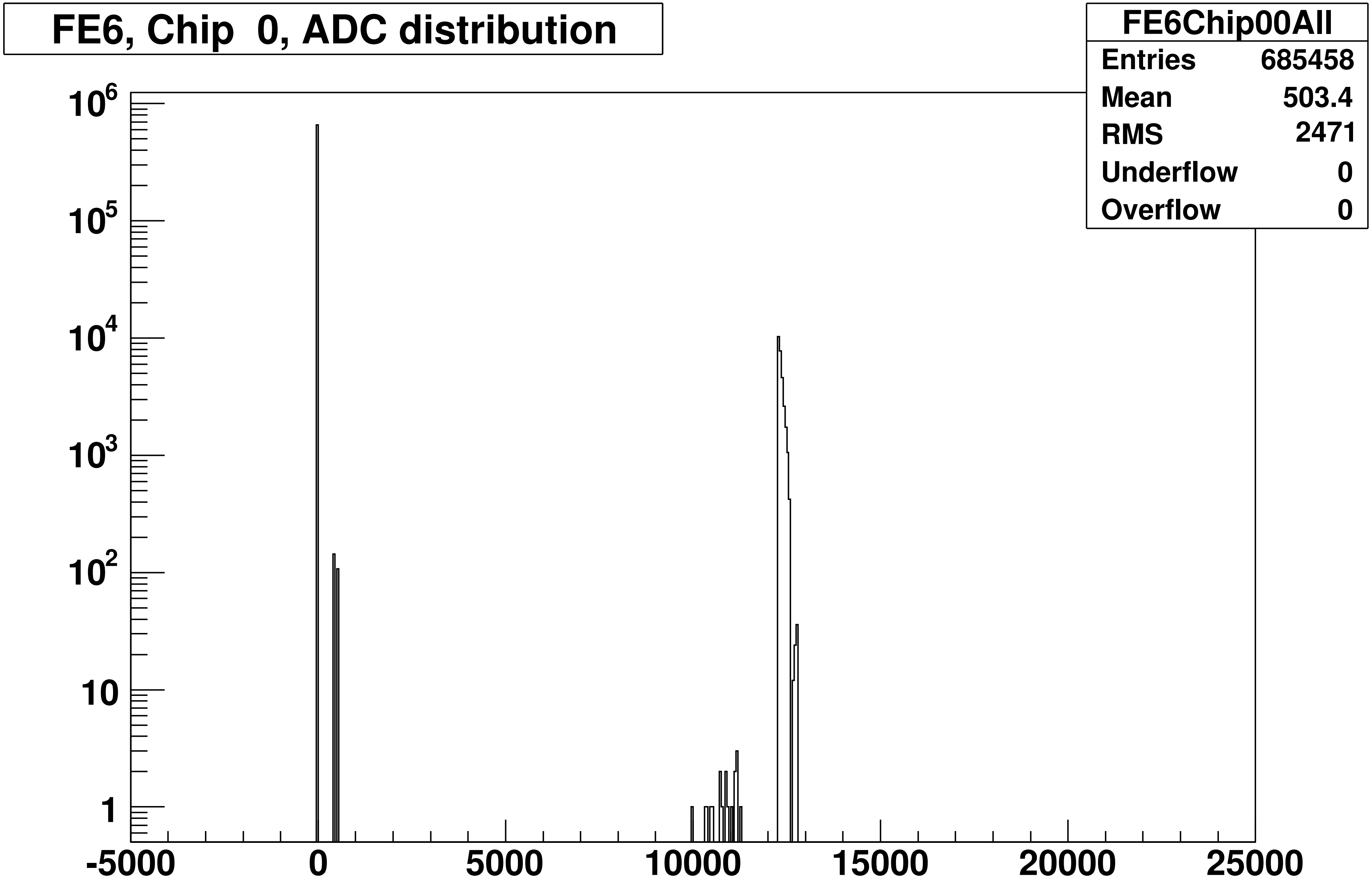
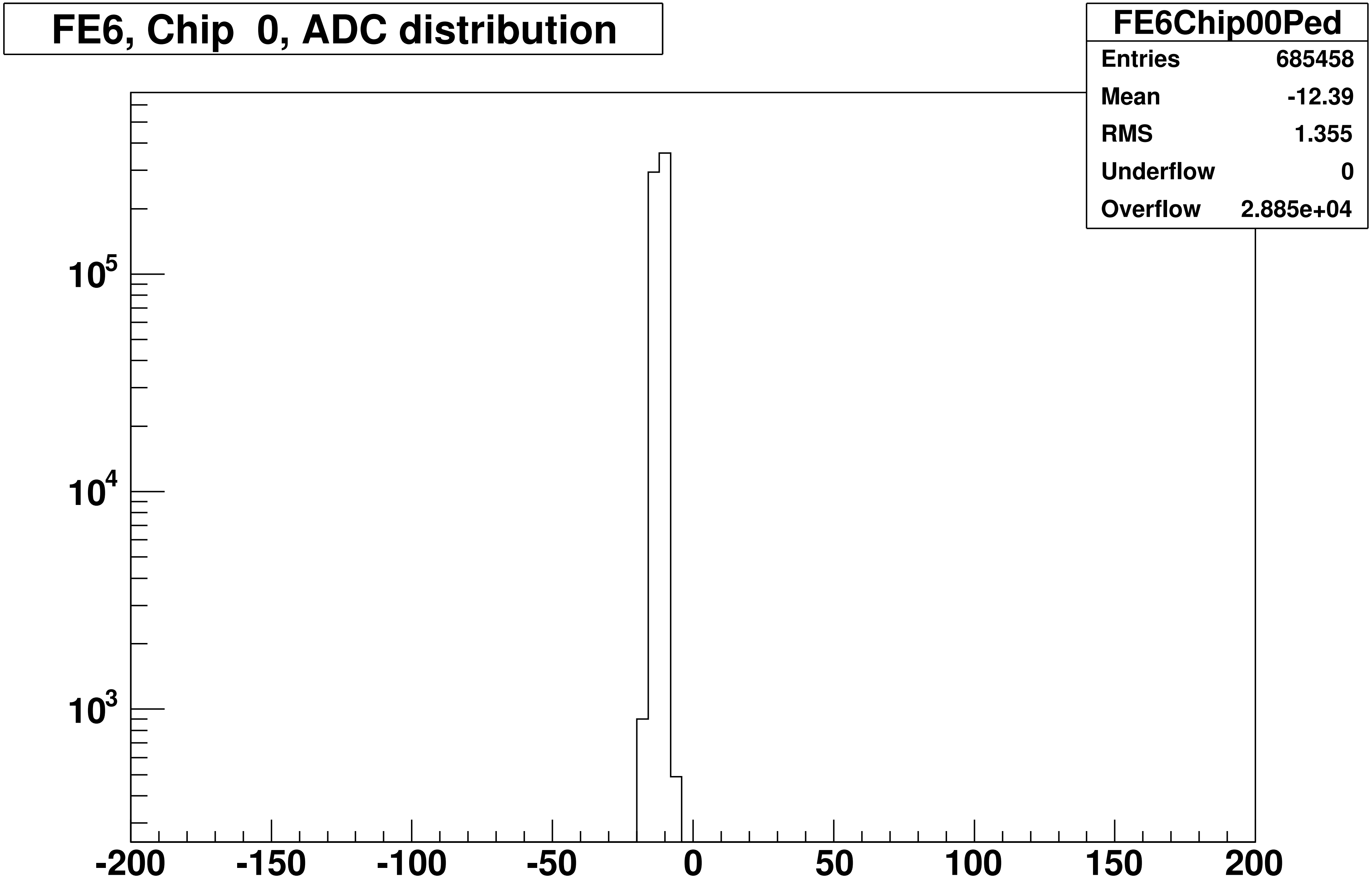
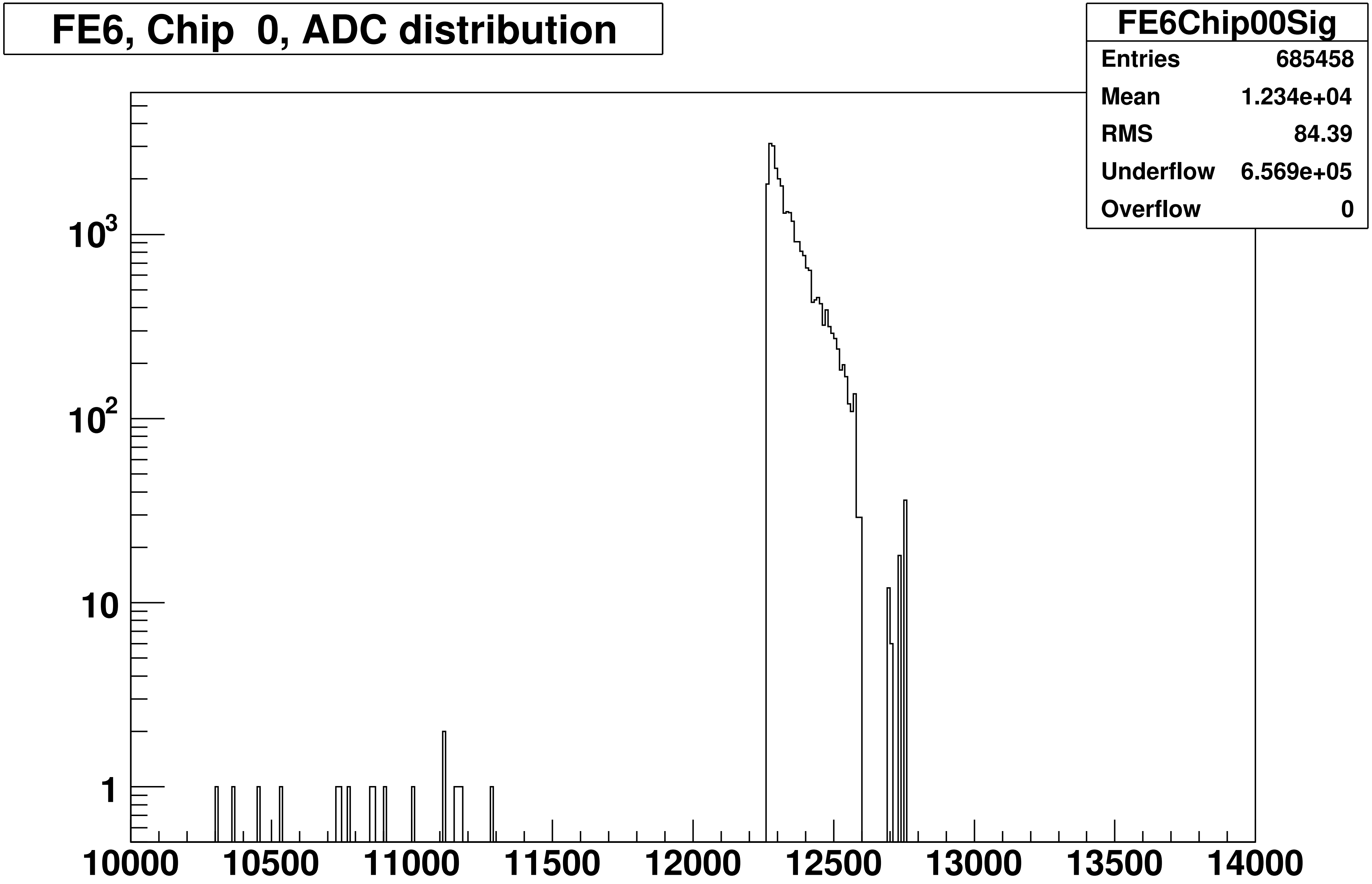
13500
14000



FE6, Chip 0, ADC distribution
FE6Chip00All
Entries 685458
Mean 503.4
RMS 2471
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE6, Chip 0, ADC distribution
FE6Chip00Ped
Entries 685458
Mean -12.39
RMS 1.355
Underflow 0
Overflow 2.885e+04
10^5
10^4
10^3
-200
-150
-100
-50
0
50
100
150
200



FE6, Chip 0, ADC distribution
FE6Chip00Sig
Entries 685458
Mean 1.234e+04
RMS 84.39
Underflow 6.569e+05
Overflow 0
10^3
10^2
10
1
10000
10500
11000
11500
12000
12500
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13500
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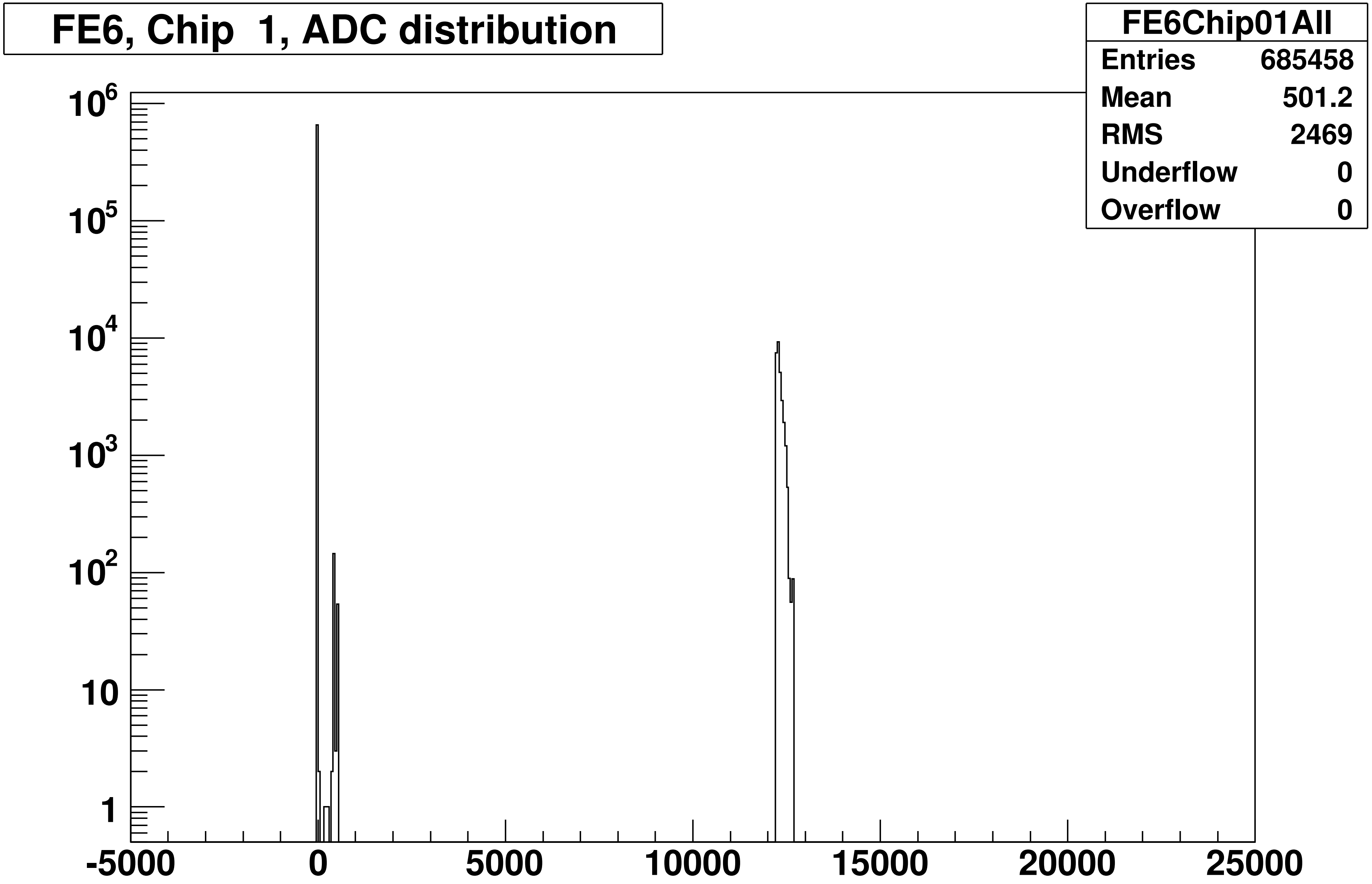
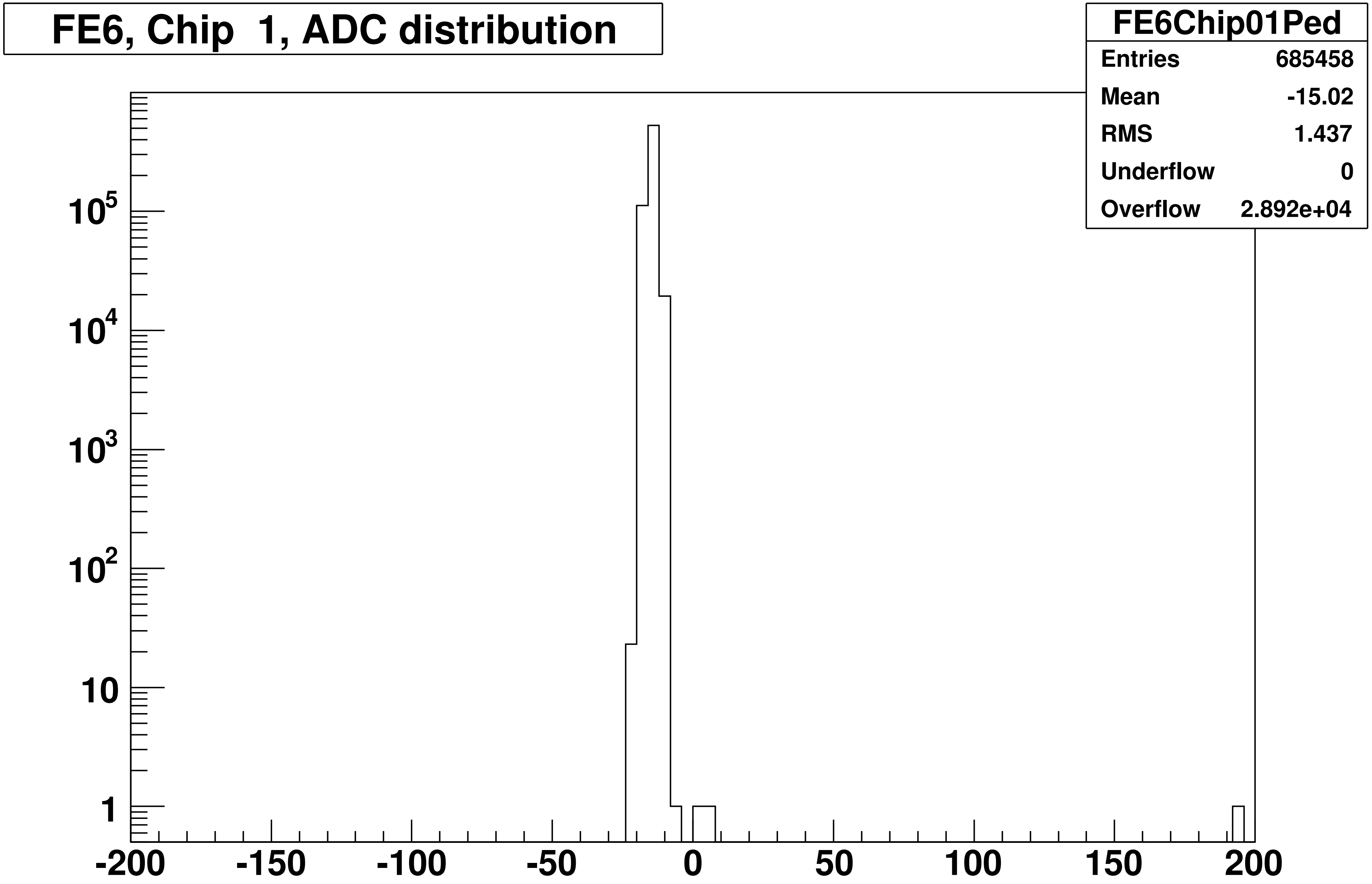


FE6, Chip 1, ADC distribution
FE6Chip01All
Entries 685458
Mean 501.2
RMS 2469
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE6, Chip 1, ADC distribution
FE6Chip01Ped
Entries 685458
Mean -15.02
RMS 1.437
Underflow 0
Overflow 2.892e+04
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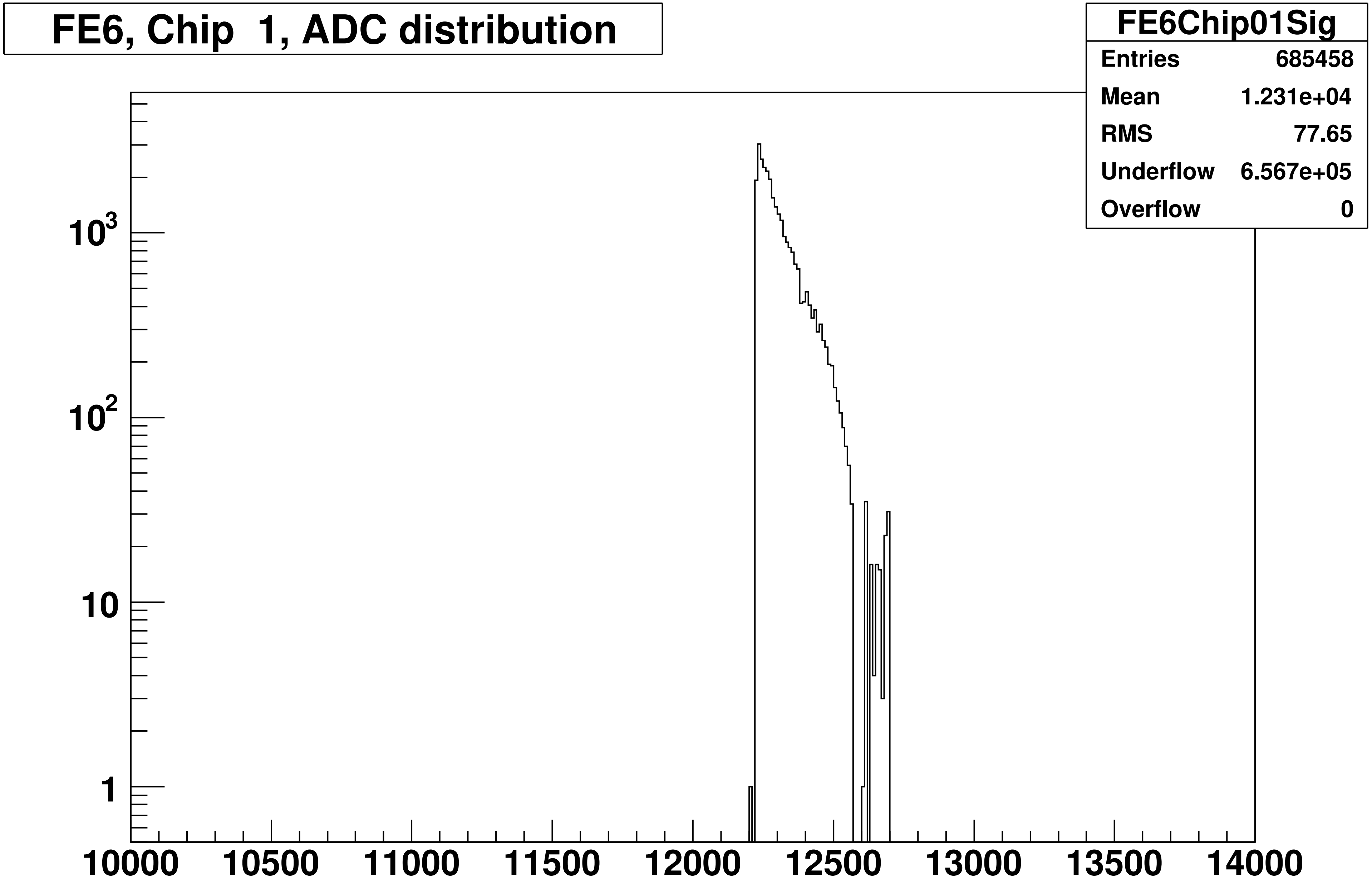
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
200



FE6, Chip 1, ADC distribution
FE6Chip01Sig
Entries 685458
Mean 1.231e+04
RMS 77.65
Underflow 6.567e+05
Overflow 0
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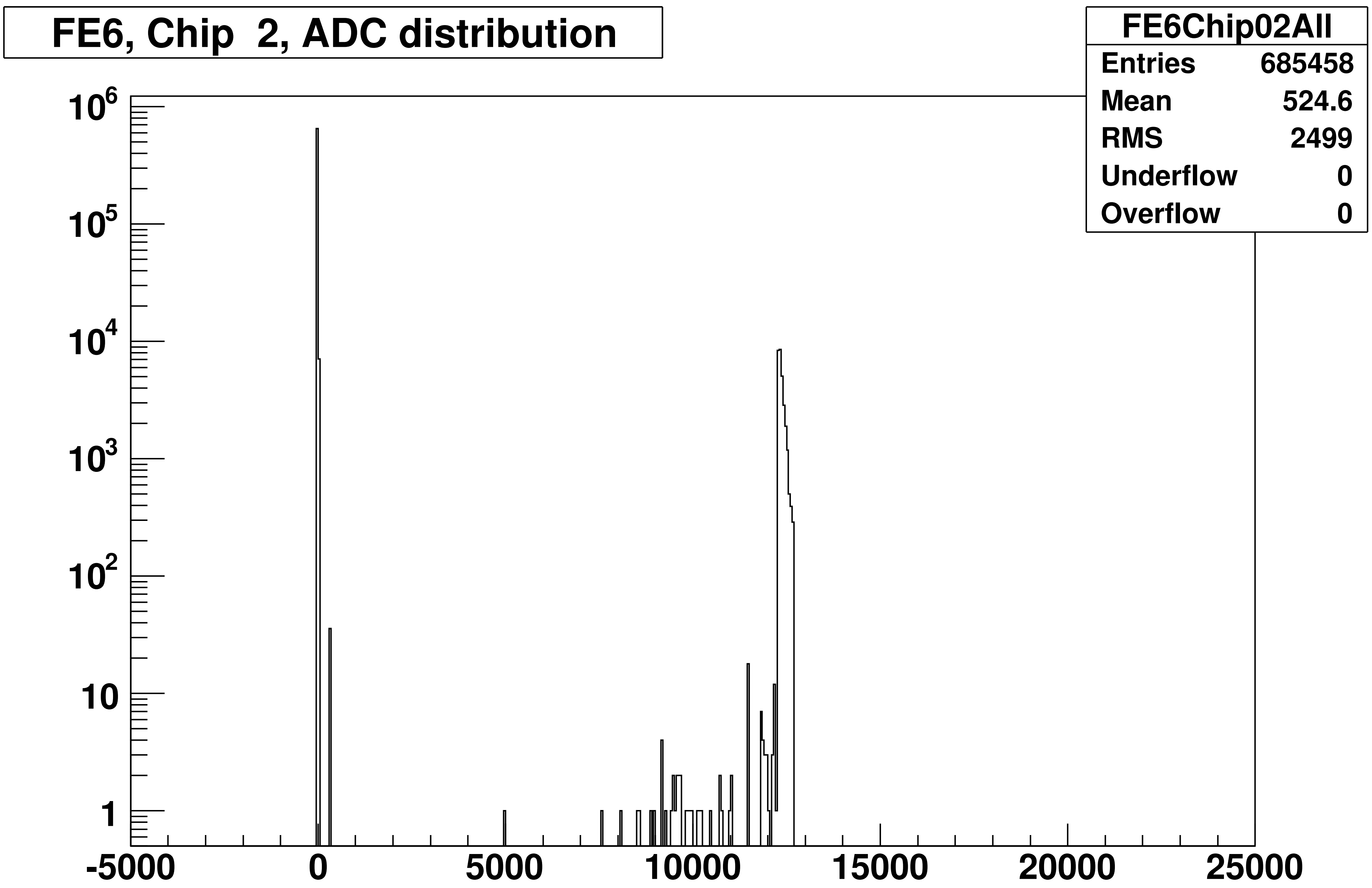
10^2
10
1
10000
10500
11000
11500
12000
12500
13000
13500
14000



FE6, Chip 2, ADC distribution
FE6Chip02All
Entries 685458
Mean 524.6
RMS 2499
Underflow 0
Overflow 0
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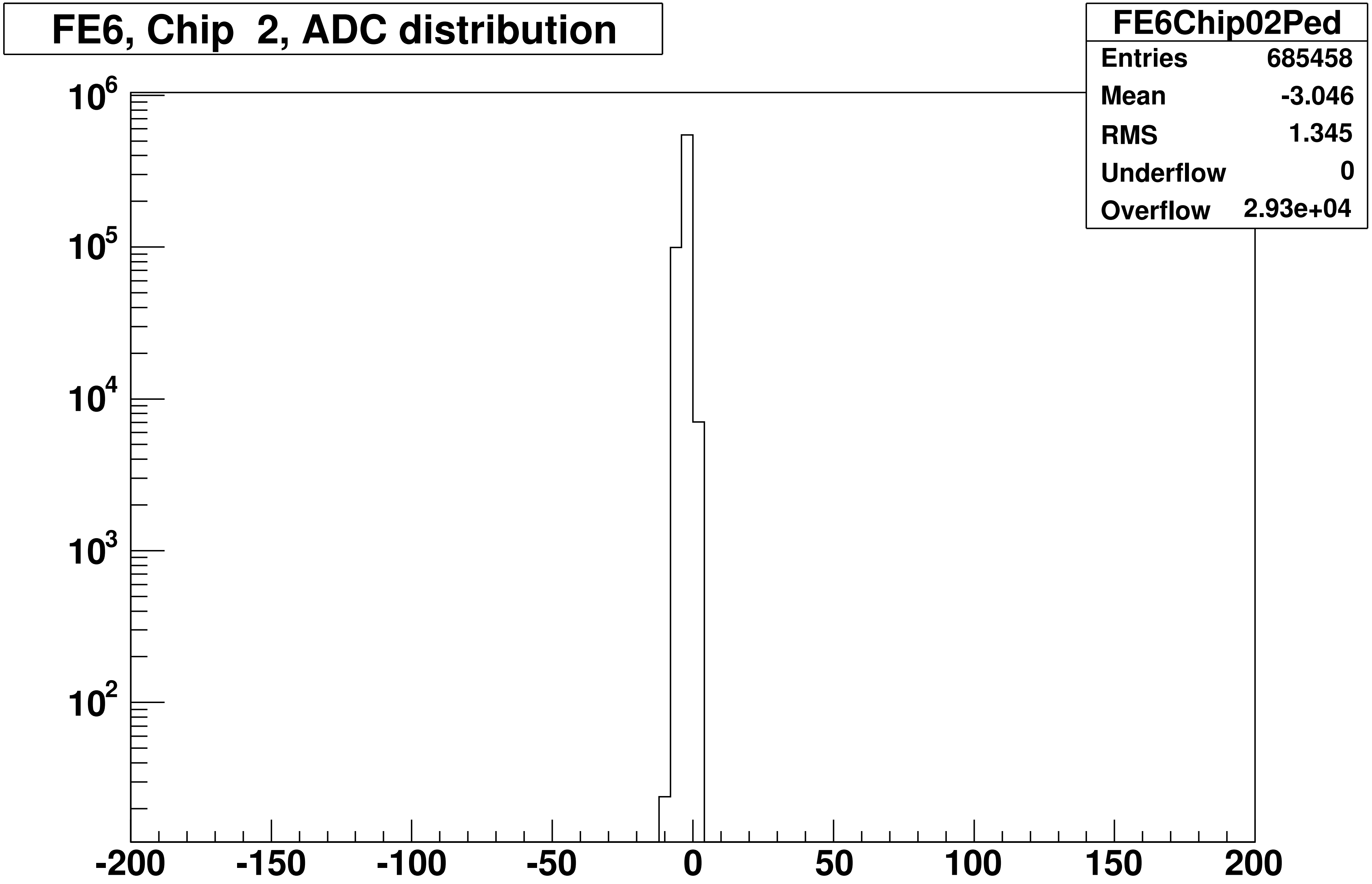
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE6, Chip 2, ADC distribution
FE6Chip02Ped
Entries 685458
Mean -3.046
RMS 1.345
Underflow 0
Overflow 2.93e+04
10^6
10^5
10^4
10^3
10^2
-200
-150
-100
-50
0
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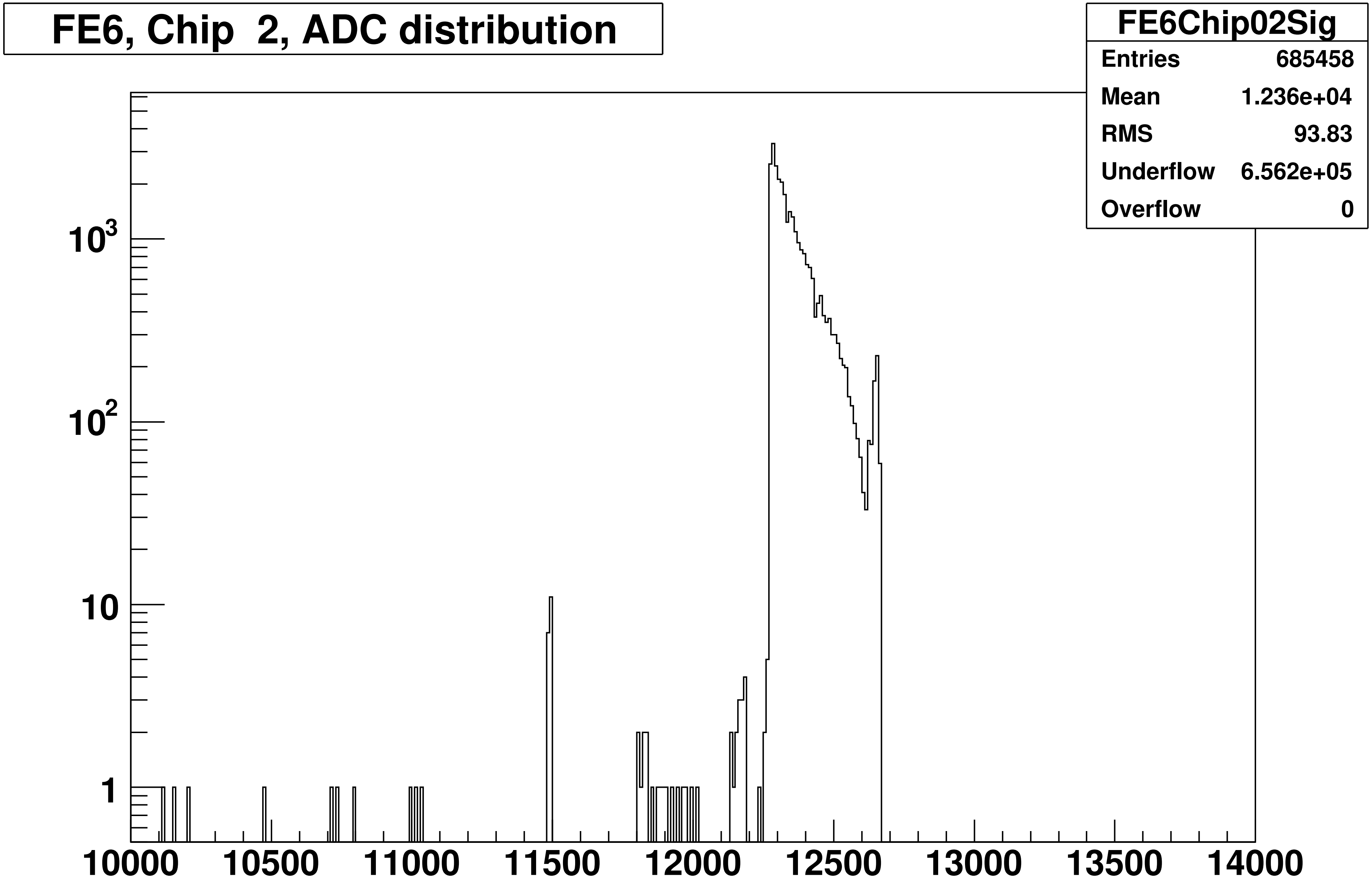
100
150
200



FE6, Chip 2, ADC distribution
FE6Chip02Sig
Entries 685458
Mean 1.236e+04
RMS 93.83
Underflow 6.562e+05
Overflow 0
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10^2
10
1
10000
10500
11000
11500
12000
12500
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13500
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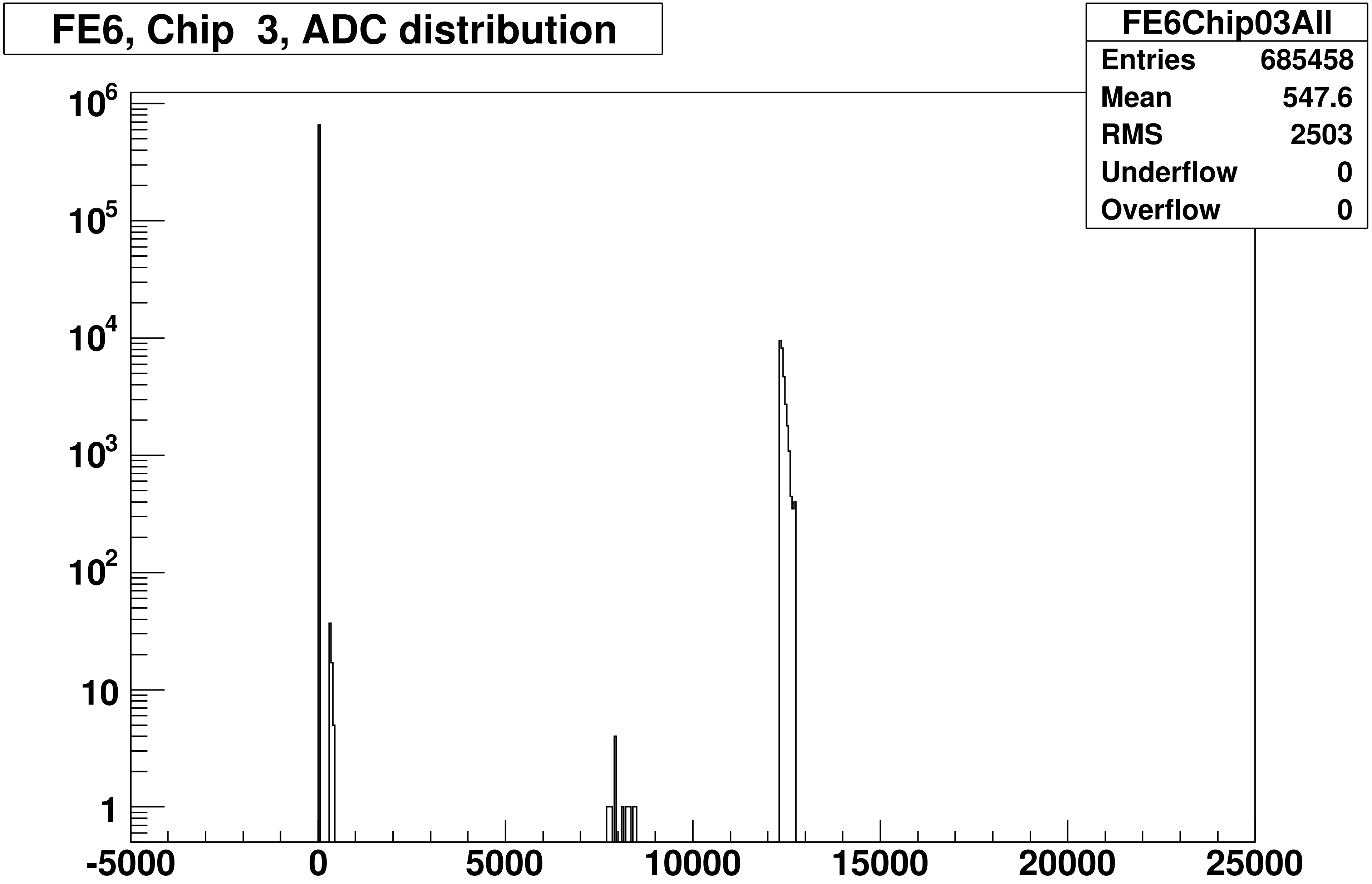
FE6, Chip 3, ADC distribution
FE6Chip03All
Entries 685458
Mean 547.6
RMS 2503
Underflow 0
Overflow 0
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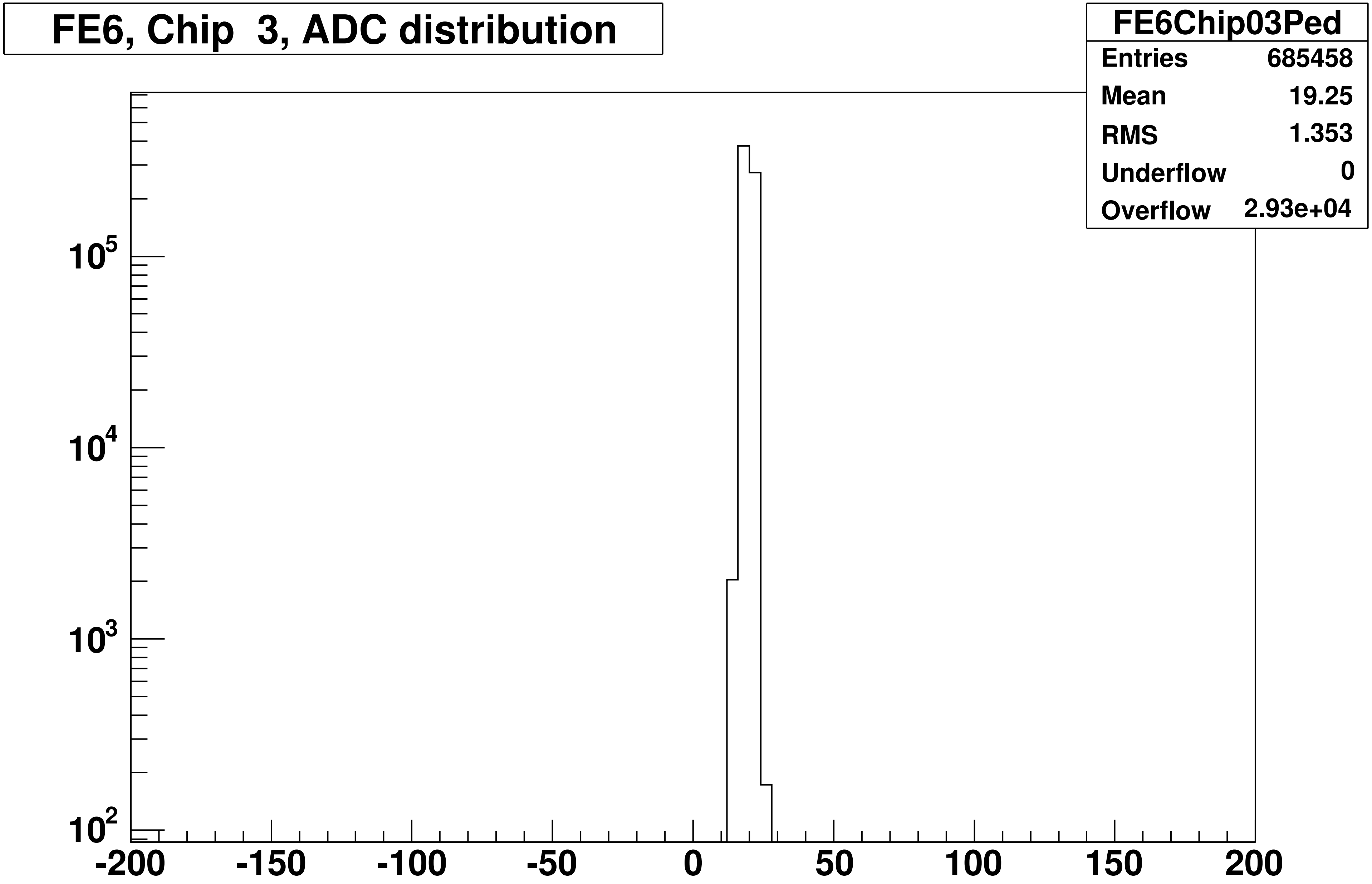
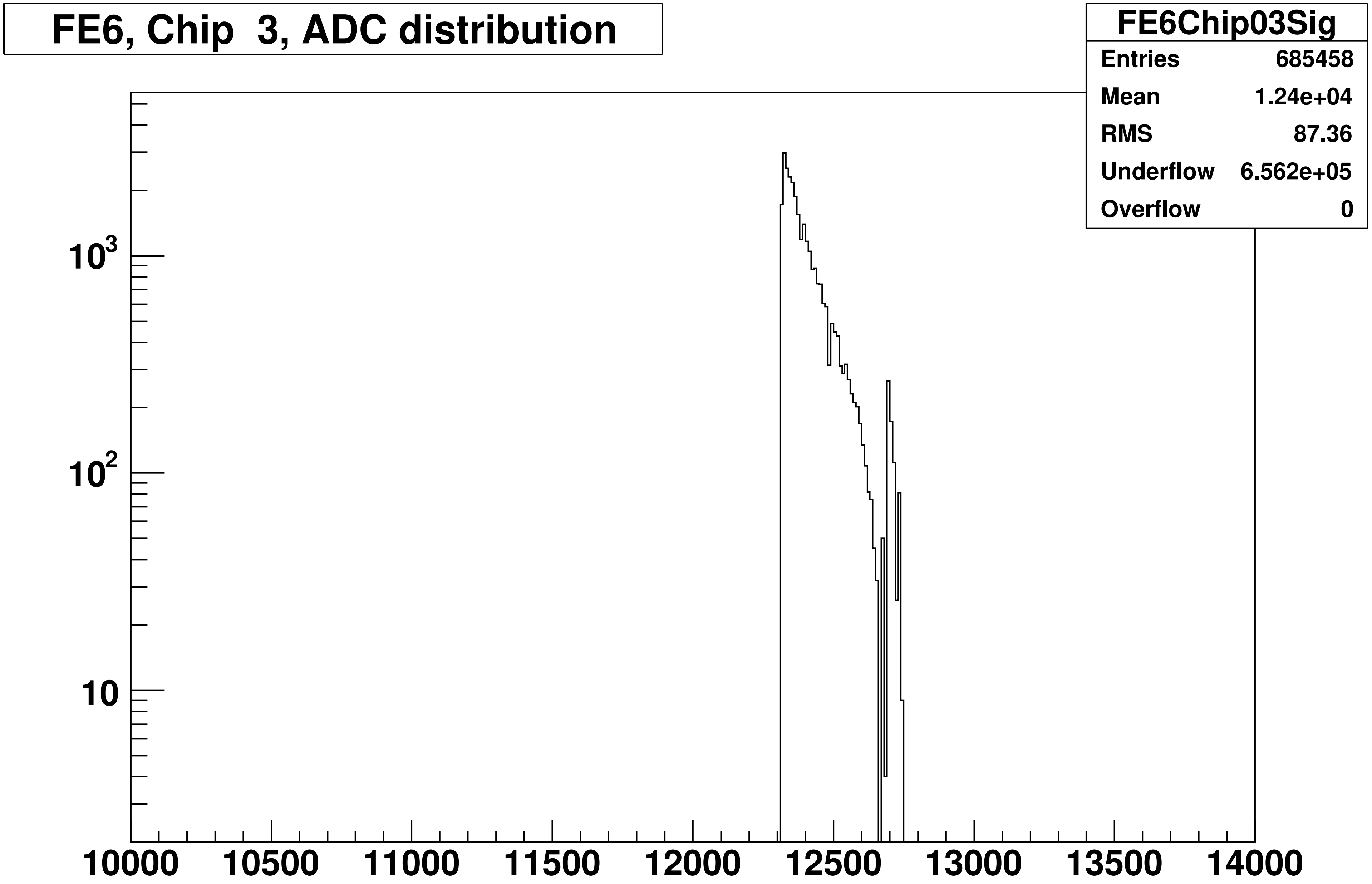
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE6, Chip 3, ADC distribution
FE6Chip03Ped
Entries 685458
Mean 19.25
RMS 1.353
Underflow 0
Overflow 2.93e+04
10^5
10^4
10^3
10^2
-200
-150
-100
-50
0
50
100
150
200



FE6, Chip 3, ADC distribution
FE6Chip03Sig
Entries 685458
Mean 1.24e+04
RMS 87.36
Underflow 6.562e+05
Overflow 0
10^3
10^2
10
10000
10500
11000
11500
12000
12500
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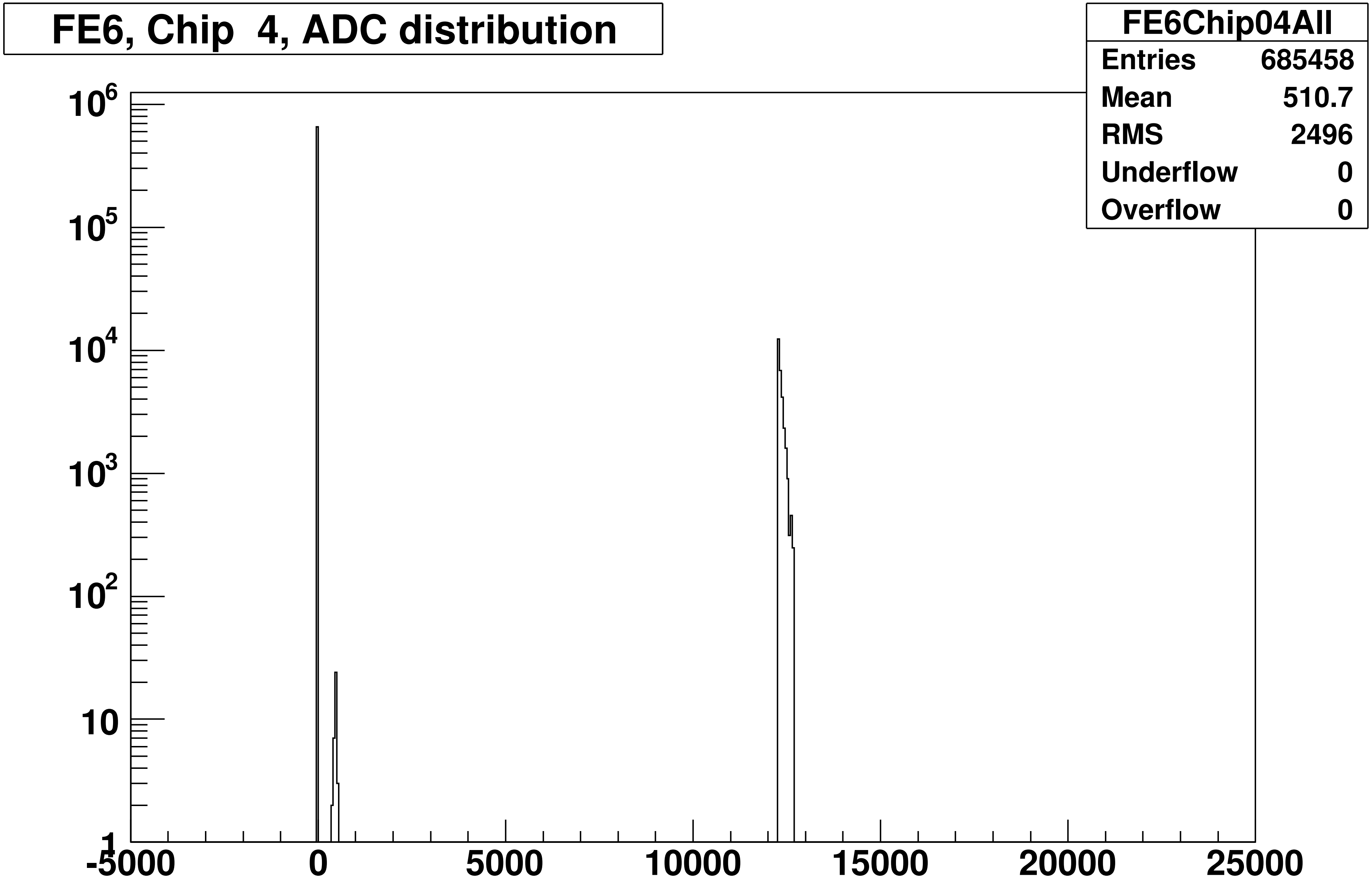
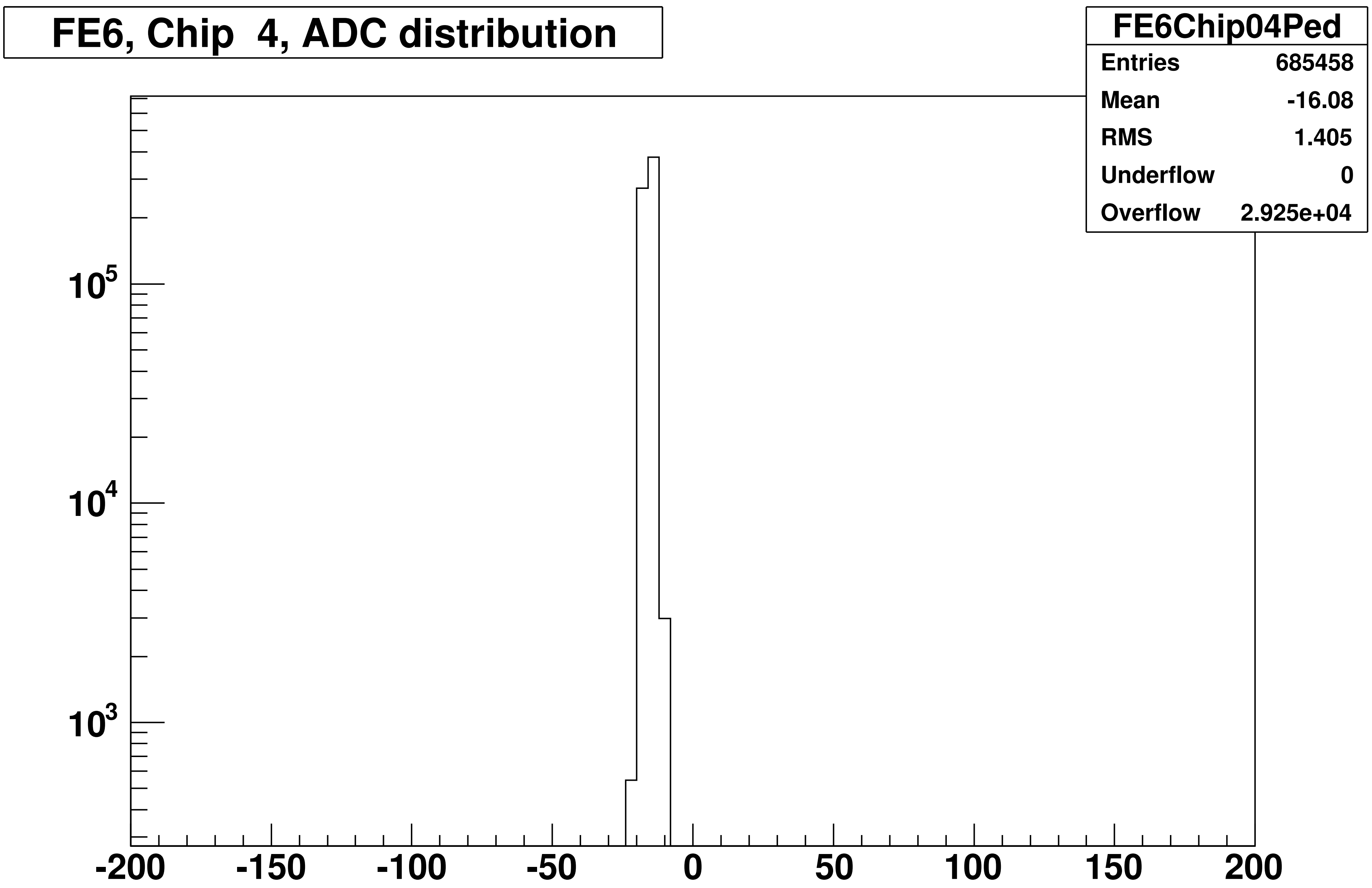
14000



FE6, Chip 4, ADC distribution
FE6Chip04All
Entries 685458
Mean 510.7
RMS 2496
Underflow 0
Overflow 0
1
10
10^2
10^3
10^4
10^5
10^6
-5000
0
5000
10000
15000
20000
25000


FE6, Chip 4, ADC distribution
FE6Chip04Ped
Entries 685458
Mean -16.08
RMS 1.405
Underflow 0
Overflow 2.925e+04
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10^4
10^3
-200
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-100
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0
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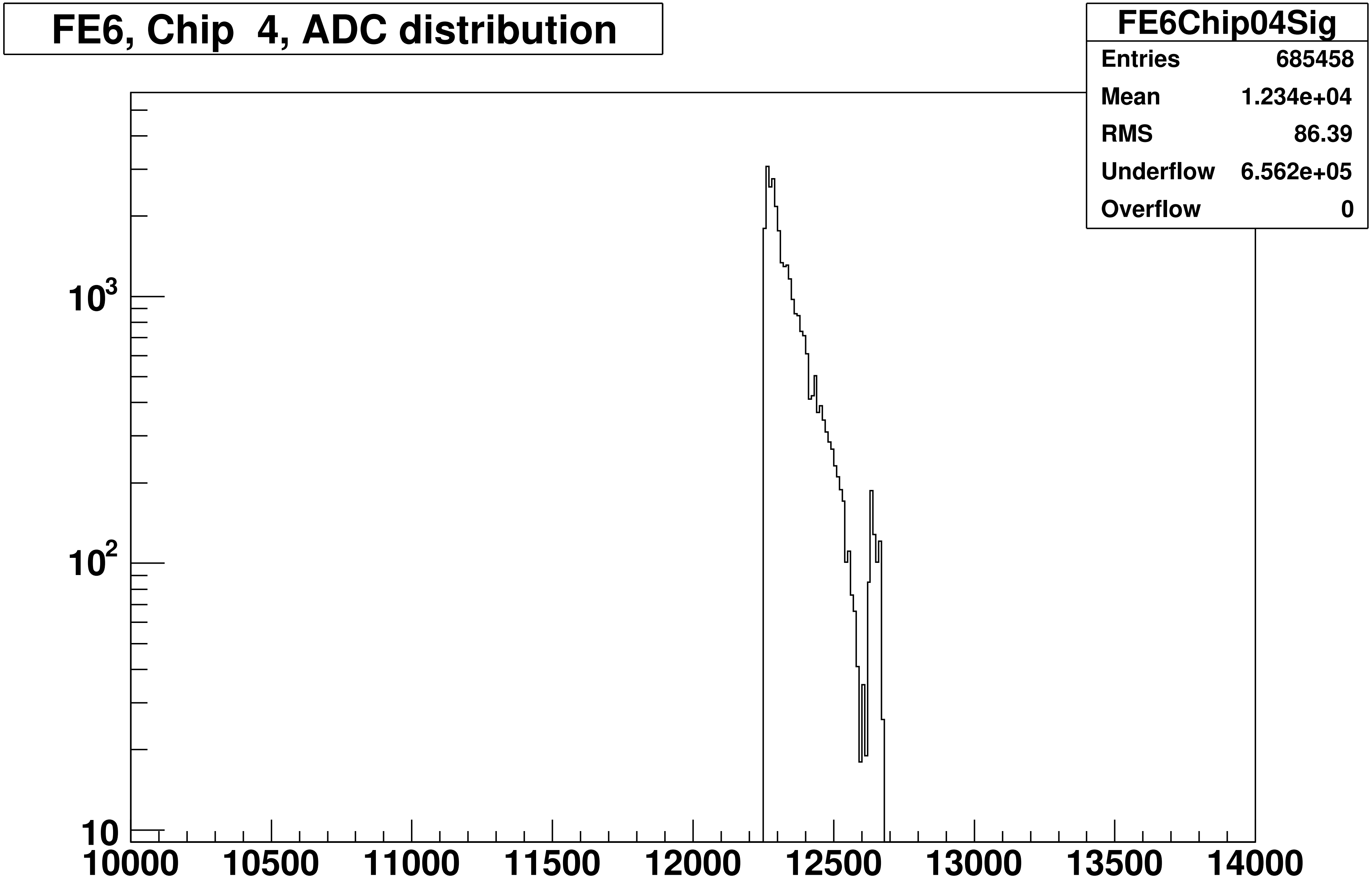
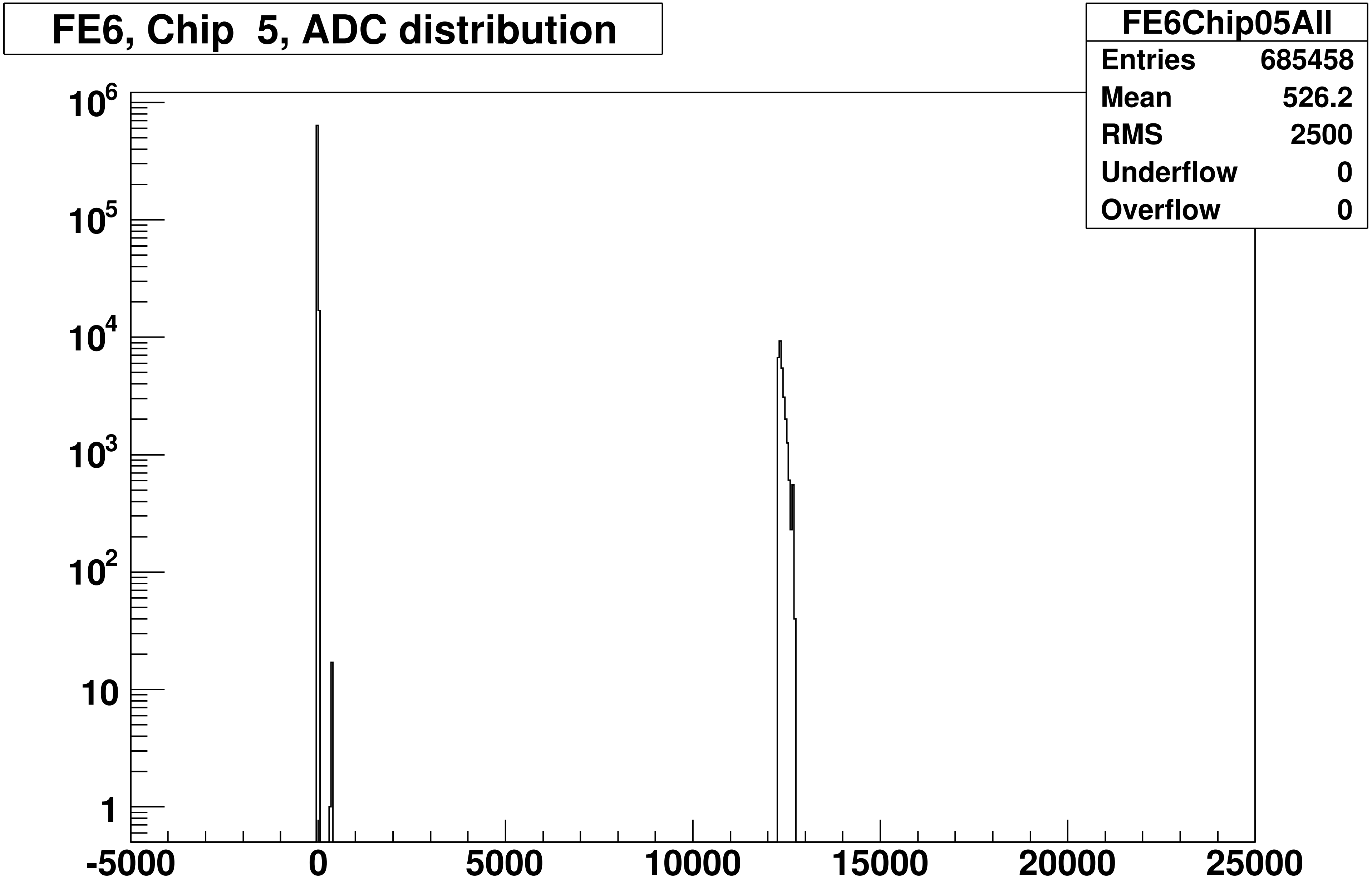
100
150
200


FE6, Chip 4, ADC distribution
FE6Chip04Sig
Entries 685458
Mean 1.234e+04
RMS 86.39
Underflow 6.562e+05
Overflow 0
10
10^2
10^3
10000
10500
11000
11500
12000
12500
13000
13500
14000


FE6, Chip 5, ADC distribution
FE6Chip05All
Entries 685458
Mean 526.2
RMS 2500
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
1
-5000
0
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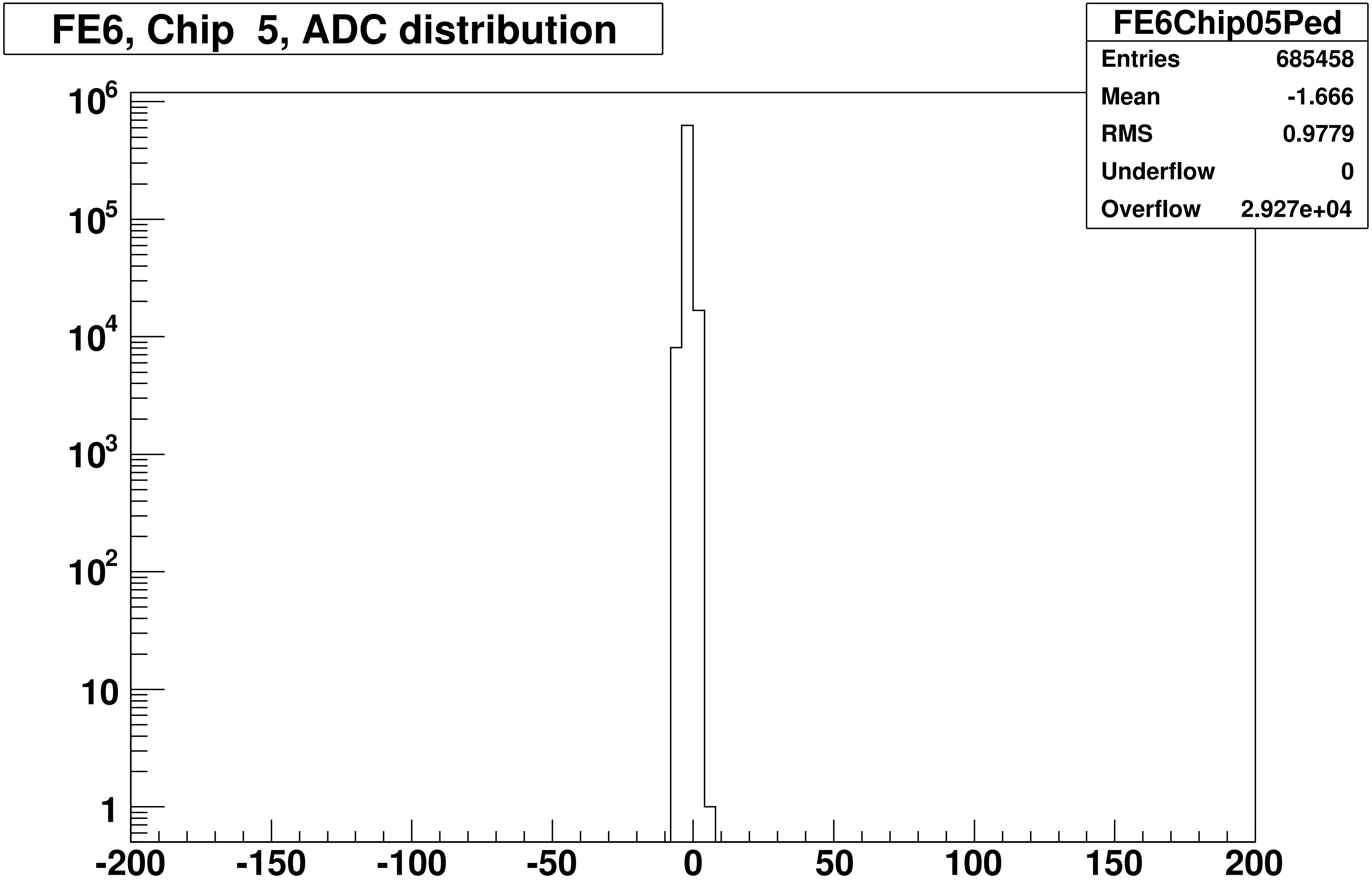
10000
15000
20000
25000


FE6, Chip 5, ADC distribution
FE6Chip05Ped
Entries 685458
Mean -1.666
RMS 0.9779
Underflow 0
Overflow 2.927e+04
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10^5
10^4
10^3
10^2
10
1
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-100
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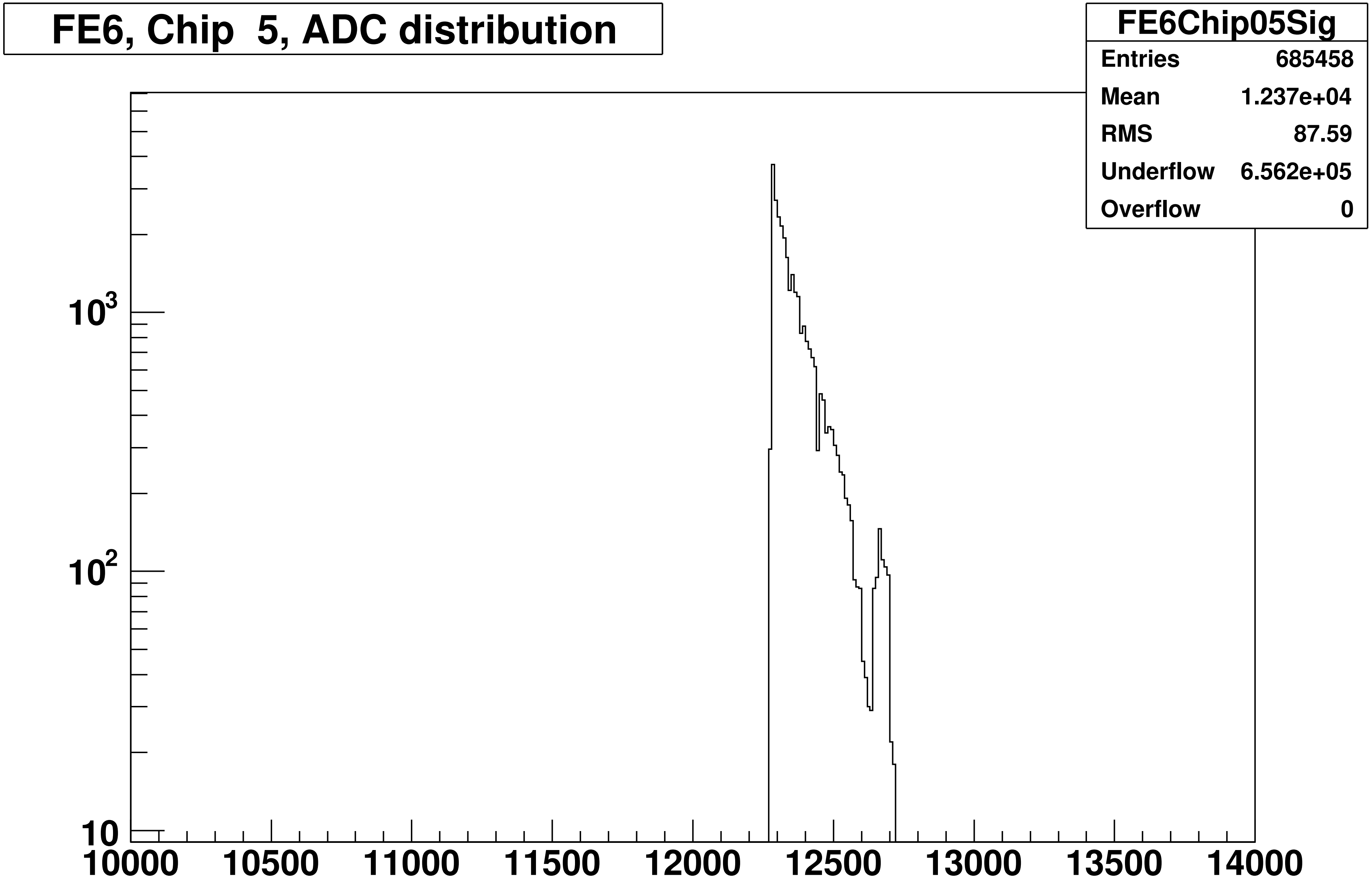
0
50
100
150
200


FE6, Chip 5, ADC distribution
FE6Chip05Sig
Entries 685458
Mean 1.237e+04
RMS 87.59
Underflow 6.562e+05
Overflow 0
10
10^2
10^3
10000
10500
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11500
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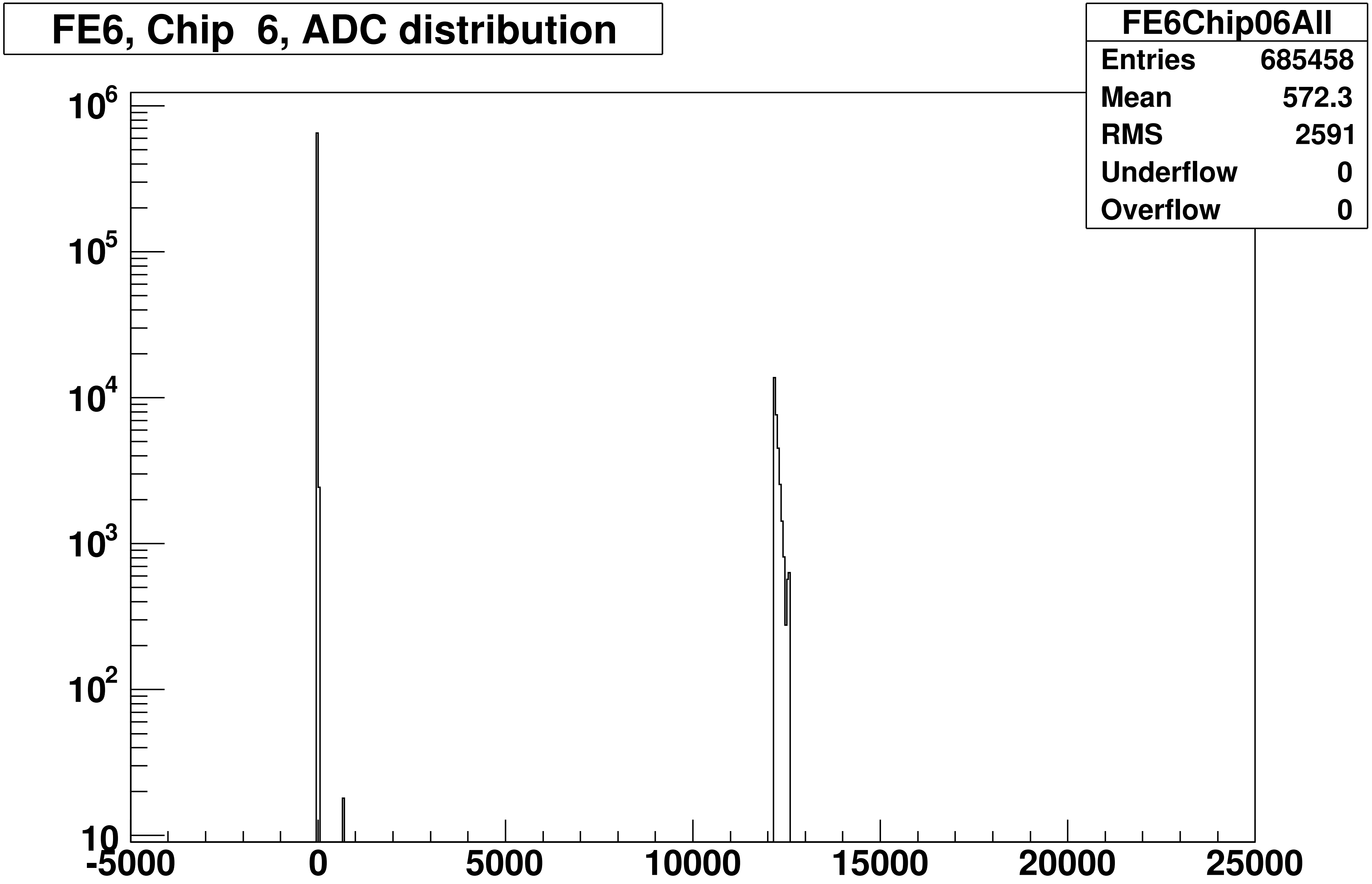
FE6, Chip 6, ADC distribution
FE6Chip06All
Entries 685458
Mean 572.3
RMS 2591
Underflow 0
Overflow 0
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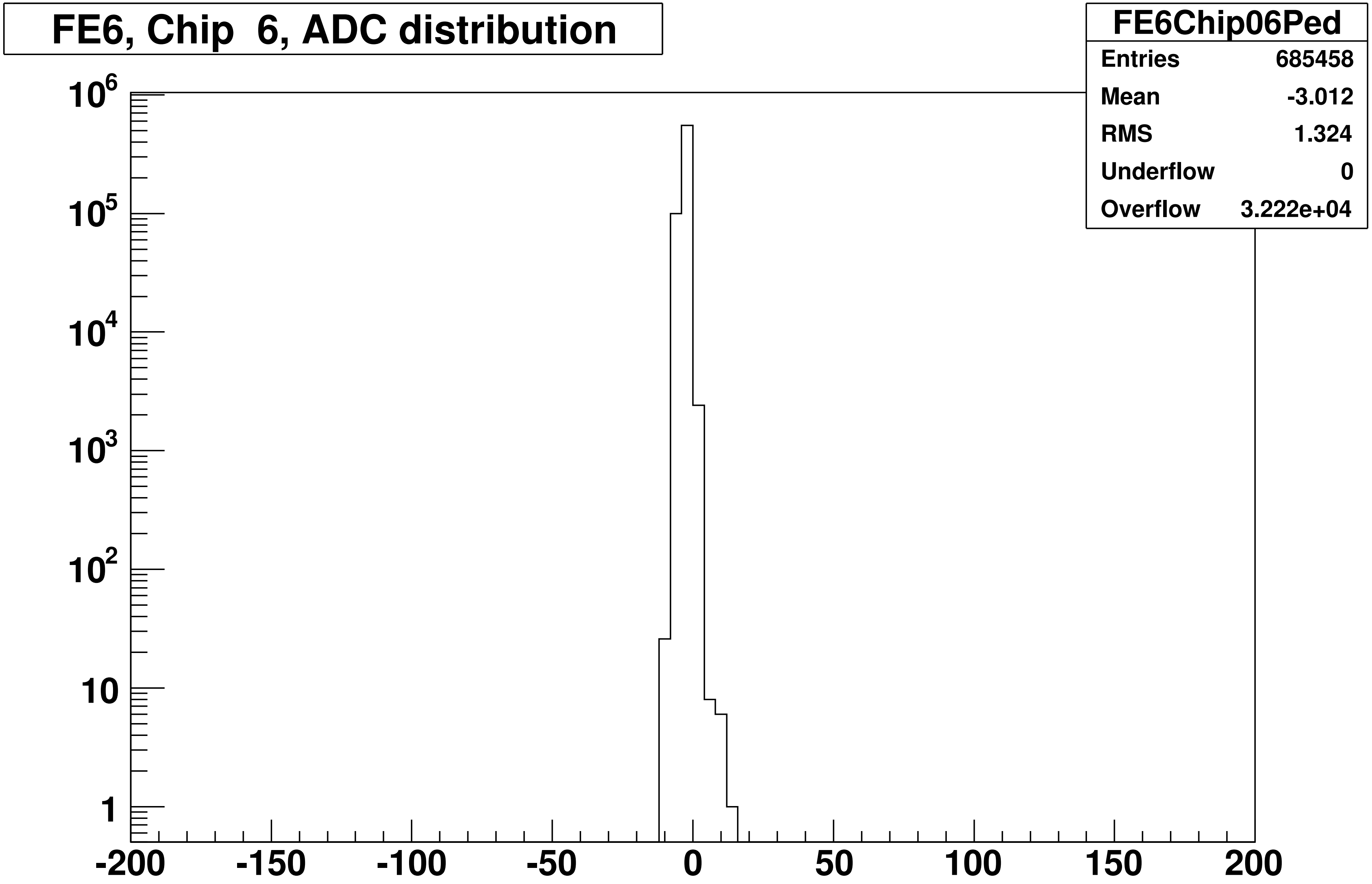
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE6, Chip 6, ADC distribution
FE6Chip06Ped
Entries 685458
Mean -3.012
RMS 1.324
Underflow 0
Overflow 3.222e+04
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10^5
10^4
10^3
10^2
10
1
-200
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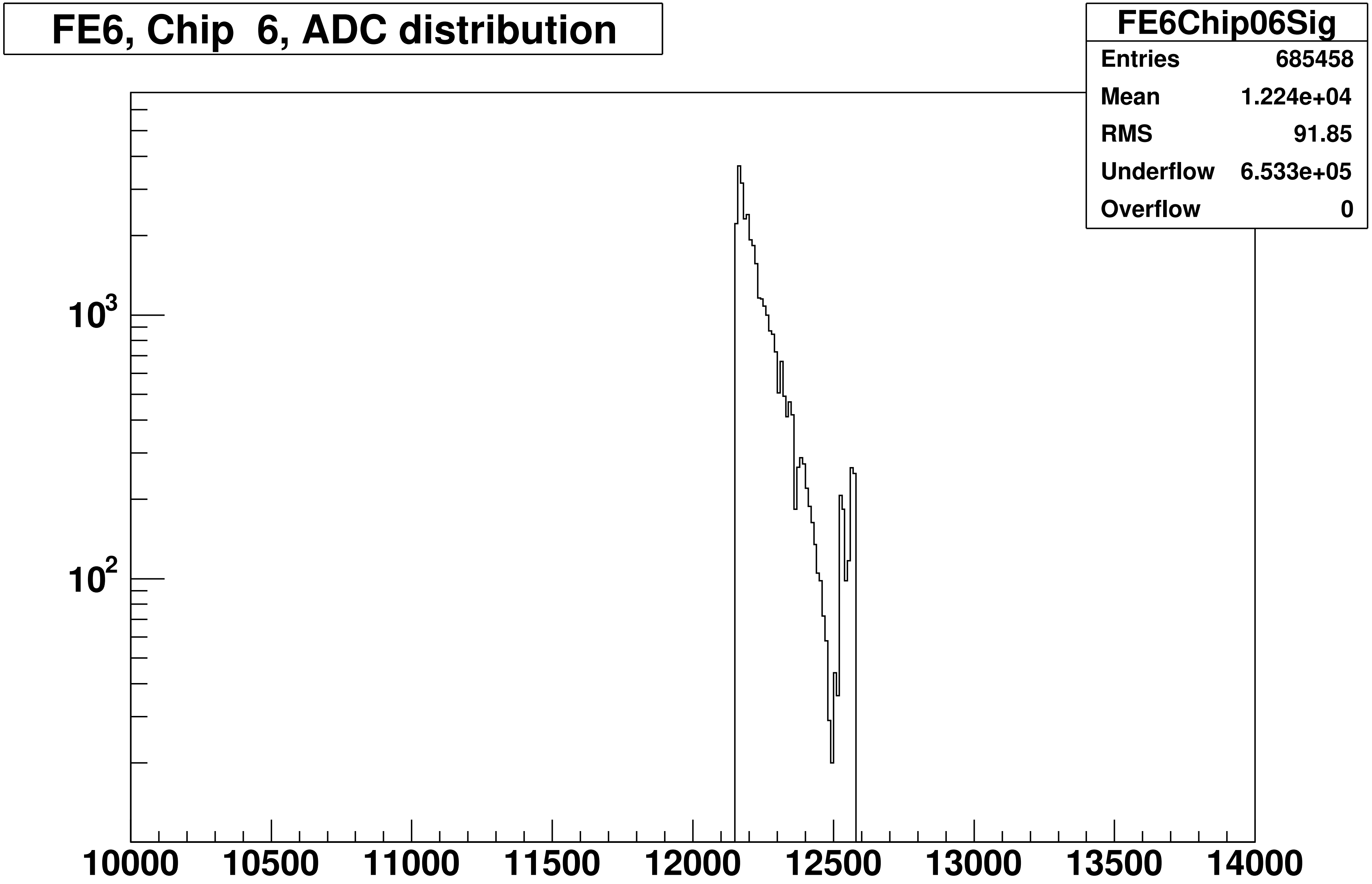
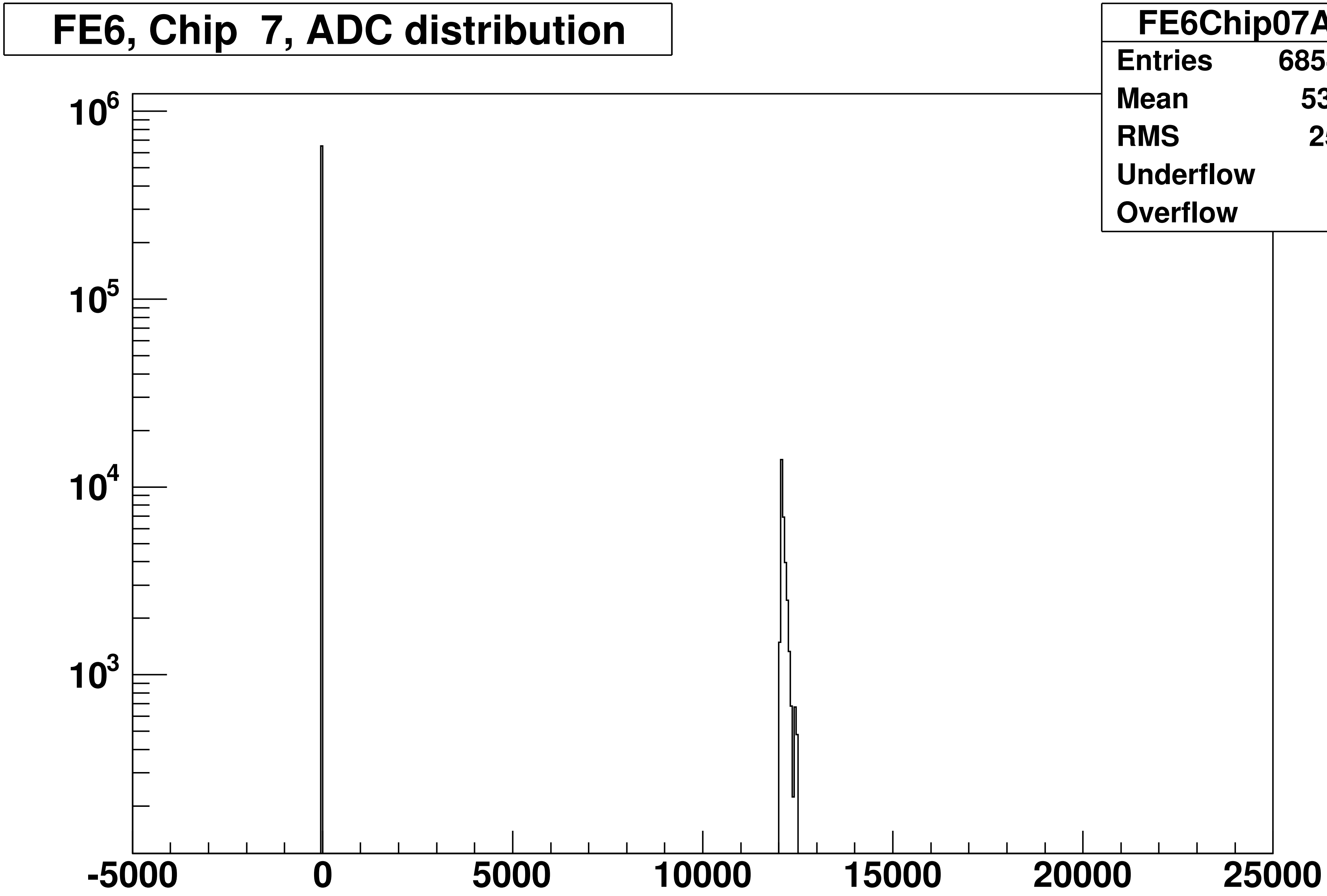
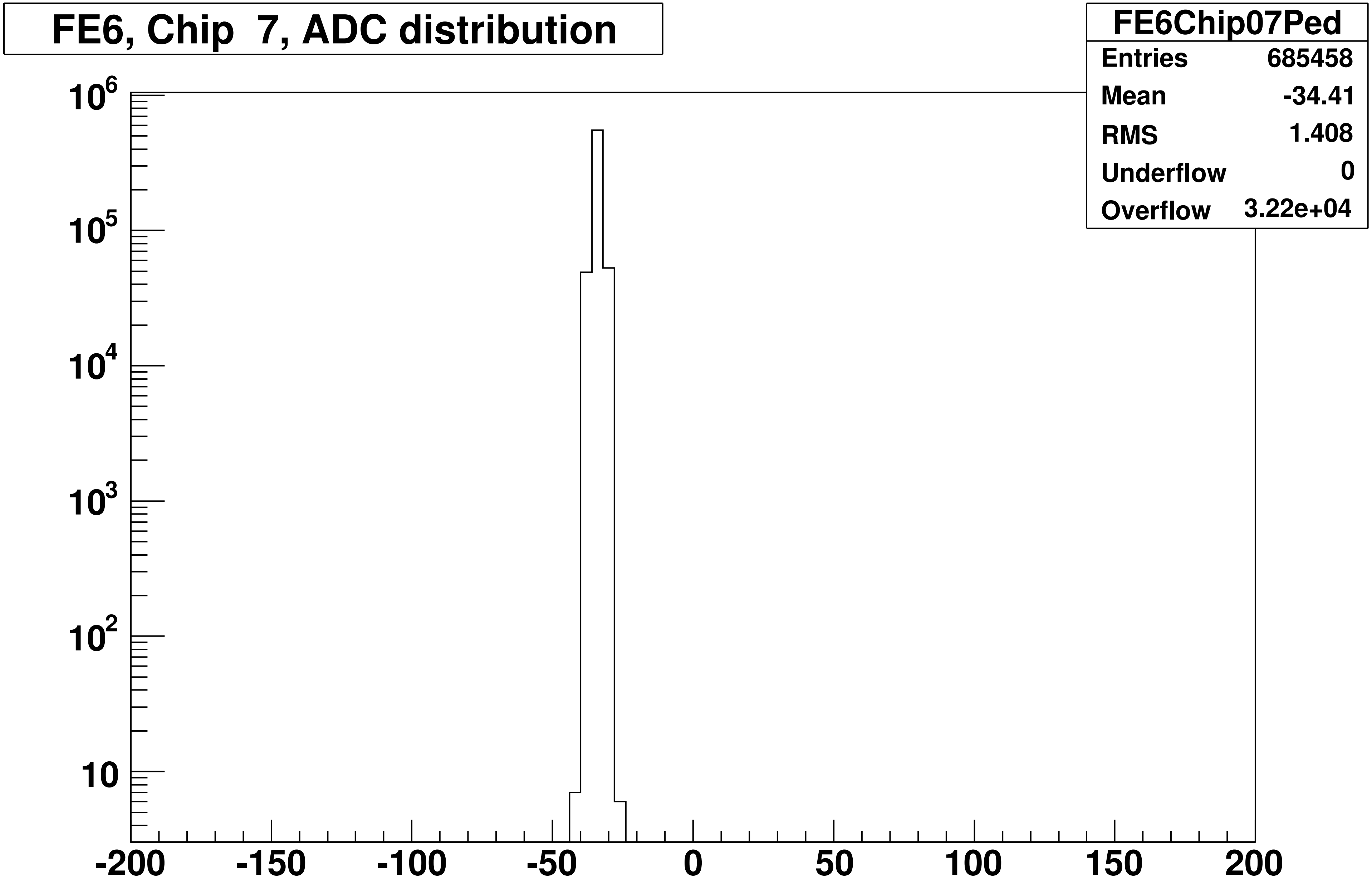
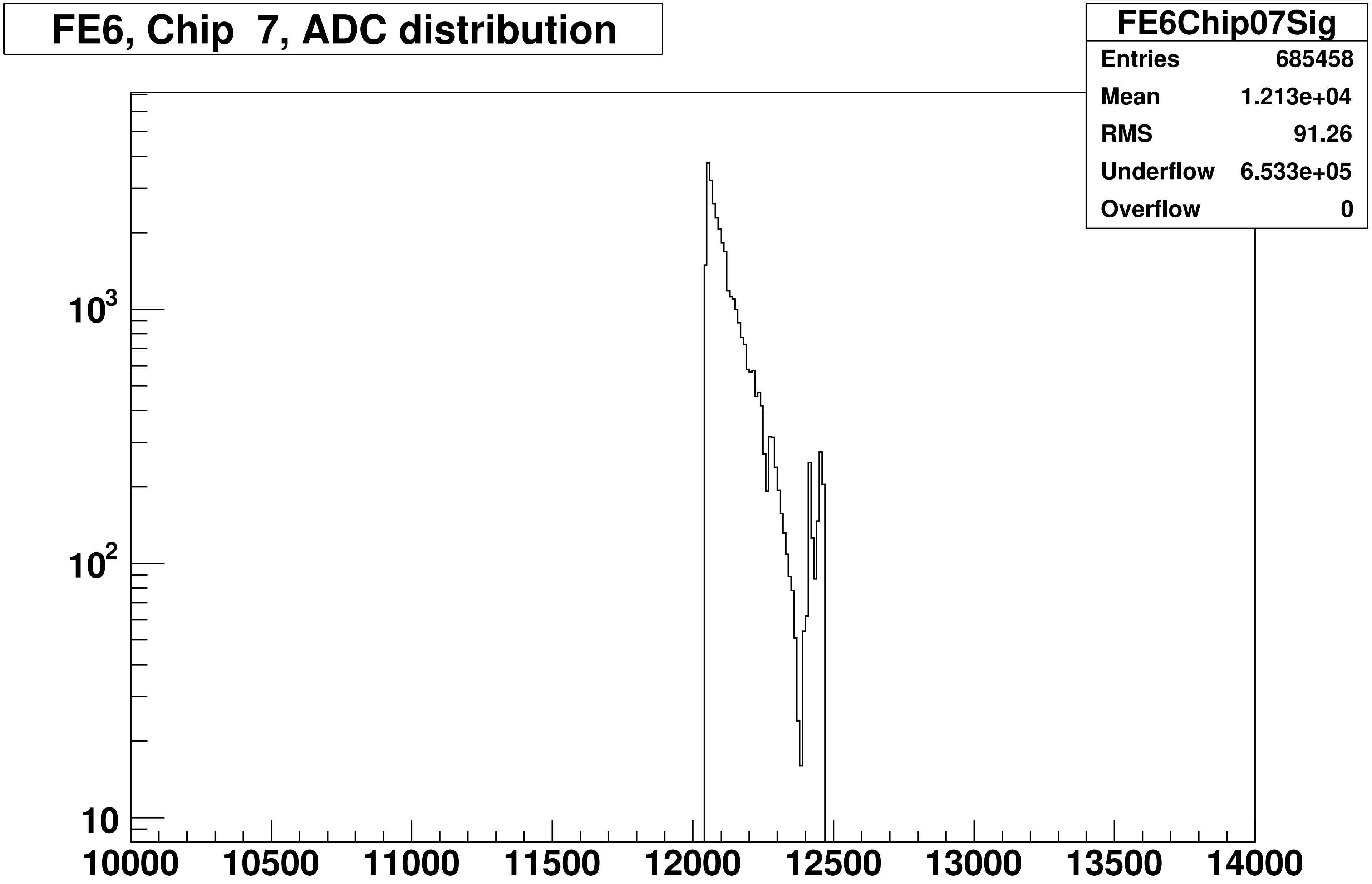
50
100
150
200


FE6, Chip 6, ADC distribution
FE6Chip06Sig
Entries 685458
Mean 1.224e+04
RMS 91.85
Underflow 6.533e+05
Overflow 0
10^3
10^2
10000
10500
11000
11500
12000
12500
13000
13500
14000



FE6, Chip 7, ADC distribution
FE6Chip07All
Entries 685458
Mean 537.2
RMS 2575
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
-5000
0
5000
10000
15000
20000
25000


FE6, Chip 7, ADC distribution
FE6Chip07Ped
Entries 685458
Mean -34.41
RMS 1.408
Underflow 0
Overflow 3.22e+04
10^6
10^5
10^4
10^3
10^2
10
-200
-150
-100
-50
0
50
100
150
200


FE6, Chip 7, ADC distribution
FE6Chip07Sig
Entries 685458
Mean 1.213e+04
RMS 91.26
Underflow 6.533e+05
Overflow 0
10
10^2
10^3
10000
10500
11000
11500
12000
12500
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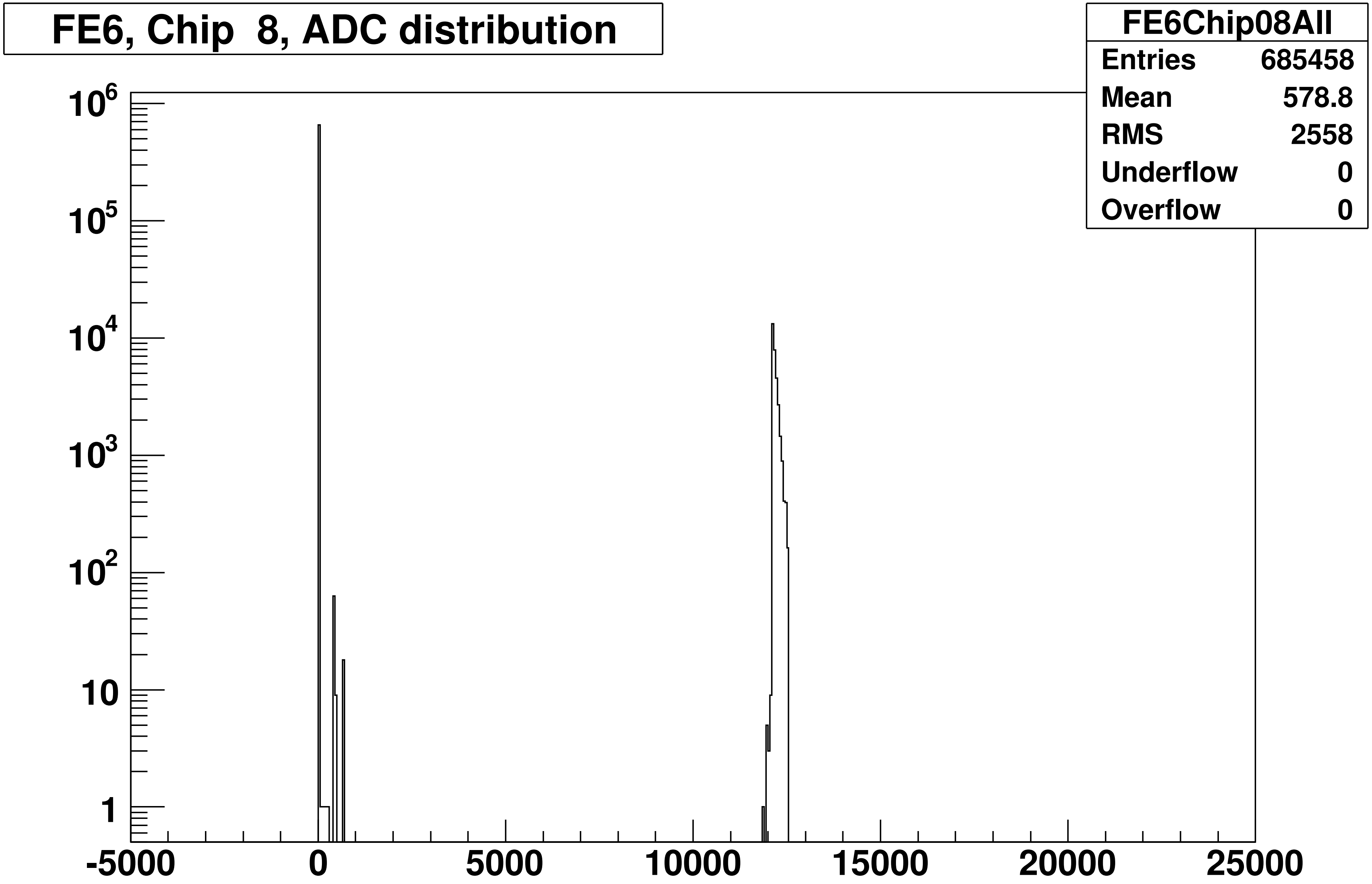
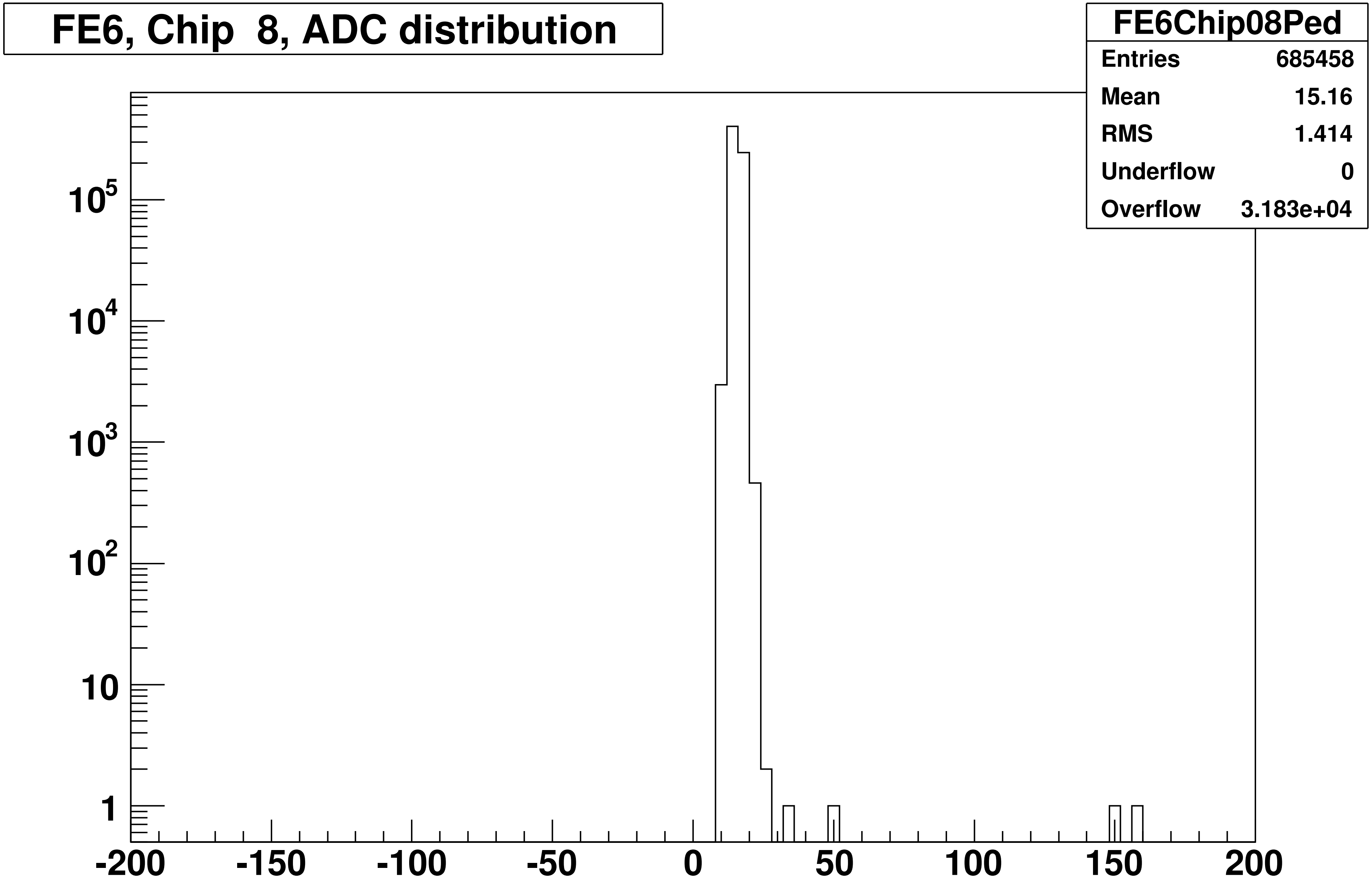


FE6, Chip 8, ADC distribution
FE6Chip08All
Entries 685458
Mean 578.8
RMS 2558
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE6, Chip 8, ADC distribution
FE6Chip08Ped
Entries 685458
Mean 15.16
RMS 1.414
Underflow 0
Overflow 3.183e+04
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10^4
10^3
10^2
10
1
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-150
-100
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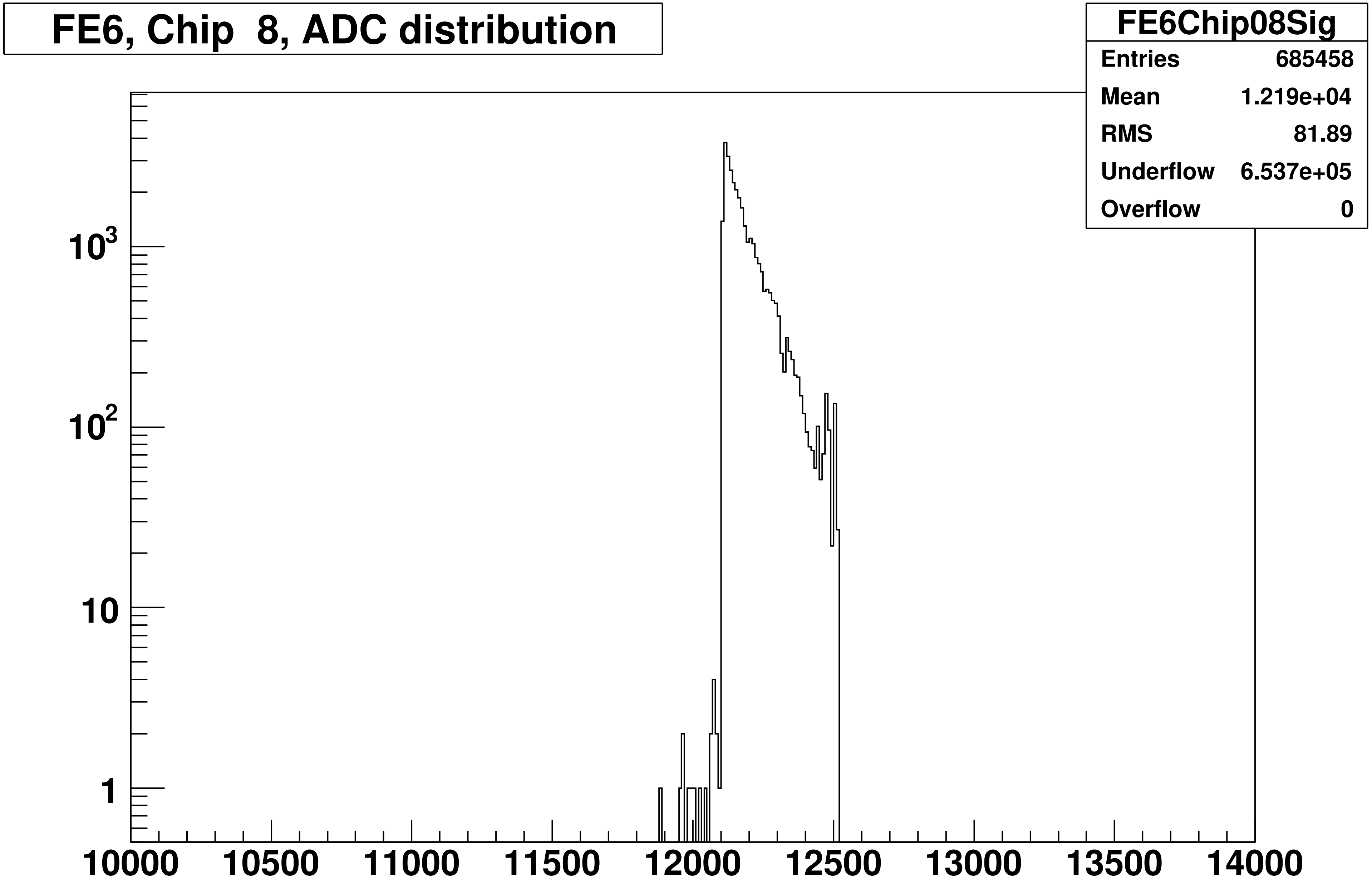
0
50
100
150
200



FE6, Chip 8, ADC distribution
FE6Chip08Sig
Entries 685458
Mean 1.219e+04
RMS 81.89
Underflow 6.537e+05
Overflow 0
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10^2
10
1
10000
10500
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11500
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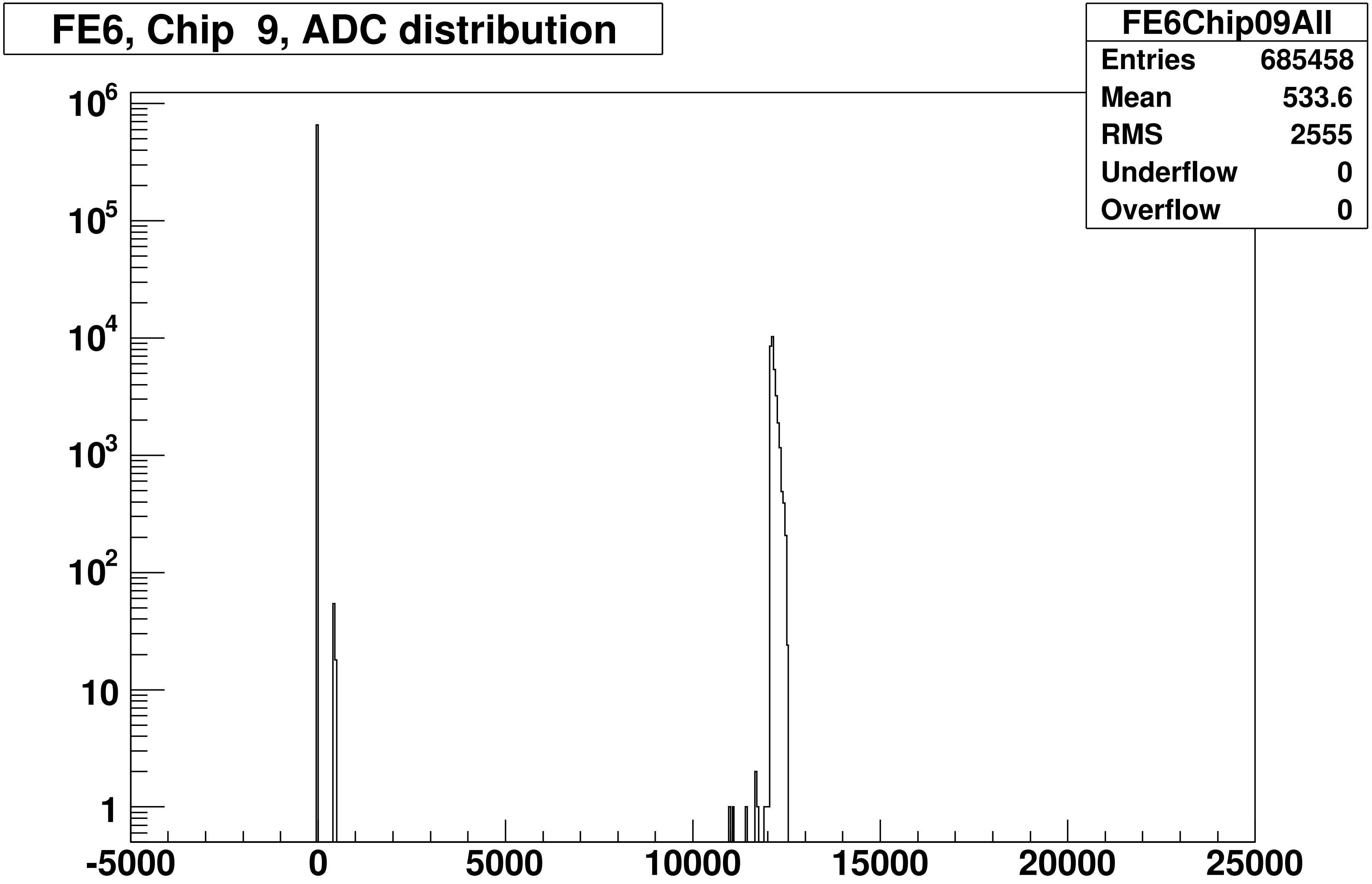
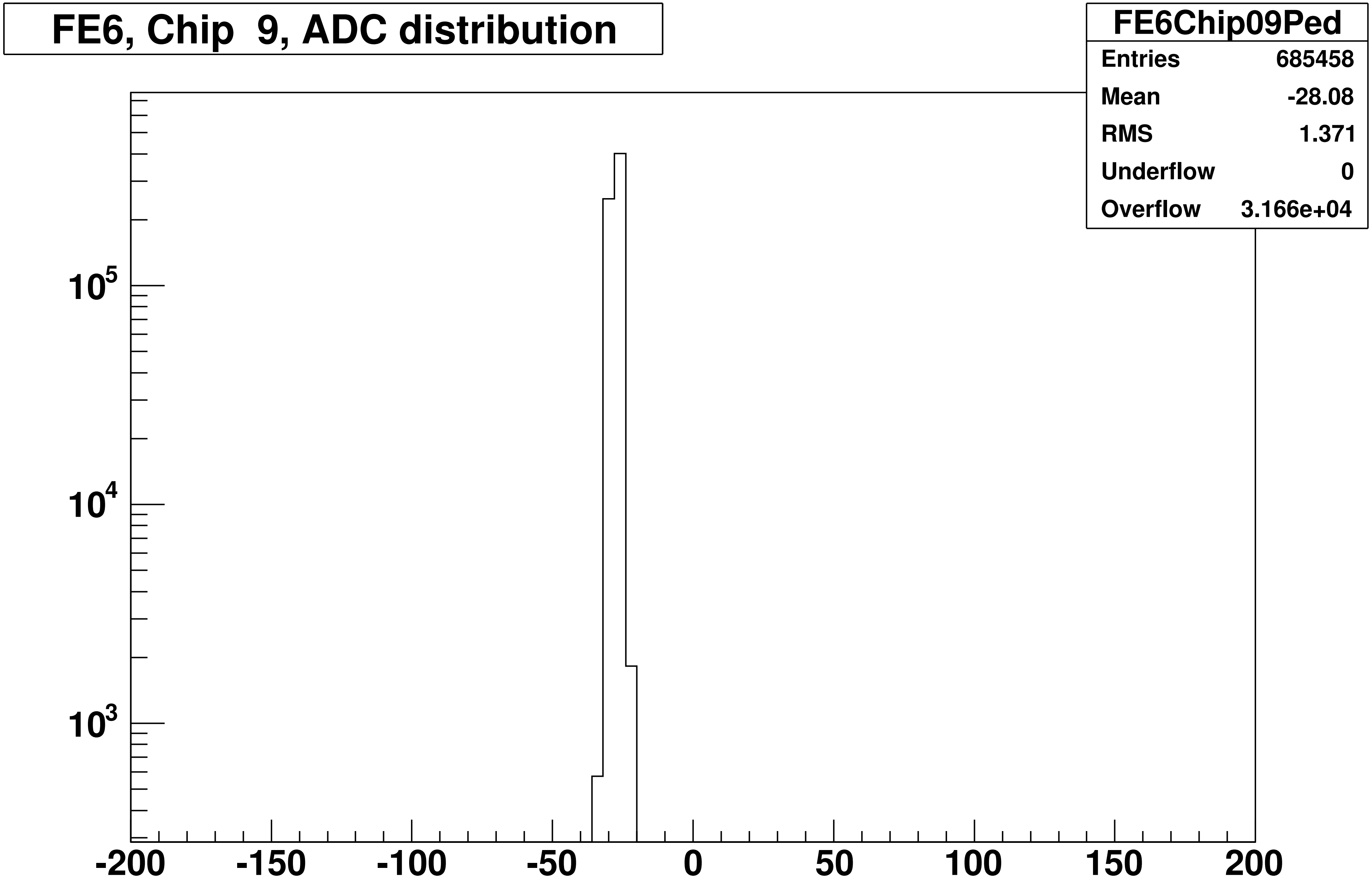
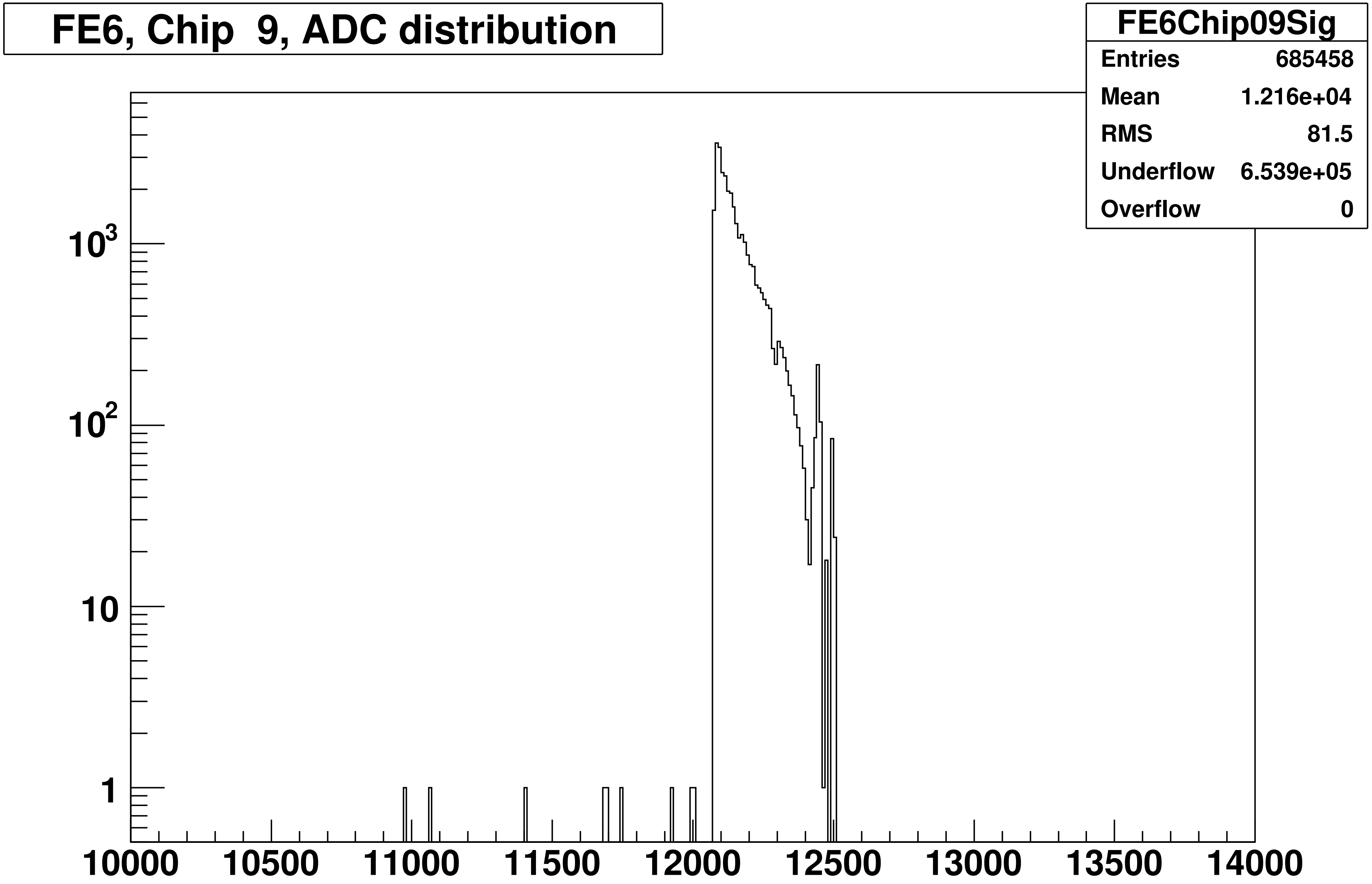


FE6, Chip 9, ADC distribution
FE6Chip09All
Entries 685458
Mean 533.6
RMS 2555
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE6, Chip 9, ADC distribution
FE6Chip09Ped
Entries 685458
Mean -28.08
RMS 1.371
Underflow 0
Overflow 3.166e+04
10^5
10^4
10^3
-200
-150
-100
-50
0
50
100
150
200



FE6, Chip 9, ADC distribution
FE6Chip09Sig
Entries 685458
Mean 1.216e+04
RMS 81.5
Underflow 6.539e+05
Overflow 0
10^3
10^2
10
1
10000
10500
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11500
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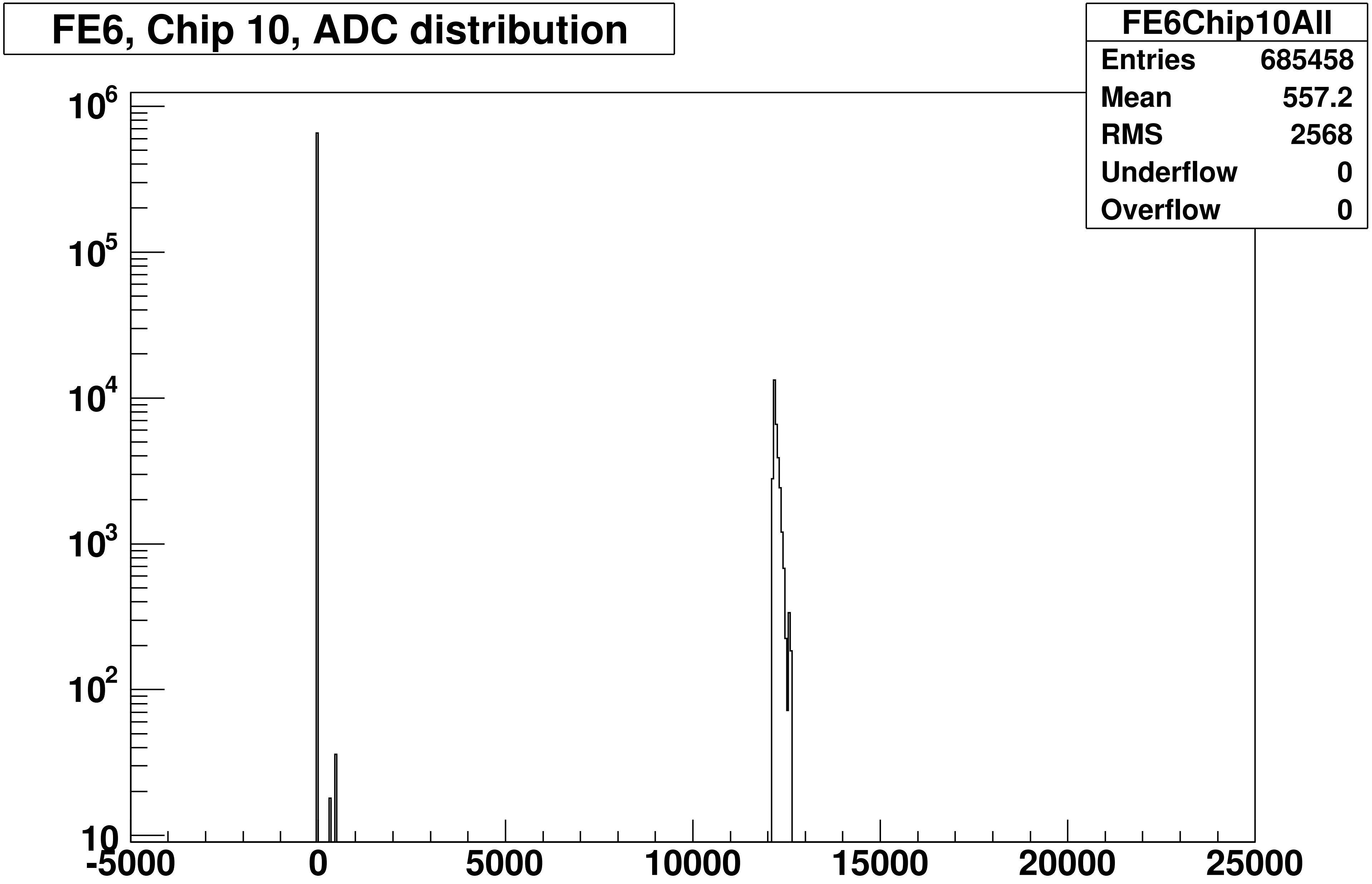
FE6, Chip 10, ADC distribution
FE6Chip10All
Entries 685458
Mean 557.2
RMS 2568
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
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-5000
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10000
15000
20000
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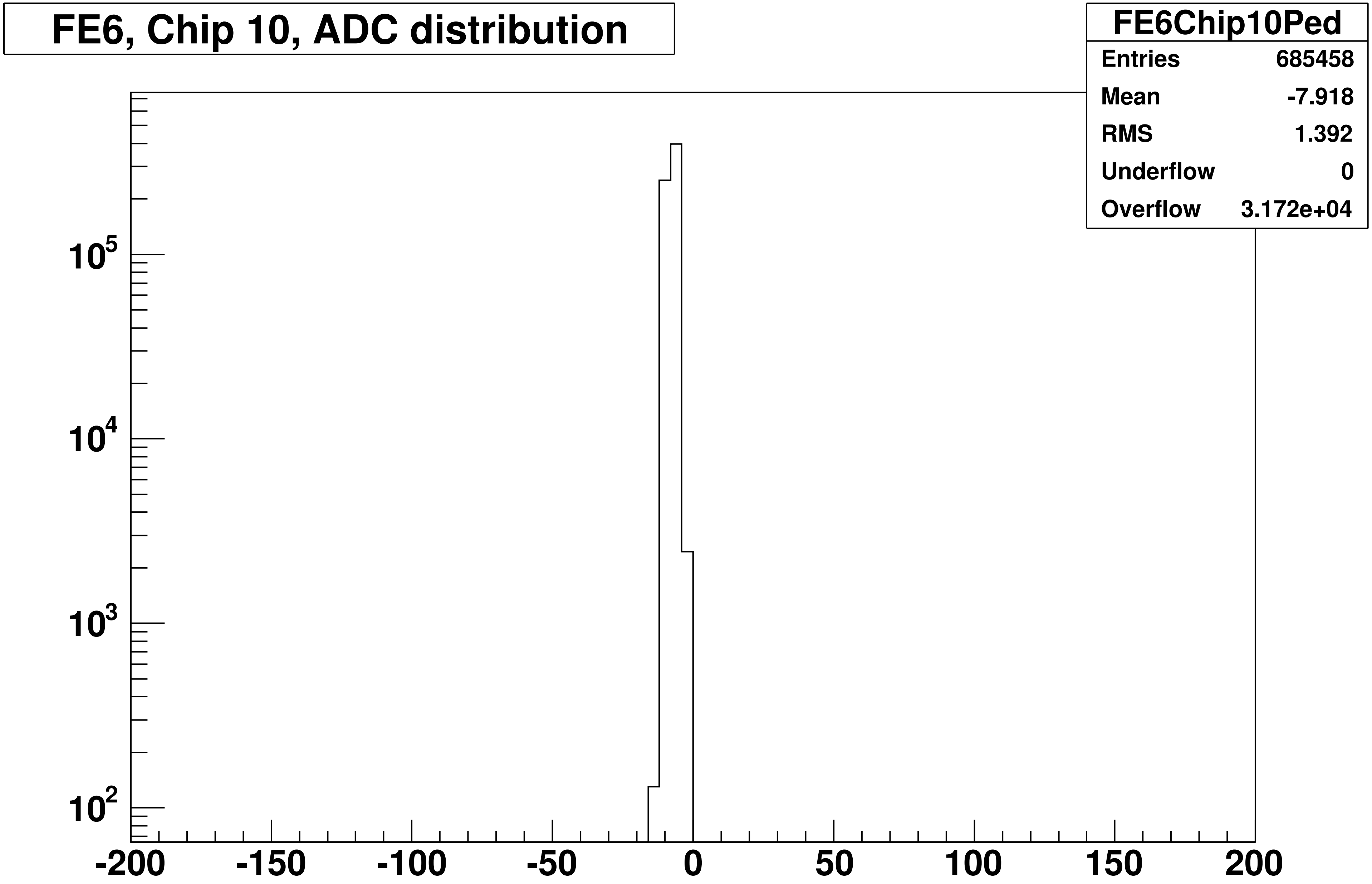
FE6, Chip 10, ADC distribution
FE6Chip10Ped
Entries 685458
Mean -7.918
RMS 1.392
Underflow 0
Overflow 3.172e+04
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10^4
10^3
10^2
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-100
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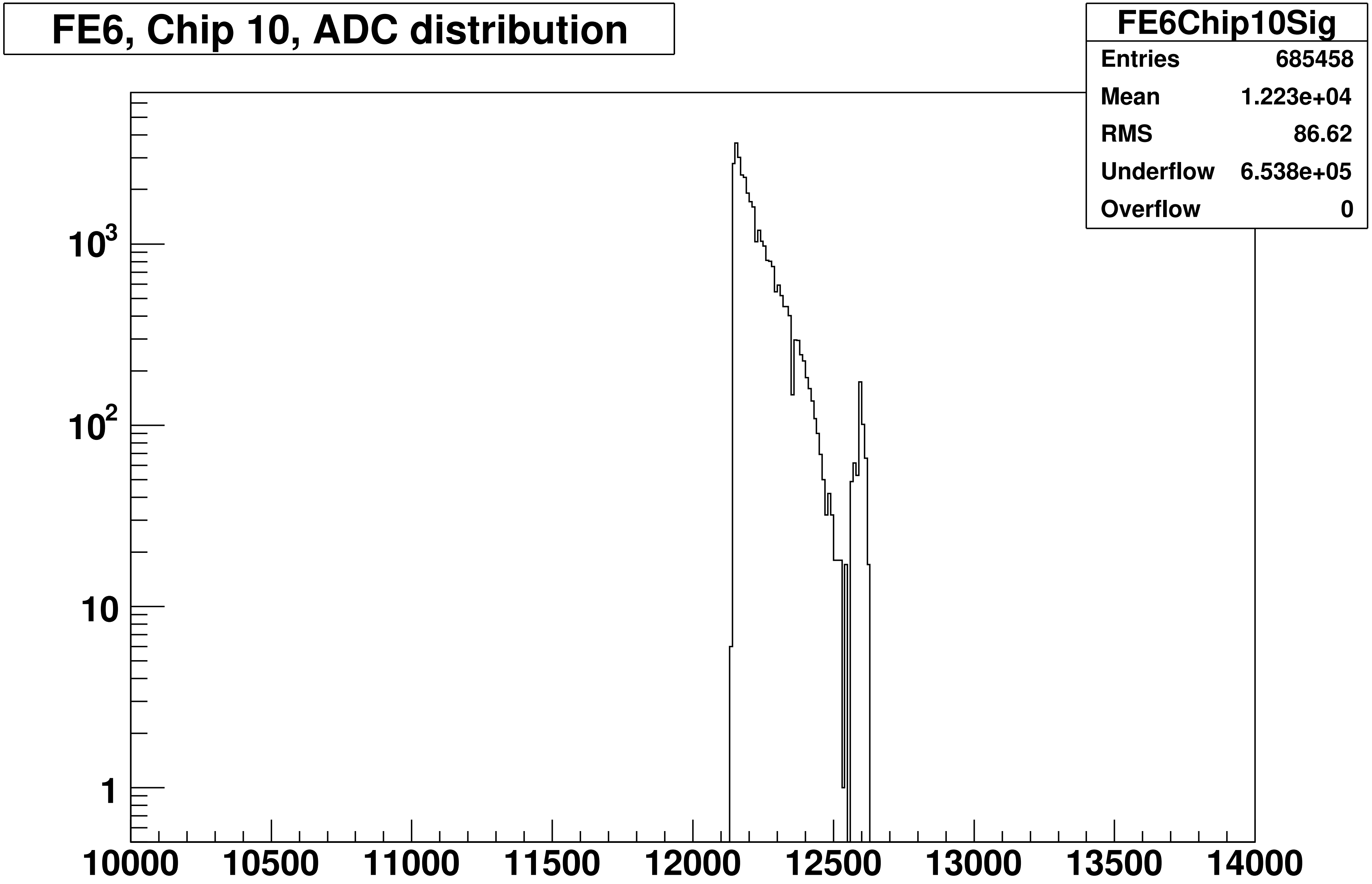
0
50
100
150
200



FE6, Chip 10, ADC distribution
FE6Chip10Sig
Entries 685458
Mean 1.223e+04
RMS 86.62
Underflow 6.538e+05
Overflow 0
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10^2
10
1
10000
10500
11000
11500
12000
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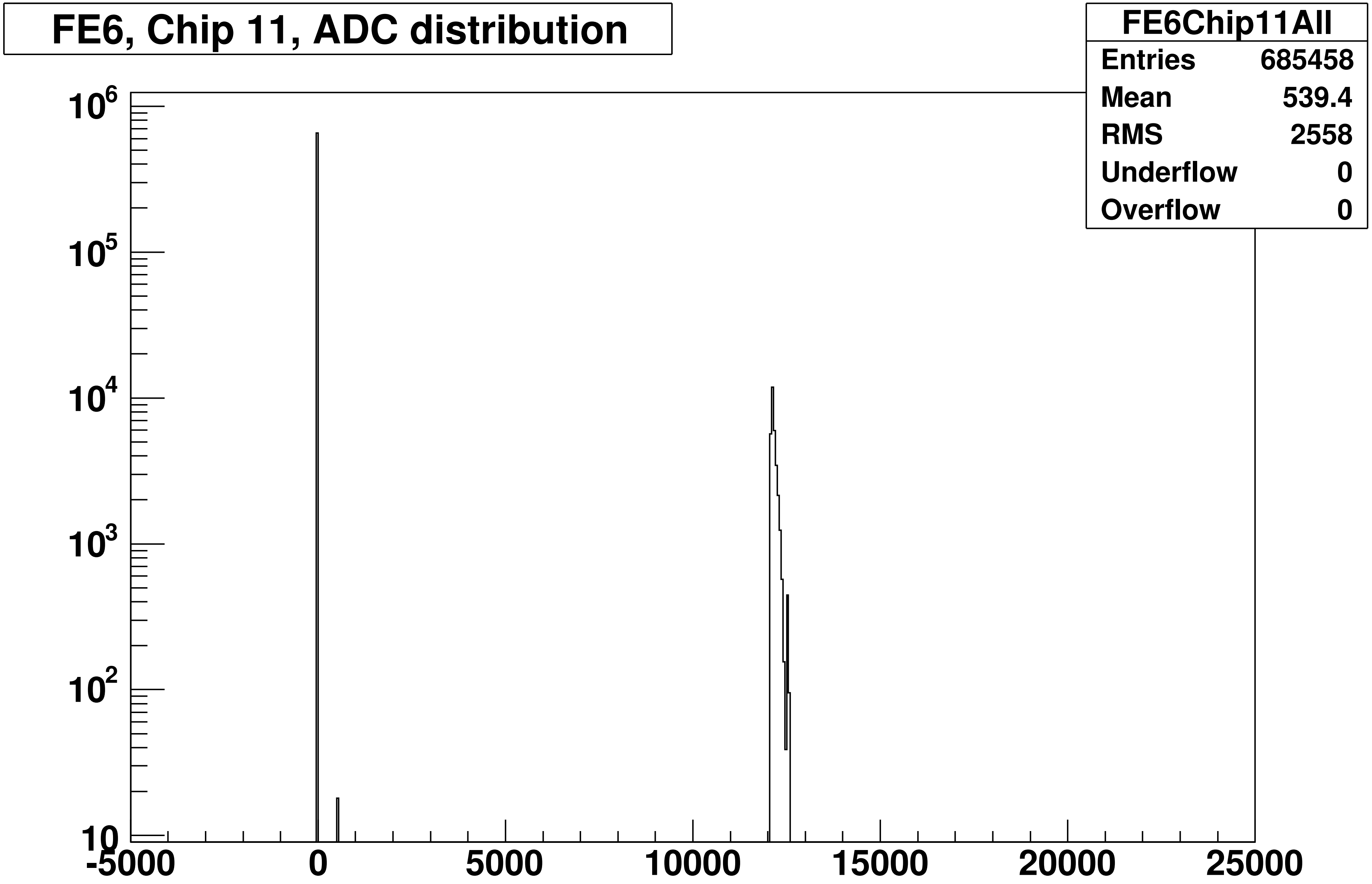
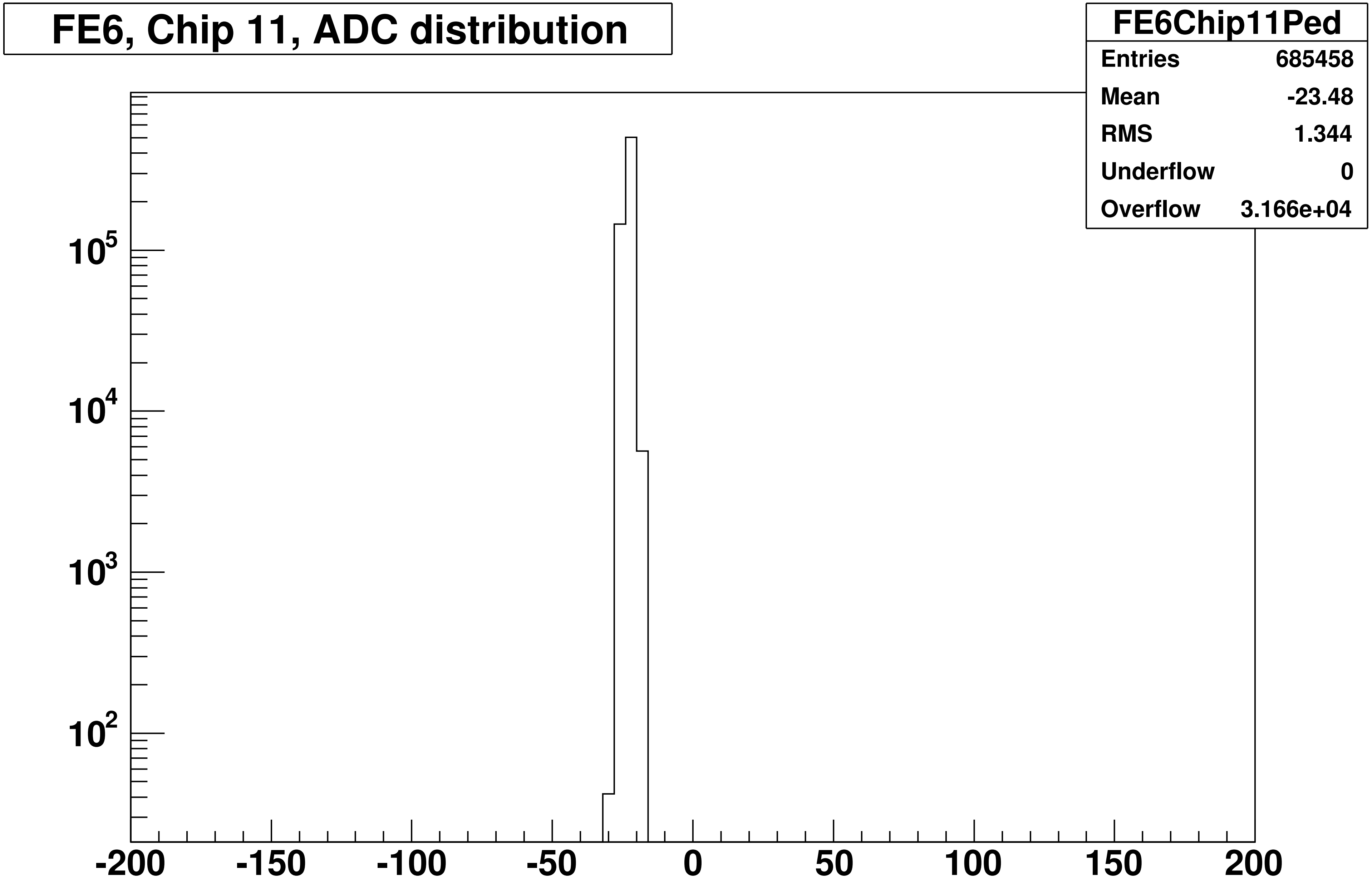

FE6, Chip 11, ADC distribution
FE6Chip11All
Entries 685458
Mean 539.4
RMS 2558
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000



FE6, Chip 11, ADC distribution
FE6Chip11Ped
Entries 685458
Mean -23.48
RMS 1.344
Underflow 0
Overflow 3.166e+04
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10^4
10^3
10^2
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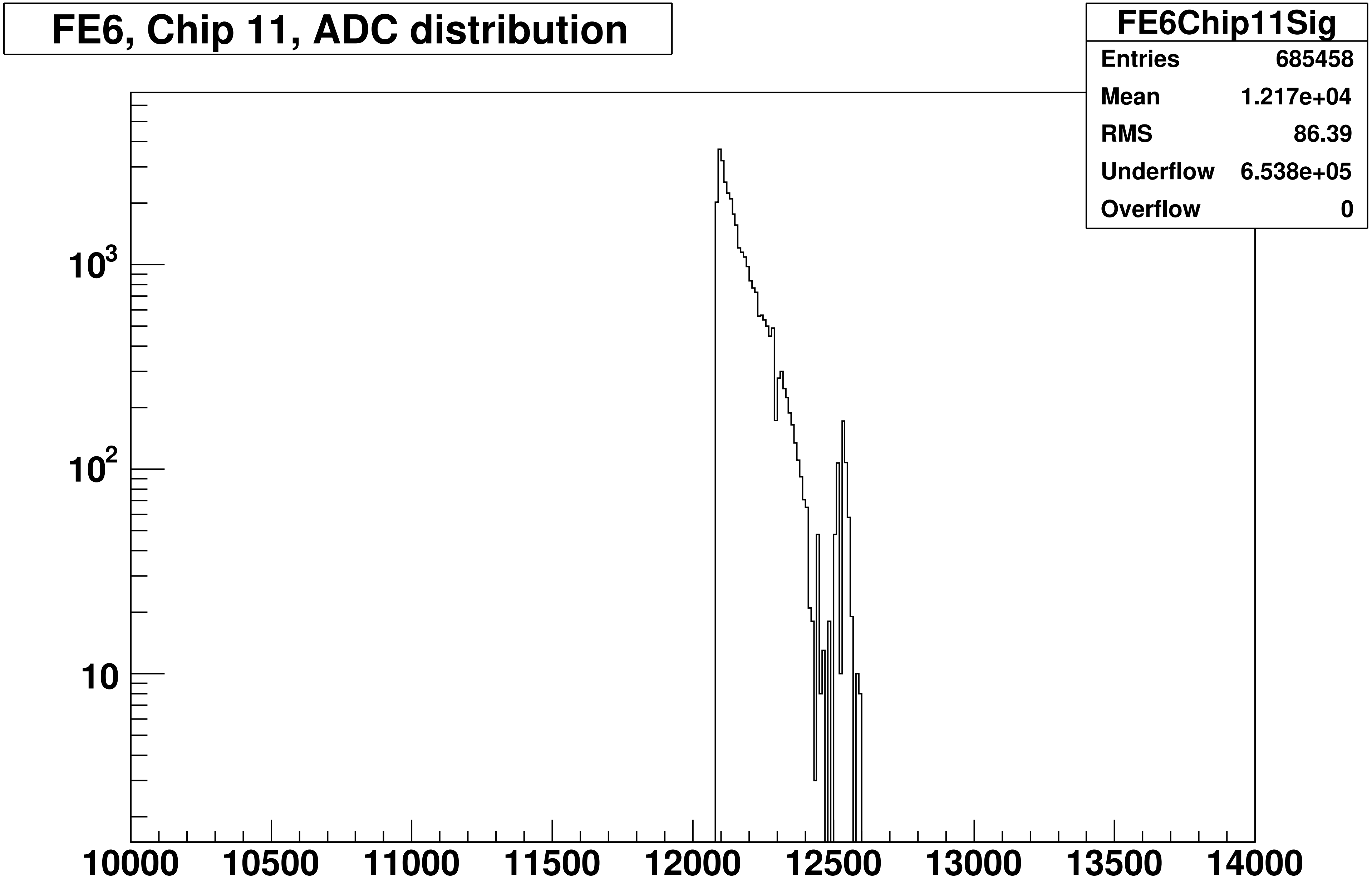

FE6, Chip 11, ADC distribution
FE6Chip11Sig
Entries 685458
Mean 1.217e+04
RMS 86.39
Underflow 6.538e+05
Overflow 0
10^3
10^2
10
10000
10500
11000
11500
12000
12500
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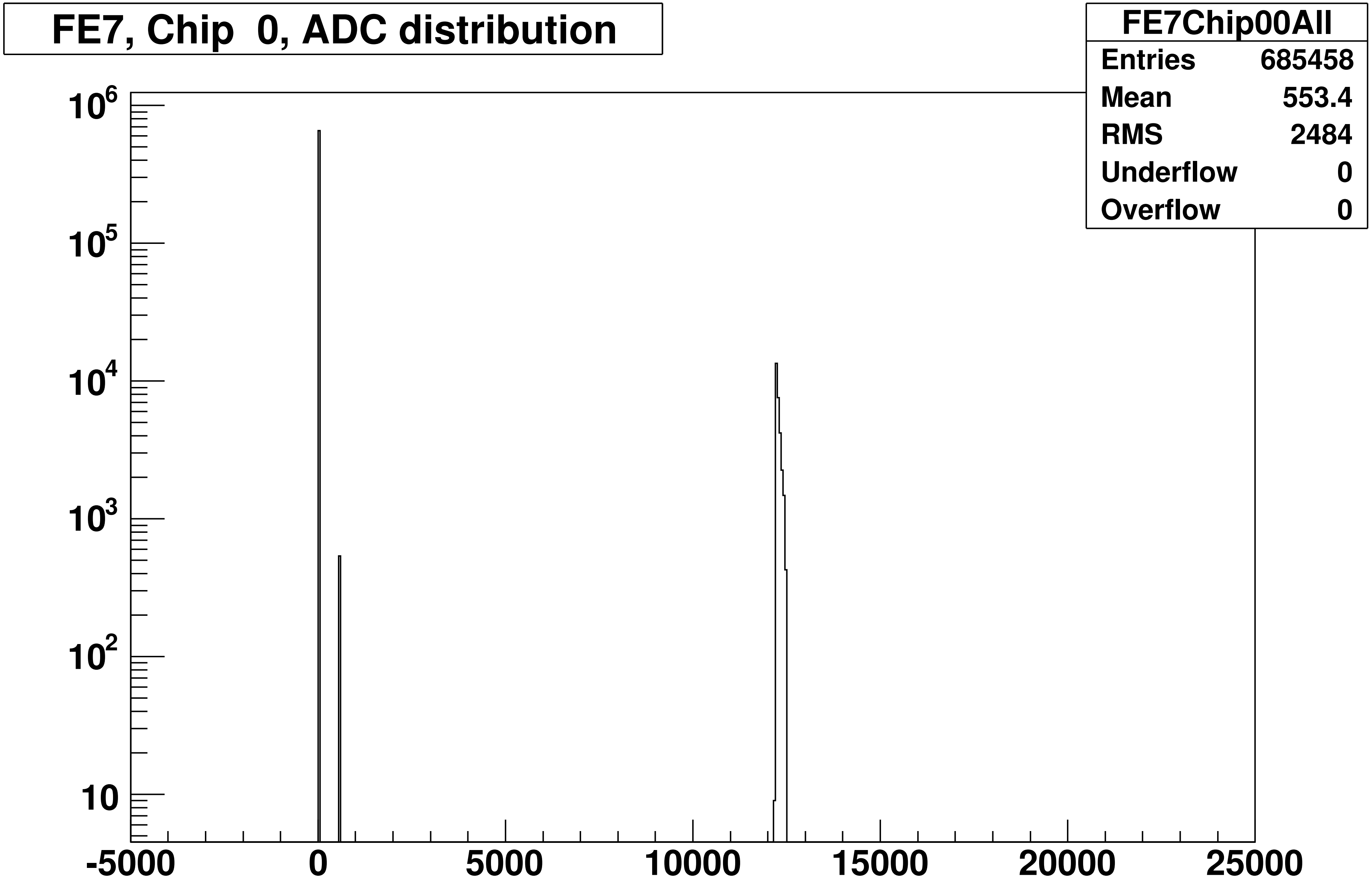
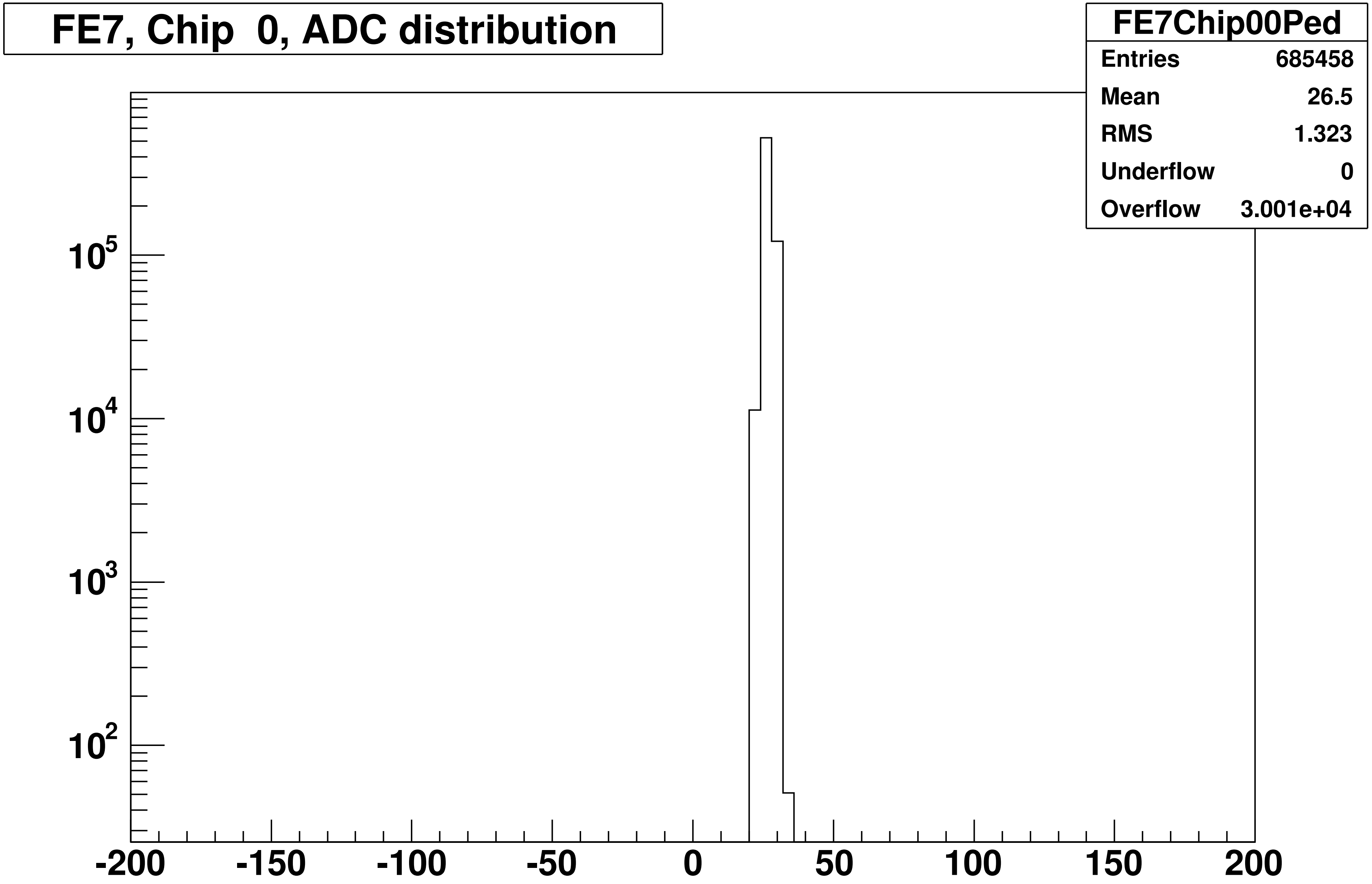

FE7, Chip 0, ADC distribution
FE7Chip00All
Entries 685458
Mean 553.4
RMS 2484
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE7, Chip 0, ADC distribution
FE7Chip00Ped
Entries 685458
Mean 26.5
RMS 1.323
Underflow 0
Overflow 3.001e+04
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10^4
10^3
10^2
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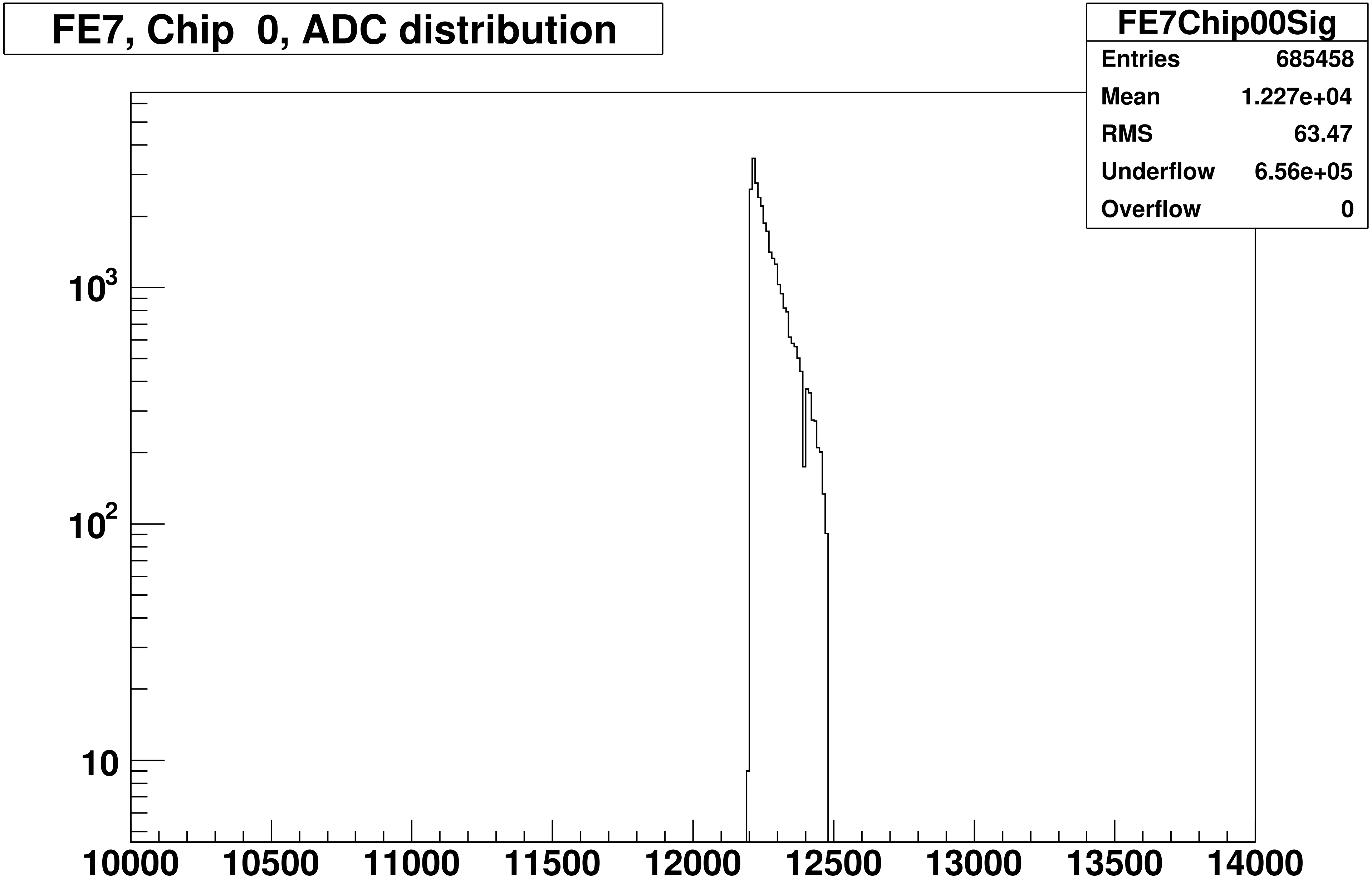
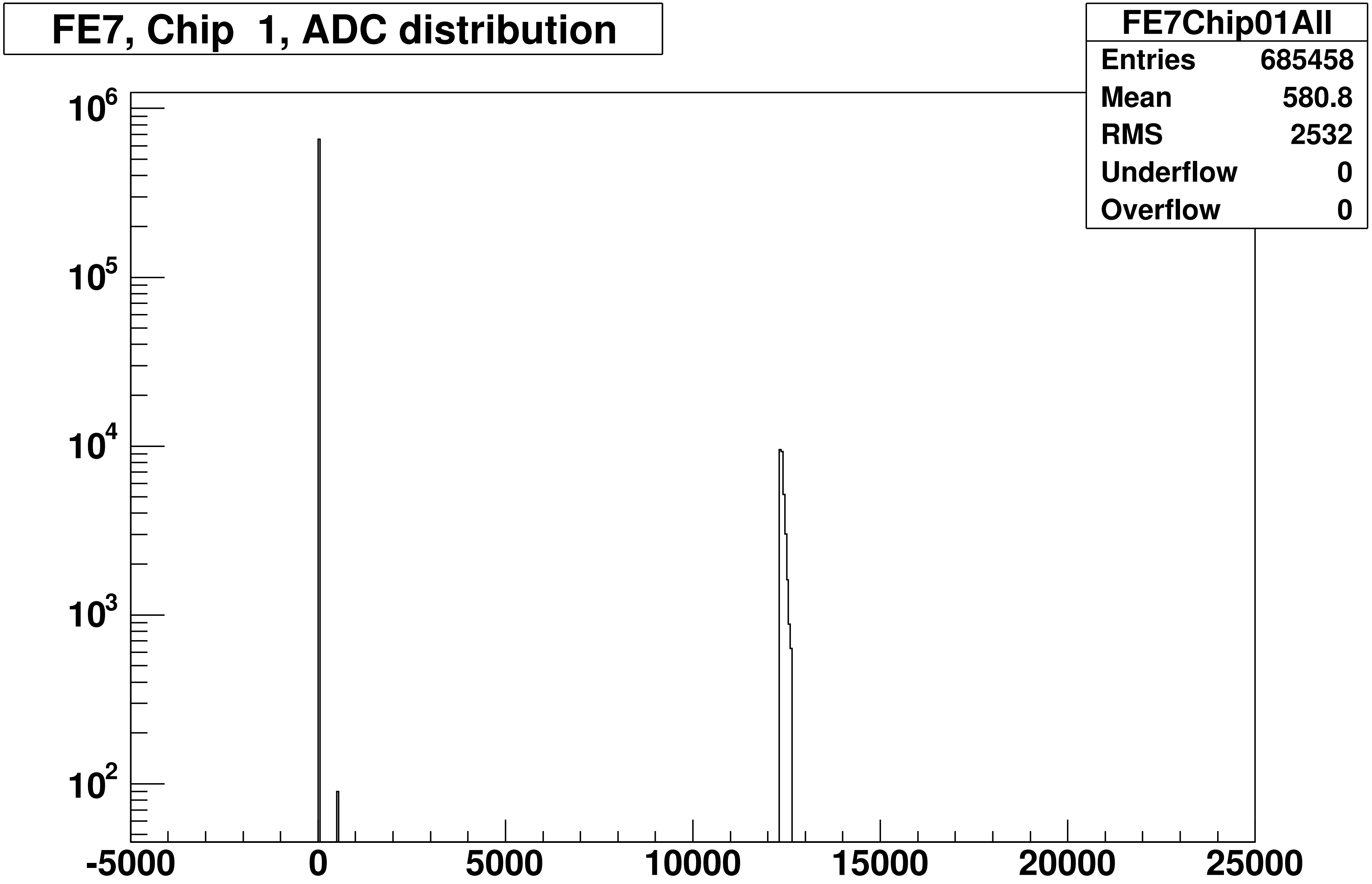
-100
-50
0
50
100
150
200



FE7, Chip 0, ADC distribution
FE7Chip00Sig
Entries 685458
Mean 1.227e+04
RMS 63.47
Underflow 6.56e+05
Overflow 0
10
10^2
10^3
10000
10500
11000
11500
12000
12500
13000
13500
14000



FE7, Chip 1, ADC distribution
FE7Chip01All
Entries 685458
Mean 580.8
RMS 2532
Underflow 0
Overflow 0
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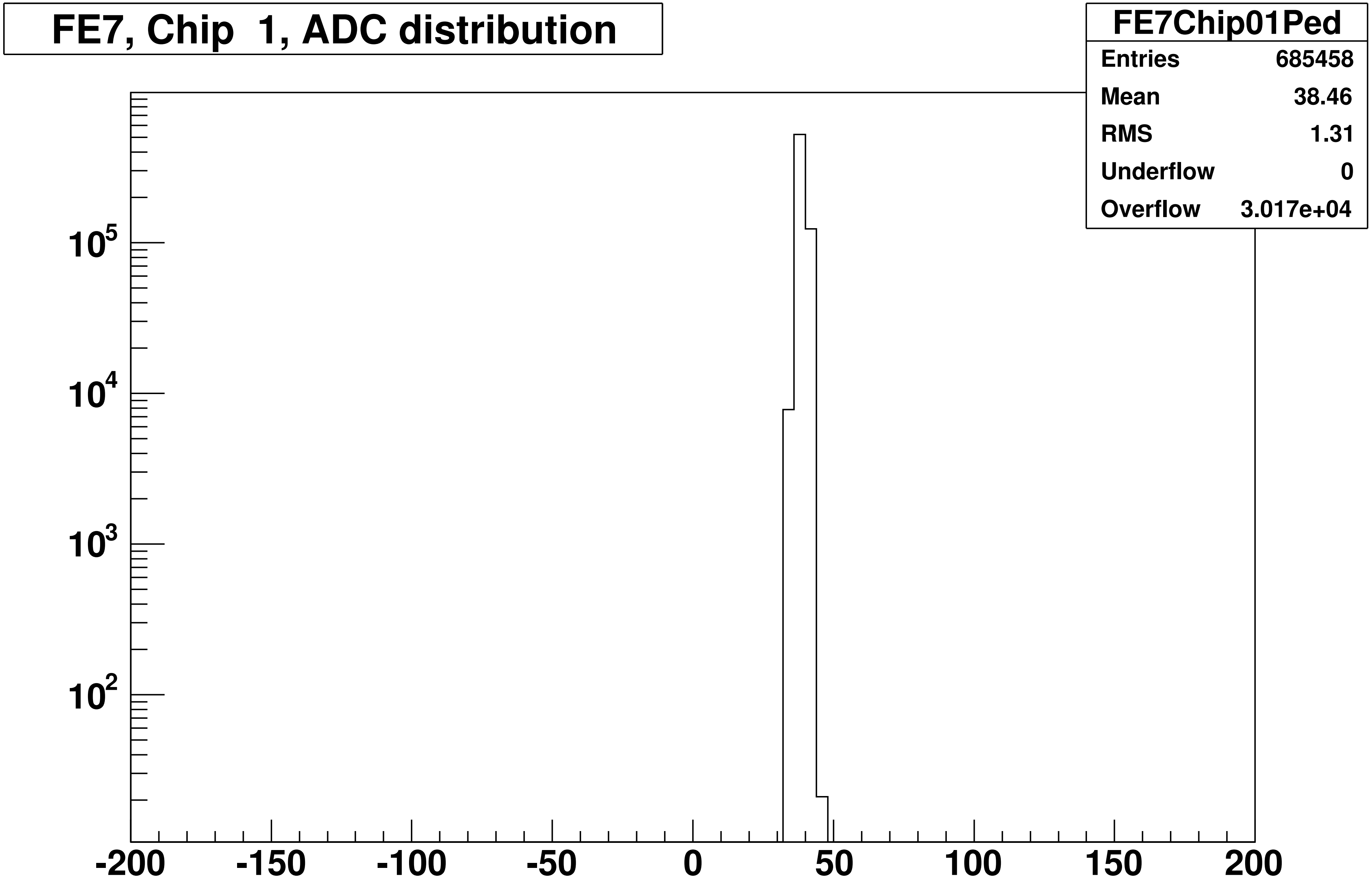
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000



FE7, Chip 1, ADC distribution
FE7Chip01Ped
Entries 685458
Mean 38.46
RMS 1.31
Underflow 0
Overflow 3.017e+04
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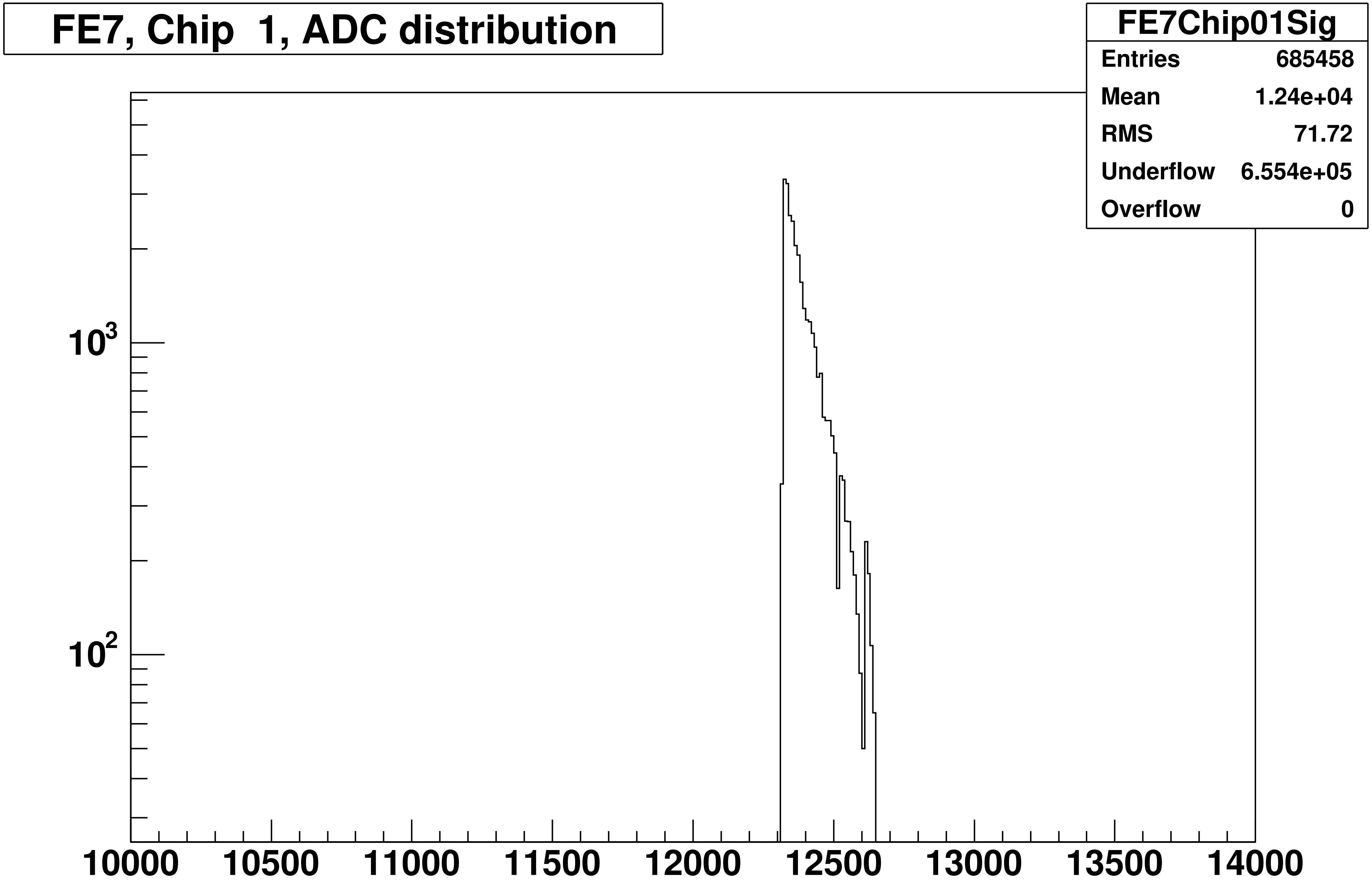
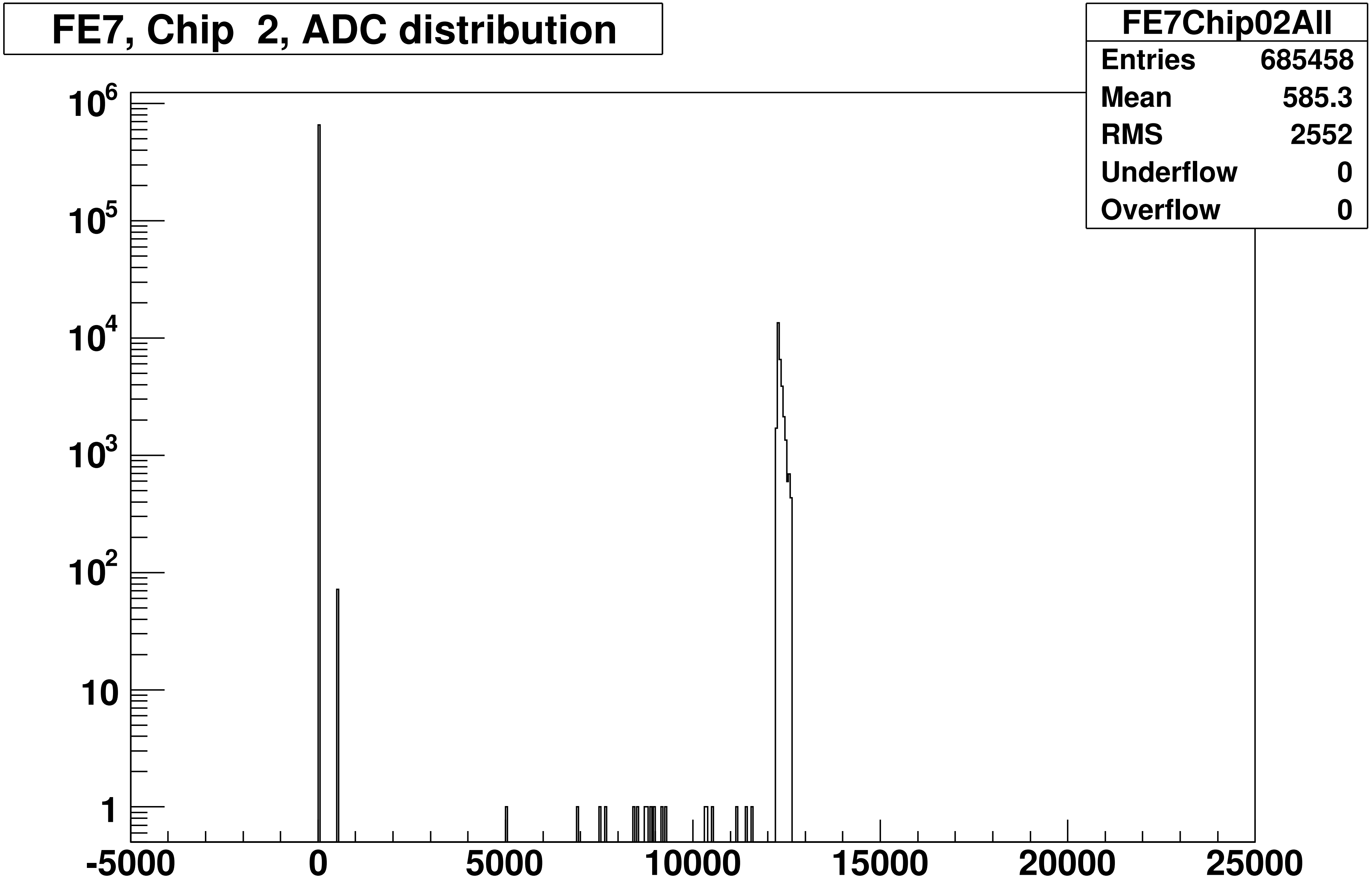
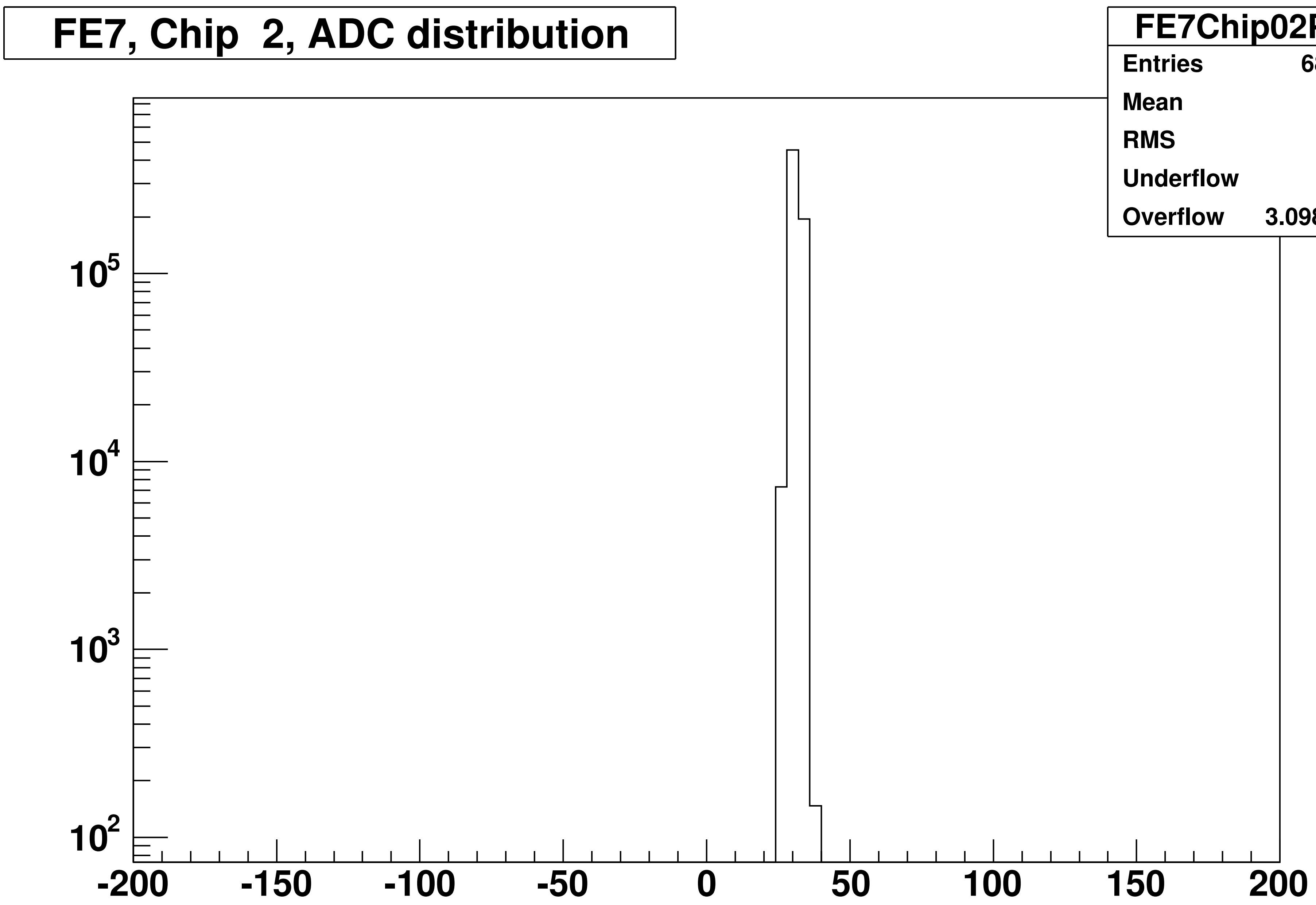
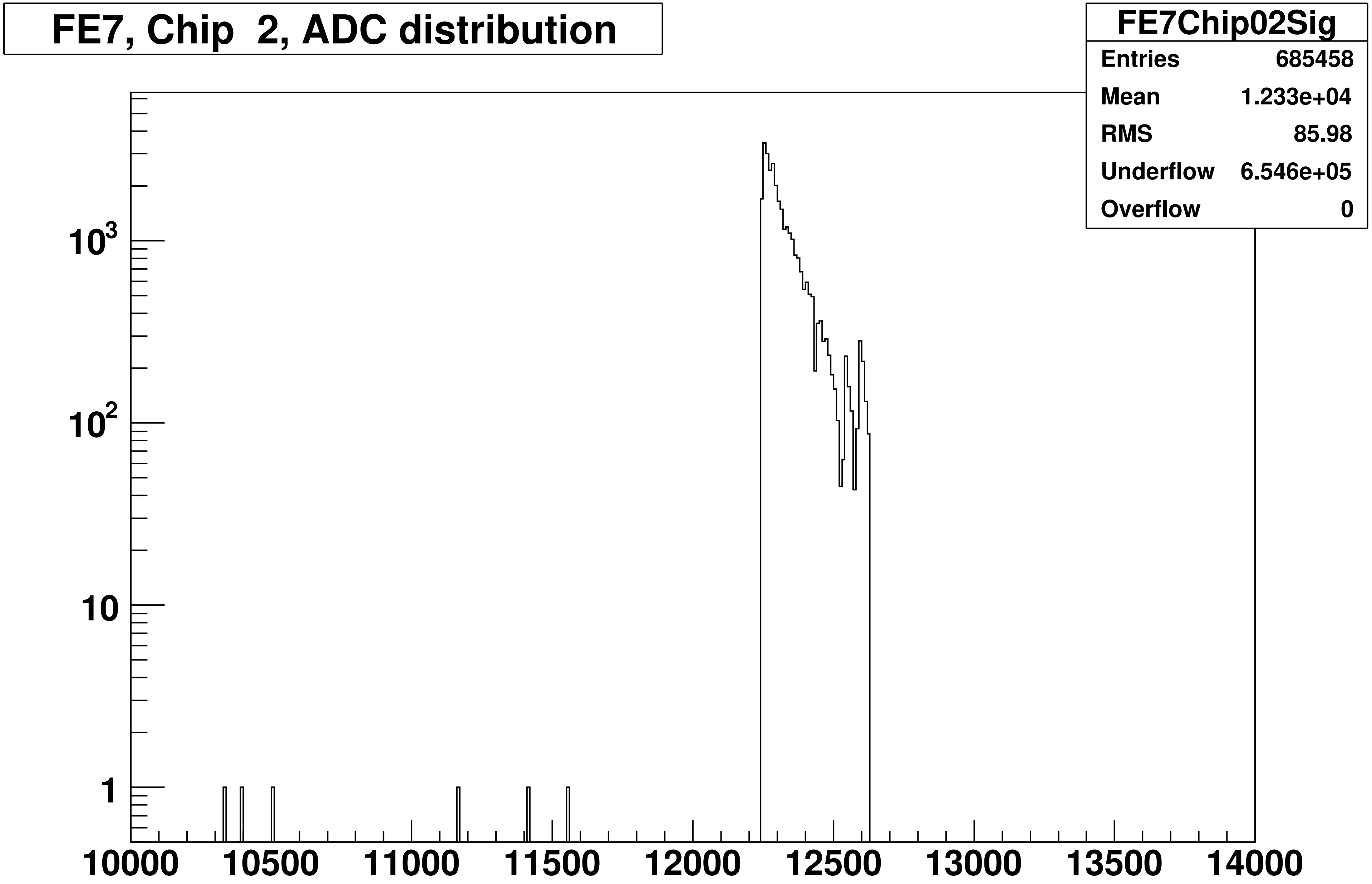
10^4
10^3
10^2
-200
-150
-100
-50
0
50
100
150
200



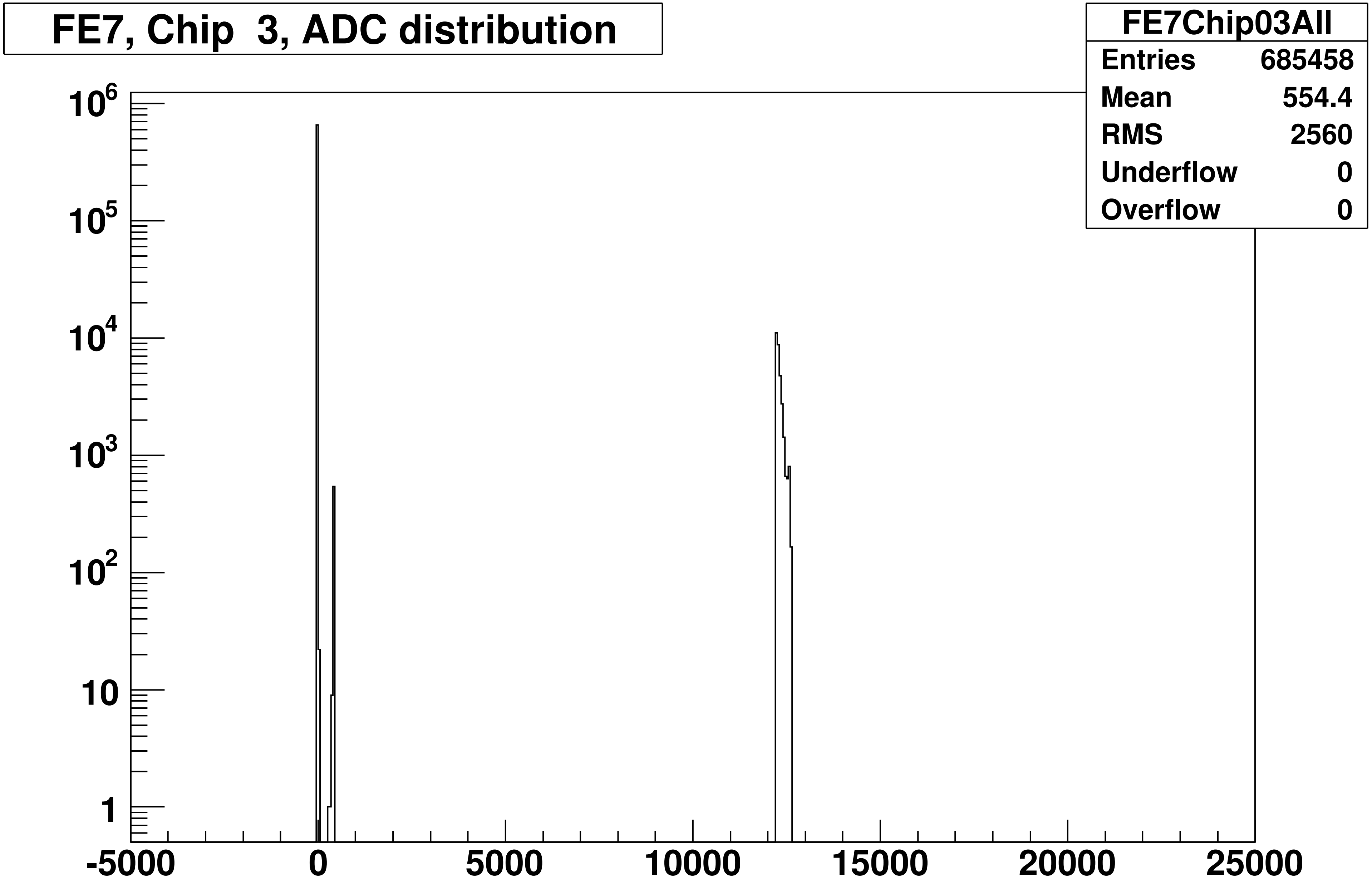
FE7, Chip 1, ADC distribution
FE7Chip01Sig
Entries 685458
Mean 1.24e+04
RMS 71.72
Underflow 6.554e+05
Overflow 0
10^3
10^2
10000
10500
11000
11500
12000
12500
13000
13500
14000

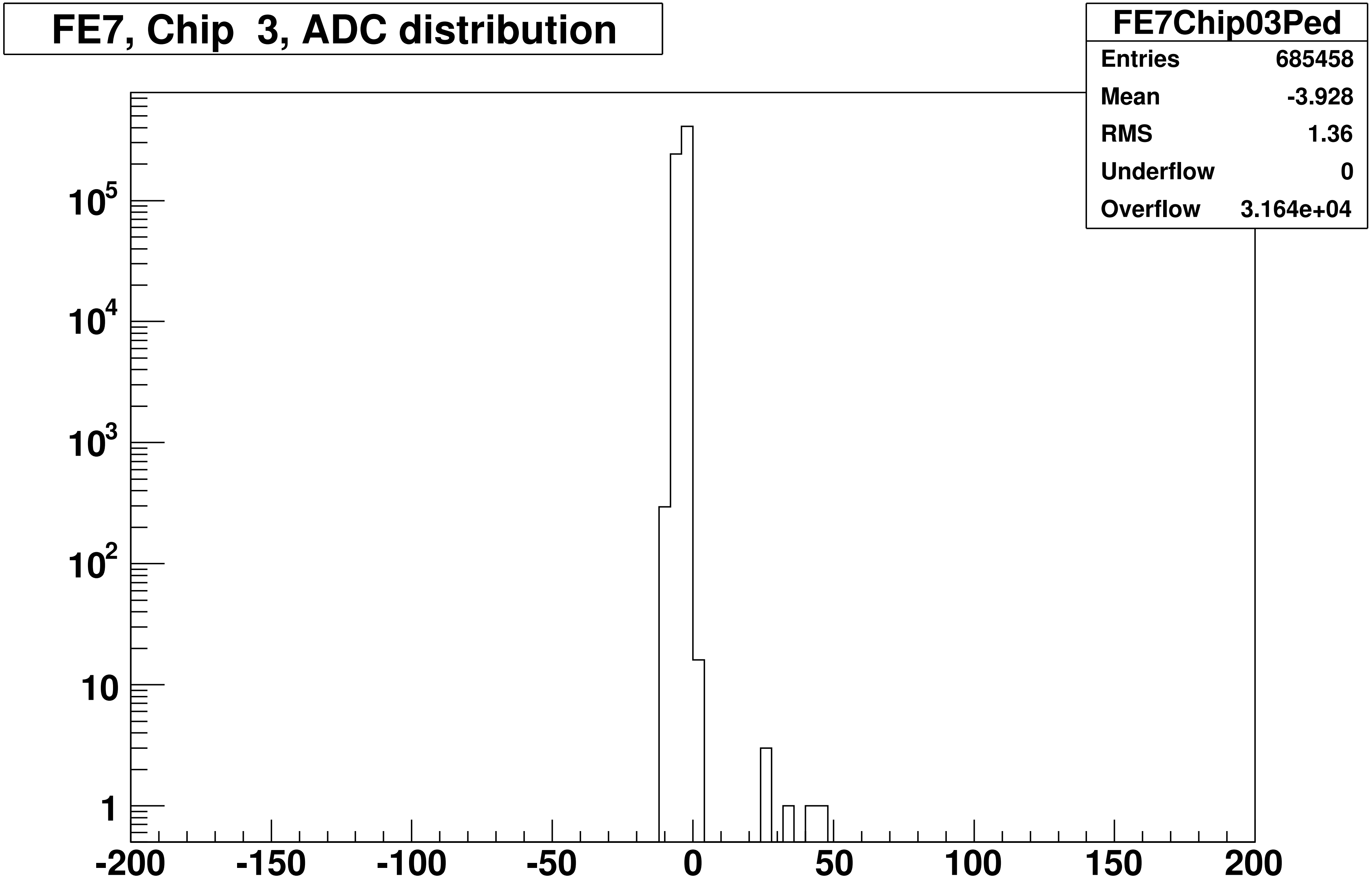

FE7, Chip 2, ADC distribution
FE7Chip02All
Entries 685458
Mean 585.3
RMS 2552
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE7, Chip 2, ADC distribution
FE7Chip02Ped
Entries 685458
Mean 30.76
RMS 1.412
Underflow 0
Overflow 3.098e+04
10^5
10^4
10^3
10^2
-200
-150
-100
-50
0
50
100
150
200



FE7, Chip 2, ADC distribution
FE7Chip02Sig
Entries 685458
Mean 1.233e+04
RMS 85.98
Underflow 6.546e+05
Overflow 0
10^3
10^2
10
1
10000
10500
11000
11500
12000
12500
13000
13500
14000


FE7, Chip 3, ADC distribution
FE7Chip03All
Entries 685458
Mean 554.4
RMS 2560
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE7, Chip 3, ADC distribution
FE7Chip03Ped
Entries 685458
Mean -3.928
RMS 1.36
Underflow 0
Overflow 3.164e+04
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10^4
10^3
10^2
10
1
-200
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-100
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0
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100
150
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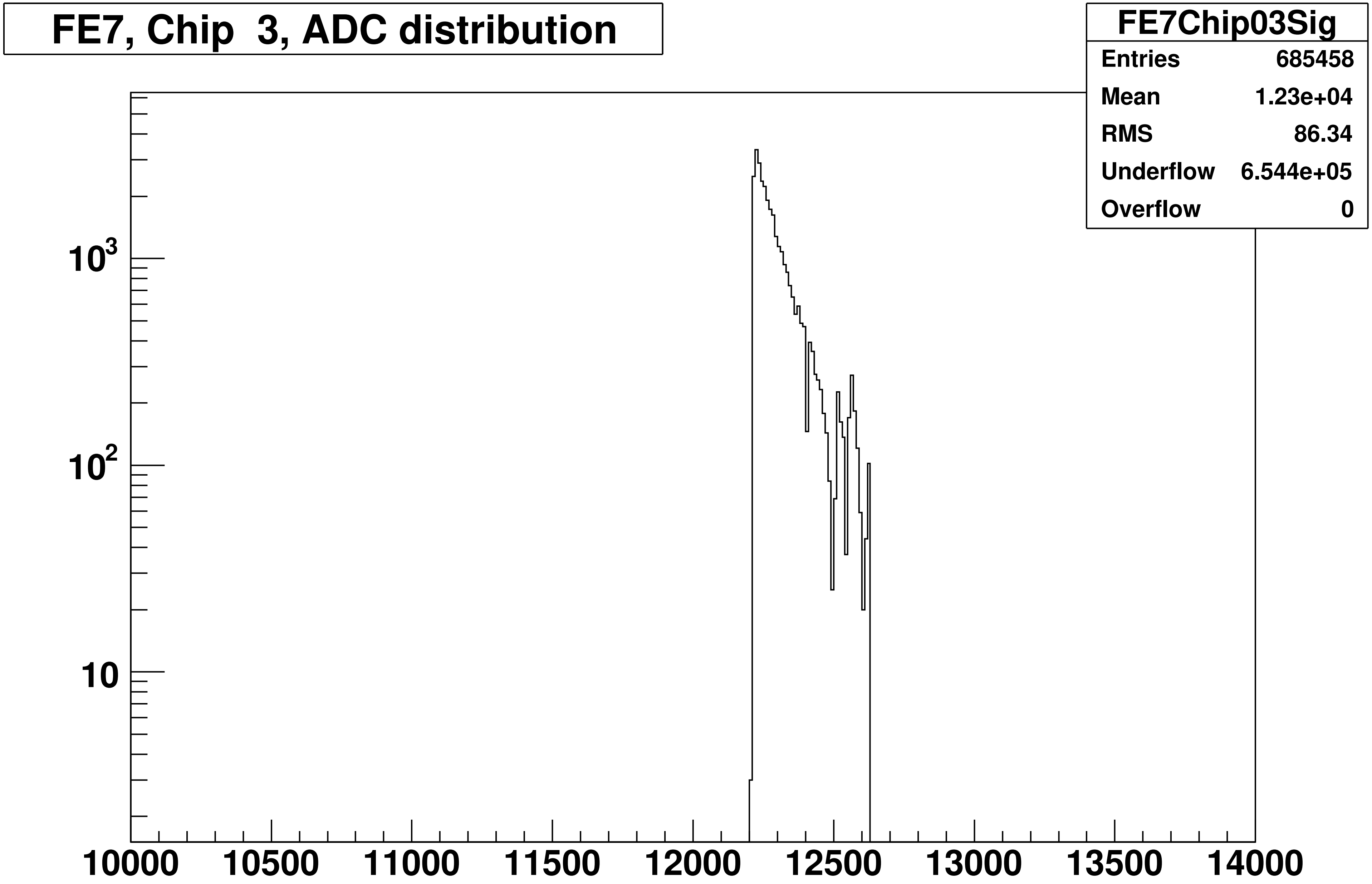
FE7, Chip 3, ADC distribution
FE7Chip03Sig
Entries 685458
Mean 1.23e+04
RMS 86.34
Underflow 6.544e+05
Overflow 0
10
10^2
10^3
10000
10500
11000
11500
12000
12500
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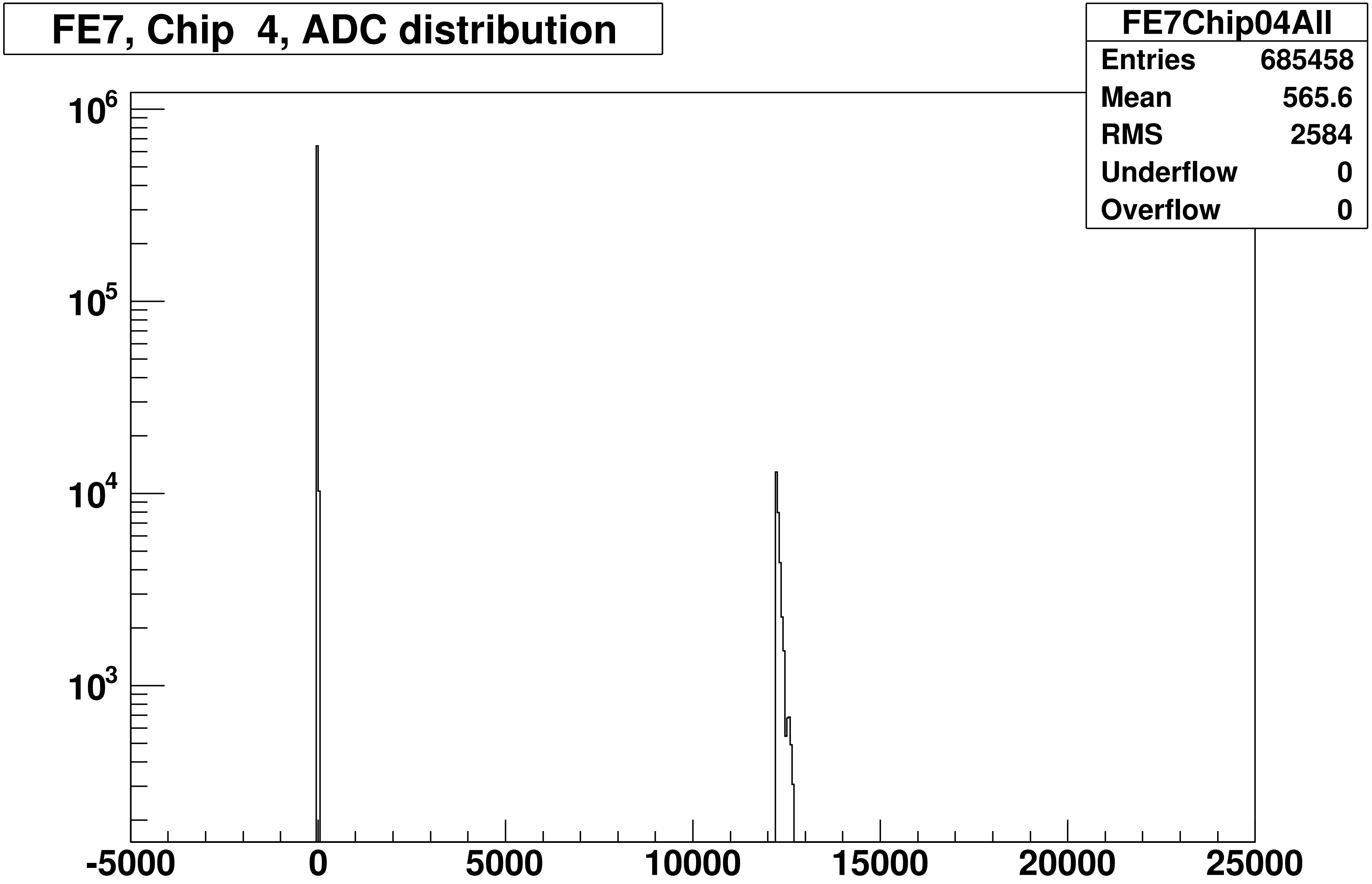
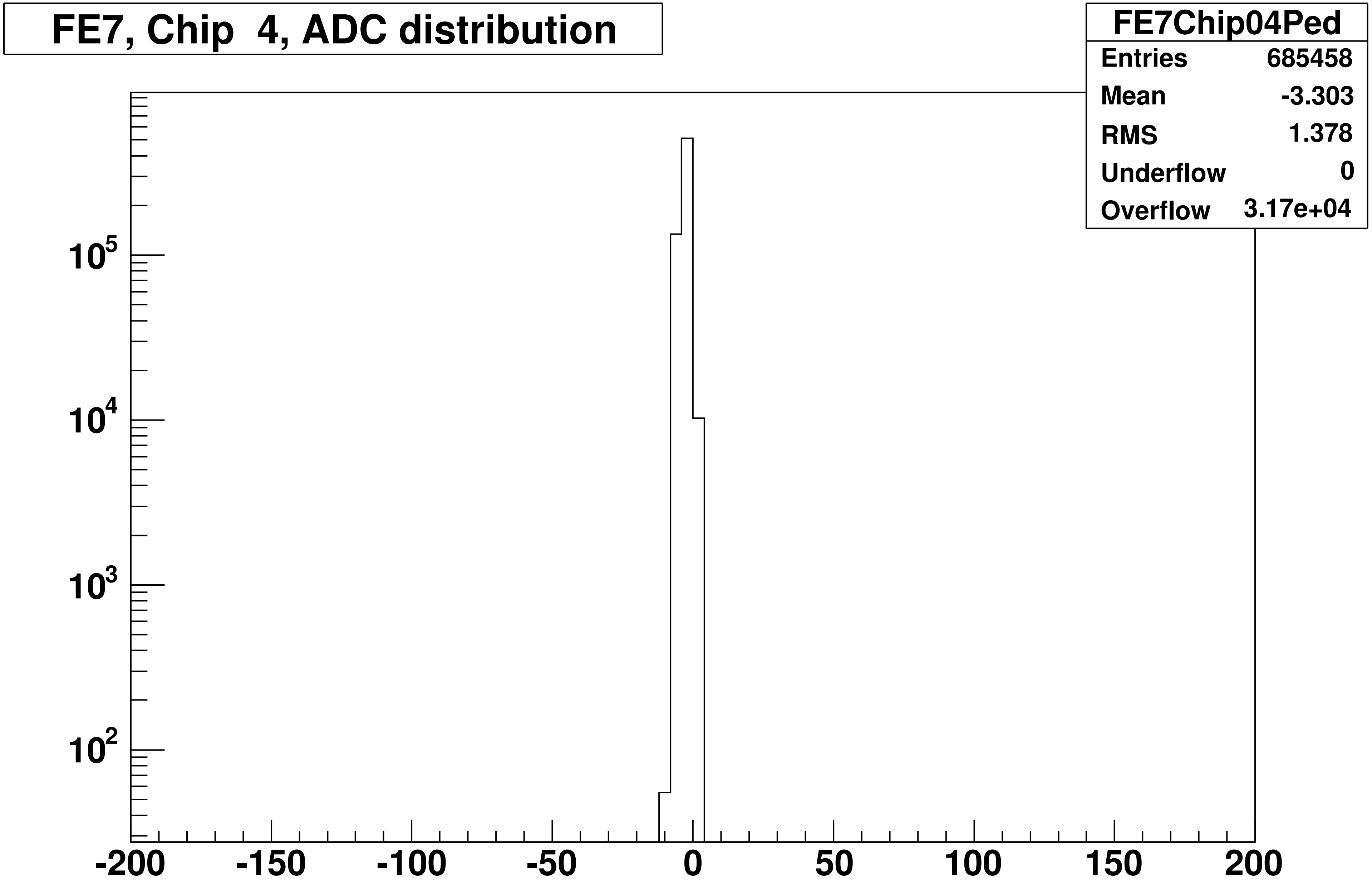

FE7, Chip 4, ADC distribution
FE7Chip04All
Entries 685458
Mean 565.6
RMS 2584
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
-5000
0
5000
10000
15000
20000
25000


FE7, Chip 4, ADC distribution
FE7Chip04Ped
Entries 685458
Mean -3.303
RMS 1.378
Underflow 0
Overflow 3.17e+04
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10^4
10^3
10^2
-200
-150
-100
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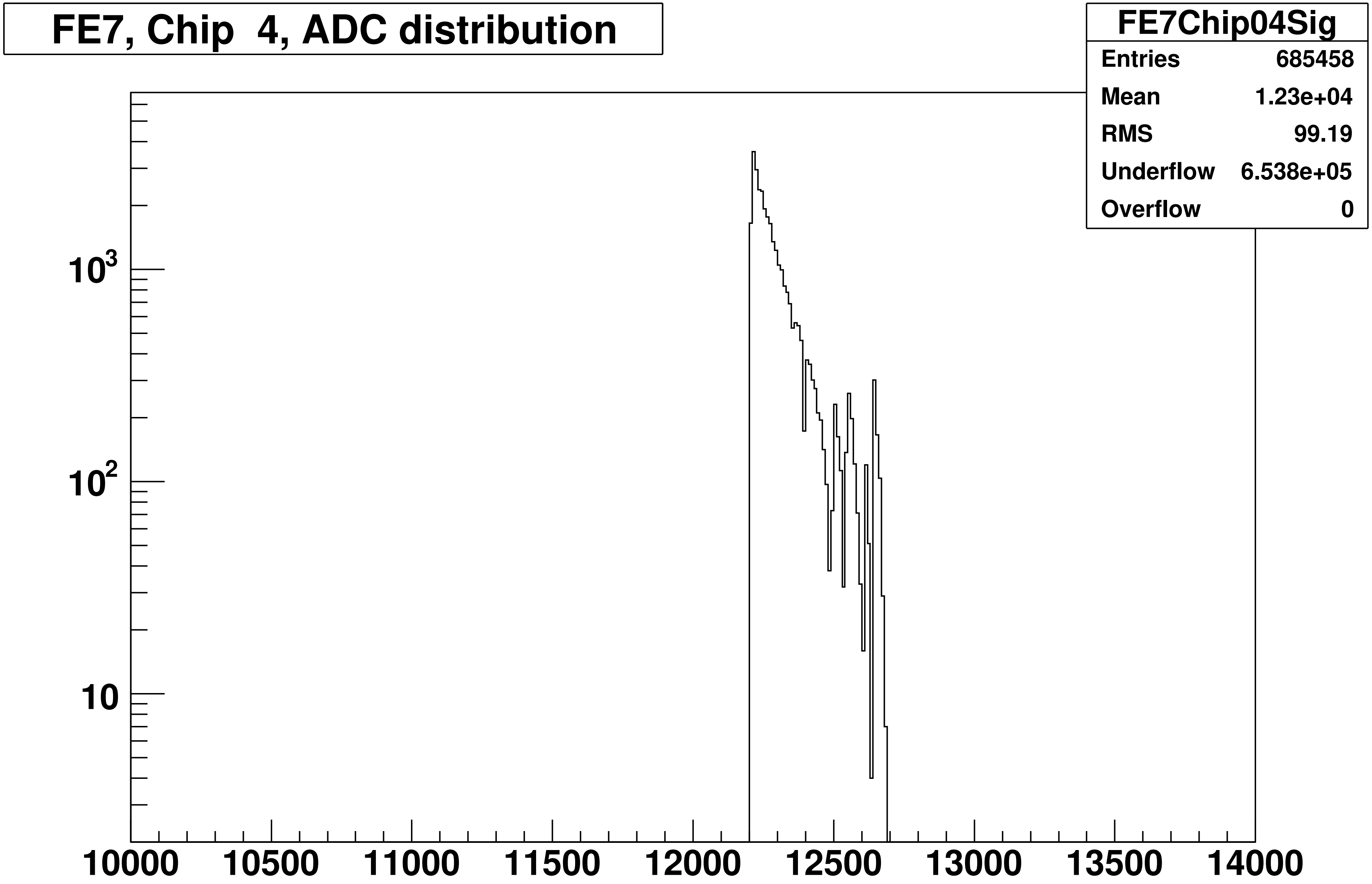
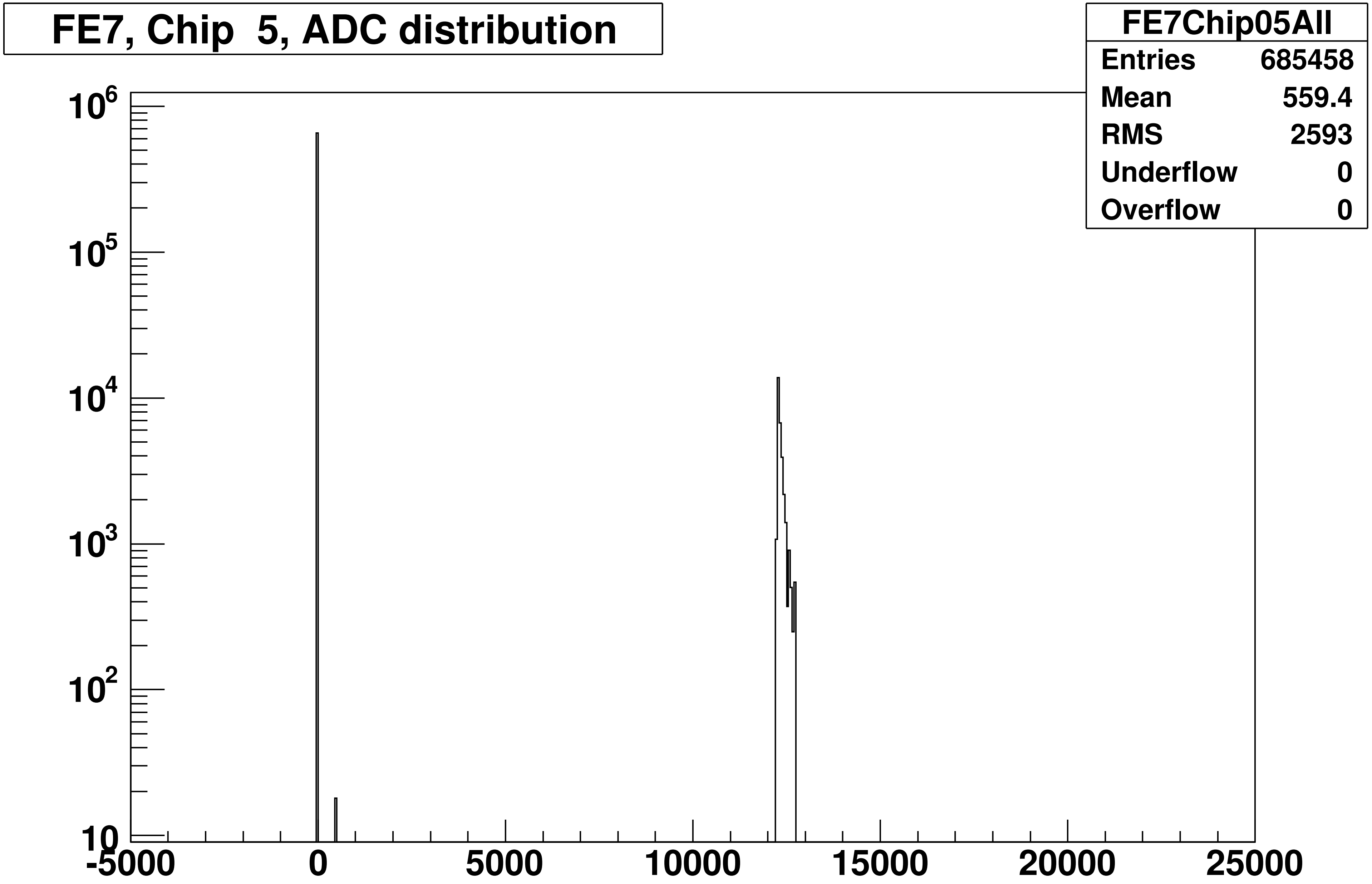
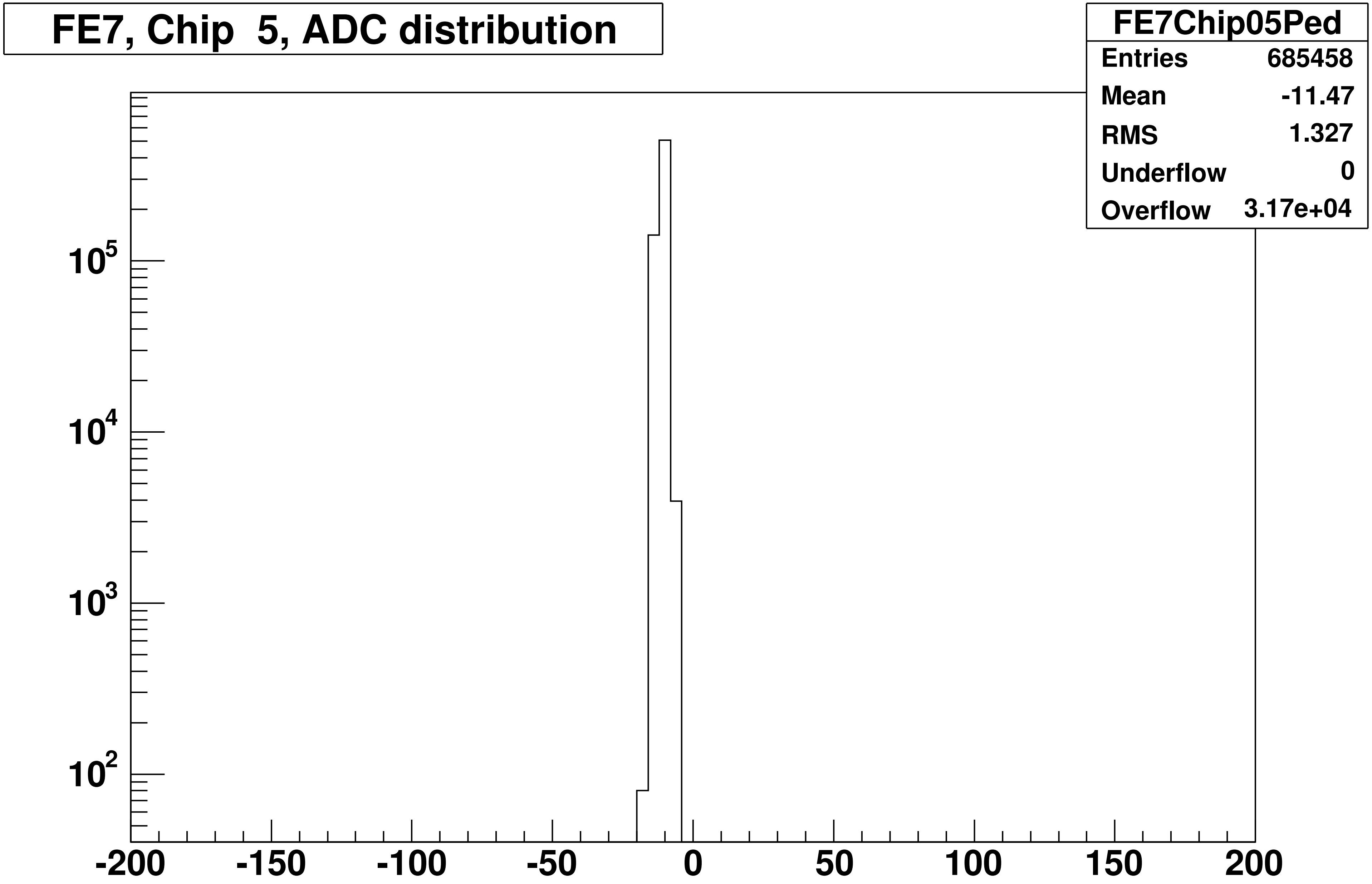
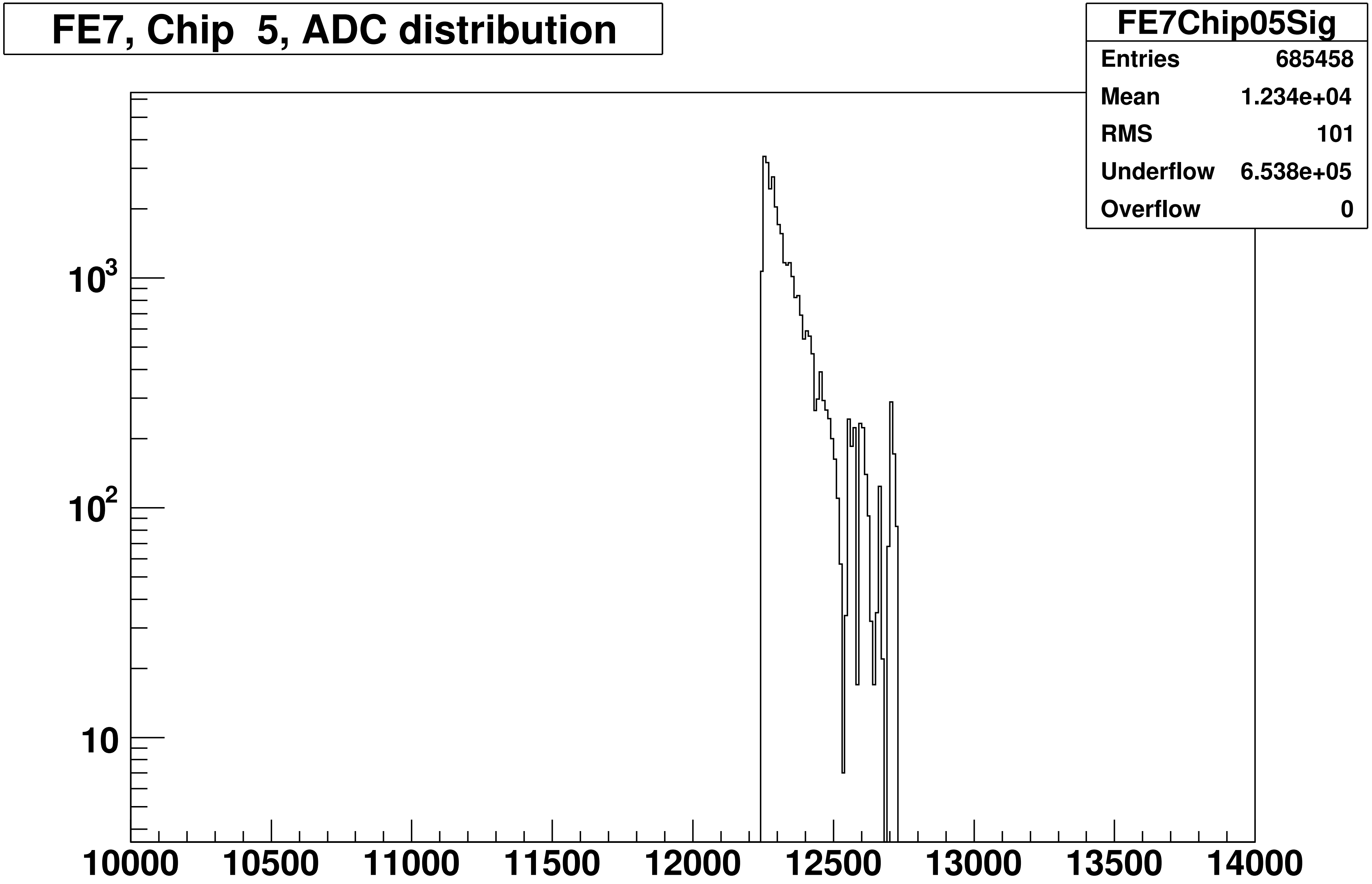
0
50
100
150
200


FE7, Chip 4, ADC distribution
FE7Chip04Sig
Entries 685458
Mean 1.23e+04
RMS 99.19
Underflow 6.538e+05
Overflow 0
10³
10²
10
10000
10500
11000
11500
12000
12500
13000
13500
14000



FE7, Chip 5, ADC distribution
FE7Chip05All
Entries 685458
Mean 559.4
RMS 2593
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE7, Chip 5, ADC distribution
FE7Chip05Ped
Entries 685458
Mean -11.47
RMS 1.327
Underflow 0
Overflow 3.17e+04
10^5
10^4
10^3
10^2
-200
-150
-100
-50
0
50
100
150
200


FE7, Chip 5, ADC distribution
FE7Chip05Sig
Entries 685458
Mean 1.234e+04
RMS 101
Underflow 6.538e+05
Overflow 0
10^3
10^2
10
10000
10500
11000
11500
12000
12500
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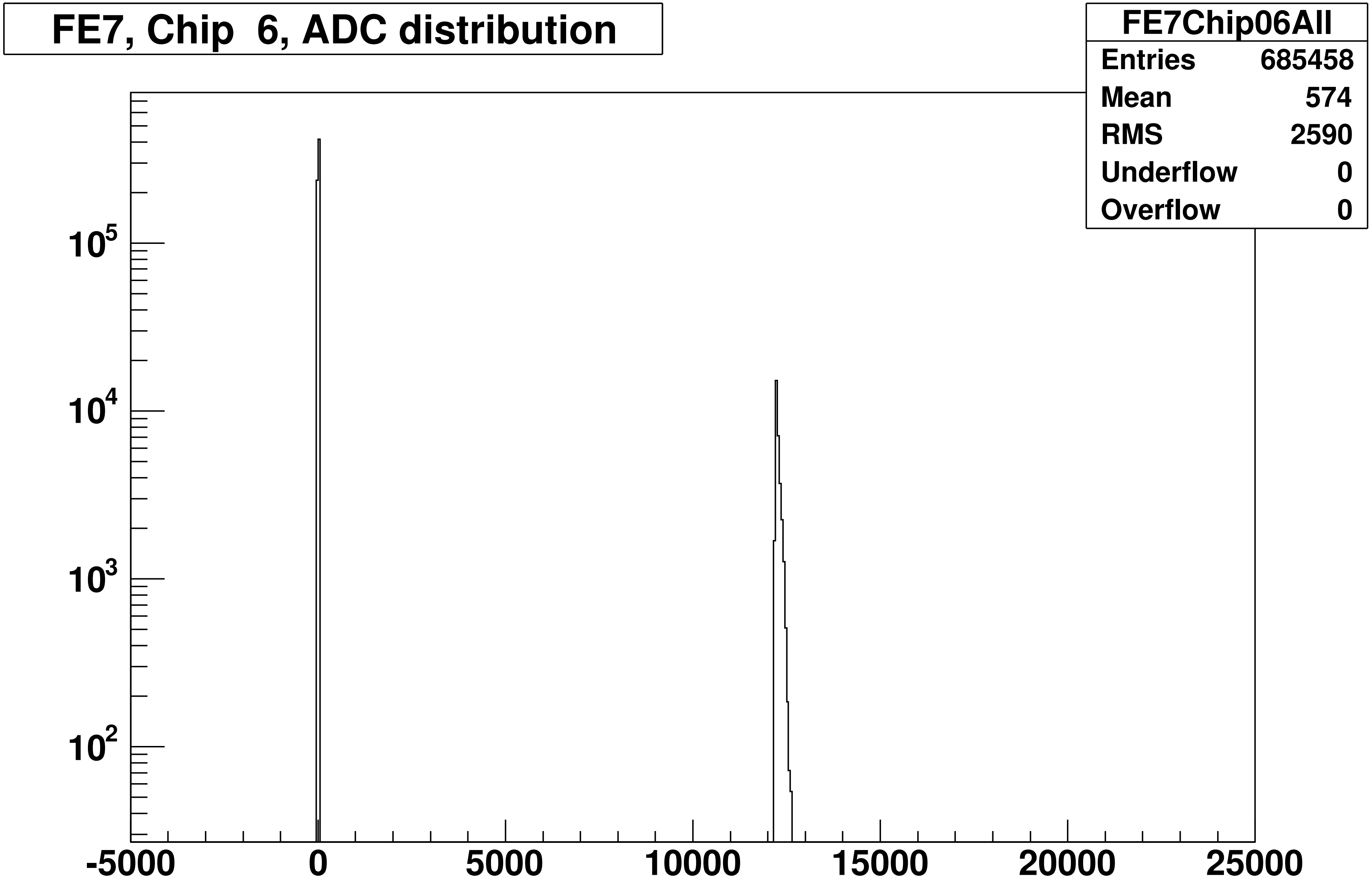
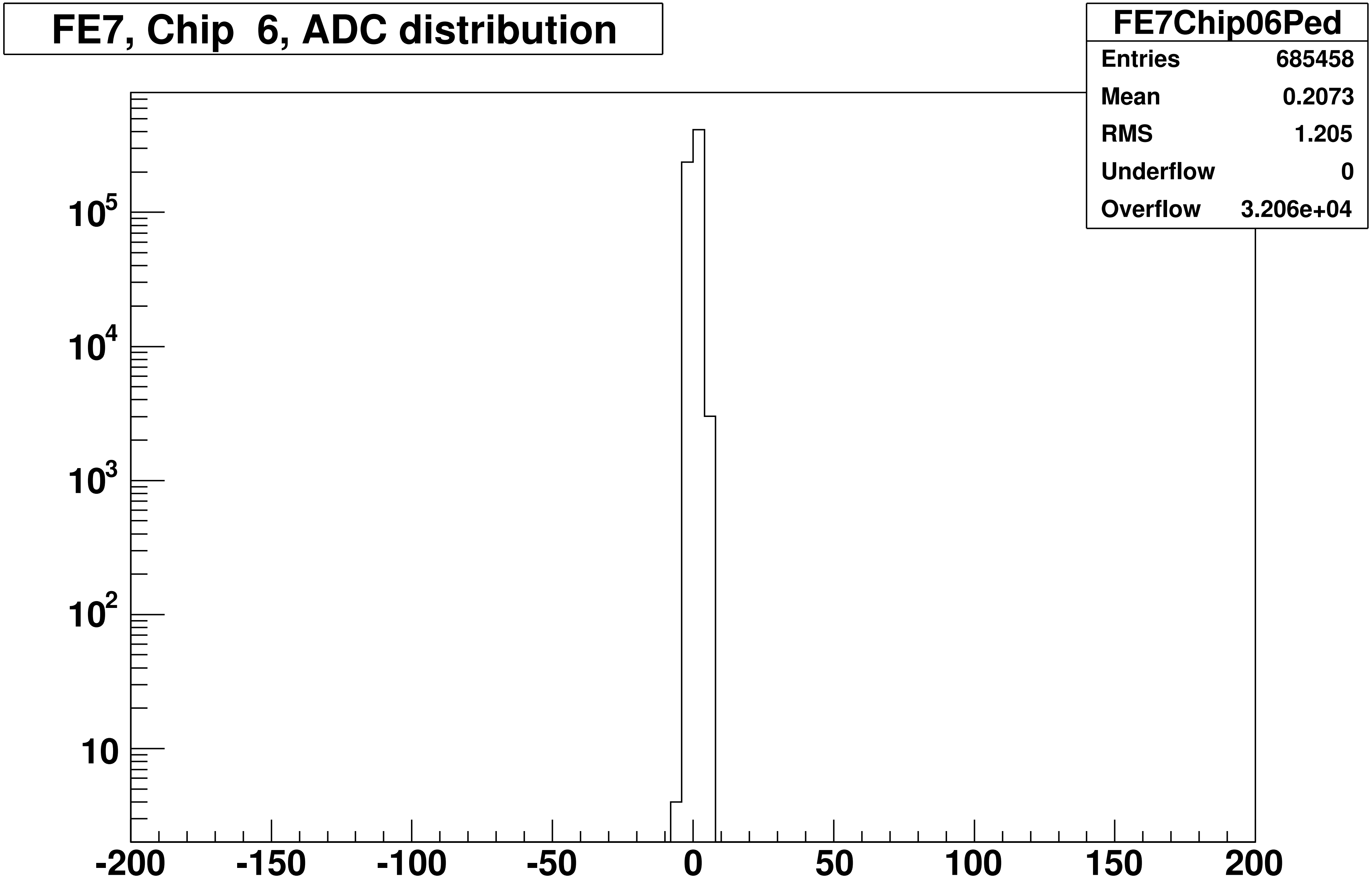
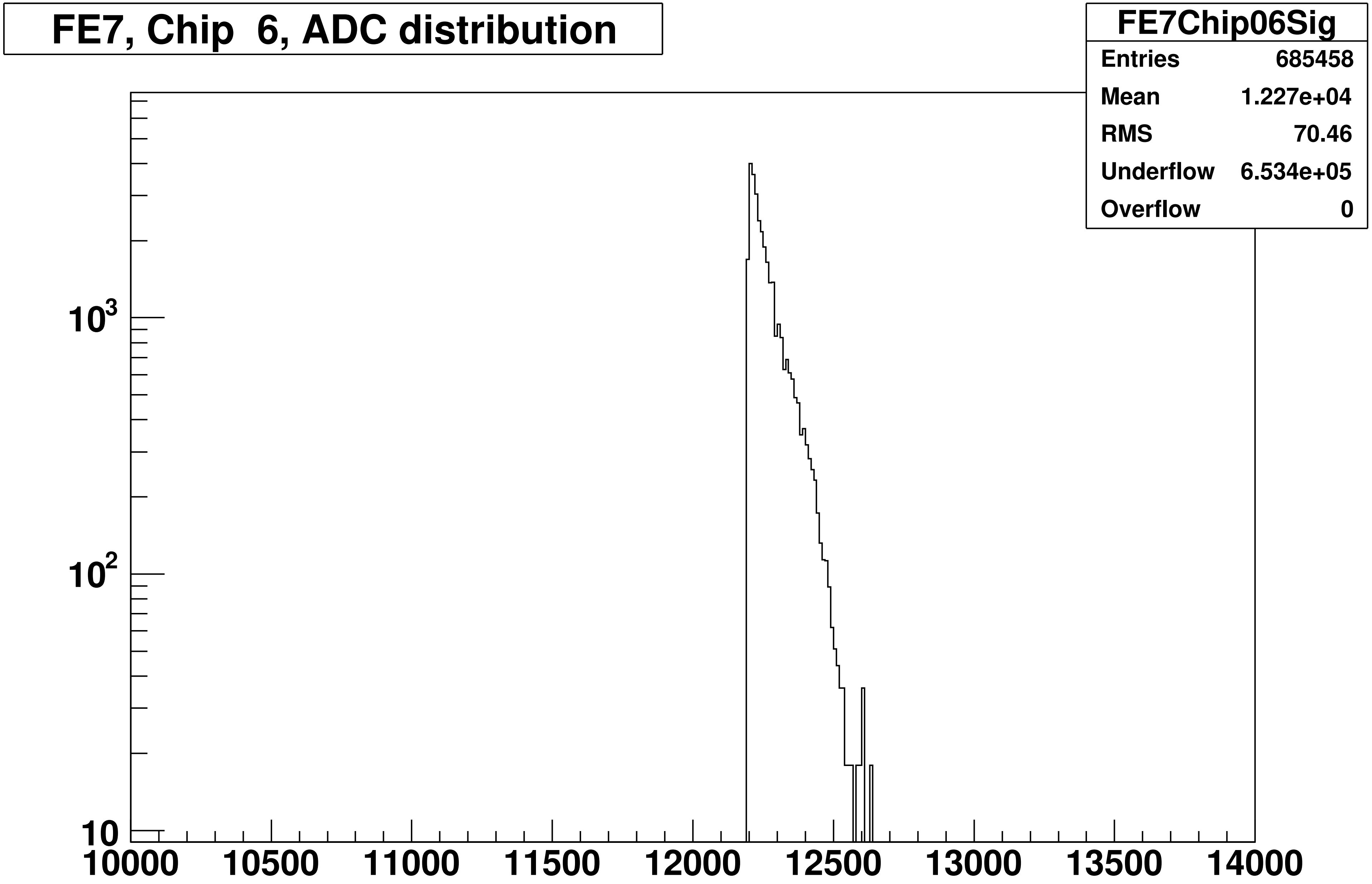
13500
14000

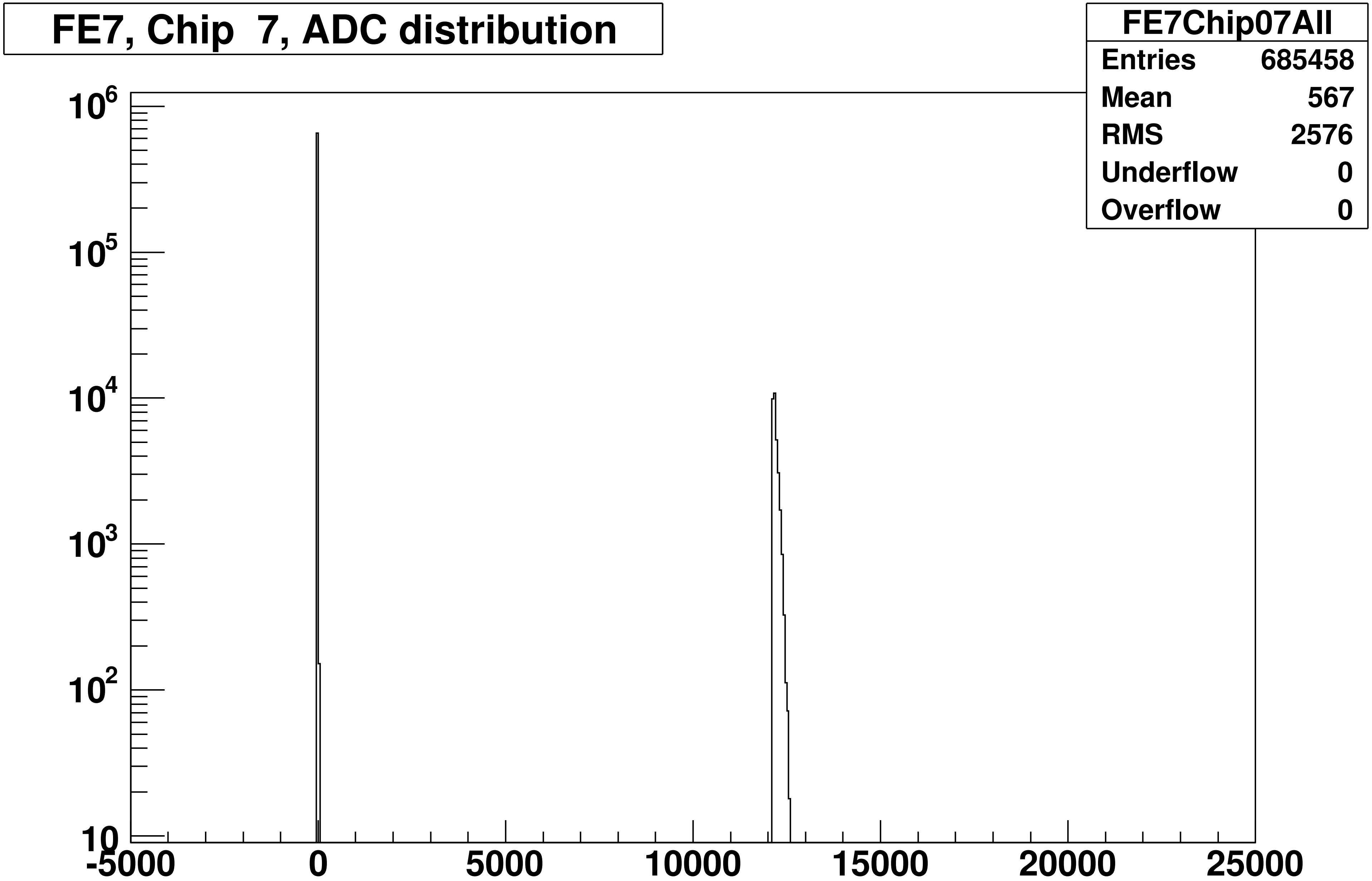

FE7, Chip 6, ADC distribution
FE7Chip06All
Entries 685458
Mean 574
RMS 2590
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000



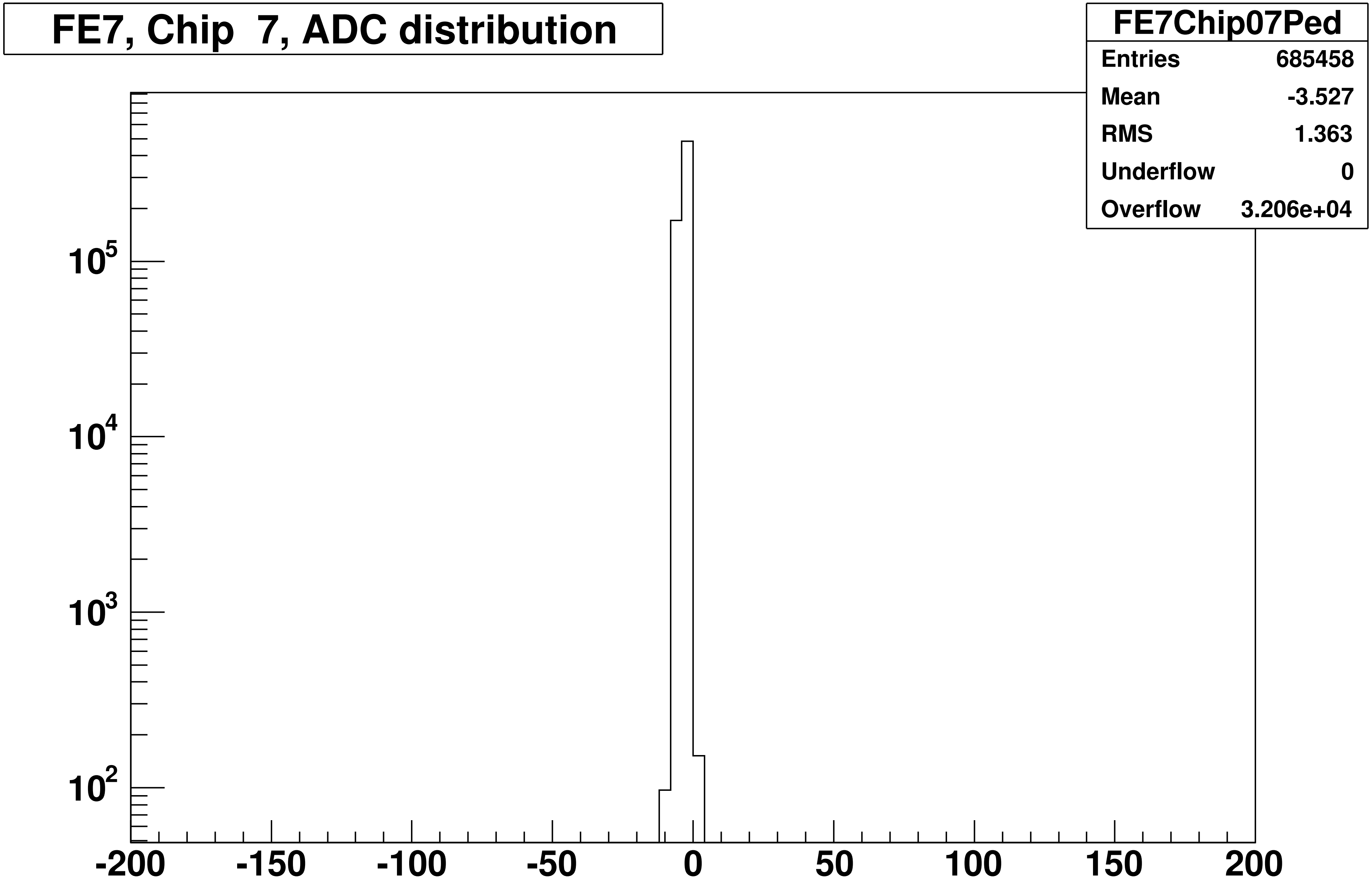
FE7, Chip 6, ADC distribution
FE7Chip06Ped
Entries 685458
Mean 0.2073
RMS 1.205
Underflow 0
Overflow 3.206e+04
10^5
10^4
10^3
10^2
10
-200
-150
-100
-50
0
50
100
150
200



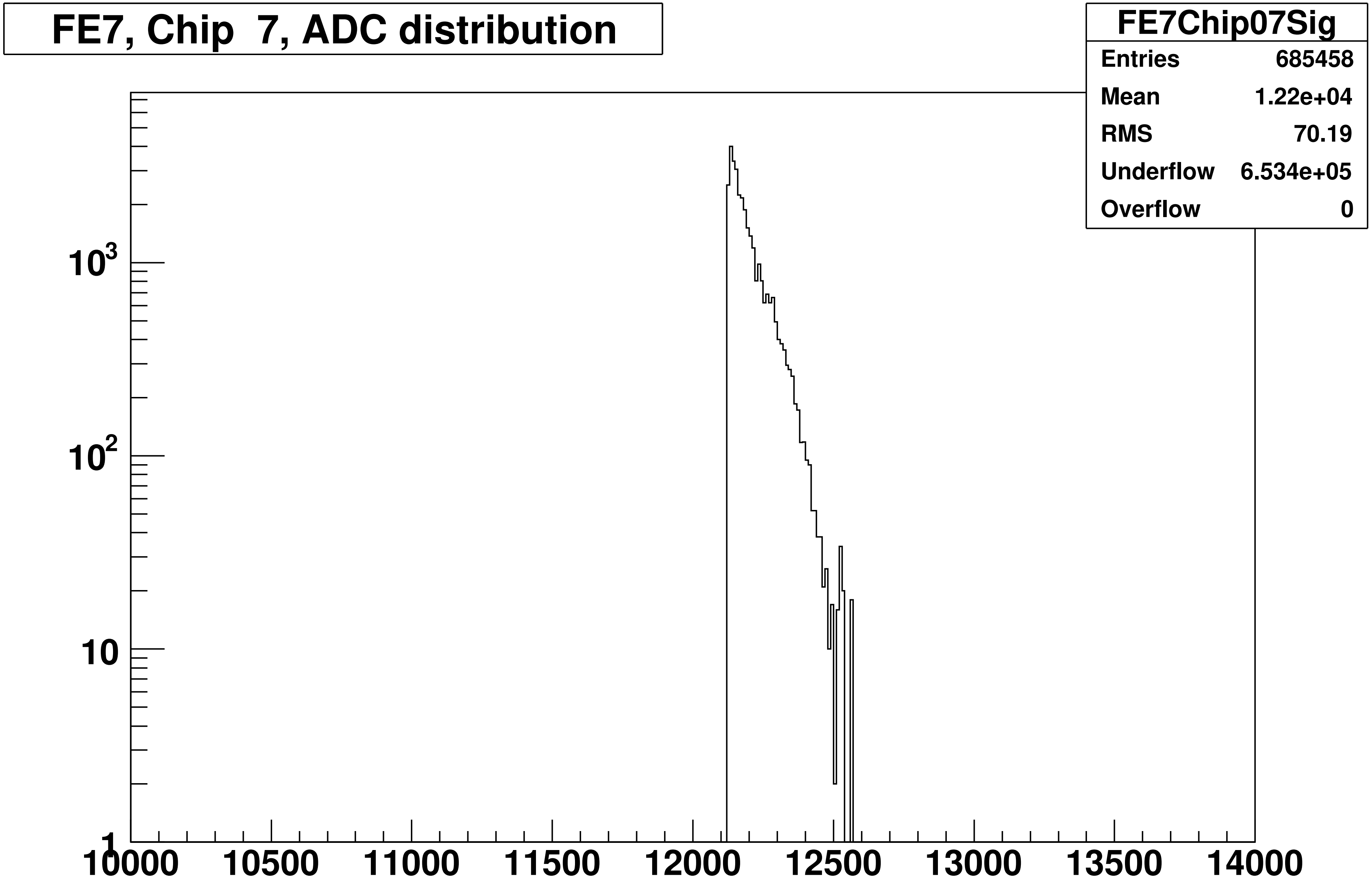
FE7, Chip 6, ADC distribution
FE7Chip06Sig
Entries 685458
Mean 1.227e+04
RMS 70.46
Underflow 6.534e+05
Overflow 0
10^3
10^2
10
10000
10500
11000
11500
12000
12500
13000
13500
14000



FE7, Chip 7, ADC distribution
FE7Chip07All
Entries 685458
Mean 567
RMS 2576
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000



FE7, Chip 7, ADC distribution
FE7Chip07Ped
Entries 685458
Mean -3.527
RMS 1.363
Underflow 0
Overflow 3.206e+04
10^5
10^4
10^3
10^2
-200
-150
-100
-50
0
50
100
150
200


FE7, Chip 7, ADC distribution
FE7Chip07Sig
Entries 685458
Mean 1.22e+04
RMS 70.19
Underflow 6.534e+05
Overflow 0
10^3
10^2
10
1
10000
10500
11000
11500
12000
12500
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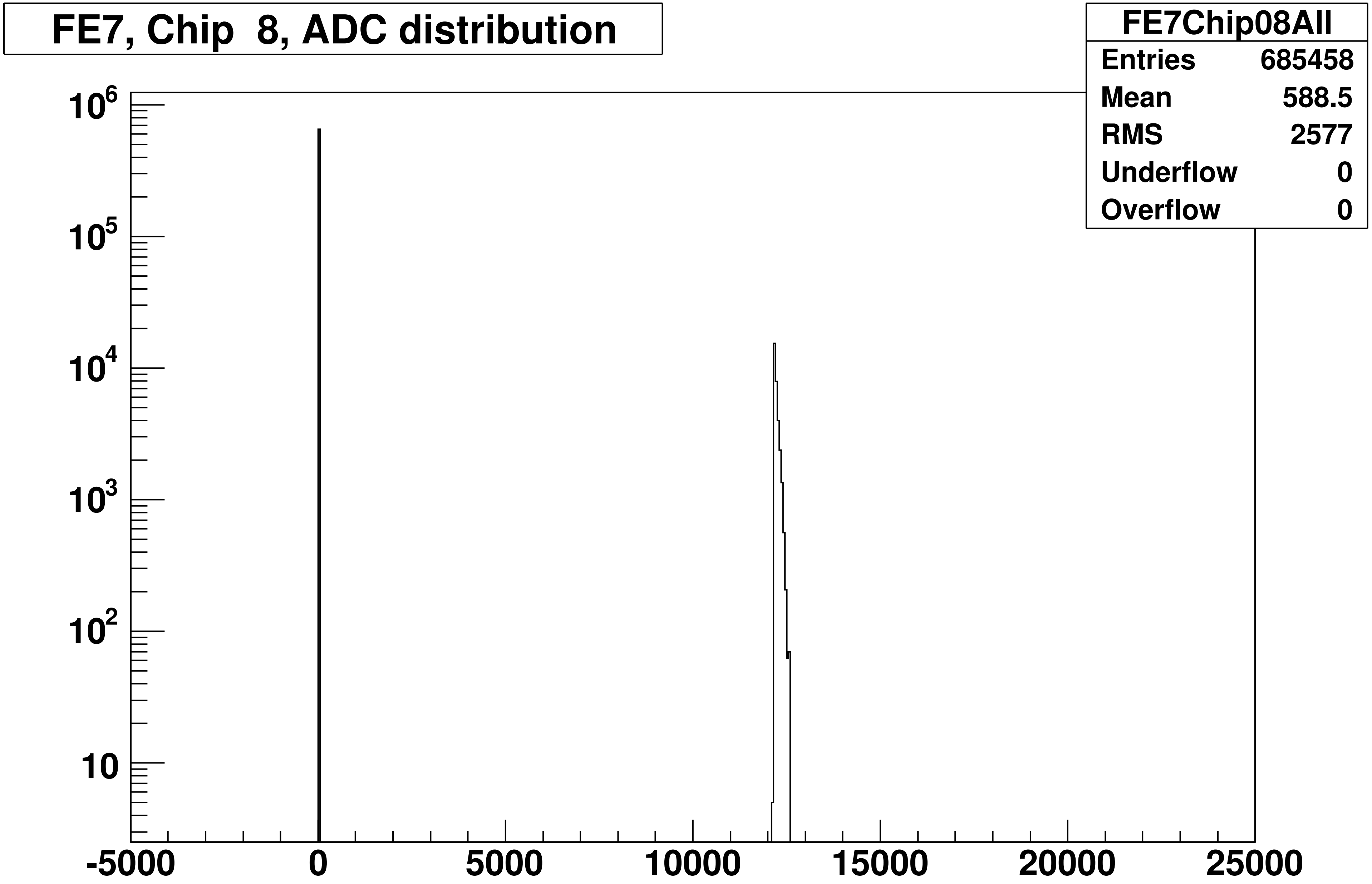
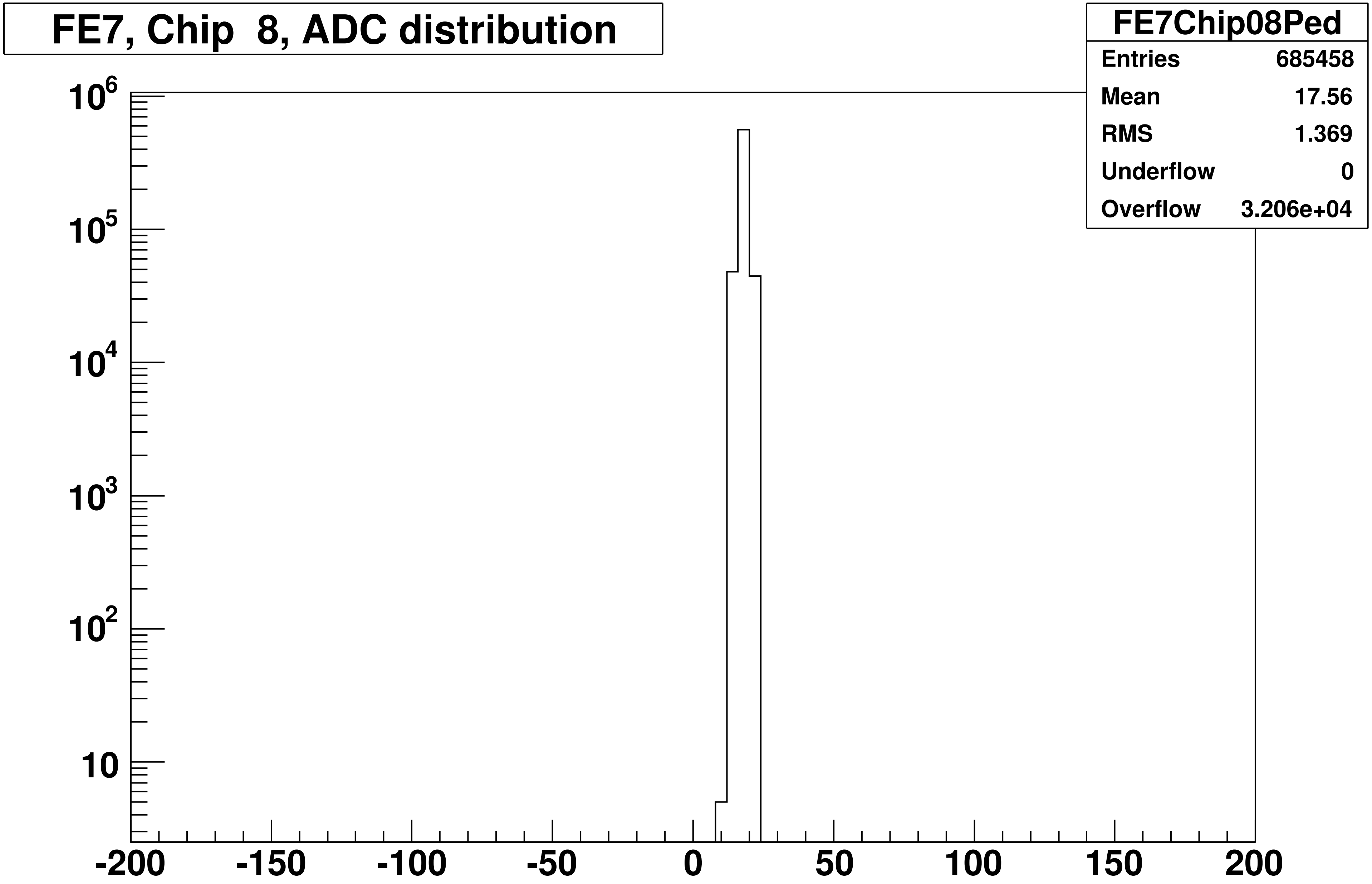
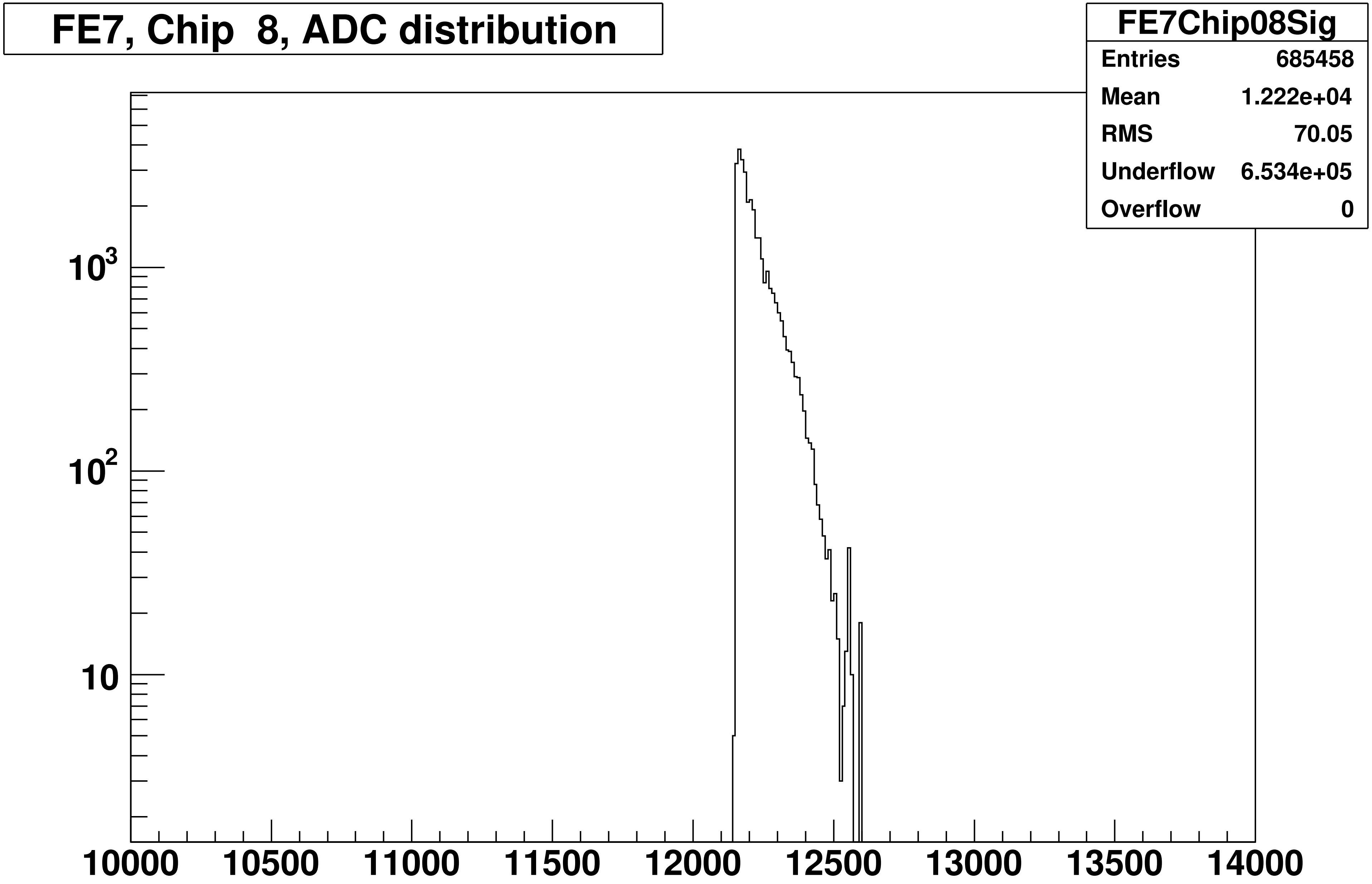


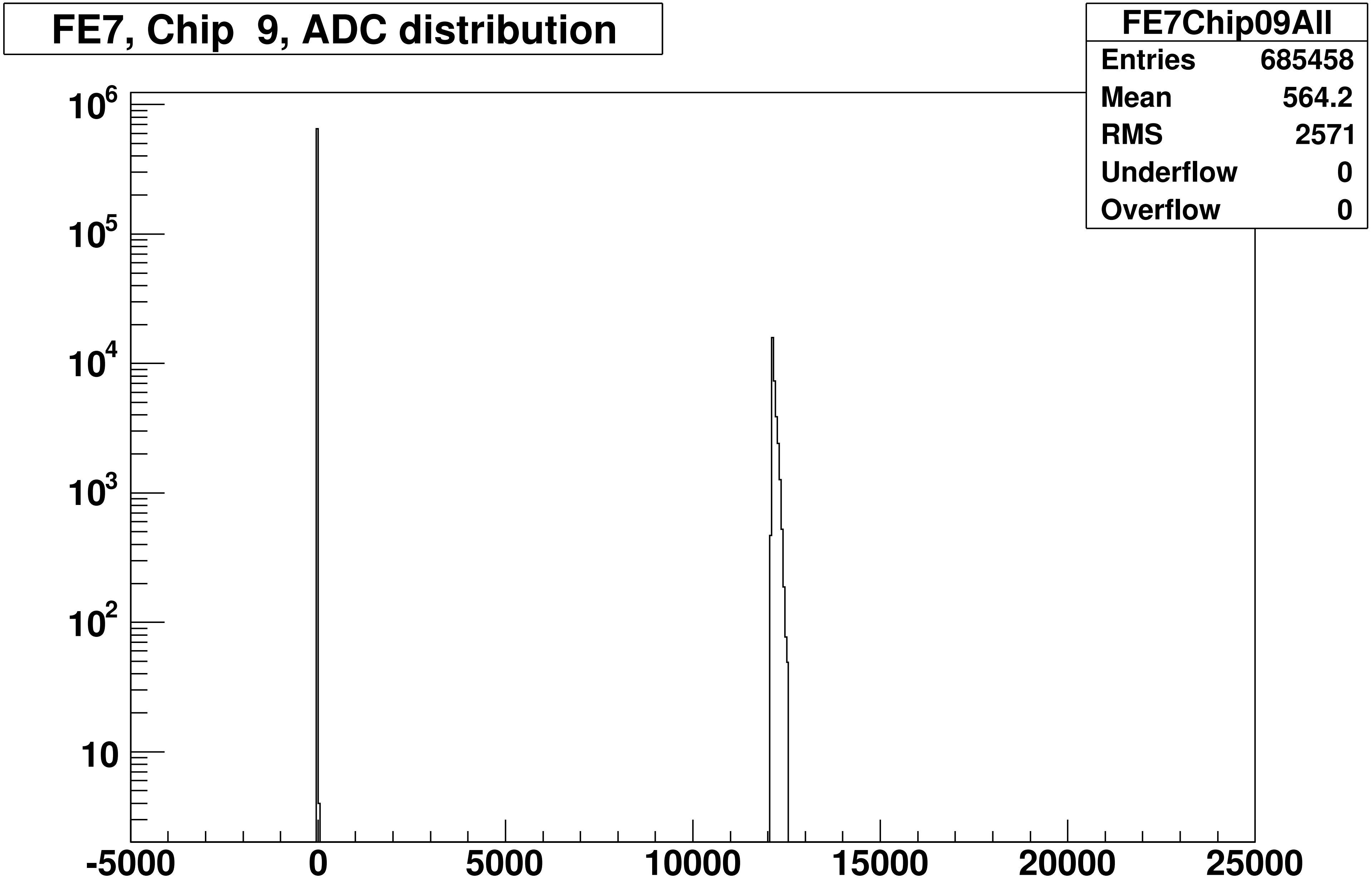
FE7, Chip 8, ADC distribution
FE7Chip08All
Entries 685458
Mean 588.5
RMS 2577
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000

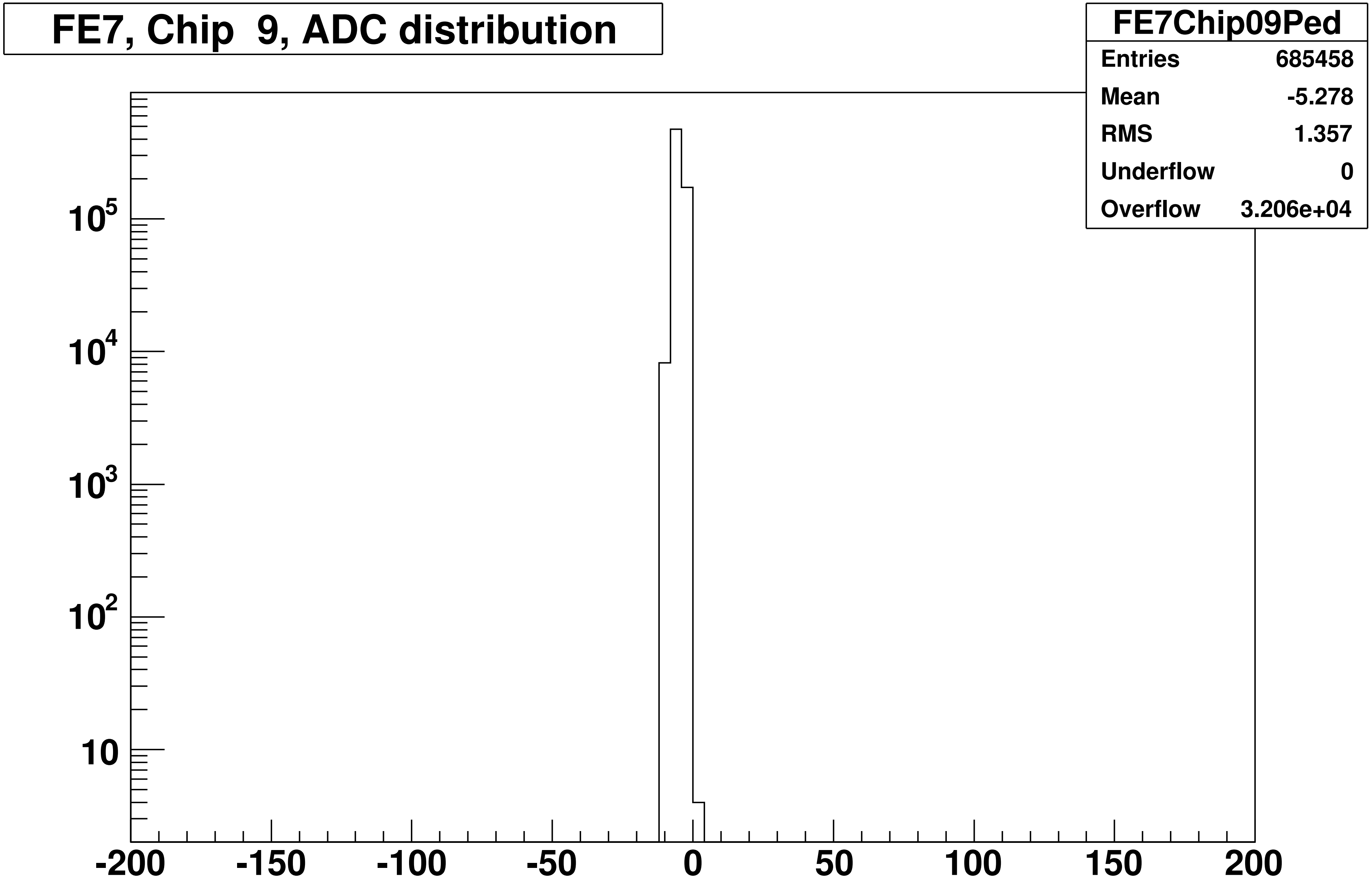


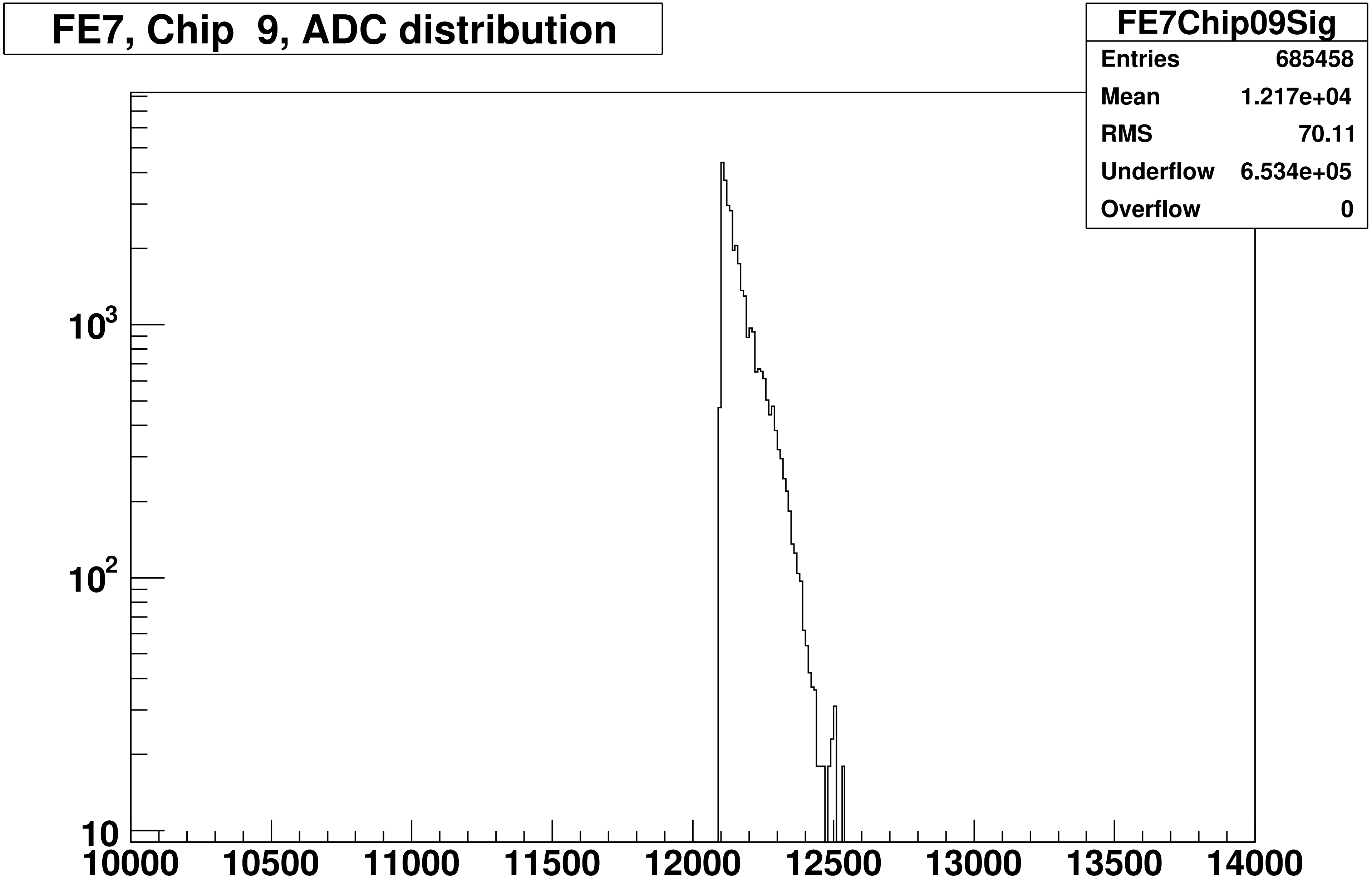
FE7, Chip 8, ADC distribution
FE7Chip08Ped
Entries 685458
Mean 17.56
RMS 1.369
Underflow 0
Overflow 3.206e+04
10^6
10^5
10^4
10^3
10^2
10
-200
-150
-100
-50
0
50
100
150
200



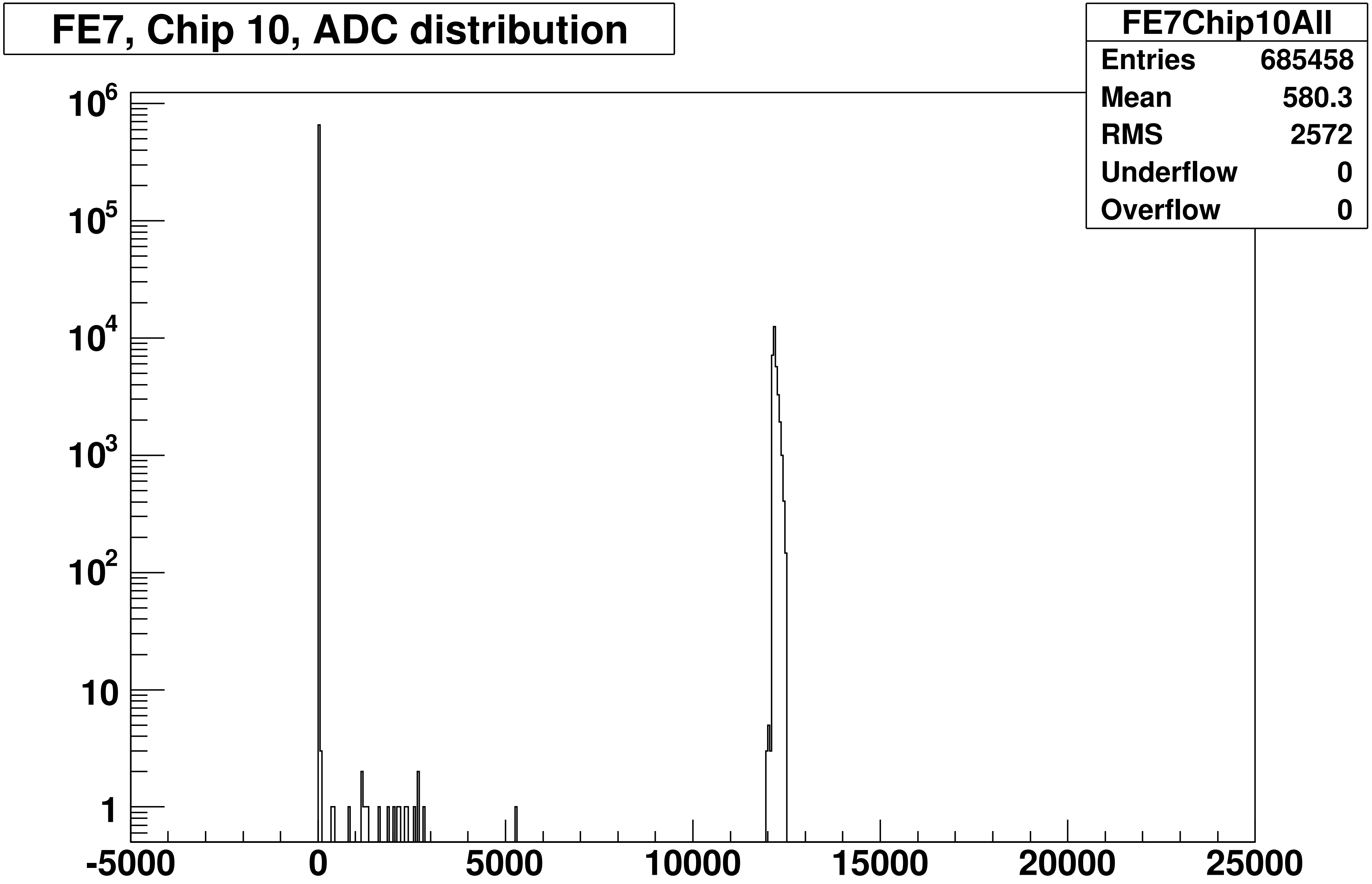
FE7, Chip 8, ADC distribution
FE7Chip08Sig
Entries 685458
Mean 1.222e+04
RMS 70.05
Underflow 6.534e+05
Overflow 0
10^3
10^2
10
10000
10500
11000
11500
12000
12500
13000
13500
14000

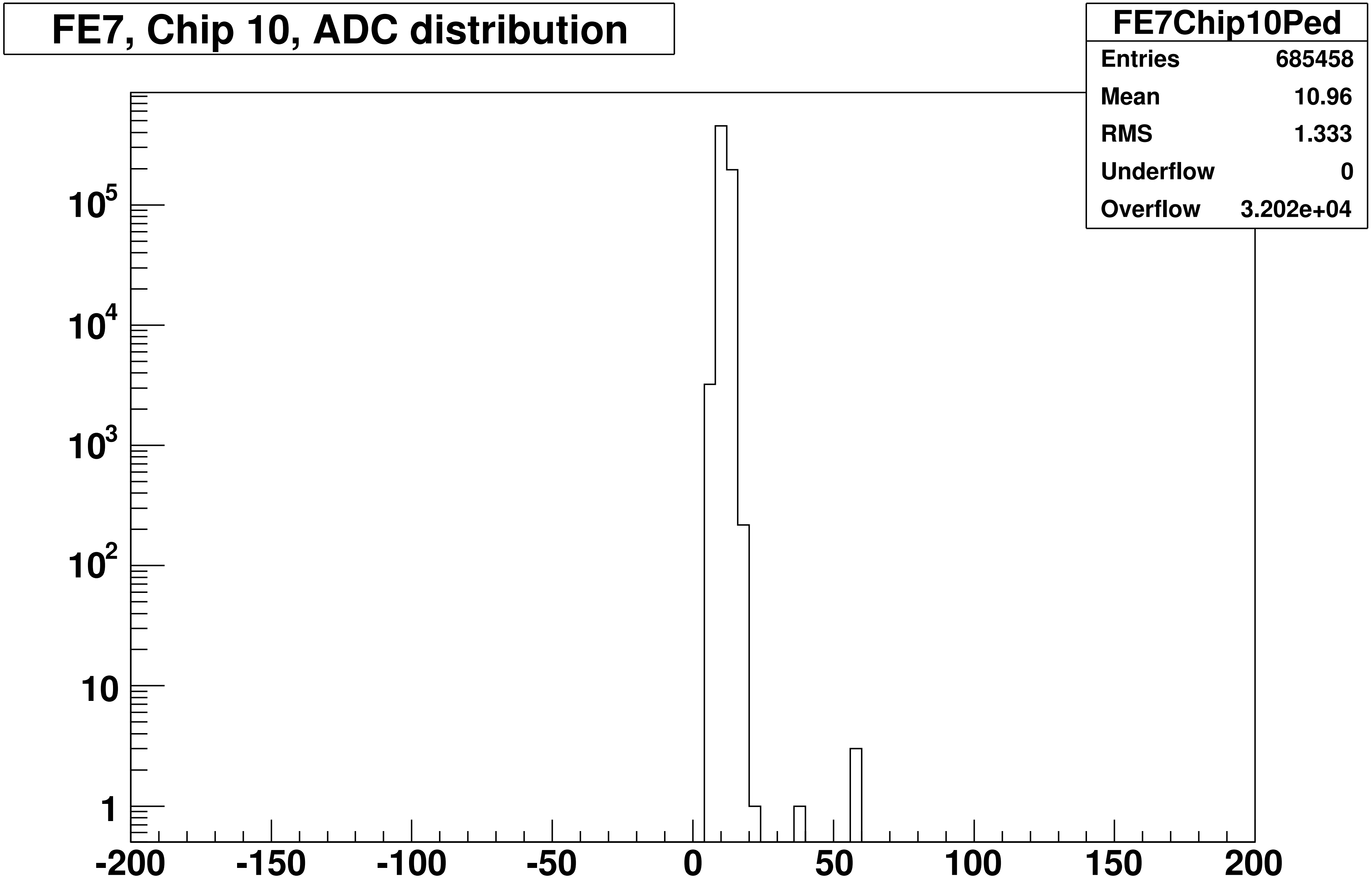

FE7, Chip 9, ADC distribution
FE7Chip09All
Entries 685458
Mean 564.2
RMS 2571
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE7, Chip 9, ADC distribution
FE7Chip09Ped
Entries 685458
Mean -5.278
RMS 1.357
Underflow 0
Overflow 3.206e+04
10^5
10^4
10^3
10^2
10
-200
-150
-100
-50
0
50
100
150
200

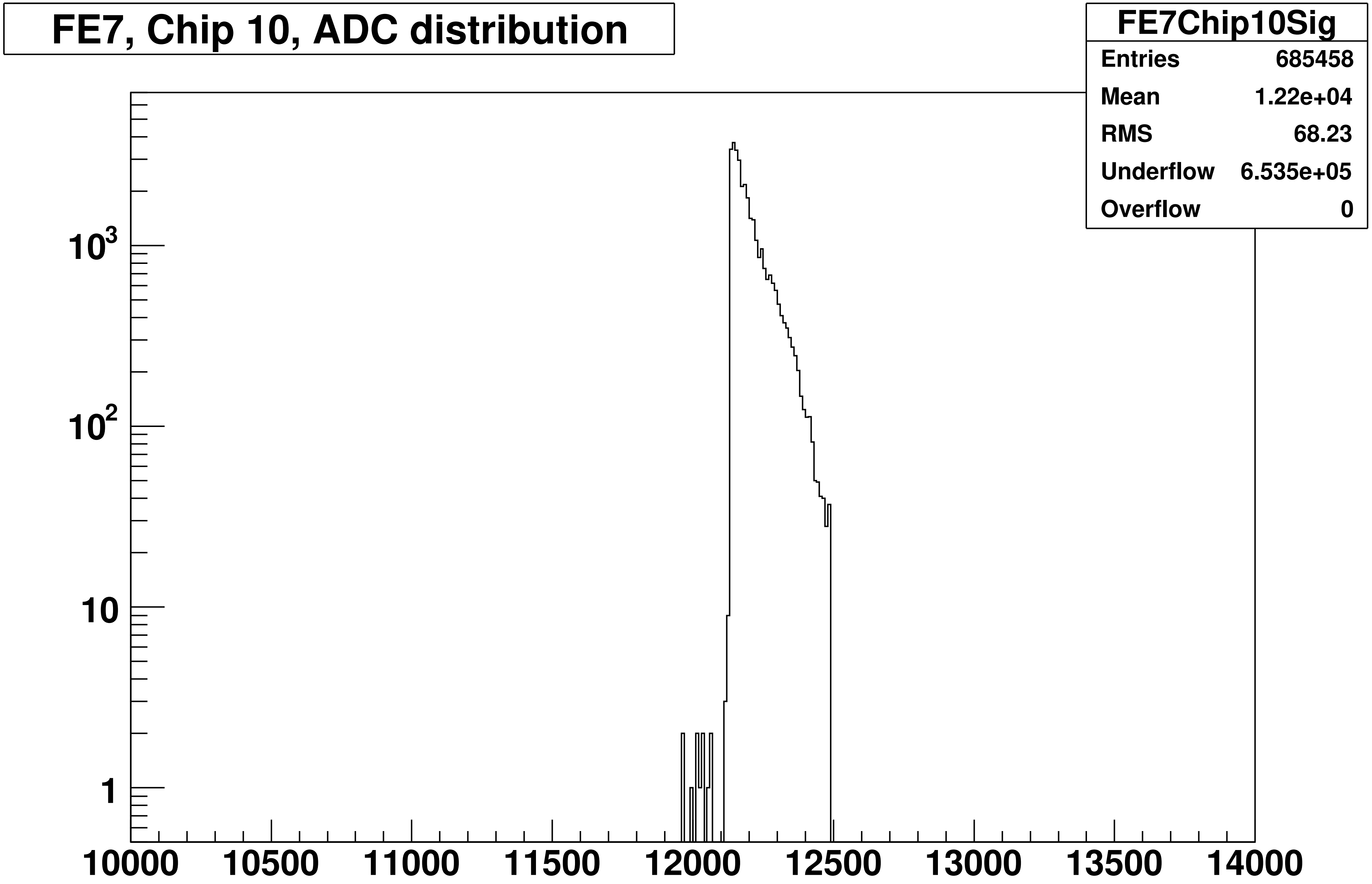


FE7, Chip 9, ADC distribution
FE7Chip09Sig
Entries 685458
Mean 1.217e+04
RMS 70.11
Underflow 6.534e+05
Overflow 0
10^3
10^2
10
10000
10500
11000
11500
12000
12500
13000
13500
14000

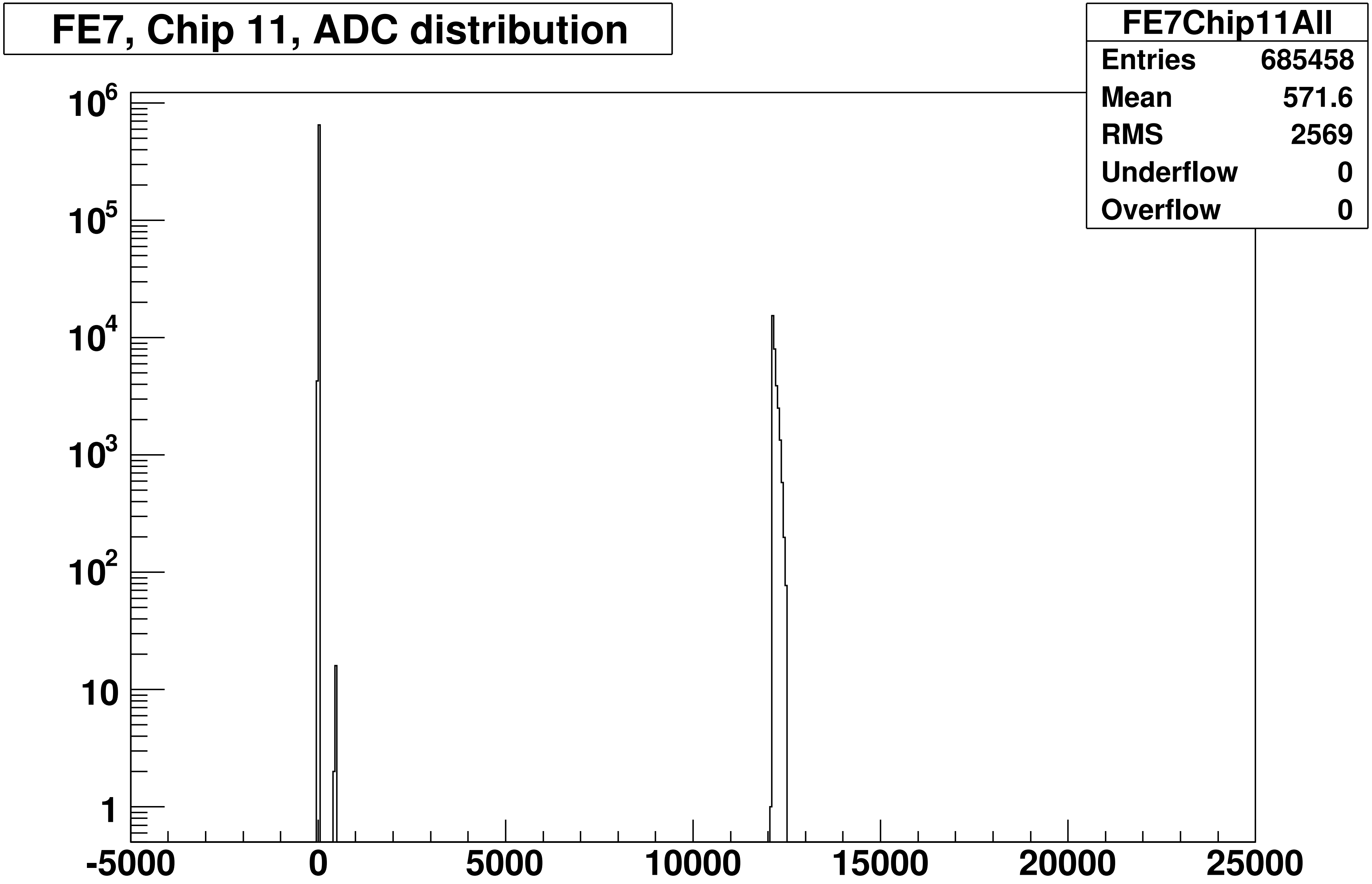

FE7, Chip 10, ADC distribution
FE7Chip10All
Entries 685458
Mean 580.3
RMS 2572
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000

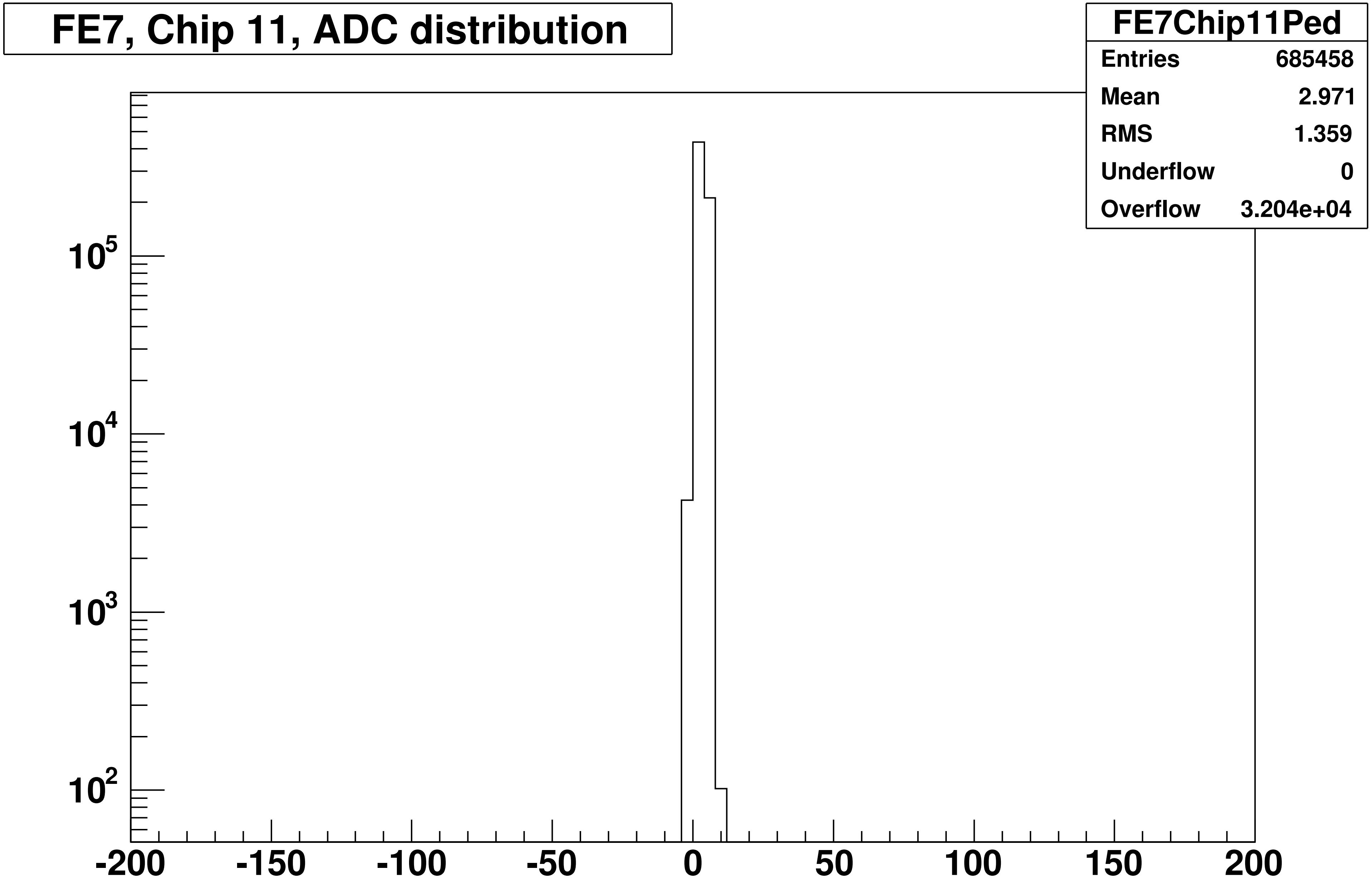


FE7, Chip 10, ADC distribution
FE7Chip10Ped
Entries 685458
Mean 10.96
RMS 1.333
Underflow 0
Overflow 3.202e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
200

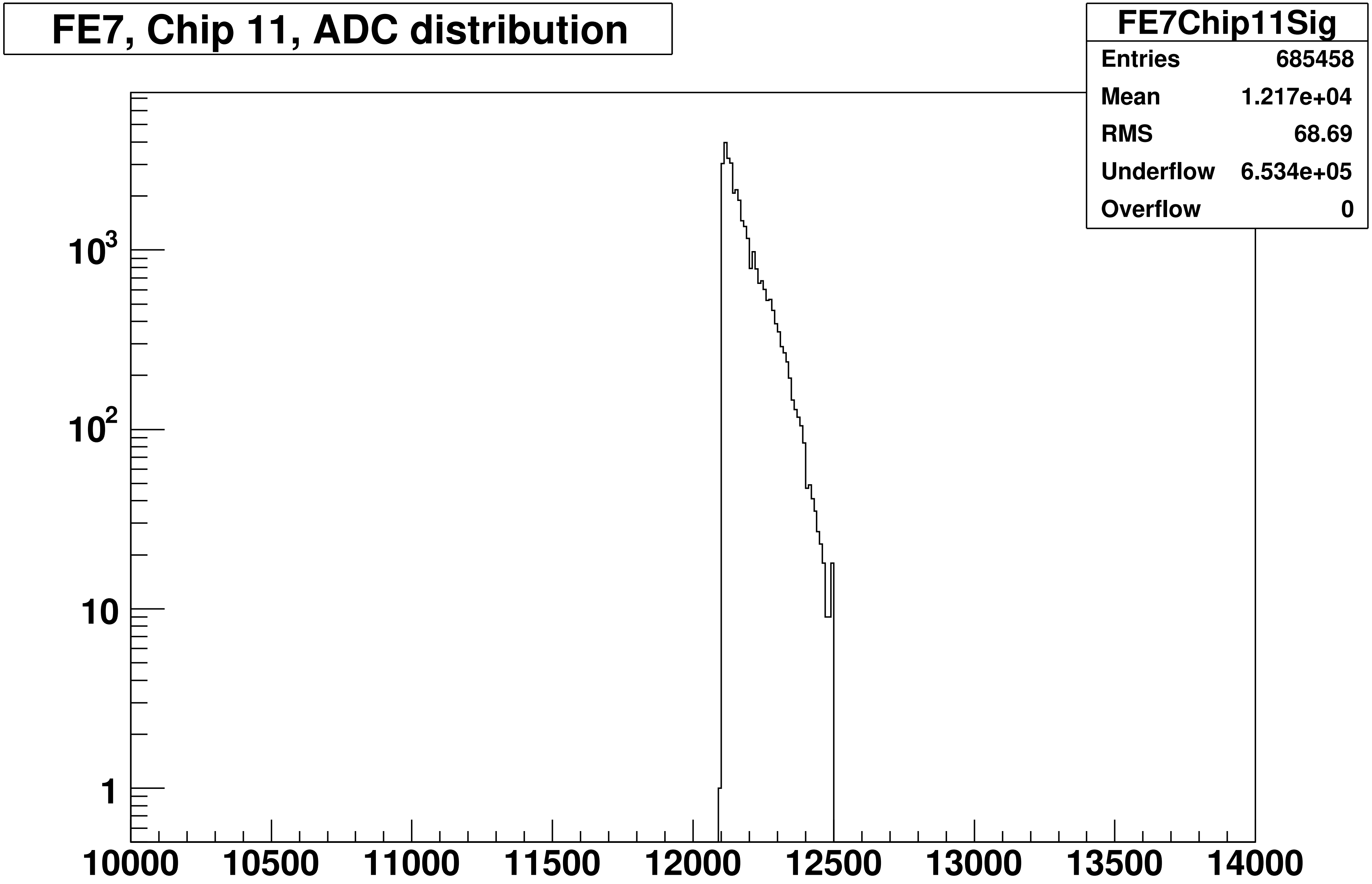


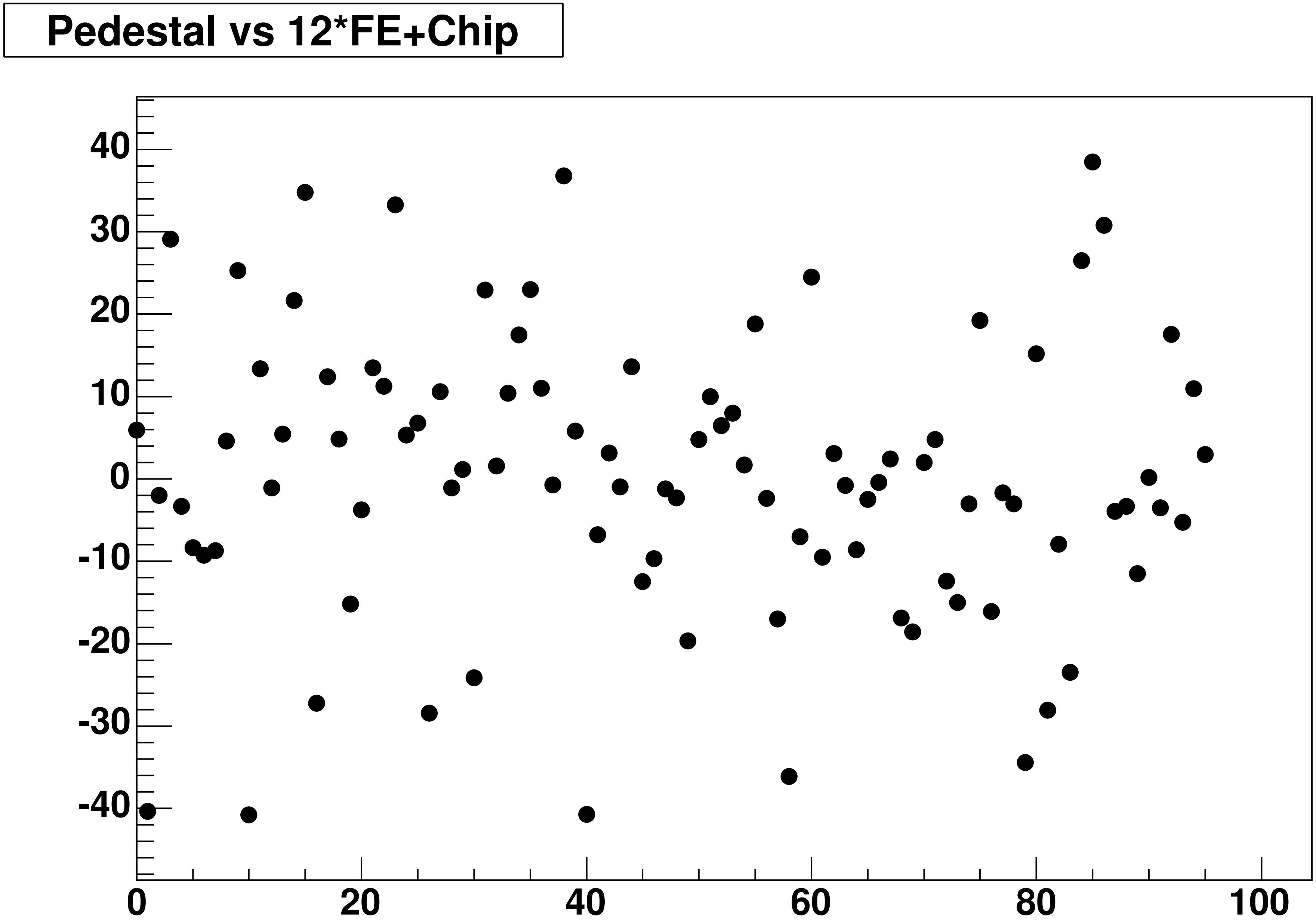
FE7, Chip 10, ADC distribution
FE7Chip10Sig
Entries 685458
Mean 1.22e+04
RMS 68.23
Underflow 6.535e+05
Overflow 0
10^3
10^2
10
1
10000
10500
11000
11500
12000
12500
13000
13500
14000

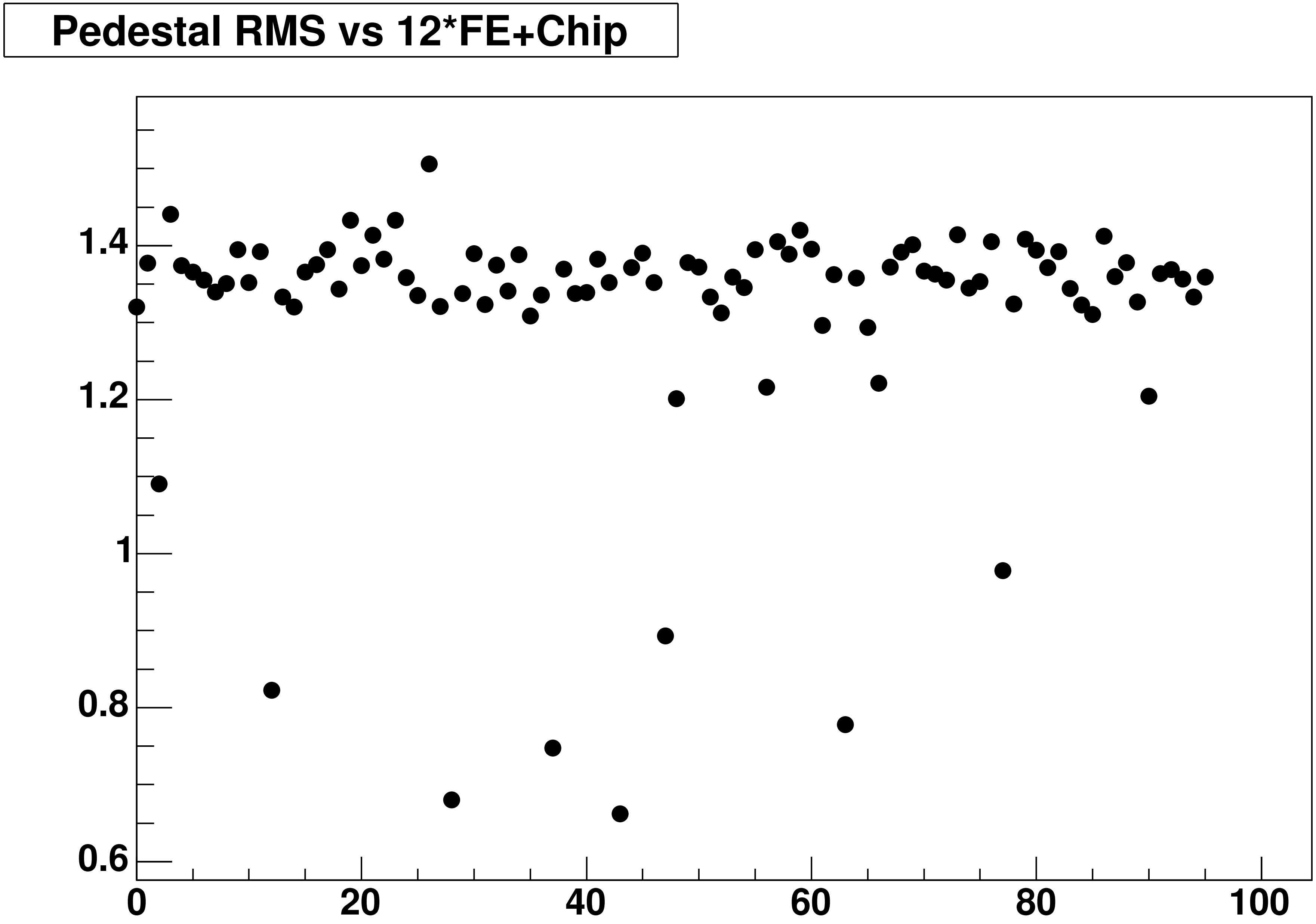

FE7, Chip 11, ADC distribution
FE7Chip11All
Entries 685458
Mean 571.6
RMS 2569
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000

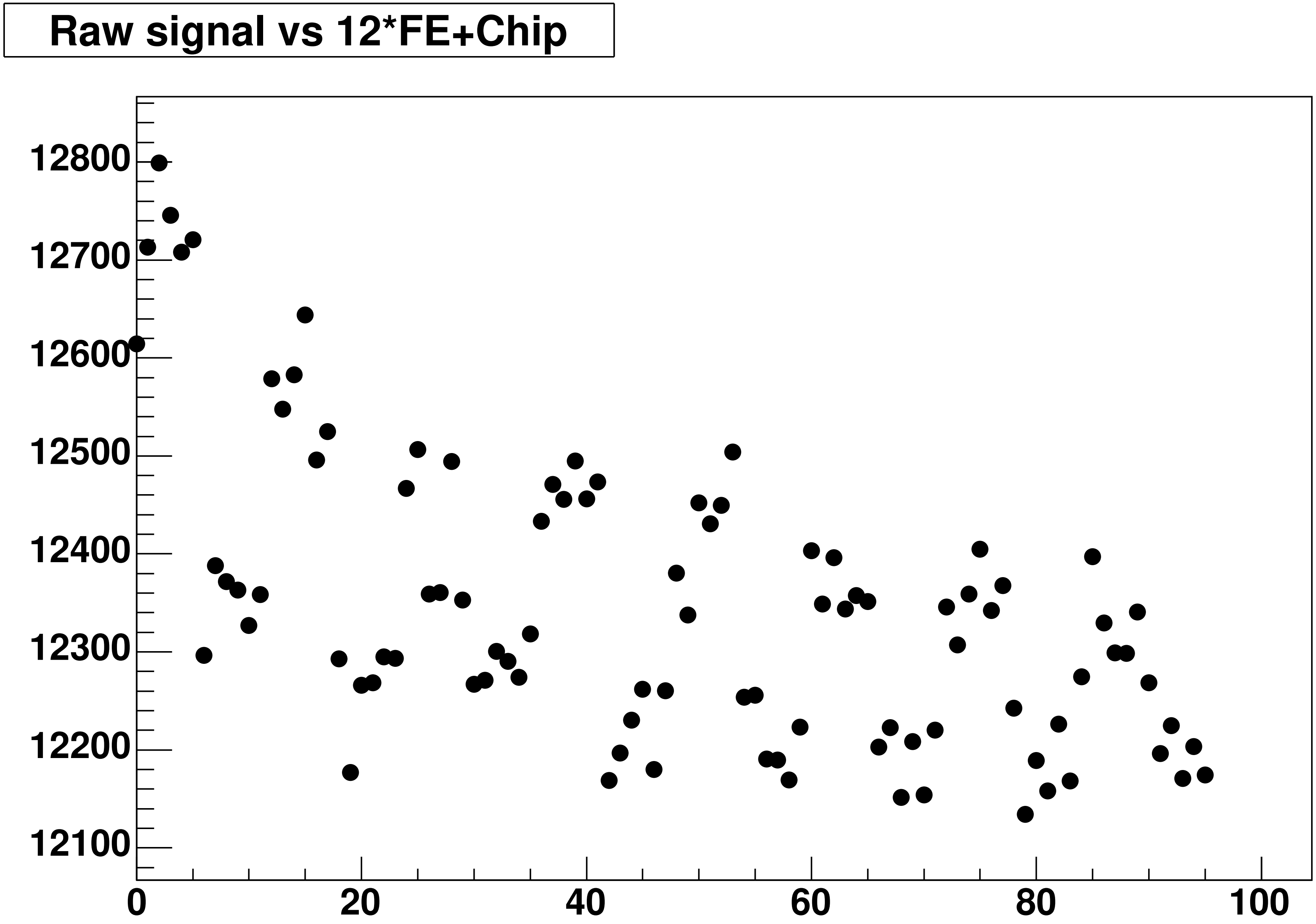


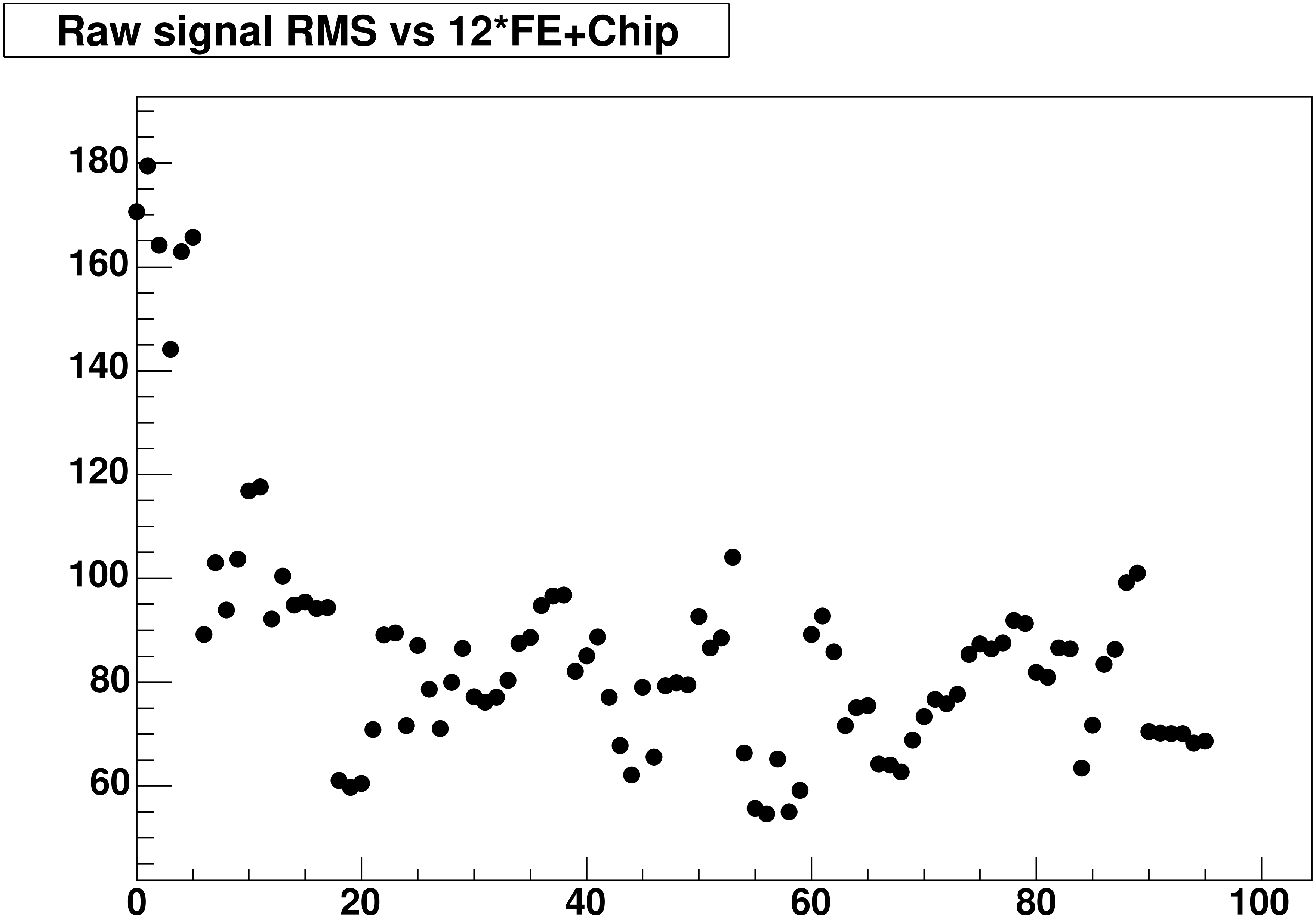
FE7, Chip 11, ADC distribution
FE7Chip11Ped
Entries 685458
Mean 2.971
RMS 1.359
Underflow 0
Overflow 3.204e+04
10^5
10^4
10^3
10^2
-200
-150
-100
-50
0
50
100
150
200

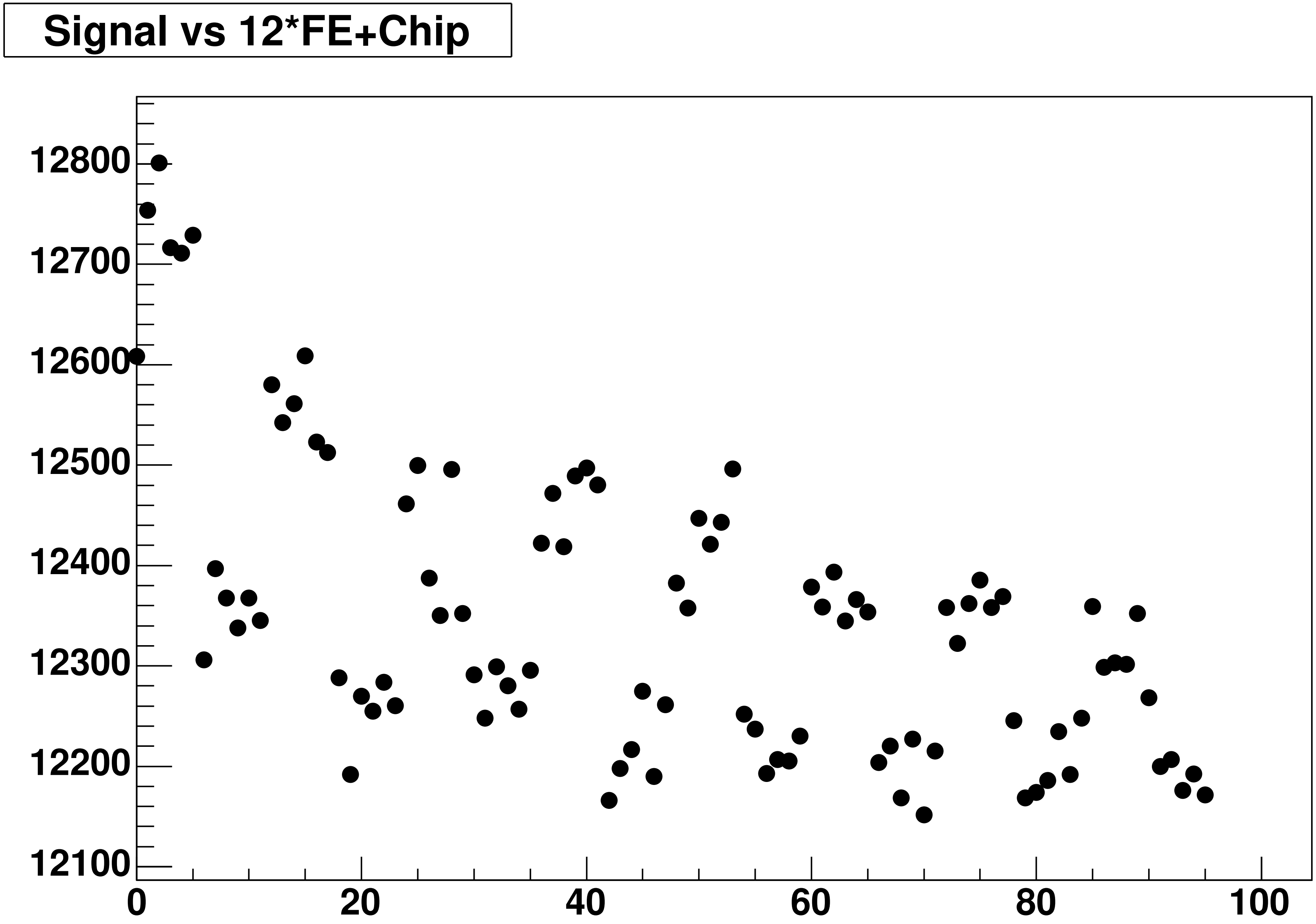

FE7, Chip 11, ADC distribution
FE7Chip11Sig
Entries 685458
Mean 1.217e+04
RMS 68.69
Underflow 6.534e+05
Overflow 0
10^3
10^2
10
1
10000
10500
11000
11500
12000
12500
13000
13500
14000

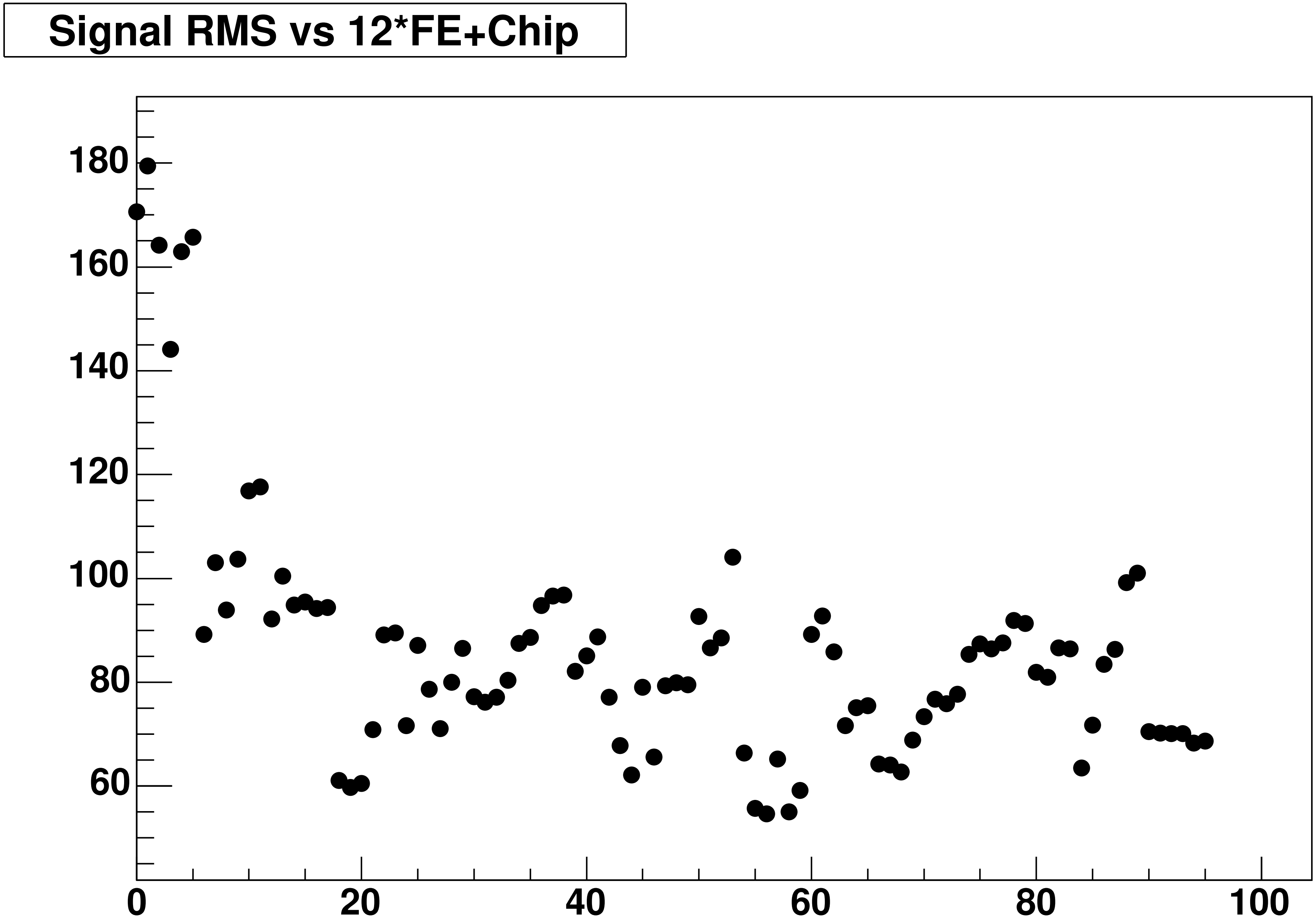

Pedestal vs 12*FE+Chip
40
30
20
10
0
-10
-20
-30
-40
0
20
40
60
80
100


Pedestal RMS vs 12*FE+Chip
1.4
1.2
1
0.8
0.6
0
20
40
60
80
100


Raw signal vs 12*FE+Chip
12800
12700
12600
12500
12400
12300
12200
12100
0
20
40
60
80
100


Raw signal RMS vs 12*FE+Chip
180
160
140
120
100
80
60
0
20
40
60
80
100


Signal vs 12*FE+Chip
12800
12700
12600
12500
12400
12300
12200
12100
0
20
40
60
80
100



Signal RMS vs 12*FE+Chip
180
160
140
120
100
80
60
0
20
40
60
80
100