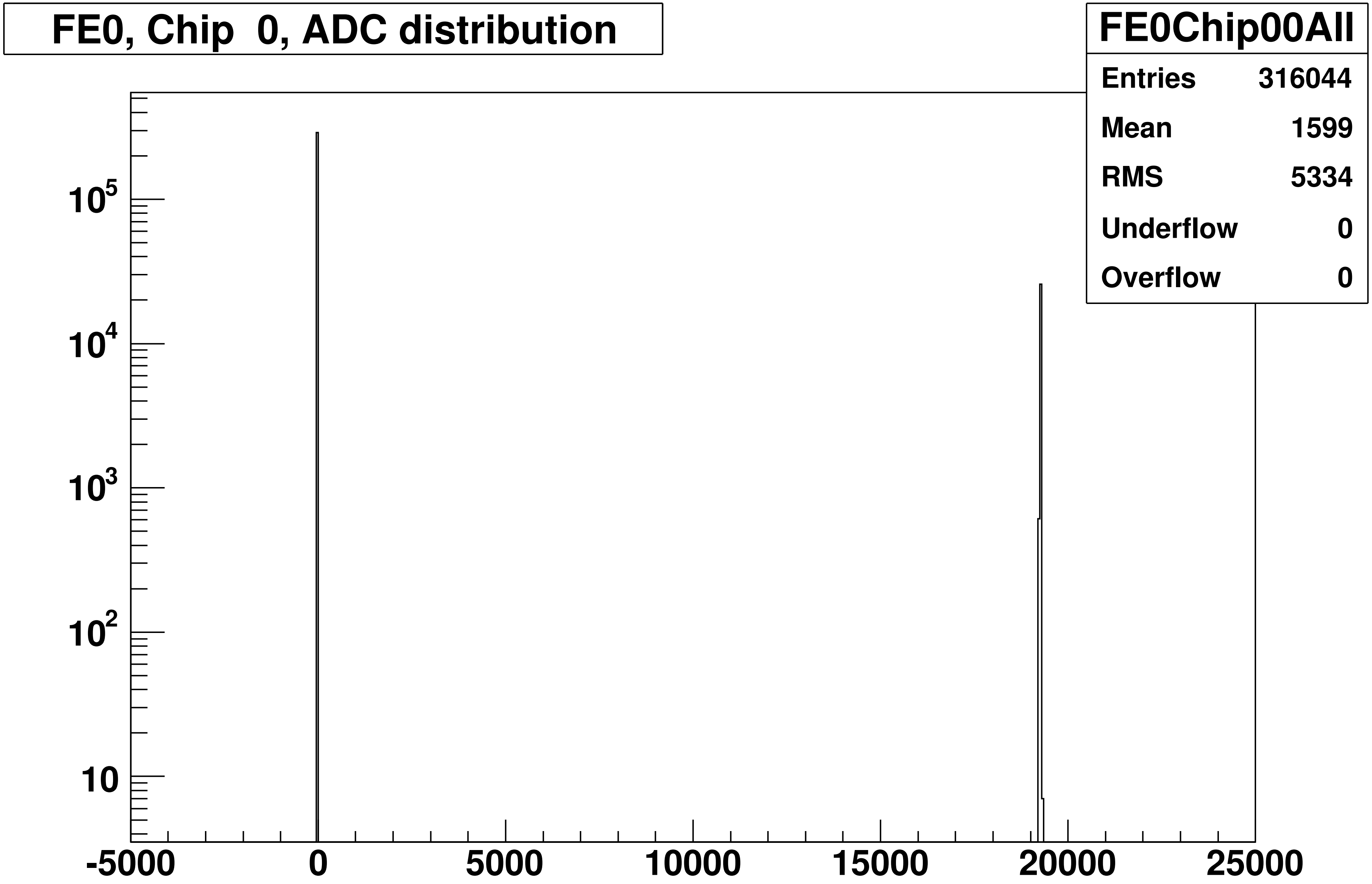
FE0, Chip 0, ADC distribution
FE0Chip00All
Entries 316044
Mean 1599
RMS 5334
Underflow 0
Overflow 0
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10^4
10^3
10^2
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-5000
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20000
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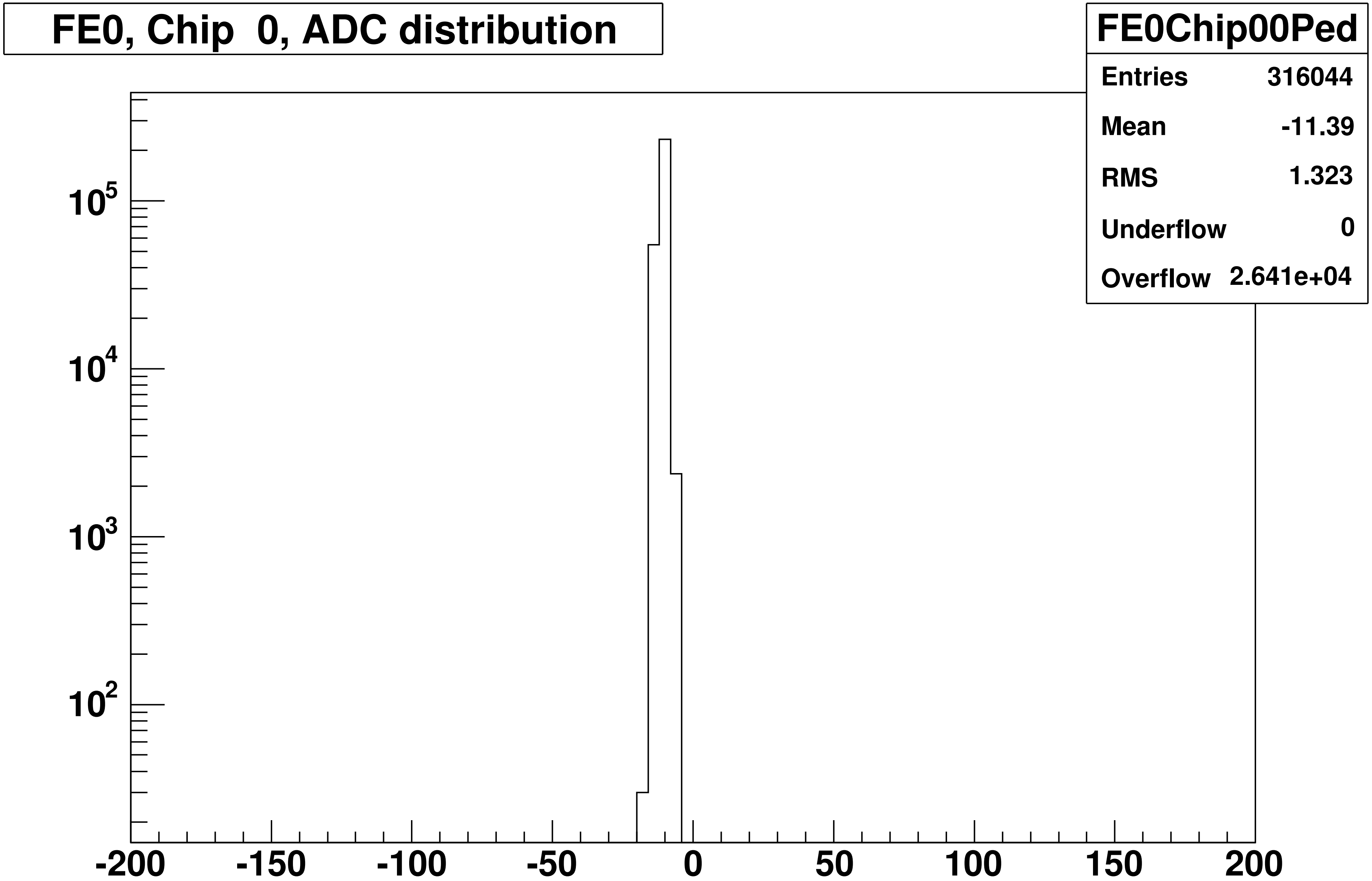

FE0, Chip 0, ADC distribution
FE0Chip00Ped
Entries 316044
Mean -11.39
RMS 1.323
Underflow 0
Overflow 2.641e+04
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10^4
10^3
10^2
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150
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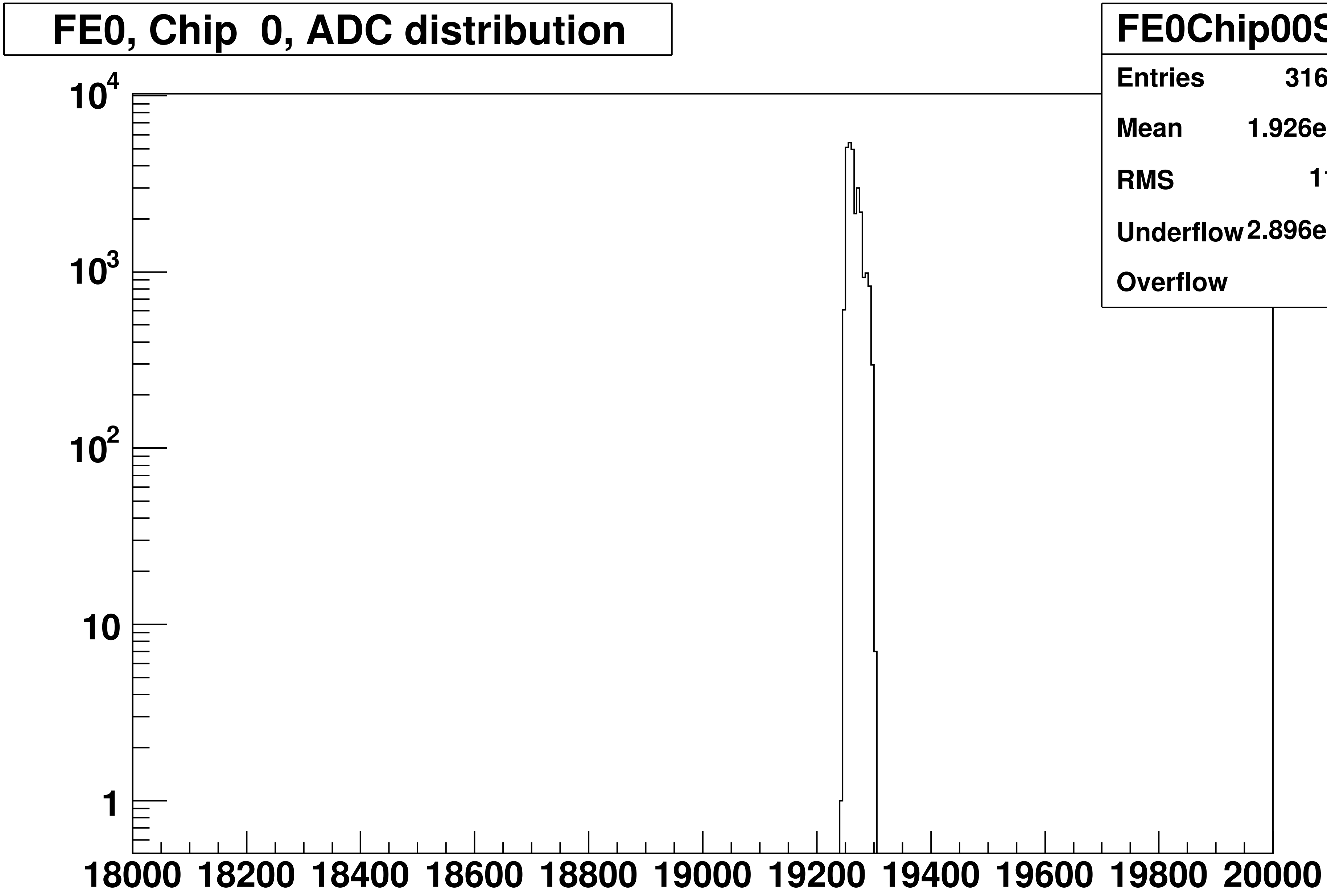
FE0, Chip 0, ADC distribution
FE0Chip00Sig
Entries 316044
Mean 1.926e+04
RMS 11.55
Underflow 2.896e+05
Overflow 0
10^4
10^3
10^2
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1
18000
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19000
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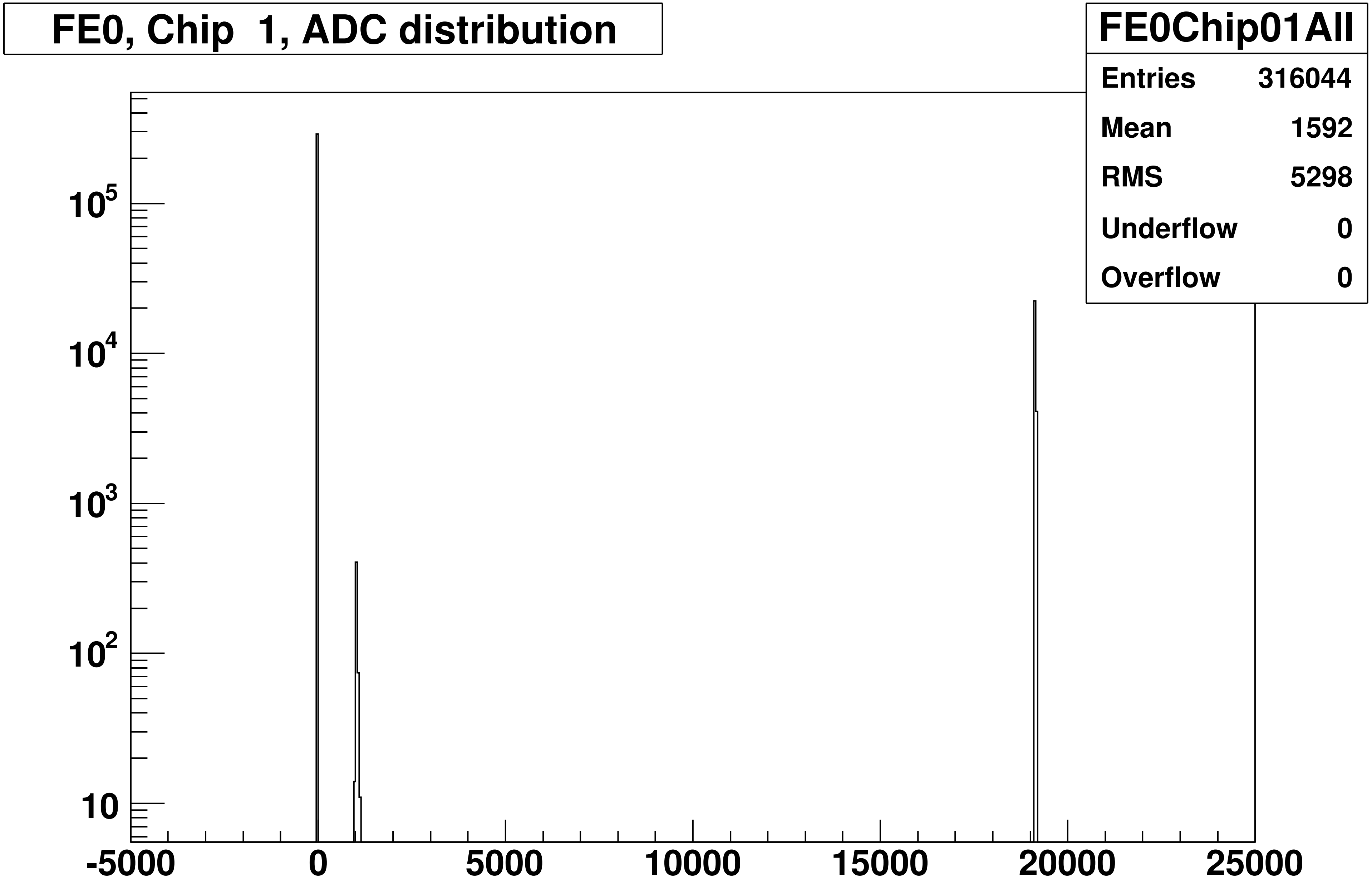
19400
19600
19800
20000


FE0, Chip 1, ADC distribution
FE0Chip01All
Entries 316044
Mean 1592
RMS 5298
Underflow 0
Overflow 0
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10^4
10^3
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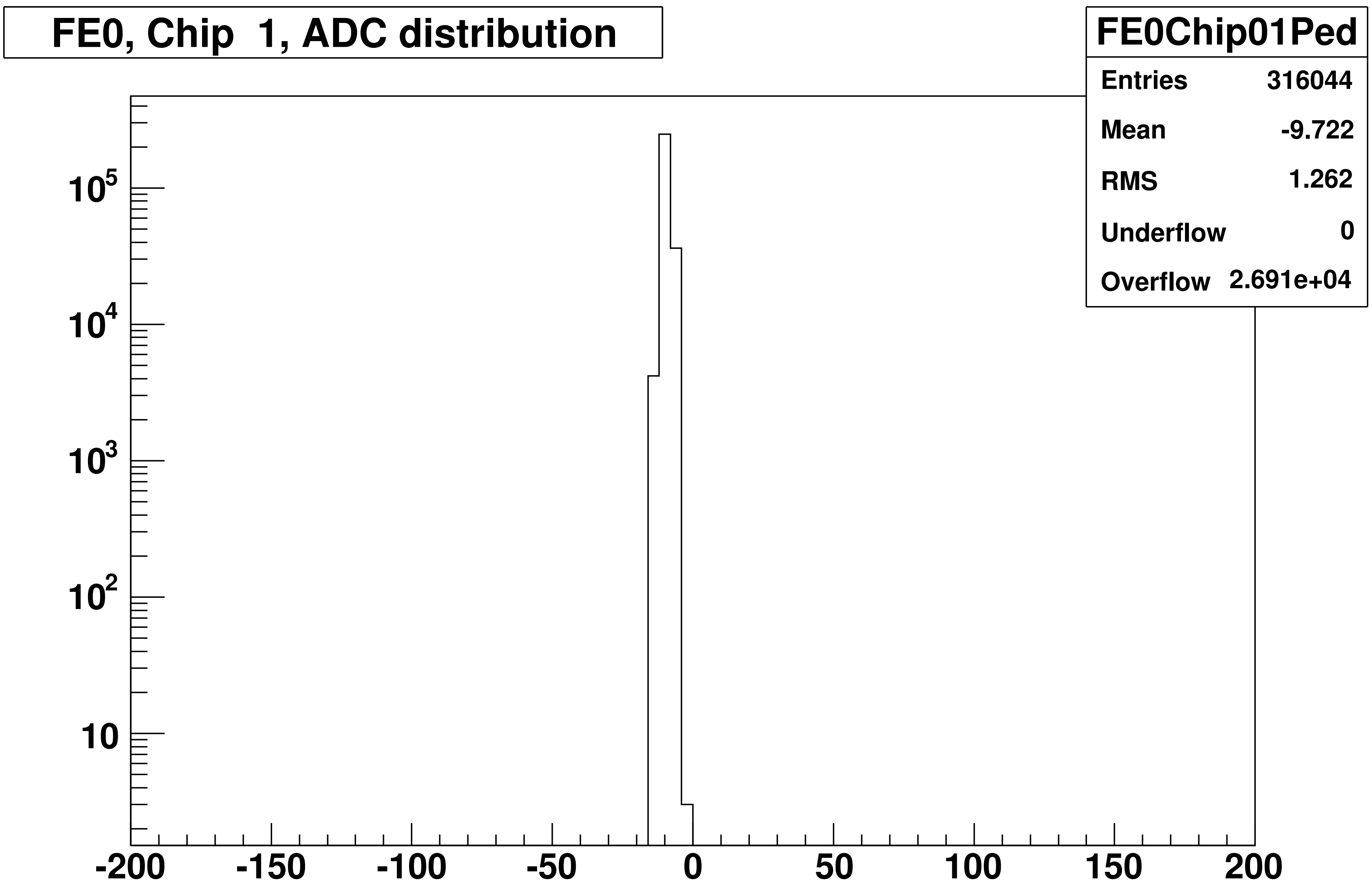
FE0, Chip 1, ADC distribution
FE0Chip01Ped
Entries 316044
Mean -9.722
RMS 1.262
Underflow 0
Overflow 2.691e+04
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10^4
10^3
10^2
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-100
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100
150
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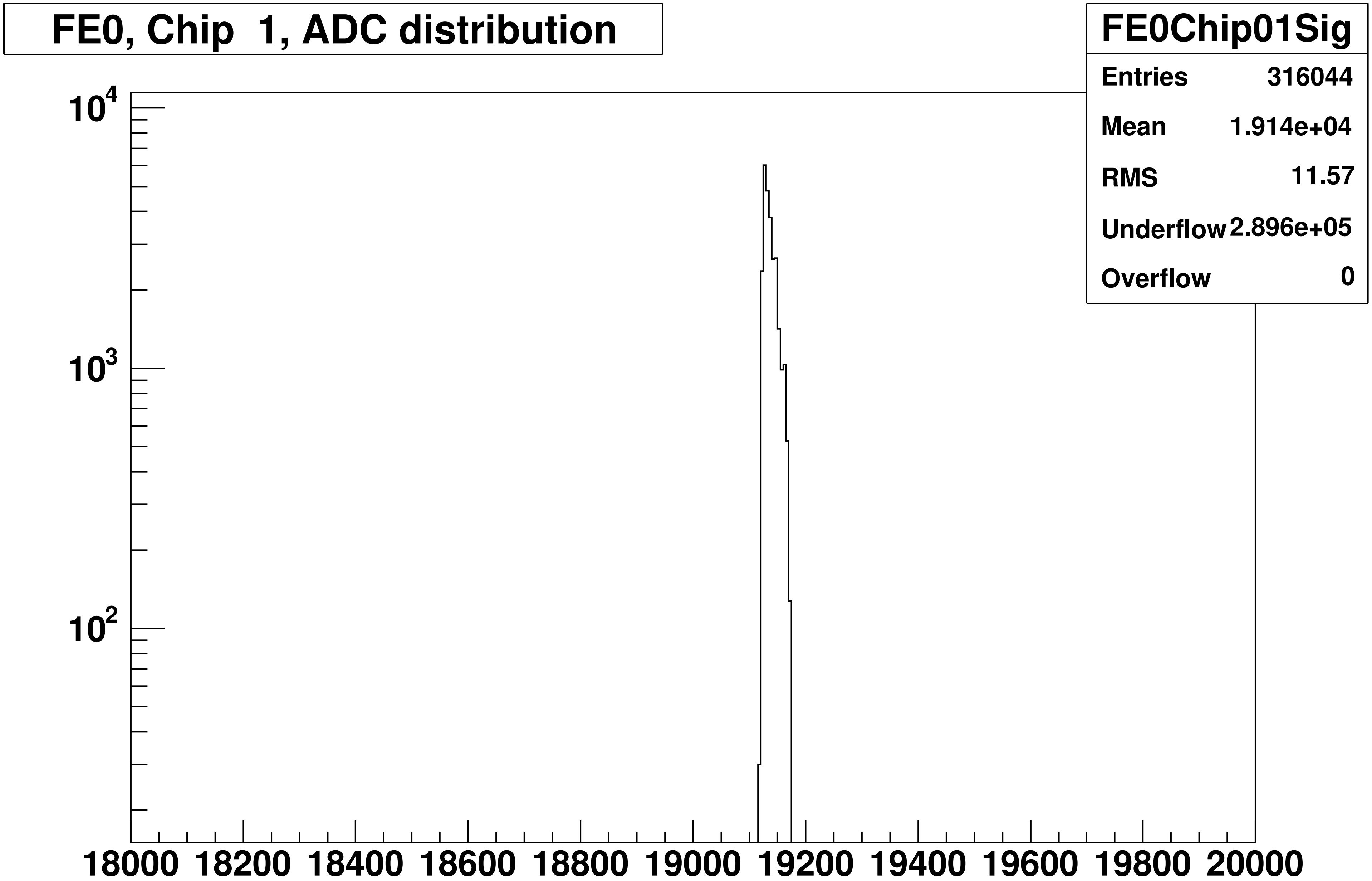
FE0, Chip 1, ADC distribution
FE0Chip01Sig
Entries 316044
Mean 1.914e+04
RMS 11.57
Underflow 2.896e+05
Overflow 0
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10^2
18000
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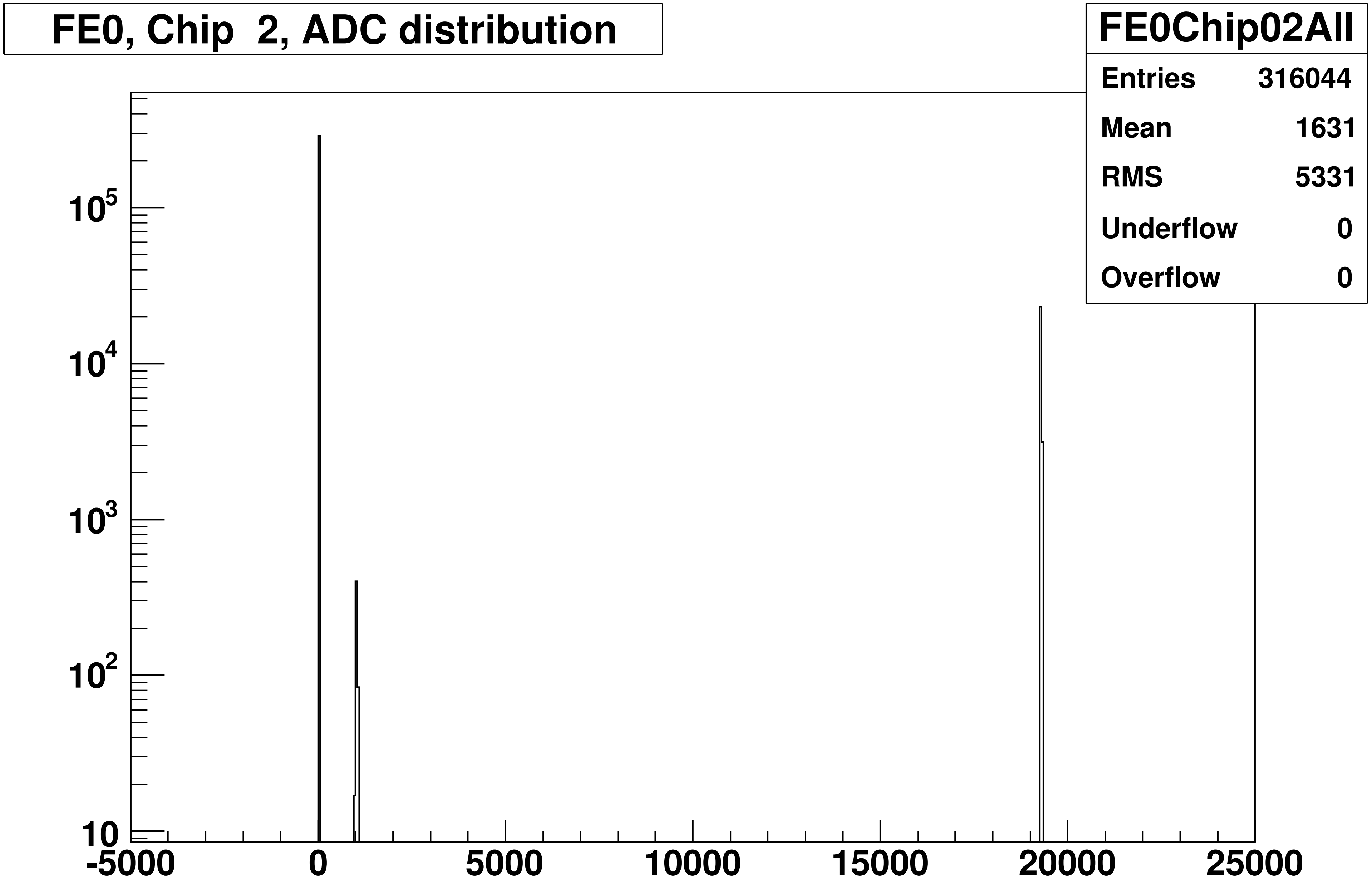
FE0, Chip 2, ADC distribution
FE0Chip02All
Entries 316044
Mean 1631
RMS 5331
Underflow 0
Overflow 0
10
10^2
10^3
10^4
10^5
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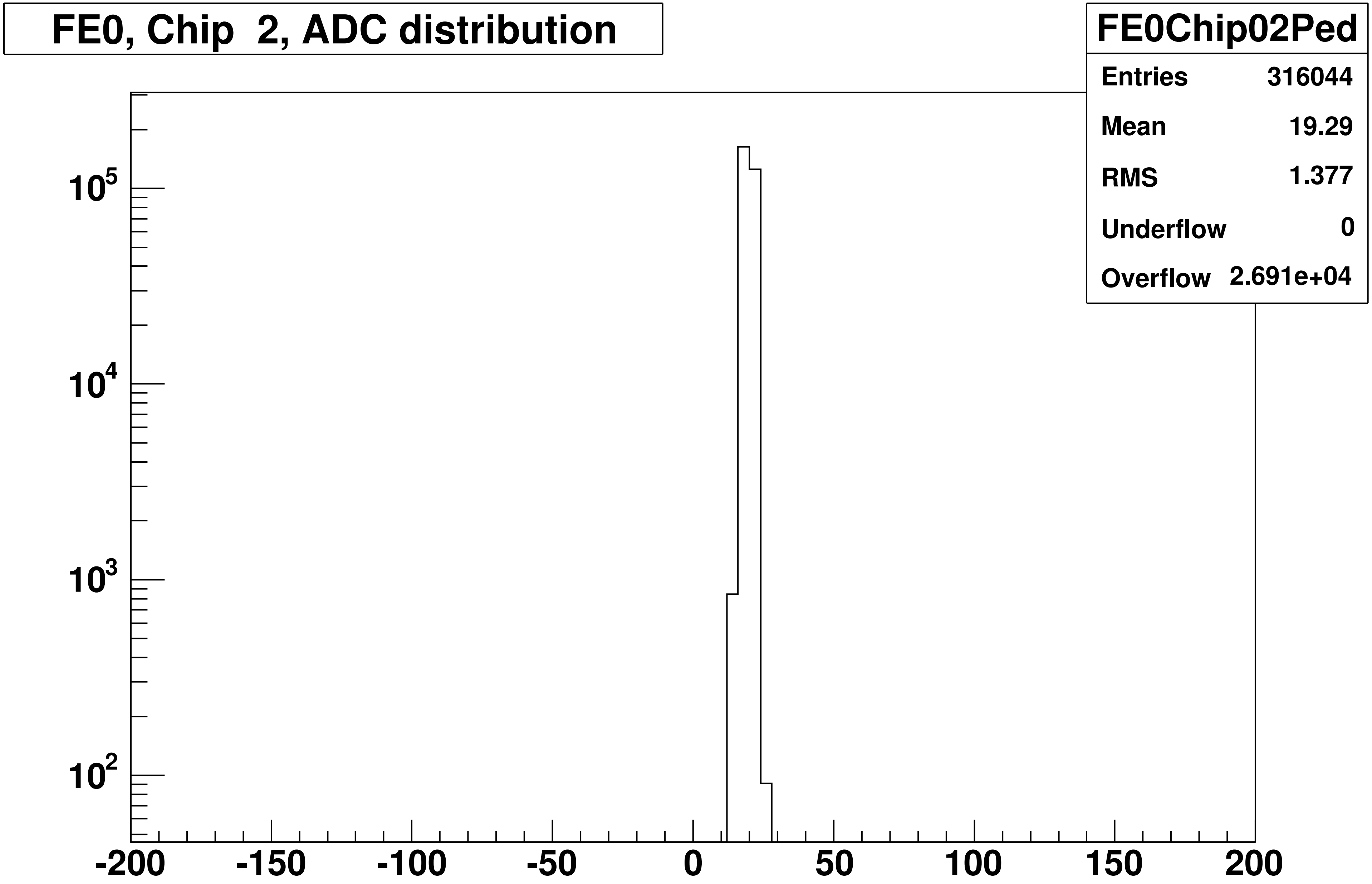
FE0, Chip 2, ADC distribution
FE0Chip02Ped
Entries 316044
Mean 19.29
RMS 1.377
Underflow 0
Overflow 2.691e+04
10^5
10^4
10^3
10^2
-200
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-100
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0
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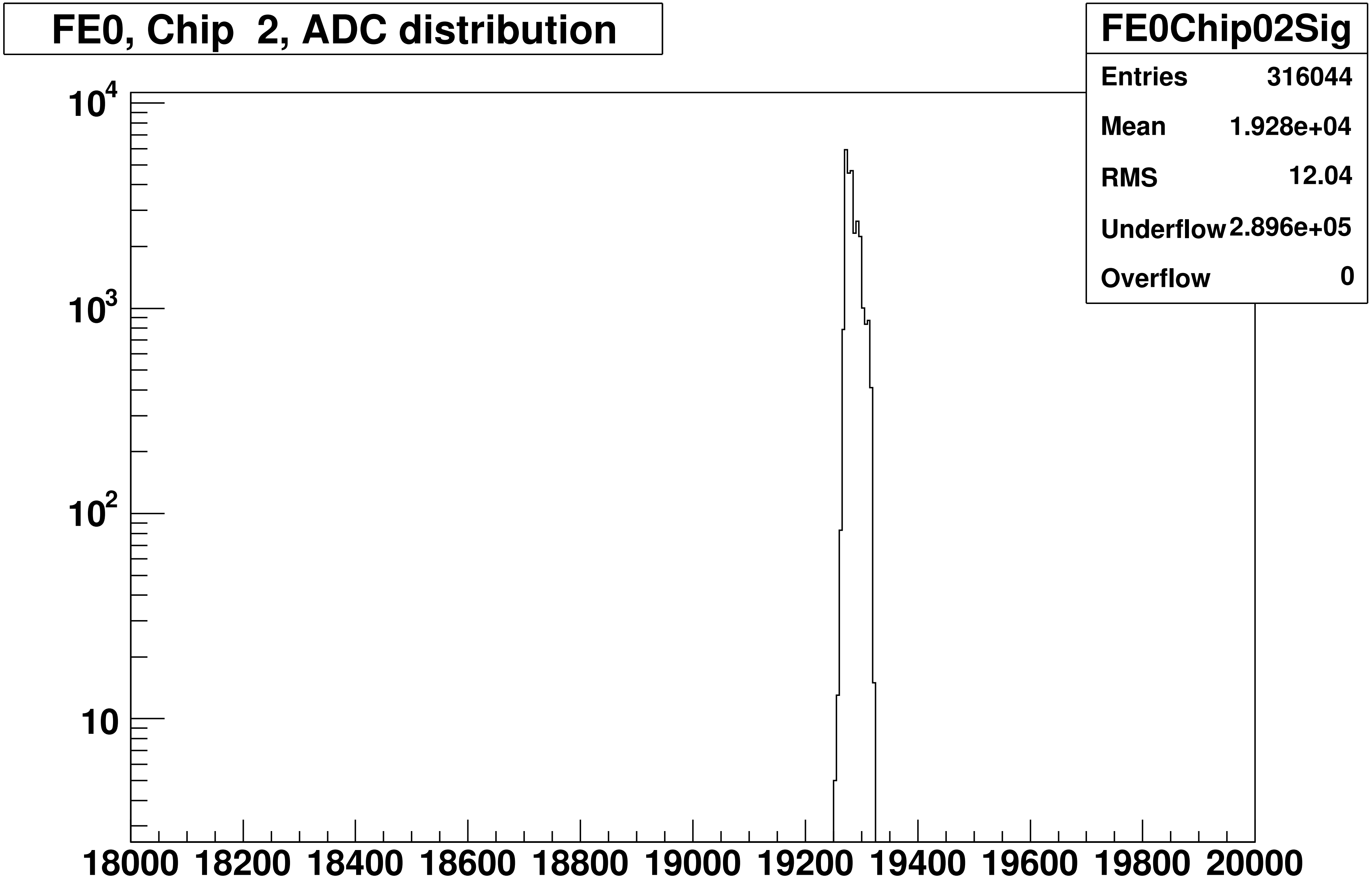
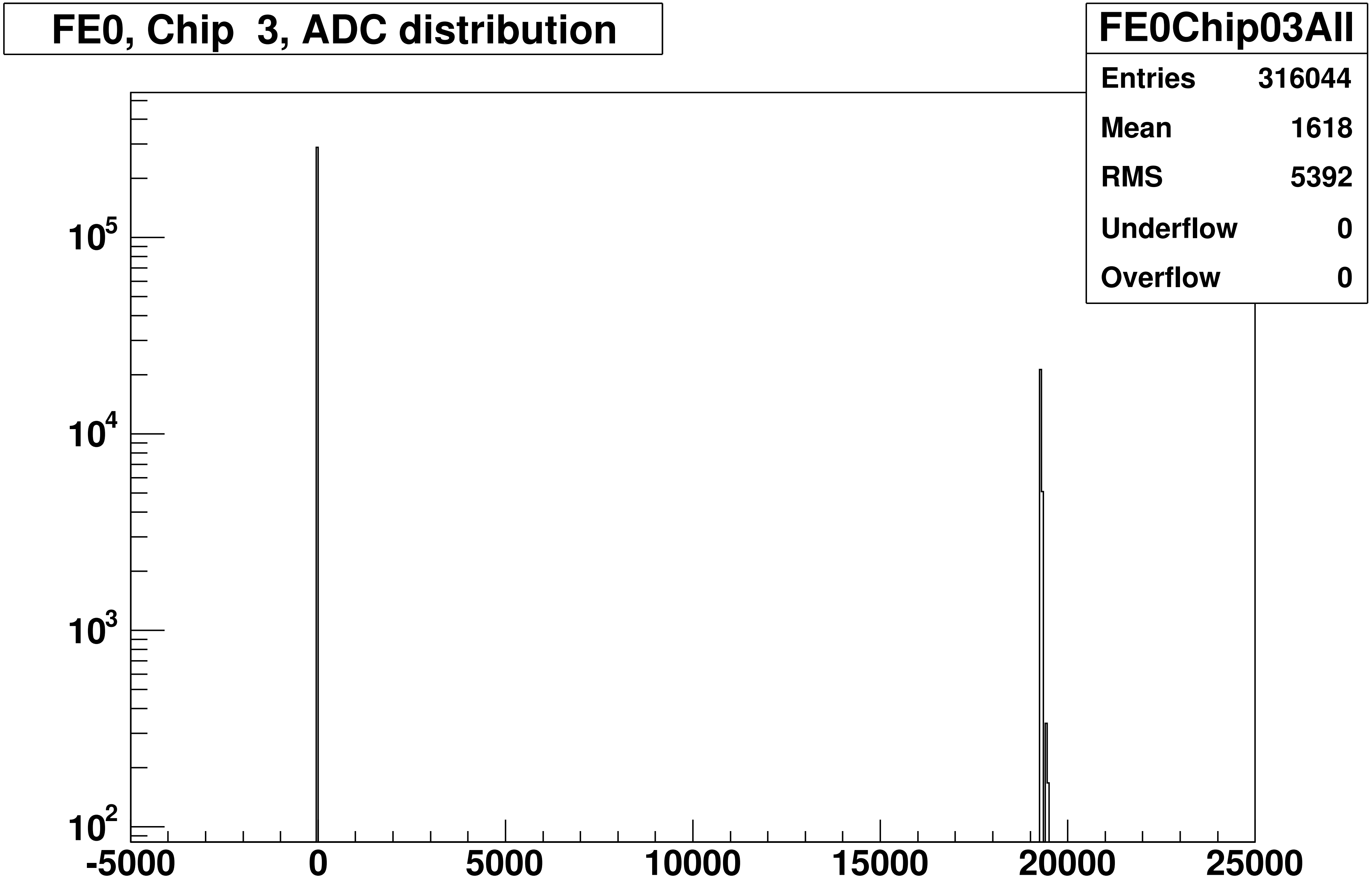
100
150
200



FE0, Chip 2, ADC distribution
FE0Chip02Sig
Entries 316044
Mean 1.928e+04
RMS 12.04
Underflow 2.896e+05
Overflow 0
10^4
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE0, Chip 3, ADC distribution
FE0Chip03All
Entries 316044
Mean 1618
RMS 5392
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
-5000
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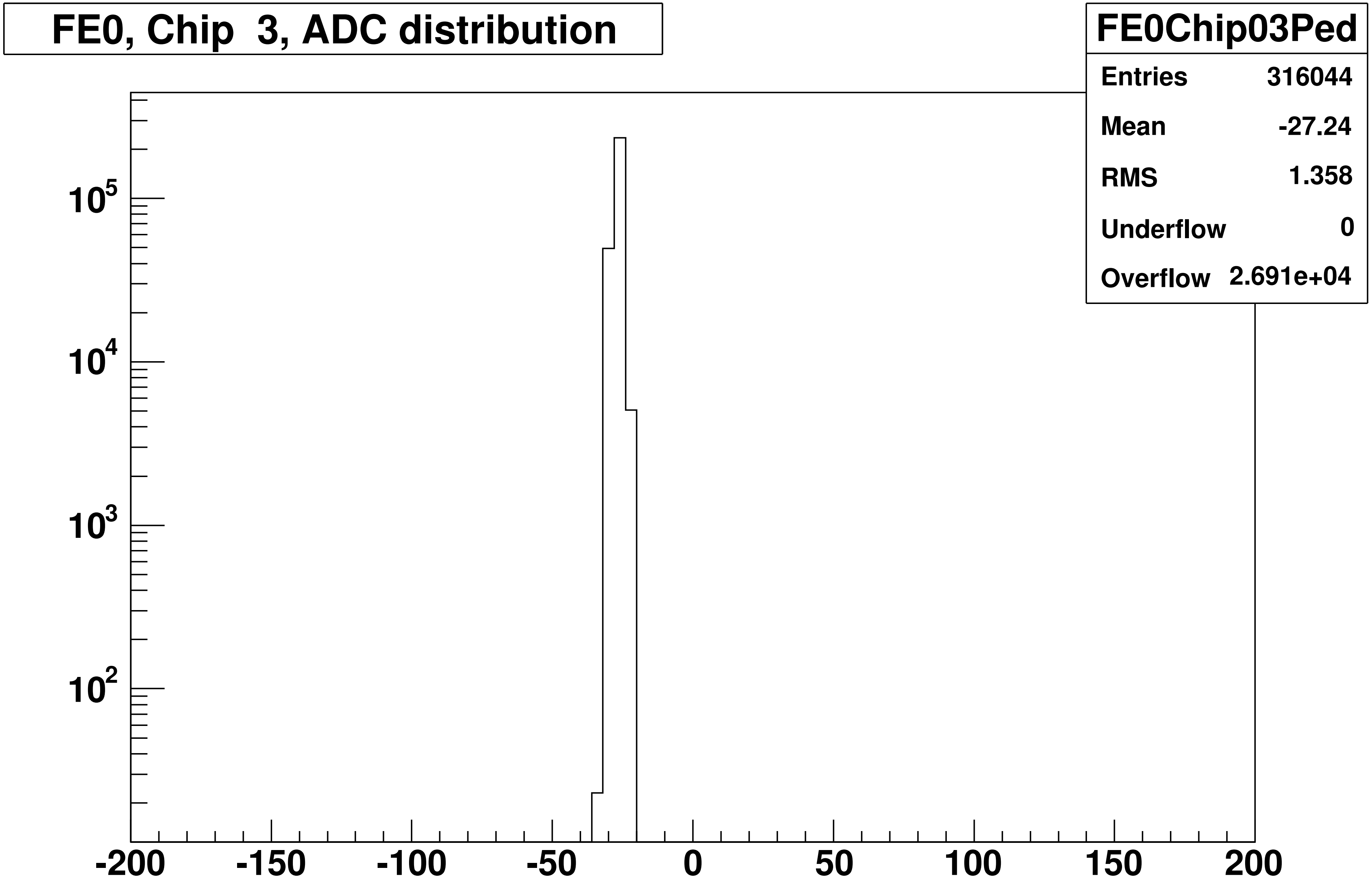
5000
10000
15000
20000
25000


FE0, Chip 3, ADC distribution
FE0Chip03Ped
Entries 316044
Mean -27.24
RMS 1.358
Underflow 0
Overflow 2.691e+04
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10^4
10^3
10^2
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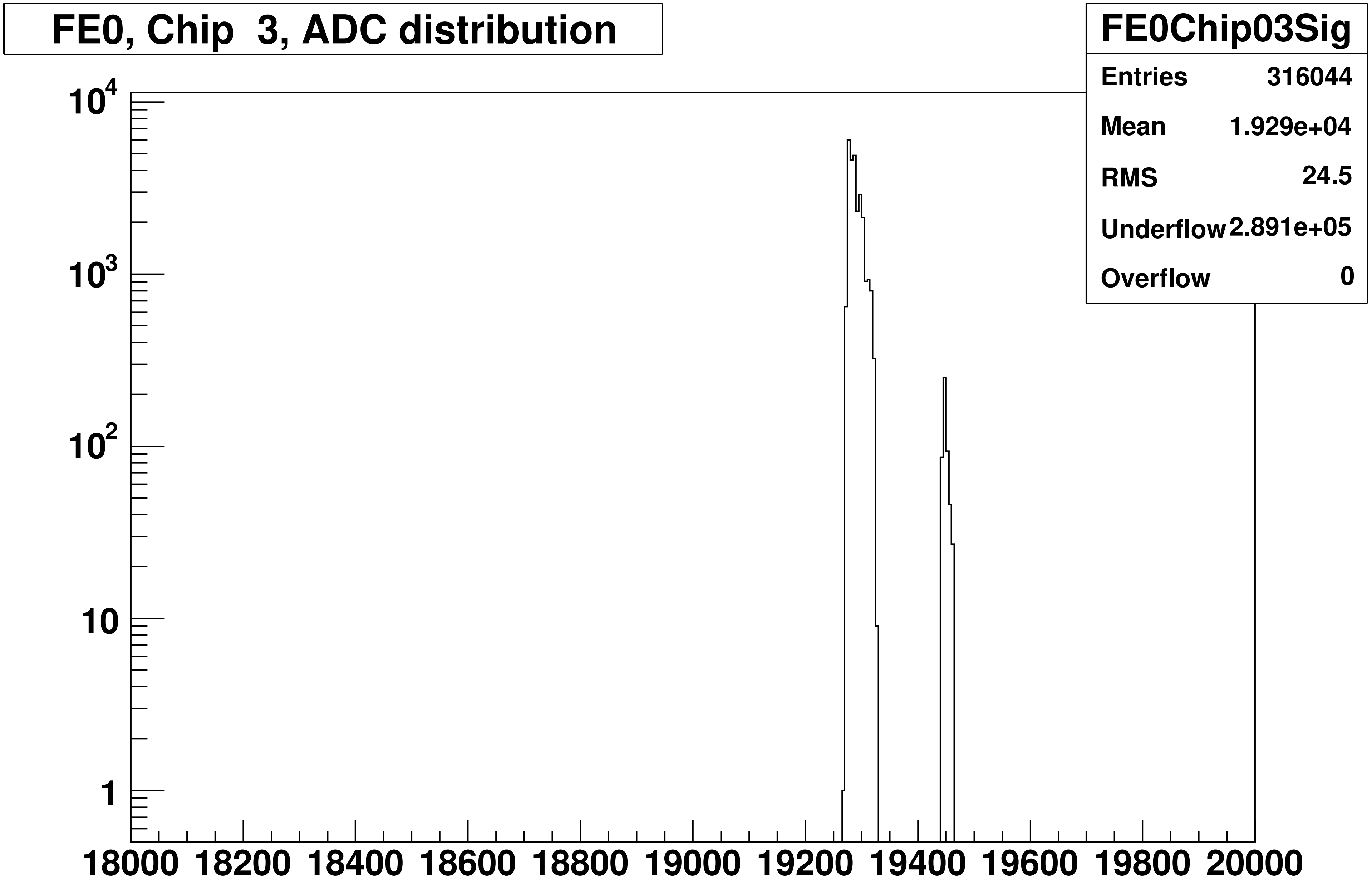
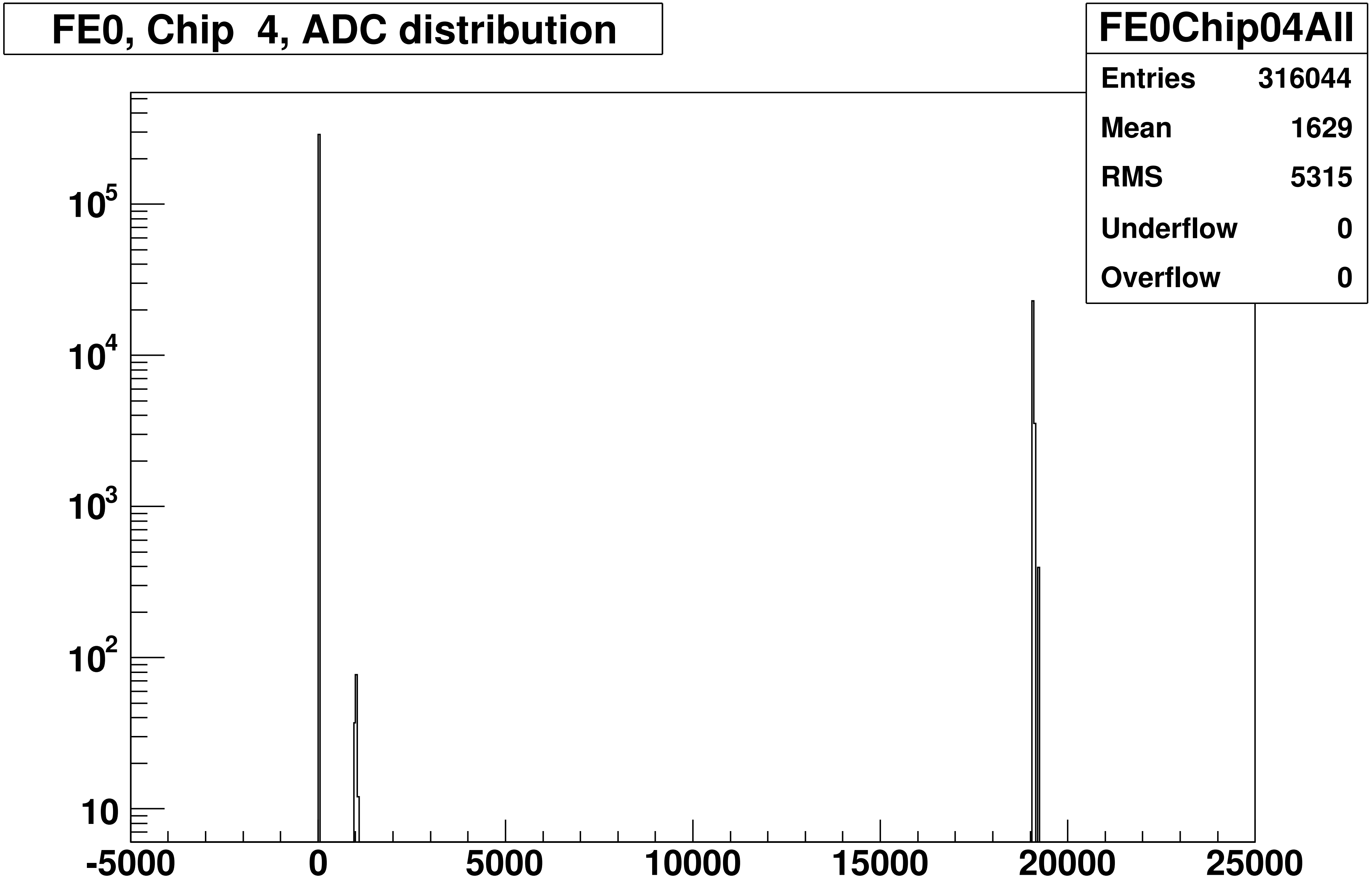
150
200


FE0, Chip 3, ADC distribution
FE0Chip03Sig
Entries 316044
Mean 1.929e+04
RMS 24.5
Underflow 2.891e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE0, Chip 4, ADC distribution
FE0Chip04All
Entries 316044
Mean 1629
RMS 5315
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
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0
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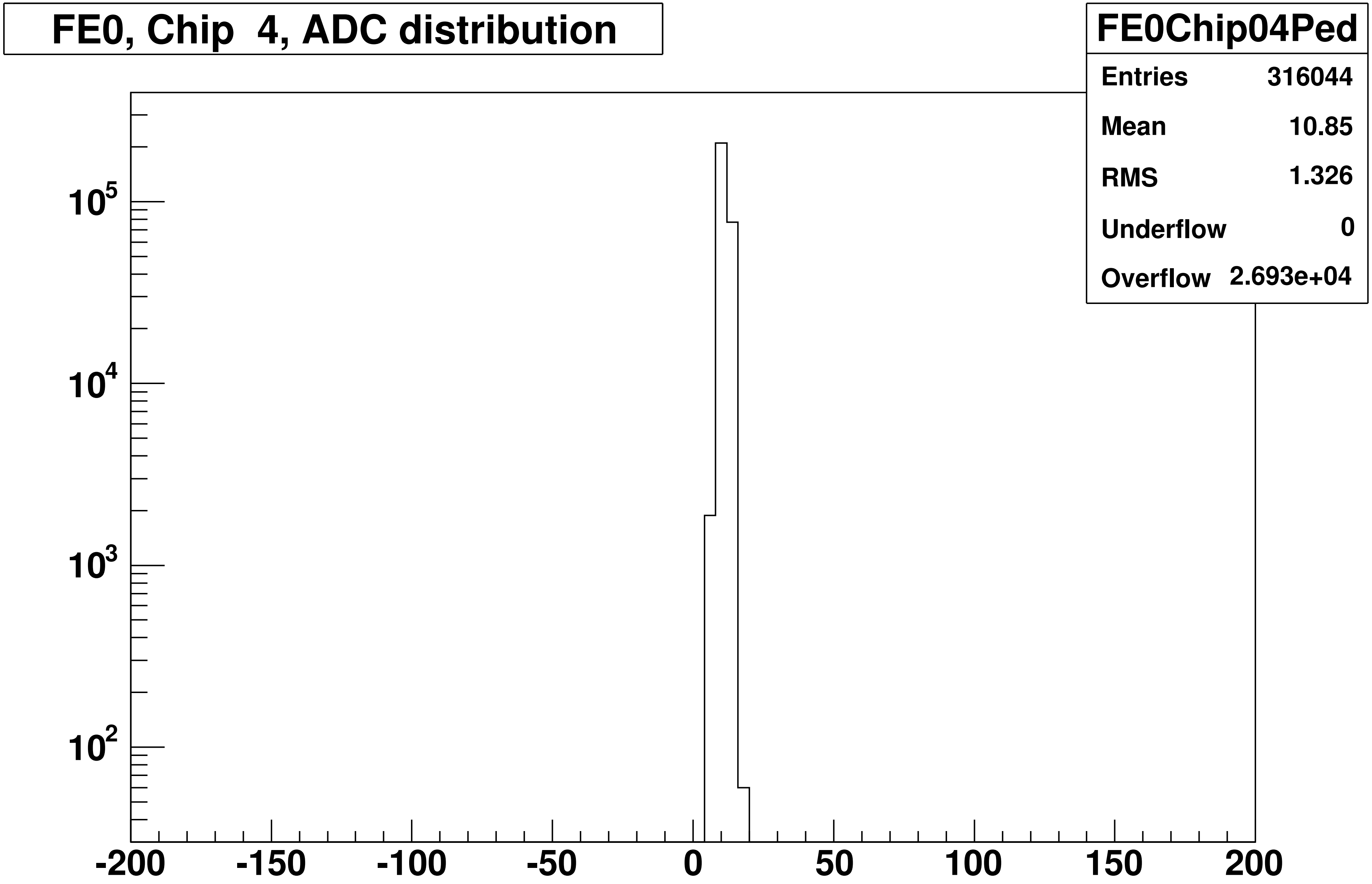
10000
15000
20000
25000


FE0, Chip 4, ADC distribution
FE0Chip04Ped
Entries 316044
Mean 10.85
RMS 1.326
Underflow 0
Overflow 2.693e+04
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10^4
10^3
10^2
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-100
-50
0
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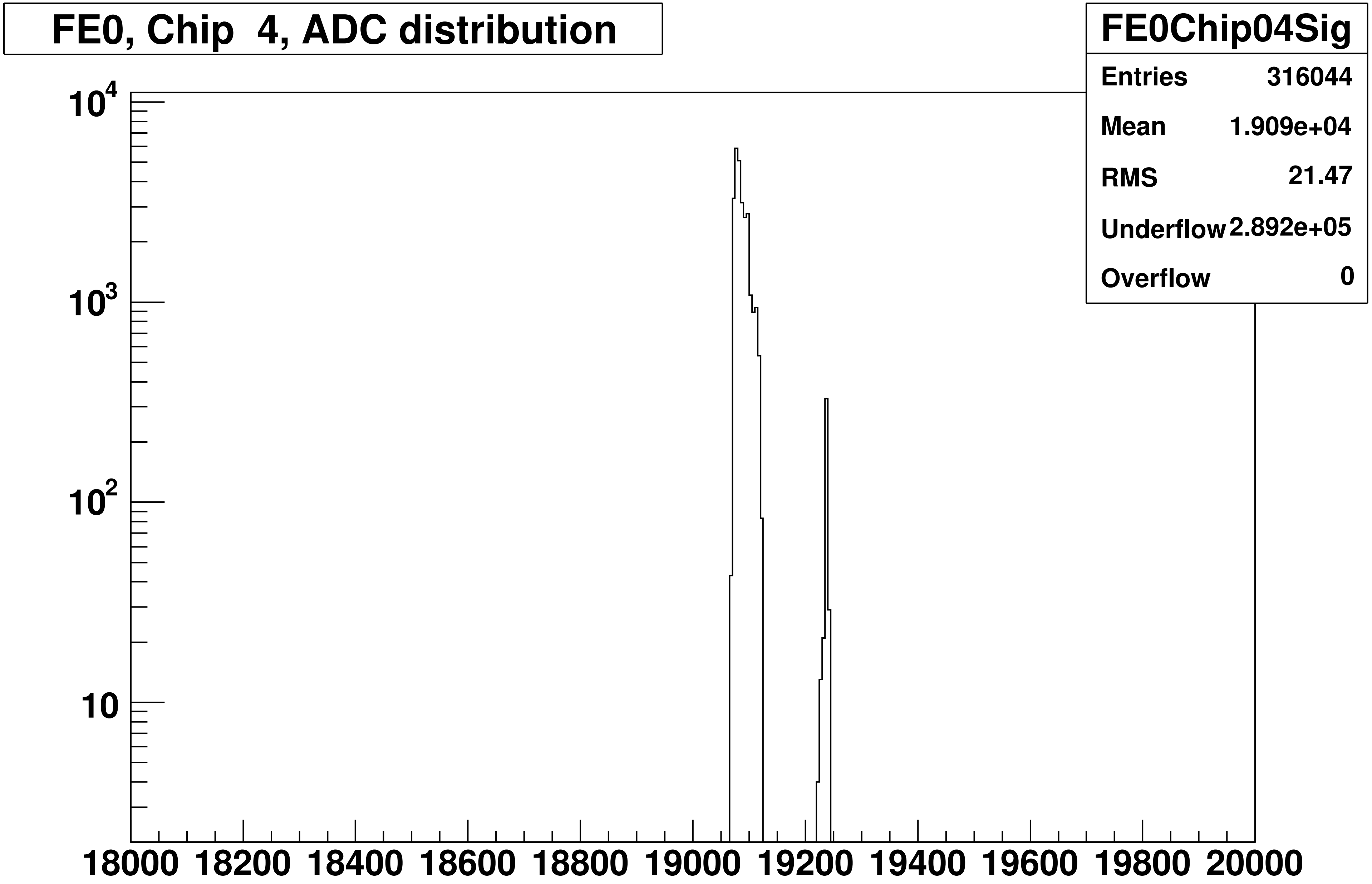
100
150
200


FE0, Chip 4, ADC distribution
FE0Chip04Sig
Entries 316044
Mean 1.909e+04
RMS 21.47
Underflow 2.892e+05
Overflow 0
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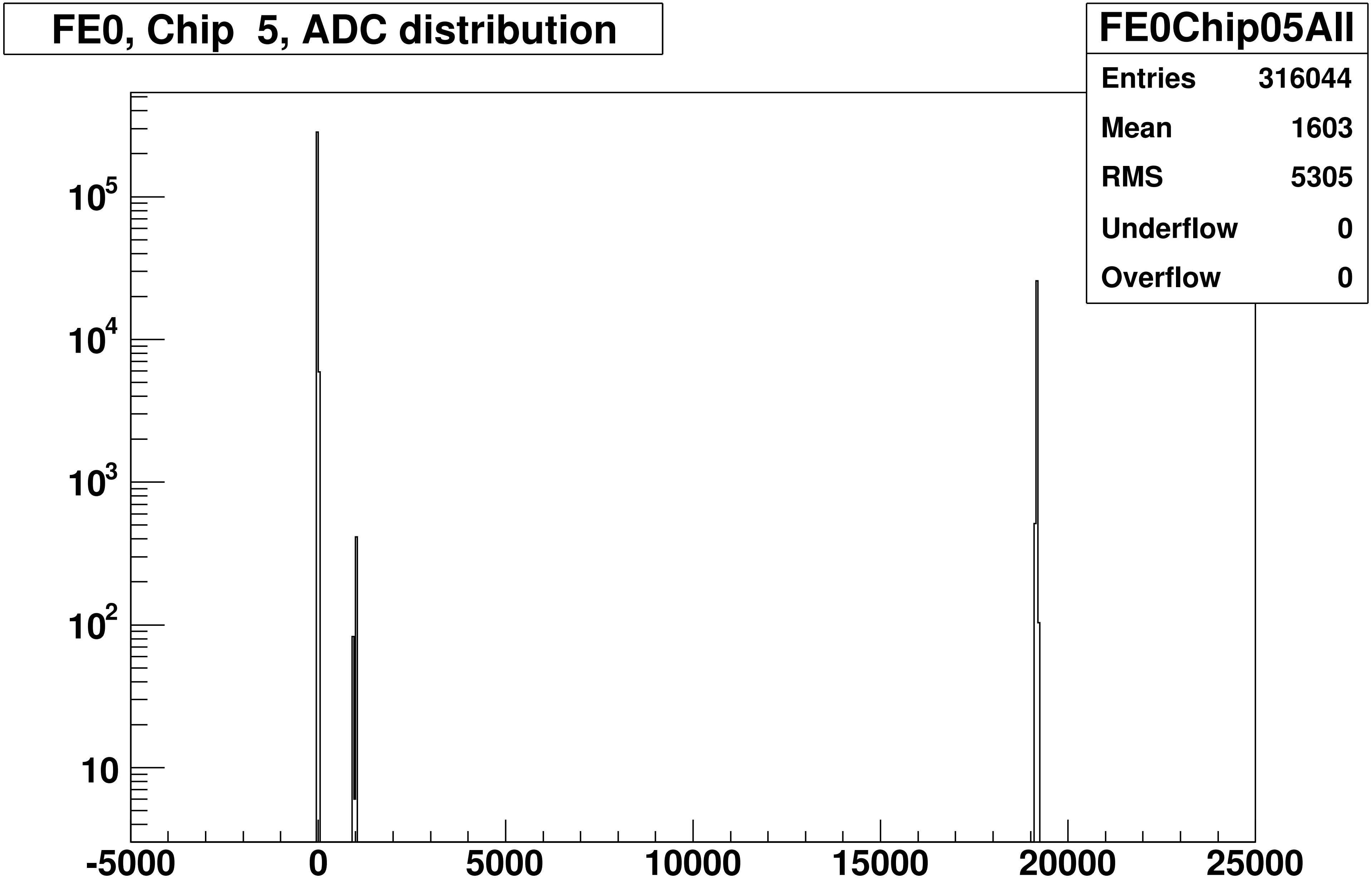
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE0, Chip 5, ADC distribution
FE0Chip05All
Entries 316044
Mean 1603
RMS 5305
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
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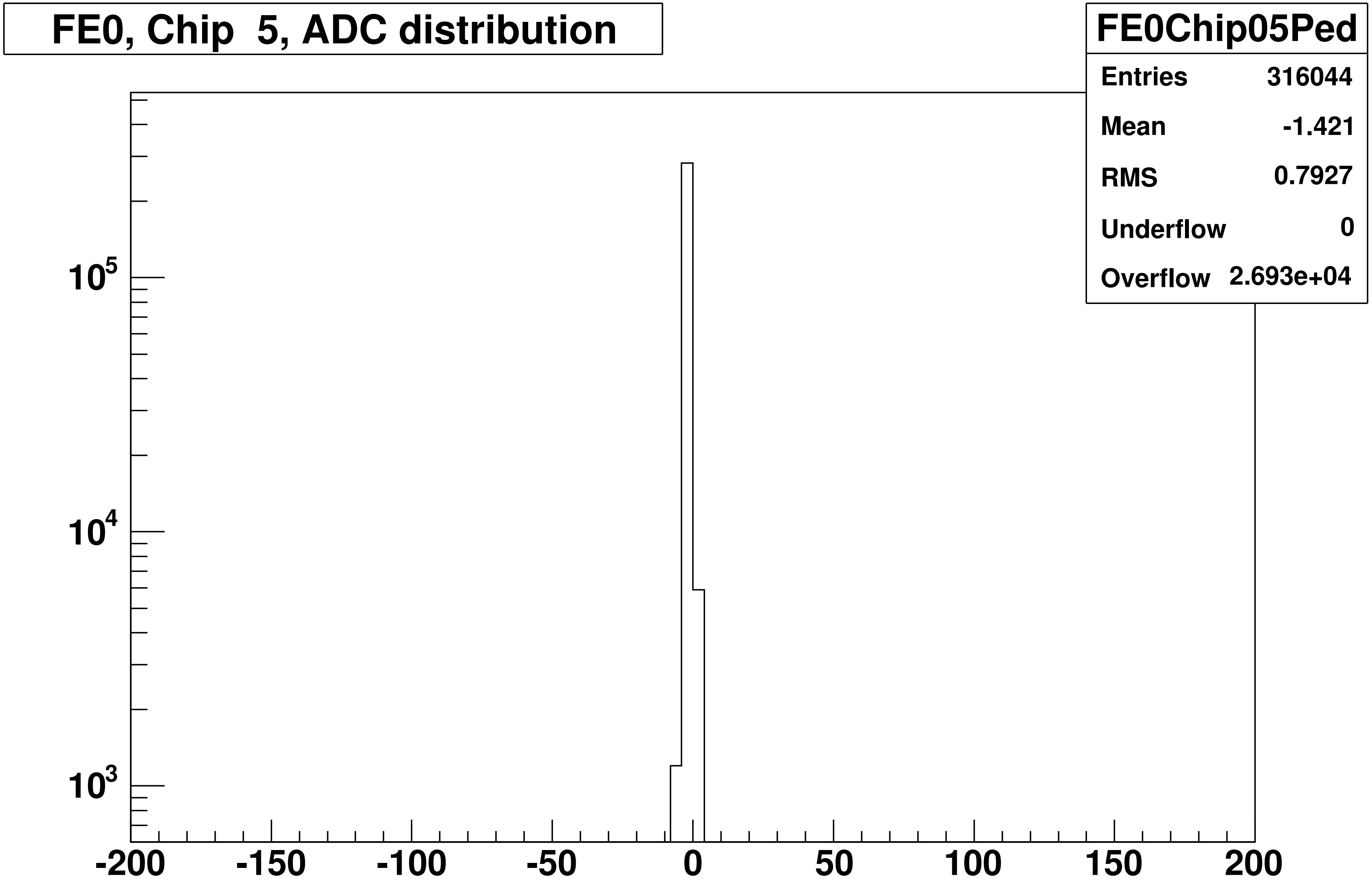
-5000
0
5000
10000
15000
20000
25000


FE0, Chip 5, ADC distribution
FE0Chip05Ped
Entries 316044
Mean -1.421
RMS 0.7927
Underflow 0
Overflow 2.693e+04
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10^4
10^3
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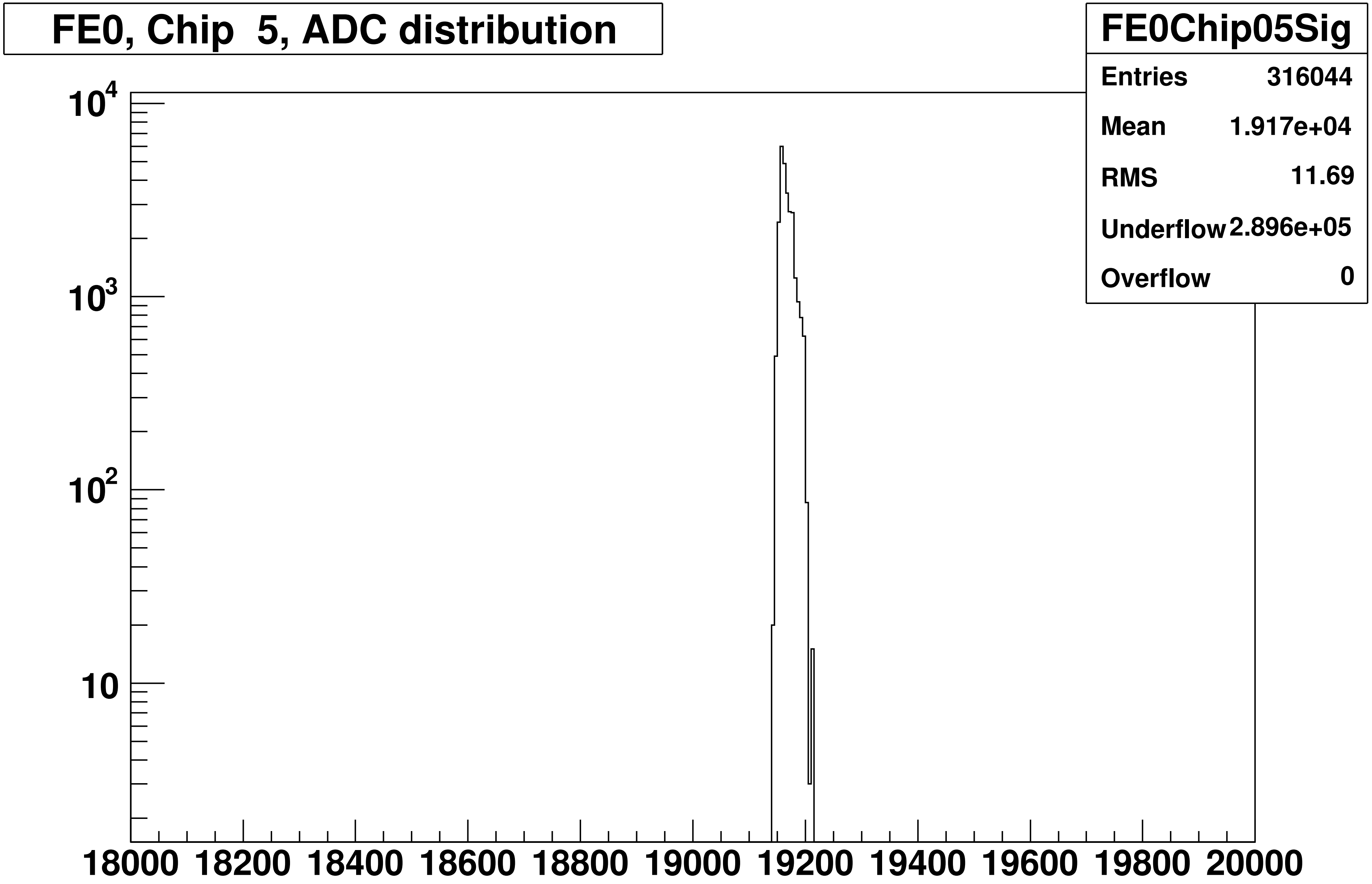
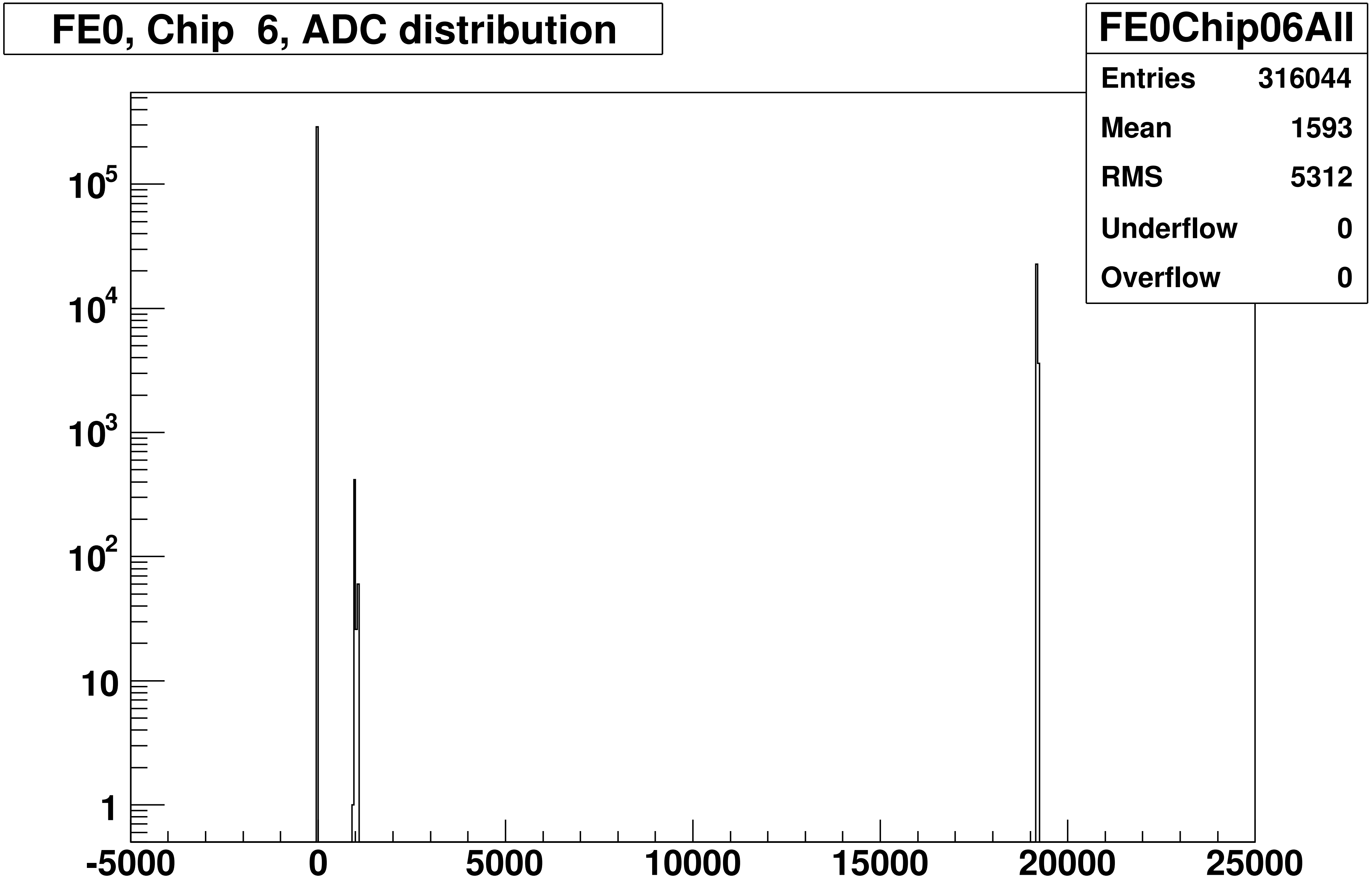
-100
-50
0
50
100
150
200



FE0, Chip 5, ADC distribution
FE0Chip05Sig
Entries 316044
Mean 1.917e+04
RMS 11.69
Underflow 2.896e+05
Overflow 0
10^4
10^3
10^2
10
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000


FE0, Chip 6, ADC distribution
FE0Chip06All
Entries 316044
Mean 1593
RMS 5312
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
1
-5000
0
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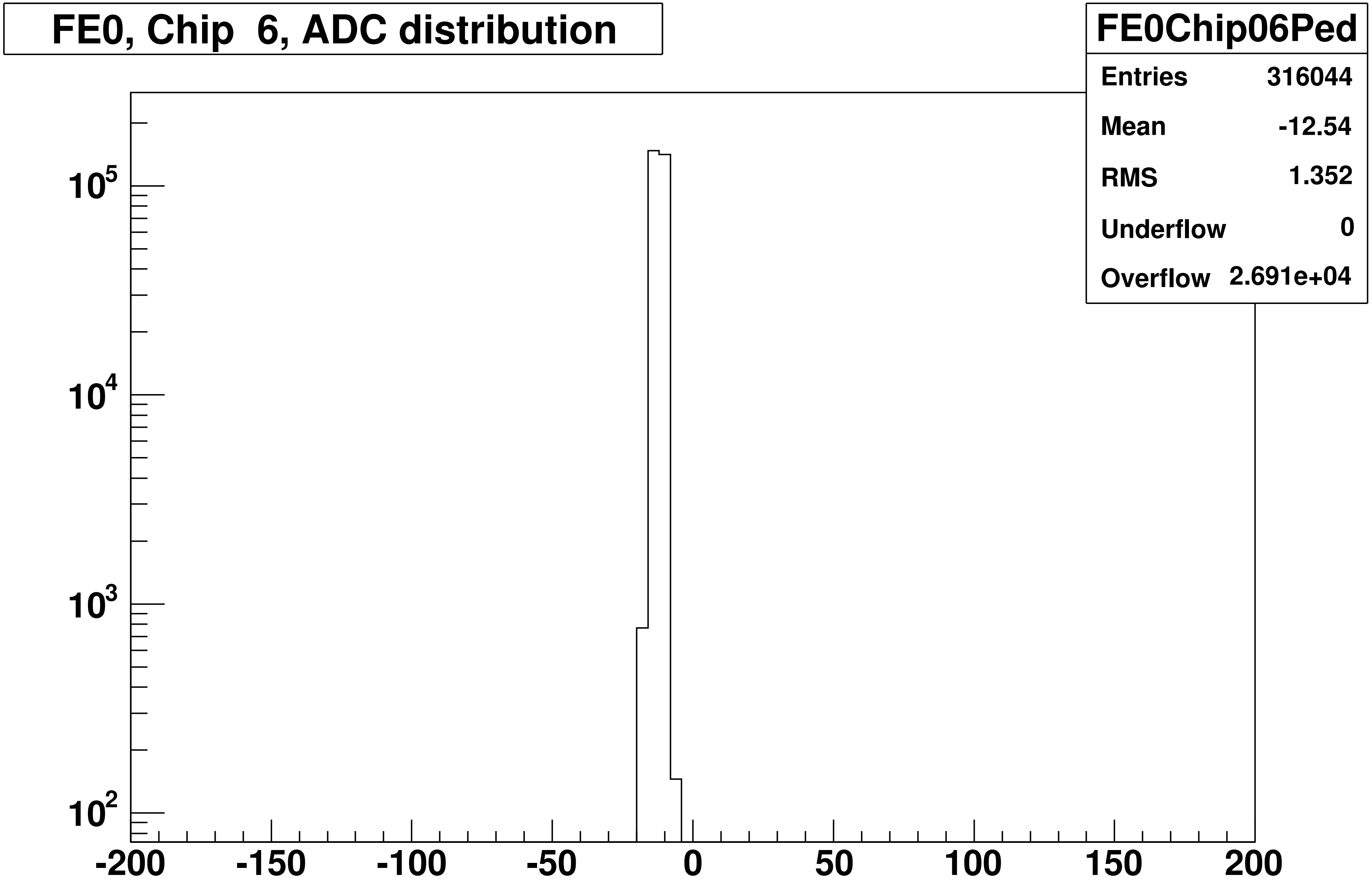
10000
15000
20000
25000


FE0, Chip 6, ADC distribution
FE0Chip06Ped
Entries 316044
Mean -12.54
RMS 1.352
Underflow 0
Overflow 2.691e+04
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10^4
10^3
10^2
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-100
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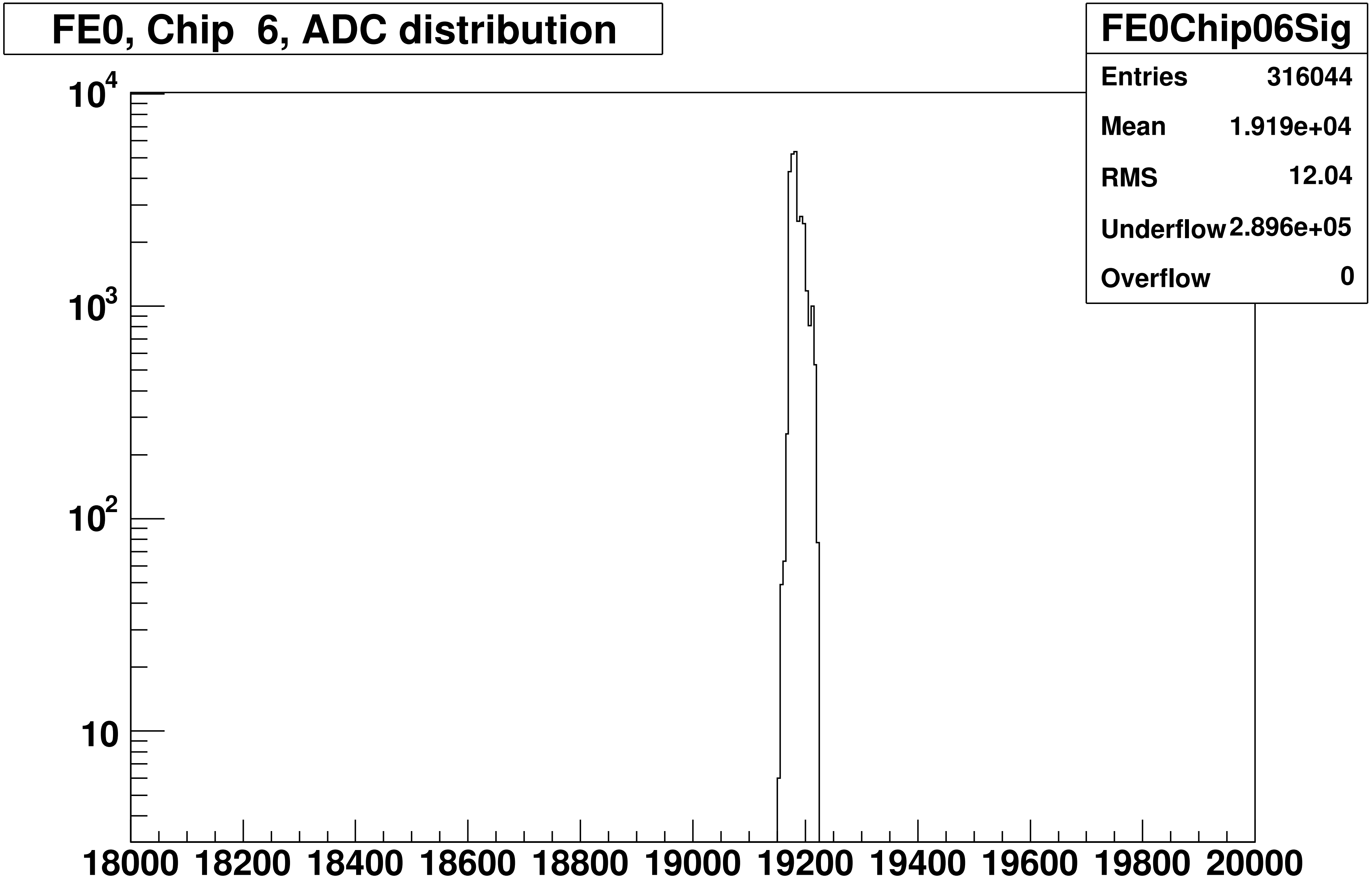
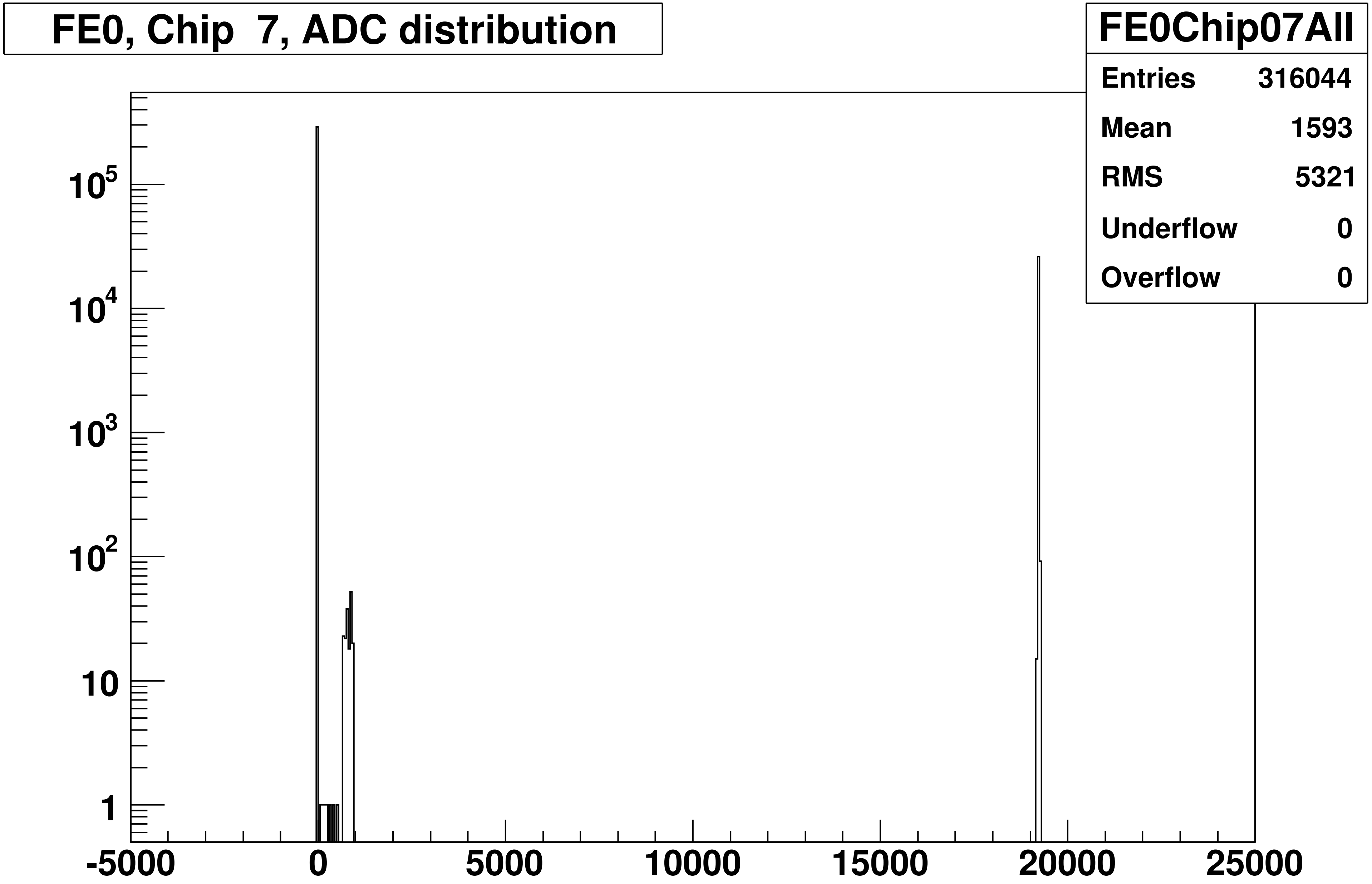
100
150
200


FE0, Chip 6, ADC distribution
FE0Chip06Sig
Entries 316044
Mean 1.919e+04
RMS 12.04
Underflow 2.896e+05
Overflow 0
10^4
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE0, Chip 7, ADC distribution
FE0Chip07All
Entries 316044
Mean 1593
RMS 5321
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
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0
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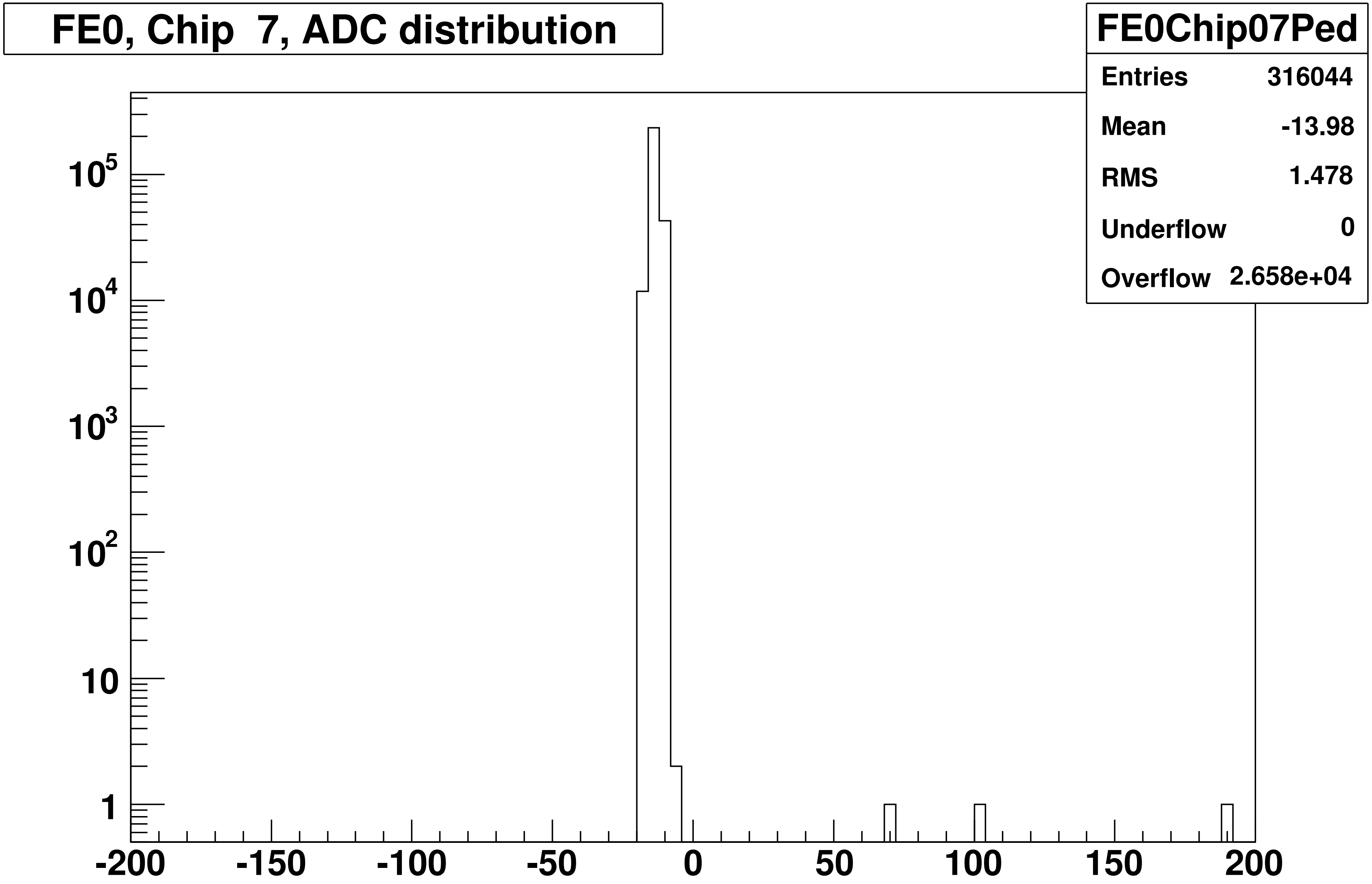
10000
15000
20000
25000


FE0, Chip 7, ADC distribution
FE0Chip07Ped
Entries 316044
Mean -13.98
RMS 1.478
Underflow 0
Overflow 2.658e+04
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10^3
10^2
10
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150
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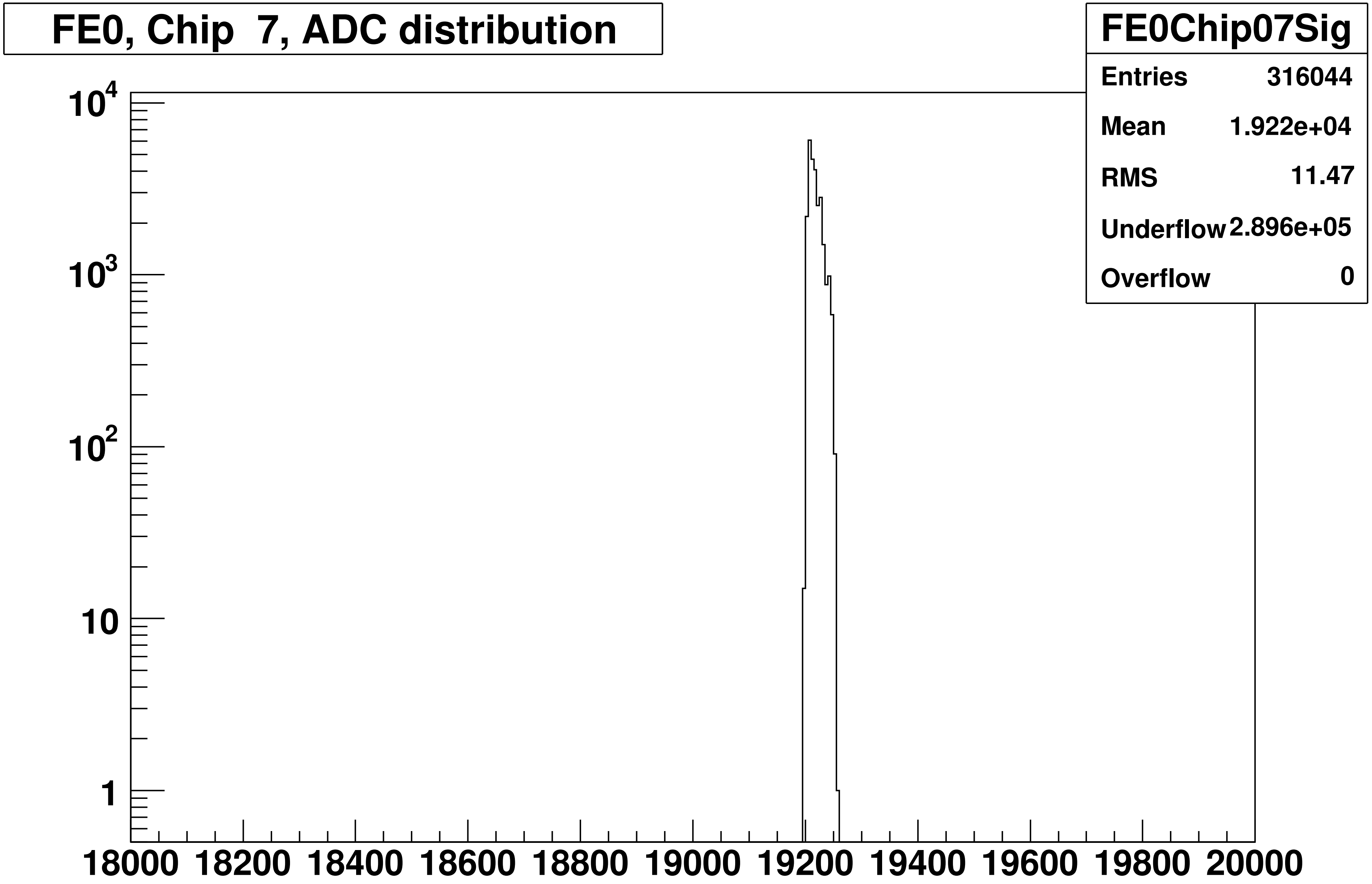
FE0, Chip 7, ADC distribution
FE0Chip07Sig
Entries 316044
Mean 1.922e+04
RMS 11.47
Underflow 2.896e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
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18400
18600
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19000
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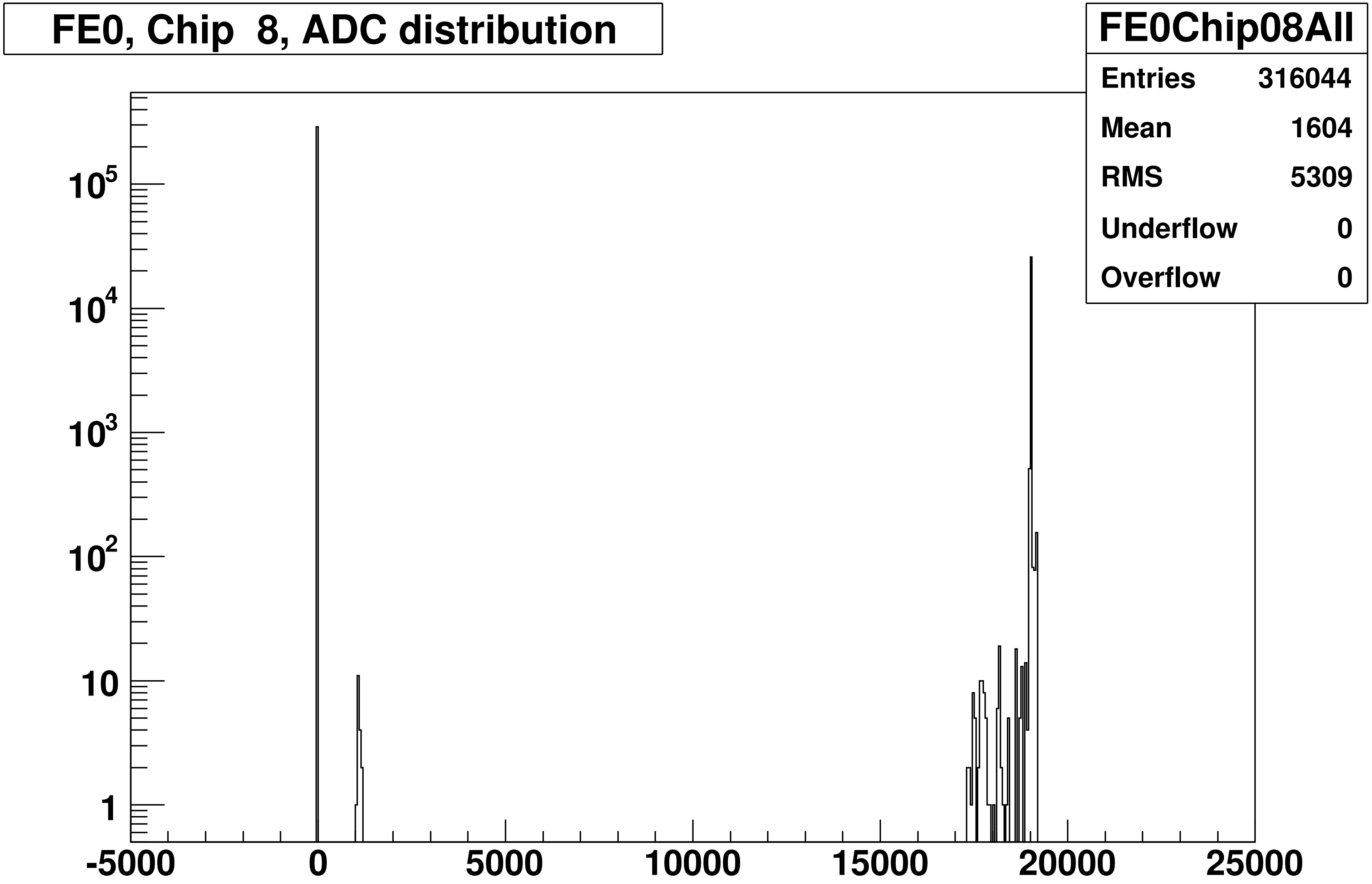
19600
19800
20000


FE0, Chip 8, ADC distribution
FE0Chip08All
Entries 316044
Mean 1604
RMS 5309
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
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0
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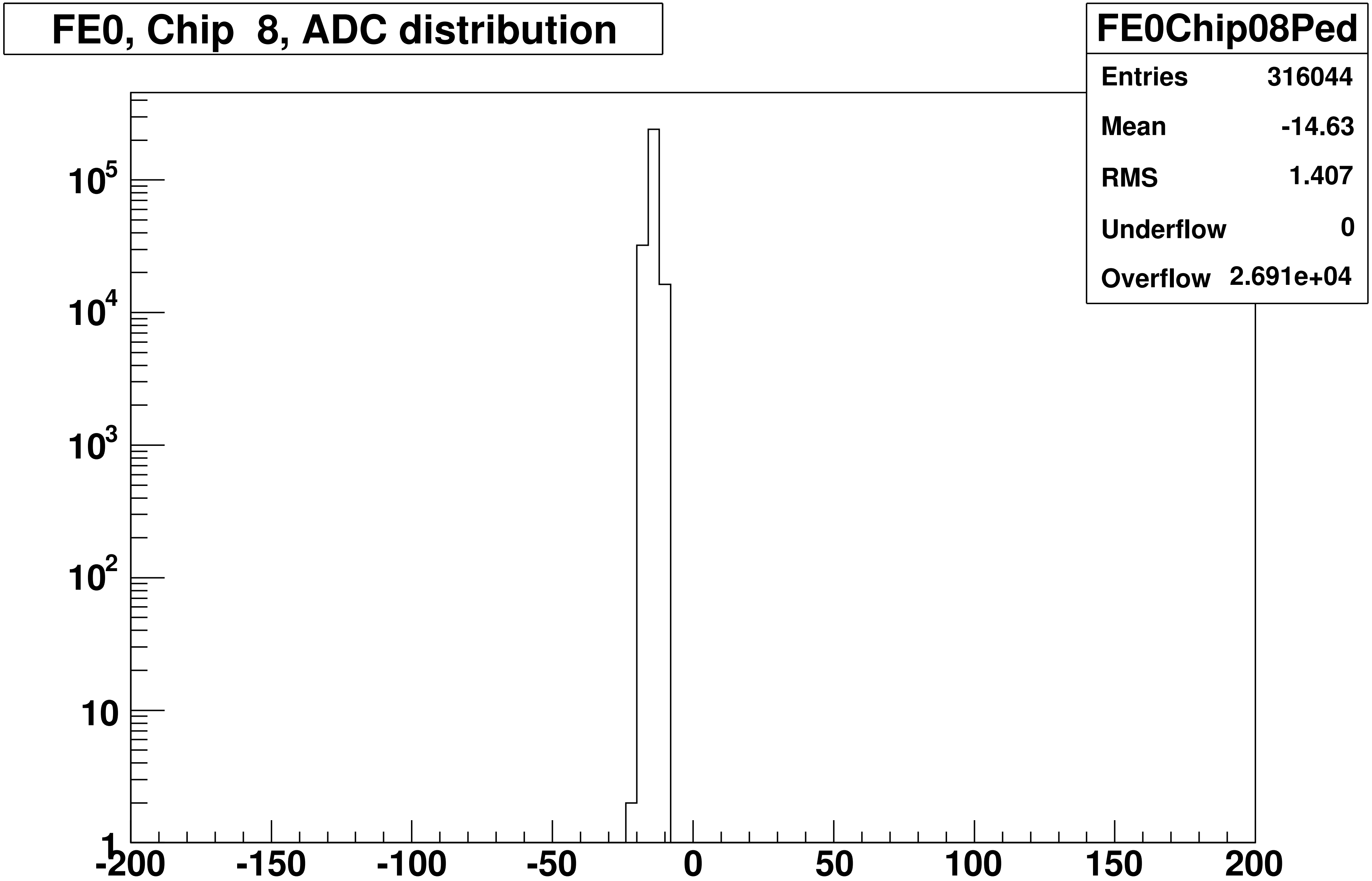
15000
20000
25000



FE0, Chip 8, ADC distribution
FE0Chip08Ped
Entries 316044
Mean -14.63
RMS 1.407
Underflow 0
Overflow 2.691e+04
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10^4
10^3
10^2
10
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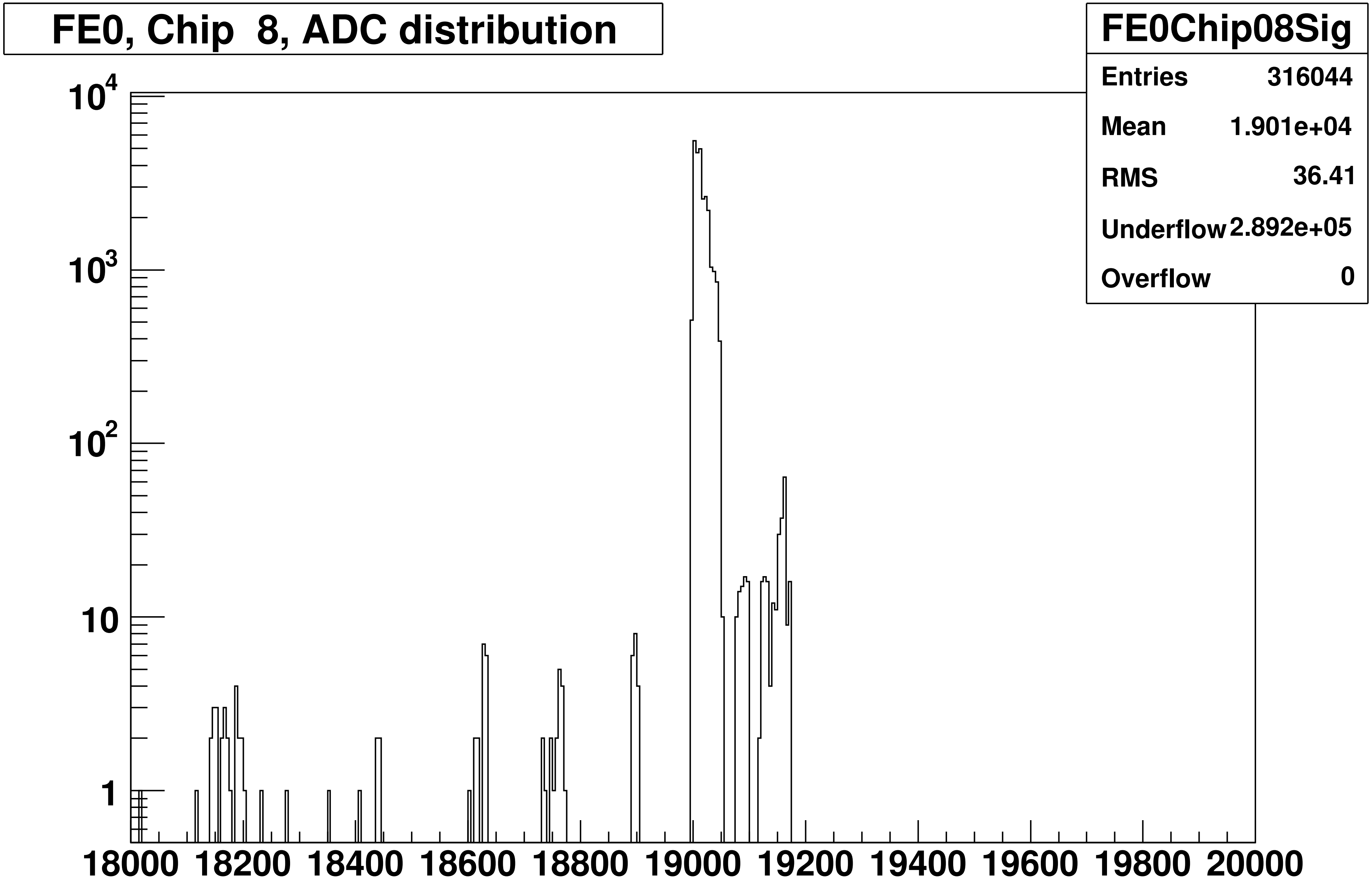
150
200



FE0, Chip 8, ADC distribution
FE0Chip08Sig
Entries 316044
Mean 1.901e+04
RMS 36.41
Underflow 2.892e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
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19000
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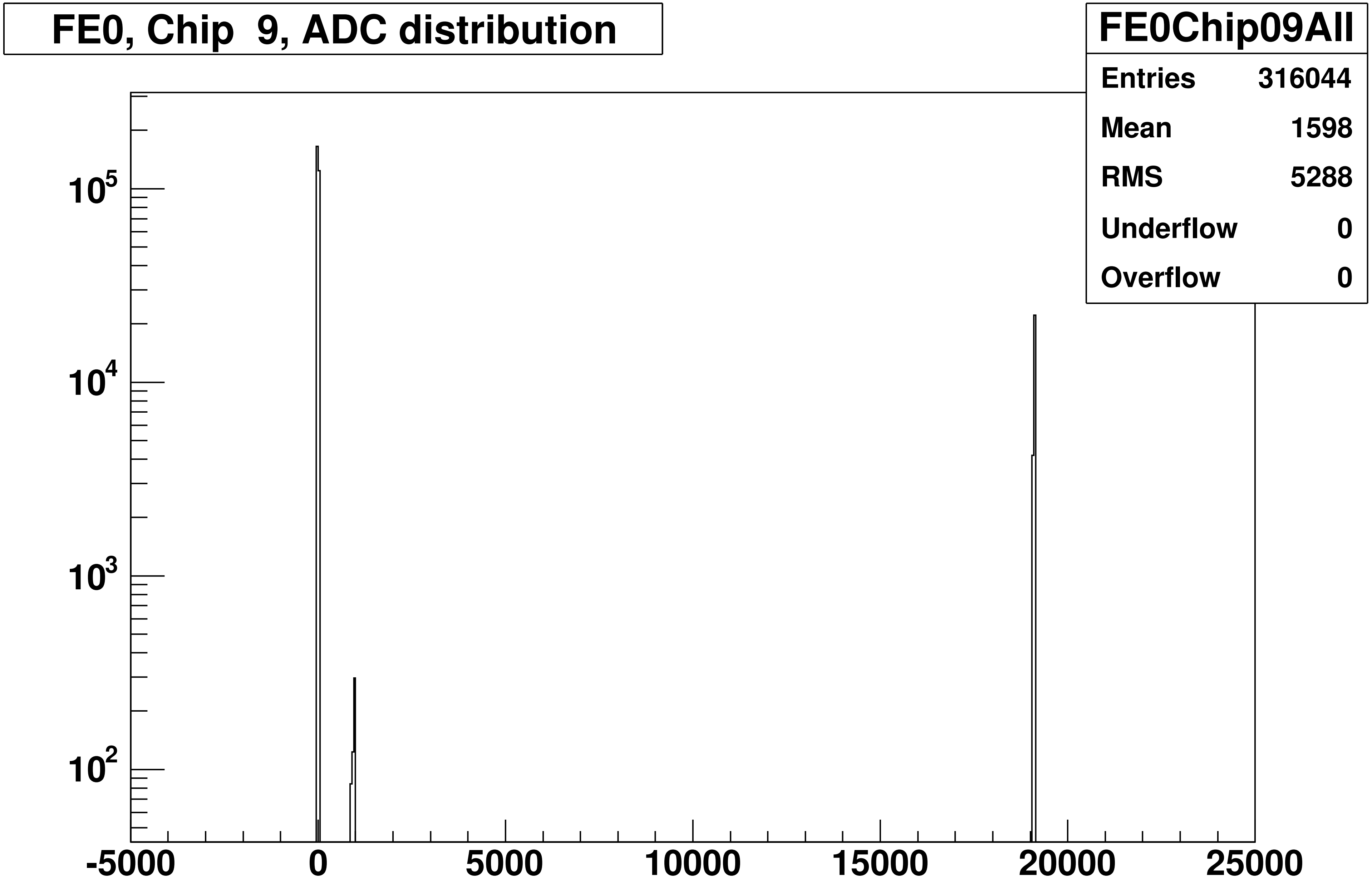
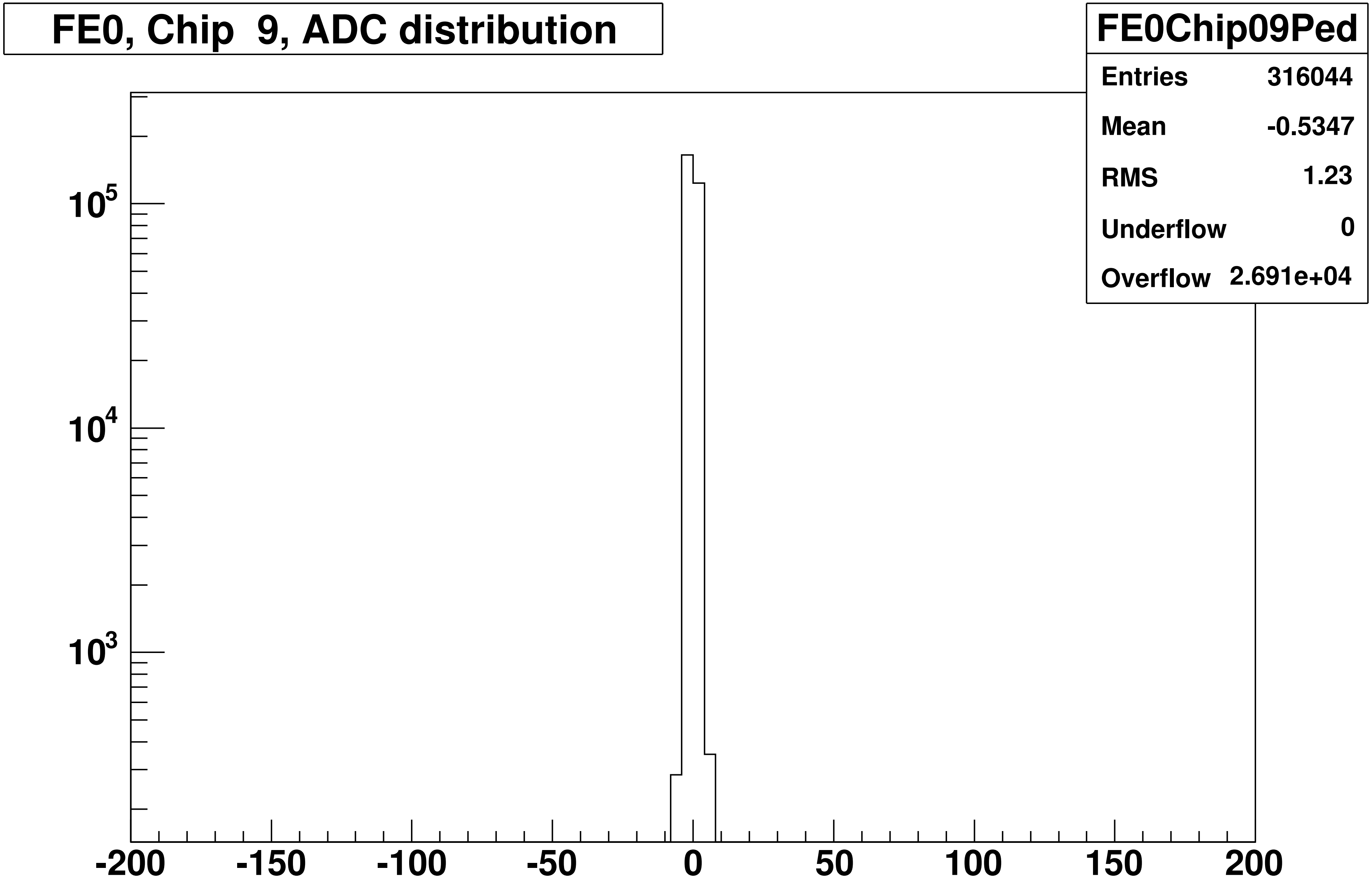
19400
19600
19800
20000


FE0, Chip 9, ADC distribution
FE0Chip09All
Entries 316044
Mean 1598
RMS 5288
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000



FE0, Chip 9, ADC distribution
FE0Chip09Ped
Entries 316044
Mean -0.5347
RMS 1.23
Underflow 0
Overflow 2.691e+04
10^5
10^4
10^3
-200
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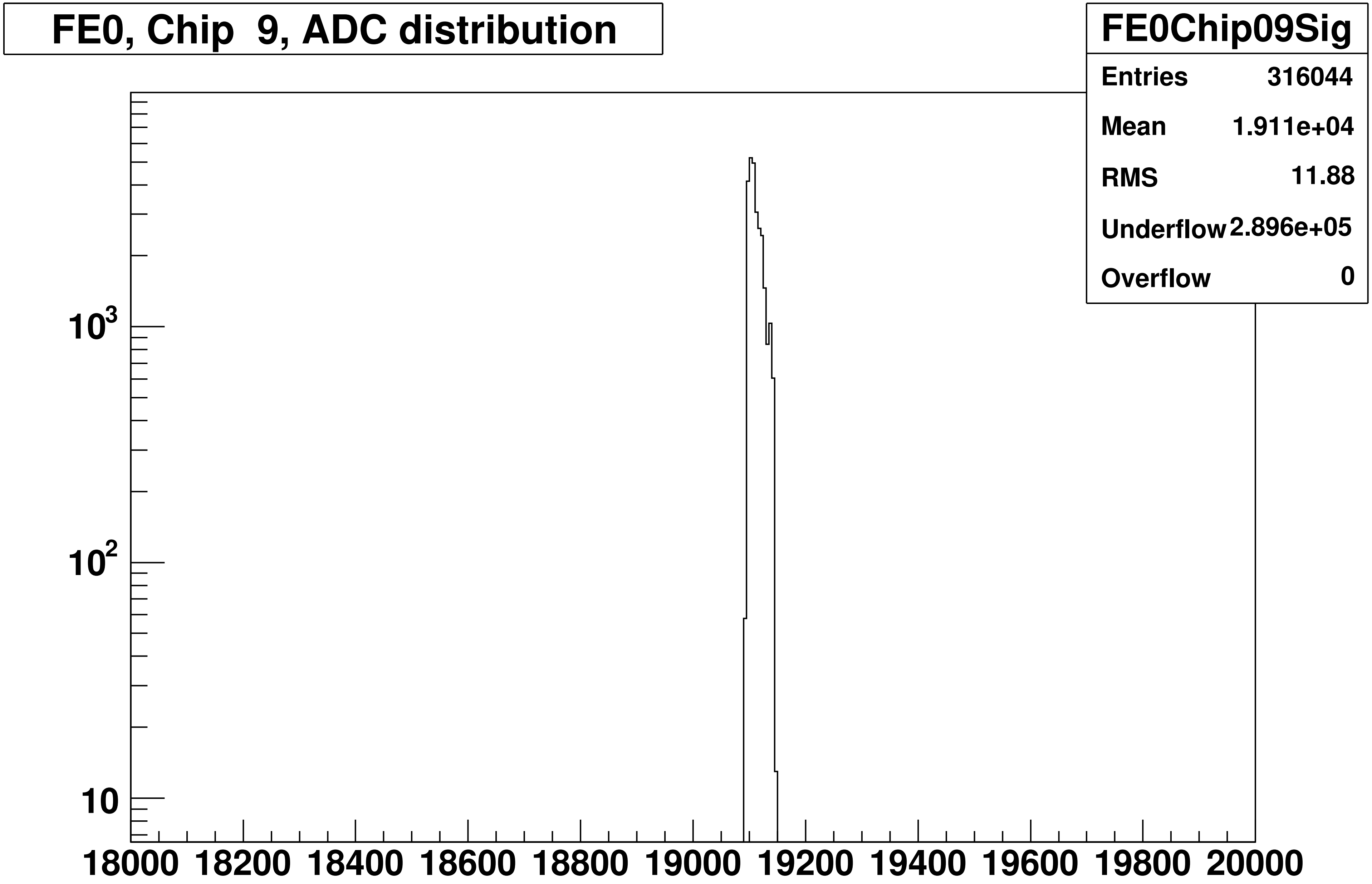
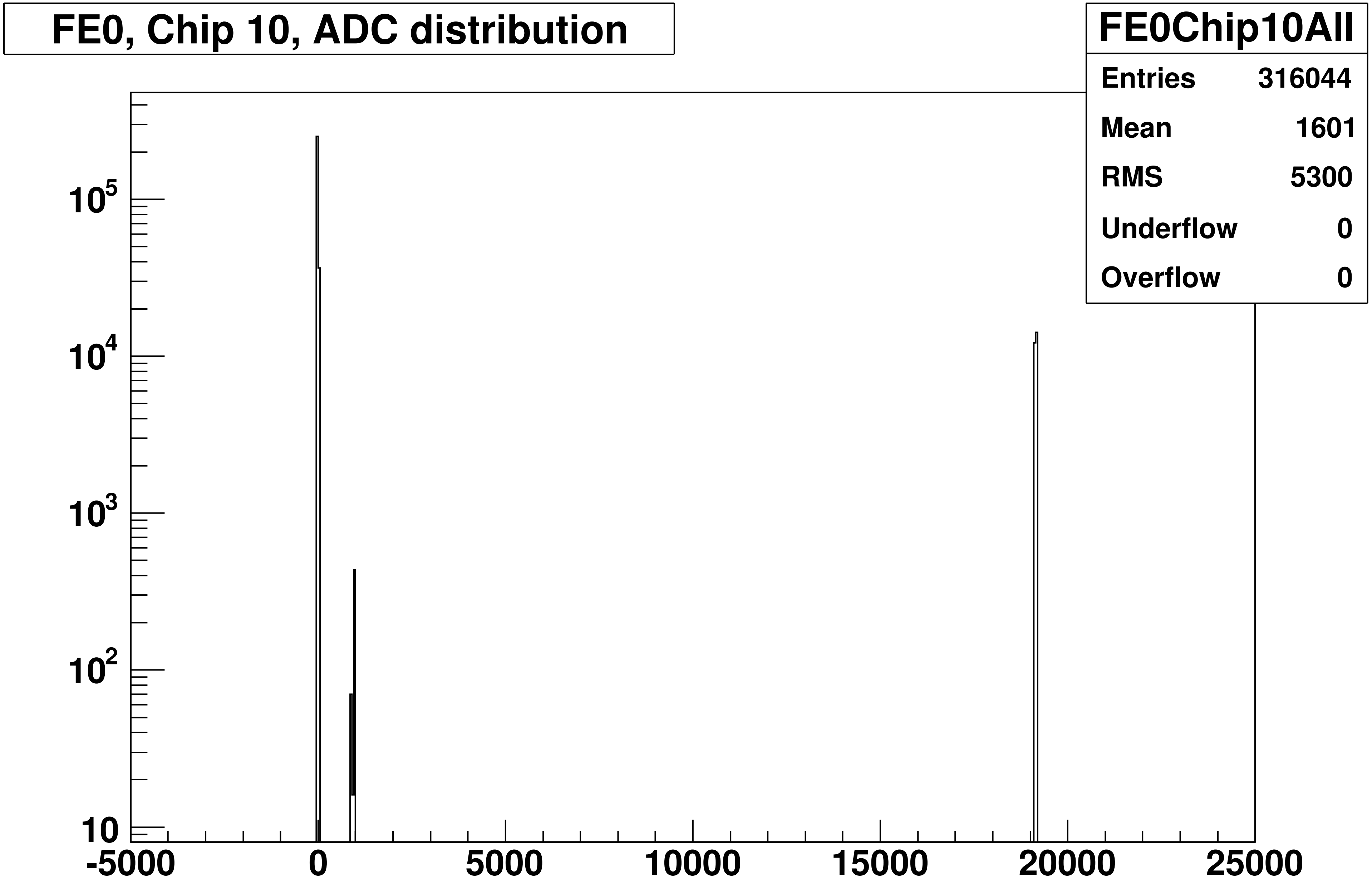
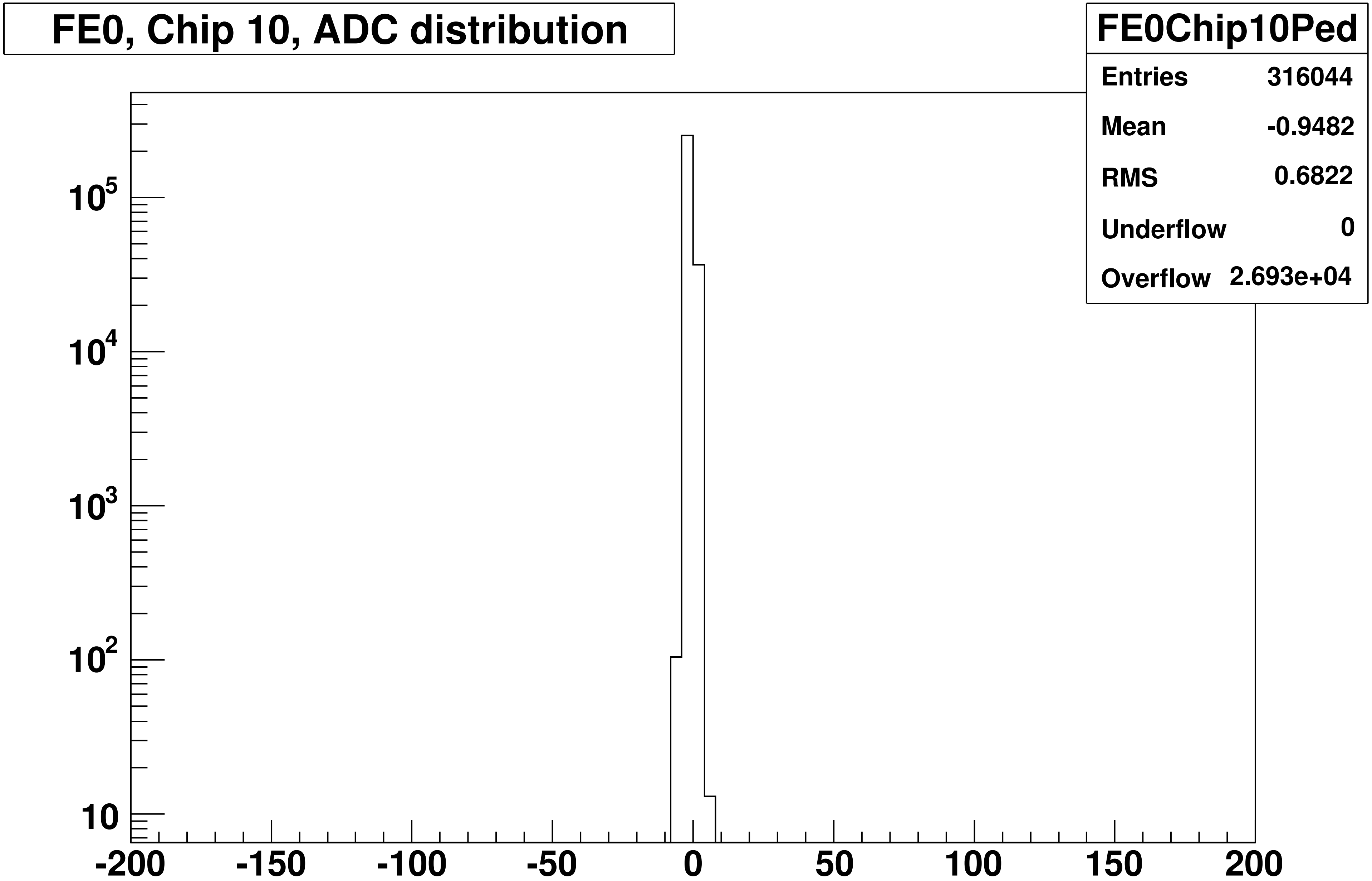
-100
-50
0
50
100
150
200


FE0, Chip 9, ADC distribution
FE0Chip09Sig
Entries 316044
Mean 1.911e+04
RMS 11.88
Underflow 2.896e+05
Overflow 0
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE0, Chip 10, ADC distribution
FE0Chip10All
Entries 316044
Mean 1601
RMS 5300
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE0, Chip 10, ADC distribution
FE0Chip10Ped
Entries 316044
Mean -0.9482
RMS 0.6822
Underflow 0
Overflow 2.693e+04
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10^2
10^3
10^4
10^5
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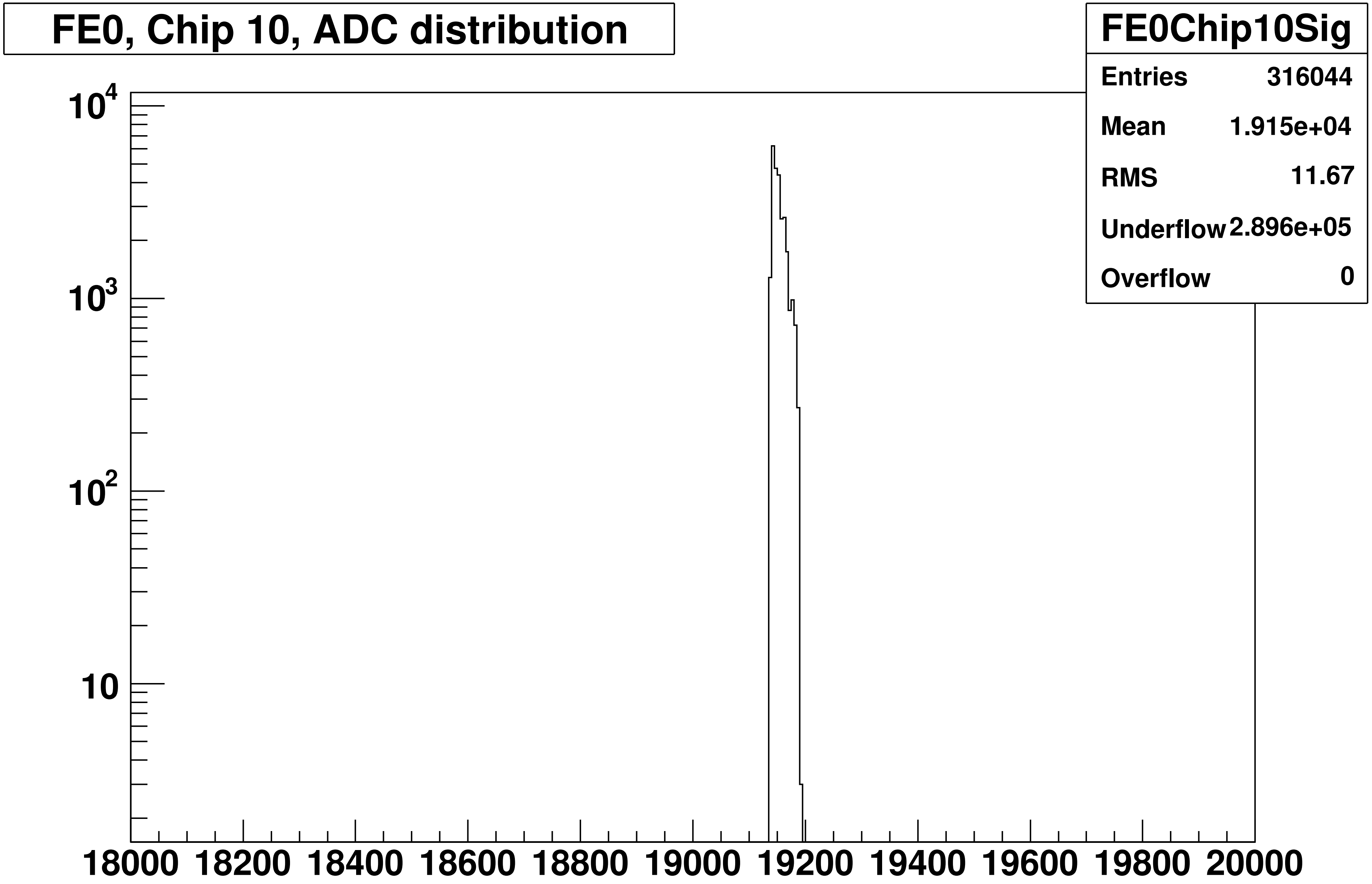
-100
-50
0
50
100
150
200



FE0, Chip 10, ADC distribution
FE0Chip10Sig
Entries 316044
Mean 1.915e+04
RMS 11.67
Underflow 2.896e+05
Overflow 0
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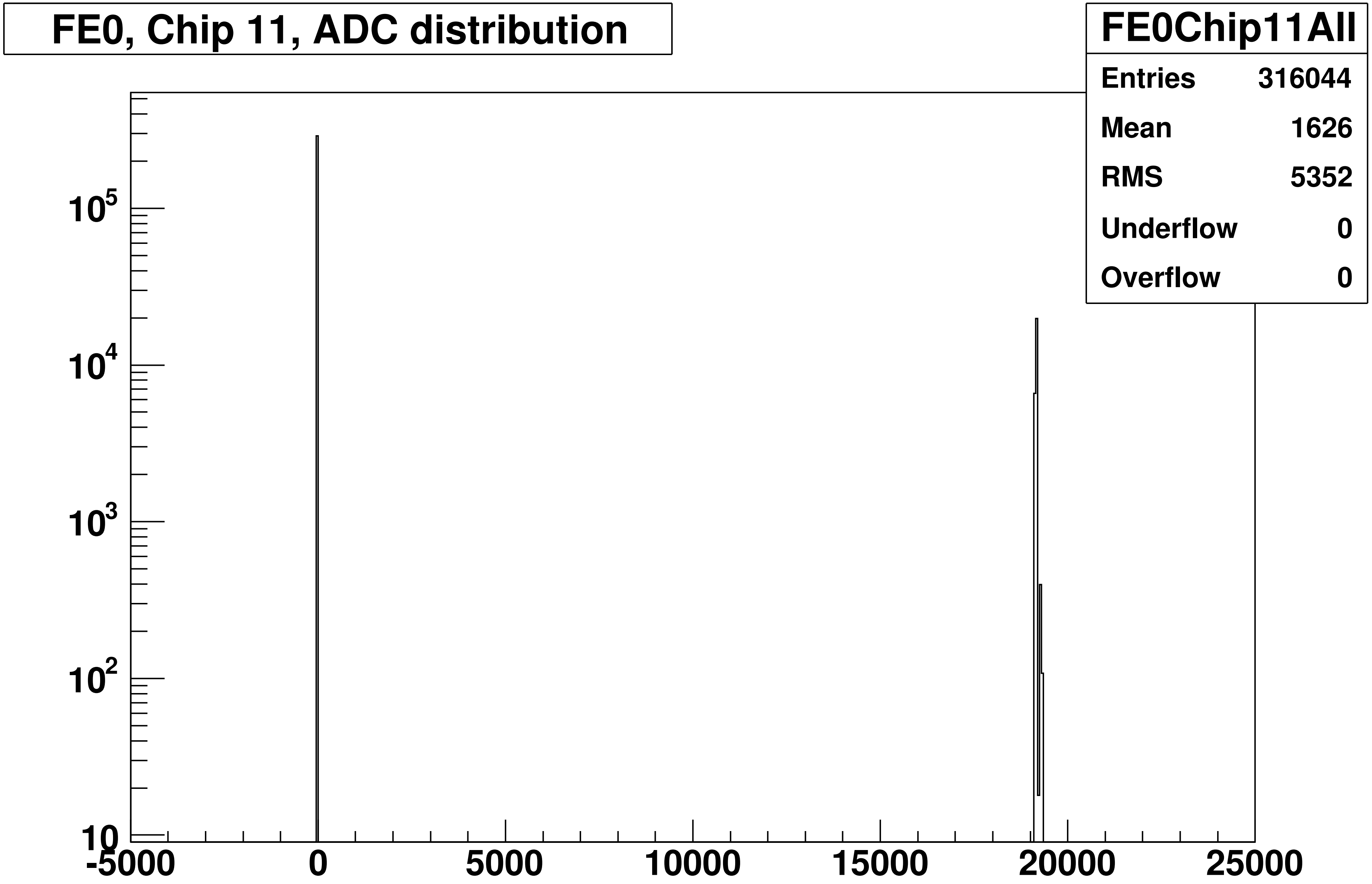
10^3
10^2
10
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000


FE0, Chip 11, ADC distribution
FE0Chip11All
Entries 316044
Mean 1626
RMS 5352
Underflow 0
Overflow 0
10
10^2
10^3
10^4
10^5
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0
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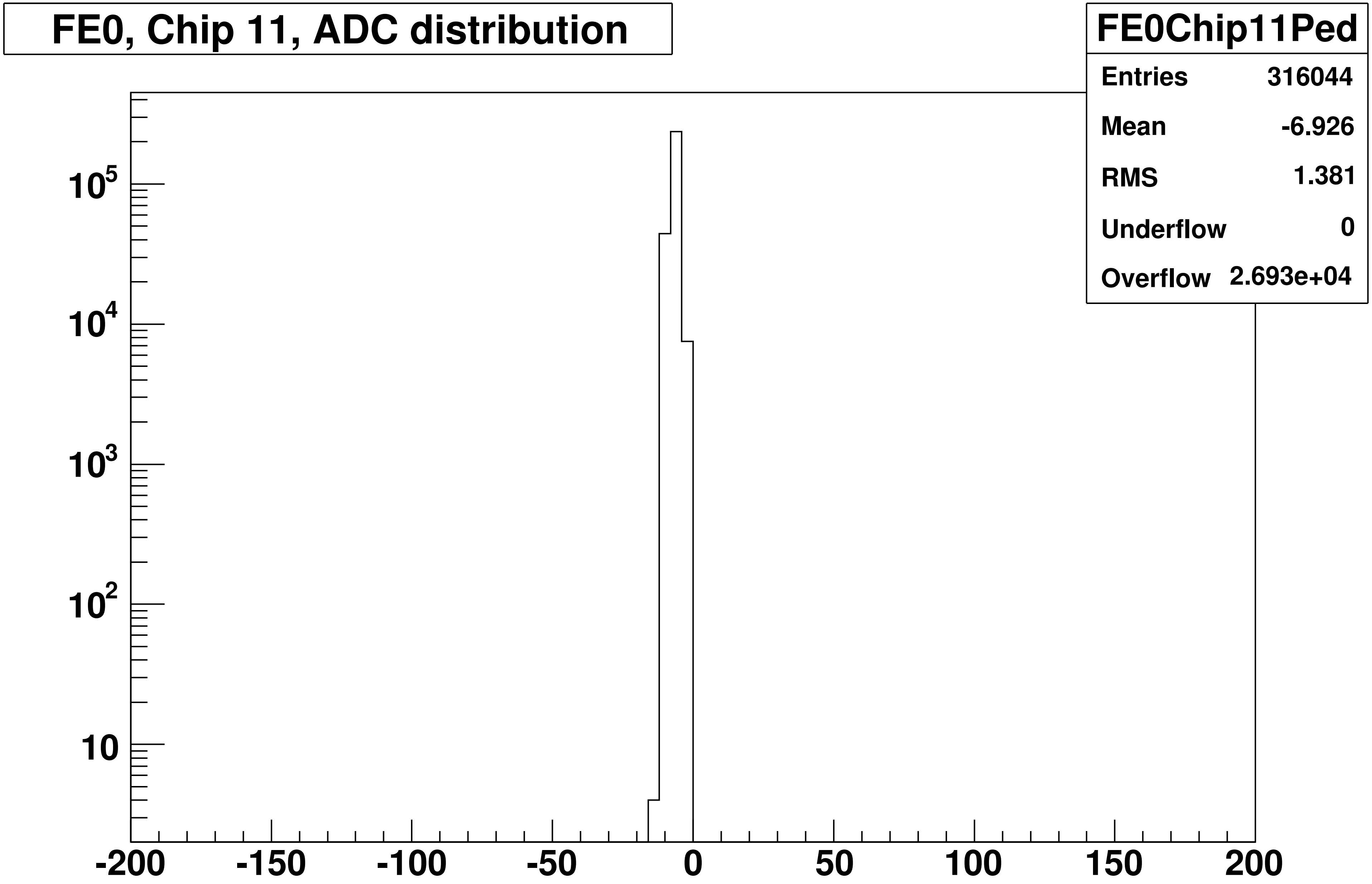
10000
15000
20000
25000


FE0, Chip 11, ADC distribution
FE0Chip11Ped
Entries 316044
Mean -6.926
RMS 1.381
Underflow 0
Overflow 2.693e+04
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10^2
10^3
10^4
10^5
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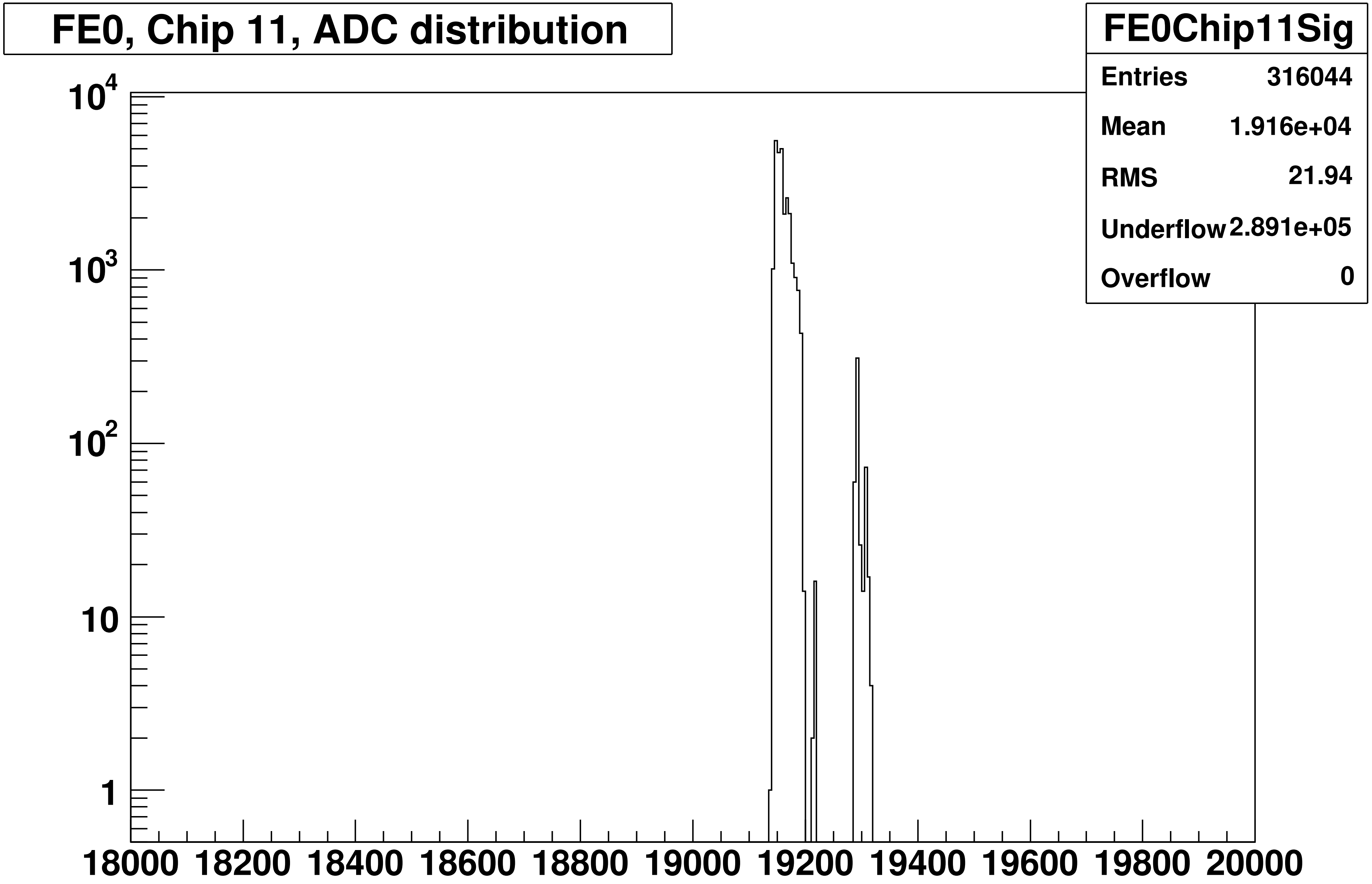
-150
-100
-50
0
50
100
150
200


FE0, Chip 11, ADC distribution
FE0Chip11Sig
Entries 316044
Mean 1.916e+04
RMS 21.94
Underflow 2.891e+05
Overflow 0
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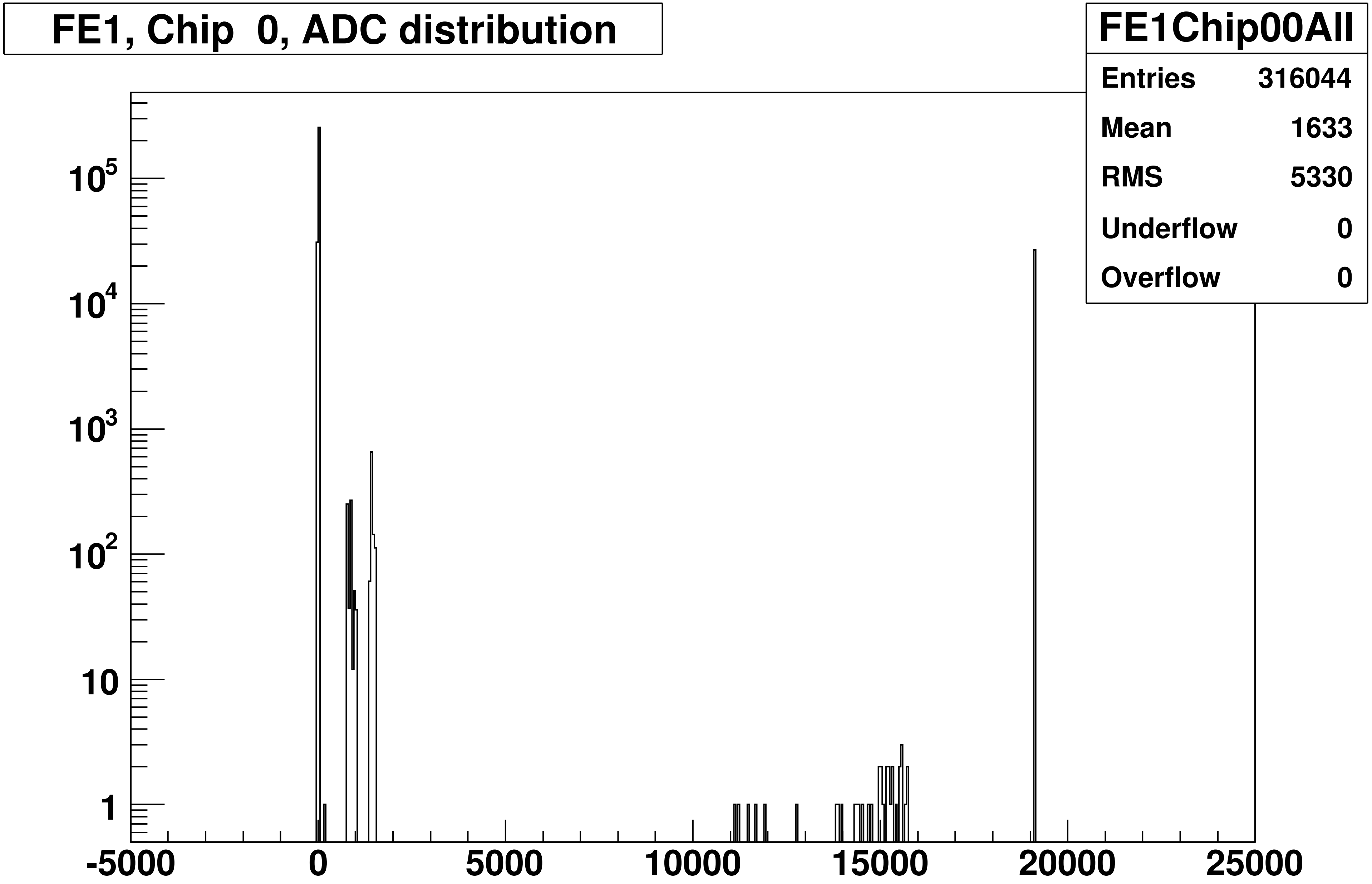
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE1, Chip 0, ADC distribution
FE1Chip00All
Entries 316044
Mean 1633
RMS 5330
Underflow 0
Overflow 0
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10^4
10^3
10^2
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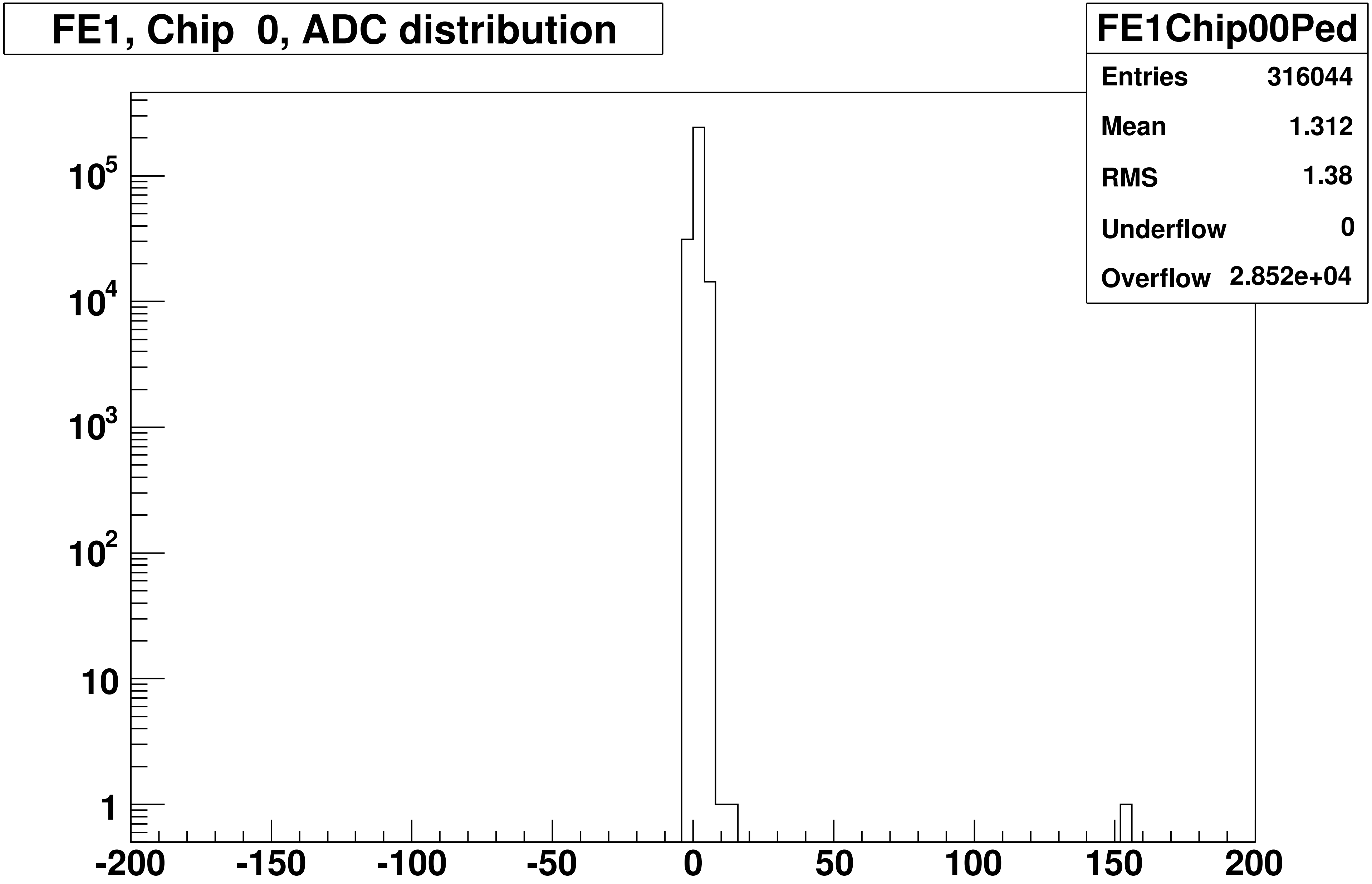
15000
20000
25000



FE1, Chip 0, ADC distribution
FE1Chip00Ped
Entries 316044
Mean 1.312
RMS 1.38
Underflow 0
Overflow 2.852e+04
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10^4
10^3
10^2
10
1
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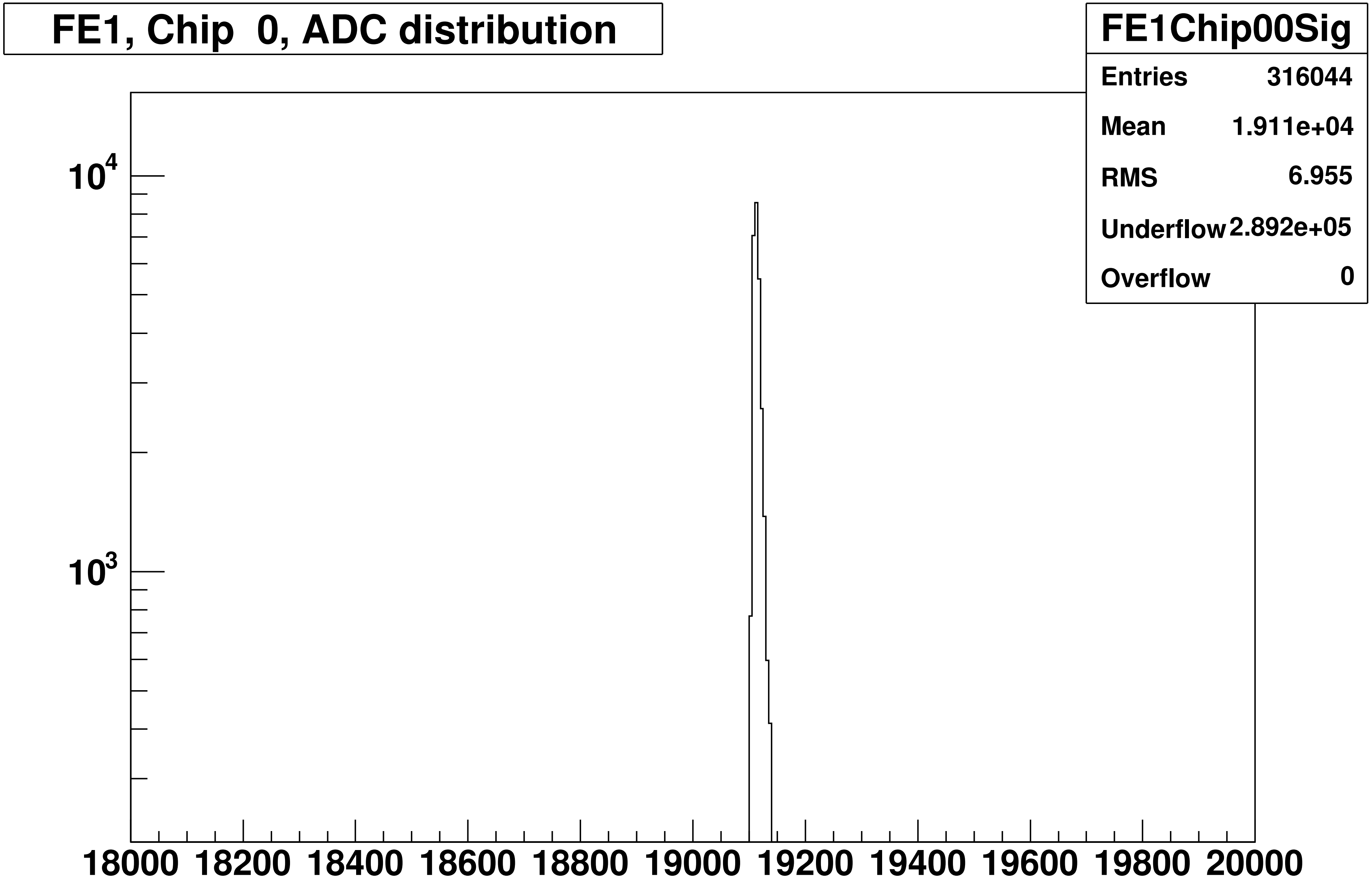
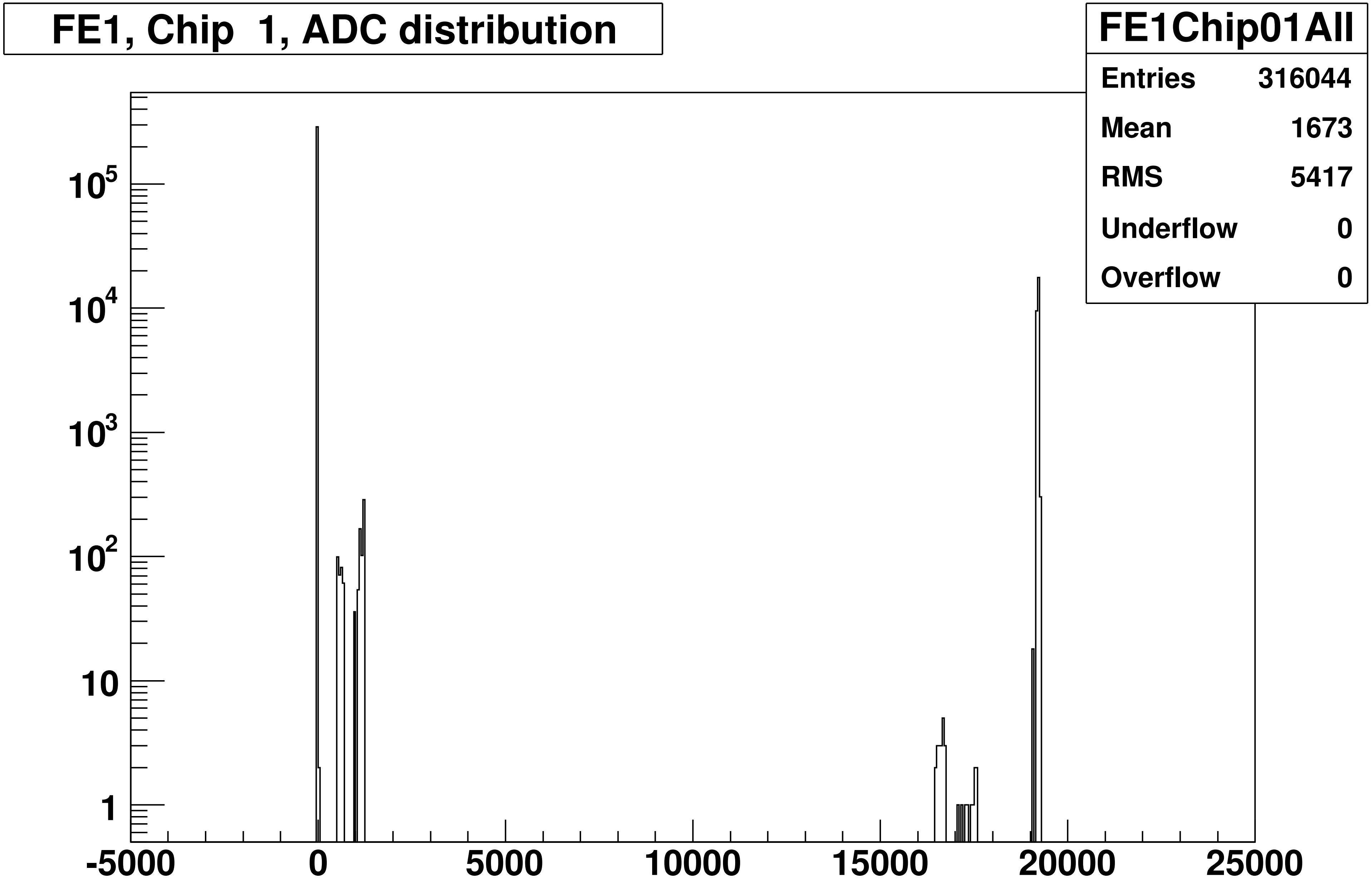
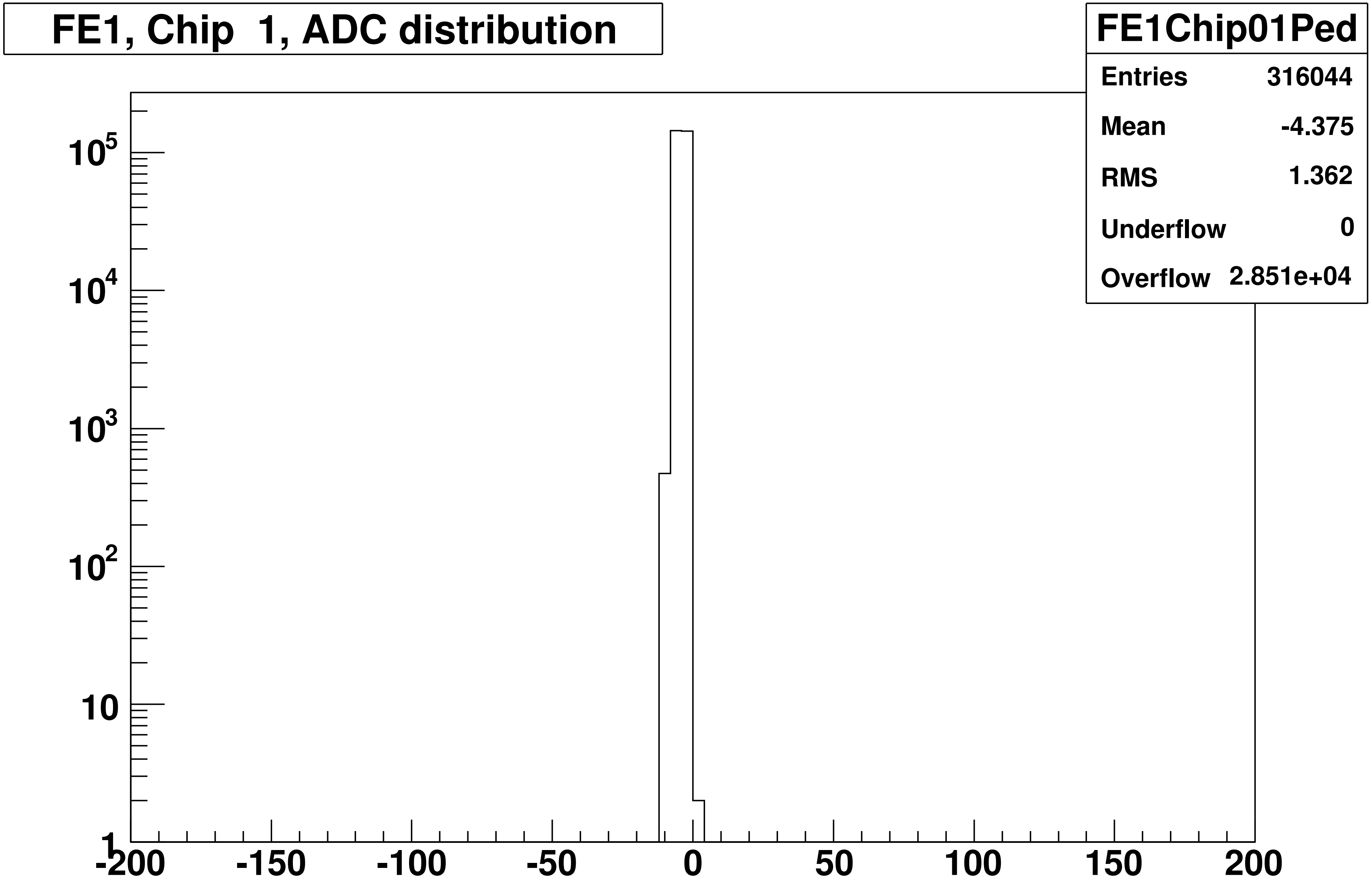
-100
-50
0
50
100
150
200


FE1, Chip 0, ADC distribution
FE1Chip00Sig
Entries 316044
Mean 1.911e+04
RMS 6.955
Underflow 2.892e+05
Overflow 0
10^4
10^3
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE1, Chip 1, ADC distribution
FE1Chip01All
Entries 316044
Mean 1673
RMS 5417
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE1, Chip 1, ADC distribution
FE1Chip01Ped
Entries 316044
Mean -4.375
RMS 1.362
Underflow 0
Overflow 2.851e+04
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10^4
10^3
10^2
10
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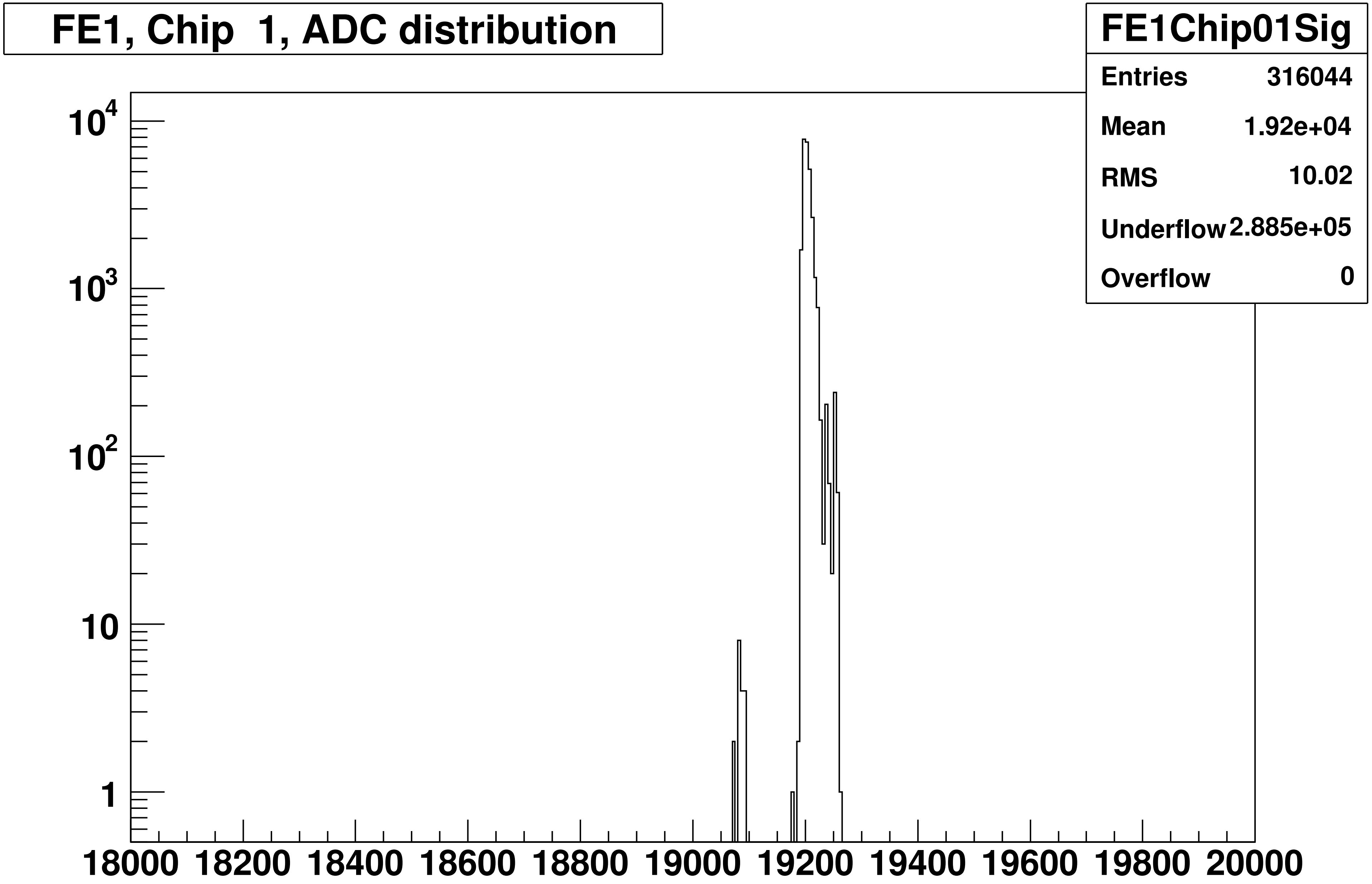
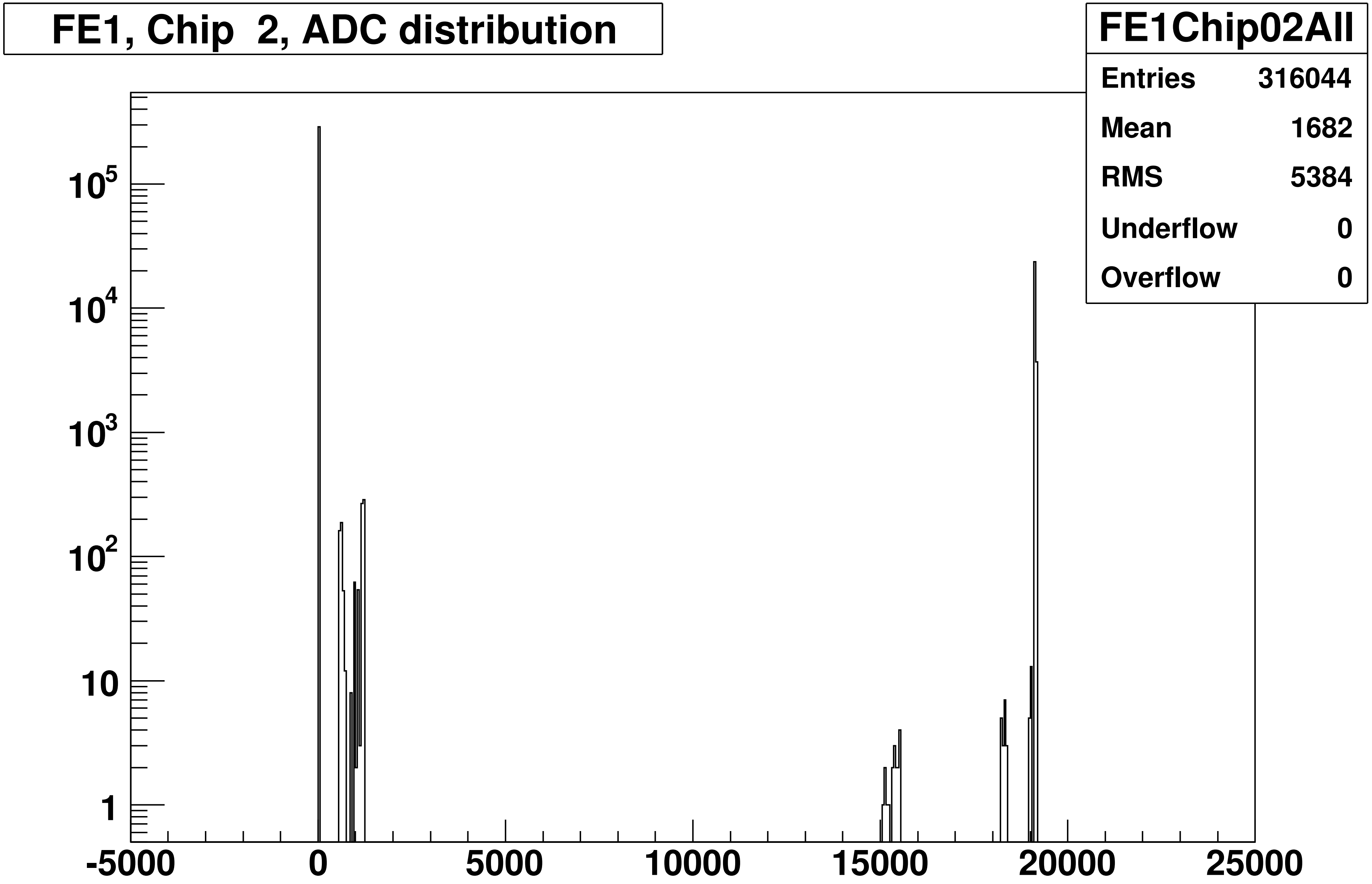
150
200


FE1, Chip 1, ADC distribution
FE1Chip01Sig
Entries 316044
Mean 1.92e+04
RMS 10.02
Underflow 2.885e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE1, Chip 2, ADC distribution
FE1Chip02All
Entries 316044
Mean 1682
RMS 5384
Underflow 0
Overflow 0
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10^4
10^3
10^2
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10000
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20000
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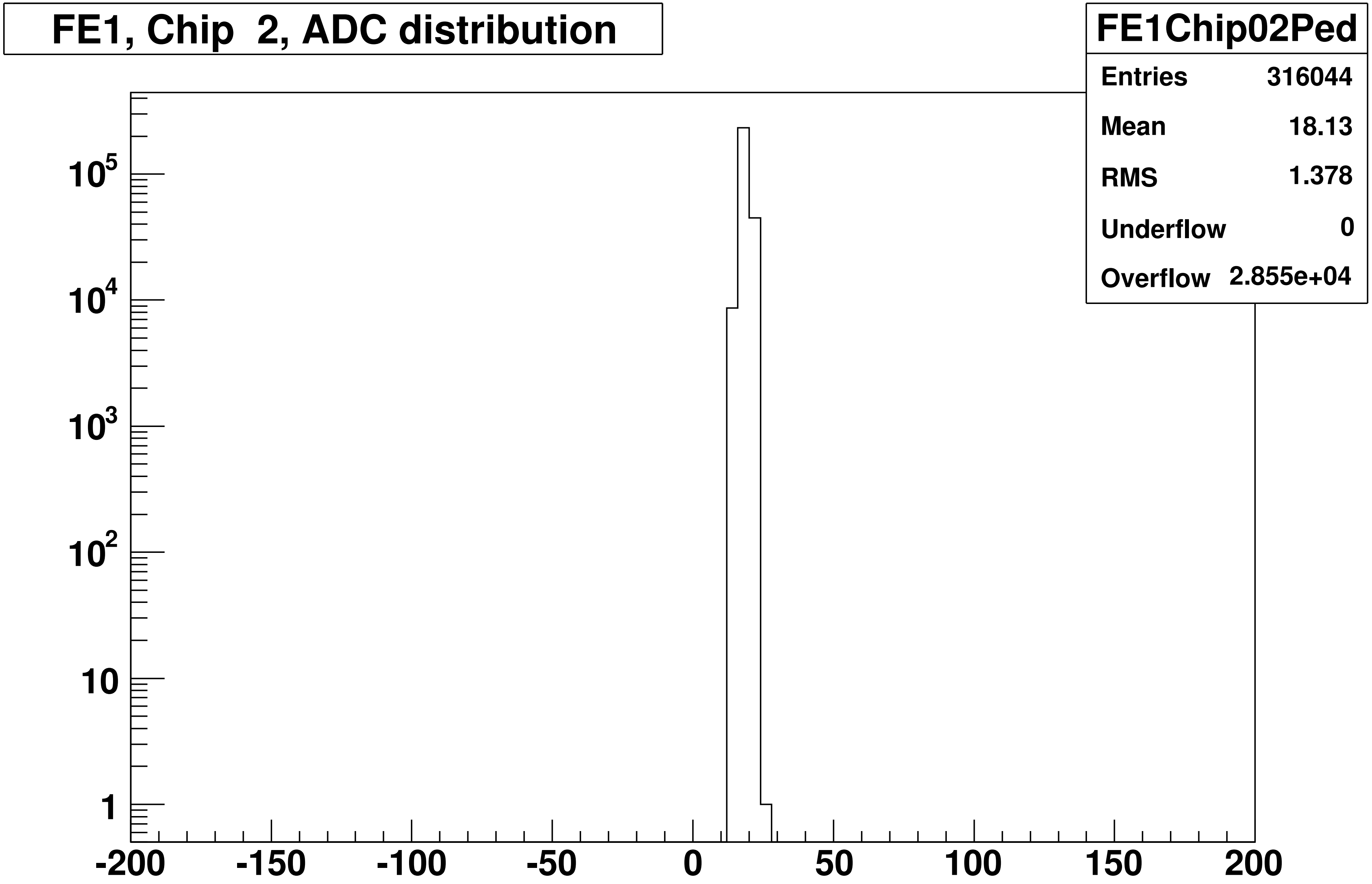

FE1, Chip 2, ADC distribution
FE1Chip02Ped
Entries 316044
Mean 18.13
RMS 1.378
Underflow 0
Overflow 2.855e+04
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10^4
10^3
10^2
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1
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150
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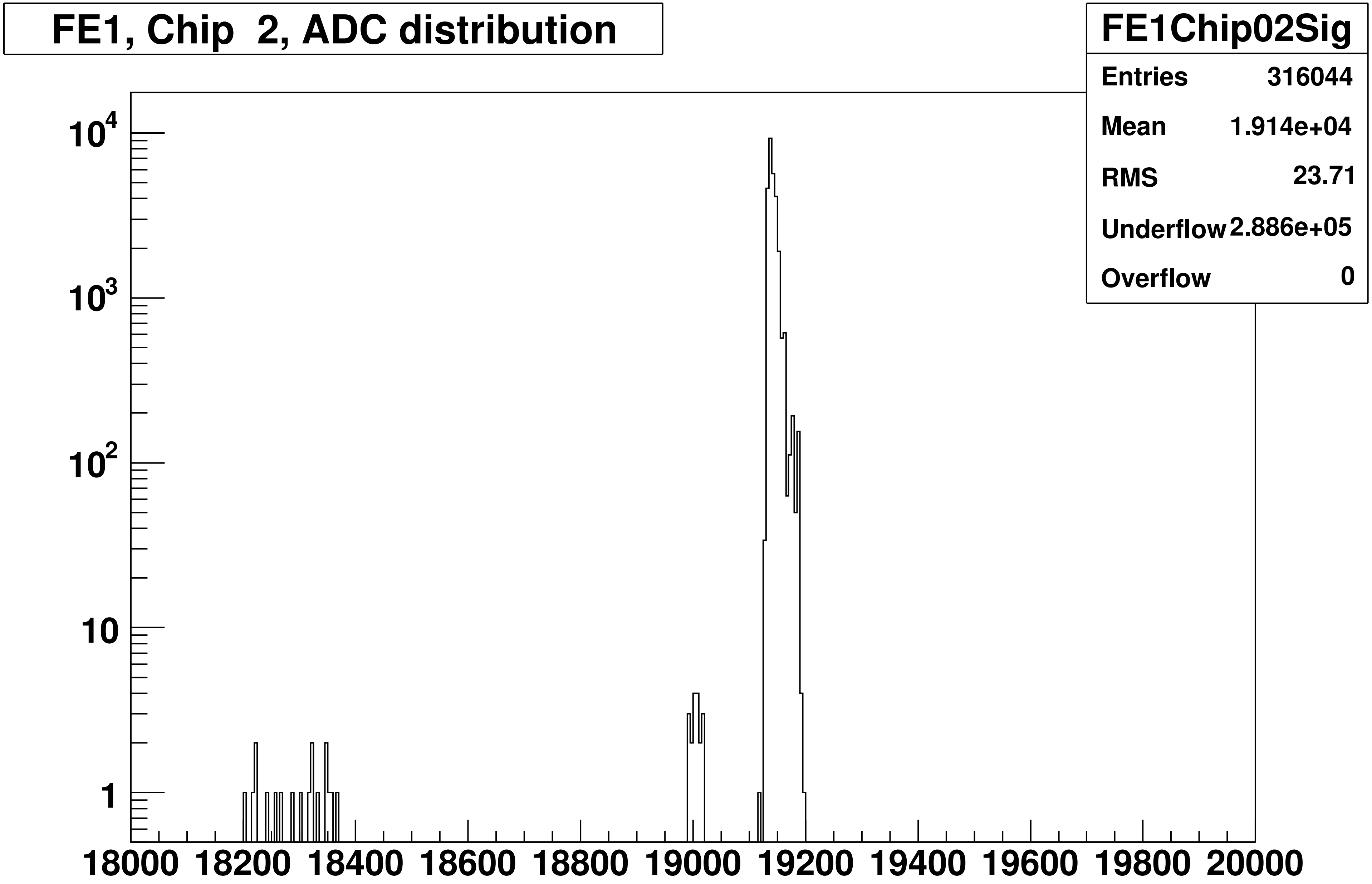

FE1, Chip 2, ADC distribution
FE1Chip02Sig
Entries 316044
Mean 1.914e+04
RMS 23.71
Underflow 2.886e+05
Overflow 0
10^4
10^3
10^2
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1
18000
18200
18400
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19800
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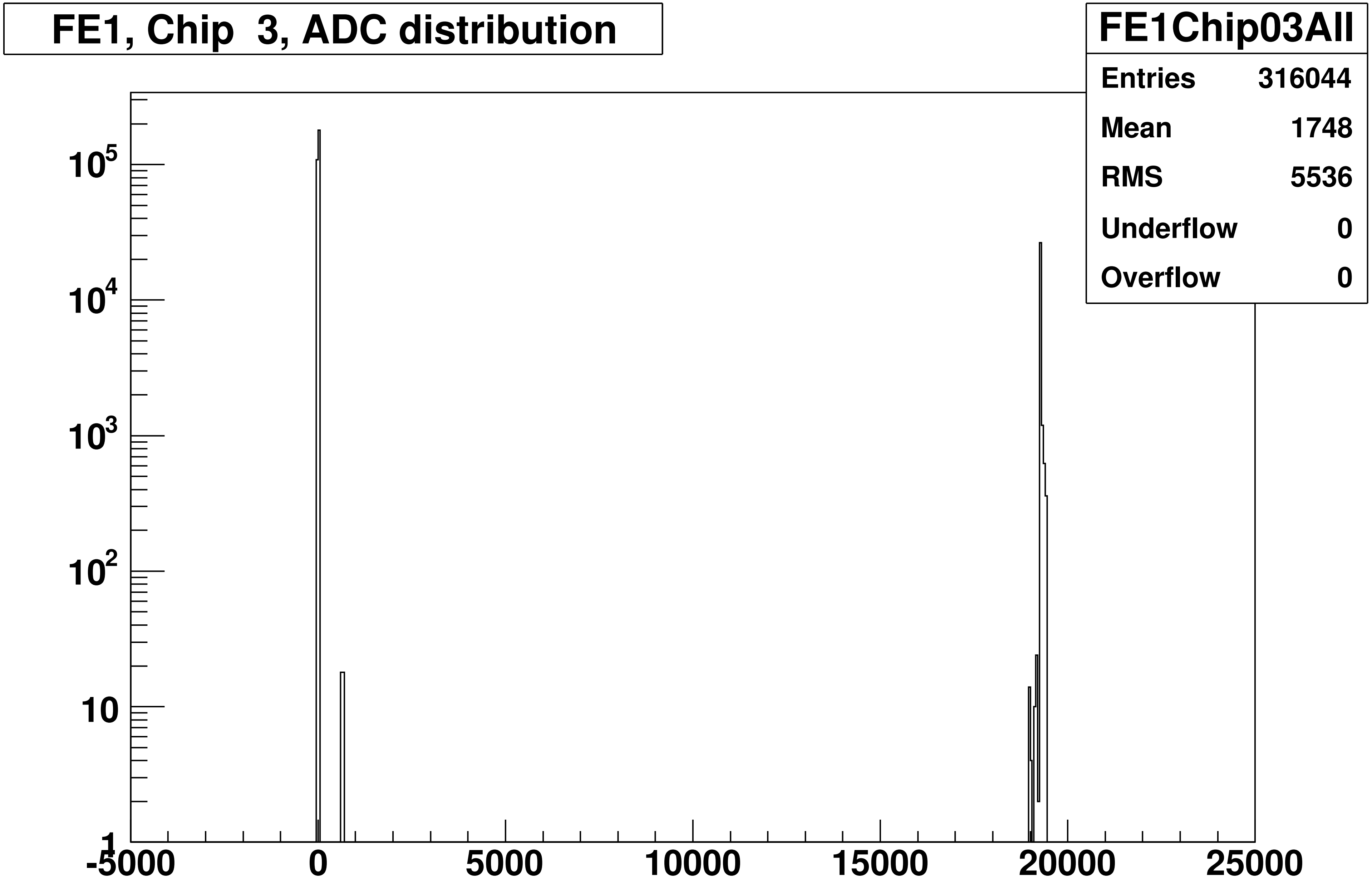
FE1, Chip 3, ADC distribution
FE1Chip03All
Entries 316044
Mean 1748
RMS 5536
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
1
-5000
0
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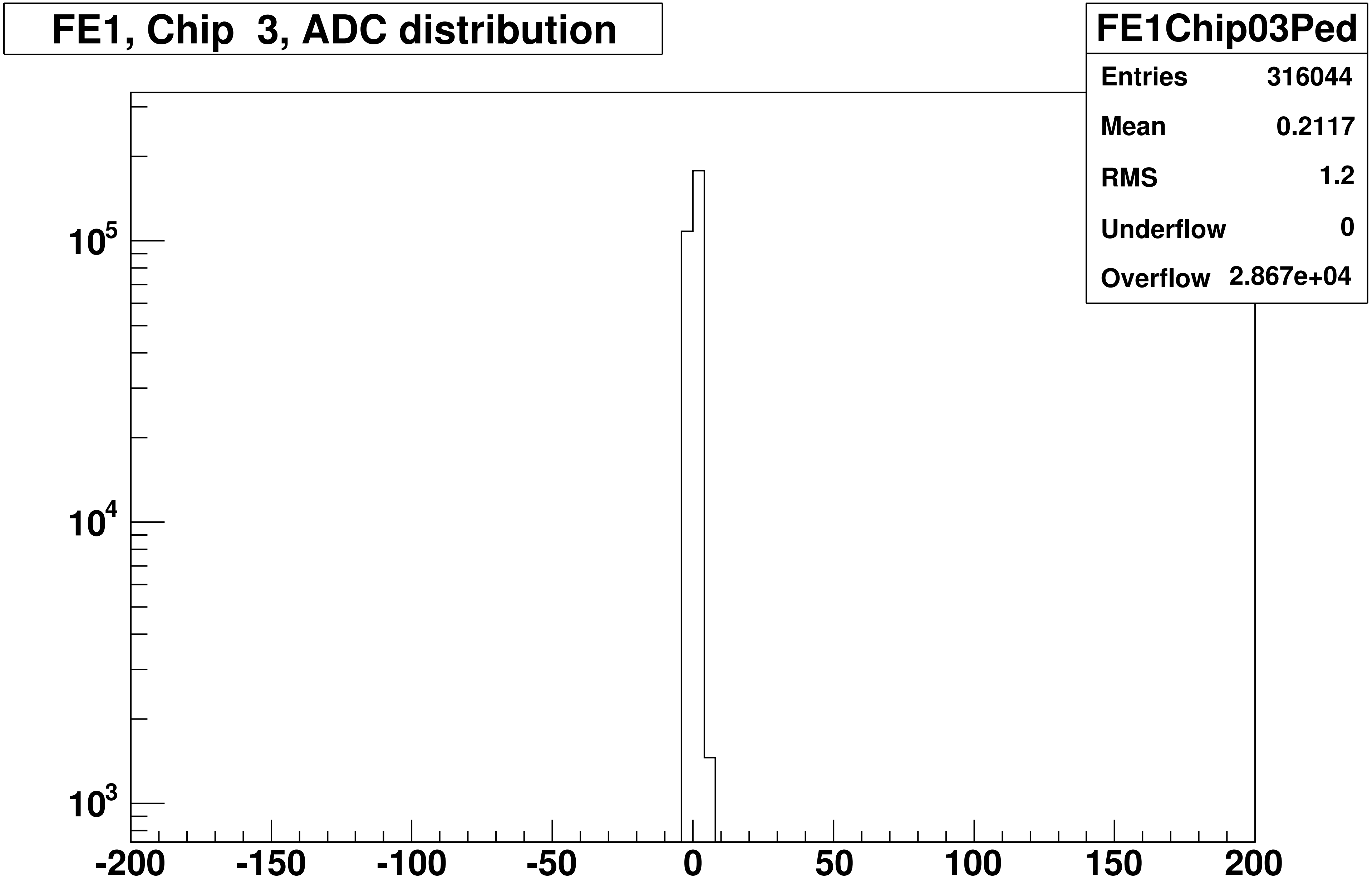
10000
15000
20000
25000


FE1, Chip 3, ADC distribution
FE1Chip03Ped
Entries 316044
Mean 0.2117
RMS 1.2
Underflow 0
Overflow 2.867e+04
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10^4
10^3
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-100
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150
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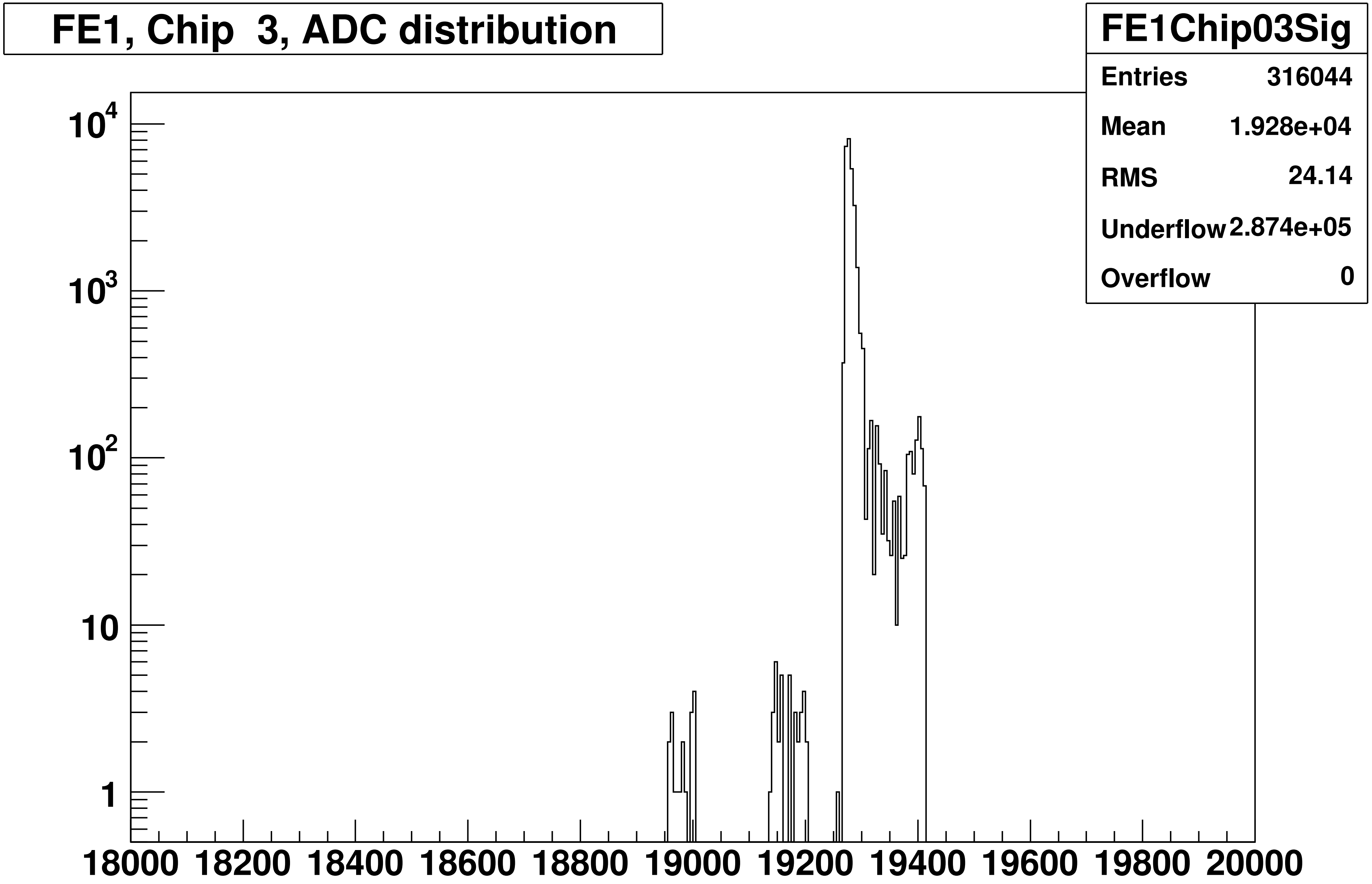
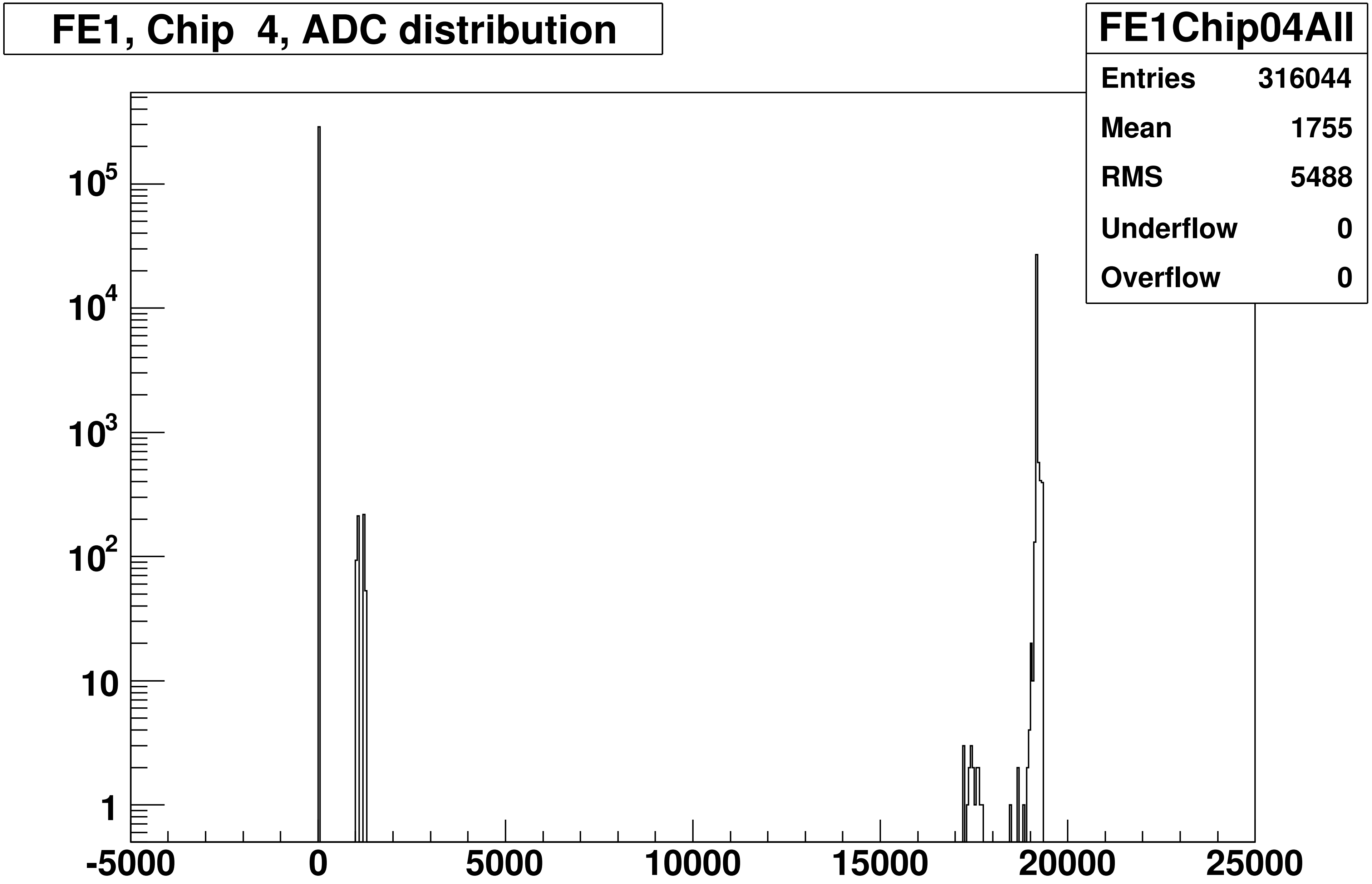

FE1, Chip 3, ADC distribution
FE1Chip03Sig
Entries 316044
Mean 1.928e+04
RMS 24.14
Underflow 2.874e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE1, Chip 4, ADC distribution
FE1Chip04All
Entries 316044
Mean 1755
RMS 5488
Underflow 0
Overflow 0
1
10
10^2
10^3
10^4
10^5
-5000
0
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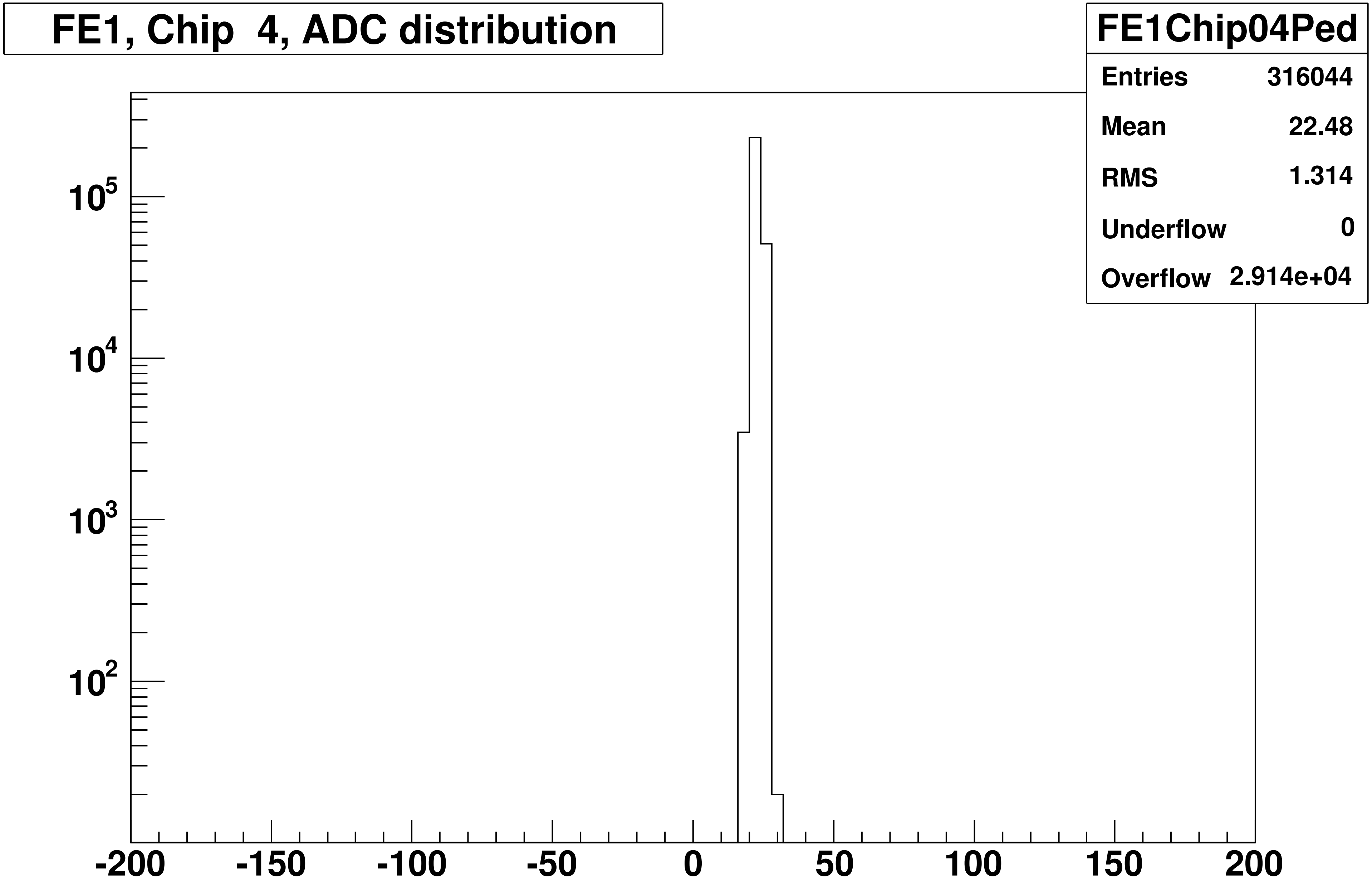
FE1, Chip 4, ADC distribution
FE1Chip04Ped
Entries 316044
Mean 22.48
RMS 1.314
Underflow 0
Overflow 2.914e+04
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10^3
10^2
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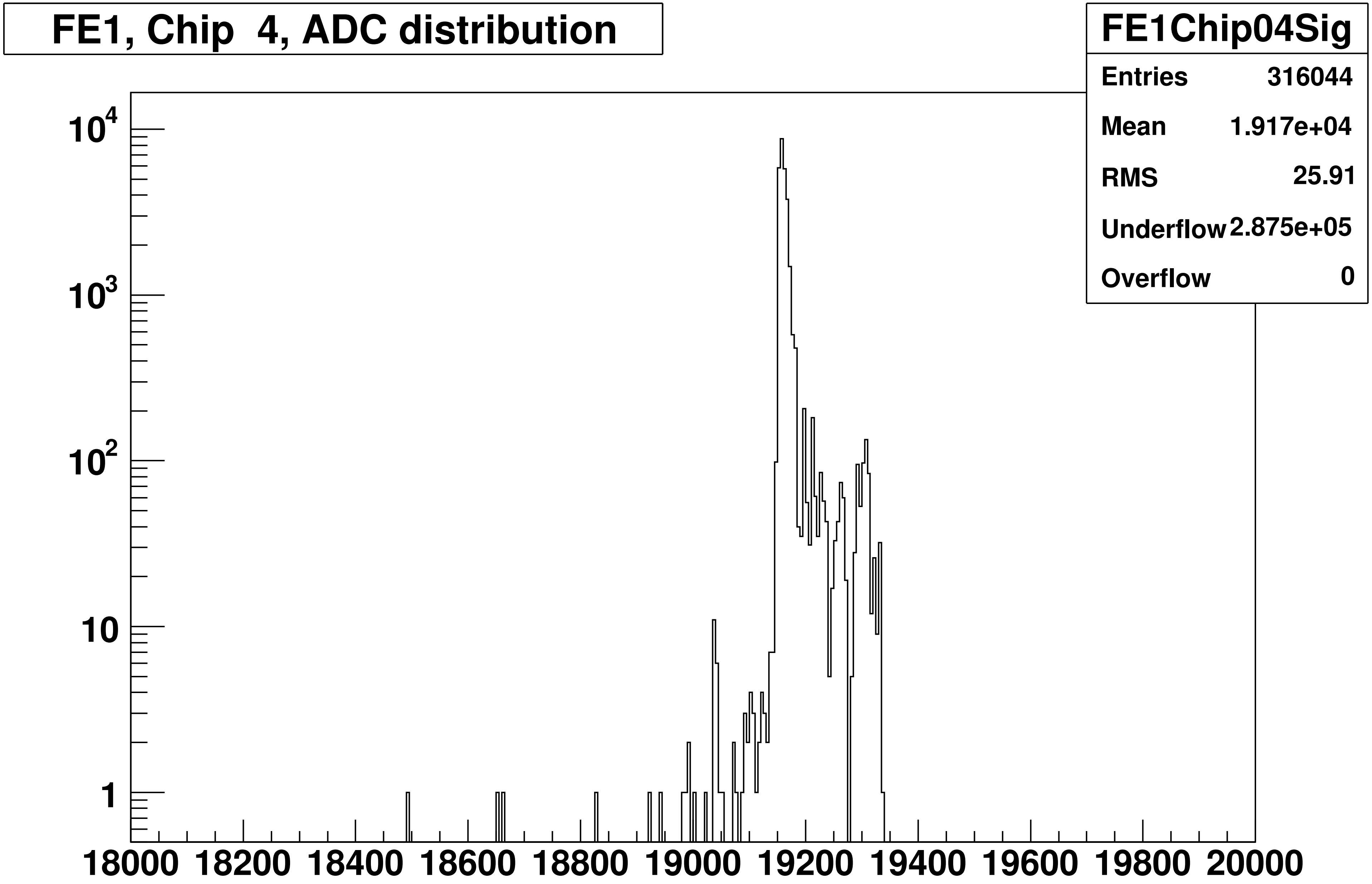
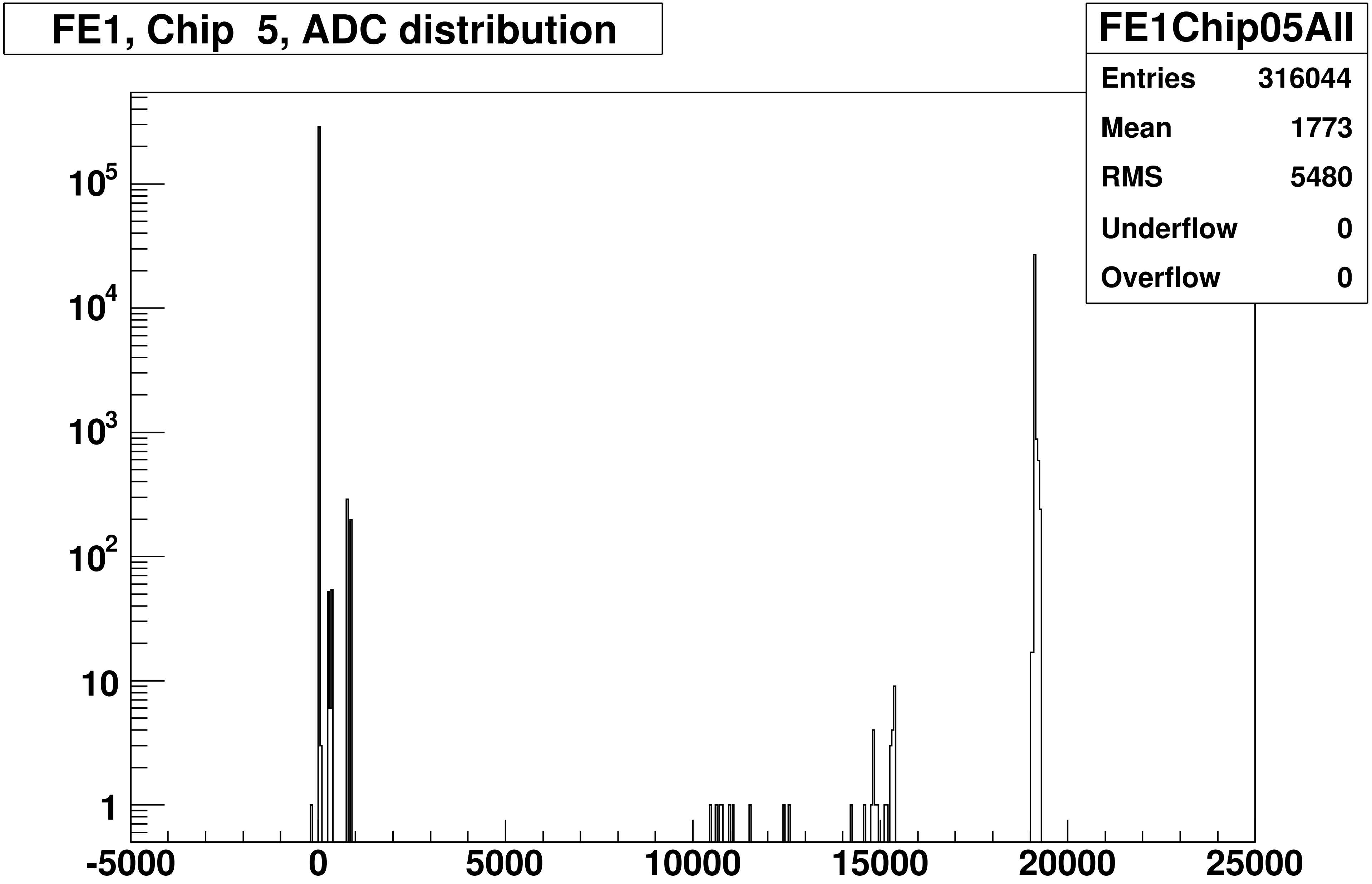

FE1, Chip 4, ADC distribution
FE1Chip04Sig
Entries 316044
Mean 1.917e+04
RMS 25.91
Underflow 2.875e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE1, Chip 5, ADC distribution
FE1Chip05All
Entries 316044
Mean 1773
RMS 5480
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
1
-5000
0
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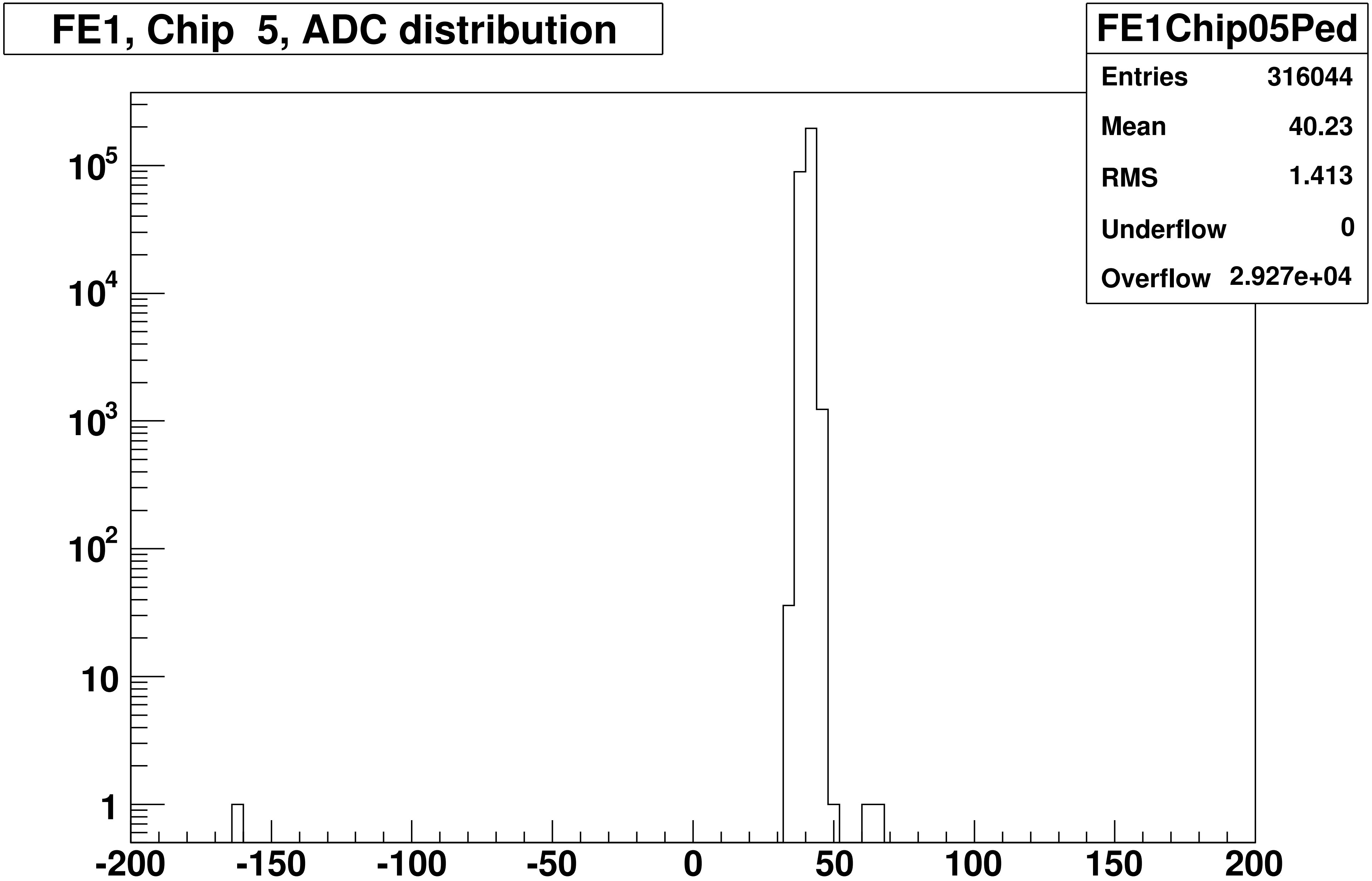
10000
15000
20000
25000


FE1, Chip 5, ADC distribution
FE1Chip05Ped
Entries 316044
Mean 40.23
RMS 1.413
Underflow 0
Overflow 2.927e+04
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10^4
10^3
10^2
10
1
-200
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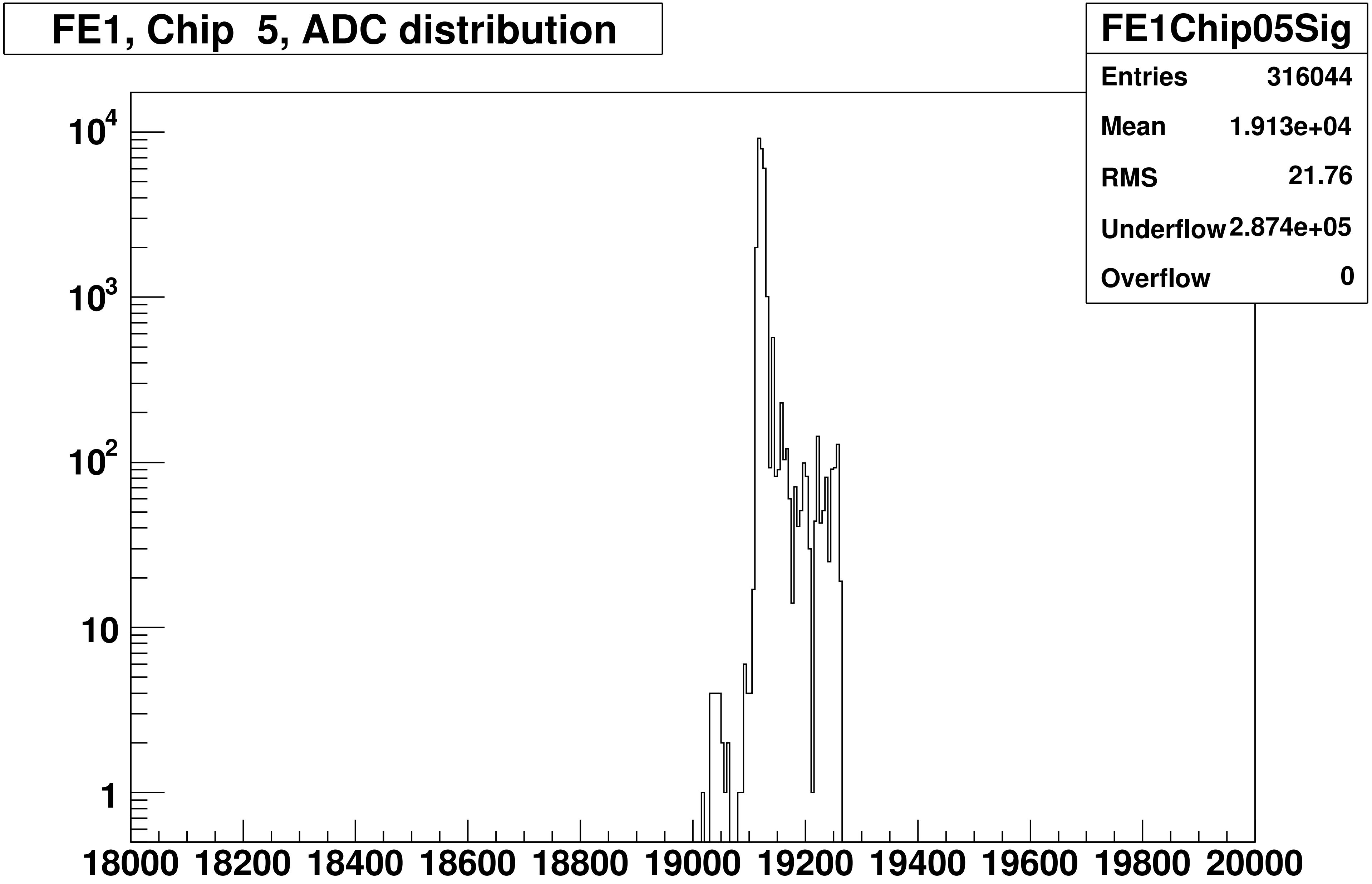
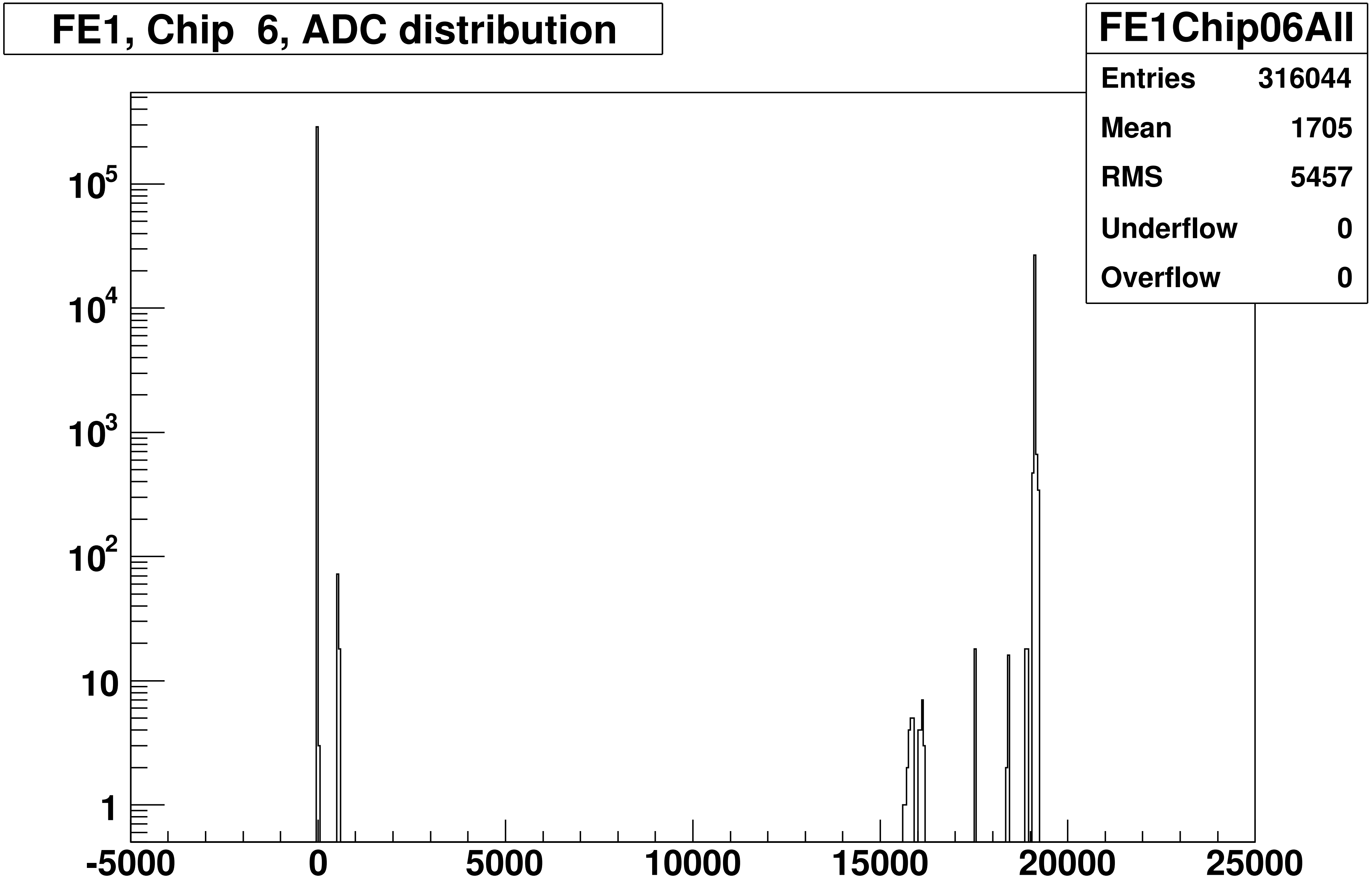
-100
-50
0
50
100
150
200


FE1, Chip 5, ADC distribution
FE1Chip05Sig
Entries 316044
Mean 1.913e+04
RMS 21.76
Underflow 2.874e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE1, Chip 6, ADC distribution
FE1Chip06All
Entries 316044
Mean 1705
RMS 5457
Underflow 0
Overflow 0
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10^4
10^3
10^2
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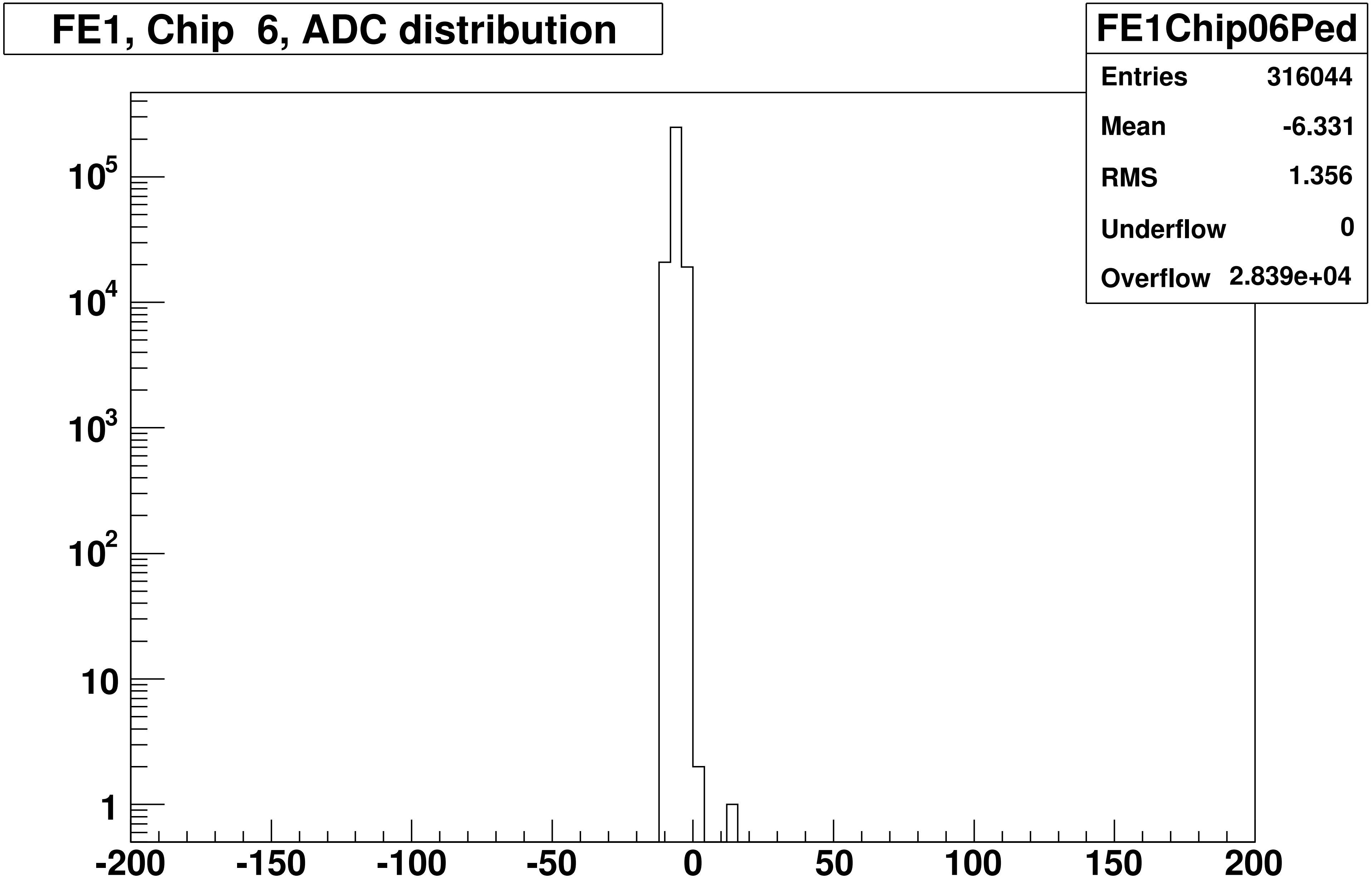
10000
15000
20000
25000


FE1, Chip 6, ADC distribution
FE1Chip06Ped
Entries 316044
Mean -6.331
RMS 1.356
Underflow 0
Overflow 2.839e+04
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10^3
10^2
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-100
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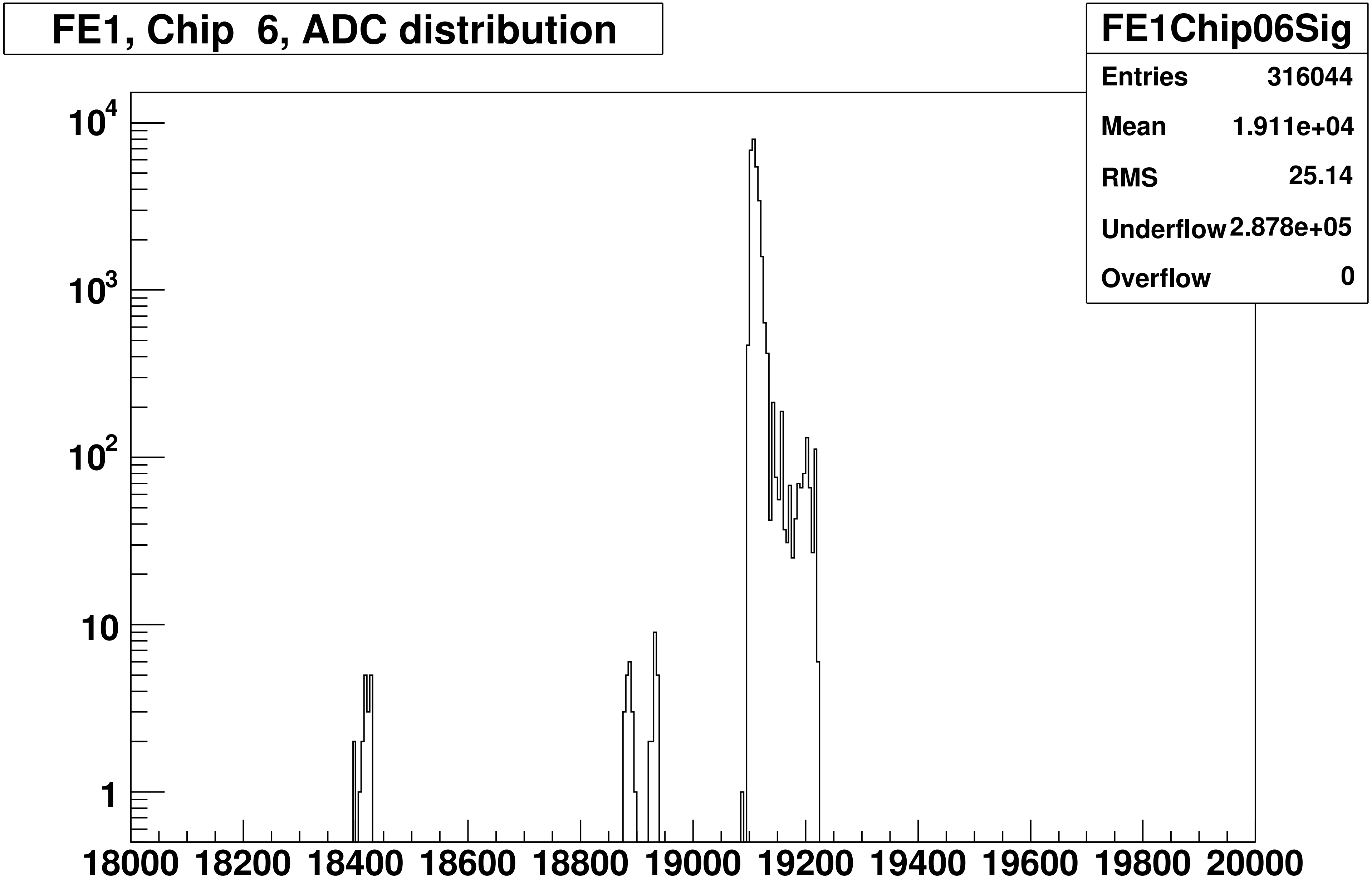
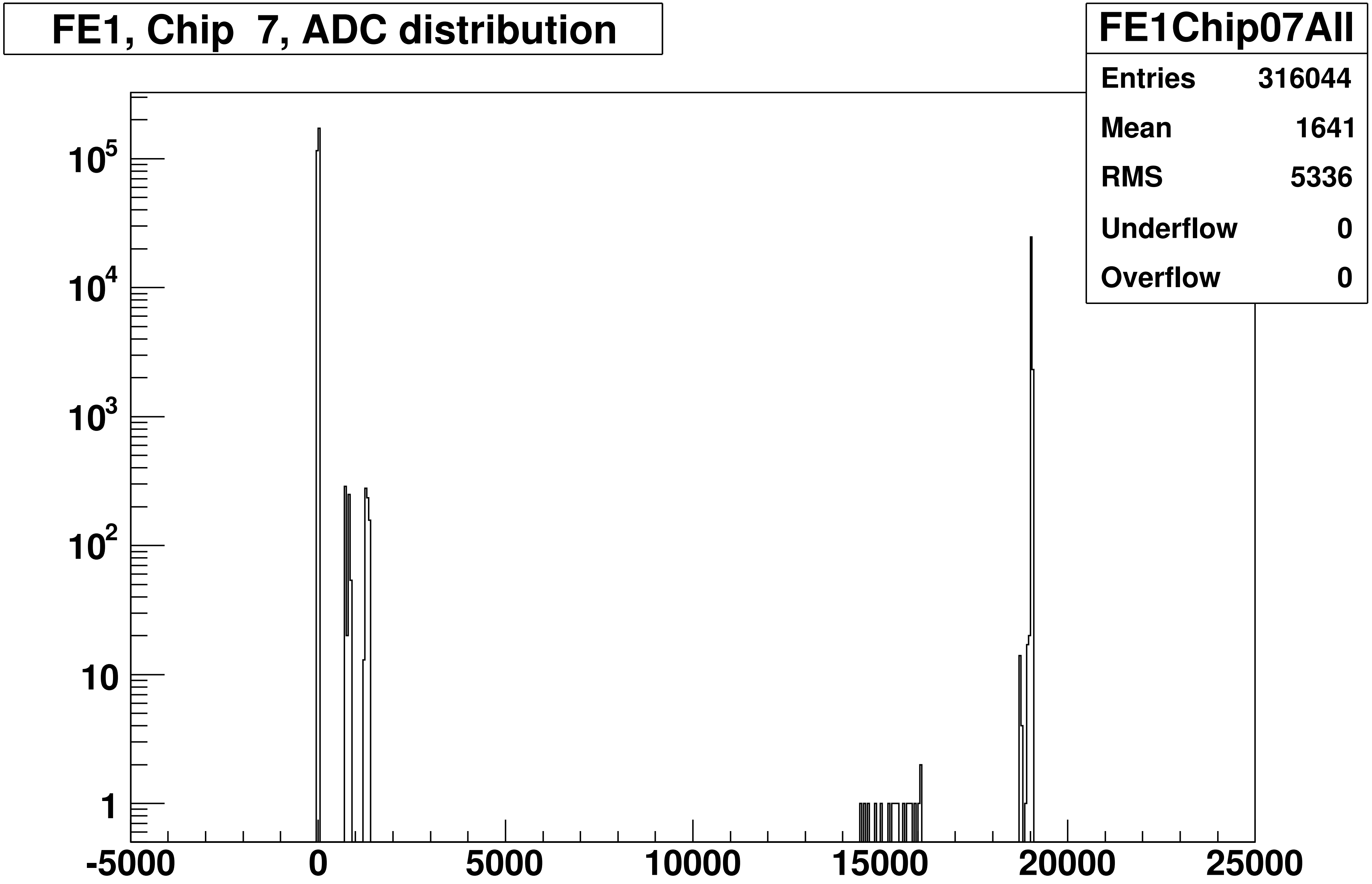
100
150
200


FE1, Chip 6, ADC distribution
FE1Chip06Sig
Entries 316044
Mean 1.911e+04
RMS 25.14
Underflow 2.878e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000


FE1, Chip 7, ADC distribution
FE1Chip07All
Entries 316044
Mean 1641
RMS 5336
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
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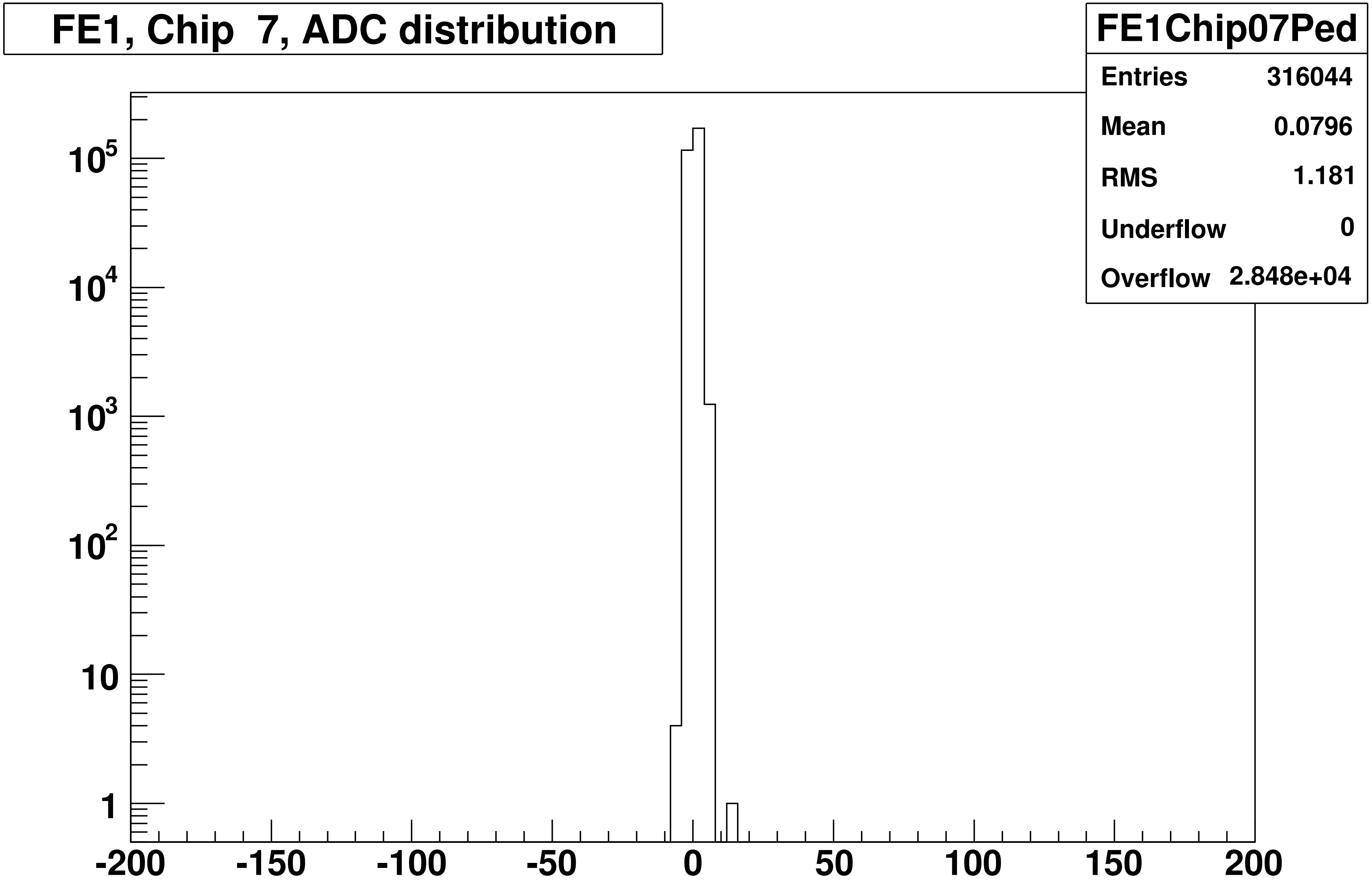
-5000
0
5000
10000
15000
20000
25000



FE1, Chip 7, ADC distribution
FE1Chip07Ped
Entries 316044
Mean 0.0796
RMS 1.181
Underflow 0
Overflow 2.848e+04
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10^4
10^3
10^2
10
1
-200
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-100
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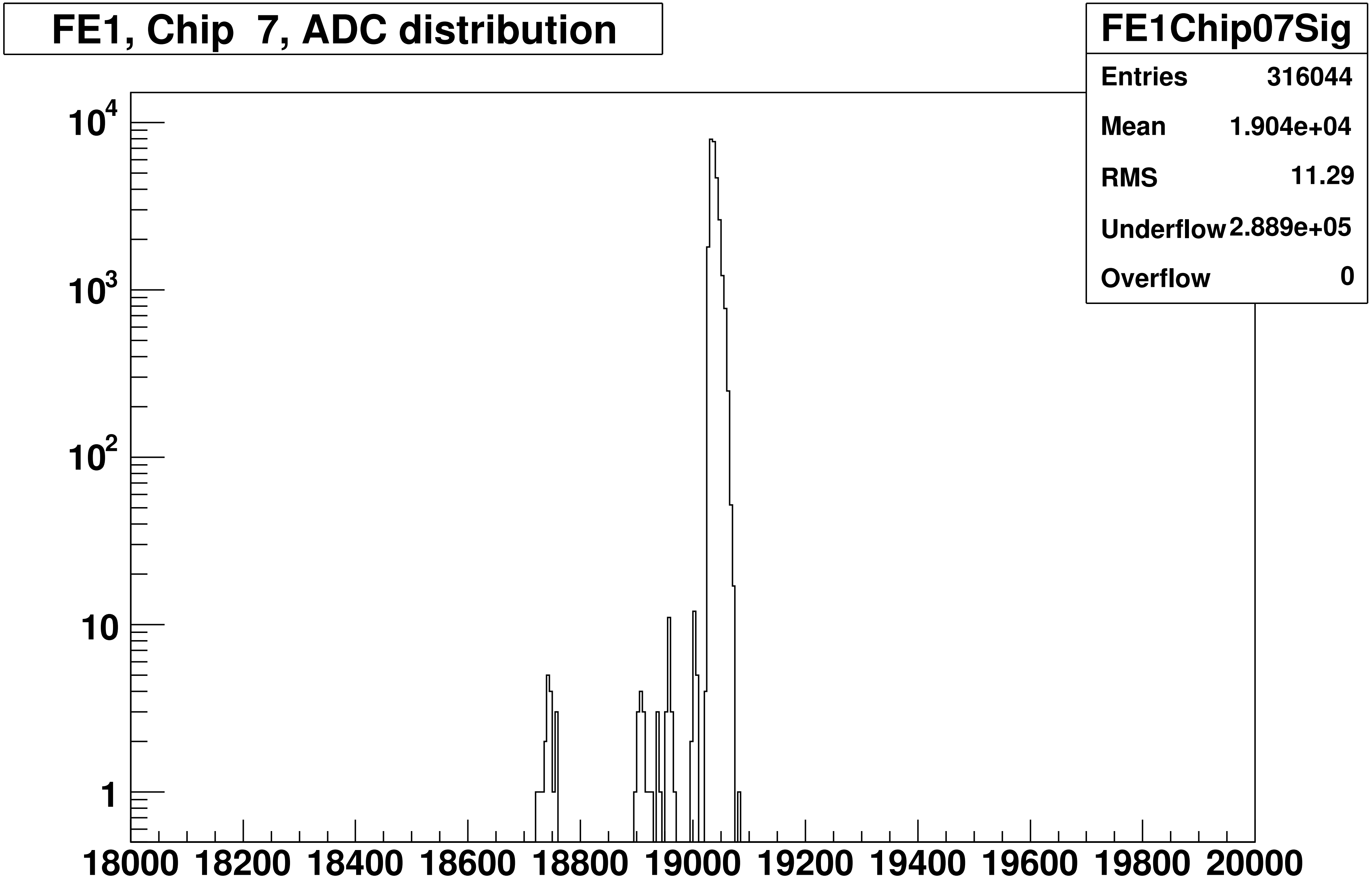
100
150
200



FE1, Chip 7, ADC distribution
FE1Chip07Sig
Entries 316044
Mean 1.904e+04
RMS 11.29
Underflow 2.889e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
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19600
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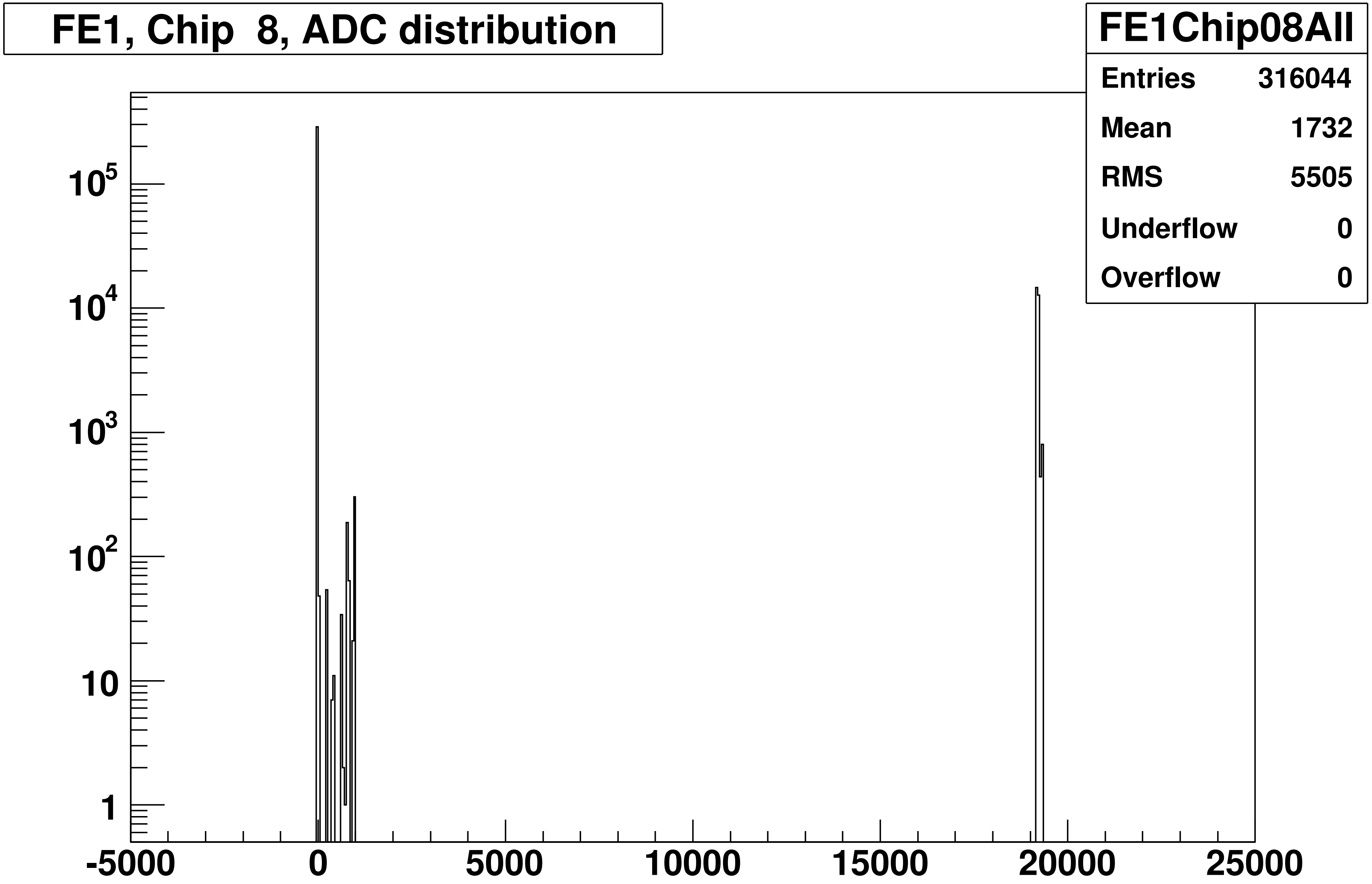
20000



FE1, Chip 8, ADC distribution
FE1Chip08All
Entries 316044
Mean 1732
RMS 5505
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
1
-5000
0
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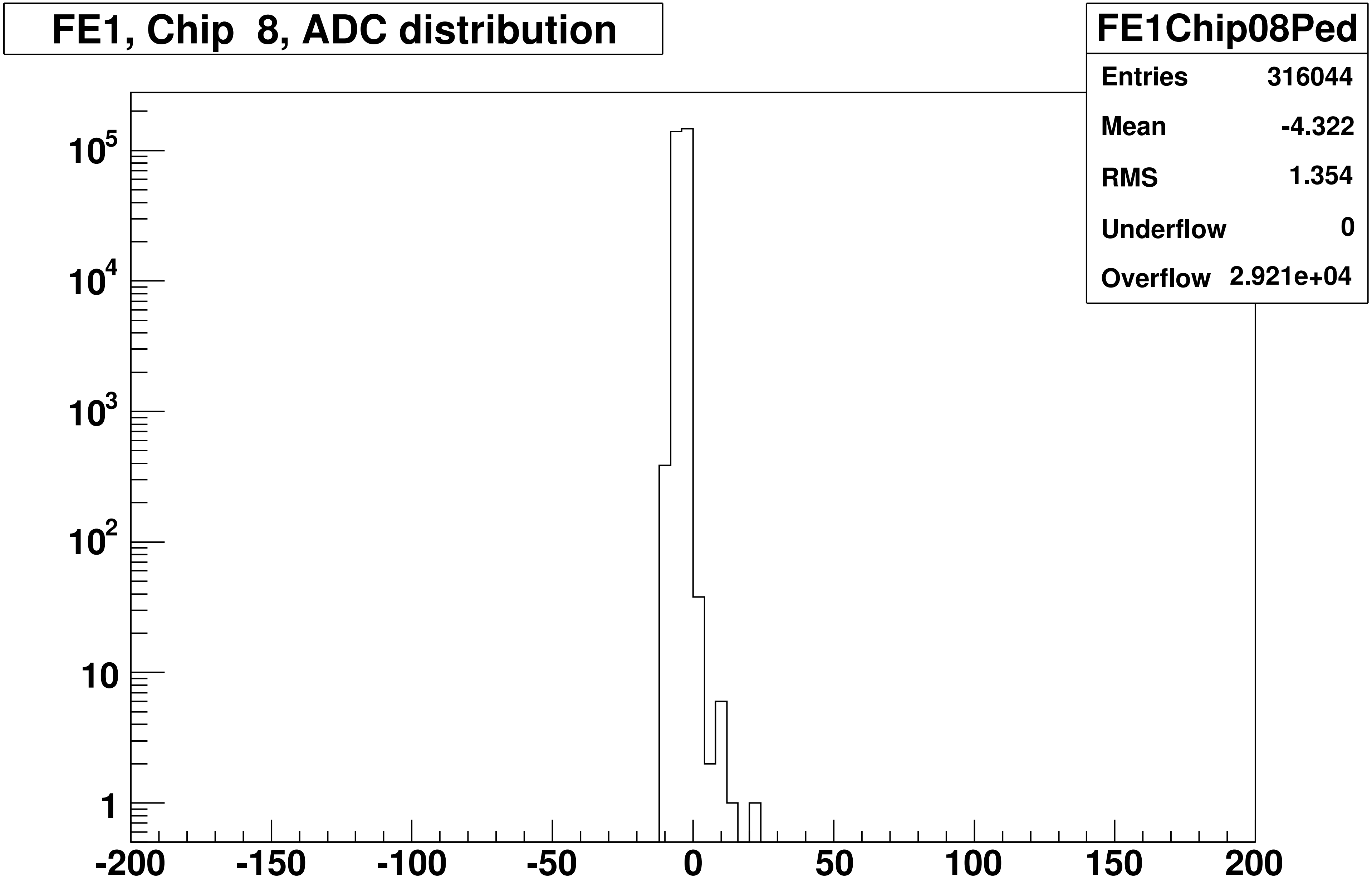
10000
15000
20000
25000



FE1, Chip 8, ADC distribution
FE1Chip08Ped
Entries 316044
Mean -4.322
RMS 1.354
Underflow 0
Overflow 2.921e+04
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10^4
10^3
10^2
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100
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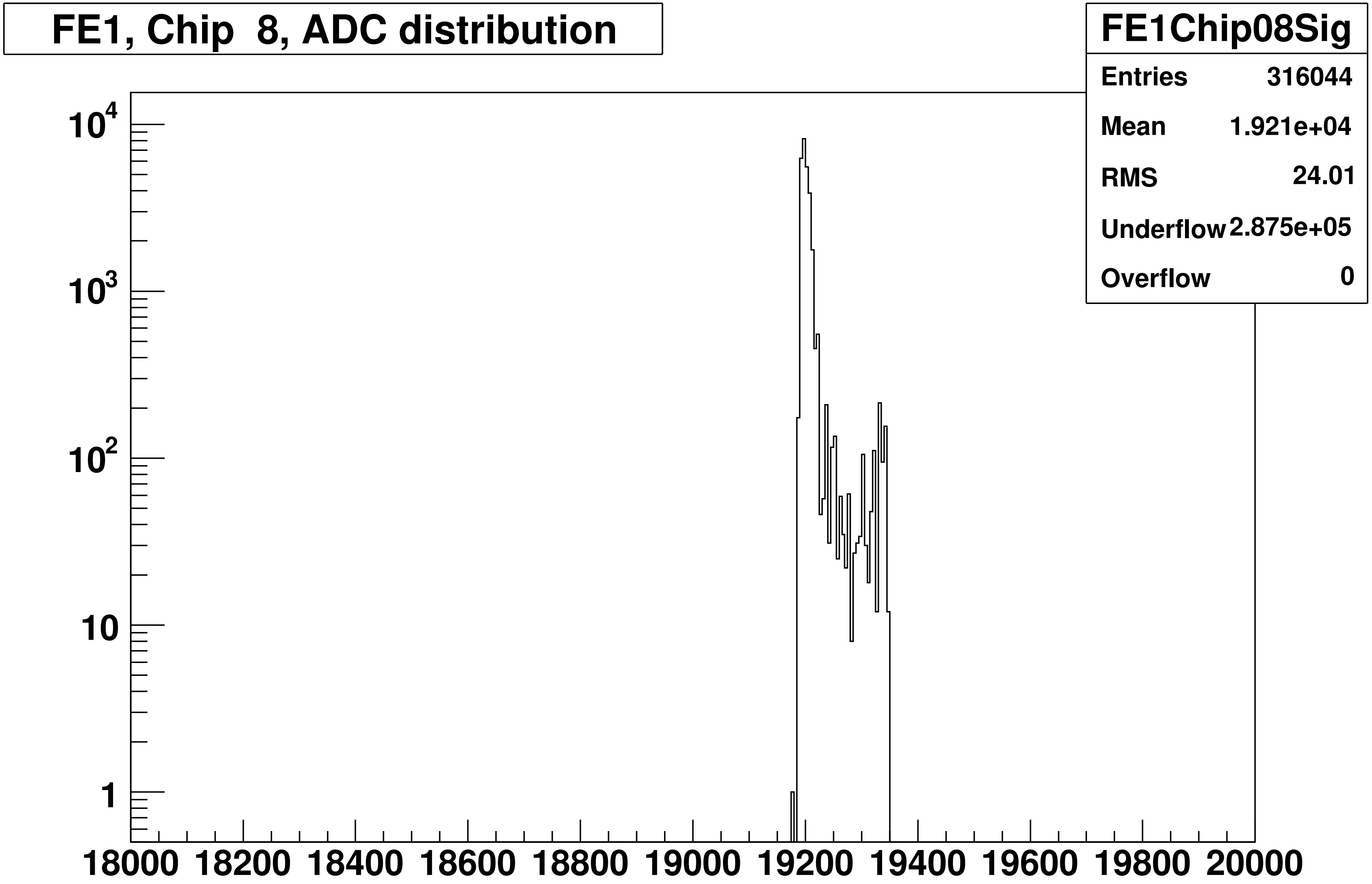
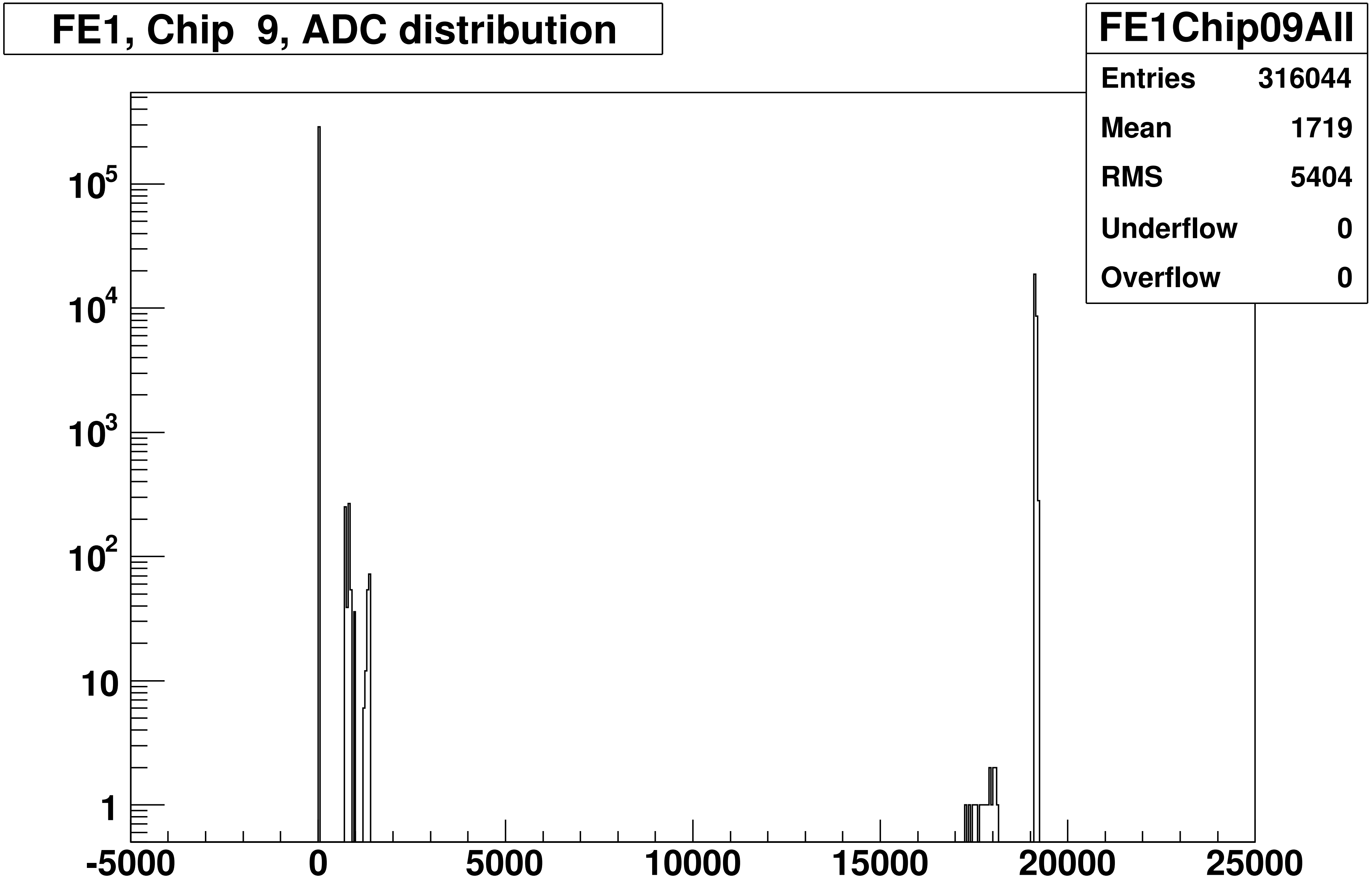

FE1, Chip 8, ADC distribution
FE1Chip08Sig
Entries 316044
Mean 1.921e+04
RMS 24.01
Underflow 2.875e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000


FE1, Chip 9, ADC distribution
FE1Chip09All
Entries 316044
Mean 1719
RMS 5404
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
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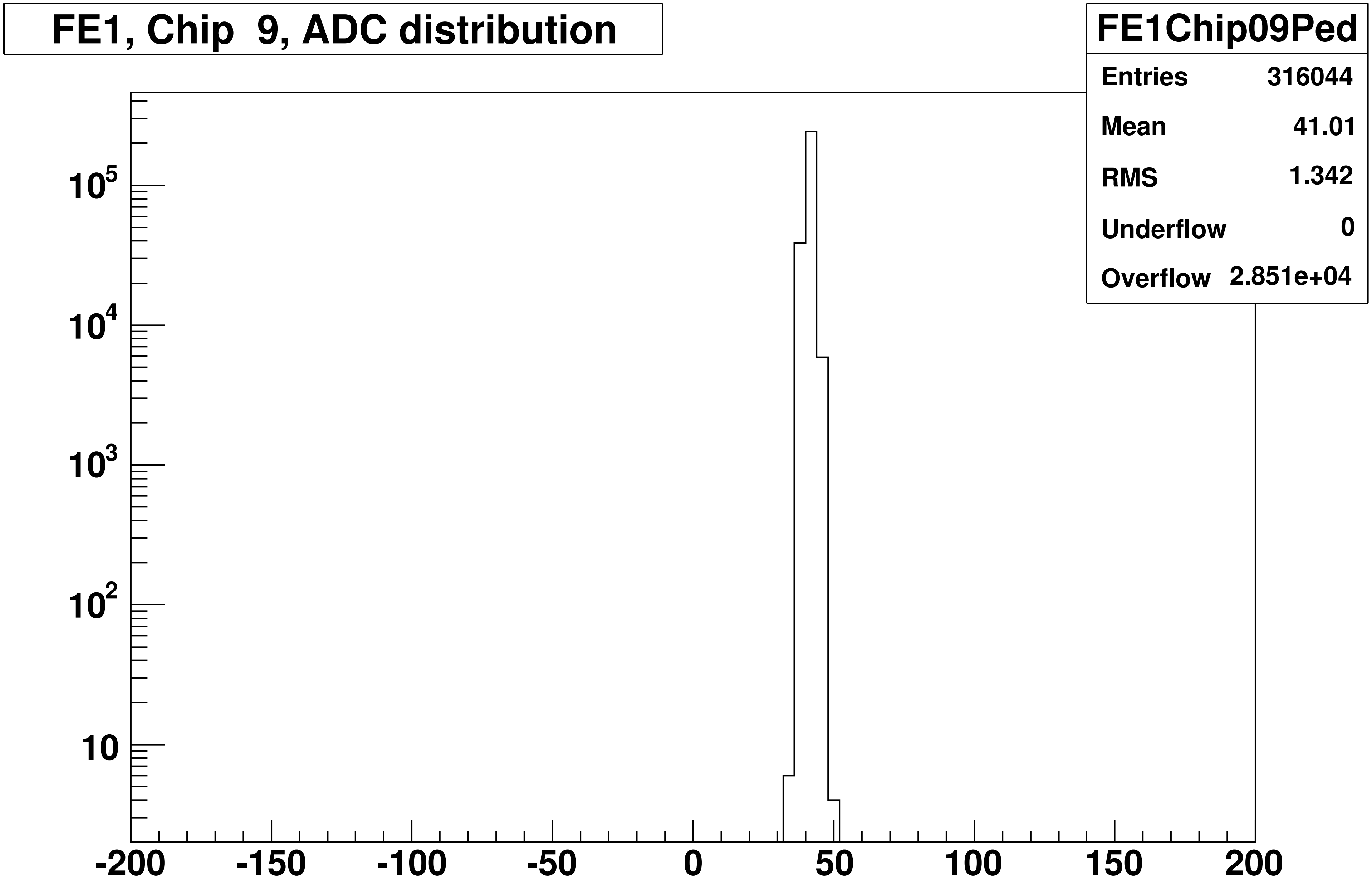
10000
15000
20000
25000



FE1, Chip 9, ADC distribution
FE1Chip09Ped
Entries 316044
Mean 41.01
RMS 1.342
Underflow 0
Overflow 2.851e+04
10
10^2
10^3
10^4
10^5
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-100
-50
0
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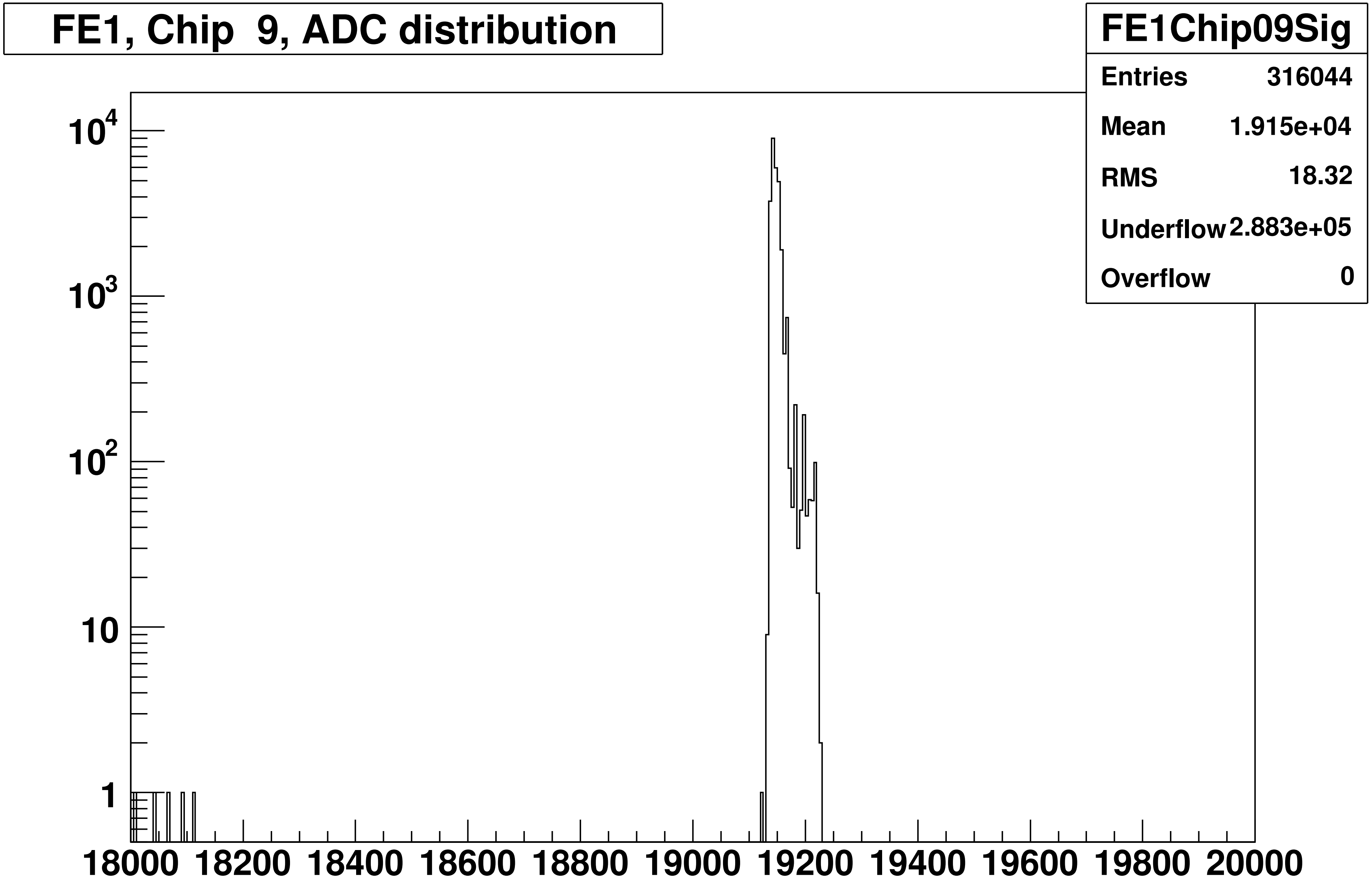
150
200


FE1, Chip 9, ADC distribution
FE1Chip09Sig
Entries 316044
Mean 1.915e+04
RMS 18.32
Underflow 2.883e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
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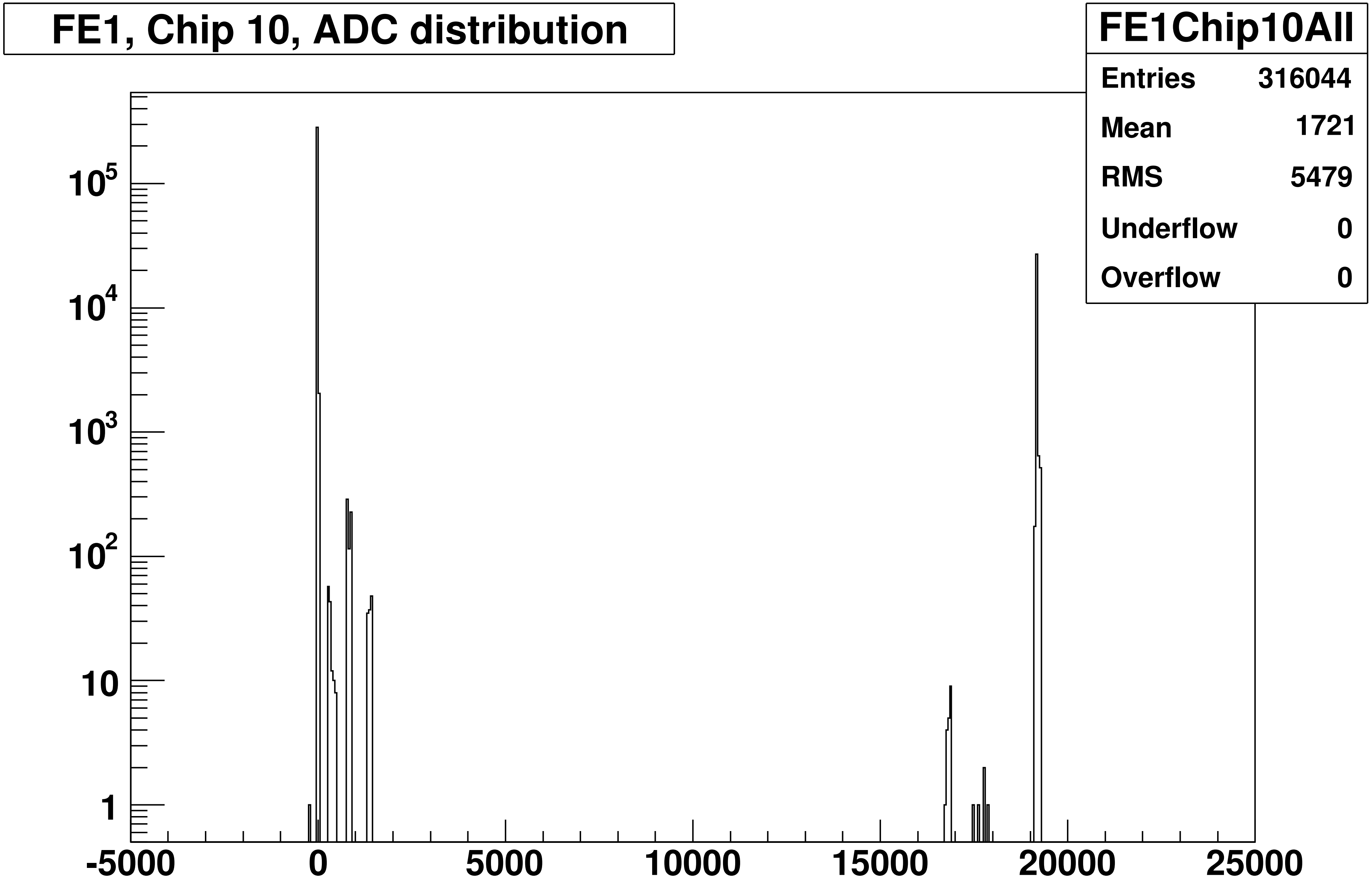
19600
19800
20000



FE1, Chip 10, ADC distribution
FE1Chip10All
Entries 316044
Mean 1721
RMS 5479
Underflow 0
Overflow 0
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10
10^2
10^3
10^4
10^5
-5000
0
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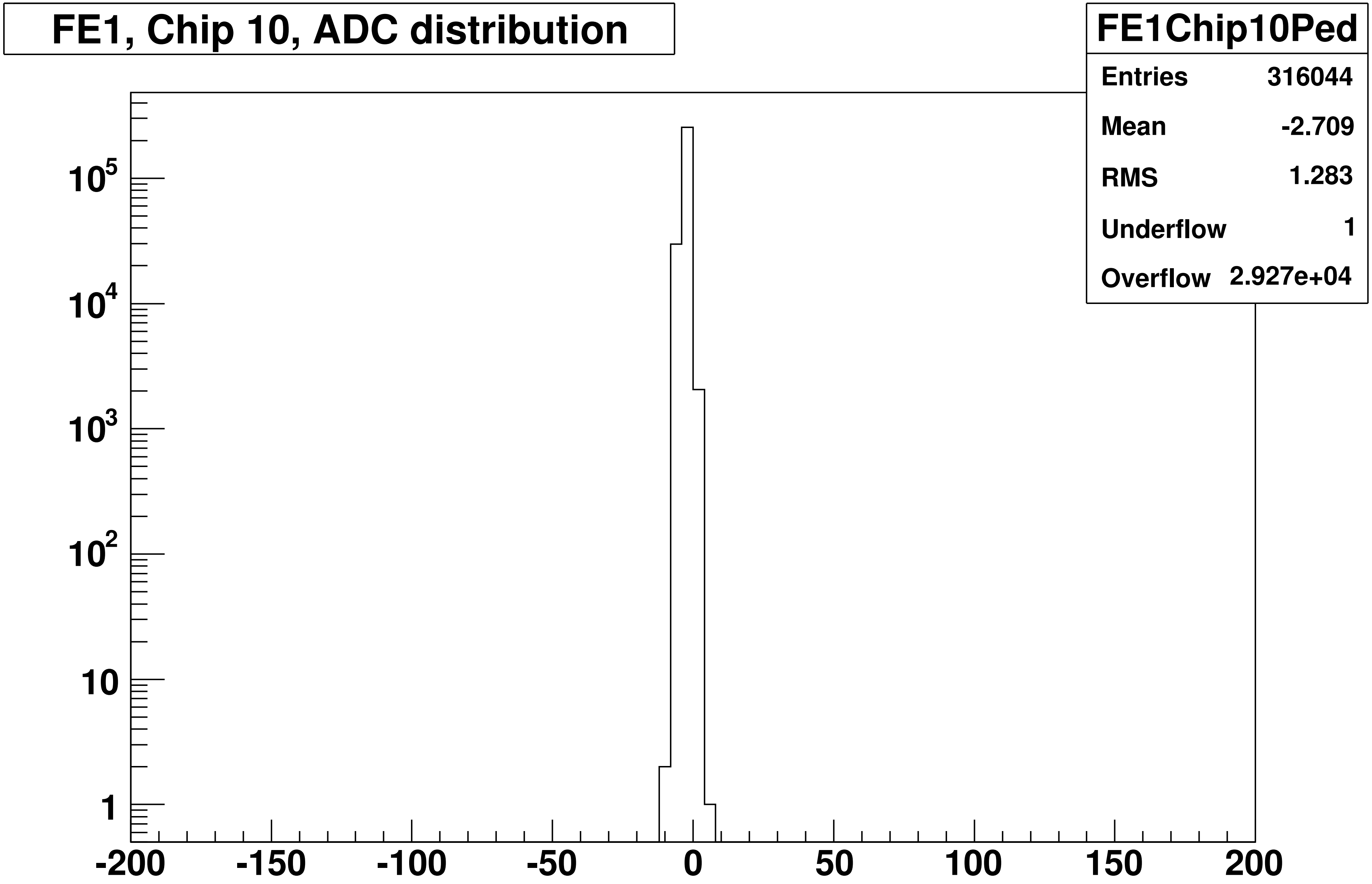
10000
15000
20000
25000


FE1, Chip 10, ADC distribution
FE1Chip10Ped
Entries 316044
Mean -2.709
RMS 1.283
Underflow 1
Overflow 2.927e+04
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10^4
10^3
10^2
10
1
-200
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-100
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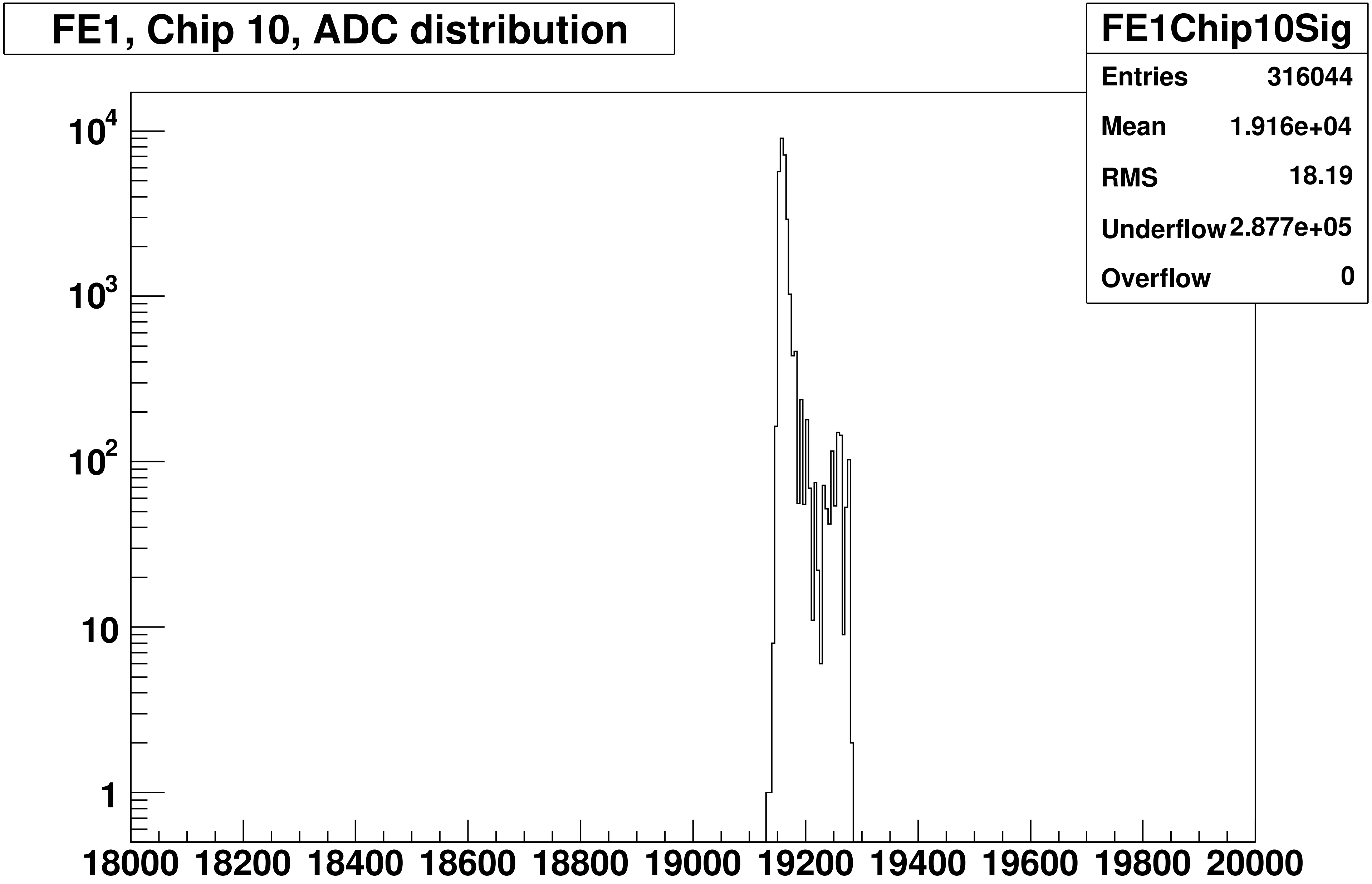
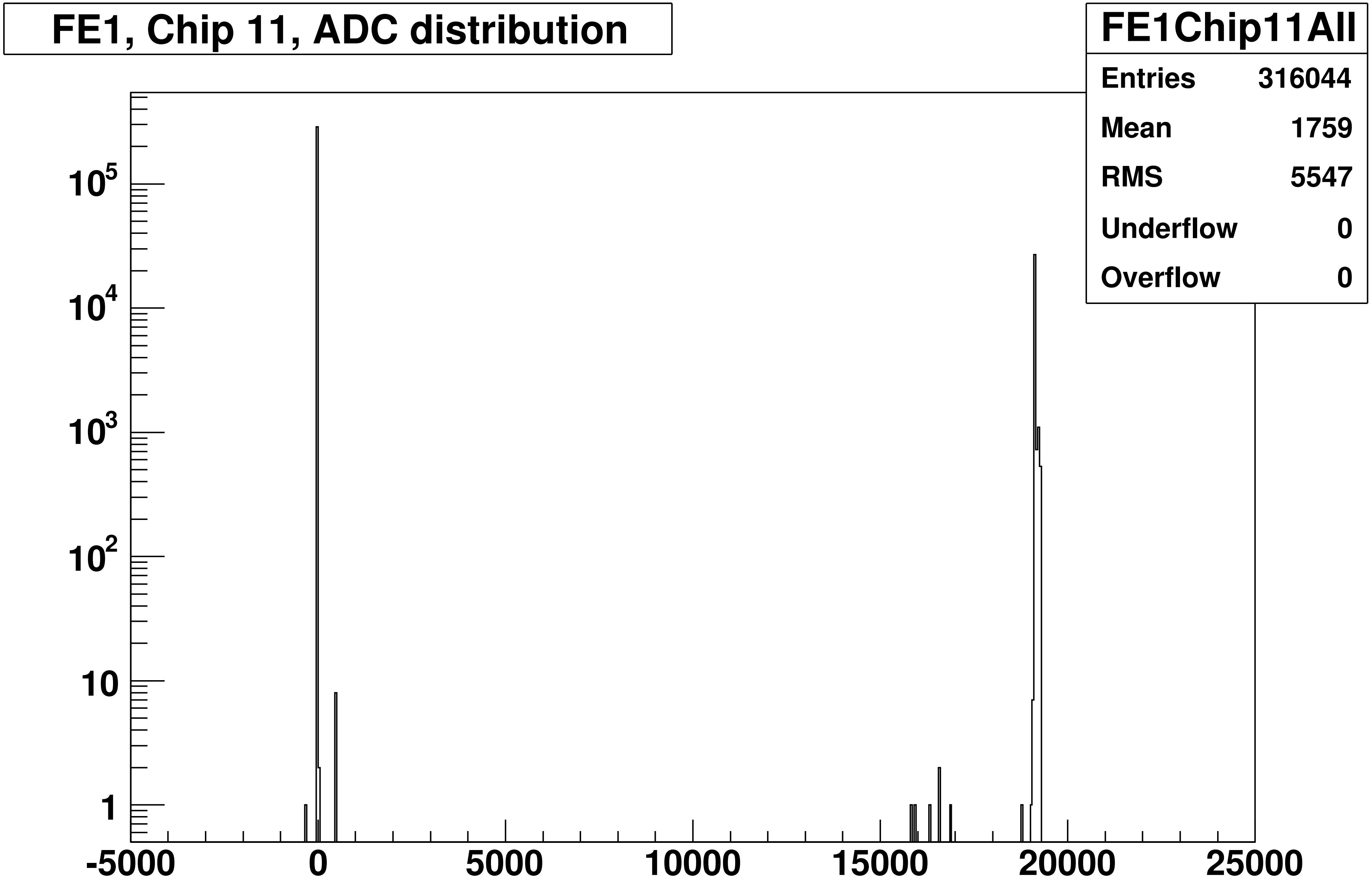
50
100
150
200



FE1, Chip 10, ADC distribution
FE1Chip10Sig
Entries 316044
Mean 1.916e+04
RMS 18.19
Underflow 2.877e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE1, Chip 11, ADC distribution
FE1Chip11All
Entries 316044
Mean 1759
RMS 5547
Underflow 0
Overflow 0
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10^4
10^3
10^2
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-5000
0
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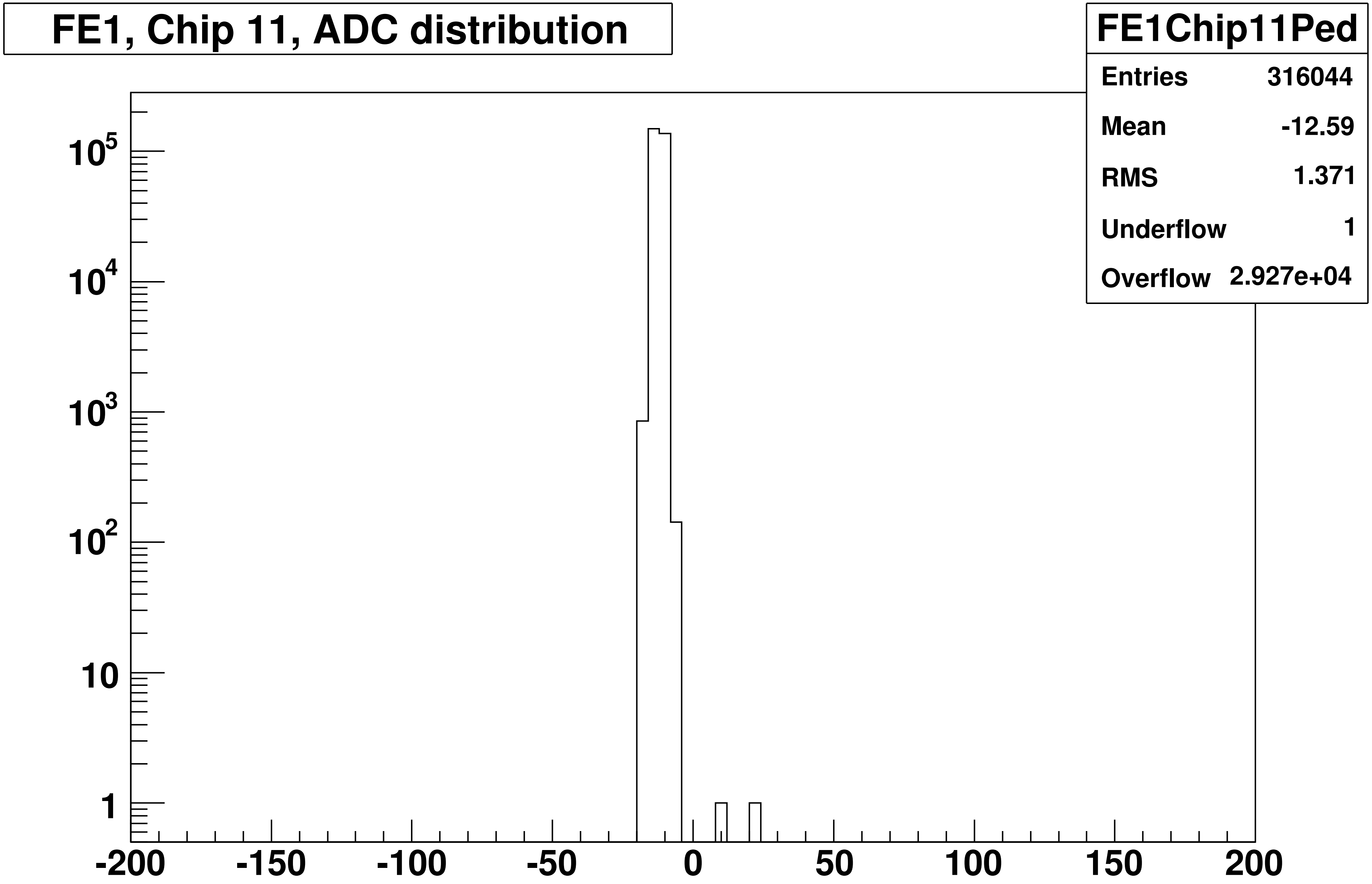
10000
15000
20000
25000


FE1, Chip 11, ADC distribution
FE1Chip11Ped
Entries 316044
Mean -12.59
RMS 1.371
Underflow 1
Overflow 2.927e+04
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10^4
10^3
10^2
10
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-100
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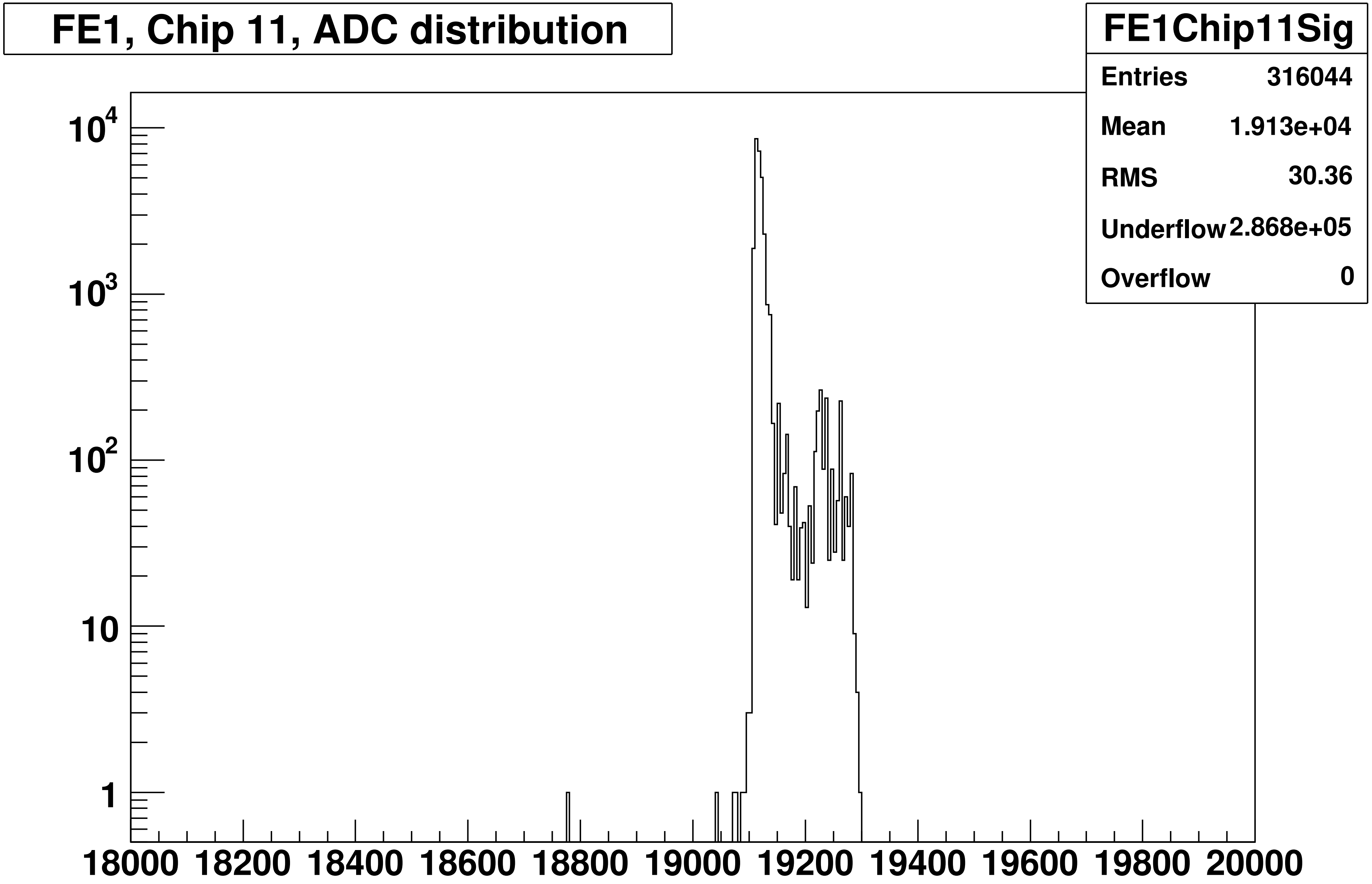
150
200


FE1, Chip 11, ADC distribution
FE1Chip11Sig
Entries 316044
Mean 1.913e+04
RMS 30.36
Underflow 2.868e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
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19000
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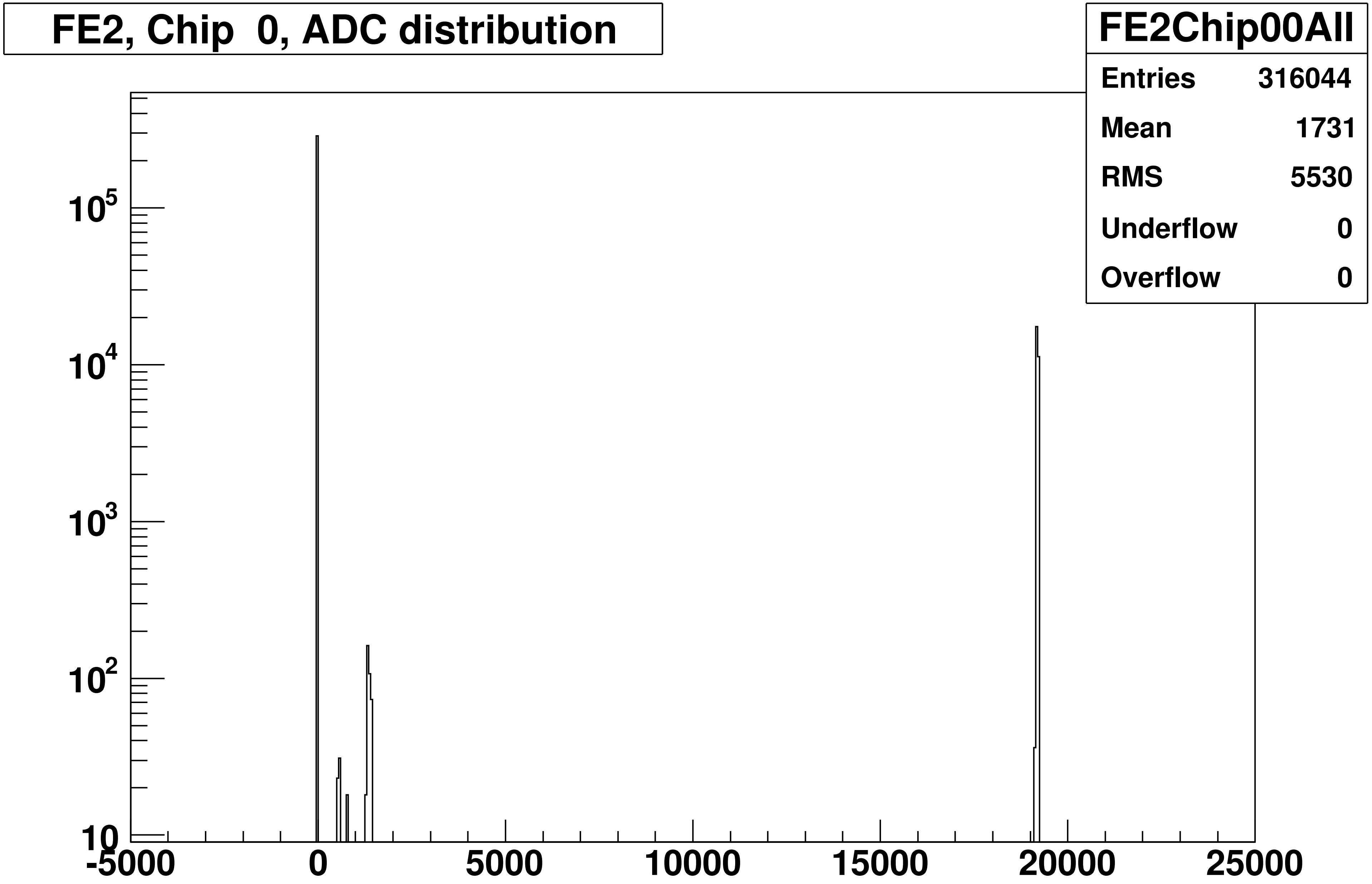
19600
19800
20000


FE2, Chip 0, ADC distribution
FE2Chip00All
Entries 316044
Mean 1731
RMS 5530
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
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0
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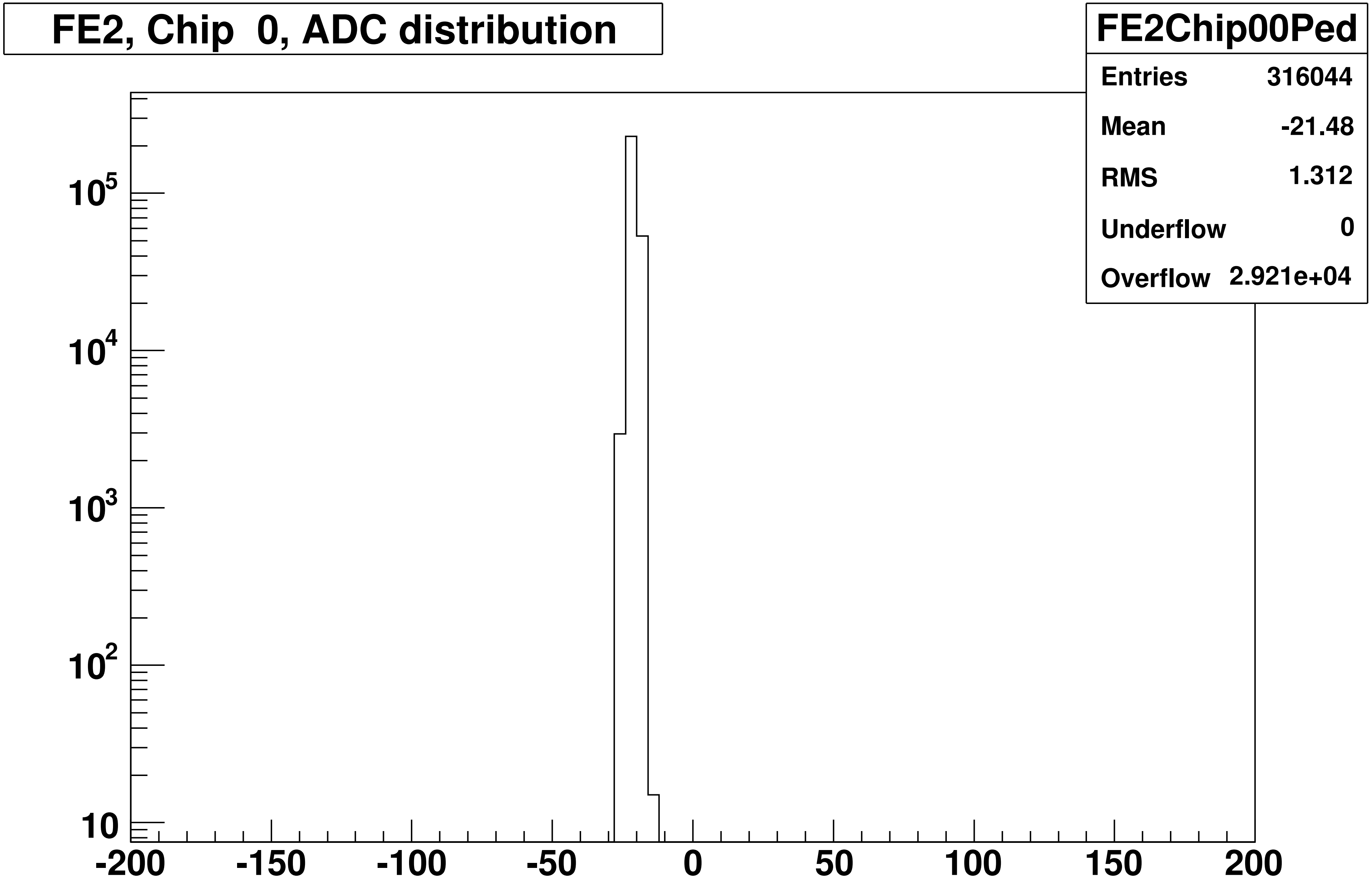
10000
15000
20000
25000


FE2, Chip 0, ADC distribution
FE2Chip00Ped
Entries 316044
Mean -21.48
RMS 1.312
Underflow 0
Overflow 2.921e+04
10^5
10^4
10^3
10^2
10
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-100
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100
150
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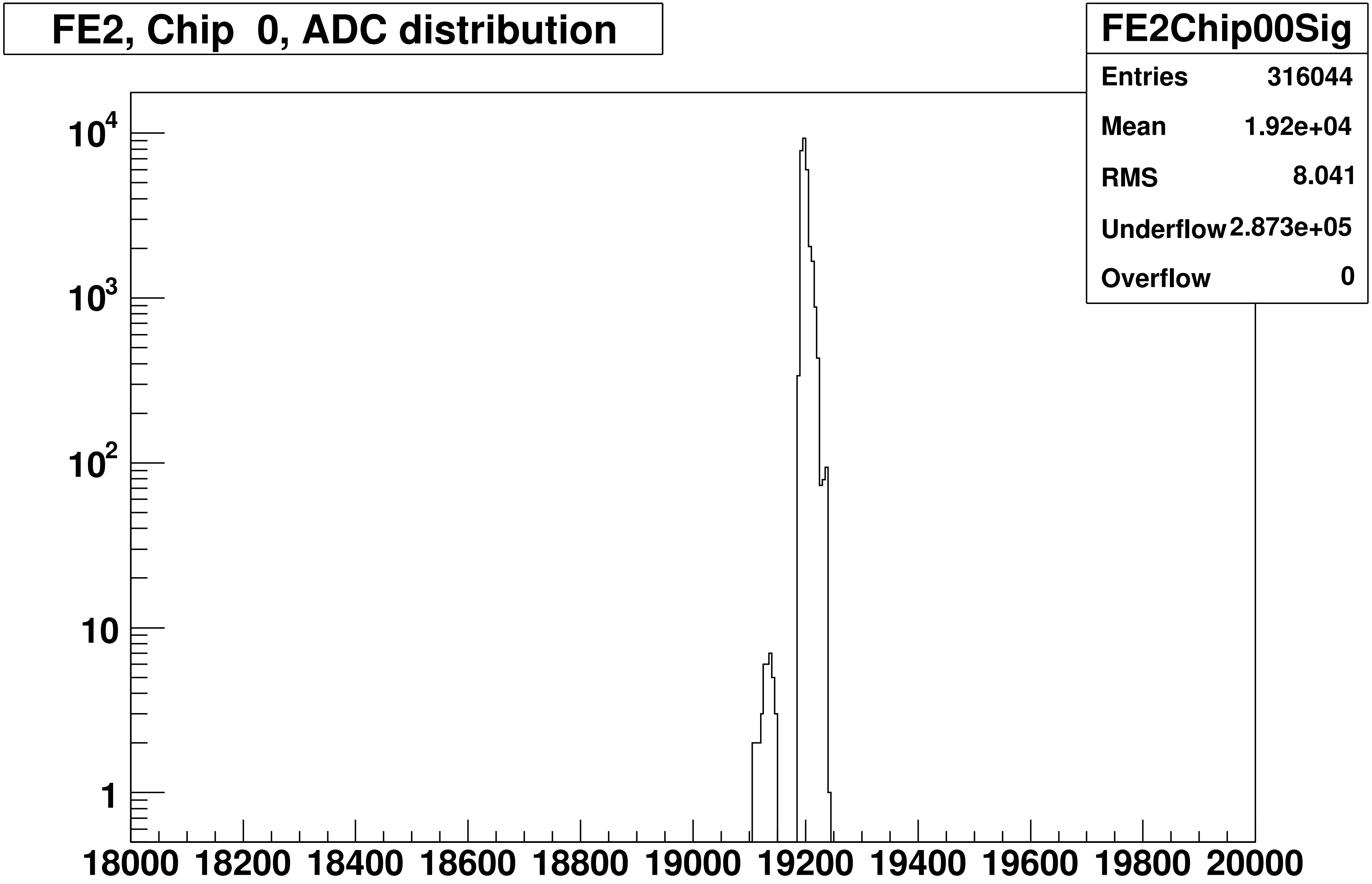
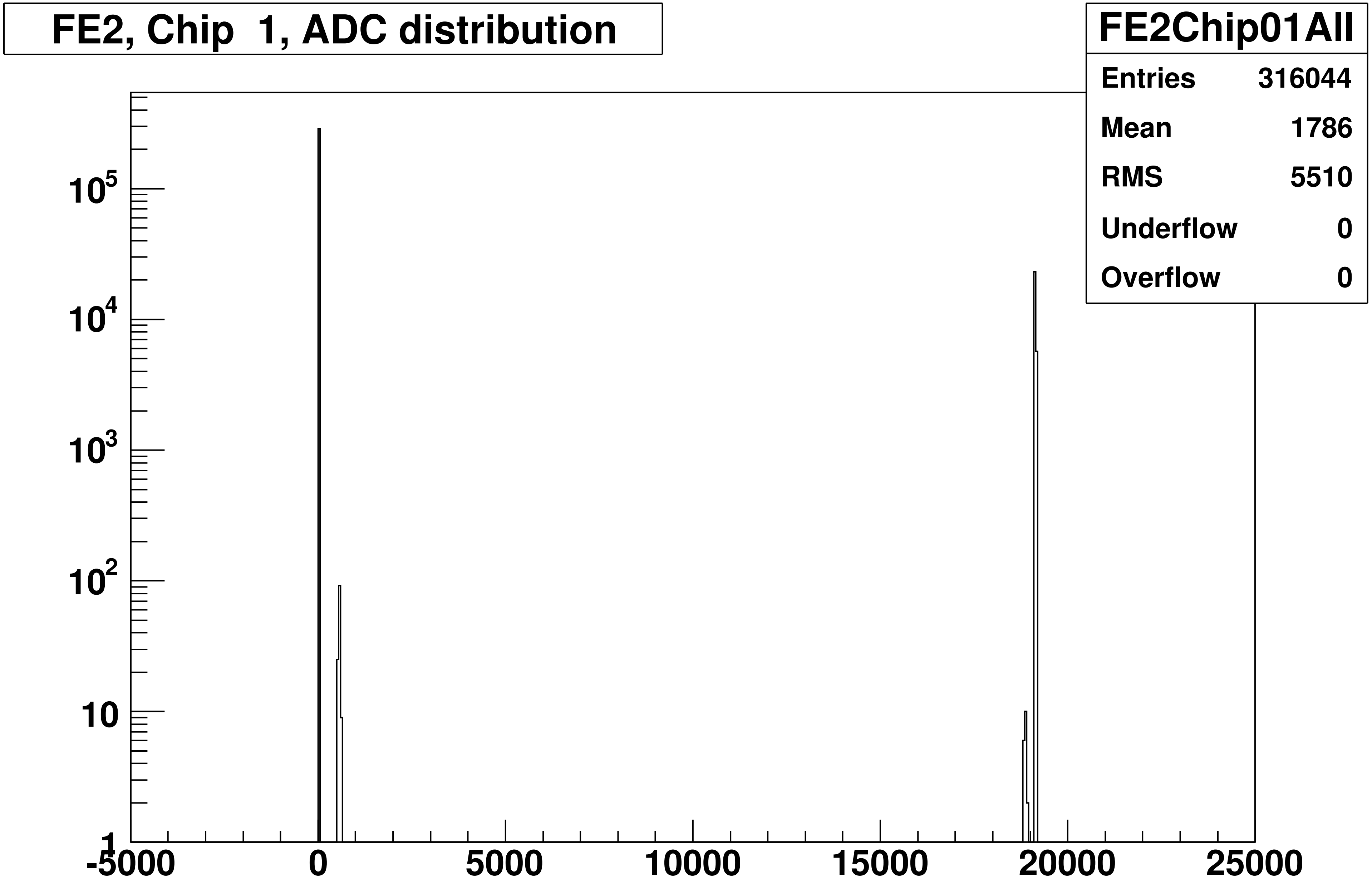


FE2, Chip 0, ADC distribution
FE2Chip00Sig
Entries 316044
Mean 1.92e+04
RMS 8.041
Underflow 2.873e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE2, Chip 1, ADC distribution
FE2Chip01All
Entries 316044
Mean 1786
RMS 5510
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
1
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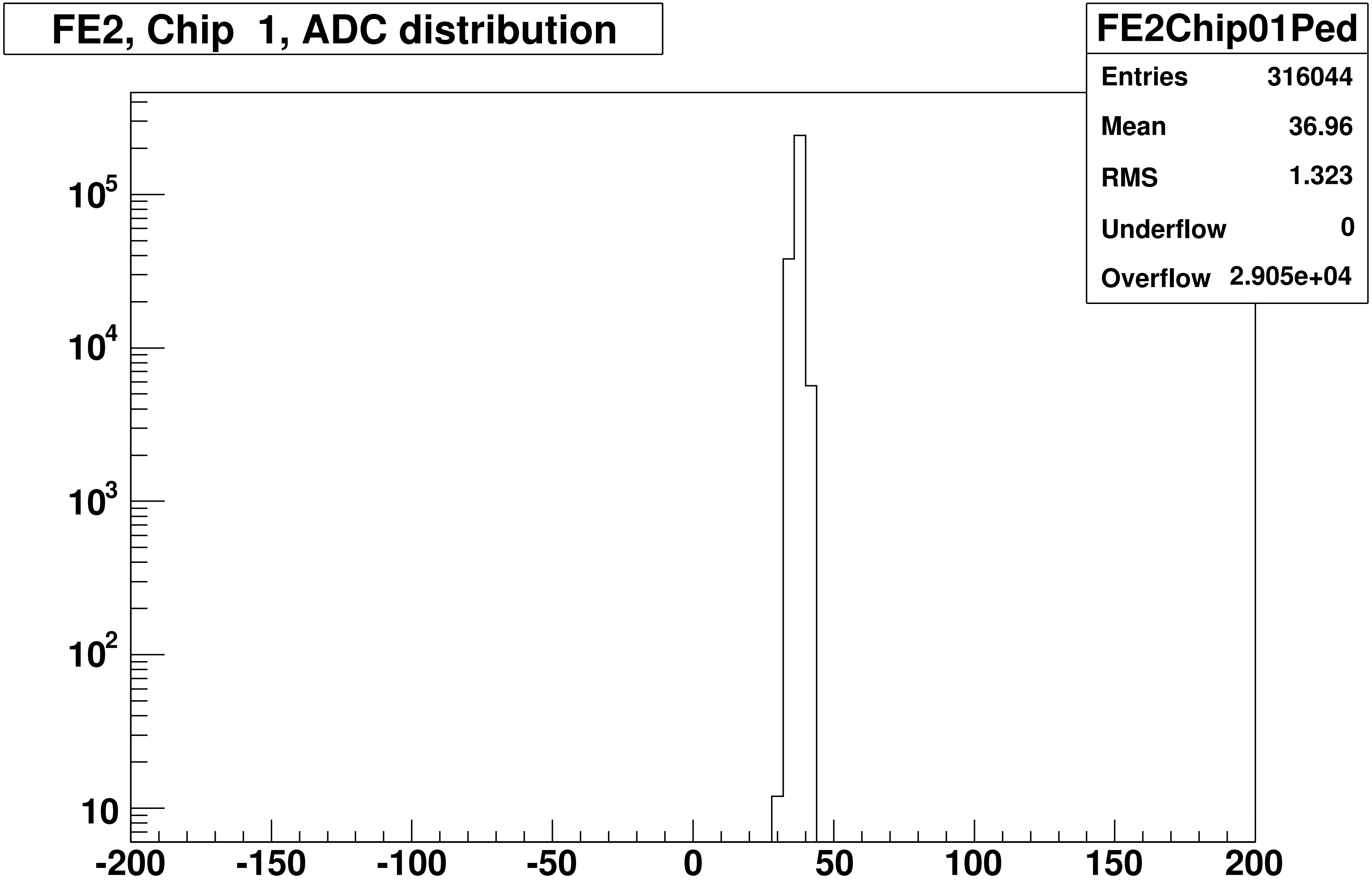
25000


FE2, Chip 1, ADC distribution
FE2Chip01Ped
Entries 316044
Mean 36.96
RMS 1.323
Underflow 0
Overflow 2.905e+04
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10^3
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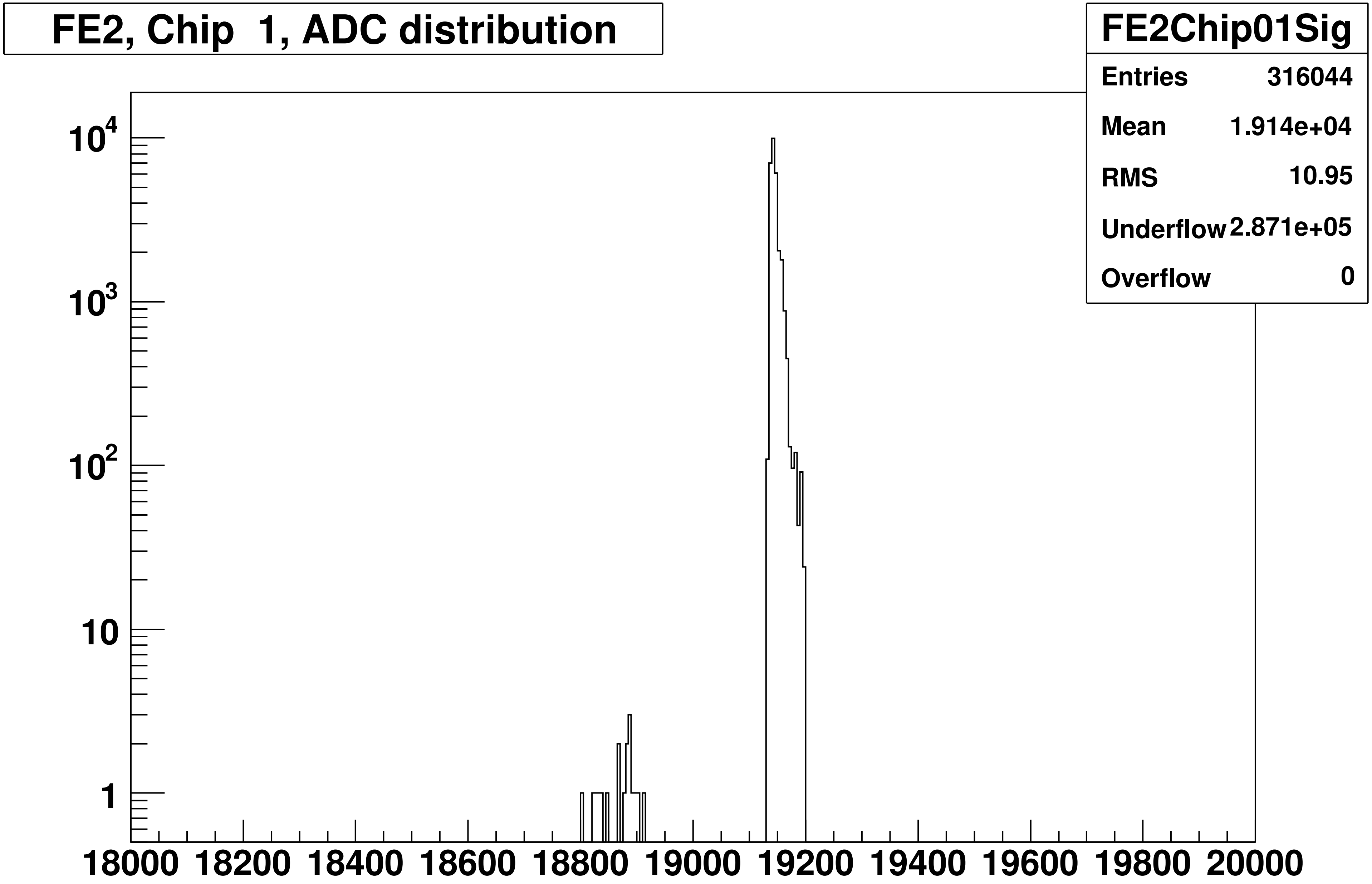
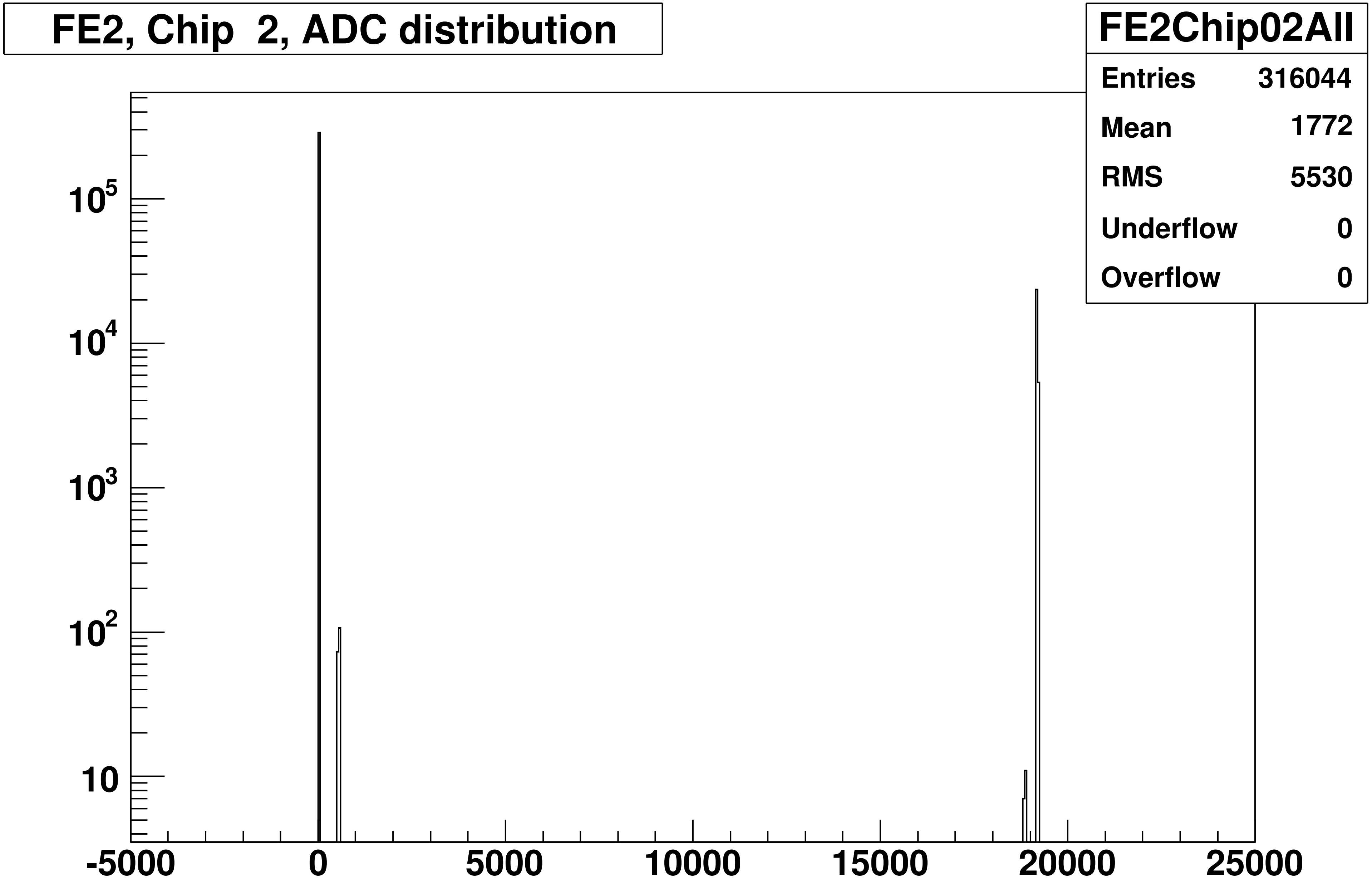
150
200



FE2, Chip 1, ADC distribution
FE2Chip01Sig
Entries 316044
Mean 1.914e+04
RMS 10.95
Underflow 2.871e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE2, Chip 2, ADC distribution
FE2Chip02All
Entries 316044
Mean 1772
RMS 5530
Underflow 0
Overflow 0
10
10^2
10^3
10^4
10^5
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0
5000
10000
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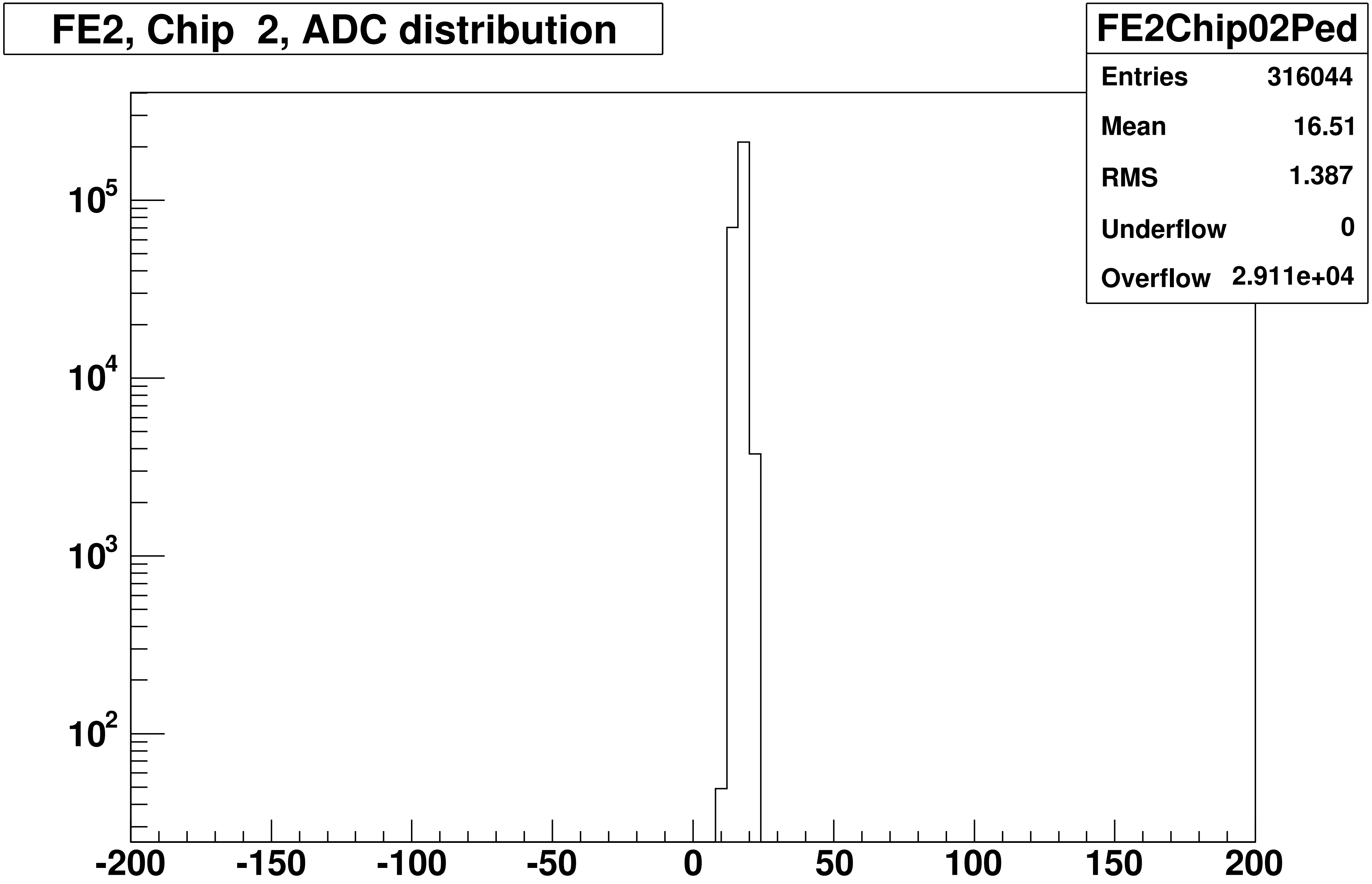
20000
25000


FE2, Chip 2, ADC distribution
FE2Chip02Ped
Entries 316044
Mean 16.51
RMS 1.387
Underflow 0
Overflow 2.911e+04
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10^4
10^3
10^2
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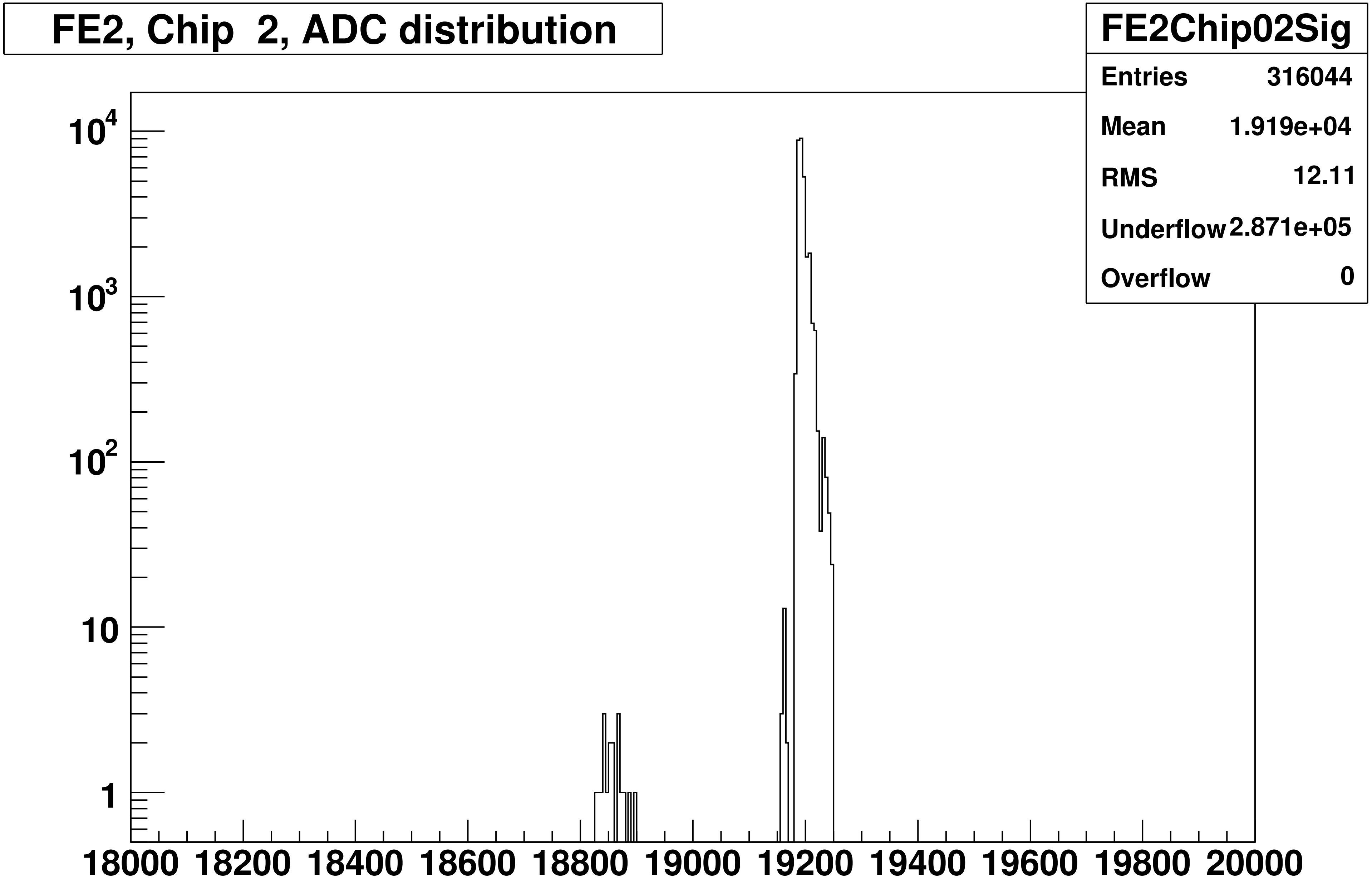
FE2, Chip 2, ADC distribution
FE2Chip02Sig
Entries 316044
Mean 1.919e+04
RMS 12.11
Underflow 2.871e+05
Overflow 0
10^4
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10^2
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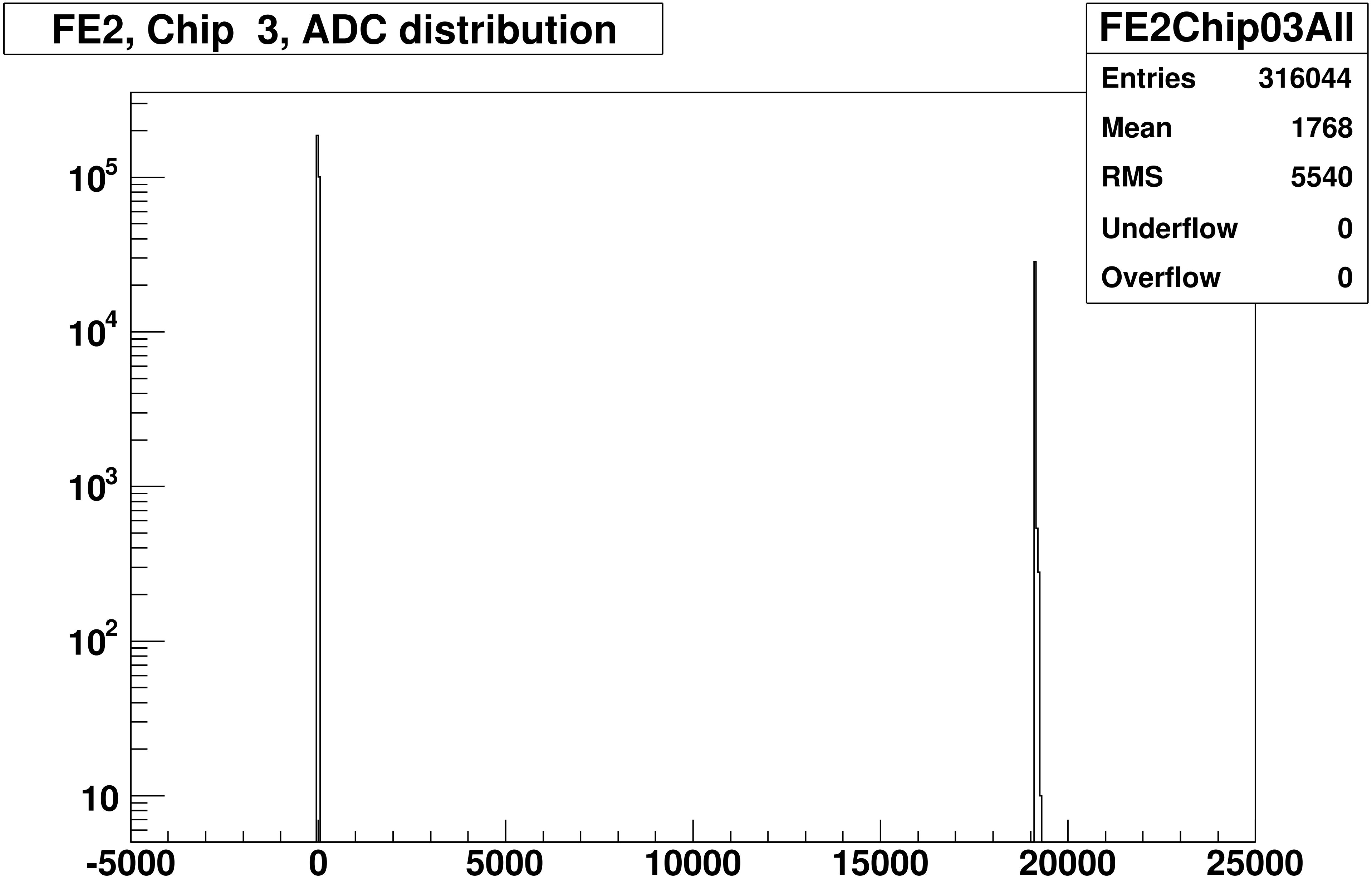
FE2, Chip 3, ADC distribution
FE2Chip03All
Entries 316044
Mean 1768
RMS 5540
Underflow 0
Overflow 0
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10^4
10^3
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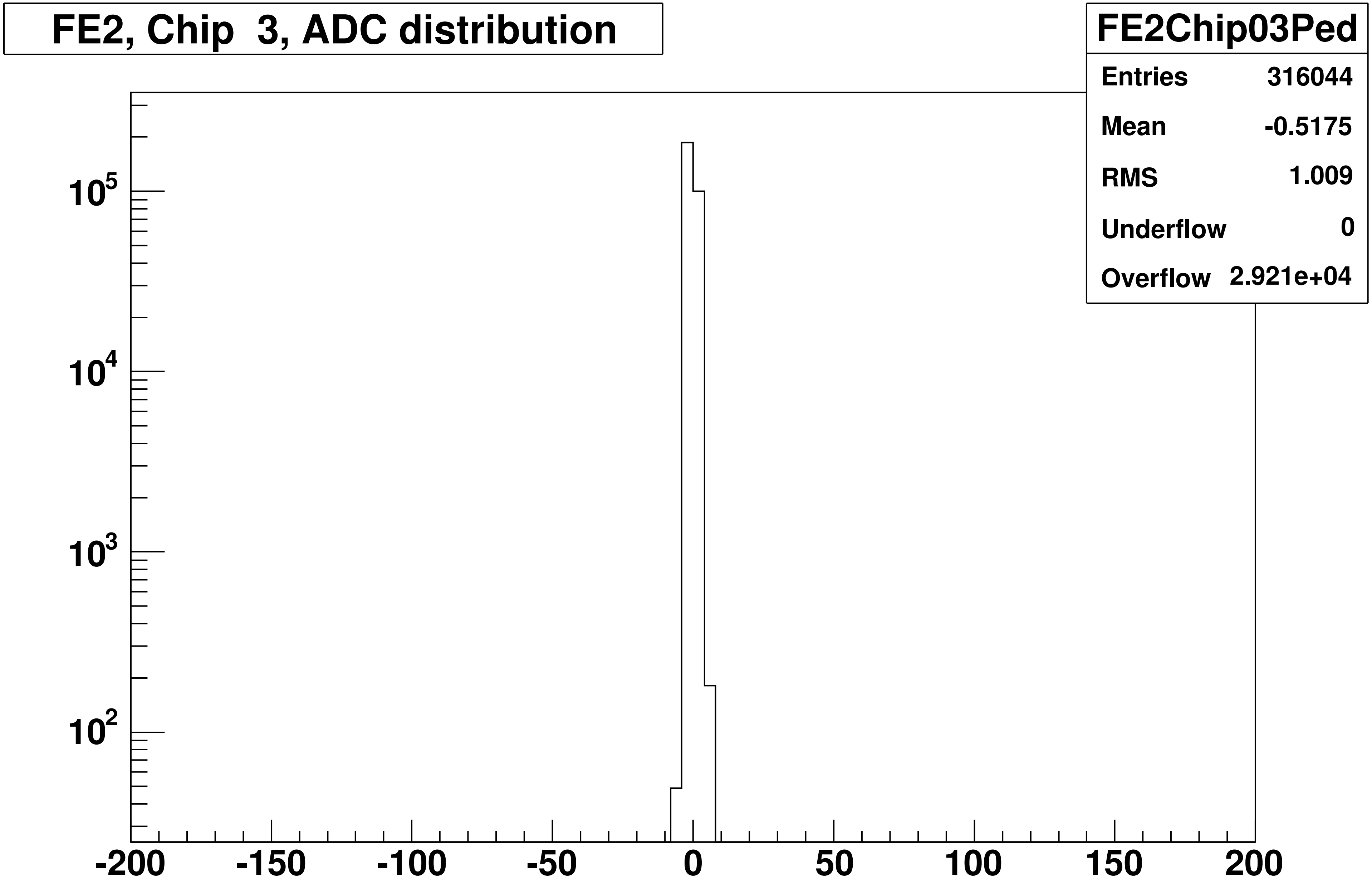

FE2, Chip 3, ADC distribution
FE2Chip03Ped
Entries 316044
Mean -0.5175
RMS 1.009
Underflow 0
Overflow 2.921e+04
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10^4
10^3
10^2
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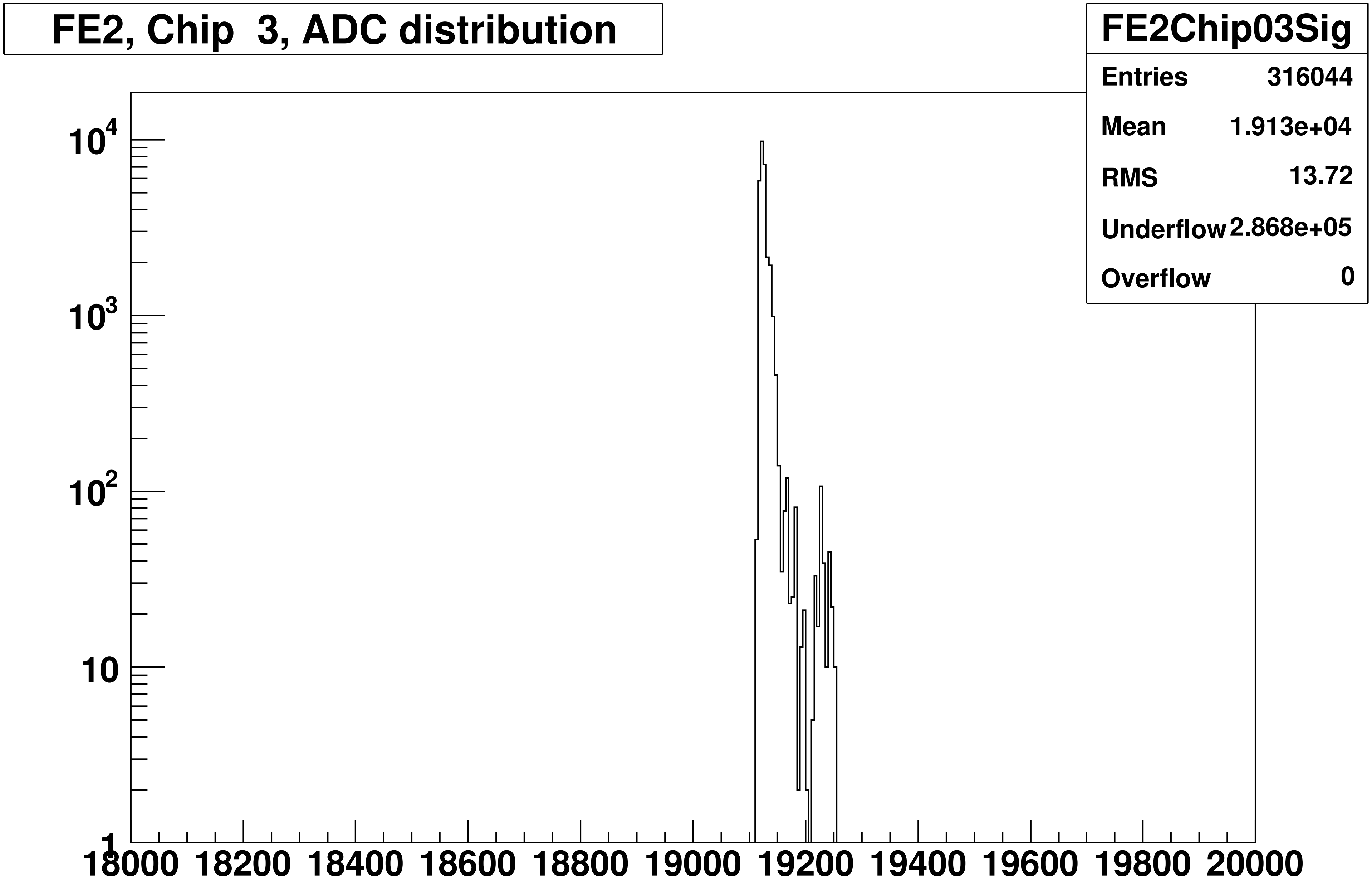

FE2, Chip 3, ADC distribution
FE2Chip03Sig
Entries 316044
Mean 1.913e+04
RMS 13.72
Underflow 2.868e+05
Overflow 0
10^4
10^3
10^2
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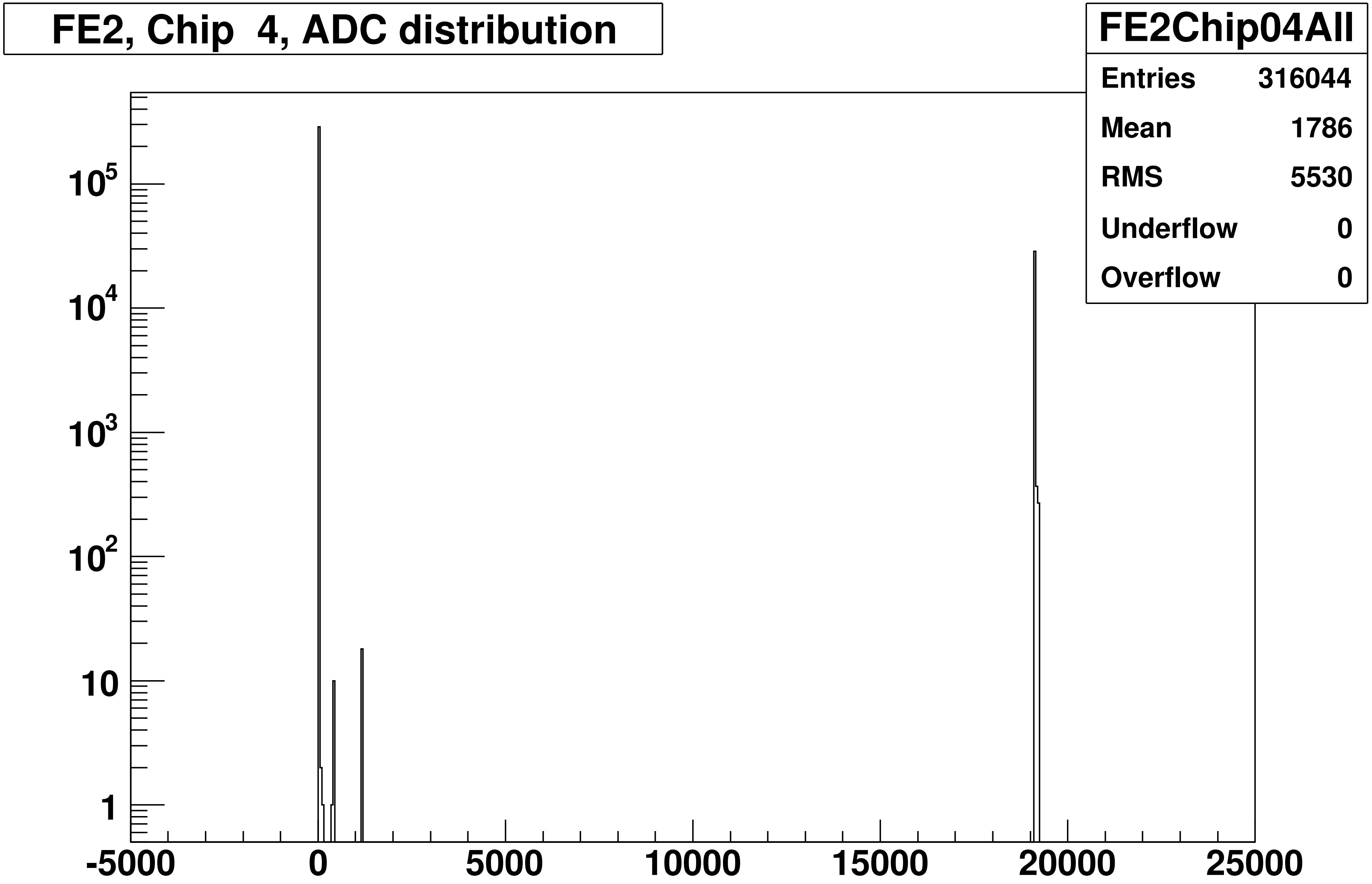
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE2, Chip 4, ADC distribution
FE2Chip04All
Entries 316044
Mean 1786
RMS 5530
Underflow 0
Overflow 0
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10^4
10^3
10^2
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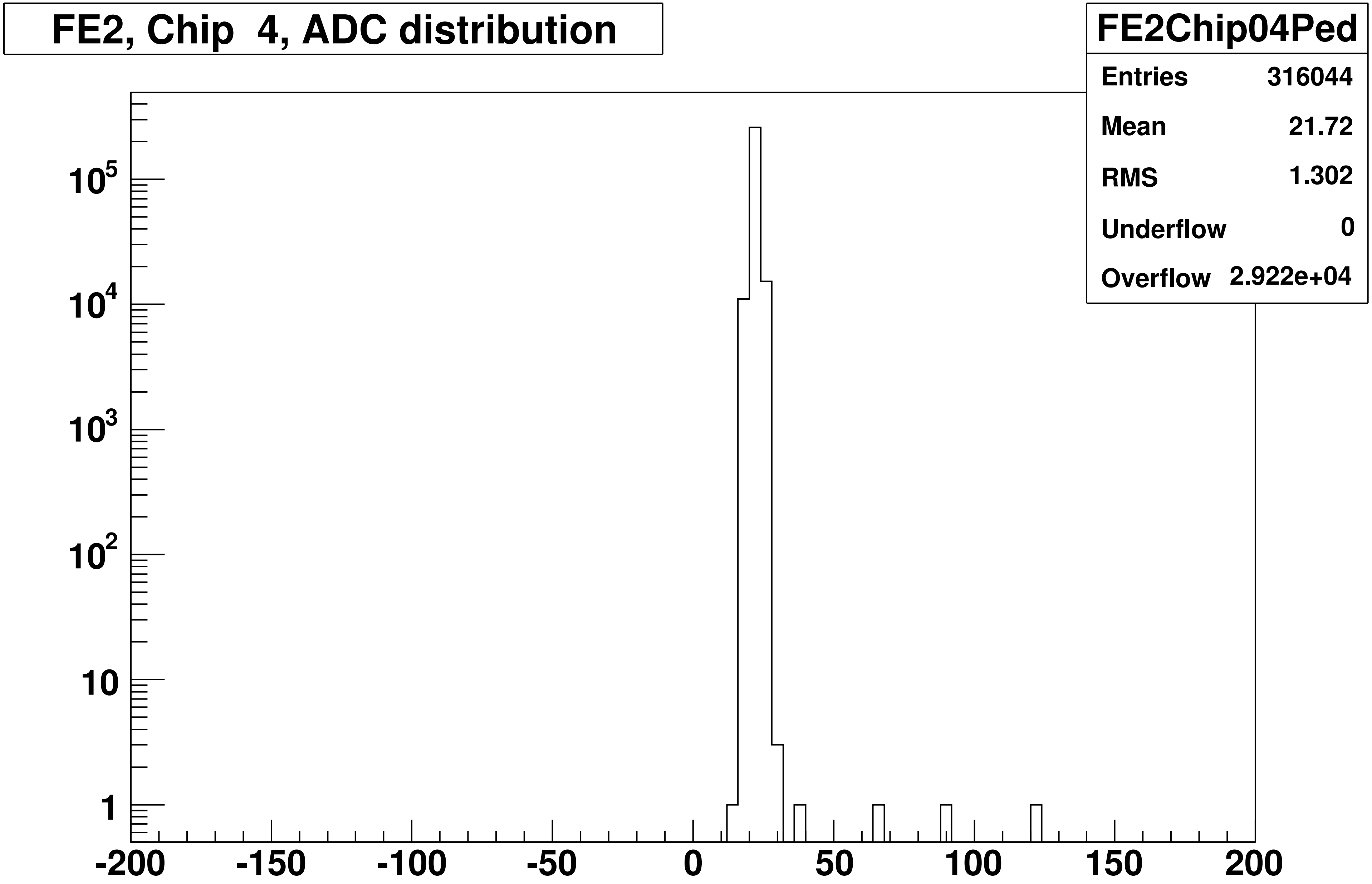
FE2, Chip 4, ADC distribution
FE2Chip04Ped
Entries 316044
Mean 21.72
RMS 1.302
Underflow 0
Overflow 2.922e+04
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10^2
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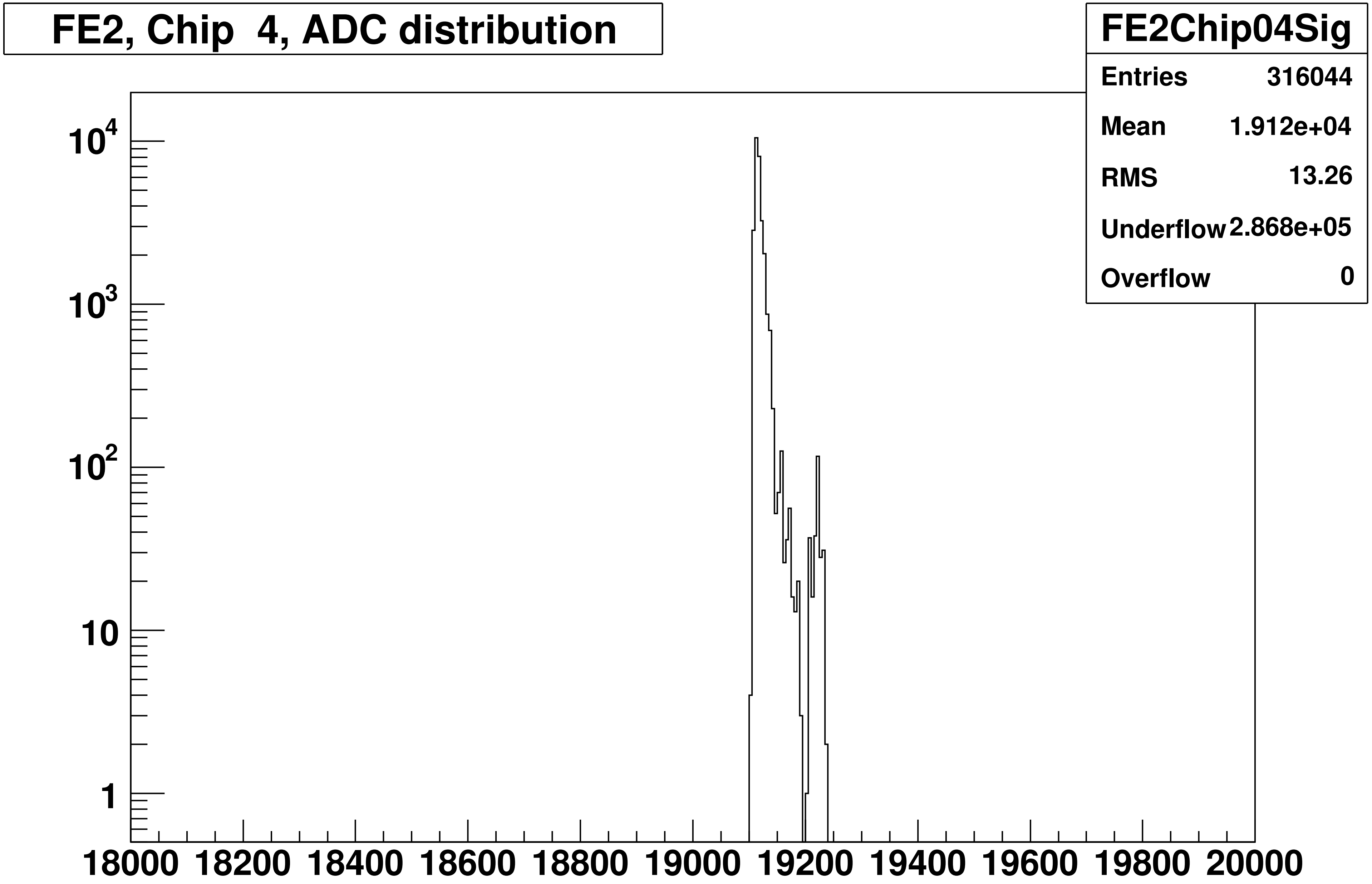

FE2, Chip 4, ADC distribution
FE2Chip04Sig
Entries 316044
Mean 1.912e+04
RMS 13.26
Underflow 2.868e+05
Overflow 0
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10^3
10^2
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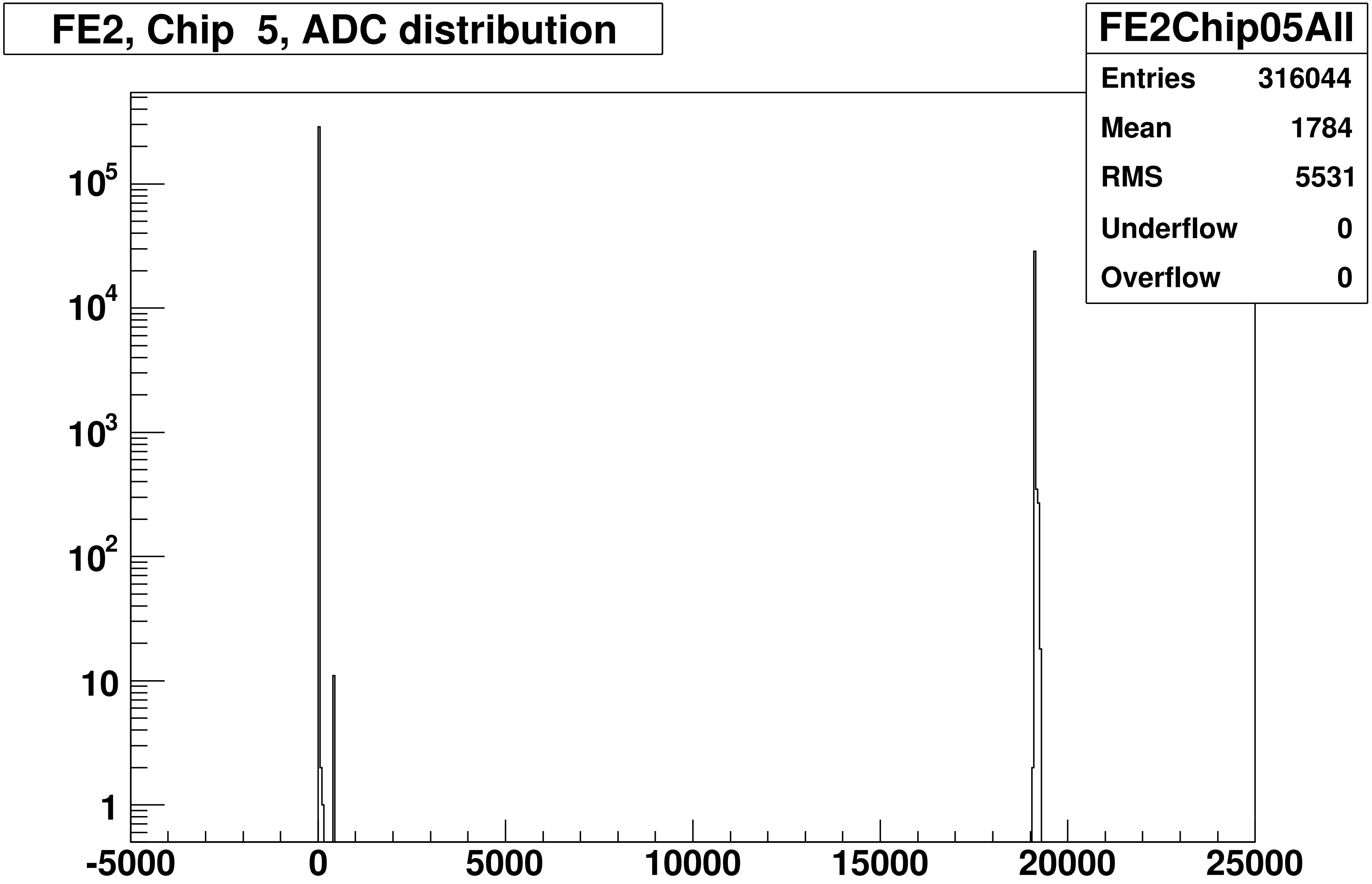
FE2, Chip 5, ADC distribution
FE2Chip05All
Entries 316044
Mean 1784
RMS 5531
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
1
-5000
0
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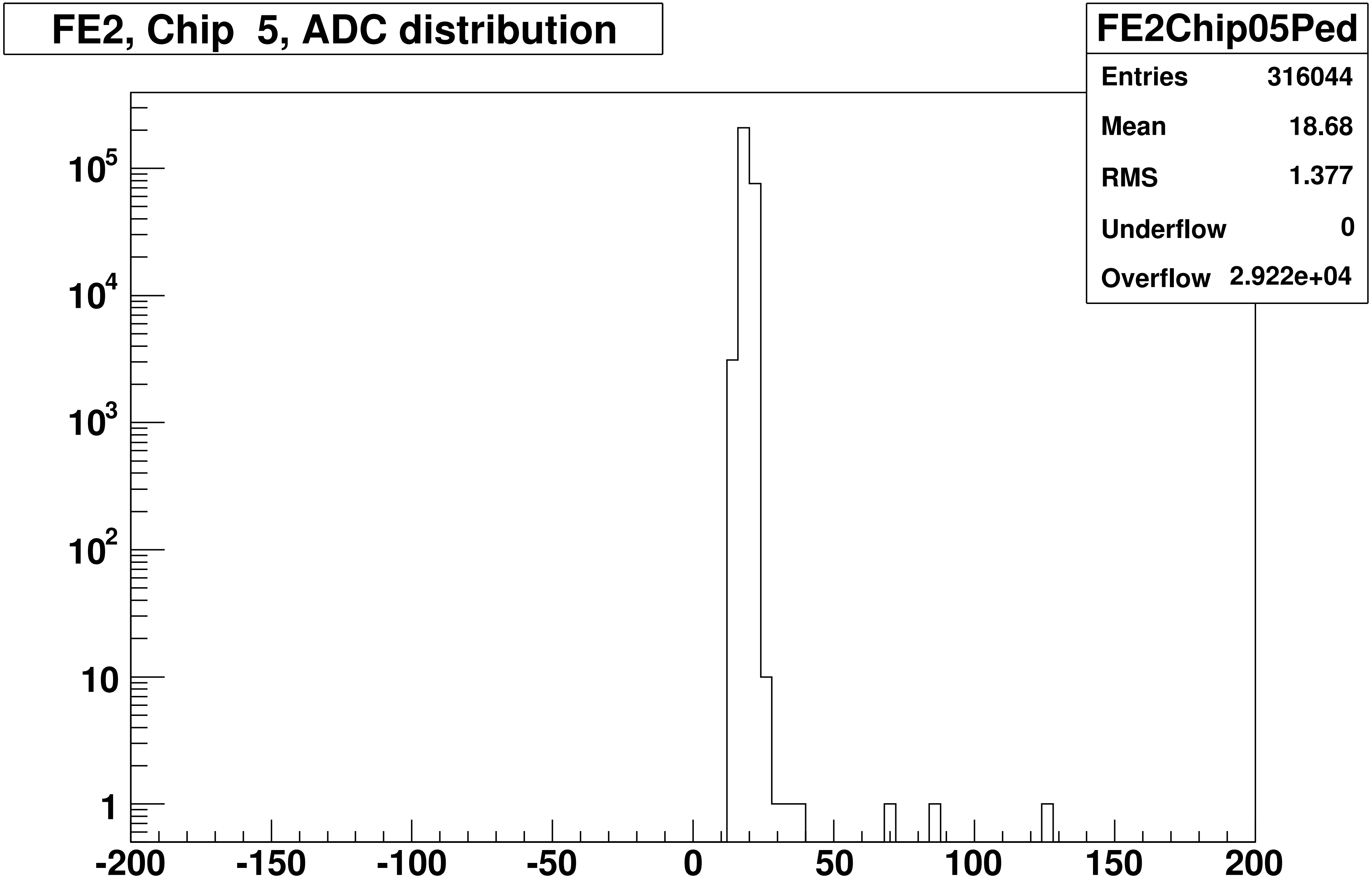
15000
20000
25000



FE2, Chip 5, ADC distribution
FE2Chip05Ped
Entries 316044
Mean 18.68
RMS 1.377
Underflow 0
Overflow 2.922e+04
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10^3
10^2
10
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150
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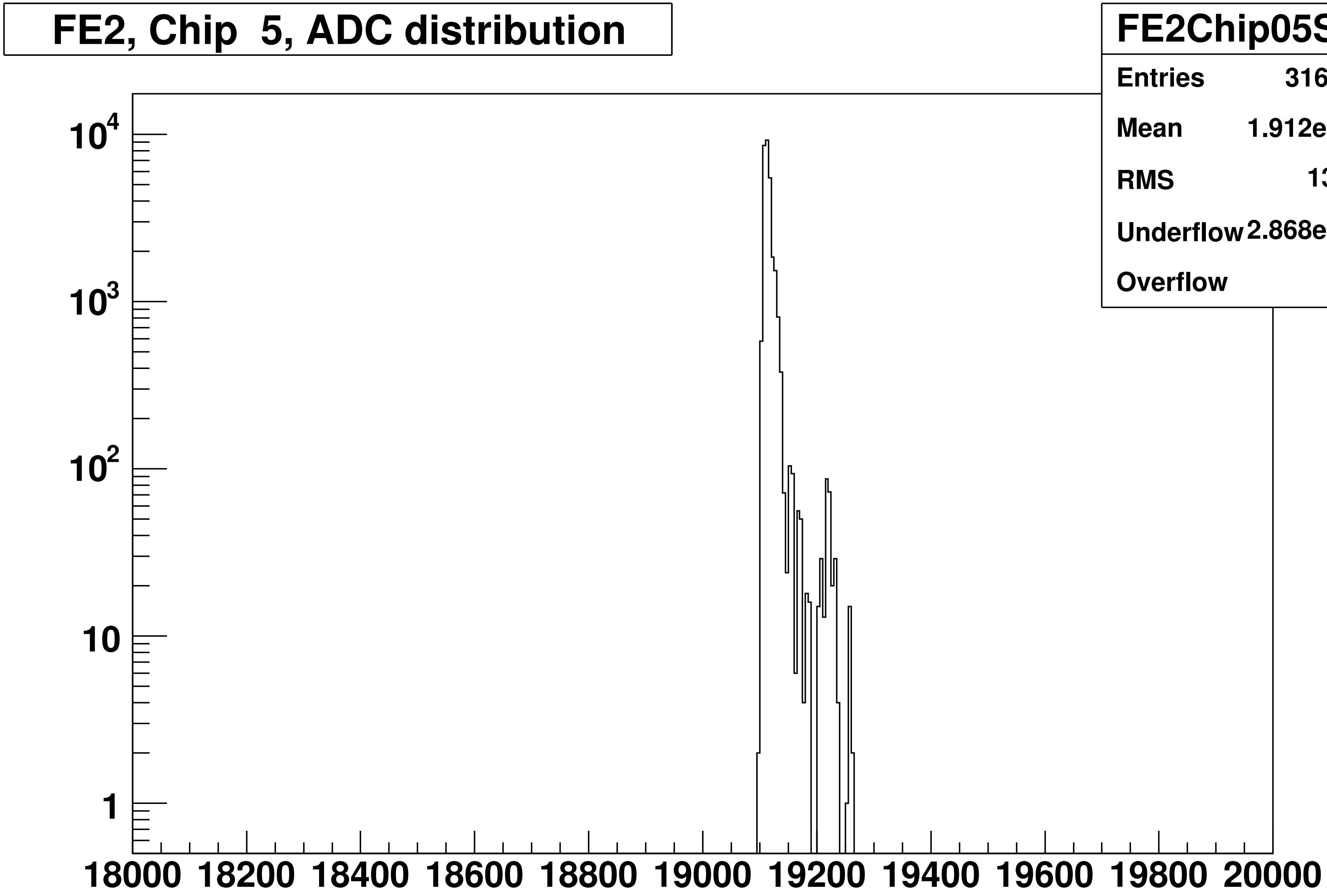
FE2, Chip 5, ADC distribution
FE2Chip05Sig
Entries 316044
Mean 1.912e+04
RMS 13.87
Underflow 2.868e+05
Overflow 0
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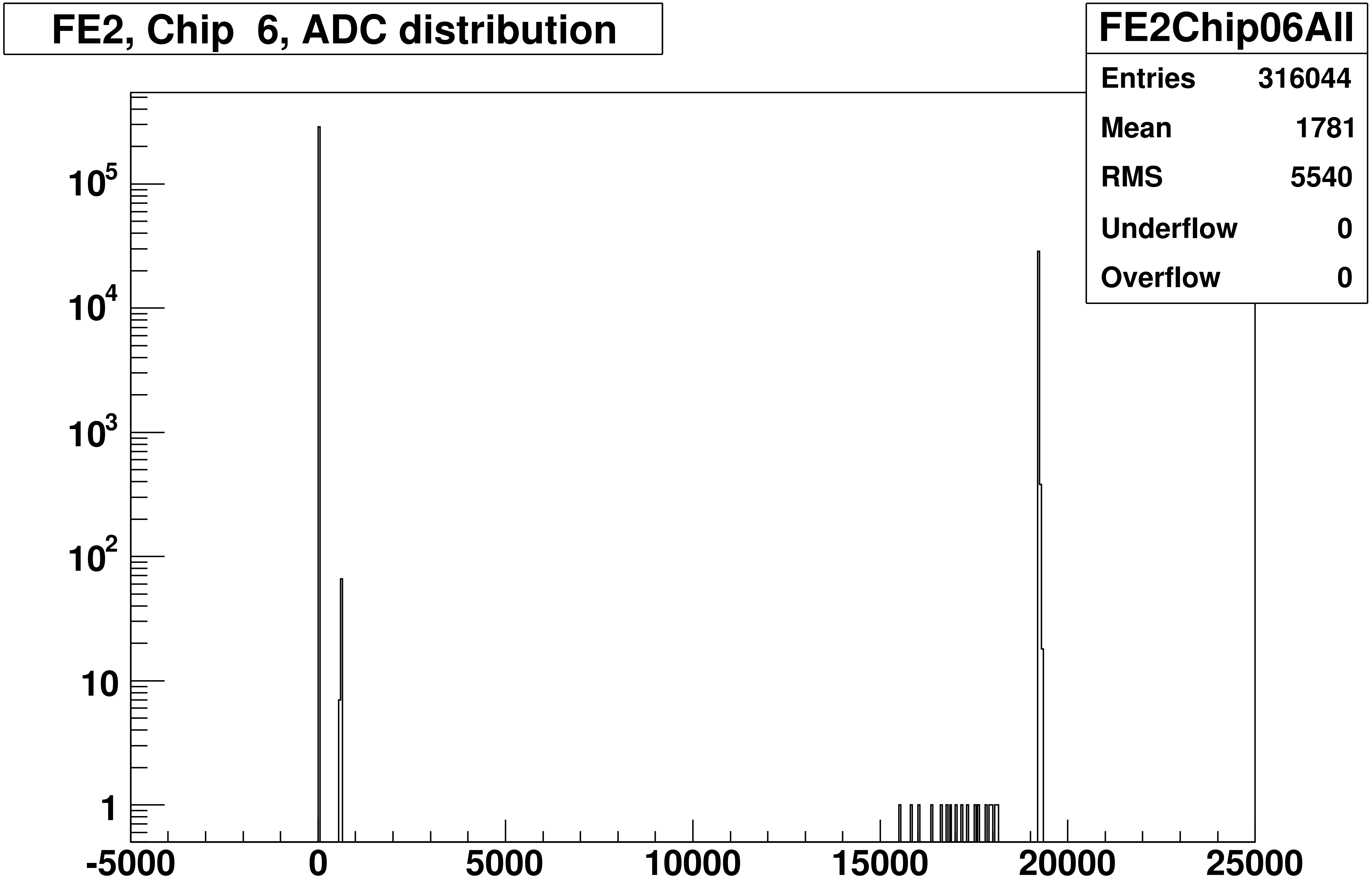
FE2, Chip 6, ADC distribution
FE2Chip06All
Entries 316044
Mean 1781
RMS 5540
Underflow 0
Overflow 0
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10^4
10^3
10^2
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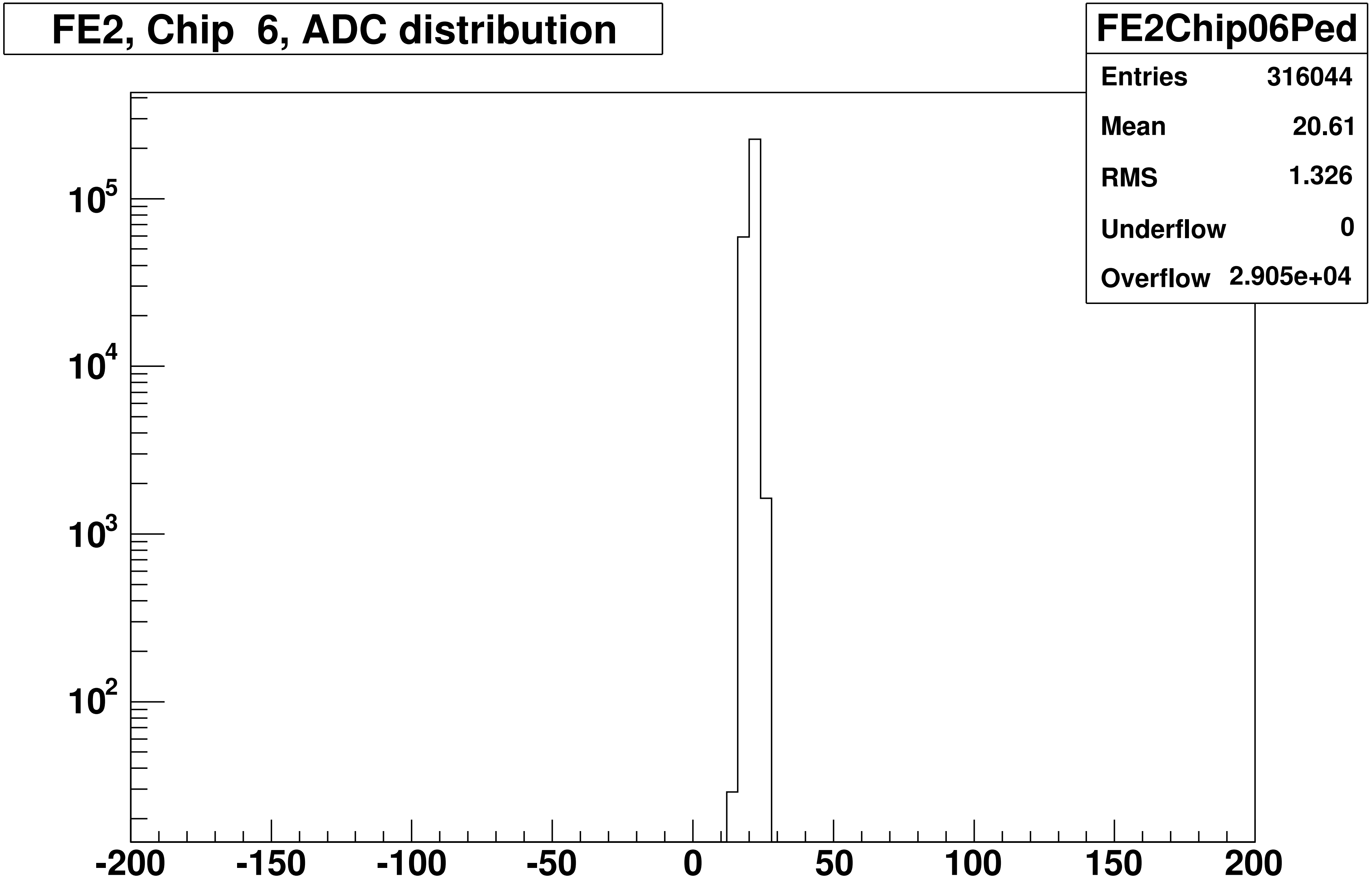
25000


FE2, Chip 6, ADC distribution
FE2Chip06Ped
Entries 316044
Mean 20.61
RMS 1.326
Underflow 0
Overflow 2.905e+04
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10^4
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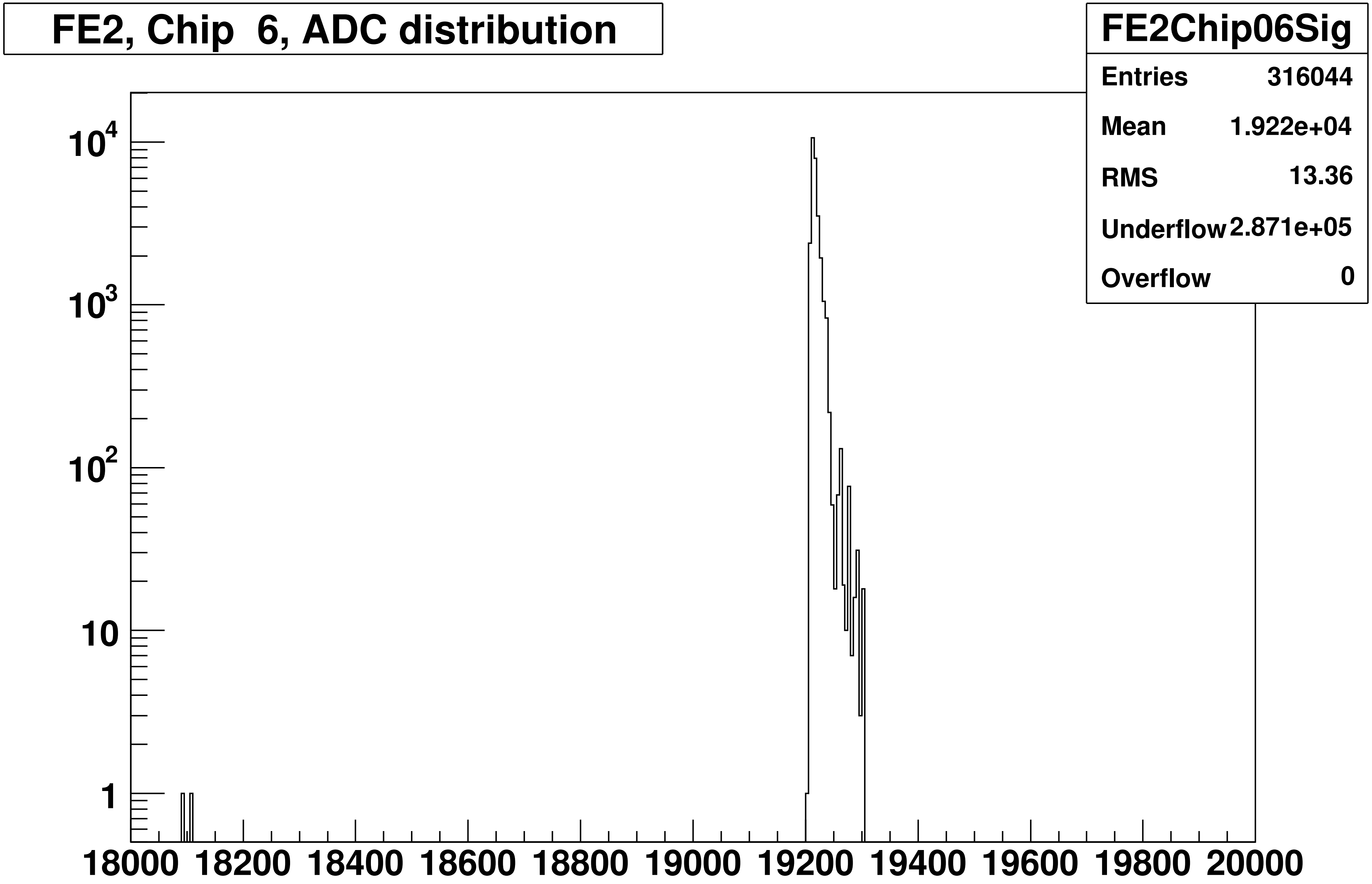

FE2, Chip 6, ADC distribution
FE2Chip06Sig
Entries 316044
Mean 1.922e+04
RMS 13.36
Underflow 2.871e+05
Overflow 0
10^4
10^3
10^2
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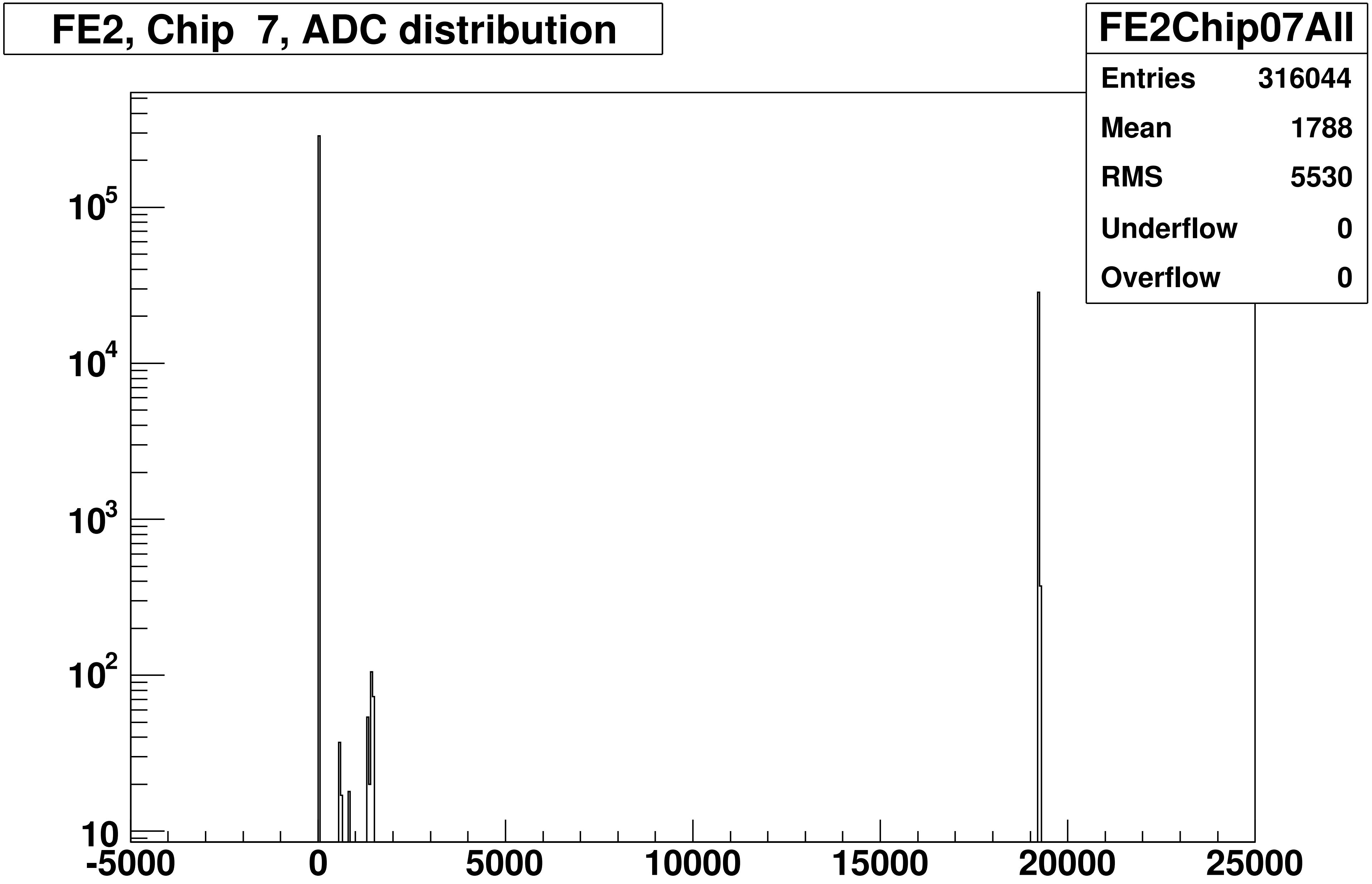
FE2, Chip 7, ADC distribution
FE2Chip07All
Entries 316044
Mean 1788
RMS 5530
Underflow 0
Overflow 0
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10^4
10^3
10^2
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15000
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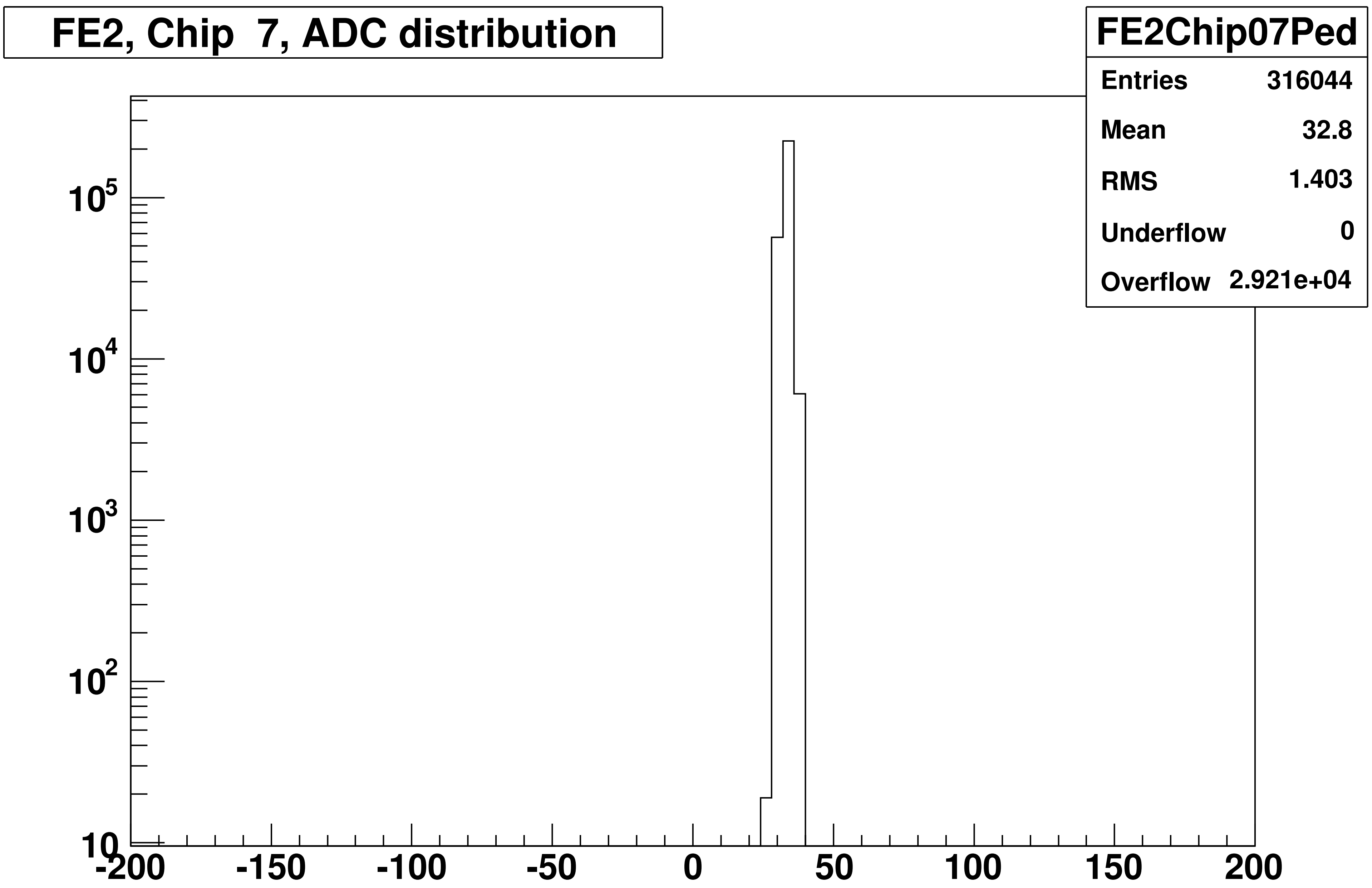
FE2, Chip 7, ADC distribution
FE2Chip07Ped
Entries 316044
Mean 32.8
RMS 1.403
Underflow 0
Overflow 2.921e+04
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10^3
10^4
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150
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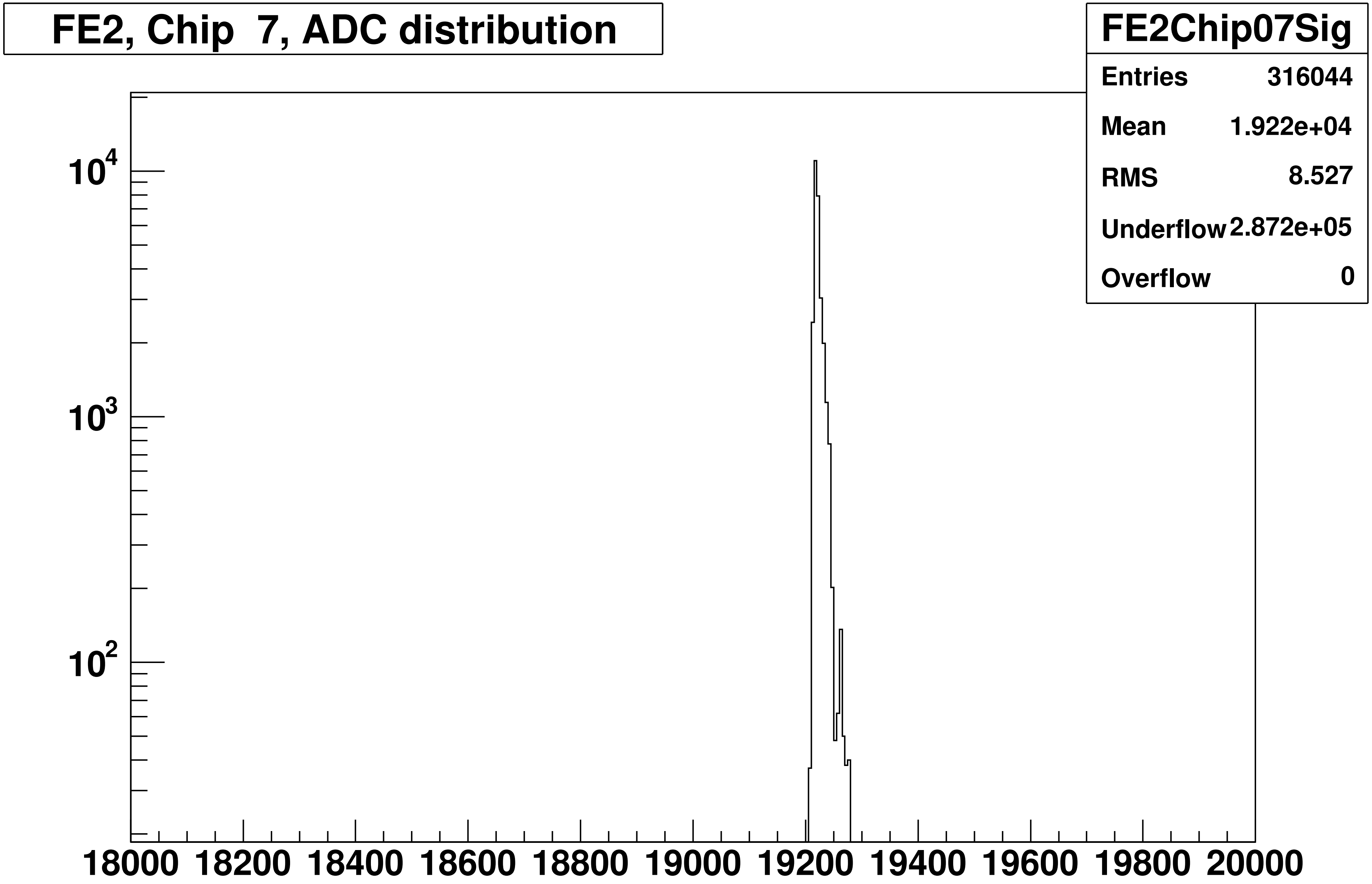
FE2, Chip 7, ADC distribution
FE2Chip07Sig
Entries 316044
Mean 1.922e+04
RMS 8.527
Underflow 2.872e+05
Overflow 0
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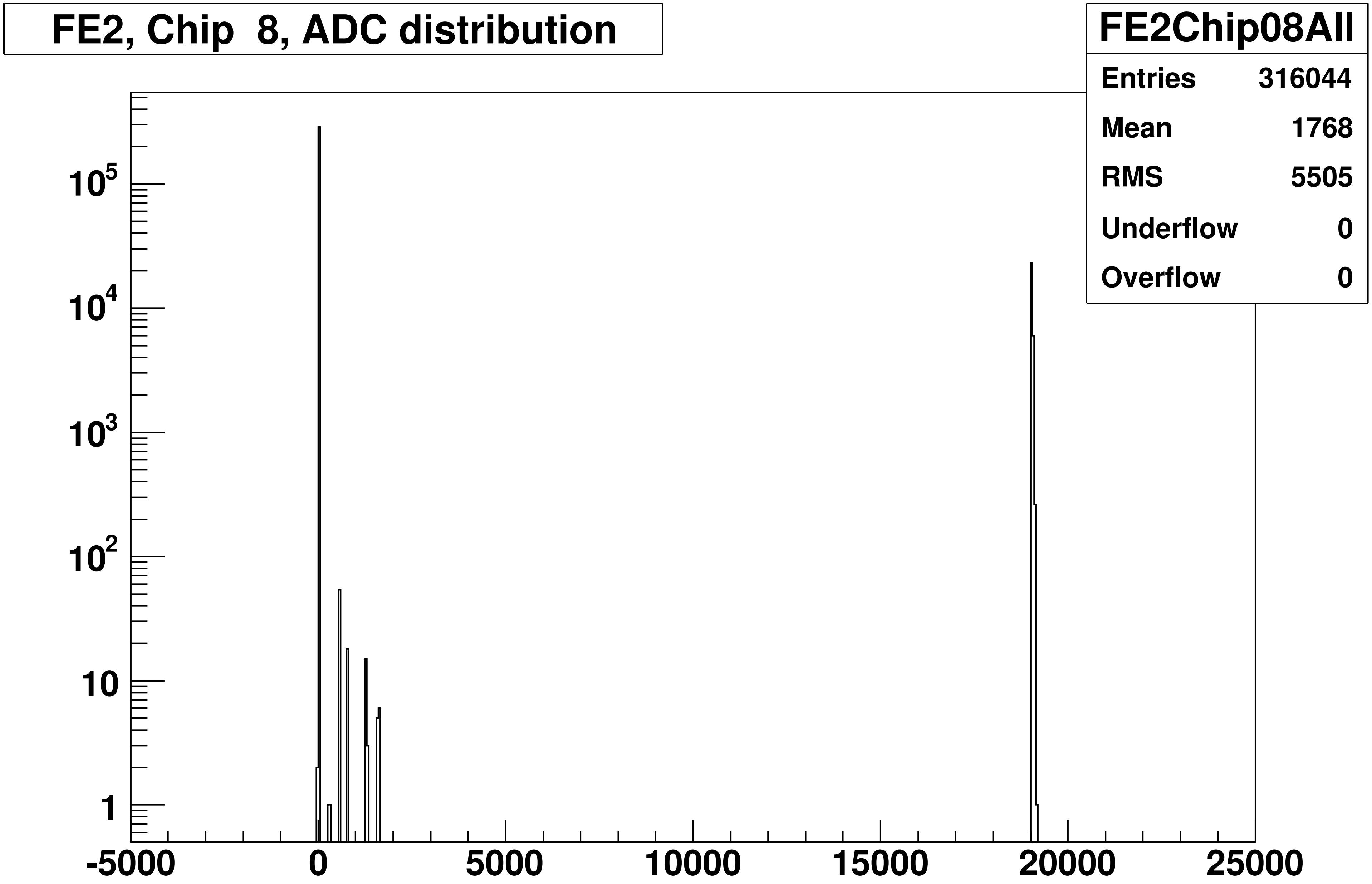
10^3
10^2
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE2, Chip 8, ADC distribution
FE2Chip08All
Entries 316044
Mean 1768
RMS 5505
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
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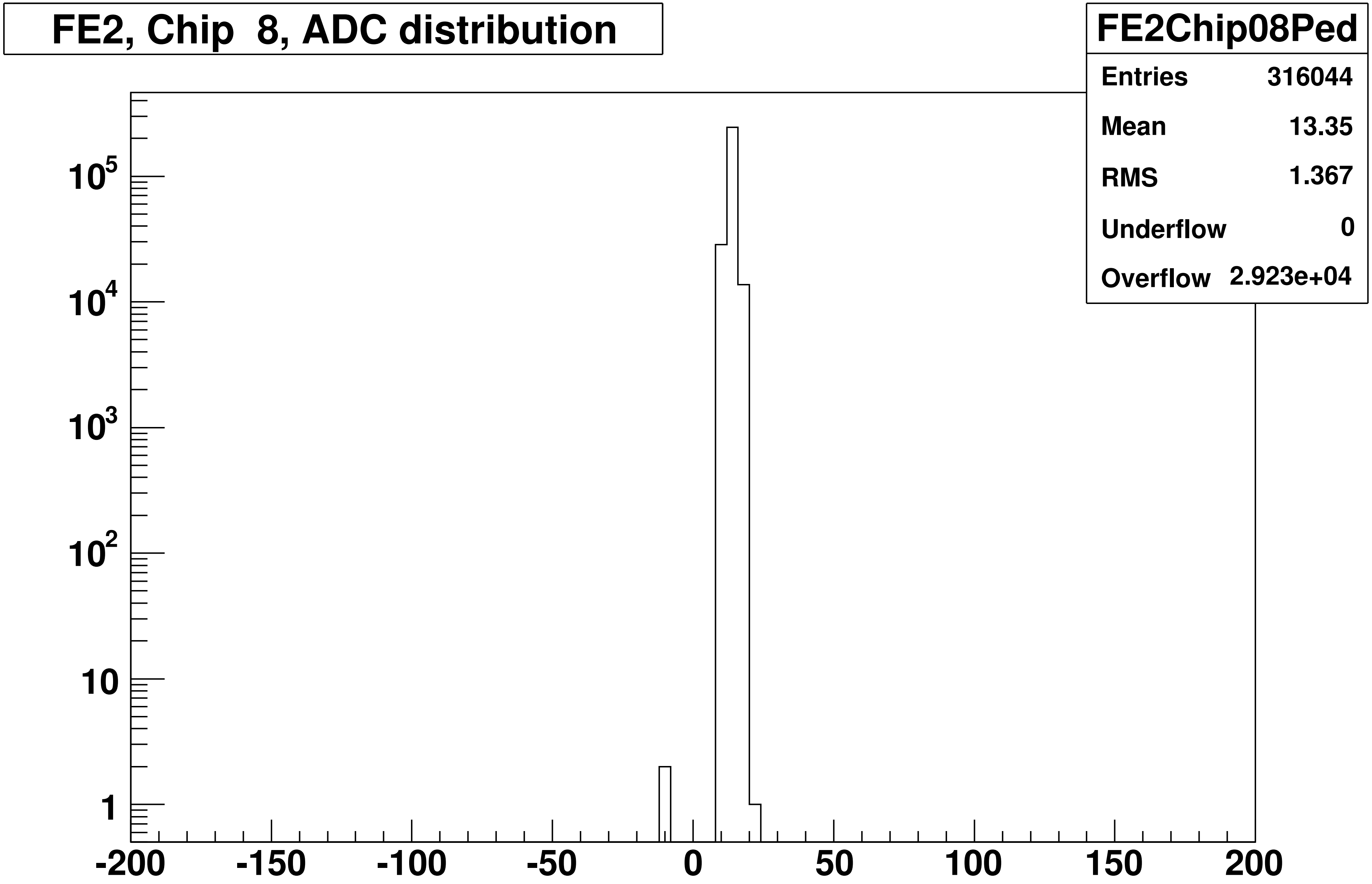
FE2, Chip 8, ADC distribution
FE2Chip08Ped
Entries 316044
Mean 13.35
RMS 1.367
Underflow 0
Overflow 2.923e+04
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10^3
10^2
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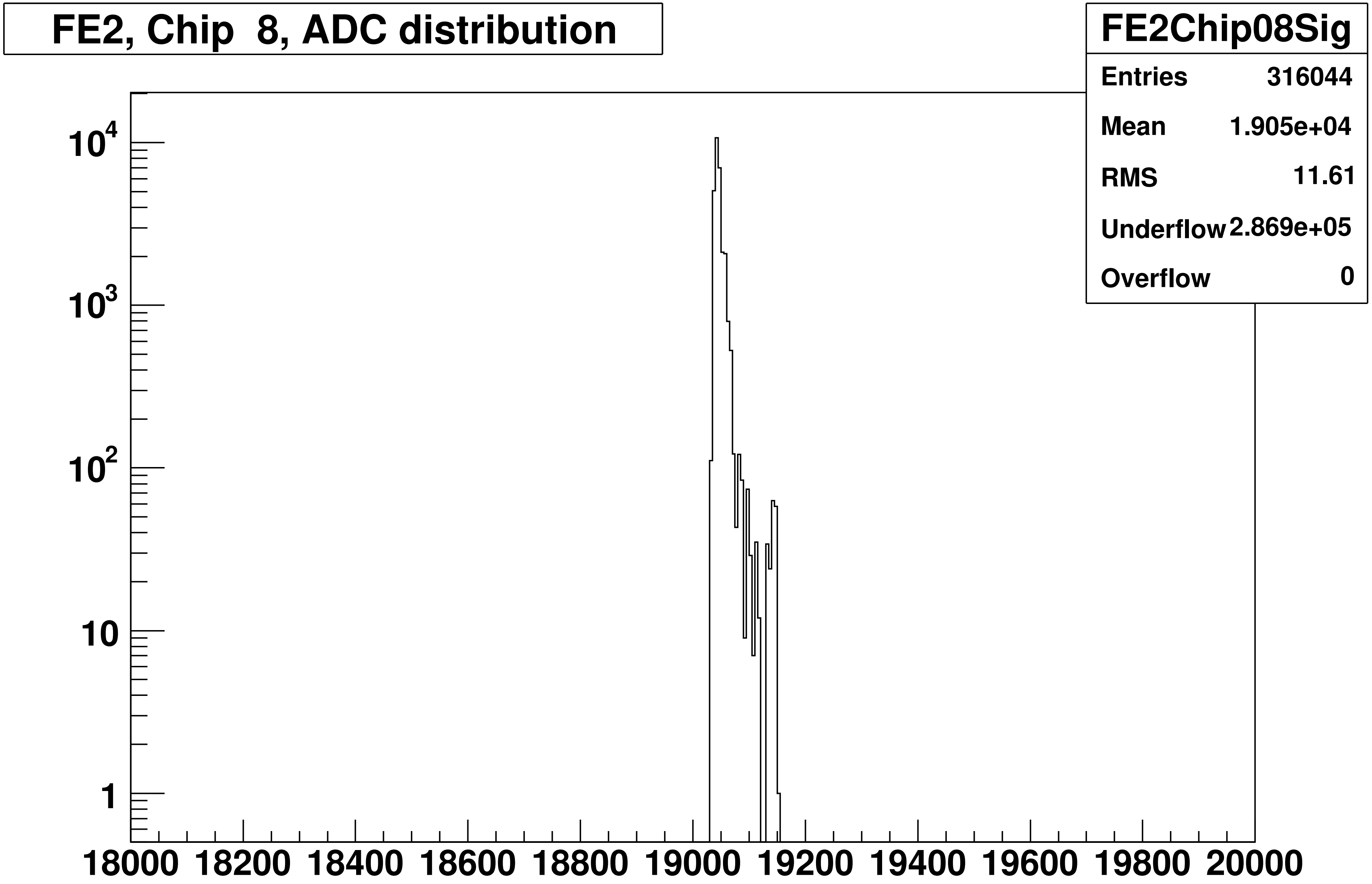
FE2, Chip 8, ADC distribution
FE2Chip08Sig
Entries 316044
Mean 1.905e+04
RMS 11.61
Underflow 2.869e+05
Overflow 0
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10^3
10^2
10
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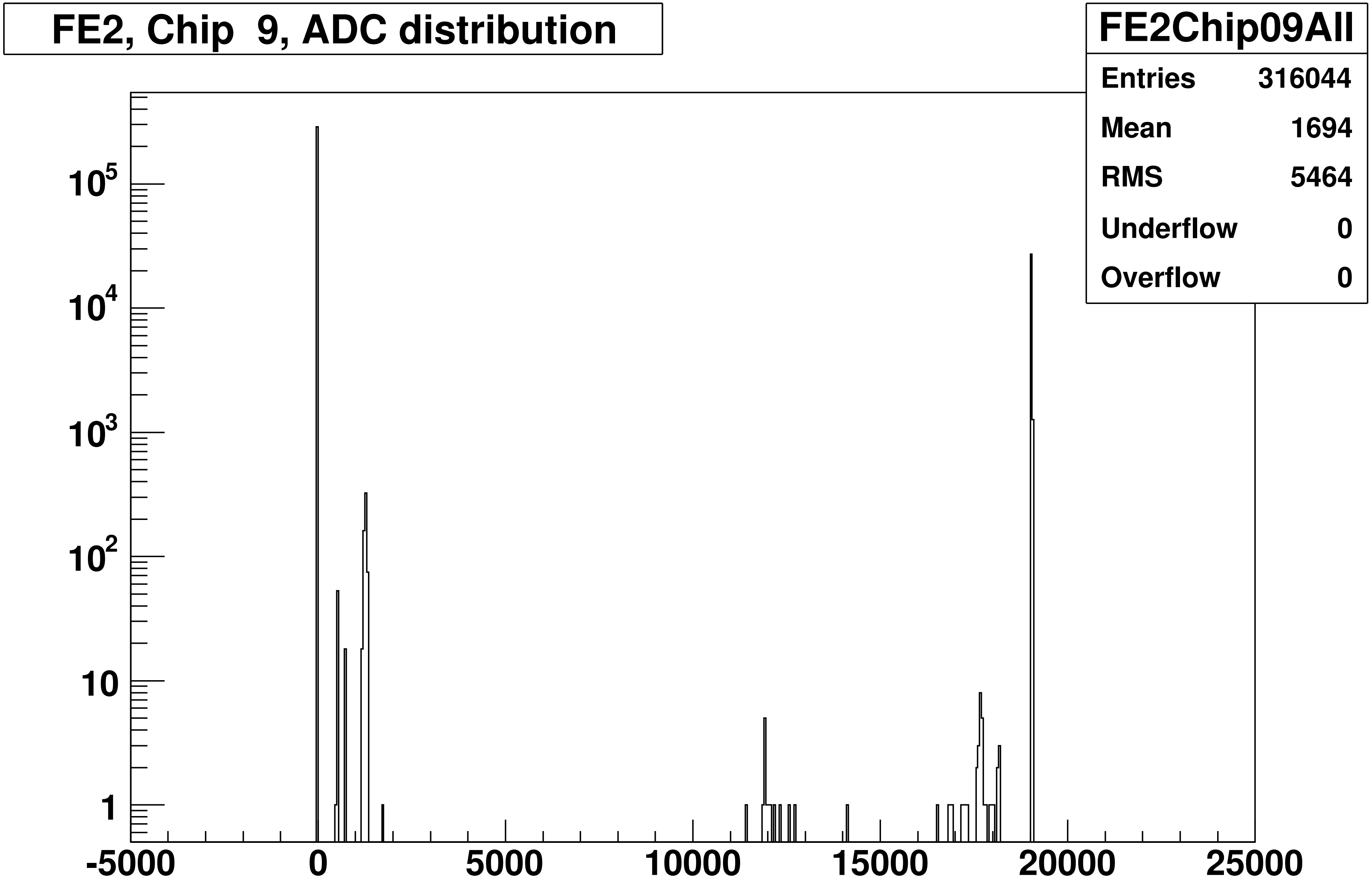
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE2, Chip 9, ADC distribution
FE2Chip09All
Entries 316044
Mean 1694
RMS 5464
Underflow 0
Overflow 0
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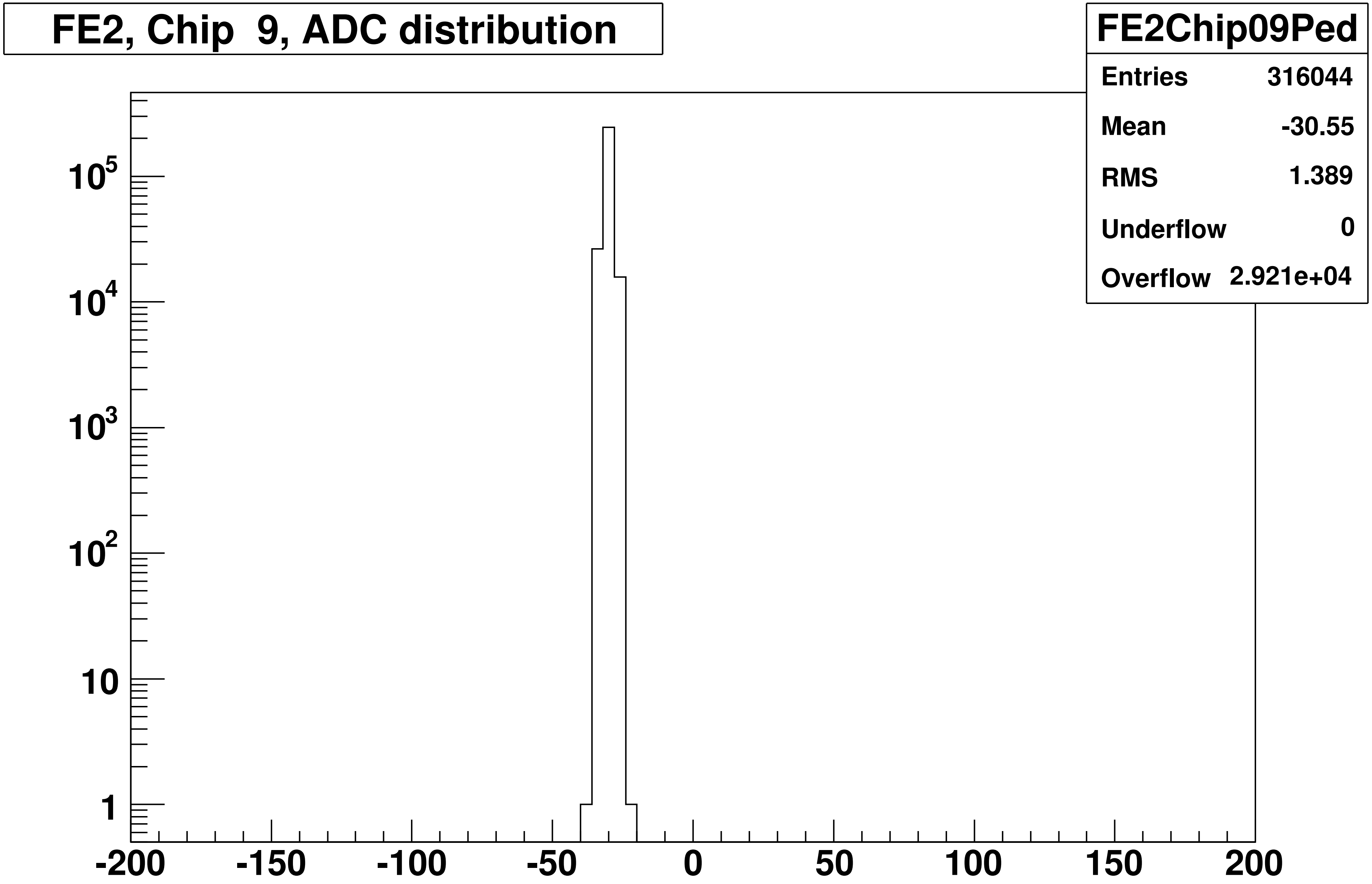
FE2, Chip 9, ADC distribution
FE2Chip09Ped
Entries 316044
Mean -30.55
RMS 1.389
Underflow 0
Overflow 2.921e+04
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10^3
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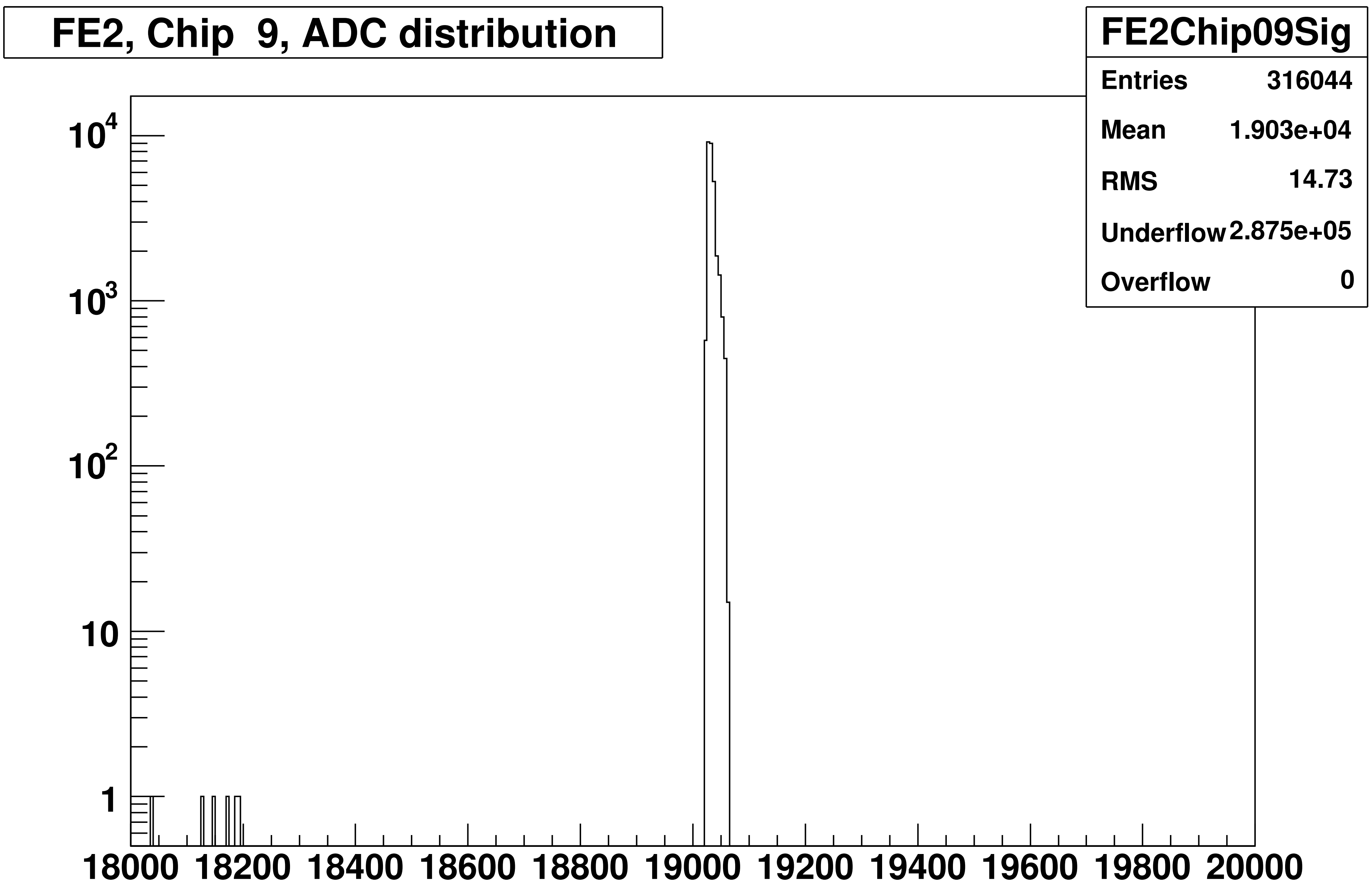
FE2, Chip 9, ADC distribution
FE2Chip09Sig
Entries 316044
Mean 1.903e+04
RMS 14.73
Underflow 2.875e+05
Overflow 0
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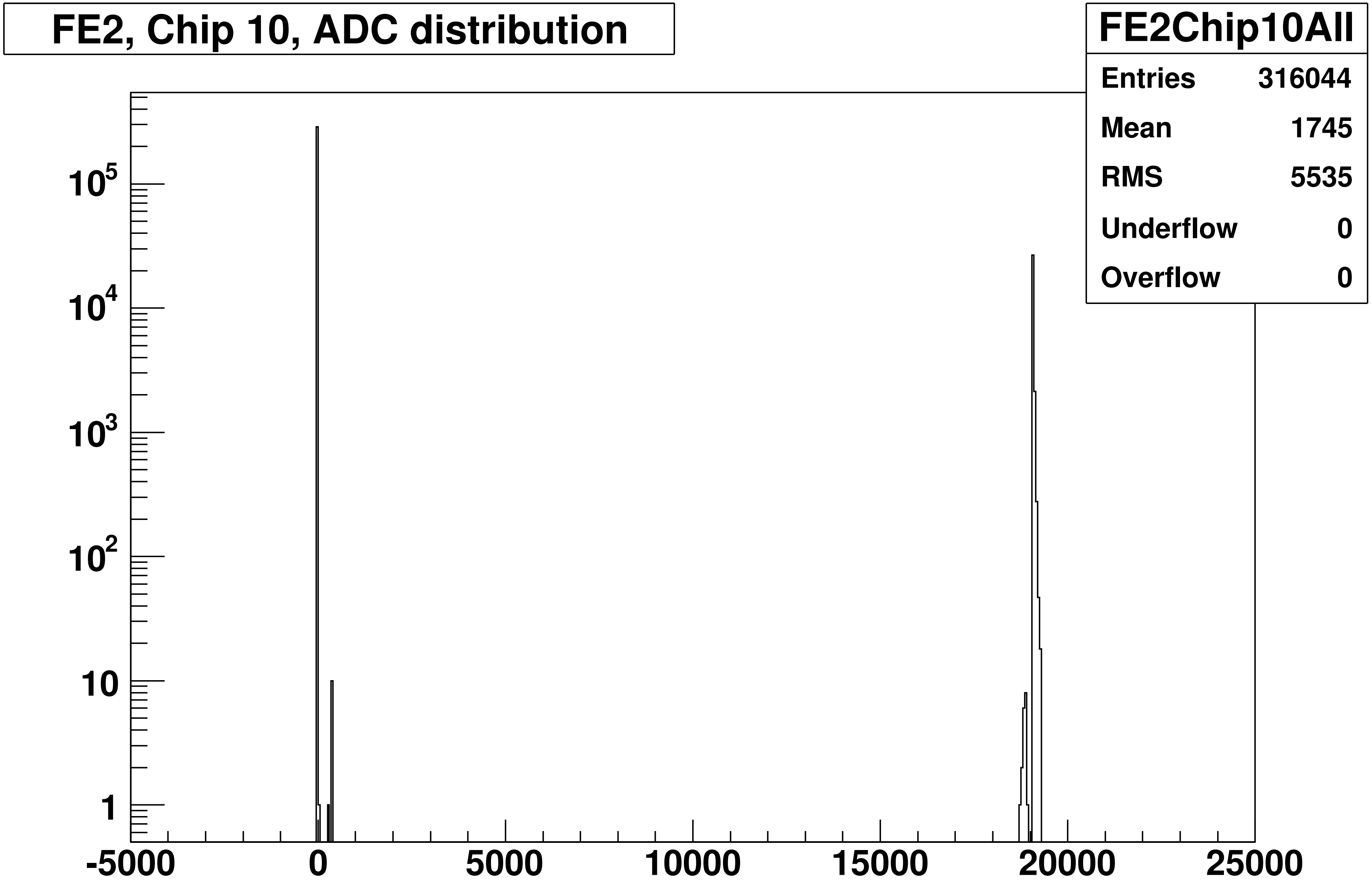
FE2, Chip 10, ADC distribution
FE2Chip10All
Entries 316044
Mean 1745
RMS 5535
Underflow 0
Overflow 0
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10^4
10^3
10^2
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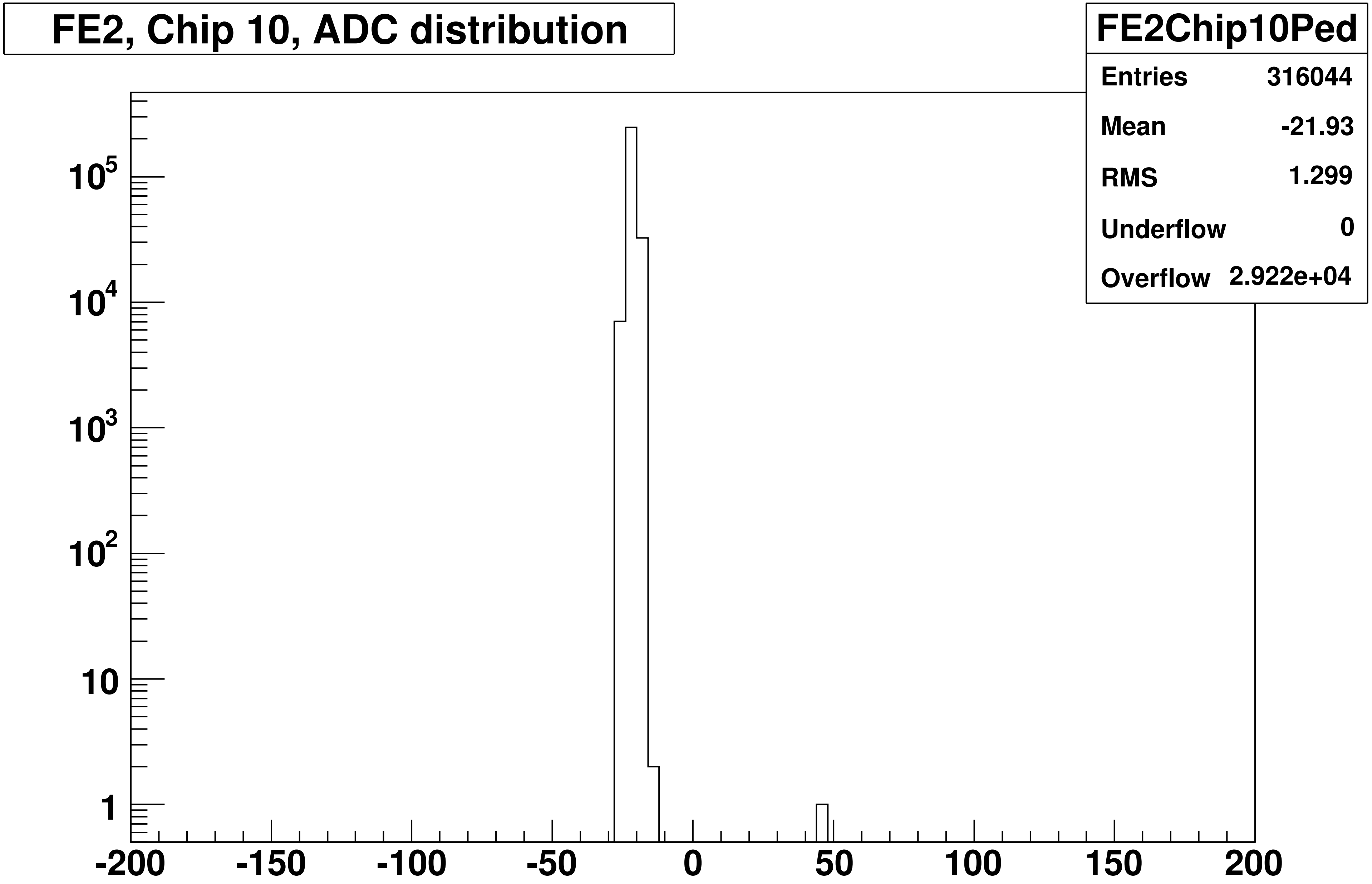
FE2, Chip 10, ADC distribution
FE2Chip10Ped
Entries 316044
Mean -21.93
RMS 1.299
Underflow 0
Overflow 2.922e+04
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10^3
10^2
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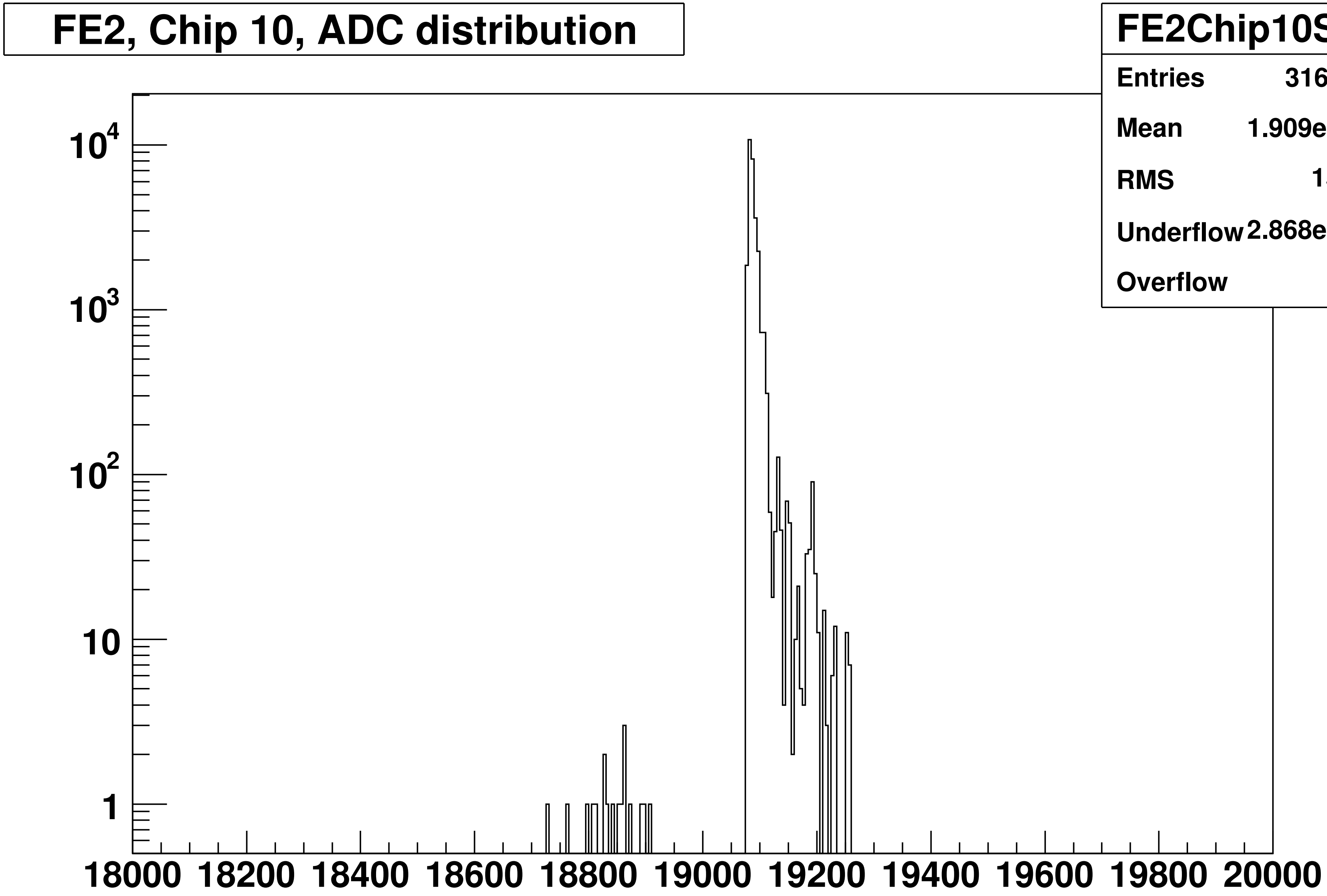
FE2, Chip 10, ADC distribution
FE2Chip10Sig
Entries 316044
Mean 1.909e+04
RMS 15.41
Underflow 2.868e+05
Overflow 0
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10^3
10^2
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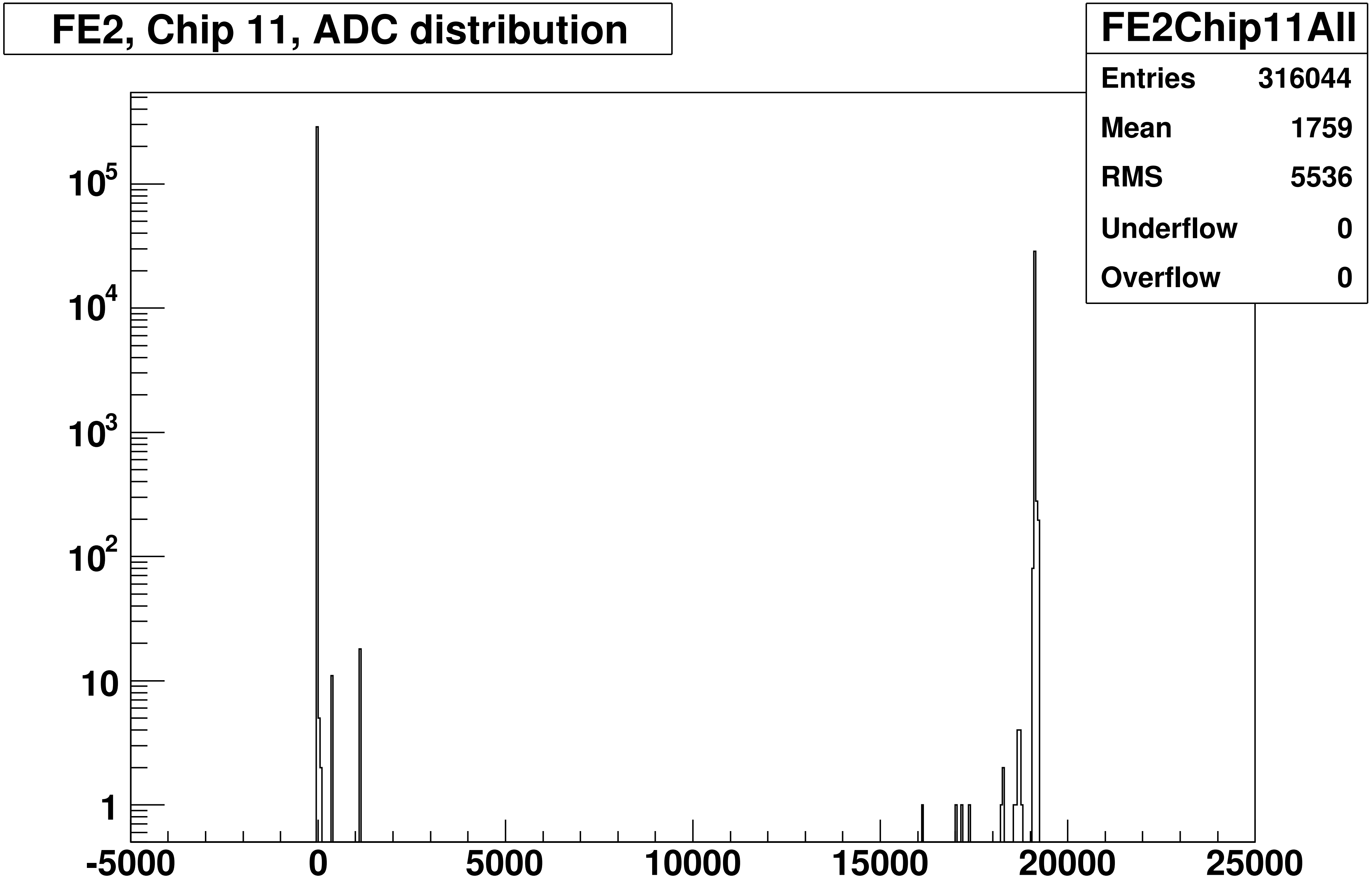
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE2, Chip 11, ADC distribution
FE2Chip11All
Entries 316044
Mean 1759
RMS 5536
Underflow 0
Overflow 0
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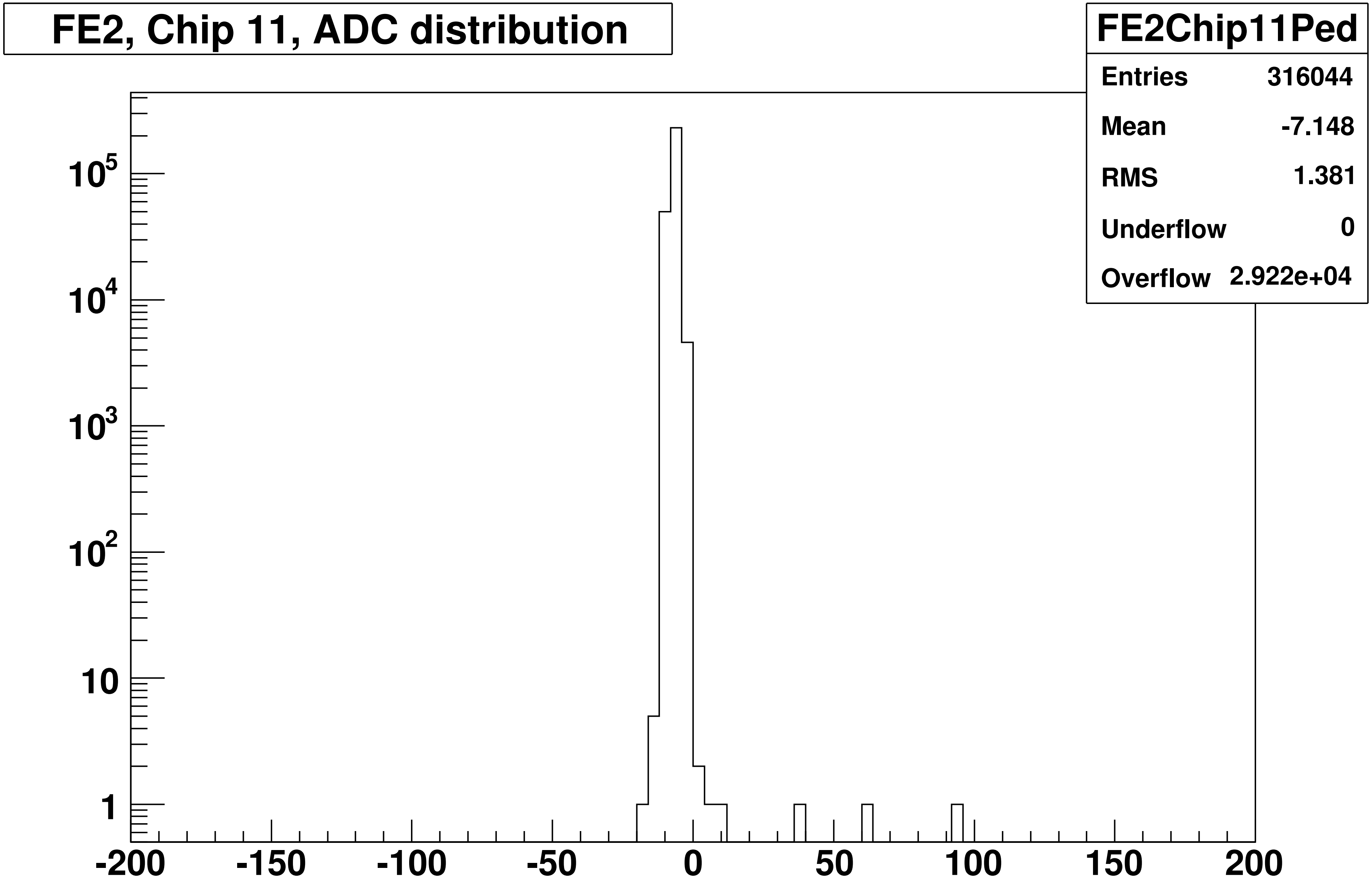
FE2, Chip 11, ADC distribution
FE2Chip11Ped
Entries 316044
Mean -7.148
RMS 1.381
Underflow 0
Overflow 2.922e+04
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10^3
10^2
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150
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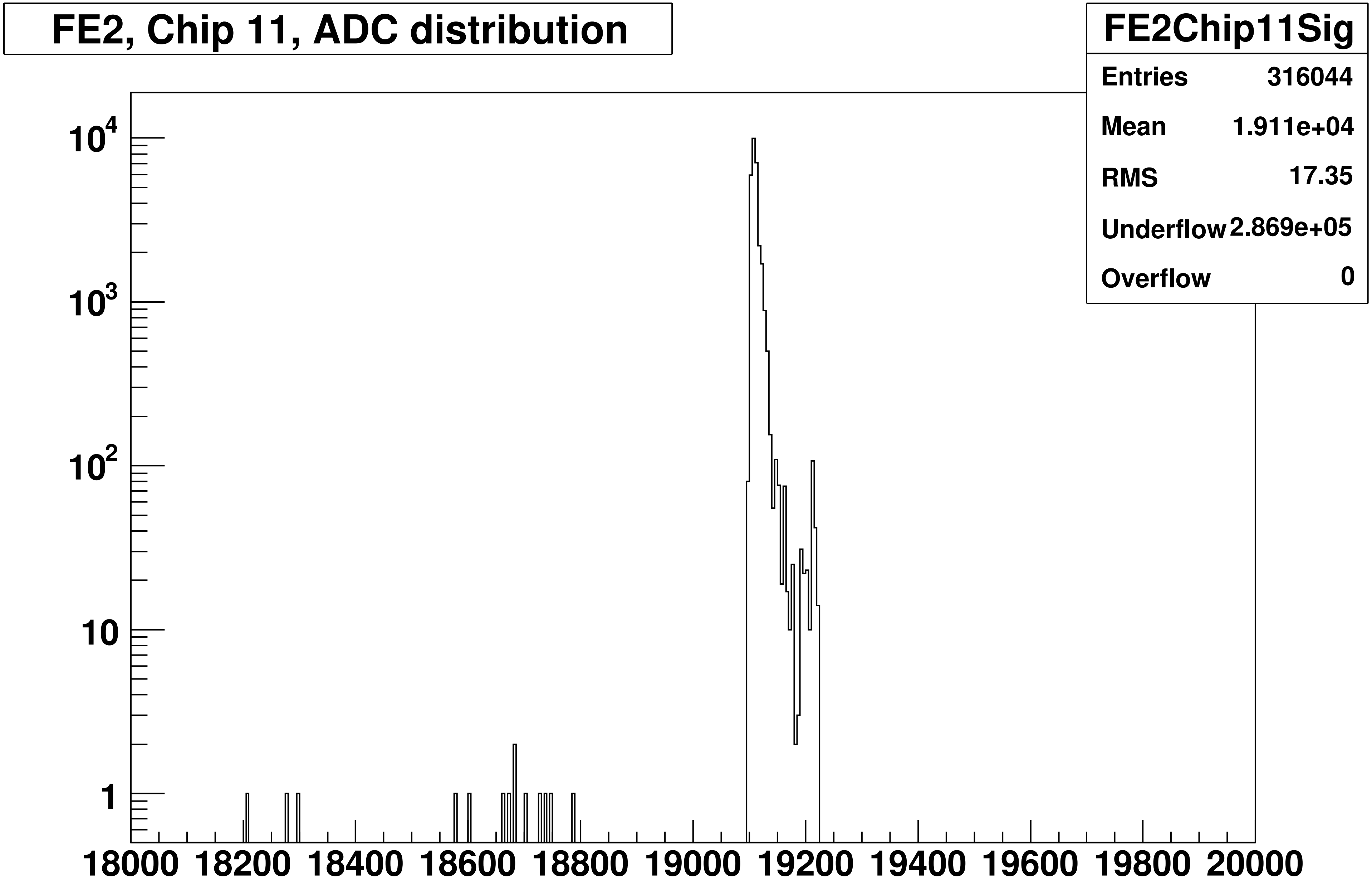
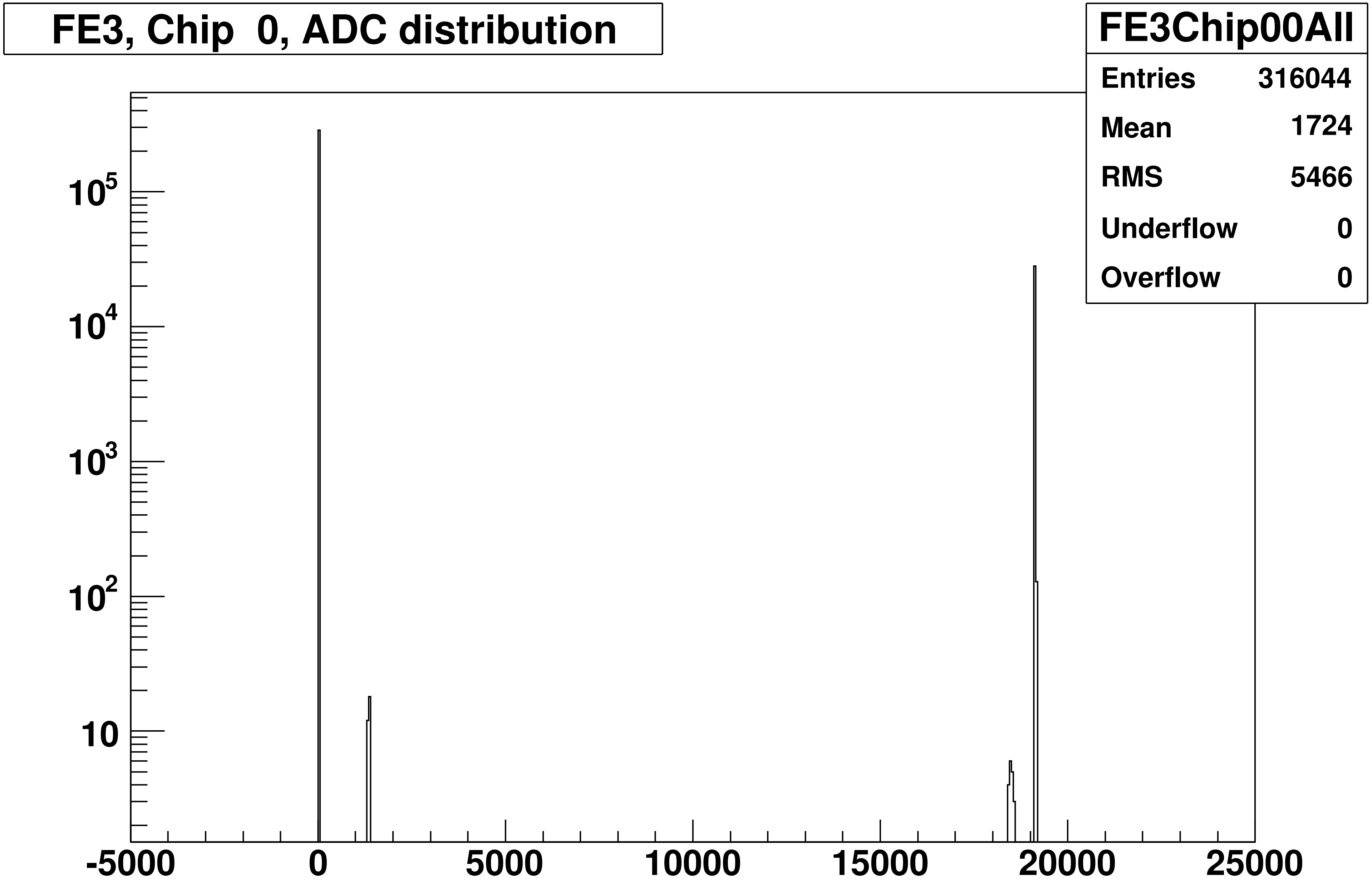

FE2, Chip 11, ADC distribution
FE2Chip11Sig
Entries 316044
Mean 1.911e+04
RMS 17.35
Underflow 2.869e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE3, Chip 0, ADC distribution
FE3Chip00All
Entries 316044
Mean 1724
RMS 5466
Underflow 0
Overflow 0
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10^4
10^3
10^2
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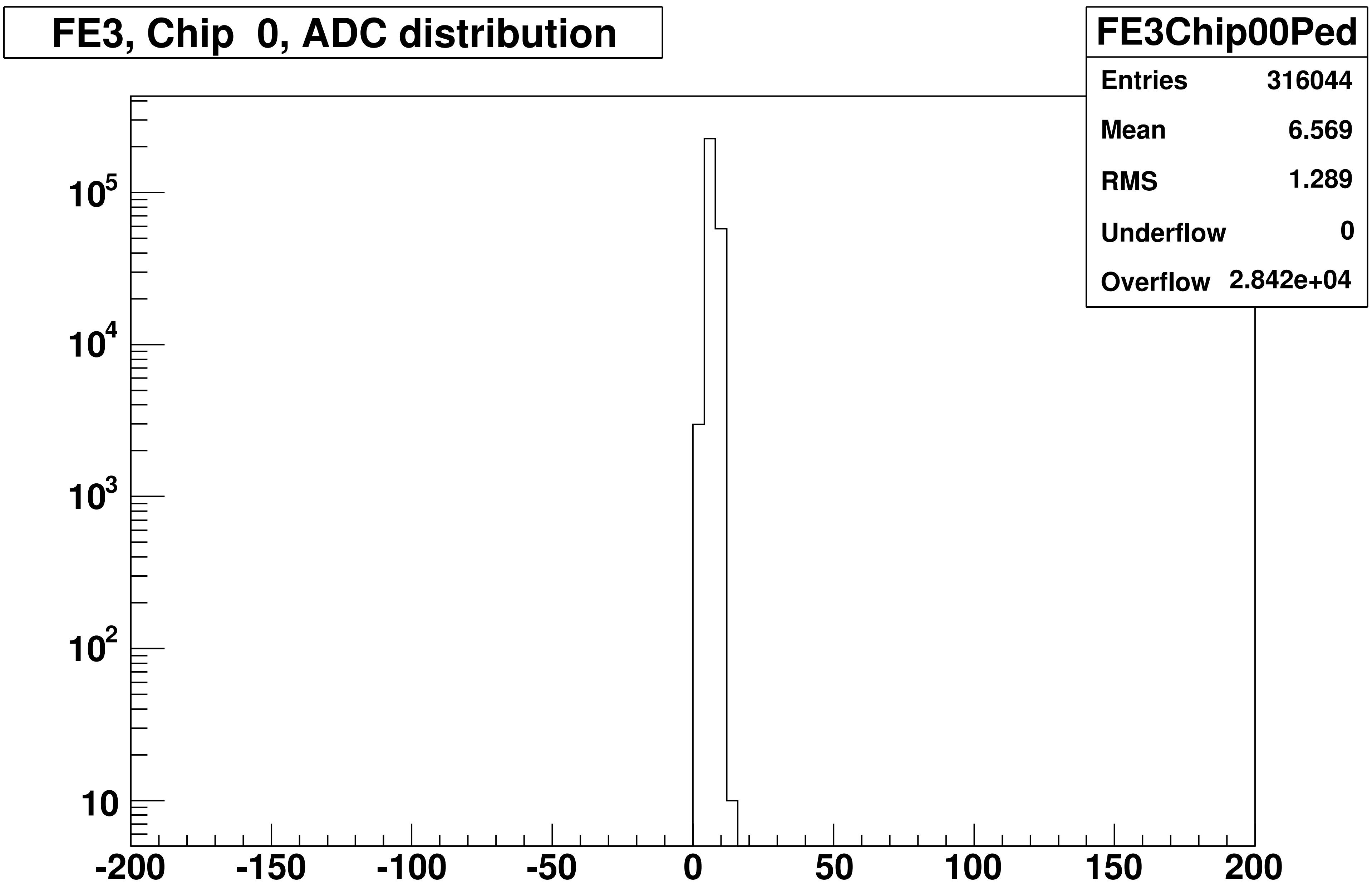
20000
25000


FE3, Chip 0, ADC distribution
FE3Chip00Ped
Entries 316044
Mean 6.569
RMS 1.289
Underflow 0
Overflow 2.842e+04
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10^4
10^3
10^2
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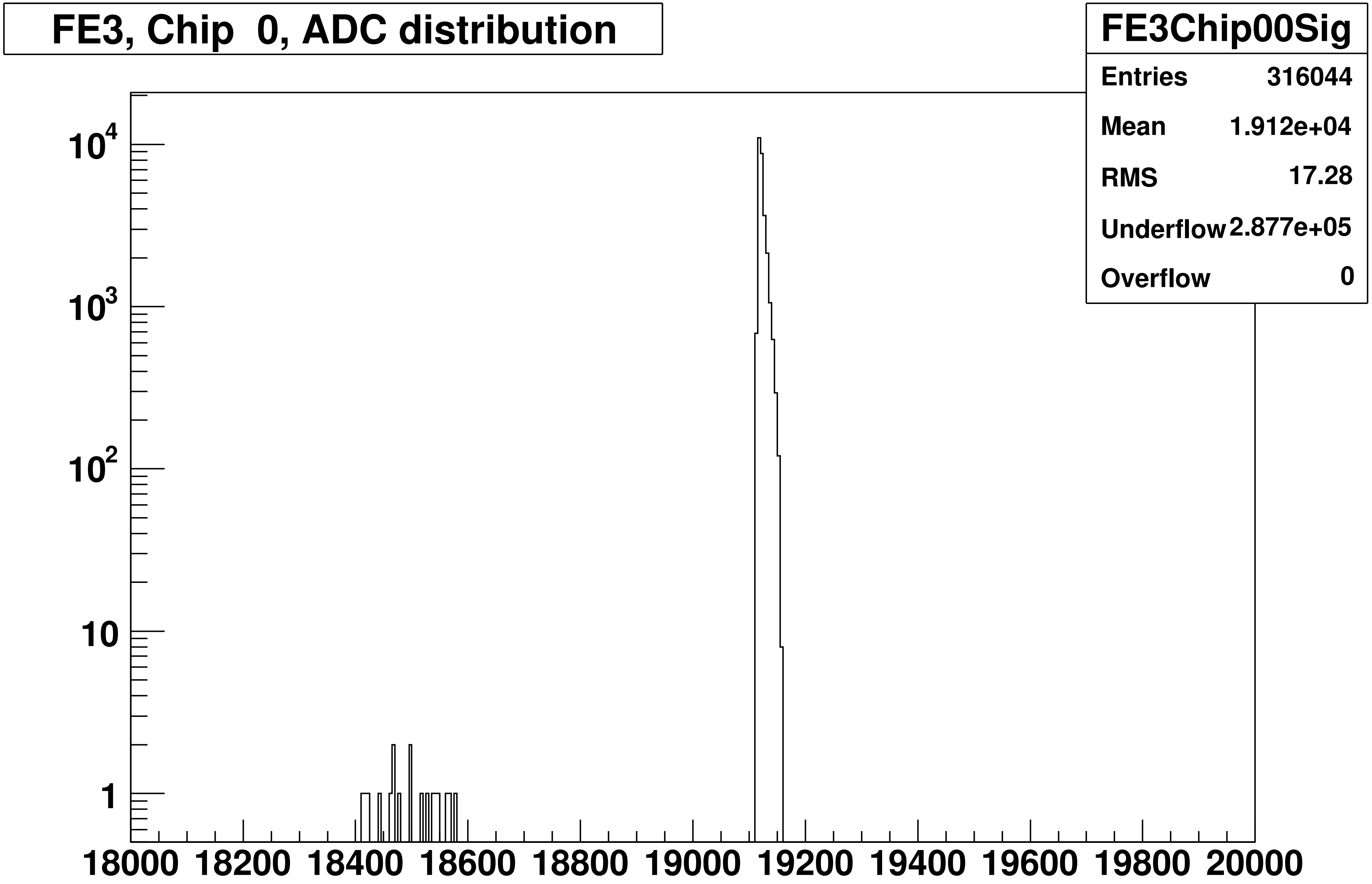
150
200


FE3, Chip 0, ADC distribution
FE3Chip00Sig
Entries 316044
Mean 1.912e+04
RMS 17.28
Underflow 2.877e+05
Overflow 0
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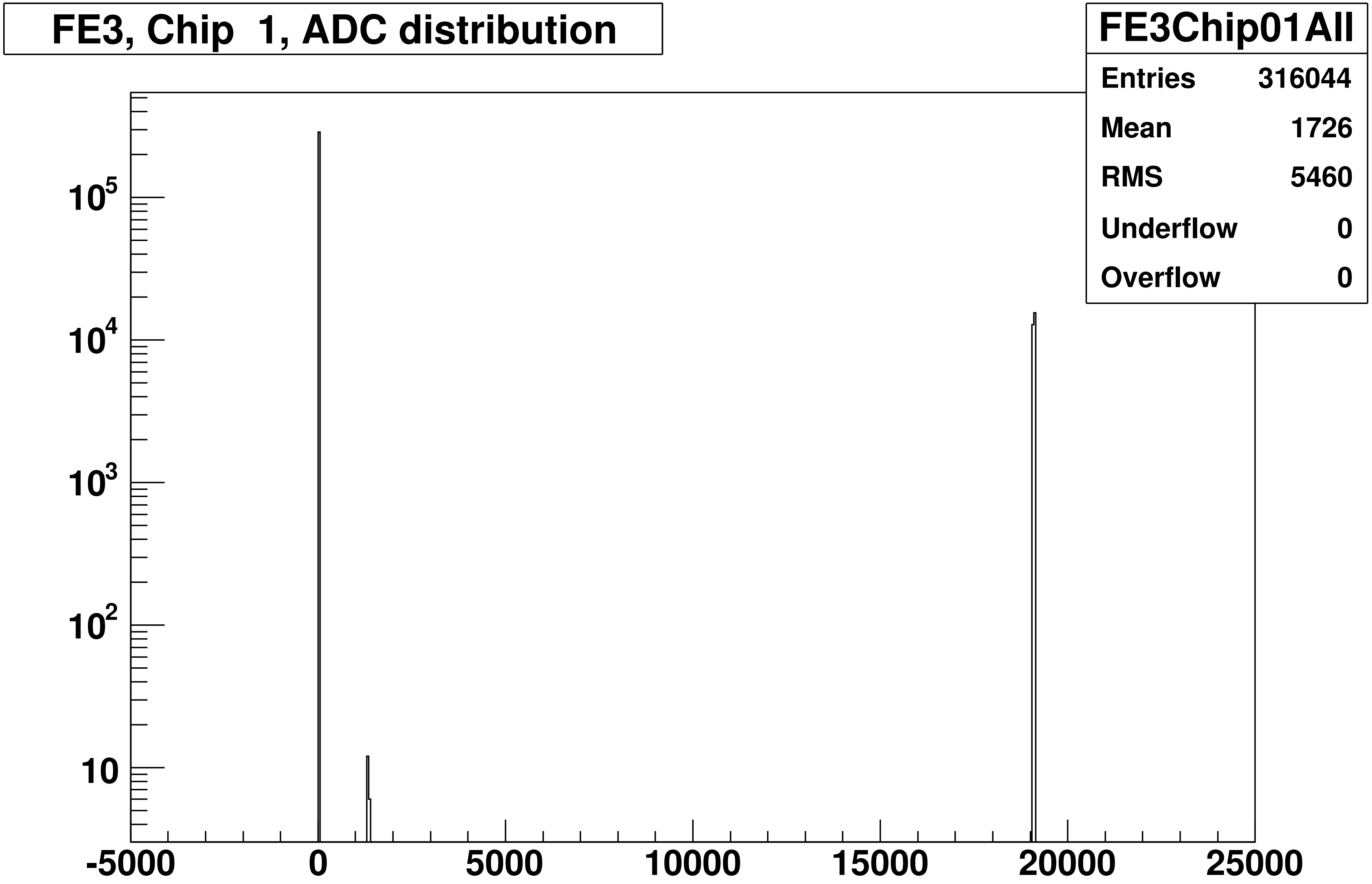
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE3, Chip 1, ADC distribution
FE3Chip01All
Entries 316044
Mean 1726
RMS 5460
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
-5000
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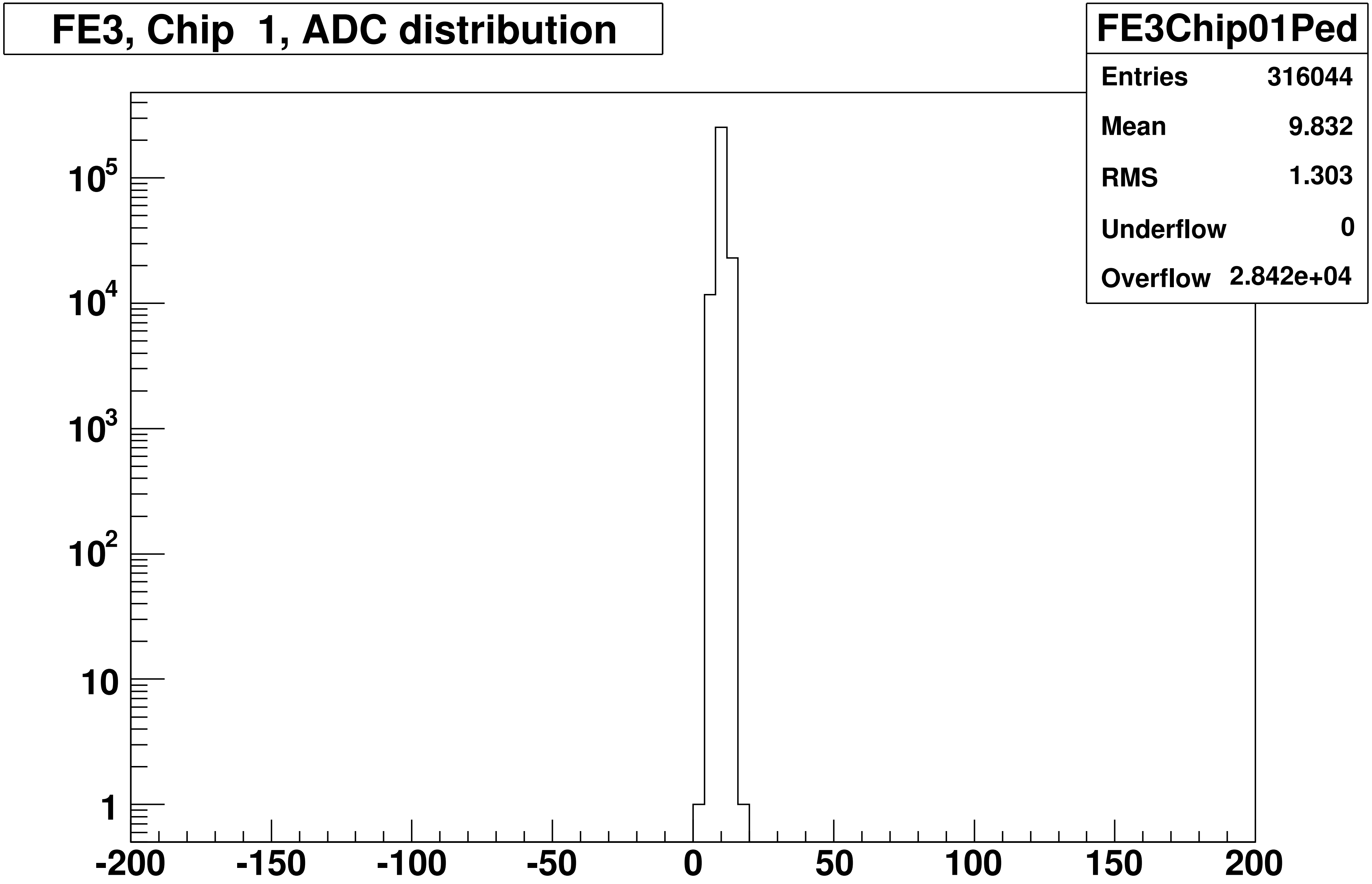
20000
25000



FE3, Chip 1, ADC distribution
FE3Chip01Ped
Entries 316044
Mean 9.832
RMS 1.303
Underflow 0
Overflow 2.842e+04
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10^4
10^3
10^2
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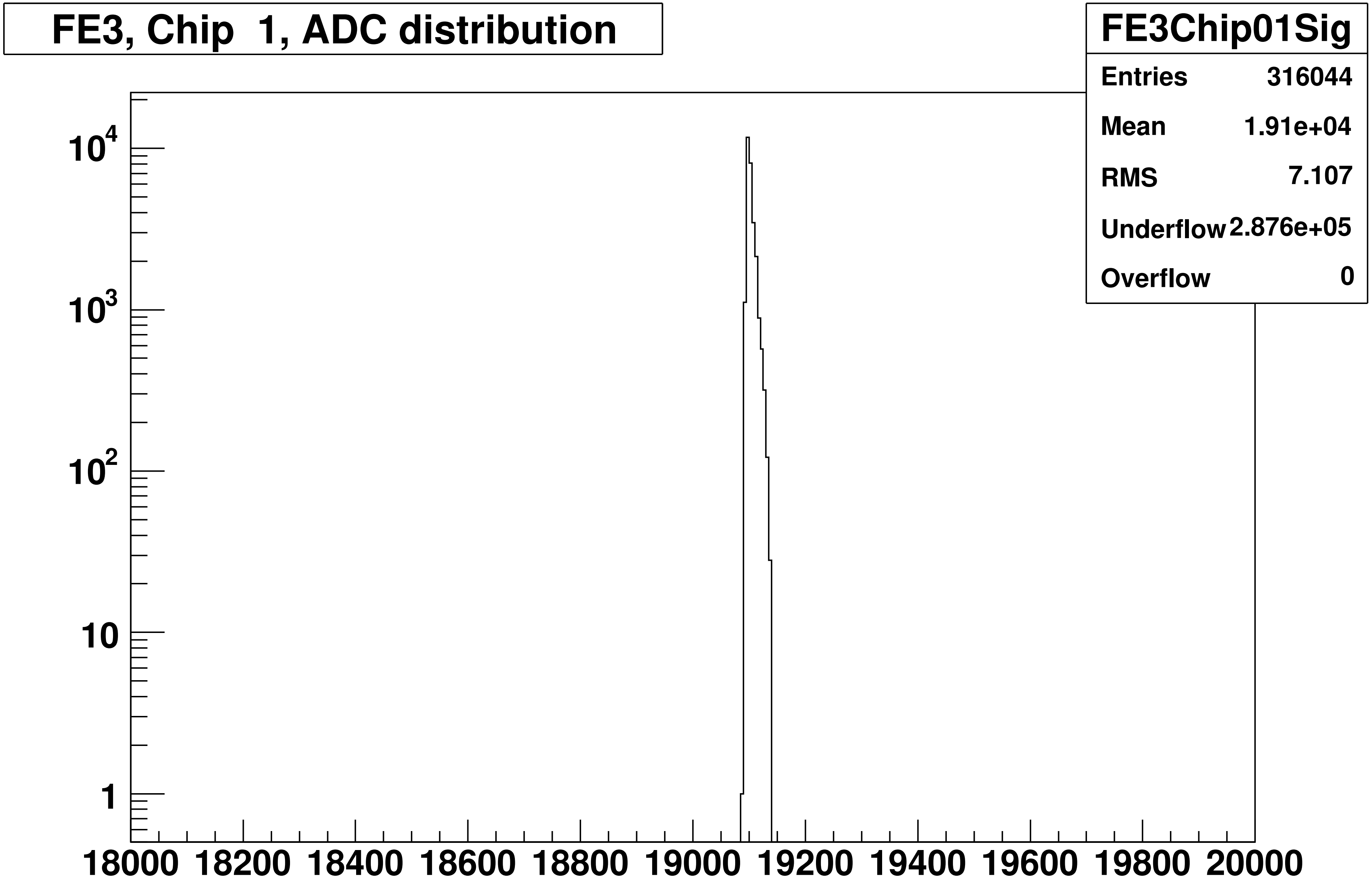
FE3, Chip 1, ADC distribution
FE3Chip01Sig
Entries 316044
Mean 1.91e+04
RMS 7.107
Underflow 2.876e+05
Overflow 0
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10^3
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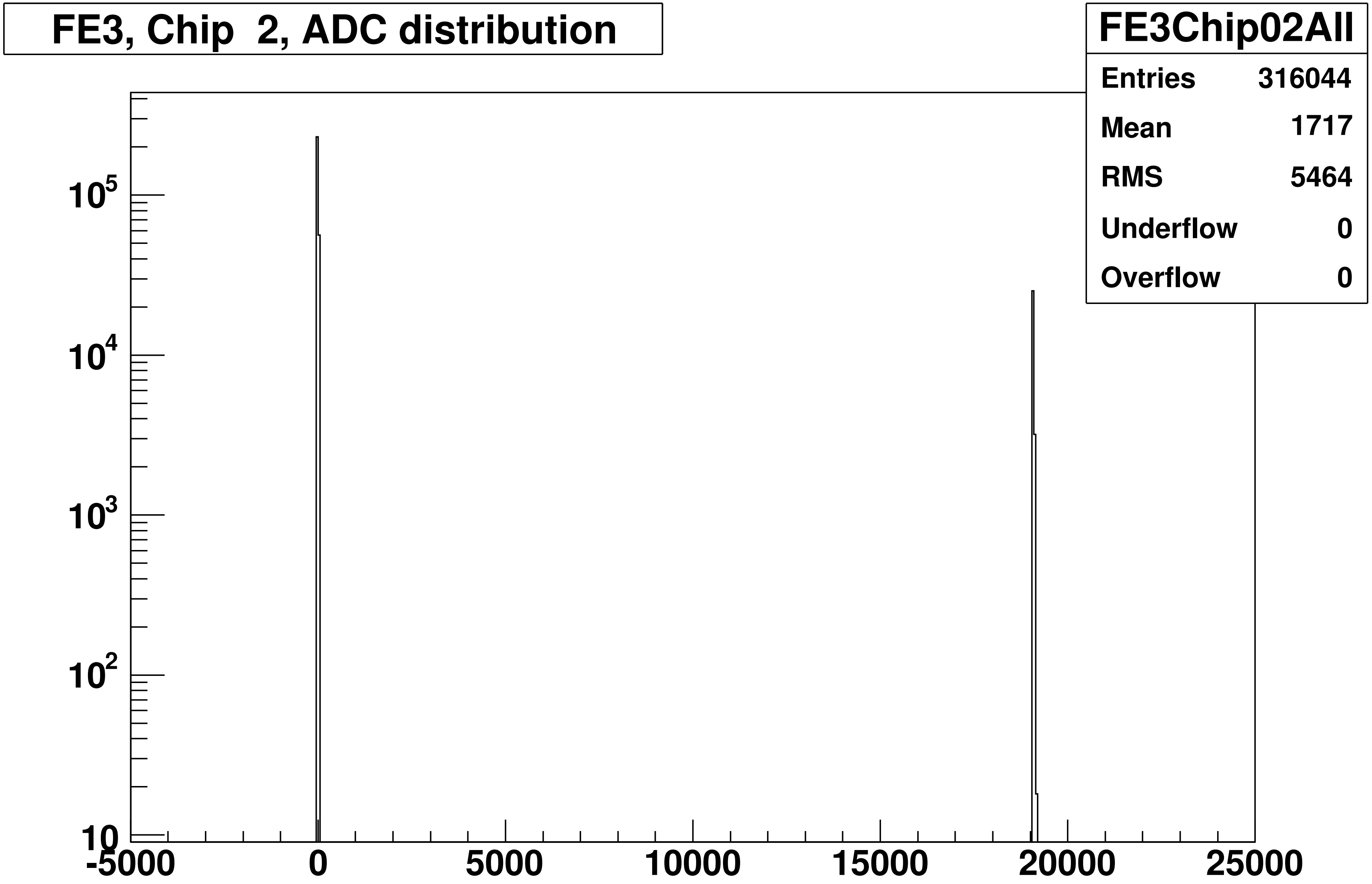
FE3, Chip 2, ADC distribution
FE3Chip02All
Entries 316044
Mean 1717
RMS 5464
Underflow 0
Overflow 0
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10^5
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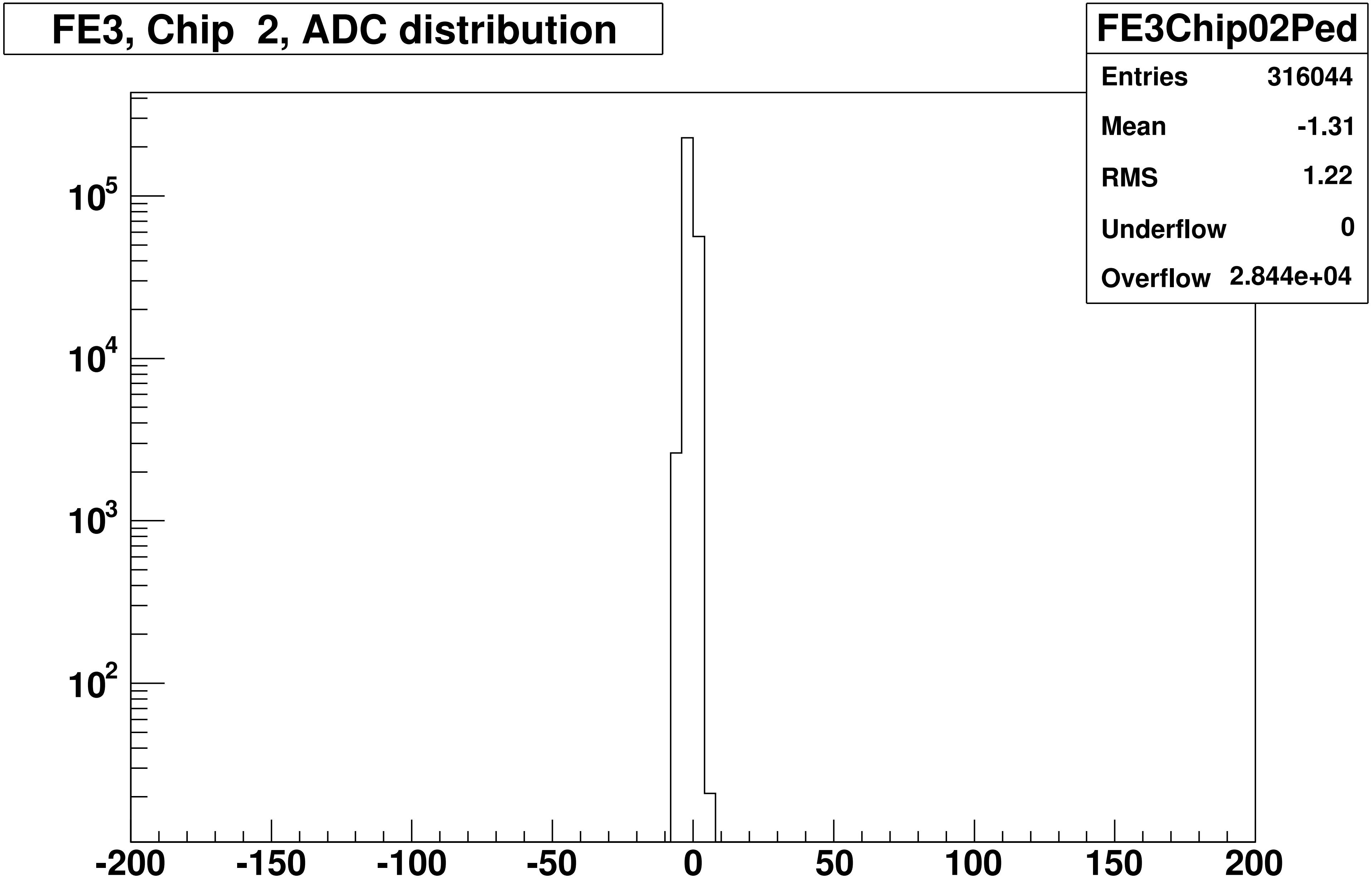

FE3, Chip 2, ADC distribution
FE3Chip02Ped
Entries 316044
Mean -1.31
RMS 1.22
Underflow 0
Overflow 2.844e+04
10^5
10^4
10^3
10^2
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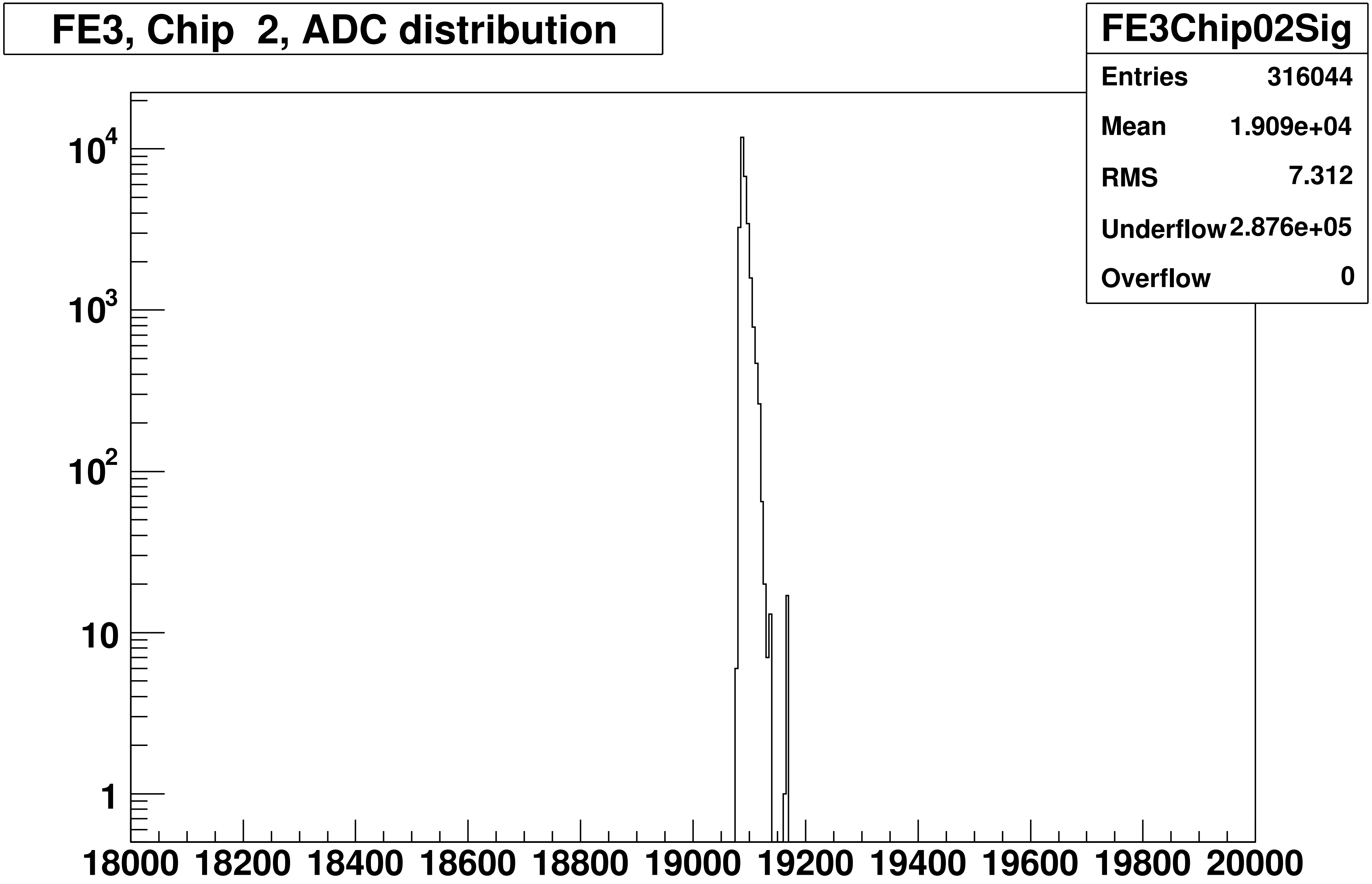
FE3, Chip 2, ADC distribution
FE3Chip02Sig
Entries 316044
Mean 1.909e+04
RMS 7.312
Underflow 2.876e+05
Overflow 0
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10^2
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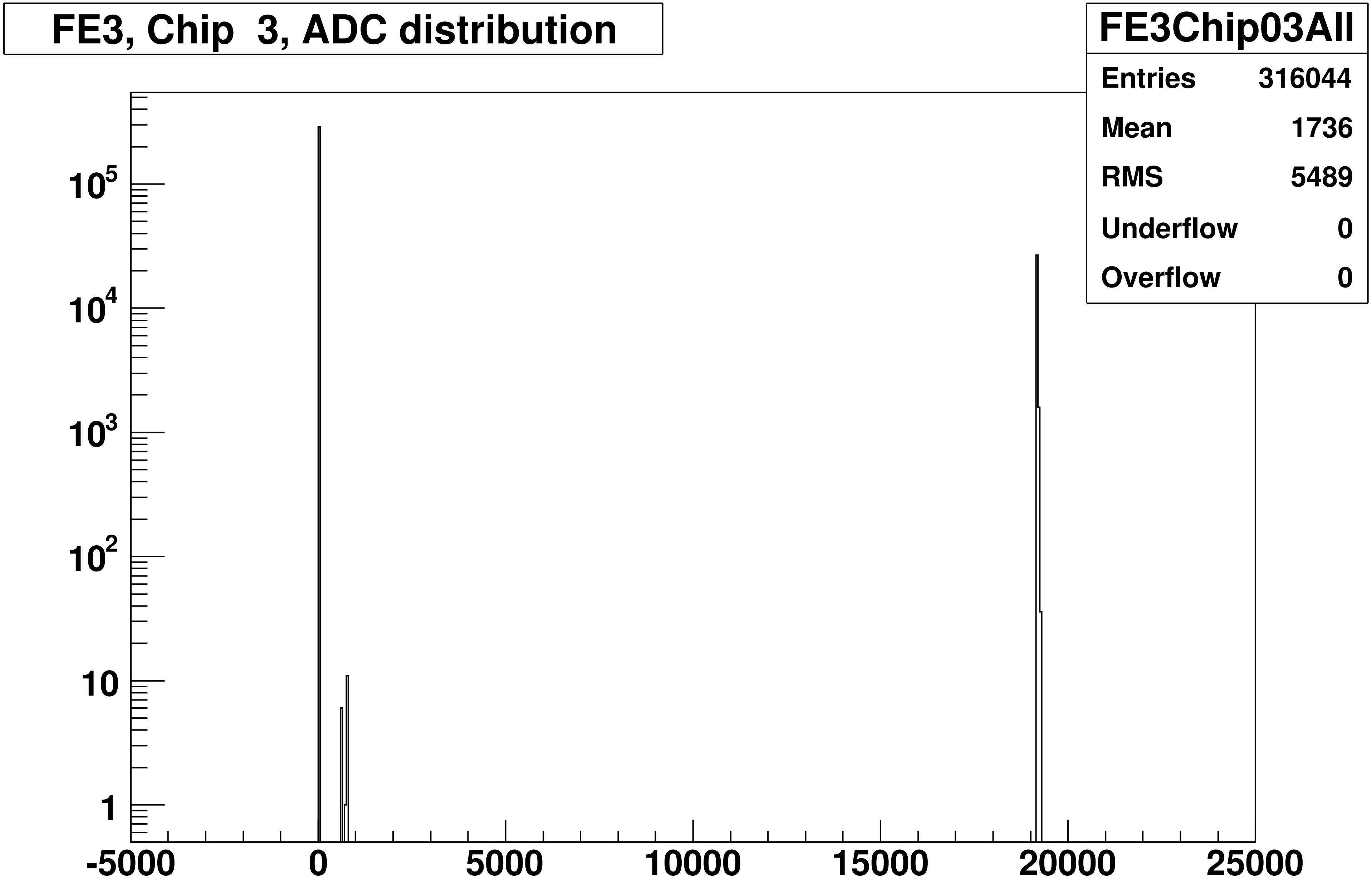
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE3, Chip 3, ADC distribution
FE3Chip03All
Entries 316044
Mean 1736
RMS 5489
Underflow 0
Overflow 0
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10^4
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10^2
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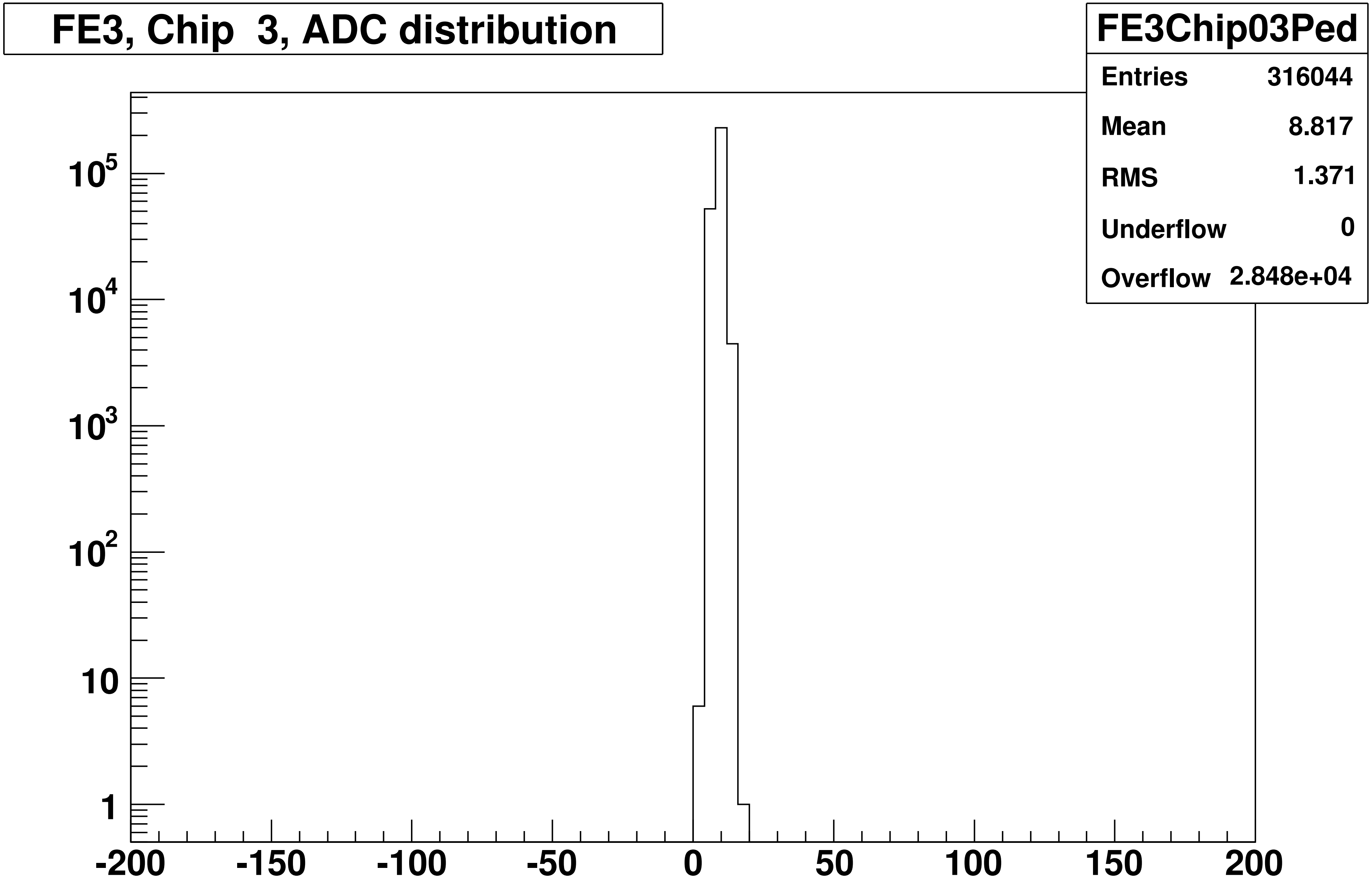
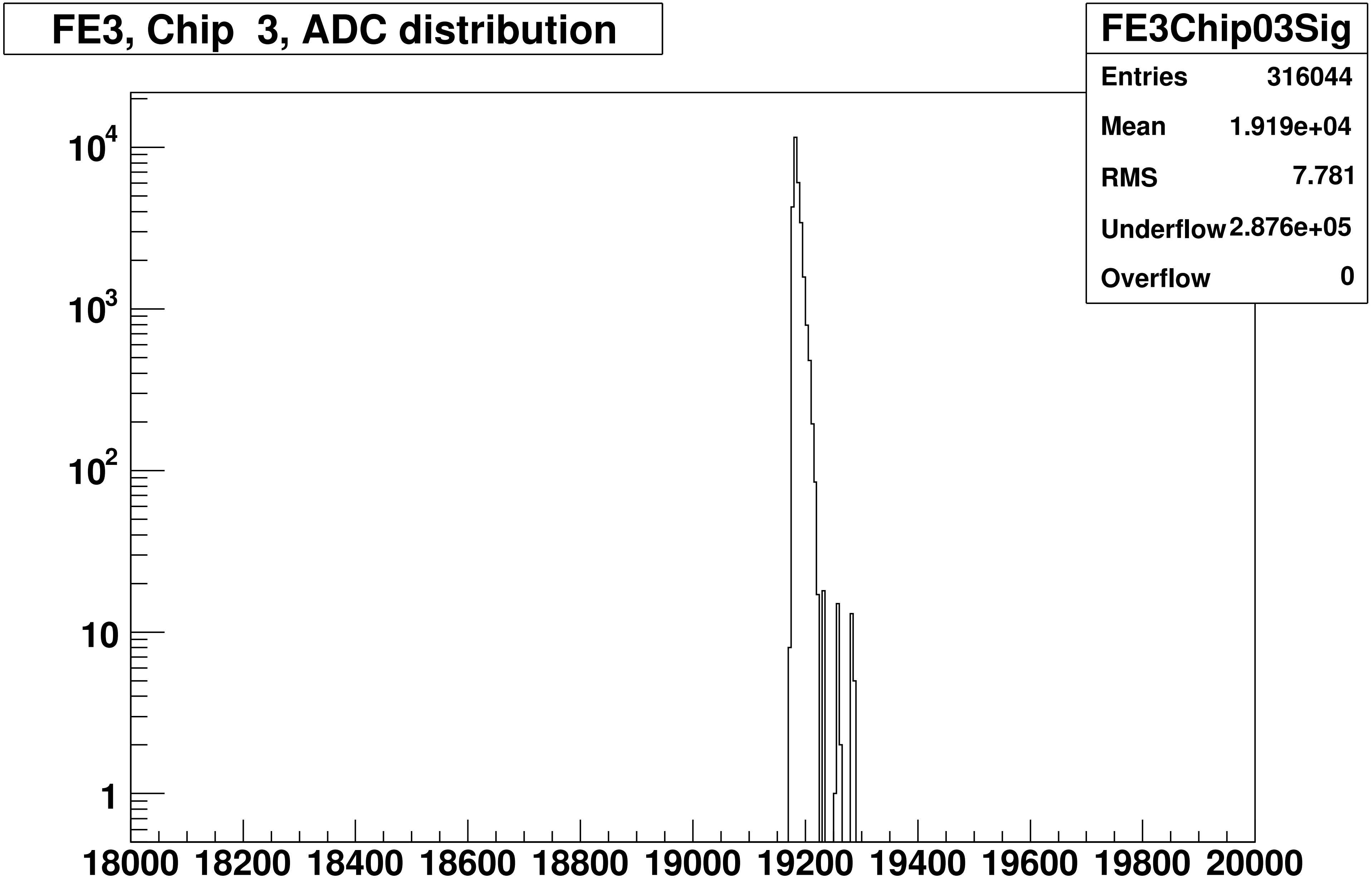

FE3, Chip 3, ADC distribution
FE3Chip03Ped
Entries 316044
Mean 8.817
RMS 1.371
Underflow 0
Overflow 2.848e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
200


FE3, Chip 3, ADC distribution
FE3Chip03Sig
Entries 316044
Mean 1.919e+04
RMS 7.781
Underflow 2.876e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
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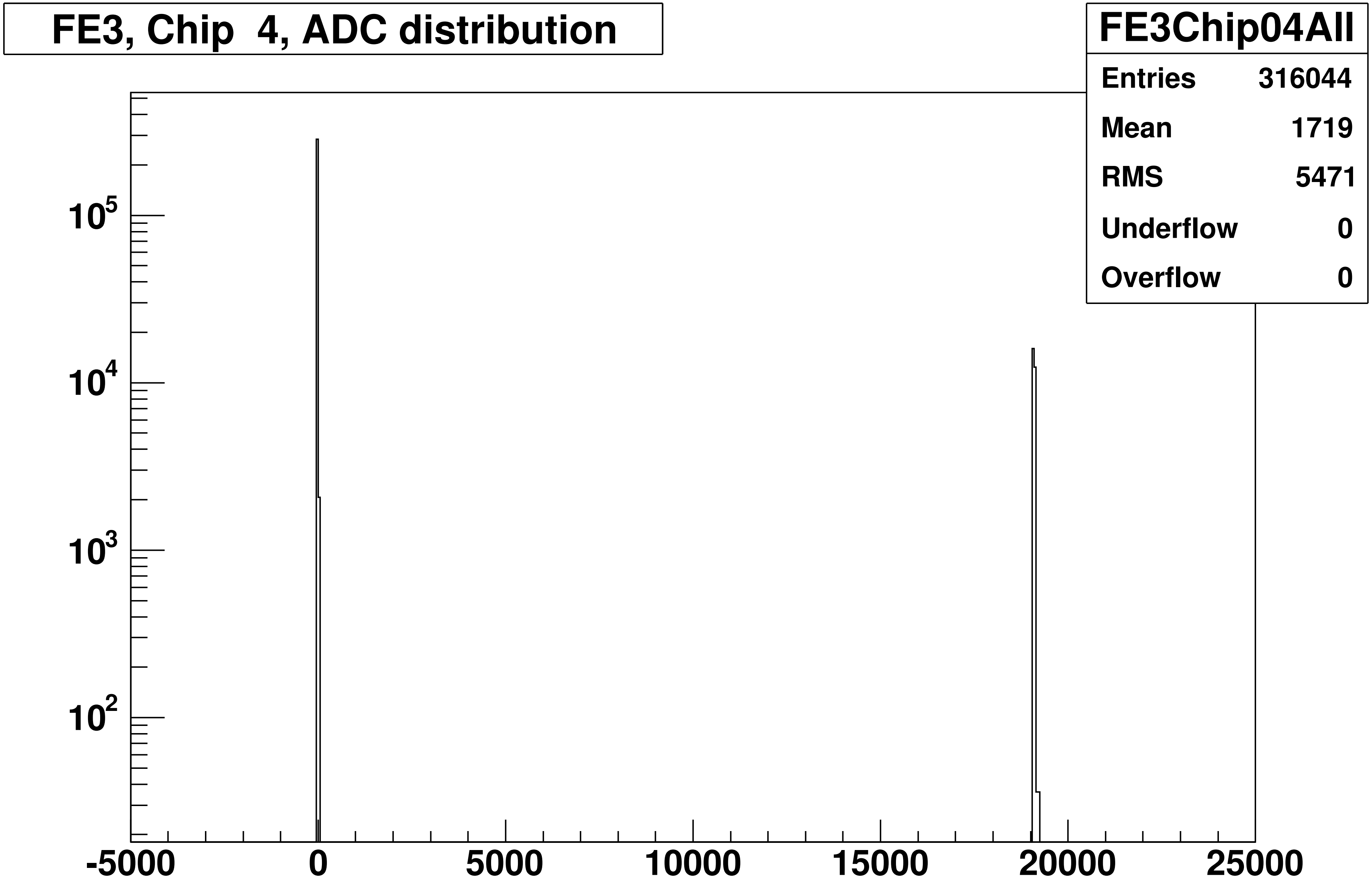
19600
19800
20000


FE3, Chip 4, ADC distribution
FE3Chip04All
Entries 316044
Mean 1719
RMS 5471
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
-5000
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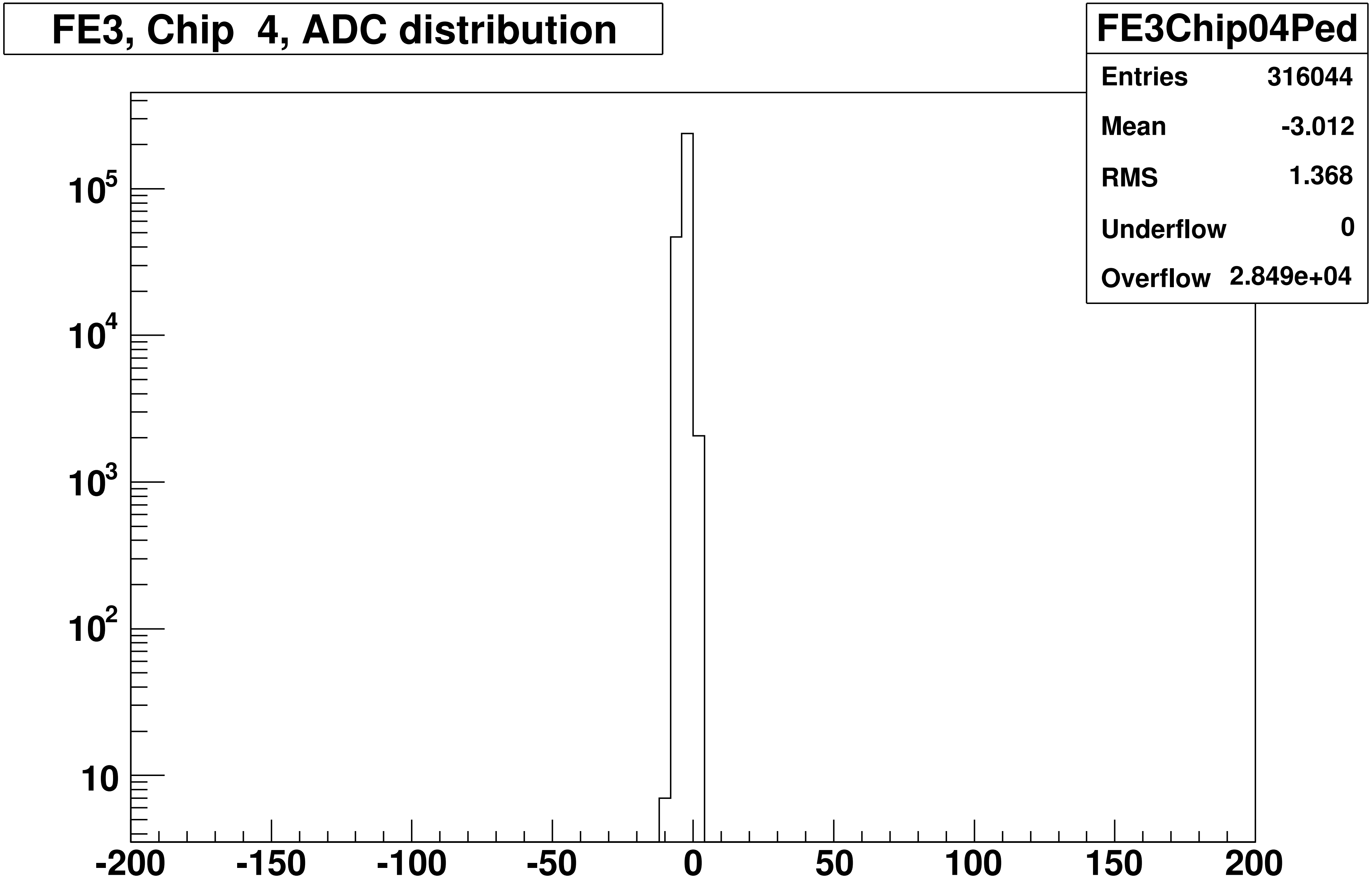
FE3, Chip 4, ADC distribution
FE3Chip04Ped
Entries 316044
Mean -3.012
RMS 1.368
Underflow 0
Overflow 2.849e+04
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10^2
10^3
10^4
10^5
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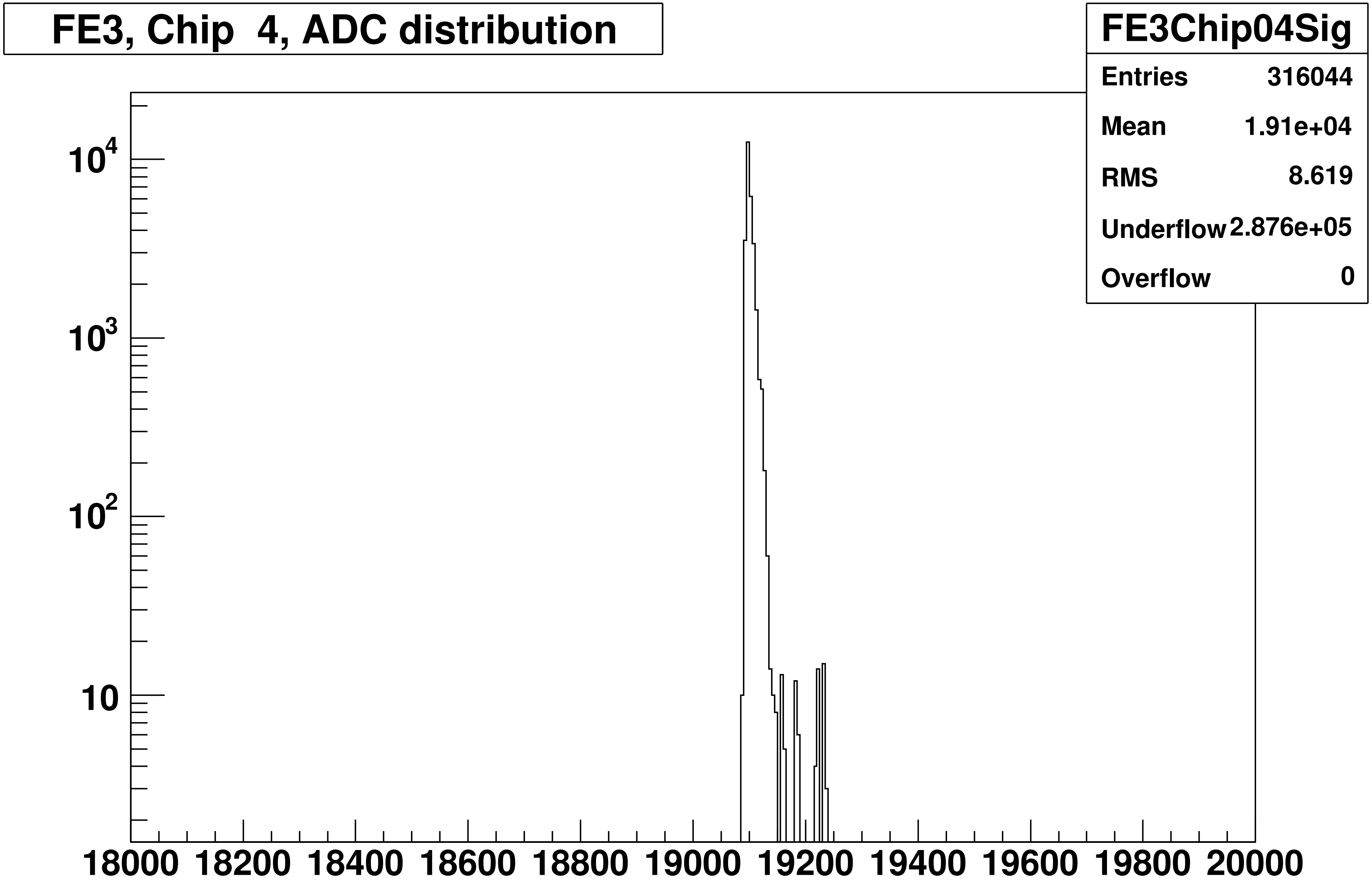
100
150
200


FE3, Chip 4, ADC distribution
FE3Chip04Sig
Entries 316044
Mean 1.91e+04
RMS 8.619
Underflow 2.876e+05
Overflow 0
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10^3
10^2
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18000
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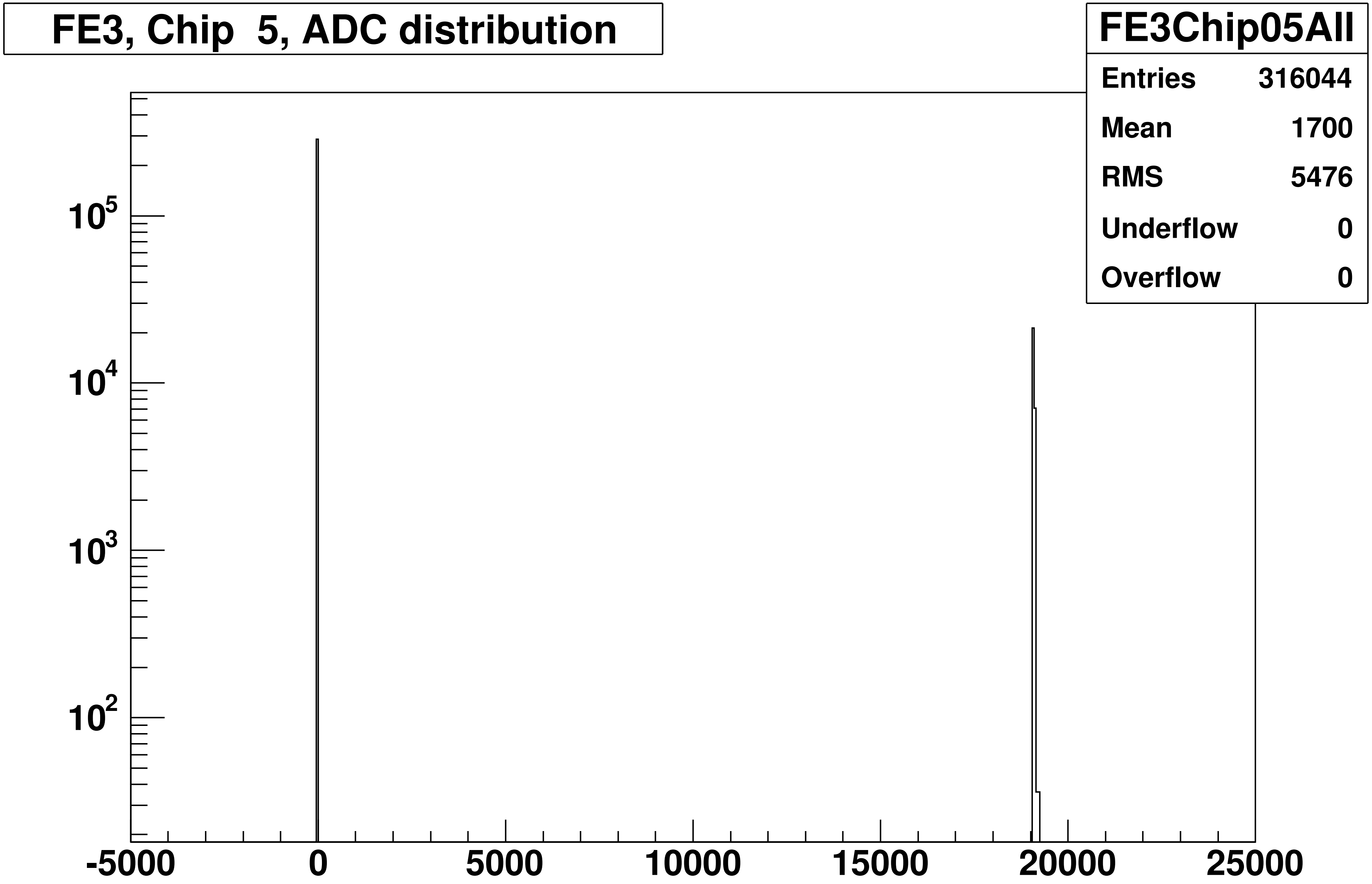
FE3, Chip 5, ADC distribution
FE3Chip05All
Entries 316044
Mean 1700
RMS 5476
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
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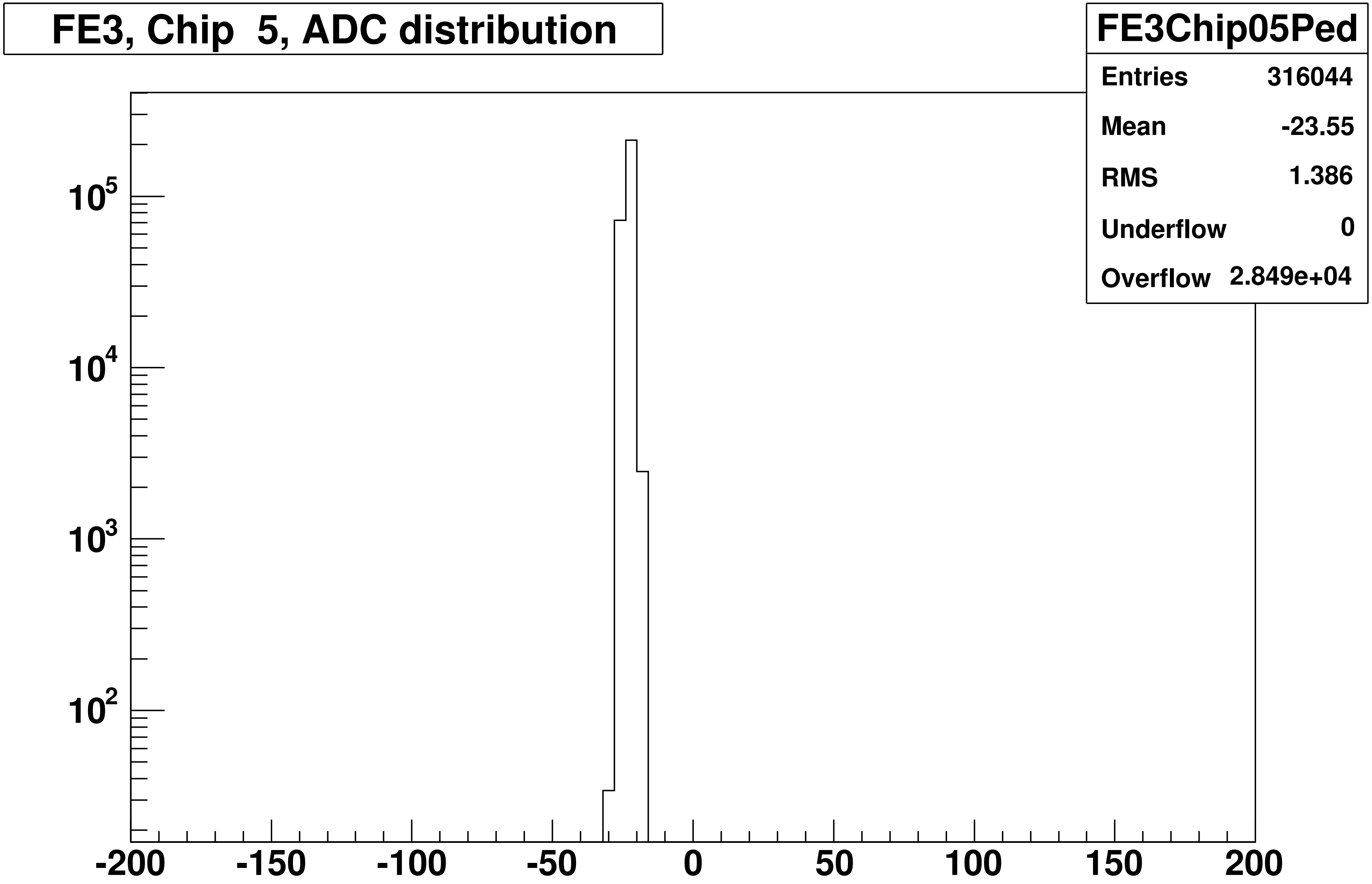
0
5000
10000
15000
20000
25000


FE3, Chip 5, ADC distribution
FE3Chip05Ped
Entries 316044
Mean -23.55
RMS 1.386
Underflow 0
Overflow 2.849e+04
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10^4
10^3
10^2
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150
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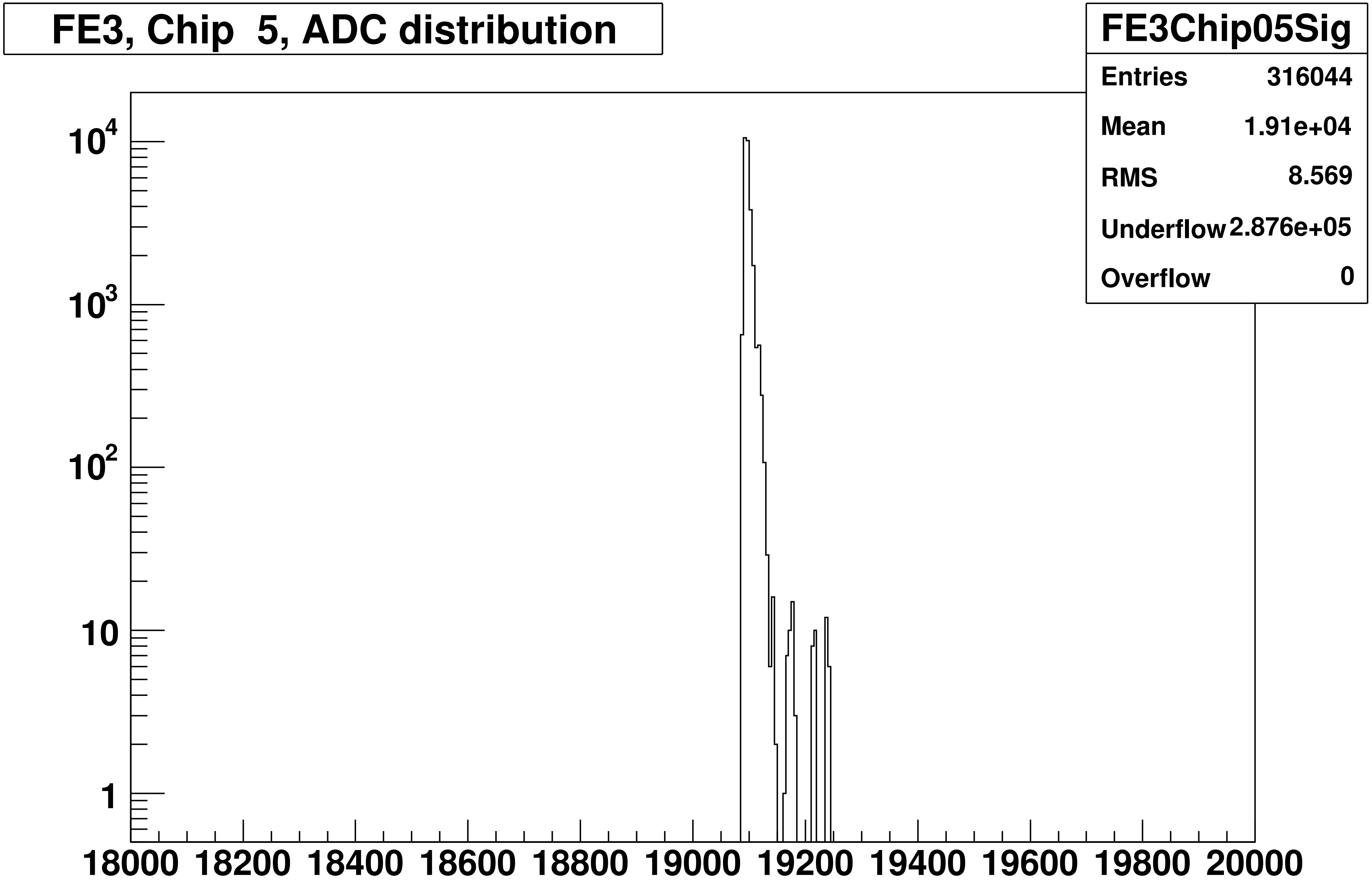
FE3, Chip 5, ADC distribution
FE3Chip05Sig
Entries 316044
Mean 1.91e+04
RMS 8.569
Underflow 2.876e+05
Overflow 0
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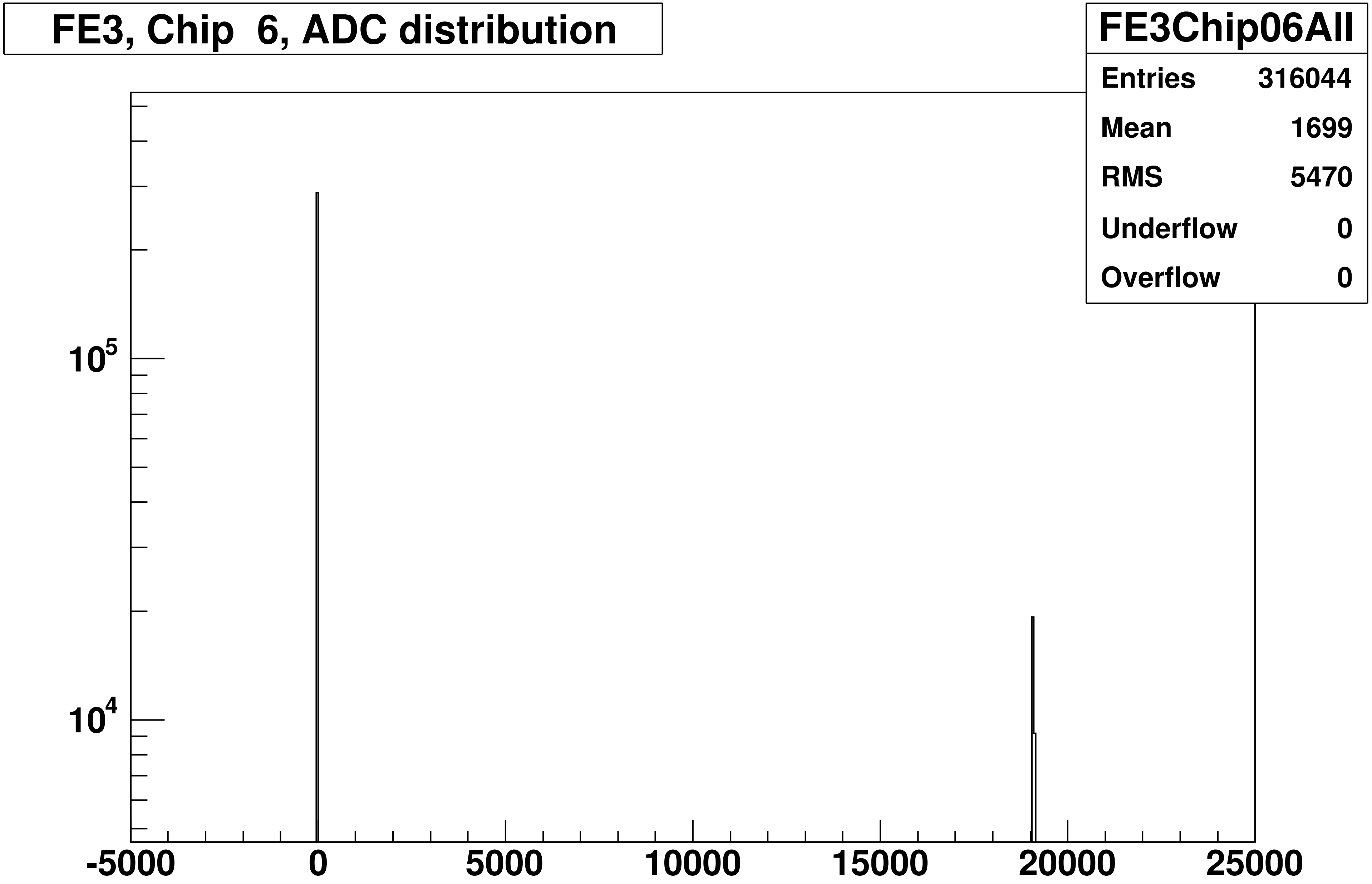
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE3, Chip 6, ADC distribution
FE3Chip06All
Entries 316044
Mean 1699
RMS 5470
Underflow 0
Overflow 0
10^5
10^4
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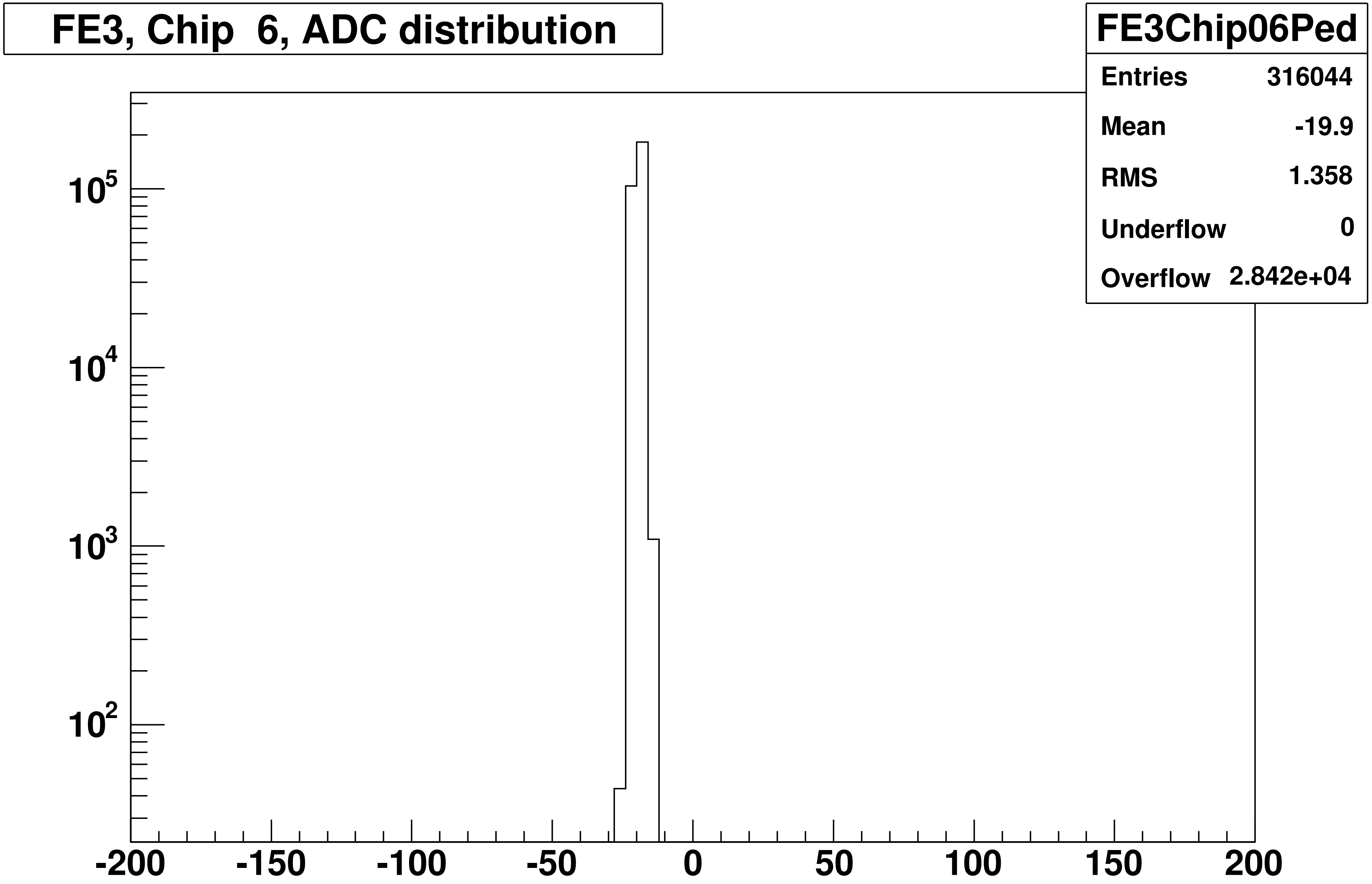
5000
10000
15000
20000
25000


FE3, Chip 6, ADC distribution
FE3Chip06Ped
Entries 316044
Mean -19.9
RMS 1.358
Underflow 0
Overflow 2.842e+04
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10^4
10^3
10^2
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100
150
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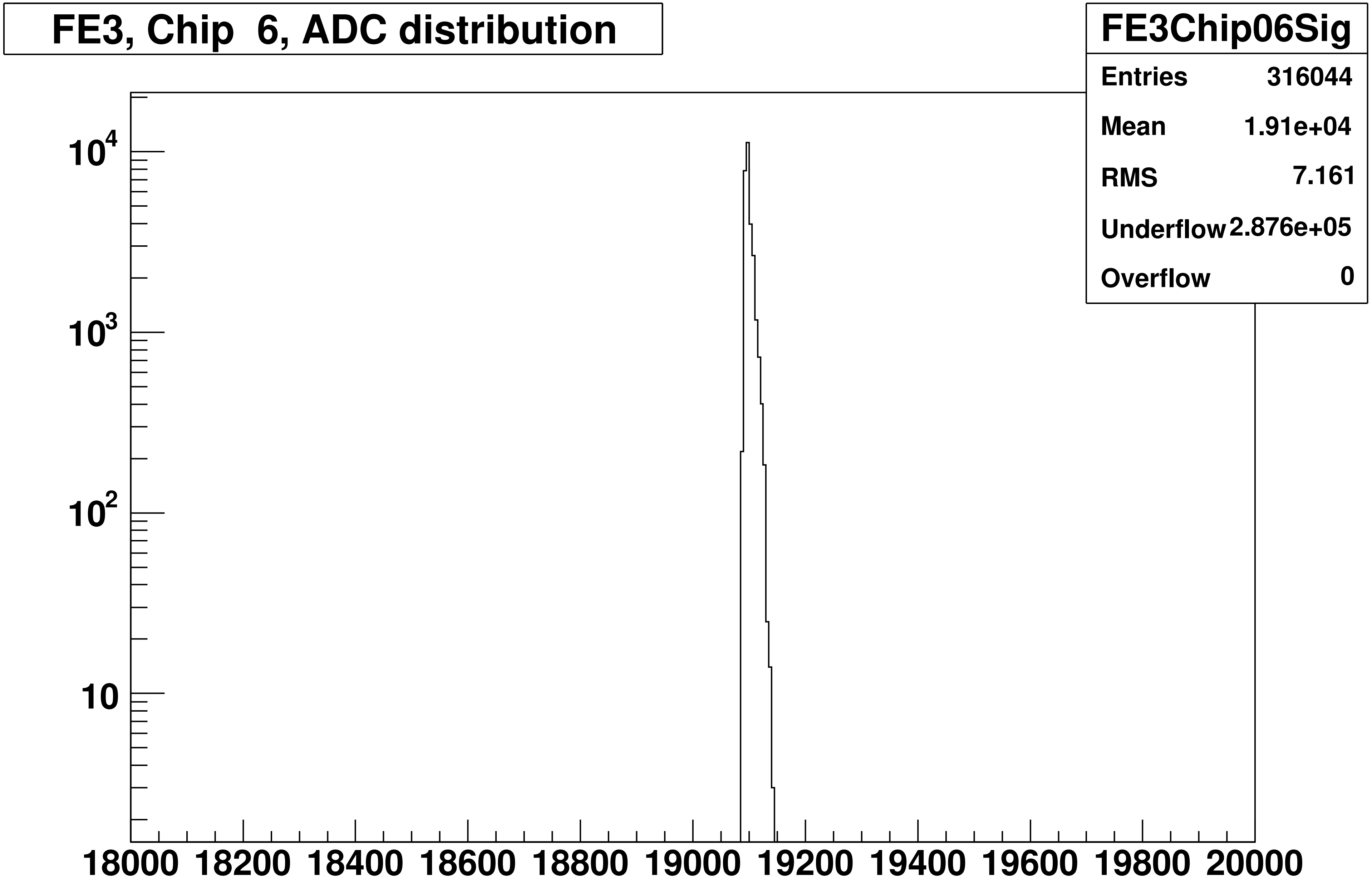
FE3, Chip 6, ADC distribution
FE3Chip06Sig
Entries 316044
Mean 1.91e+04
RMS 7.161
Underflow 2.876e+05
Overflow 0
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10^3
10^2
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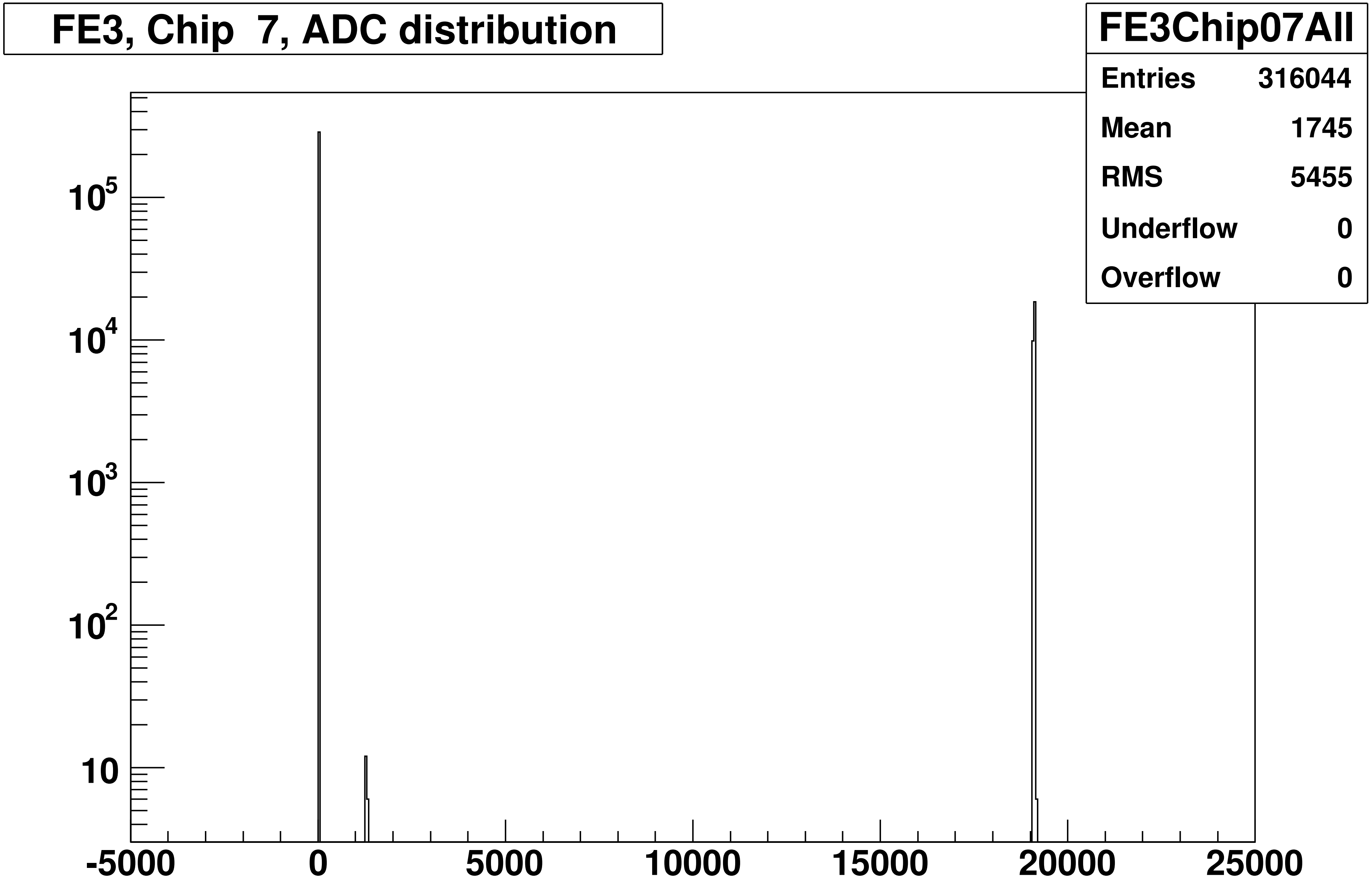
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE3, Chip 7, ADC distribution
FE3Chip07All
Entries 316044
Mean 1745
RMS 5455
Underflow 0
Overflow 0
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10^4
10^3
10^2
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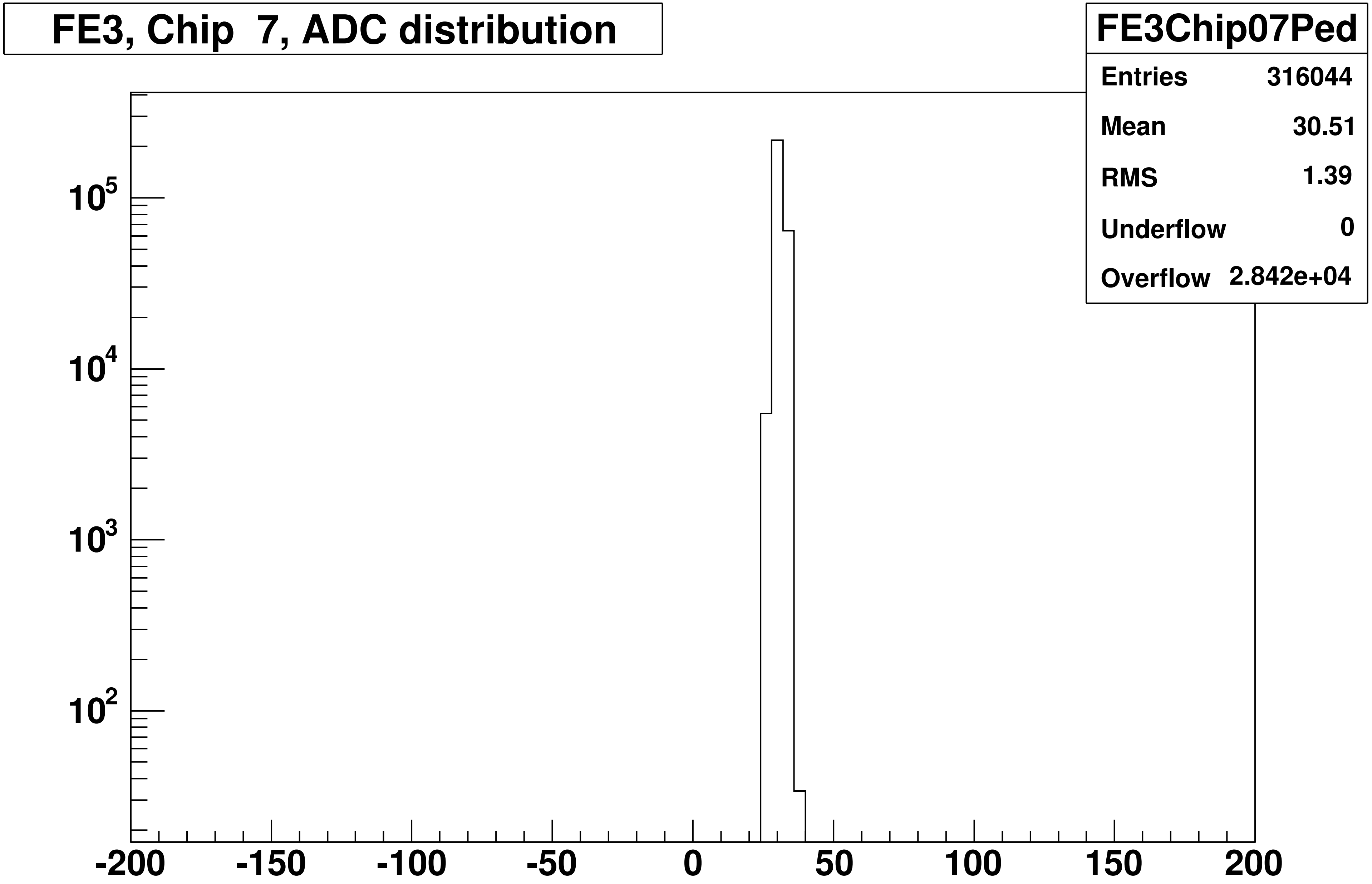
FE3, Chip 7, ADC distribution
FE3Chip07Ped
Entries 316044
Mean 30.51
RMS 1.39
Underflow 0
Overflow 2.842e+04
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10^4
10^3
10^2
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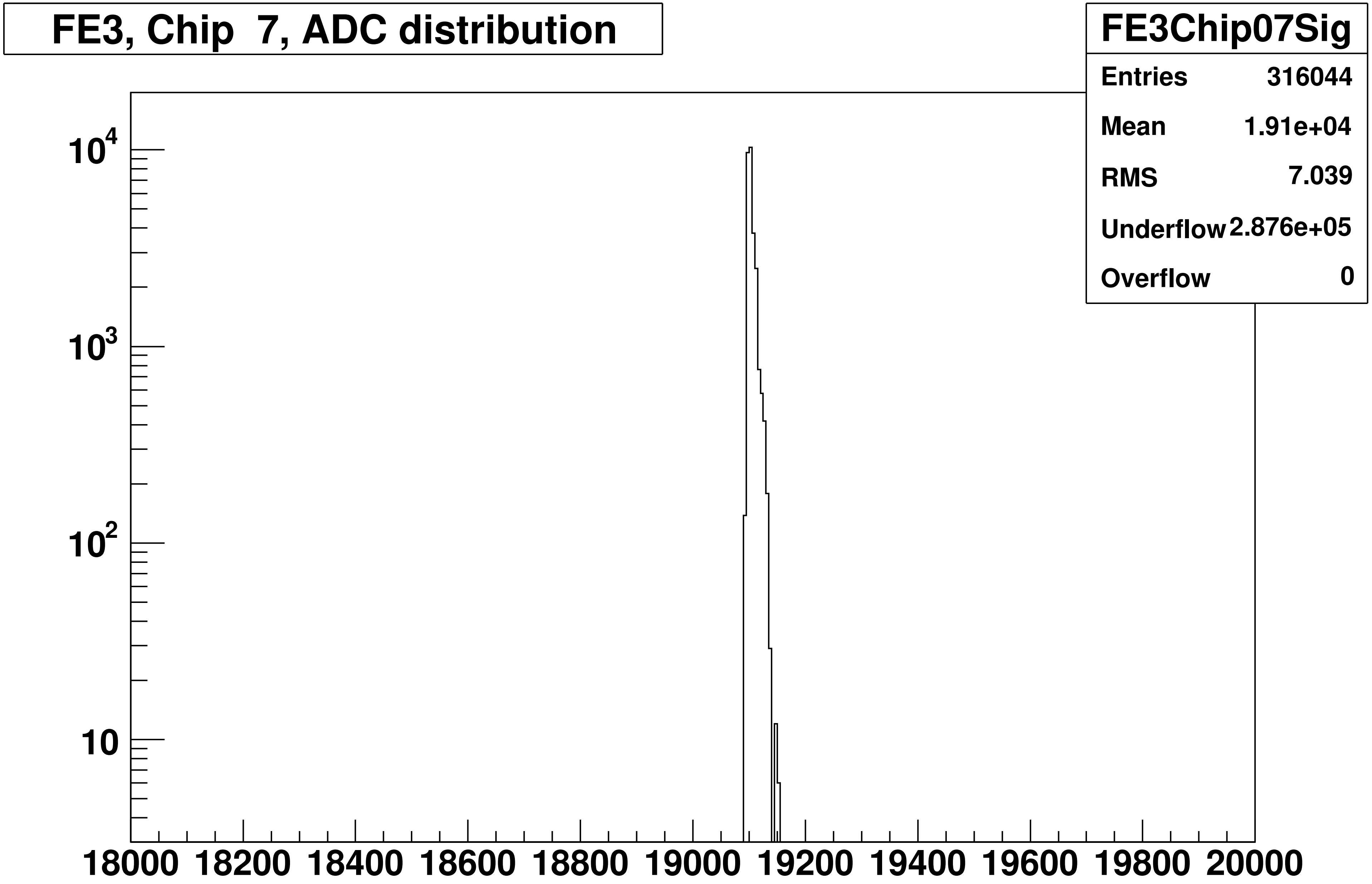
100
150
200



FE3, Chip 7, ADC distribution
FE3Chip07Sig
Entries 316044
Mean 1.91e+04
RMS 7.039
Underflow 2.876e+05
Overflow 0
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10^3
10^2
10
18000
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18400
18600
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19000
19200
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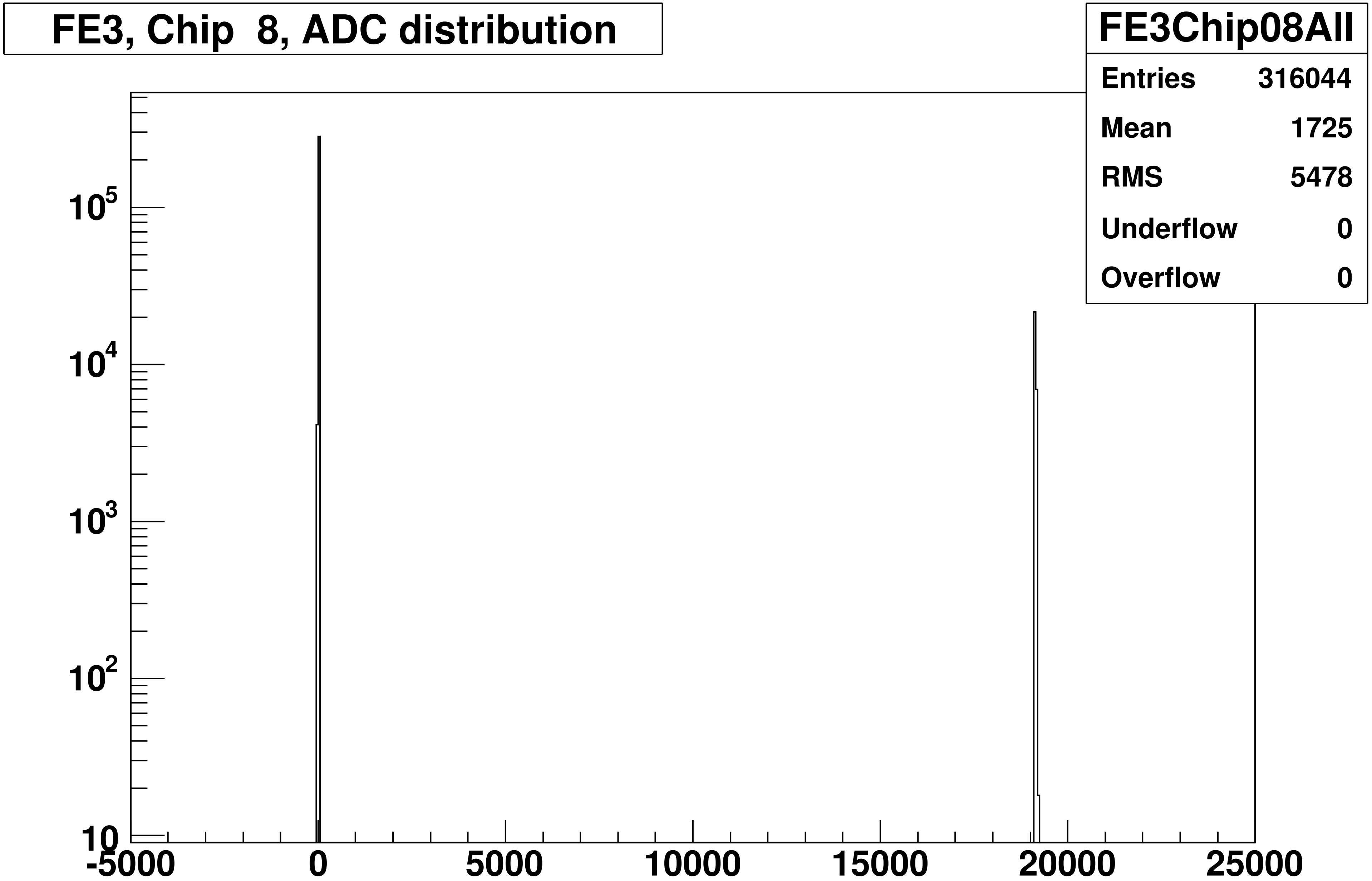
19600
19800
20000



FE3, Chip 8, ADC distribution
FE3Chip08All
Entries 316044
Mean 1725
RMS 5478
Underflow 0
Overflow 0
10
10^2
10^3
10^4
10^5
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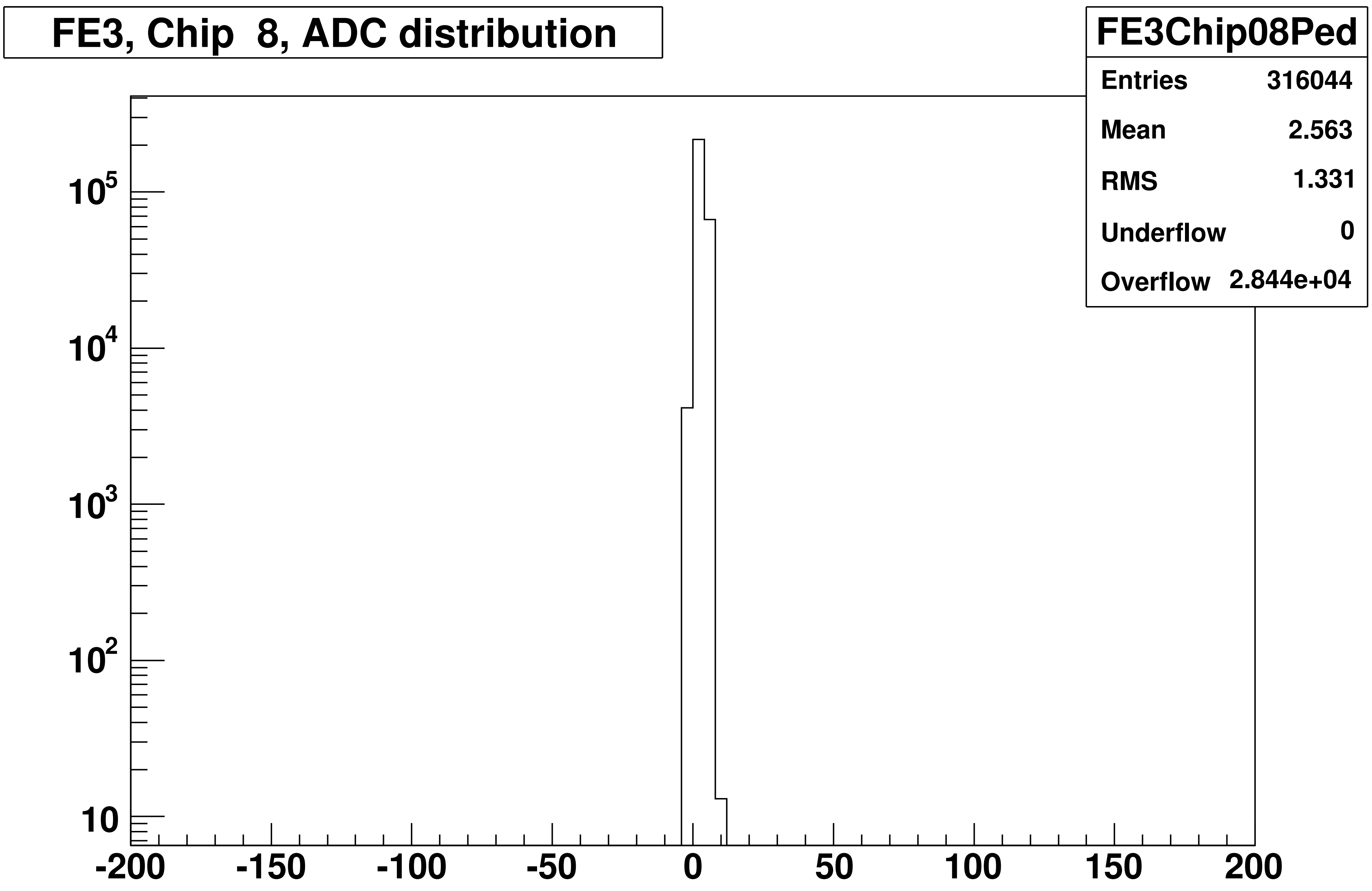
15000
20000
25000


FE3, Chip 8, ADC distribution
FE3Chip08Ped
Entries 316044
Mean 2.563
RMS 1.331
Underflow 0
Overflow 2.844e+04
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10^4
10^3
10^2
10
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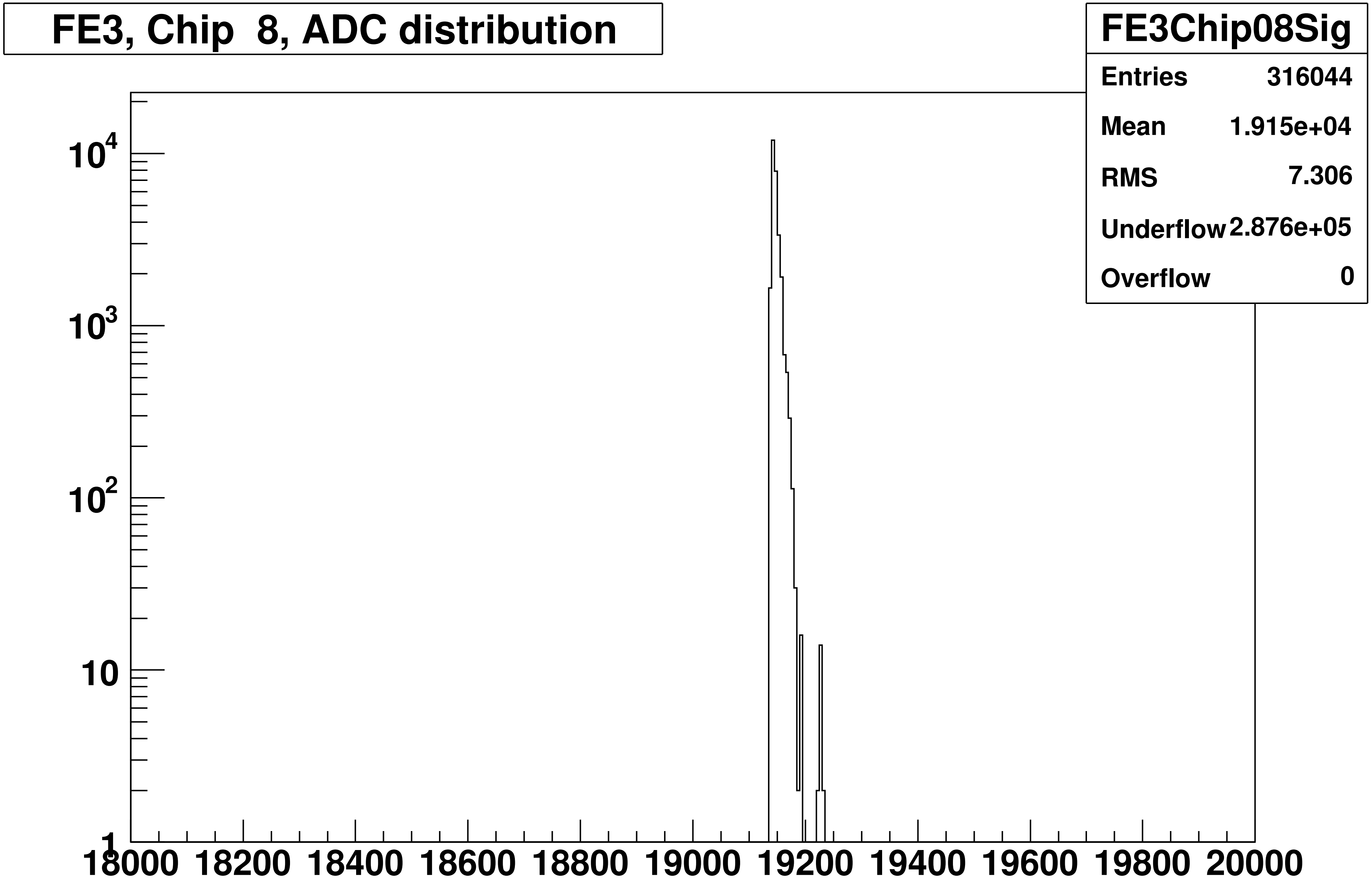
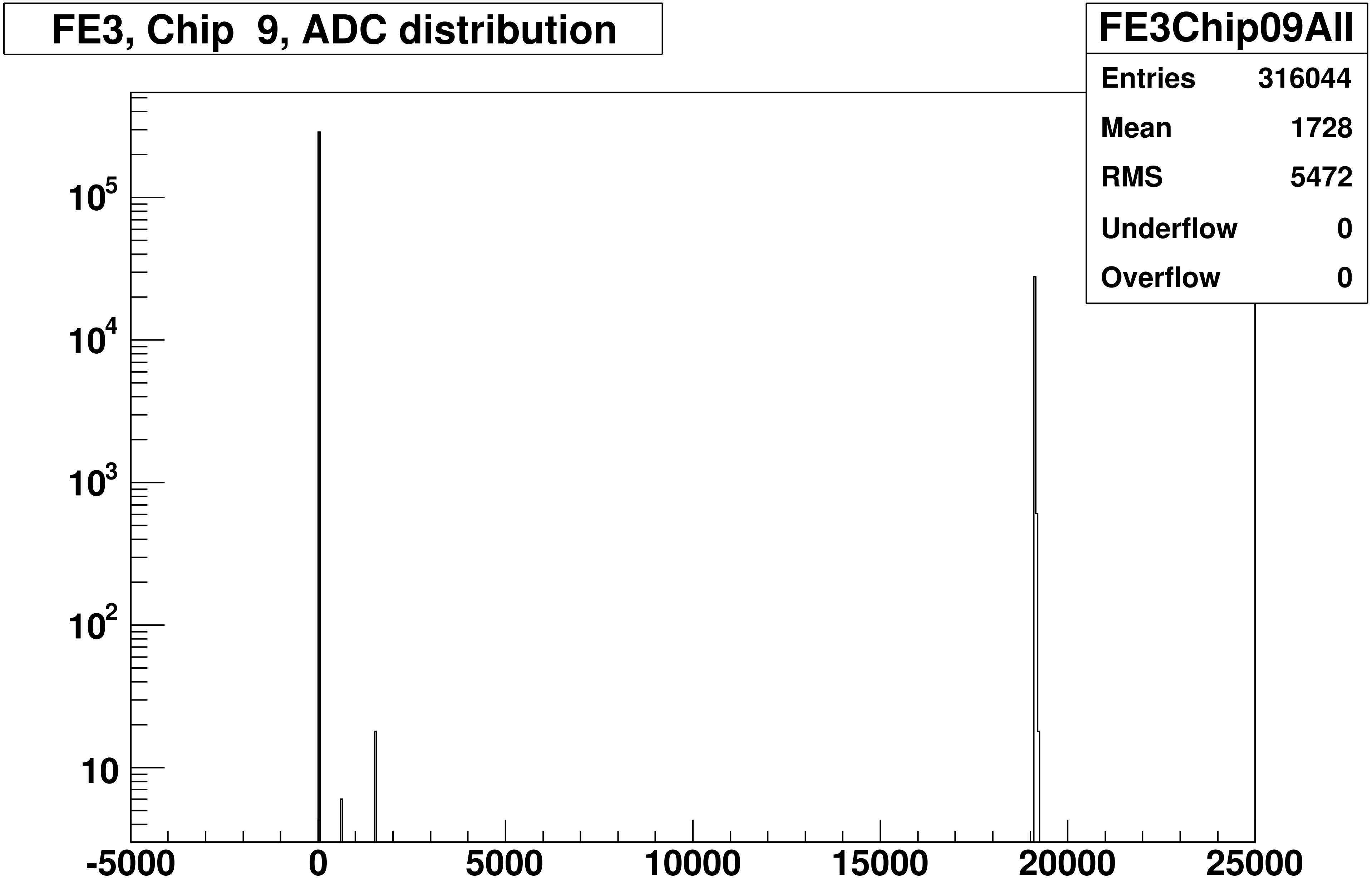
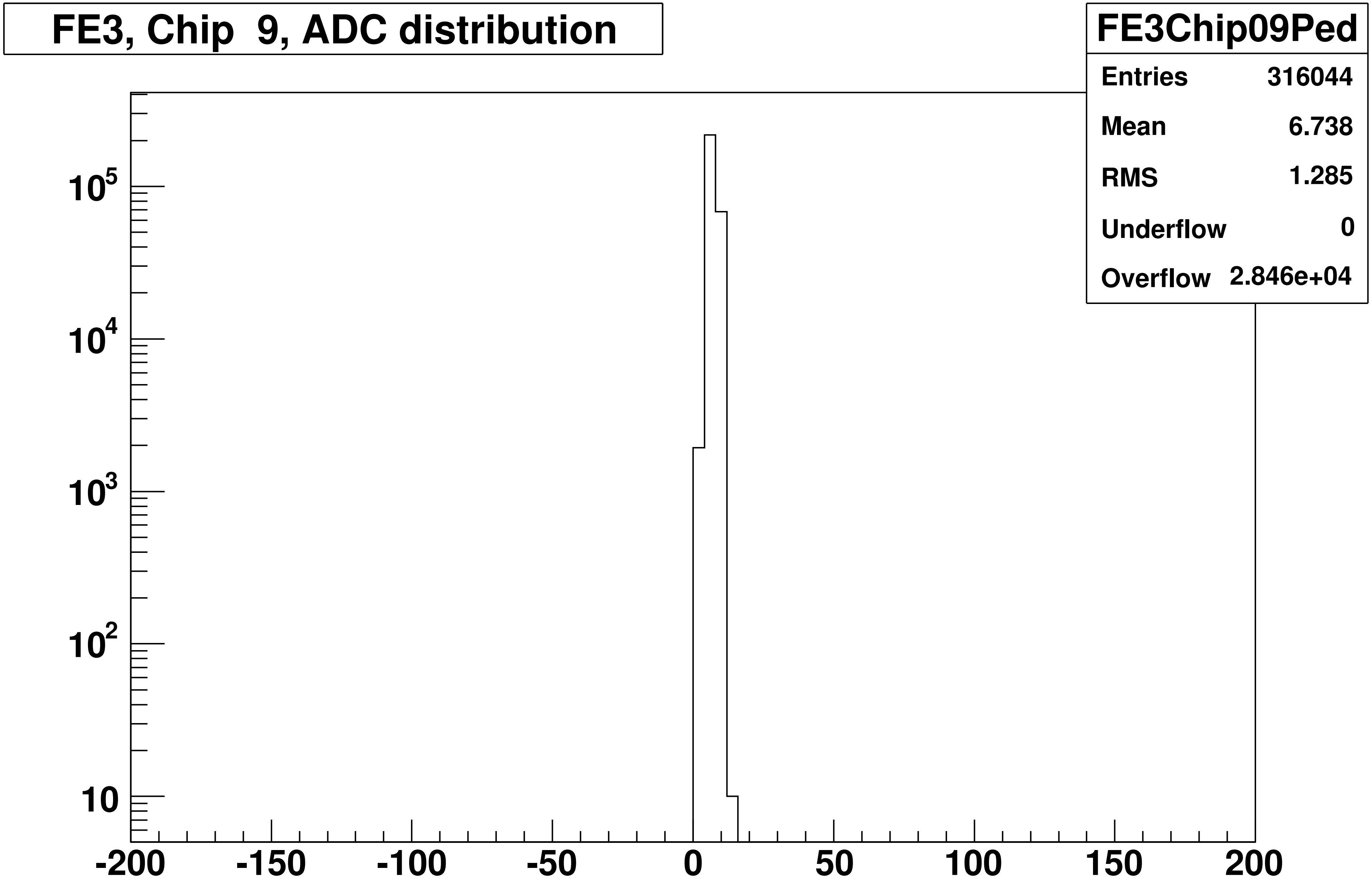
-100
-50
0
50
100
150
200


FE3, Chip 8, ADC distribution
FE3Chip08Sig
Entries 316044
Mean 1.915e+04
RMS 7.306
Underflow 2.876e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000



FE3, Chip 9, ADC distribution
FE3Chip09All
Entries 316044
Mean 1728
RMS 5472
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE3, Chip 9, ADC distribution
FE3Chip09Ped
Entries 316044
Mean 6.738
RMS 1.285
Underflow 0
Overflow 2.846e+04
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10^4
10^3
10^2
10
-200
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-100
-50
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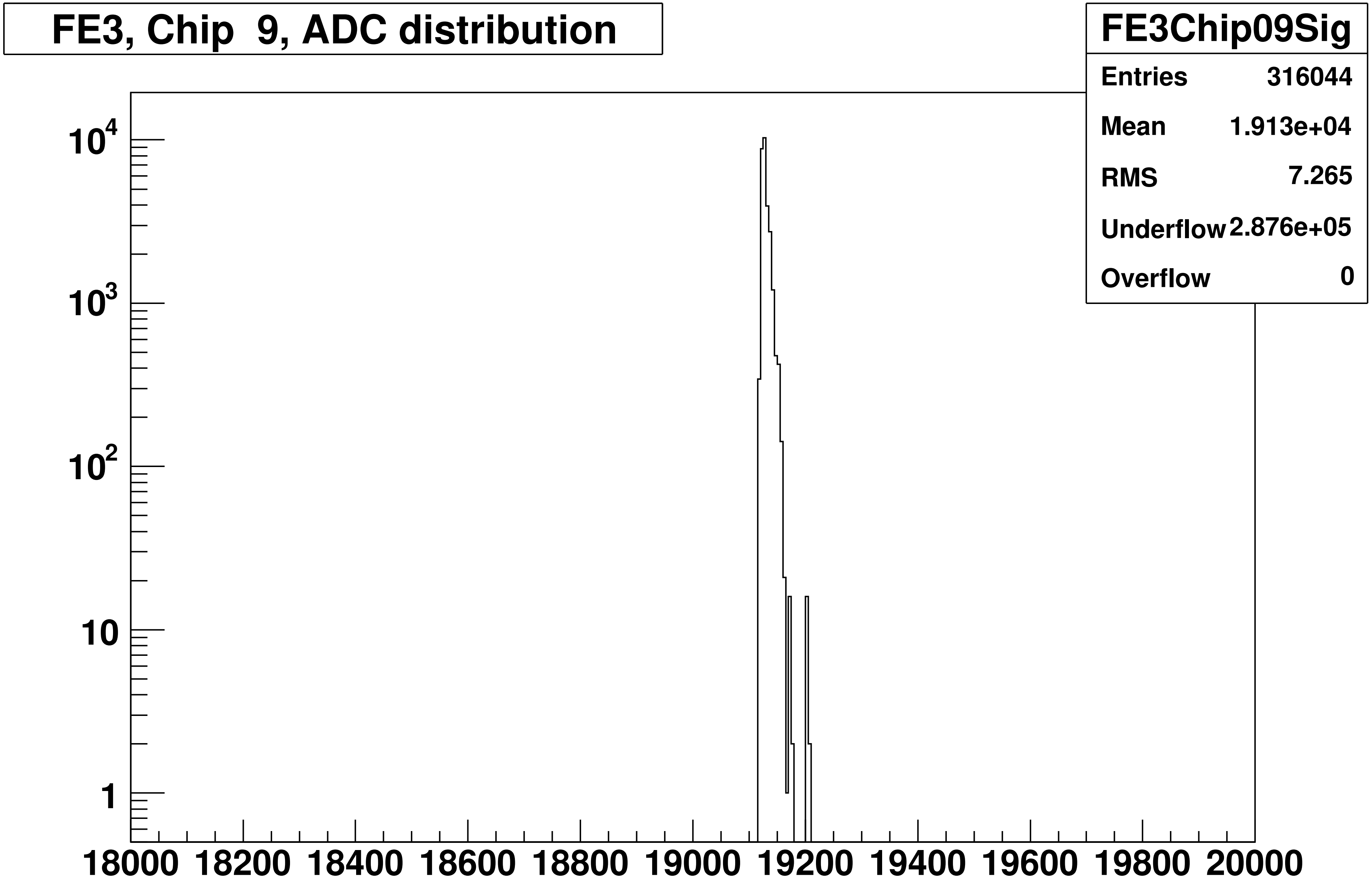
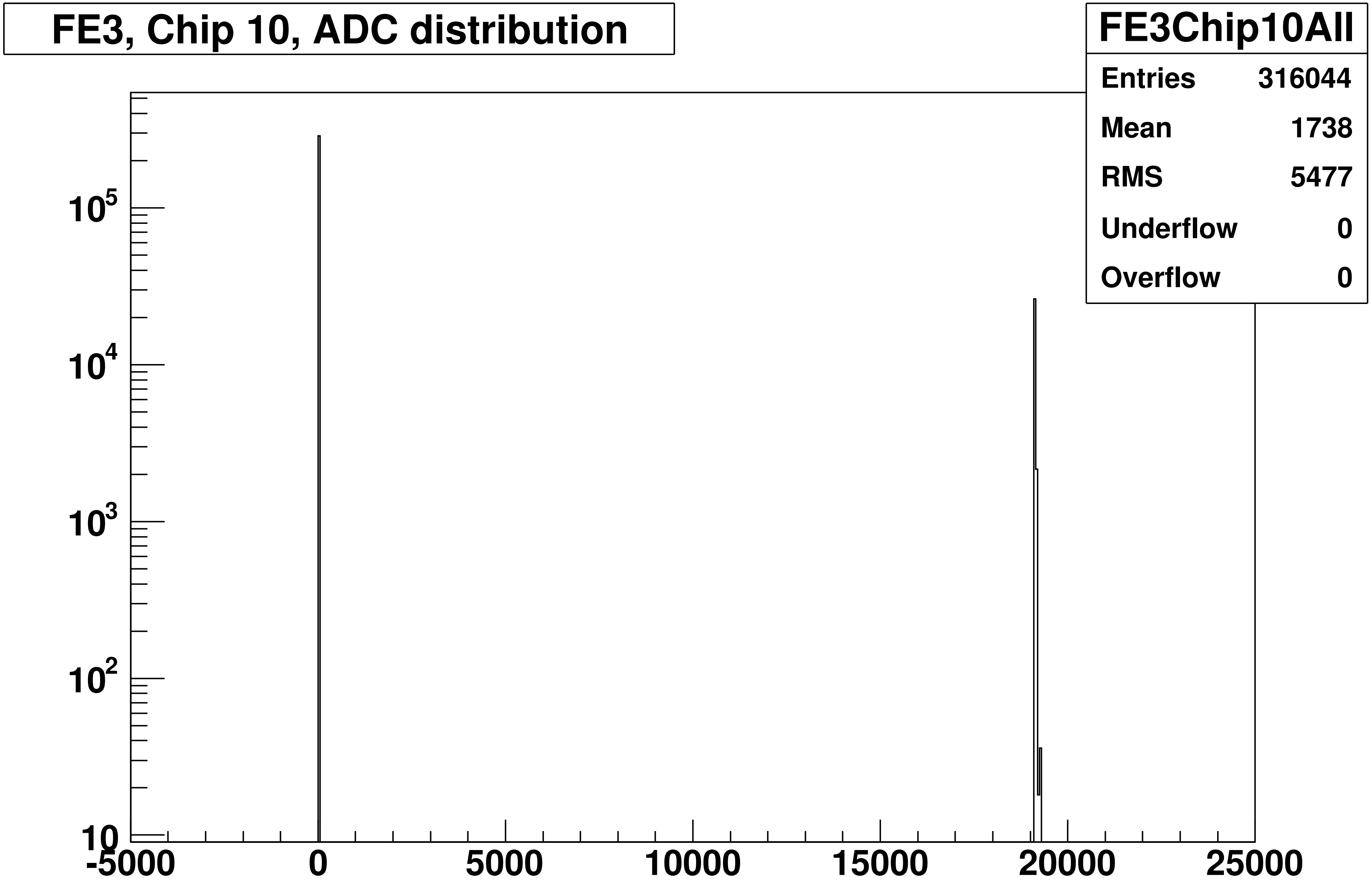
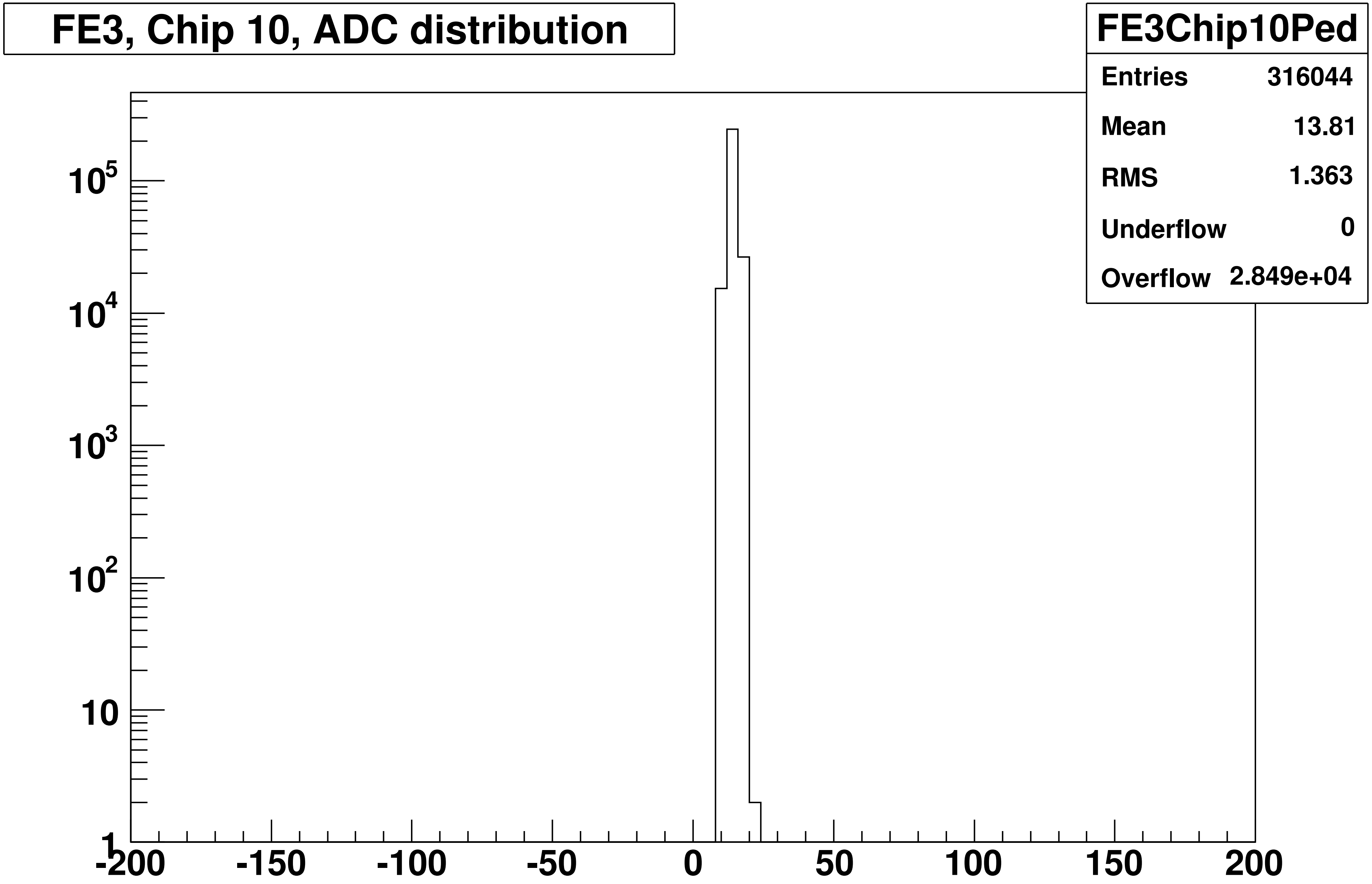
50
100
150
200


FE3, Chip 9, ADC distribution
FE3Chip09Sig
Entries 316044
Mean 1.913e+04
RMS 7.265
Underflow 2.876e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000


FE3, Chip 10, ADC distribution
FE3Chip10All
Entries 316044
Mean 1738
RMS 5477
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE3, Chip 10, ADC distribution
FE3Chip10Ped
Entries 316044
Mean 13.81
RMS 1.363
Underflow 0
Overflow 2.849e+04
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10^4
10^3
10^2
10
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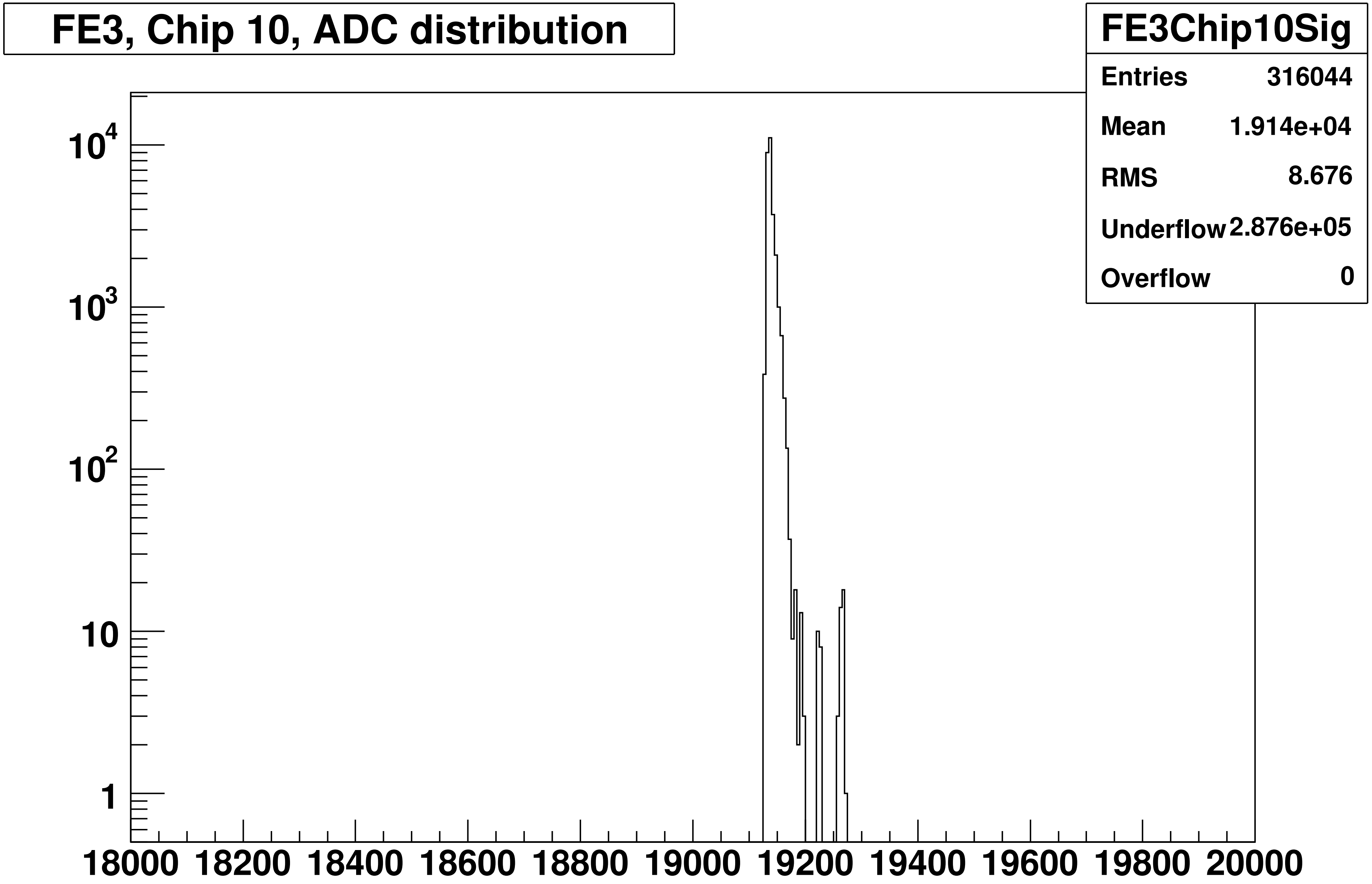
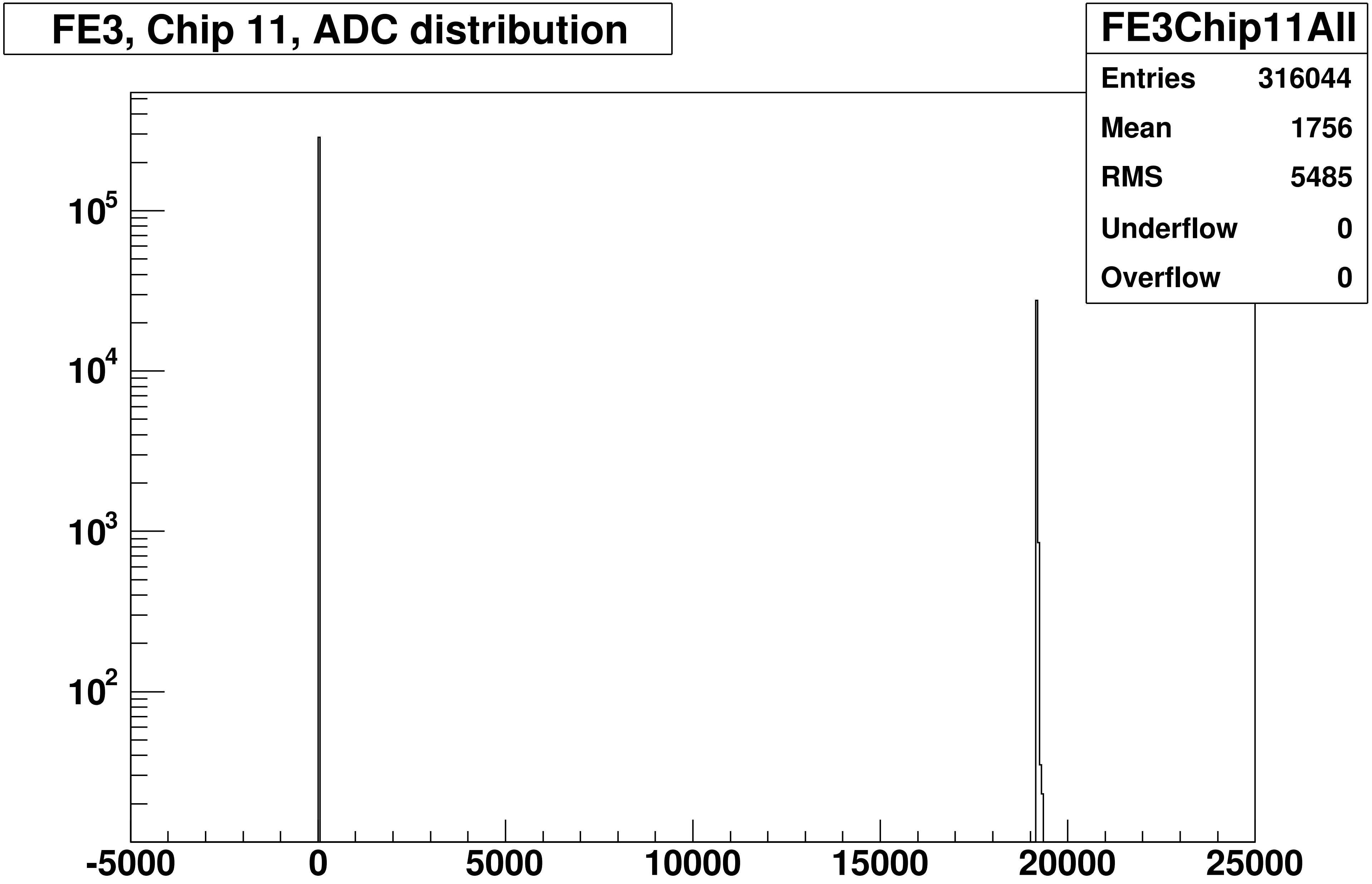
100
150
200


FE3, Chip 10, ADC distribution
FE3Chip10Sig
Entries 316044
Mean 1.914e+04
RMS 8.676
Underflow 2.876e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000


FE3, Chip 11, ADC distribution
FE3Chip11All
Entries 316044
Mean 1756
RMS 5485
Underflow 0
Overflow 0
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10^4
10^3
10^2
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0
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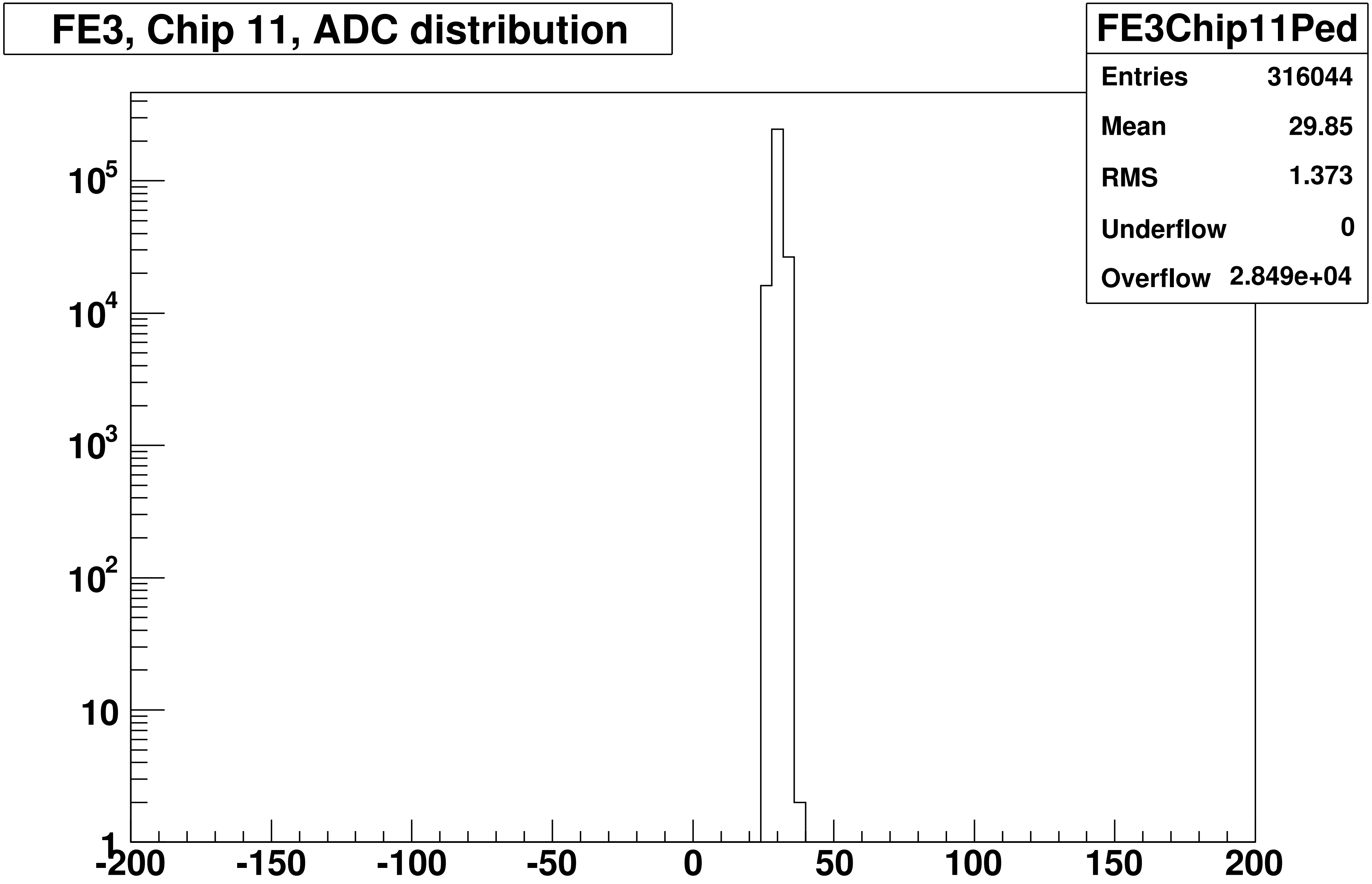
10000
15000
20000
25000



FE3, Chip 11, ADC distribution
FE3Chip11Ped
Entries 316044
Mean 29.85
RMS 1.373
Underflow 0
Overflow 2.849e+04
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10^4
10^3
10^2
10
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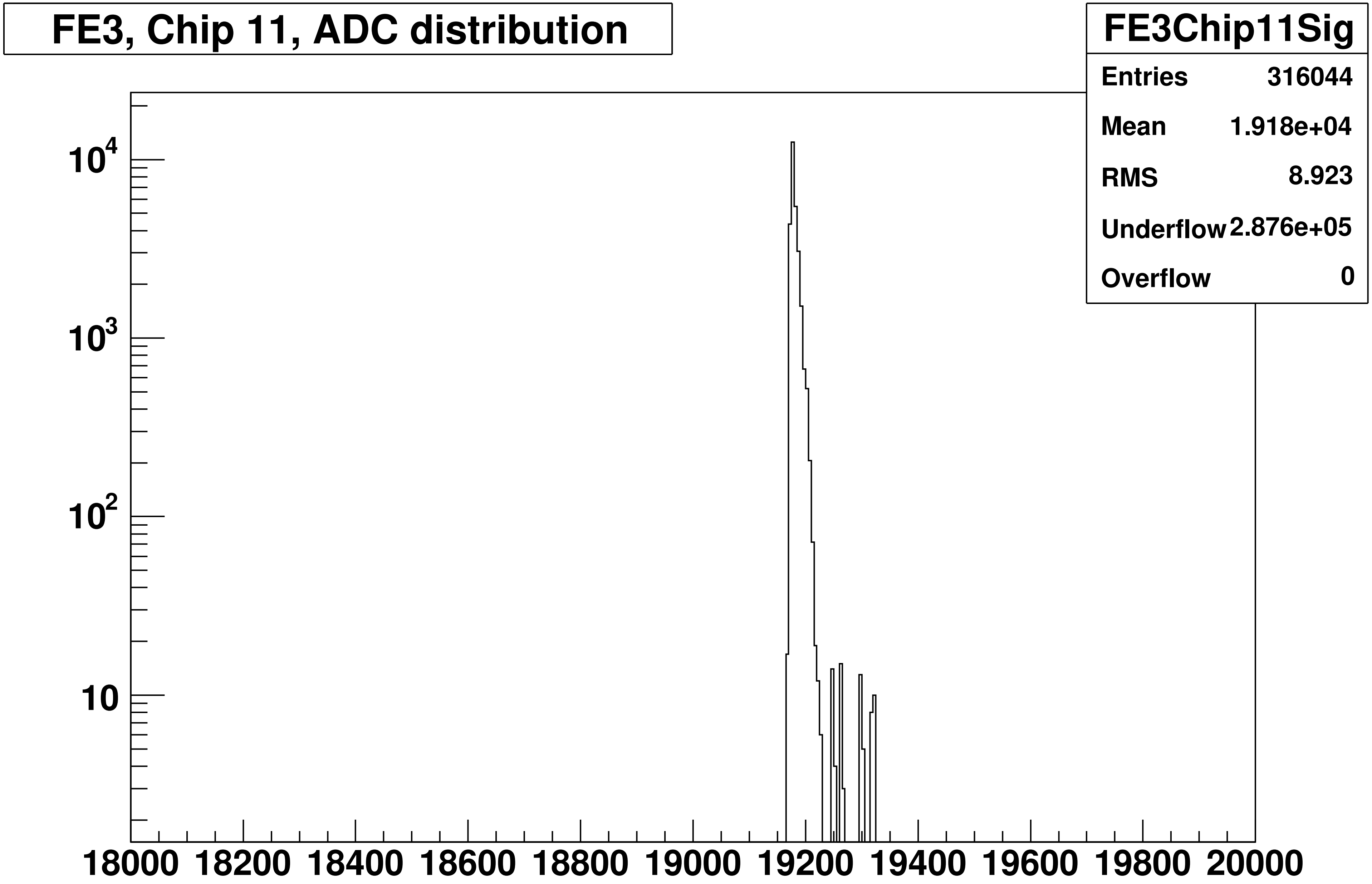
100
150
200


FE3, Chip 11, ADC distribution
FE3Chip11Sig
Entries 316044
Mean 1.918e+04
RMS 8.923
Underflow 2.876e+05
Overflow 0
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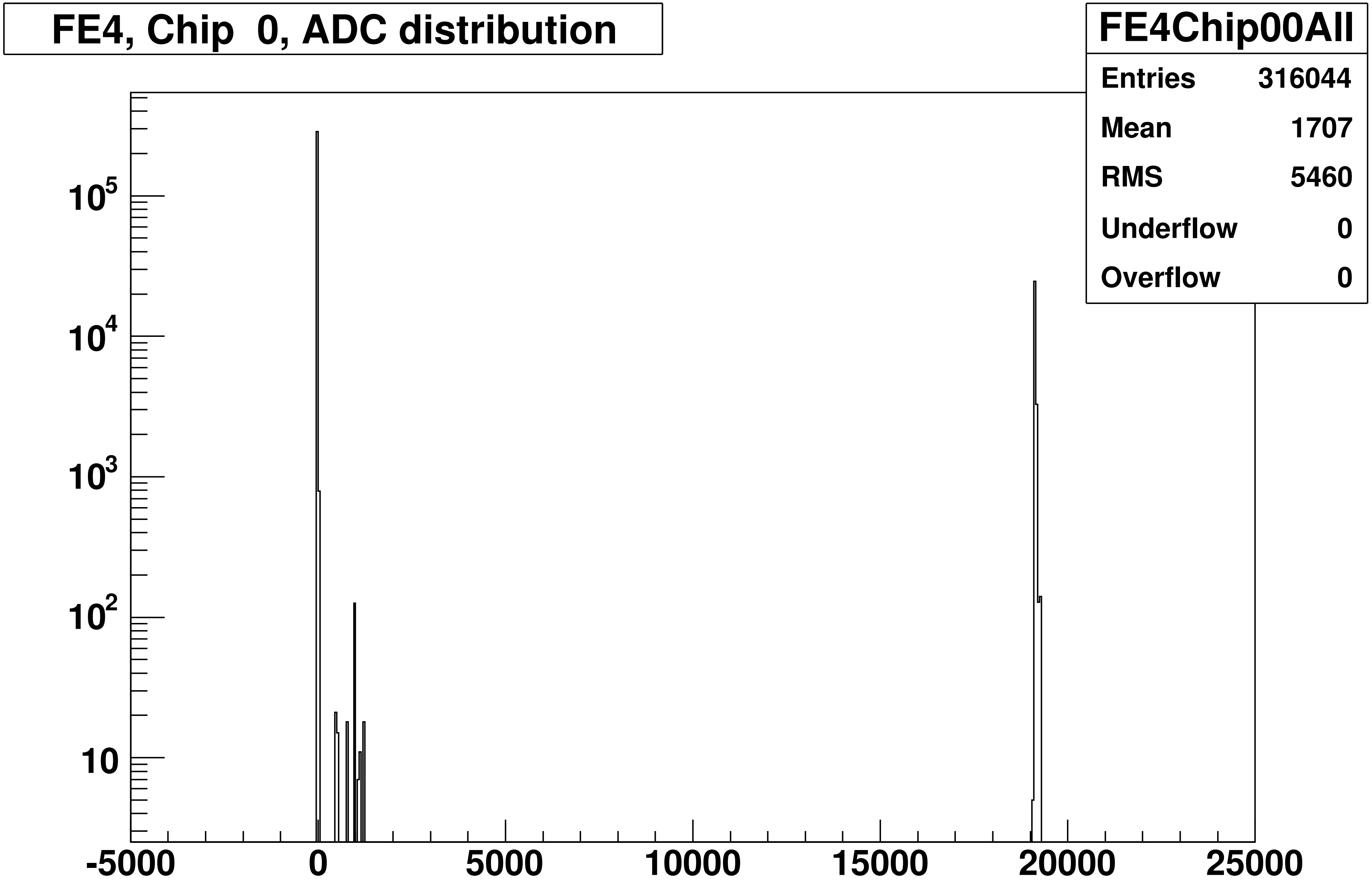
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE4, Chip 0, ADC distribution
FE4Chip00All
Entries 316044
Mean 1707
RMS 5460
Underflow 0
Overflow 0
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10^4
10^3
10^2
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-5000
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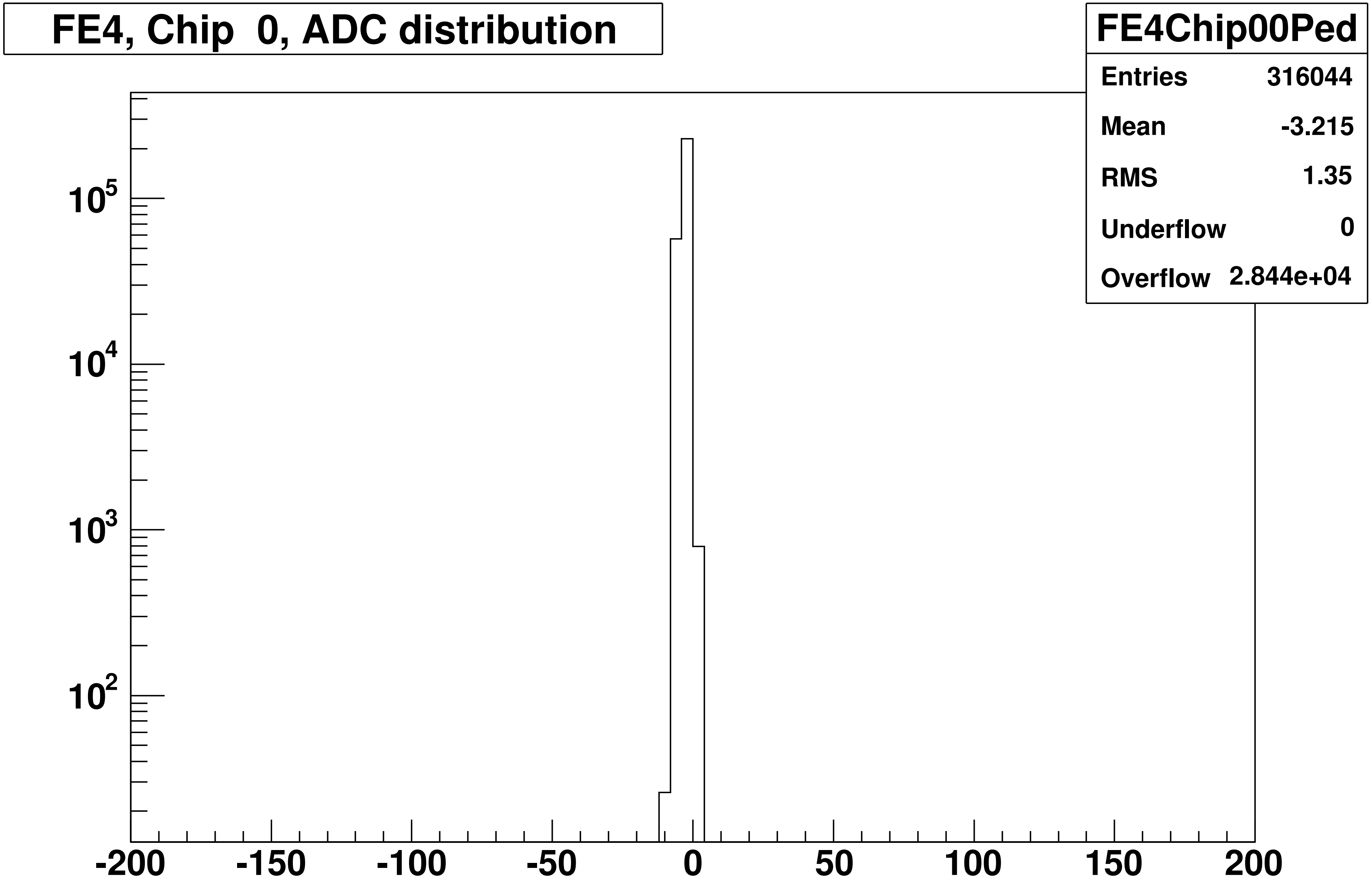
25000



FE4, Chip 0, ADC distribution
FE4Chip00Ped
Entries 316044
Mean -3.215
RMS 1.35
Underflow 0
Overflow 2.844e+04
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10^4
10^3
10^2
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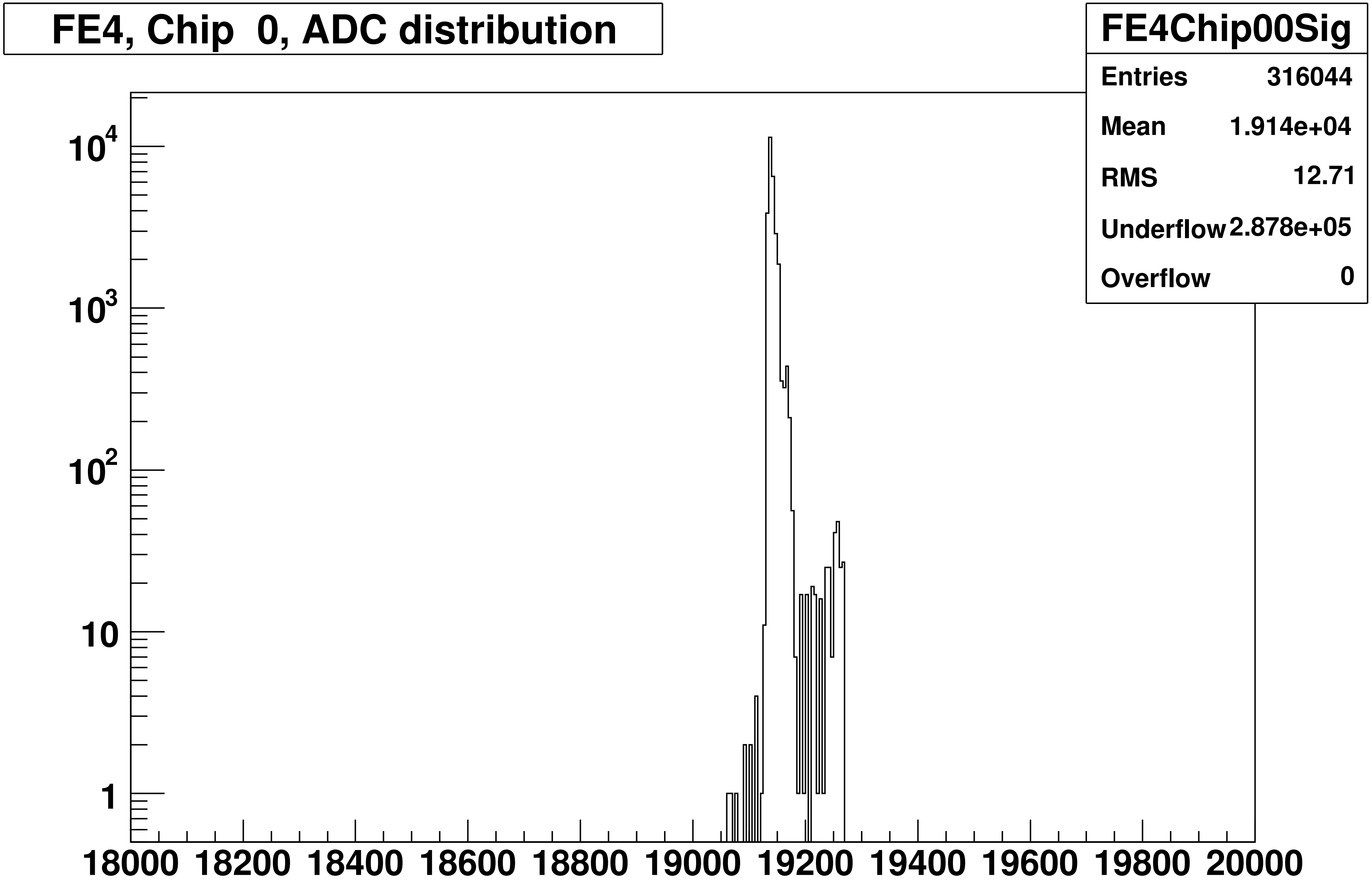
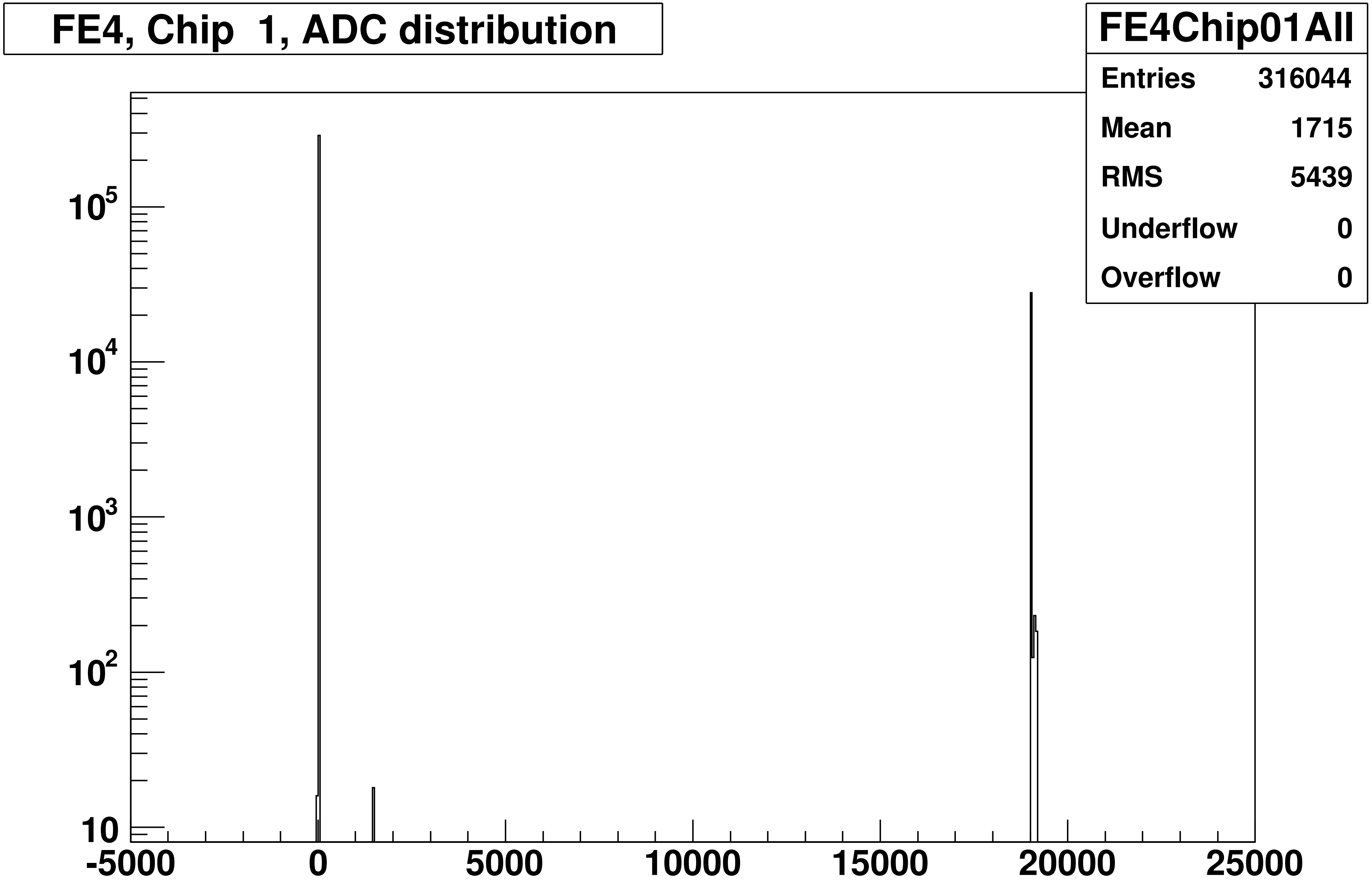
200



FE4, Chip 0, ADC distribution
FE4Chip00Sig
Entries 316044
Mean 1.914e+04
RMS 12.71
Underflow 2.878e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE4, Chip 1, ADC distribution
FE4Chip01All
Entries 316044
Mean 1715
RMS 5439
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
-5000
0
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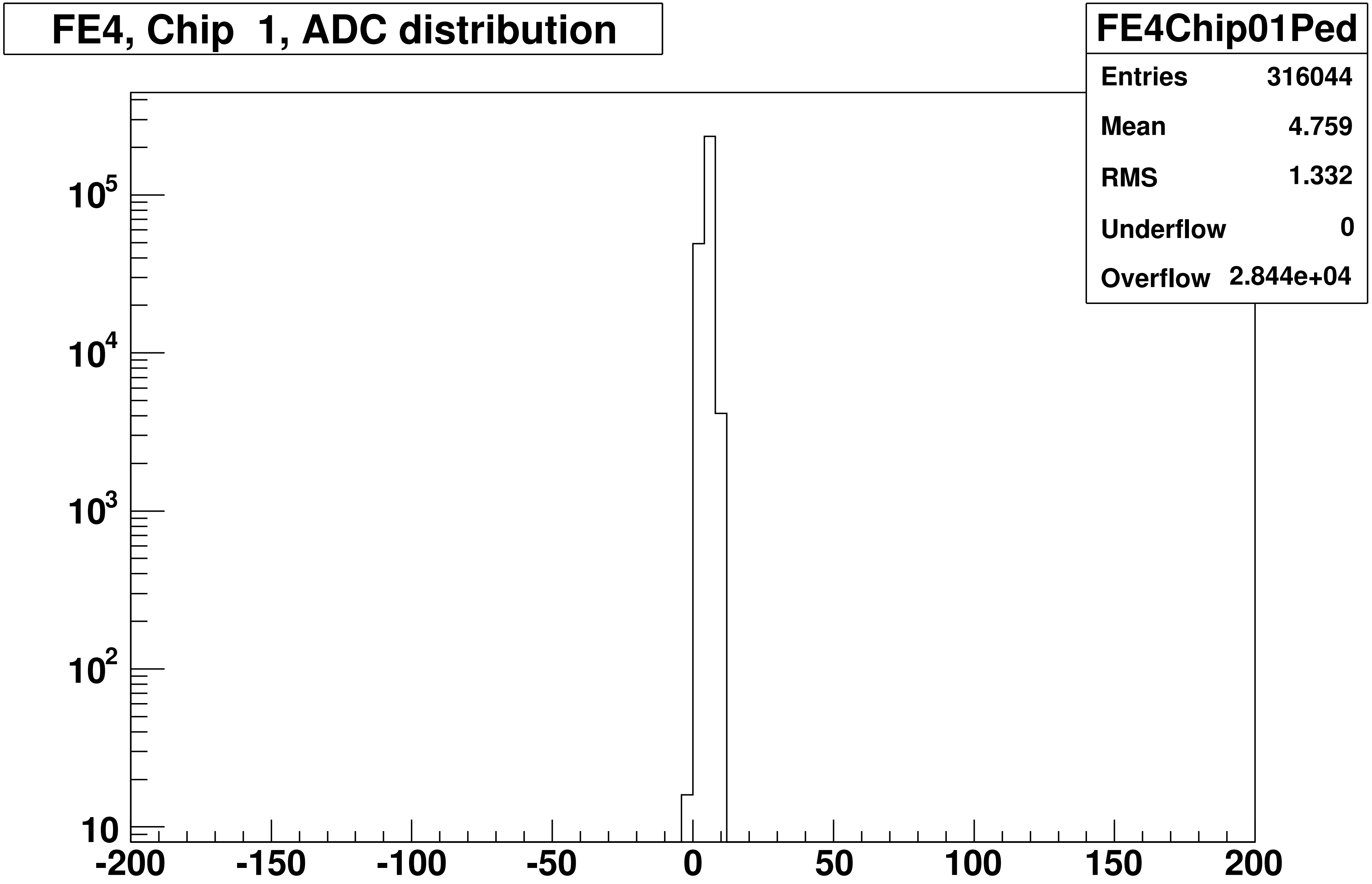
10000
15000
20000
25000



FE4, Chip 1, ADC distribution
FE4Chip01Ped
Entries 316044
Mean 4.759
RMS 1.332
Underflow 0
Overflow 2.844e+04
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10^4
10^3
10^2
10
-200
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-100
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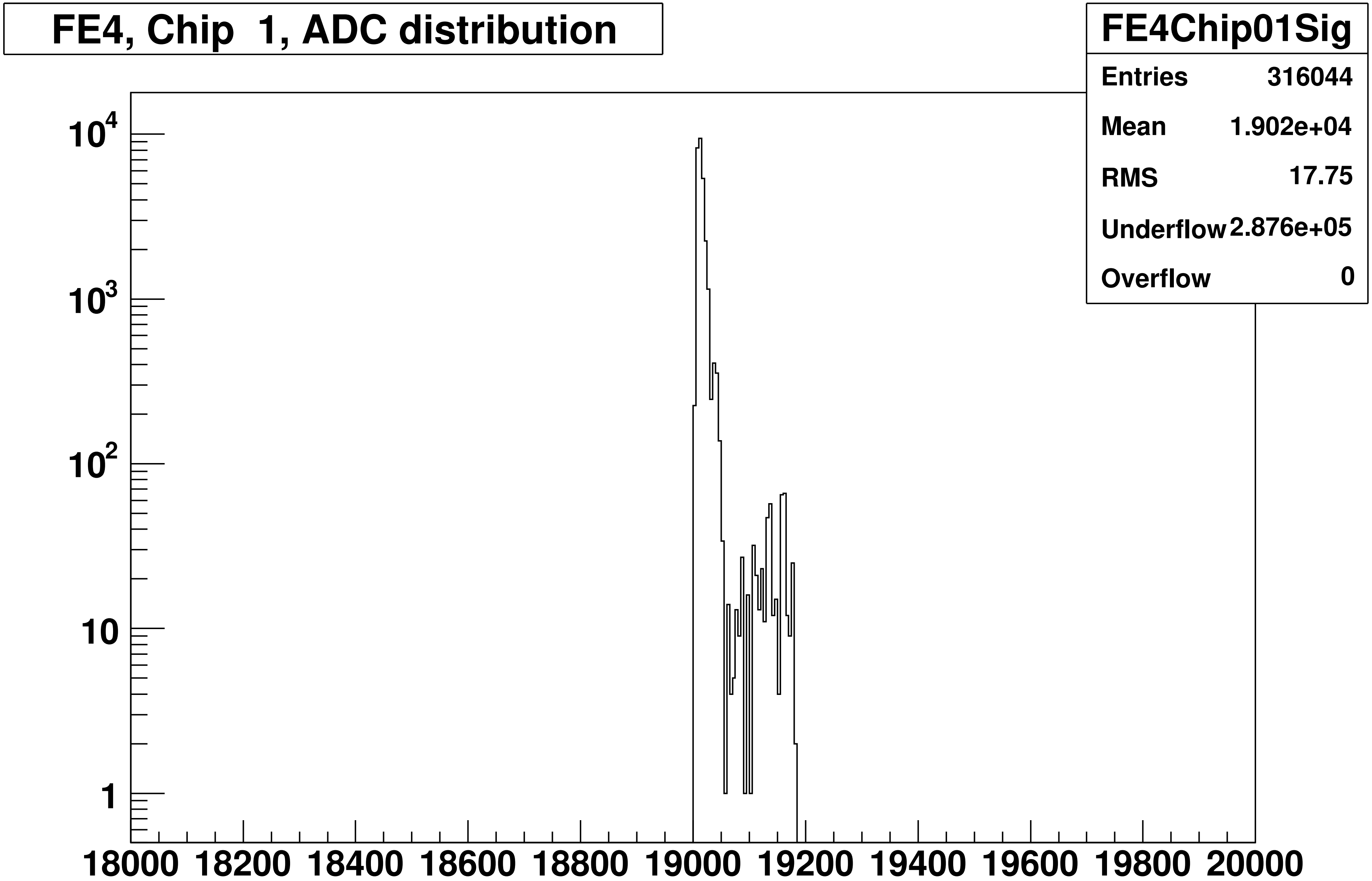
50
100
150
200



FE4, Chip 1, ADC distribution
FE4Chip01Sig
Entries 316044
Mean 1.902e+04
RMS 17.75
Underflow 2.876e+05
Overflow 0
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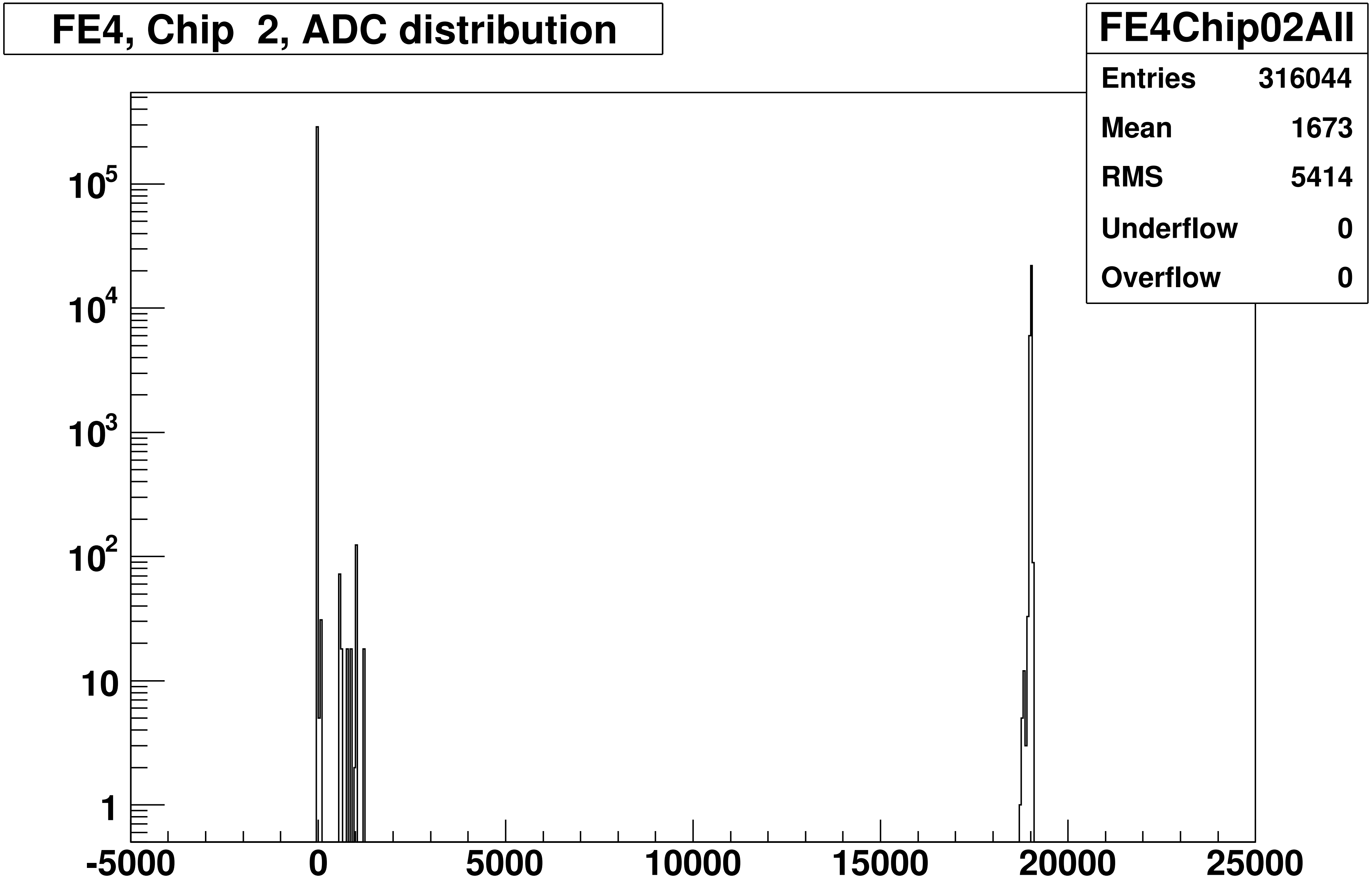
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE4, Chip 2, ADC distribution
FE4Chip02All
Entries 316044
Mean 1673
RMS 5414
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
1
-5000
0
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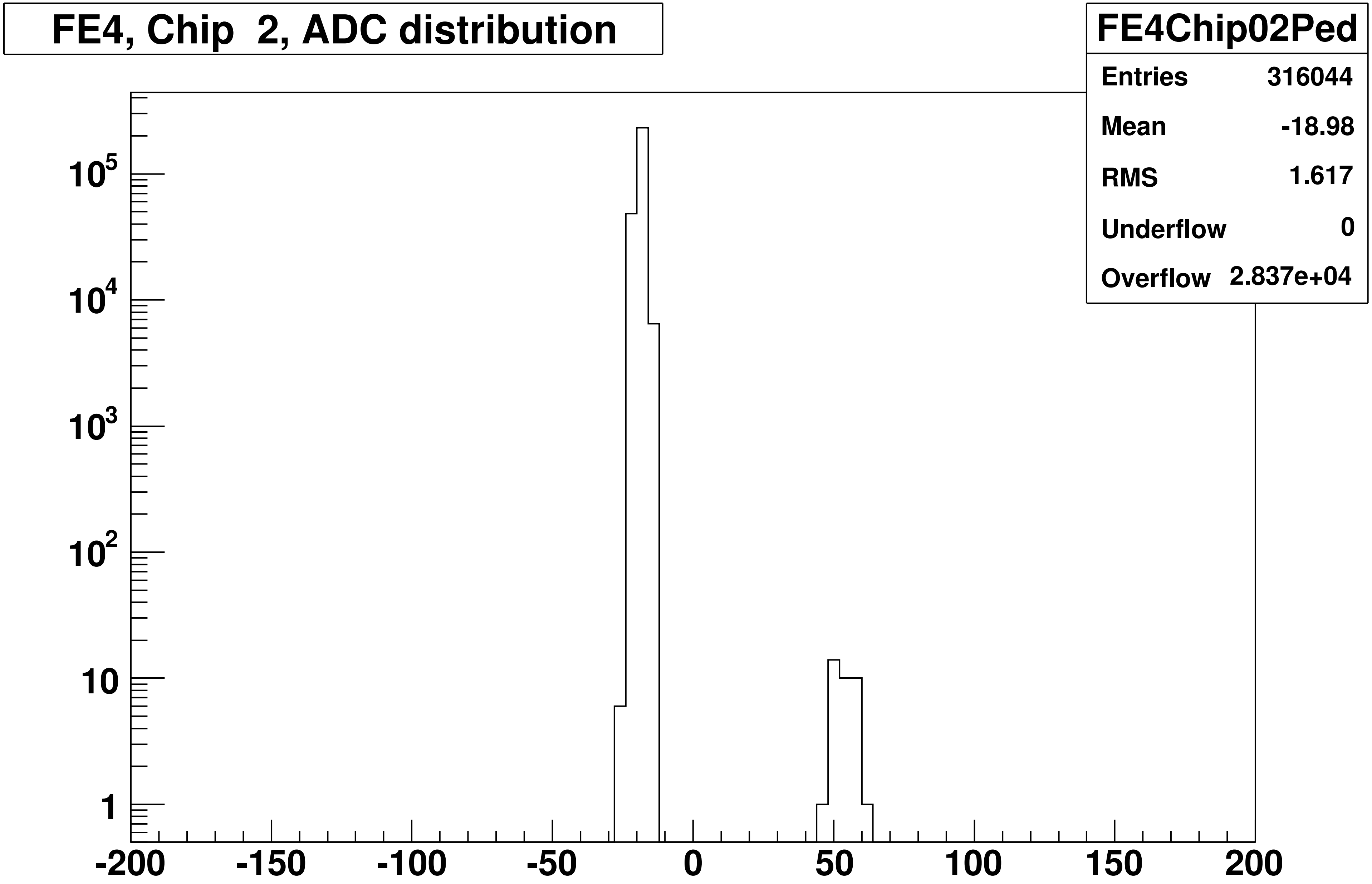
10000
15000
20000
25000



FE4, Chip 2, ADC distribution
FE4Chip02Ped
Entries 316044
Mean -18.98
RMS 1.617
Underflow 0
Overflow 2.837e+04
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10^4
10^3
10^2
10
1
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-100
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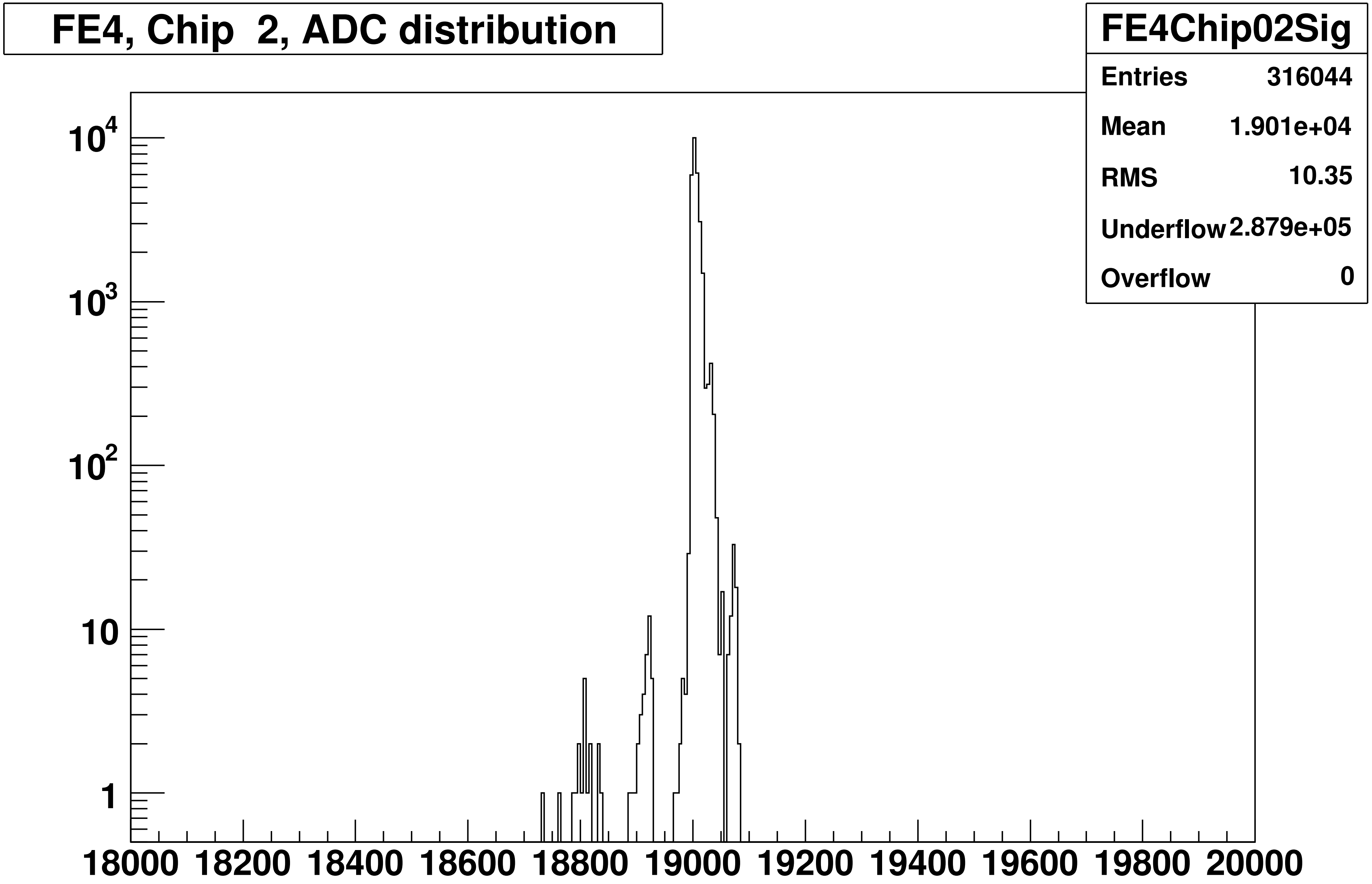
50
100
150
200



FE4, Chip 2, ADC distribution
FE4Chip02Sig
Entries 316044
Mean 1.901e+04
RMS 10.35
Underflow 2.879e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
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19000
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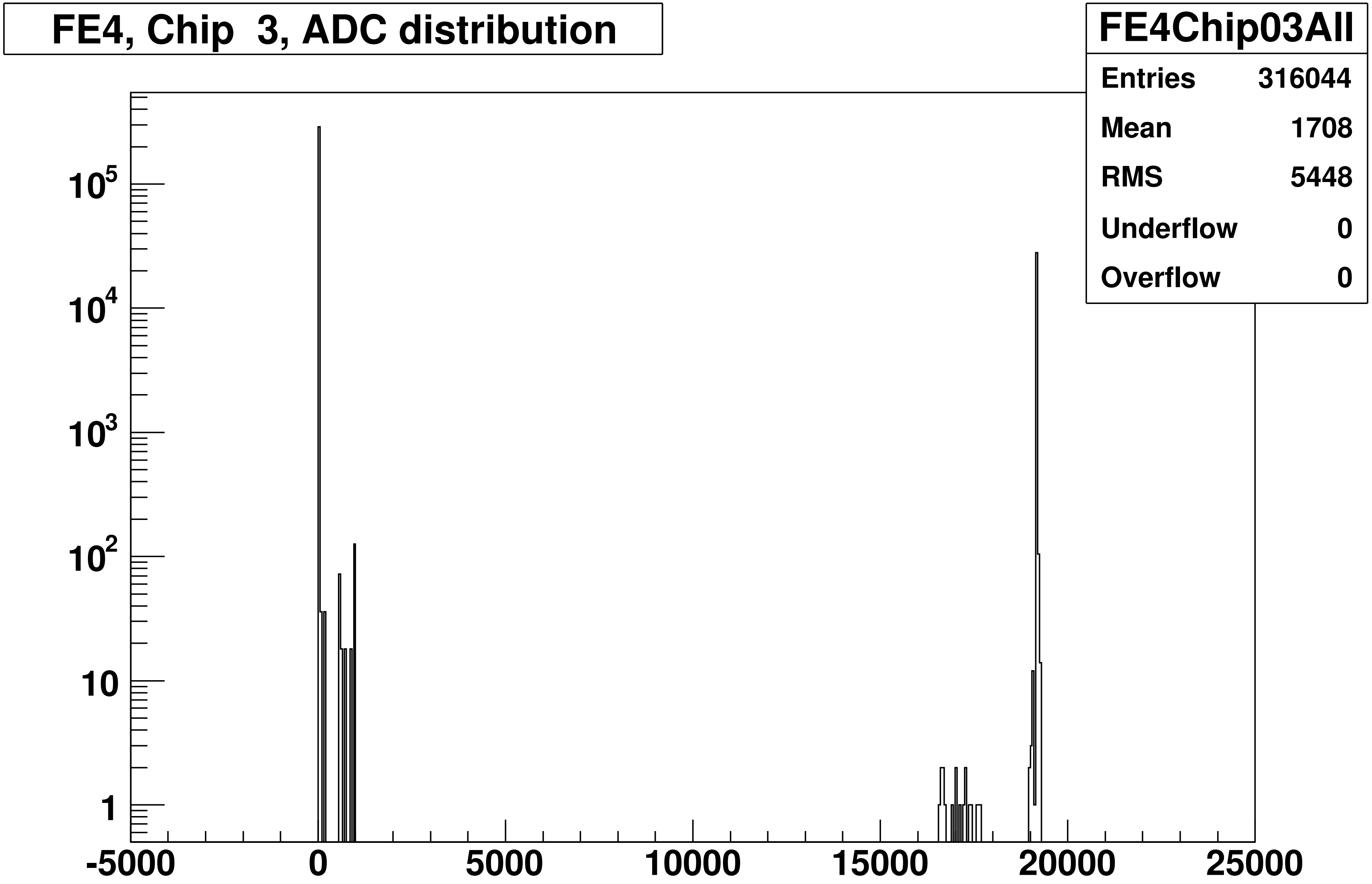
19600
19800
20000



FE4, Chip 3, ADC distribution
FE4Chip03All
Entries 316044
Mean 1708
RMS 5448
Underflow 0
Overflow 0
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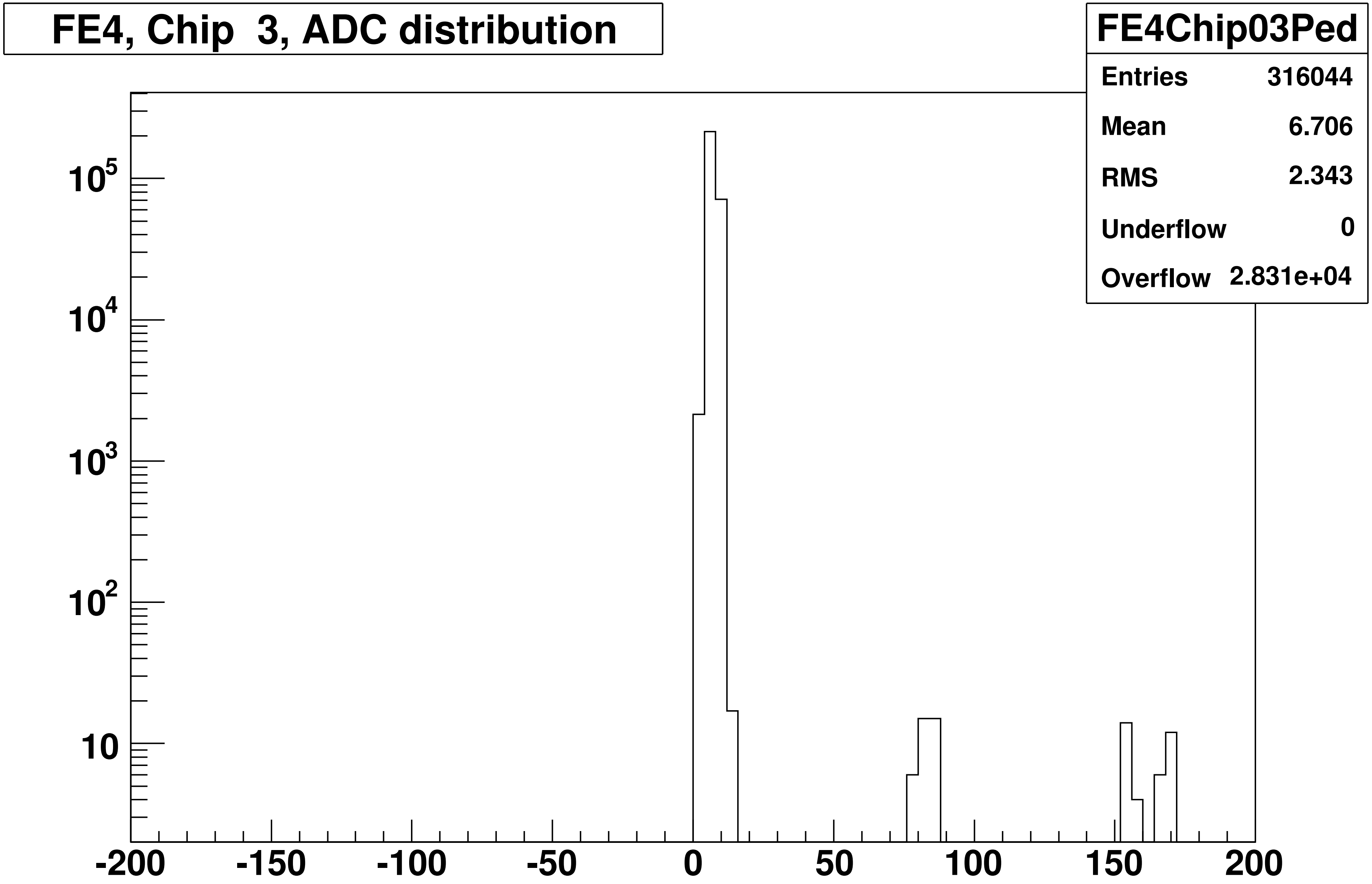
10
10^2
10^3
10^4
10^5
-5000
0
5000
10000
15000
20000
25000



FE4, Chip 3, ADC distribution
FE4Chip03Ped
Entries 316044
Mean 6.706
RMS 2.343
Underflow 0
Overflow 2.831e+04
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10^4
10^3
10^2
10
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-100
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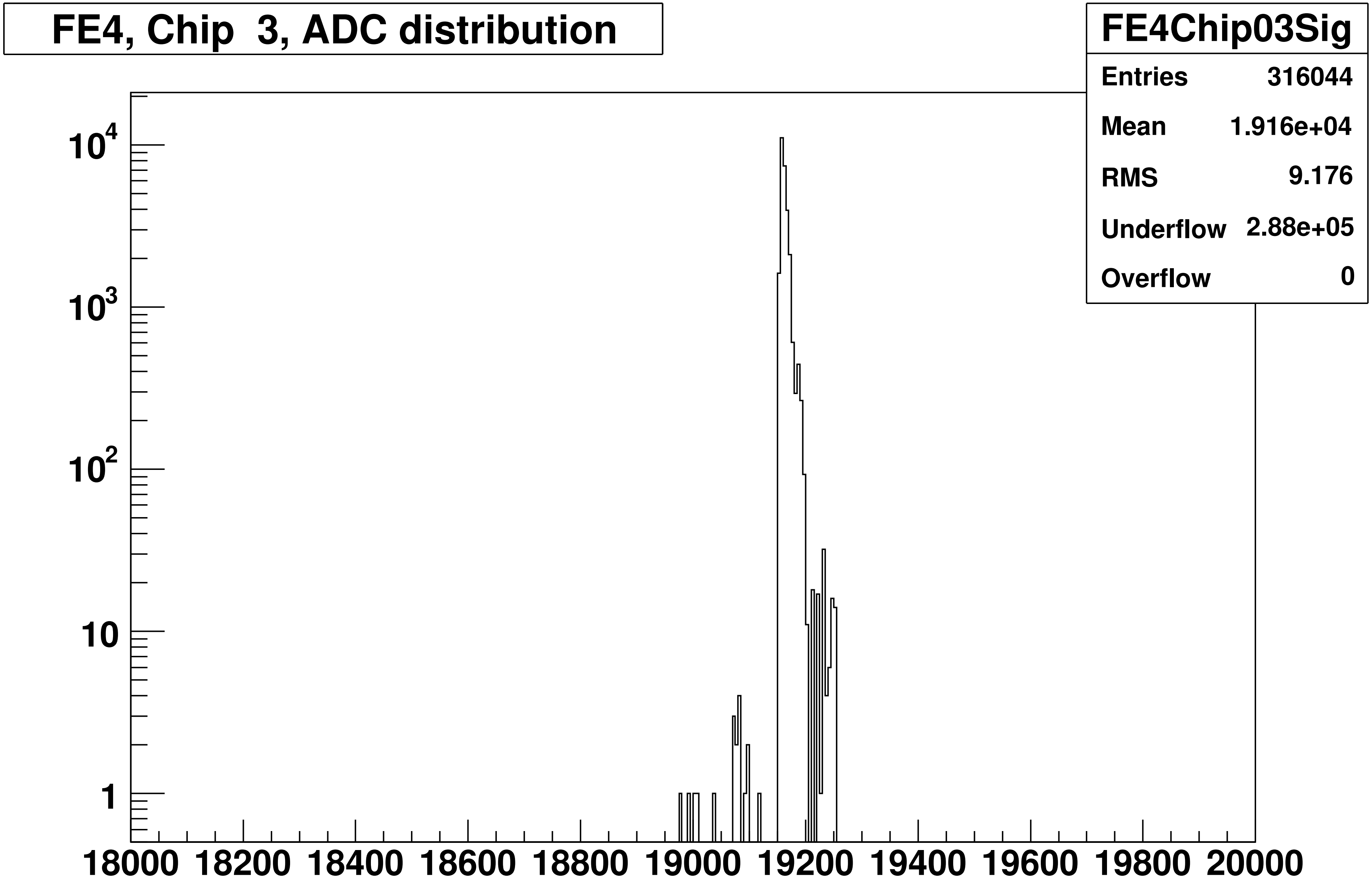
0
50
100
150
200


FE4, Chip 3, ADC distribution
FE4Chip03Sig
Entries 316044
Mean 1.916e+04
RMS 9.176
Underflow 2.88e+05
Overflow 0
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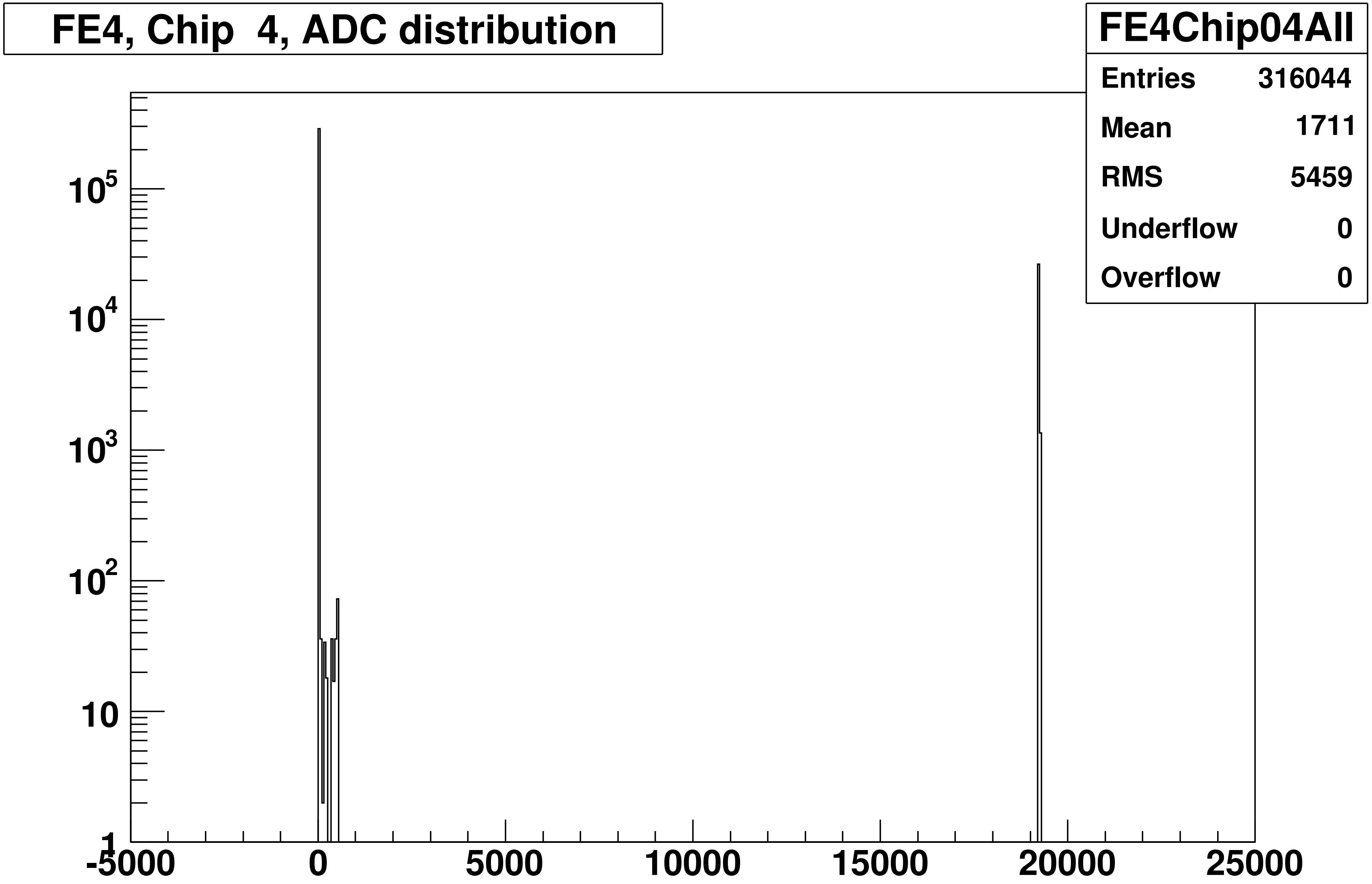
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE4, Chip 4, ADC distribution
FE4Chip04All
Entries 316044
Mean 1711
RMS 5459
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
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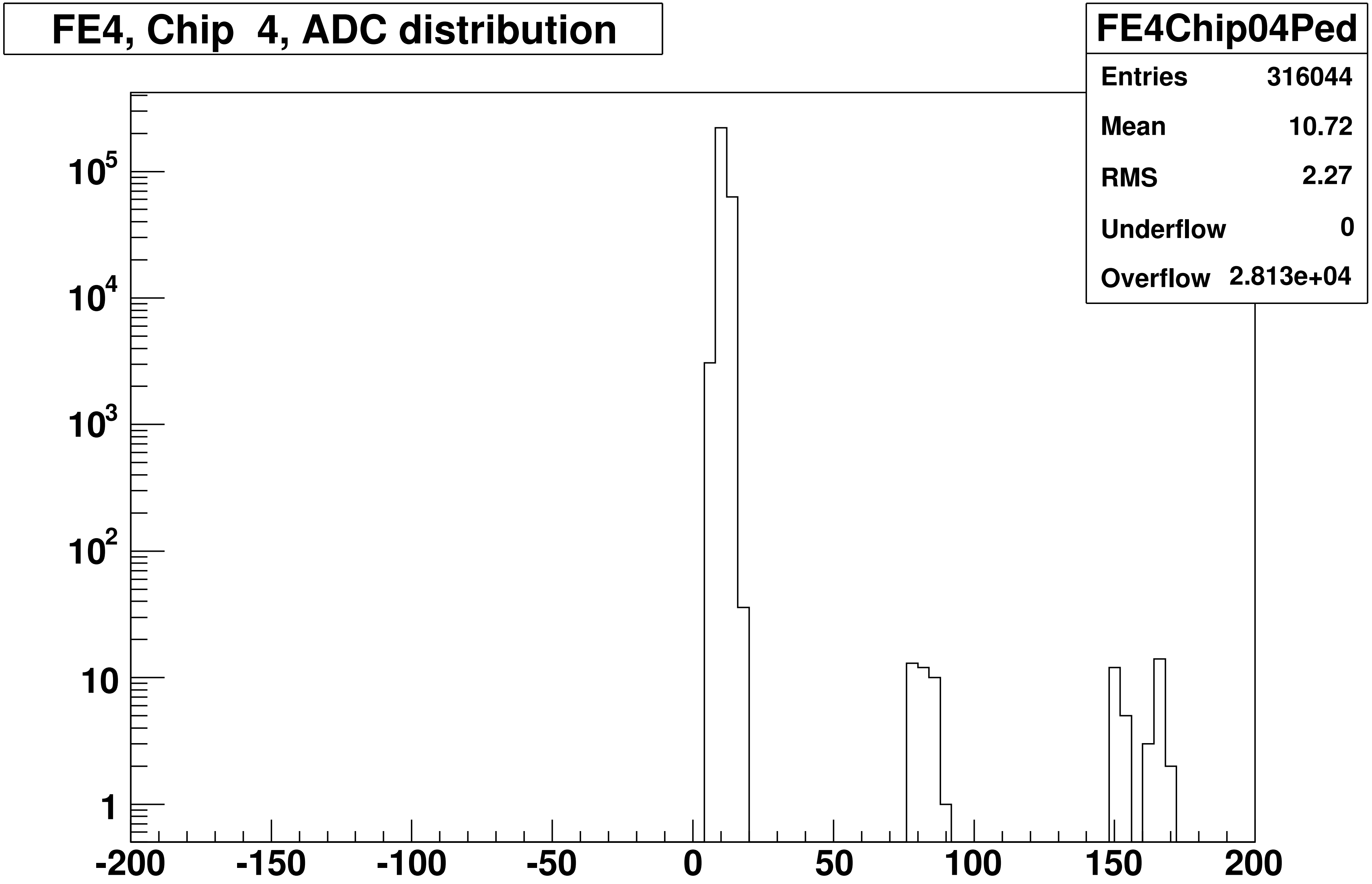
10000
15000
20000
25000


FE4, Chip 4, ADC distribution
FE4Chip04Ped
Entries 316044
Mean 10.72
RMS 2.27
Underflow 0
Overflow 2.813e+04
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10^4
10^3
10^2
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1
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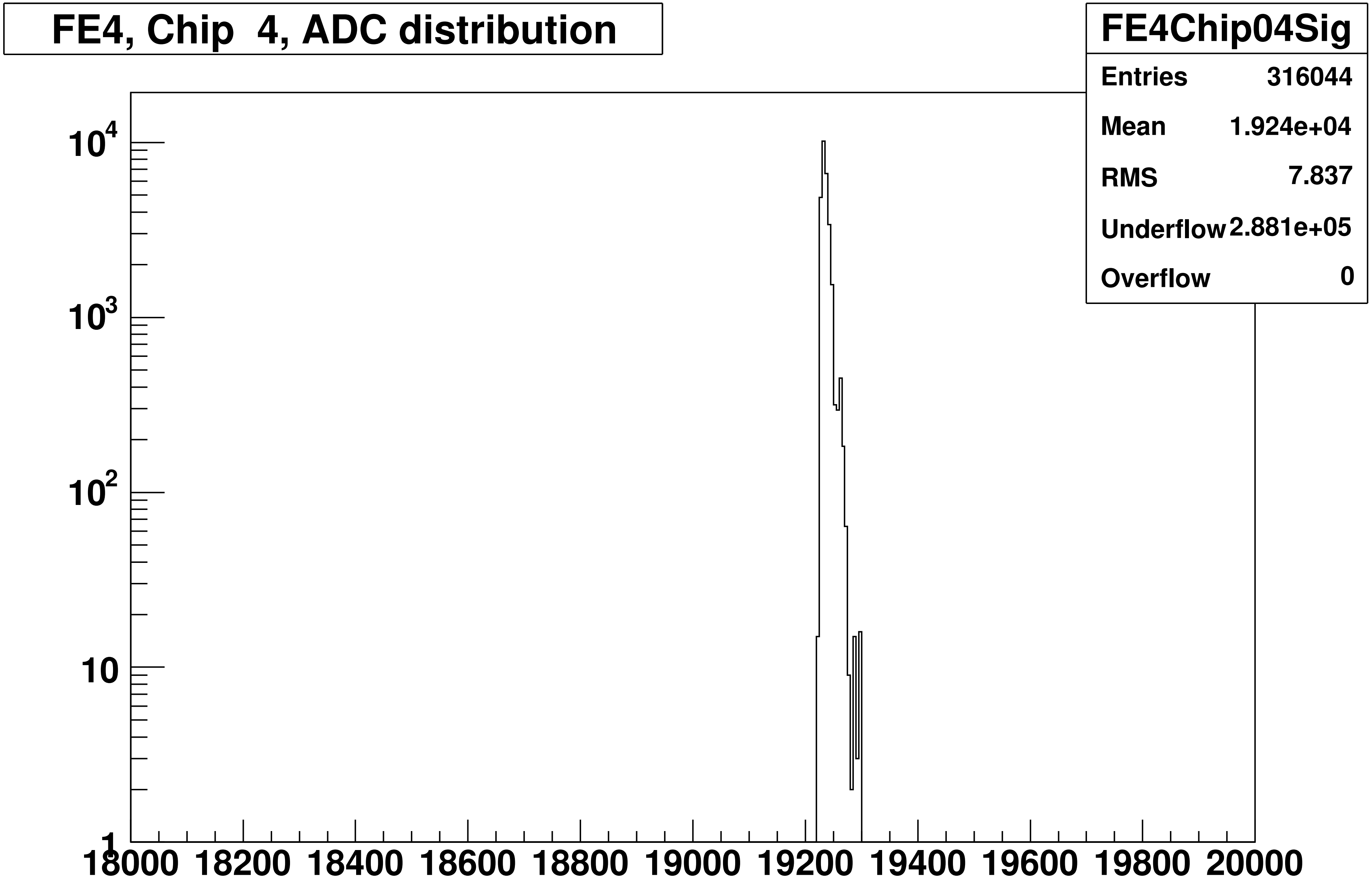
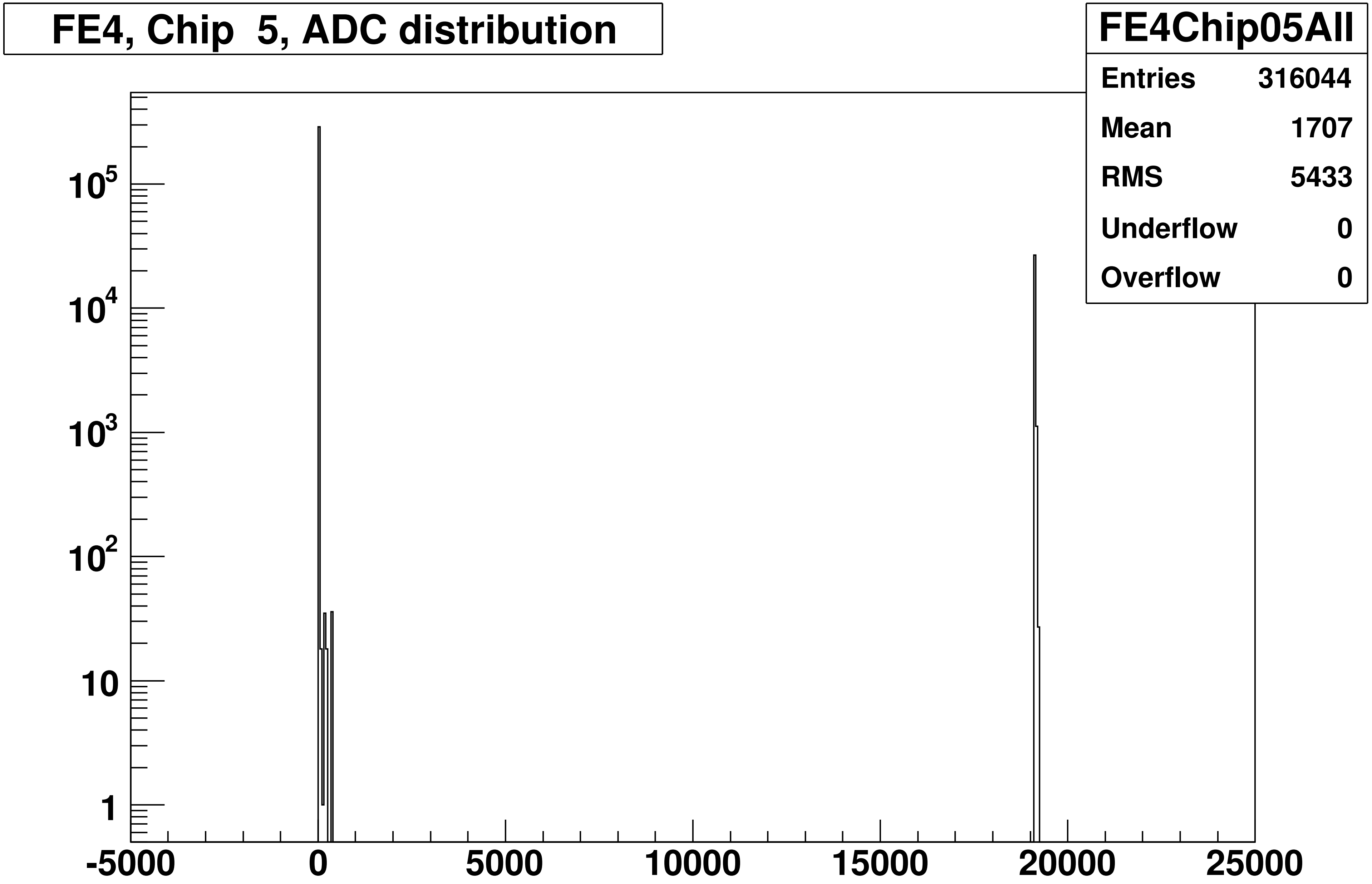
100
150
200



FE4, Chip 4, ADC distribution
FE4Chip04Sig
Entries 316044
Mean 1.924e+04
RMS 7.837
Underflow 2.881e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE4, Chip 5, ADC distribution
FE4Chip05All
Entries 316044
Mean 1707
RMS 5433
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
1
-5000
0
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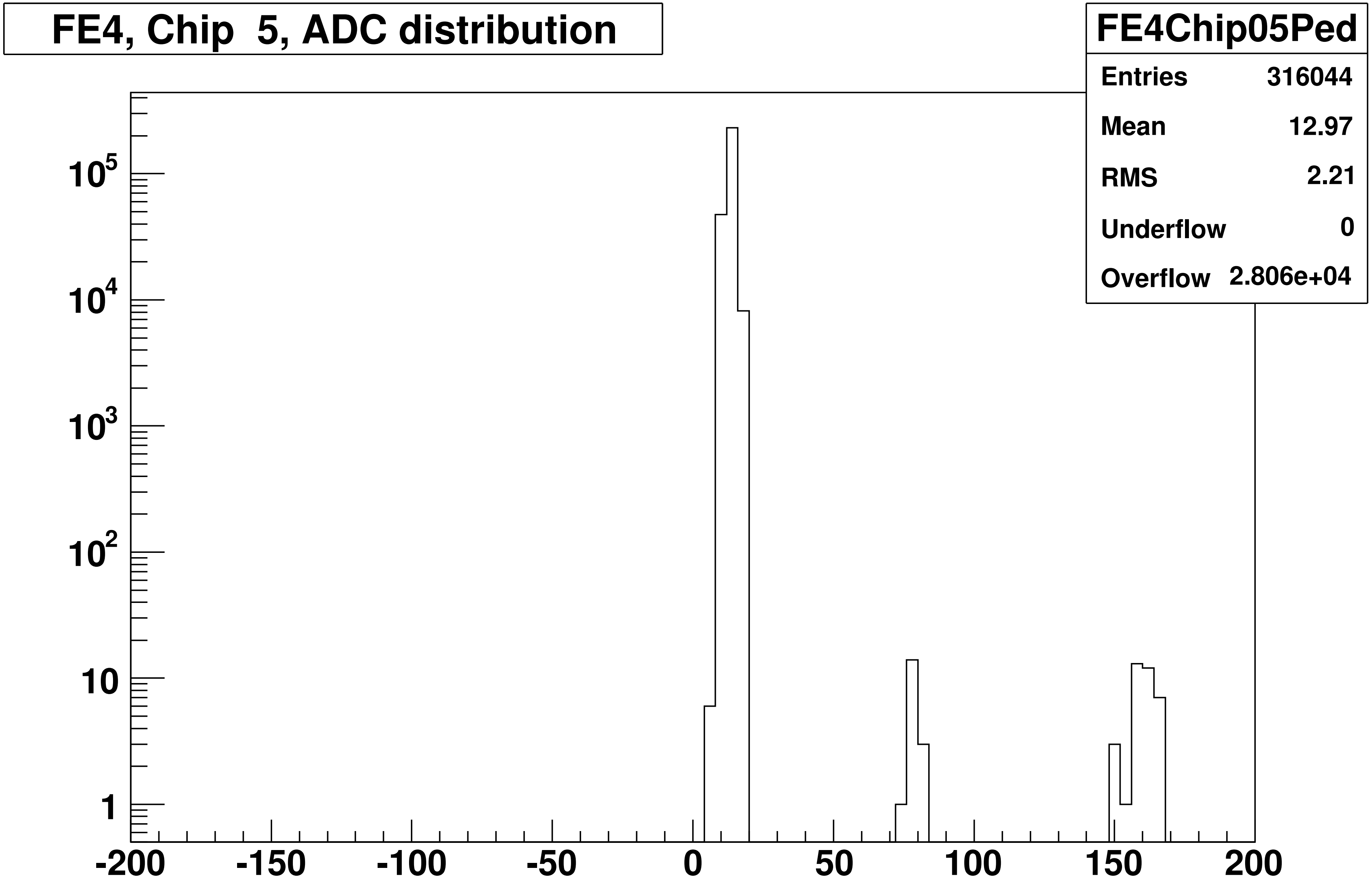
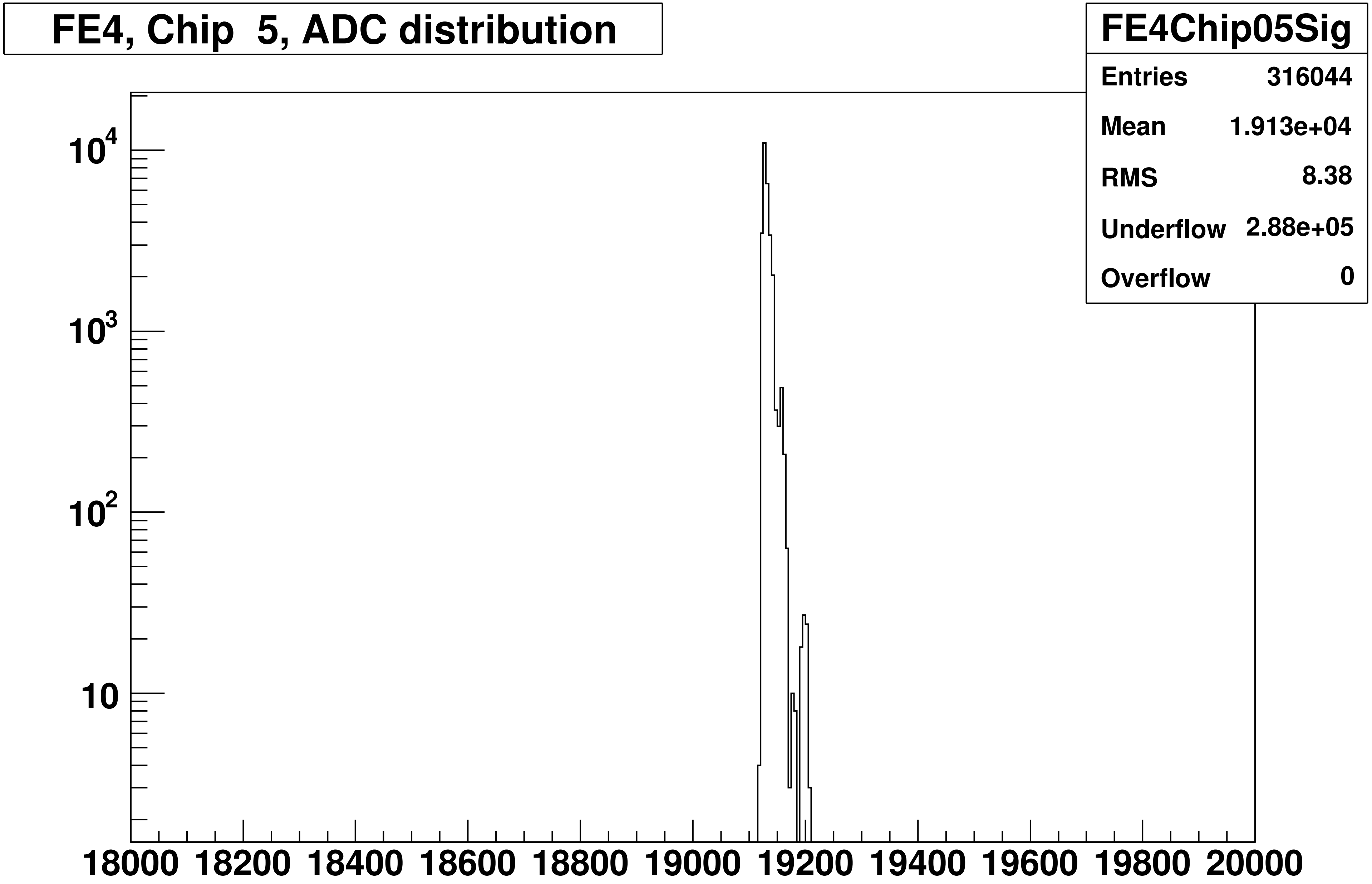
10000
15000
20000
25000



FE4, Chip 5, ADC distribution
FE4Chip05Ped
Entries 316044
Mean 12.97
RMS 2.21
Underflow 0
Overflow 2.806e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
200



FE4, Chip 5, ADC distribution
FE4Chip05Sig
Entries 316044
Mean 1.913e+04
RMS 8.38
Underflow 2.88e+05
Overflow 0
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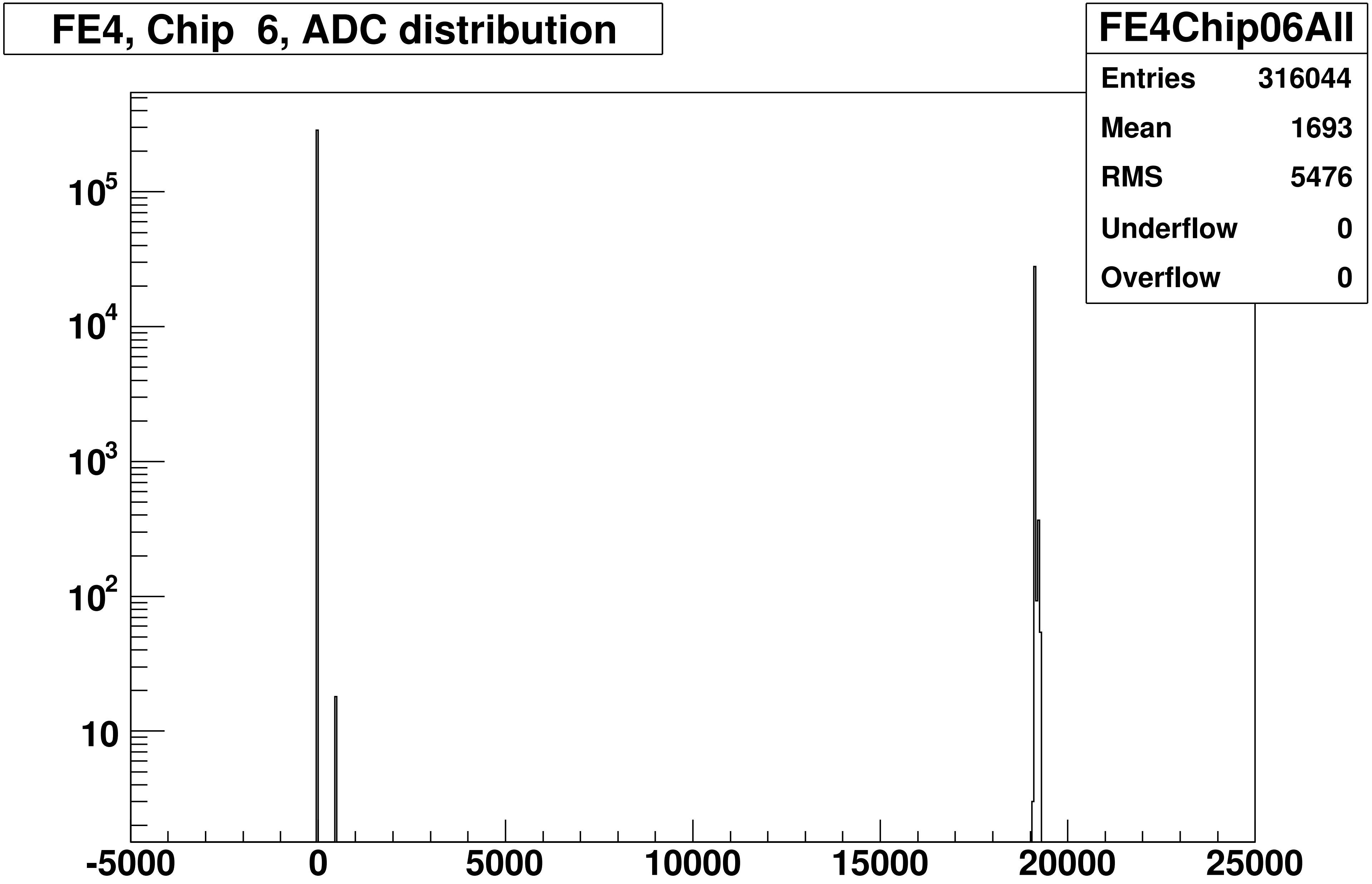
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE4, Chip 6, ADC distribution
FE4Chip06All
Entries 316044
Mean 1693
RMS 5476
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
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-5000
0
5000
10000
15000
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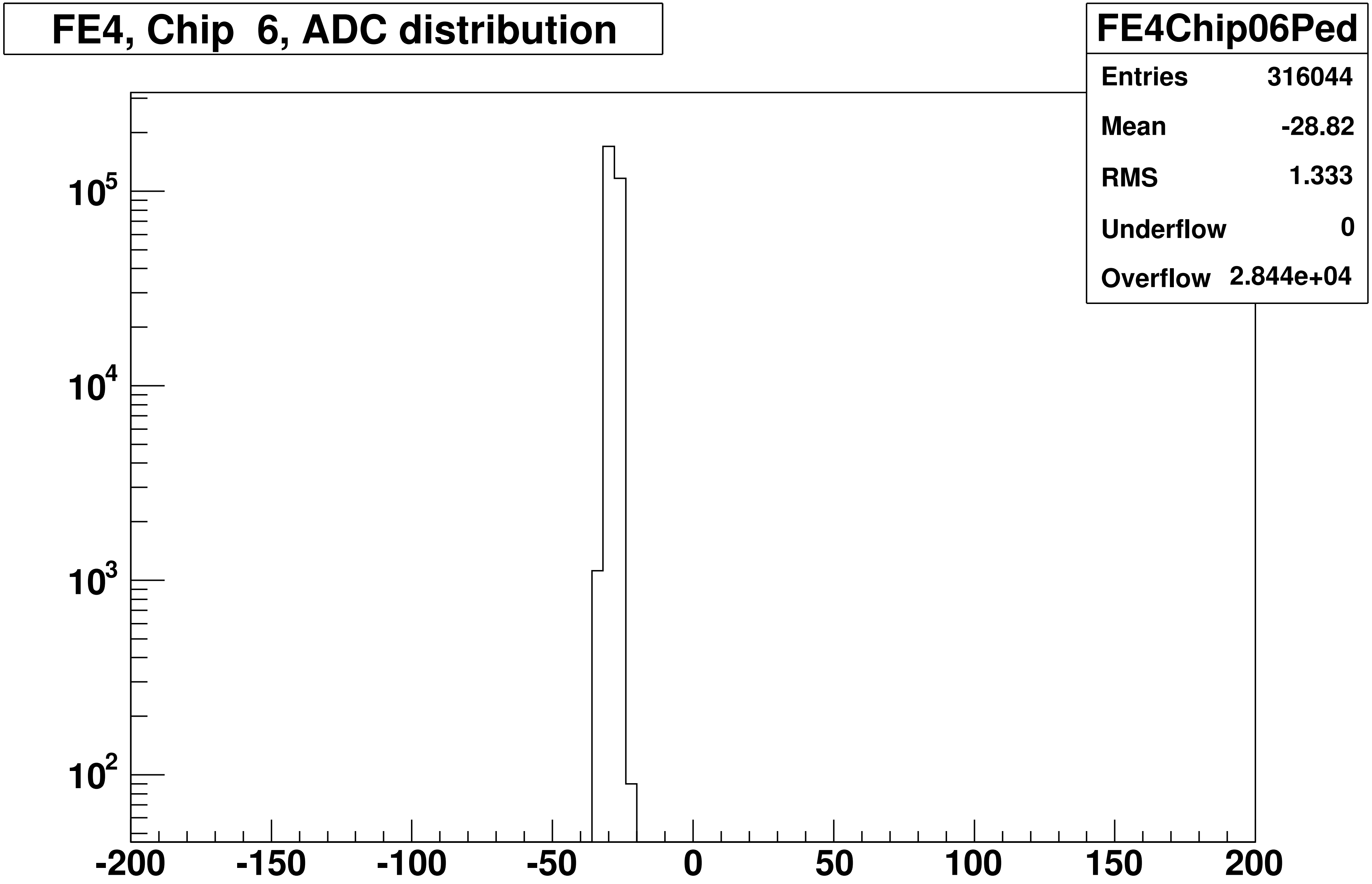
FE4, Chip 6, ADC distribution
FE4Chip06Ped
Entries 316044
Mean -28.82
RMS 1.333
Underflow 0
Overflow 2.844e+04
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10^4
10^3
10^2
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-100
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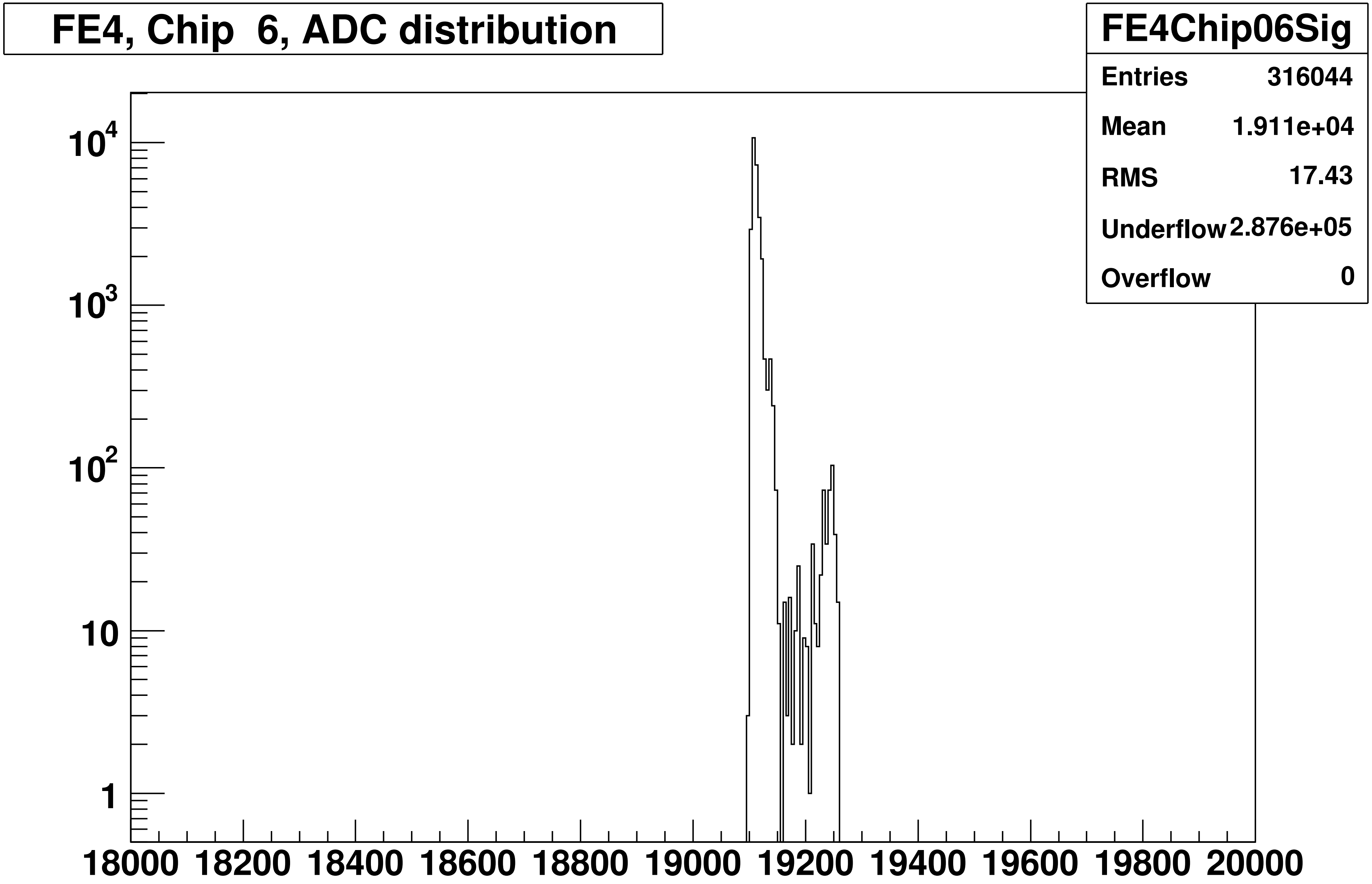
0
50
100
150
200


FE4, Chip 6, ADC distribution
FE4Chip06Sig
Entries 316044
Mean 1.911e+04
RMS 17.43
Underflow 2.876e+05
Overflow 0
10^4
10^3
10^2
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1
18000
18200
18400
18600
18800
19000
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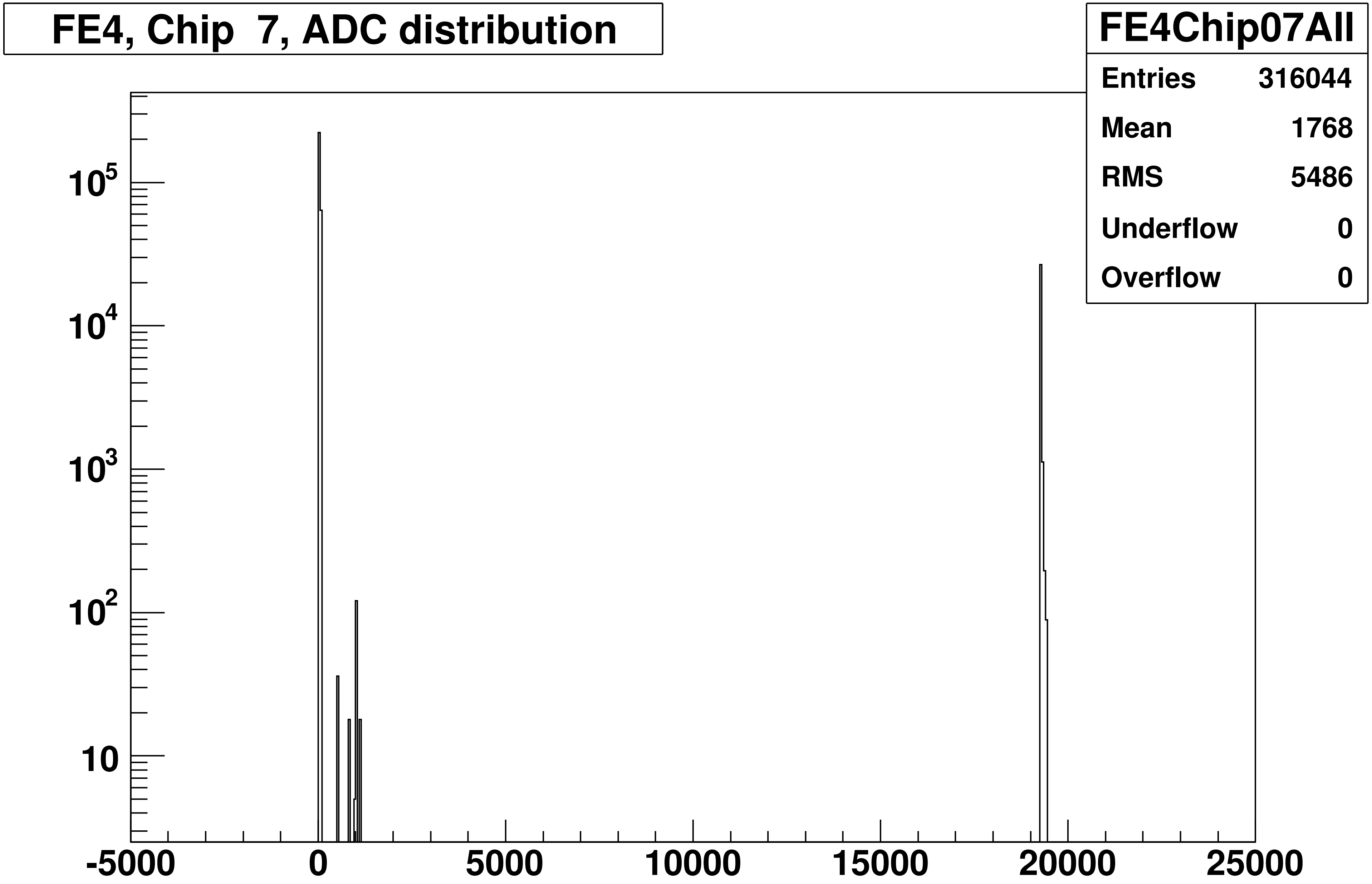
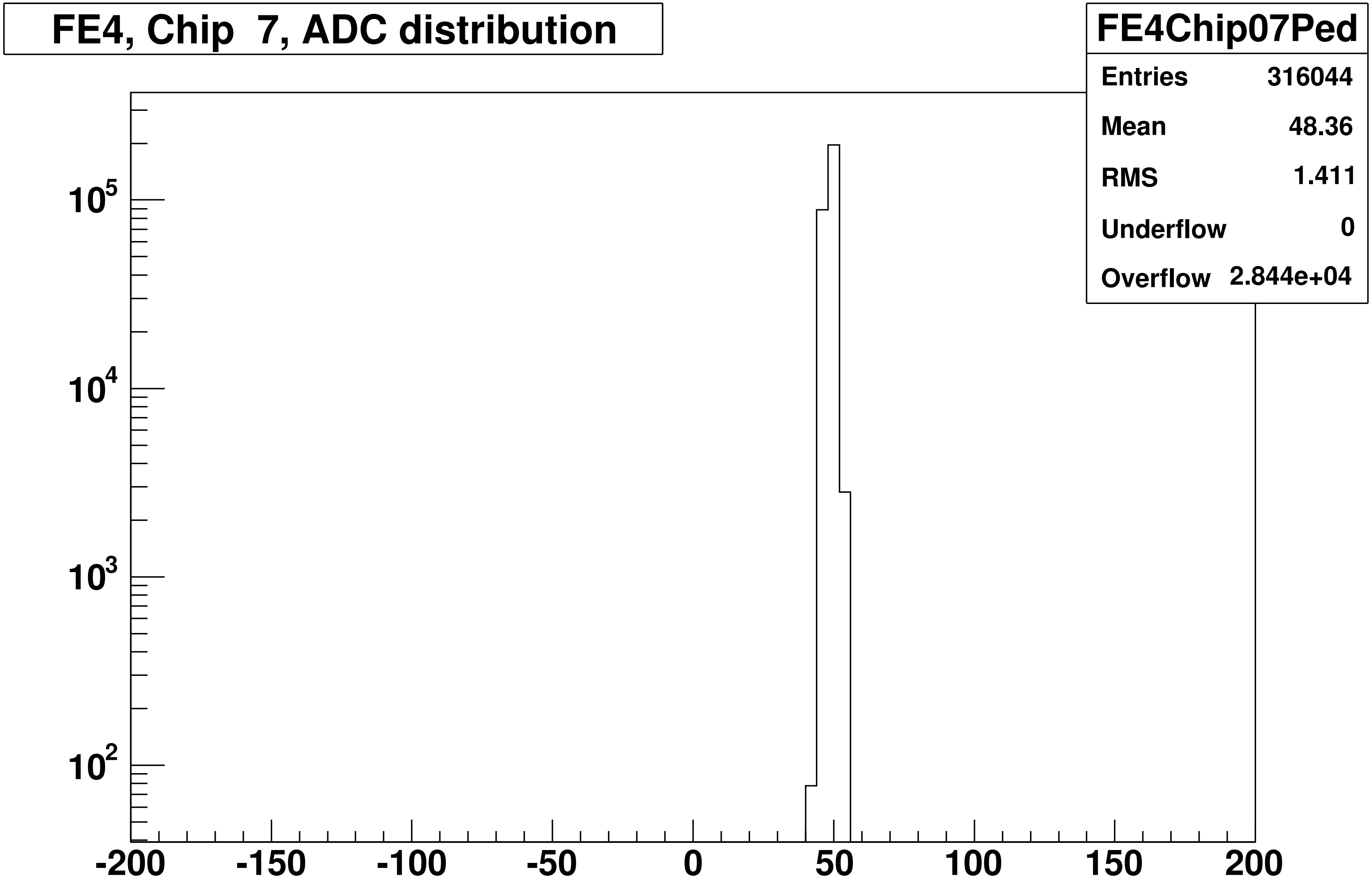
19400
19600
19800
20000



FE4, Chip 7, ADC distribution
FE4Chip07All
Entries 316044
Mean 1768
RMS 5486
Underflow 0
Overflow 0
10
10^2
10^3
10^4
10^5
-5000
0
5000
10000
15000
20000
25000



FE4, Chip 7, ADC distribution
FE4Chip07Ped
Entries 316044
Mean 48.36
RMS 1.411
Underflow 0
Overflow 2.844e+04
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10^4
10^3
10^2
-200
-150
-100
-50
0
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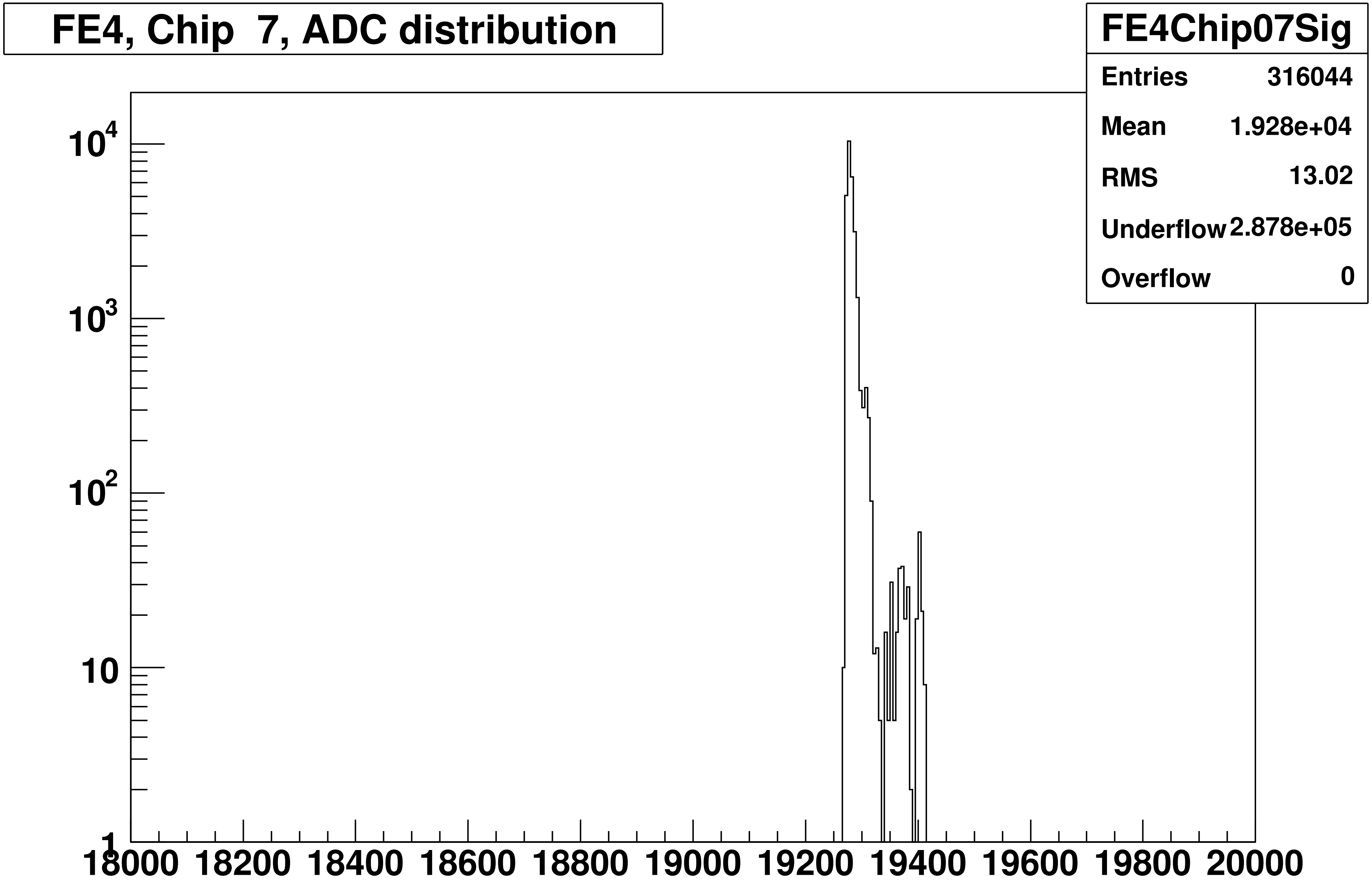
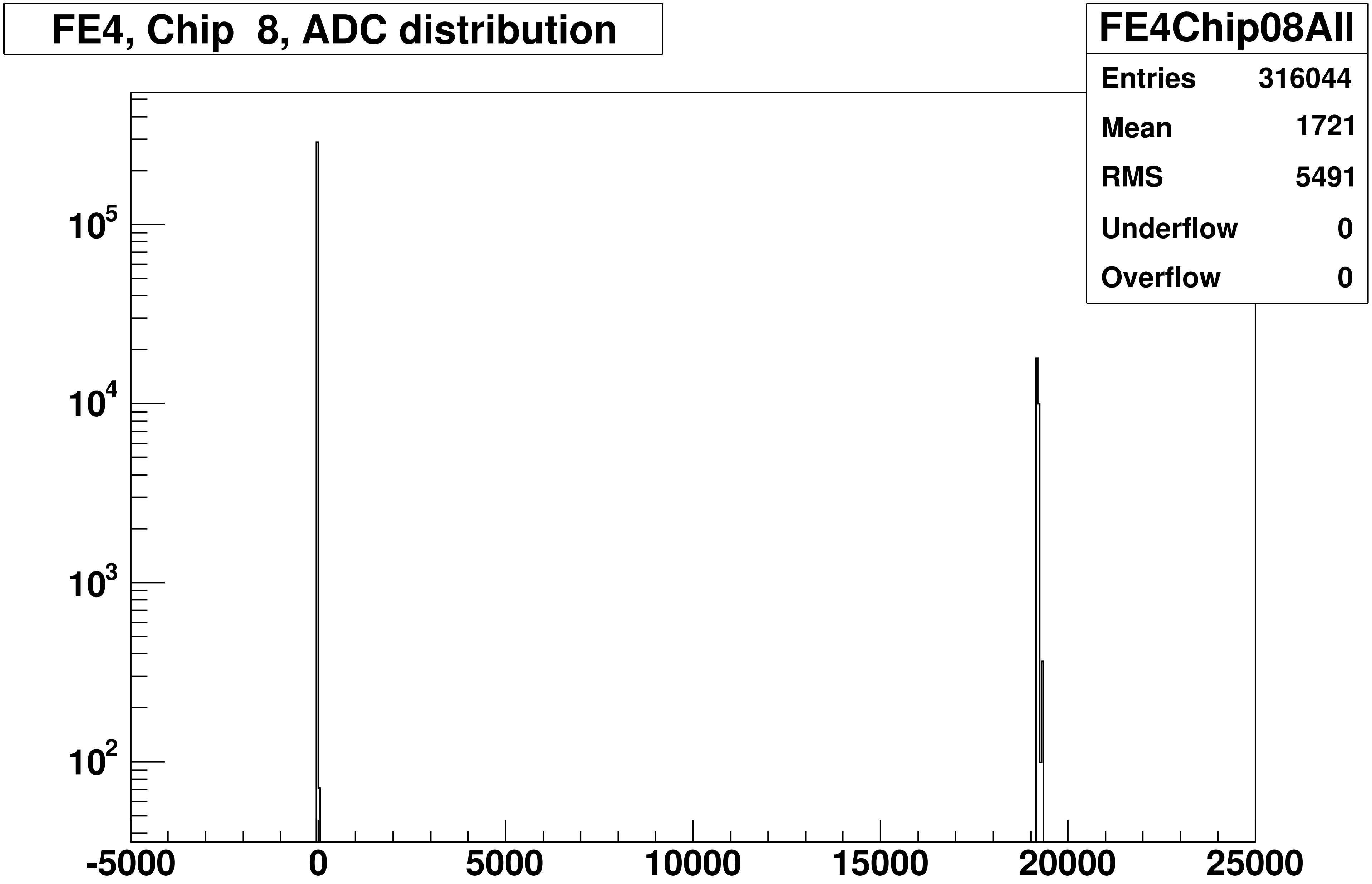
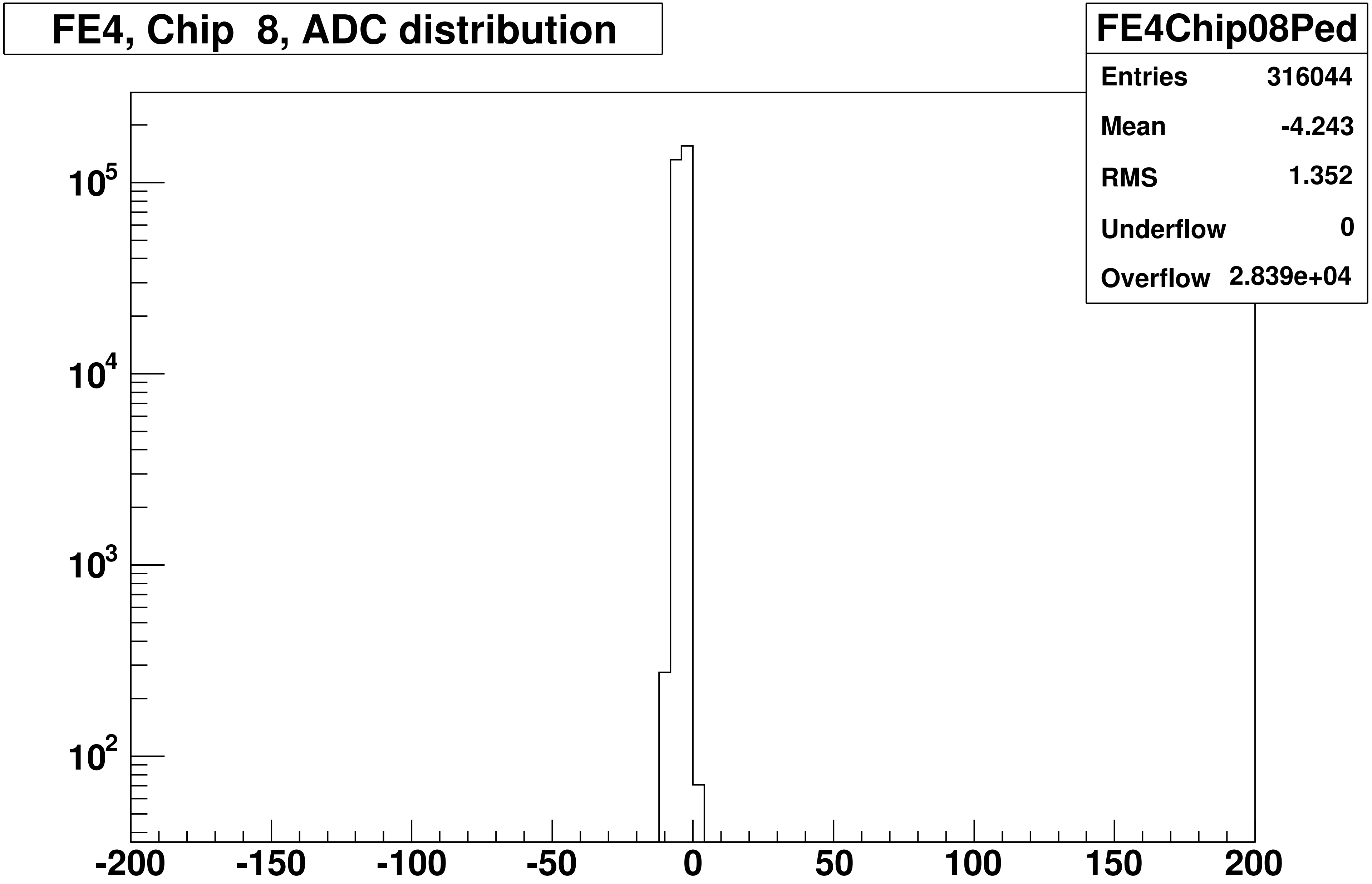
100
150
200


FE4, Chip 7, ADC distribution
FE4Chip07Sig
Entries 316044
Mean 1.928e+04
RMS 13.02
Underflow 2.878e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE4, Chip 8, ADC distribution
FE4Chip08All
Entries 316044
Mean 1721
RMS 5491
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000


FE4, Chip 8, ADC distribution
FE4Chip08Ped
Entries 316044
Mean -4.243
RMS 1.352
Underflow 0
Overflow 2.839e+04
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10^4
10^3
10^2
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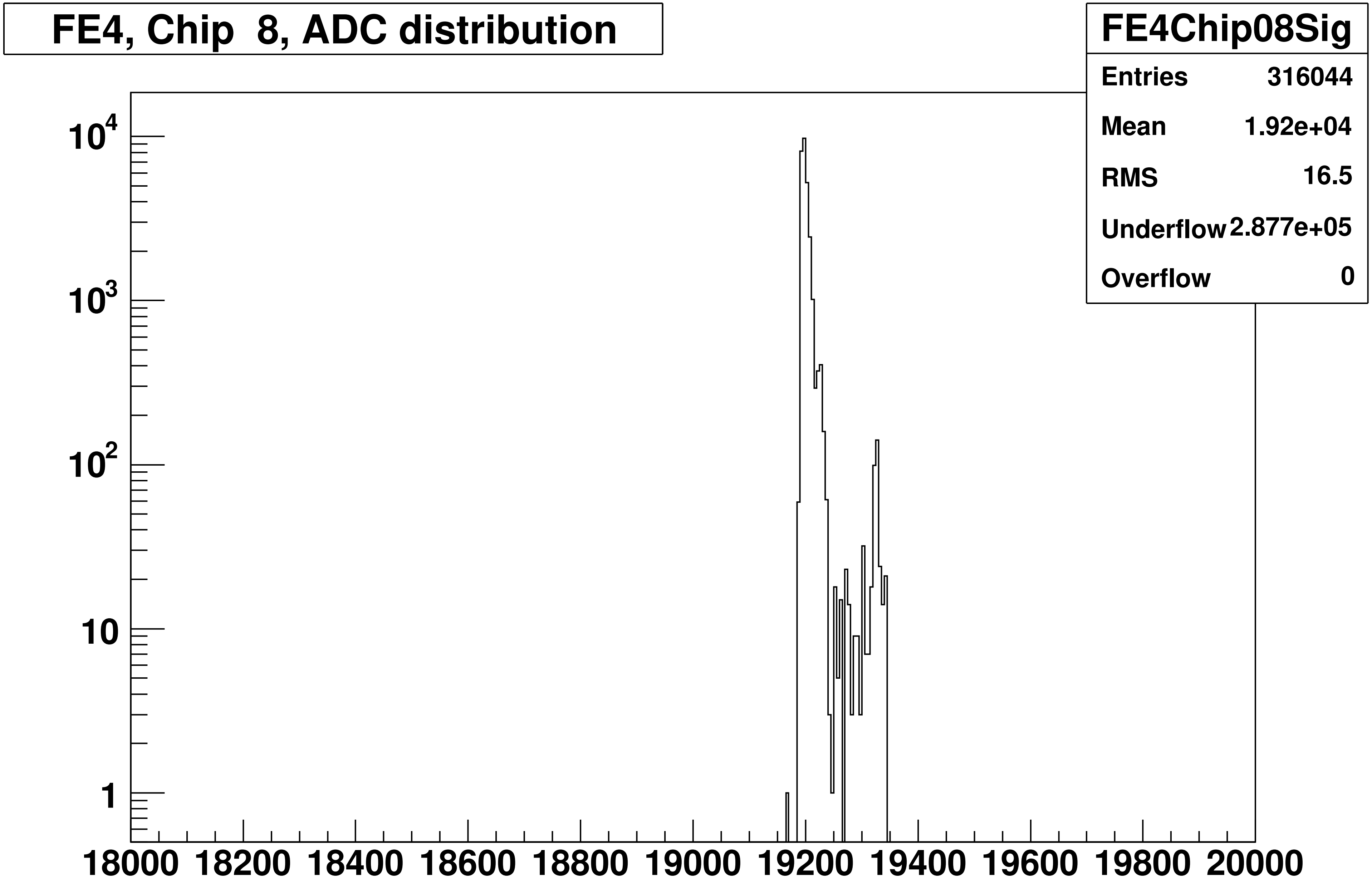
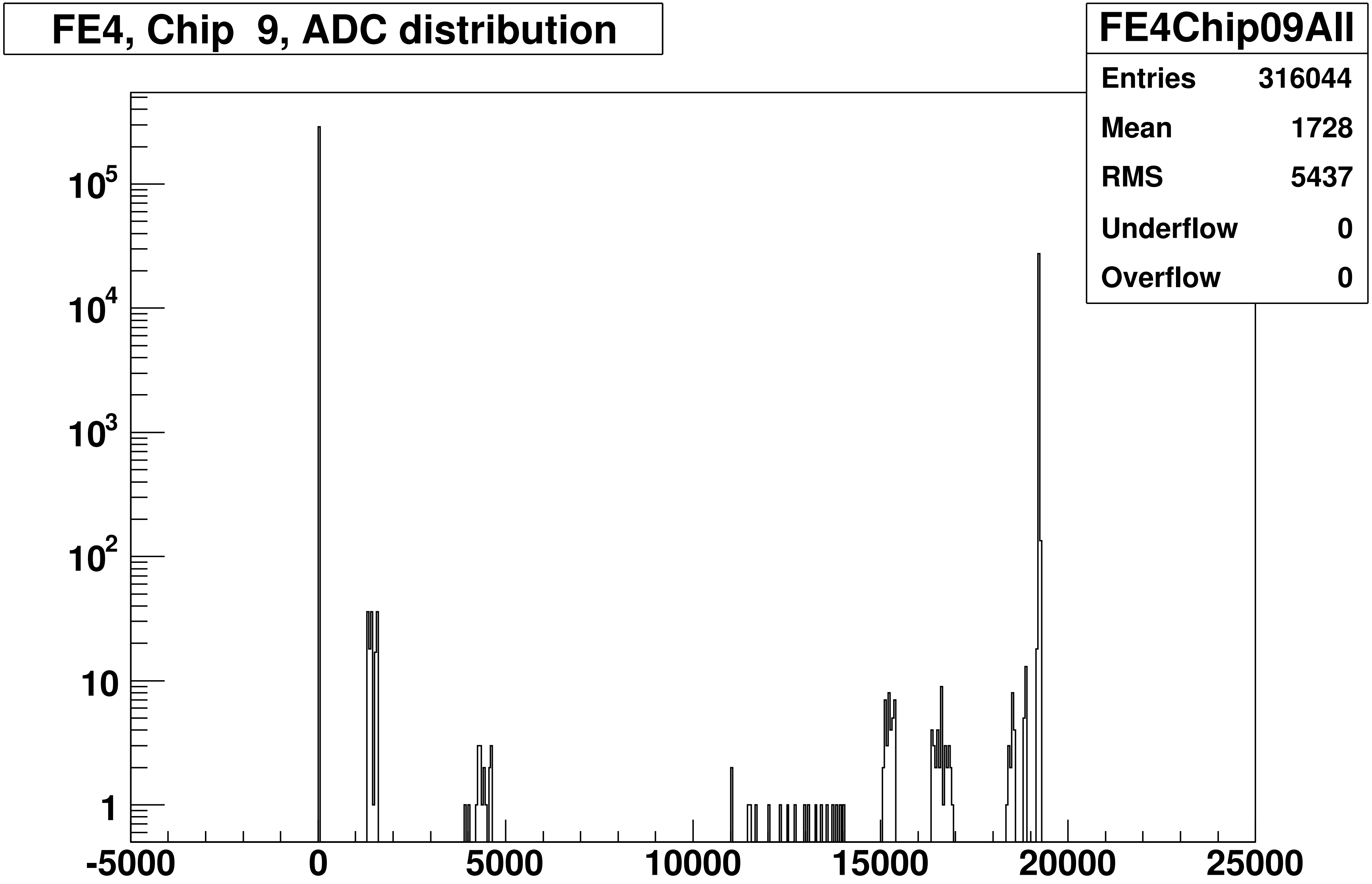
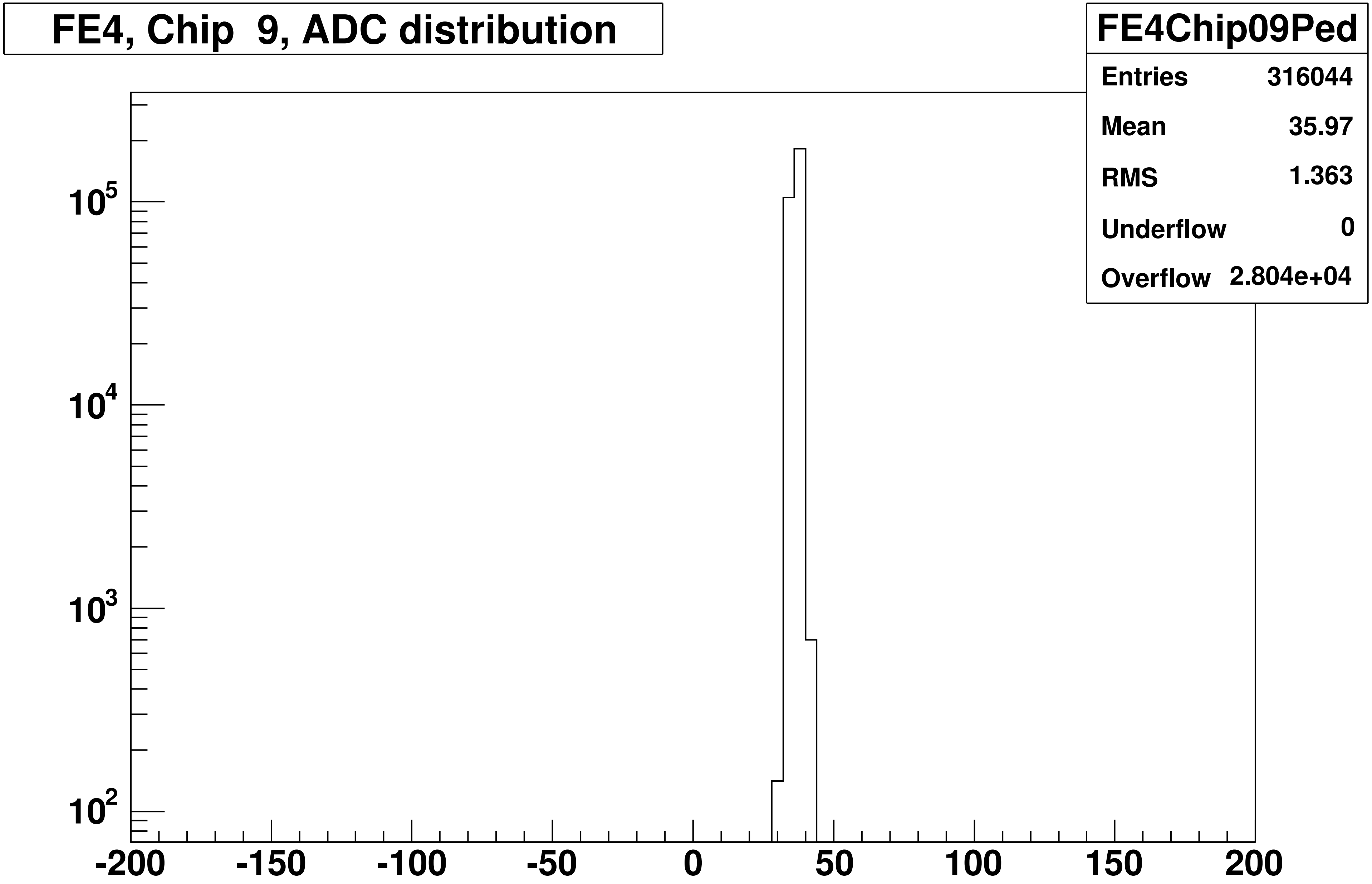
-150
-100
-50
0
50
100
150
200



FE4, Chip 8, ADC distribution
FE4Chip08Sig
Entries 316044
Mean 1.92e+04
RMS 16.5
Underflow 2.877e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE4, Chip 9, ADC distribution
FE4Chip09All
Entries 316044
Mean 1728
RMS 5437
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE4, Chip 9, ADC distribution
FE4Chip09Ped
Entries 316044
Mean 35.97
RMS 1.363
Underflow 0
Overflow 2.804e+04
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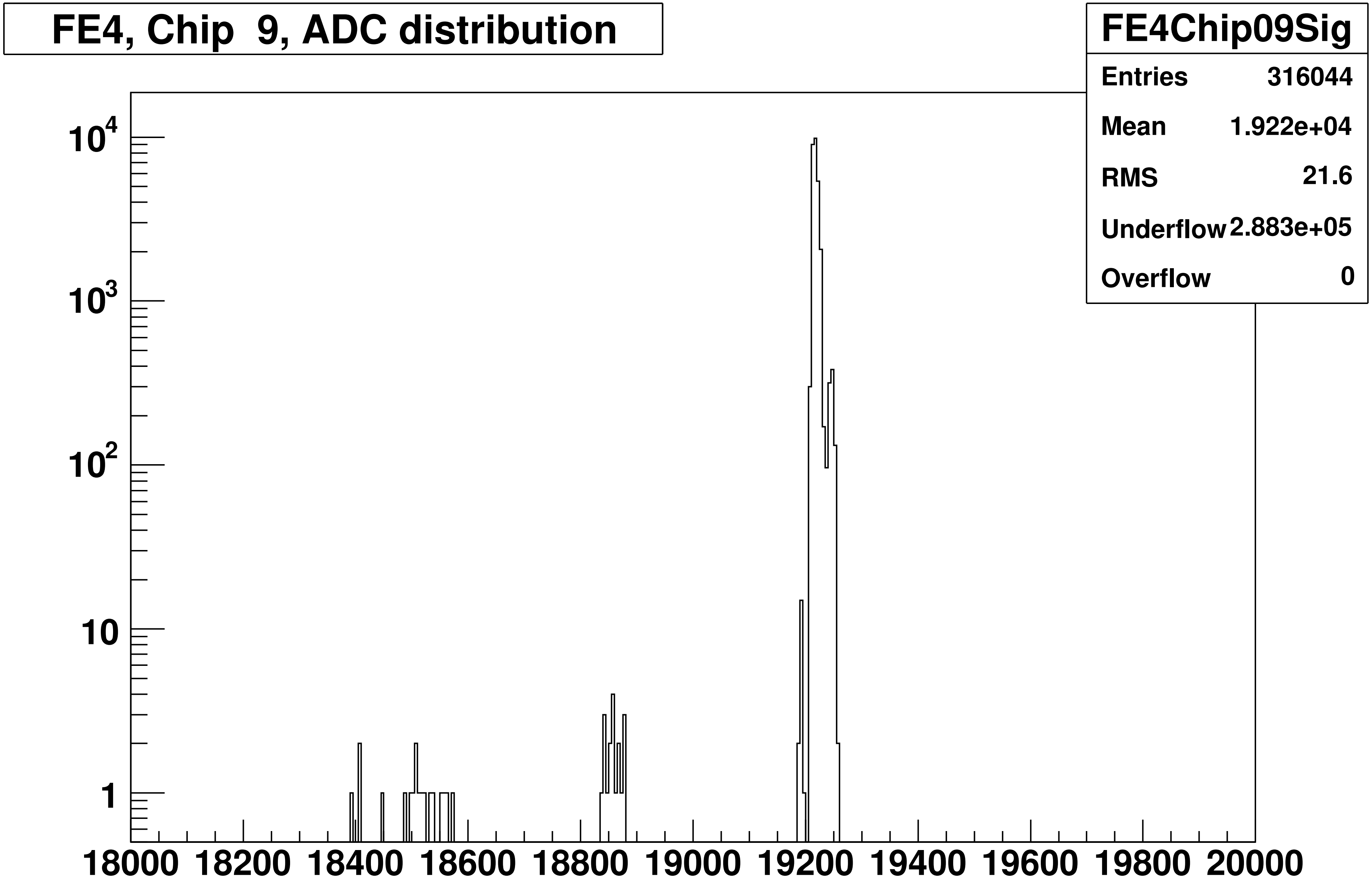
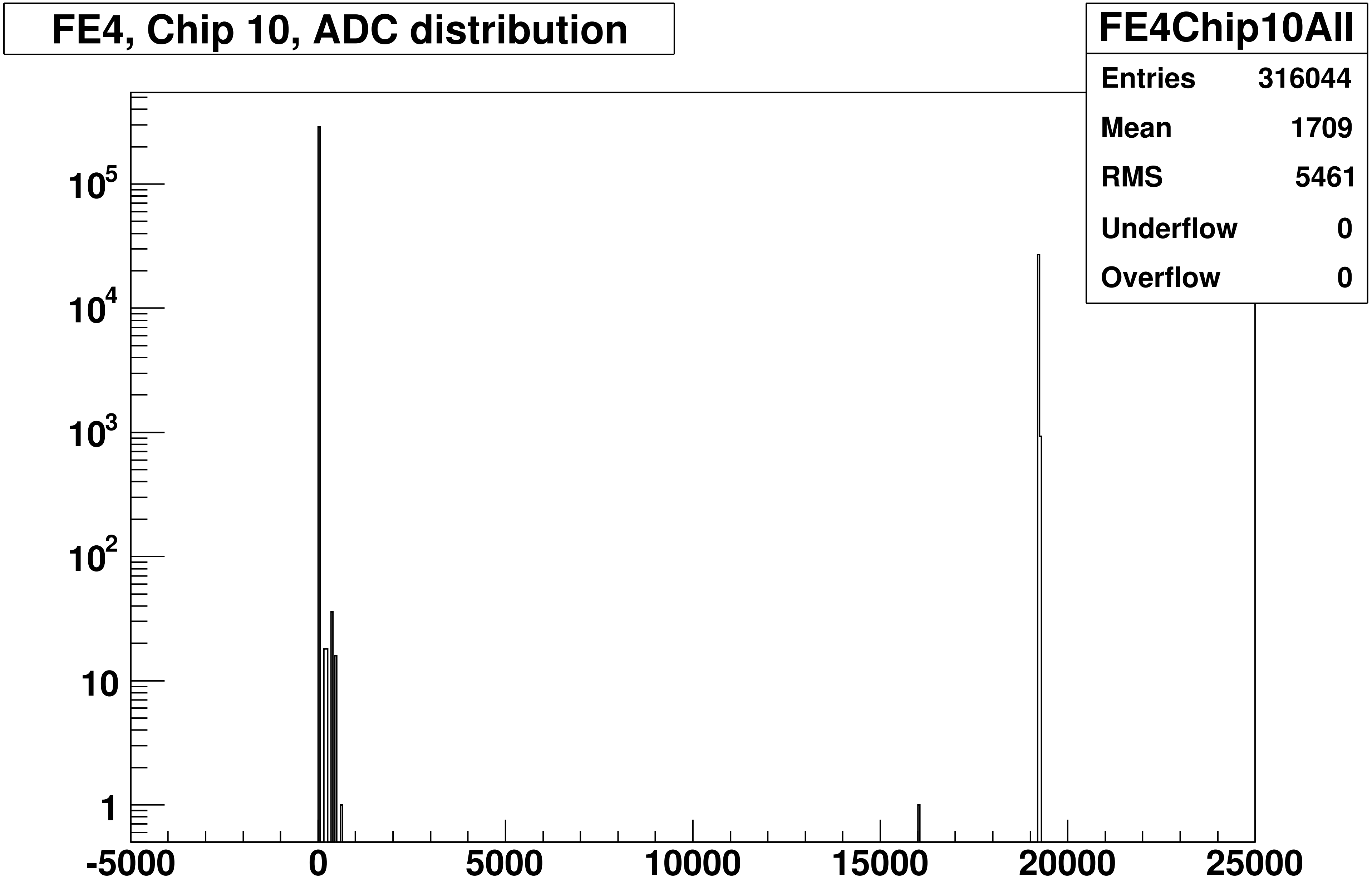
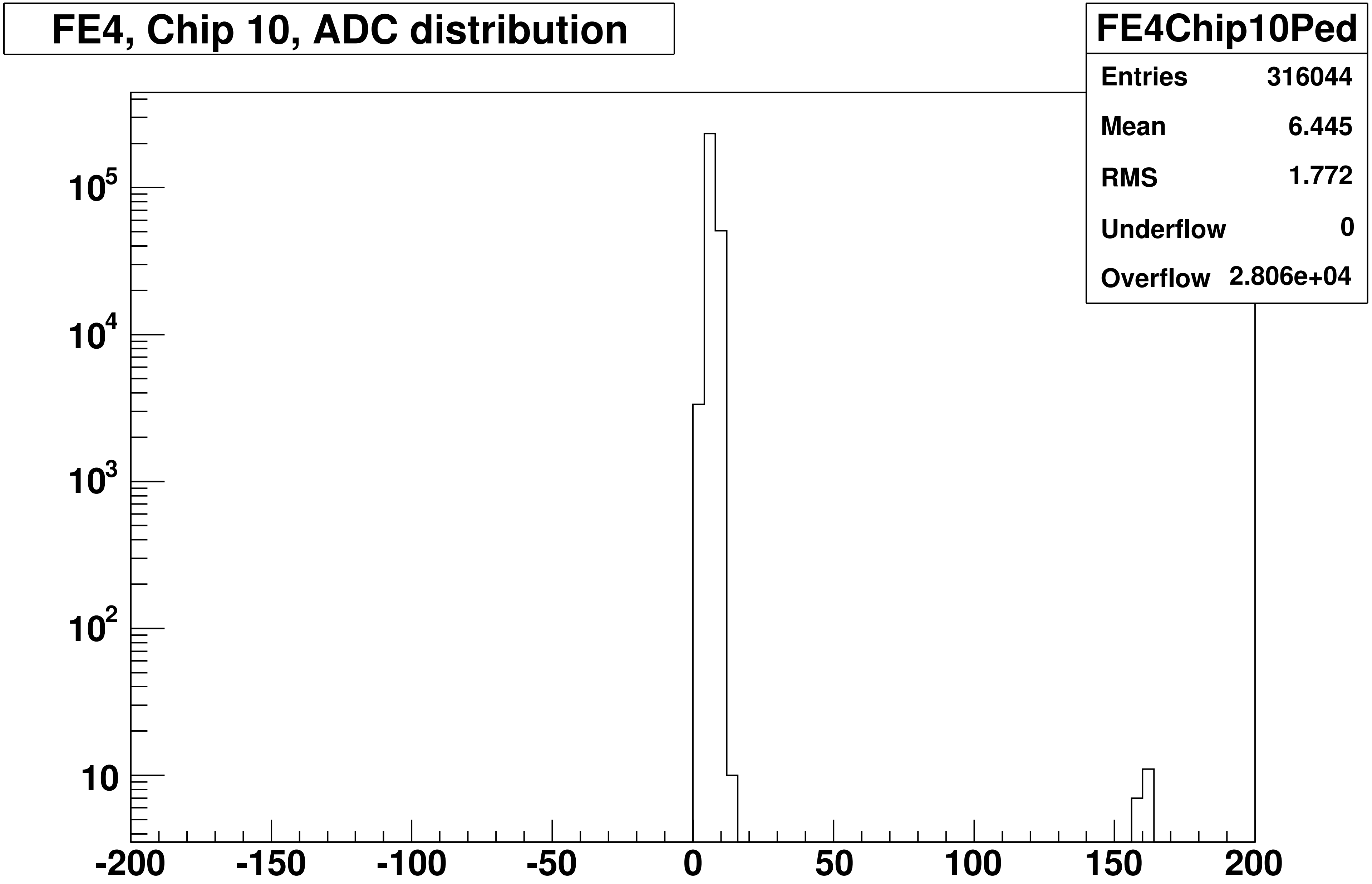
10^4
10^3
10^2
-200
-150
-100
-50
0
50
100
150
200


FE4, Chip 9, ADC distribution
FE4Chip09Sig
Entries 316044
Mean 1.922e+04
RMS 21.6
Underflow 2.883e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000



FE4, Chip 10, ADC distribution
FE4Chip10All
Entries 316044
Mean 1709
RMS 5461
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE4, Chip 10, ADC distribution
FE4Chip10Ped
Entries 316044
Mean 6.445
RMS 1.772
Underflow 0
Overflow 2.806e+04
10^5
10^4
10^3
10^2
10
-200
-150
-100
-50
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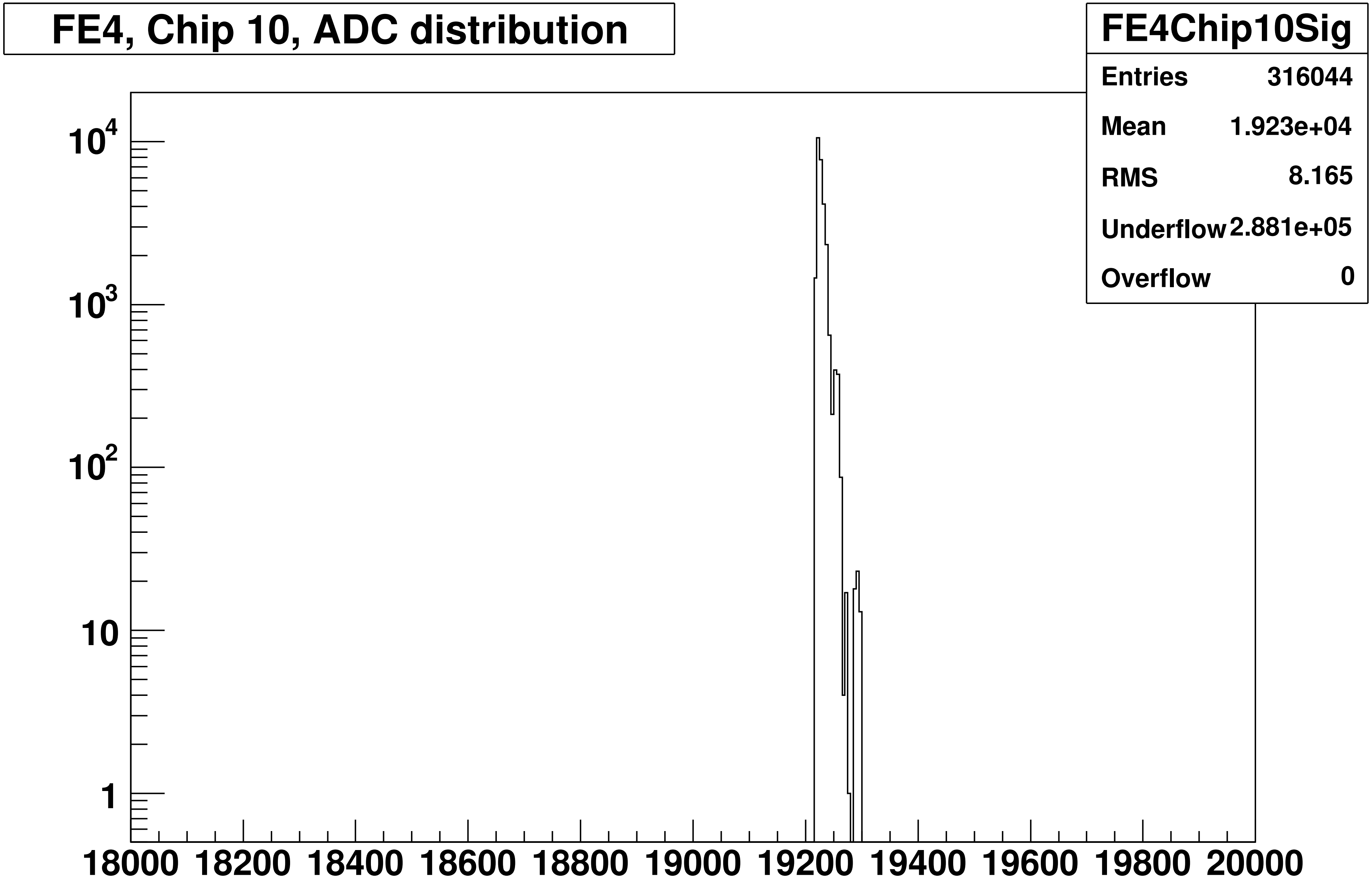
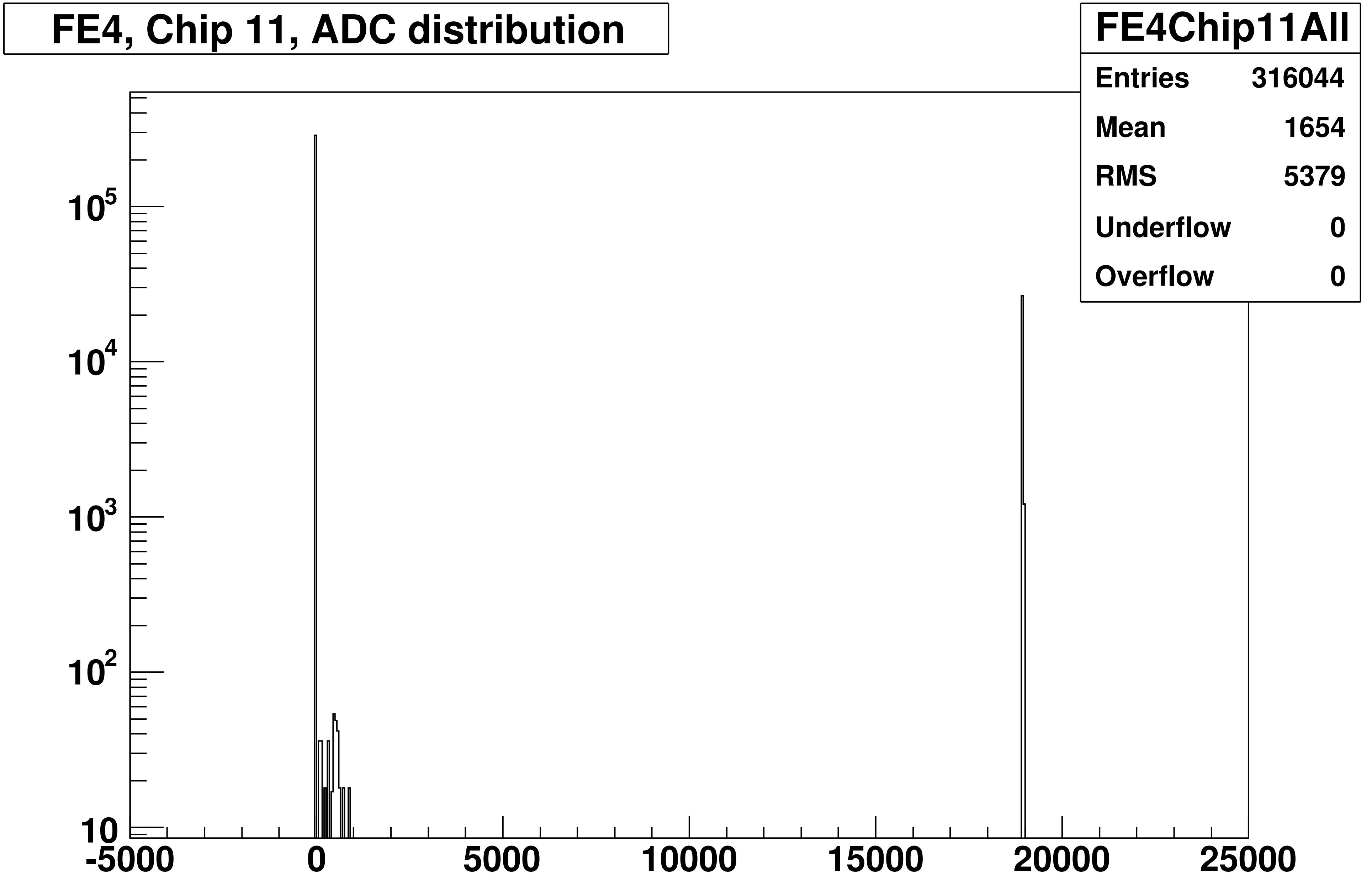
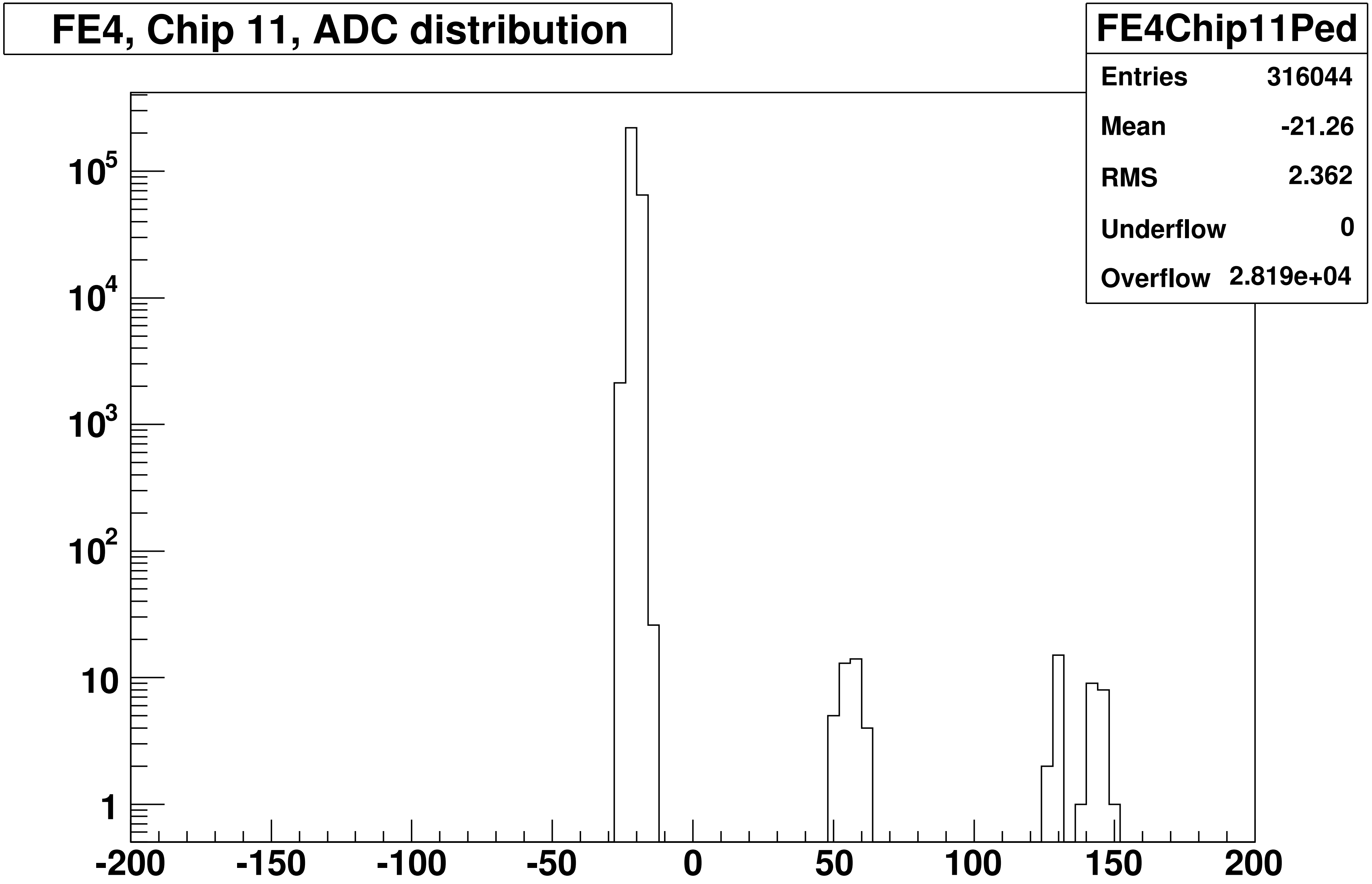
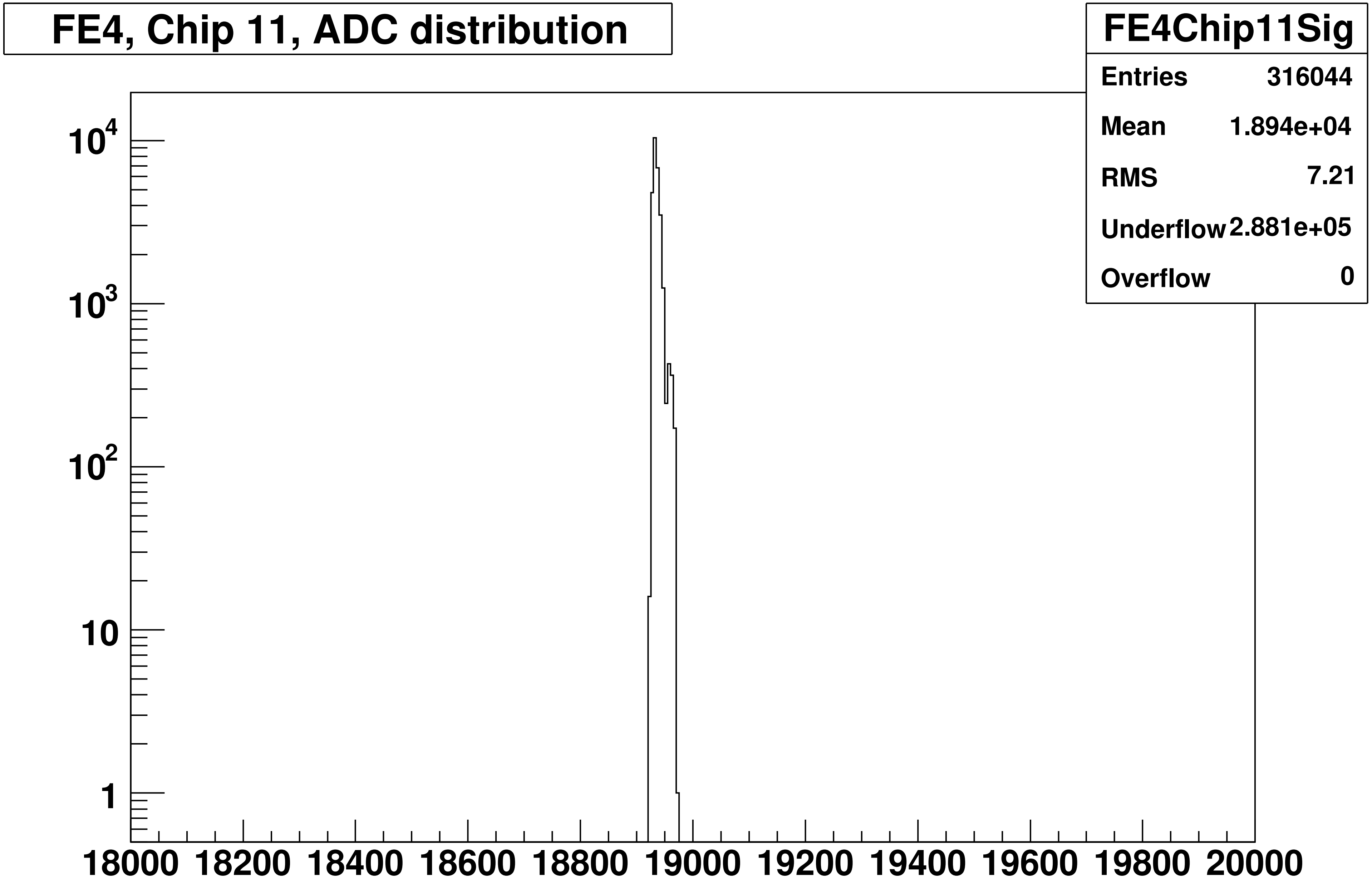
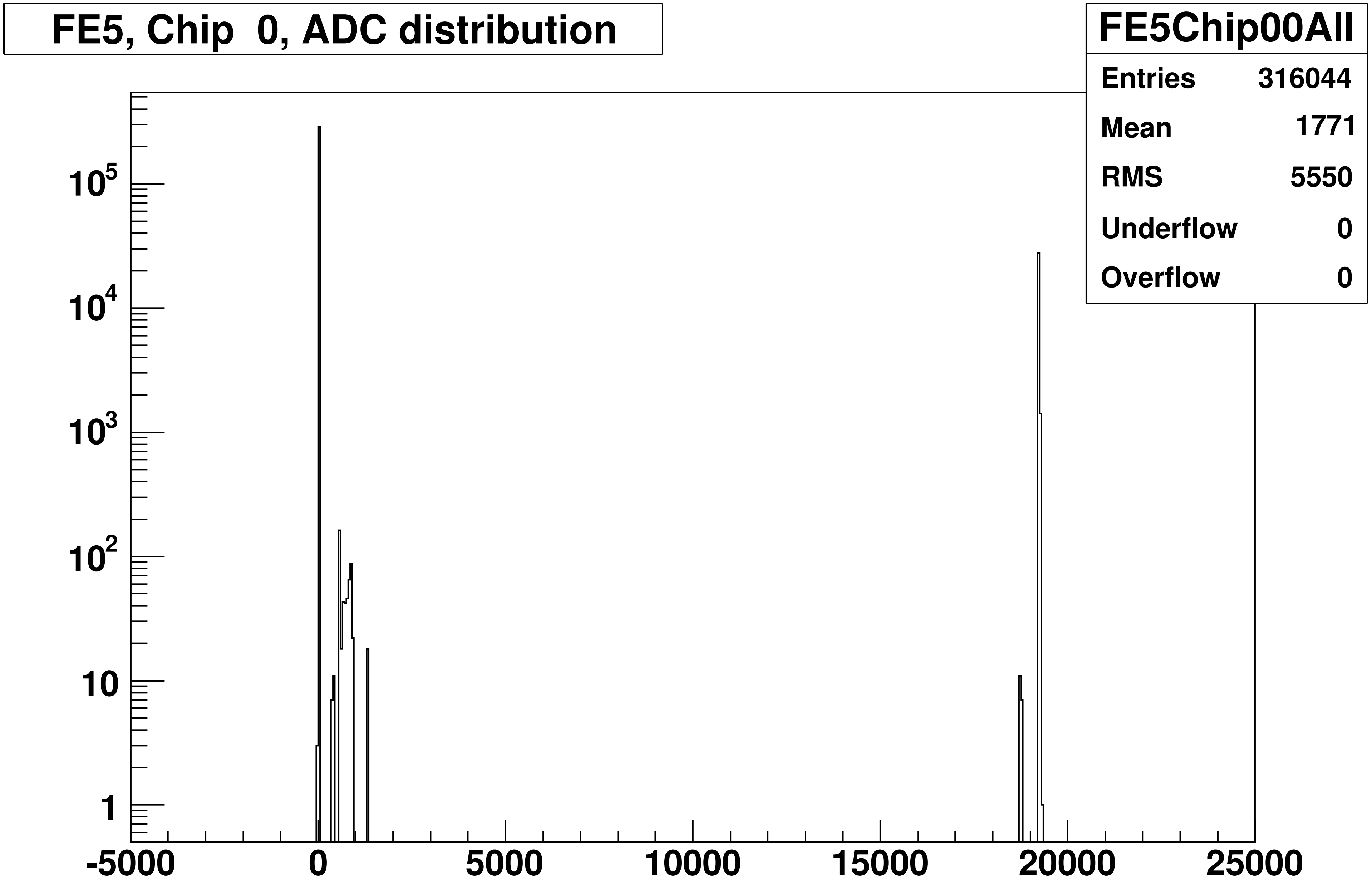
100
150
200

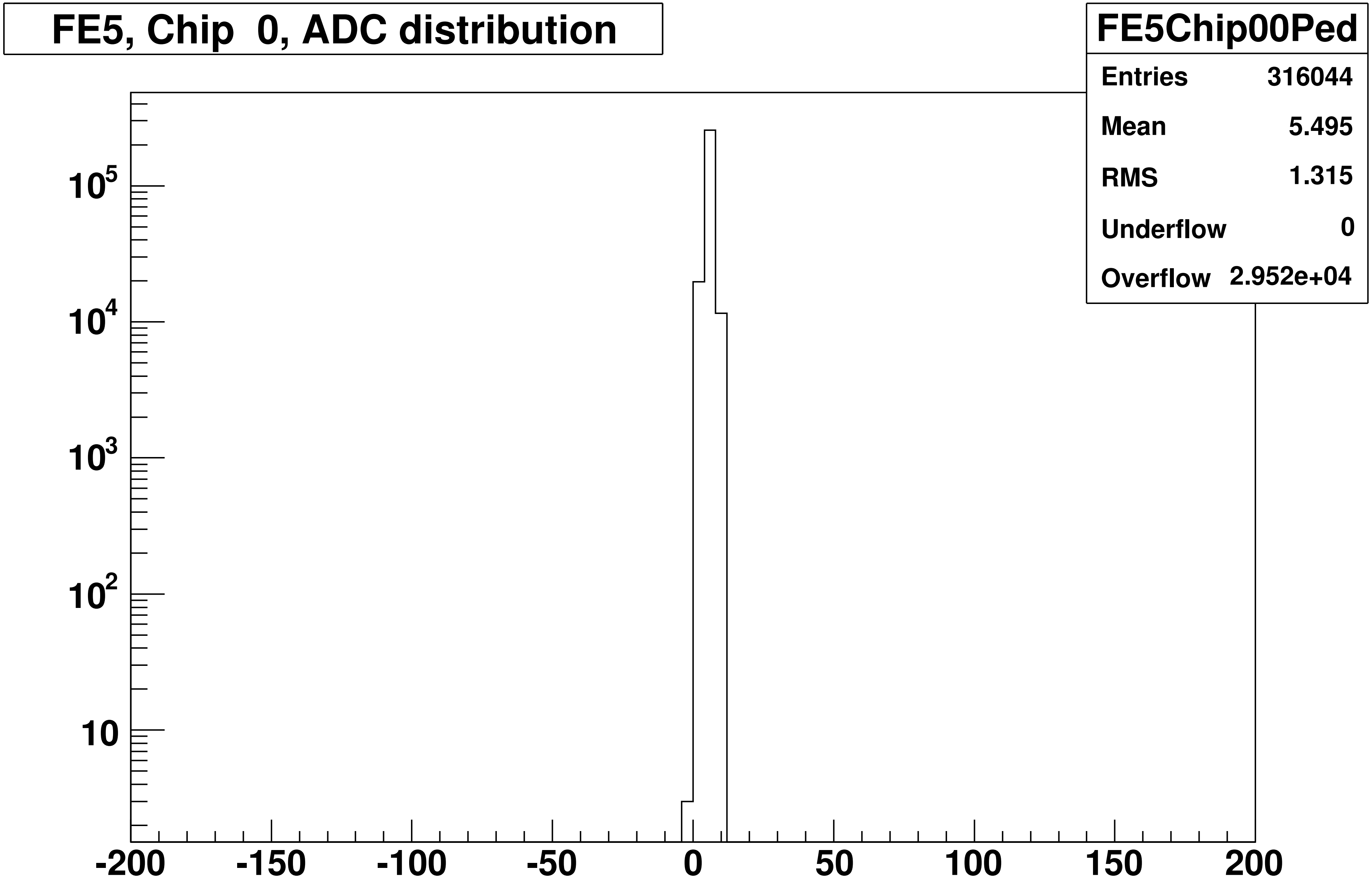

FE4, Chip 10, ADC distribution
FE4Chip10Sig
Entries 316044
Mean 1.923e+04
RMS 8.165
Underflow 2.881e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000

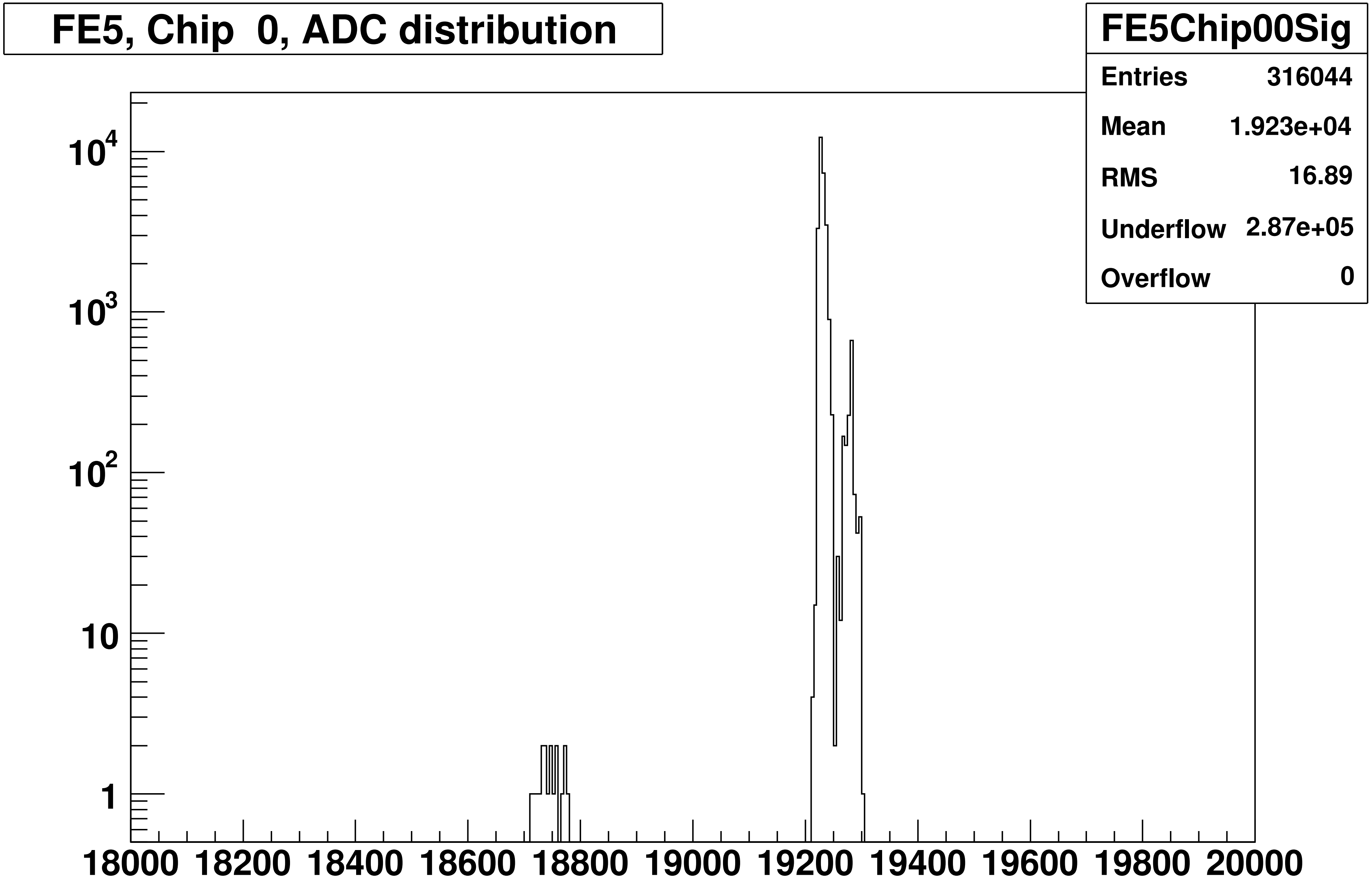

FE4, Chip 11, ADC distribution
FE4Chip11All
Entries 316044
Mean 1654
RMS 5379
Underflow 0
Overflow 0
10
10^2
10^3
10^4
10^5
-5000
0
5000
10000
15000
20000
25000

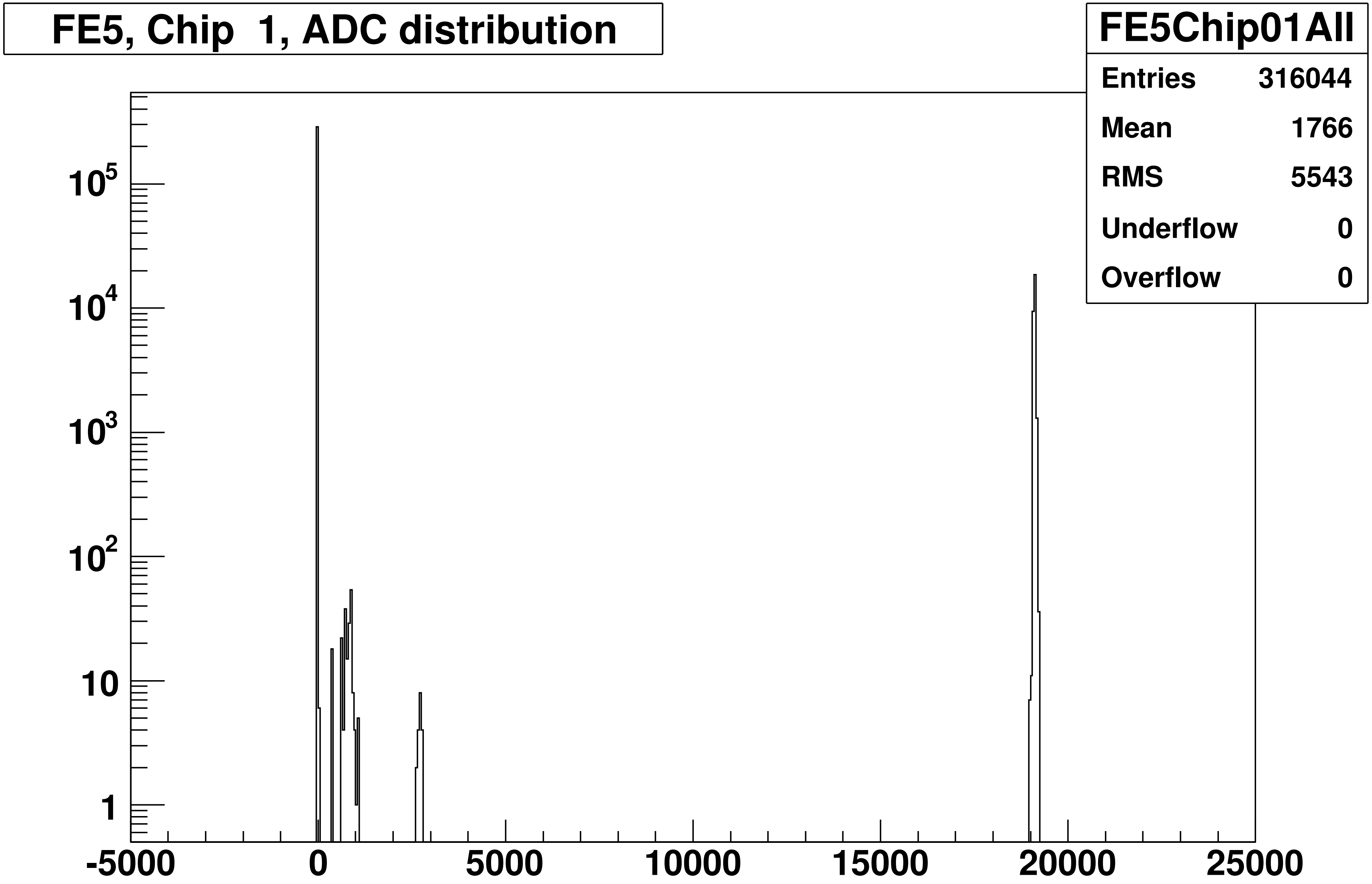

FE4, Chip 11, ADC distribution
FE4Chip11Ped
Entries 316044
Mean -21.26
RMS 2.362
Underflow 0
Overflow 2.819e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
200

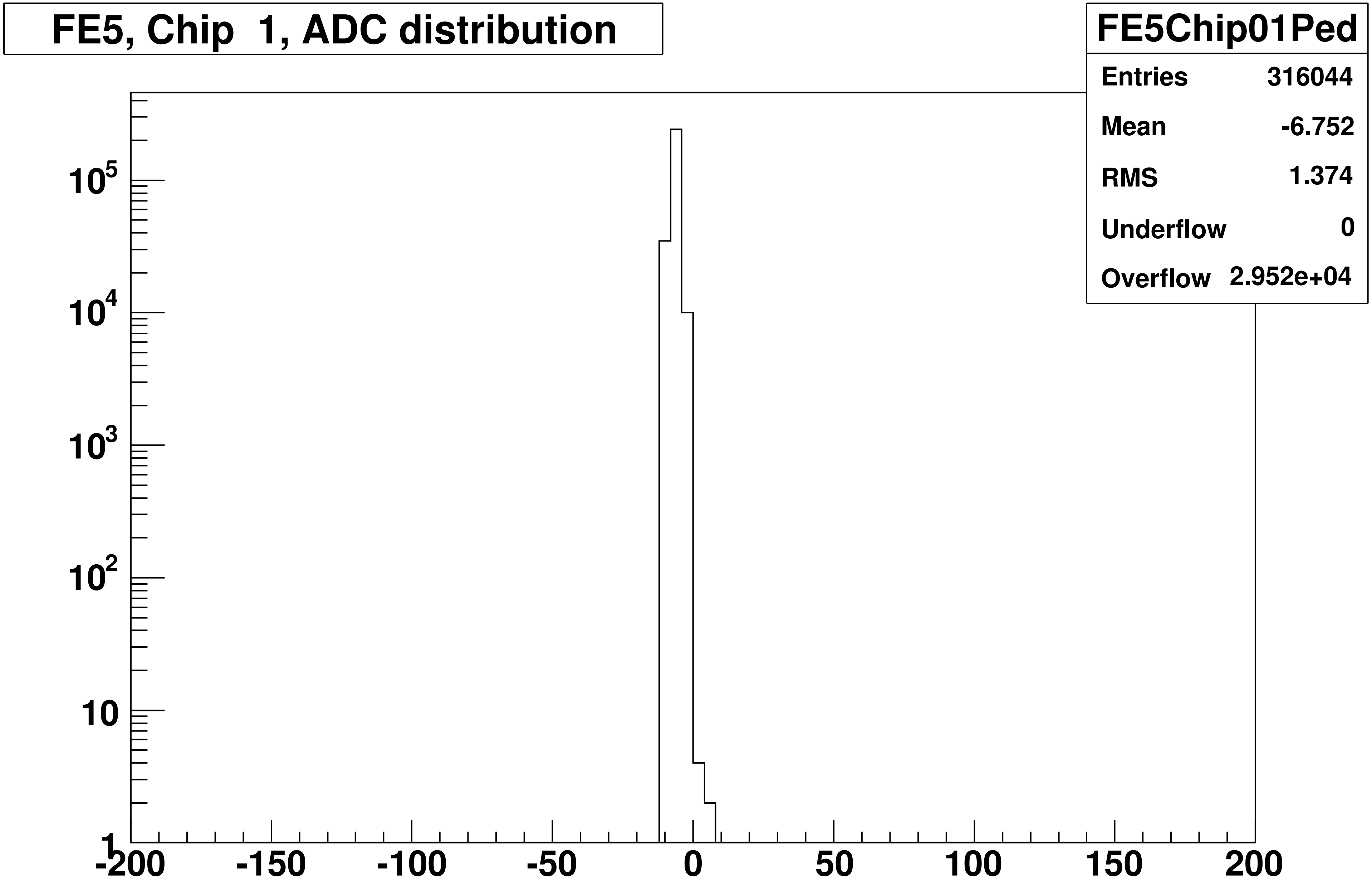

FE4, Chip 11, ADC distribution
FE4Chip11Sig
Entries 316044
Mean 1.894e+04
RMS 7.21
Underflow 2.881e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE5, Chip 0, ADC distribution
FE5Chip00All
Entries 316044
Mean 1771
RMS 5550
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE5, Chip 0, ADC distribution
FE5Chip00Ped
Entries 316044
Mean 5.495
RMS 1.315
Underflow 0
Overflow 2.952e+04
10^5
10^4
10^3
10^2
10
-200
-150
-100
-50
0
50
100
150
200


FE5, Chip 0, ADC distribution
FE5Chip00Sig
Entries 316044
Mean 1.923e+04
RMS 16.89
Underflow 2.87e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000


FE5, Chip 1, ADC distribution
FE5Chip01All
Entries 316044
Mean 1766
RMS 5543
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE5, Chip 1, ADC distribution
FE5Chip01Ped
Entries 316044
Mean -6.752
RMS 1.374
Underflow 0
Overflow 2.952e+04
10^5
10^4
10^3
10^2
10
1
-200
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-100
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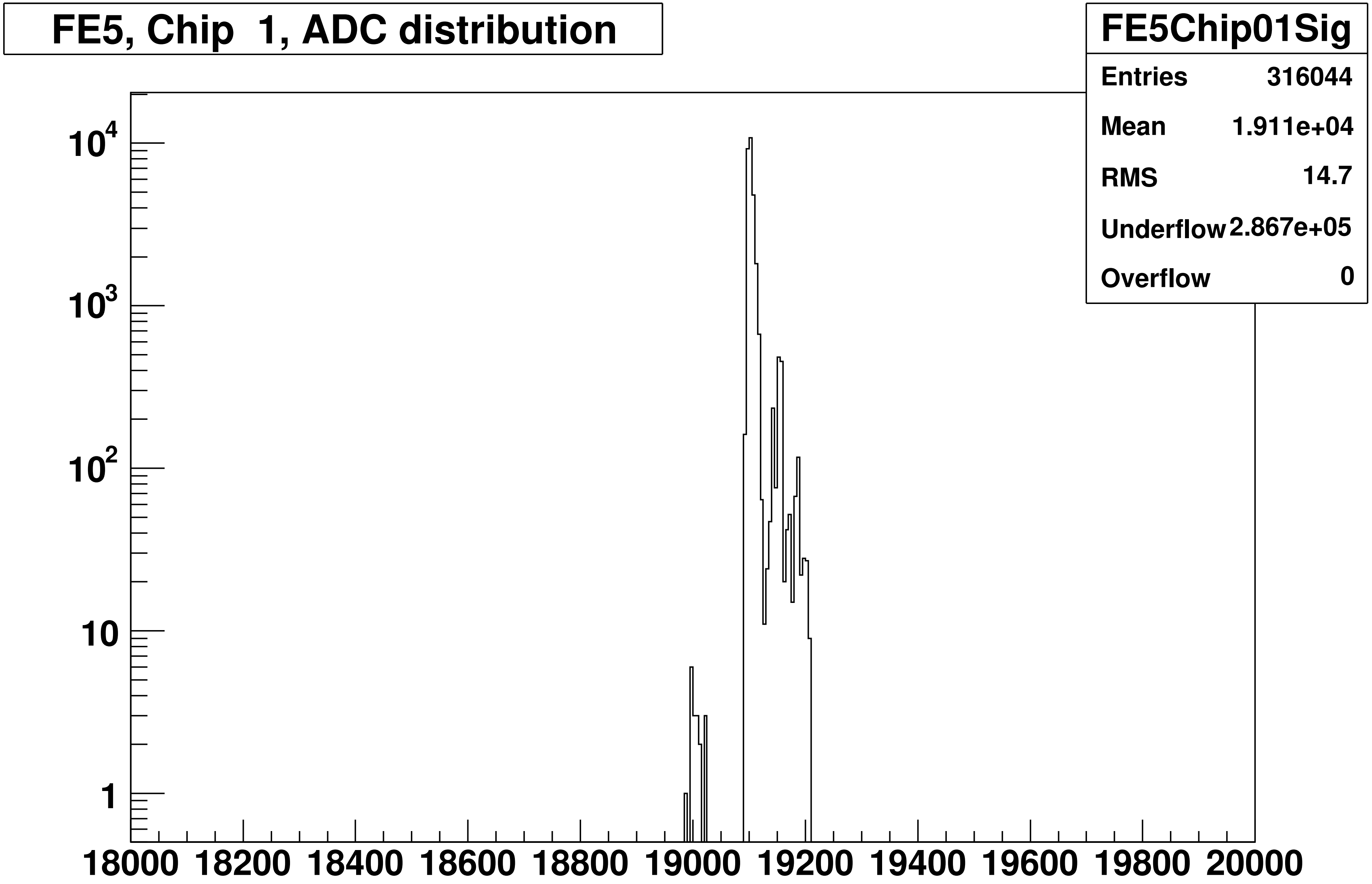
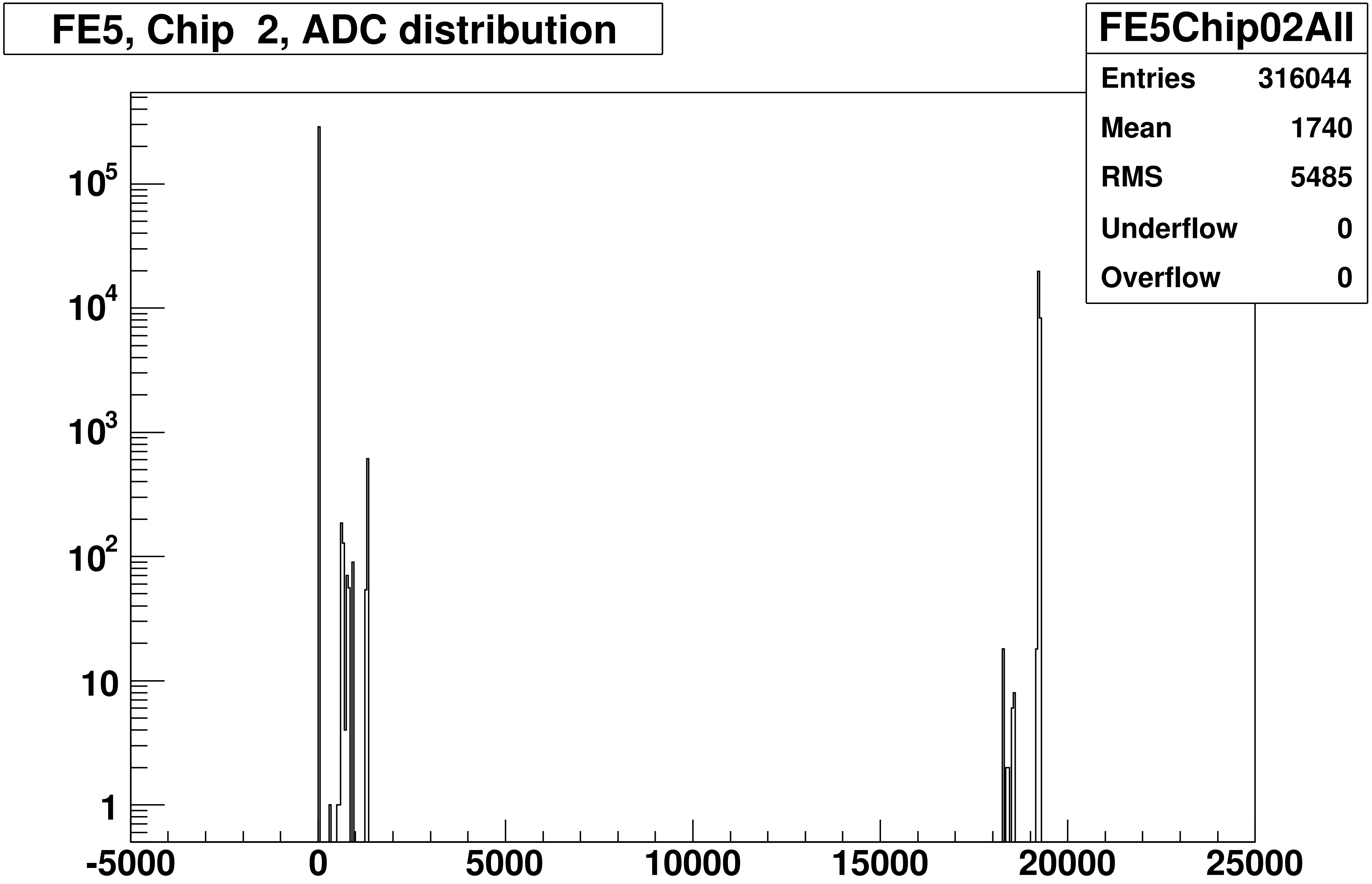
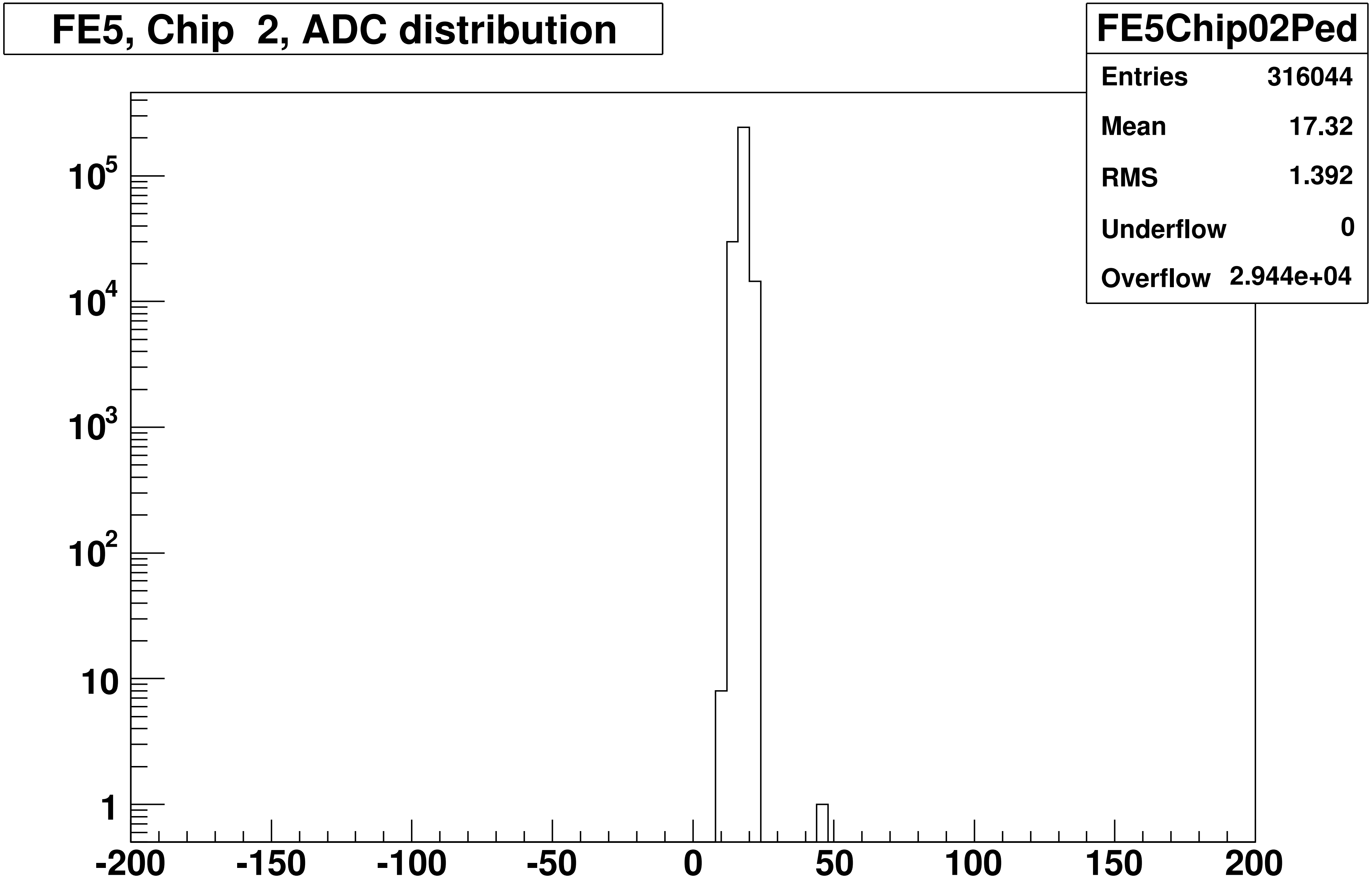
150
200



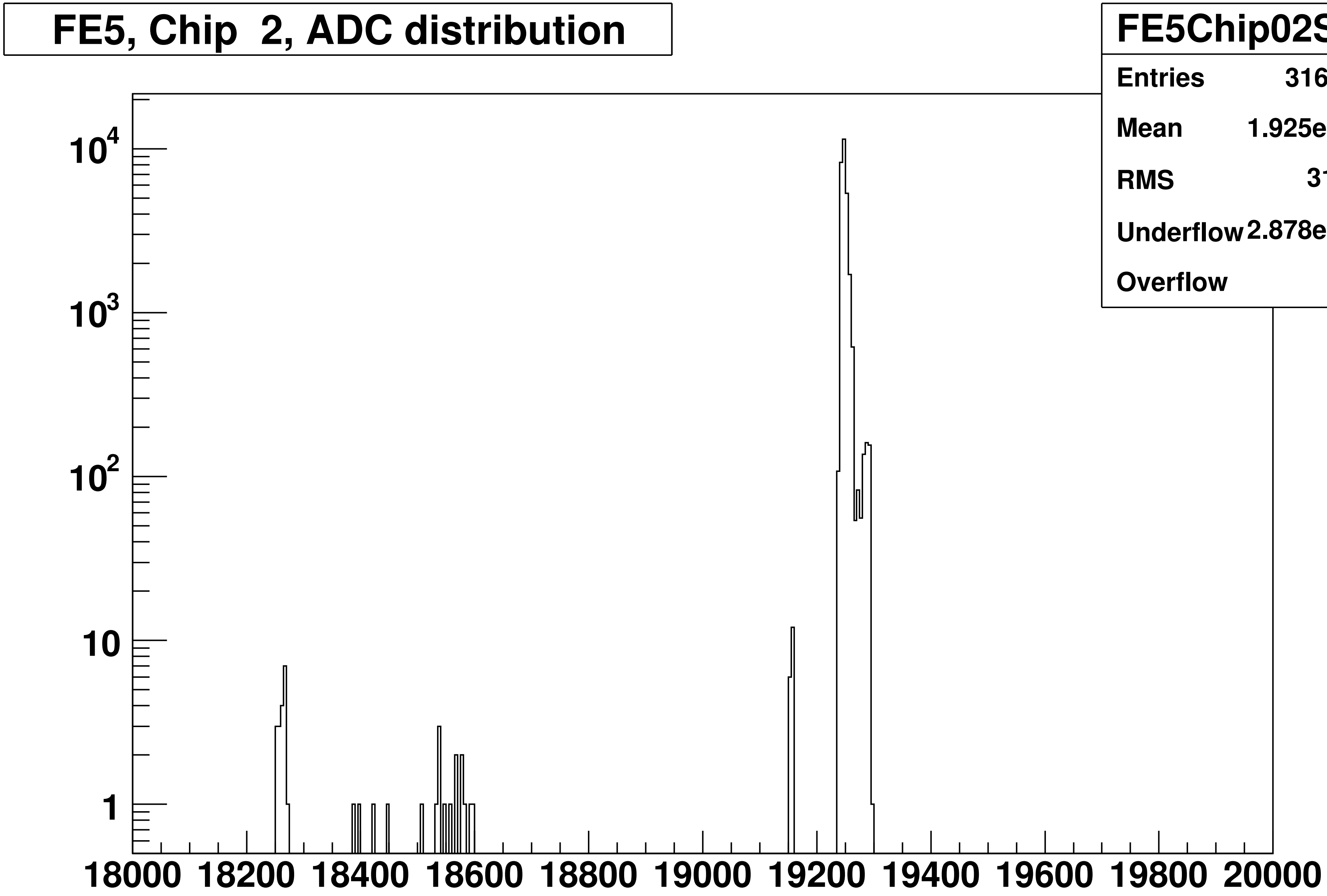
FE5, Chip 1, ADC distribution
FE5Chip01Sig
Entries 316044
Mean 1.911e+04
RMS 14.7
Underflow 2.867e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000

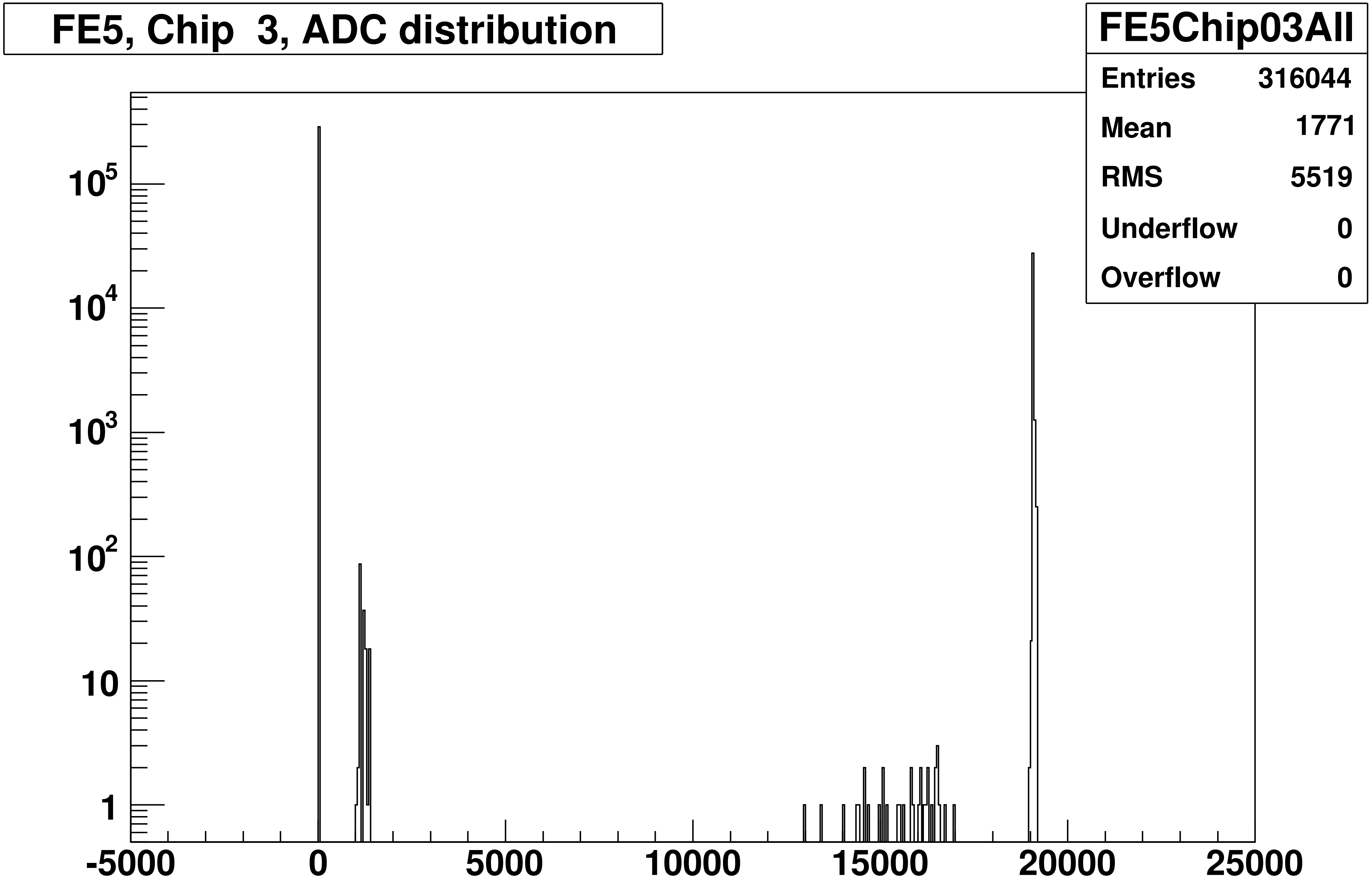


FE5, Chip 2, ADC distribution
FE5Chip02All
Entries 316044
Mean 1740
RMS 5485
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE5, Chip 2, ADC distribution
FE5Chip02Ped
Entries 316044
Mean 17.32
RMS 1.392
Underflow 0
Overflow 2.944e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
200


FE5, Chip 2, ADC distribution
FE5Chip02Sig
Entries 316044
Mean 1.925e+04
RMS 31.76
Underflow 2.878e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000


FE5, Chip 3, ADC distribution
FE5Chip03All
Entries 316044
Mean 1771
RMS 5519
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
1
-5000
0
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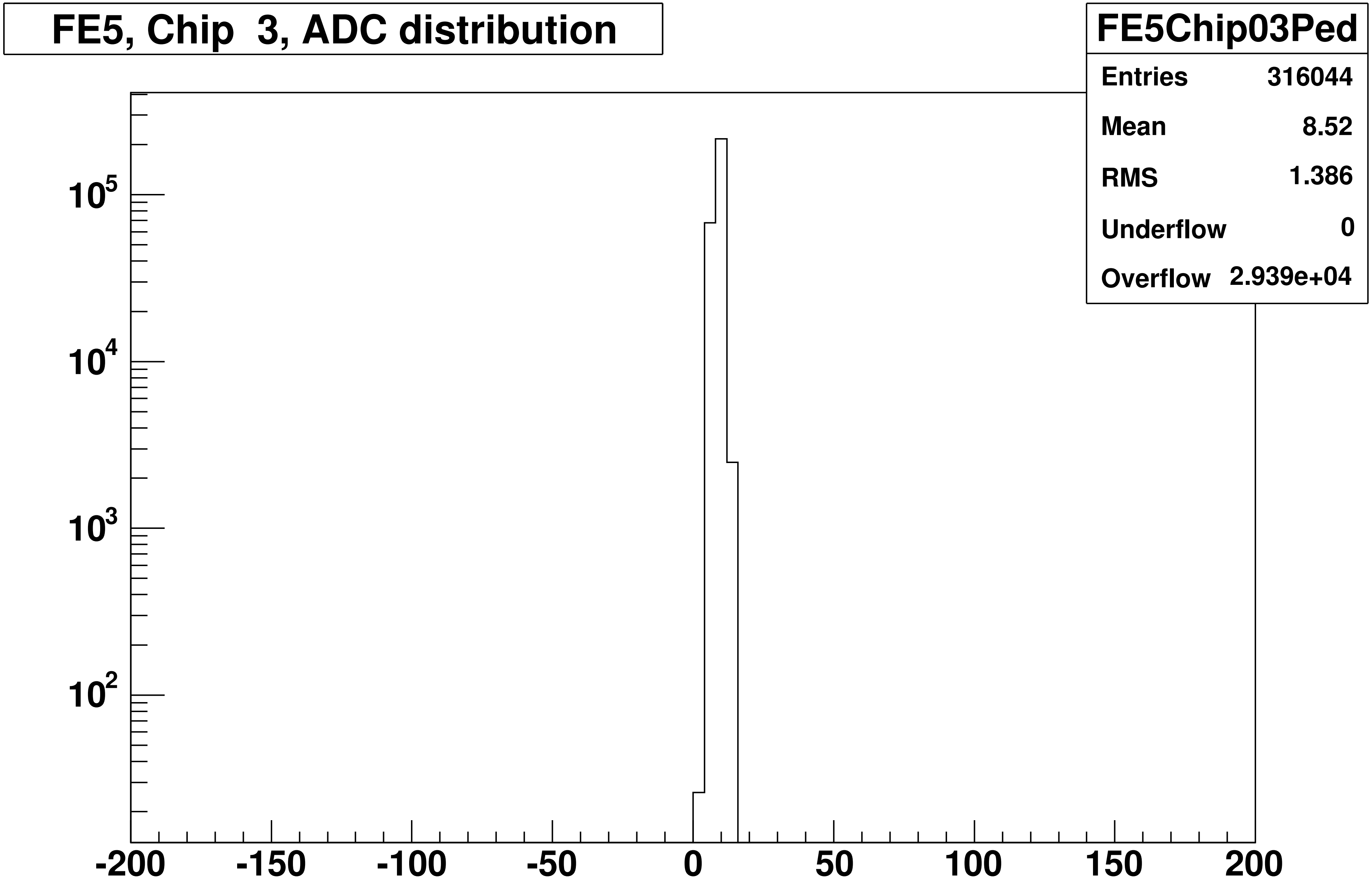
10000
15000
20000
25000


FE5, Chip 3, ADC distribution
FE5Chip03Ped
Entries 316044
Mean 8.52
RMS 1.386
Underflow 0
Overflow 2.939e+04
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10^4
10^3
10^2
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-100
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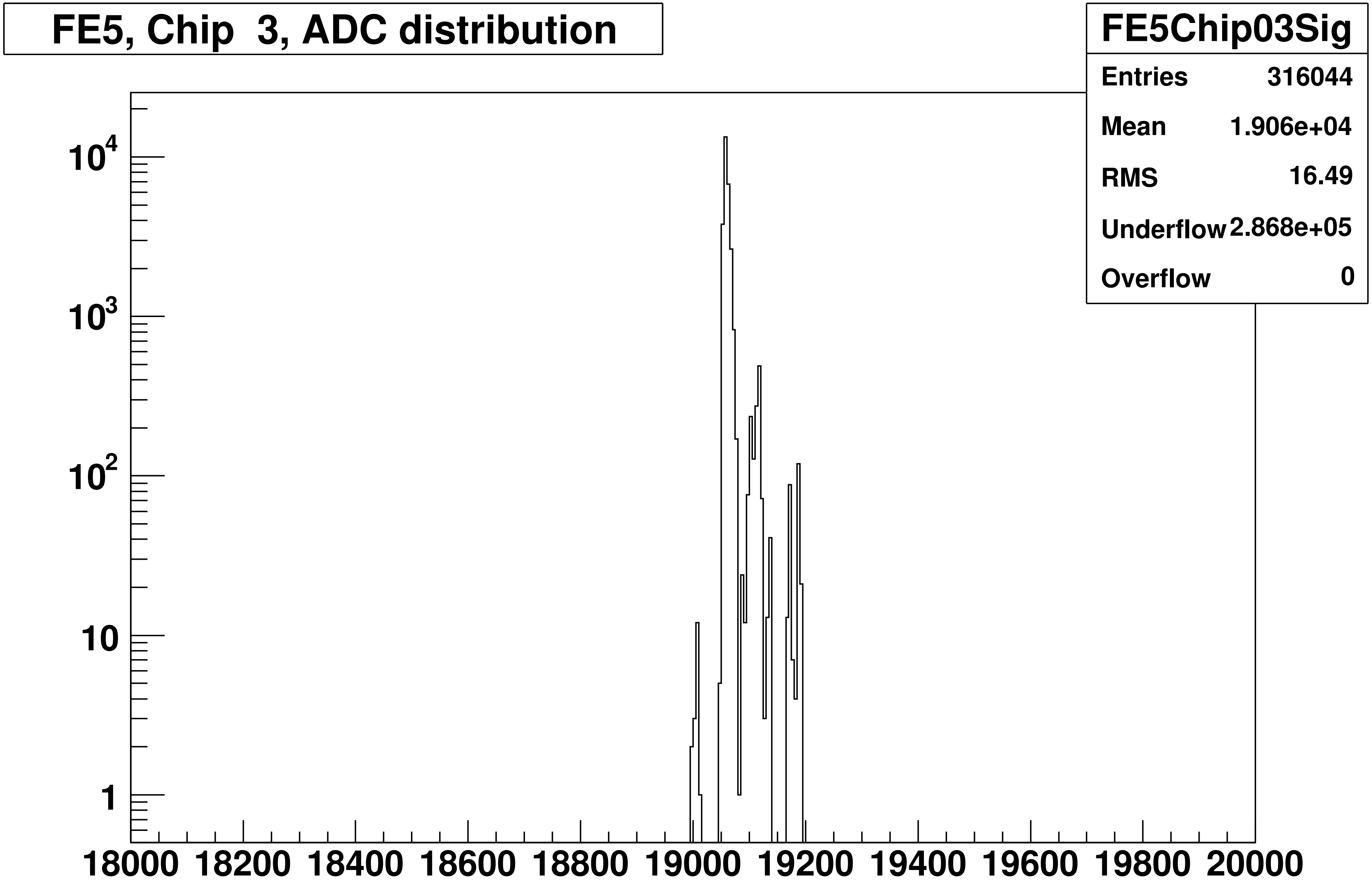
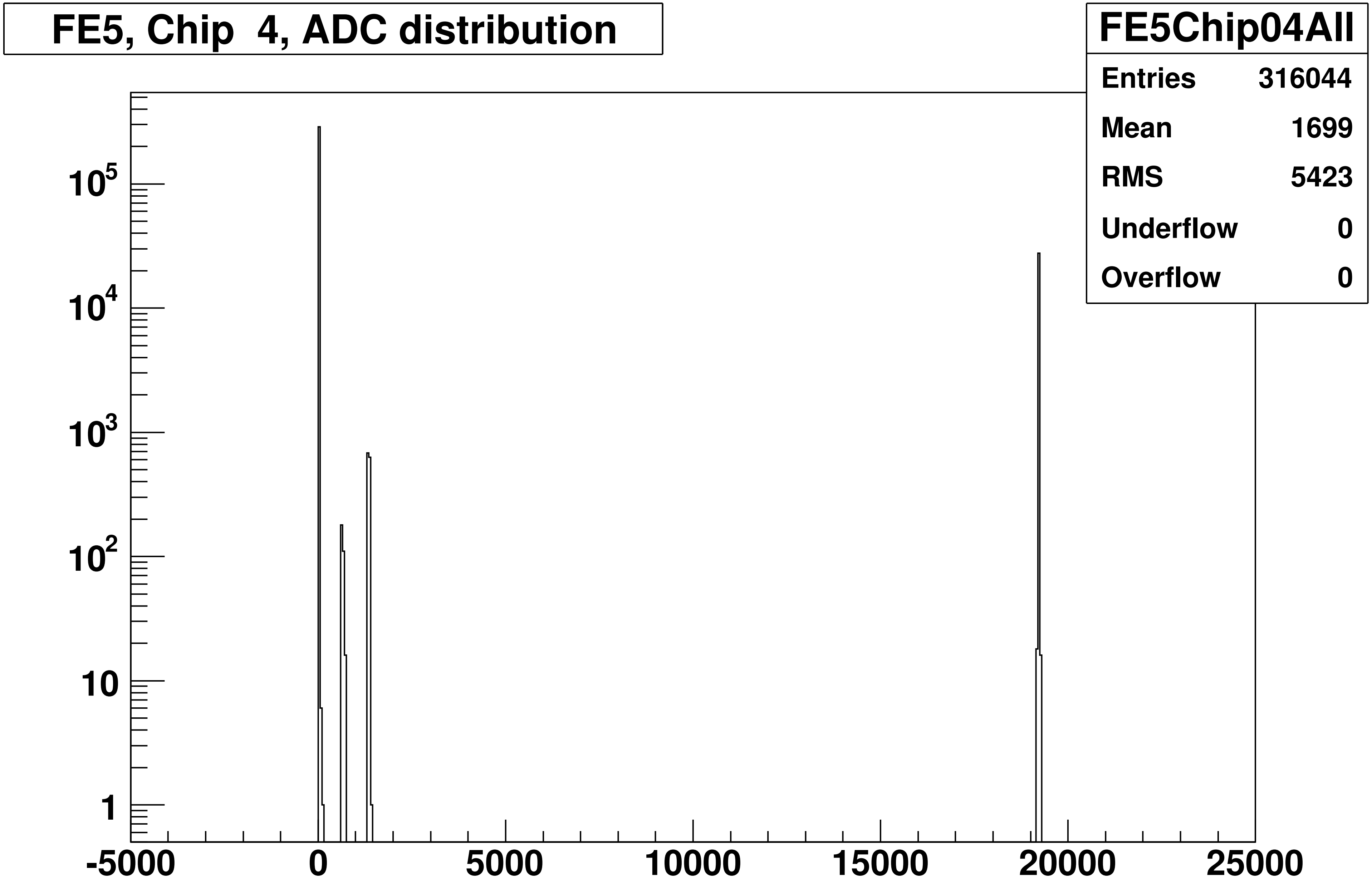
0
50
100
150
200


FE5, Chip 3, ADC distribution
FE5Chip03Sig
Entries 316044
Mean 1.906e+04
RMS 16.49
Underflow 2.868e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE5, Chip 4, ADC distribution
FE5Chip04All
Entries 316044
Mean 1699
RMS 5423
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
1
-5000
0
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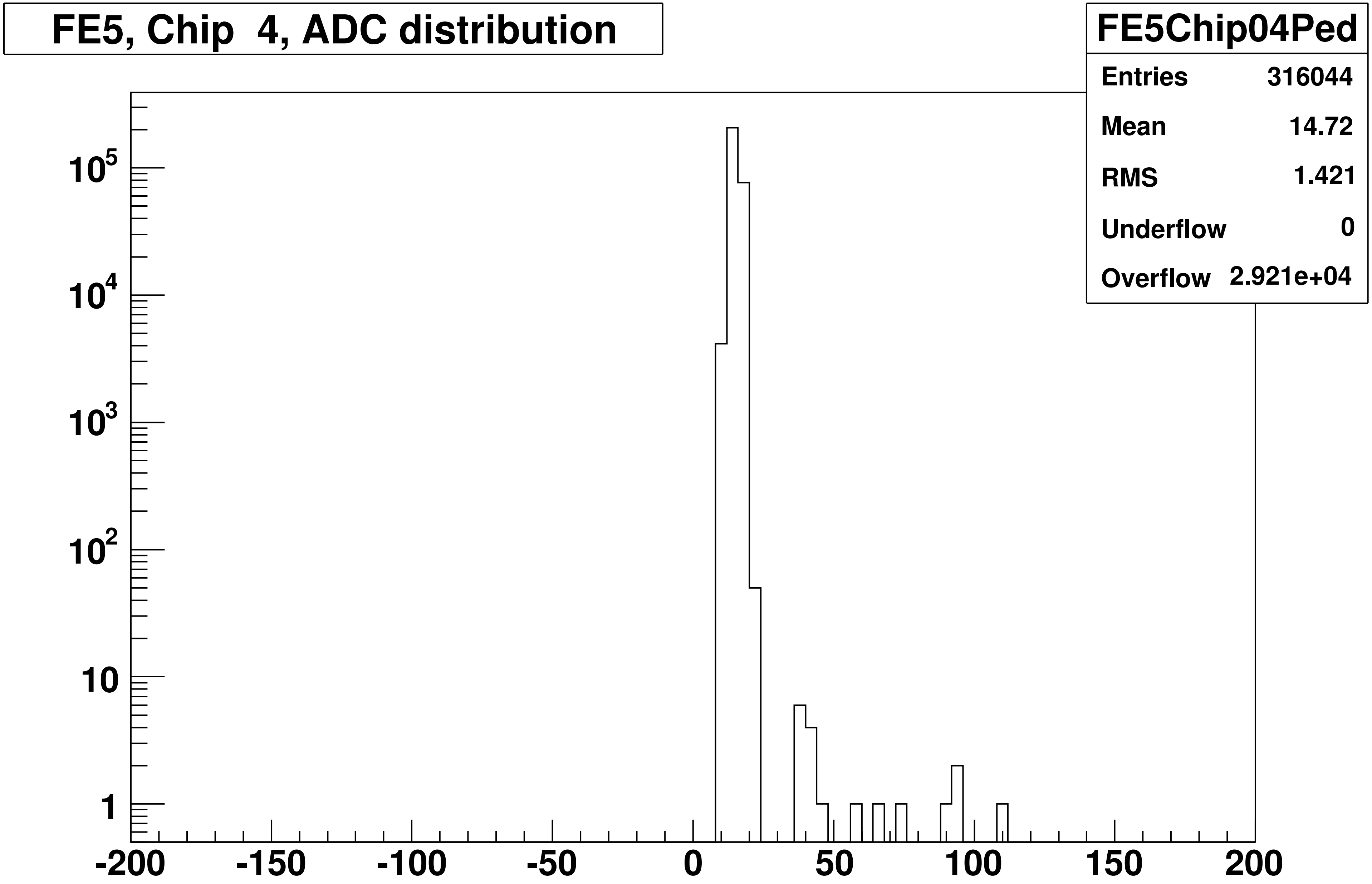
10000
15000
20000
25000


FE5, Chip 4, ADC distribution
FE5Chip04Ped
Entries 316044
Mean 14.72
RMS 1.421
Underflow 0
Overflow 2.921e+04
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10^4
10^3
10^2
10
1
-200
-150
-100
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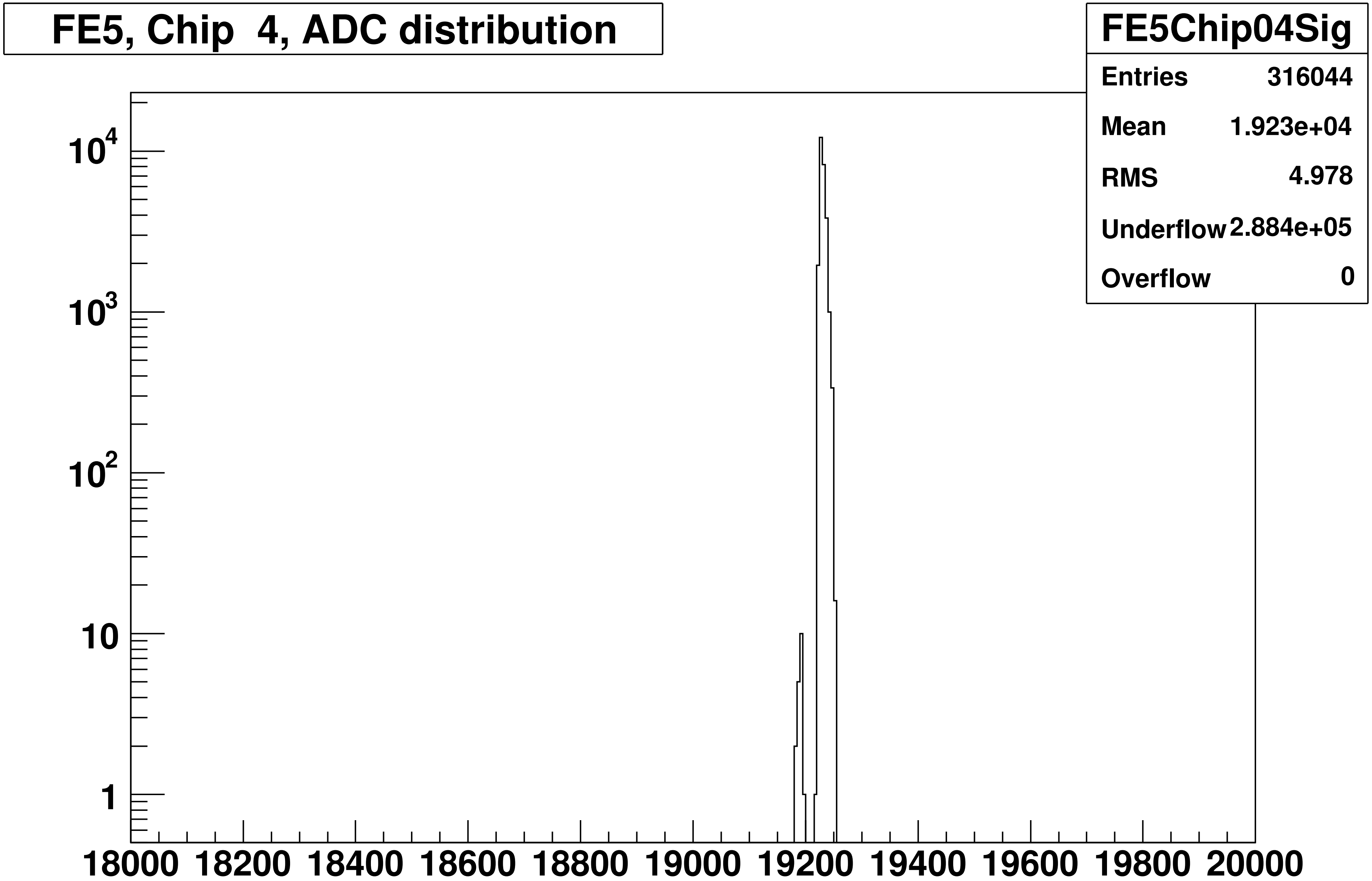
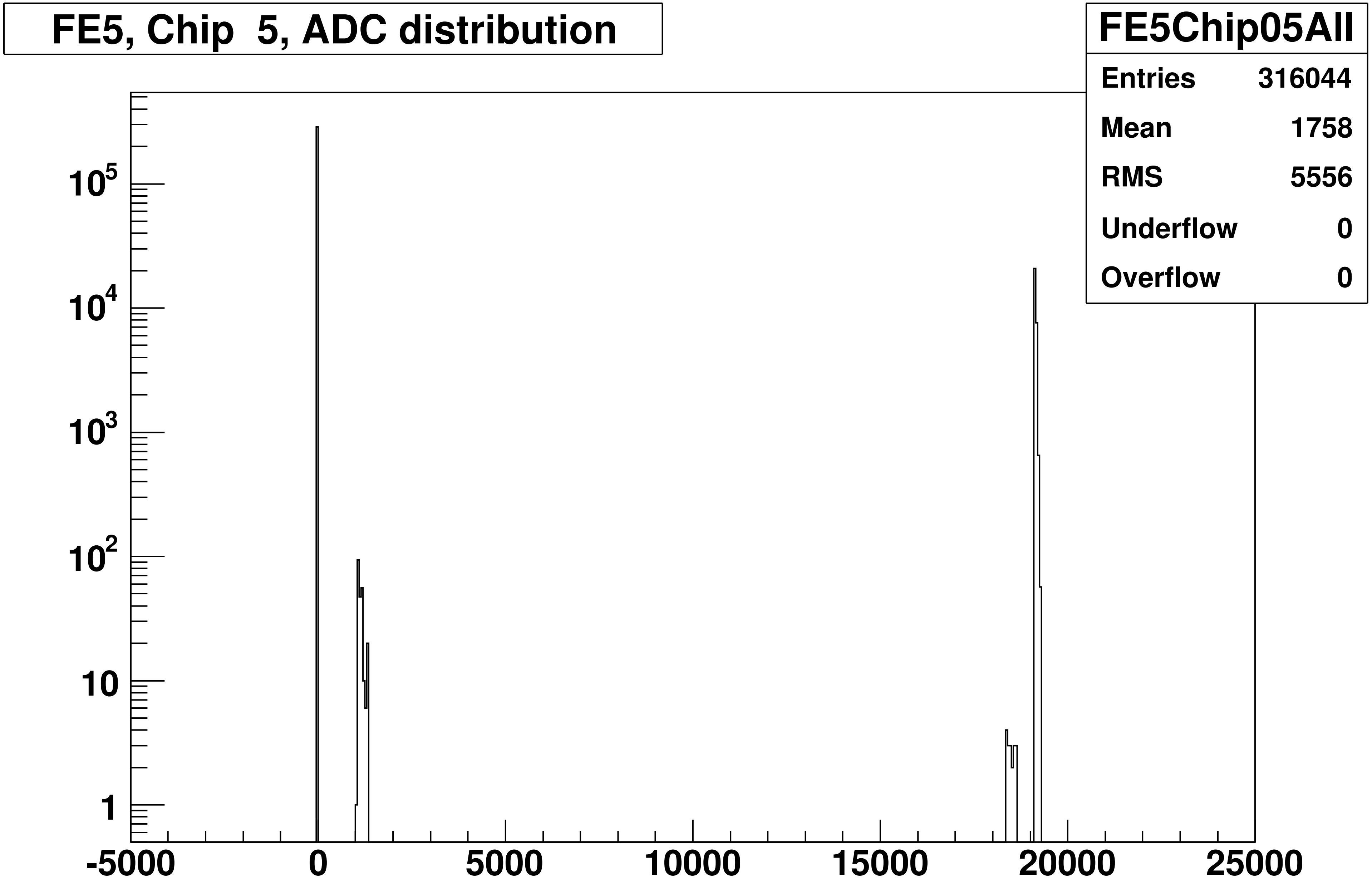
0
50
100
150
200


FE5, Chip 4, ADC distribution
FE5Chip04Sig
Entries 316044
Mean 1.923e+04
RMS 4.978
Underflow 2.884e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE5, Chip 5, ADC distribution
FE5Chip05All
Entries 316044
Mean 1758
RMS 5556
Underflow 0
Overflow 0
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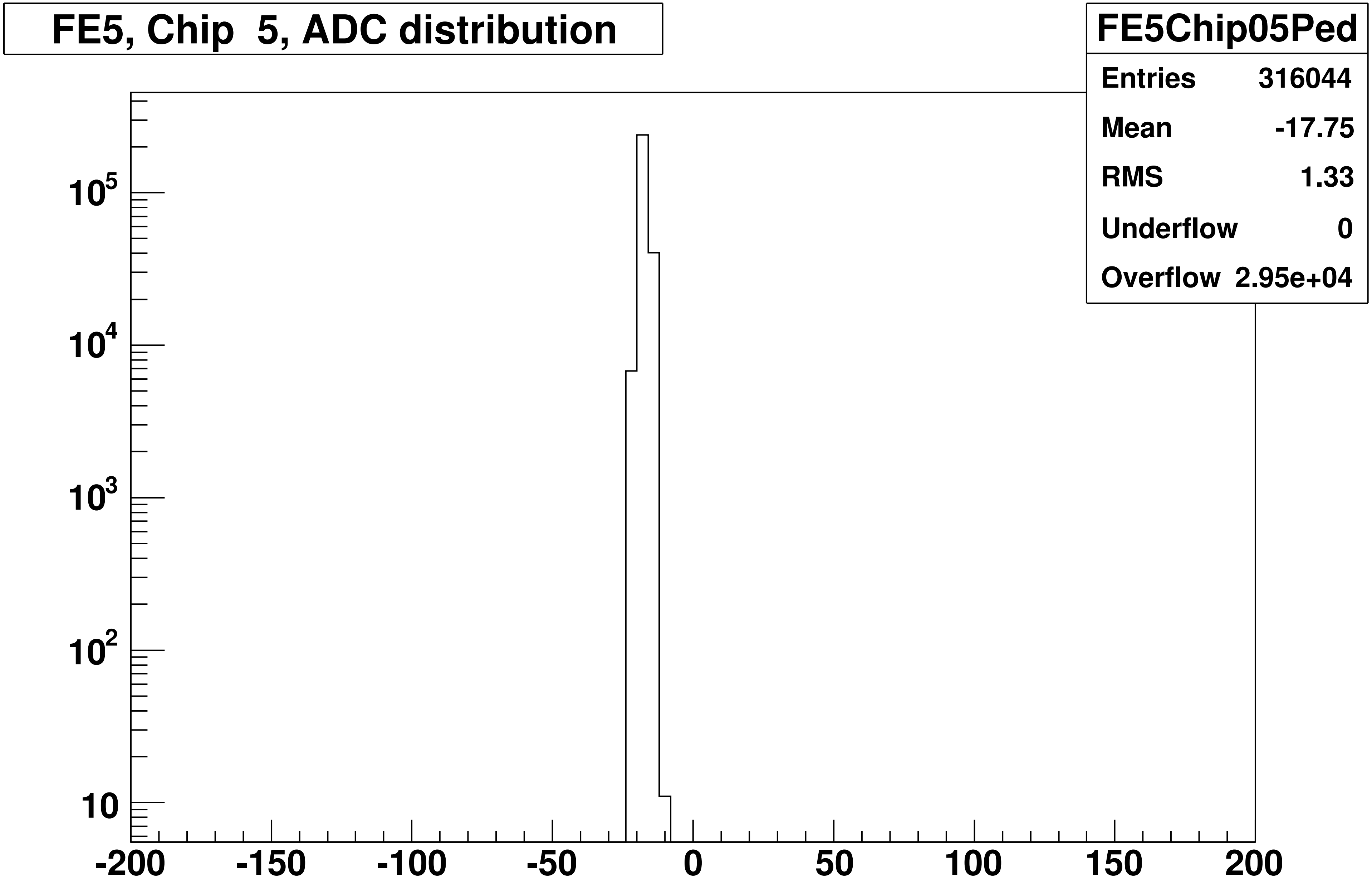
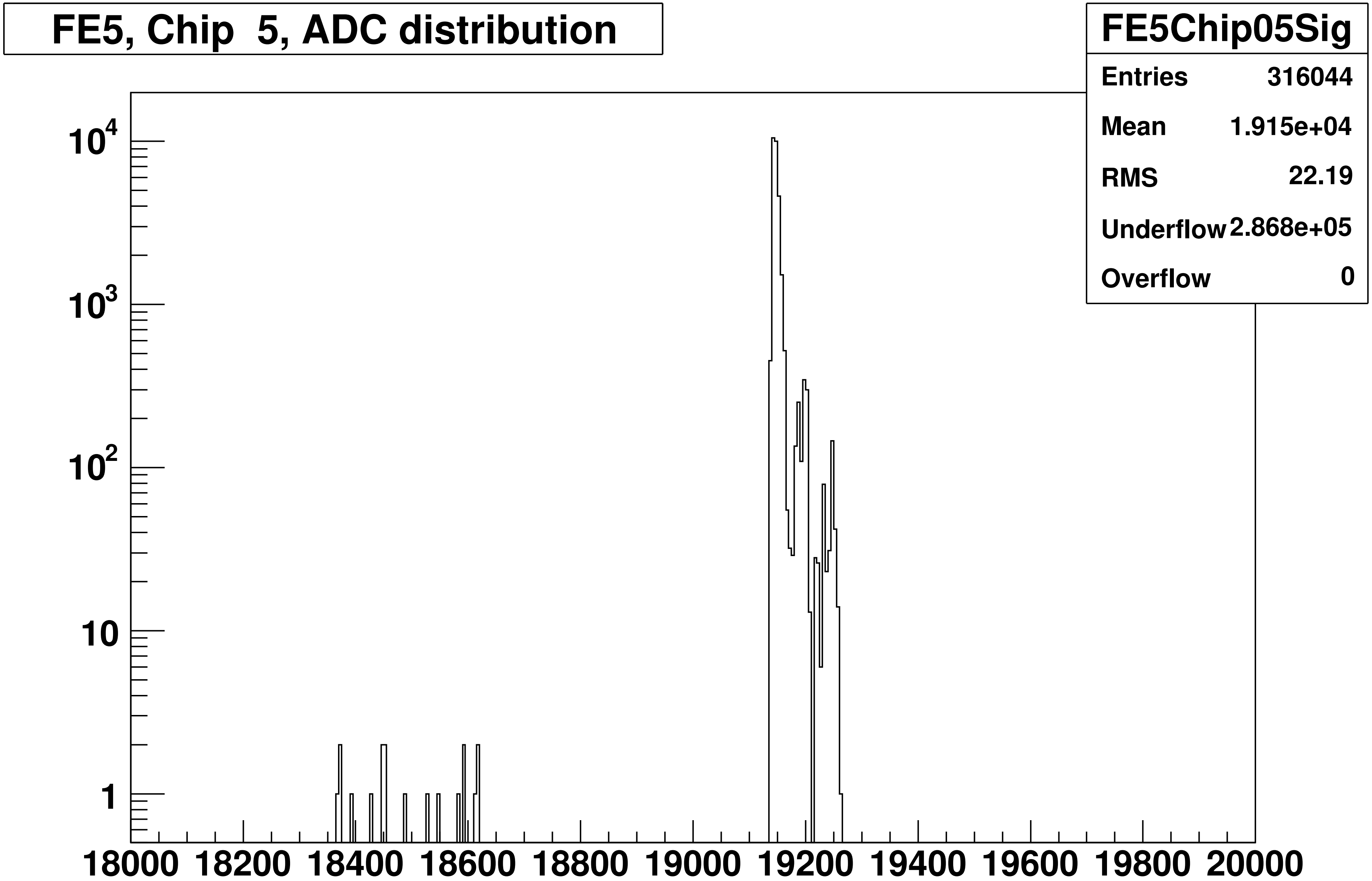
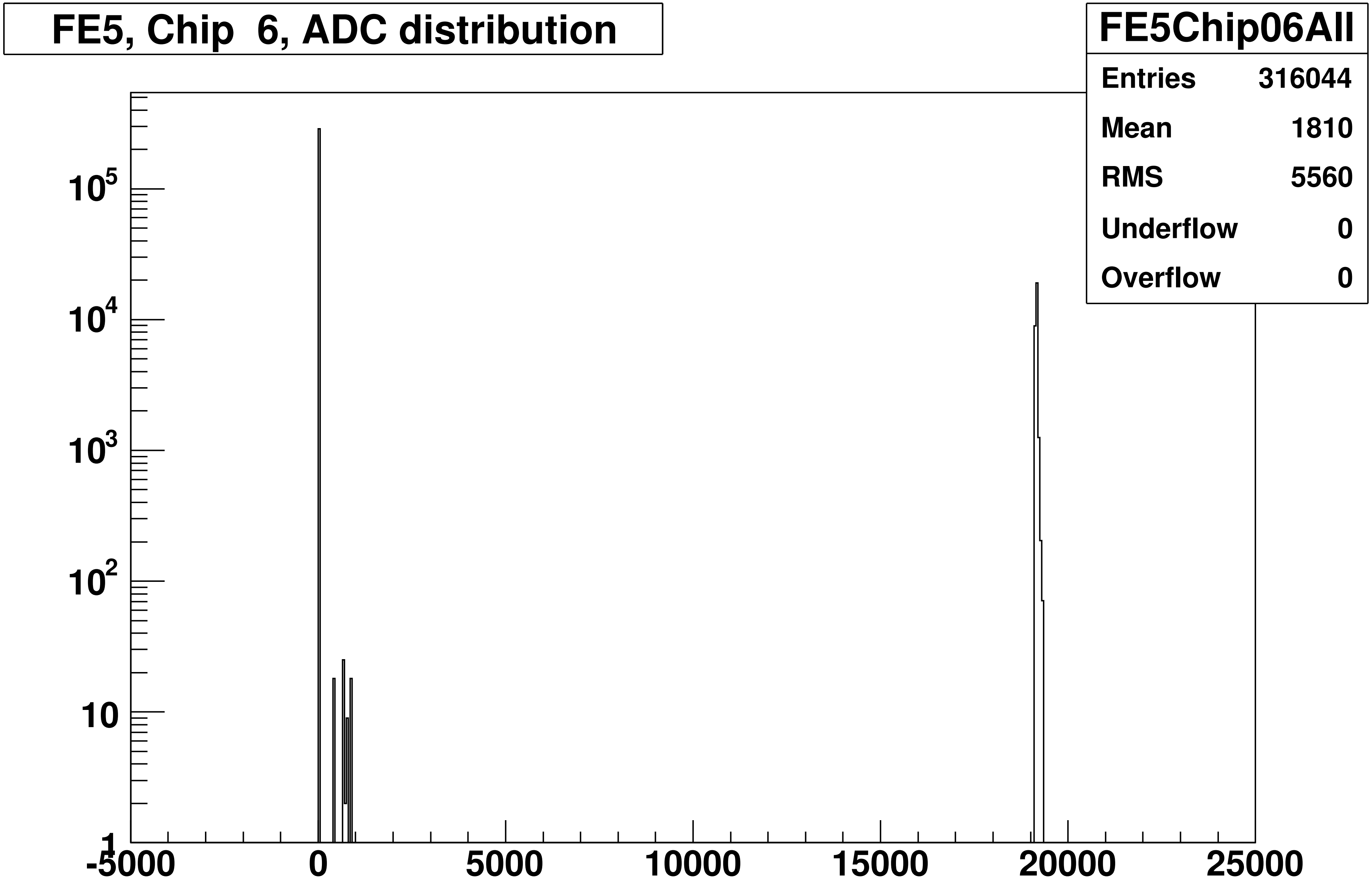
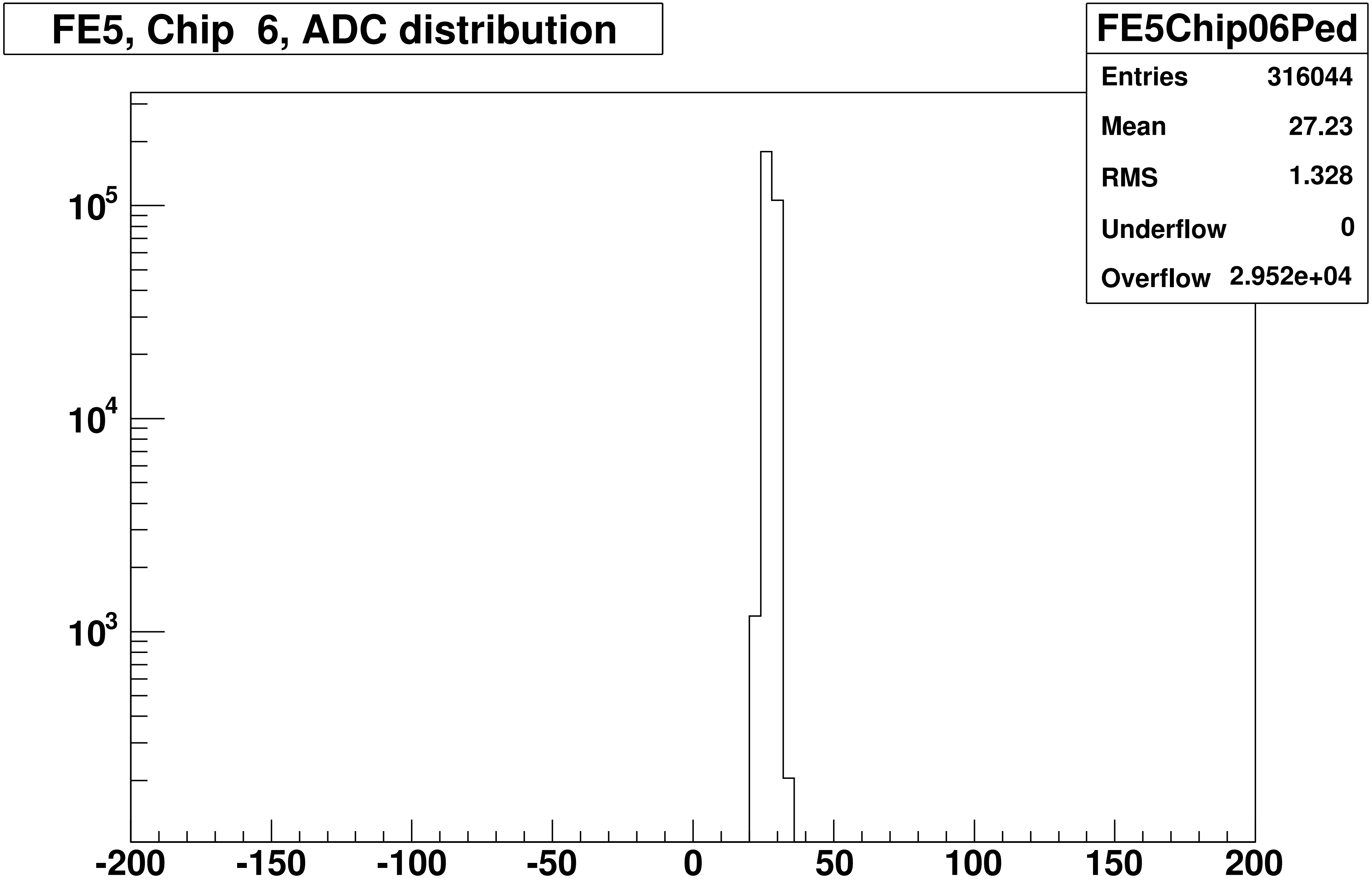
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000

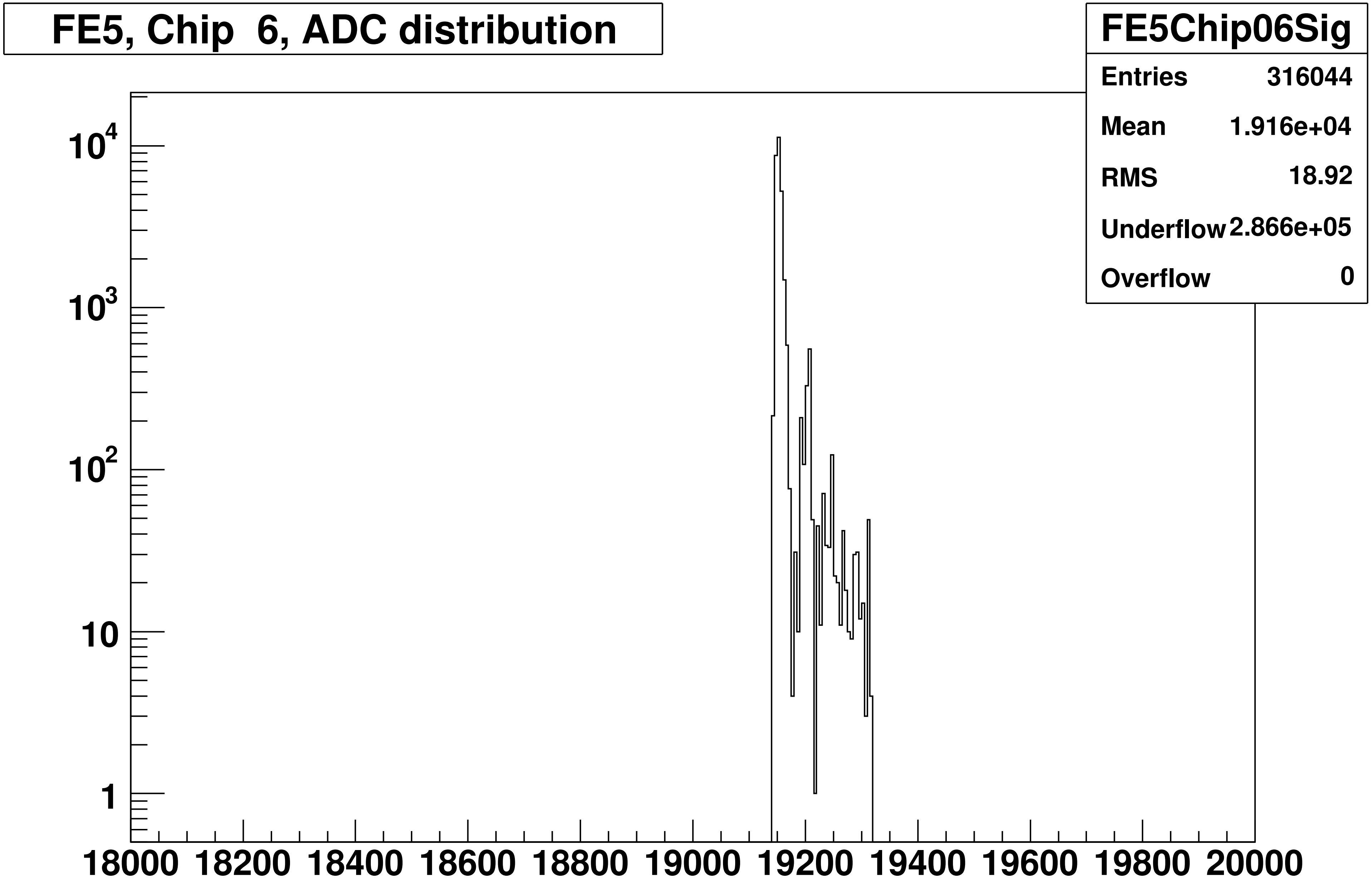

FE5, Chip 5, ADC distribution
FE5Chip05Ped
Entries 316044
Mean -17.75
RMS 1.33
Underflow 0
Overflow 2.95e+04
10^5
10^4
10^3
10^2
10
-200
-150
-100
-50
0
50
100
150
200

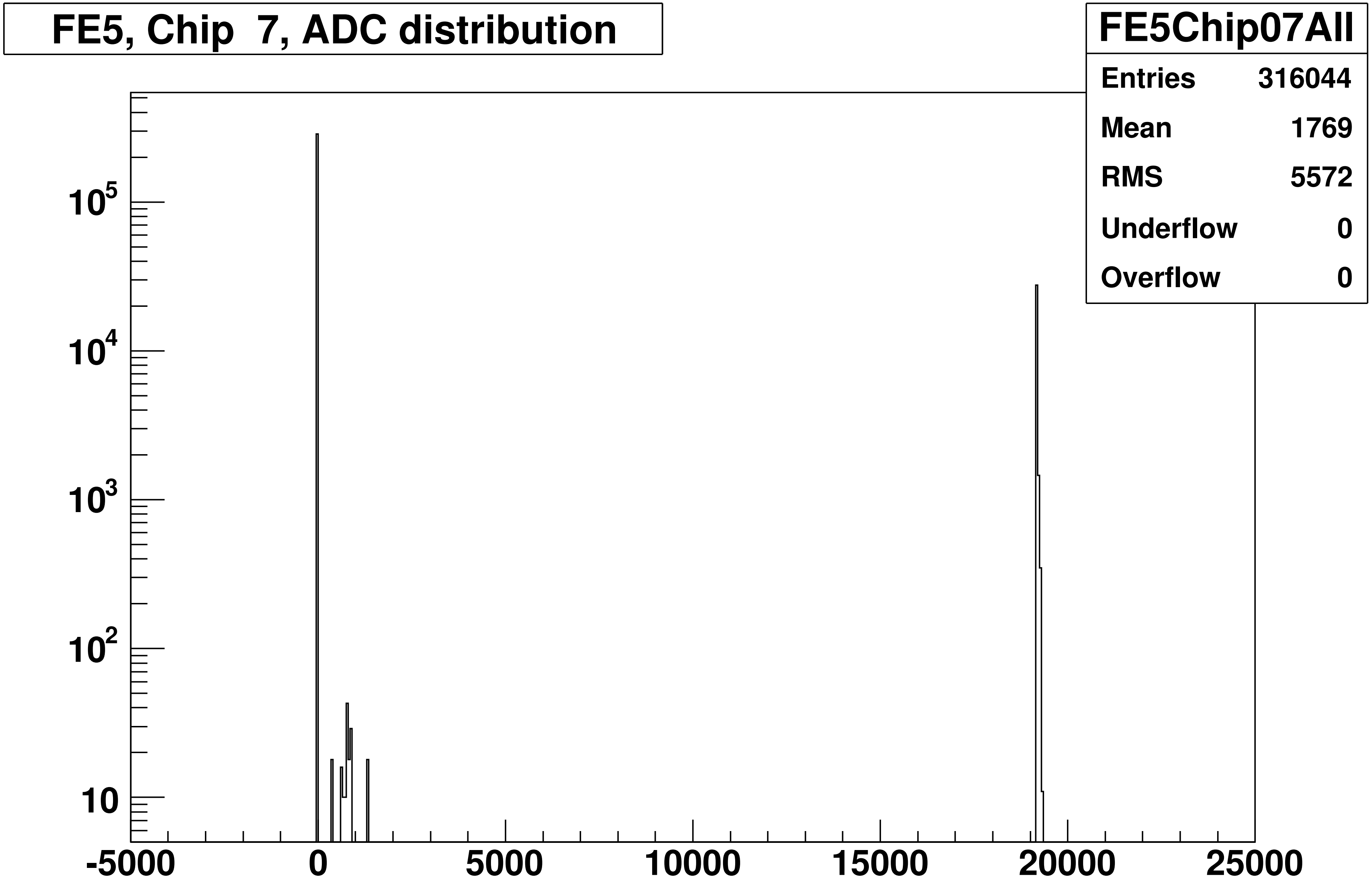


FE5, Chip 5, ADC distribution
FE5Chip05Sig
Entries 316044
Mean 1.915e+04
RMS 22.19
Underflow 2.868e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE5, Chip 6, ADC distribution
FE5Chip06All
Entries 316044
Mean 1810
RMS 5560
Underflow 0
Overflow 0
1
10
10^2
10^3
10^4
10^5
-5000
0
5000
10000
15000
20000
25000


FE5, Chip 6, ADC distribution
FE5Chip06Ped
Entries 316044
Mean 27.23
RMS 1.328
Underflow 0
Overflow 2.952e+04
10^5
10^4
10^3
-200
-150
-100
-50
0
50
100
150
200


FE5, Chip 6, ADC distribution
FE5Chip06Sig
Entries 316044
Mean 1.916e+04
RMS 18.92
Underflow 2.866e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE5, Chip 7, ADC distribution
FE5Chip07All
Entries 316044
Mean 1769
RMS 5572
Underflow 0
Overflow 0
10
10^2
10^3
10^4
10^5
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0
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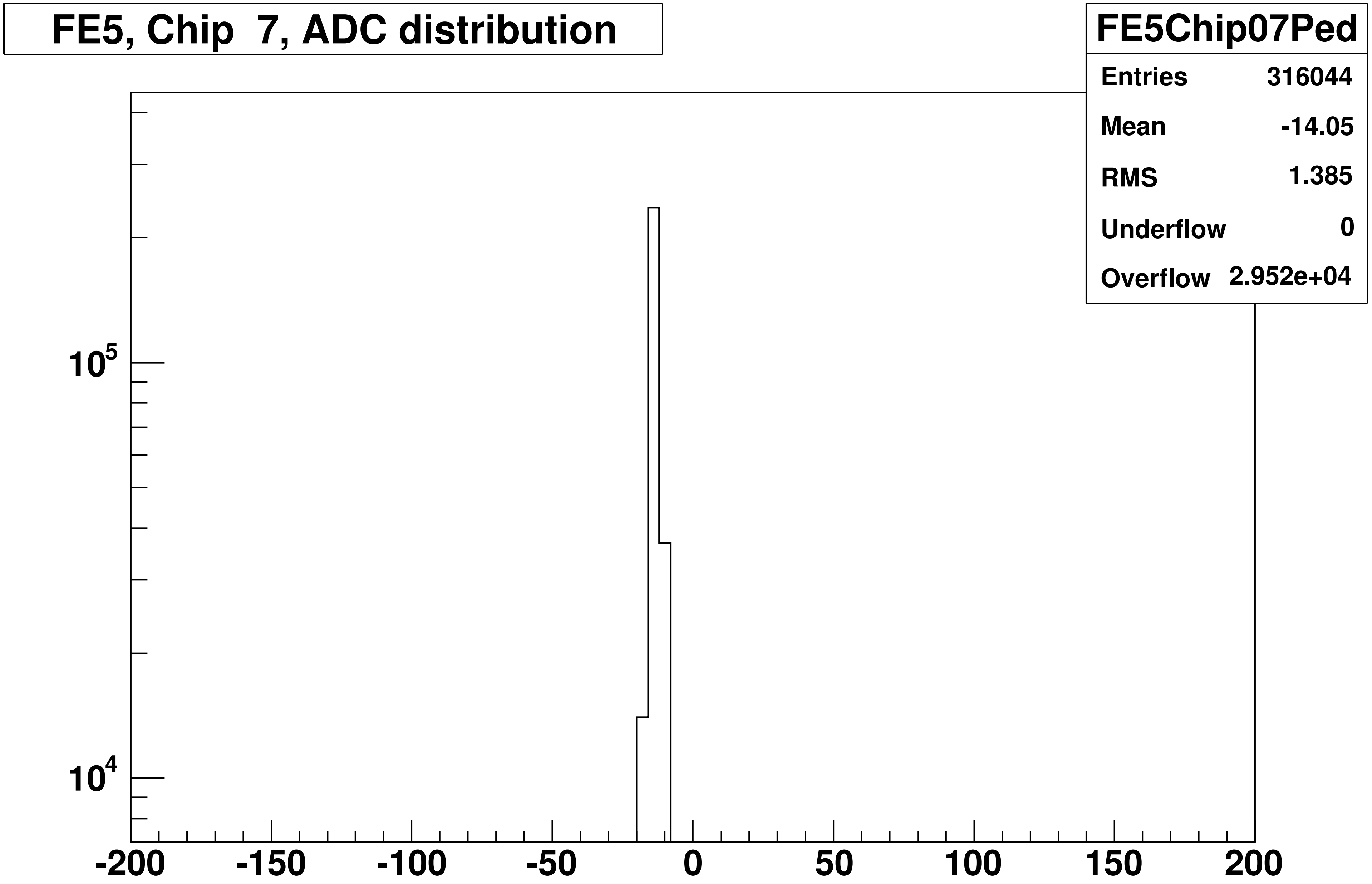
10000
15000
20000
25000


FE5, Chip 7, ADC distribution
FE5Chip07Ped
Entries 316044
Mean -14.05
RMS 1.385
Underflow 0
Overflow 2.952e+04
10^5
10^4
-200
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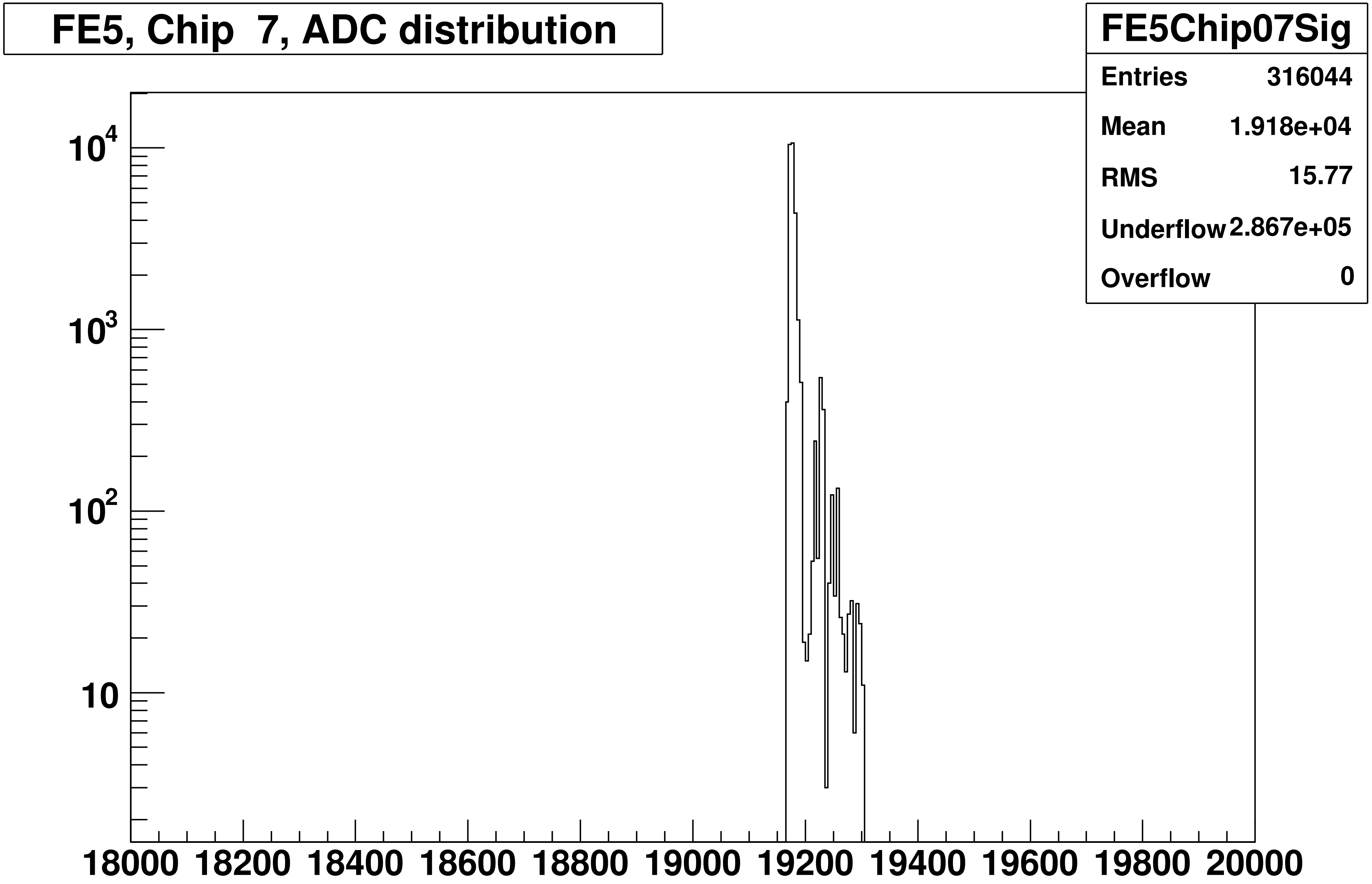
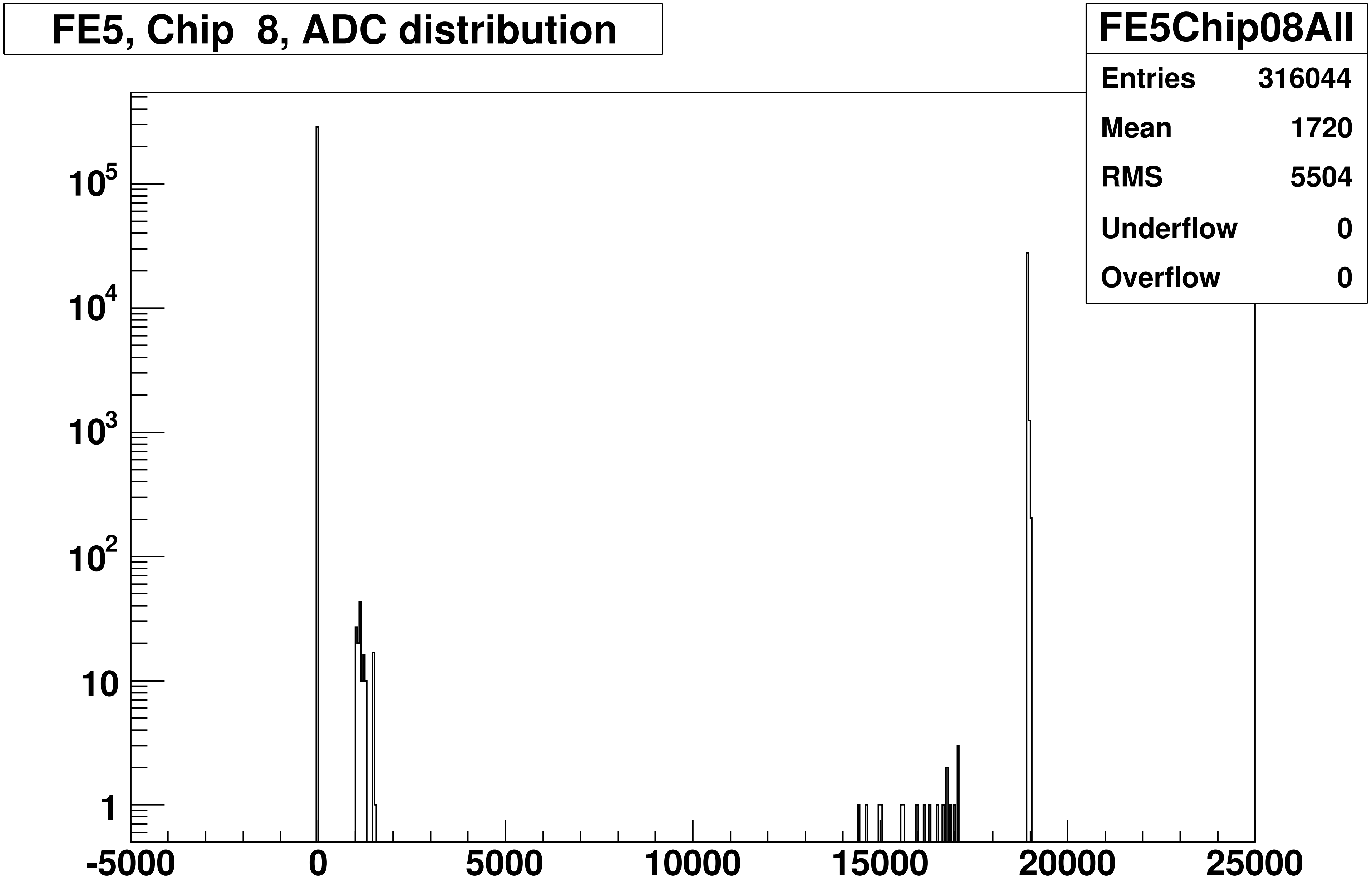
50
100
150
200


FE5, Chip 7, ADC distribution
FE5Chip07Sig
Entries 316044
Mean 1.918e+04
RMS 15.77
Underflow 2.867e+05
Overflow 0
10^4
10^3
10^2
10
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000


FE5, Chip 8, ADC distribution
FE5Chip08All
Entries 316044
Mean 1720
RMS 5504
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
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10000
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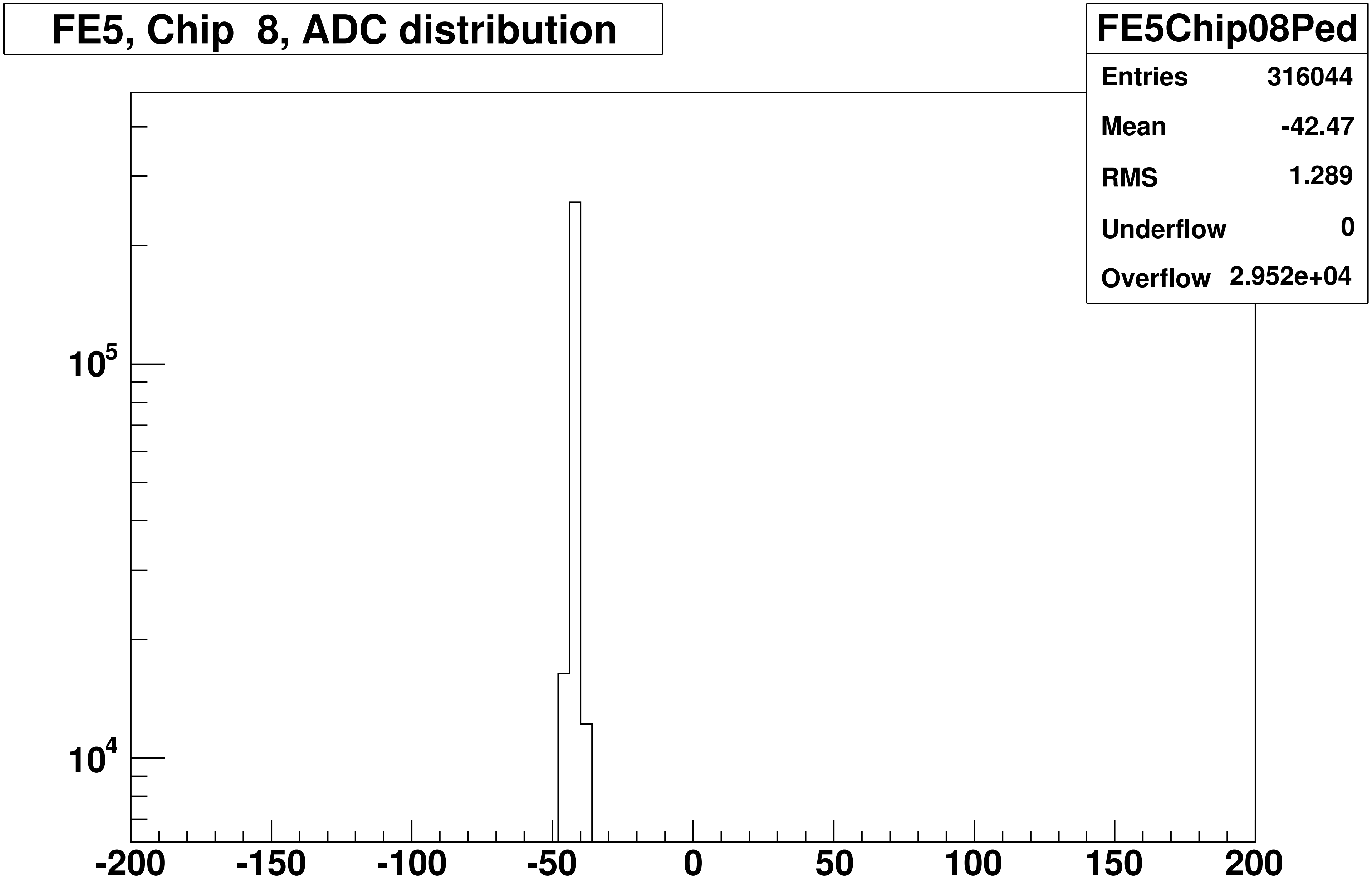
20000
25000


FE5, Chip 8, ADC distribution
FE5Chip08Ped
Entries 316044
Mean -42.47
RMS 1.289
Underflow 0
Overflow 2.952e+04
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10^4
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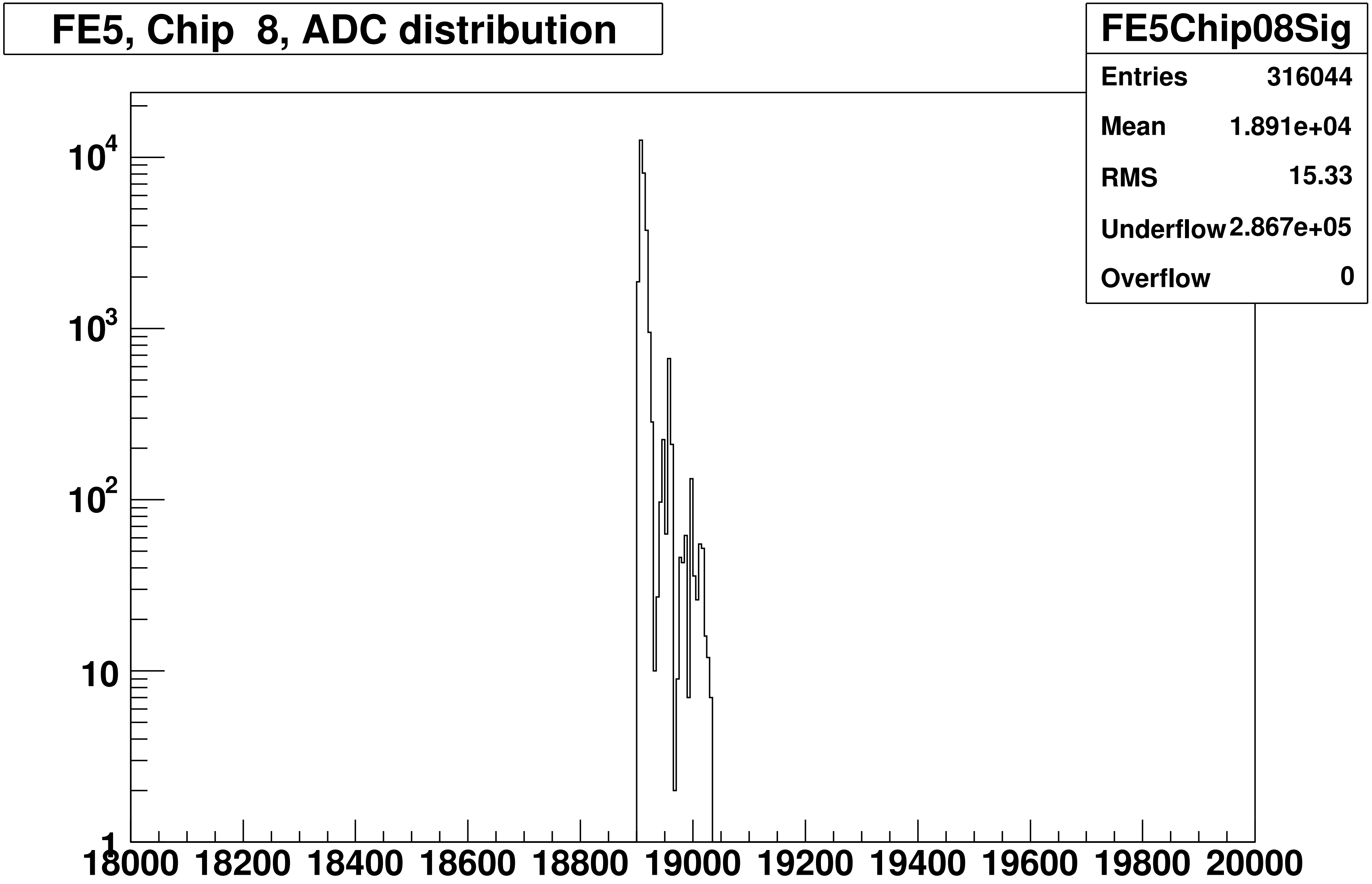
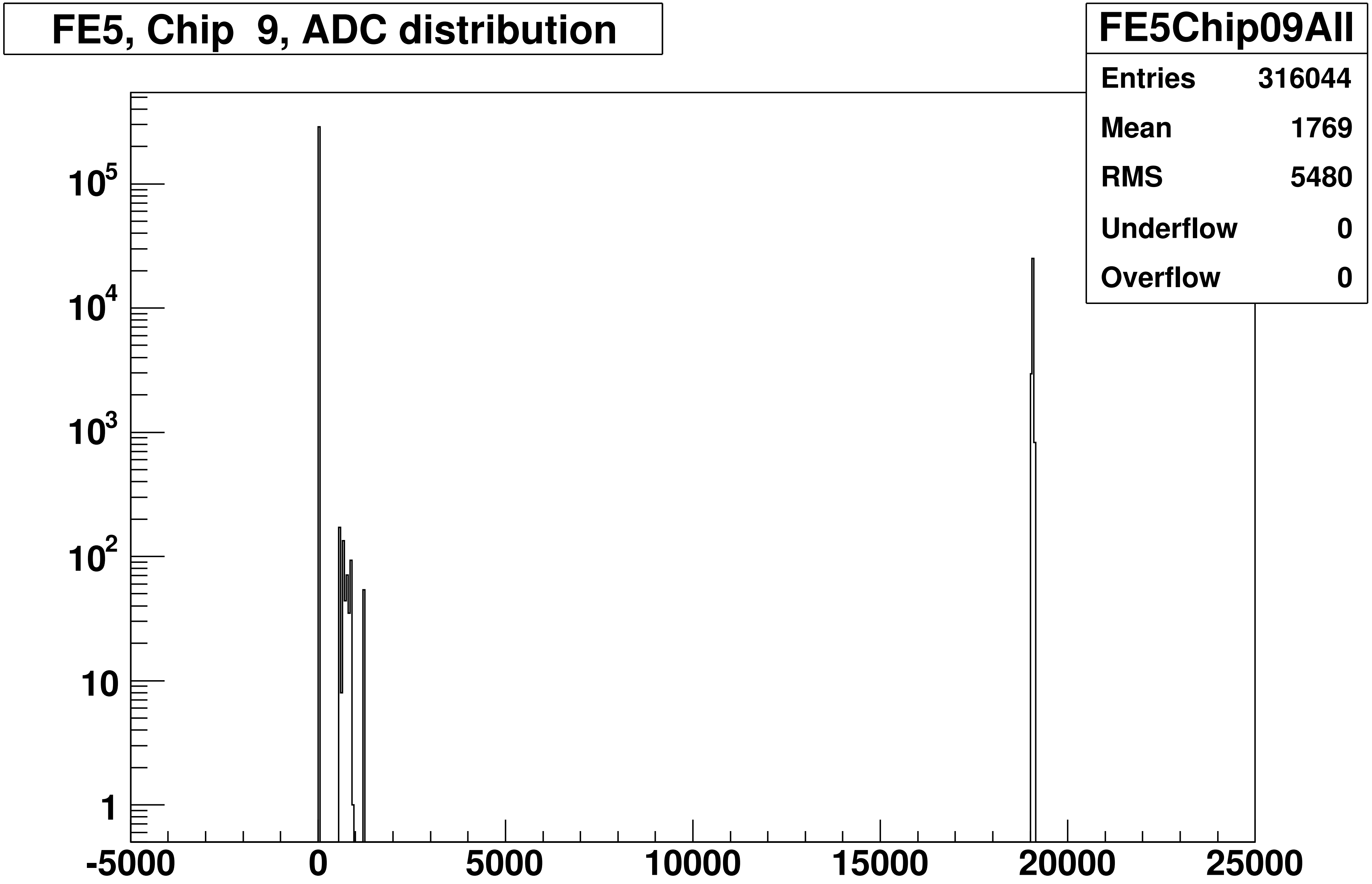
150
200


FE5, Chip 8, ADC distribution
FE5Chip08Sig
Entries 316044
Mean 1.891e+04
RMS 15.33
Underflow 2.867e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE5, Chip 9, ADC distribution
FE5Chip09All
Entries 316044
Mean 1769
RMS 5480
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
1
-5000
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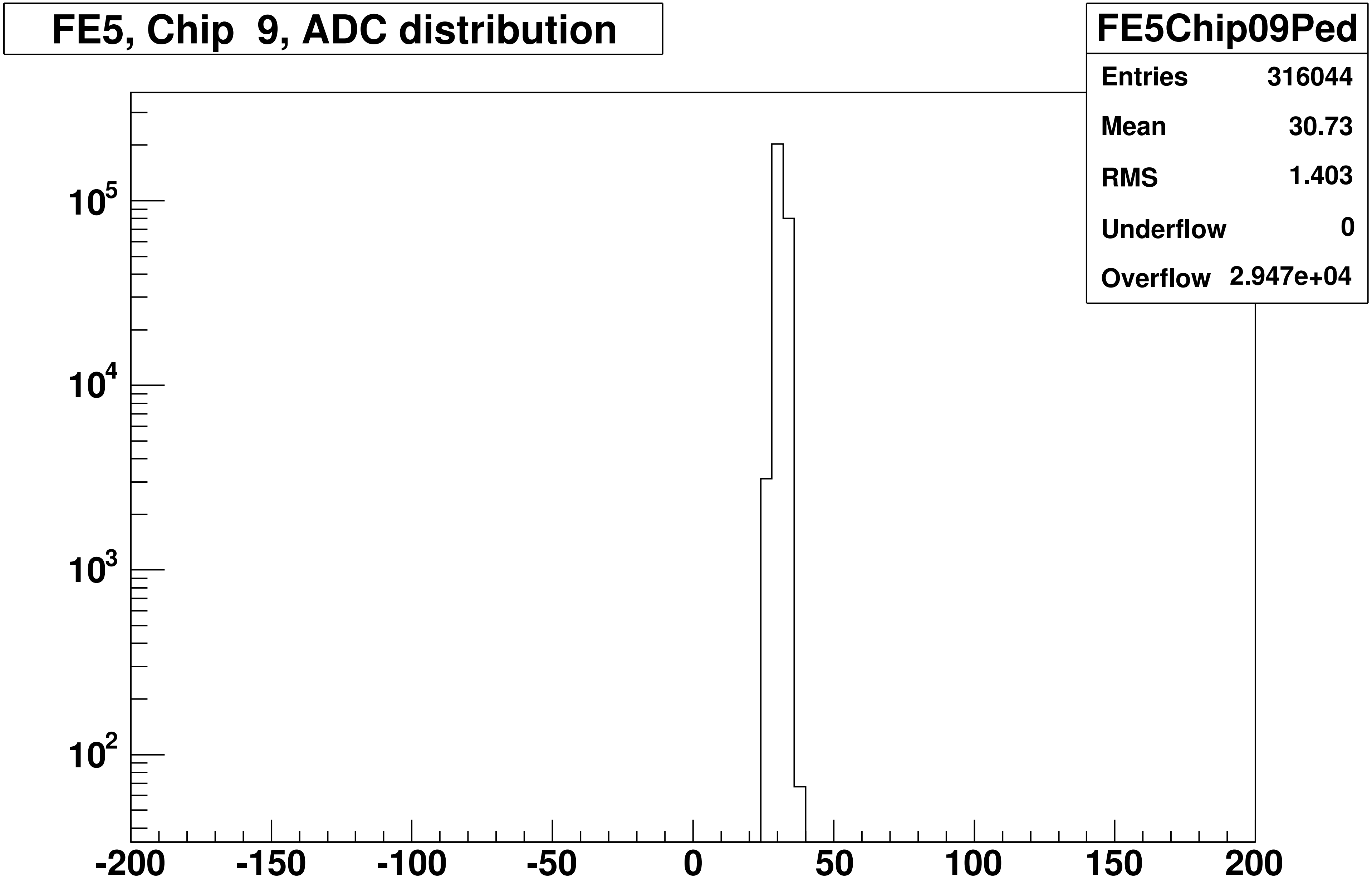
5000
10000
15000
20000
25000


FE5, Chip 9, ADC distribution
FE5Chip09Ped
Entries 316044
Mean 30.73
RMS 1.403
Underflow 0
Overflow 2.947e+04
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10^4
10^3
10^2
-200
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-100
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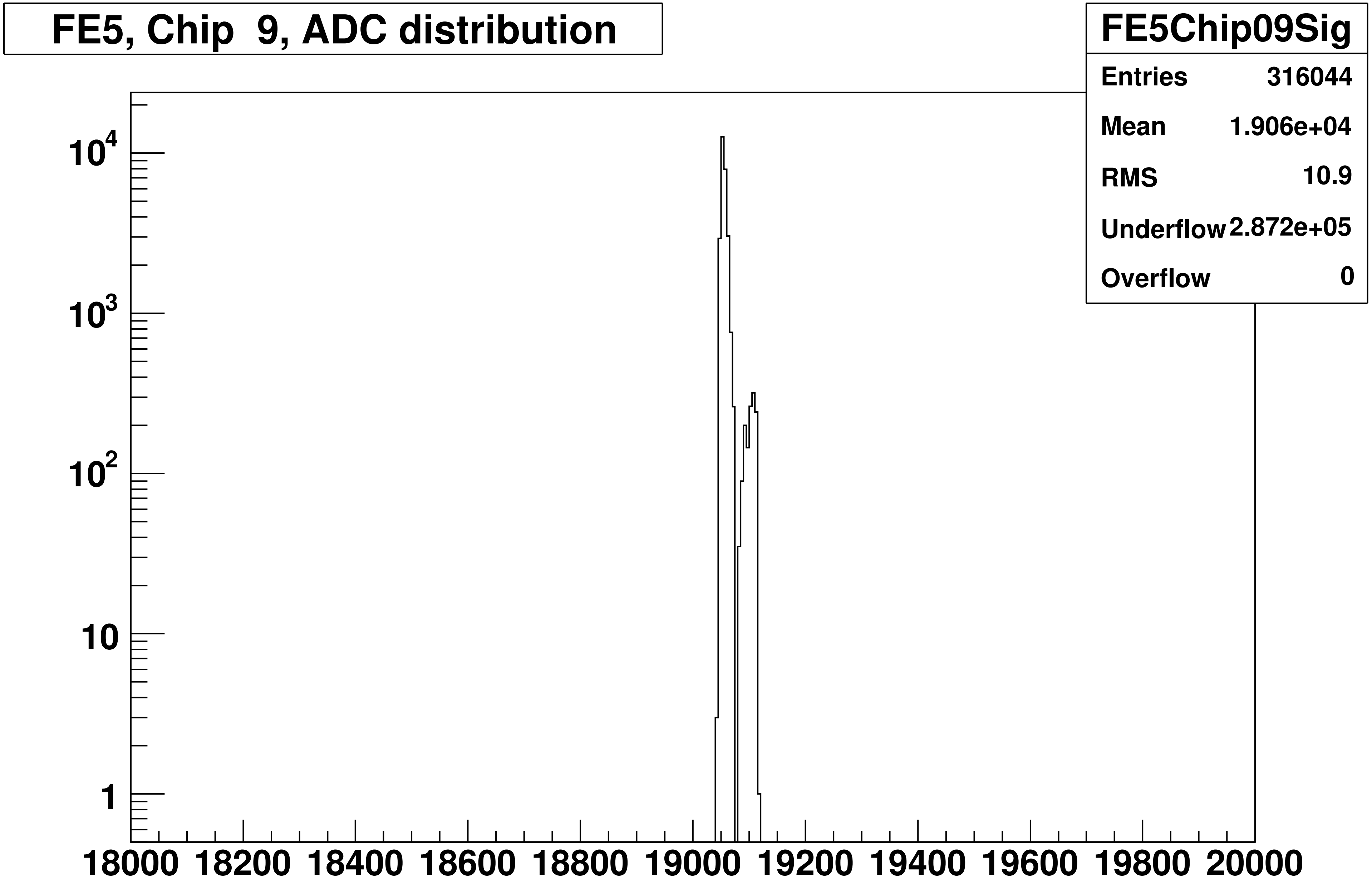
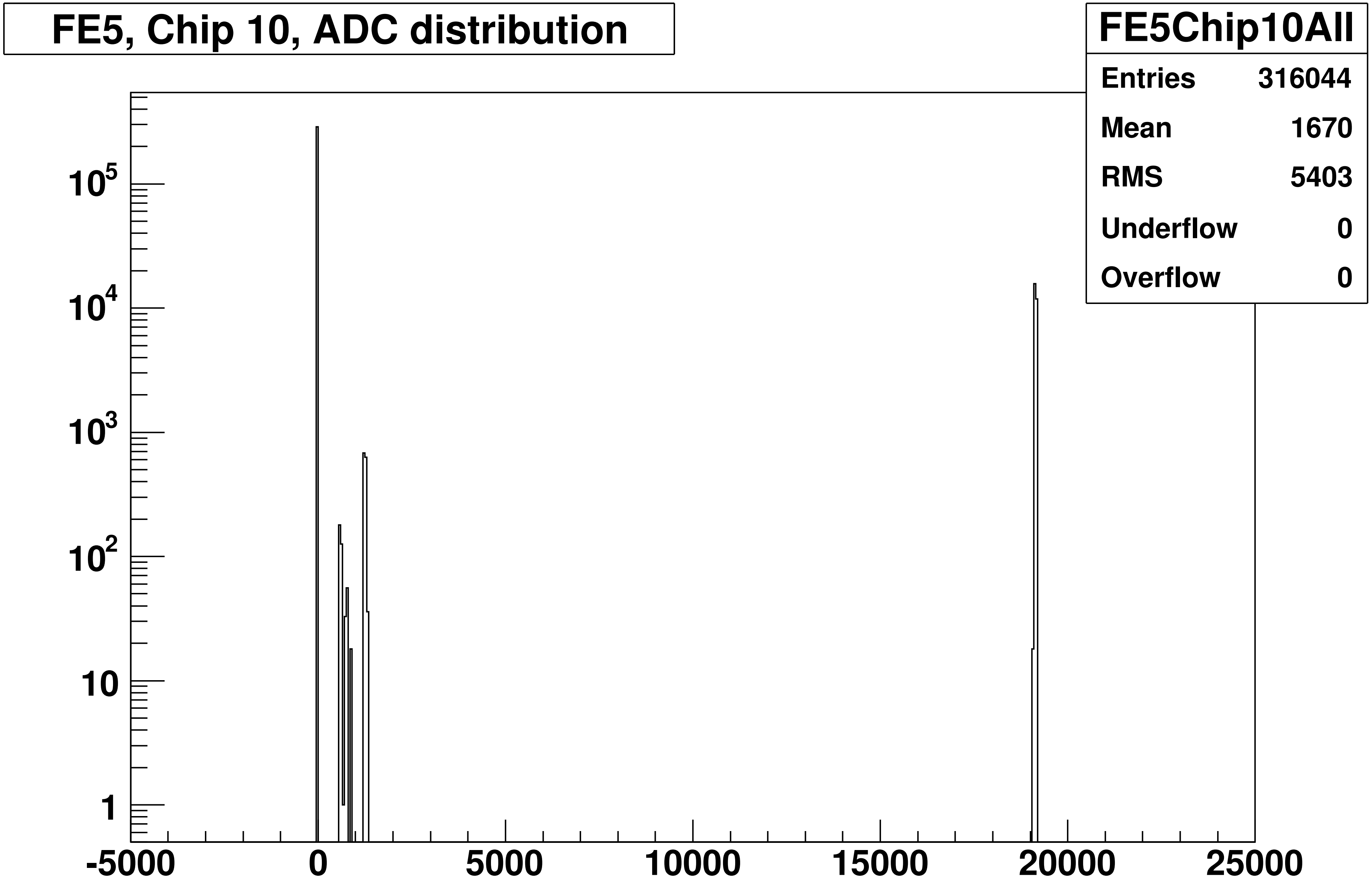
0
50
100
150
200



FE5, Chip 9, ADC distribution
FE5Chip09Sig
Entries 316044
Mean 1.906e+04
RMS 10.9
Underflow 2.872e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000


FE5, Chip 10, ADC distribution
FE5Chip10All
Entries 316044
Mean 1670
RMS 5403
Underflow 0
Overflow 0
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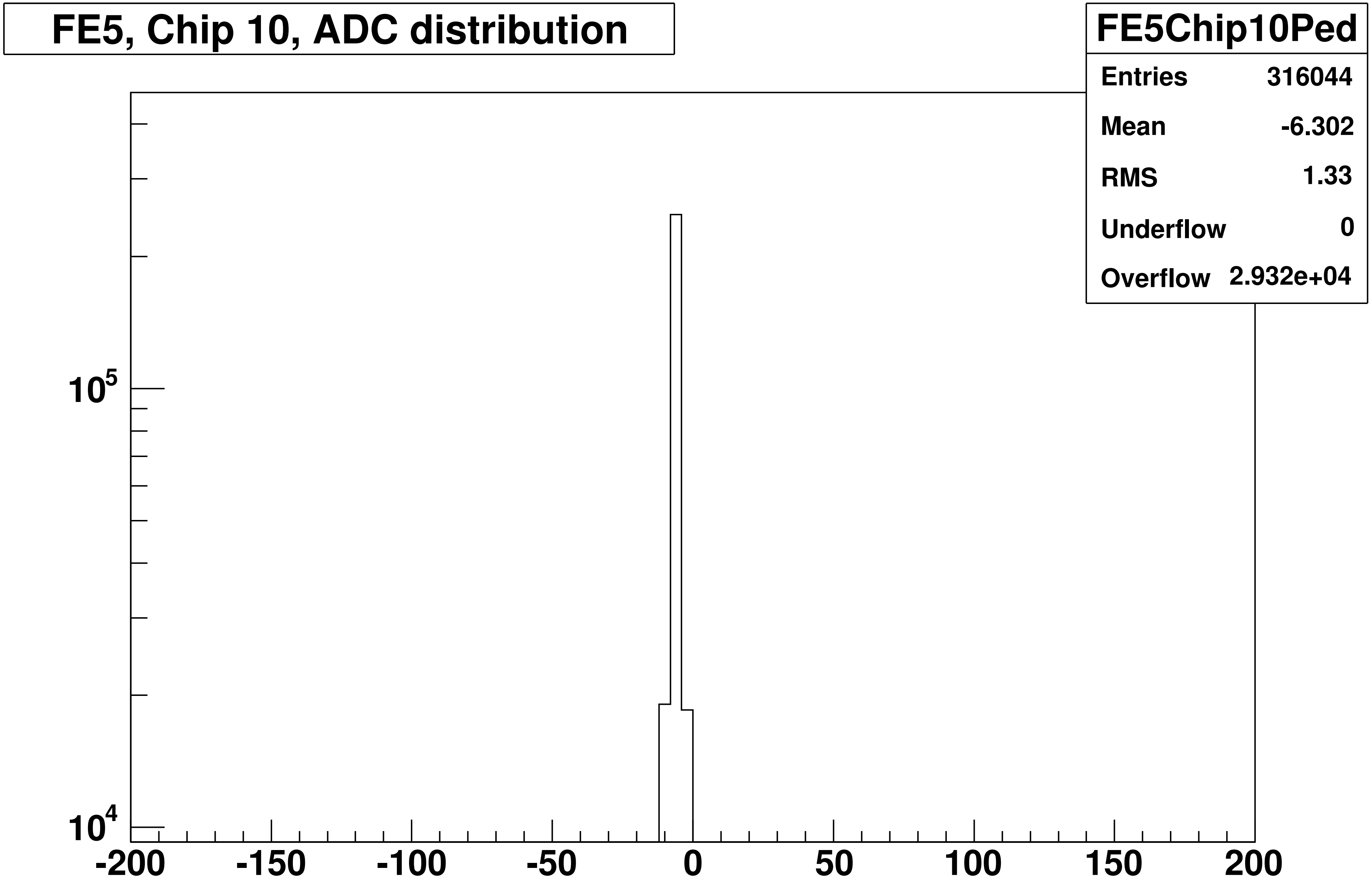
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE5, Chip 10, ADC distribution
FE5Chip10Ped
Entries 316044
Mean -6.302
RMS 1.33
Underflow 0
Overflow 2.932e+04
10^5
10^4
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-100
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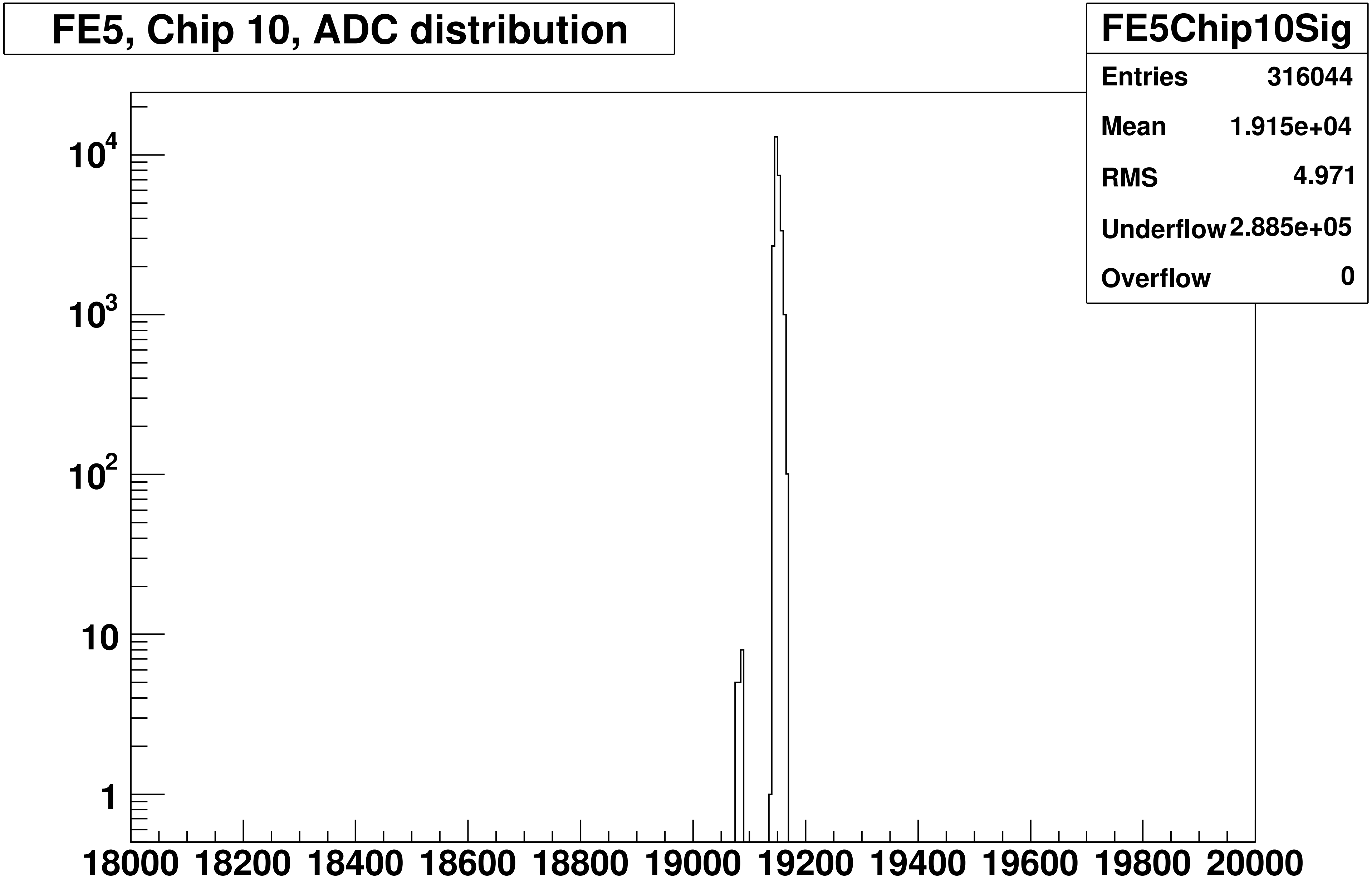
150
200


FE5, Chip 10, ADC distribution
FE5Chip10Sig
Entries 316044
Mean 1.915e+04
RMS 4.971
Underflow 2.885e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
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19000
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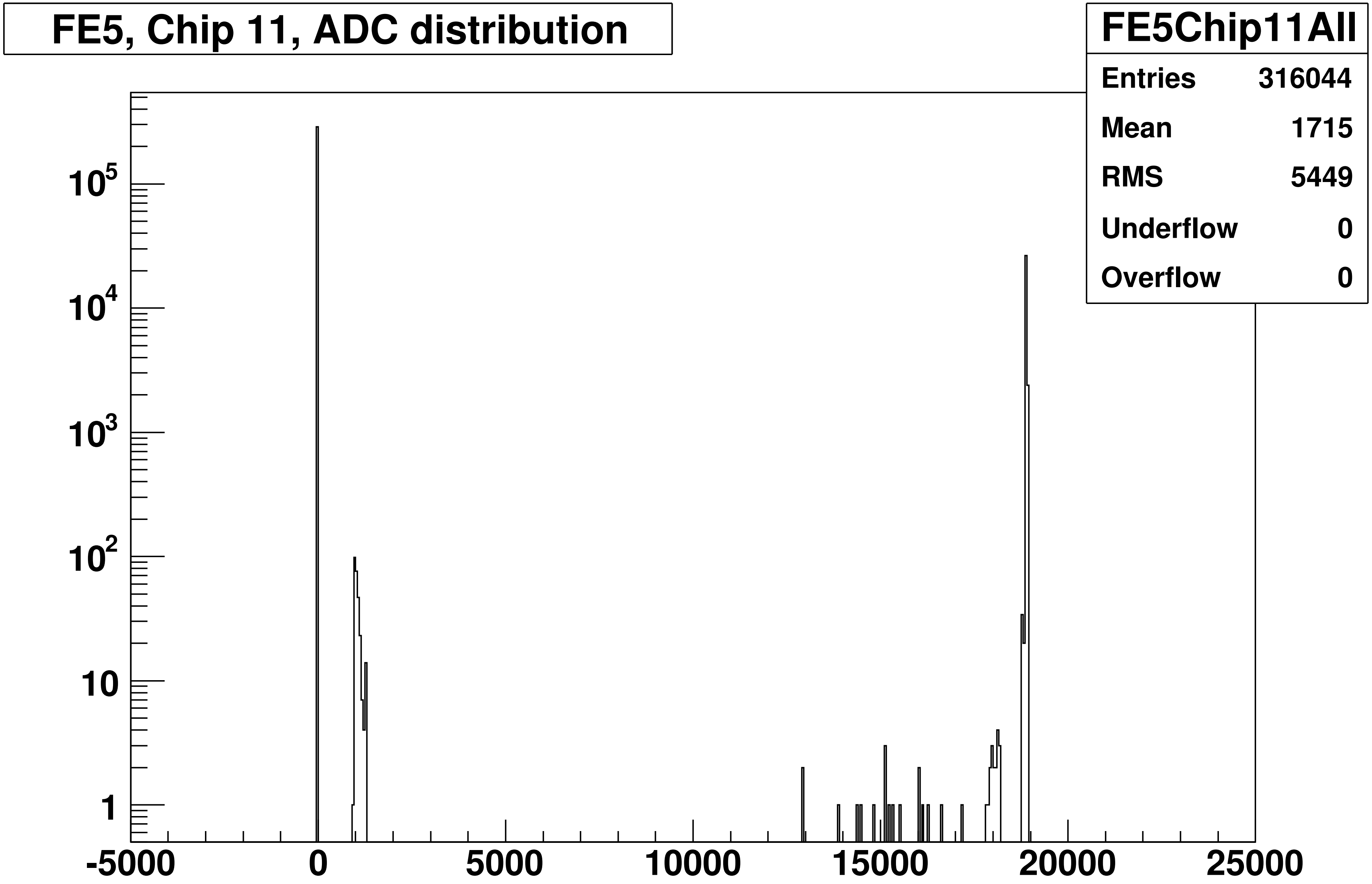
19400
19600
19800
20000



FE5, Chip 11, ADC distribution
FE5Chip11All
Entries 316044
Mean 1715
RMS 5449
Underflow 0
Overflow 0
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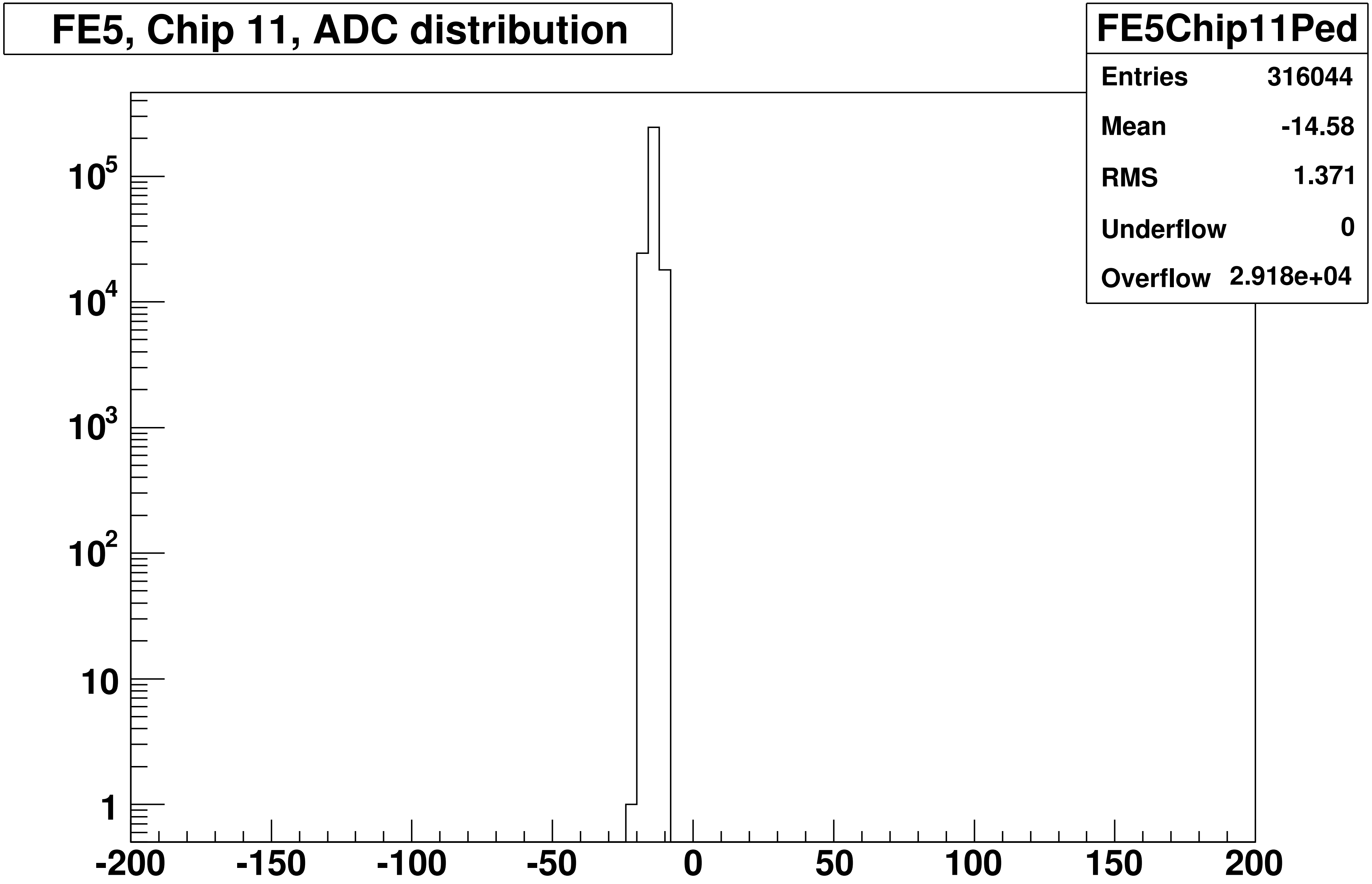
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE5, Chip 11, ADC distribution
FE5Chip11Ped
Entries 316044
Mean -14.58
RMS 1.371
Underflow 0
Overflow 2.918e+04
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10^4
10^3
10^2
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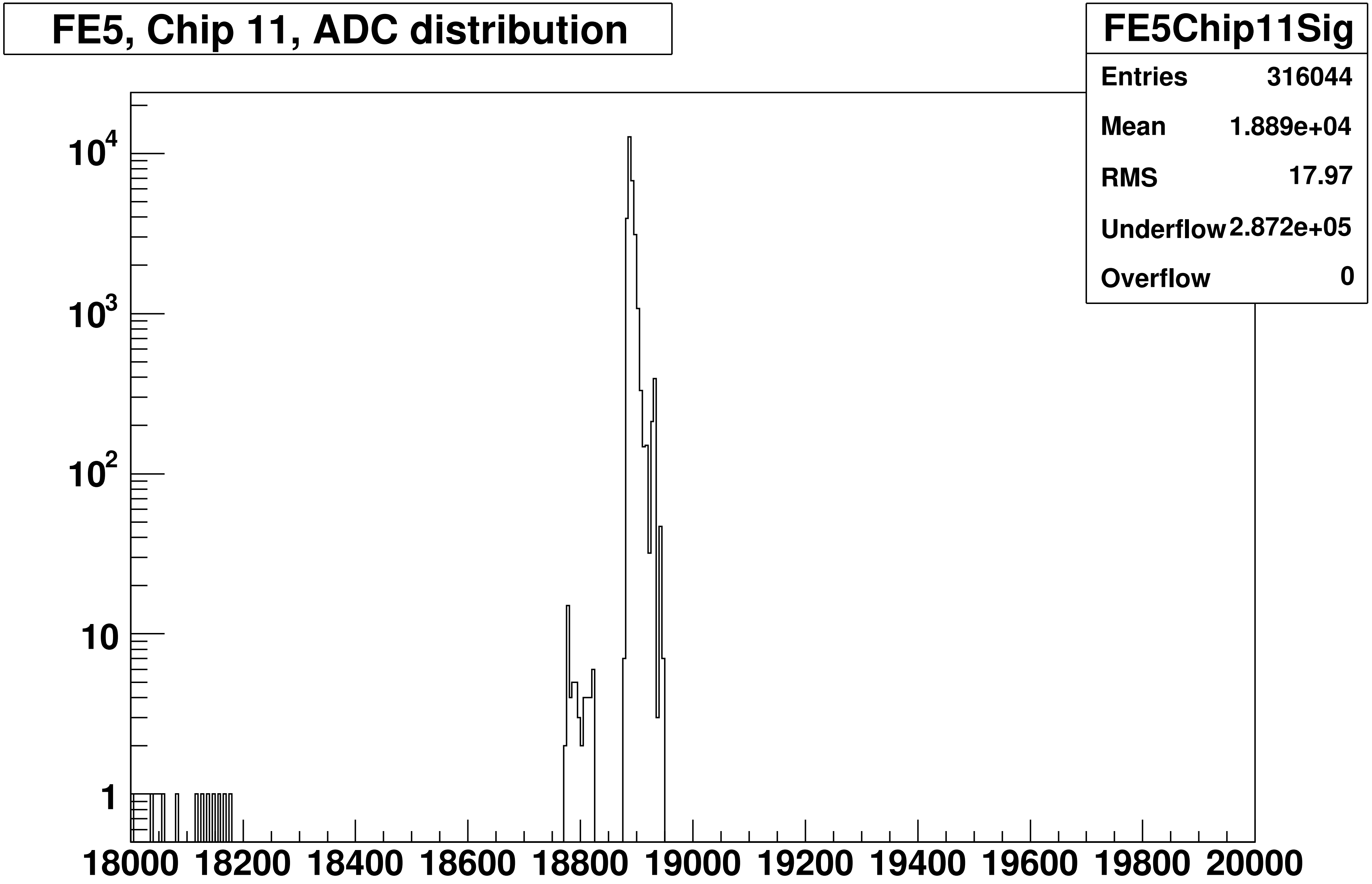
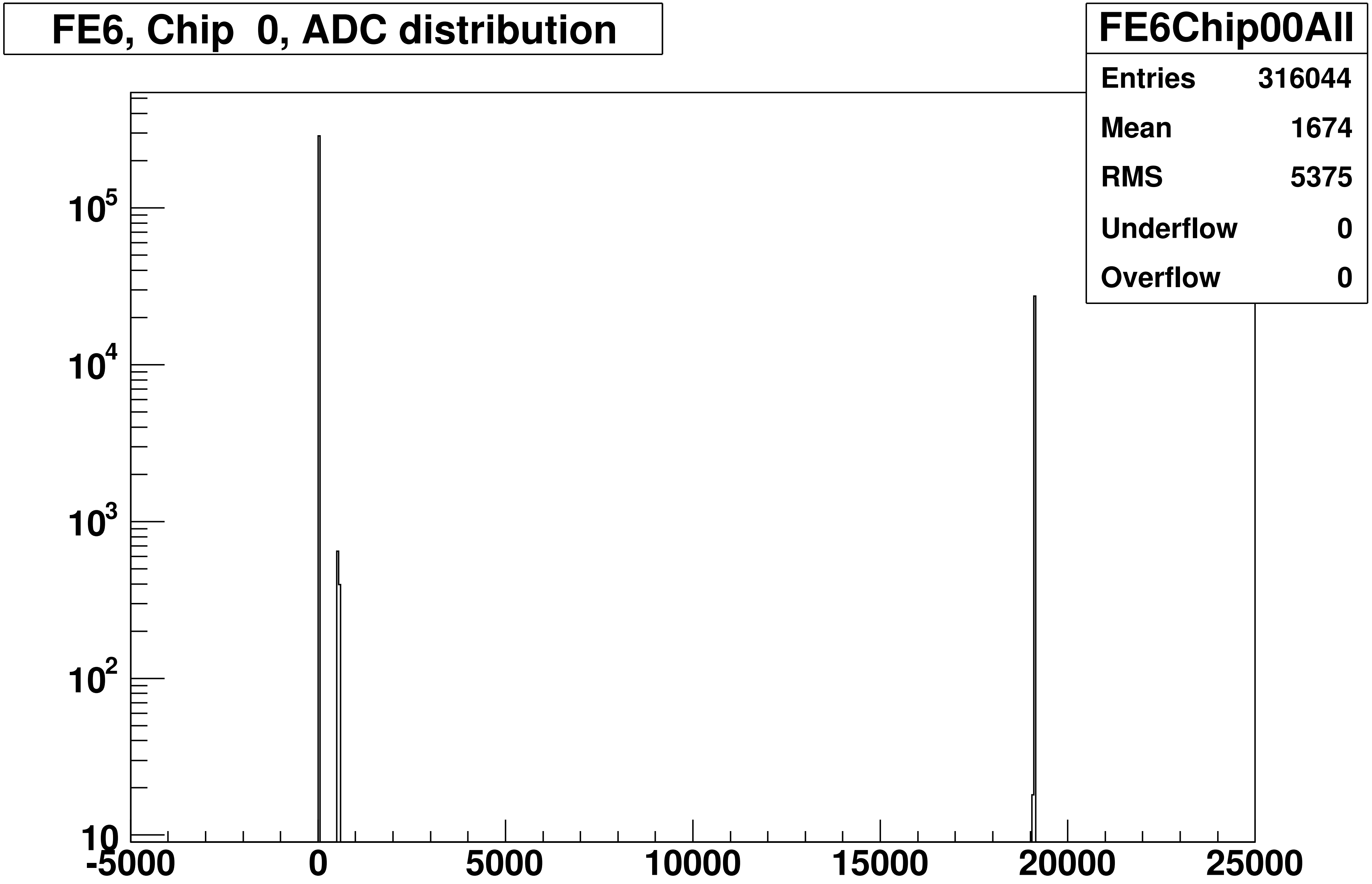
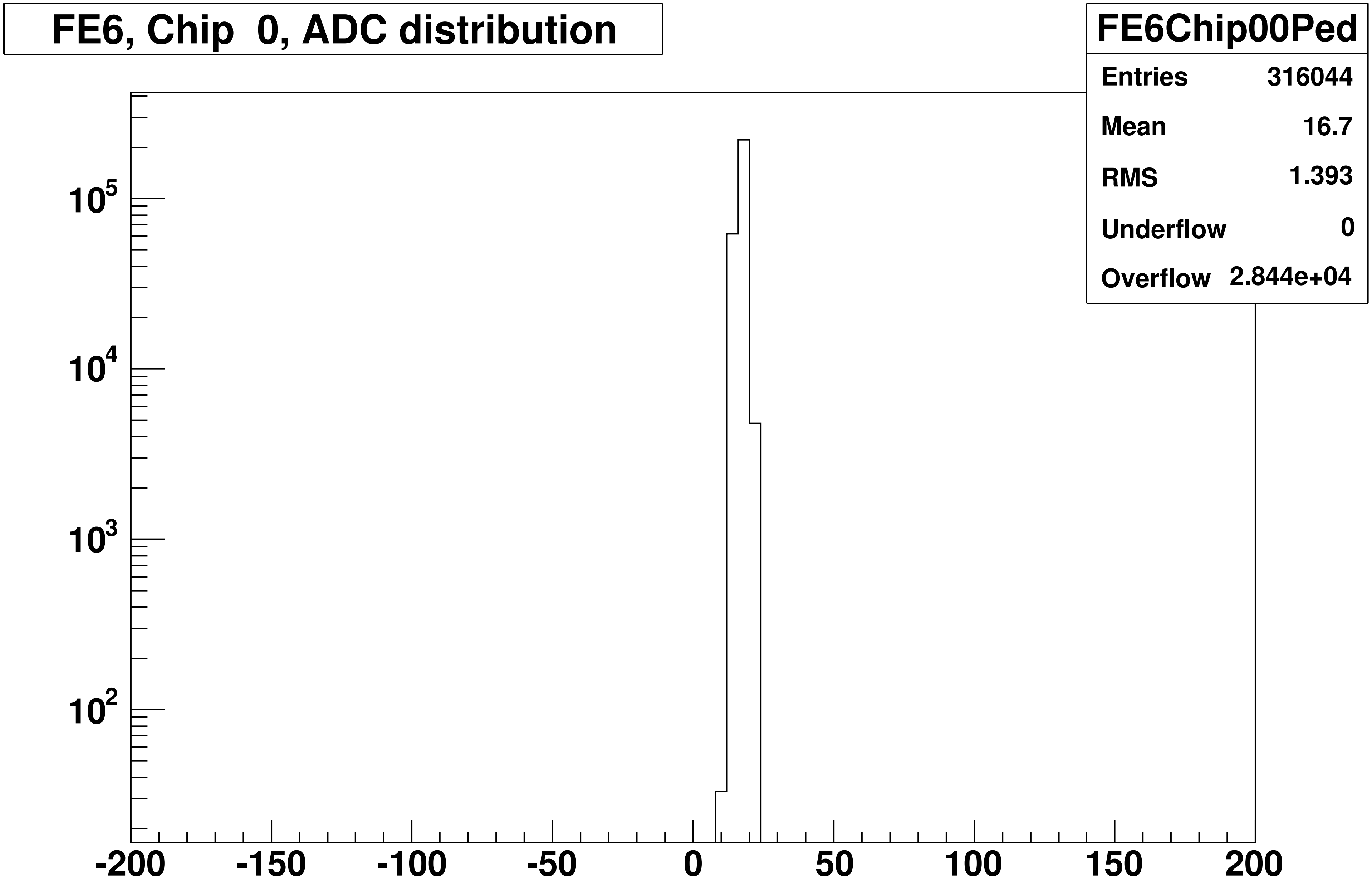
100
150
200


FE5, Chip 11, ADC distribution
FE5Chip11Sig
Entries 316044
Mean 1.889e+04
RMS 17.97
Underflow 2.872e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000


FE6, Chip 0, ADC distribution
FE6Chip00All
Entries 316044
Mean 1674
RMS 5375
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE6, Chip 0, ADC distribution
FE6Chip00Ped
Entries 316044
Mean 16.7
RMS 1.393
Underflow 0
Overflow 2.844e+04
10^5
10^4
10^3
10^2
-200
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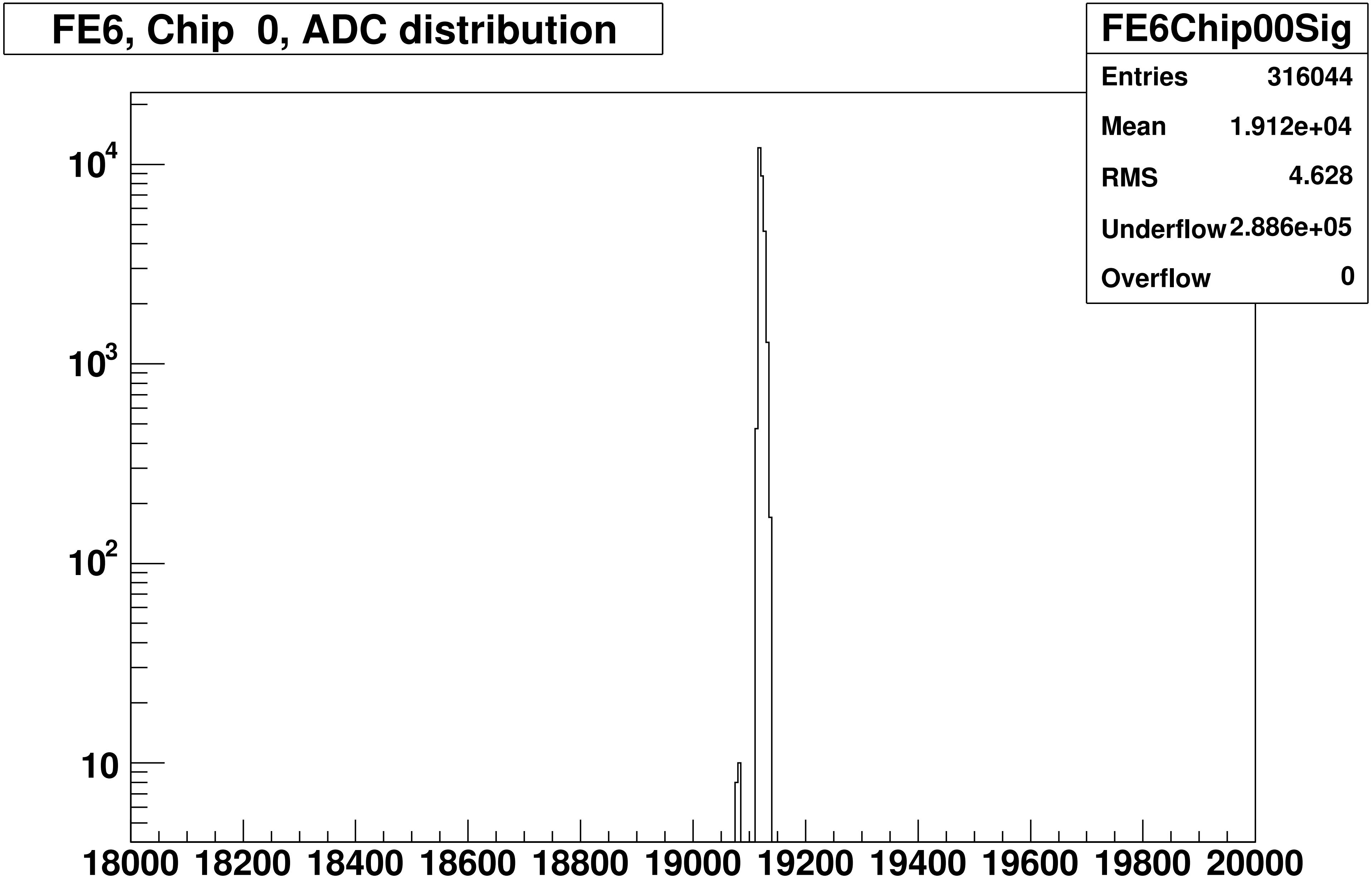
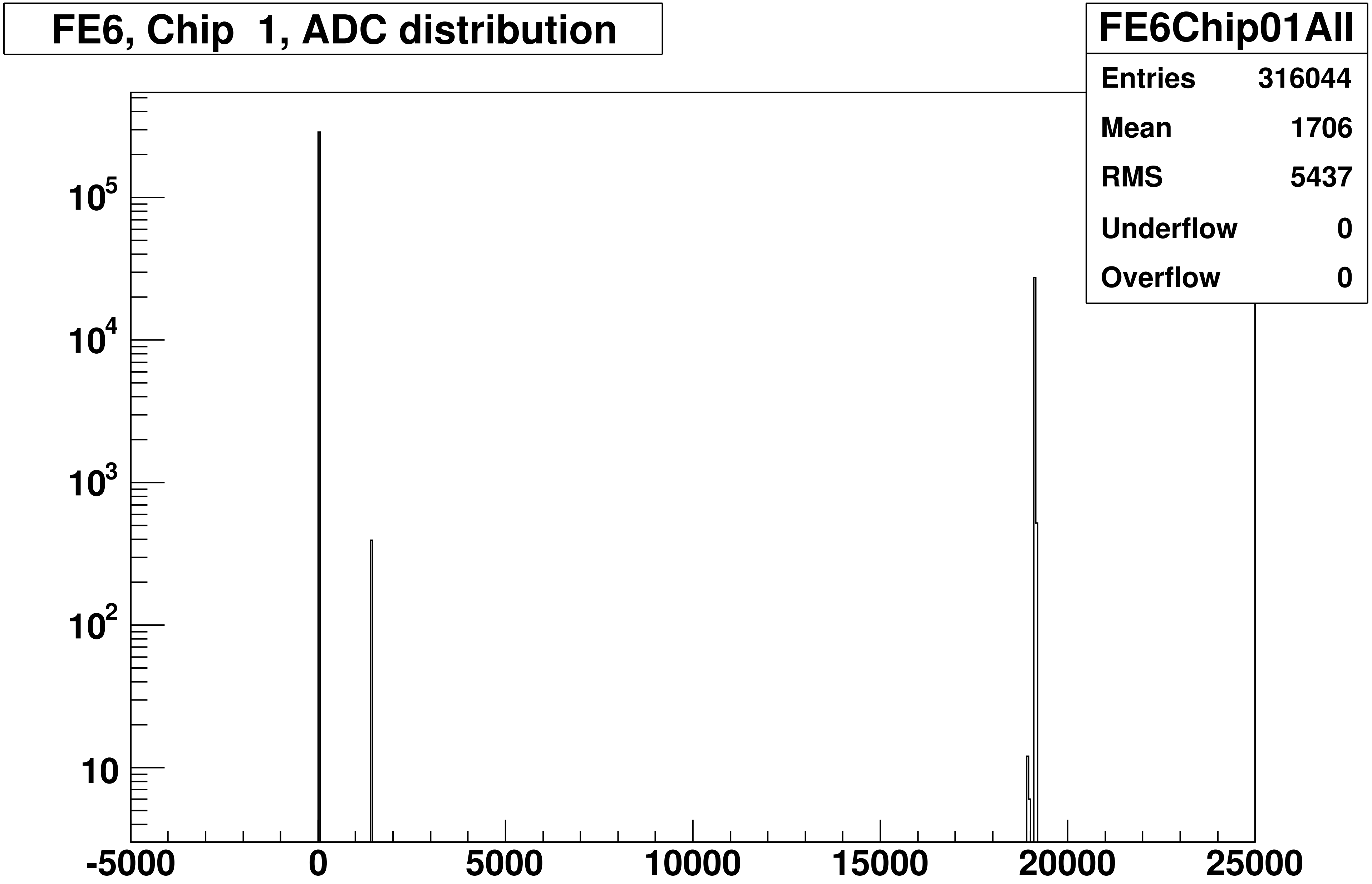
-100
-50
0
50
100
150
200


FE6, Chip 0, ADC distribution
FE6Chip00Sig
Entries 316044
Mean 1.912e+04
RMS 4.628
Underflow 2.886e+05
Overflow 0
10^4
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE6, Chip 1, ADC distribution
FE6Chip01All
Entries 316044
Mean 1706
RMS 5437
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
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-5000
0
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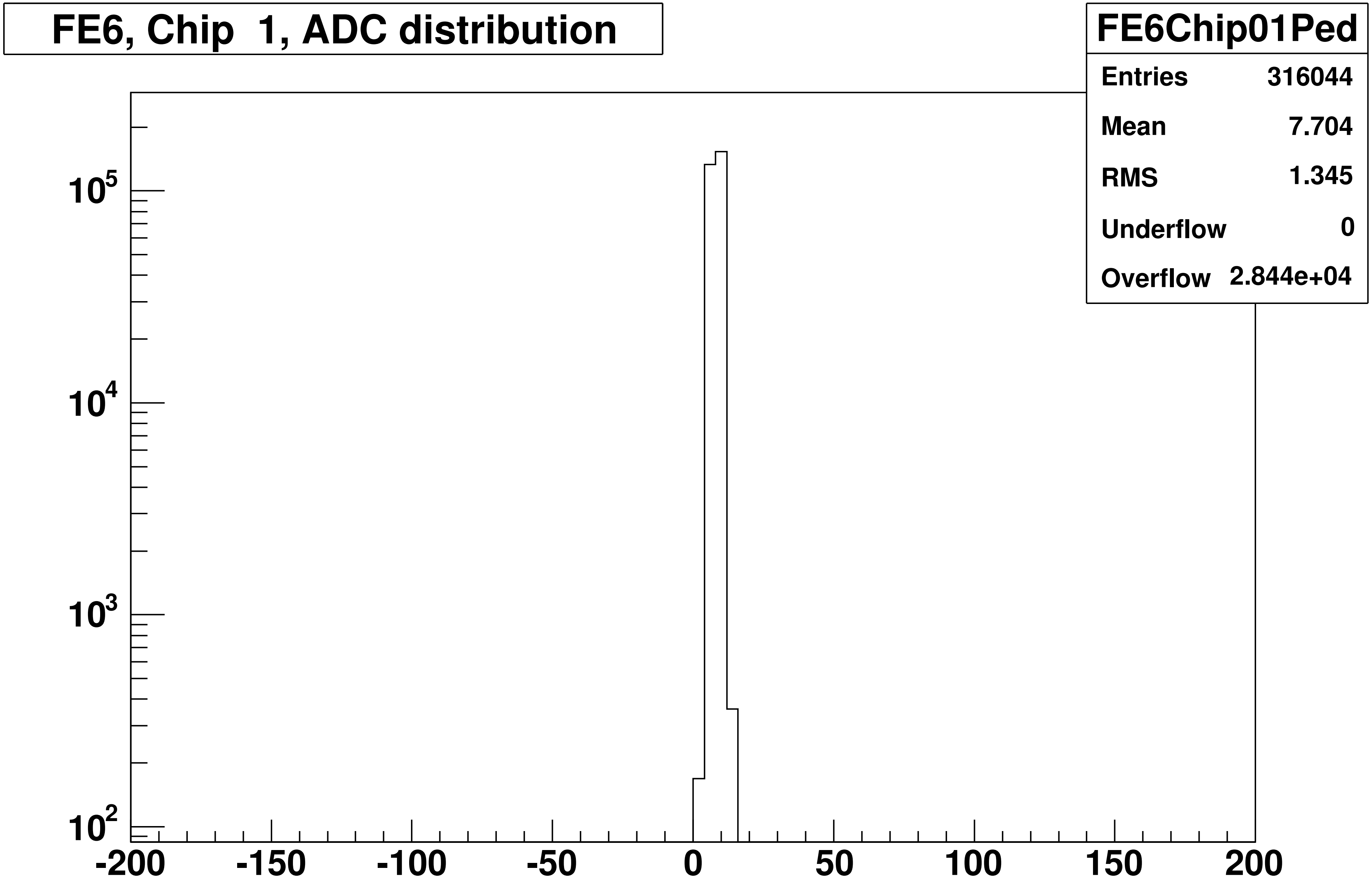
10000
15000
20000
25000


FE6, Chip 1, ADC distribution
FE6Chip01Ped
Entries 316044
Mean 7.704
RMS 1.345
Underflow 0
Overflow 2.844e+04
10^5
10^4
10^3
10^2
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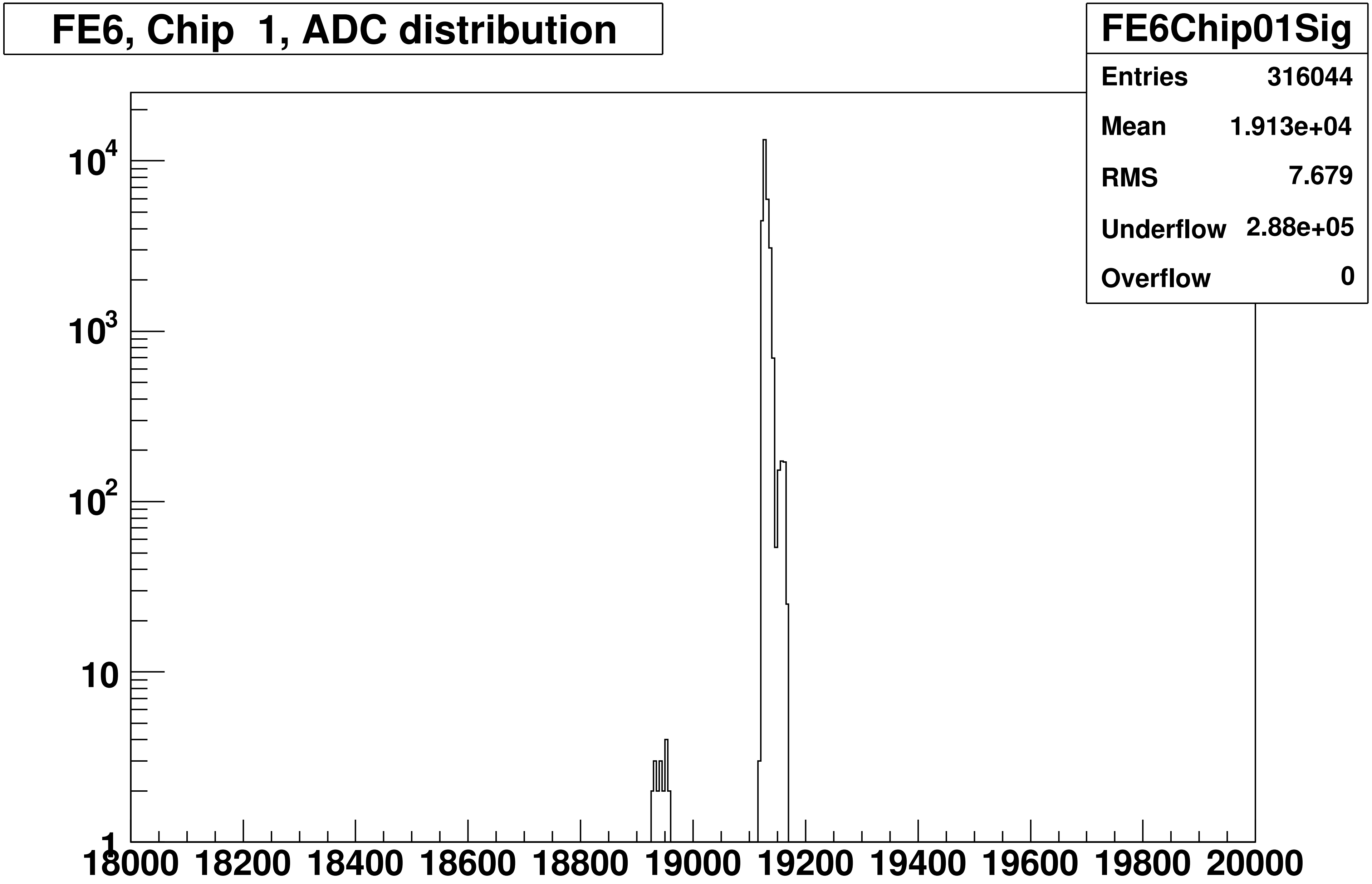
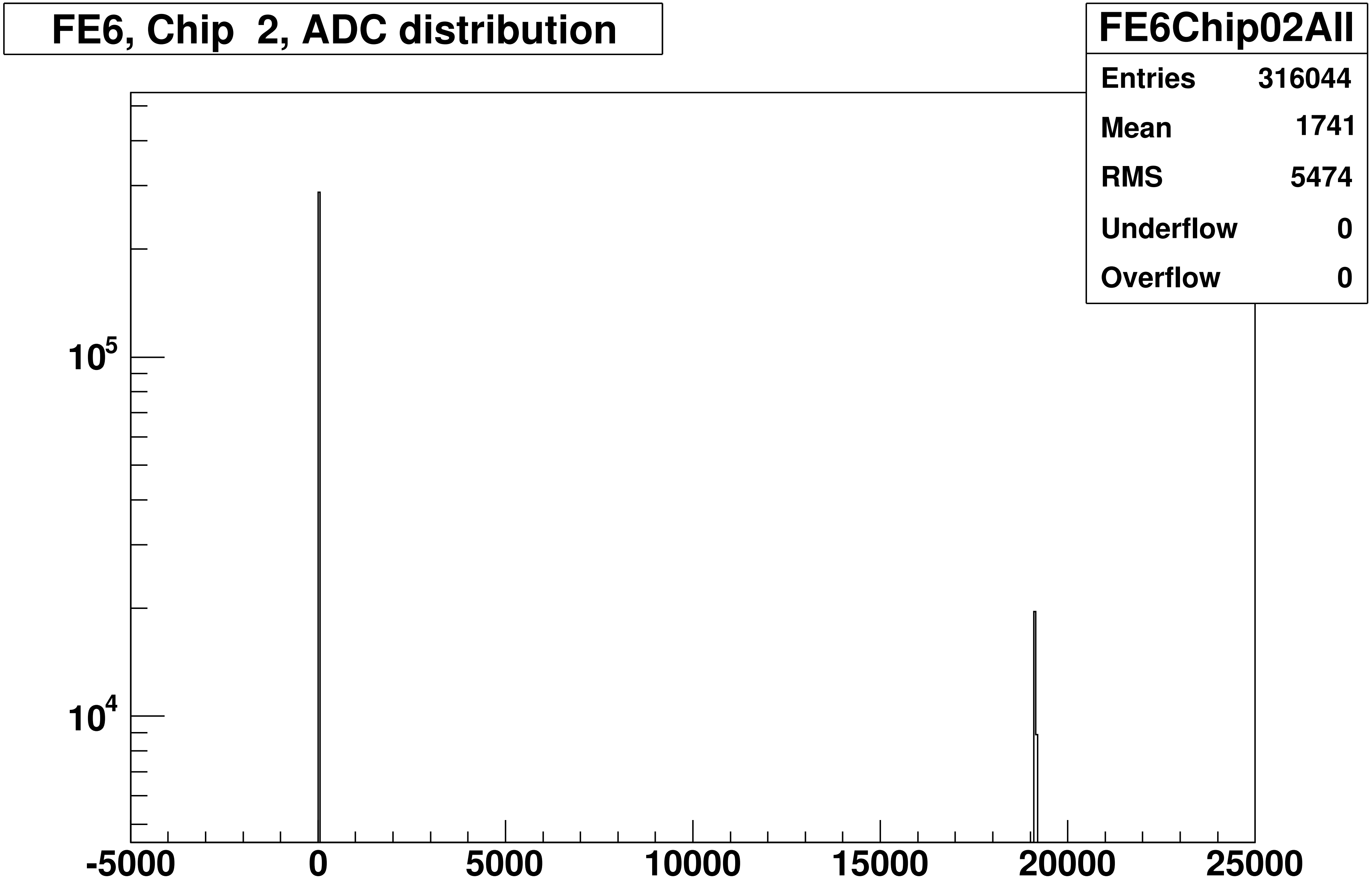
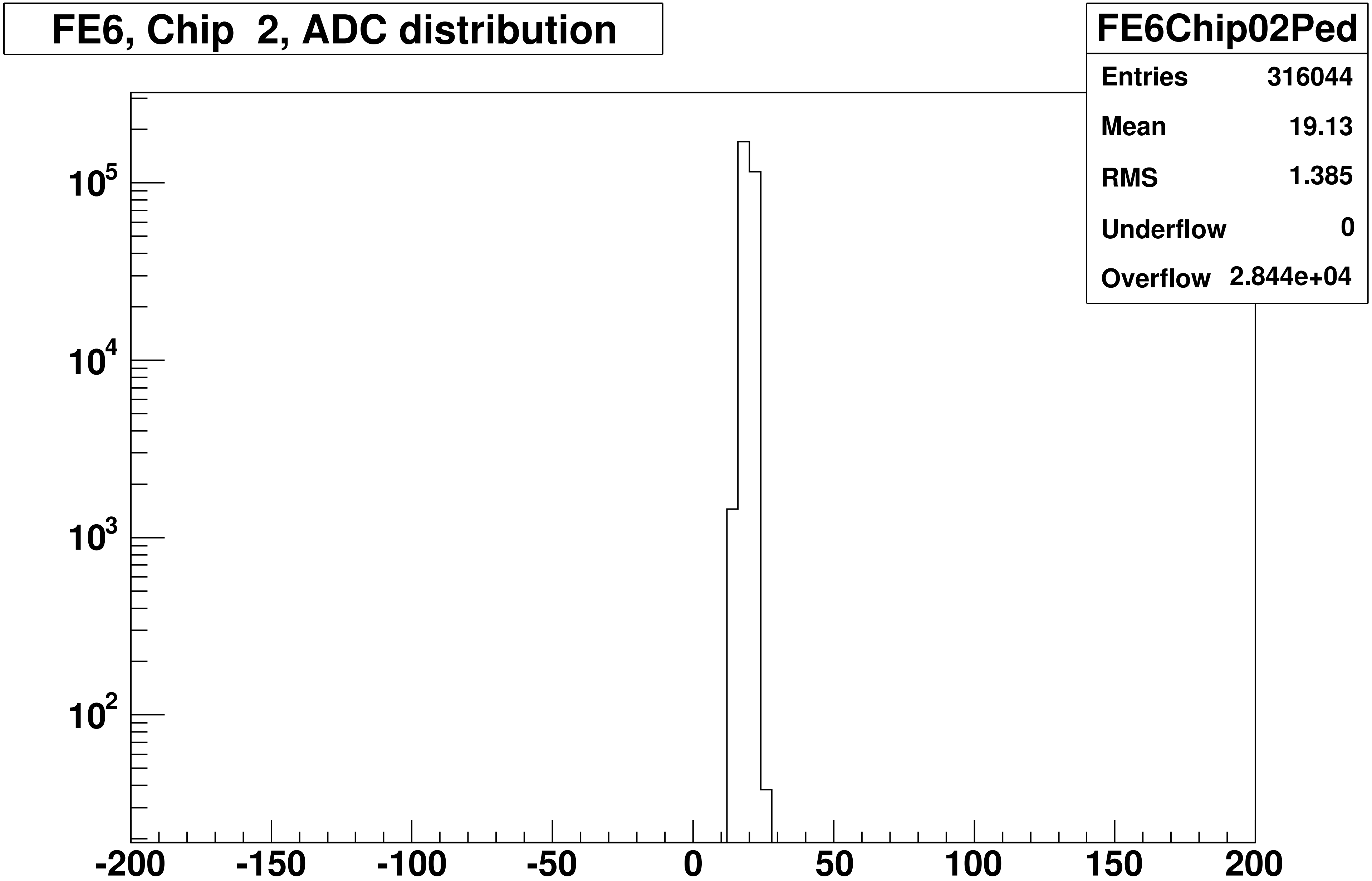
-100
-50
0
50
100
150
200


FE6, Chip 1, ADC distribution
FE6Chip01Sig
Entries 316044
Mean 1.913e+04
RMS 7.679
Underflow 2.88e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE6, Chip 2, ADC distribution
FE6Chip02All
Entries 316044
Mean 1741
RMS 5474
Underflow 0
Overflow 0
10^5
10^4
-5000
0
5000
10000
15000
20000
25000


FE6, Chip 2, ADC distribution
FE6Chip02Ped
Entries 316044
Mean 19.13
RMS 1.385
Underflow 0
Overflow 2.844e+04
10^5
10^4
10^3
10^2
-200
-150
-100
-50
0
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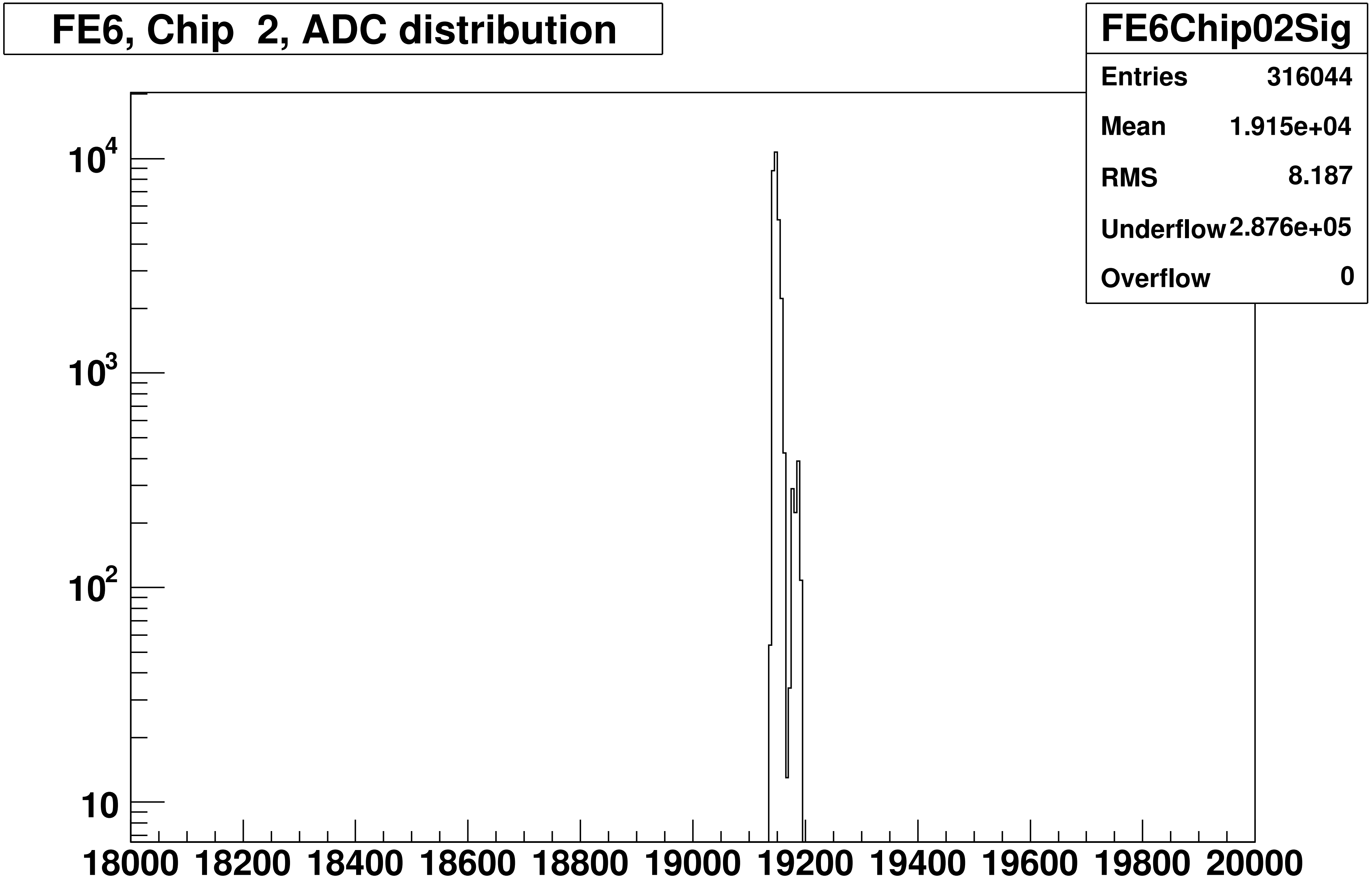
100
150
200


FE6, Chip 2, ADC distribution
FE6Chip02Sig
Entries 316044
Mean 1.915e+04
RMS 8.187
Underflow 2.876e+05
Overflow 0
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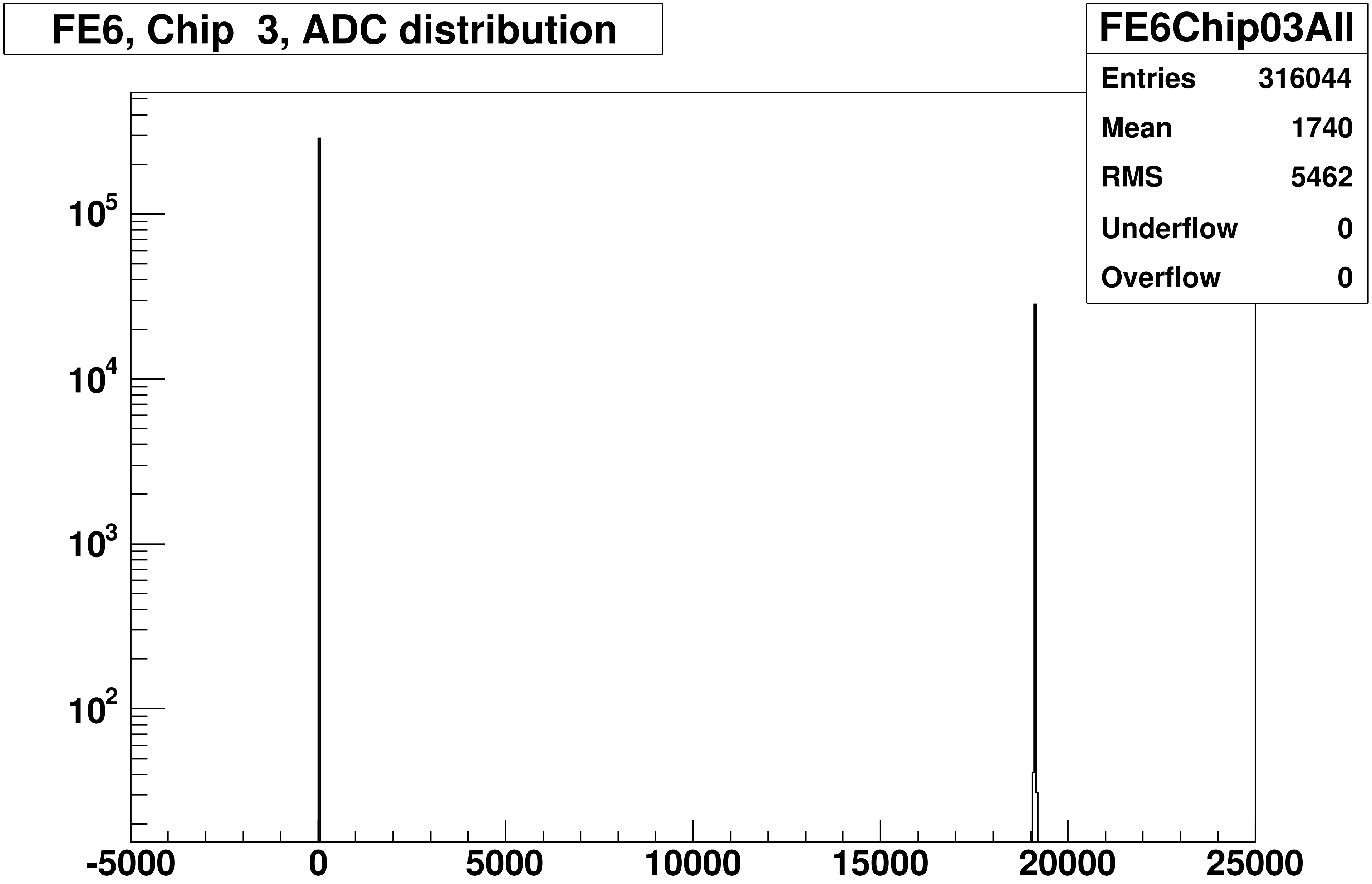
10^3
10^2
10
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000


FE6, Chip 3, ADC distribution
FE6Chip03All
Entries 316044
Mean 1740
RMS 5462
Underflow 0
Overflow 0
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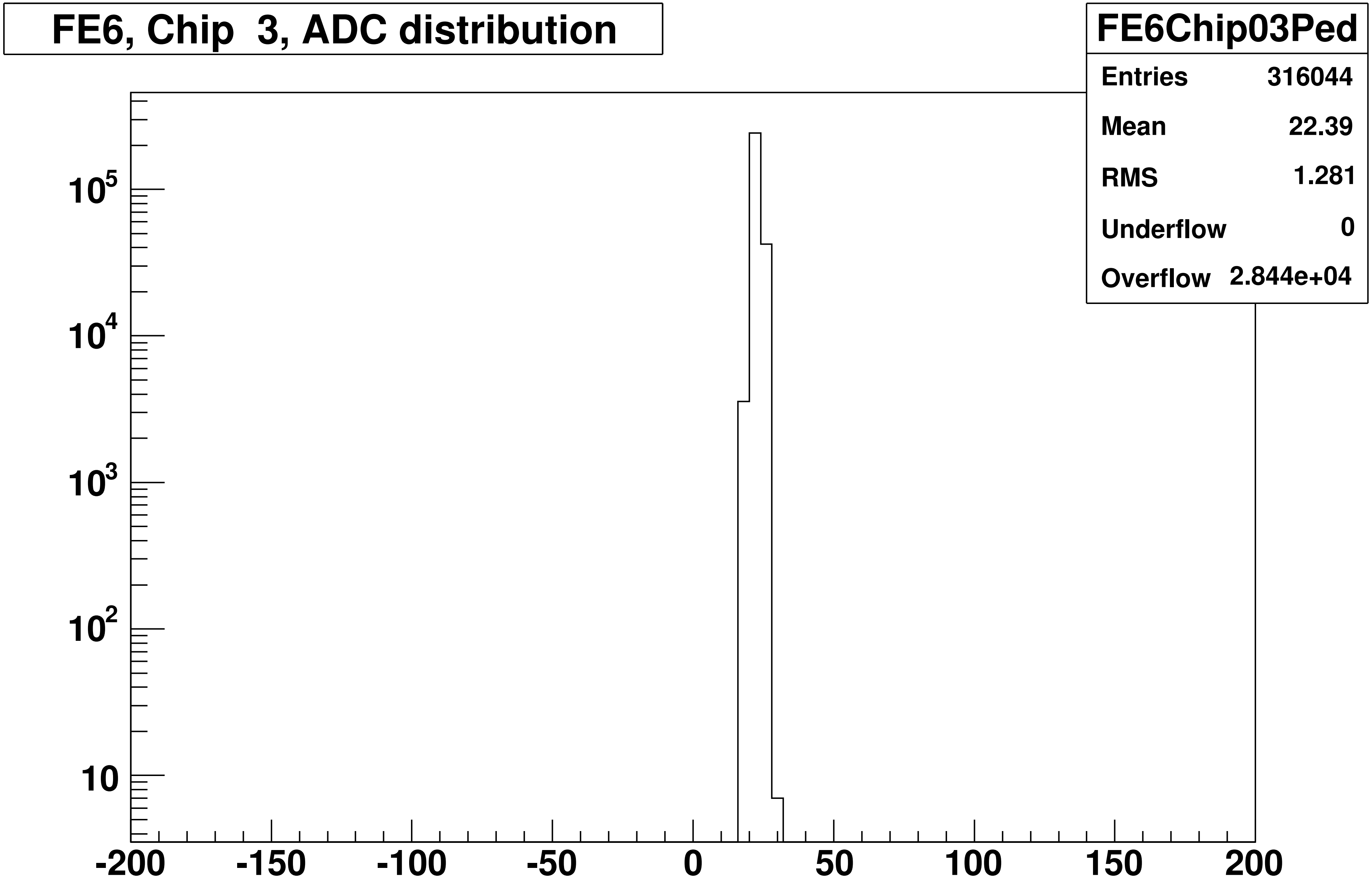
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000


FE6, Chip 3, ADC distribution
FE6Chip03Ped
Entries 316044
Mean 22.39
RMS 1.281
Underflow 0
Overflow 2.844e+04
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10^4
10^3
10^2
10
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-150
-100
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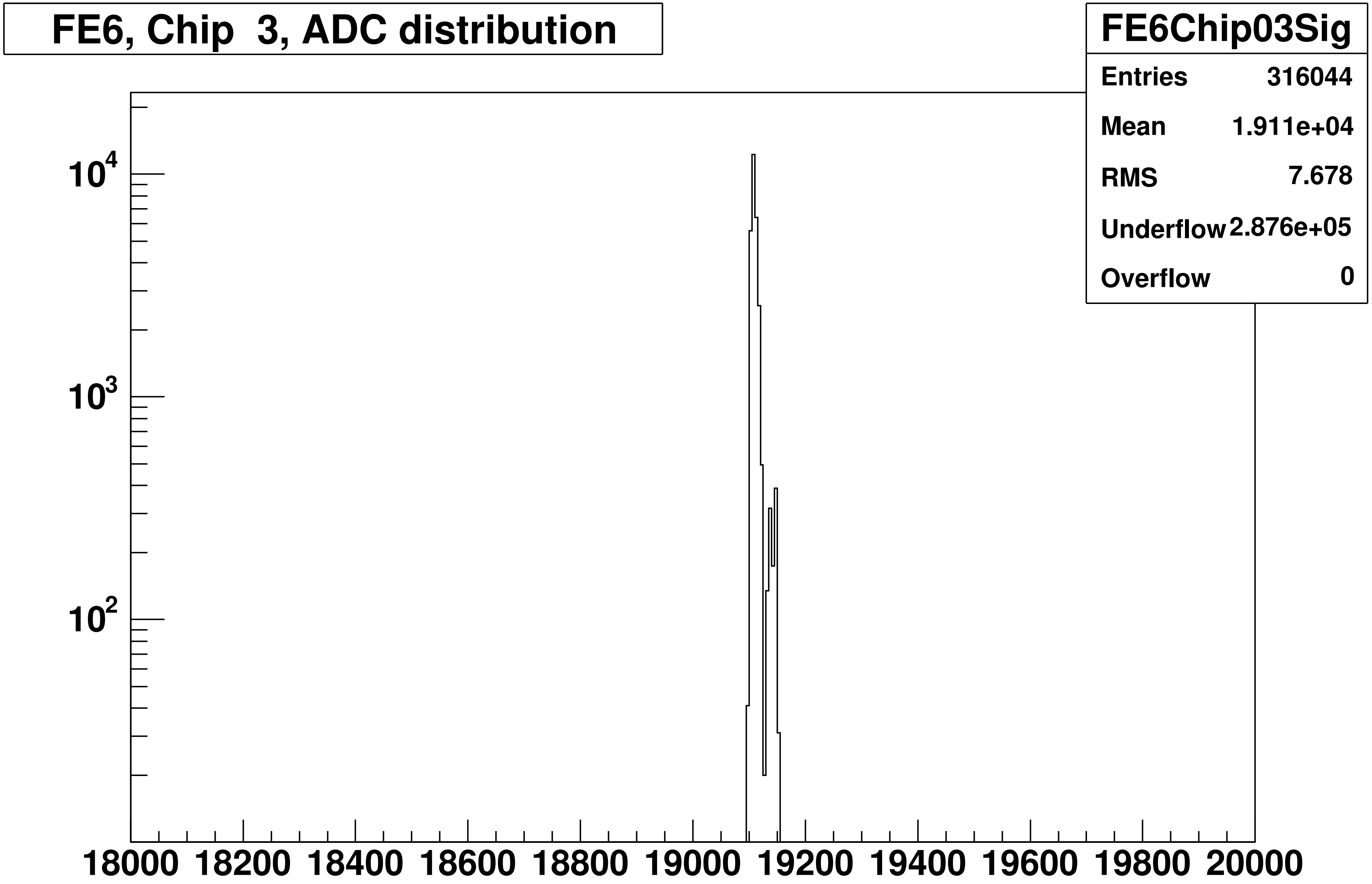
150
200



FE6, Chip 3, ADC distribution
FE6Chip03Sig
Entries 316044
Mean 1.911e+04
RMS 7.678
Underflow 2.876e+05
Overflow 0
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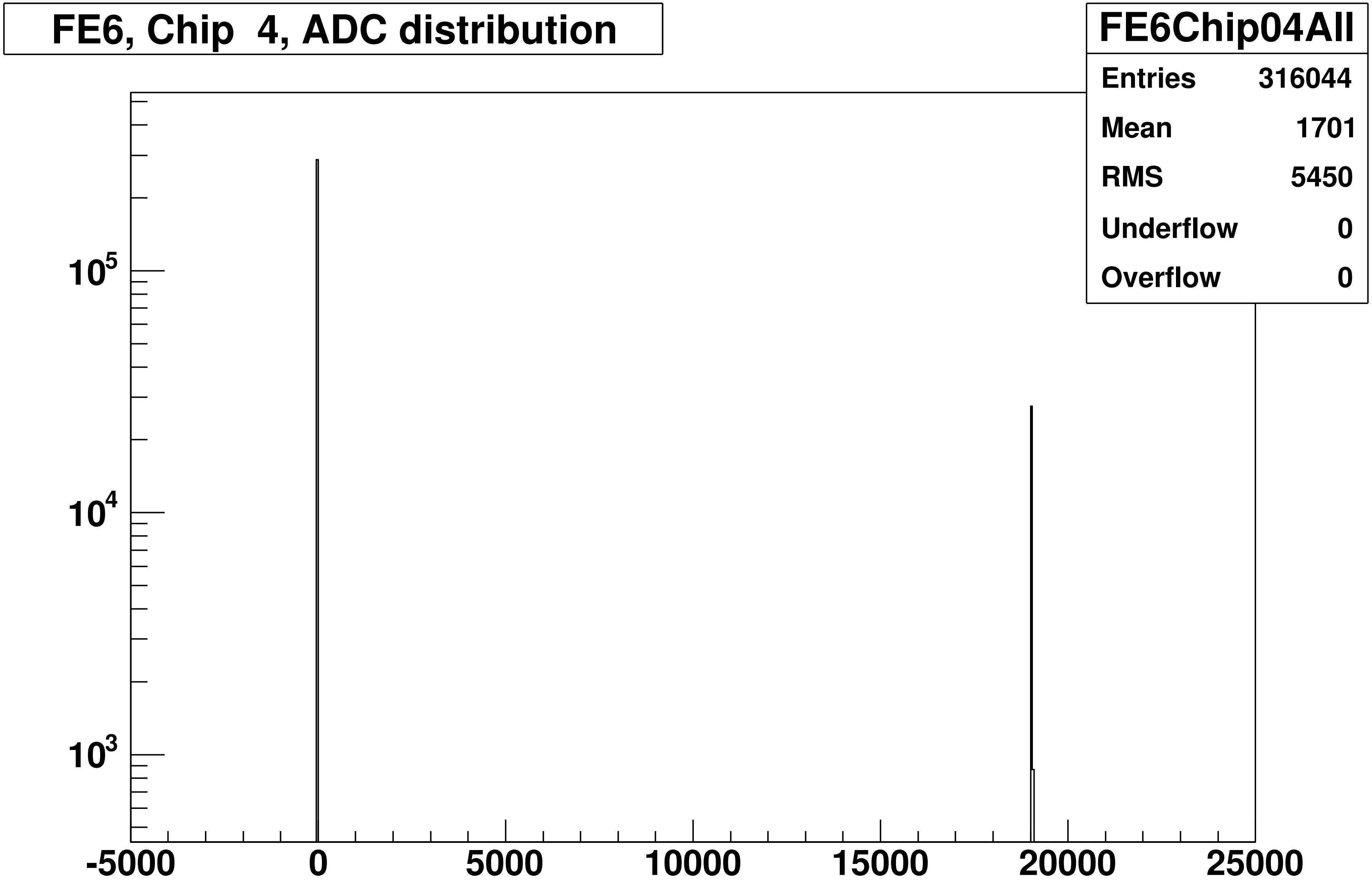
10^3
10^2
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000



FE6, Chip 4, ADC distribution
FE6Chip04All
Entries 316044
Mean 1701
RMS 5450
Underflow 0
Overflow 0
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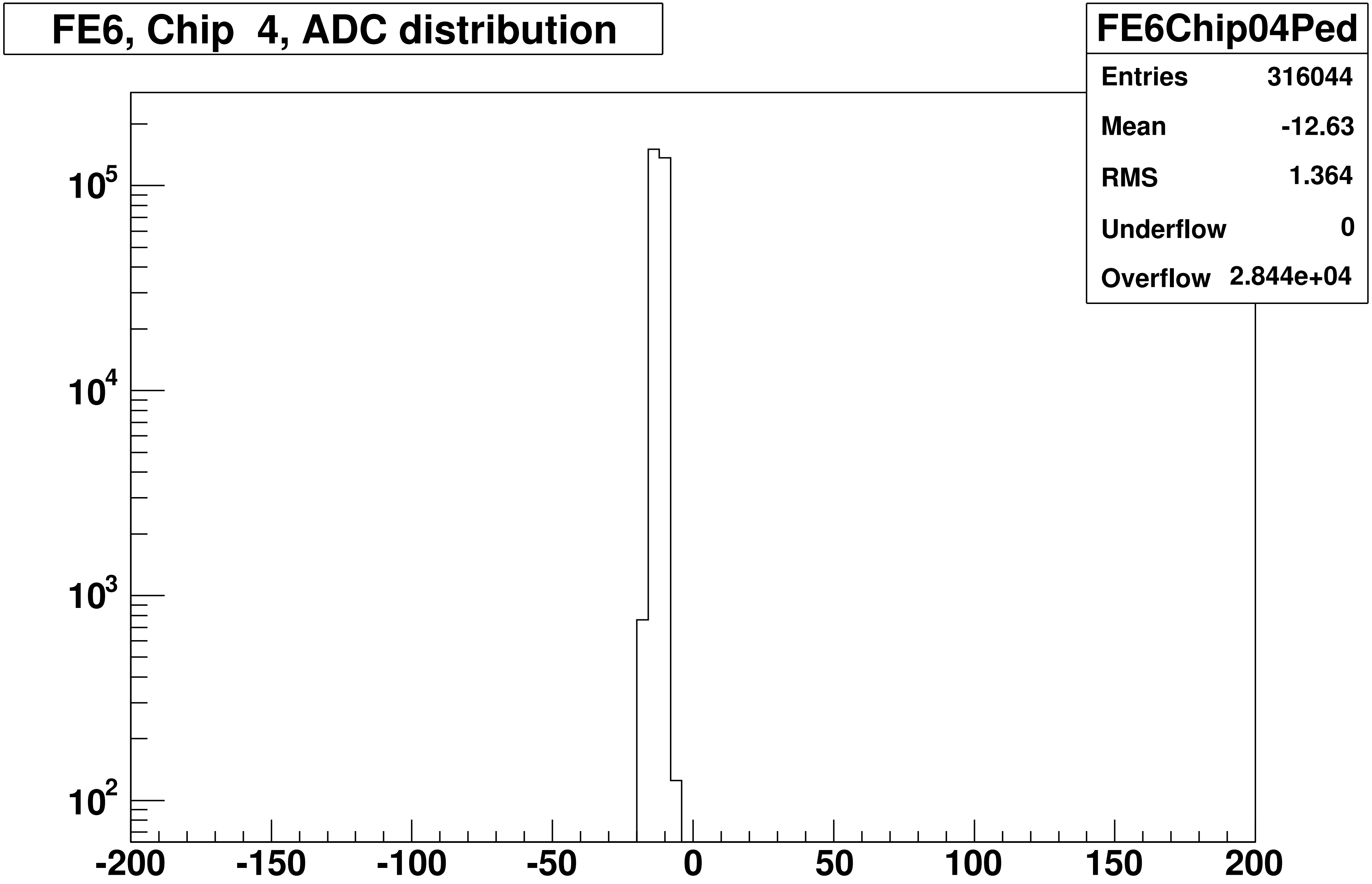
10^4
10^3
-5000
0
5000
10000
15000
20000
25000


FE6, Chip 4, ADC distribution
FE6Chip04Ped
Entries 316044
Mean -12.63
RMS 1.364
Underflow 0
Overflow 2.844e+04
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10^4
10^3
10^2
-200
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-100
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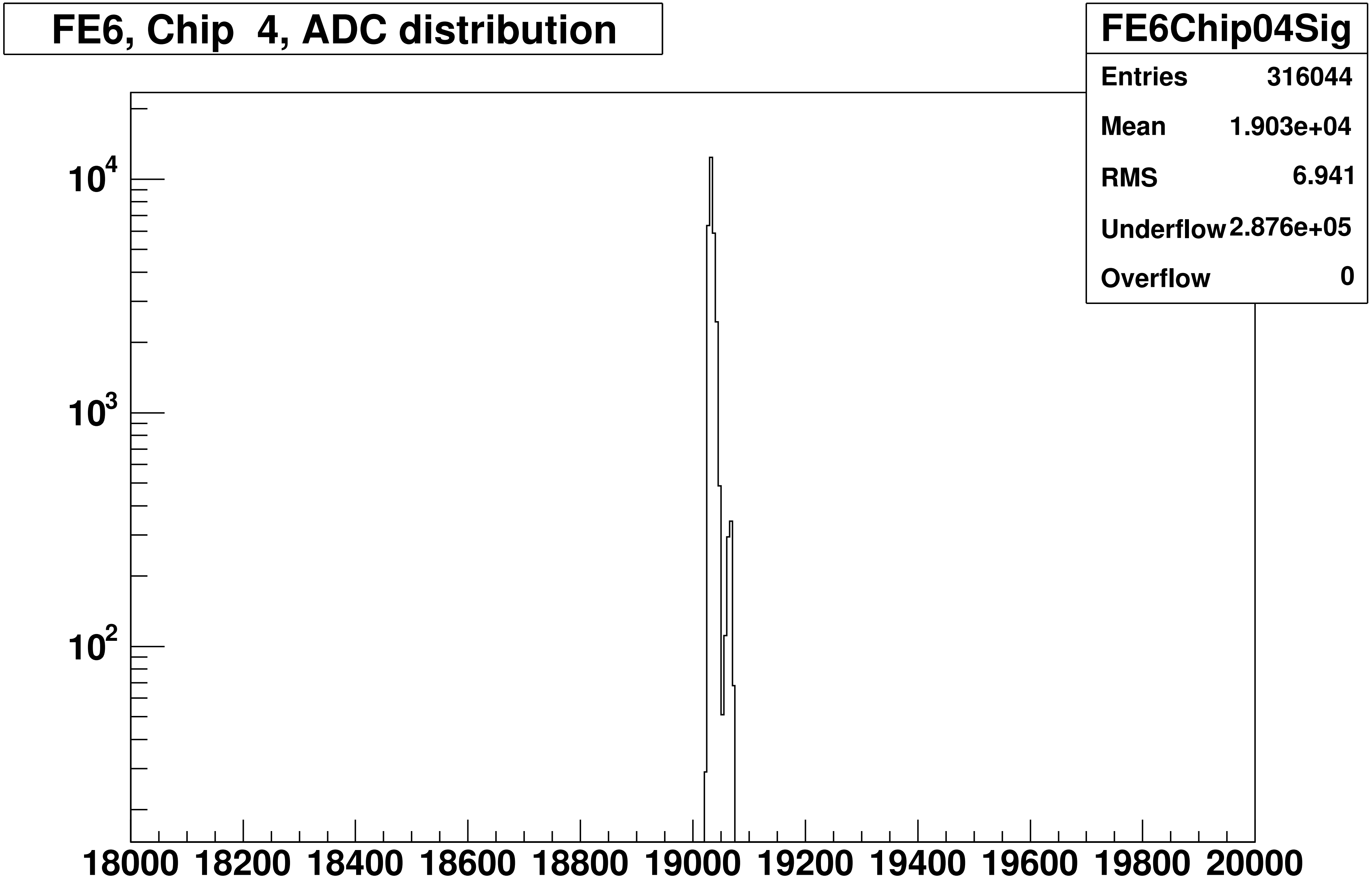
100
150
200



FE6, Chip 4, ADC distribution
FE6Chip04Sig
Entries 316044
Mean 1.903e+04
RMS 6.941
Underflow 2.876e+05
Overflow 0
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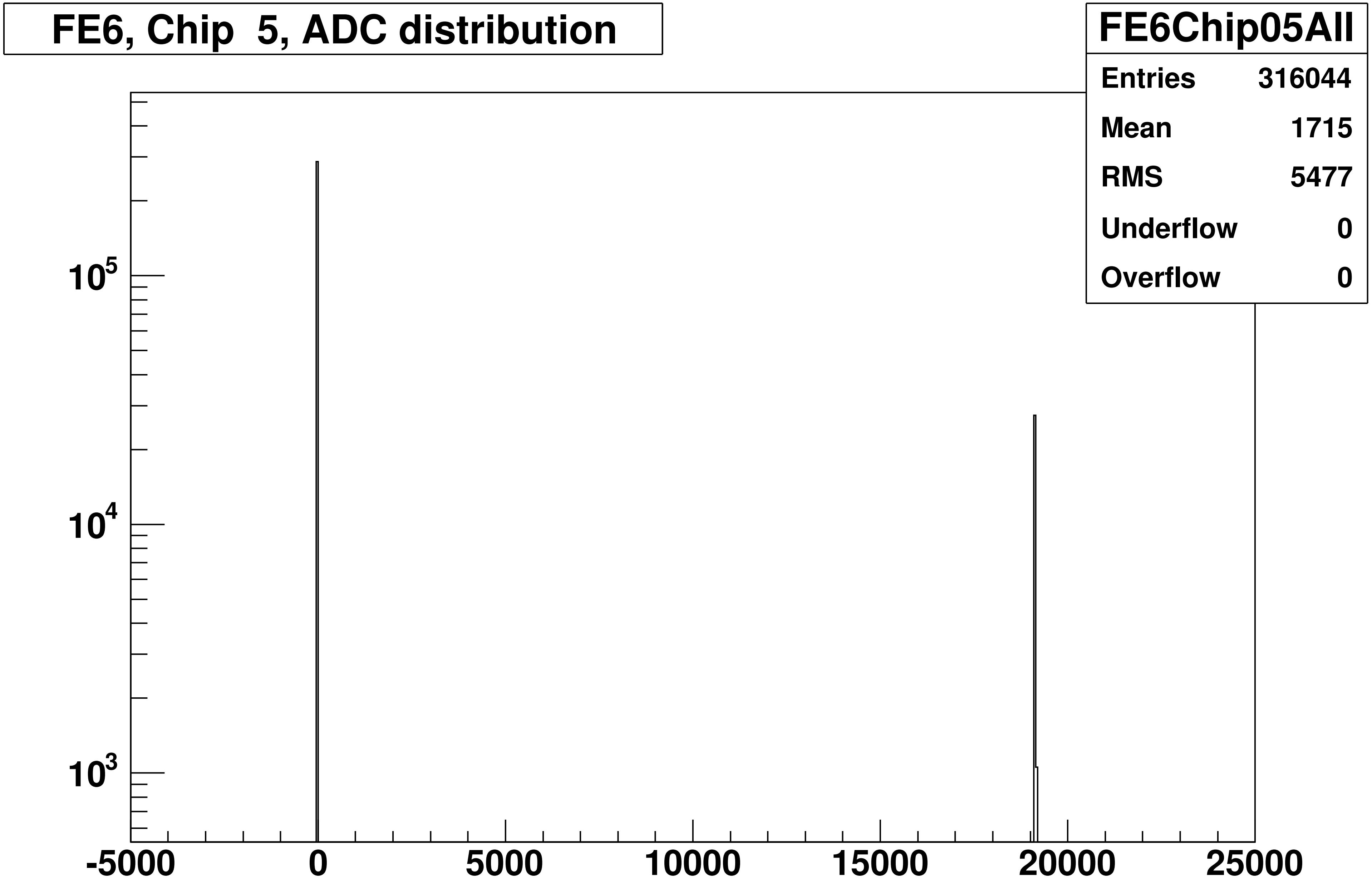
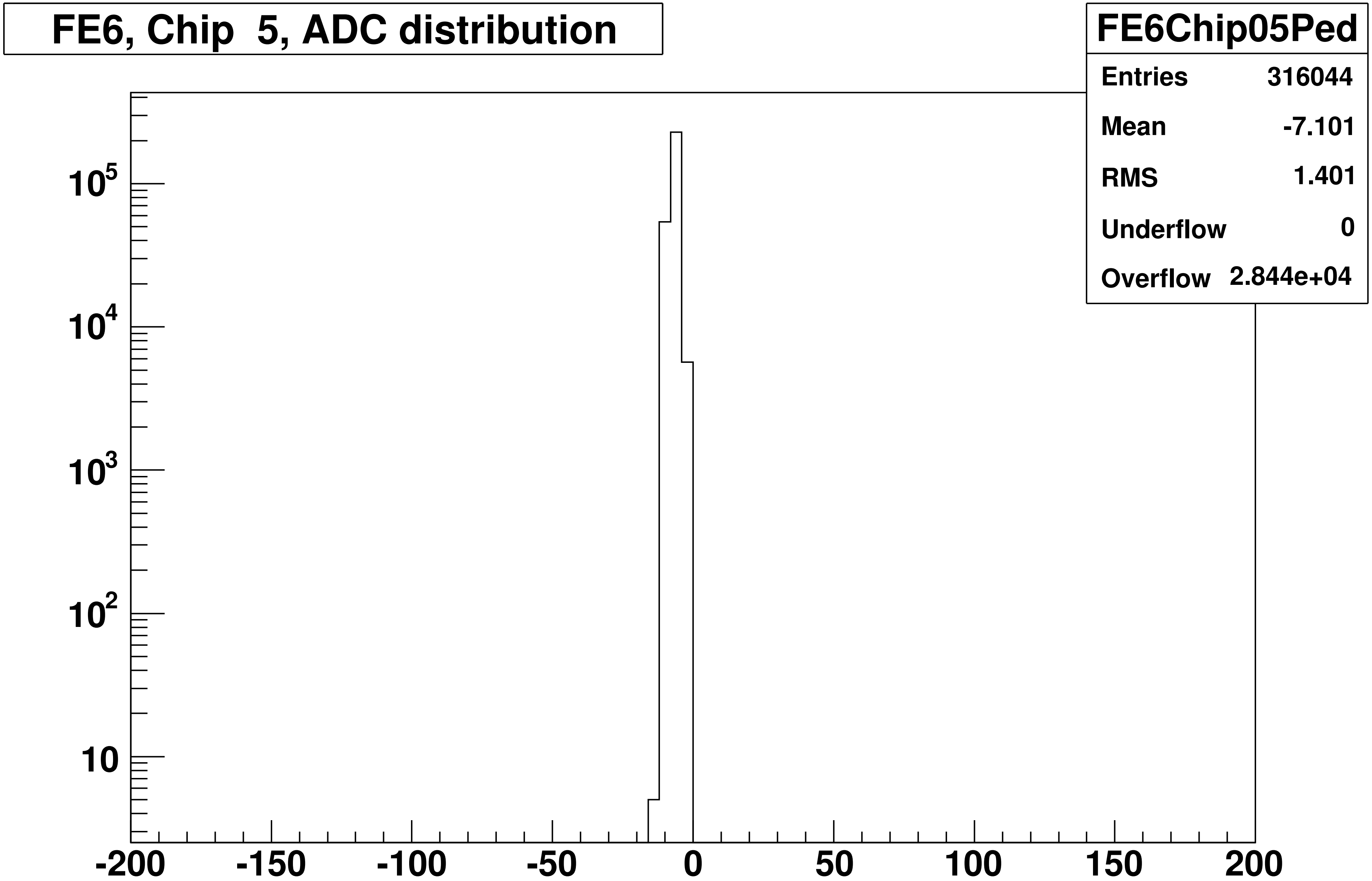
10^3
10^2
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE6, Chip 5, ADC distribution
FE6Chip05All
Entries 316044
Mean 1715
RMS 5477
Underflow 0
Overflow 0
10^5
10^4
10^3
-5000
0
5000
10000
15000
20000
25000



FE6, Chip 5, ADC distribution
FE6Chip05Ped
Entries 316044
Mean -7.101
RMS 1.401
Underflow 0
Overflow 2.844e+04
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10^4
10^3
10^2
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-200
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-100
-50
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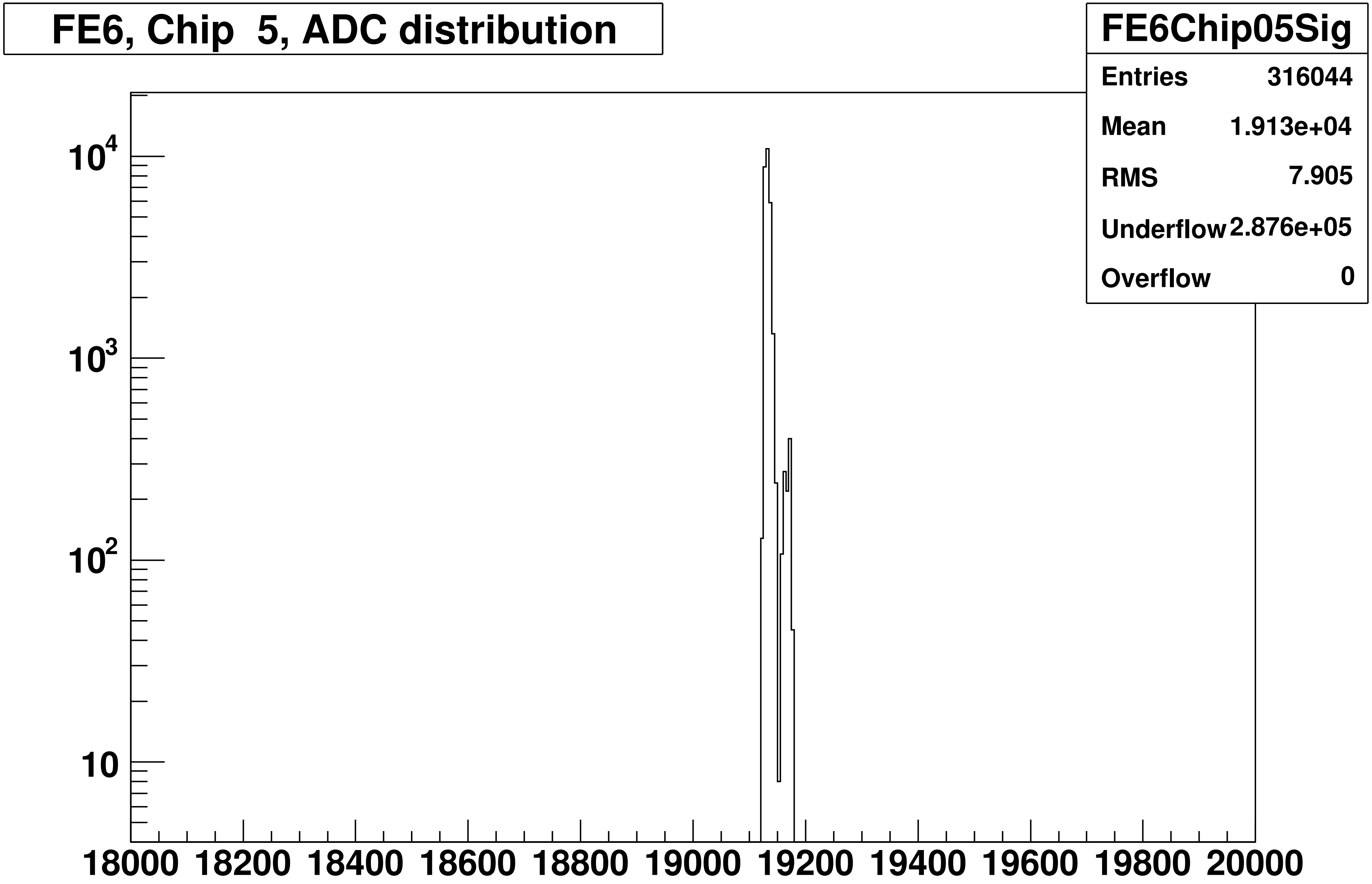
100
150
200



FE6, Chip 5, ADC distribution
FE6Chip05Sig
Entries 316044
Mean 1.913e+04
RMS 7.905
Underflow 2.876e+05
Overflow 0
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10^3
10^2
10
18000
18200
18400
18600
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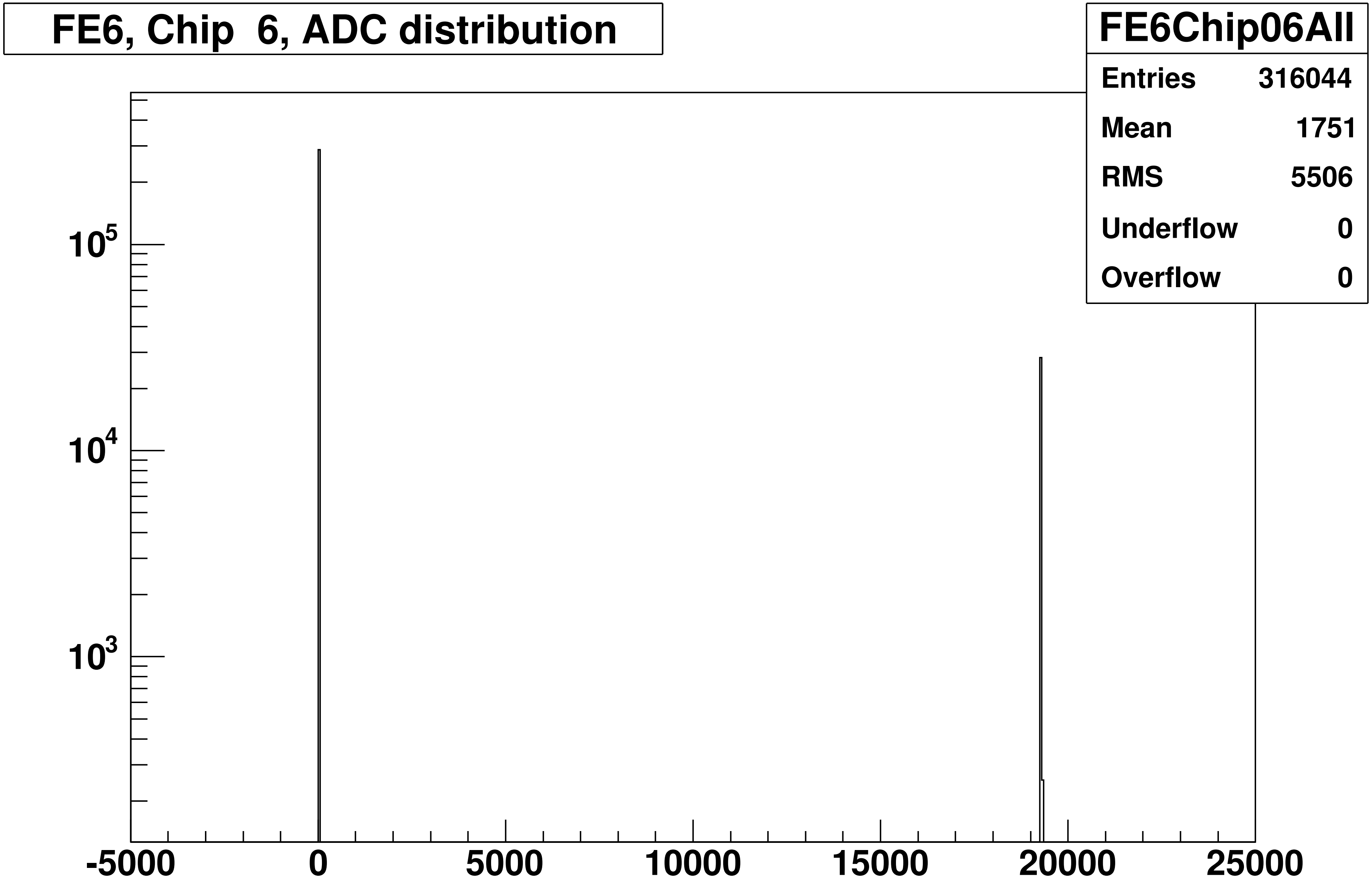
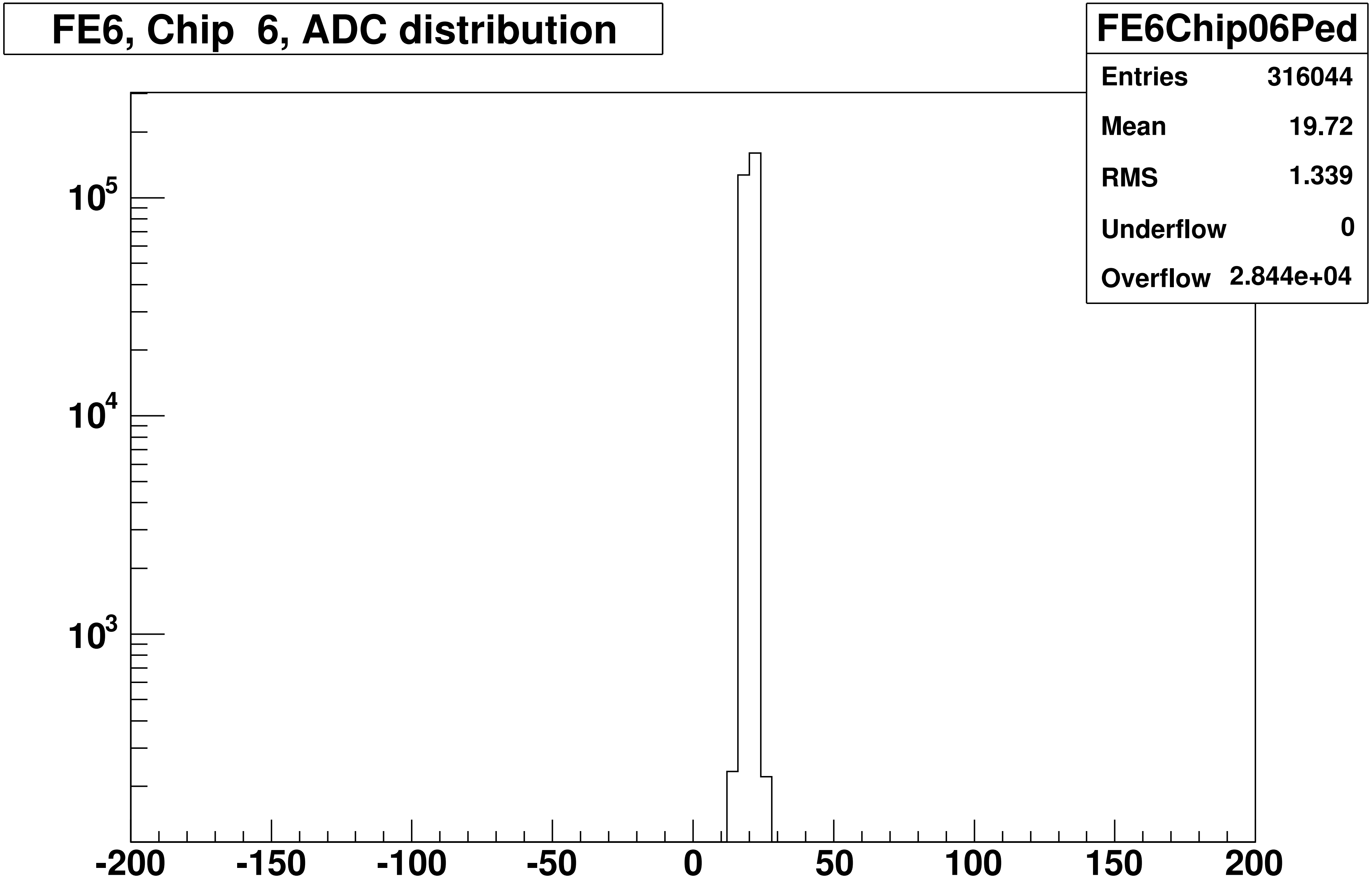
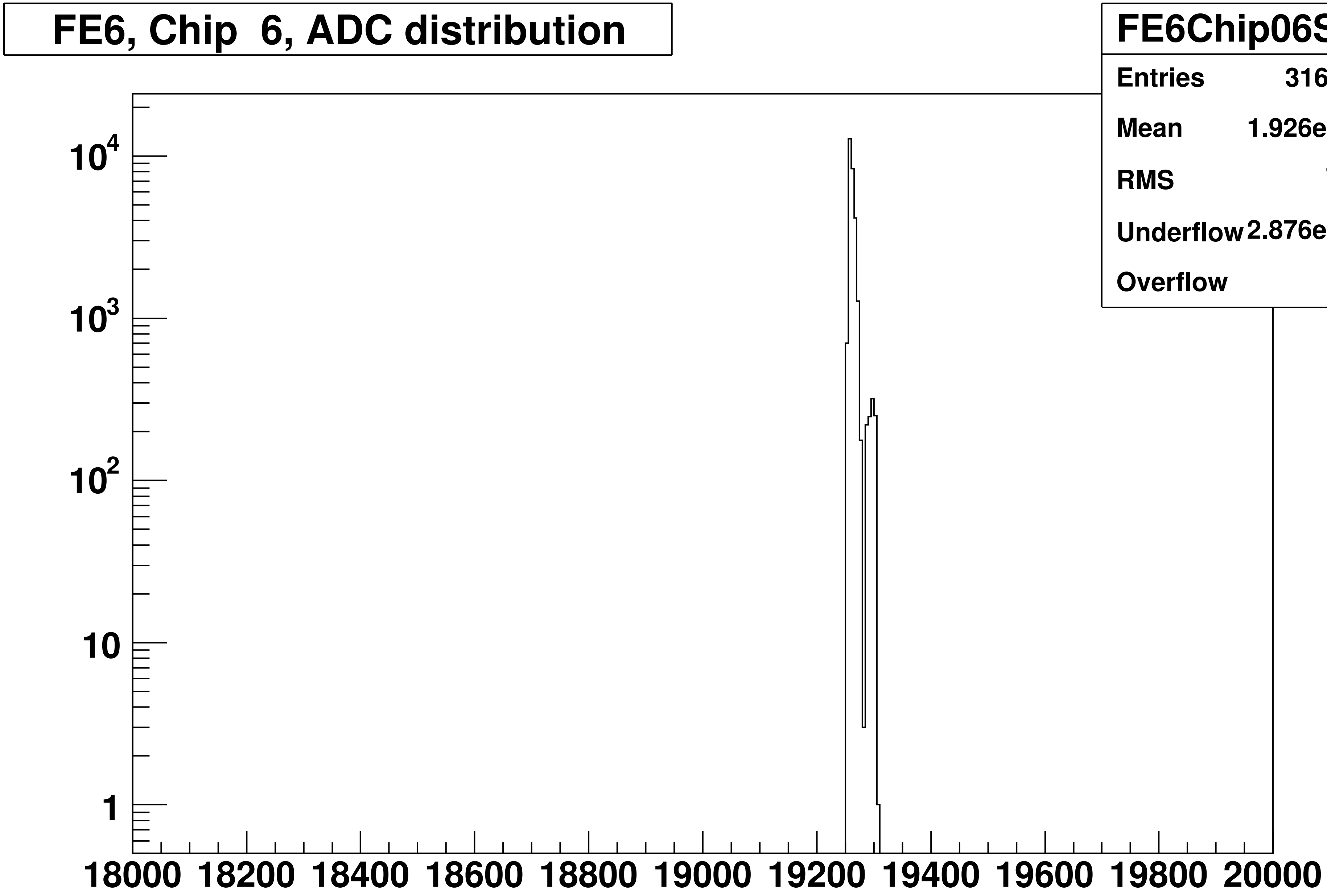
19000
19200
19400
19600
19800
20000


FE6, Chip 6, ADC distribution
FE6Chip06All
Entries 316044
Mean 1751
RMS 5506
Underflow 0
Overflow 0
10^5
10^4
10^3
-5000
0
5000
10000
15000
20000
25000


FE6, Chip 6, ADC distribution
FE6Chip06Ped
Entries 316044
Mean 19.72
RMS 1.339
Underflow 0
Overflow 2.844e+04
10^5
10^4
10^3
-200 -150 -100 -50 0 50 100 150 200


FE6, Chip 6, ADC distribution
FE6Chip06Sig
Entries 316044
Mean 1.926e+04
RMS 7.91
Underflow 2.876e+05
Overflow 0
10^4
10^3
10^2
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1
18000
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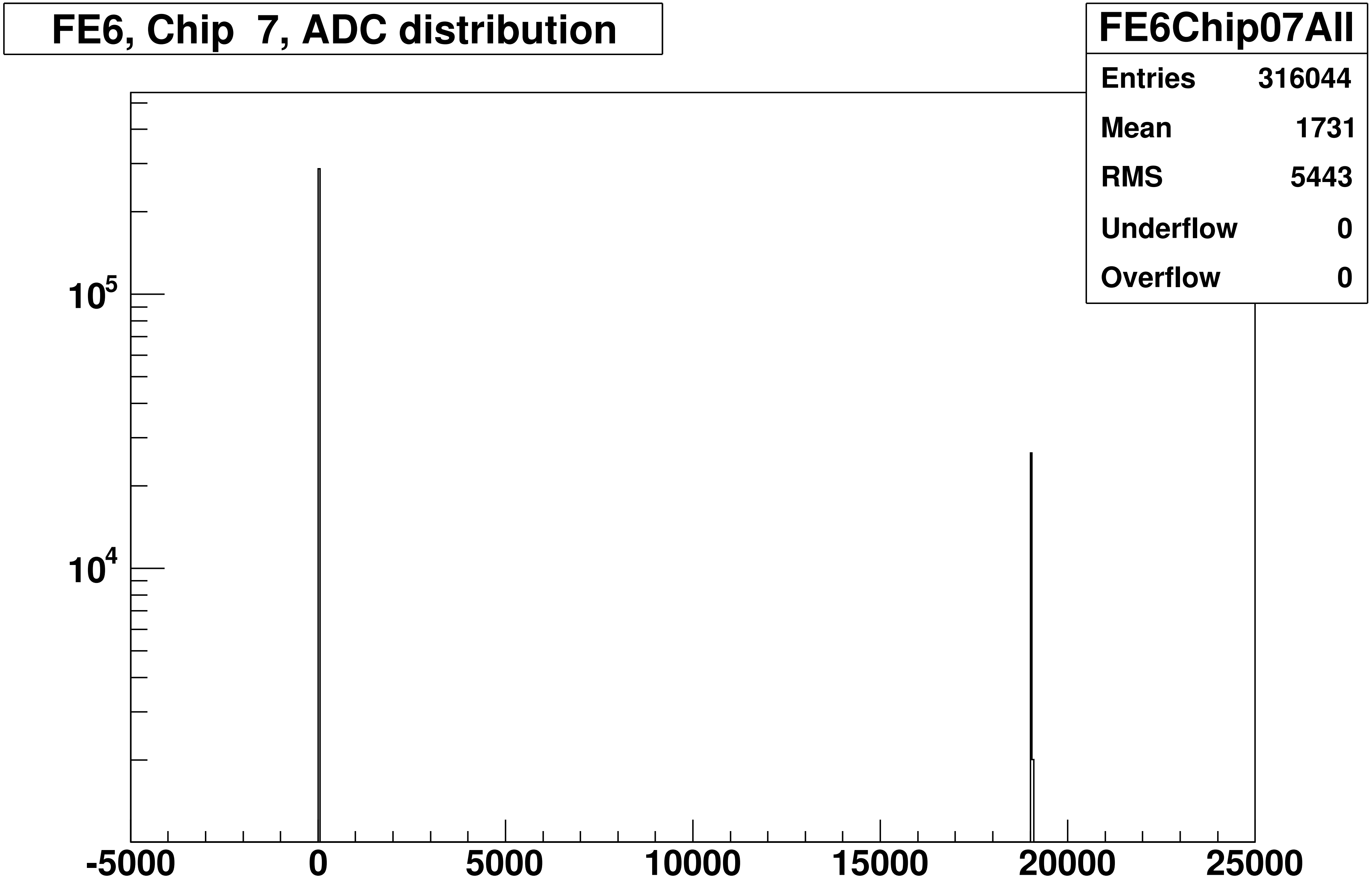
19000
19200
19400
19600
19800
20000



FE6, Chip 7, ADC distribution
FE6Chip07All
Entries 316044
Mean 1731
RMS 5443
Underflow 0
Overflow 0
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10^4
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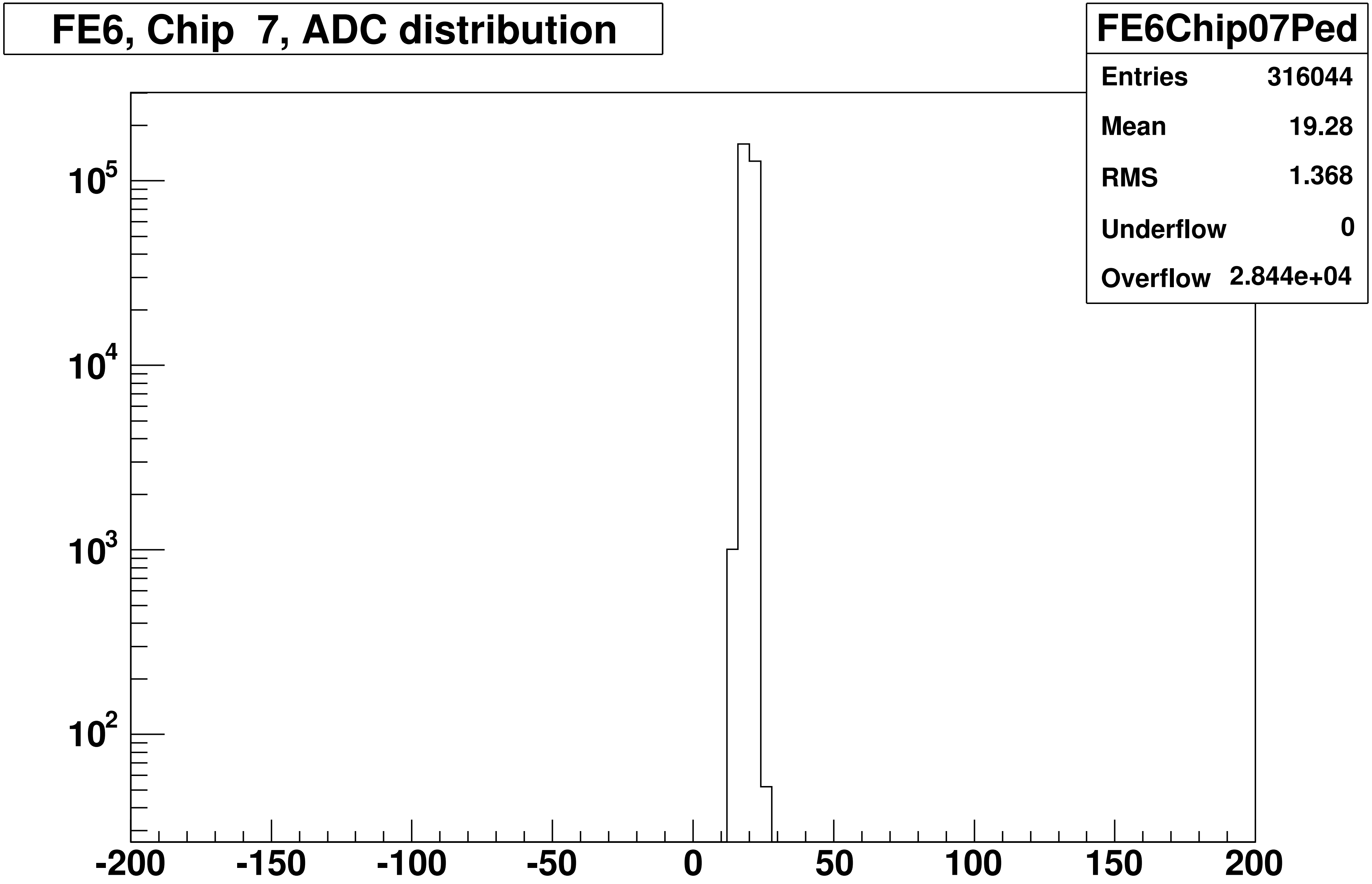
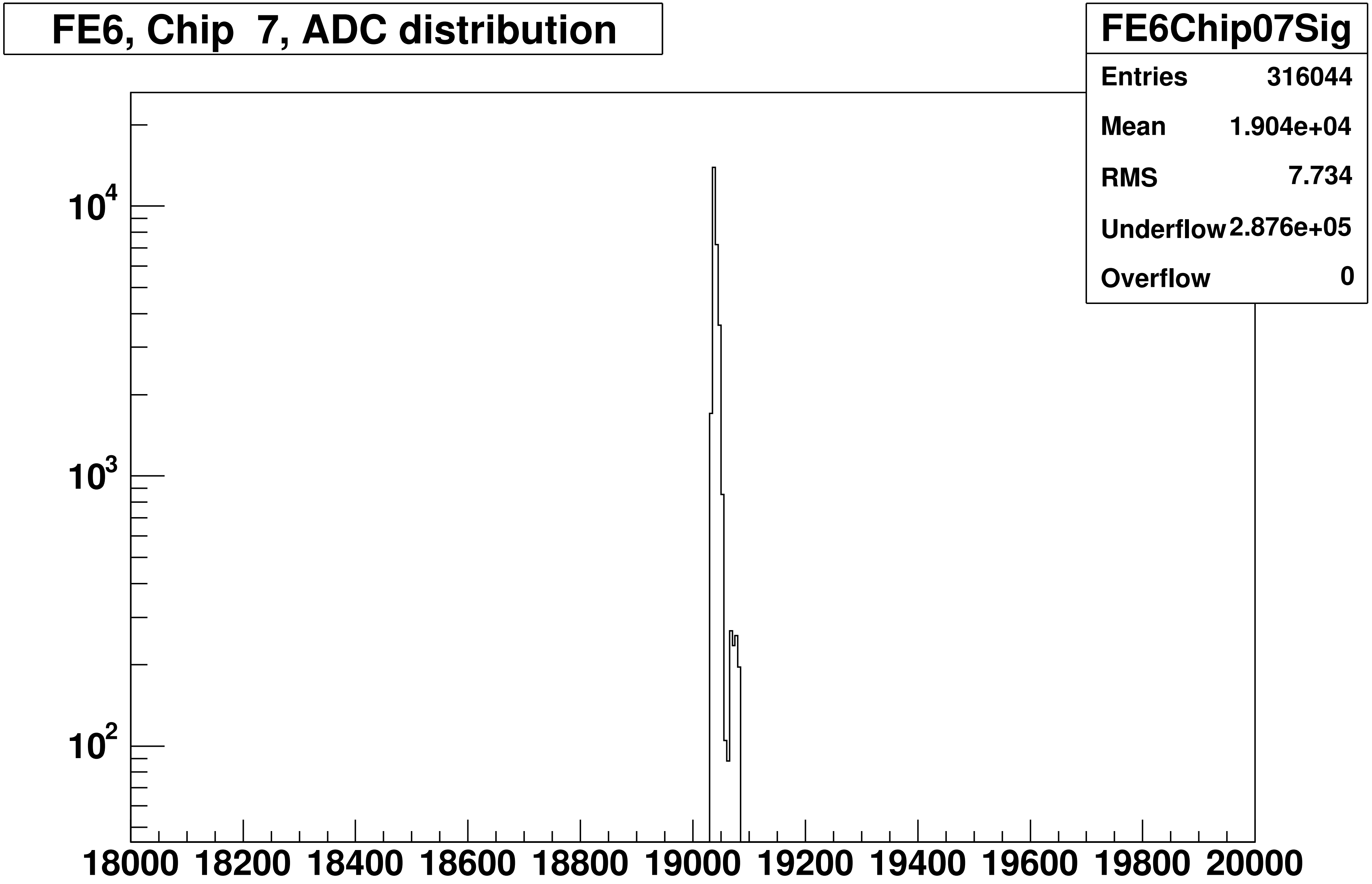
0
5000
10000
15000
20000
25000



FE6, Chip 7, ADC distribution
FE6Chip07Ped
Entries 316044
Mean 19.28
RMS 1.368
Underflow 0
Overflow 2.844e+04
10^5
10^4
10^3
10^2
-200
-150
-100
-50
0
50
100
150
200


FE6, Chip 7, ADC distribution
FE6Chip07Sig
Entries 316044
Mean 1.904e+04
RMS 7.734
Underflow 2.876e+05
Overflow 0
10^4
10^3
10^2
18000
18200
18400
18600
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19000
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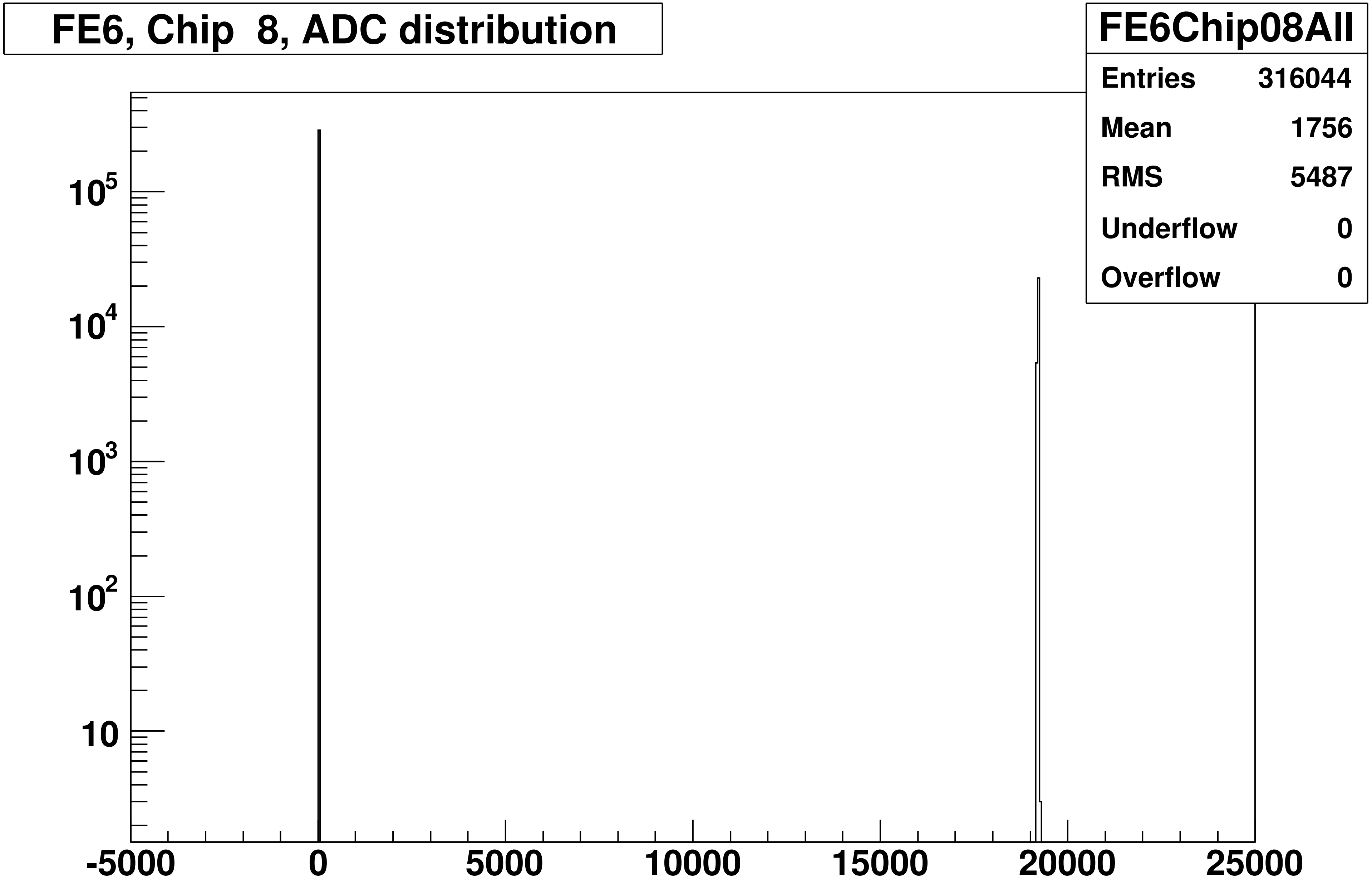
FE6, Chip 8, ADC distribution
FE6Chip08All
Entries 316044
Mean 1756
RMS 5487
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
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-5000
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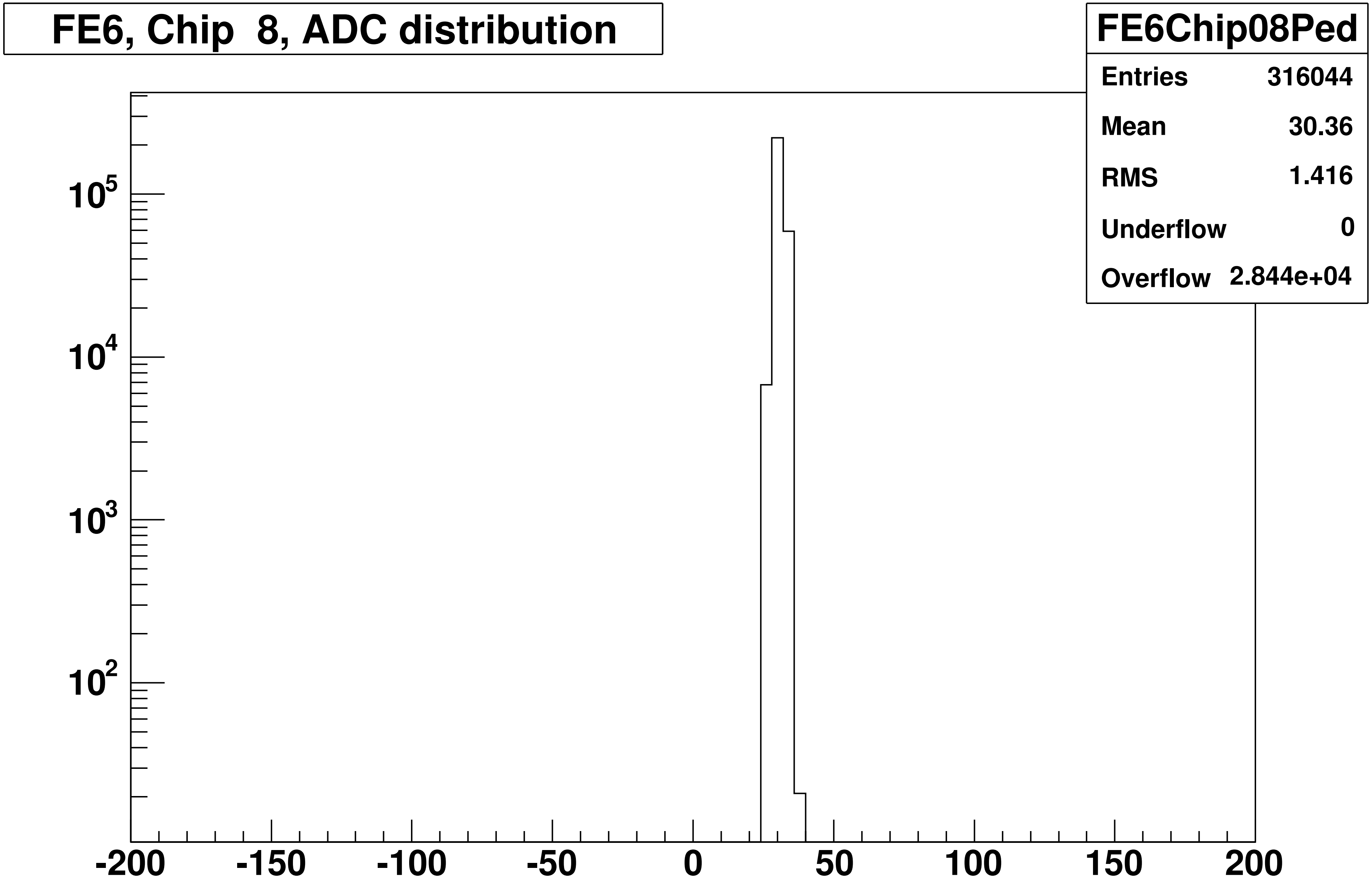

FE6, Chip 8, ADC distribution
FE6Chip08Ped
Entries 316044
Mean 30.36
RMS 1.416
Underflow 0
Overflow 2.844e+04
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10^3
10^2
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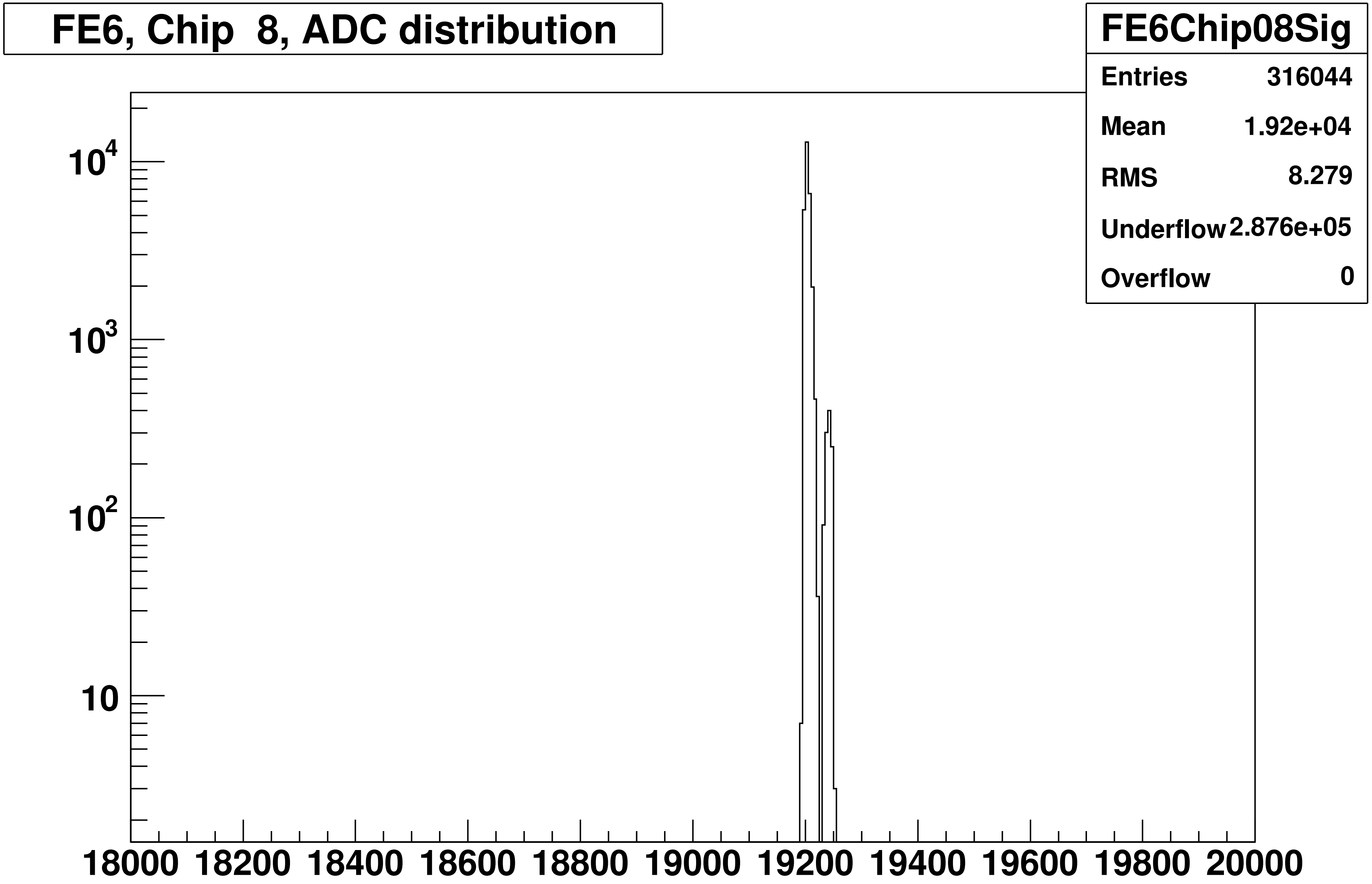
150
200


FE6, Chip 8, ADC distribution
FE6Chip08Sig
Entries 316044
Mean 1.92e+04
RMS 8.279
Underflow 2.876e+05
Overflow 0
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10^3
10^2
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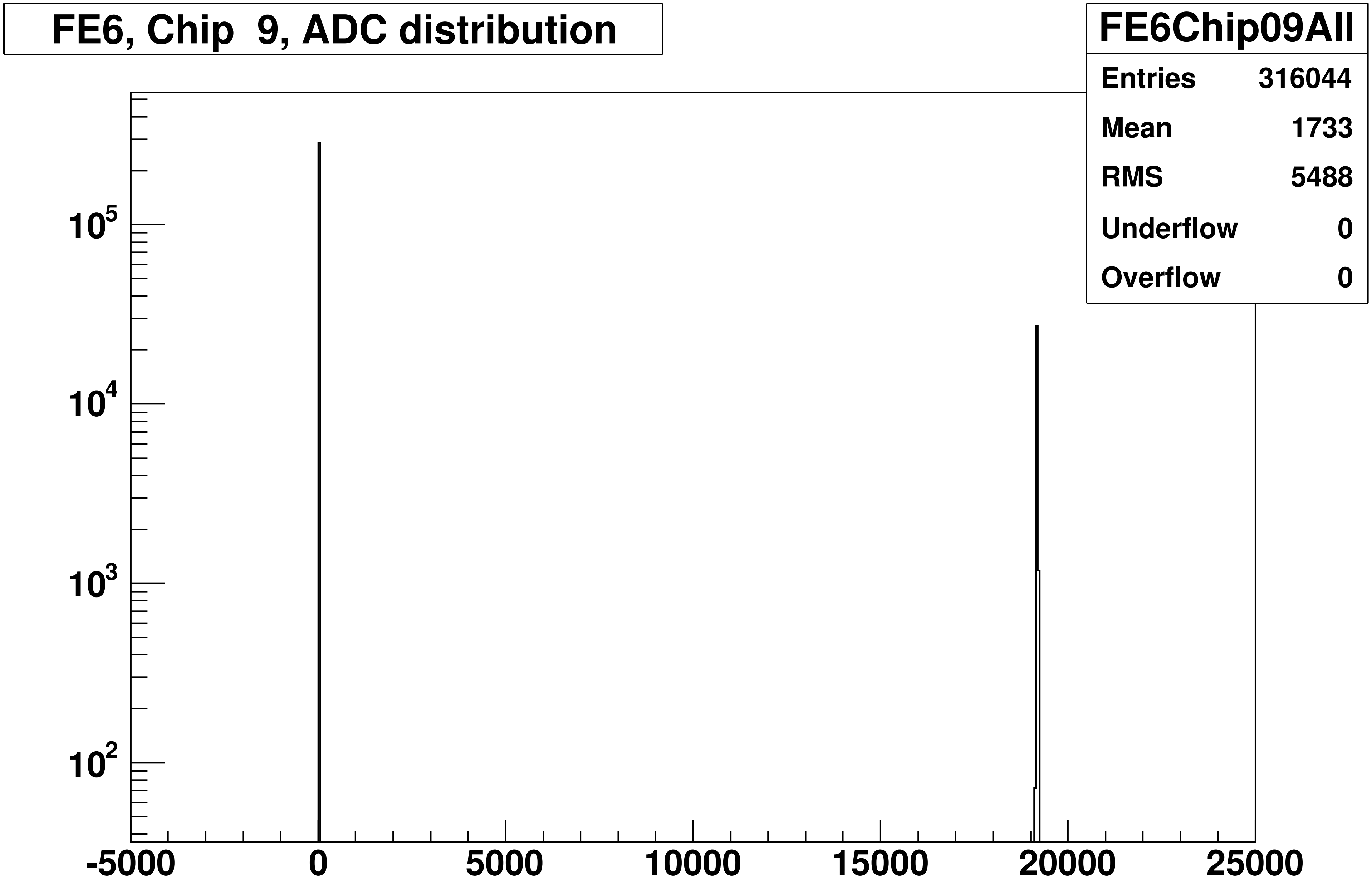
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE6, Chip 9, ADC distribution
FE6Chip09All
Entries 316044
Mean 1733
RMS 5488
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
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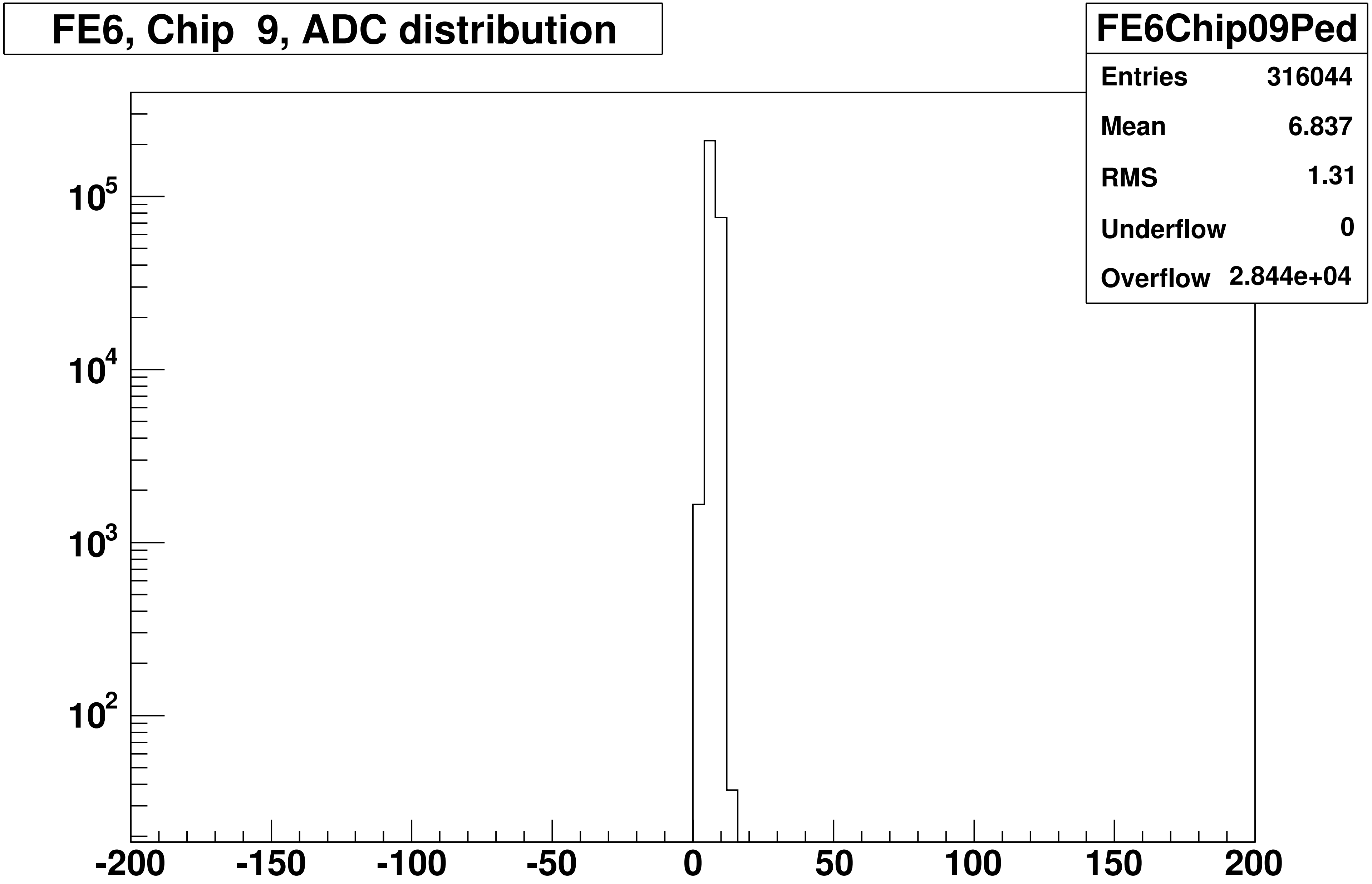
0
5000
10000
15000
20000
25000


FE6, Chip 9, ADC distribution
FE6Chip09Ped
Entries 316044
Mean 6.837
RMS 1.31
Underflow 0
Overflow 2.844e+04
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10^4
10^3
10^2
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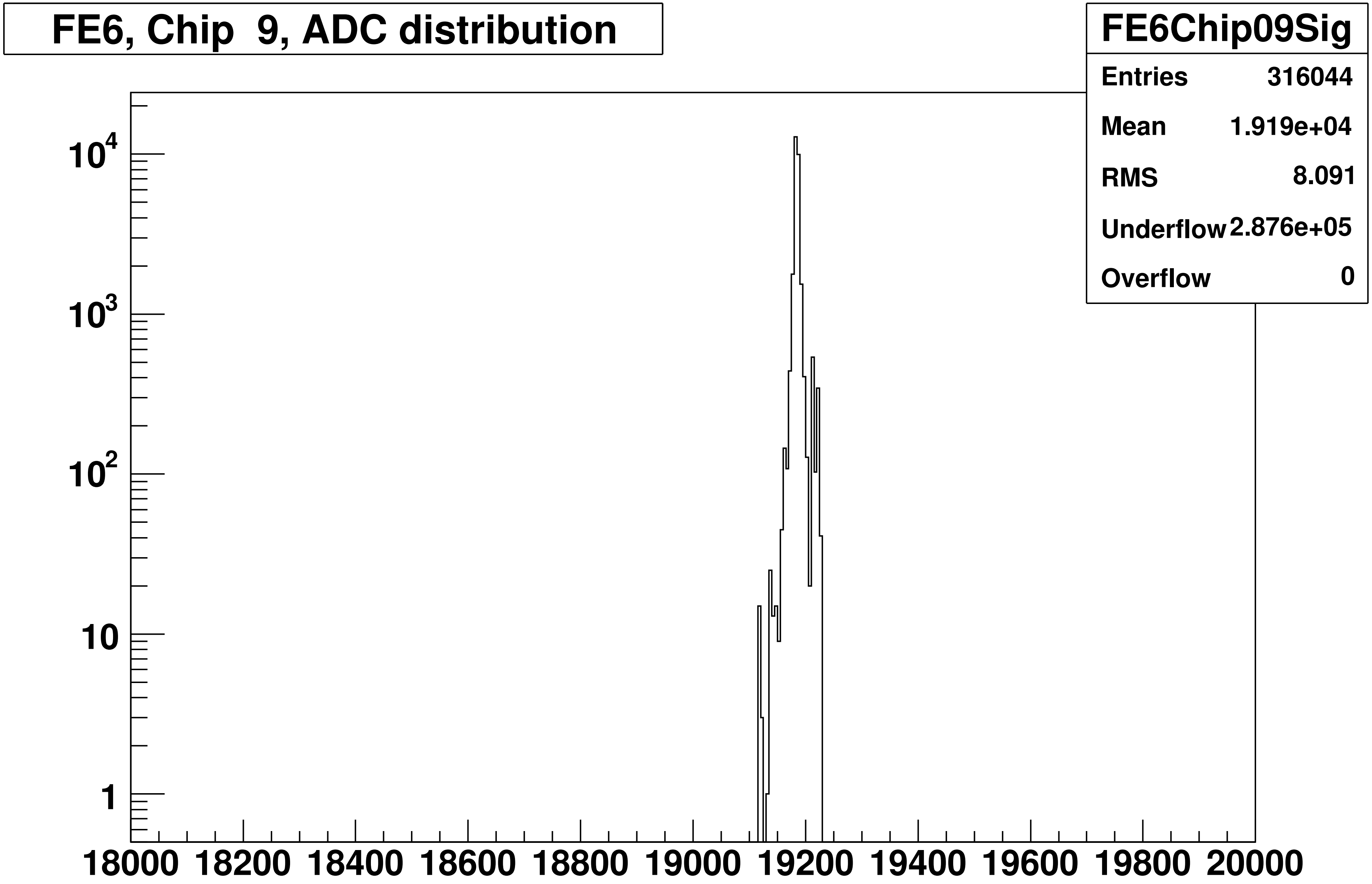
100
150
200


FE6, Chip 9, ADC distribution
FE6Chip09Sig
Entries 316044
Mean 1.919e+04
RMS 8.091
Underflow 2.876e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
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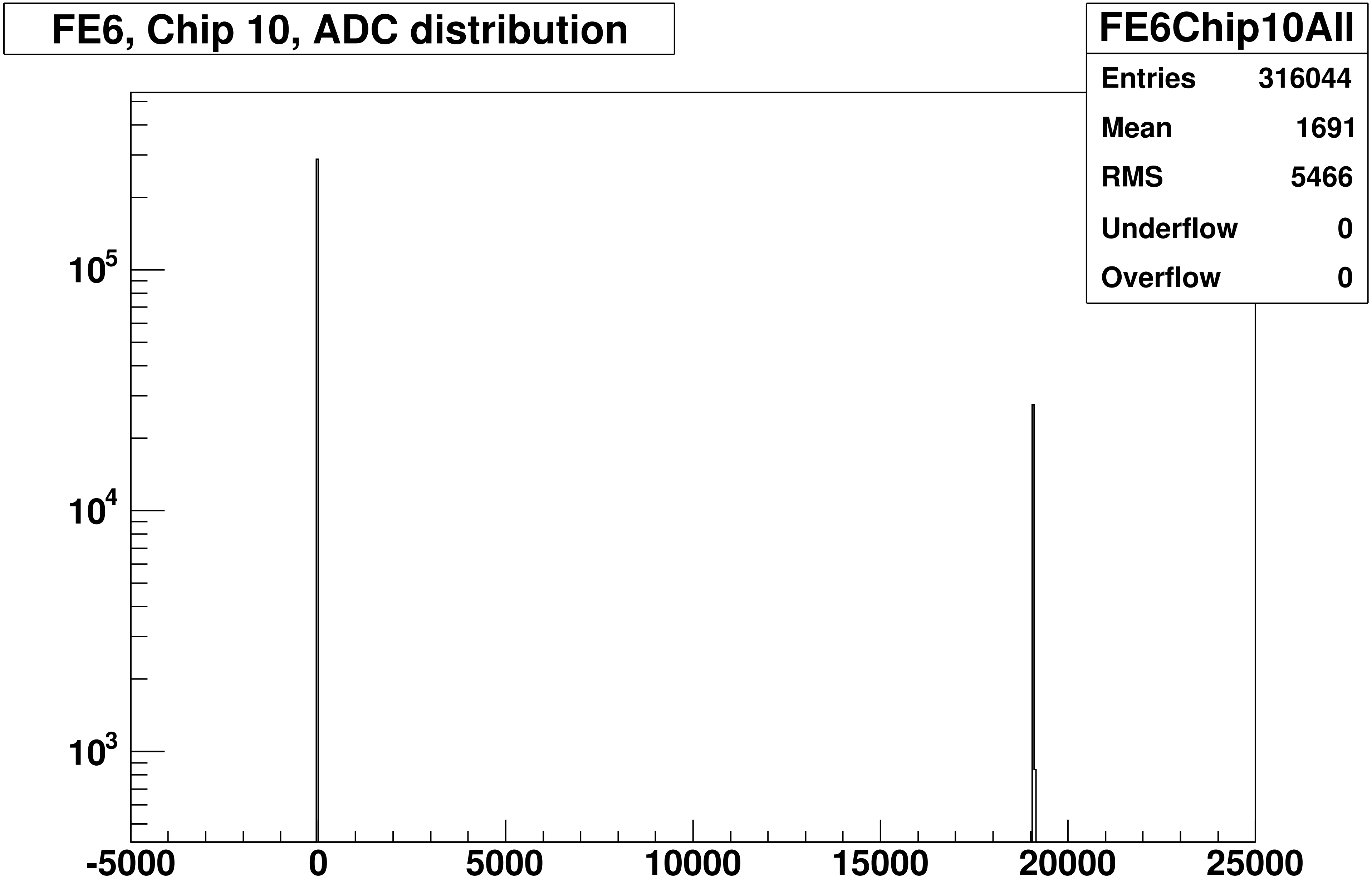
19000
19200
19400
19600
19800
20000


FE6, Chip 10, ADC distribution
FE6Chip10All
Entries 316044
Mean 1691
RMS 5466
Underflow 0
Overflow 0
10^5
10^4
10^3
-5000
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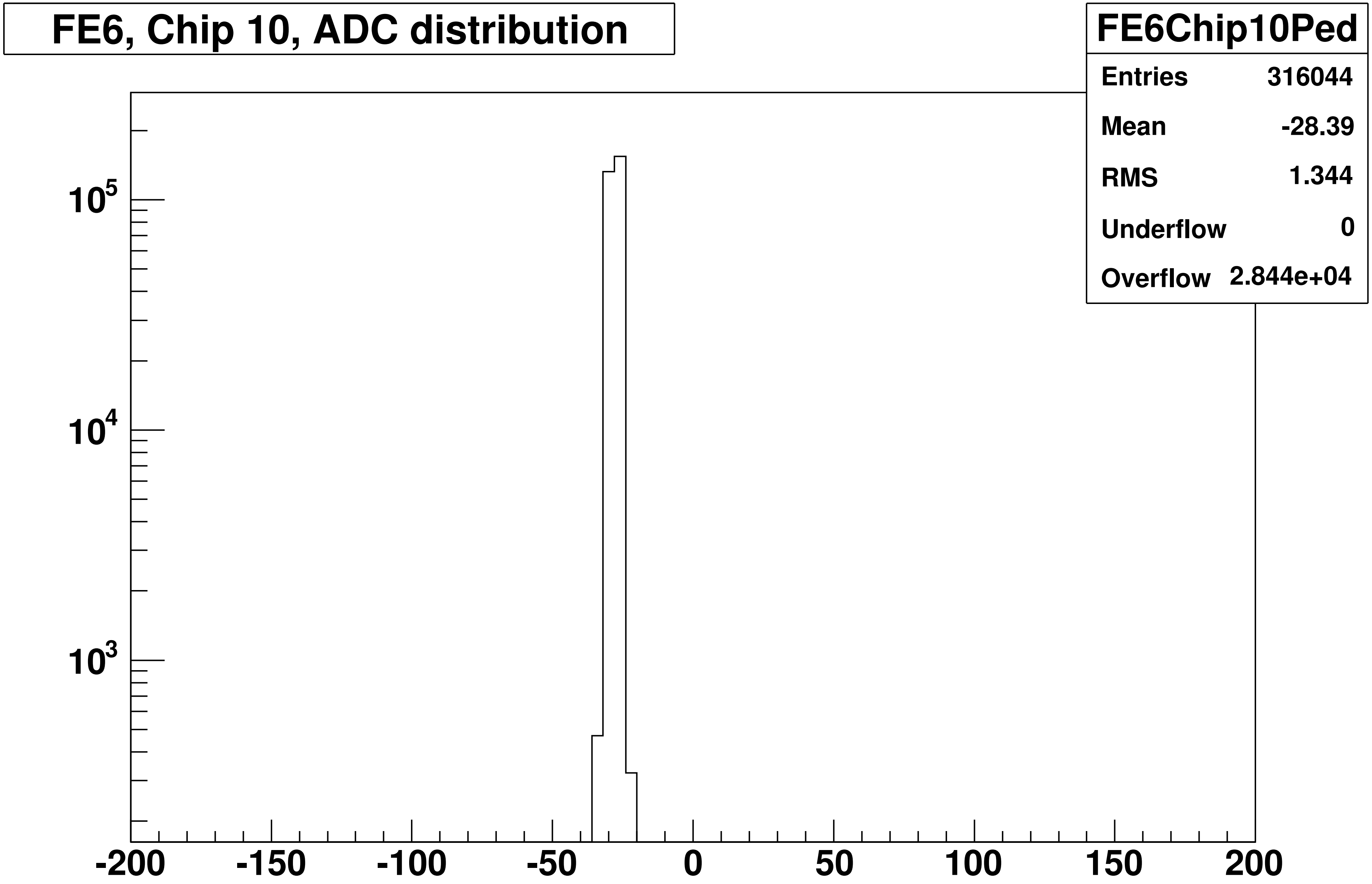
10000
15000
20000
25000



FE6, Chip 10, ADC distribution
FE6Chip10Ped
Entries 316044
Mean -28.39
RMS 1.344
Underflow 0
Overflow 2.844e+04
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10^4
10^3
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-100
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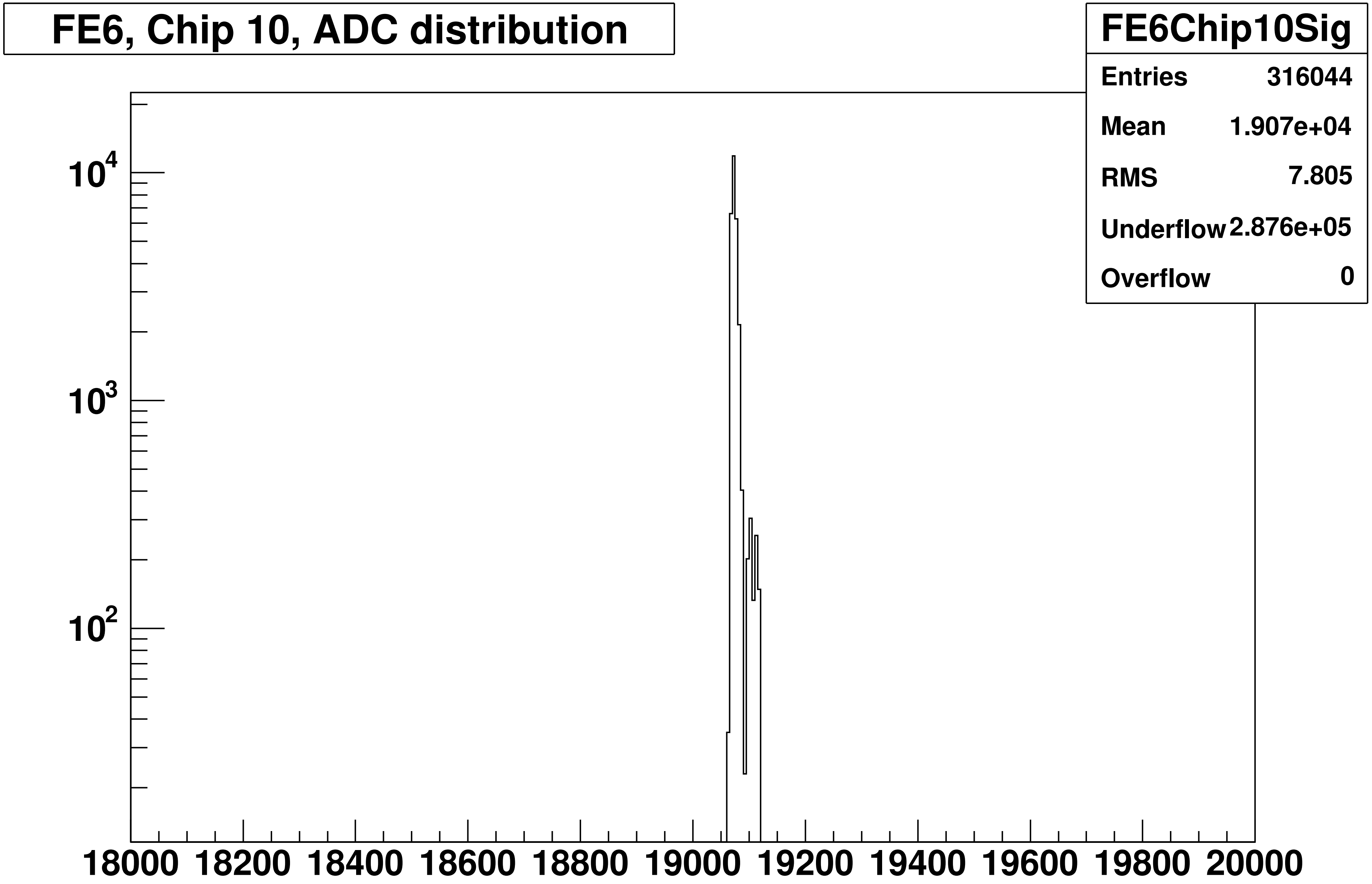
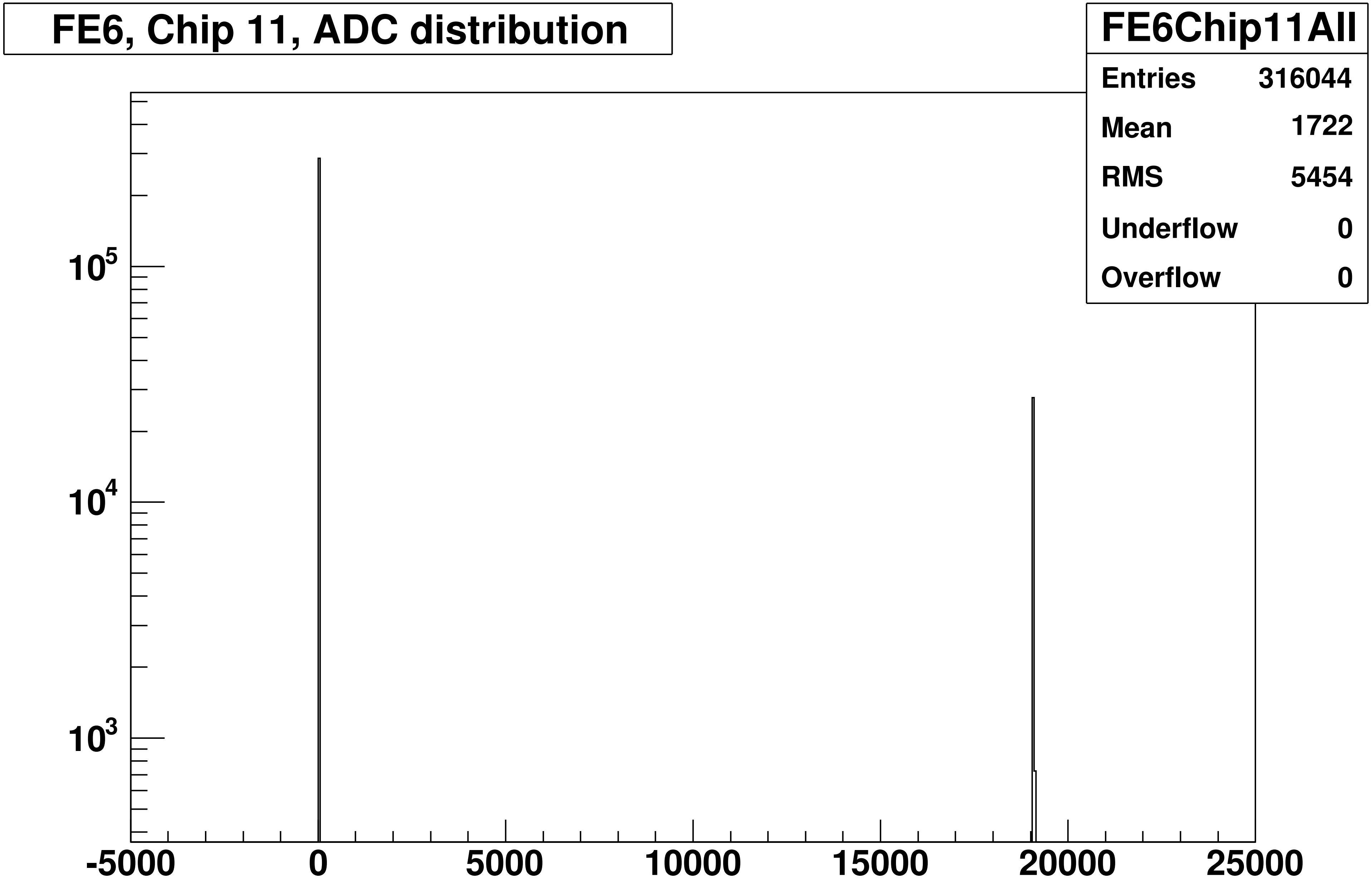
0
50
100
150
200


FE6, Chip 10, ADC distribution
FE6Chip10Sig
Entries 316044
Mean 1.907e+04
RMS 7.805
Underflow 2.876e+05
Overflow 0
10^4
10^3
10^2
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE6, Chip 11, ADC distribution
FE6Chip11All
Entries 316044
Mean 1722
RMS 5454
Underflow 0
Overflow 0
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10^4
10^3
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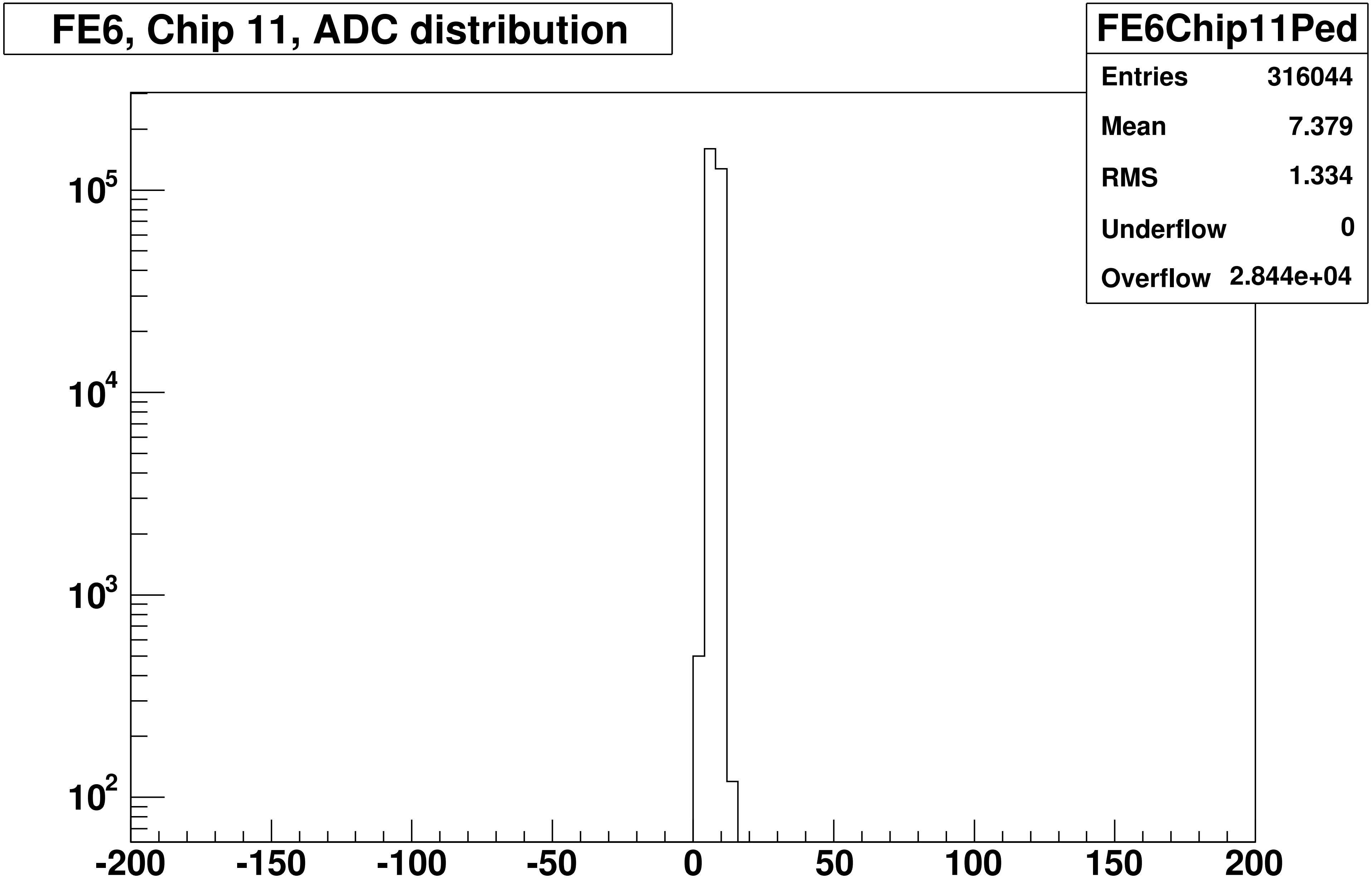
10000
15000
20000
25000


FE6, Chip 11, ADC distribution
FE6Chip11Ped
Entries 316044
Mean 7.379
RMS 1.334
Underflow 0
Overflow 2.844e+04
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10^4
10^3
10^2
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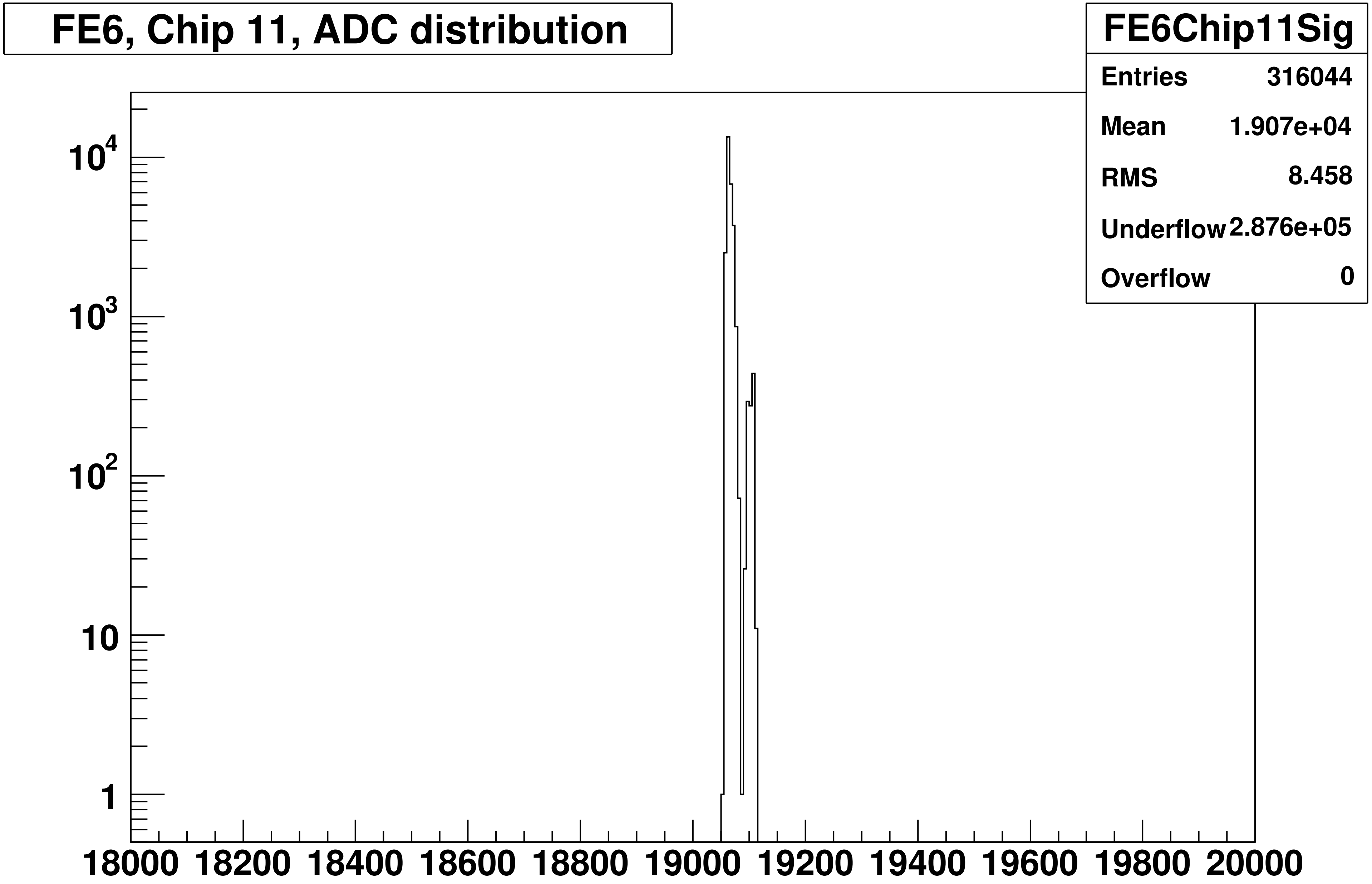
150
200


FE6, Chip 11, ADC distribution
FE6Chip11Sig
Entries 316044
Mean 1.907e+04
RMS 8.458
Underflow 2.876e+05
Overflow 0
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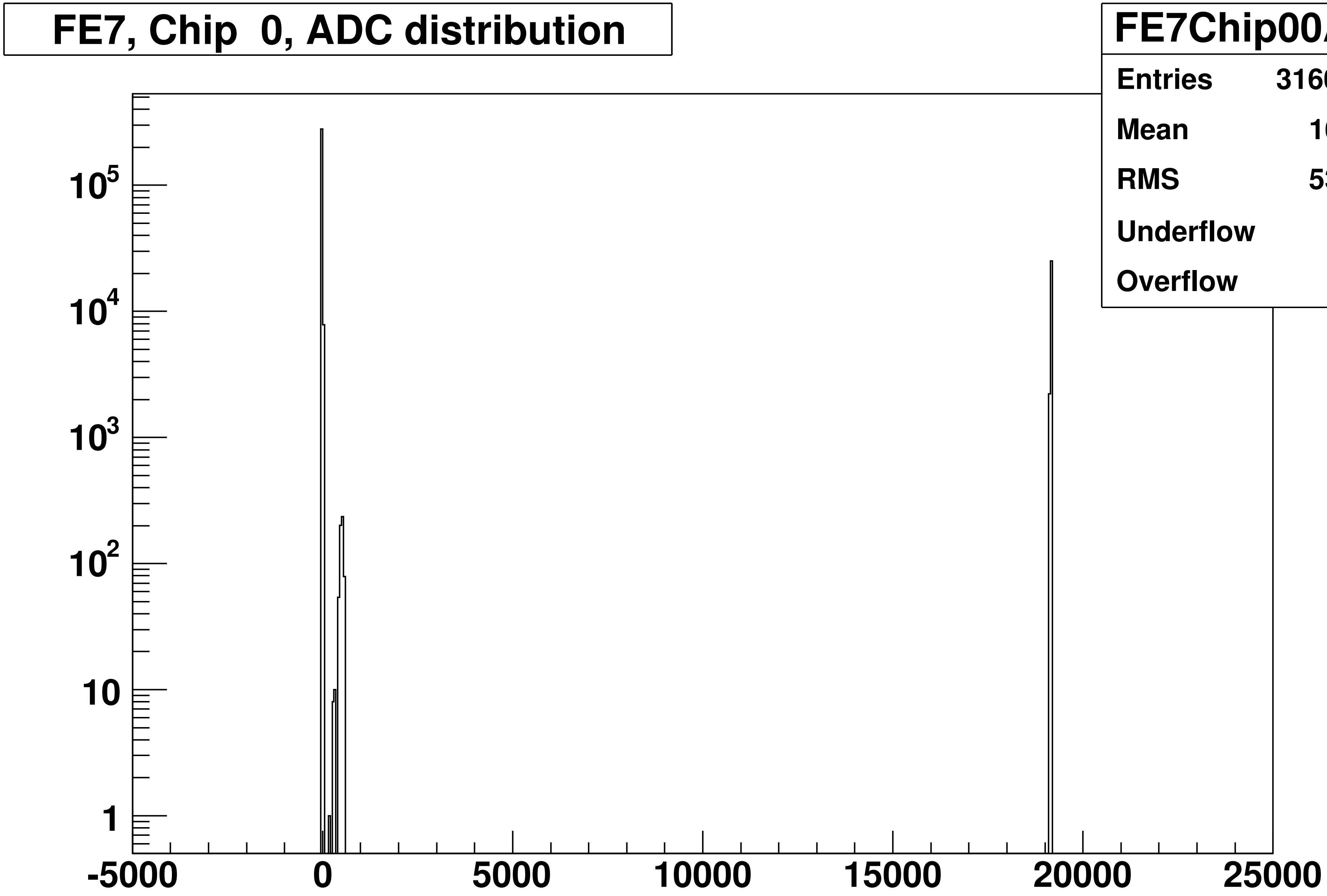
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE7, Chip 0, ADC distribution
FE7Chip00All
Entries 316044
Mean 1650
RMS 5376
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
1
-5000
0
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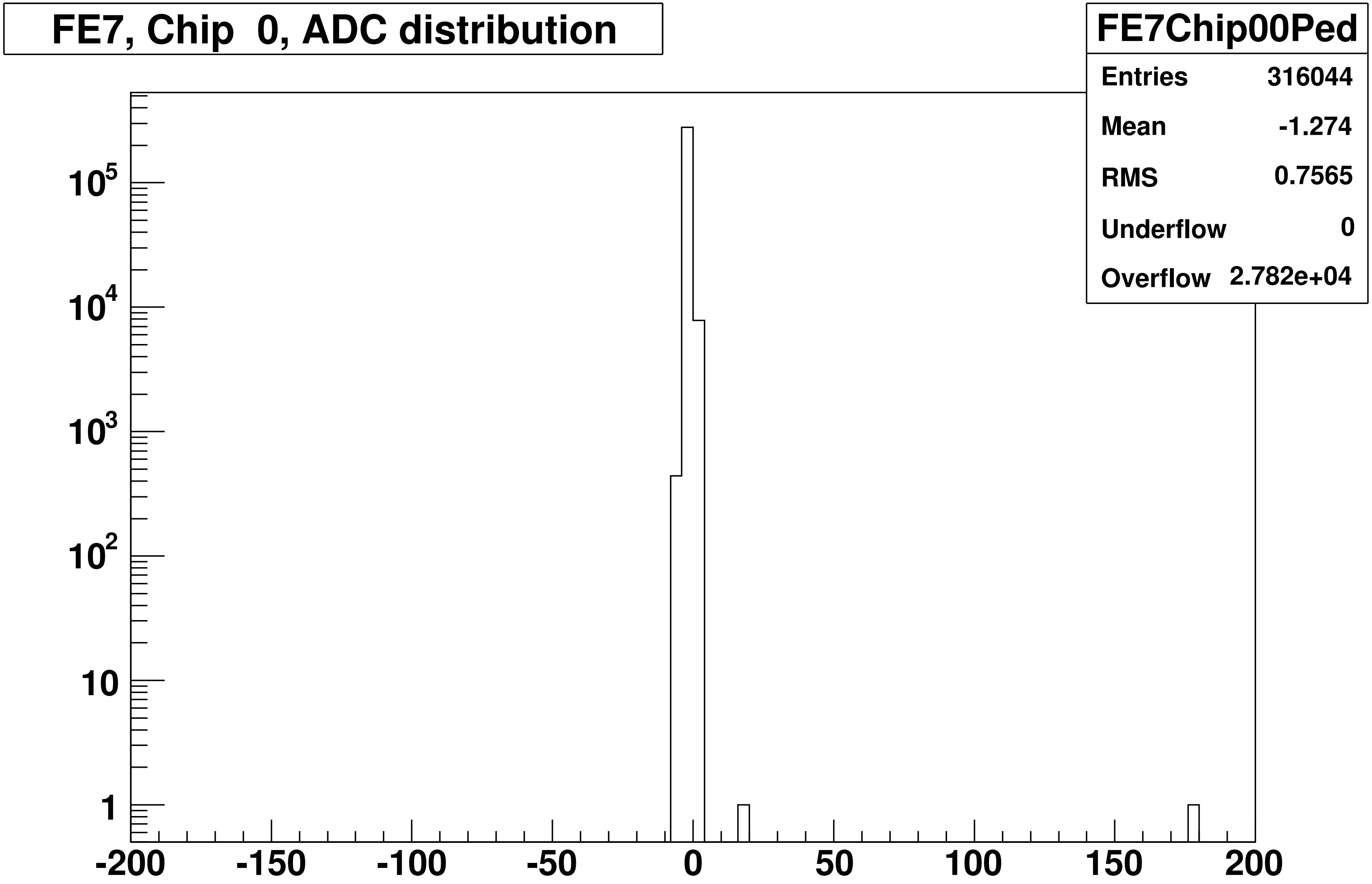
15000
20000
25000


FE7, Chip 0, ADC distribution
FE7Chip00Ped
Entries 316044
Mean -1.274
RMS 0.7565
Underflow 0
Overflow 2.782e+04
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10^4
10^3
10^2
10
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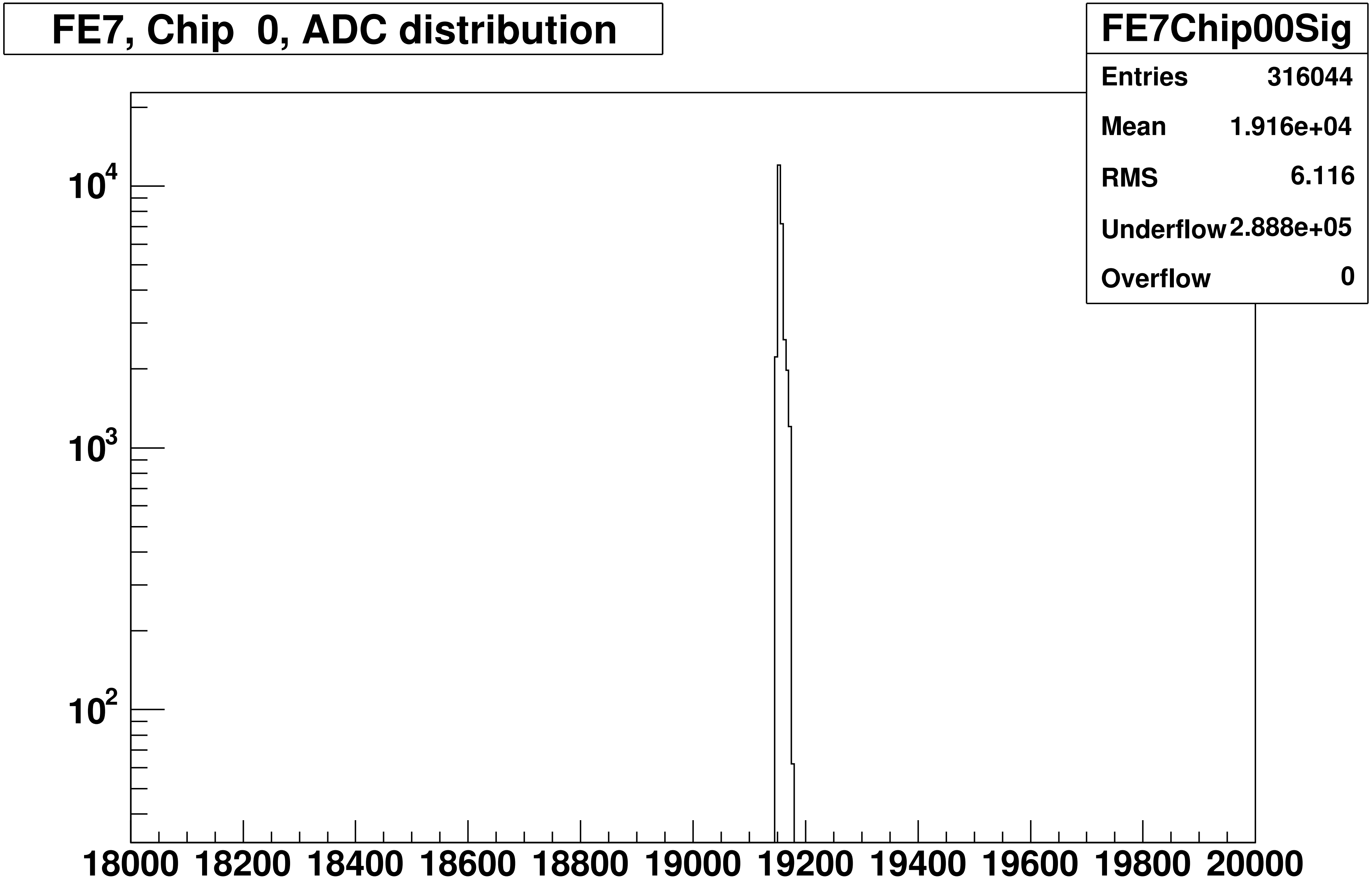
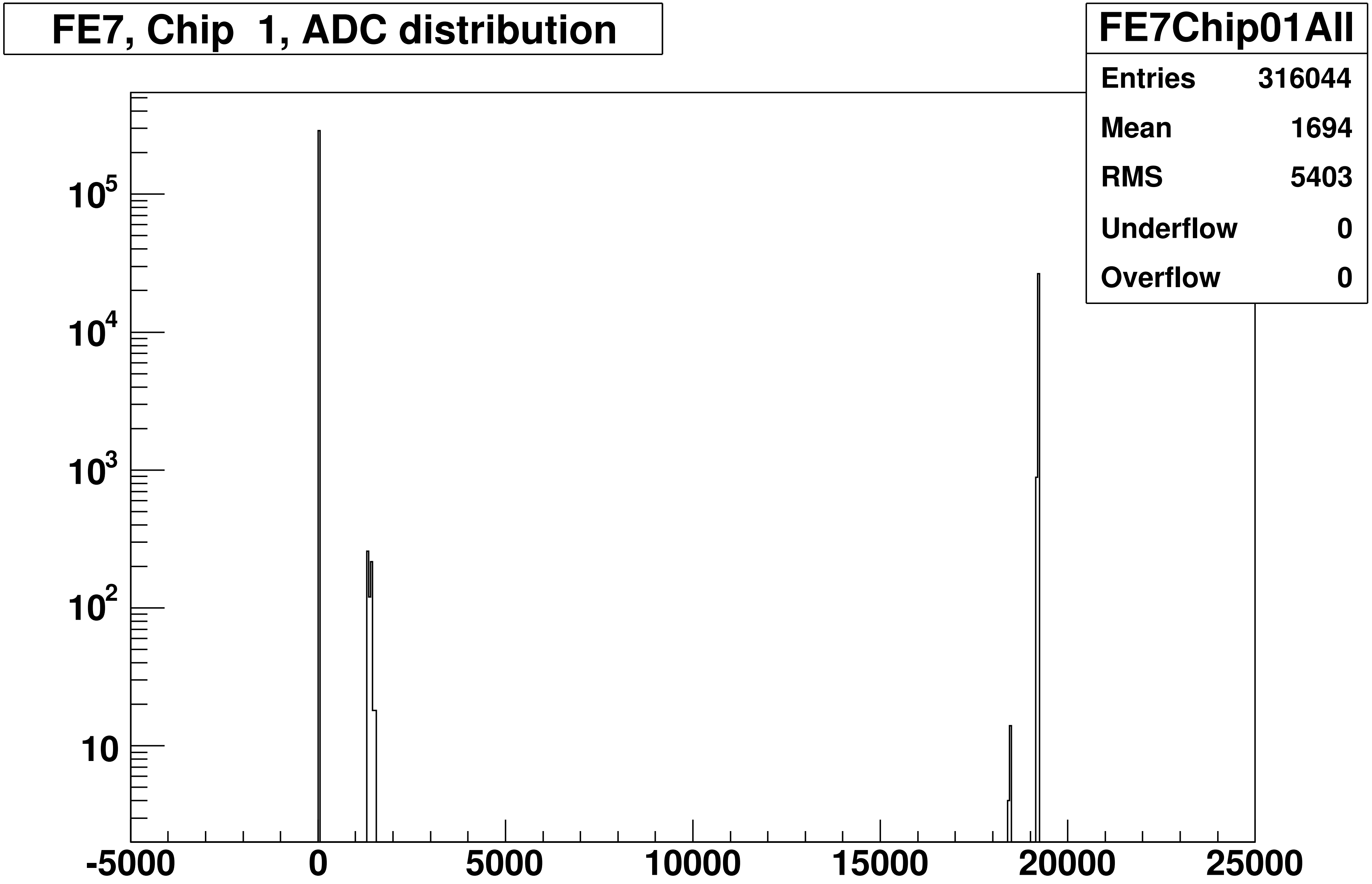
50
100
150
200


FE7, Chip 0, ADC distribution
FE7Chip00Sig
Entries 316044
Mean 1.916e+04
RMS 6.116
Underflow 2.888e+05
Overflow 0
10^4
10^3
10^2
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE7, Chip 1, ADC distribution
FE7Chip01All
Entries 316044
Mean 1694
RMS 5403
Underflow 0
Overflow 0
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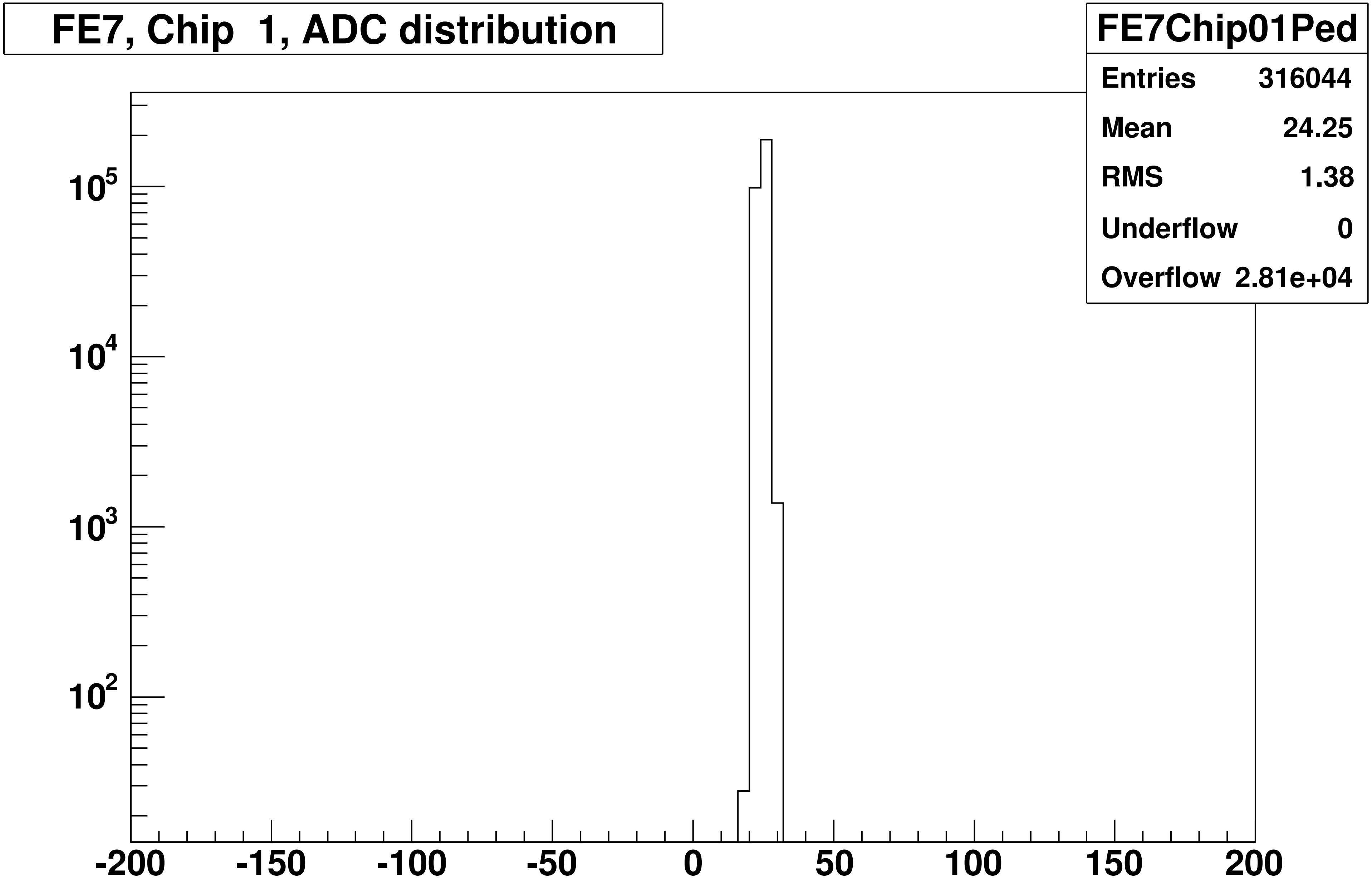
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE7, Chip 1, ADC distribution
FE7Chip01Ped
Entries 316044
Mean 24.25
RMS 1.38
Underflow 0
Overflow 2.81e+04
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10^4
10^3
10^2
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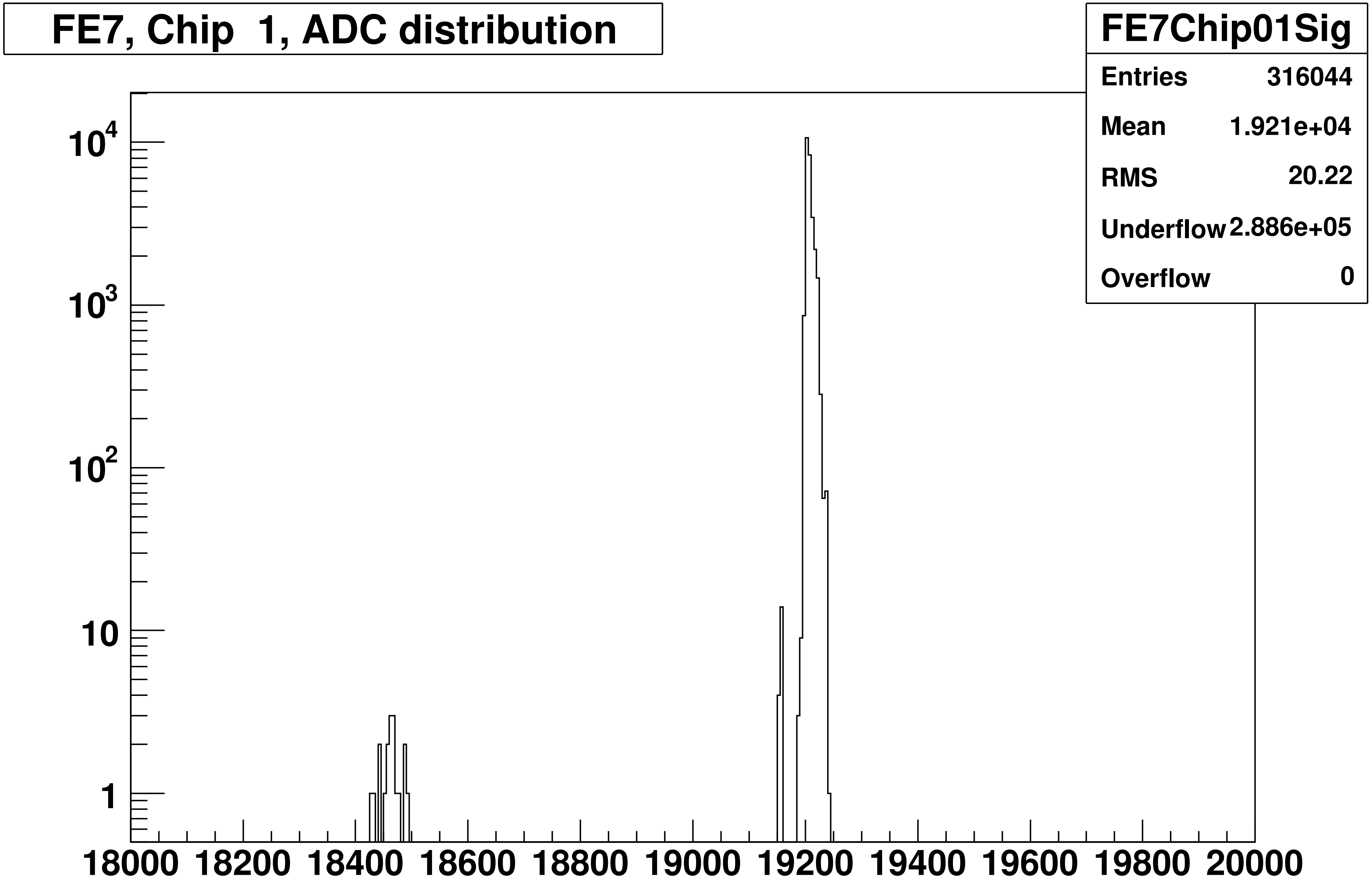
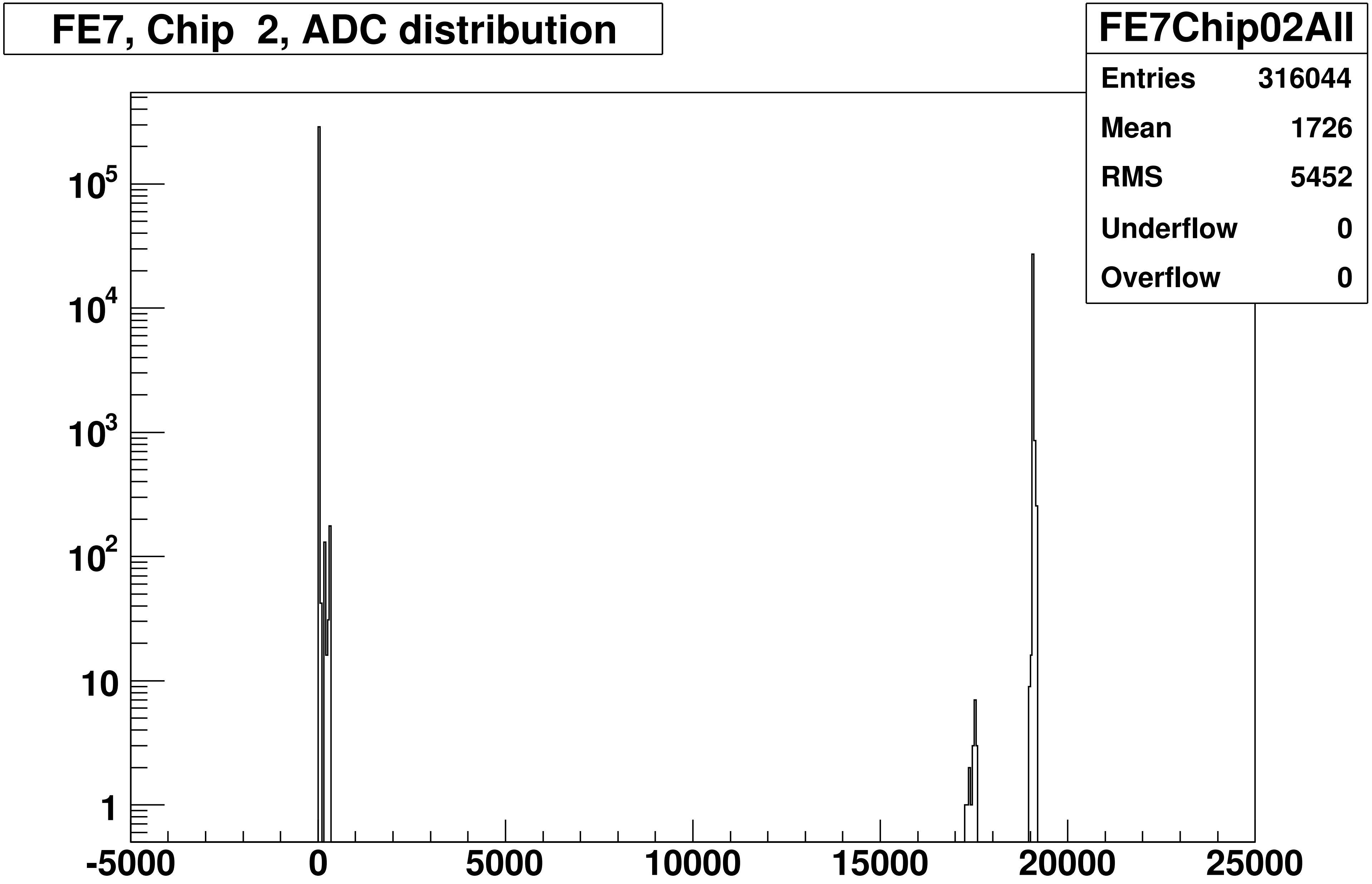
-100
-50
0
50
100
150
200


FE7, Chip 1, ADC distribution
FE7Chip01Sig
Entries 316044
Mean 1.921e+04
RMS 20.22
Underflow 2.886e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE7, Chip 2, ADC distribution
FE7Chip02All
Entries 316044
Mean 1726
RMS 5452
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
1
-5000
0
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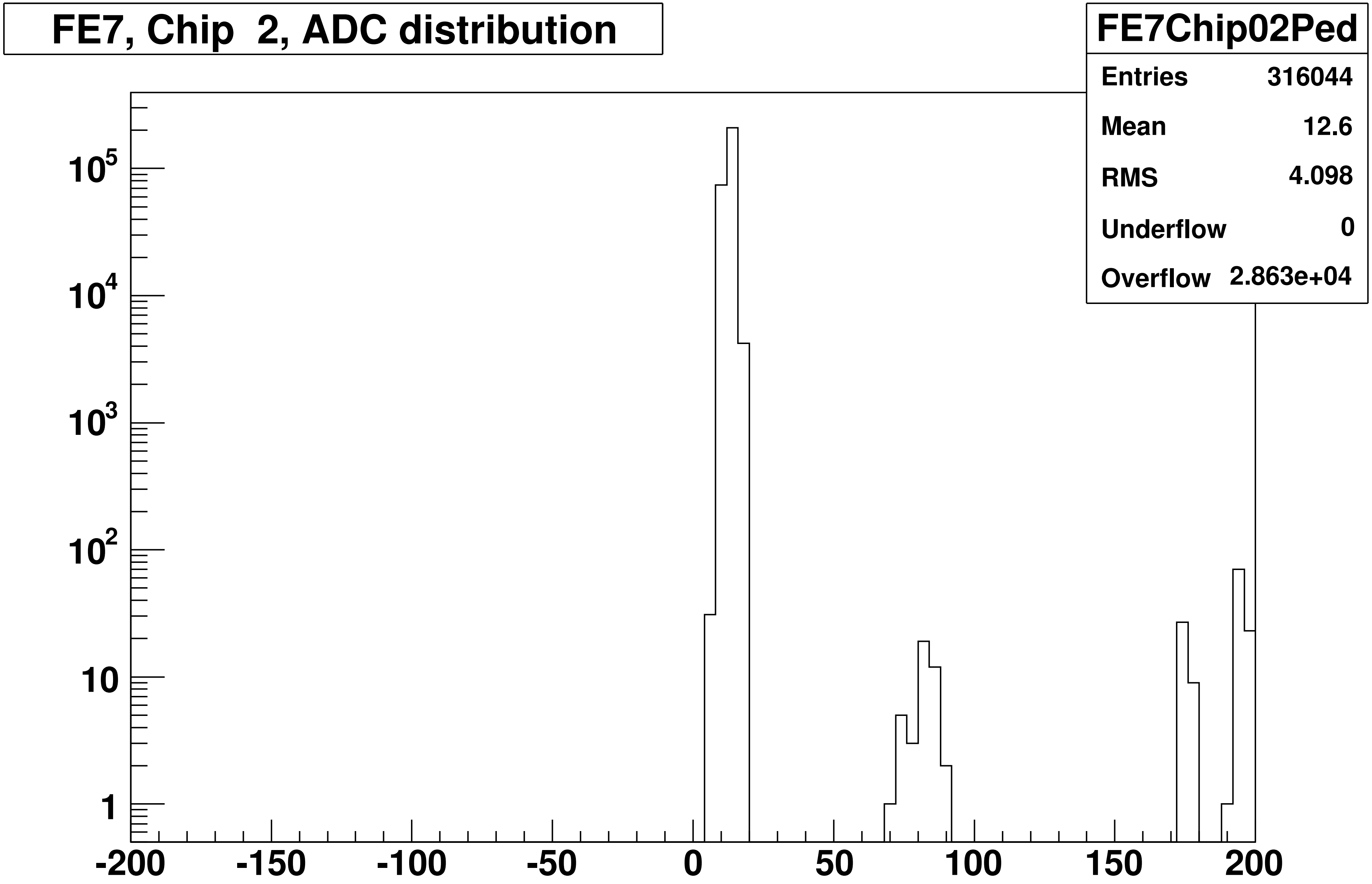
15000
20000
25000


FE7, Chip 2, ADC distribution
FE7Chip02Ped
Entries 316044
Mean 12.6
RMS 4.098
Underflow 0
Overflow 2.863e+04
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10^4
10^3
10^2
10
1
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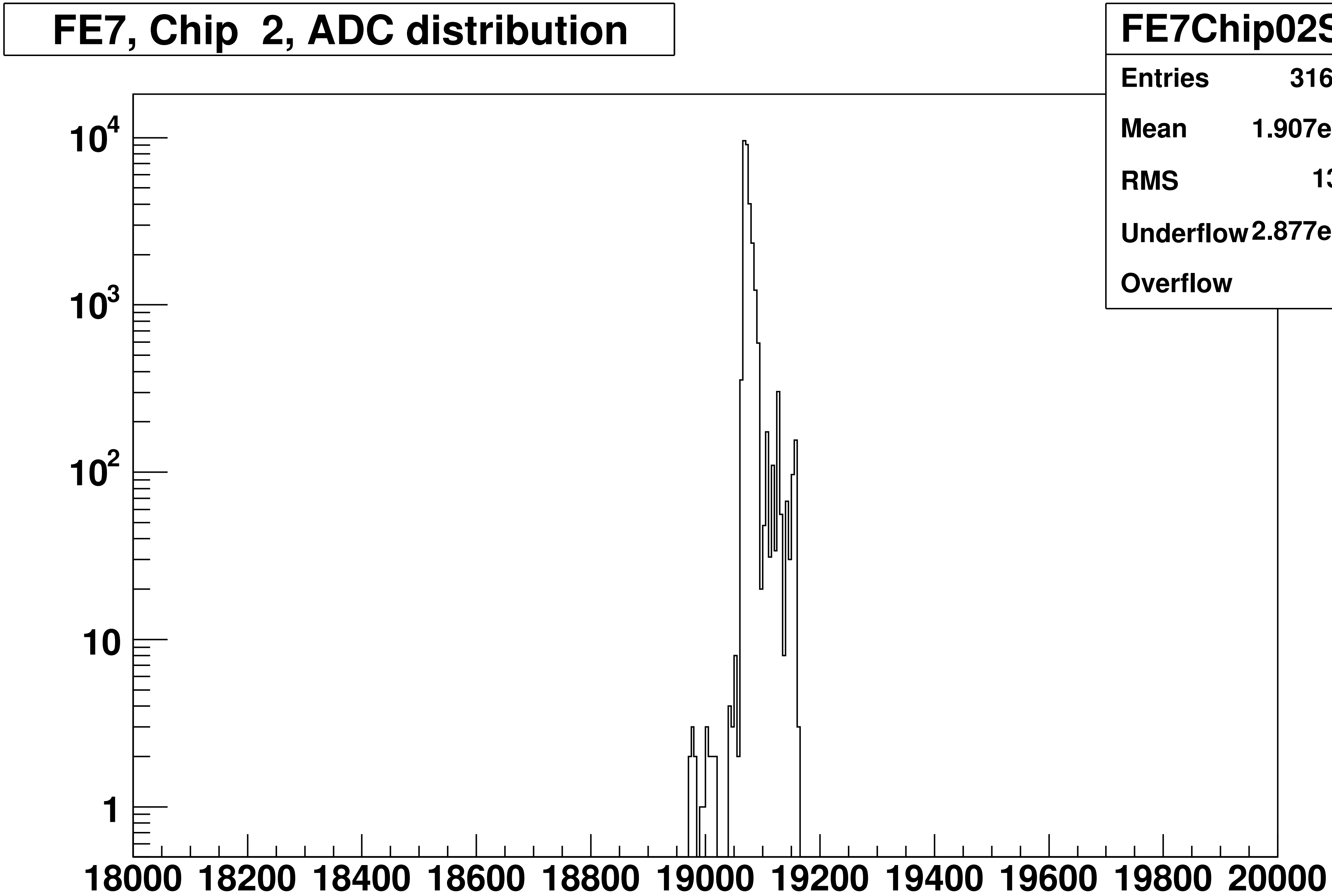
-100
-50
0
50
100
150
200


FE7, Chip 2, ADC distribution
FE7Chip02Sig
Entries 316044
Mean 1.907e+04
RMS 13.24
Underflow 2.877e+05
Overflow 0
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10^3
10^2
10
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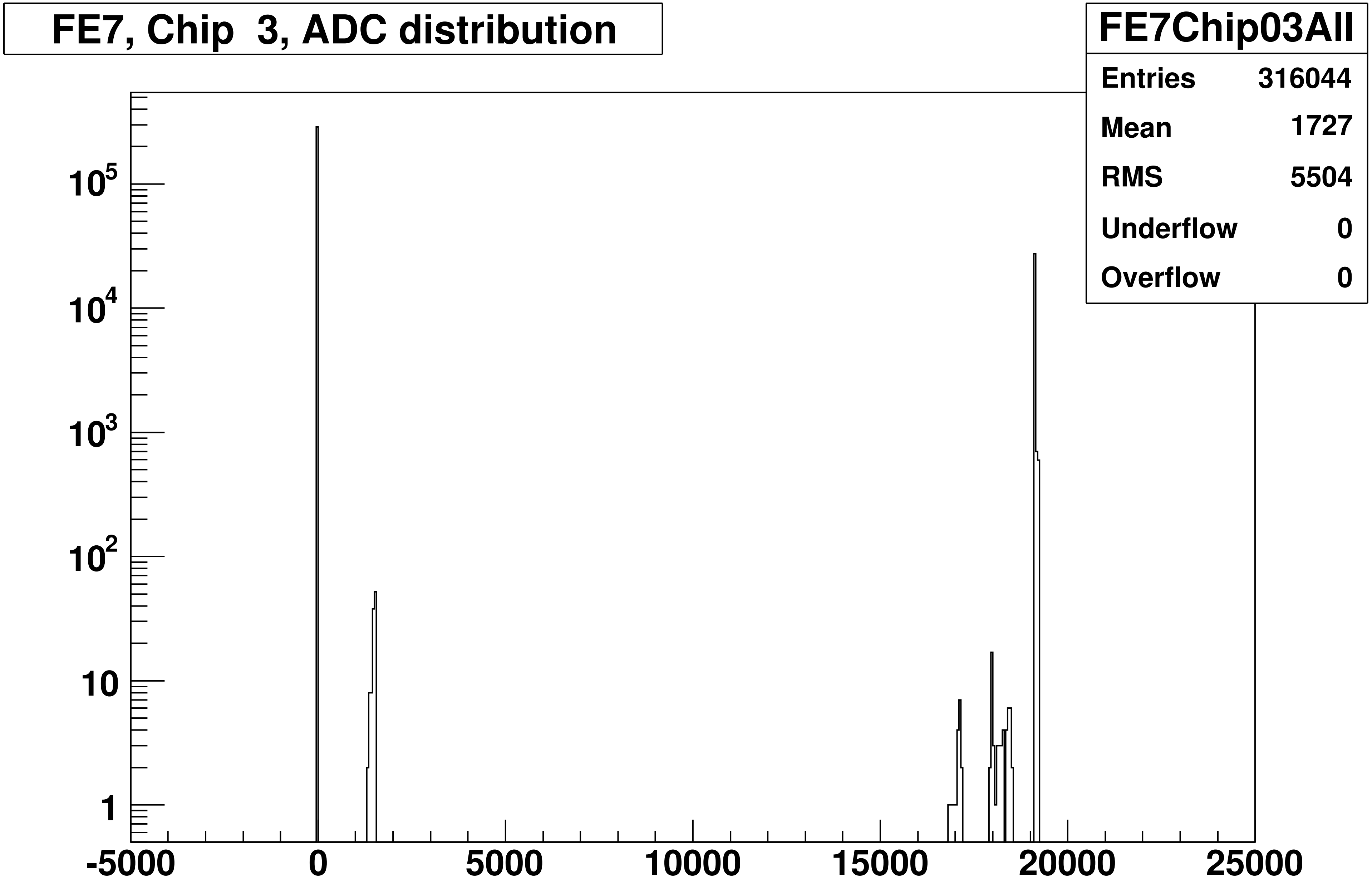
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE7, Chip 3, ADC distribution
FE7Chip03All
Entries 316044
Mean 1727
RMS 5504
Underflow 0
Overflow 0
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10^3
10^2
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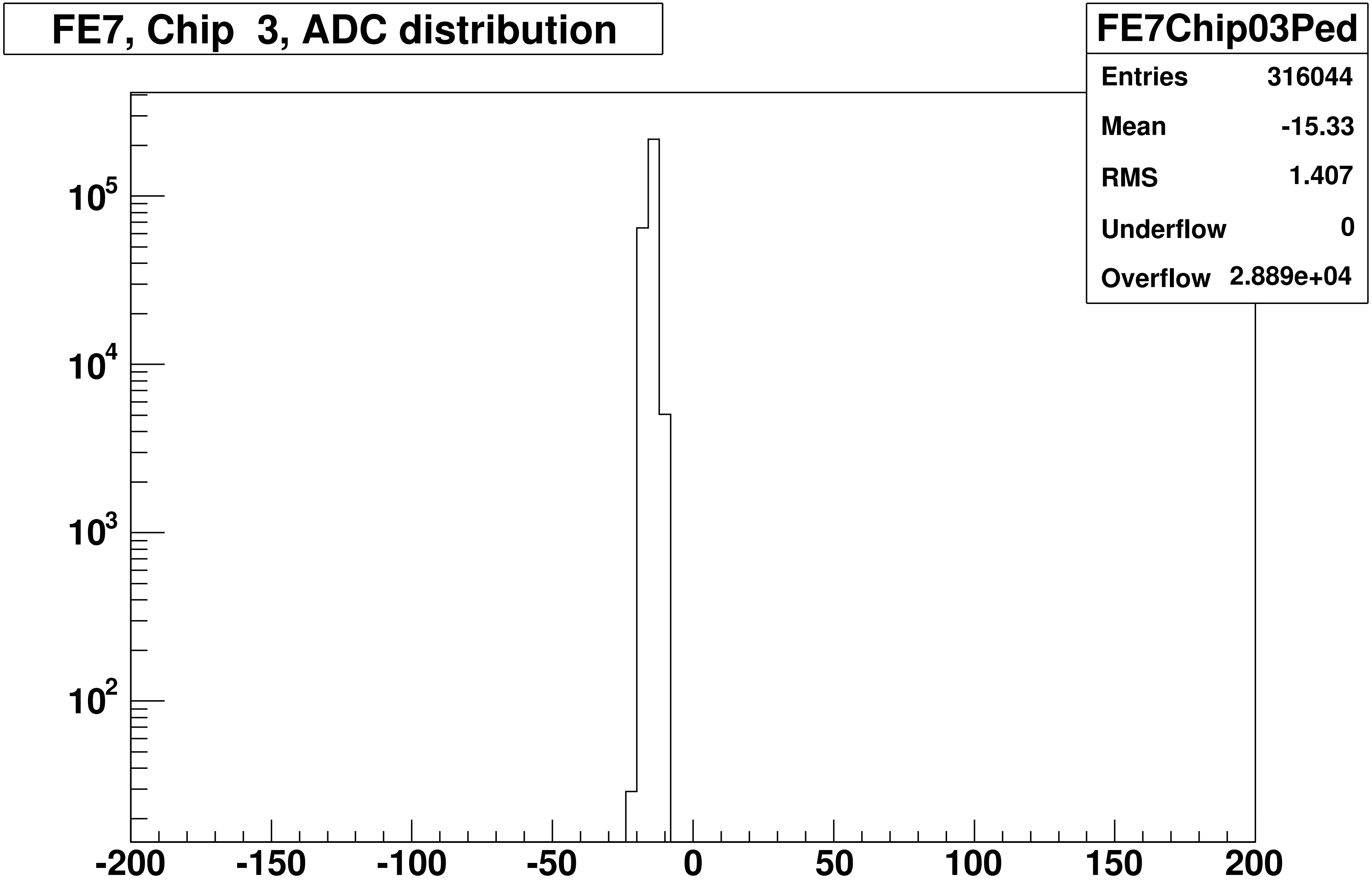
FE7, Chip 3, ADC distribution
FE7Chip03Ped
Entries 316044
Mean -15.33
RMS 1.407
Underflow 0
Overflow 2.889e+04
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10^4
10^3
10^2
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150
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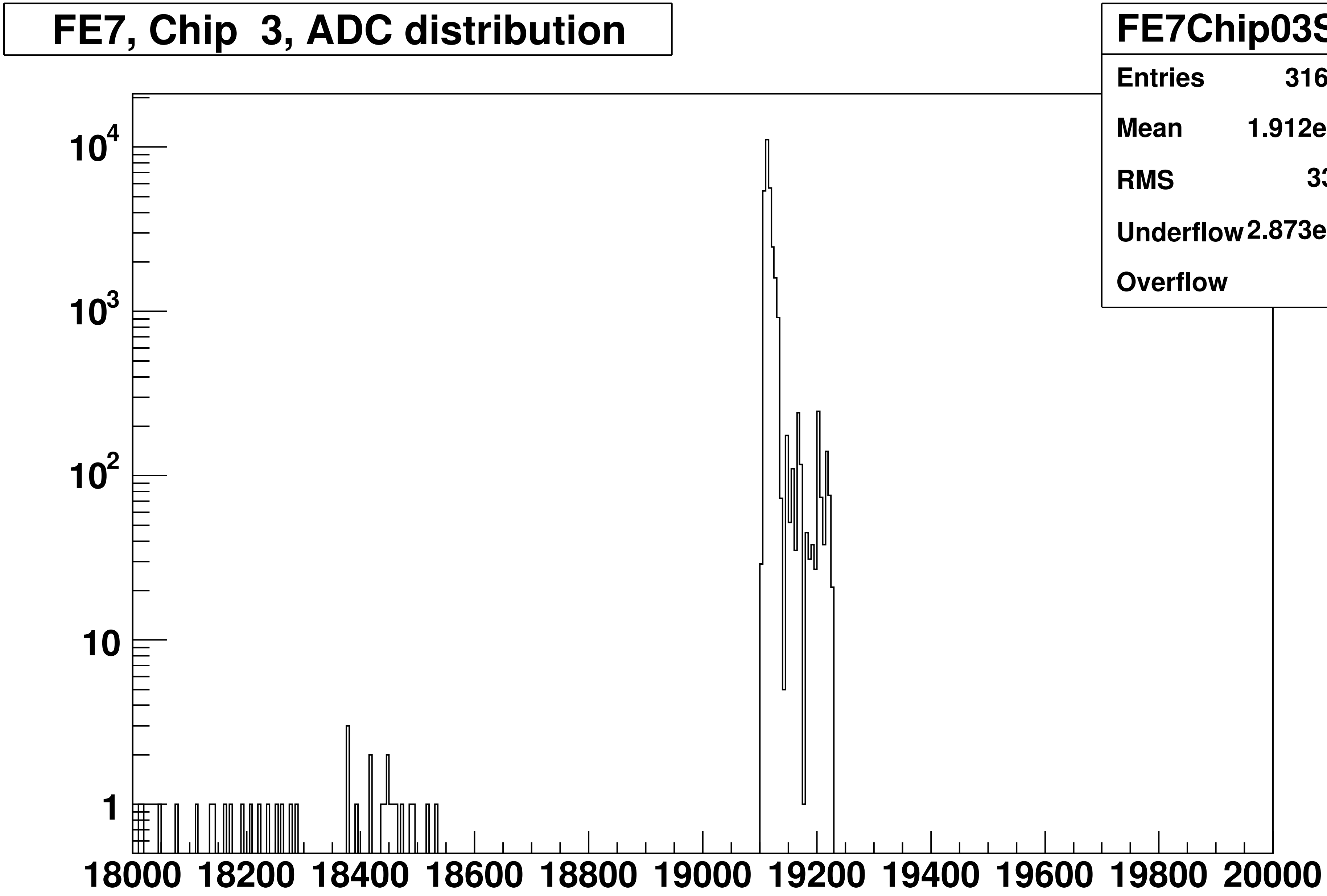
FE7, Chip 3, ADC distribution
FE7Chip03Sig
Entries 316044
Mean 1.912e+04
RMS 33.55
Underflow 2.873e+05
Overflow 0
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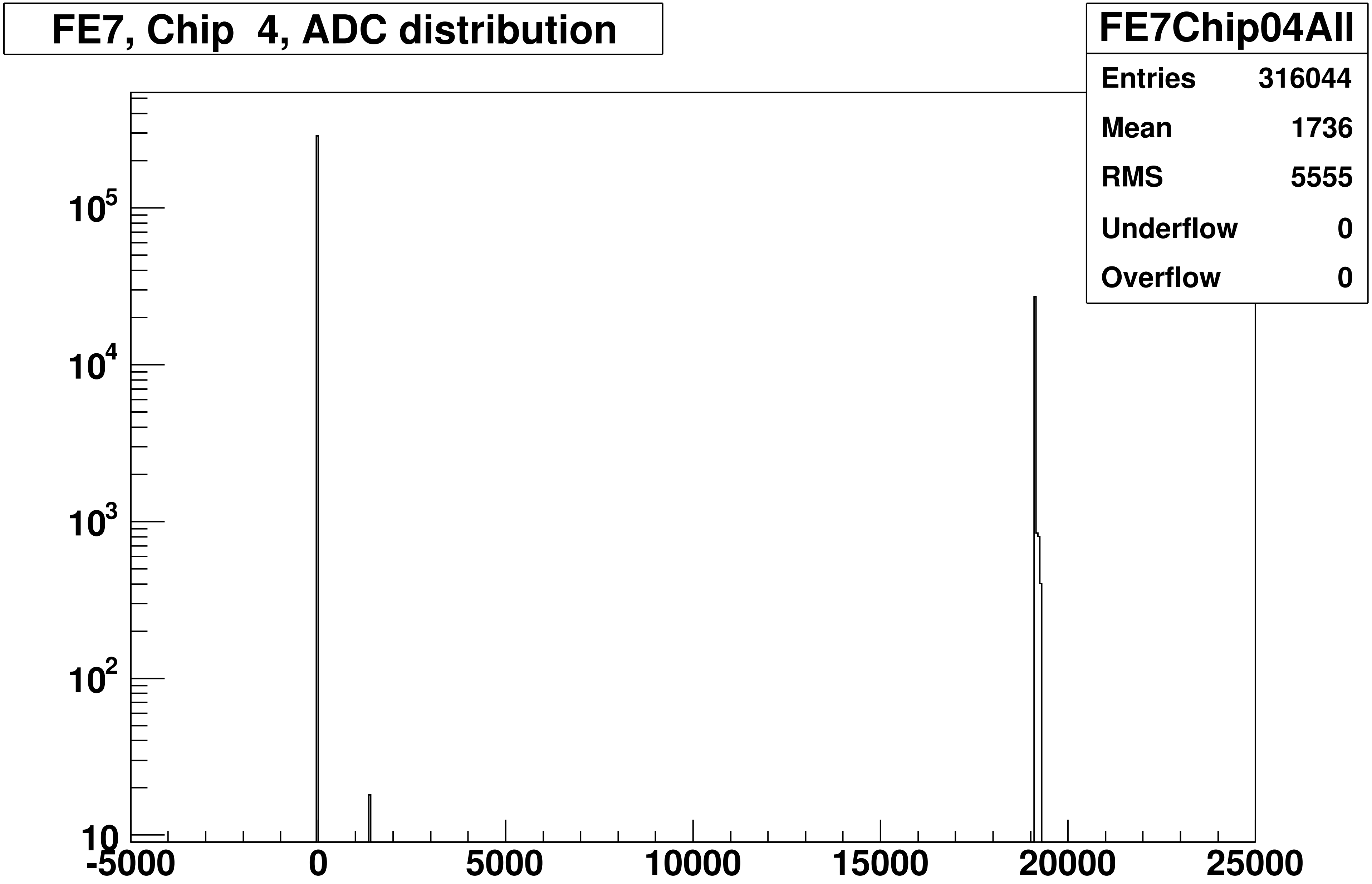
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE7, Chip 4, ADC distribution
FE7Chip04All
Entries 316044
Mean 1736
RMS 5555
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
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15000
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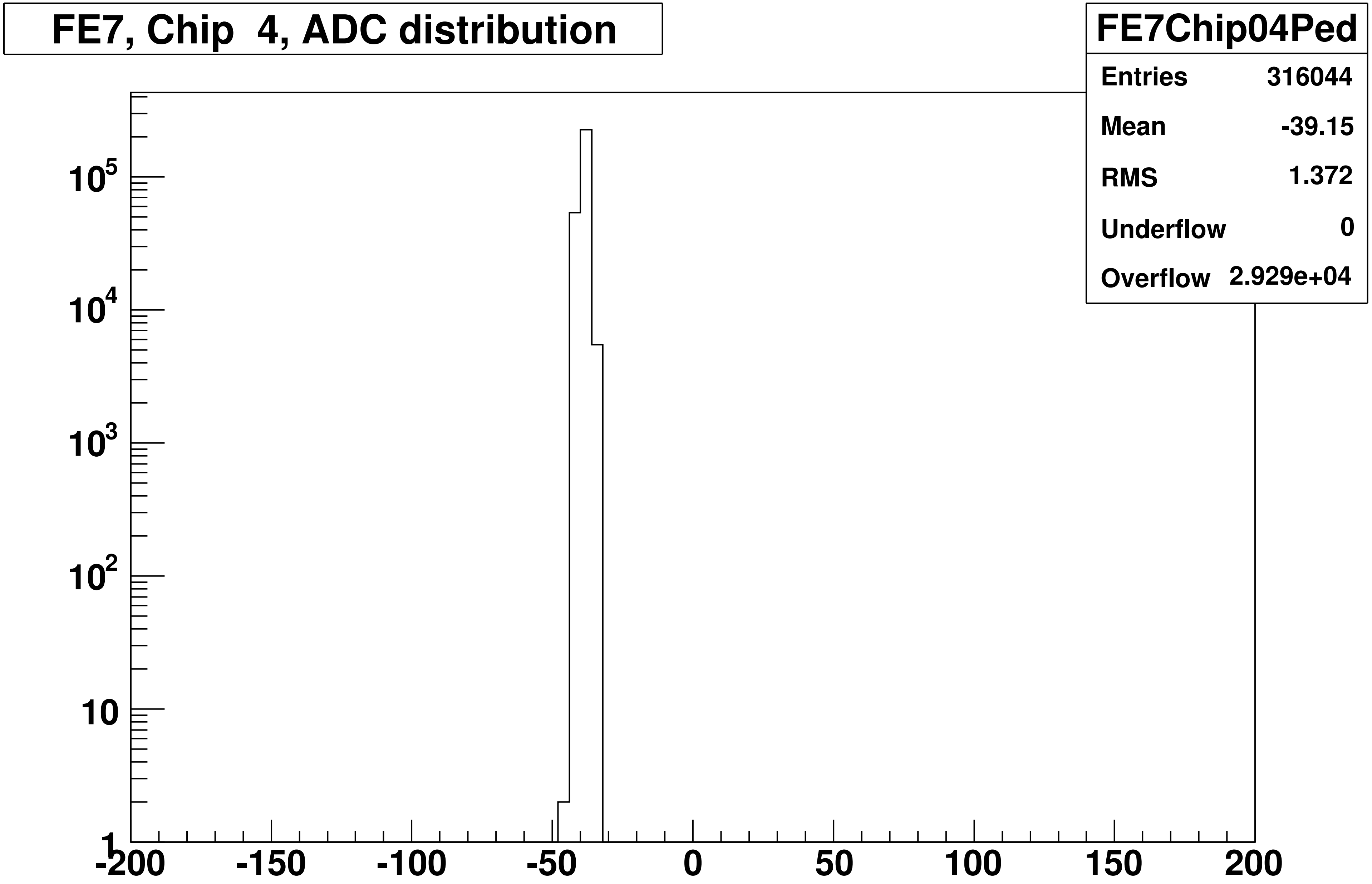
25000



FE7, Chip 4, ADC distribution
FE7Chip04Ped
Entries 316044
Mean -39.15
RMS 1.372
Underflow 0
Overflow 2.929e+04
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10^4
10^3
10^2
10
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150
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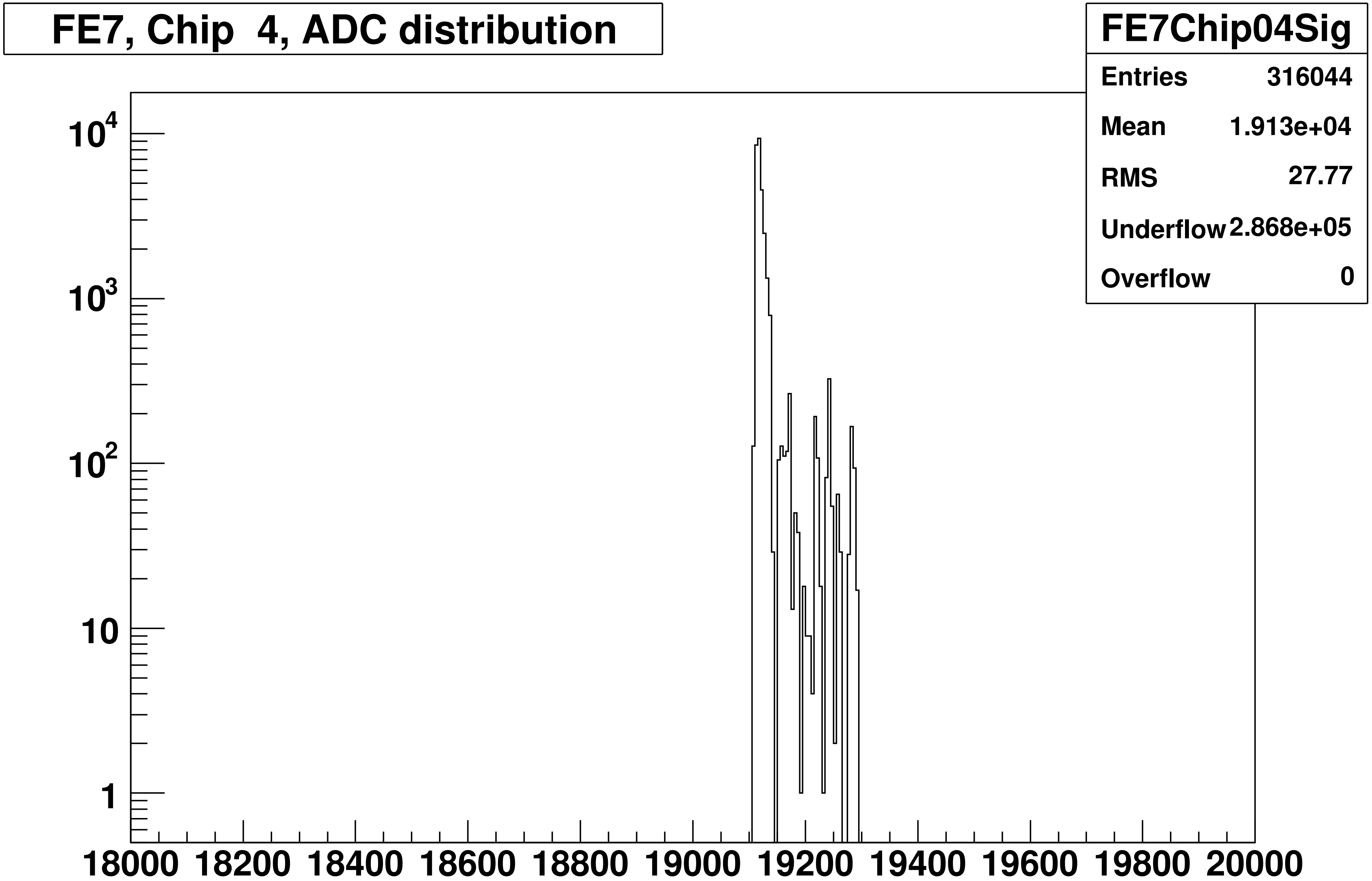
FE7, Chip 4, ADC distribution
FE7Chip04Sig
Entries 316044
Mean 1.913e+04
RMS 27.77
Underflow 2.868e+05
Overflow 0
10^4
10^3
10^2
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1
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19000
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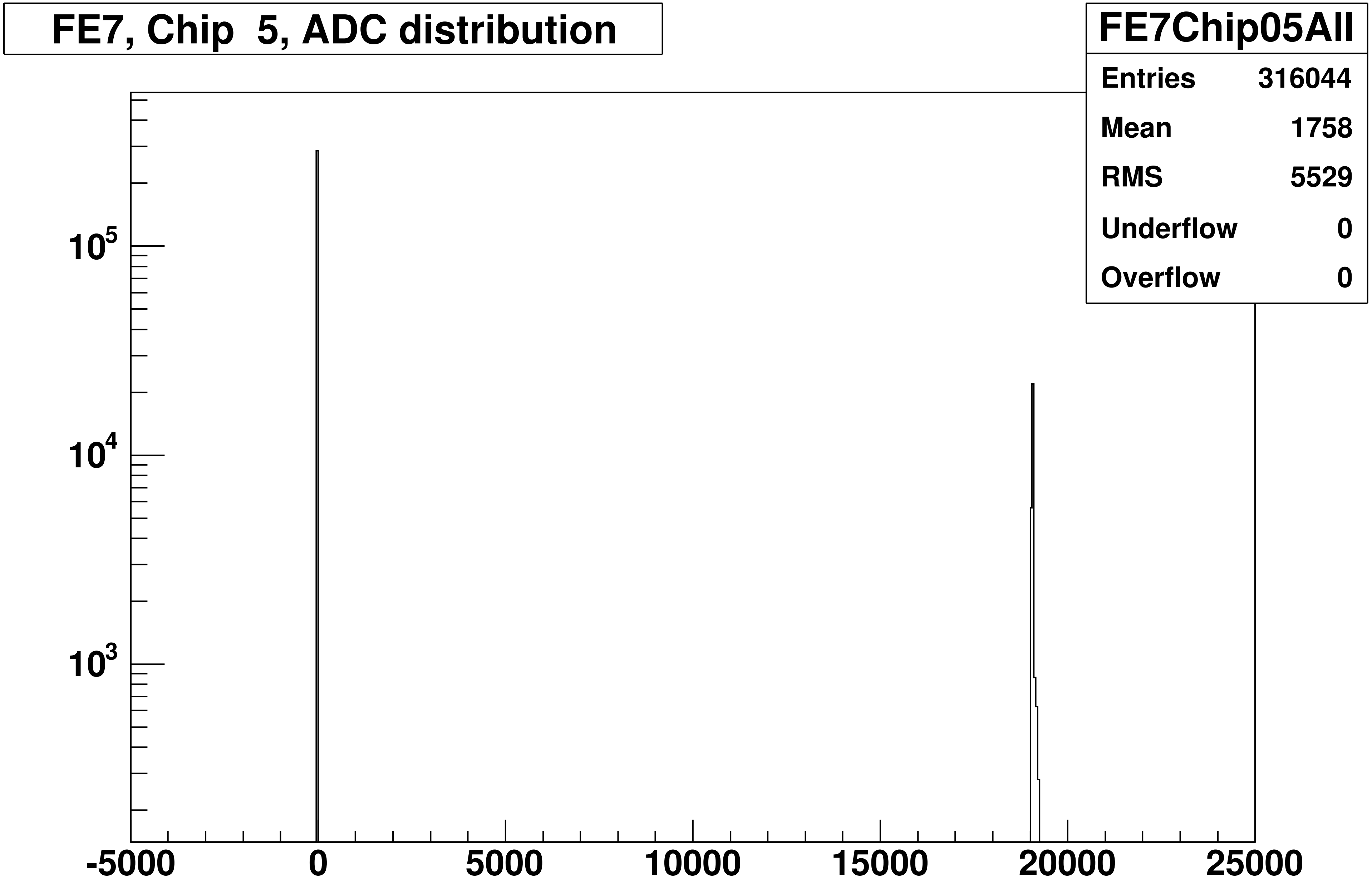
20000



FE7, Chip 5, ADC distribution
FE7Chip05All
Entries 316044
Mean 1758
RMS 5529
Underflow 0
Overflow 0
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10^4
10^3
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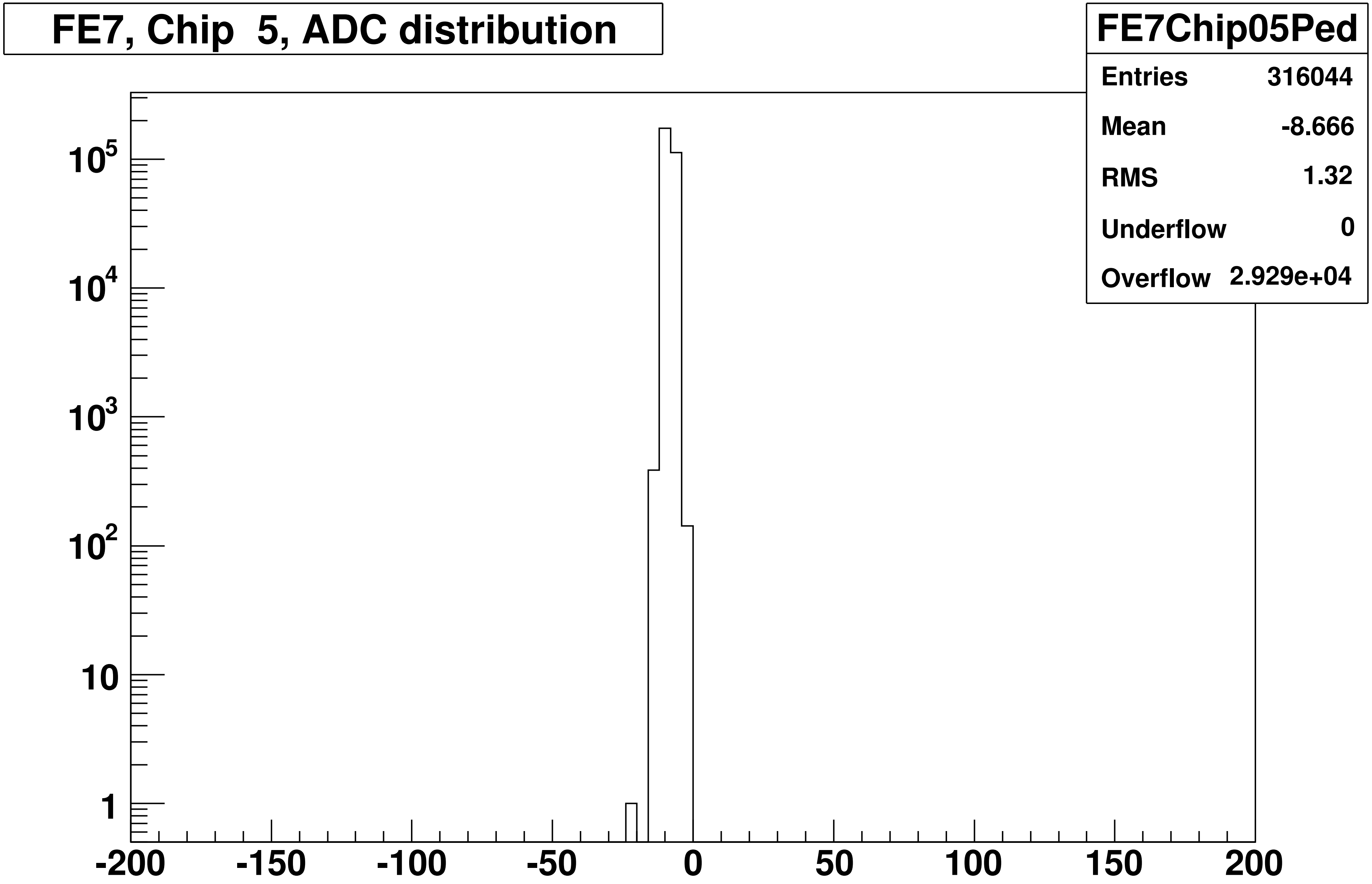
0
5000
10000
15000
20000
25000


FE7, Chip 5, ADC distribution
FE7Chip05Ped
Entries 316044
Mean -8.666
RMS 1.32
Underflow 0
Overflow 2.929e+04
10^5
10^4
10^3
10^2
10
1
-200
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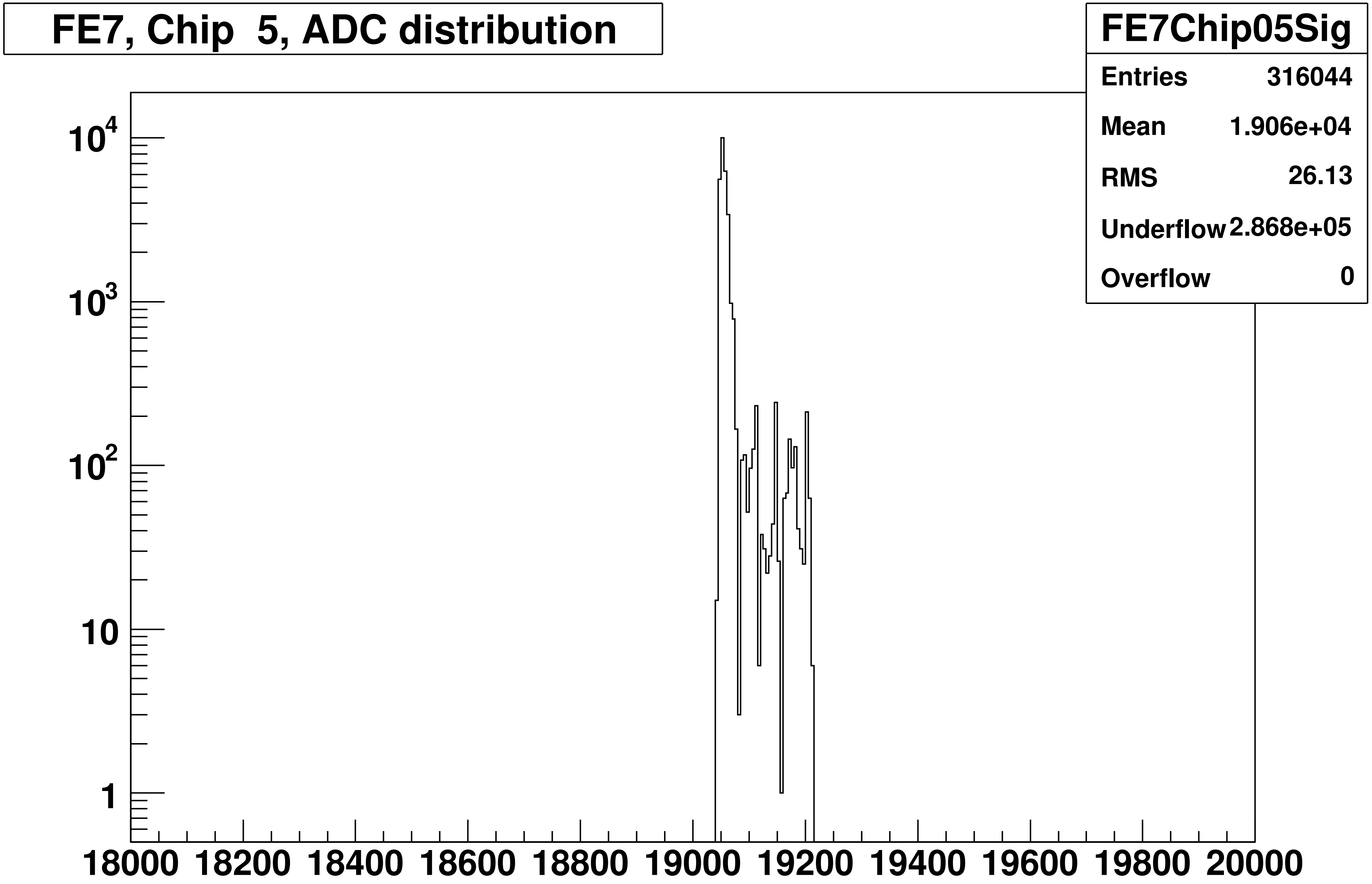
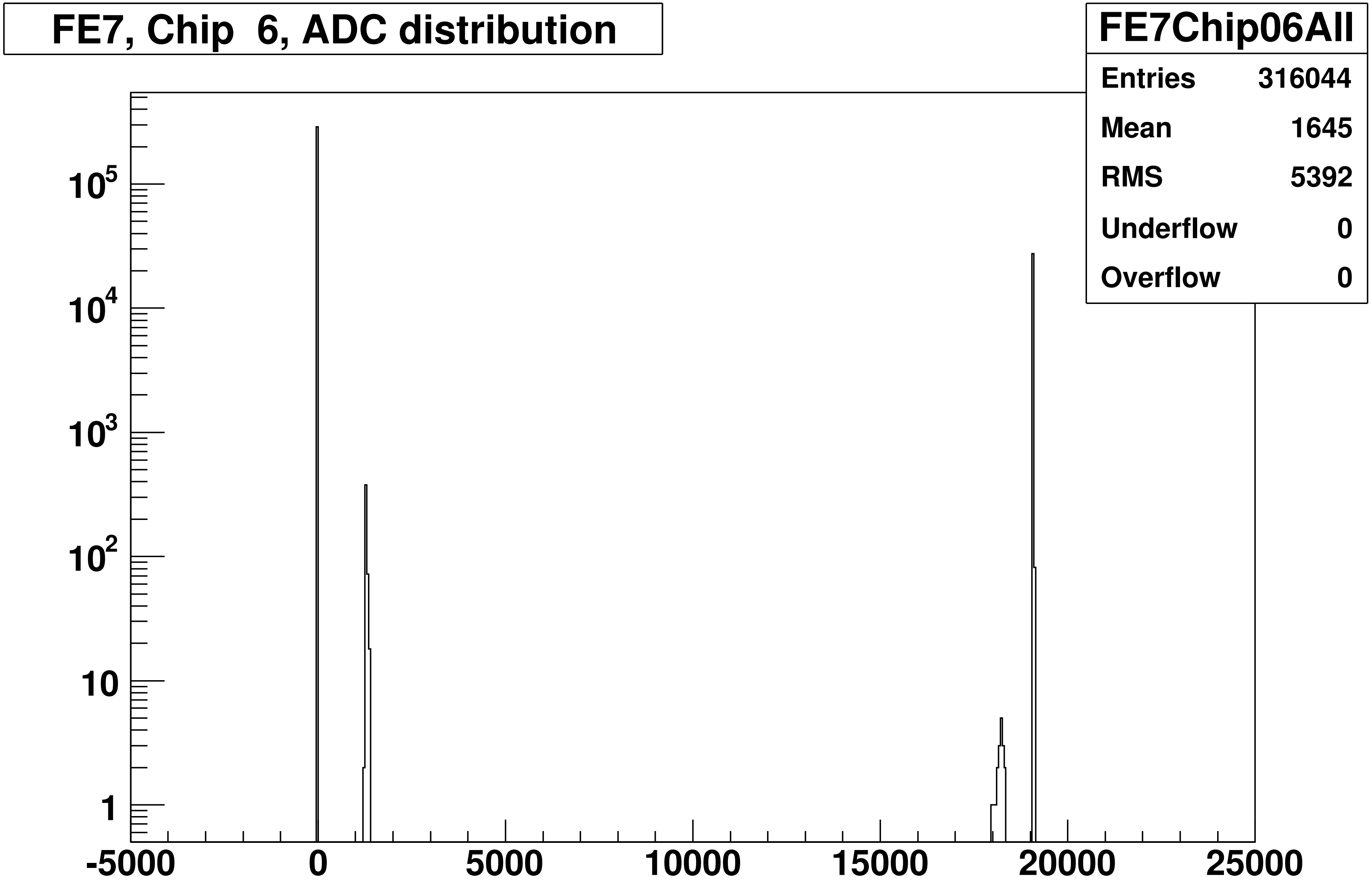
50
100
150
200


FE7, Chip 5, ADC distribution
FE7Chip05Sig
Entries 316044
Mean 1.906e+04
RMS 26.13
Underflow 2.868e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE7, Chip 6, ADC distribution
FE7Chip06All
Entries 316044
Mean 1645
RMS 5392
Underflow 0
Overflow 0
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10^4
10^3
10^2
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0
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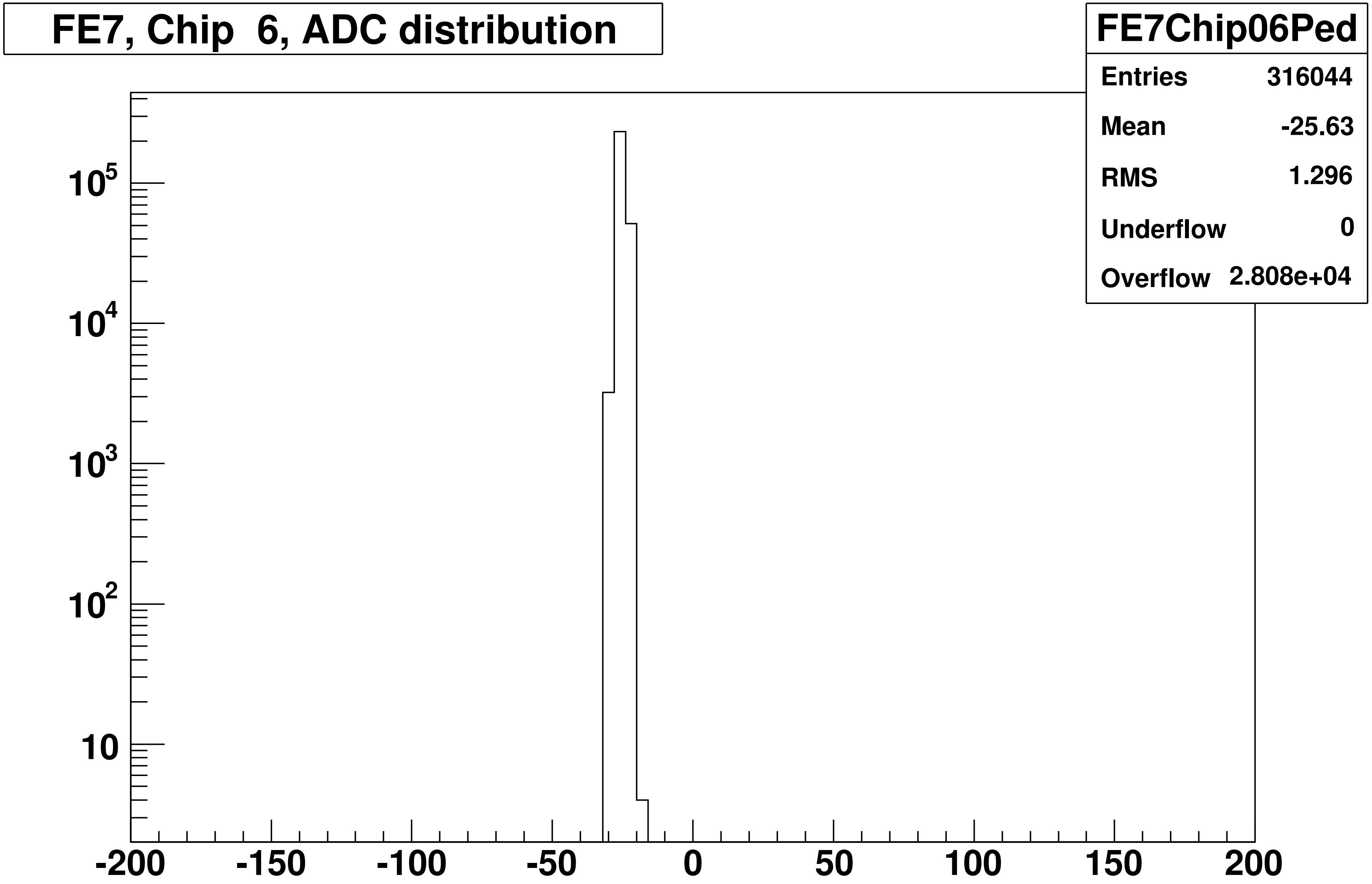
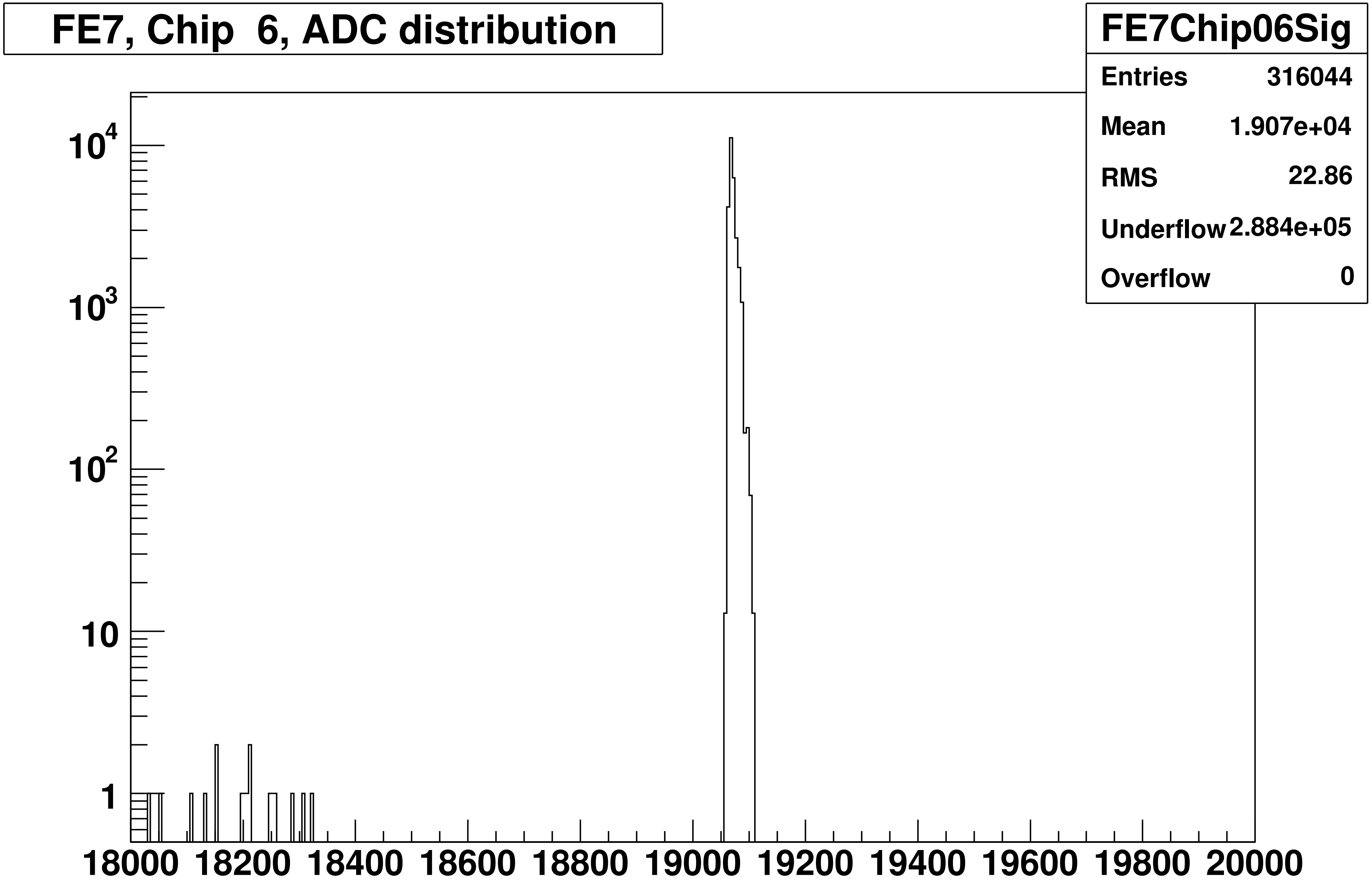
10000
15000
20000
25000


FE7, Chip 6, ADC distribution
FE7Chip06Ped
Entries 316044
Mean -25.63
RMS 1.296
Underflow 0
Overflow 2.808e+04
10
10^2
10^3
10^4
10^5
-200
-150
-100
-50
0
50
100
150
200


FE7, Chip 6, ADC distribution
FE7Chip06Sig
Entries 316044
Mean 1.907e+04
RMS 22.86
Underflow 2.884e+05
Overflow 0
10^4
10^3
10^2
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1
18000
18200
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18600
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19000
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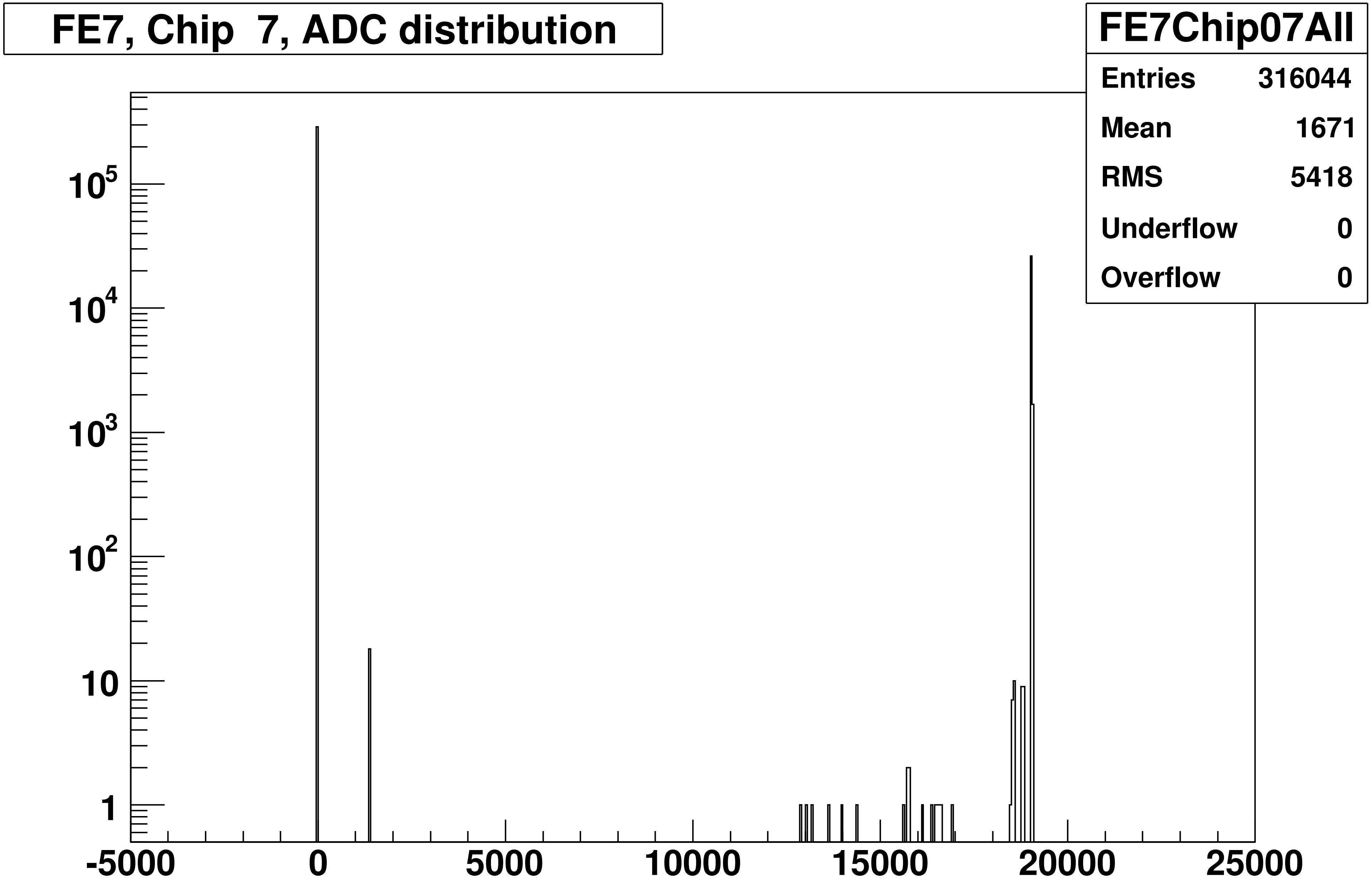
19600
19800
20000


FE7, Chip 7, ADC distribution
FE7Chip07All
Entries 316044
Mean 1671
RMS 5418
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
1
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0
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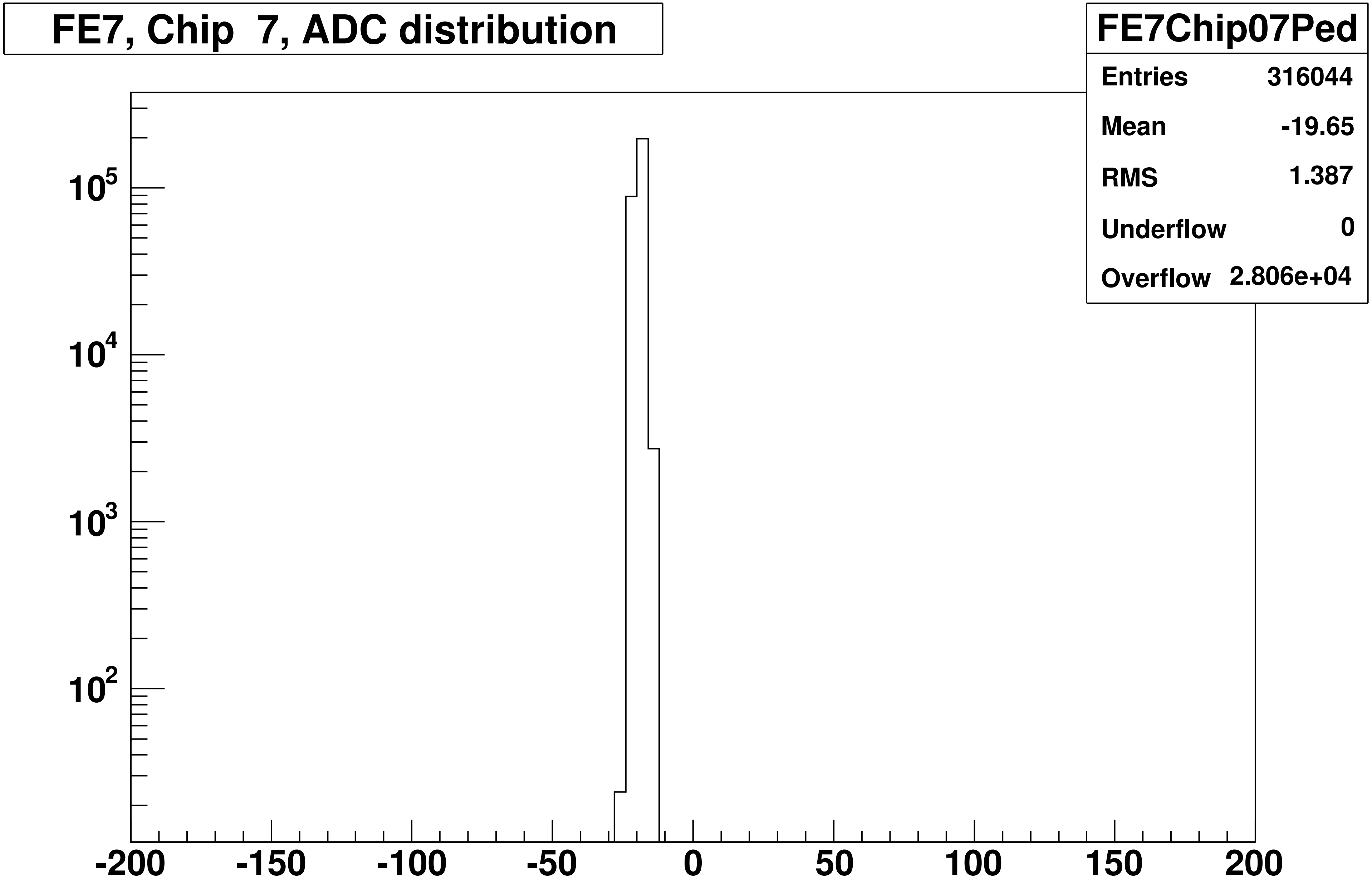
25000



FE7, Chip 7, ADC distribution
FE7Chip07Ped
Entries 316044
Mean -19.65
RMS 1.387
Underflow 0
Overflow 2.806e+04
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10^4
10^3
10^2
-200
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-100
-50
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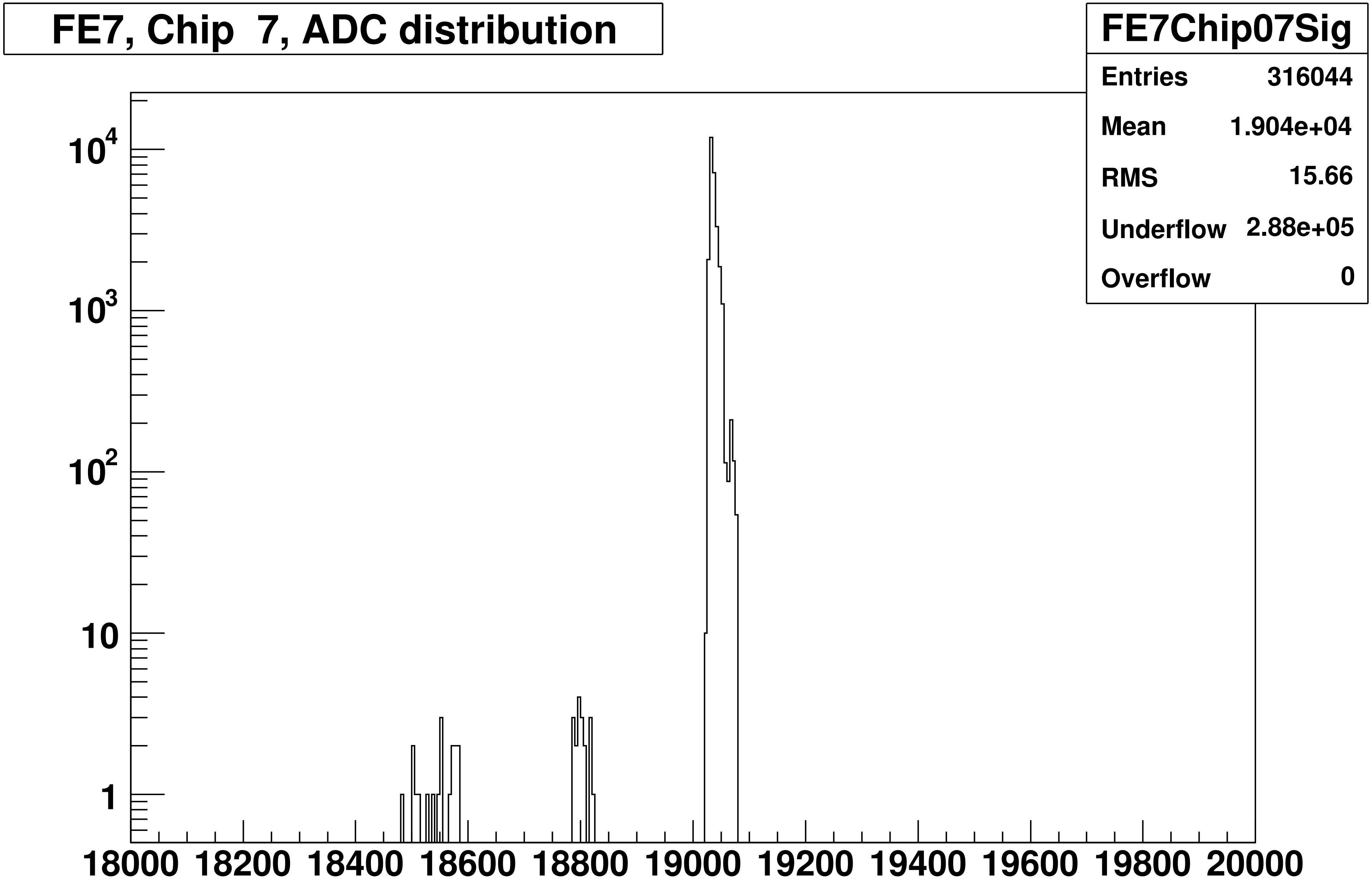
50
100
150
200


FE7, Chip 7, ADC distribution
FE7Chip07Sig
Entries 316044
Mean 1.904e+04
RMS 15.66
Underflow 2.88e+05
Overflow 0
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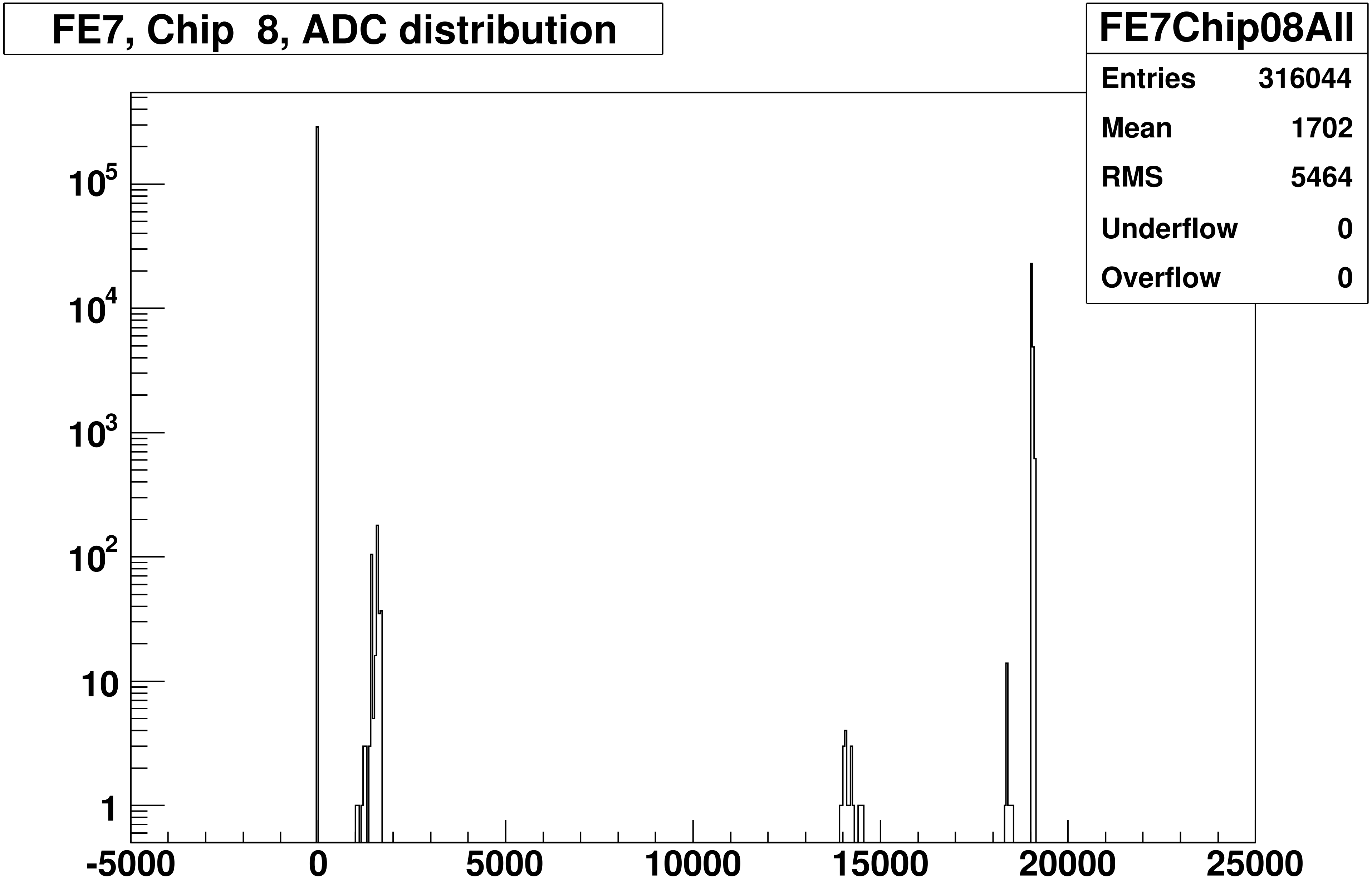
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE7, Chip 8, ADC distribution
FE7Chip08All
Entries 316044
Mean 1702
RMS 5464
Underflow 0
Overflow 0
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10^3
10^2
10
1
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5000
10000
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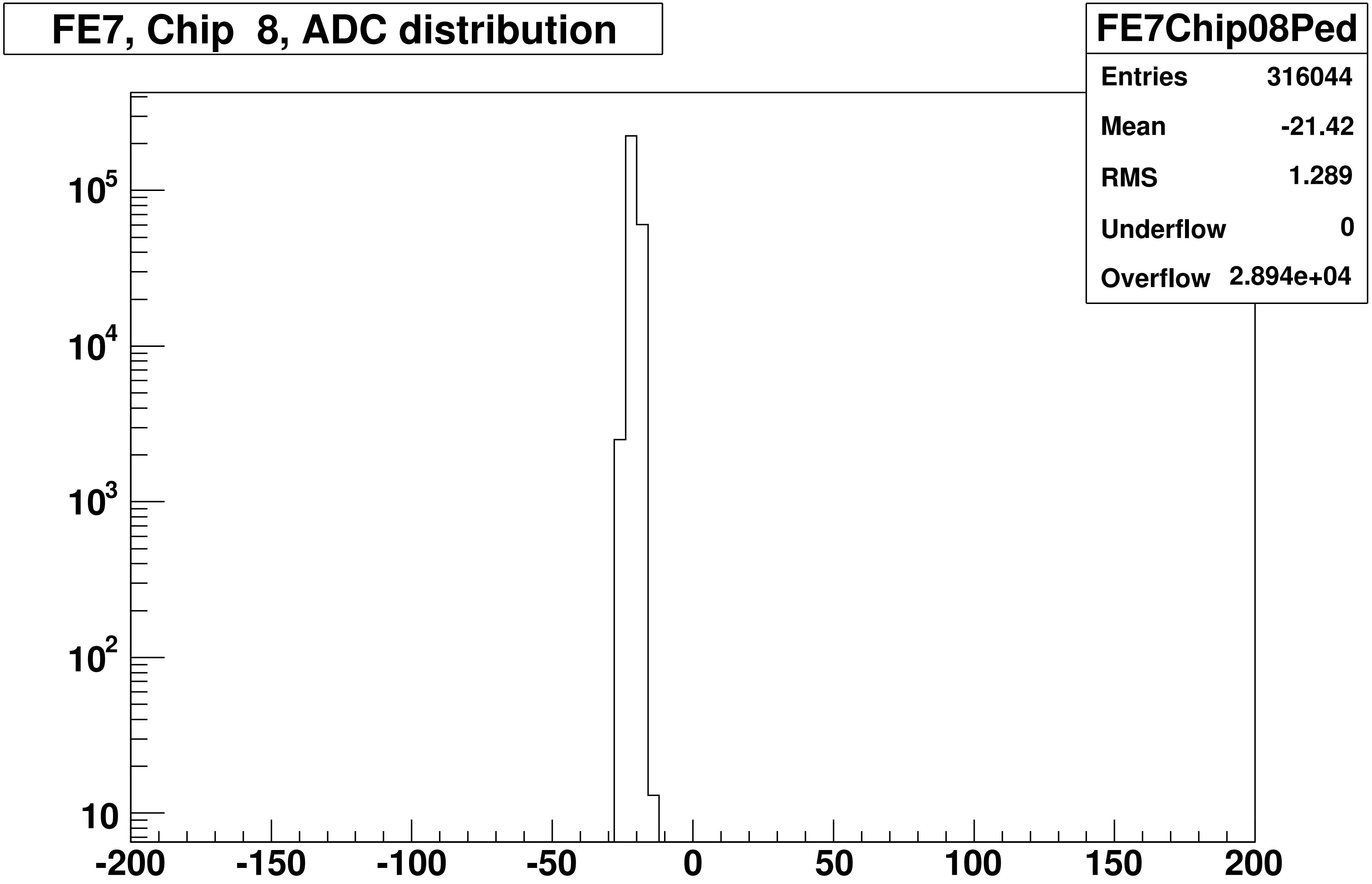
20000
25000



FE7, Chip 8, ADC distribution
FE7Chip08Ped
Entries 316044
Mean -21.42
RMS 1.289
Underflow 0
Overflow 2.894e+04
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10^4
10^3
10^2
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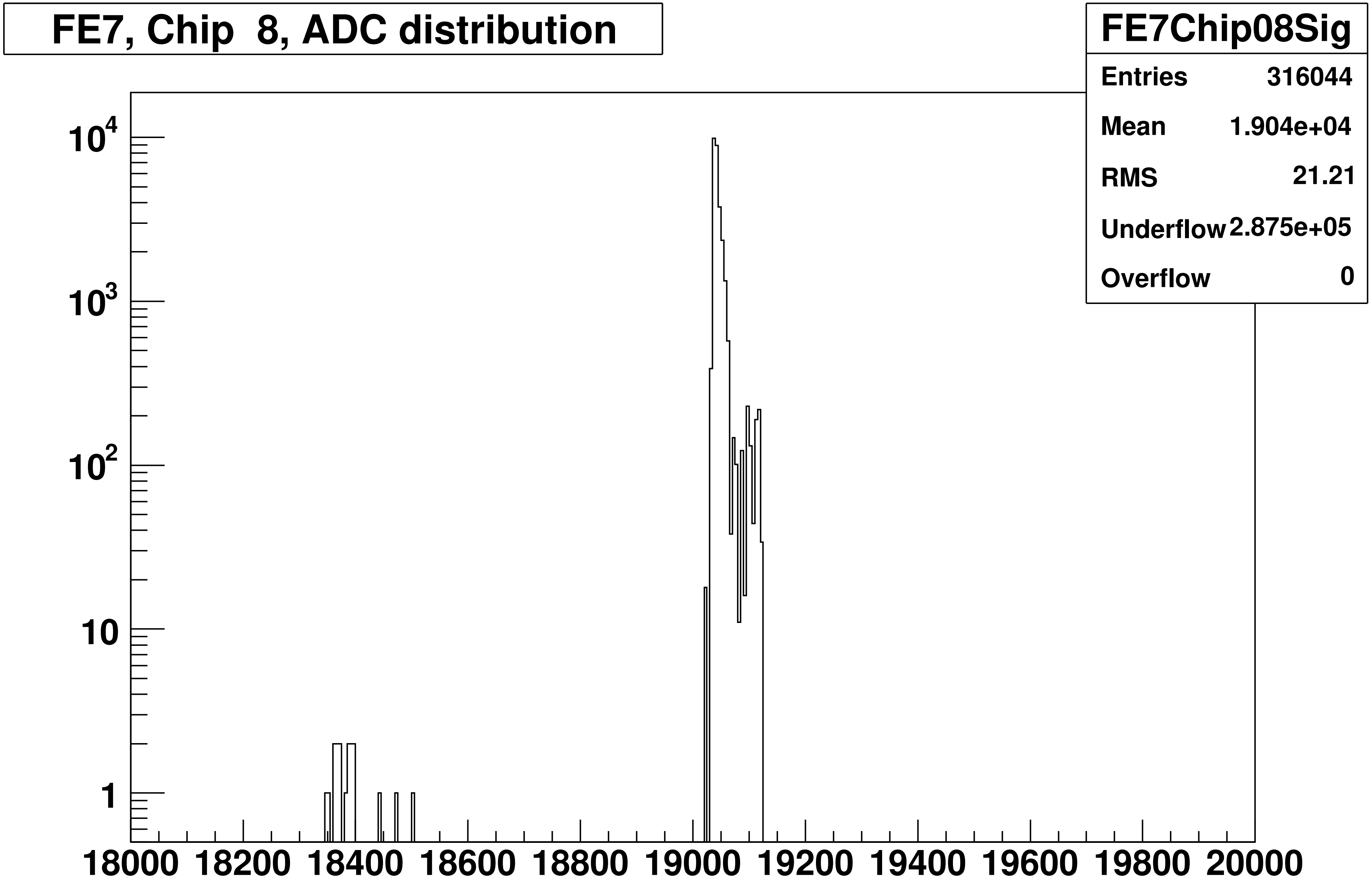
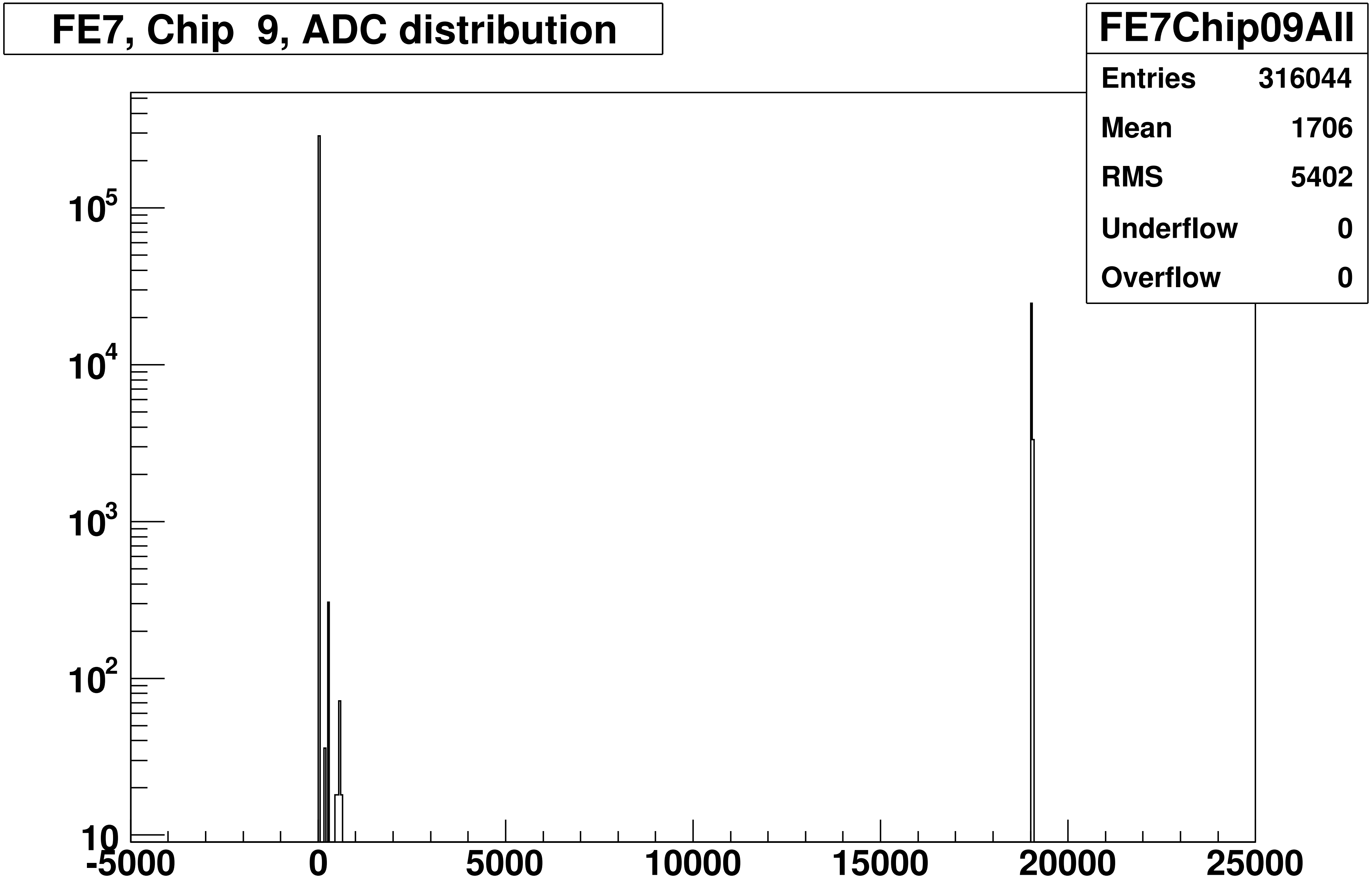
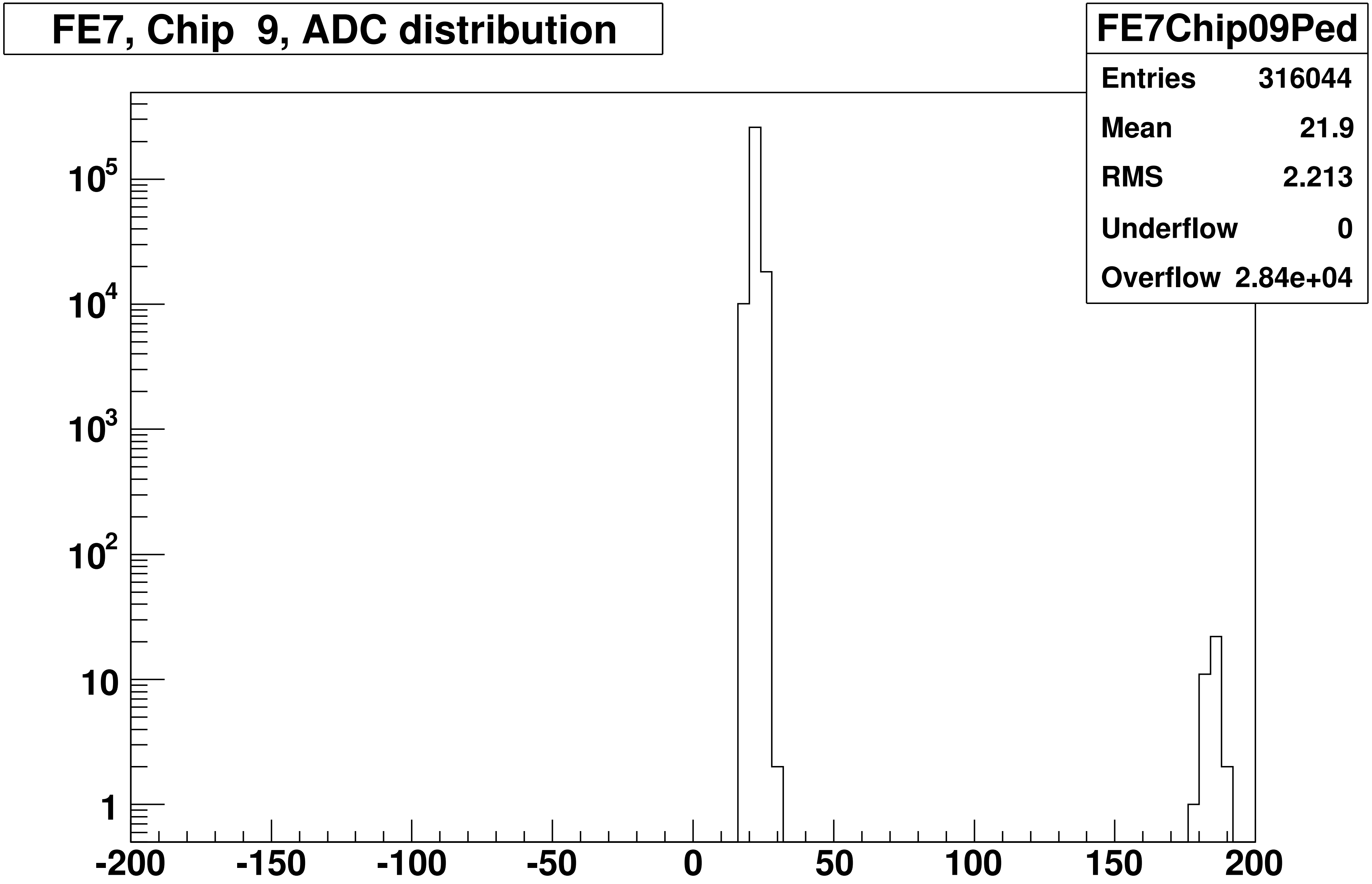
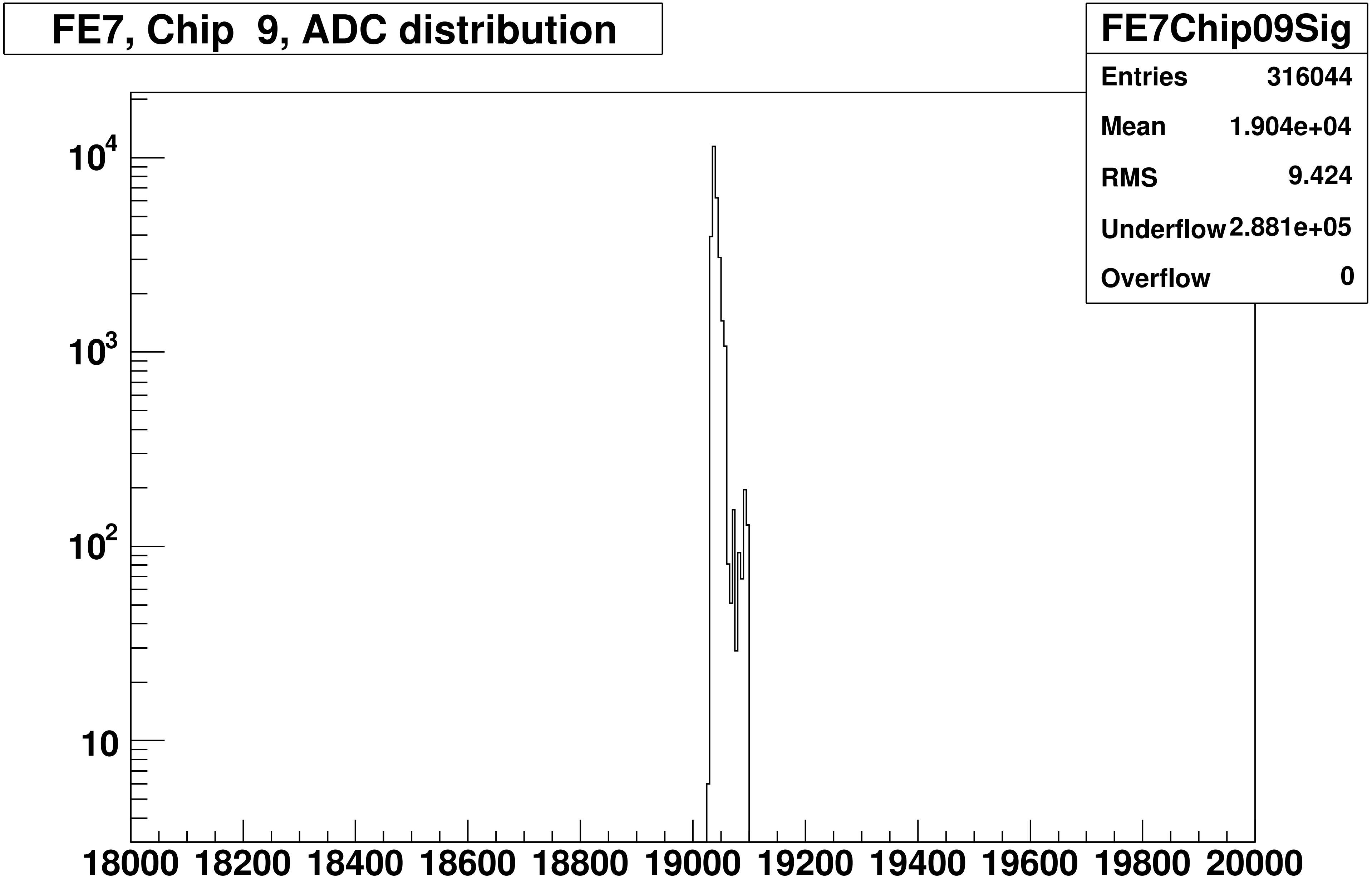
150
200

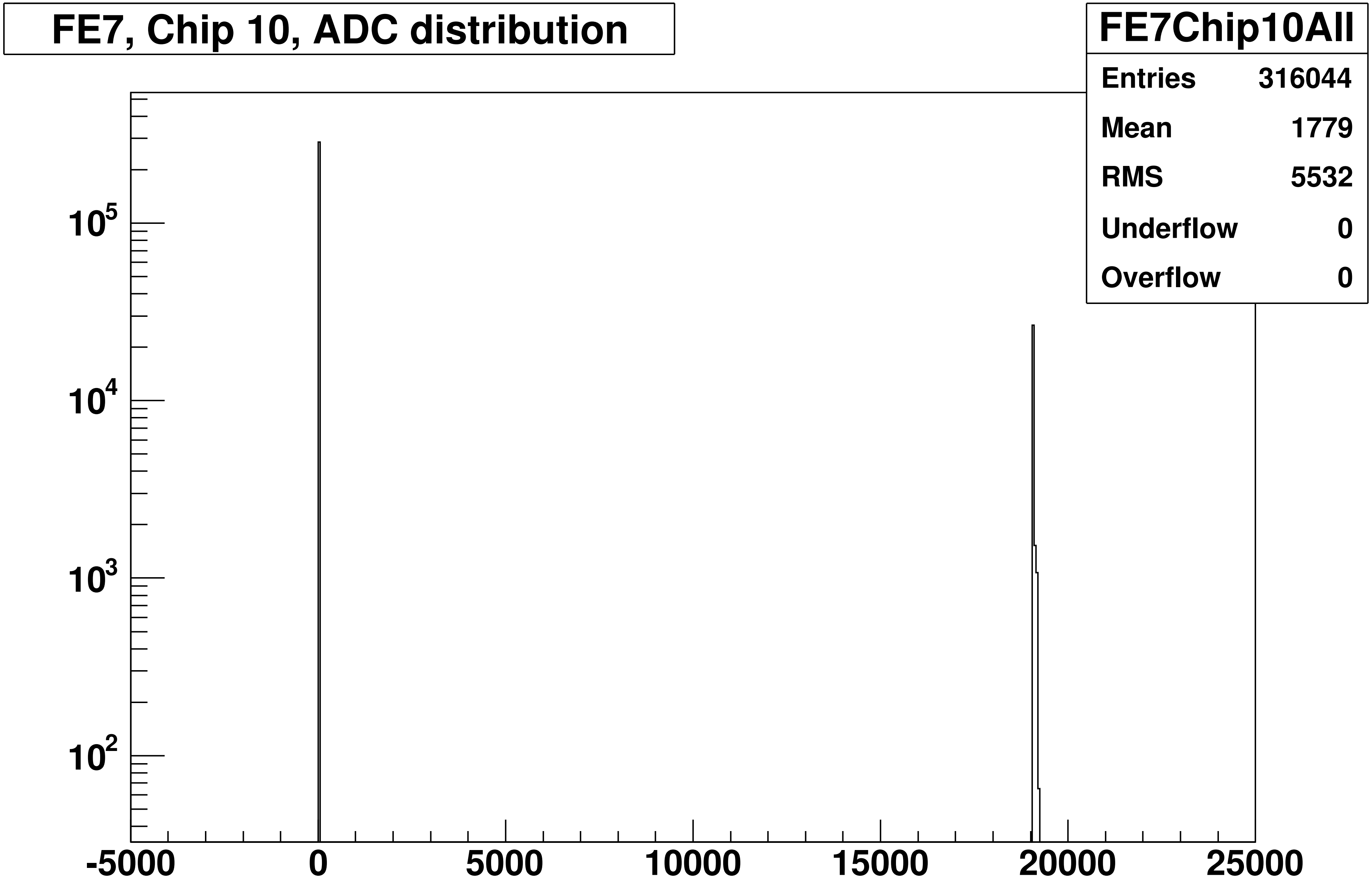

FE7, Chip 8, ADC distribution
FE7Chip08Sig
Entries 316044
Mean 1.904e+04
RMS 21.21
Underflow 2.875e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000

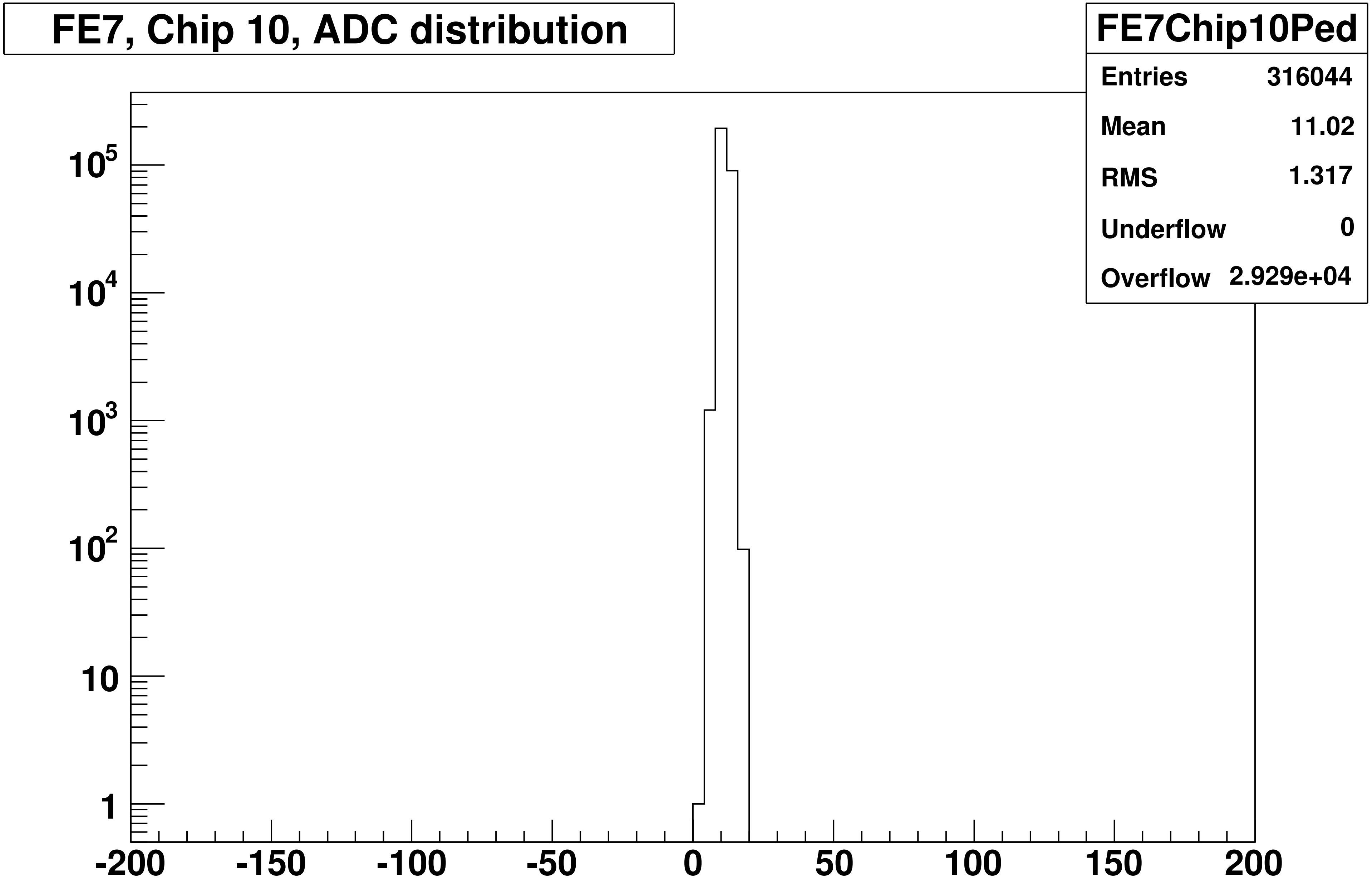

FE7, Chip 9, ADC distribution
FE7Chip09All
Entries 316044
Mean 1706
RMS 5402
Underflow 0
Overflow 0
10
10^2
10^3
10^4
10^5
-5000
0
5000
10000
15000
20000
25000

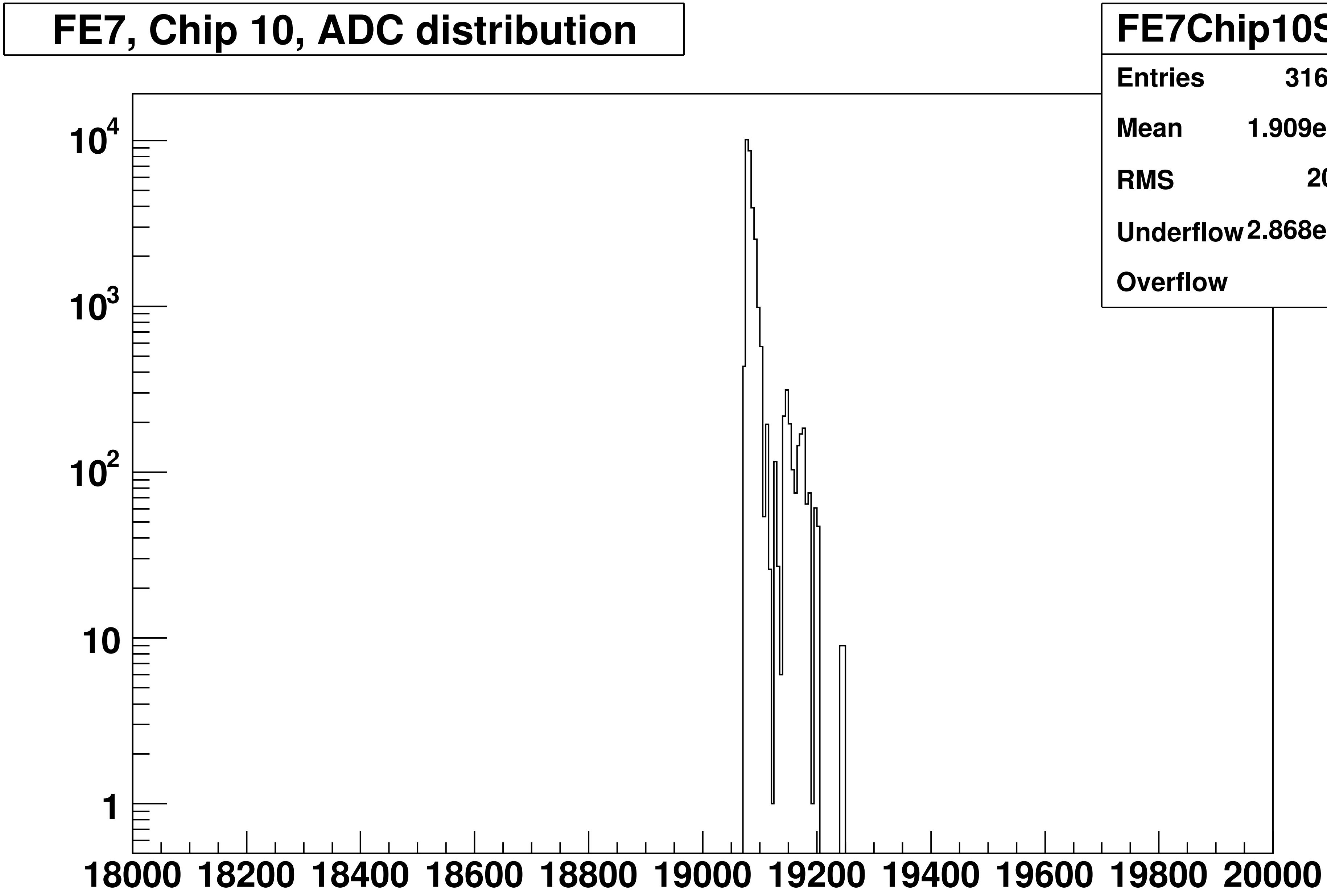


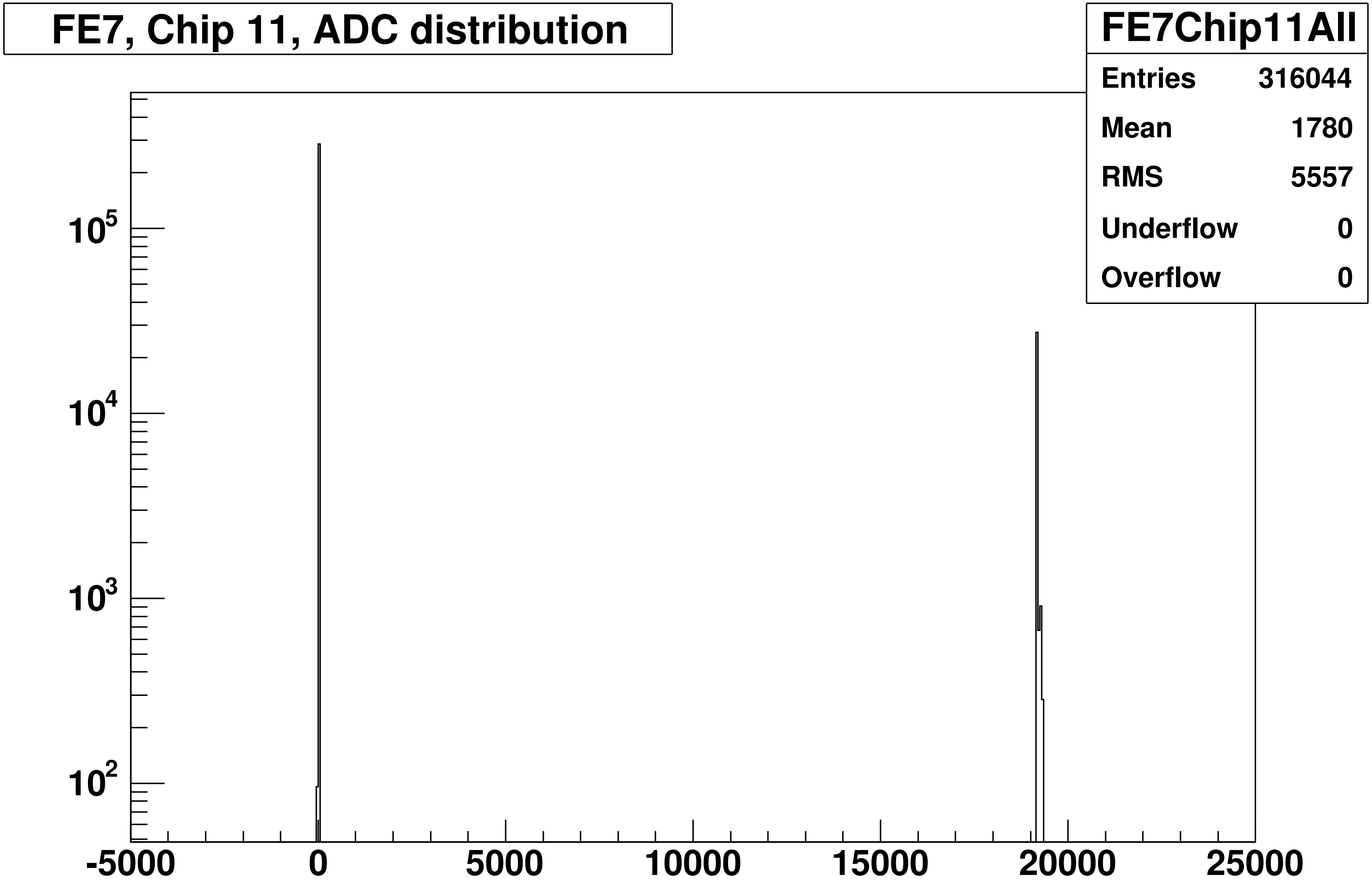
FE7, Chip 9, ADC distribution
FE7Chip09Ped
Entries 316044
Mean 21.9
RMS 2.213
Underflow 0
Overflow 2.84e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
200

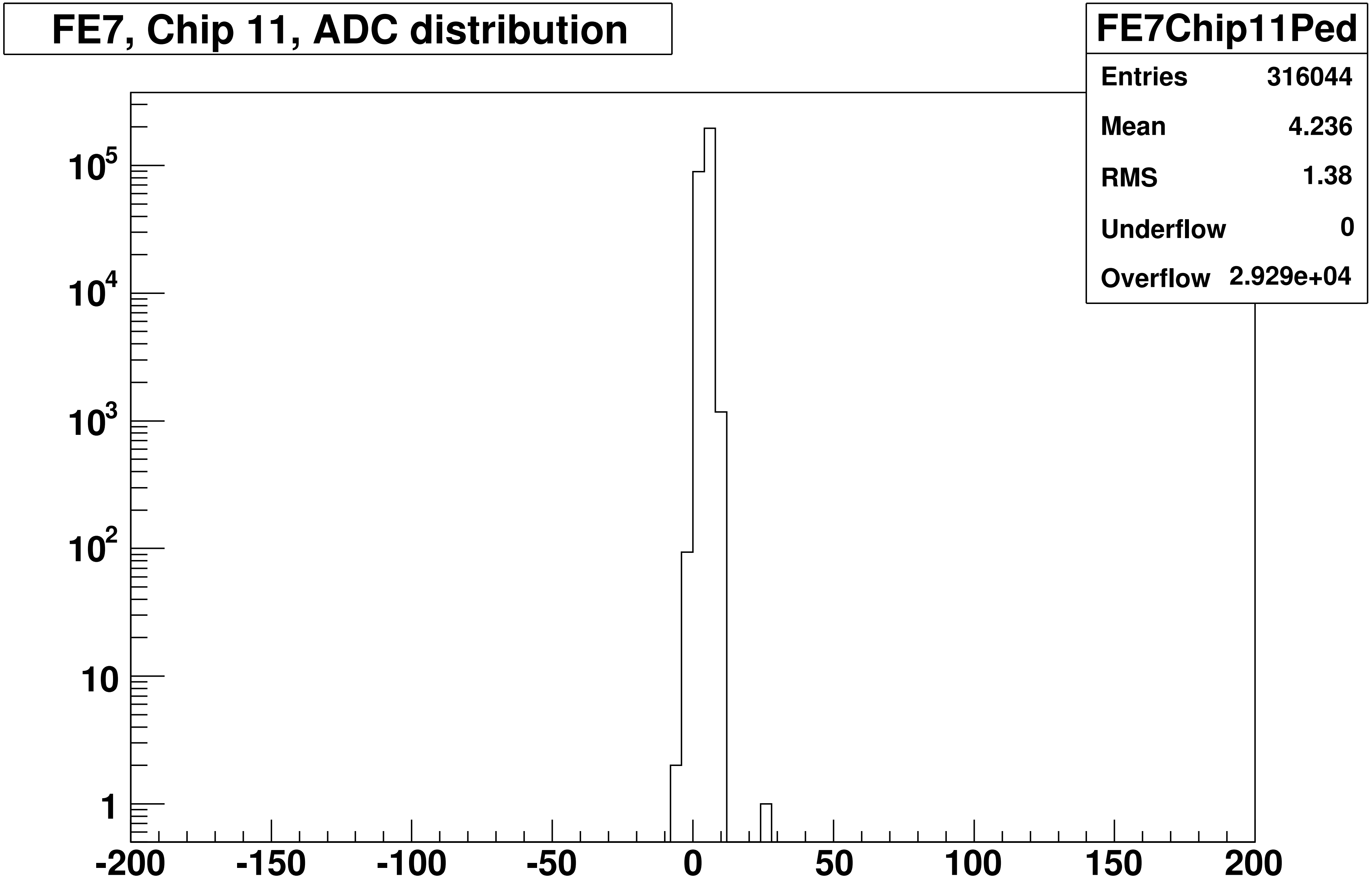

FE7, Chip 9, ADC distribution
FE7Chip09Sig
Entries 316044
Mean 1.904e+04
RMS 9.424
Underflow 2.881e+05
Overflow 0
10^4
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000

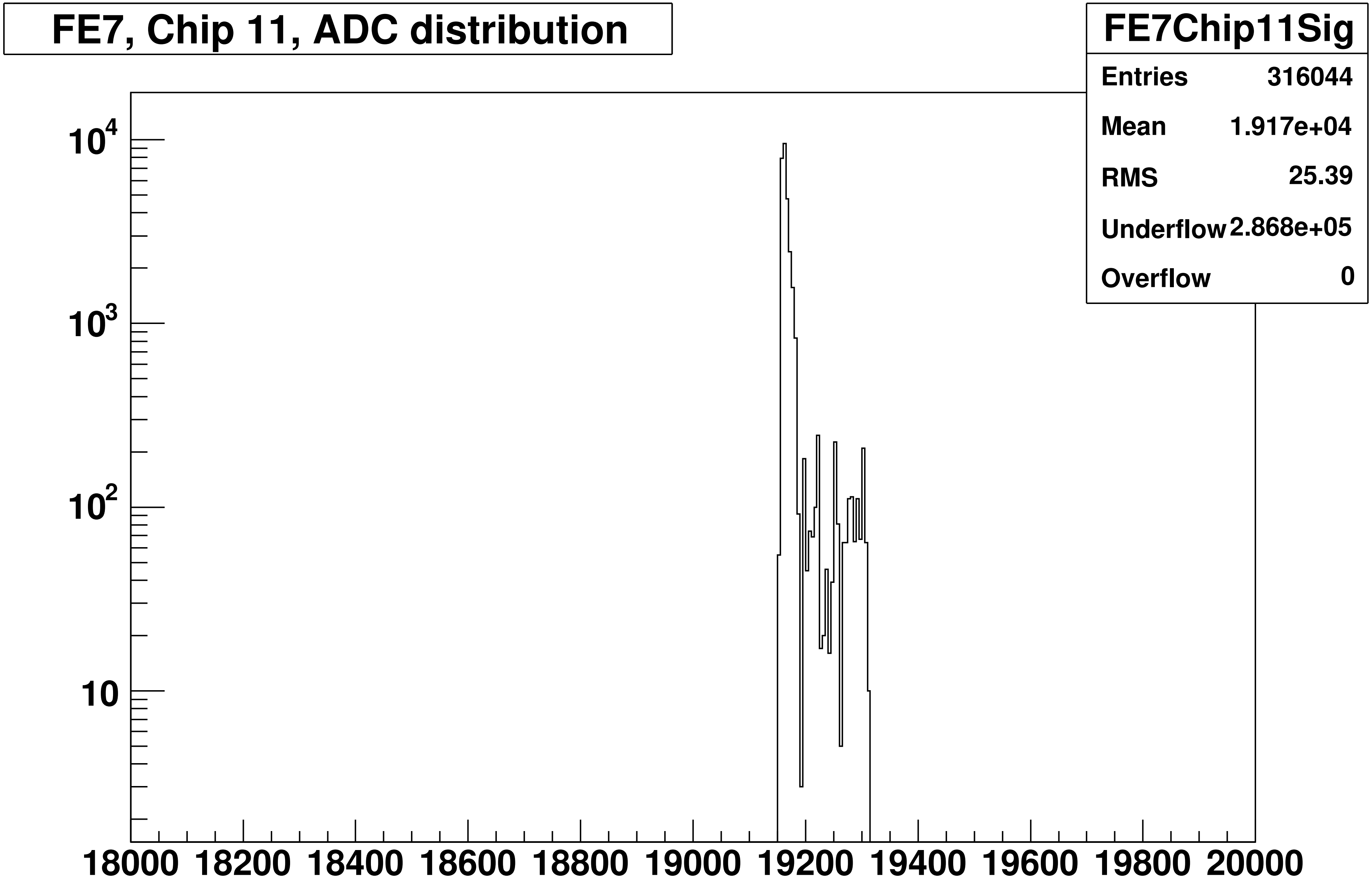

FE7, Chip 10, ADC distribution
FE7Chip10All
Entries 316044
Mean 1779
RMS 5532
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000


FE7, Chip 10, ADC distribution
FE7Chip10Ped
Entries 316044
Mean 11.02
RMS 1.317
Underflow 0
Overflow 2.929e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
200

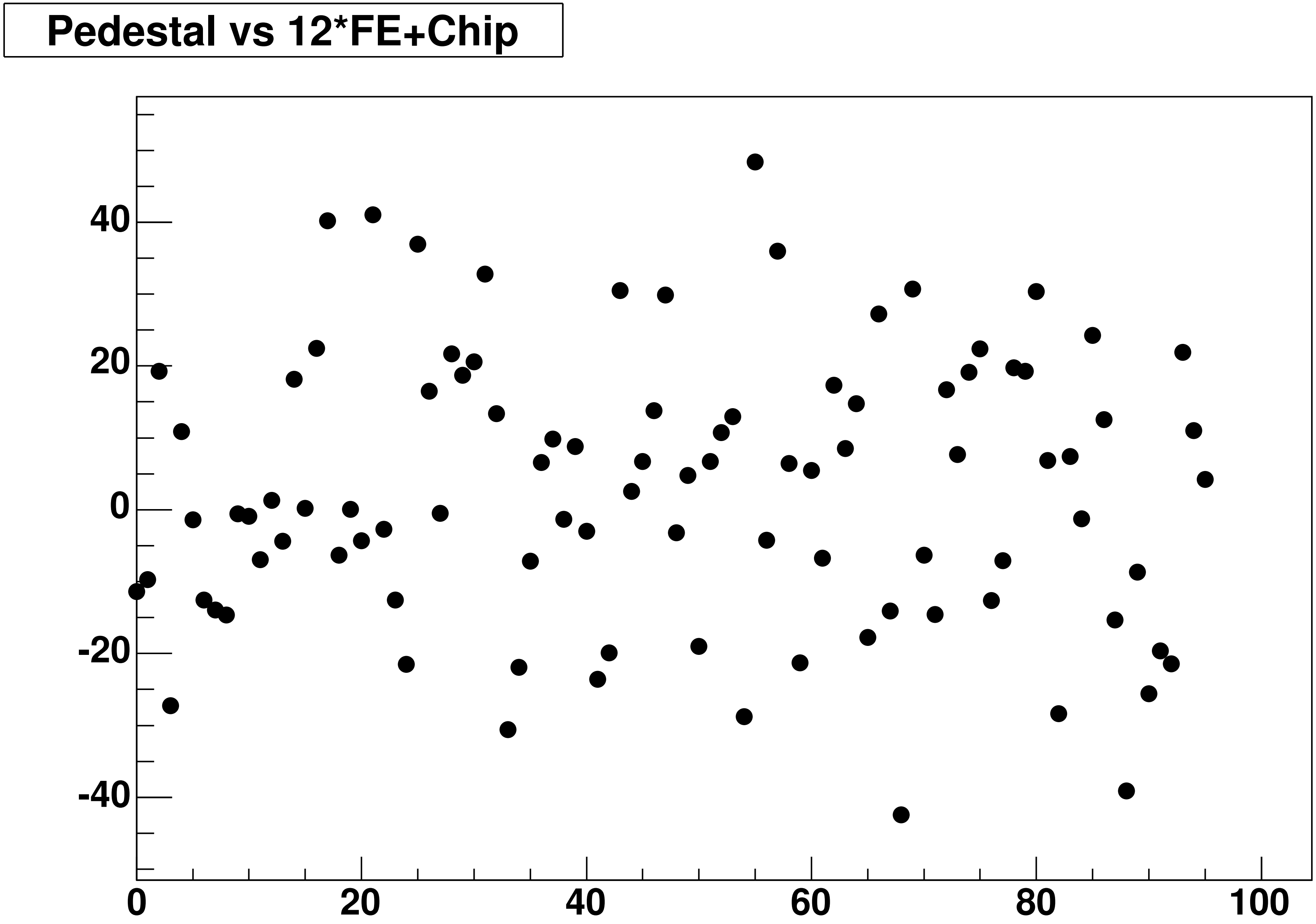

FE7, Chip 10, ADC distribution
FE7Chip10Sig
Entries 316044
Mean 1.909e+04
RMS 20.47
Underflow 2.868e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000

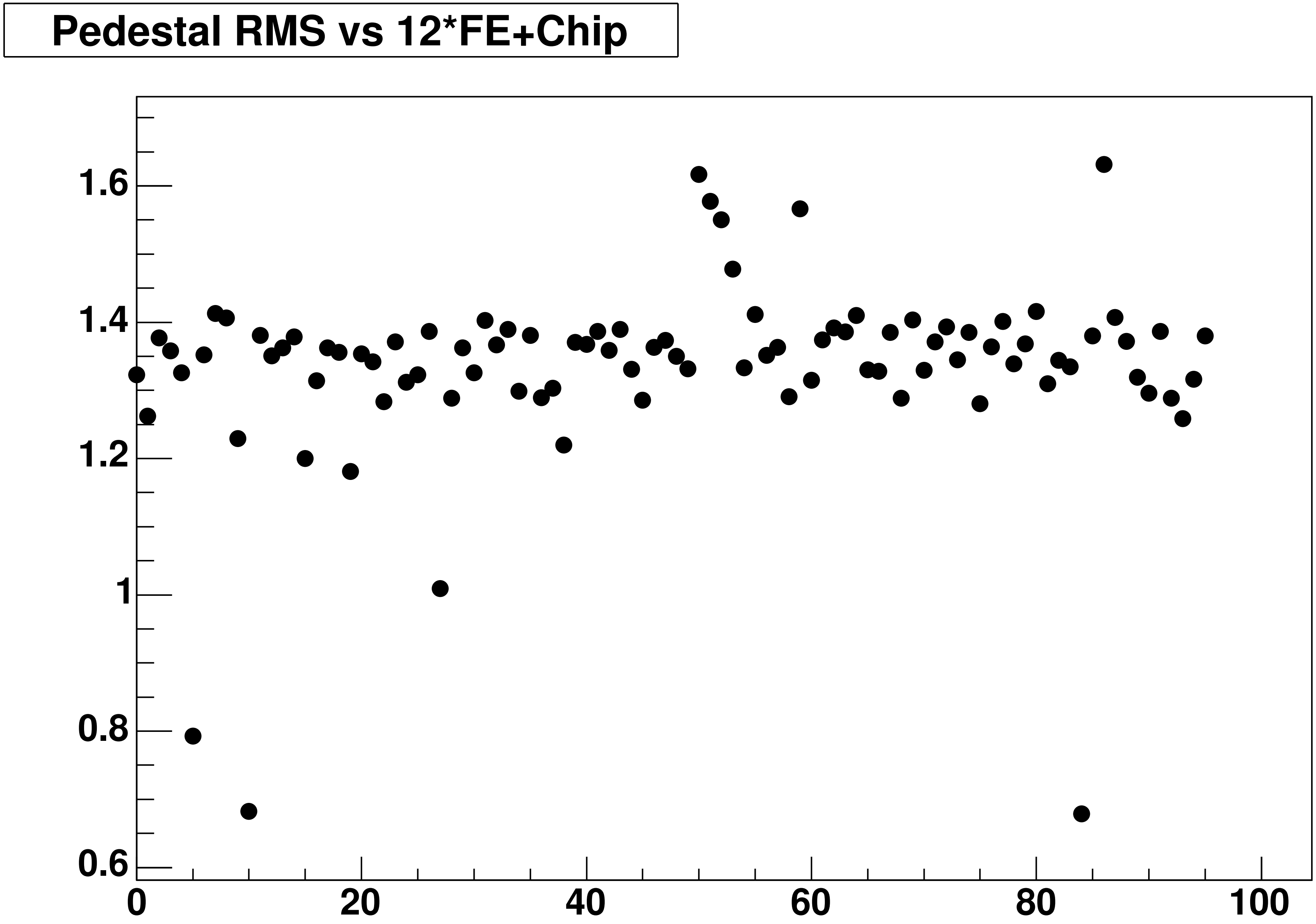

FE7, Chip 11, ADC distribution
FE7Chip11All
Entries 316044
Mean 1780
RMS 5557
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000

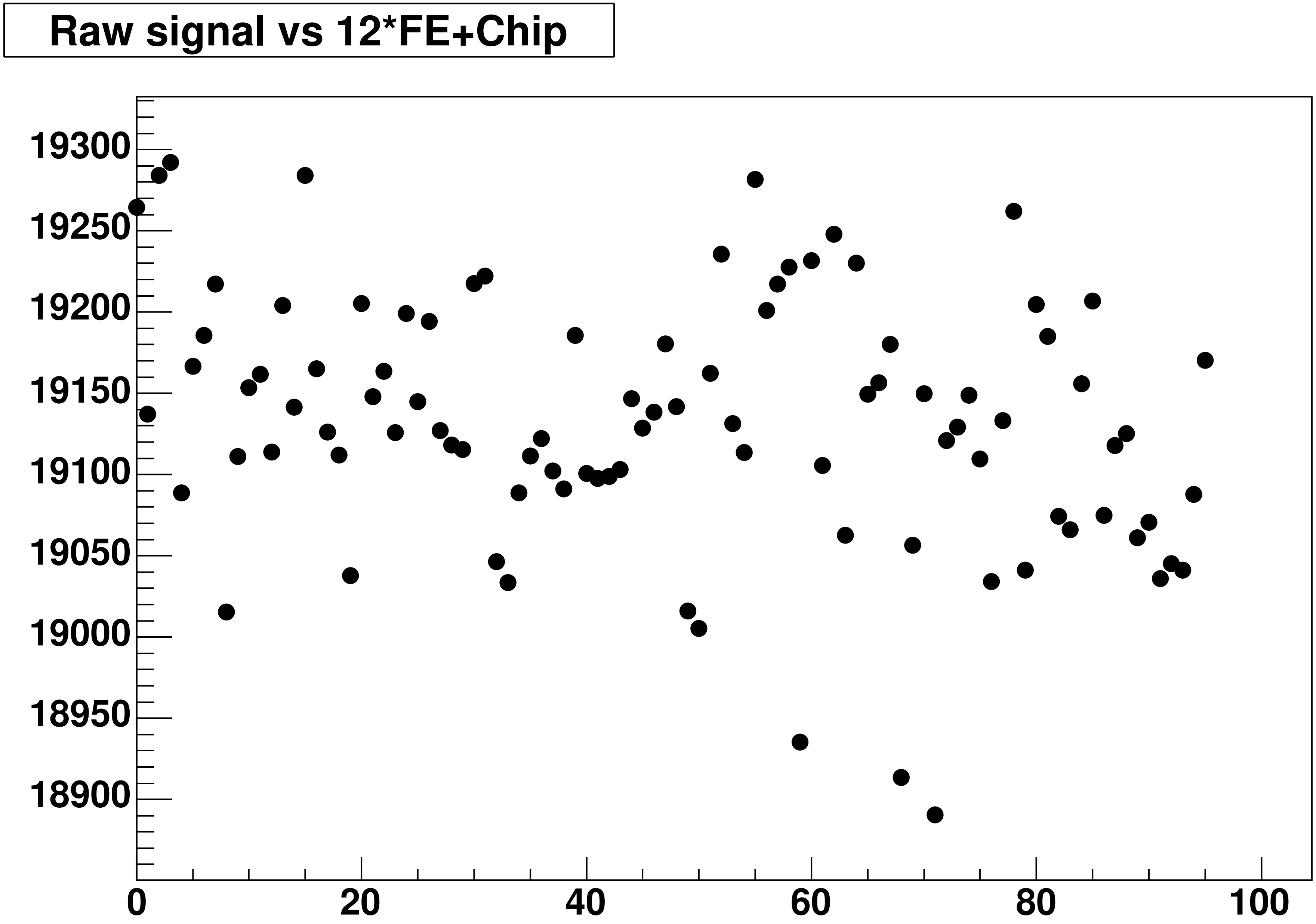

FE7, Chip 11, ADC distribution
FE7Chip11Ped
Entries 316044
Mean 4.236
RMS 1.38
Underflow 0
Overflow 2.929e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
200

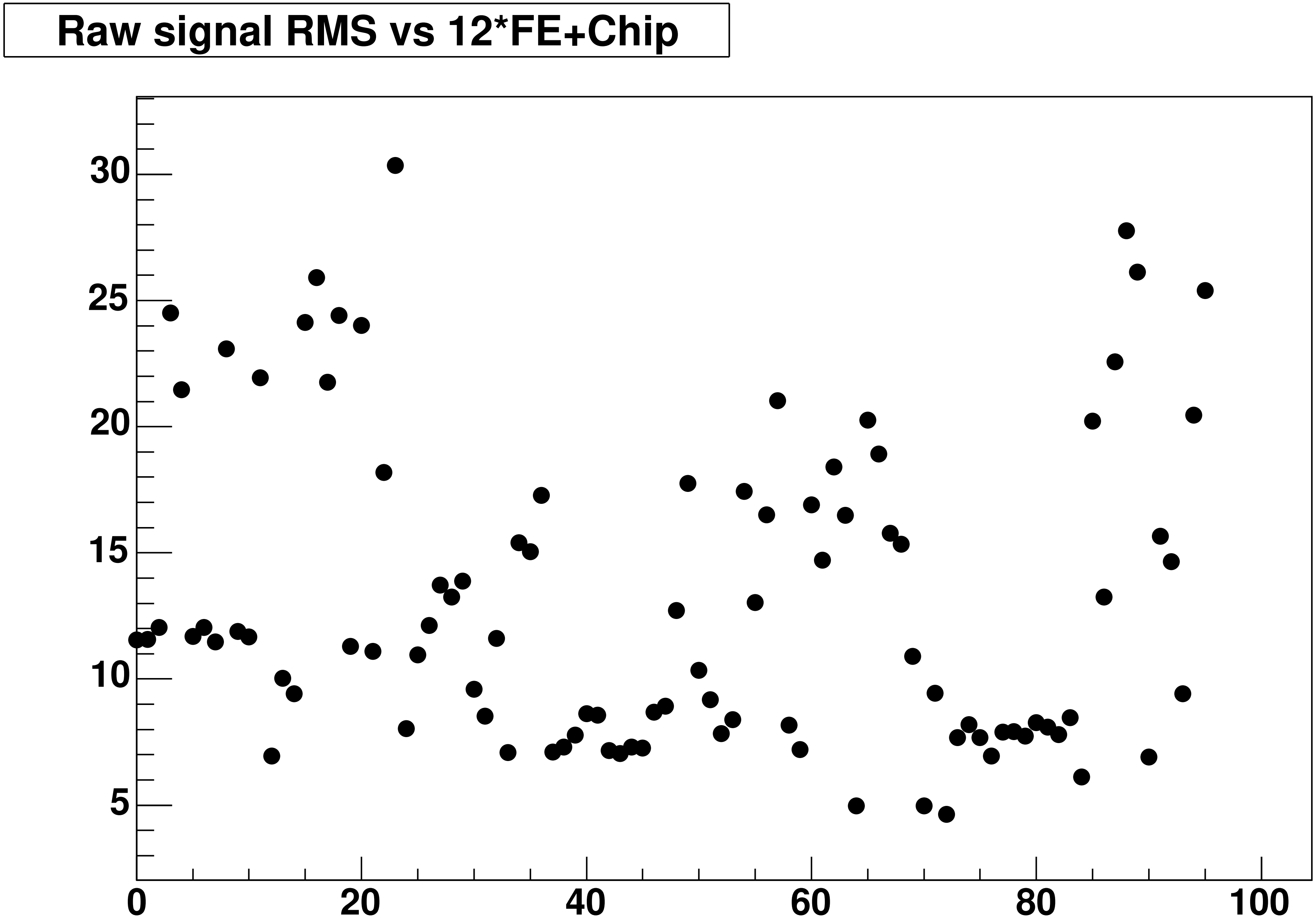


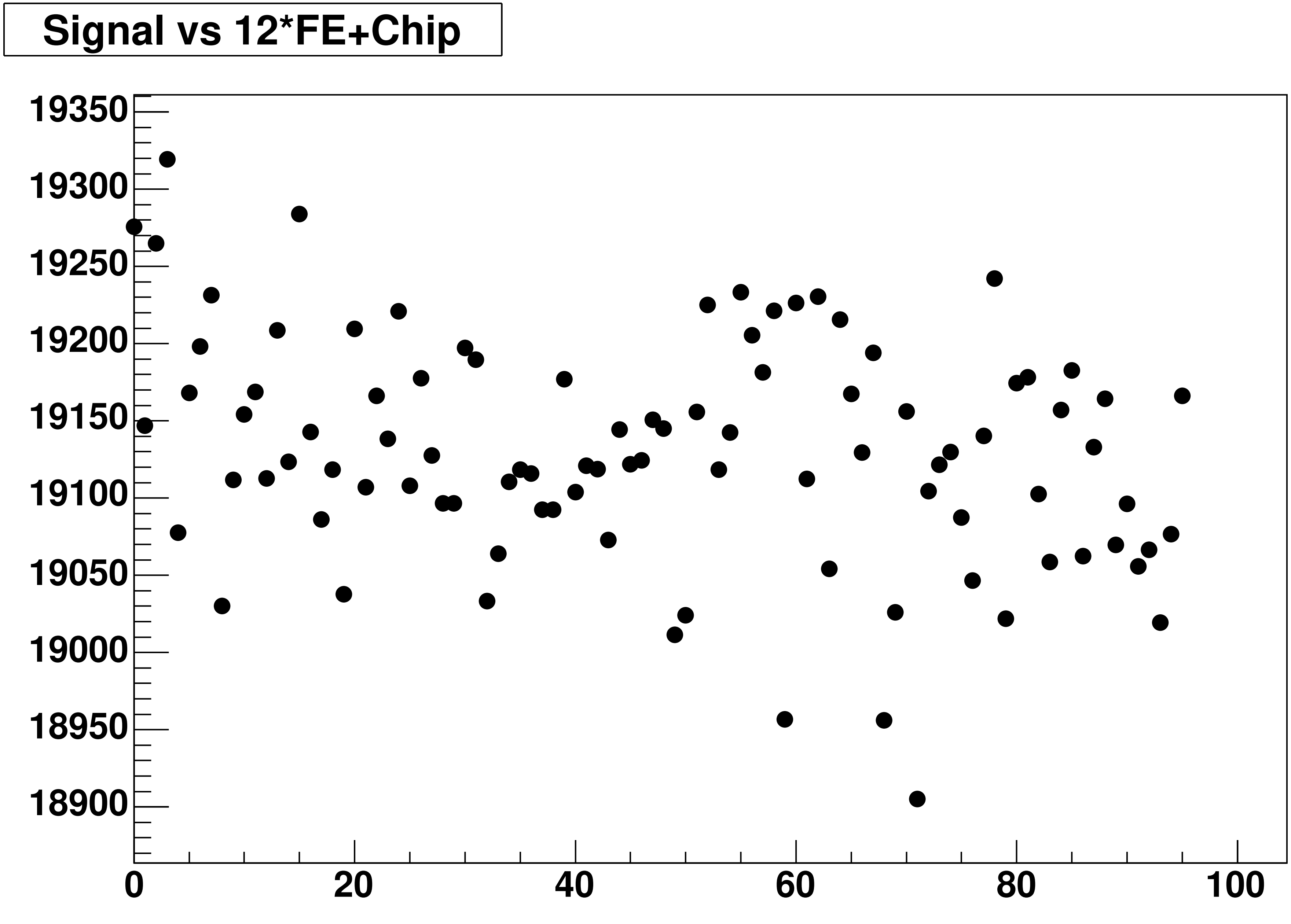
FE7, Chip 11, ADC distribution
FE7Chip11Sig
Entries 316044
Mean 1.917e+04
RMS 25.39
Underflow 2.868e+05
Overflow 0
10^4
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


Pedestal vs 12*FE+Chip
40
20
0
-20
-40
0
20
40
60
80
100

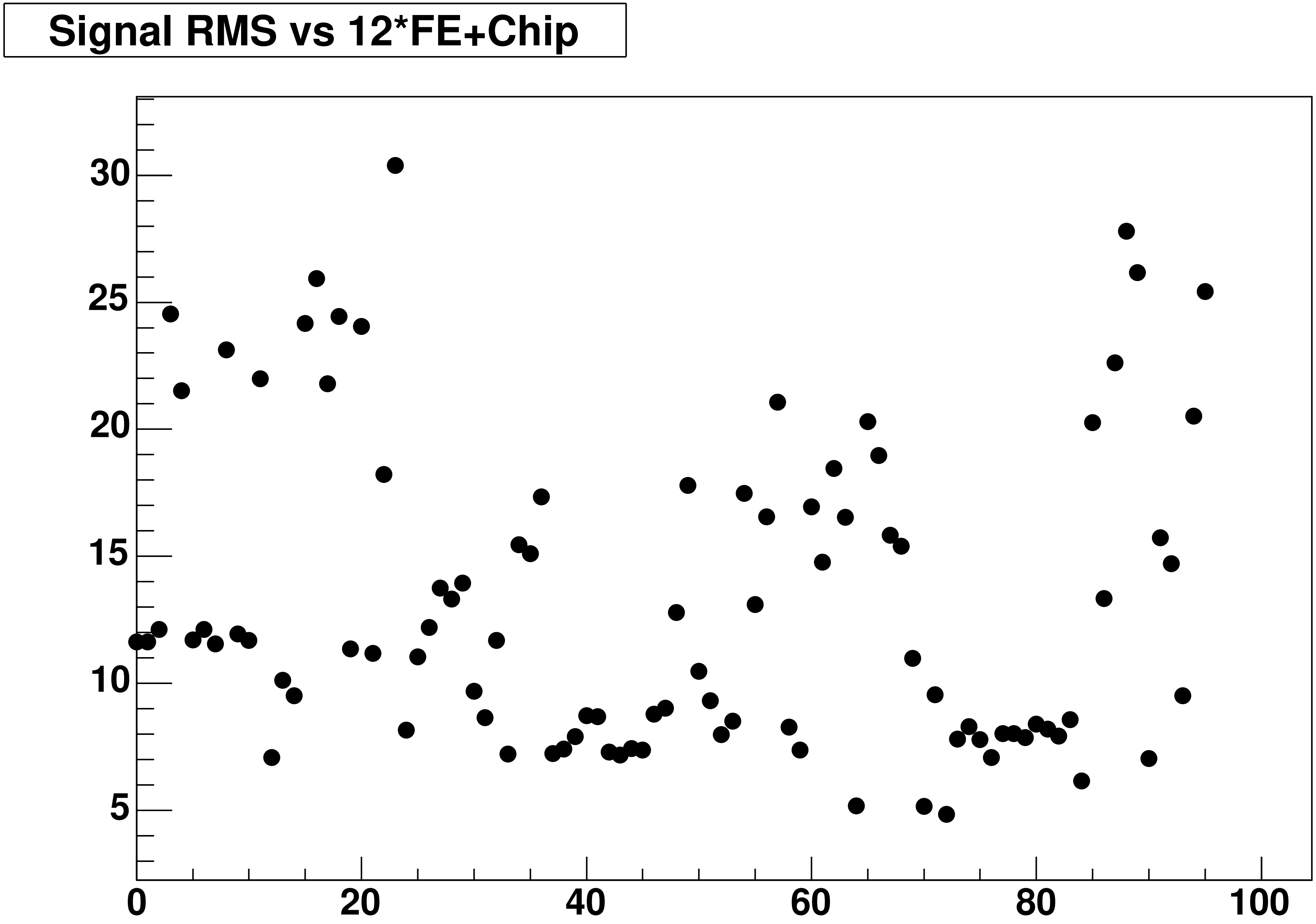

Pedestal RMS vs 12*FE+Chip
1.6
1.4
1.2
1
0.8
0.6
0
20
40
60
80
100


Raw signal vs 12*FE+Chip
19300
19250
19200
19150
19100
19050
19000
18950
18900
0
20
40
60
80
100


Raw signal RMS vs 12*FE+Chip
30
25
20
15
10
5
0
20
40
60
80
100



Signal vs 12*FE+Chip
19350
19300
19250
19200
19150
19100
19050
19000
18950
18900
0
20
40
60
80
100


Signal RMS vs 12*FE+Chip
30
25
20
15
10
5
0
20
40
60
80
100