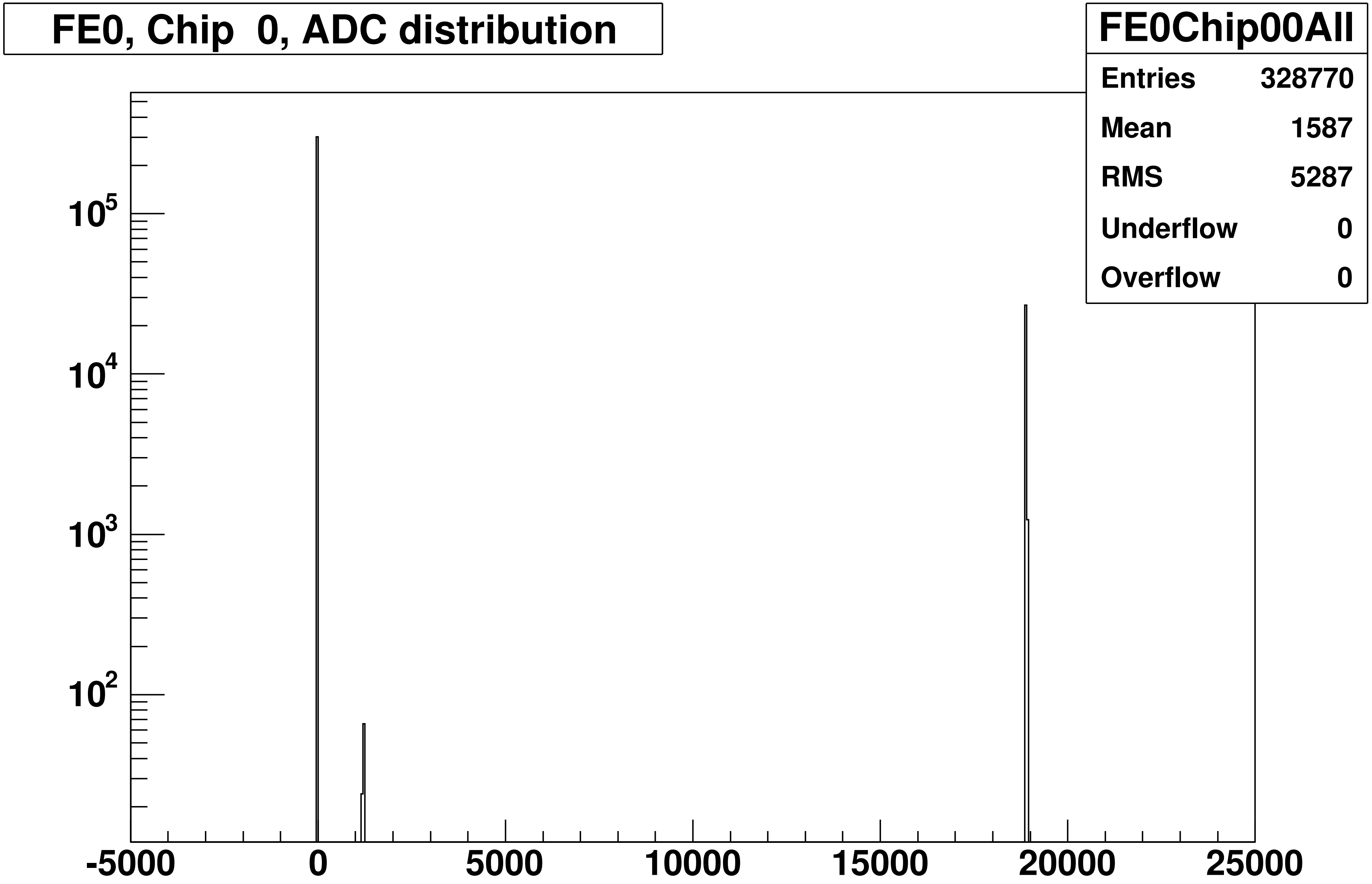
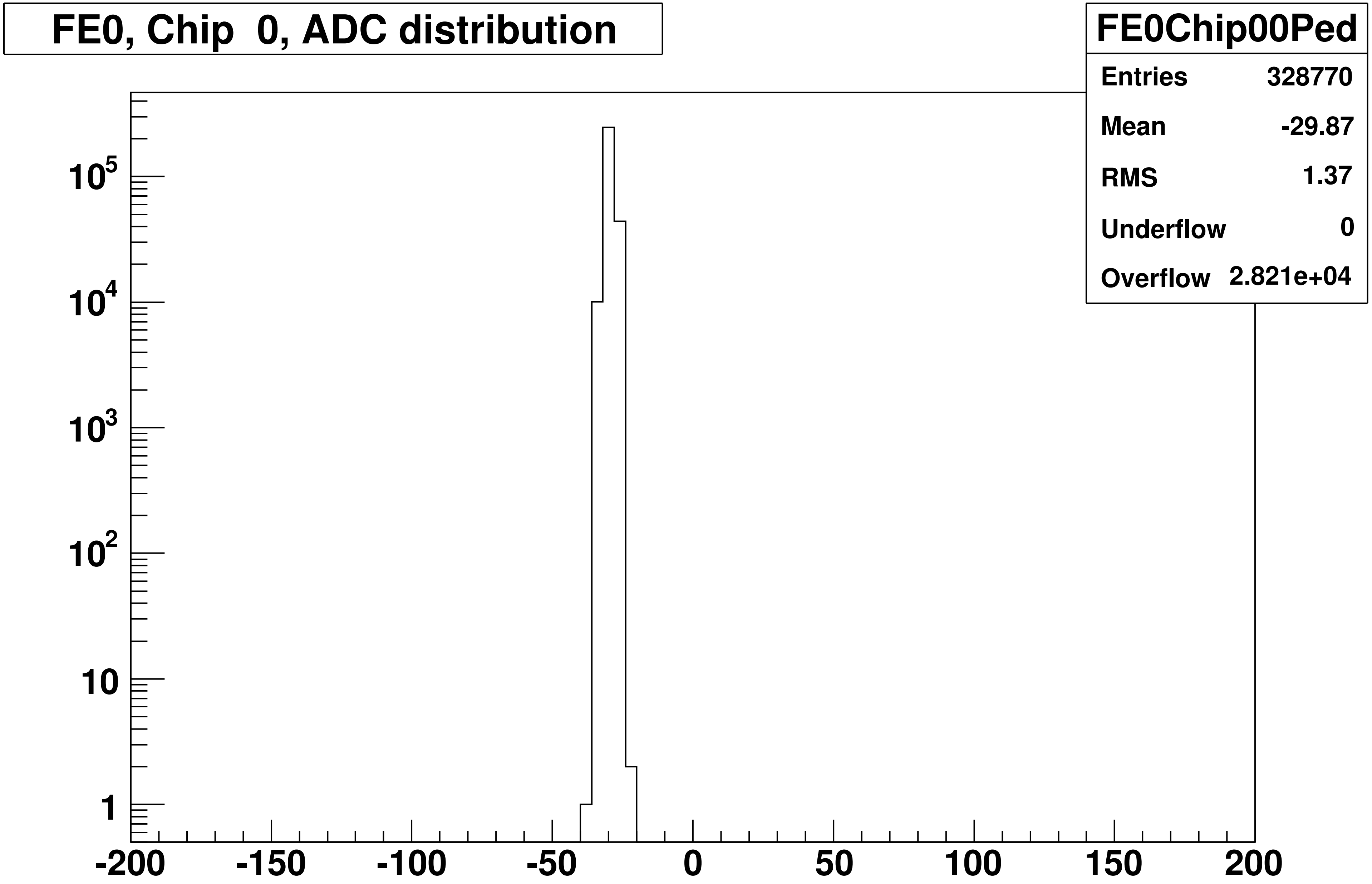
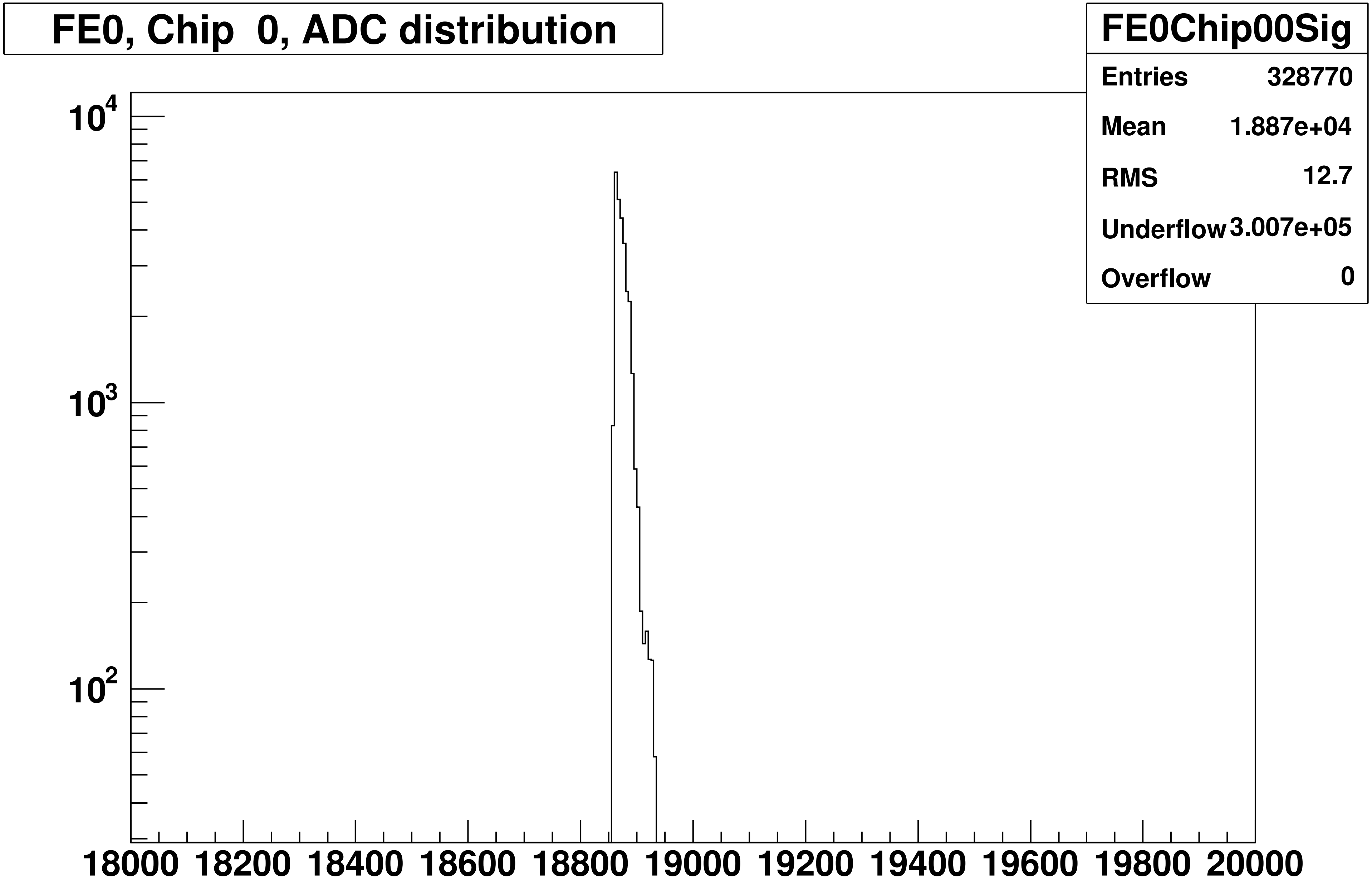

FE0, Chip 0, ADC distribution
FE0Chip00All
Entries 328770
Mean 1587
RMS 5287
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000



FE0, Chip 0, ADC distribution
FE0Chip00Ped
Entries 328770
Mean -29.87
RMS 1.37
Underflow 0
Overflow 2.821e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
200


FE0, Chip 0, ADC distribution
FE0Chip00Sig
Entries 328770
Mean 1.887e+04
RMS 12.7
Underflow 3.007e+05
Overflow 0
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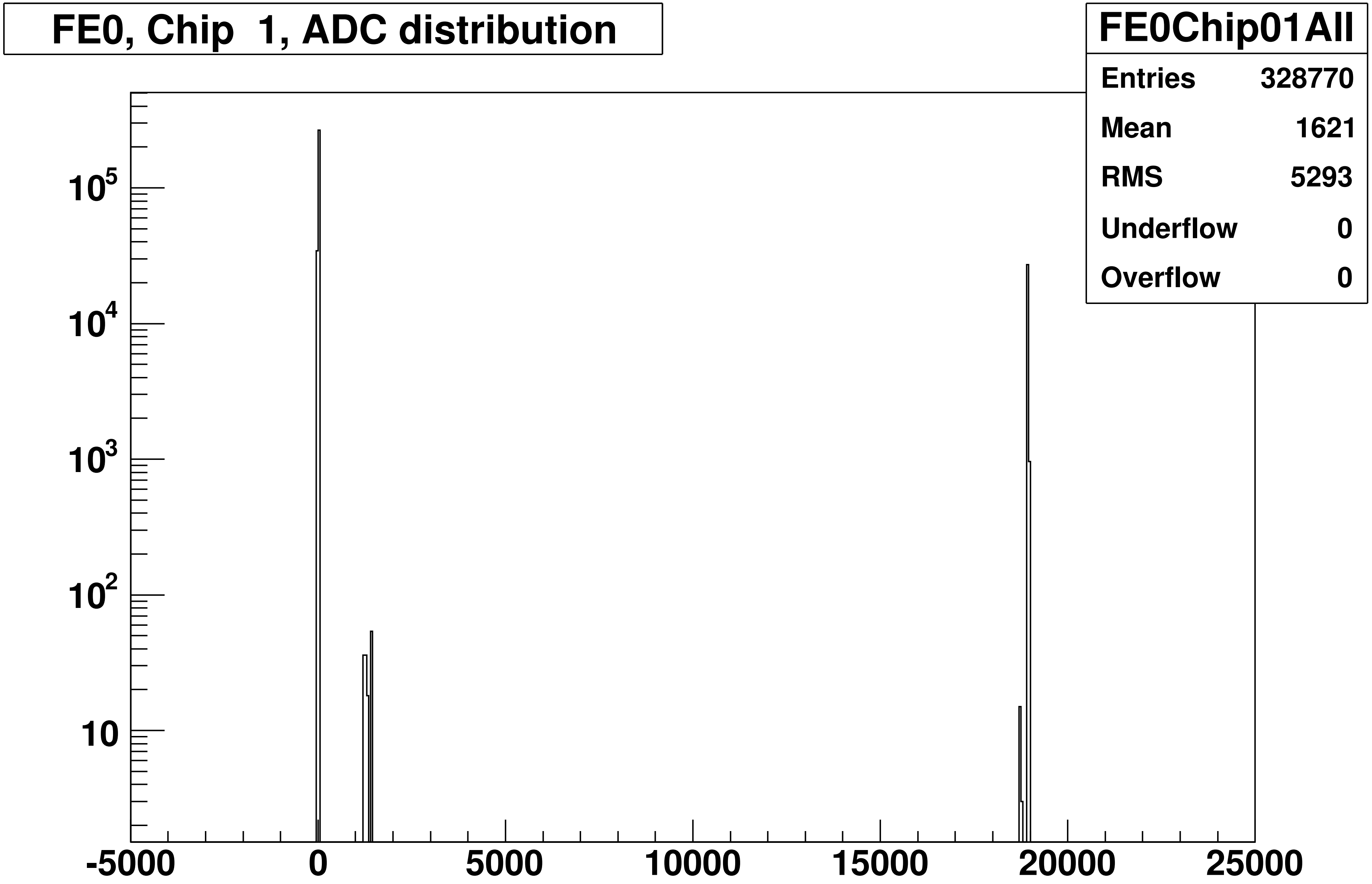
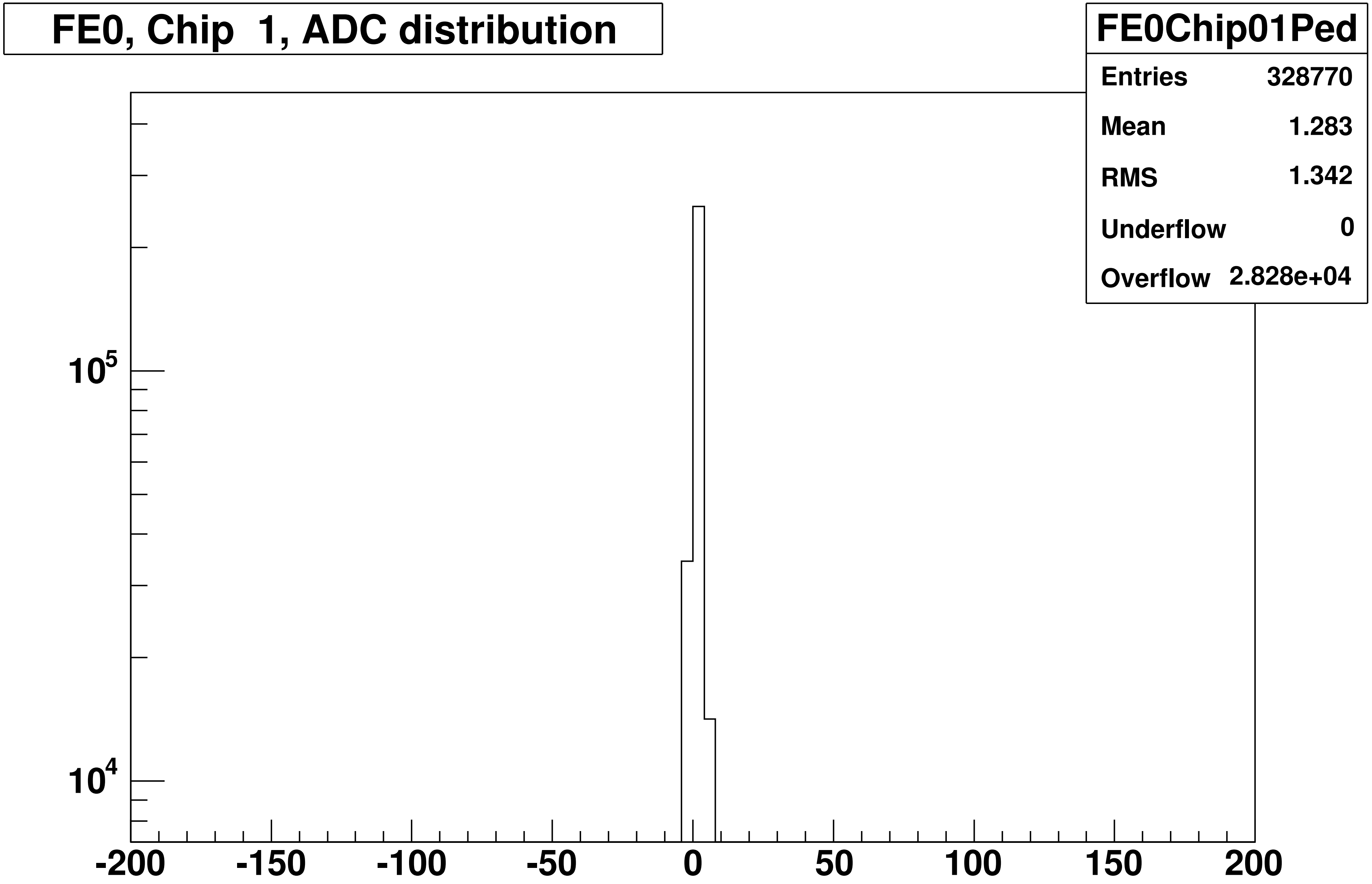
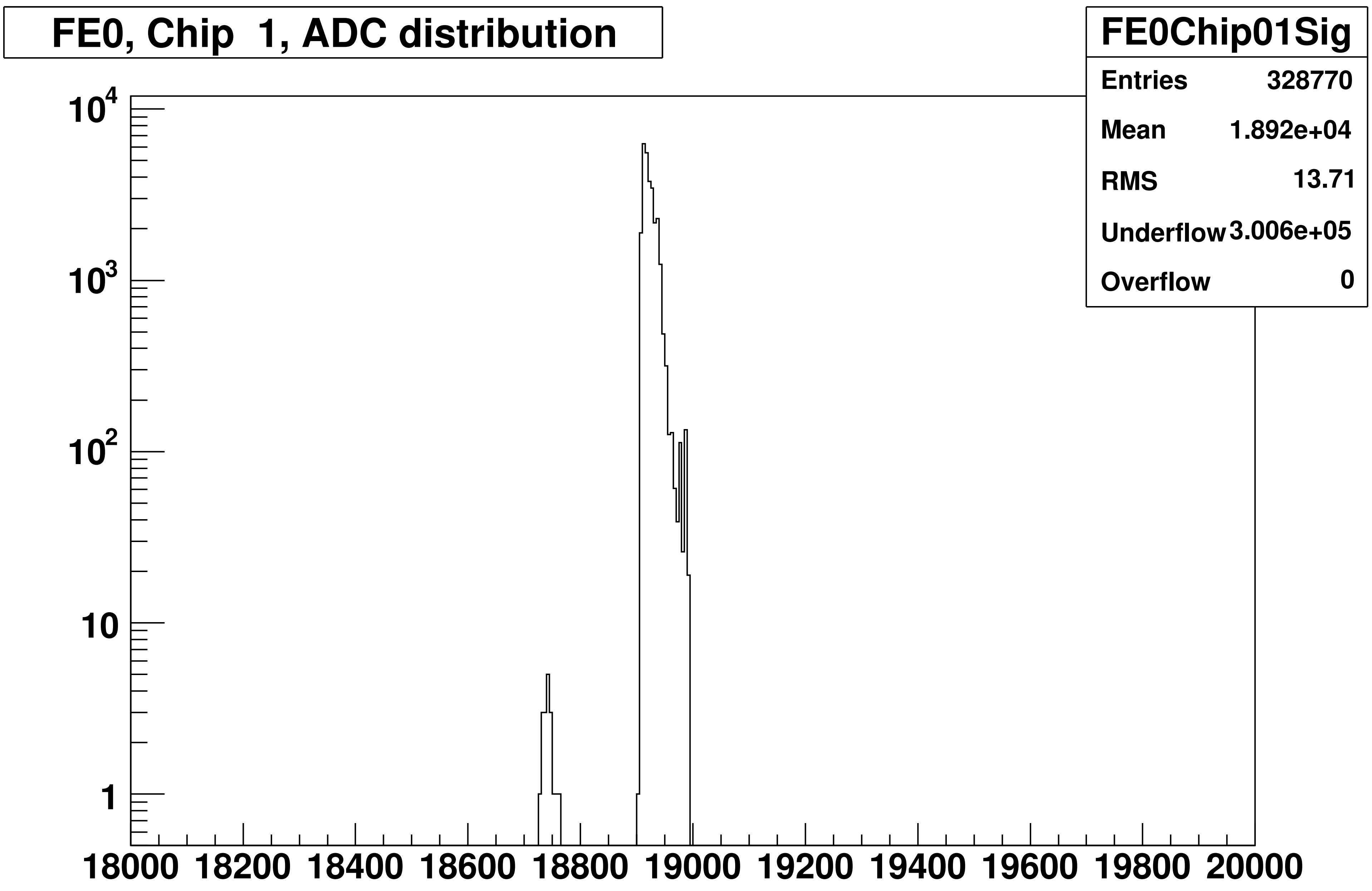
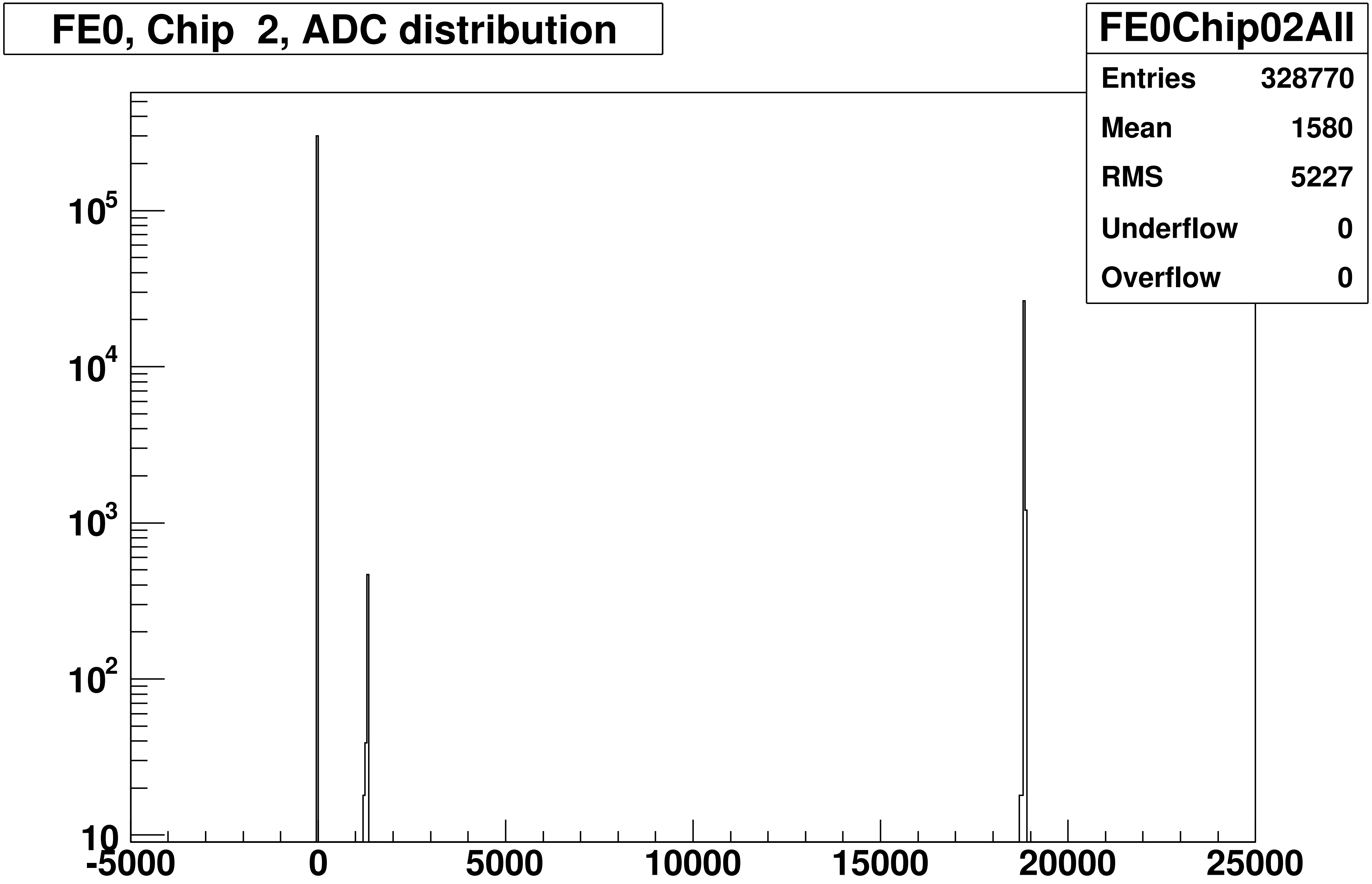
10^3
10^2
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000

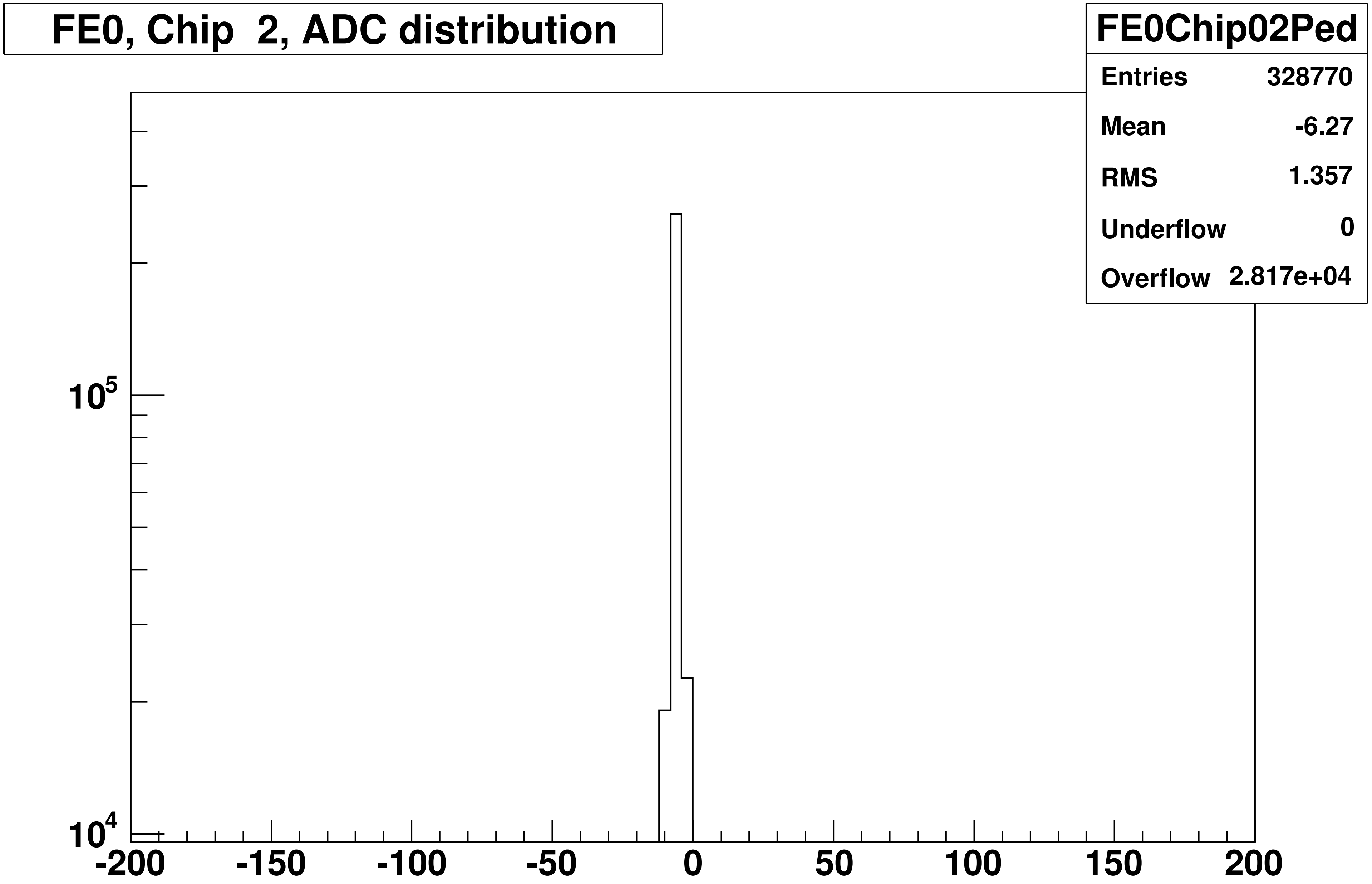


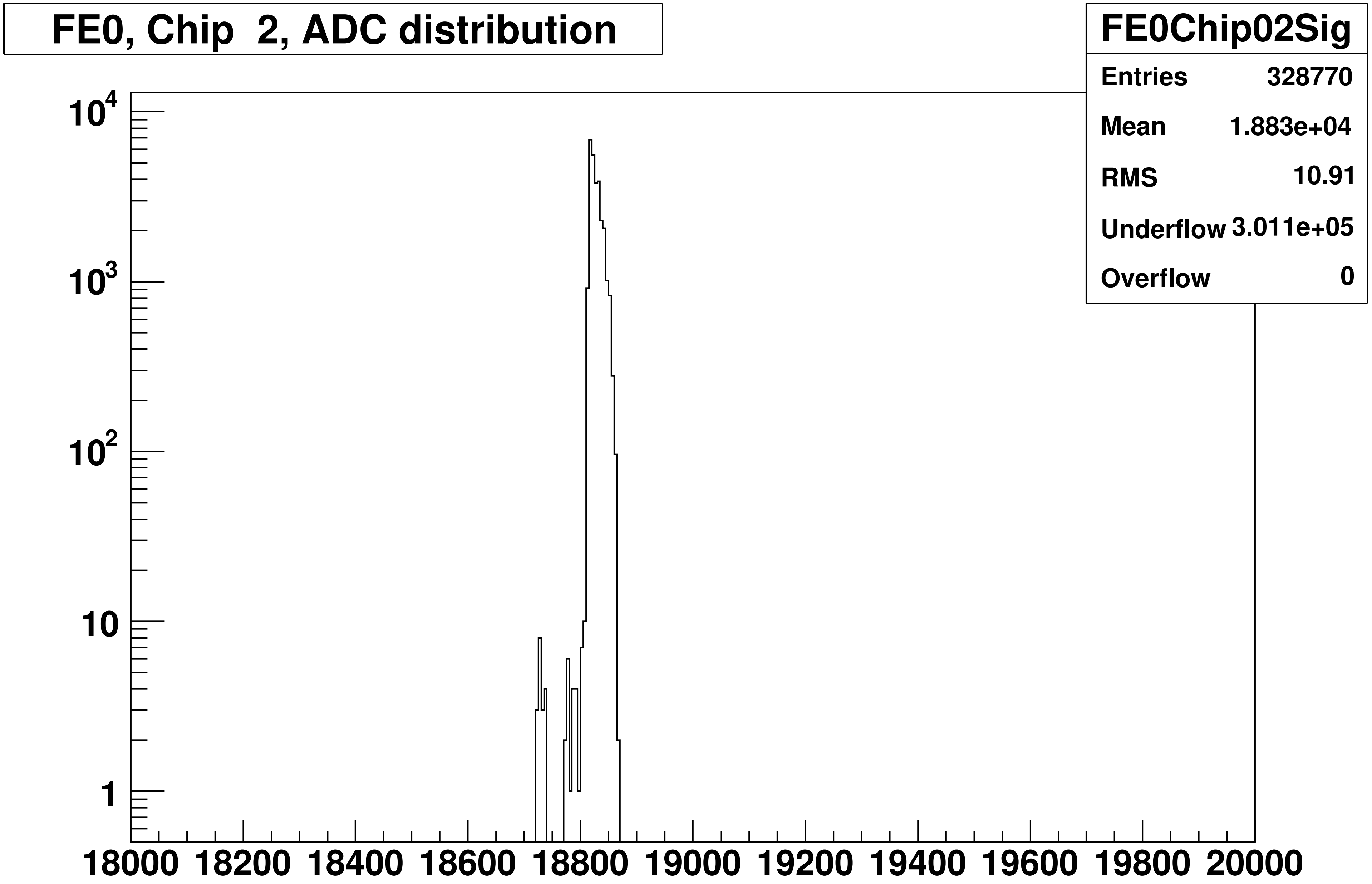
FE0, Chip 1, ADC distribution
FE0Chip01All
Entries 328770
Mean 1621
RMS 5293
Underflow 0
Overflow 0
10
10^2
10^3
10^4
10^5
-5000
0
5000
10000
15000
20000
25000

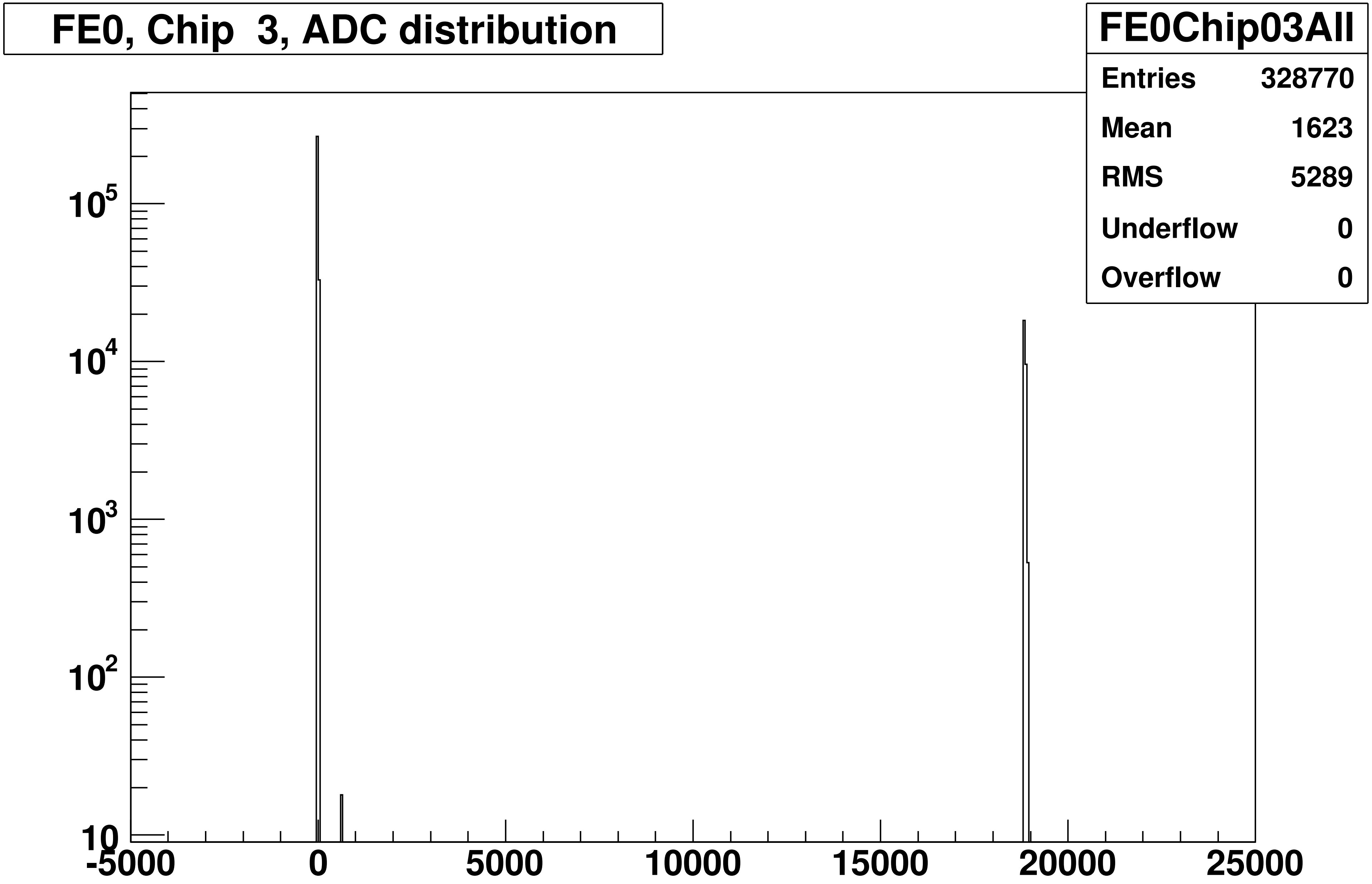

FE0, Chip 1, ADC distribution
FE0Chip01Ped
Entries 328770
Mean 1.283
RMS 1.342
Underflow 0
Overflow 2.828e+04
10^5
10^4
-200
-150
-100
-50
0
50
100
150
200


FE0, Chip 1, ADC distribution
FE0Chip01Sig
Entries 328770
Mean 1.892e+04
RMS 13.71
Underflow 3.006e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE0, Chip 2, ADC distribution
FE0Chip02All
Entries 328770
Mean 1580
RMS 5227
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE0, Chip 2, ADC distribution
FE0Chip02Ped
Entries 328770
Mean -6.27
RMS 1.357
Underflow 0
Overflow 2.817e+04
10^5
10^4
-200
-150
-100
-50
0
50
100
150
200


FE0, Chip 2, ADC distribution
FE0Chip02Sig
Entries 328770
Mean 1.883e+04
RMS 10.91
Underflow 3.011e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE0, Chip 3, ADC distribution
FE0Chip03All
Entries 328770
Mean 1623
RMS 5289
Underflow 0
Overflow 0
10
10^2
10^3
10^4
10^5
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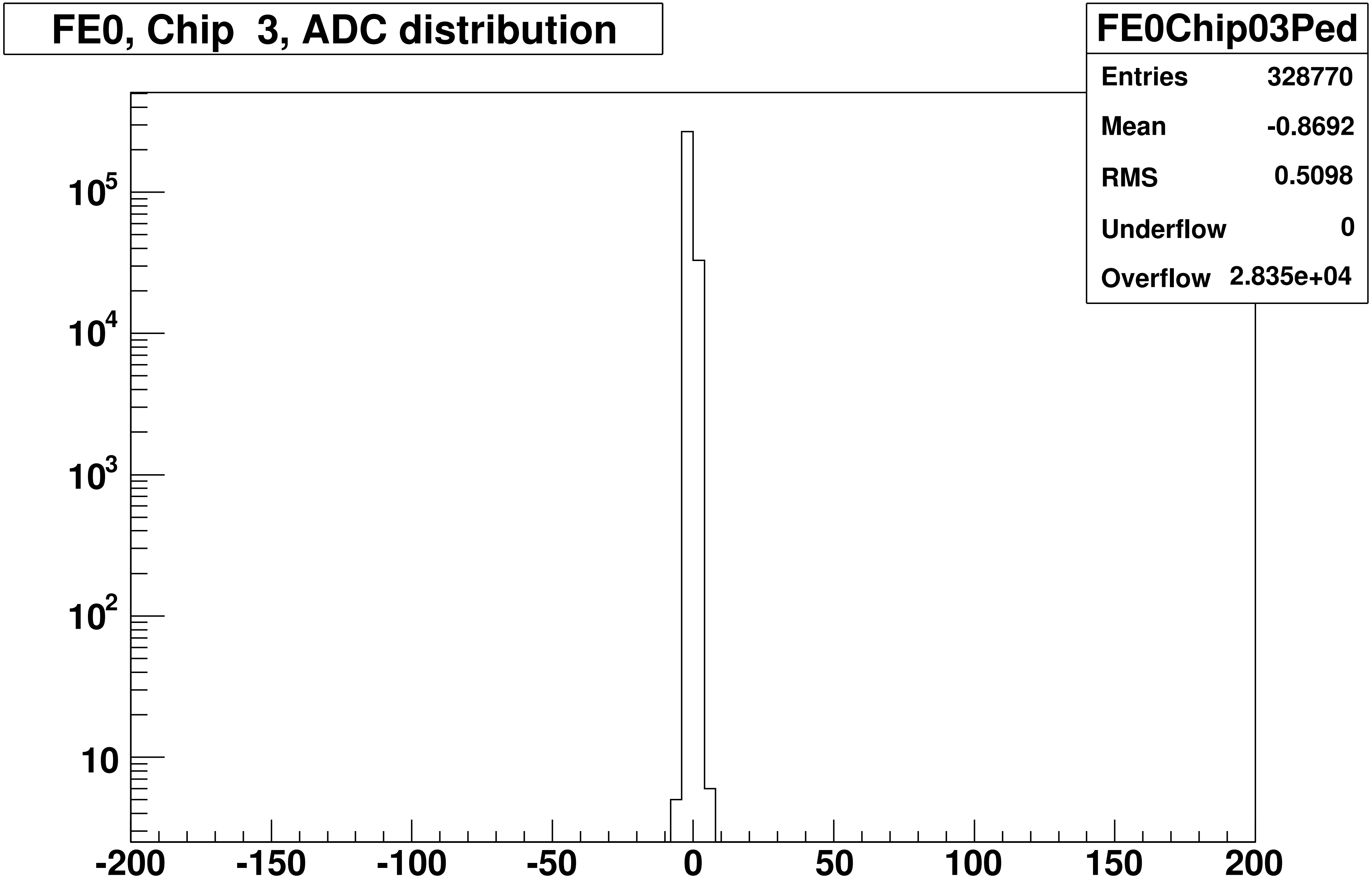
10000
15000
20000
25000


FE0, Chip 3, ADC distribution
FE0Chip03Ped
Entries 328770
Mean -0.8692
RMS 0.5098
Underflow 0
Overflow 2.835e+04
10^5
10^4
10^3
10^2
10
-200
-150
-100
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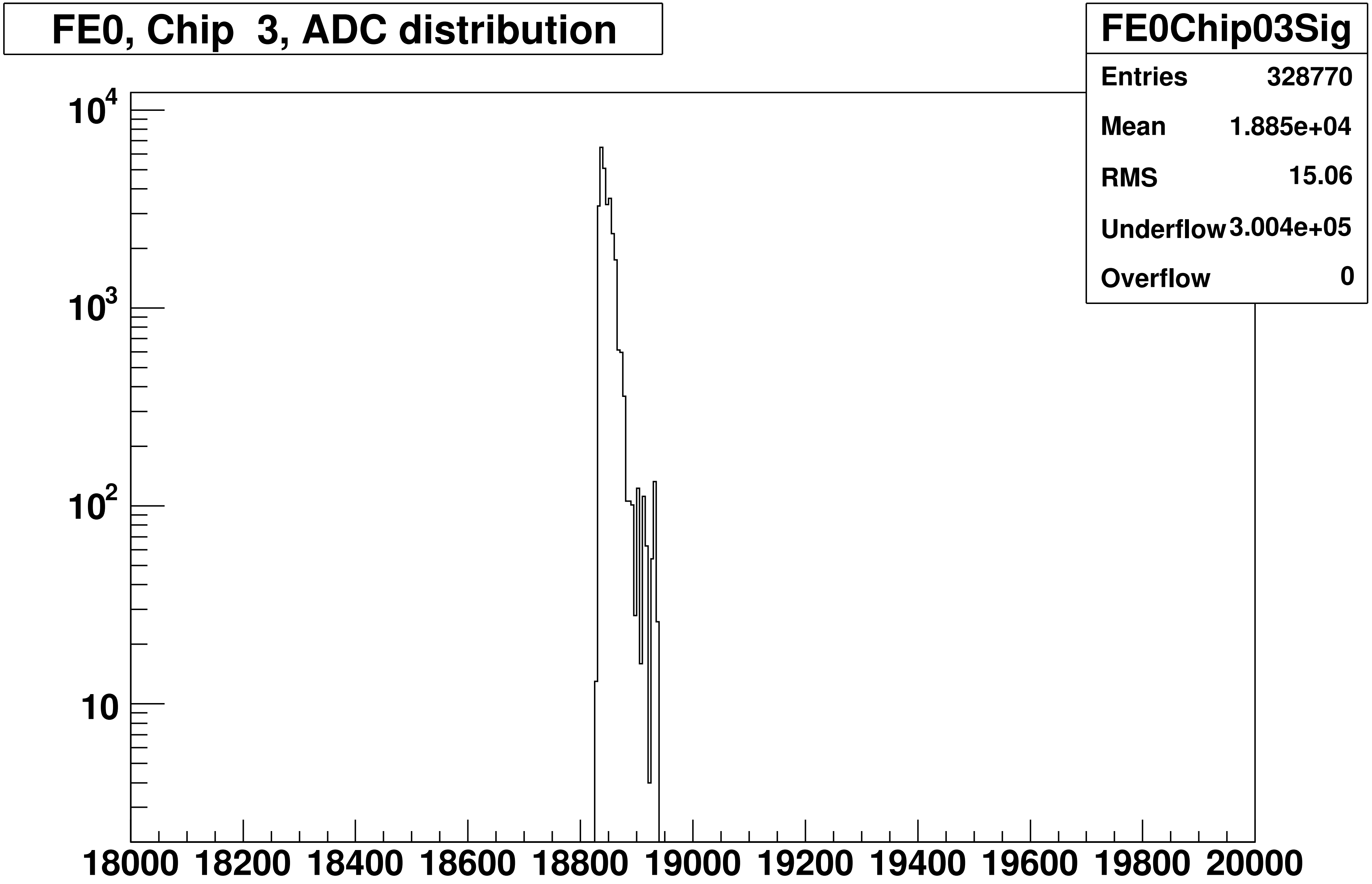
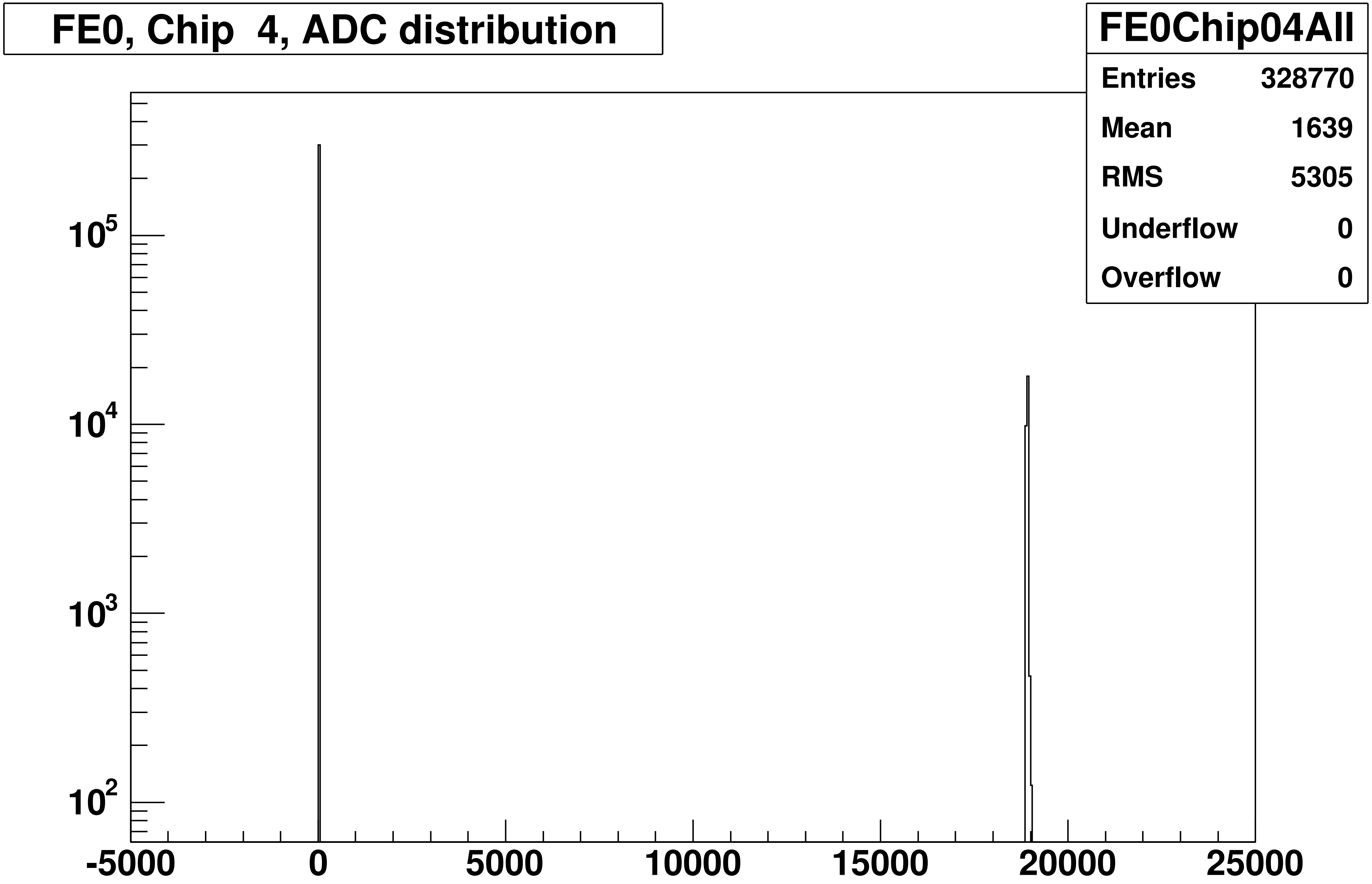
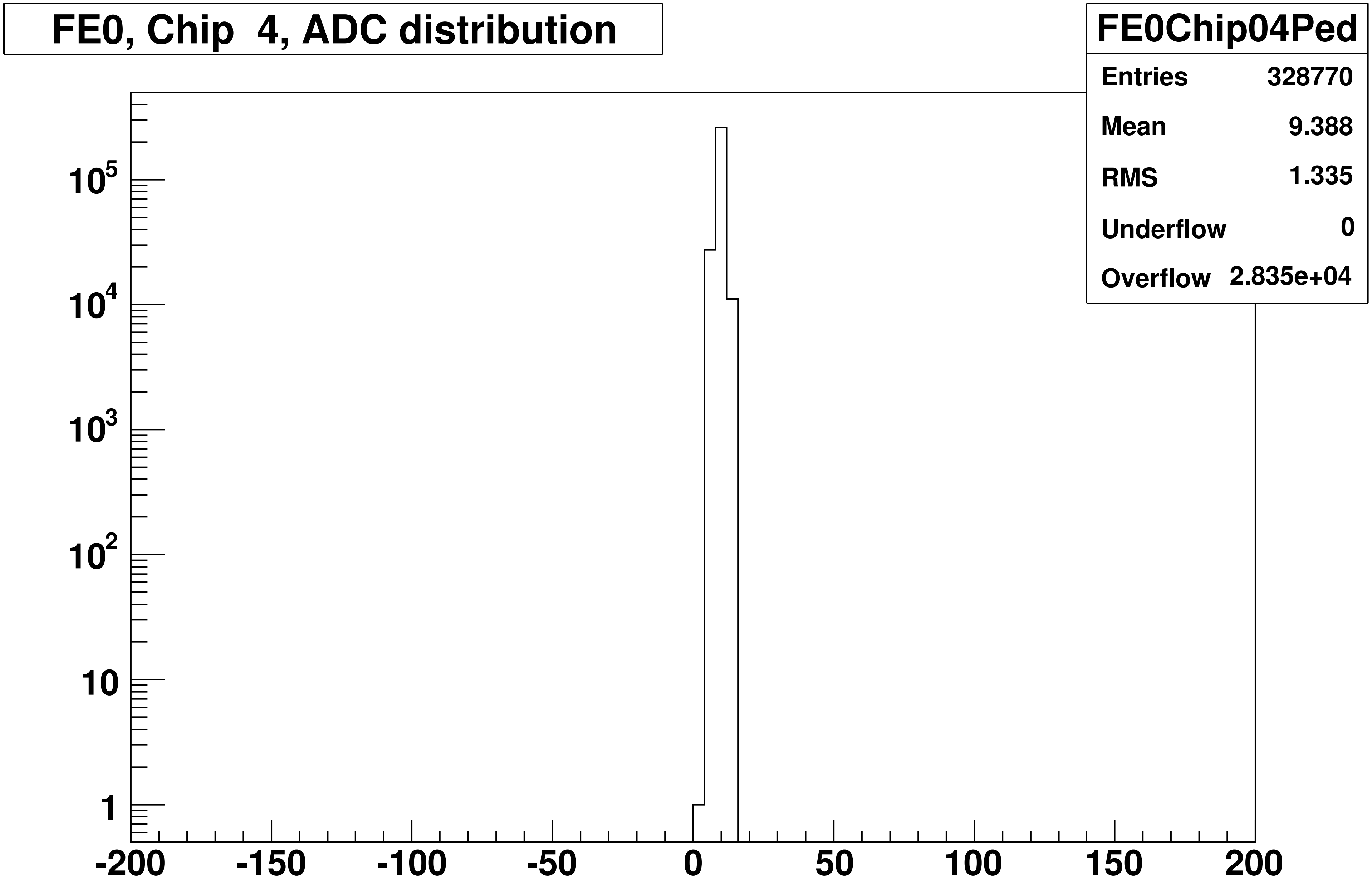
0
50
100
150
200


FE0, Chip 3, ADC distribution
FE0Chip03Sig
Entries 328770
Mean 1.885e+04
RMS 15.06
Underflow 3.004e+05
Overflow 0
10^4
10^3
10^2
10
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000



FE0, Chip 4, ADC distribution
FE0Chip04All
Entries 328770
Mean 1639
RMS 5305
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000



FE0, Chip 4, ADC distribution
FE0Chip04Ped
Entries 328770
Mean 9.388
RMS 1.335
Underflow 0
Overflow 2.835e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
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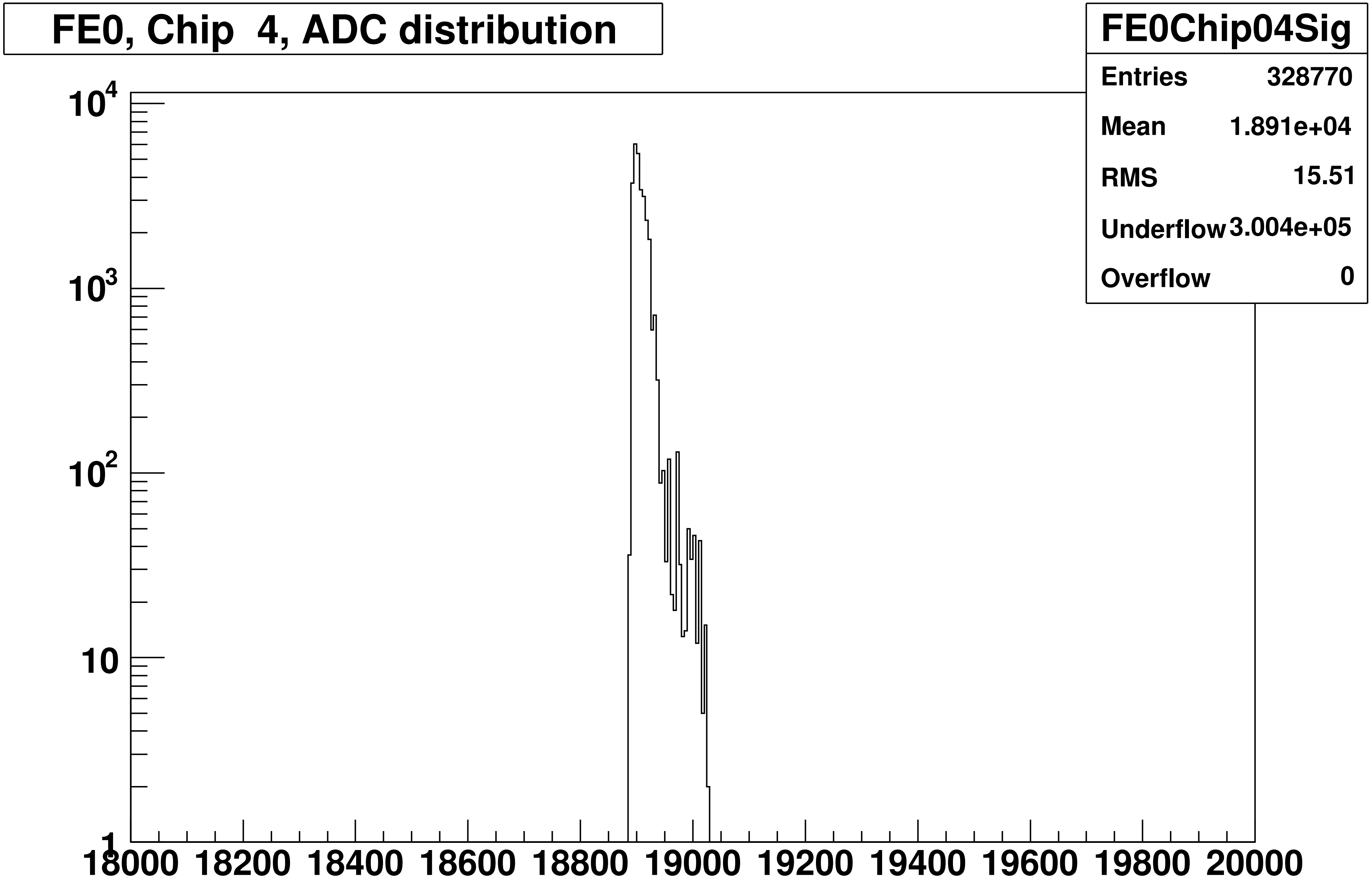
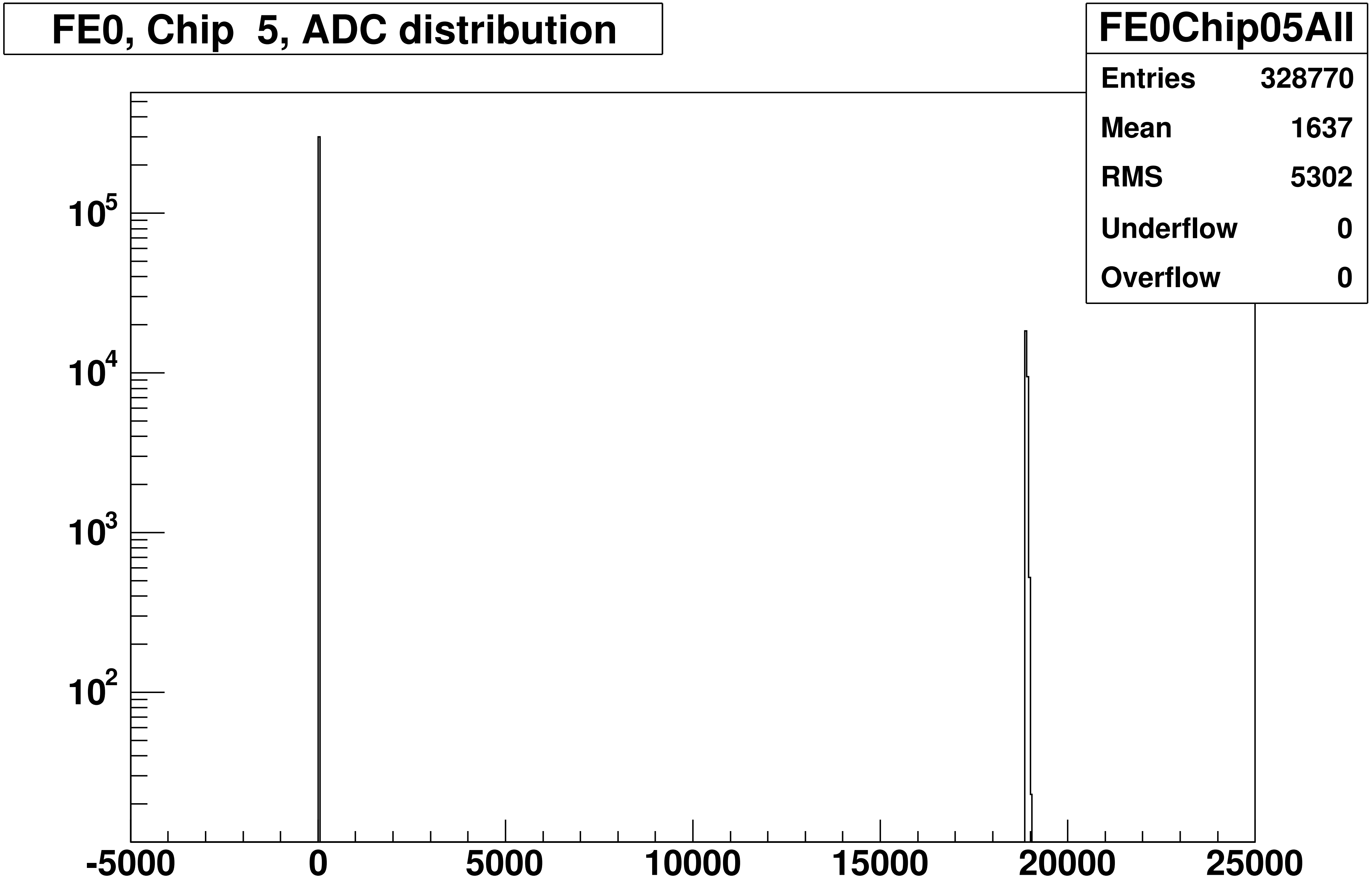
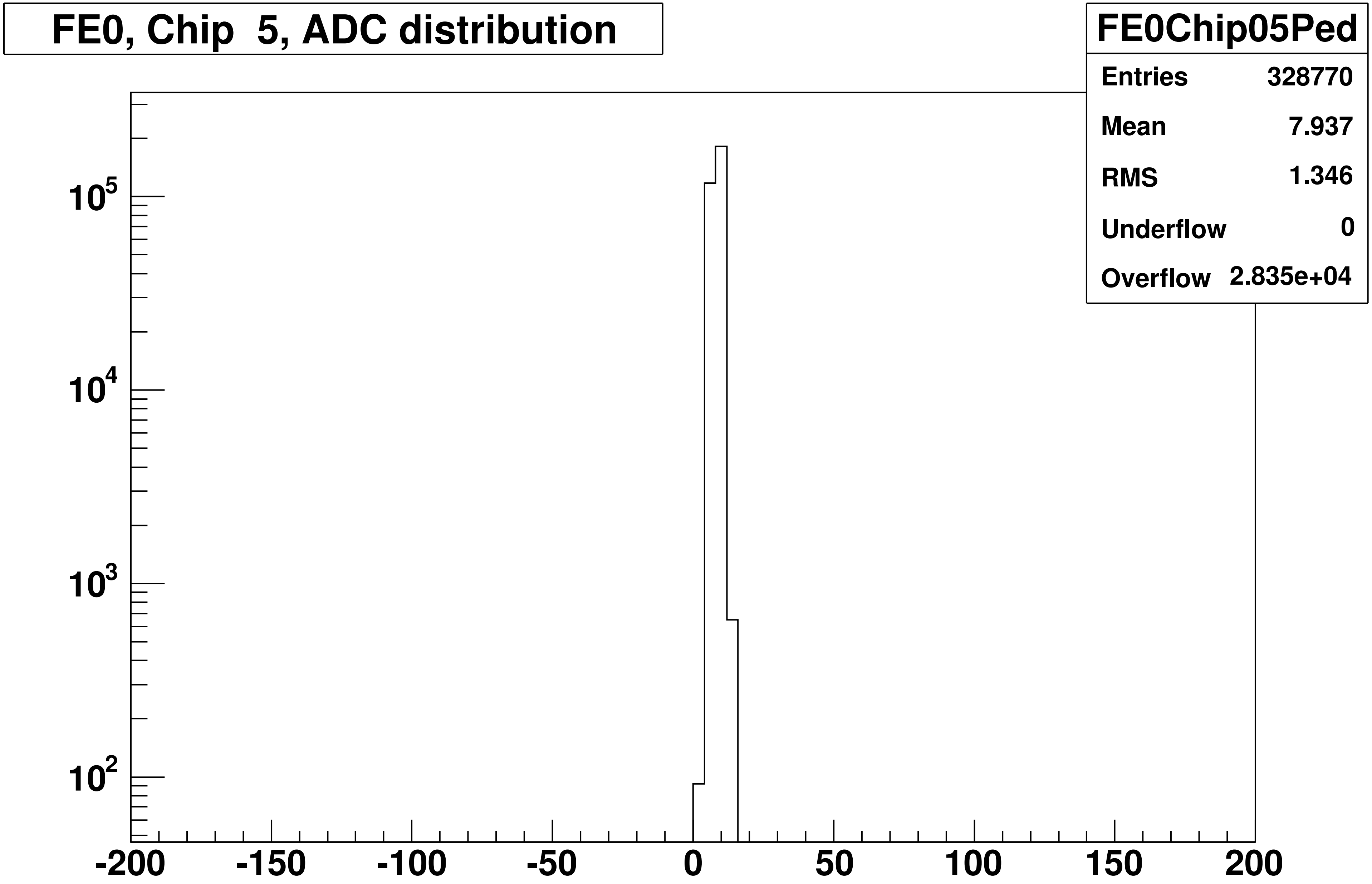
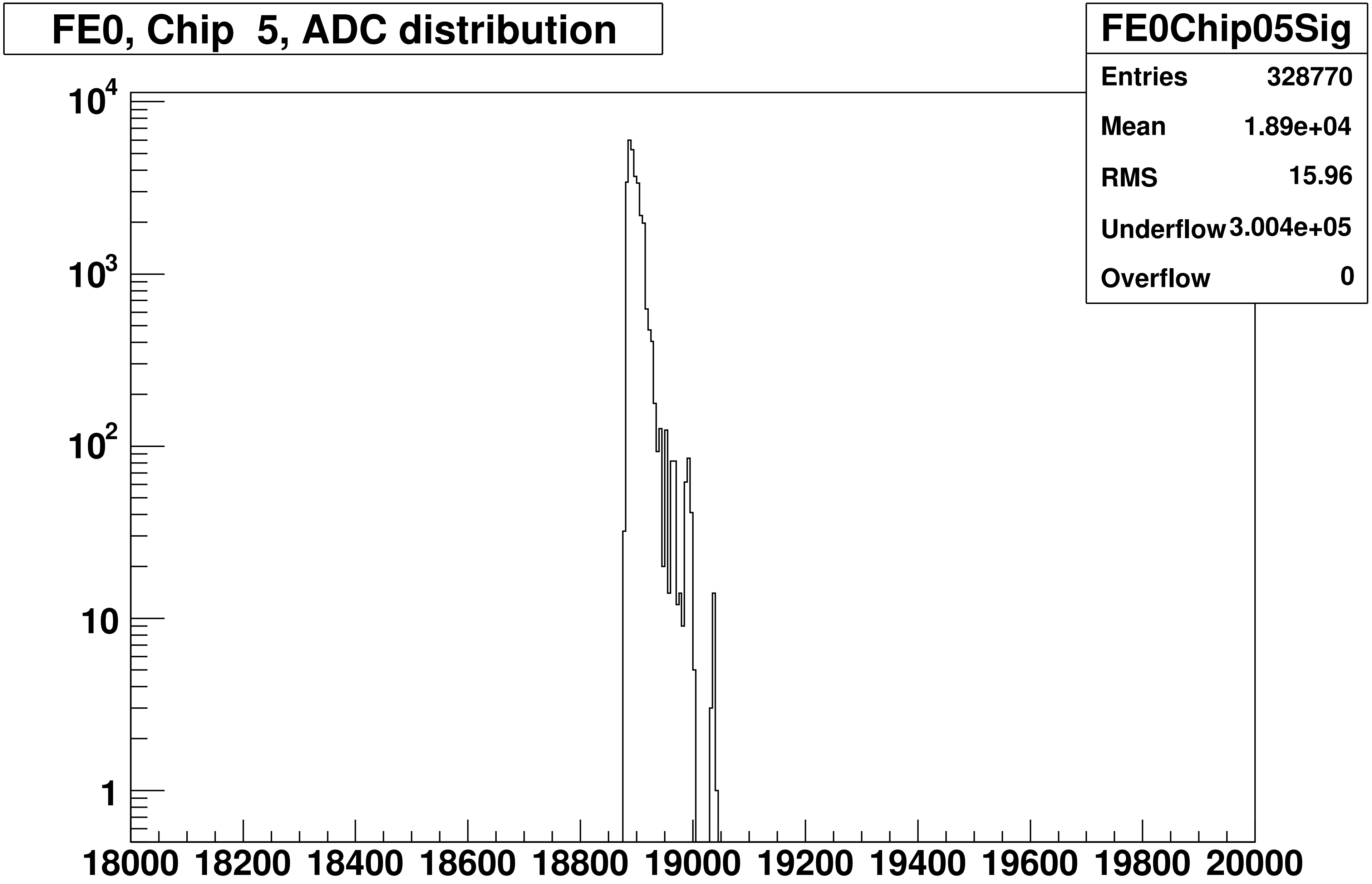
50
100
150
200

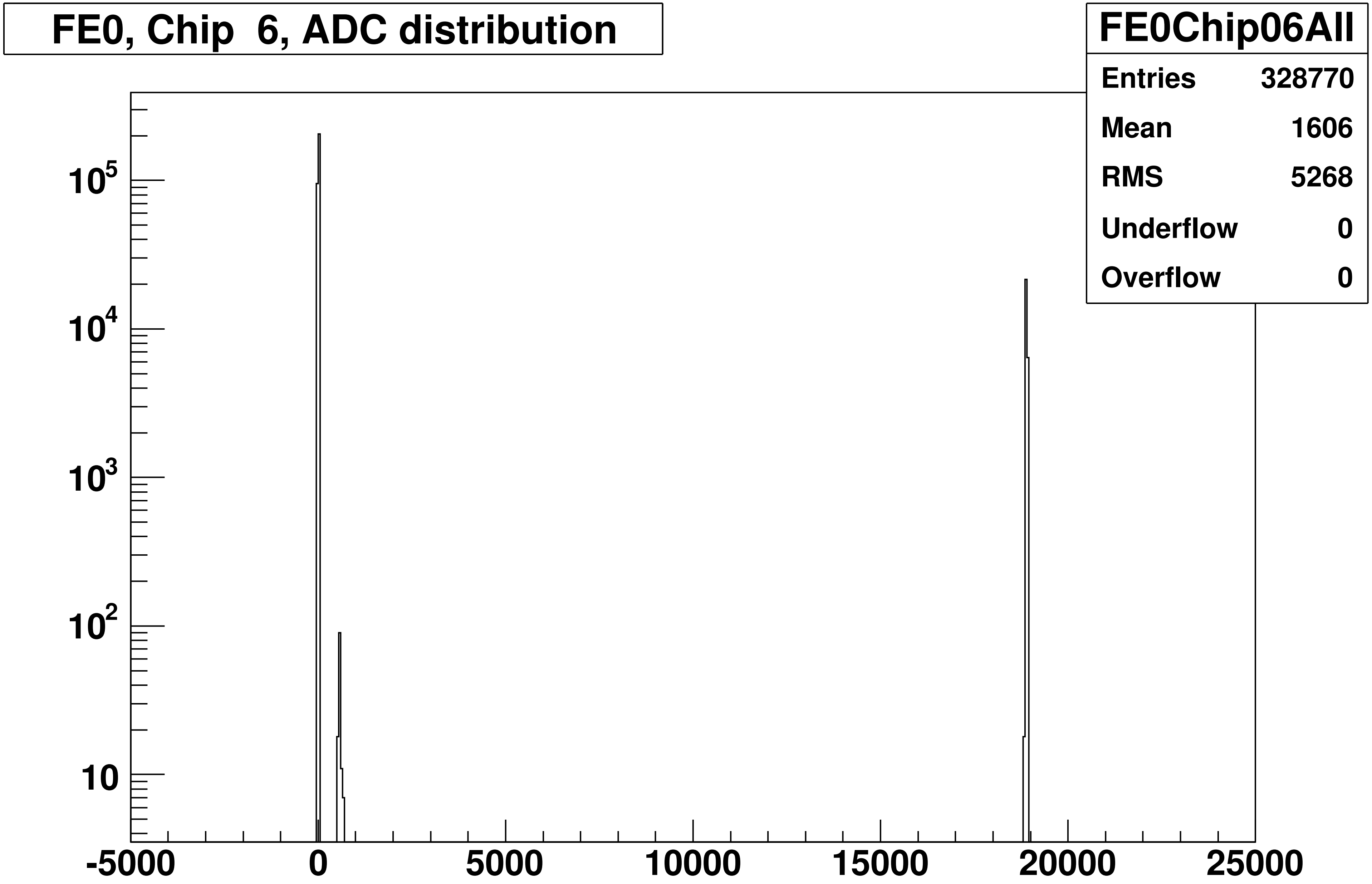

FE0, Chip 4, ADC distribution
FE0Chip04Sig
Entries 328770
Mean 1.891e+04
RMS 15.51
Underflow 3.004e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000

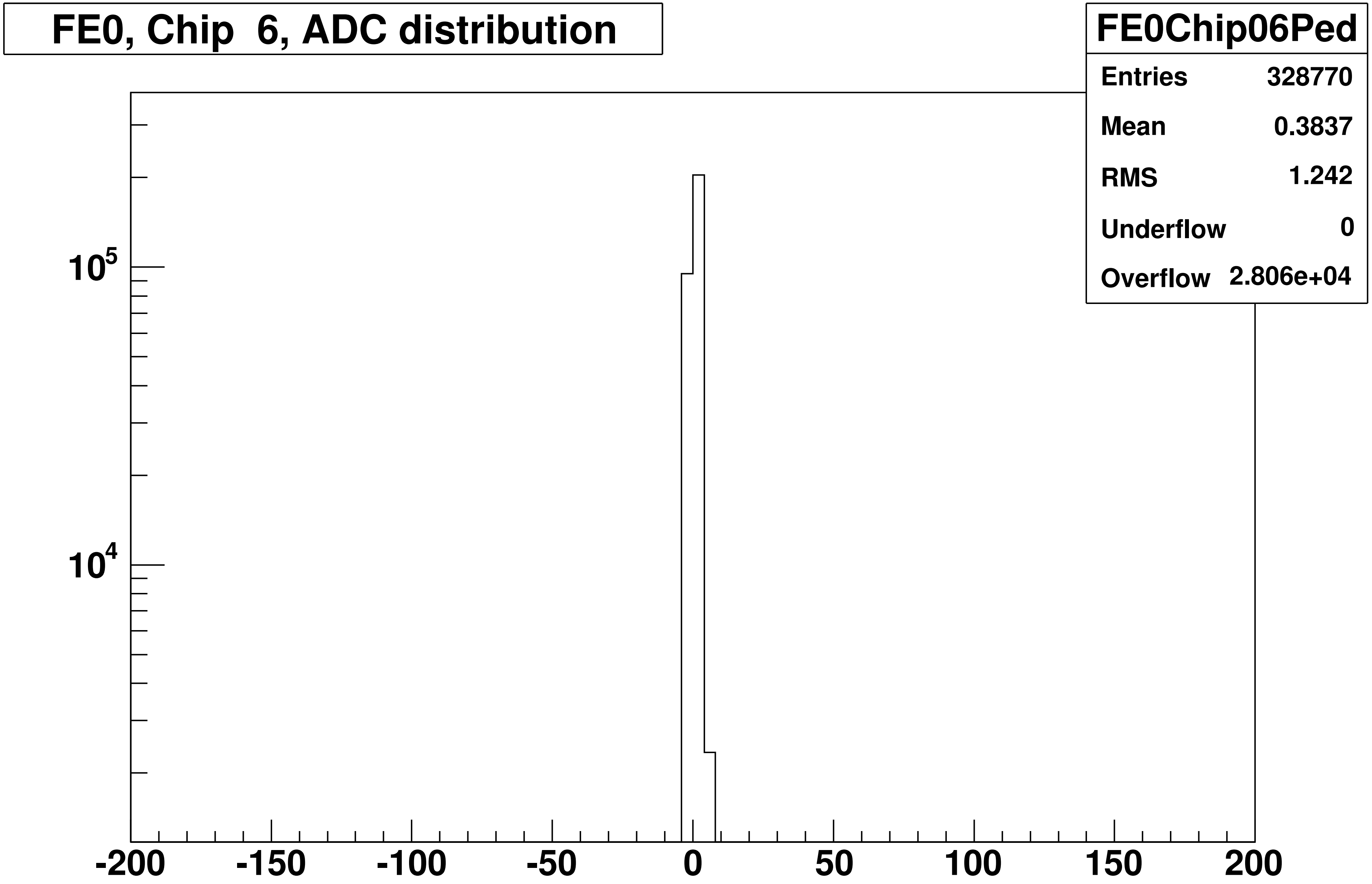

FE0, Chip 5, ADC distribution
FE0Chip05All
Entries 328770
Mean 1637
RMS 5302
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000



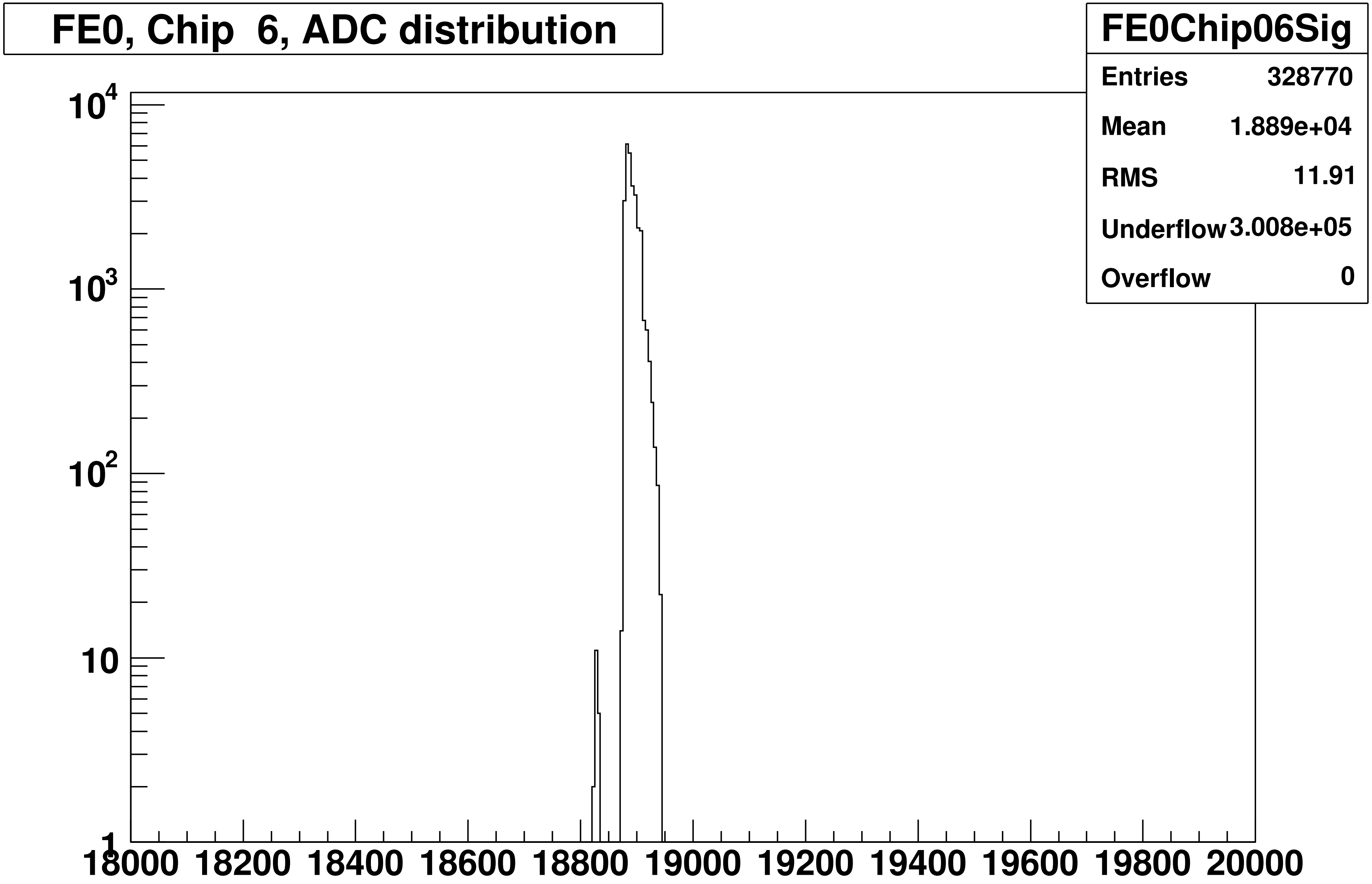
FE0, Chip 5, ADC distribution
FE0Chip05Ped
Entries 328770
Mean 7.937
RMS 1.346
Underflow 0
Overflow 2.835e+04
10^5
10^4
10^3
10^2
-200
-150
-100
-50
0
50
100
150
200


FE0, Chip 5, ADC distribution
FE0Chip05Sig
Entries 328770
Mean 1.89e+04
RMS 15.96
Underflow 3.004e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000

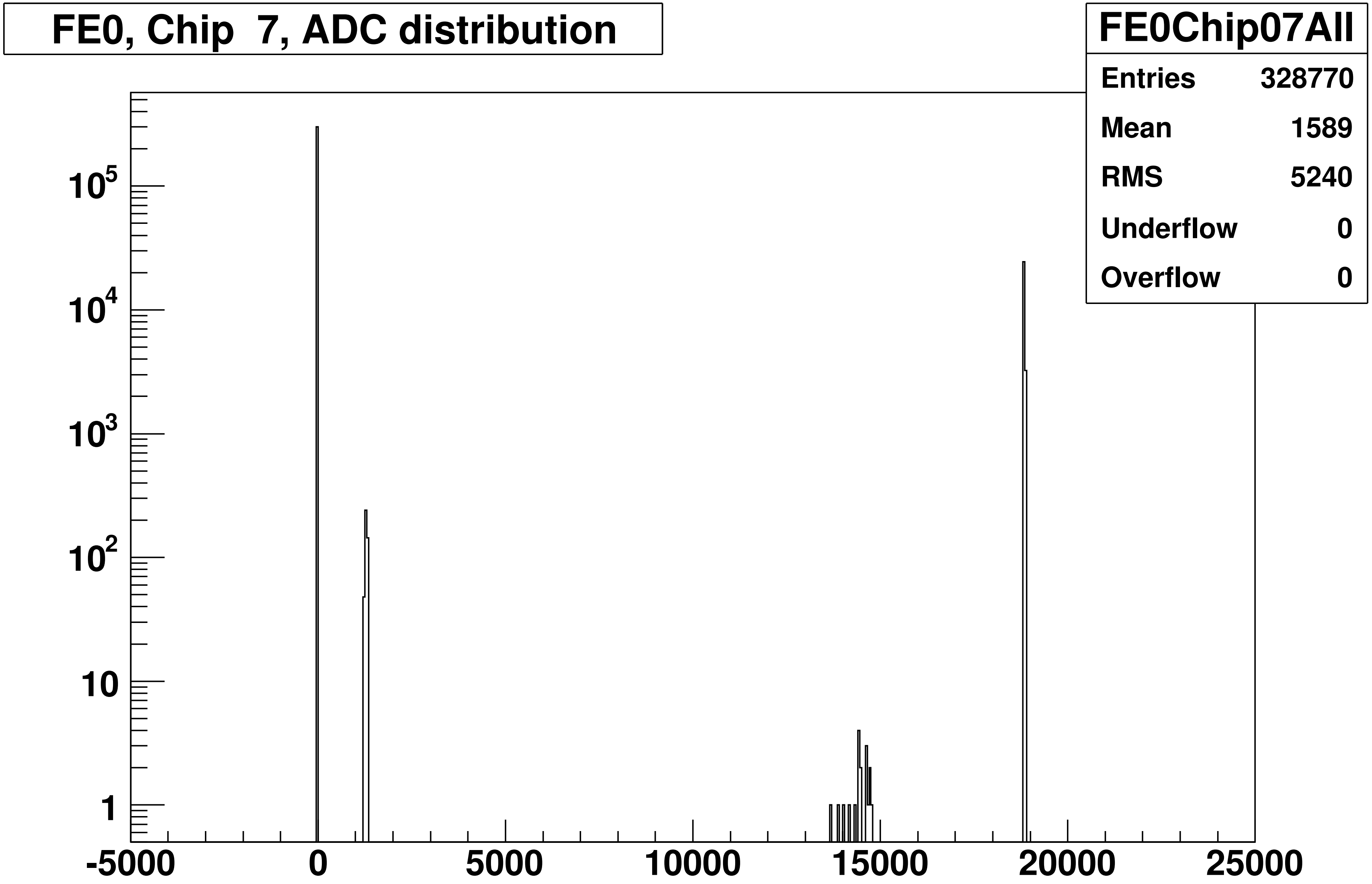

FE0, Chip 6, ADC distribution
FE0Chip06All
Entries 328770
Mean 1606
RMS 5268
Underflow 0
Overflow 0
10
10^2
10^3
10^4
10^5
-5000
0
5000
10000
15000
20000
25000



FE0, Chip 6, ADC distribution
FE0Chip06Ped
Entries 328770
Mean 0.3837
RMS 1.242
Underflow 0
Overflow 2.806e+04
10^5
10^4
-200
-150
-100
-50
0
50
100
150
200



FE0, Chip 6, ADC distribution
FE0Chip06Sig
Entries 328770
Mean 1.889e+04
RMS 11.91
Underflow 3.008e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE0, Chip 7, ADC distribution
FE0Chip07All
Entries 328770
Mean 1589
RMS 5240
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
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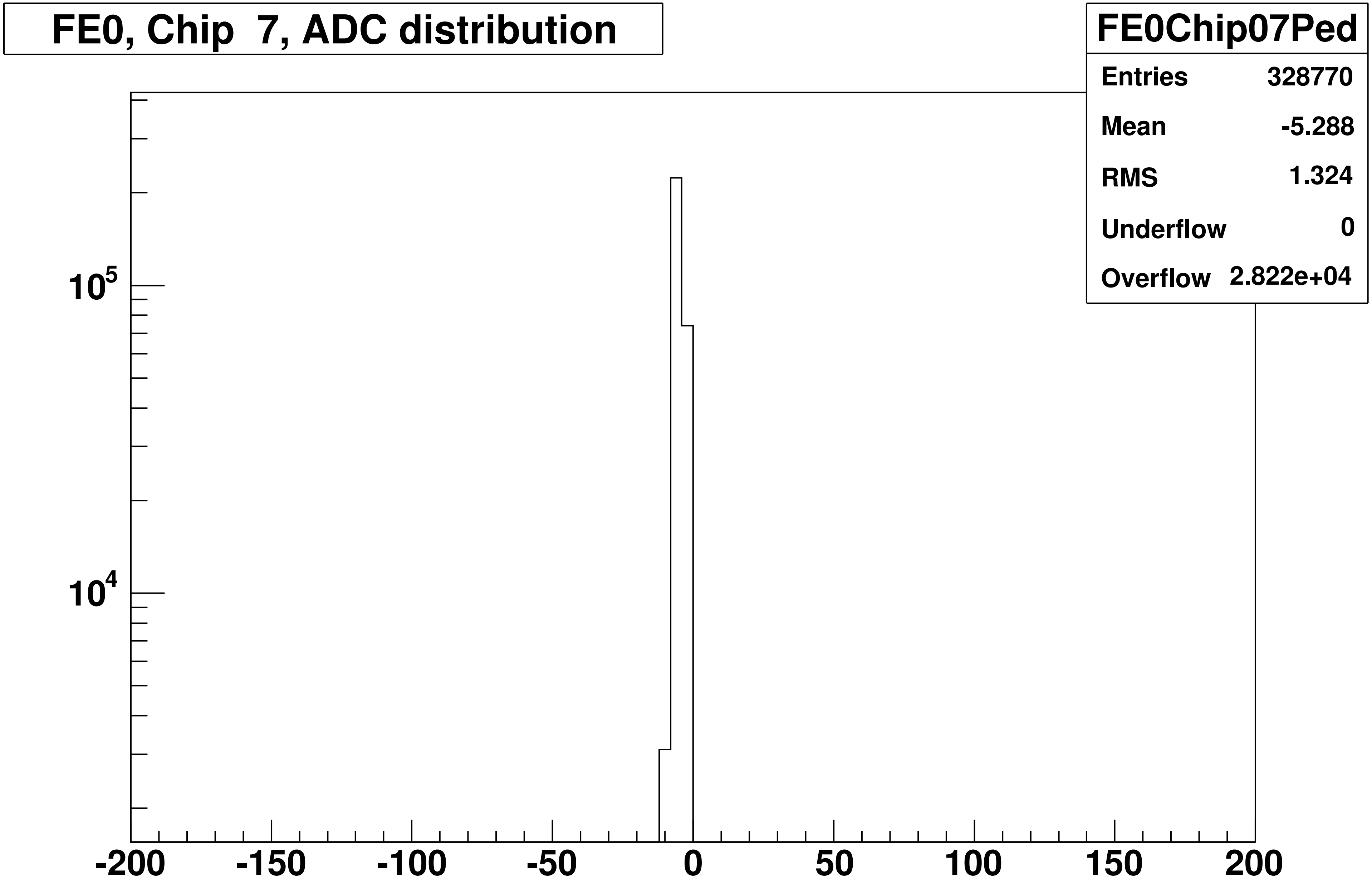
10000
15000
20000
25000


FE0, Chip 7, ADC distribution
FE0Chip07Ped
Entries 328770
Mean -5.288
RMS 1.324
Underflow 0
Overflow 2.822e+04
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10^4
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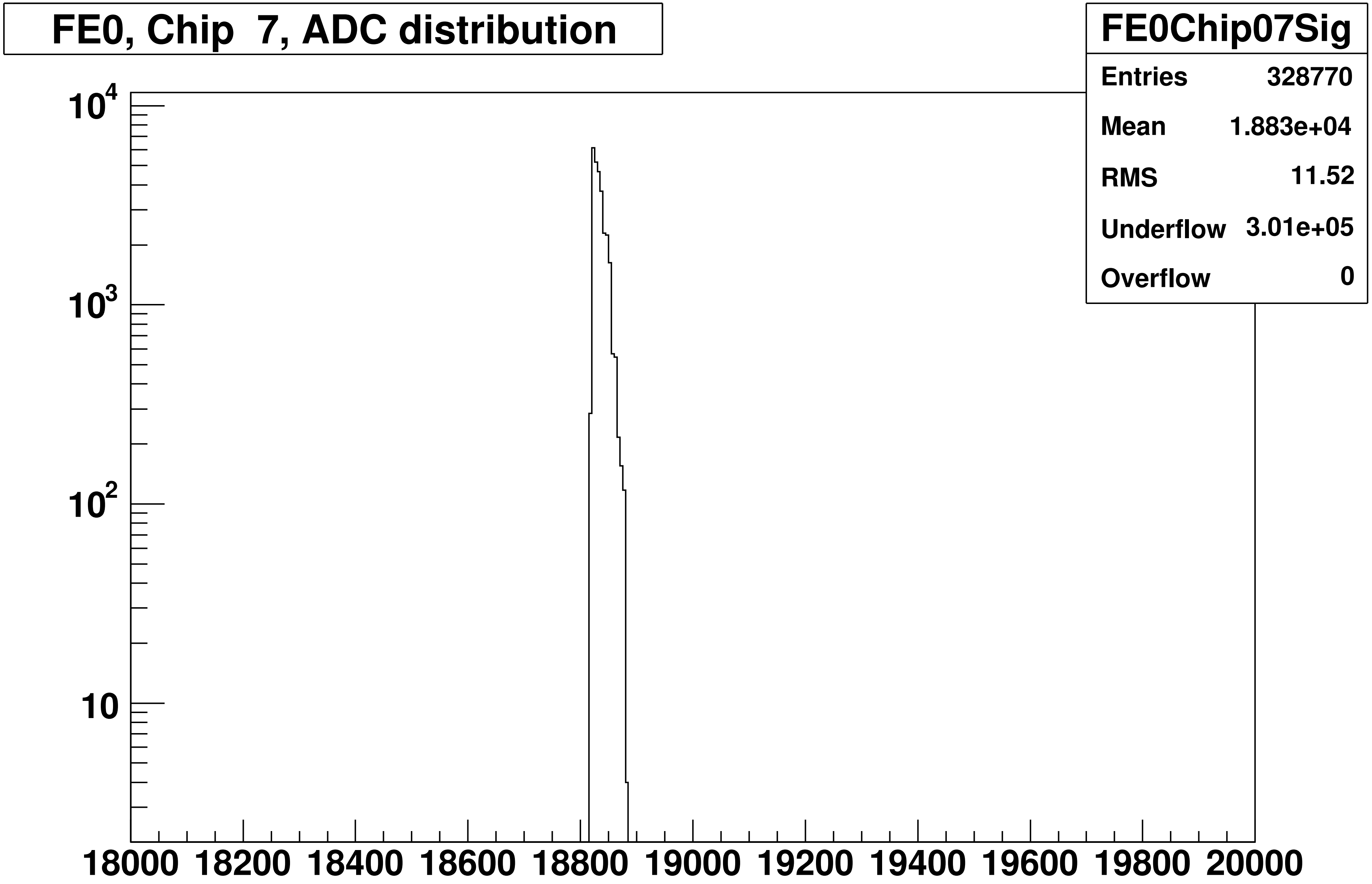
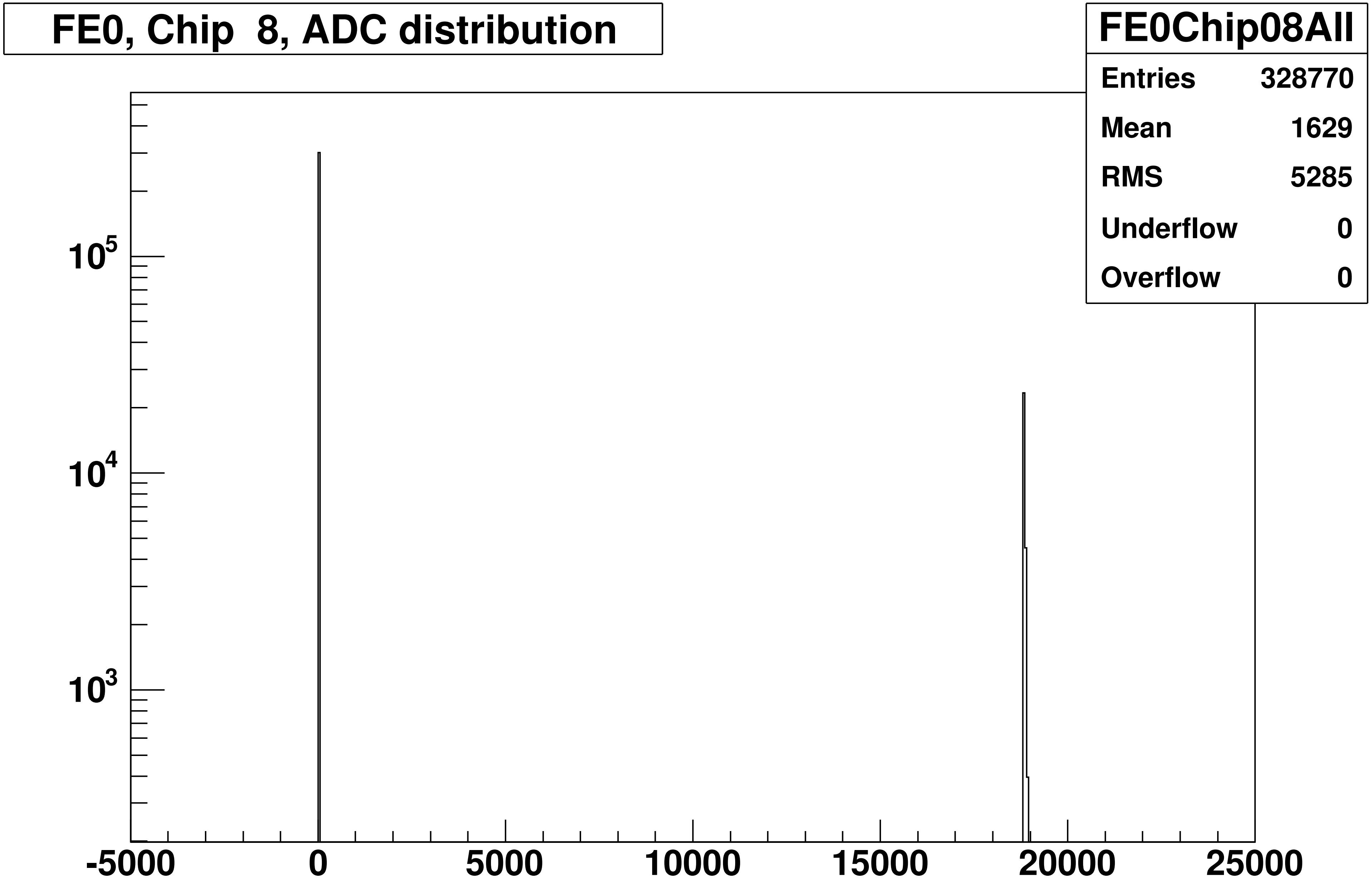
-100
-50
0
50
100
150
200


FE0, Chip 7, ADC distribution
FE0Chip07Sig
Entries 328770
Mean 1.883e+04
RMS 11.52
Underflow 3.01e+05
Overflow 0
10^4
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE0, Chip 8, ADC distribution
FE0Chip08All
Entries 328770
Mean 1629
RMS 5285
Underflow 0
Overflow 0
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10^4
10^3
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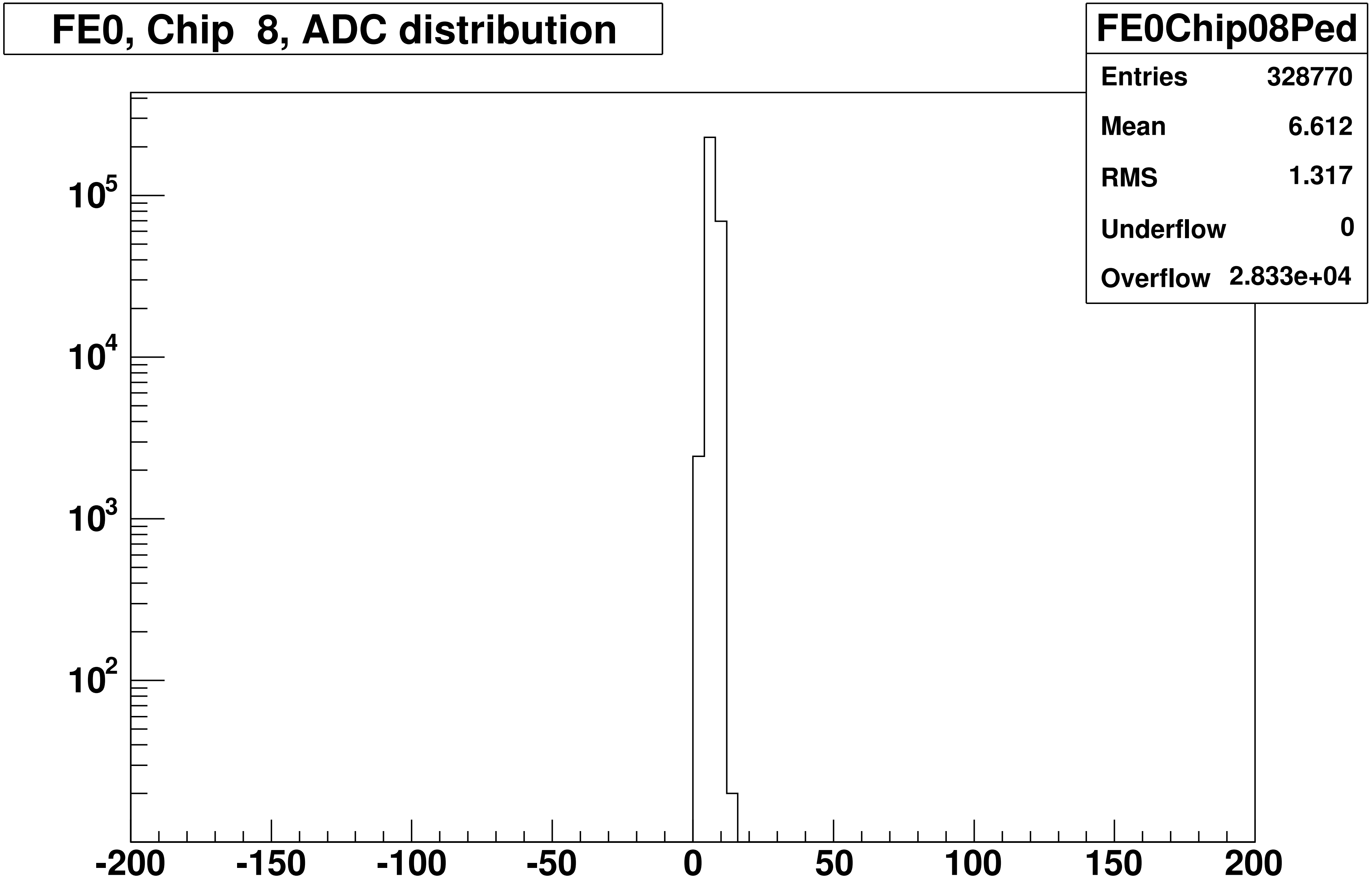
0
5000
10000
15000
20000
25000



FE0, Chip 8, ADC distribution
FE0Chip08Ped
Entries 328770
Mean 6.612
RMS 1.317
Underflow 0
Overflow 2.833e+04
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10^4
10^3
10^2
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-100
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150
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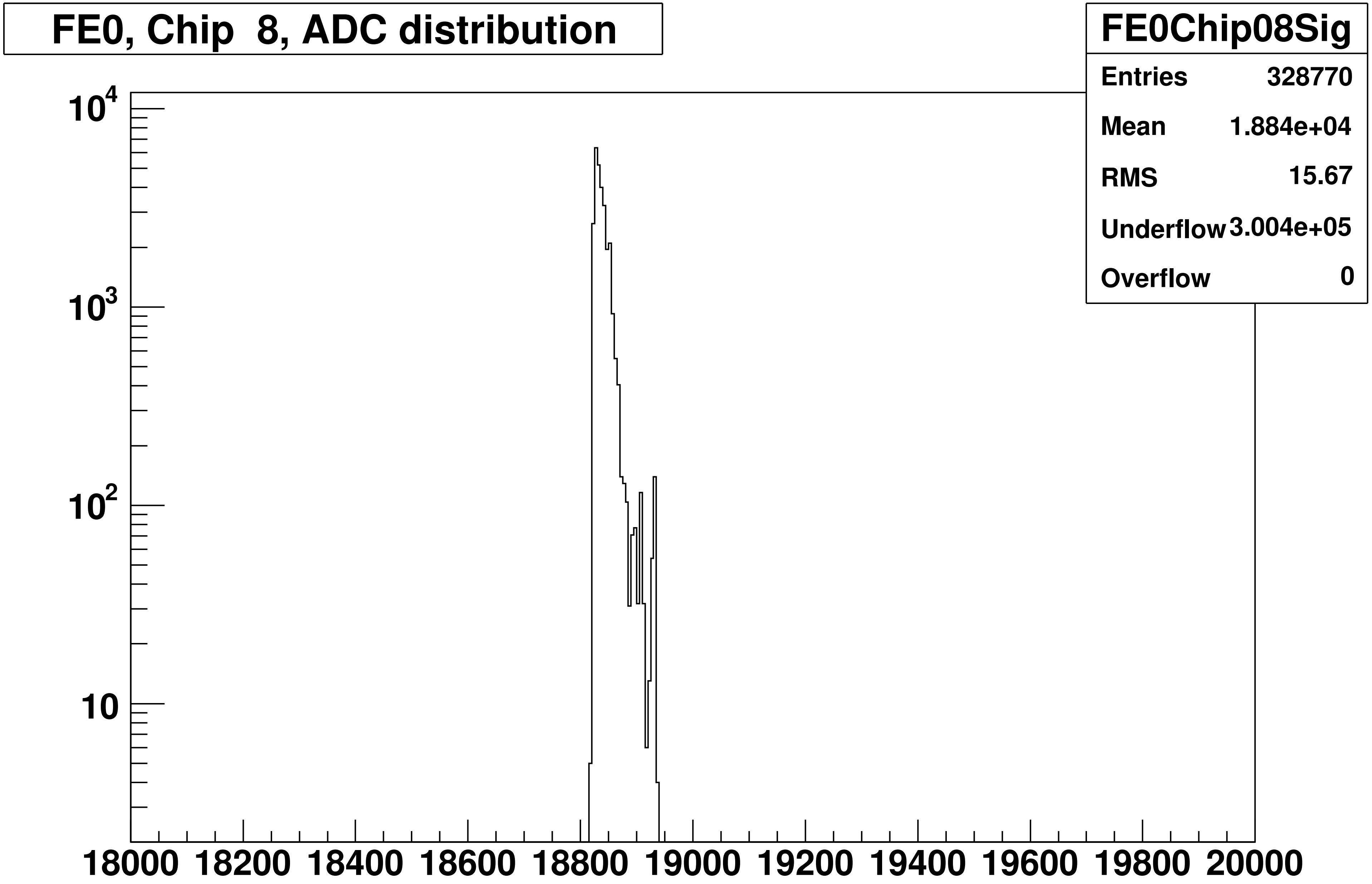
FE0, Chip 8, ADC distribution
FE0Chip08Sig
Entries 328770
Mean 1.884e+04
RMS 15.67
Underflow 3.004e+05
Overflow 0
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10^3
10^2
10
18000
18200
18400
18600
18800
19000
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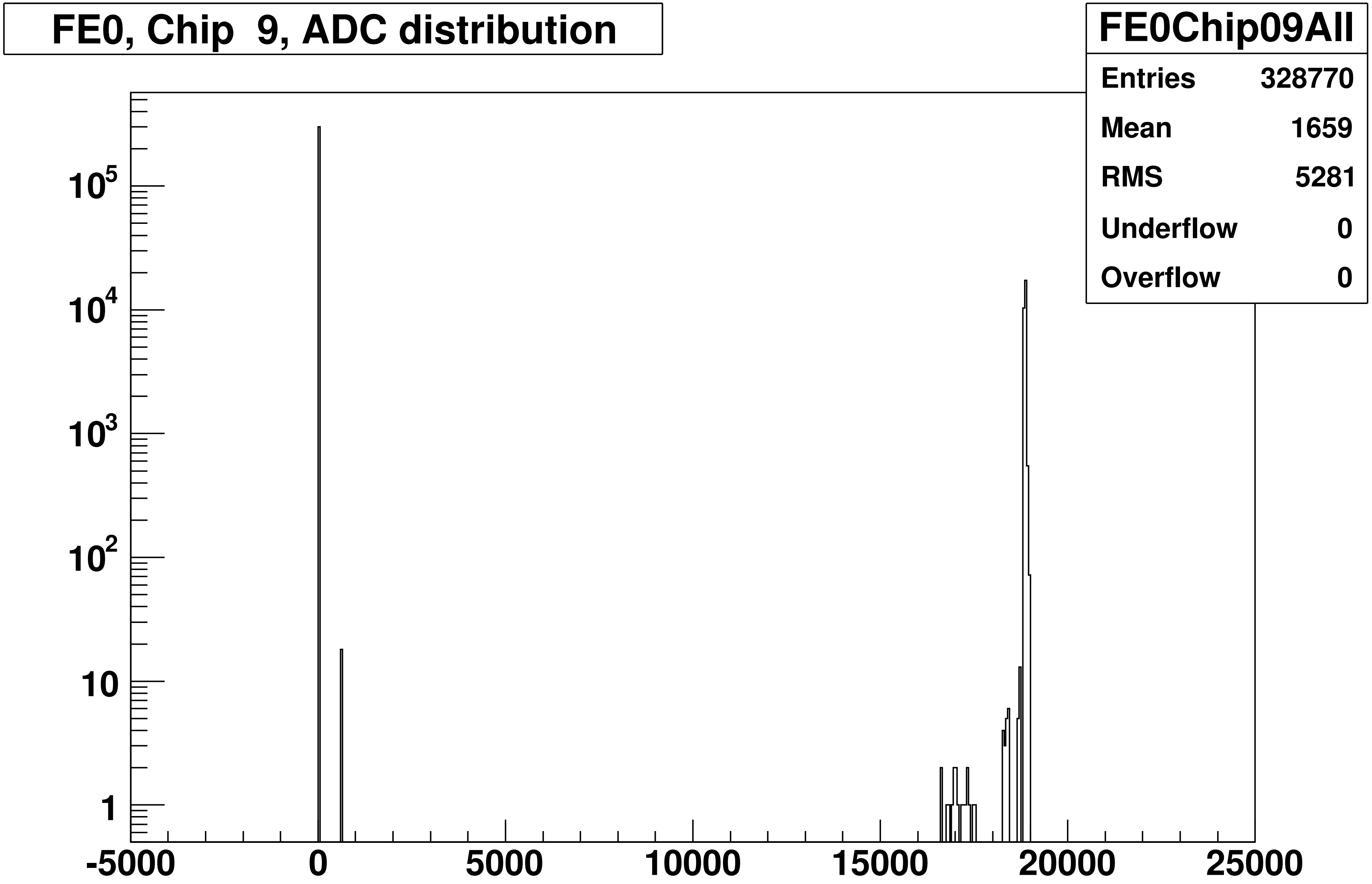
19600
19800
20000


FE0, Chip 9, ADC distribution
FE0Chip09All
Entries 328770
Mean 1659
RMS 5281
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
1
-5000
0
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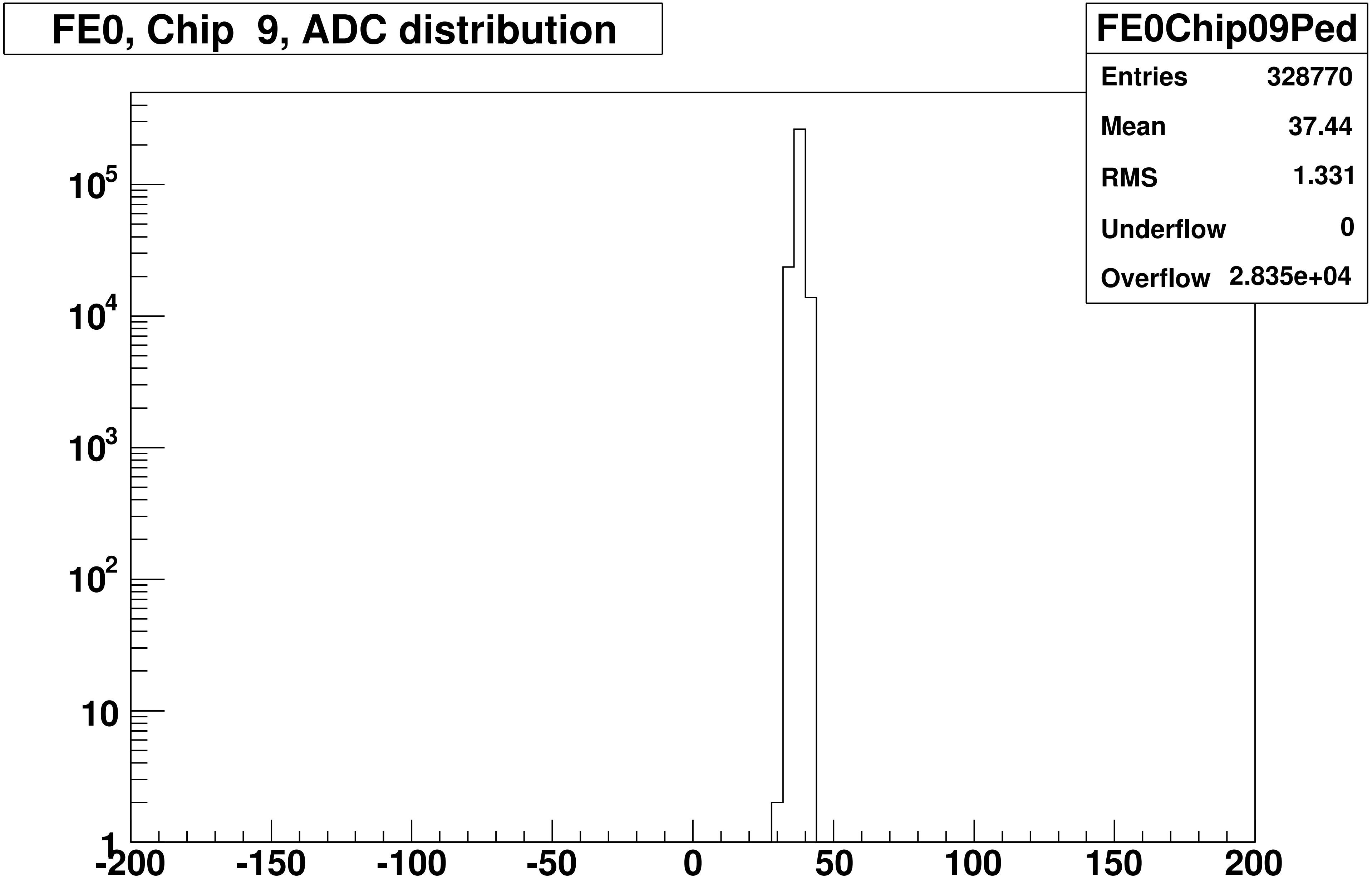
10000
15000
20000
25000


FE0, Chip 9, ADC distribution
FE0Chip09Ped
Entries 328770
Mean 37.44
RMS 1.331
Underflow 0
Overflow 2.835e+04
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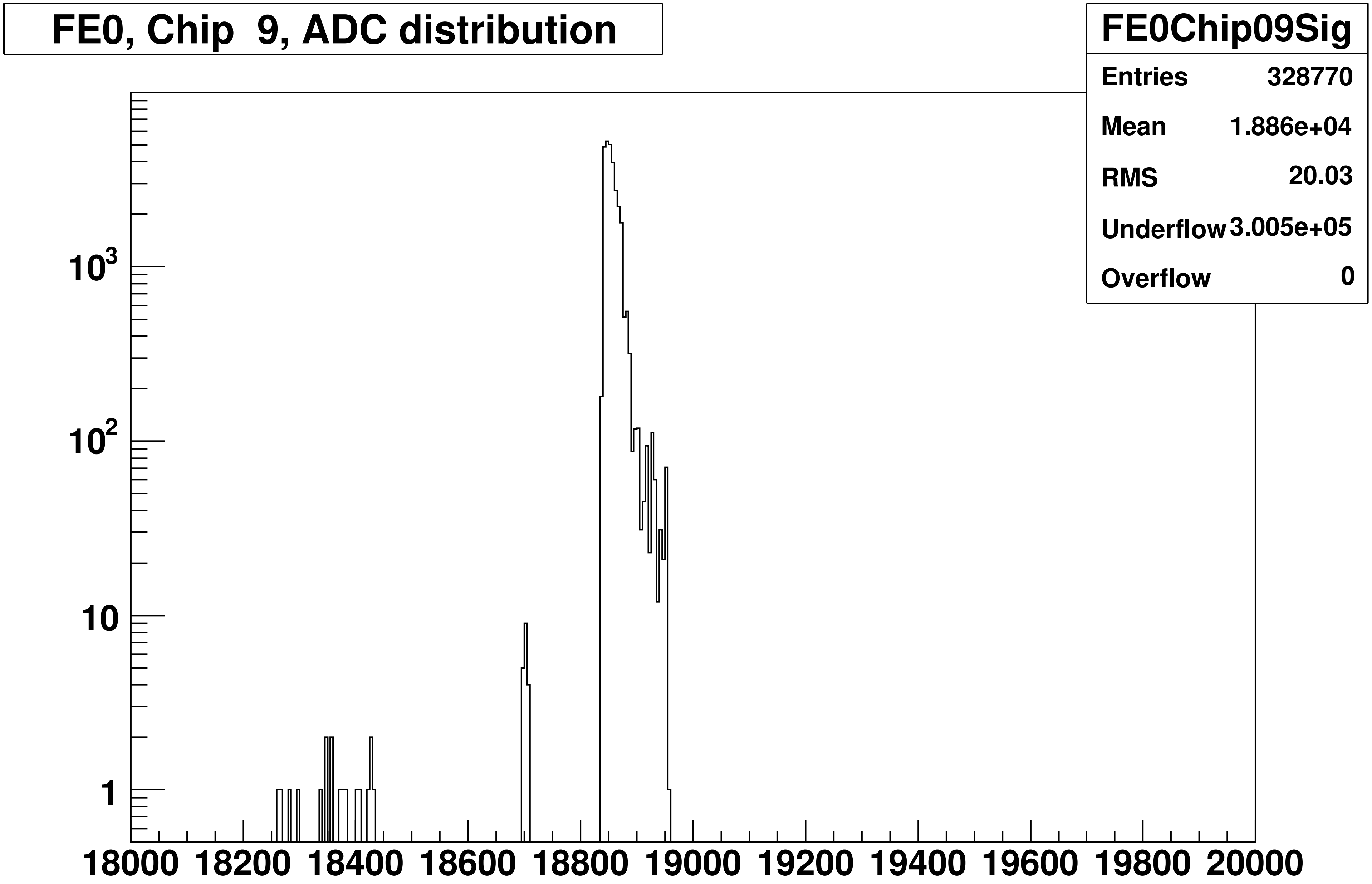
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
200


FE0, Chip 9, ADC distribution
FE0Chip09Sig
Entries 328770
Mean 1.886e+04
RMS 20.03
Underflow 3.005e+05
Overflow 0
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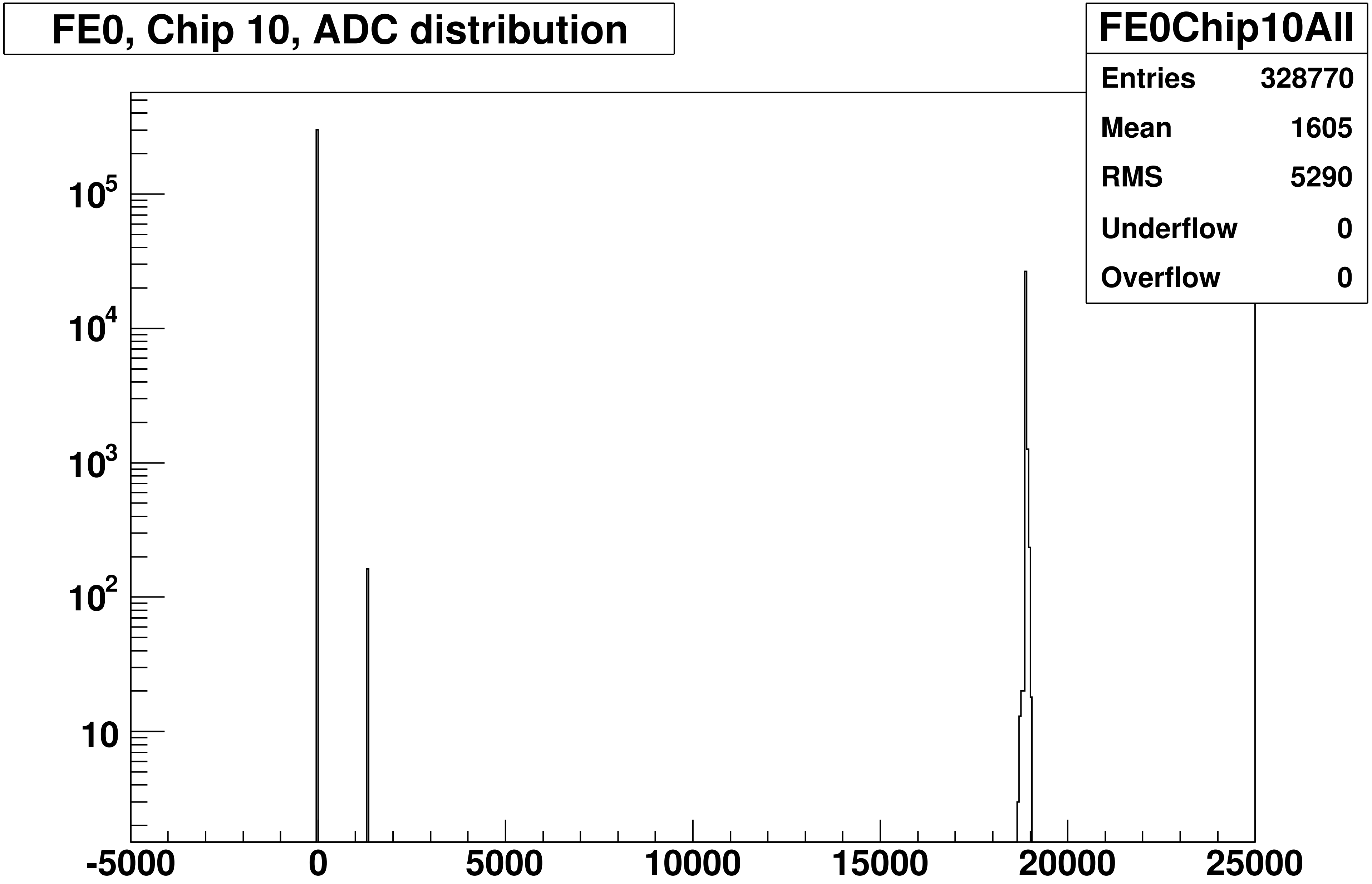
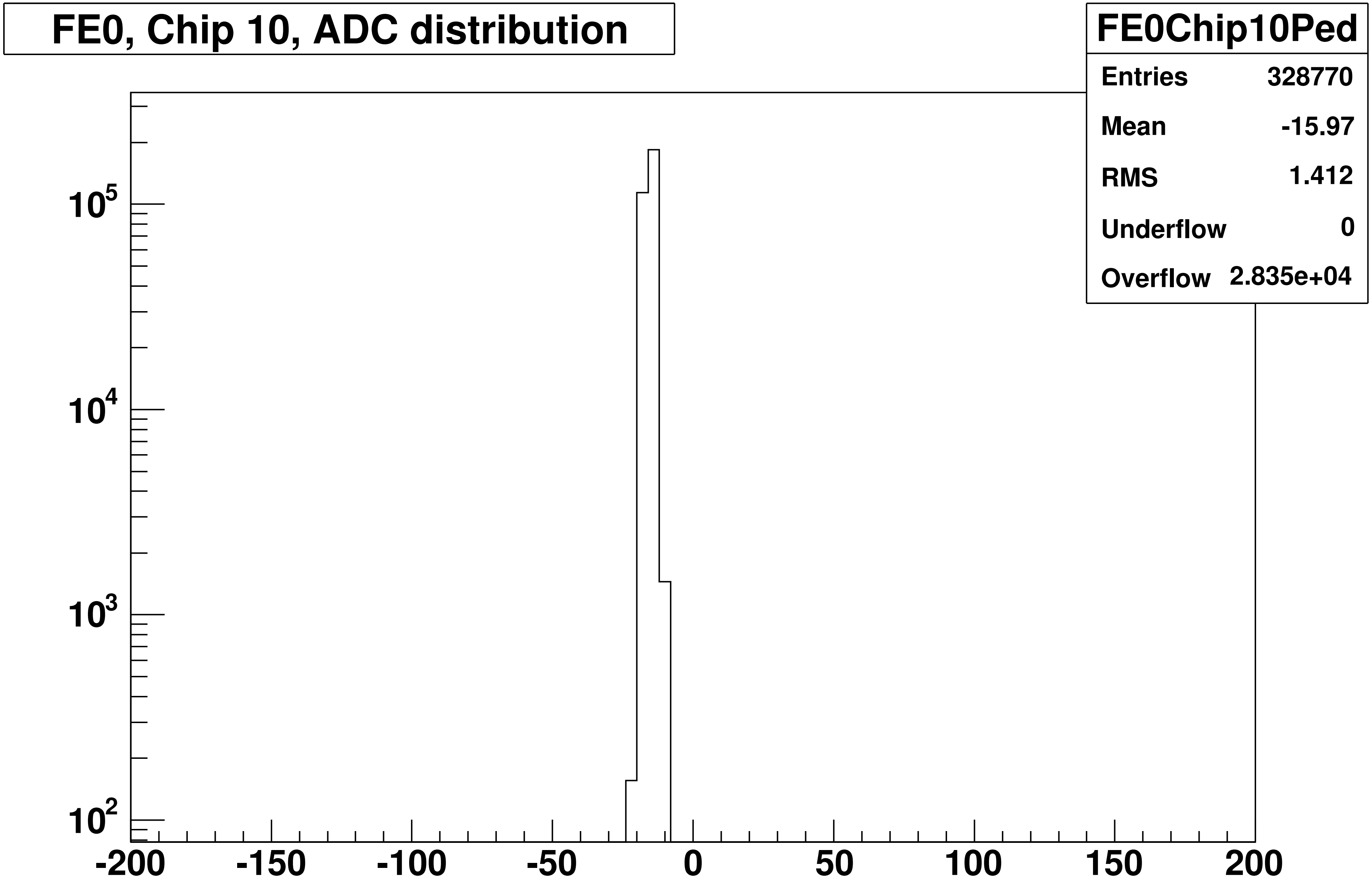
19400
19600
19800
20000


FE0, Chip 10, ADC distribution
FE0Chip10All
Entries 328770
Mean 1605
RMS 5290
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000



FE0, Chip 10, ADC distribution
FE0Chip10Ped
Entries 328770
Mean -15.97
RMS 1.412
Underflow 0
Overflow 2.835e+04
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10^4
10^3
10^2
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-100
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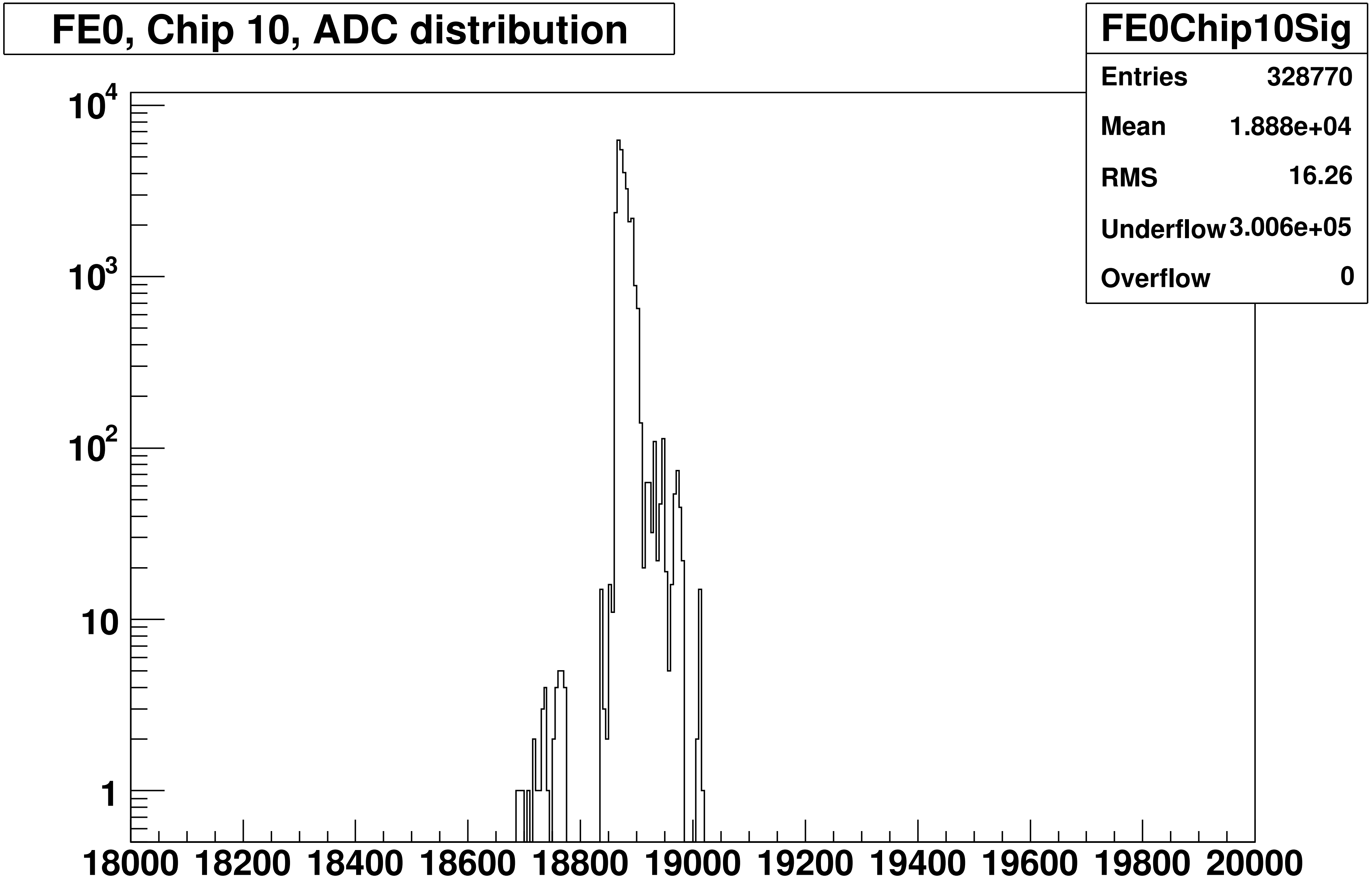
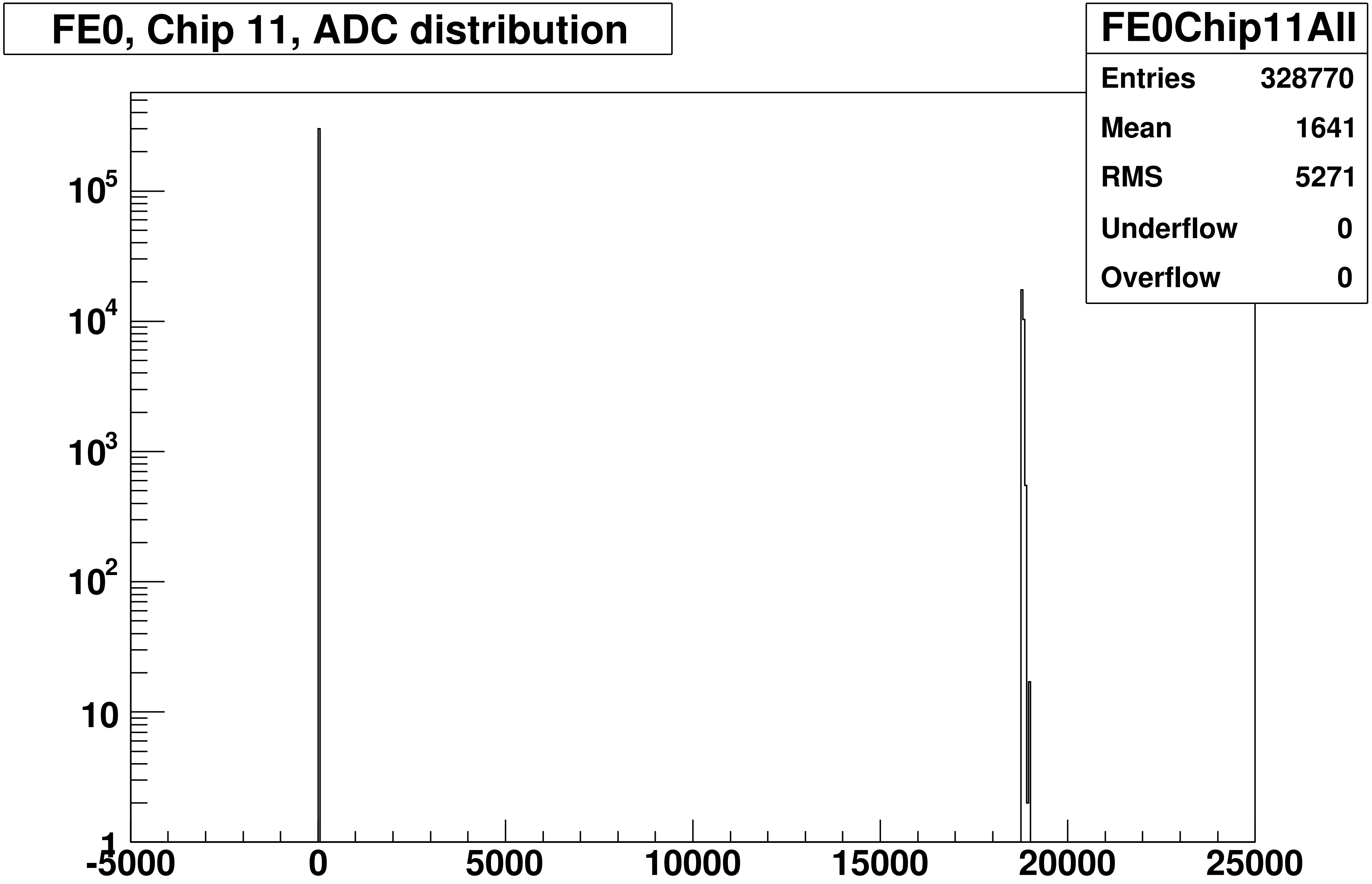
0
50
100
150
200



FE0, Chip 10, ADC distribution
FE0Chip10Sig
Entries 328770
Mean 1.888e+04
RMS 16.26
Underflow 3.006e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE0, Chip 11, ADC distribution
FE0Chip11All
Entries 328770
Mean 1641
RMS 5271
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
1
-5000
0
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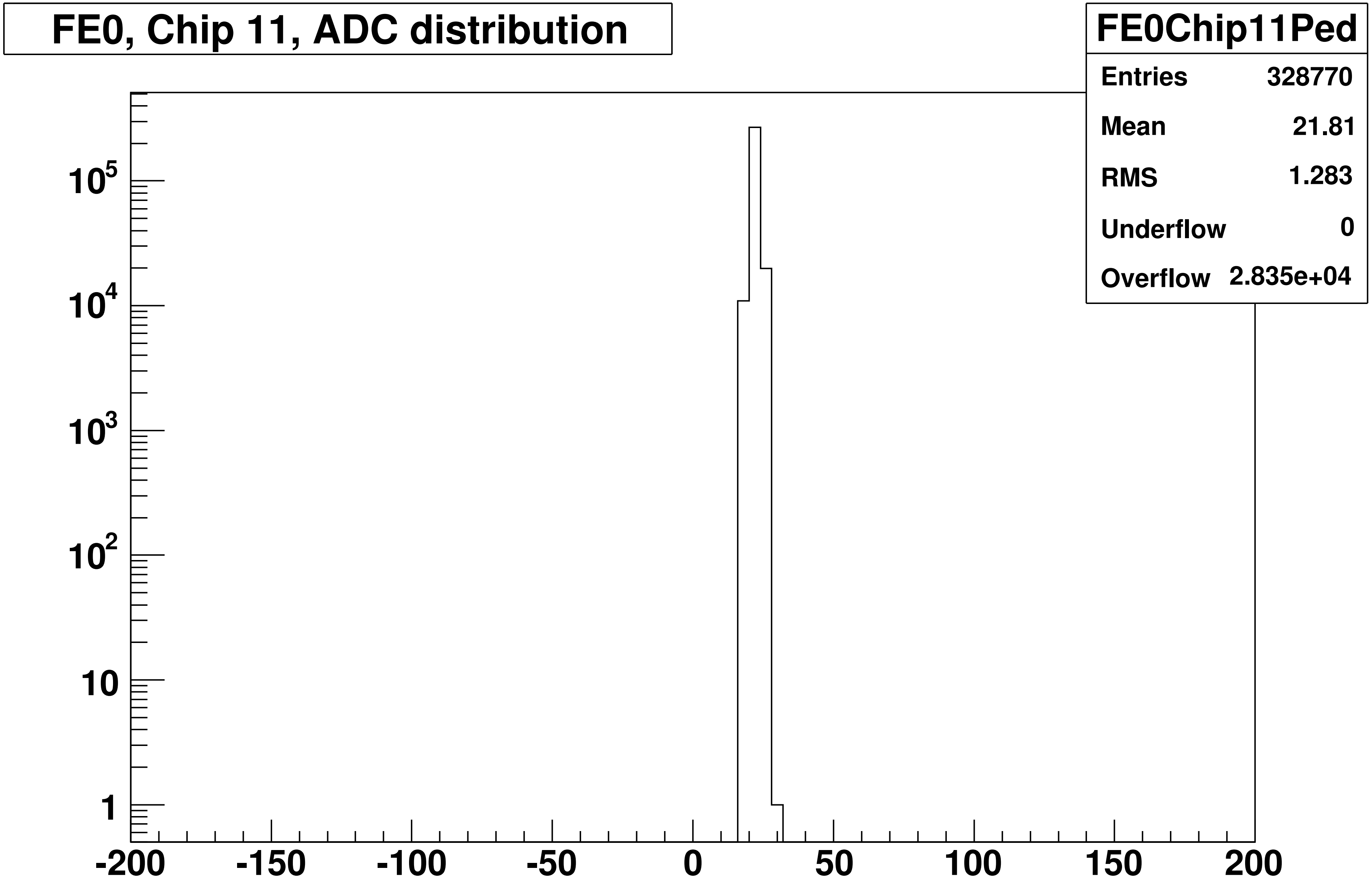
10000
15000
20000
25000


FE0, Chip 11, ADC distribution
FE0Chip11Ped
Entries 328770
Mean 21.81
RMS 1.283
Underflow 0
Overflow 2.835e+04
10^5
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10^3
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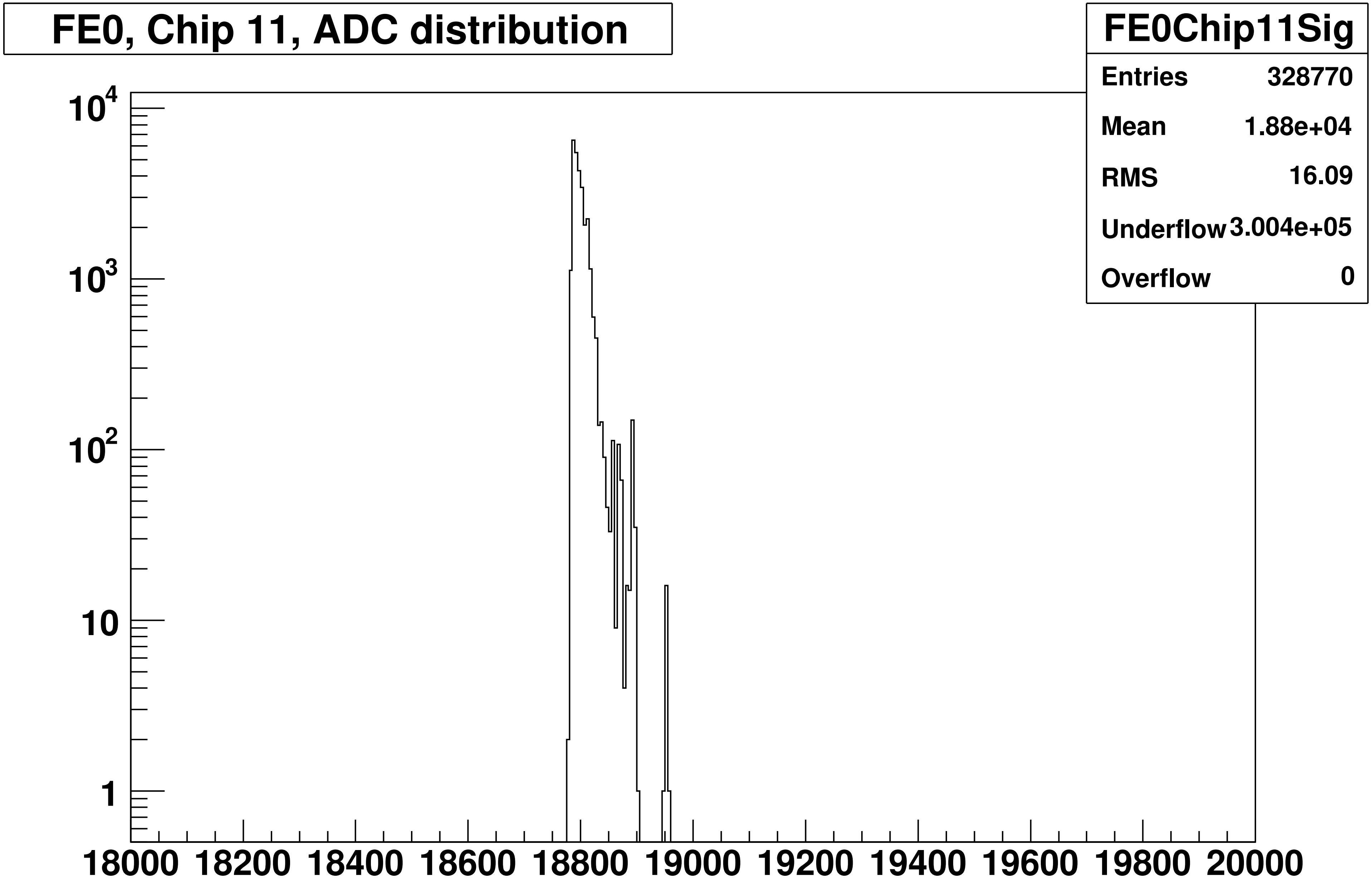
-200 -150 -100 -50 0 50 100 150 200



FE0, Chip 11, ADC distribution
FE0Chip11Sig
Entries 328770
Mean 1.88e+04
RMS 16.09
Underflow 3.004e+05
Overflow 0
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10^3
10^2
10
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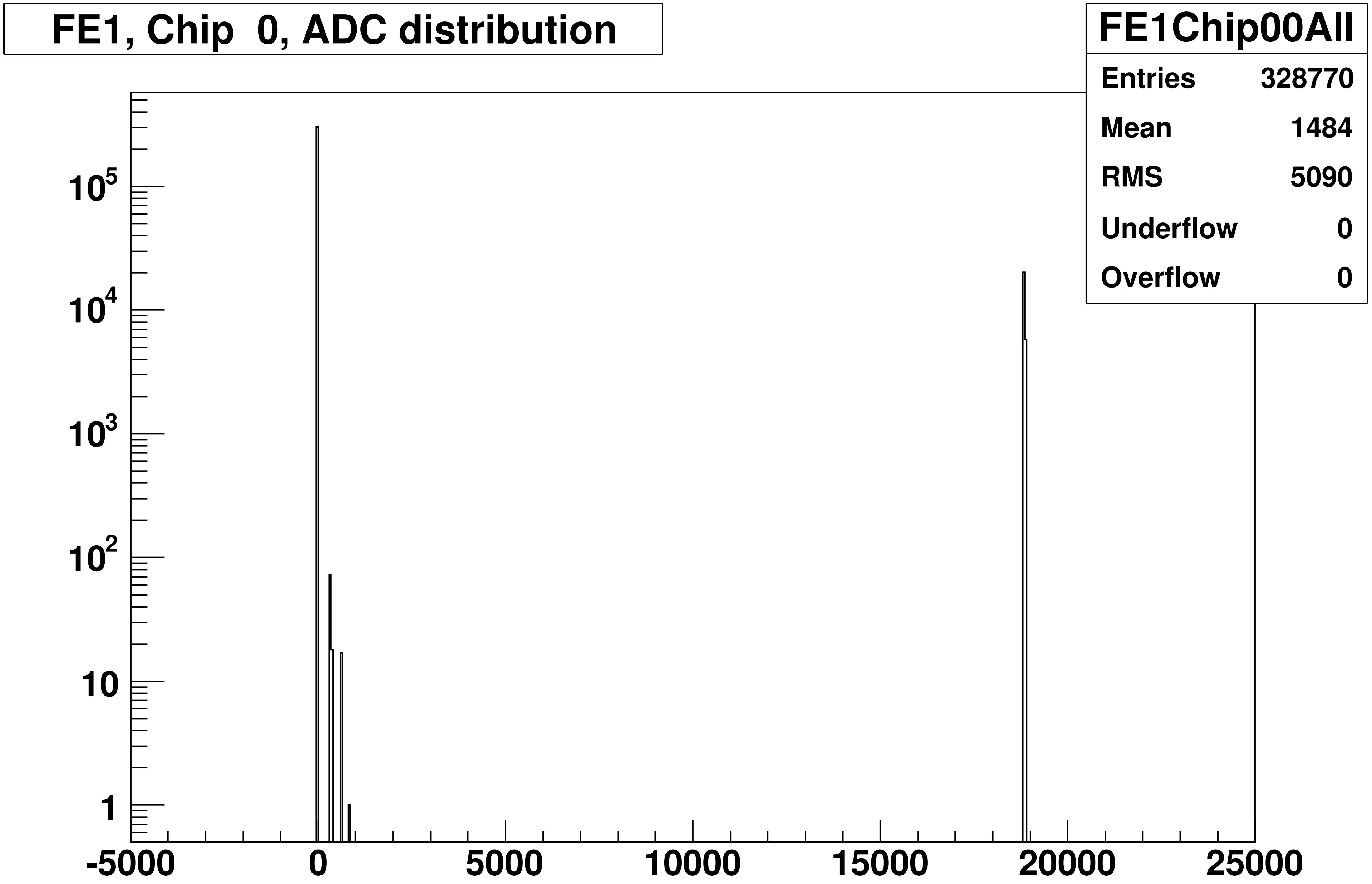
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE1, Chip 0, ADC distribution
FE1Chip00All
Entries 328770
Mean 1484
RMS 5090
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
1
-5000
0
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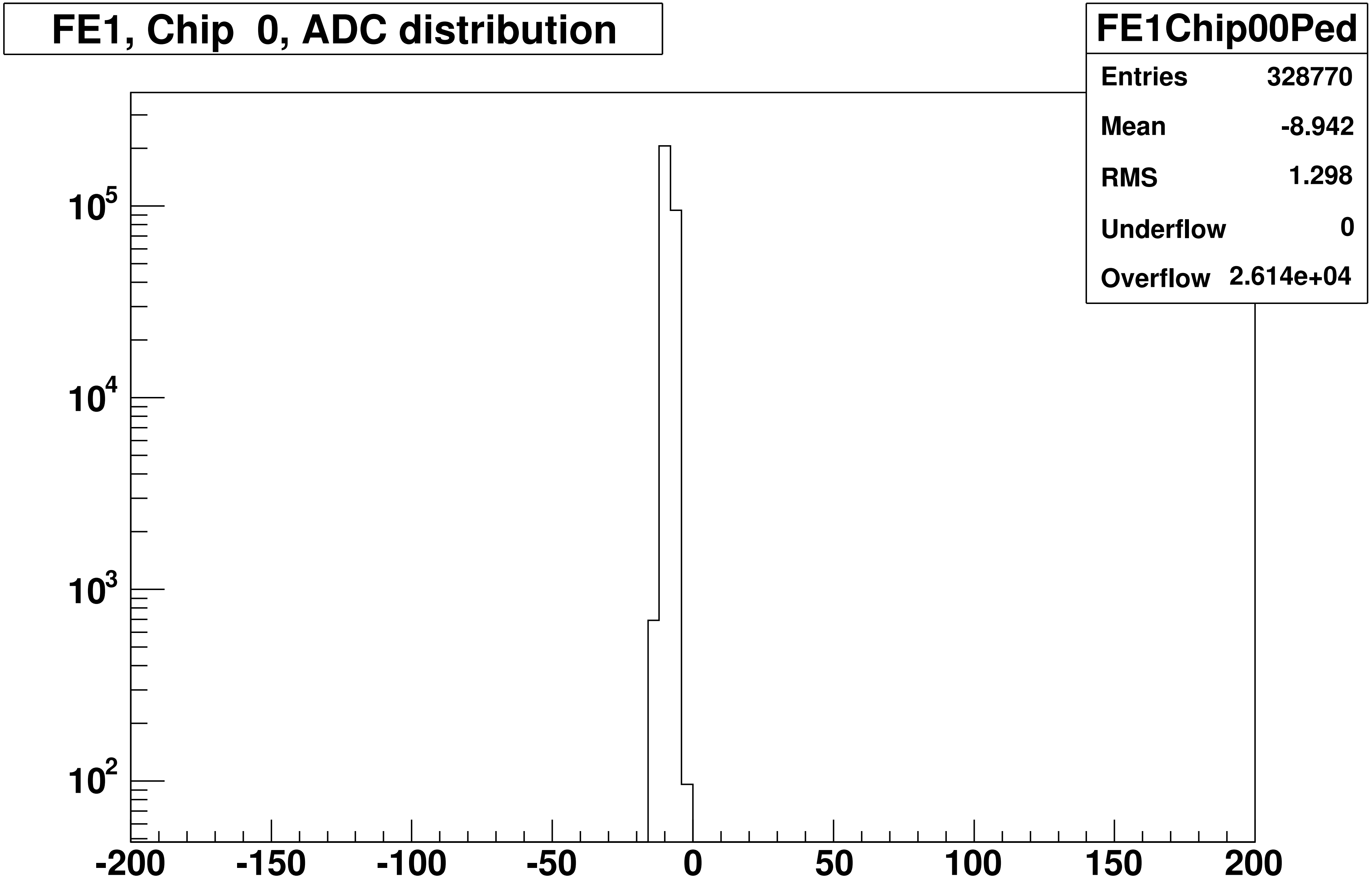
10000
15000
20000
25000



FE1, Chip 0, ADC distribution
FE1Chip00Ped
Entries 328770
Mean -8.942
RMS 1.298
Underflow 0
Overflow 2.614e+04
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10^4
10^3
10^2
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-100
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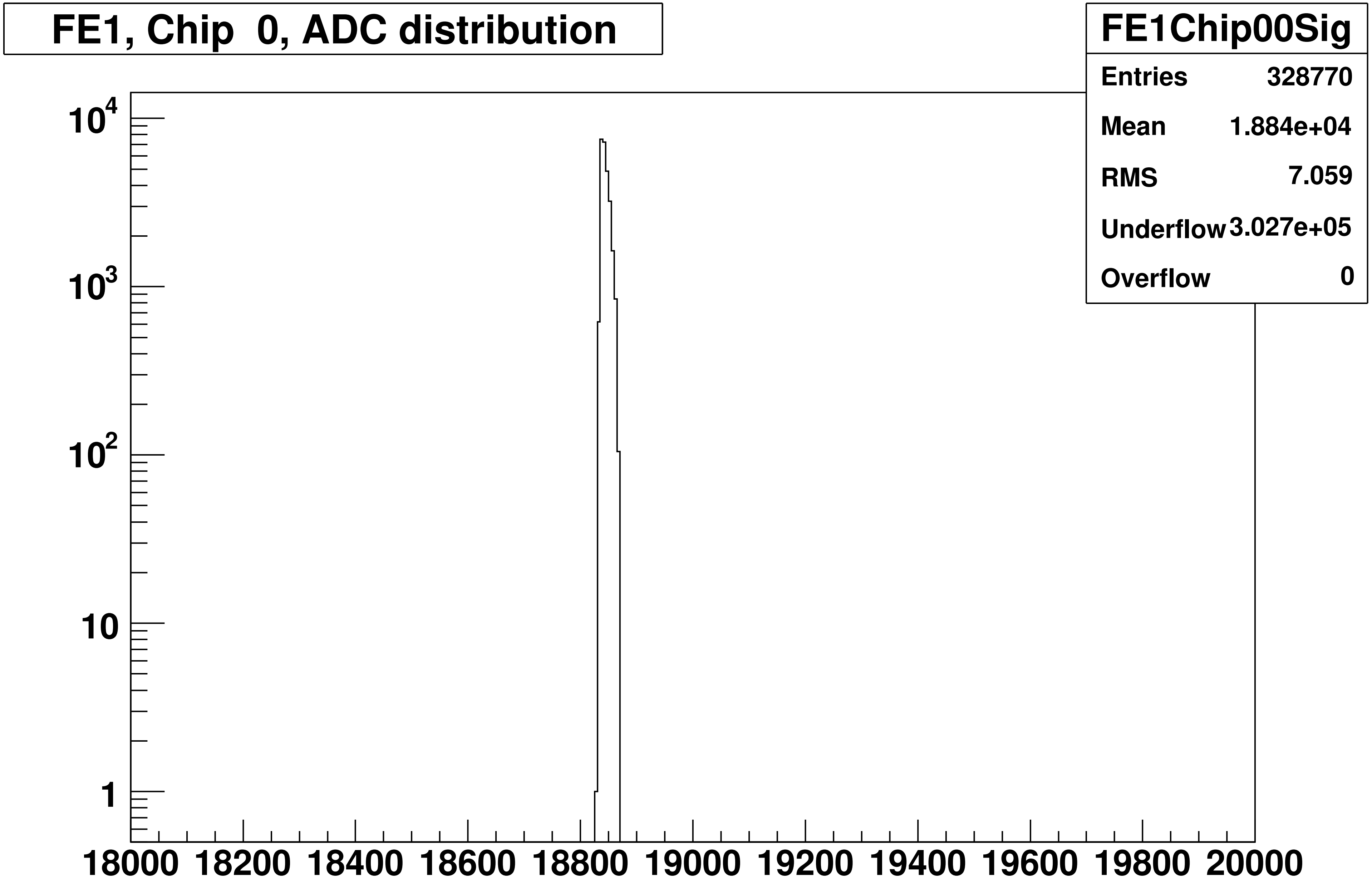
0
50
100
150
200


FE1, Chip 0, ADC distribution
FE1Chip00Sig
Entries 328770
Mean 1.884e+04
RMS 7.059
Underflow 3.027e+05
Overflow 0
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10^3
10^2
10
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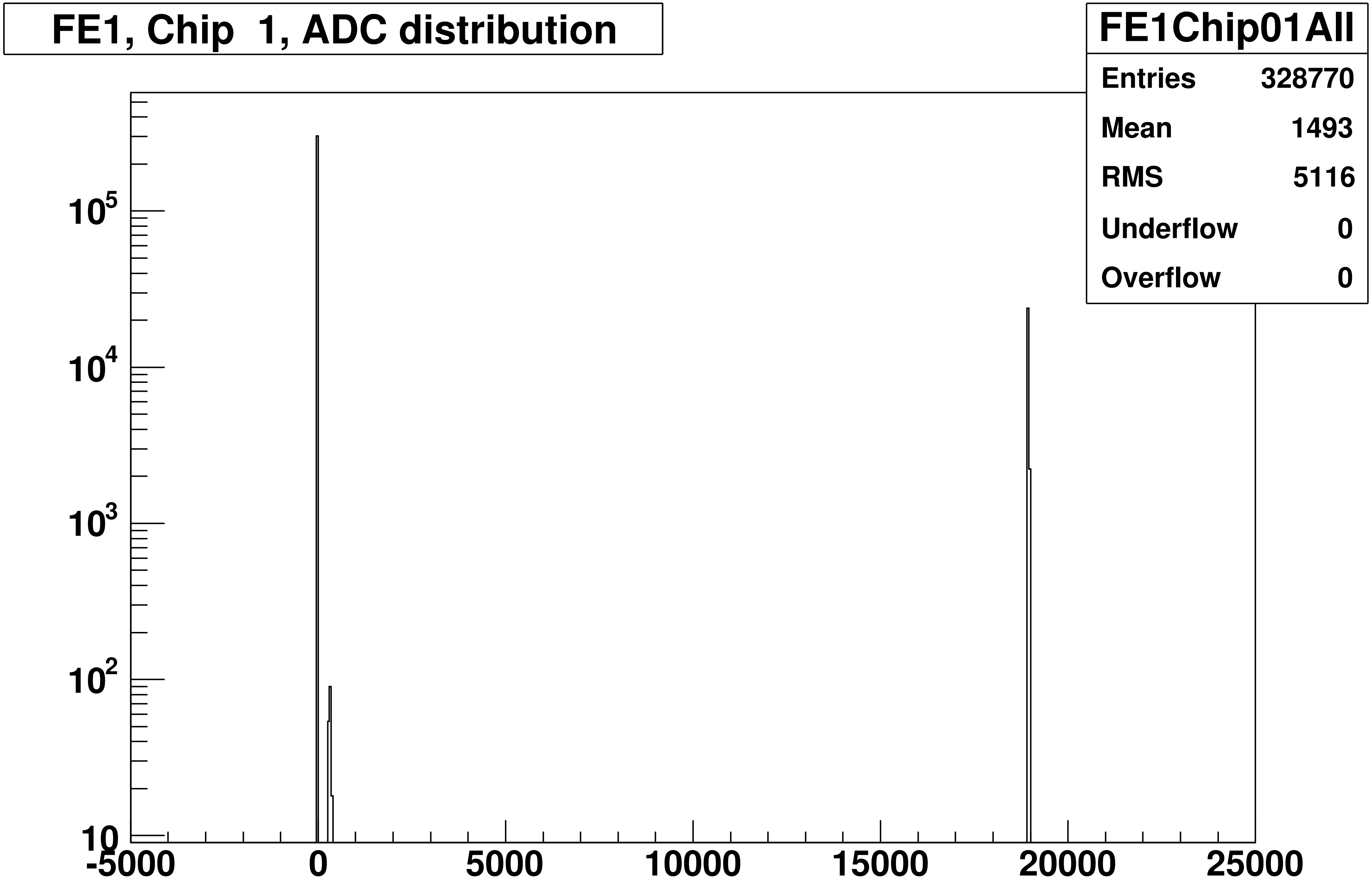
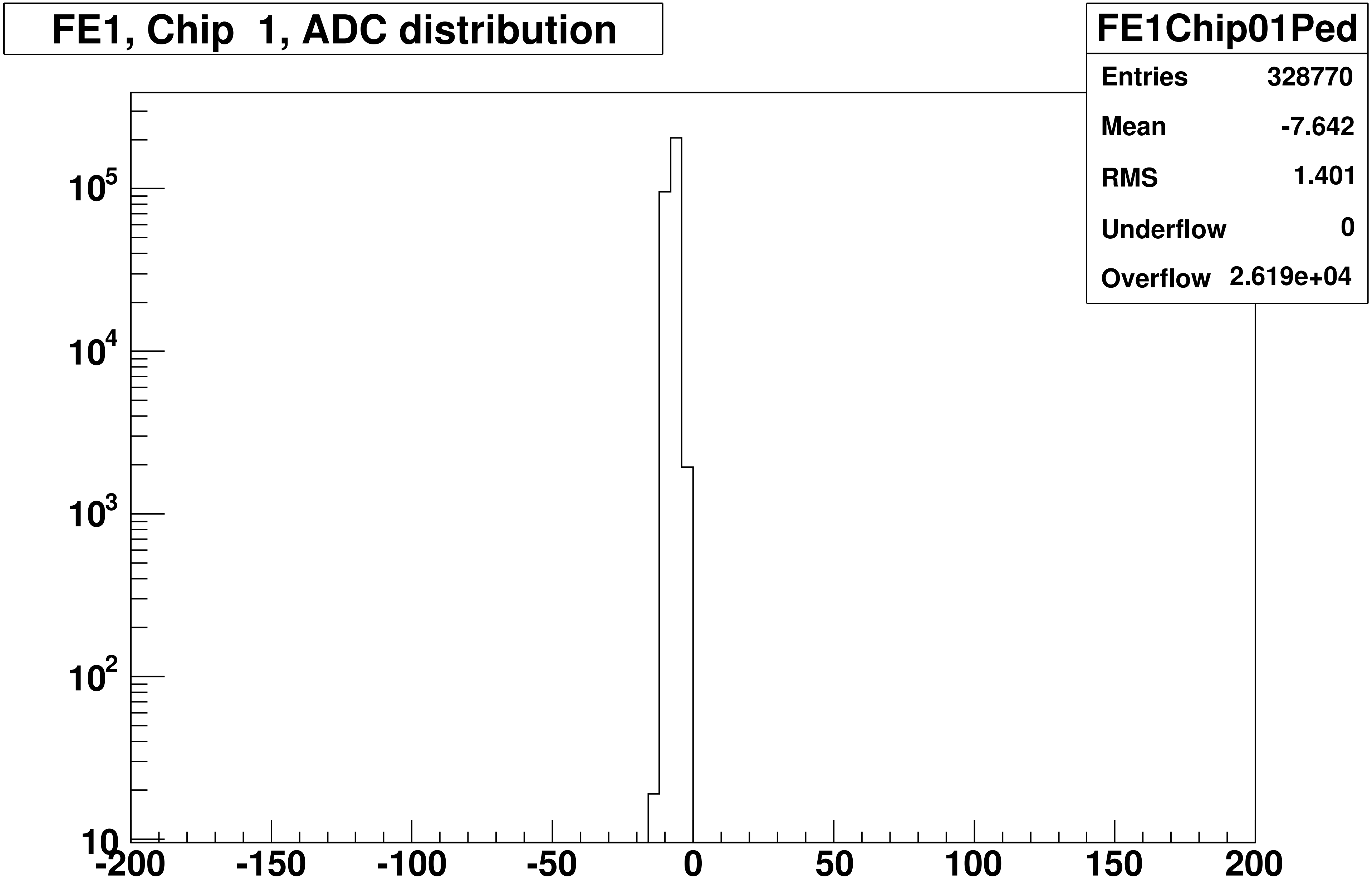
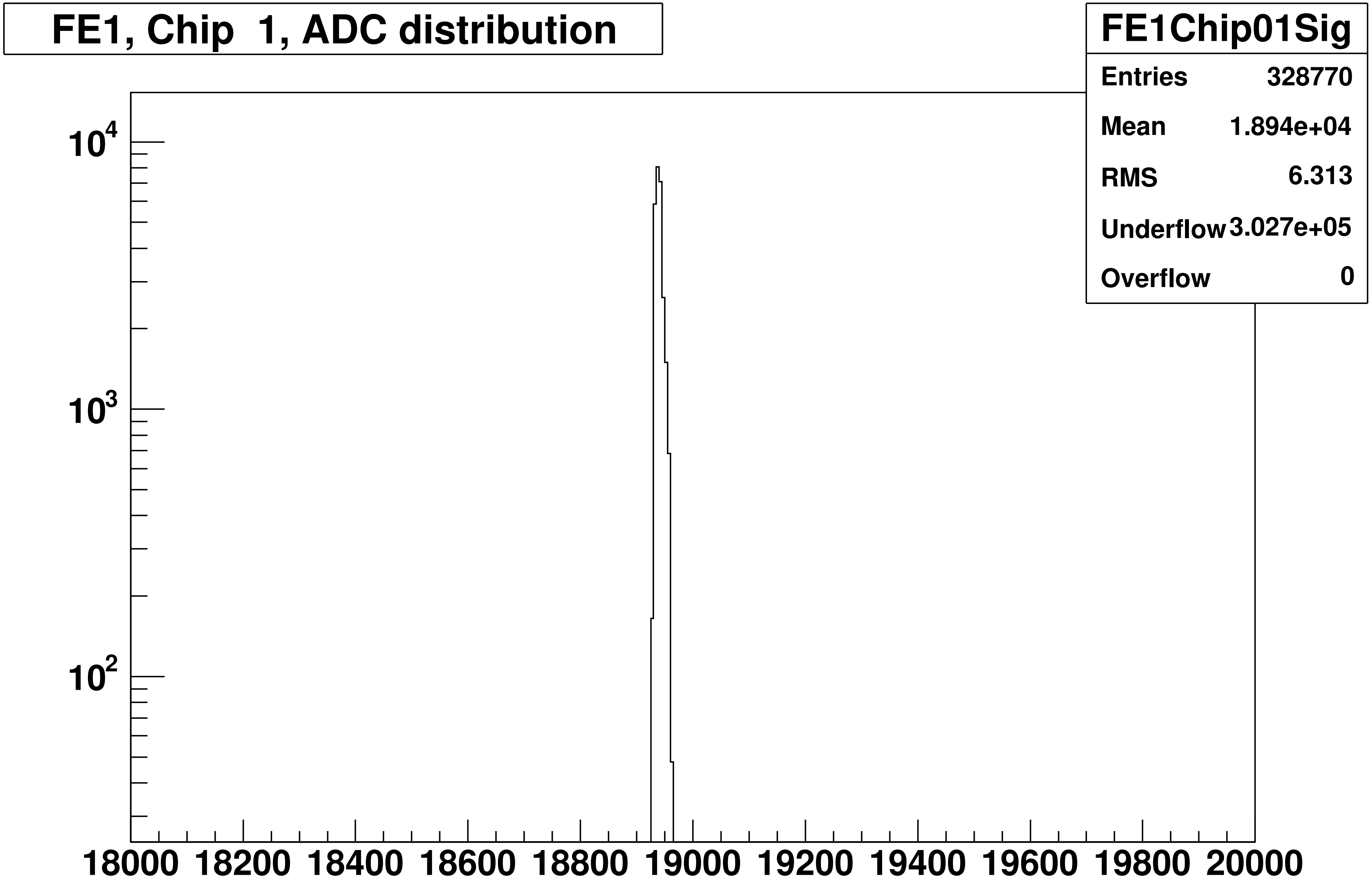
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000

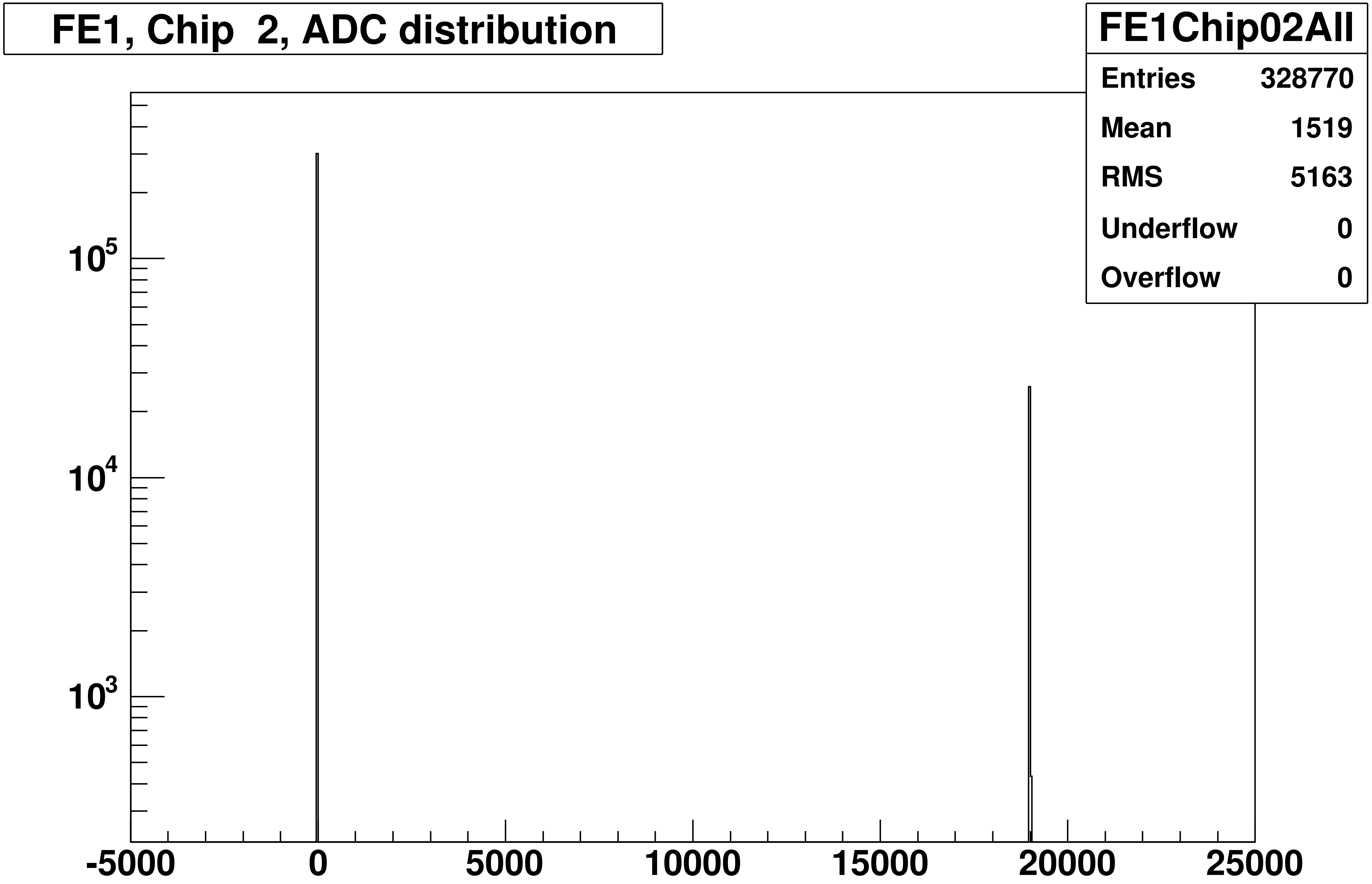


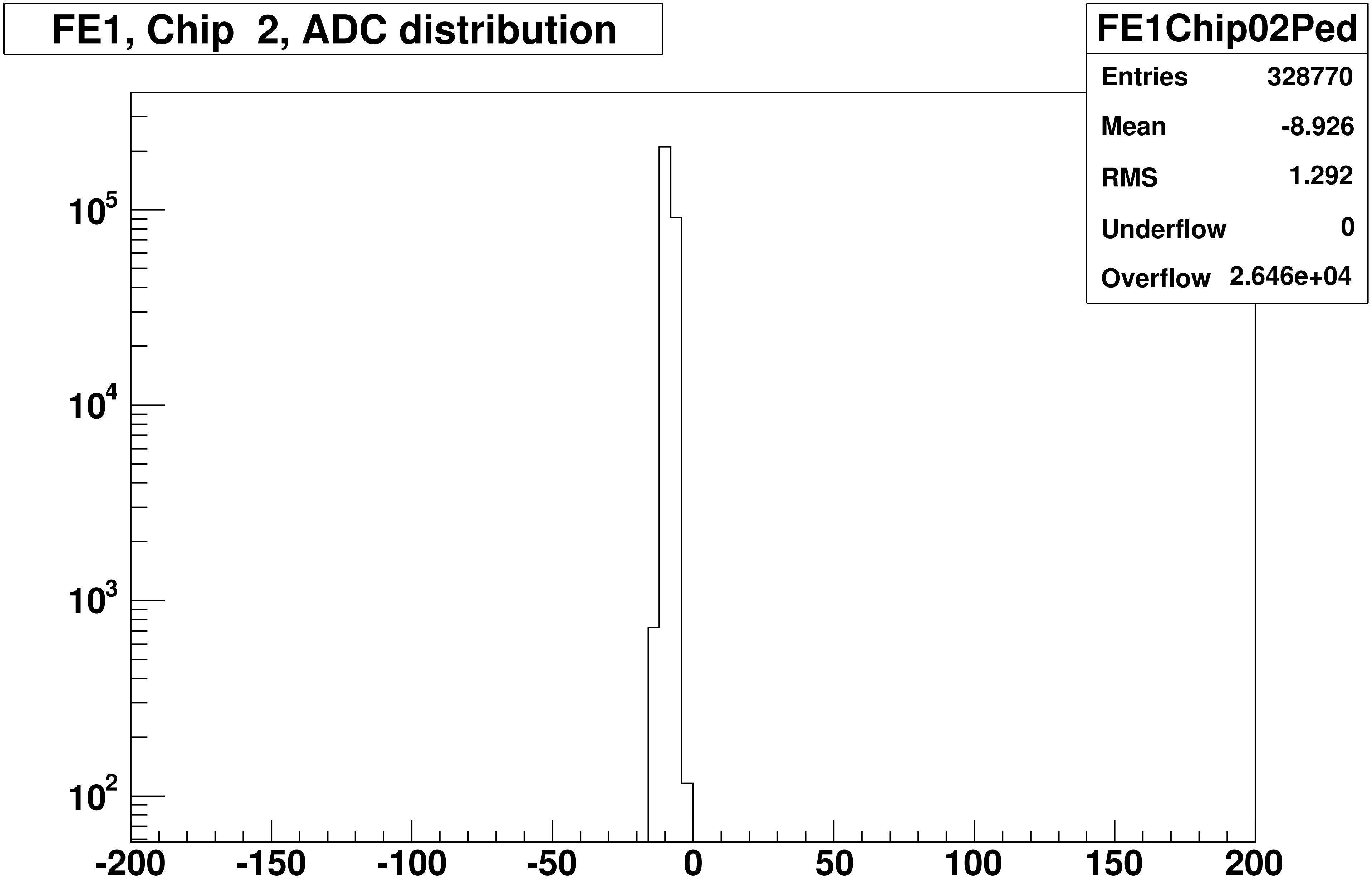
FE1, Chip 1, ADC distribution
FE1Chip01All
Entries 328770
Mean 1493
RMS 5116
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE1, Chip 1, ADC distribution
FE1Chip01Ped
Entries 328770
Mean -7.642
RMS 1.401
Underflow 0
Overflow 2.619e+04
10
10^2
10^3
10^4
10^5
-200
-150
-100
-50
0
50
100
150
200



FE1, Chip 1, ADC distribution
FE1Chip01Sig
Entries 328770
Mean 1.894e+04
RMS 6.313
Underflow 3.027e+05
Overflow 0
10^4
10^3
10^2
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE1, Chip 2, ADC distribution
FE1Chip02All
Entries 328770
Mean 1519
RMS 5163
Underflow 0
Overflow 0
10^5
10^4
10^3
-5000
0
5000
10000
15000
20000
25000


FE1, Chip 2, ADC distribution
FE1Chip02Ped
Entries 328770
Mean -8.926
RMS 1.292
Underflow 0
Overflow 2.646e+04
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10^4
10^3
10^2
-200
-150
-100
-50
0
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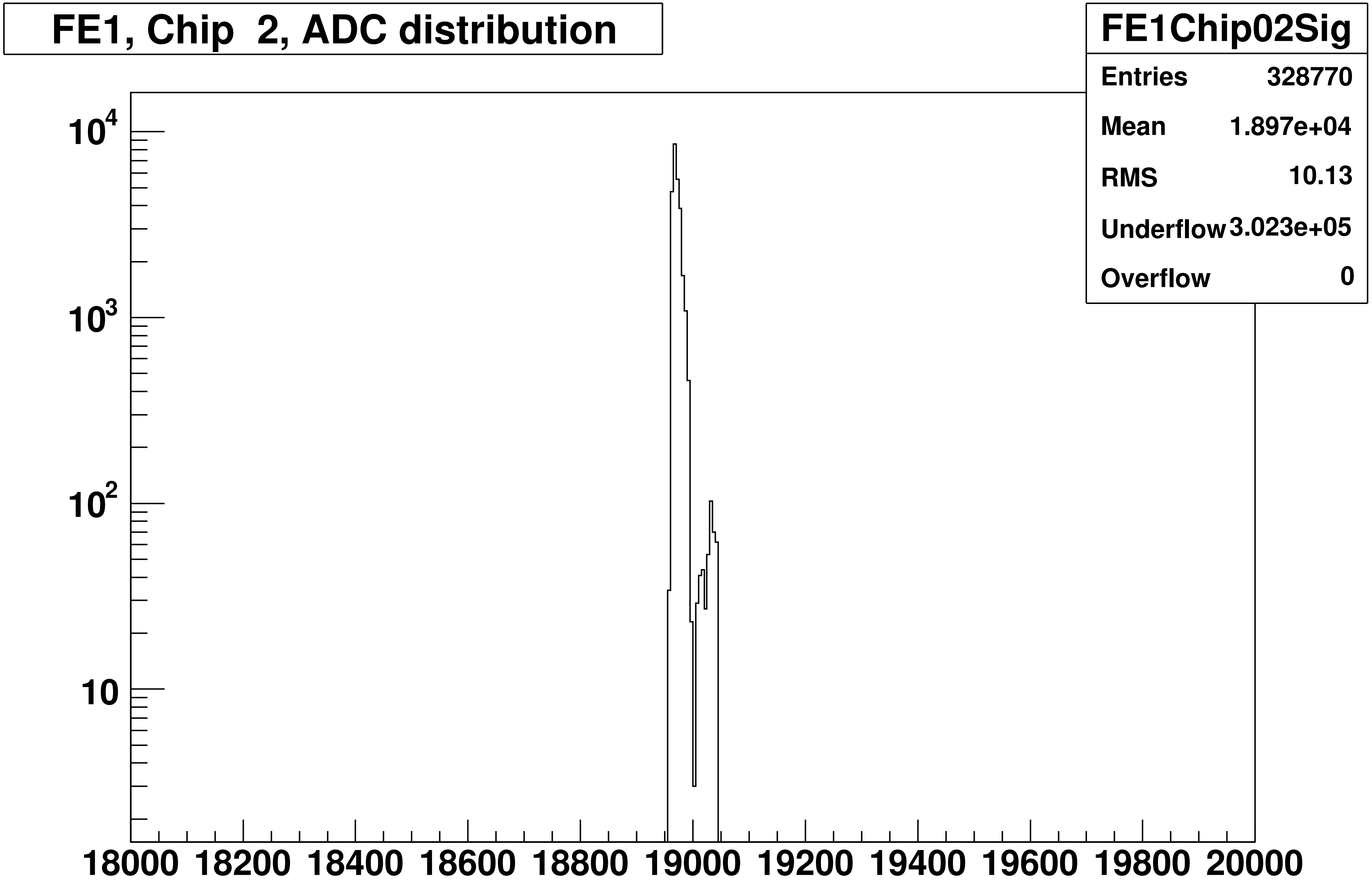
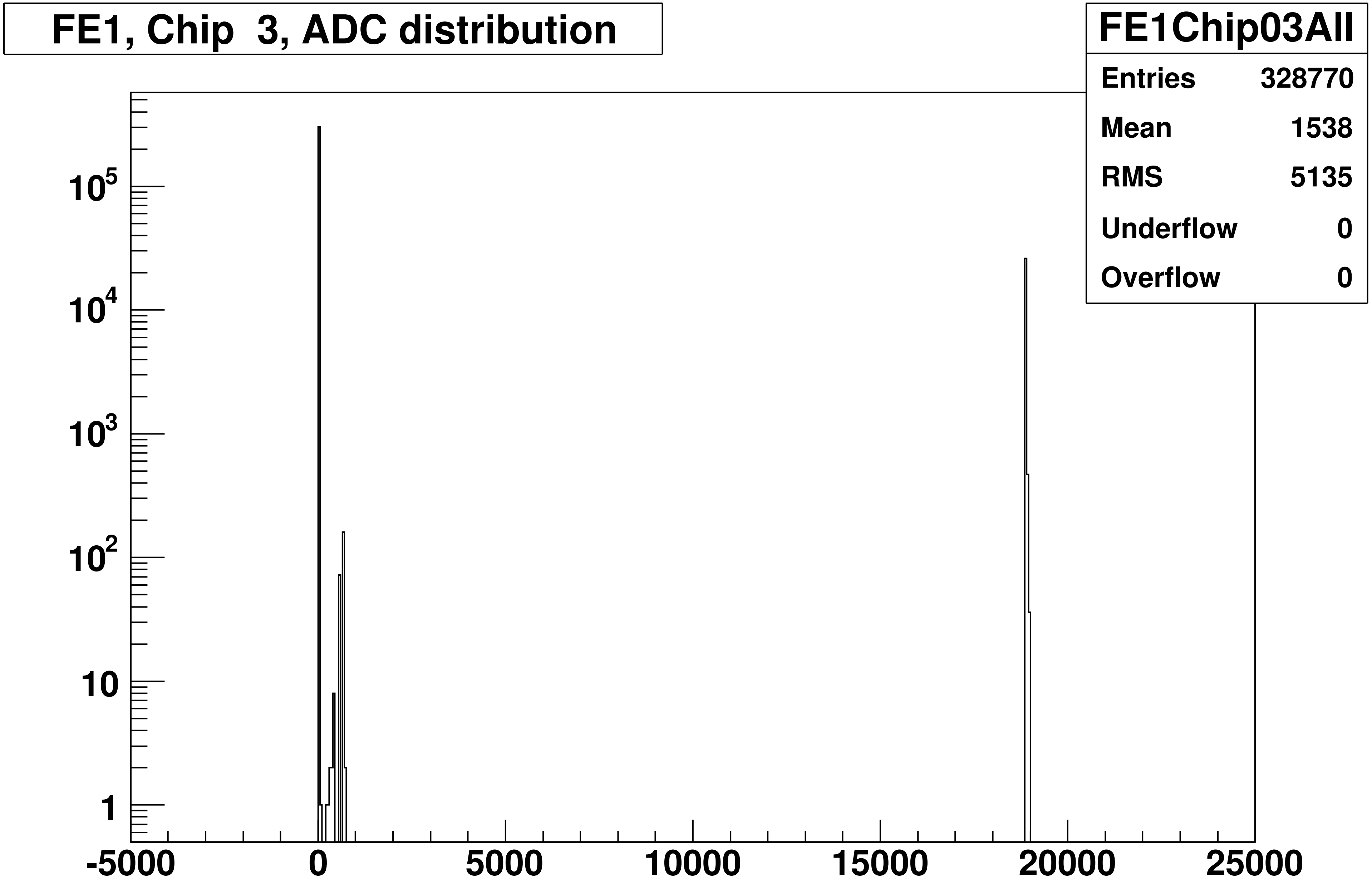
100
150
200



FE1, Chip 2, ADC distribution
FE1Chip02Sig
Entries 328770
Mean 1.897e+04
RMS 10.13
Underflow 3.023e+05
Overflow 0
10^4
10^3
10^2
10
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000


FE1, Chip 3, ADC distribution
FE1Chip03All
Entries 328770
Mean 1538
RMS 5135
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
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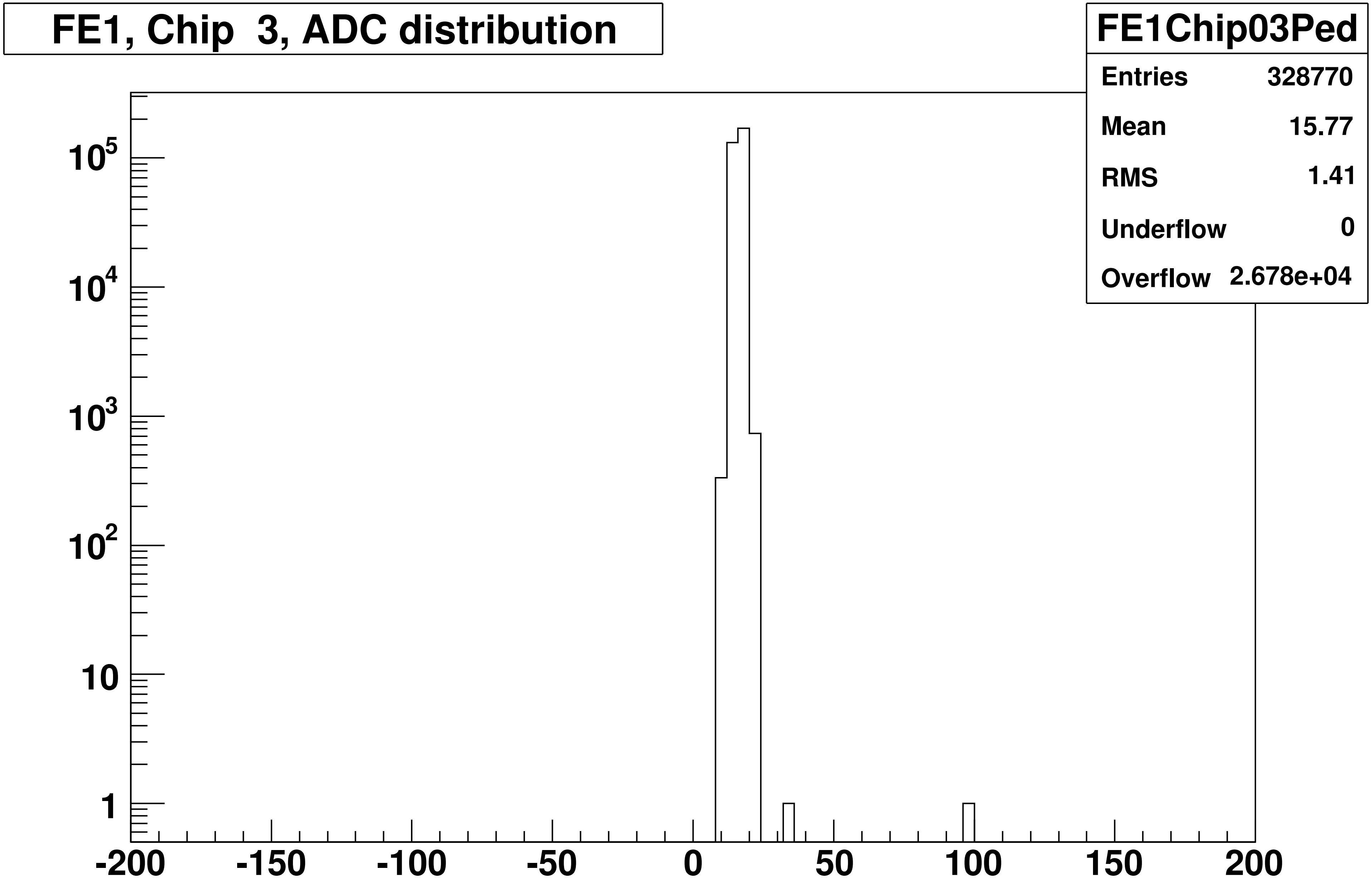
5000
10000
15000
20000
25000



FE1, Chip 3, ADC distribution
FE1Chip03Ped
Entries 328770
Mean 15.77
RMS 1.41
Underflow 0
Overflow 2.678e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
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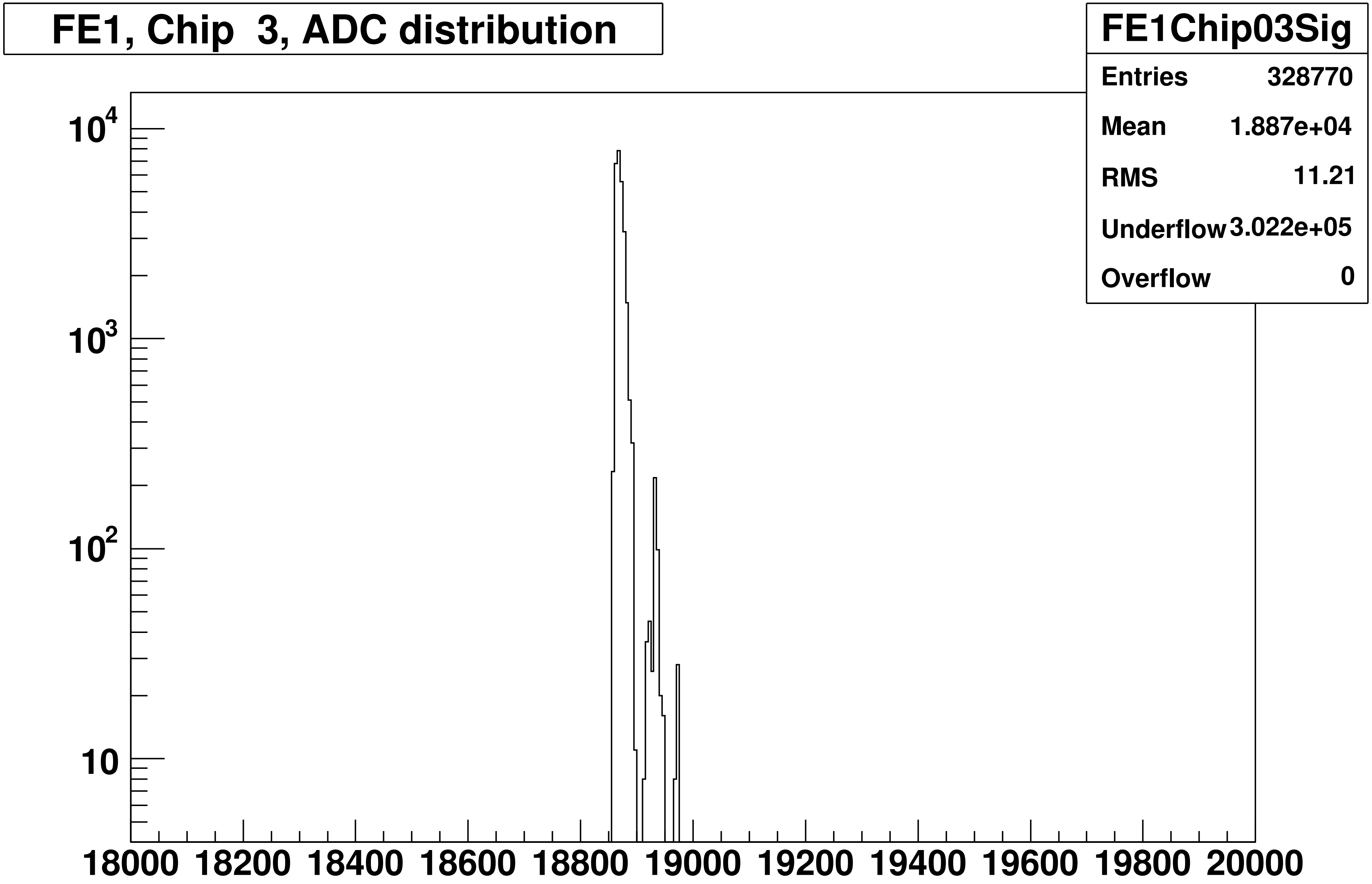
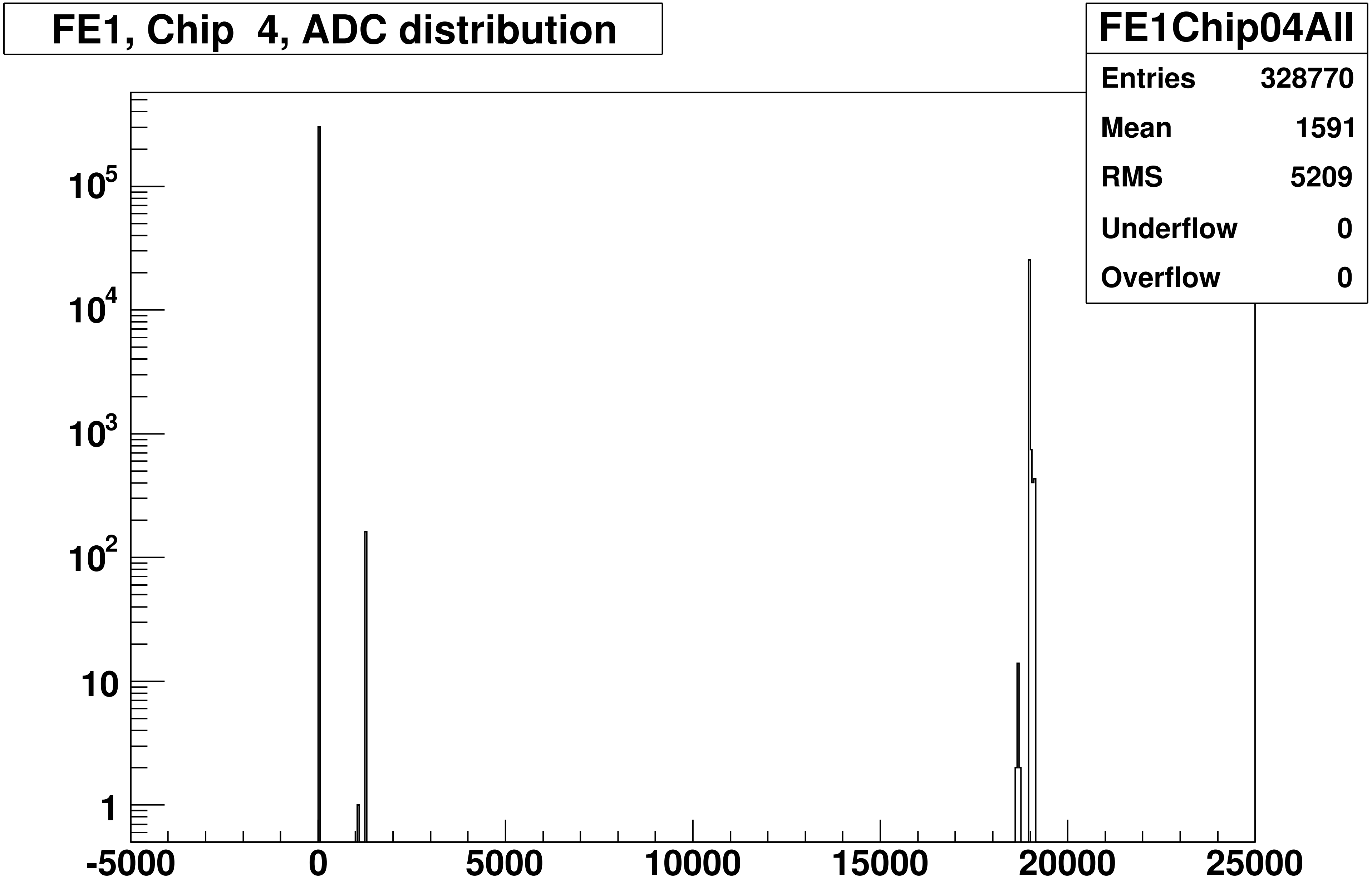
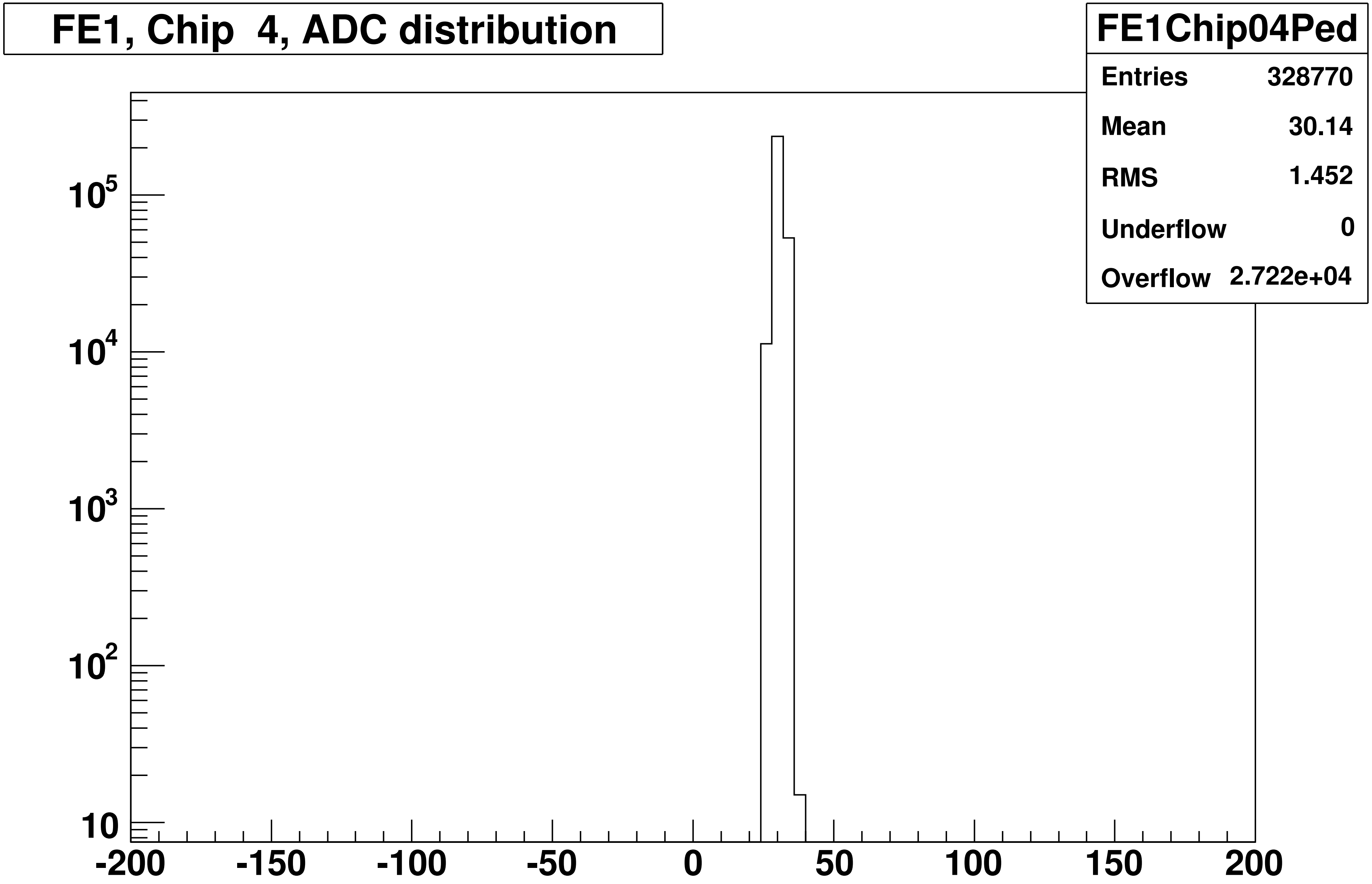
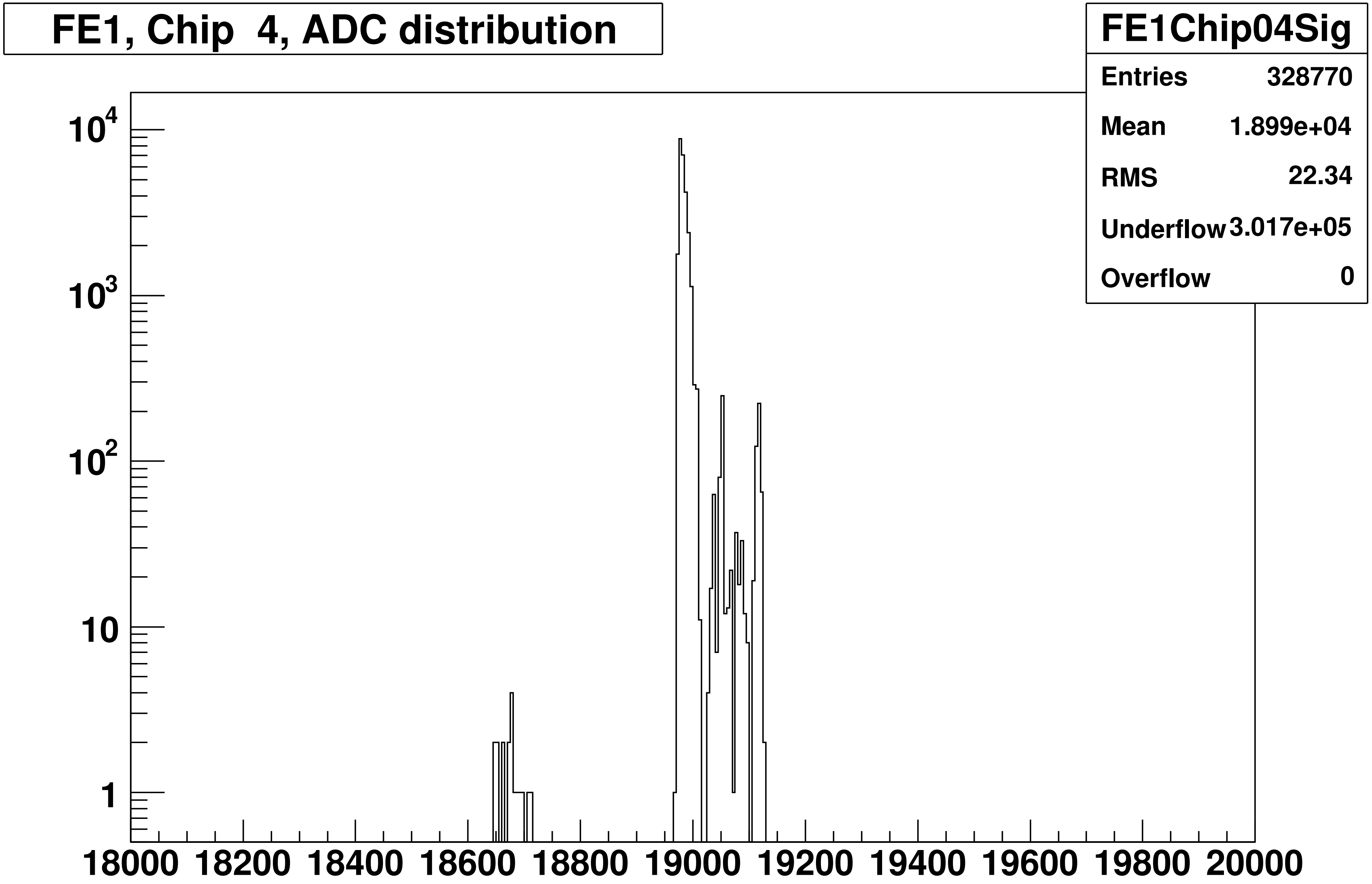
50
100
150
200

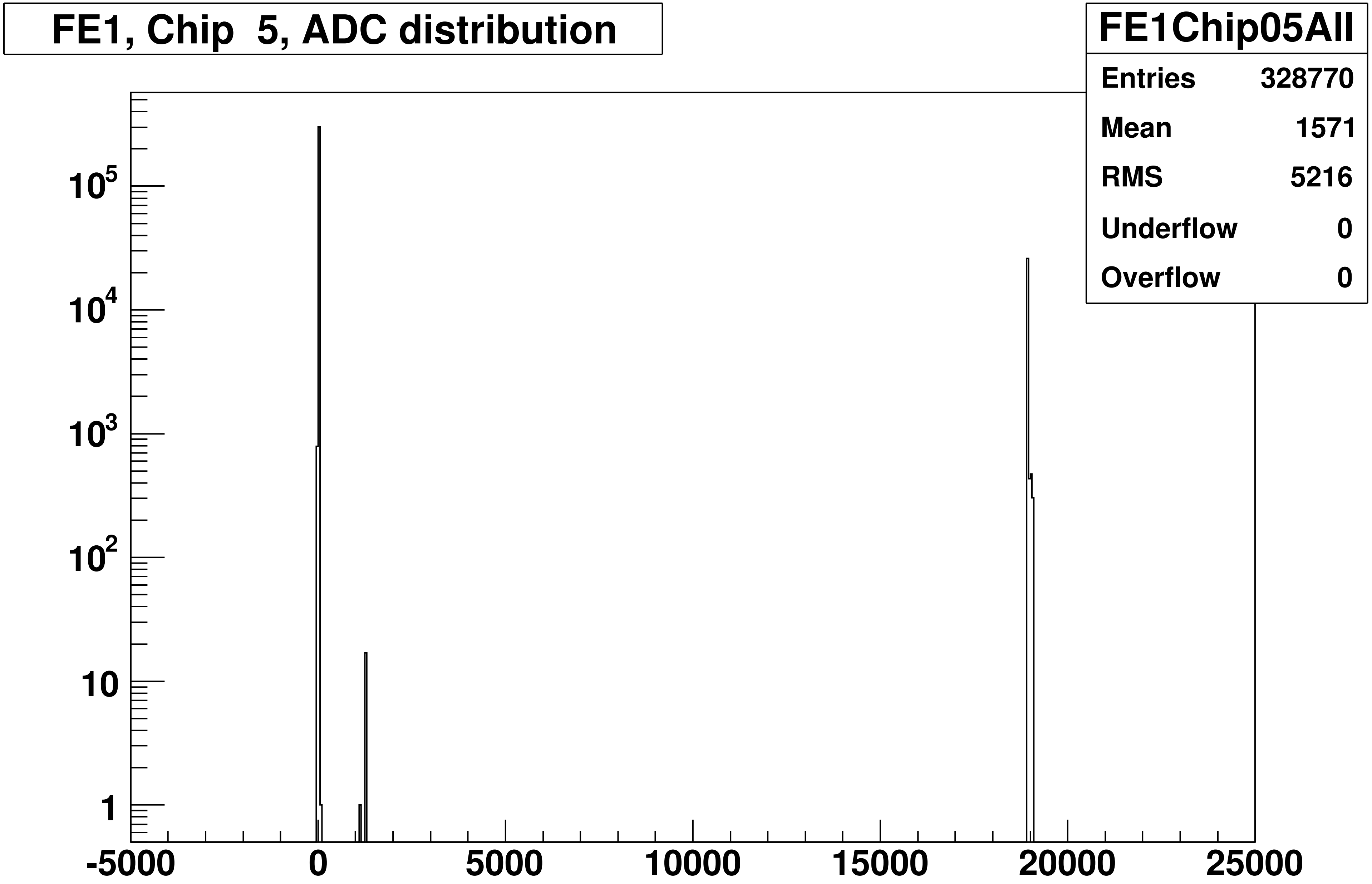

FE1, Chip 3, ADC distribution
FE1Chip03Sig
Entries 328770
Mean 1.887e+04
RMS 11.21
Underflow 3.022e+05
Overflow 0
10^4
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000

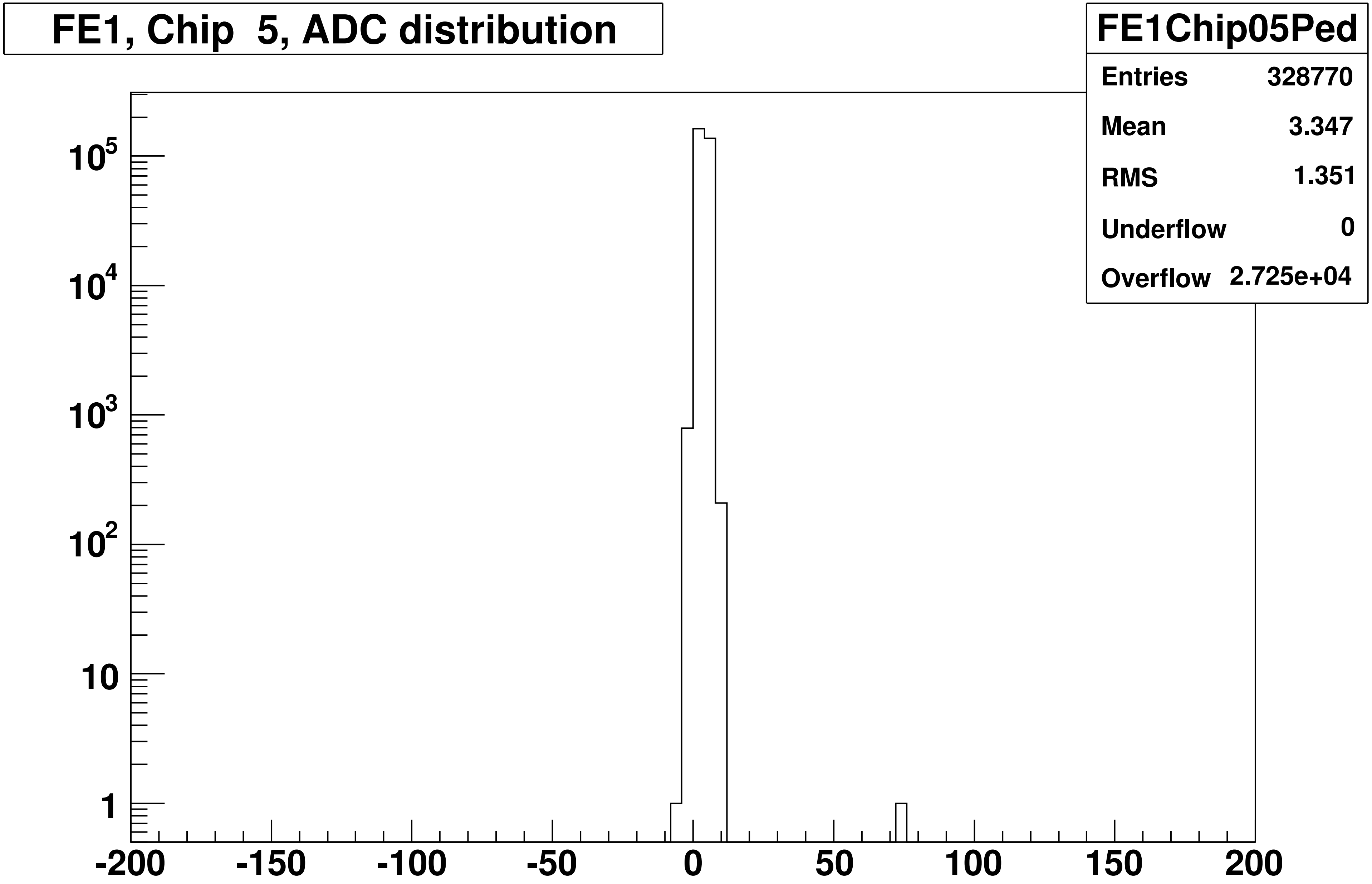

FE1, Chip 4, ADC distribution
FE1Chip04All
Entries 328770
Mean 1591
RMS 5209
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE1, Chip 4, ADC distribution
FE1Chip04Ped
Entries 328770
Mean 30.14
RMS 1.452
Underflow 0
Overflow 2.722e+04
10⁵
10⁴
10³
10²
10
-200
-150
-100
-50
0
50
100
150
200


FE1, Chip 4, ADC distribution
FE1Chip04Sig
Entries 328770
Mean 1.899e+04
RMS 22.34
Underflow 3.017e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000


FE1, Chip 5, ADC distribution
FE1Chip05All
Entries 328770
Mean 1571
RMS 5216
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE1, Chip 5, ADC distribution
FE1Chip05Ped
Entries 328770
Mean 3.347
RMS 1.351
Underflow 0
Overflow 2.725e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
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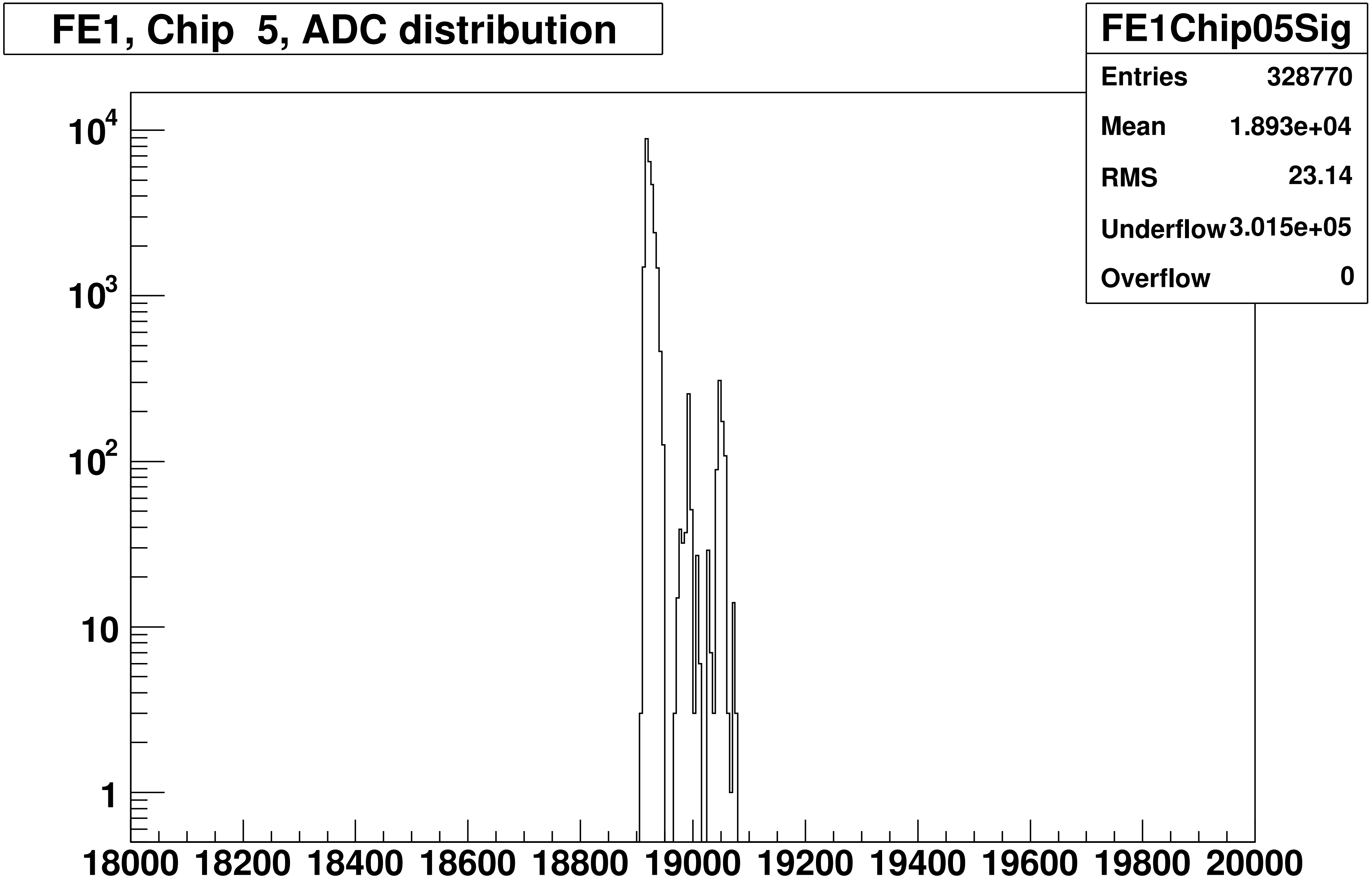
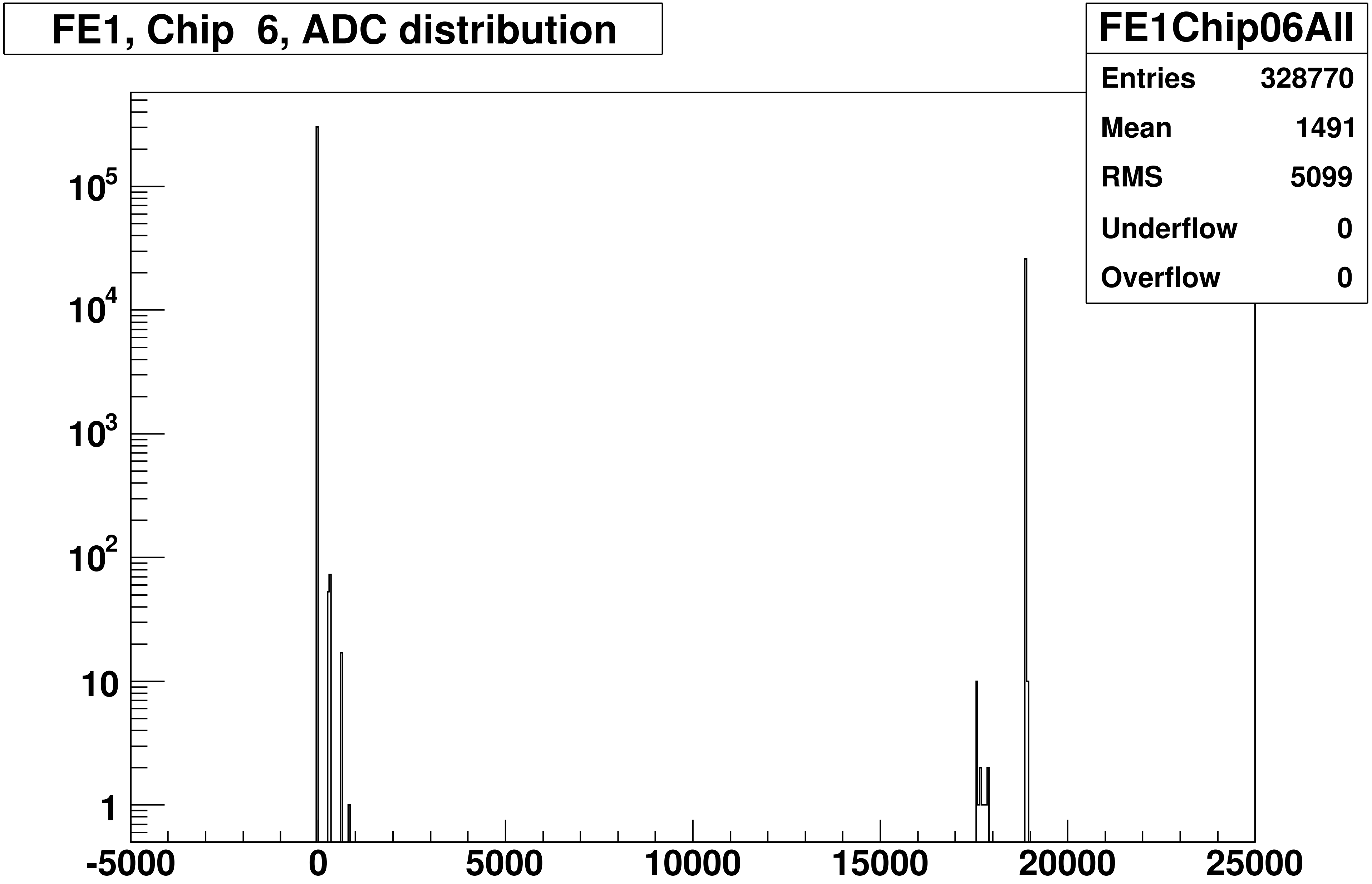
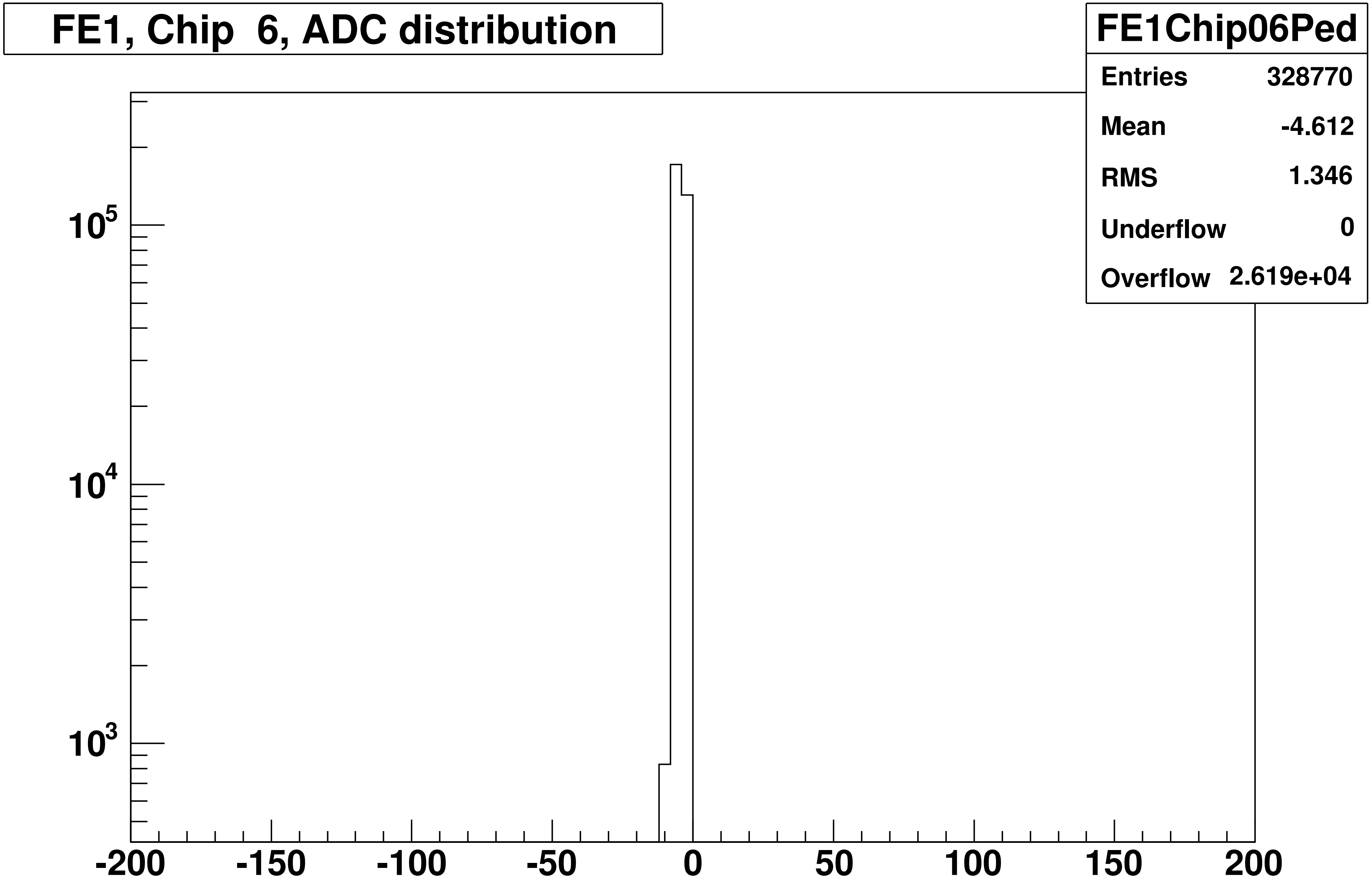
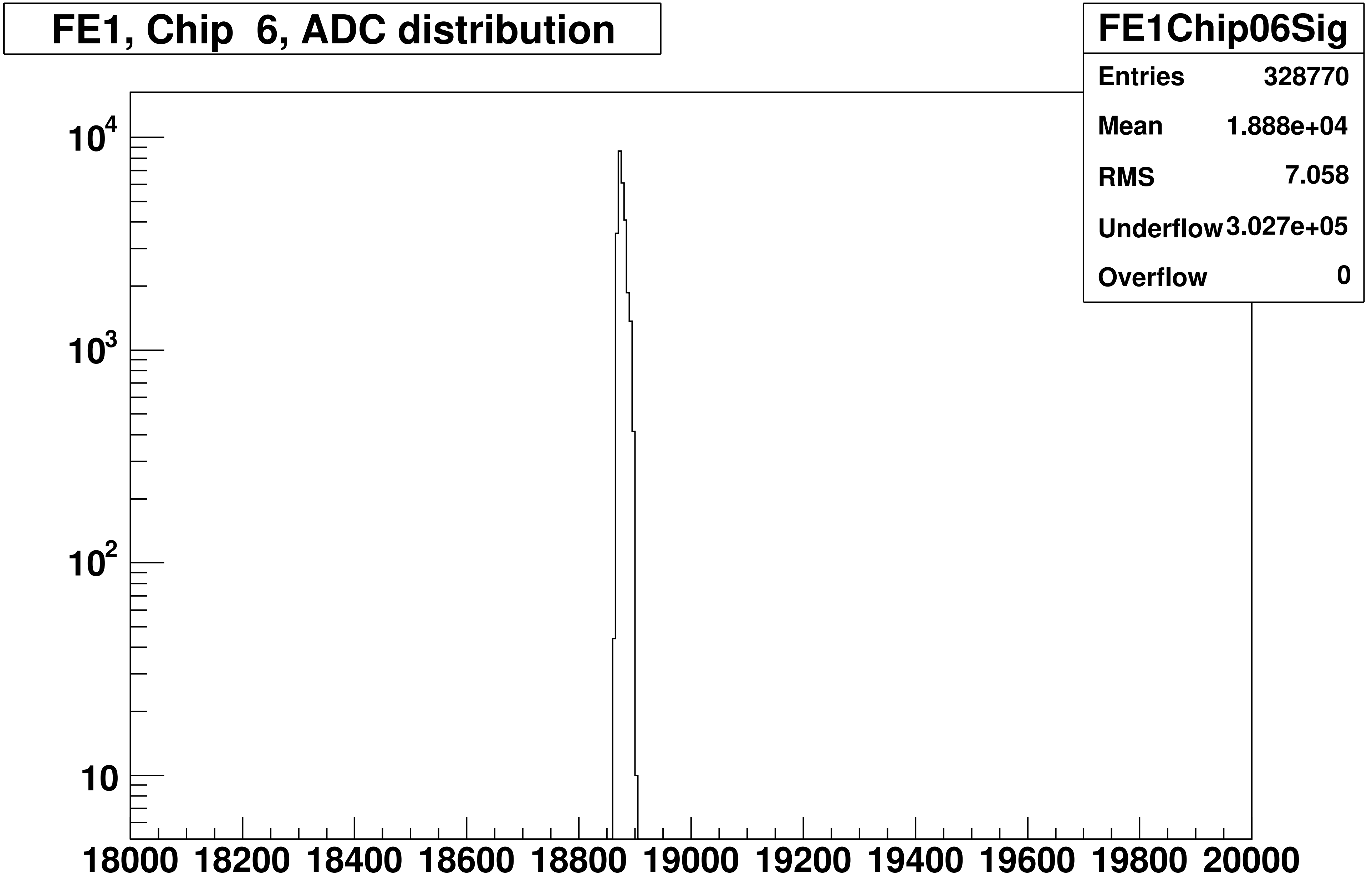
0
50
100
150
200

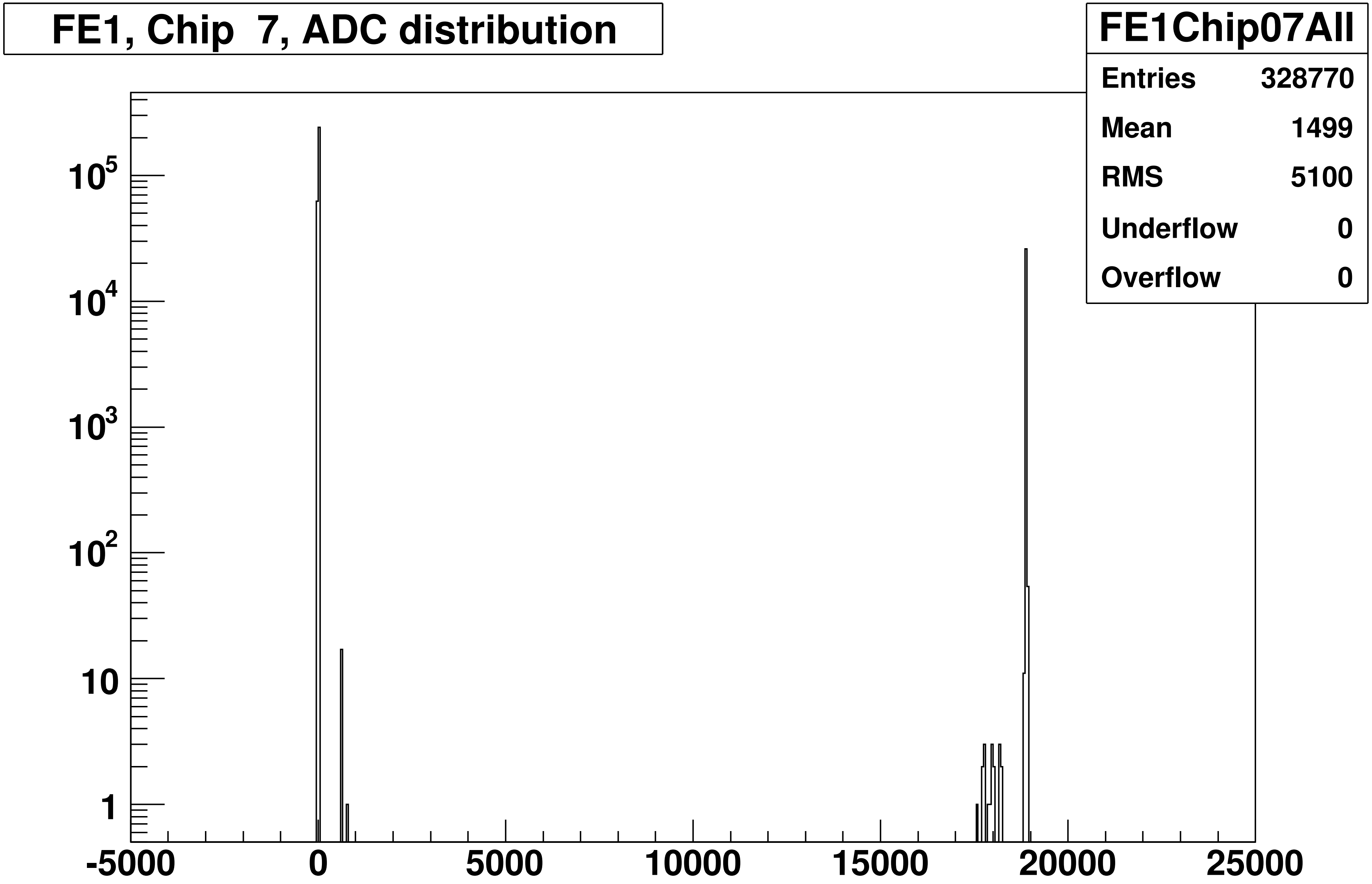

FE1, Chip 5, ADC distribution
FE1Chip05Sig
Entries 328770
Mean 1.893e+04
RMS 23.14
Underflow 3.015e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000

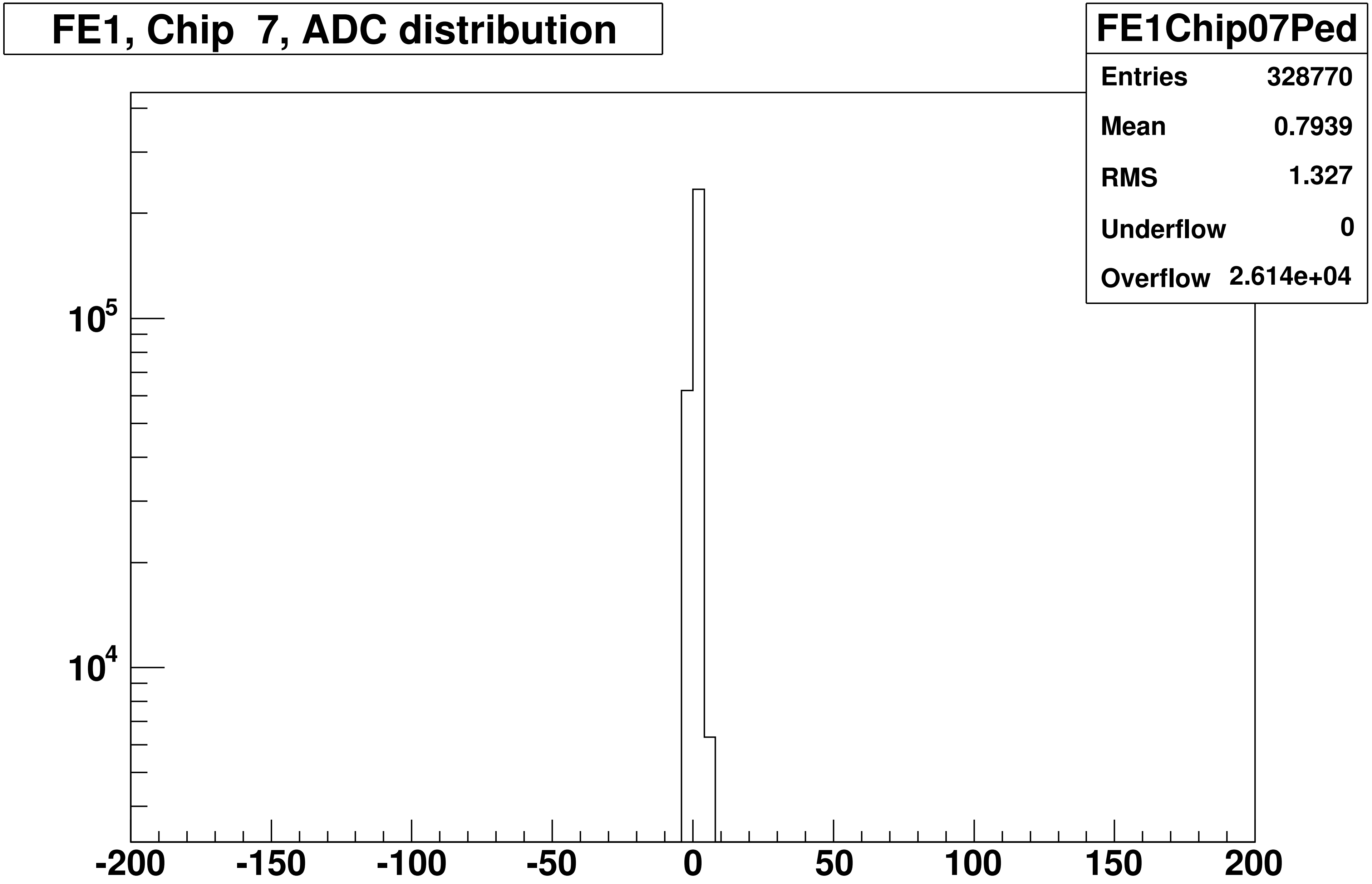


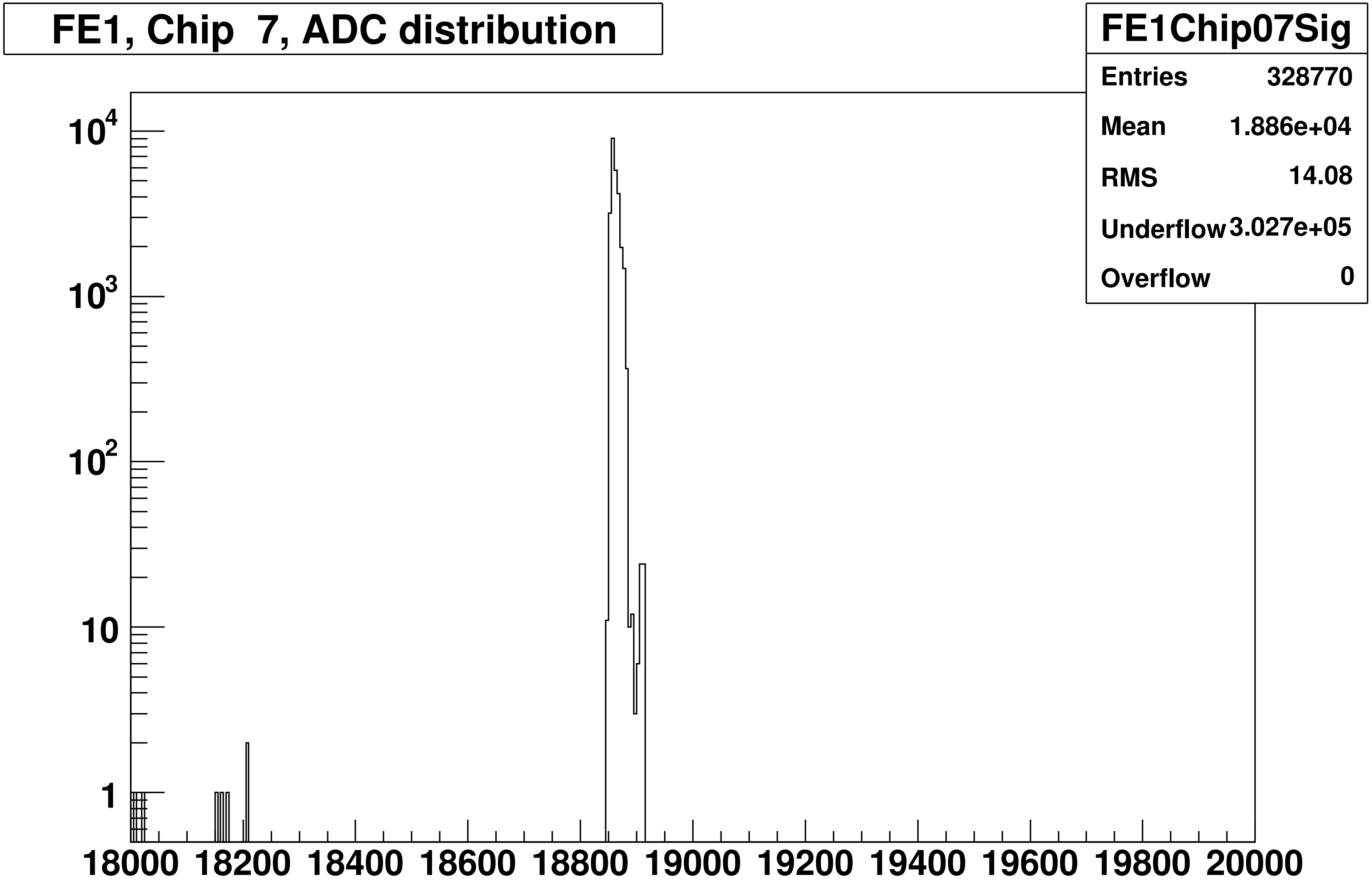
FE1, Chip 6, ADC distribution
FE1Chip06All
Entries 328770
Mean 1491
RMS 5099
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000

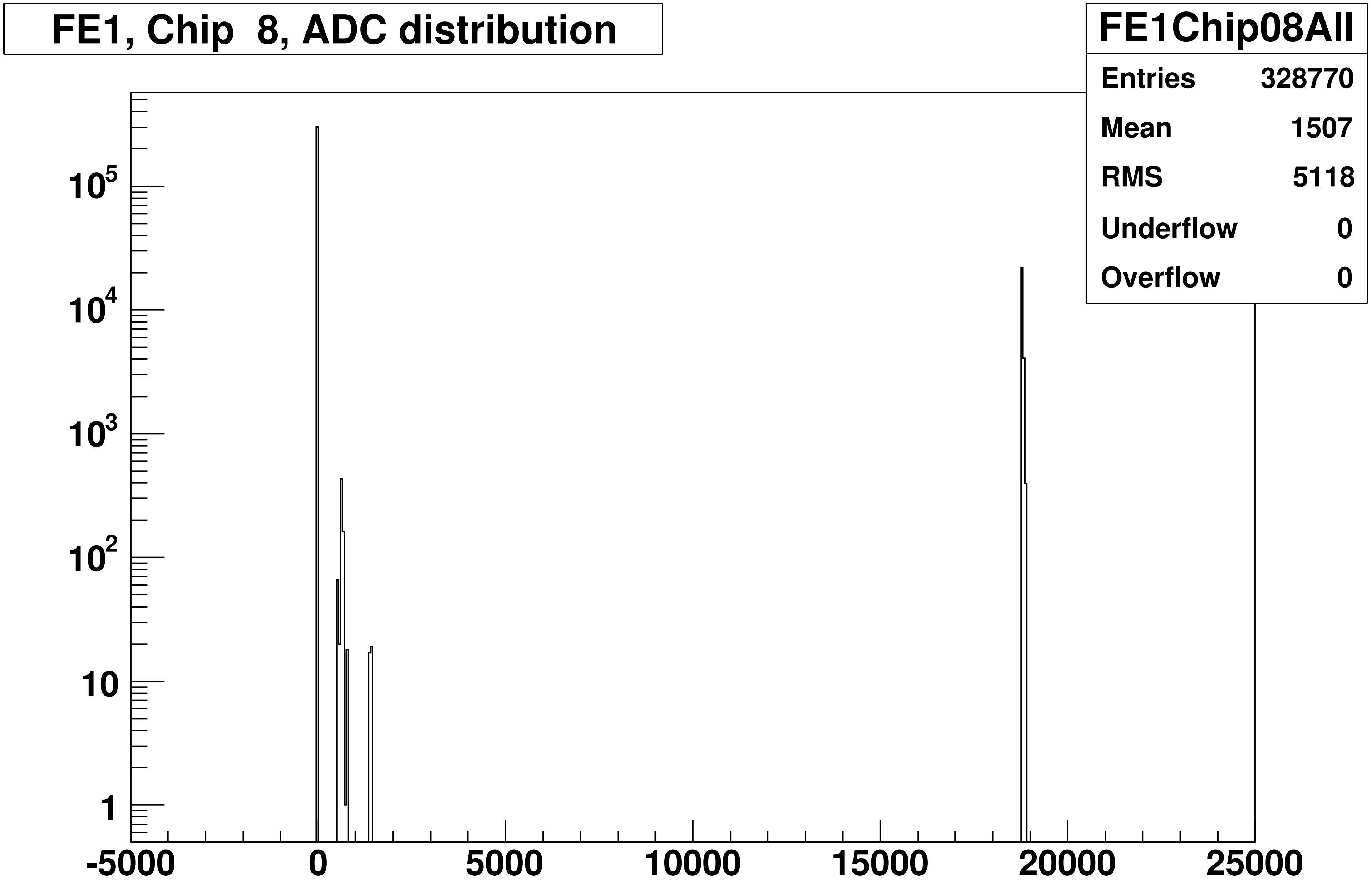

FE1, Chip 6, ADC distribution
FE1Chip06Ped
Entries 328770
Mean -4.612
RMS 1.346
Underflow 0
Overflow 2.619e+04
10^5
10^4
10^3
-200
-150
-100
-50
0
50
100
150
200


FE1, Chip 6, ADC distribution
FE1Chip06Sig
Entries 328770
Mean 1.888e+04
RMS 7.058
Underflow 3.027e+05
Overflow 0
10^4
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000

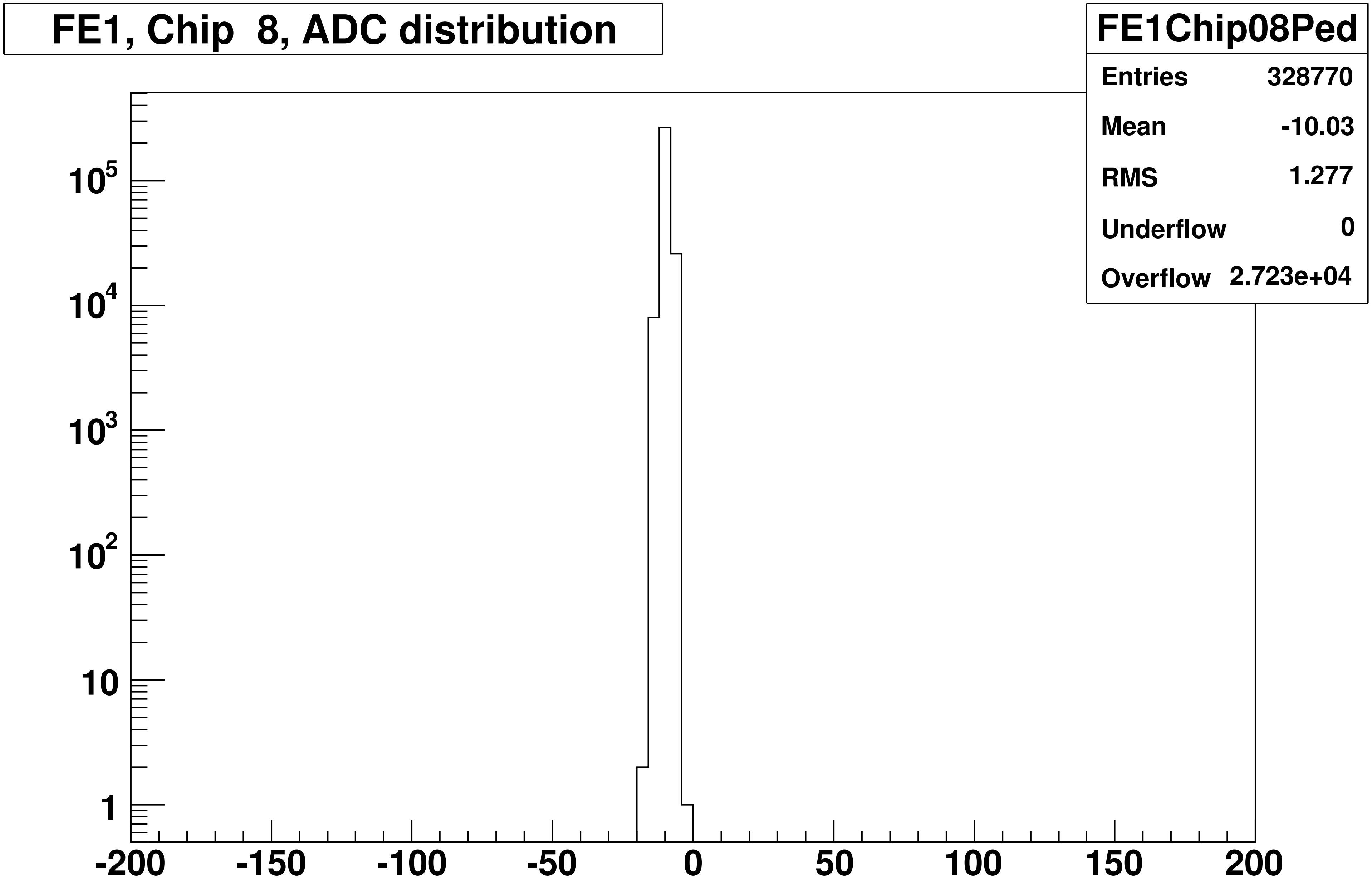

FE1, Chip 7, ADC distribution
FE1Chip07All
Entries 328770
Mean 1499
RMS 5100
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE1, Chip 7, ADC distribution
FE1Chip07Ped
Entries 328770
Mean 0.7939
RMS 1.327
Underflow 0
Overflow 2.614e+04
10^5
10^4
-200
-150
-100
-50
0
50
100
150
200

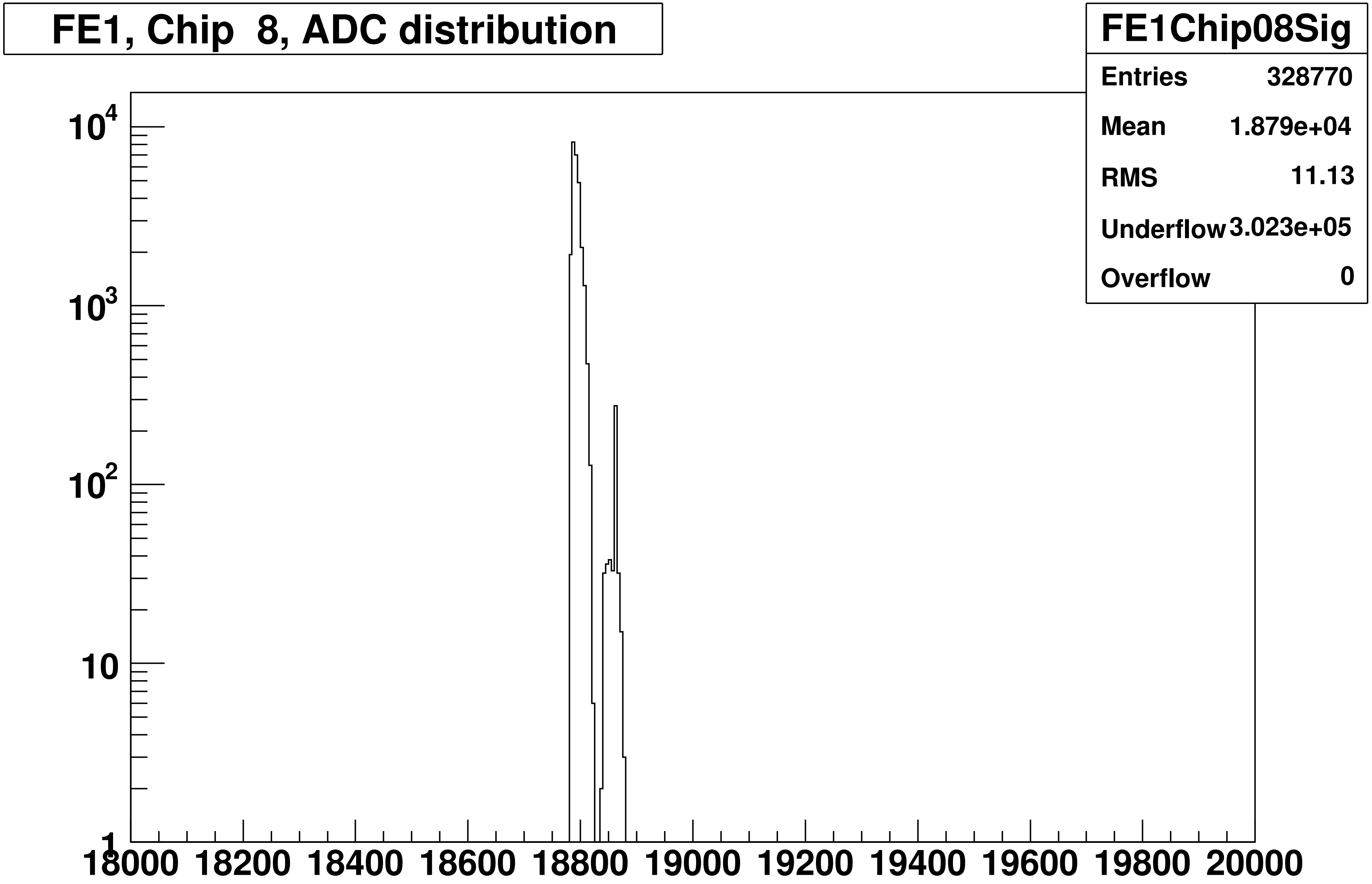

FE1, Chip 7, ADC distribution
FE1Chip07Sig
Entries 328770
Mean 1.886e+04
RMS 14.08
Underflow 3.027e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000



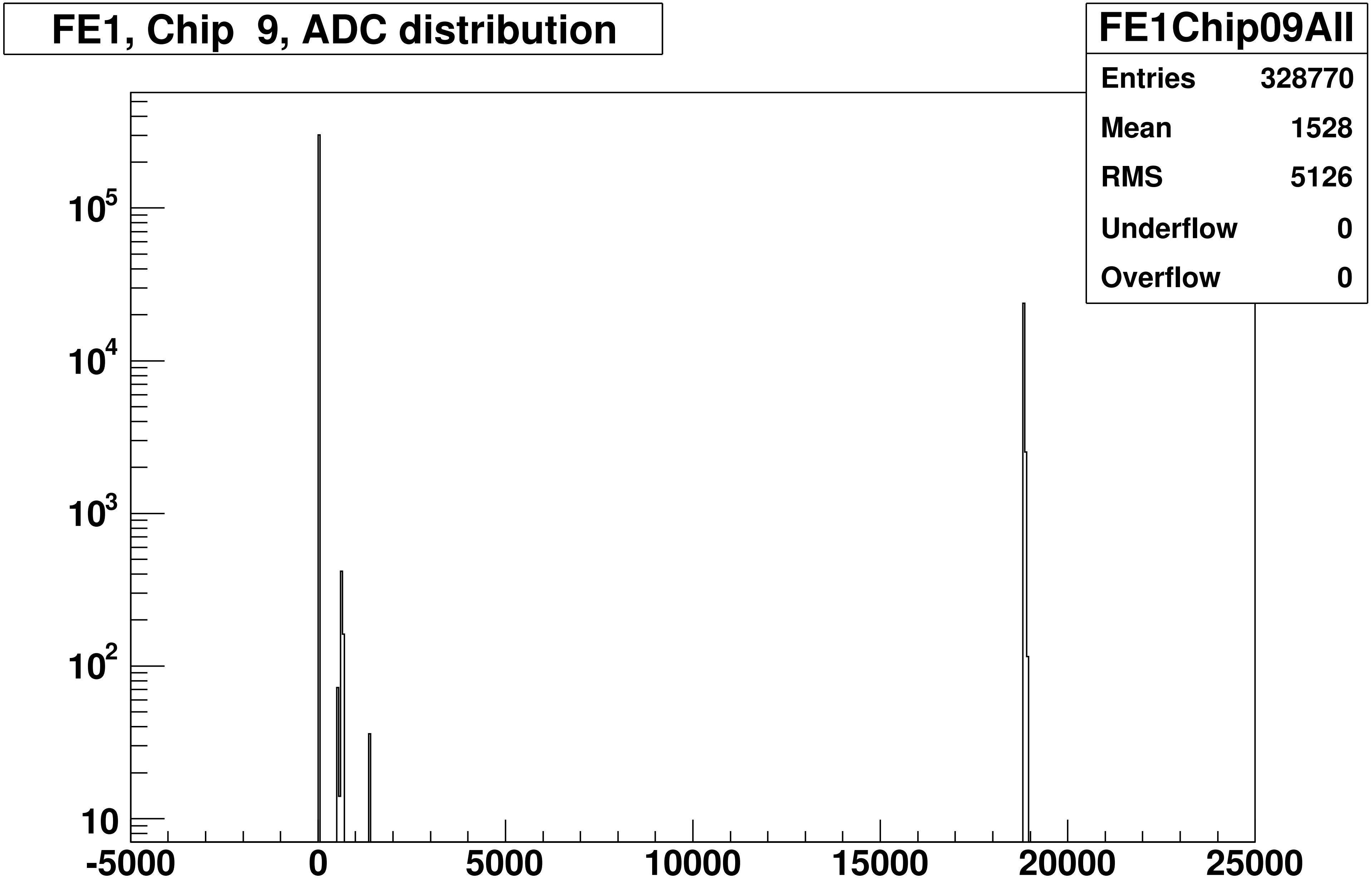
FE1, Chip 8, ADC distribution
FE1Chip08All
Entries 328770
Mean 1507
RMS 5118
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000

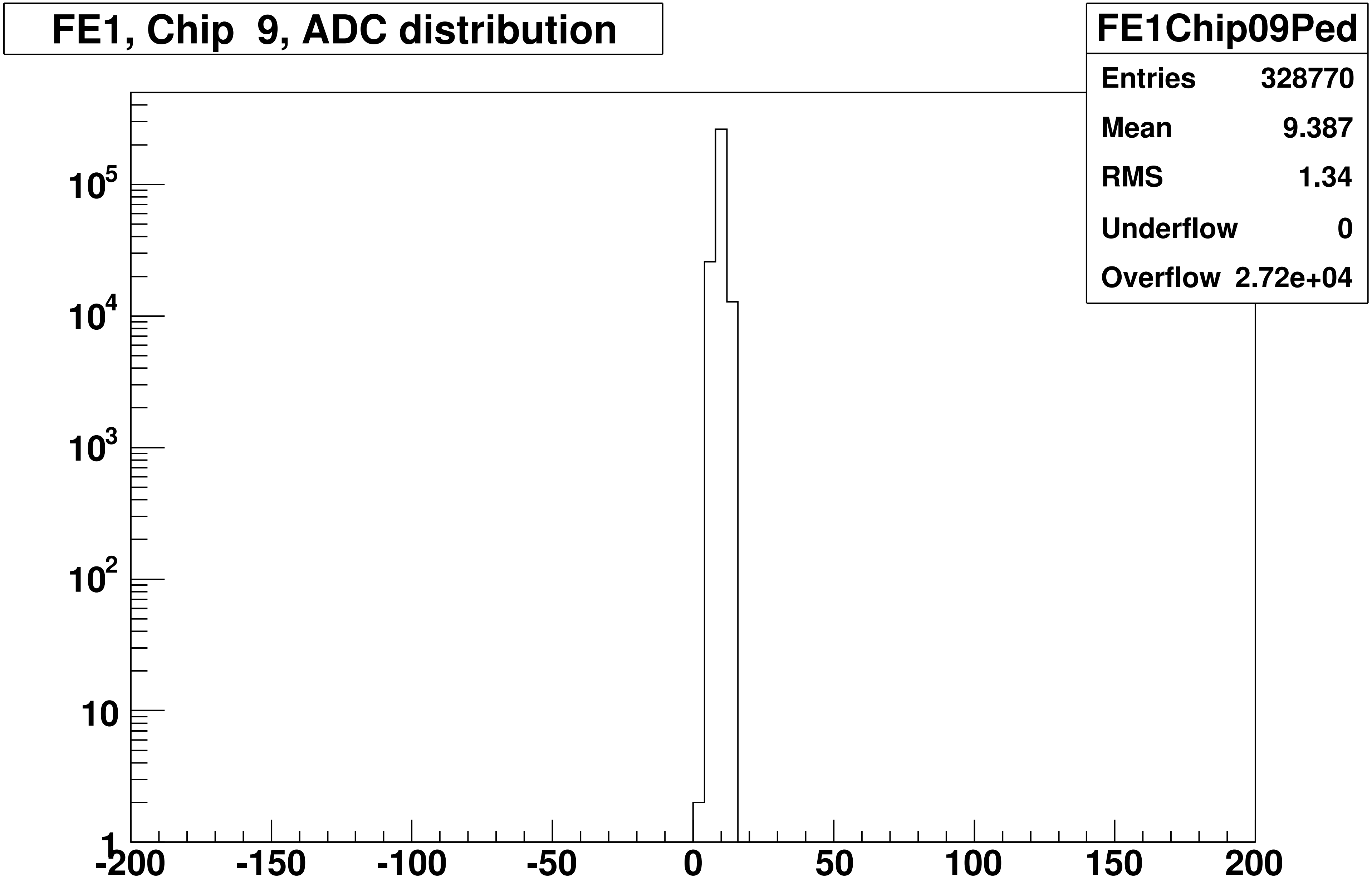


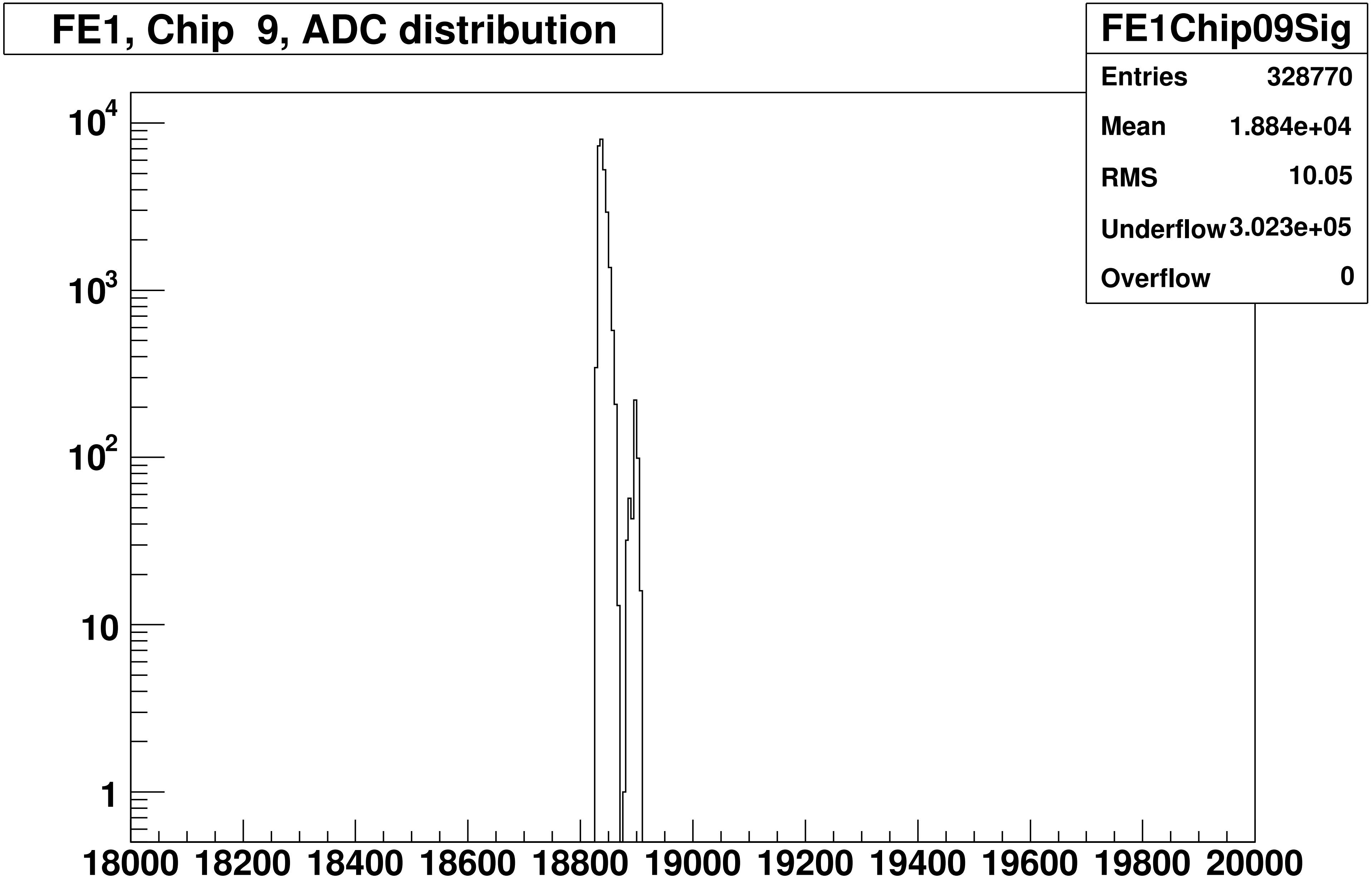
FE1, Chip 8, ADC distribution
FE1Chip08Ped
Entries 328770
Mean -10.03
RMS 1.277
Underflow 0
Overflow 2.723e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
200

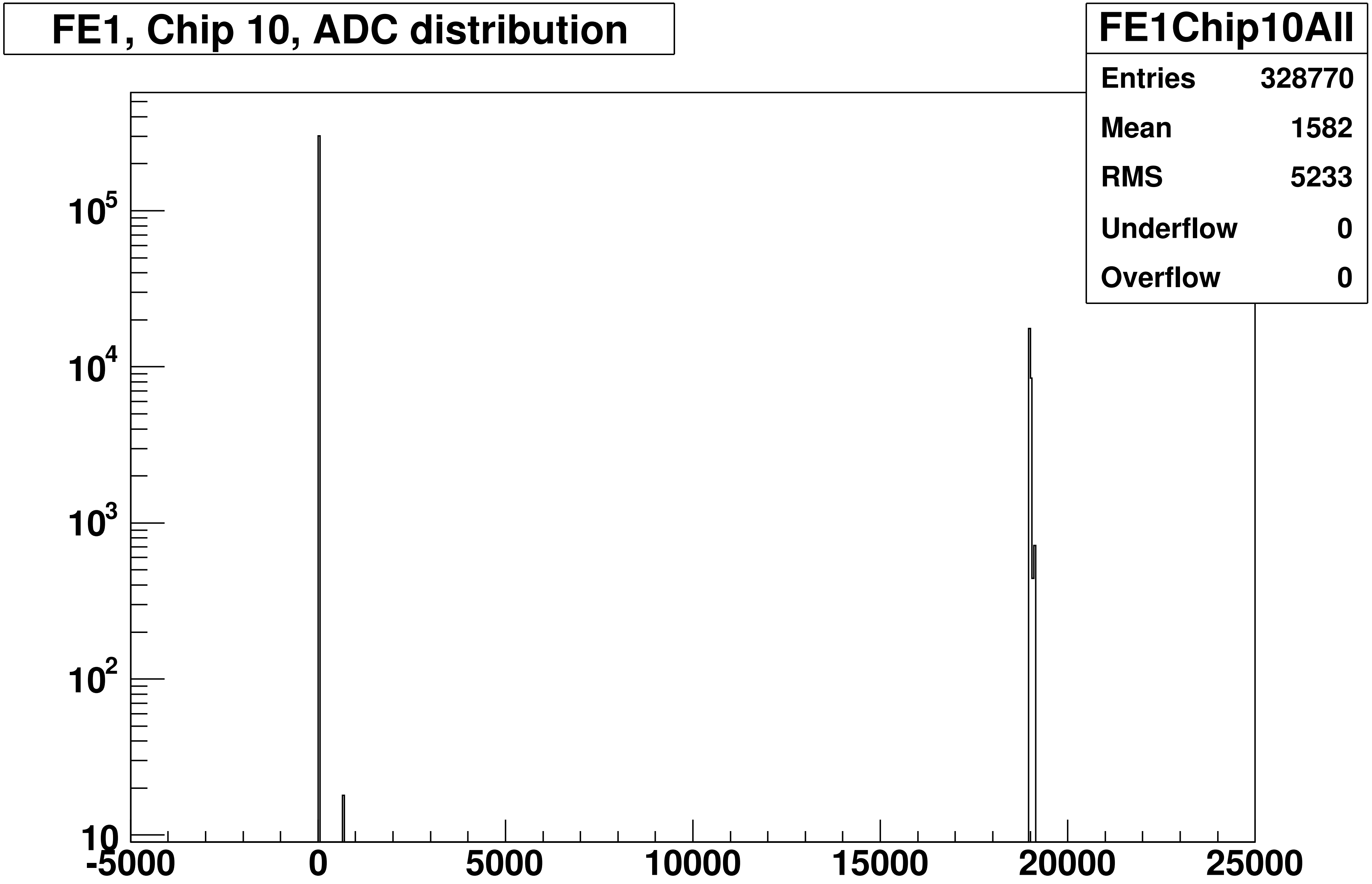


FE1, Chip 8, ADC distribution
FE1Chip08Sig
Entries 328770
Mean 1.879e+04
RMS 11.13
Underflow 3.023e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000

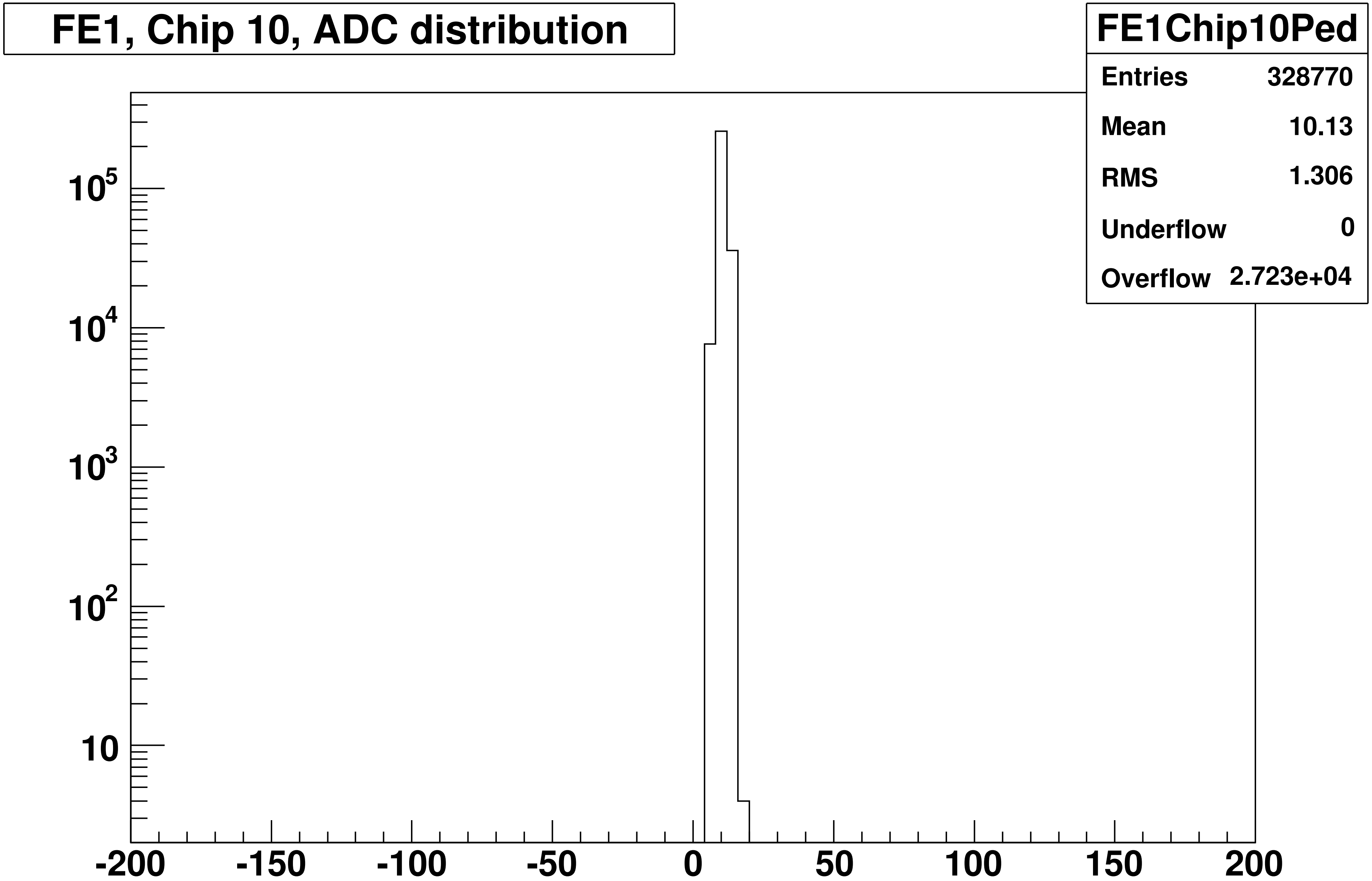

FE1, Chip 9, ADC distribution
FE1Chip09All
Entries 328770
Mean 1528
RMS 5126
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE1, Chip 9, ADC distribution
FE1Chip09Ped
Entries 328770
Mean 9.387
RMS 1.34
Underflow 0
Overflow 2.72e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
200

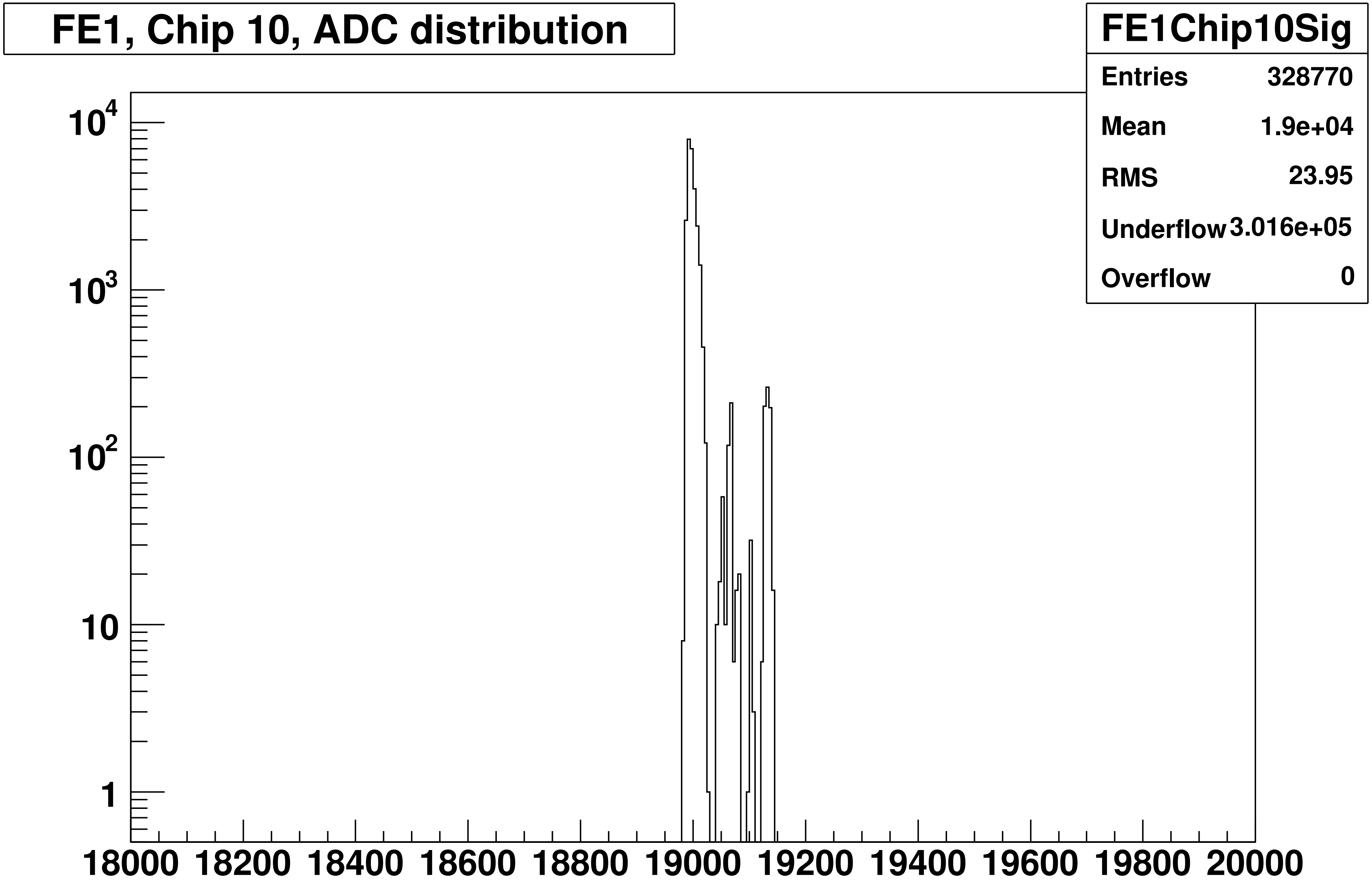

FE1, Chip 9, ADC distribution
FE1Chip09Sig
Entries 328770
Mean 1.884e+04
RMS 10.05
Underflow 3.023e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000

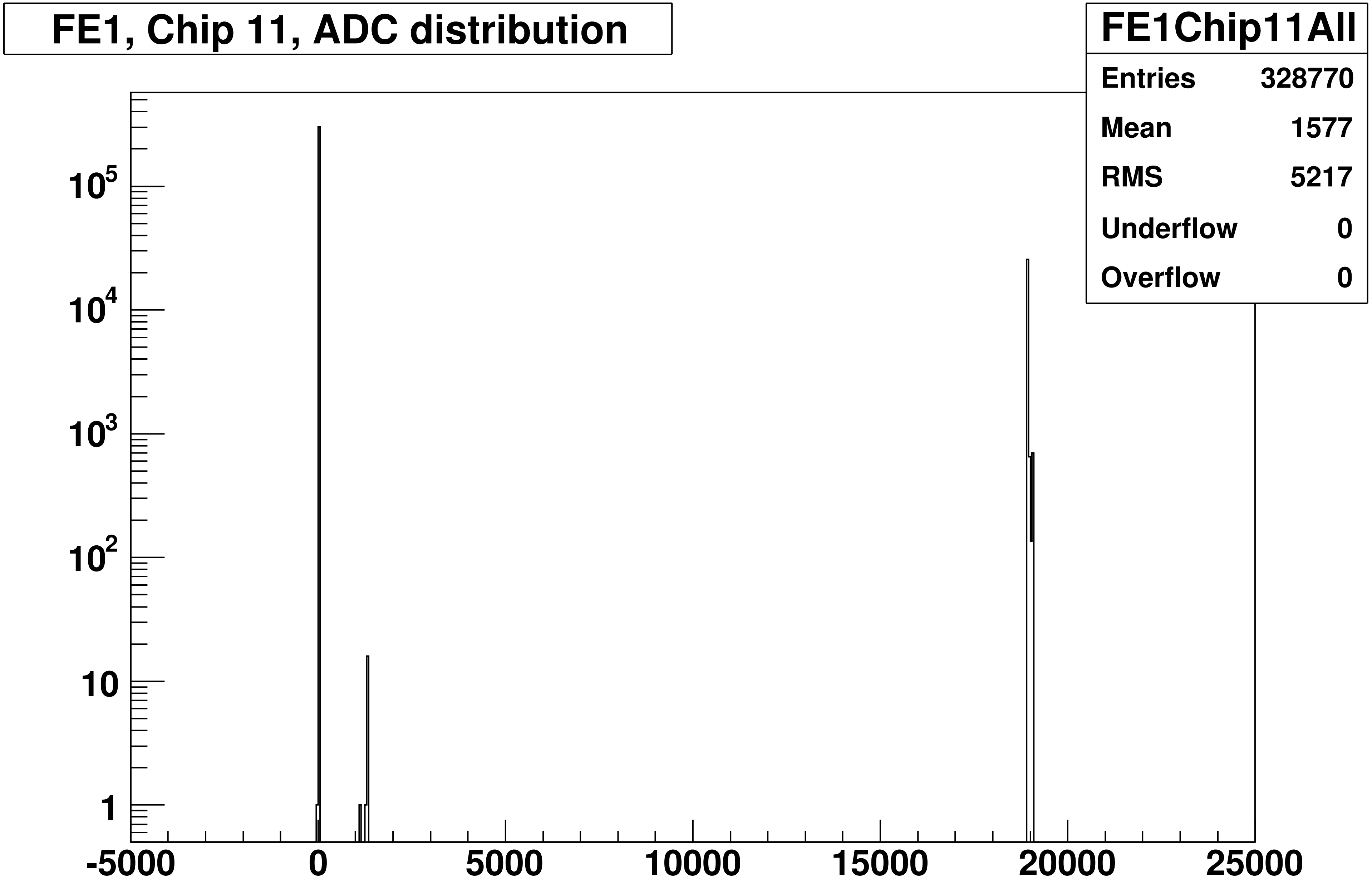


FE1, Chip 10, ADC distribution
FE1Chip10All
Entries 328770
Mean 1582
RMS 5233
Underflow 0
Overflow 0
10
10^2
10^3
10^4
10^5
-5000
0
5000
10000
15000
20000
25000

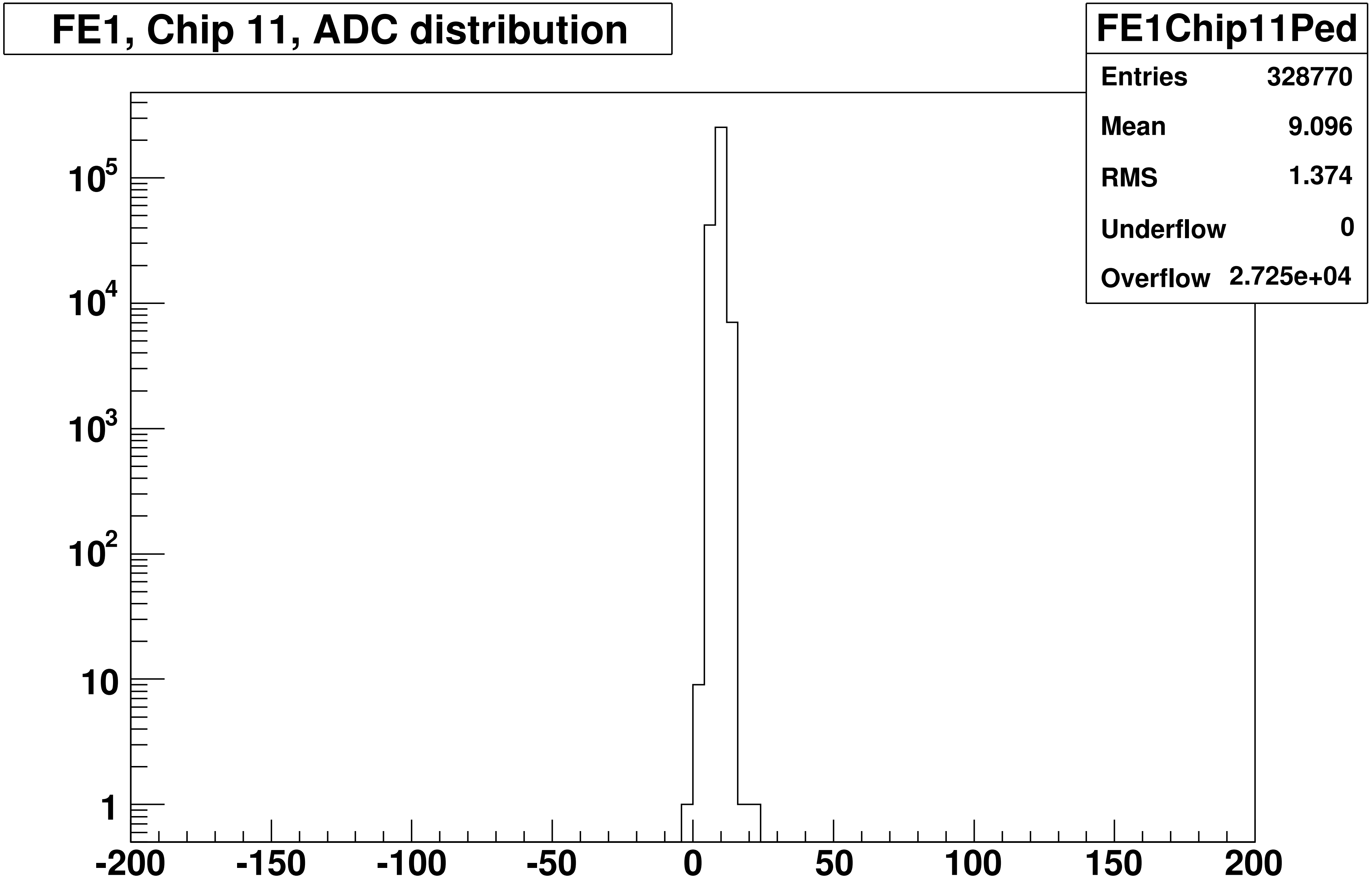


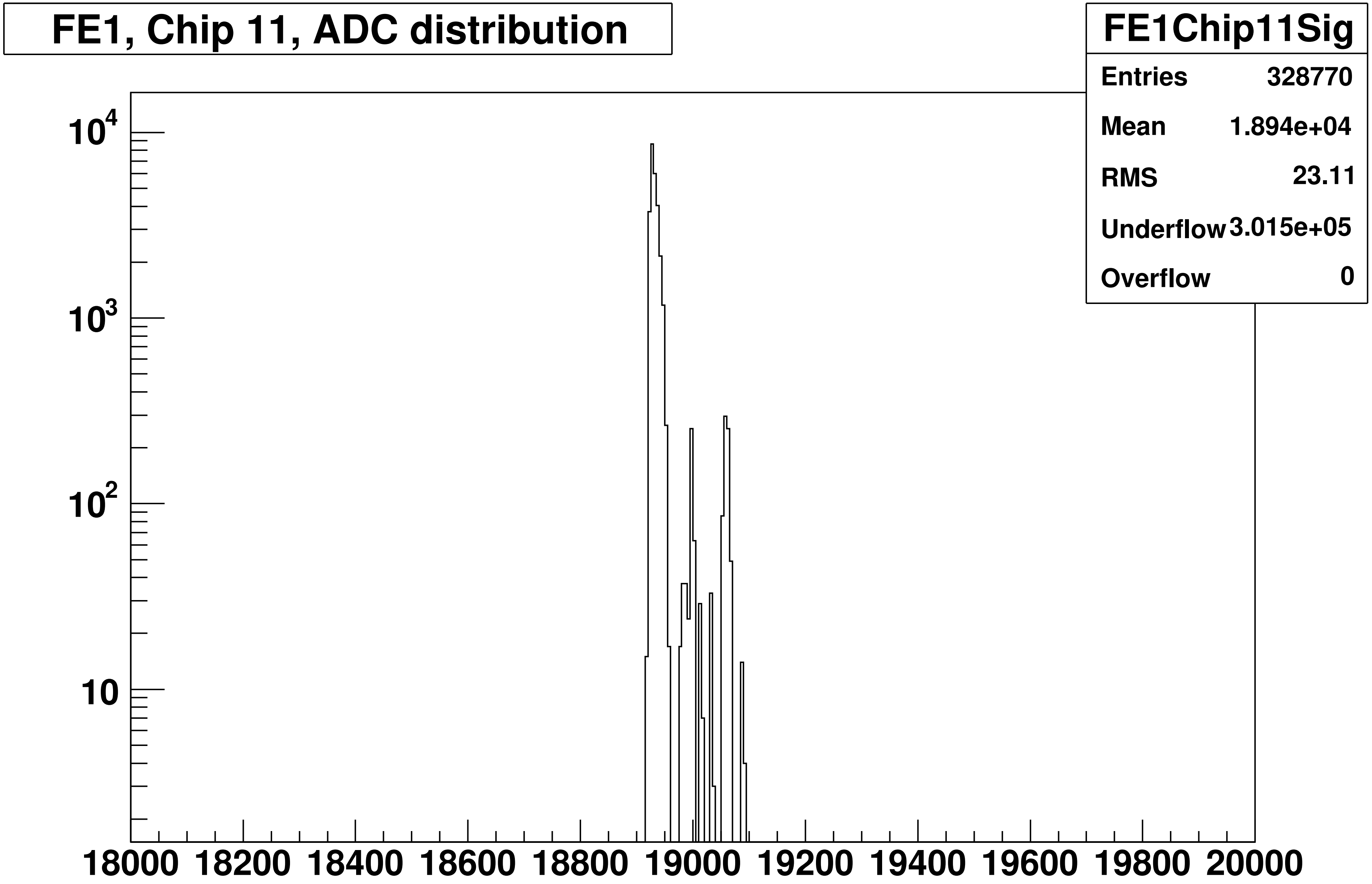
FE1, Chip 10, ADC distribution
FE1Chip10Ped
Entries 328770
Mean 10.13
RMS 1.306
Underflow 0
Overflow 2.723e+04
10^5
10^4
10^3
10^2
10
-200
-150
-100
-50
0
50
100
150
200


FE1, Chip 10, ADC distribution
FE1Chip10Sig
Entries 328770
Mean 1.9e+04
RMS 23.95
Underflow 3.016e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000

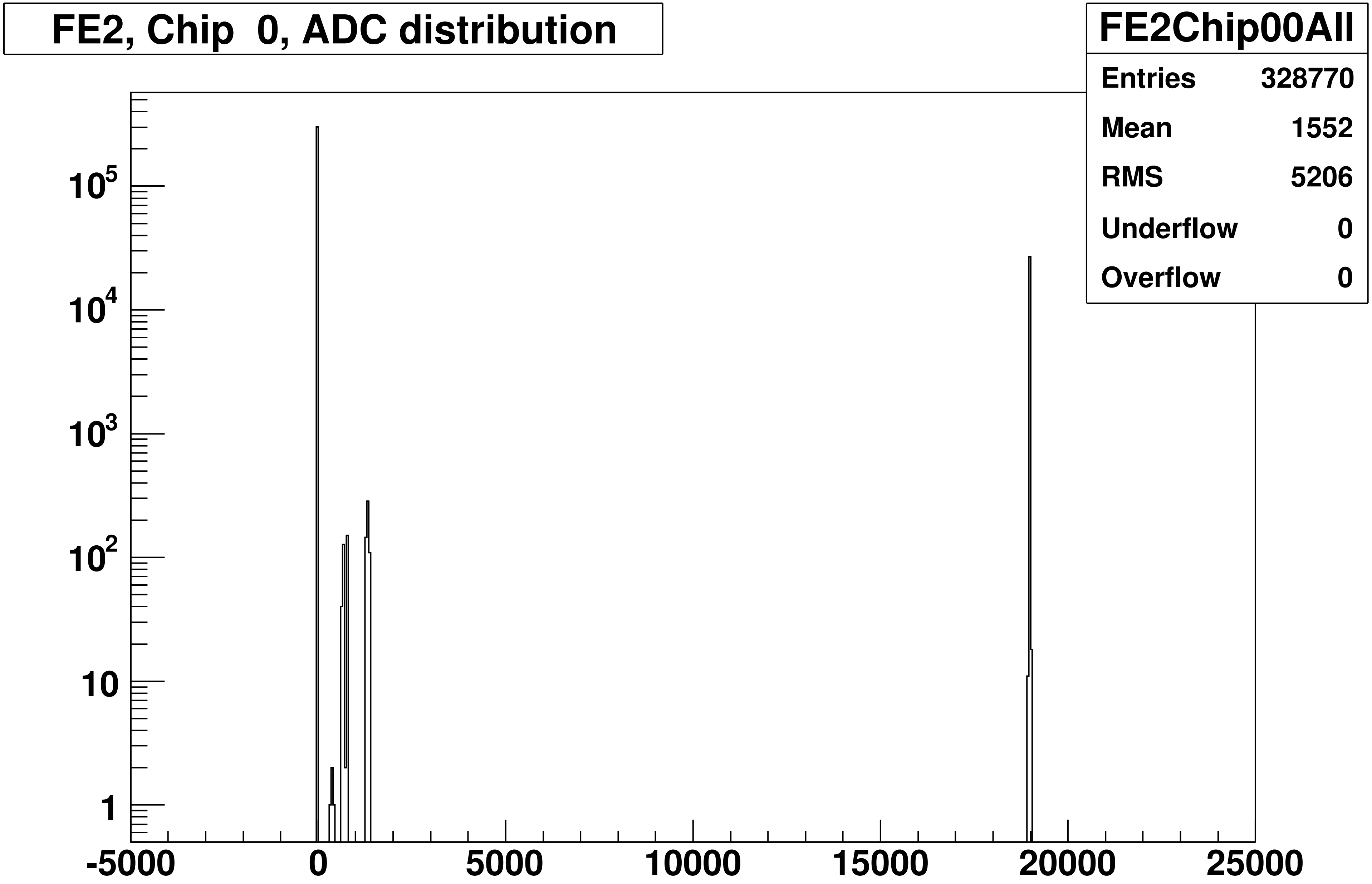


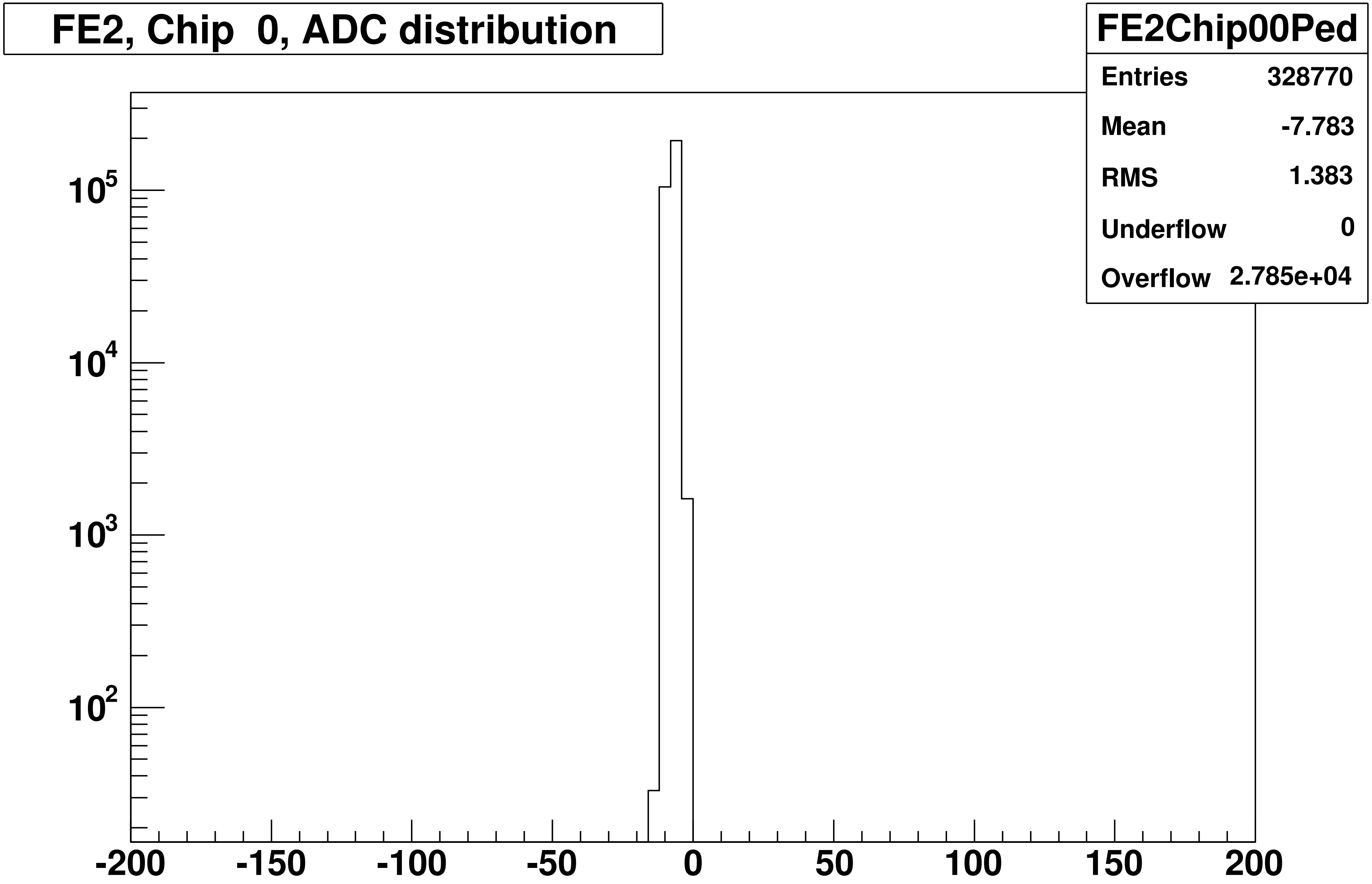
FE1, Chip 11, ADC distribution
FE1Chip11All
Entries 328770
Mean 1577
RMS 5217
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000

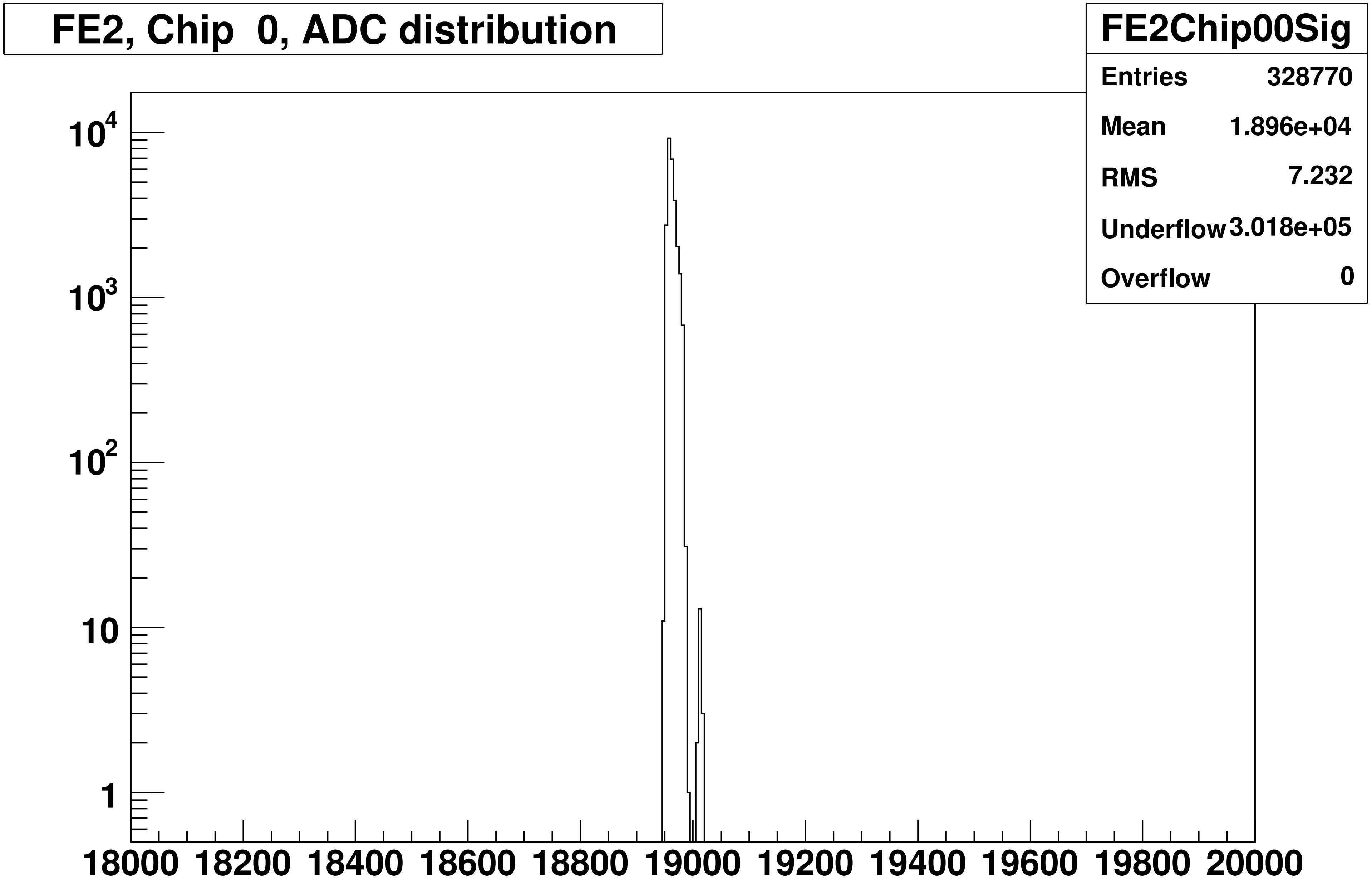

FE1, Chip 11, ADC distribution
FE1Chip11Ped
Entries 328770
Mean 9.096
RMS 1.374
Underflow 0
Overflow 2.725e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
200



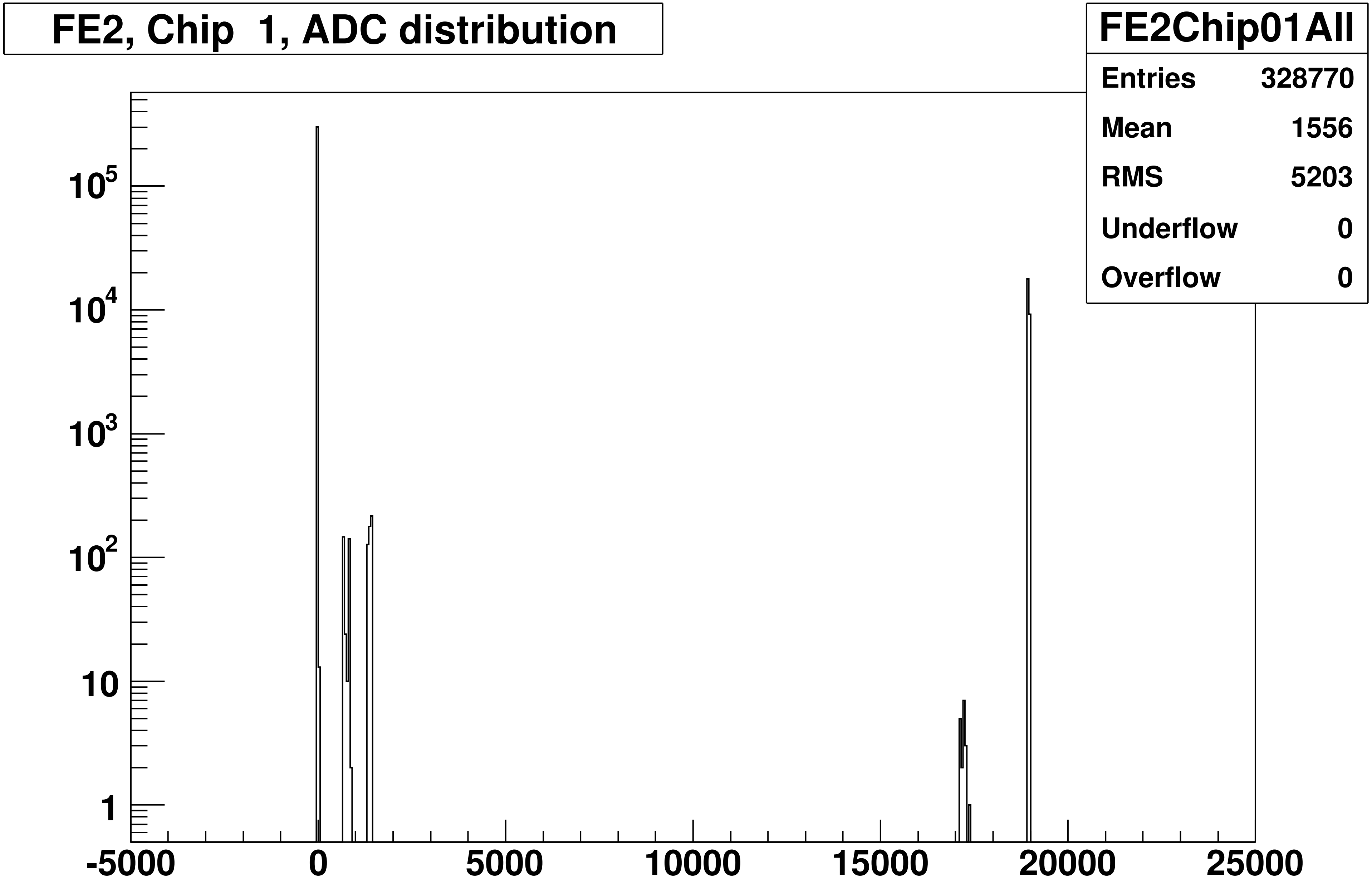
FE1, Chip 11, ADC distribution
FE1Chip11Sig
Entries 328770
Mean 1.894e+04
RMS 23.11
Underflow 3.015e+05
Overflow 0
10^4
10^3
10^2
10
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000


FE2, Chip 0, ADC distribution
FE2Chip00All
Entries 328770
Mean 1552
RMS 5206
Underflow 0
Overflow 0
-5000
0
5000
10000
15000
20000
25000
1
10
10^2
10^3
10^4
10^5

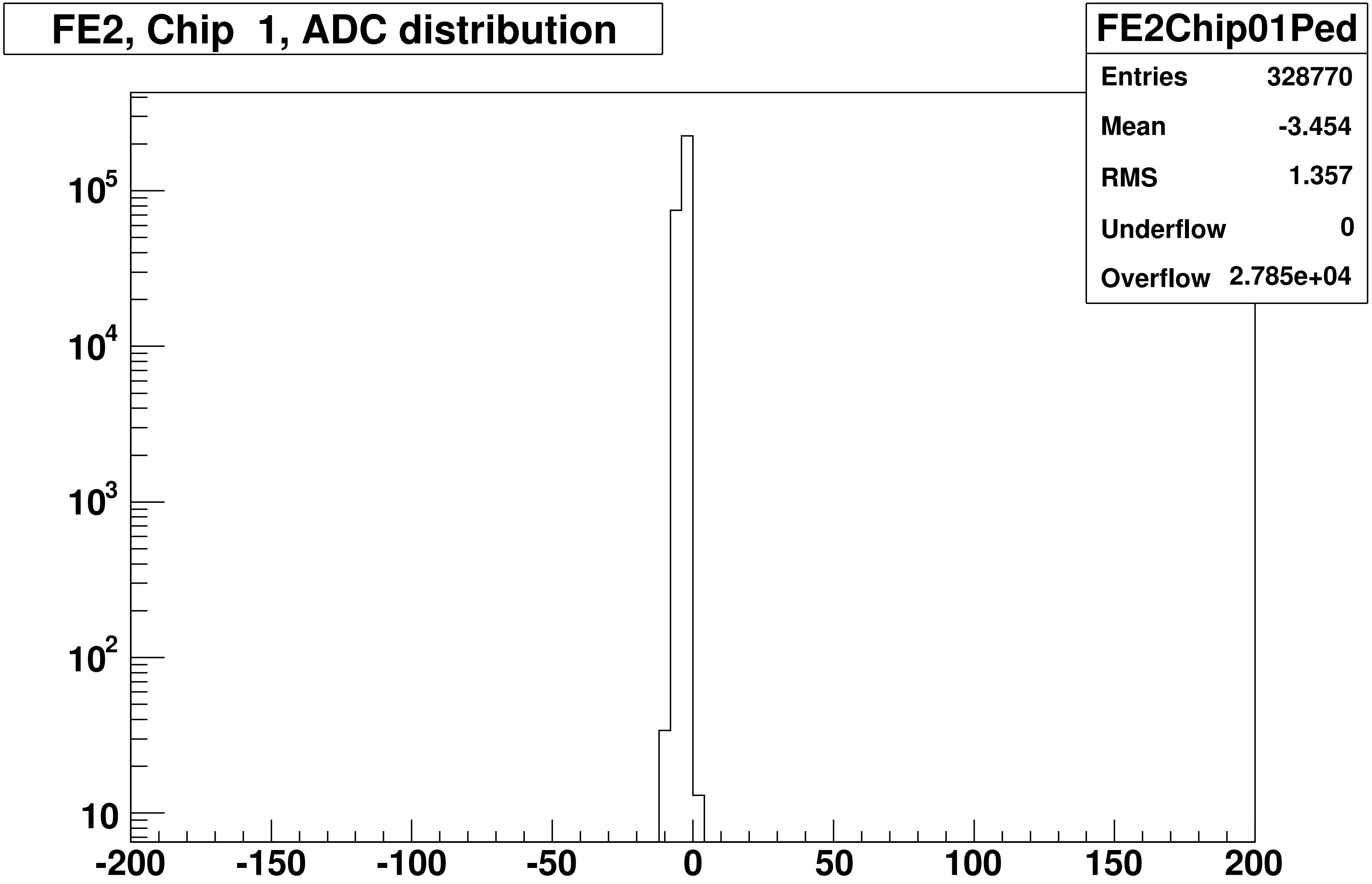

FE2, Chip 0, ADC distribution
FE2Chip00Ped
Entries 328770
Mean -7.783
RMS 1.383
Underflow 0
Overflow 2.785e+04
10^5
10^4
10^3
10^2
-200 -150 -100 -50 0 50 100 150 200

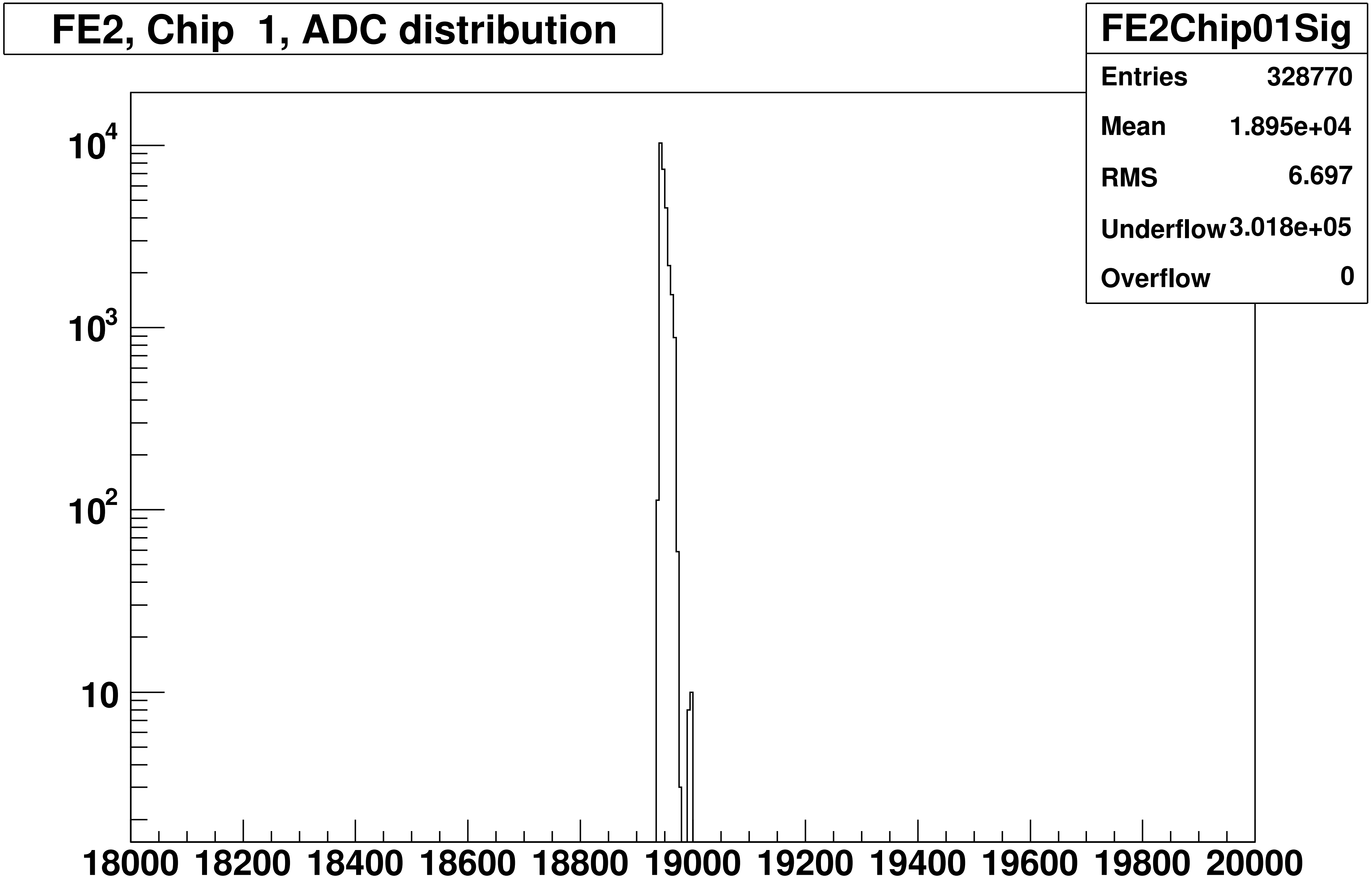


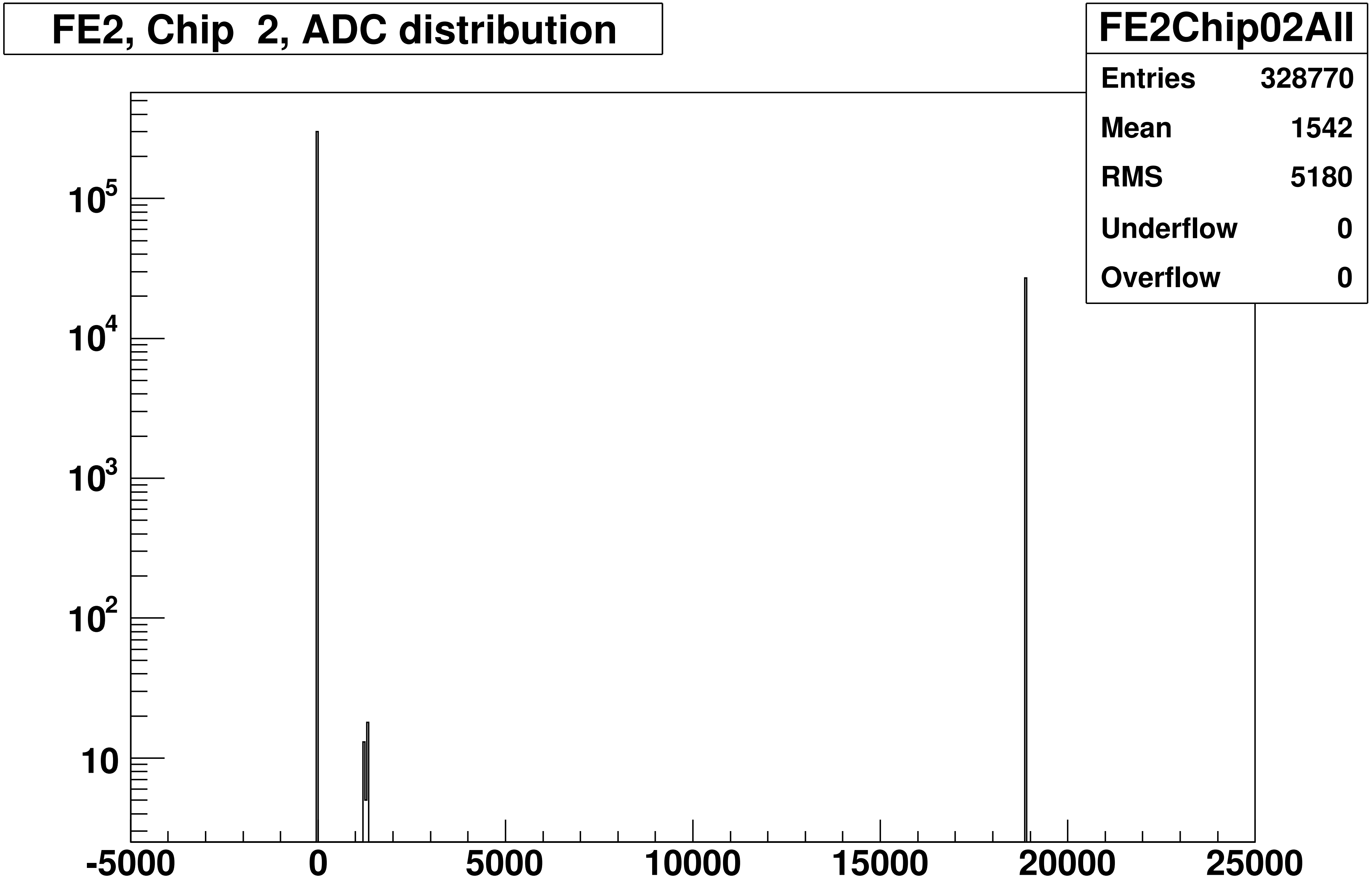
FE2, Chip 0, ADC distribution
FE2Chip00Sig
Entries 328770
Mean 1.896e+04
RMS 7.232
Underflow 3.018e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000

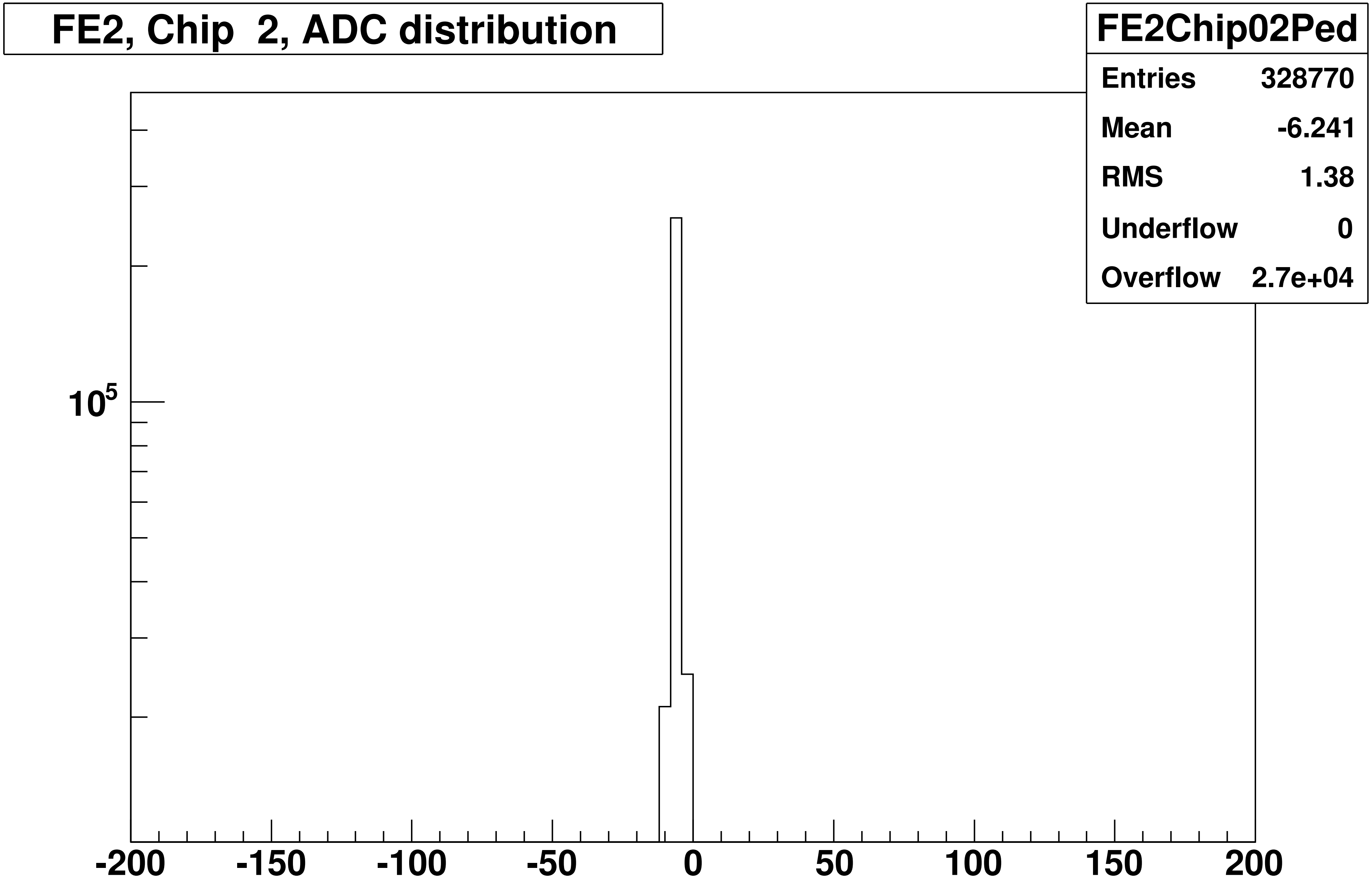


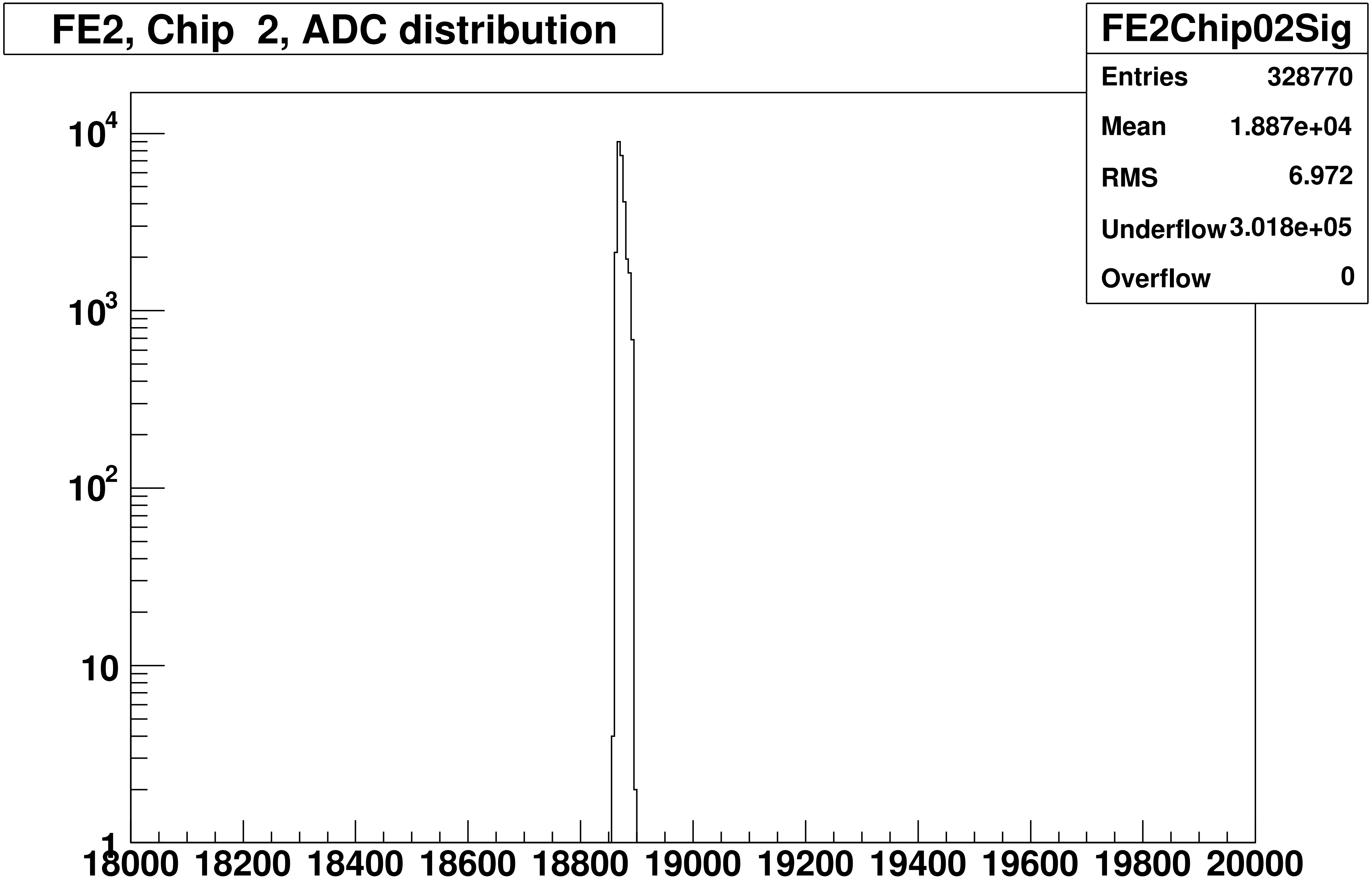
FE2, Chip 1, ADC distribution
FE2Chip01All
Entries 328770
Mean 1556
RMS 5203
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE2, Chip 1, ADC distribution
FE2Chip01Ped
Entries 328770
Mean -3.454
RMS 1.357
Underflow 0
Overflow 2.785e+04
10^5
10^4
10^3
10^2
10
-200
-150
-100
-50
0
50
100
150
200

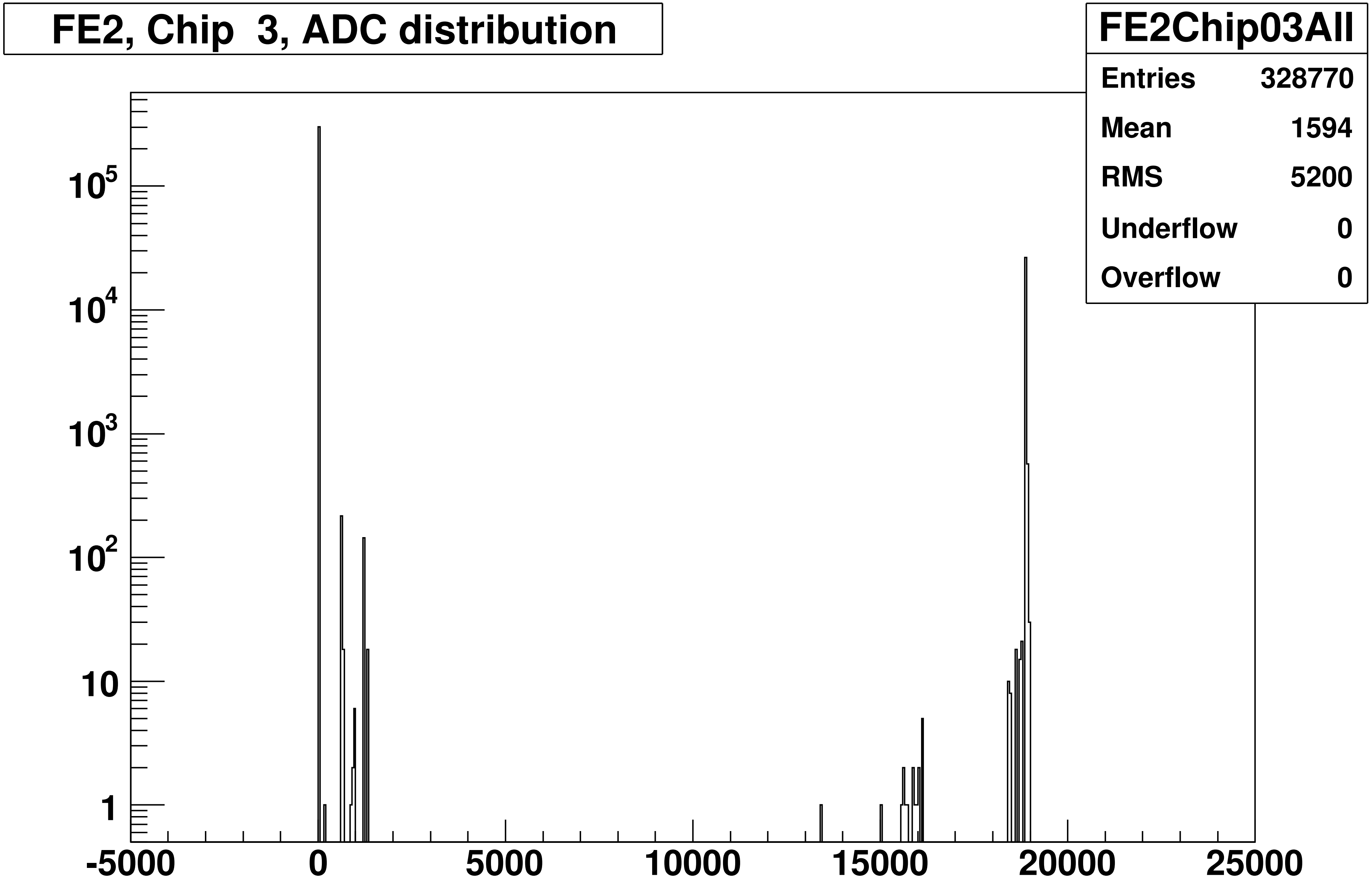

FE2, Chip 1, ADC distribution
FE2Chip01Sig
Entries 328770
Mean 1.895e+04
RMS 6.697
Underflow 3.018e+05
Overflow 0
10^4
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000

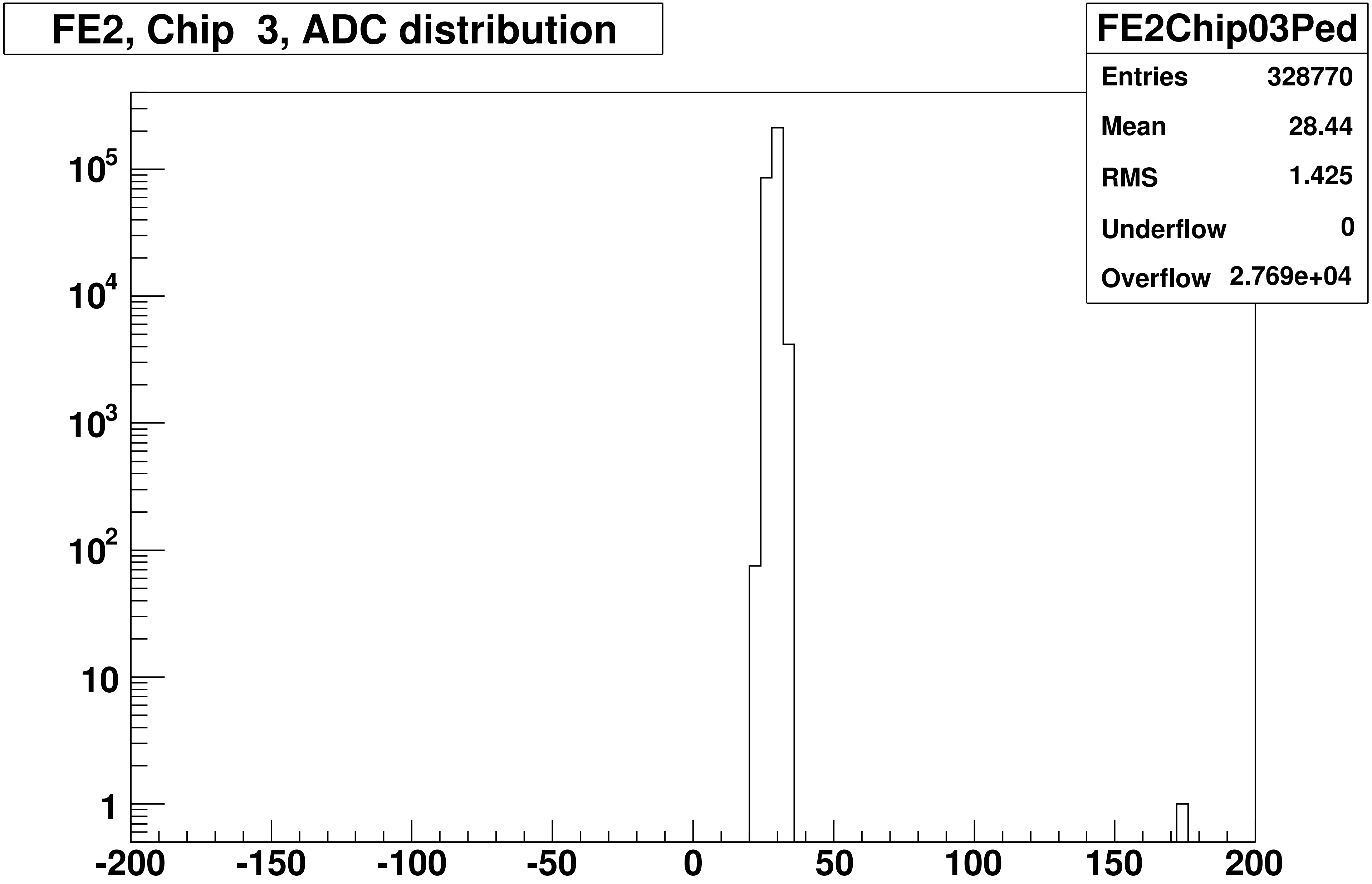

FE2, Chip 2, ADC distribution
FE2Chip02All
Entries 328770
Mean 1542
RMS 5180
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE2, Chip 2, ADC distribution
FE2Chip02Ped
Entries 328770
Mean -6.241
RMS 1.38
Underflow 0
Overflow 2.7e+04
10^5
-200
-150
-100
-50
0
50
100
150
200



FE2, Chip 2, ADC distribution
FE2Chip02Sig
Entries 328770
Mean 1.887e+04
RMS 6.972
Underflow 3.018e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE2, Chip 3, ADC distribution
FE2Chip03All
Entries 328770
Mean 1594
RMS 5200
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE2, Chip 3, ADC distribution
FE2Chip03Ped
Entries 328770
Mean 28.44
RMS 1.425
Underflow 0
Overflow 2.769e+04
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10^4
10^3
10^2
10
1
-200
-150
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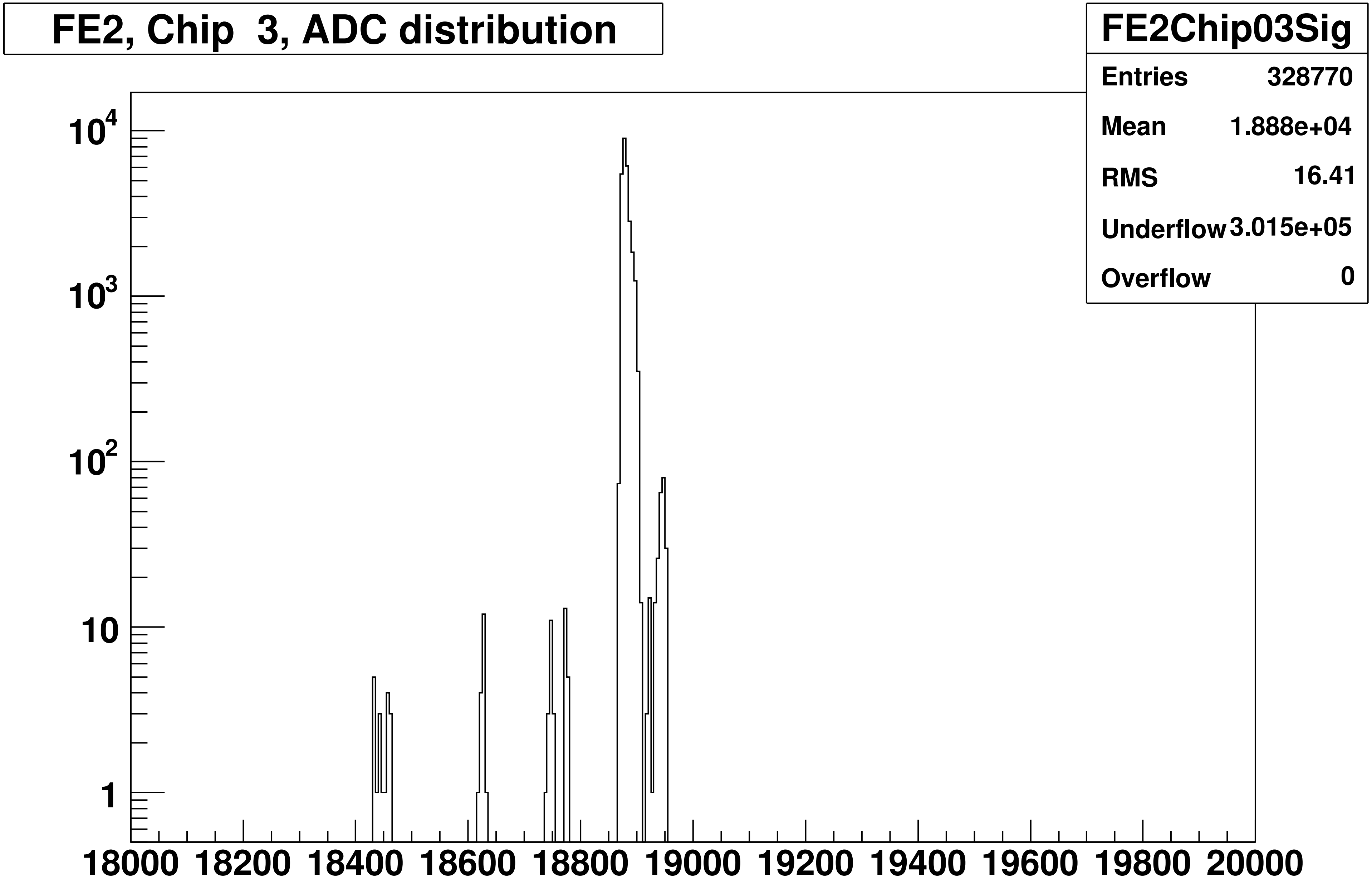
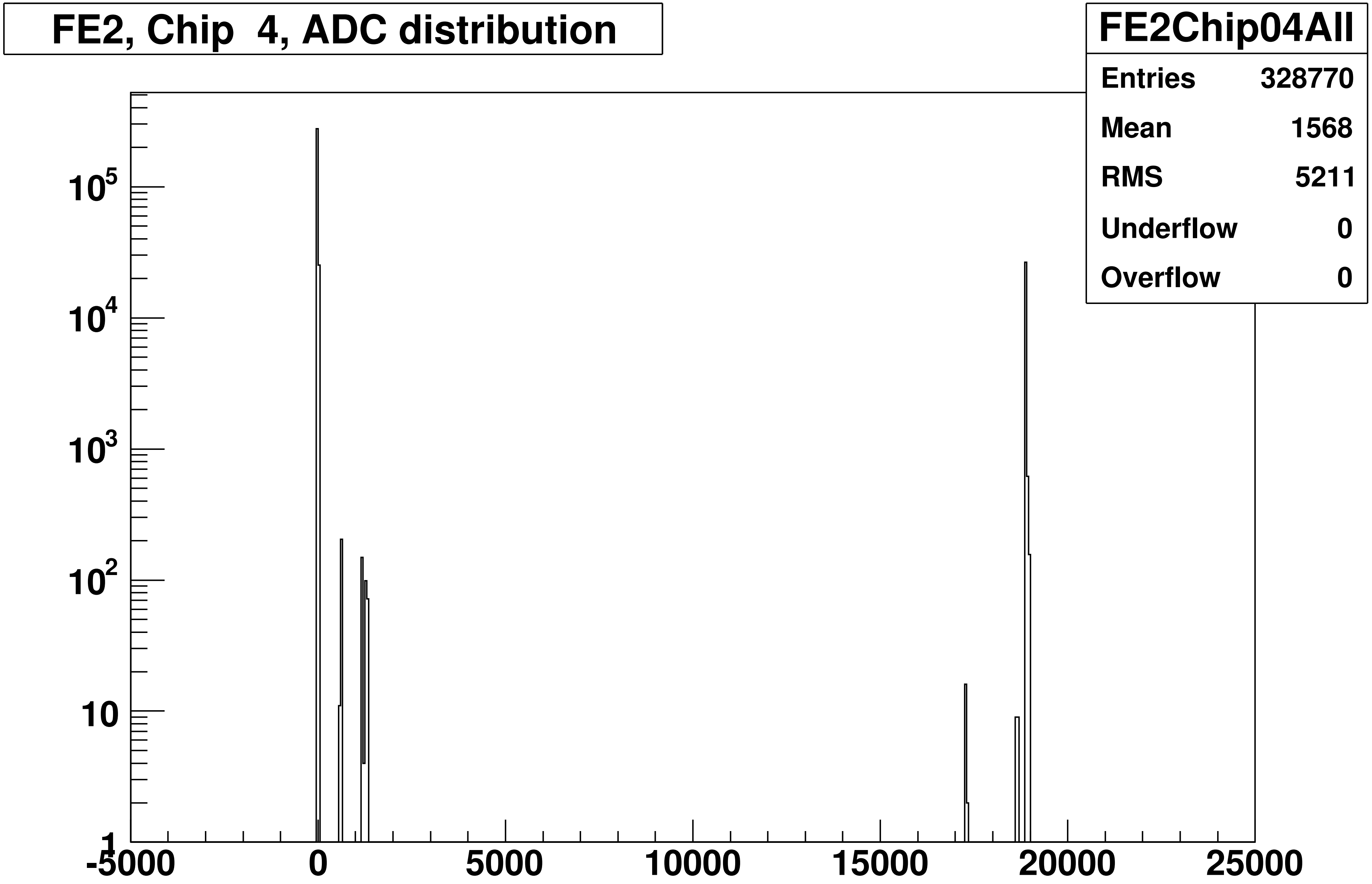
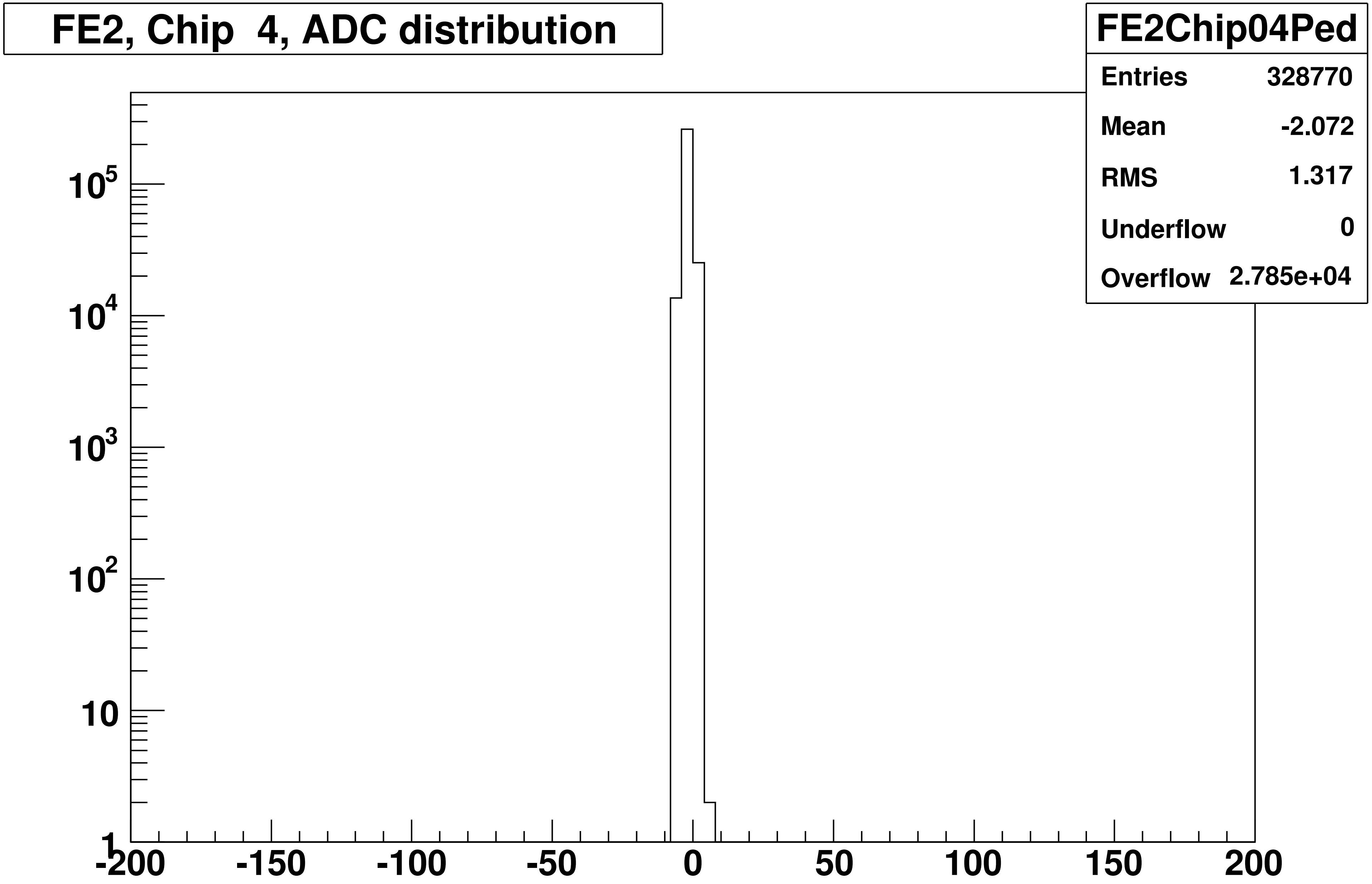
0
50
100
150
200


FE2, Chip 3, ADC distribution
FE2Chip03Sig
Entries 328770
Mean 1.888e+04
RMS 16.41
Underflow 3.015e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE2, Chip 4, ADC distribution
FE2Chip04All
Entries 328770
Mean 1568
RMS 5211
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE2, Chip 4, ADC distribution
FE2Chip04Ped
Entries 328770
Mean -2.072
RMS 1.317
Underflow 0
Overflow 2.785e+04
1
10
10^2
10^3
10^4
10^5
-200
-150
-100
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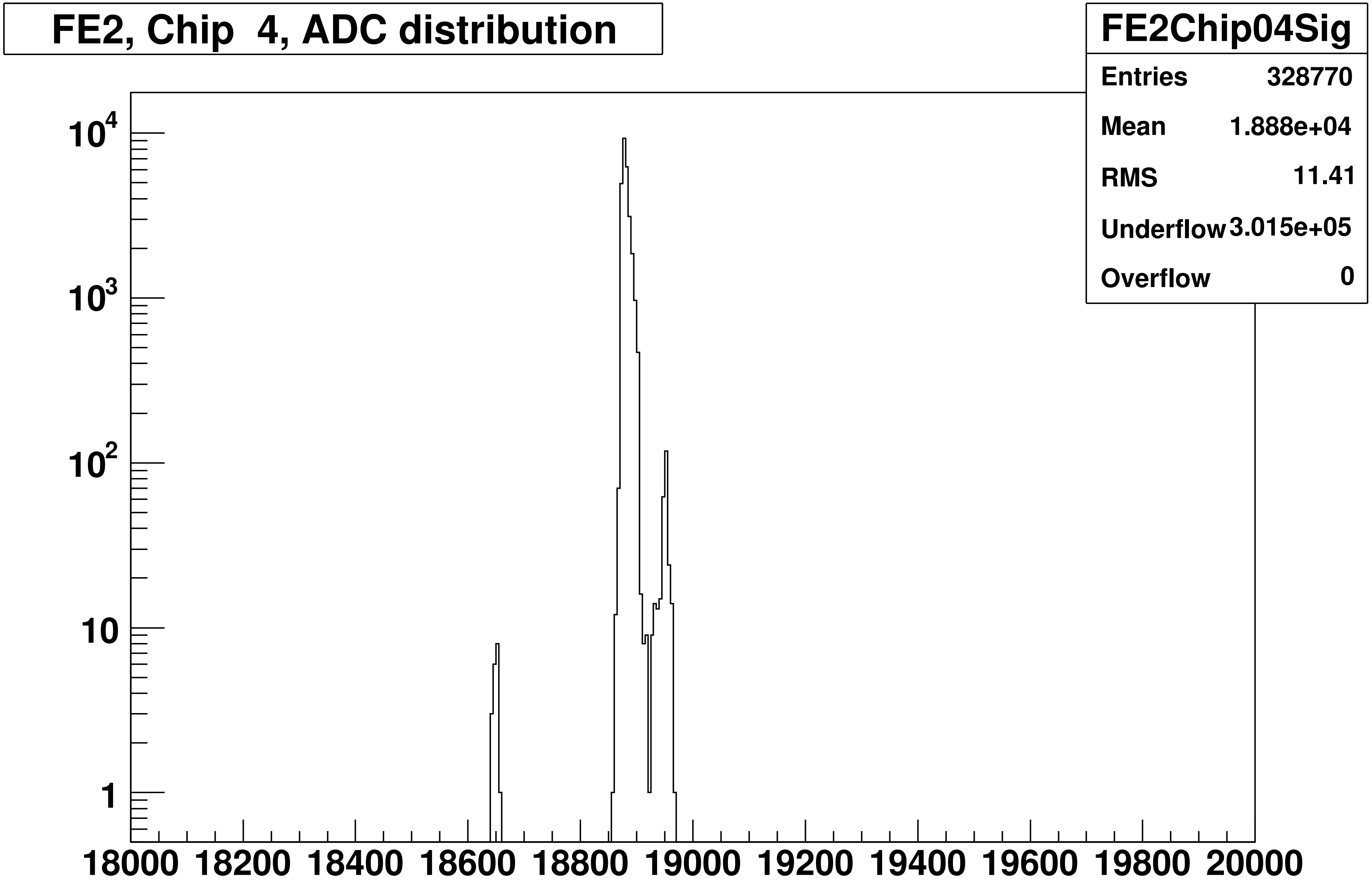
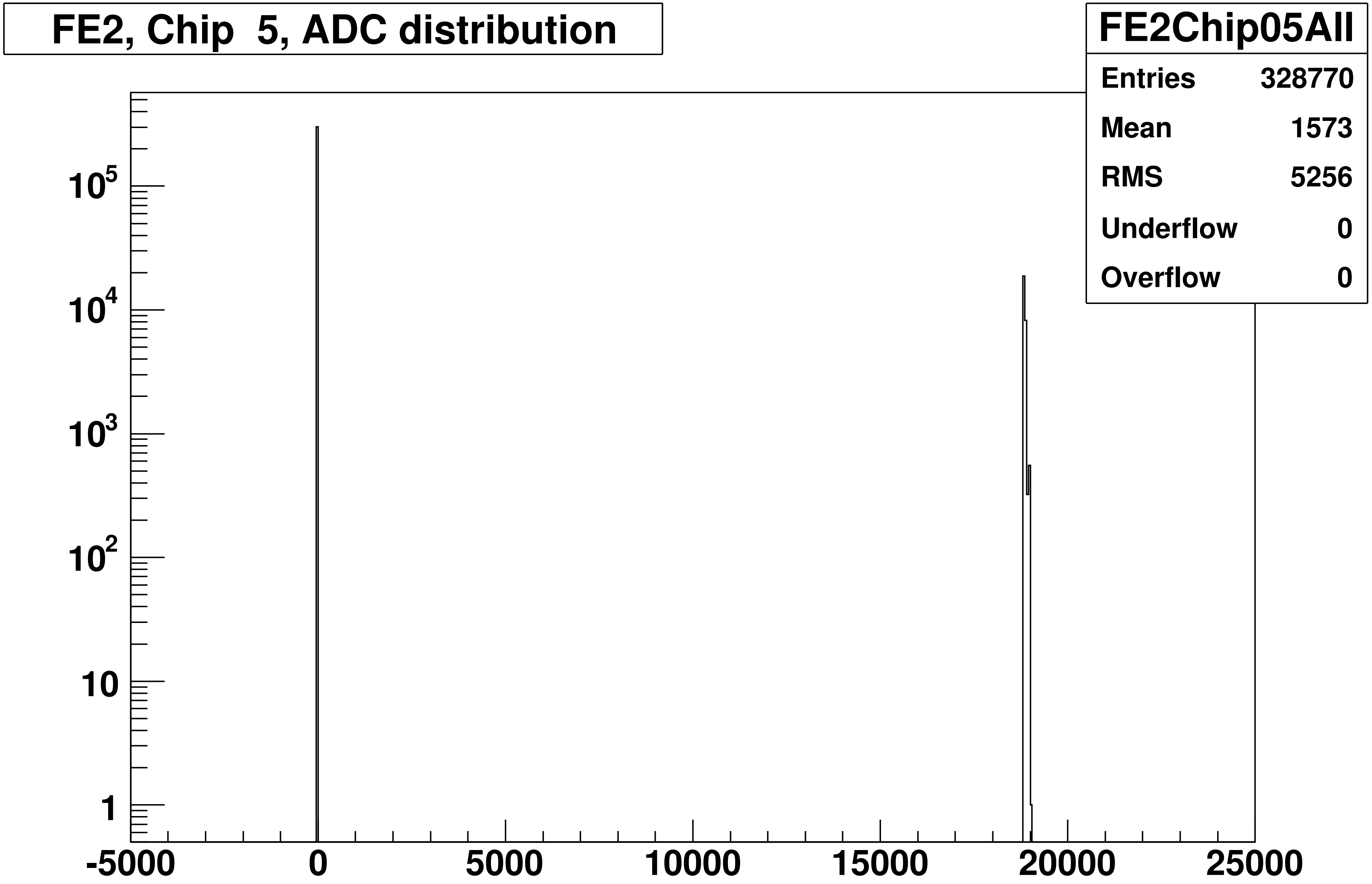
0
50
100
150
200



FE2, Chip 4, ADC distribution
FE2Chip04Sig
Entries 328770
Mean 1.888e+04
RMS 11.41
Underflow 3.015e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE2, Chip 5, ADC distribution
FE2Chip05All
Entries 328770
Mean 1573
RMS 5256
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
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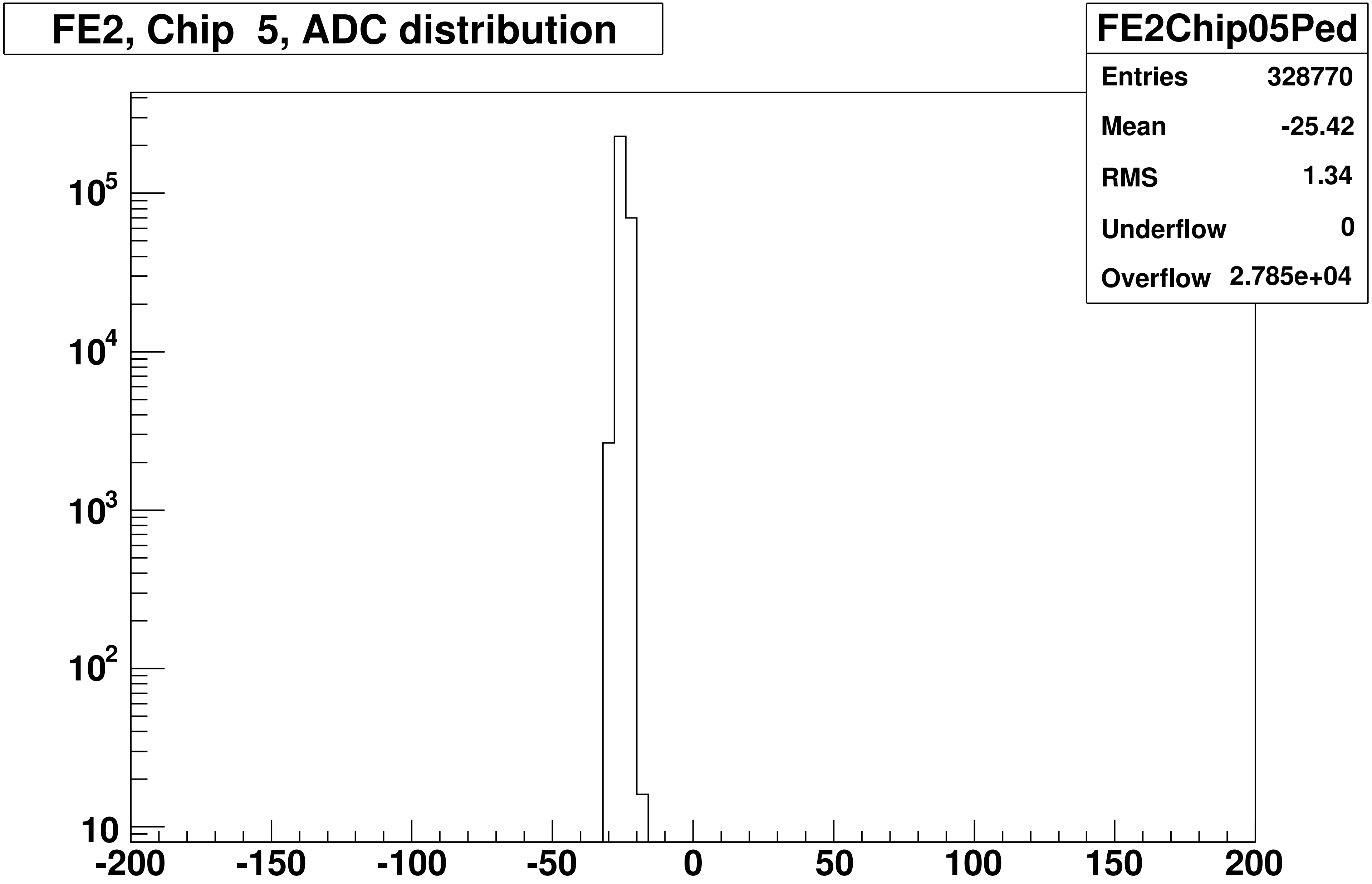
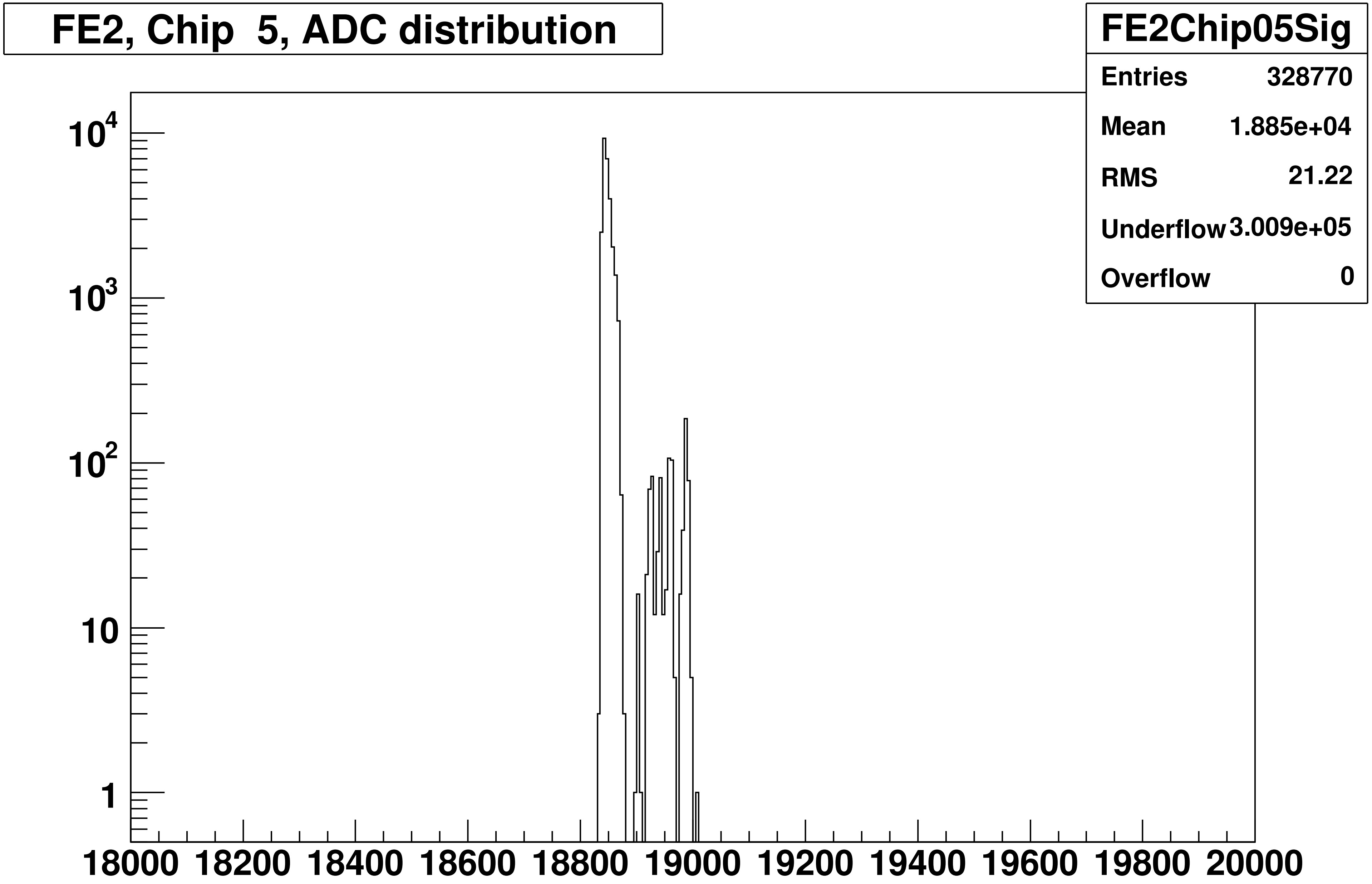
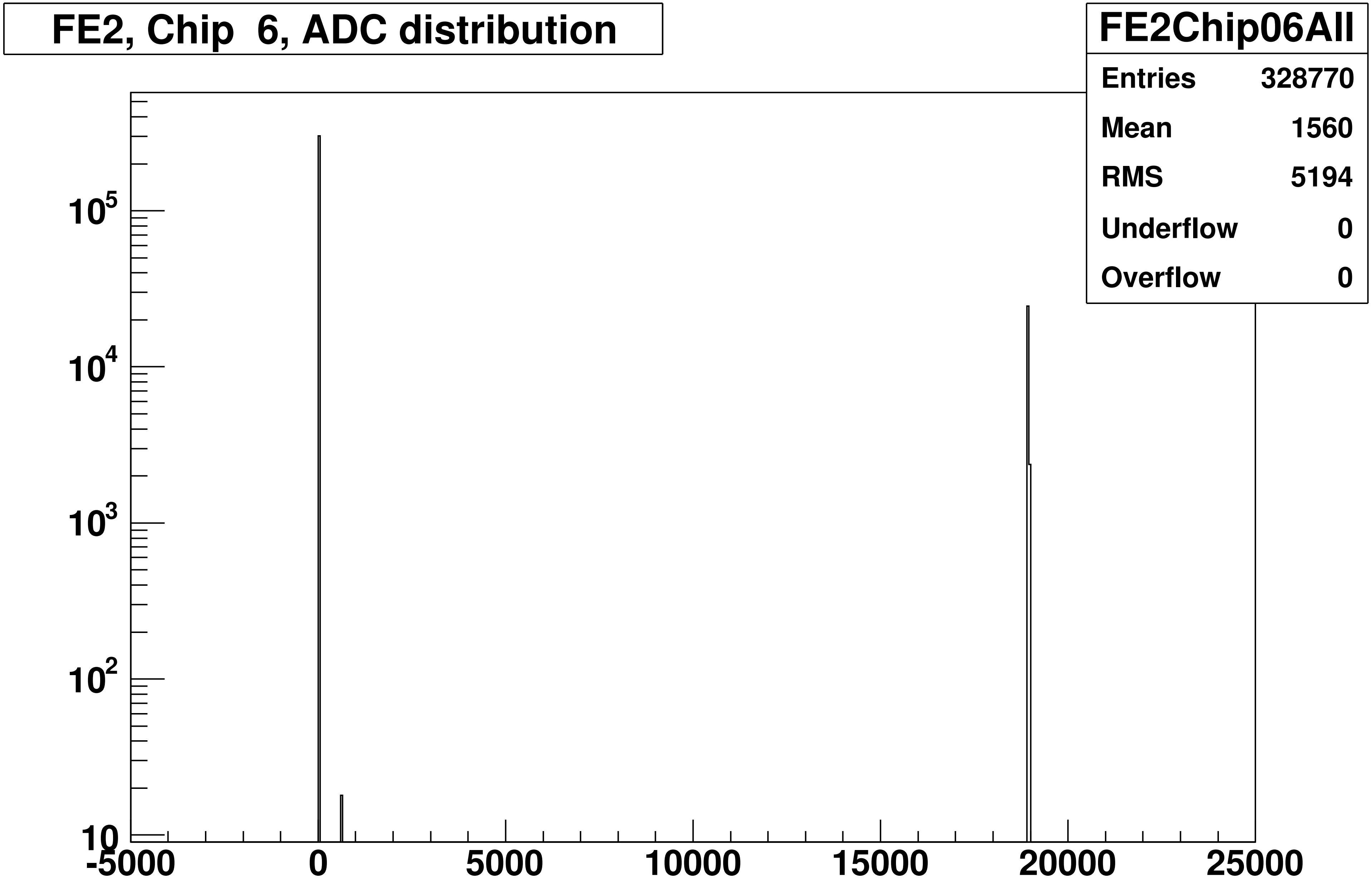
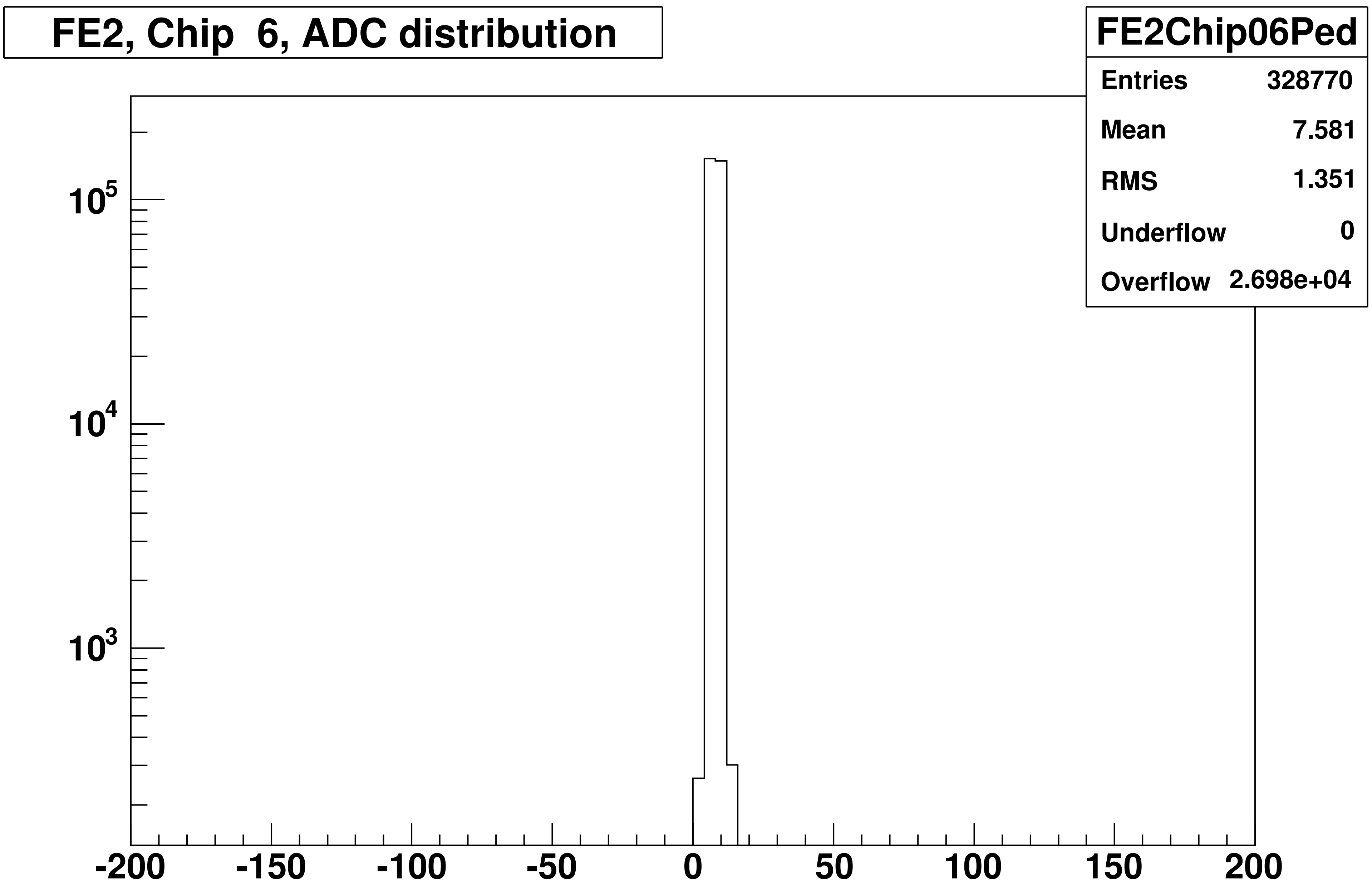
10000
15000
20000
25000


FE2, Chip 5, ADC distribution
FE2Chip05Ped
Entries 328770
Mean -25.42
RMS 1.34
Underflow 0
Overflow 2.785e+04
10
10^2
10^3
10^4
10^5
-200
-150
-100
-50
0
50
100
150
200

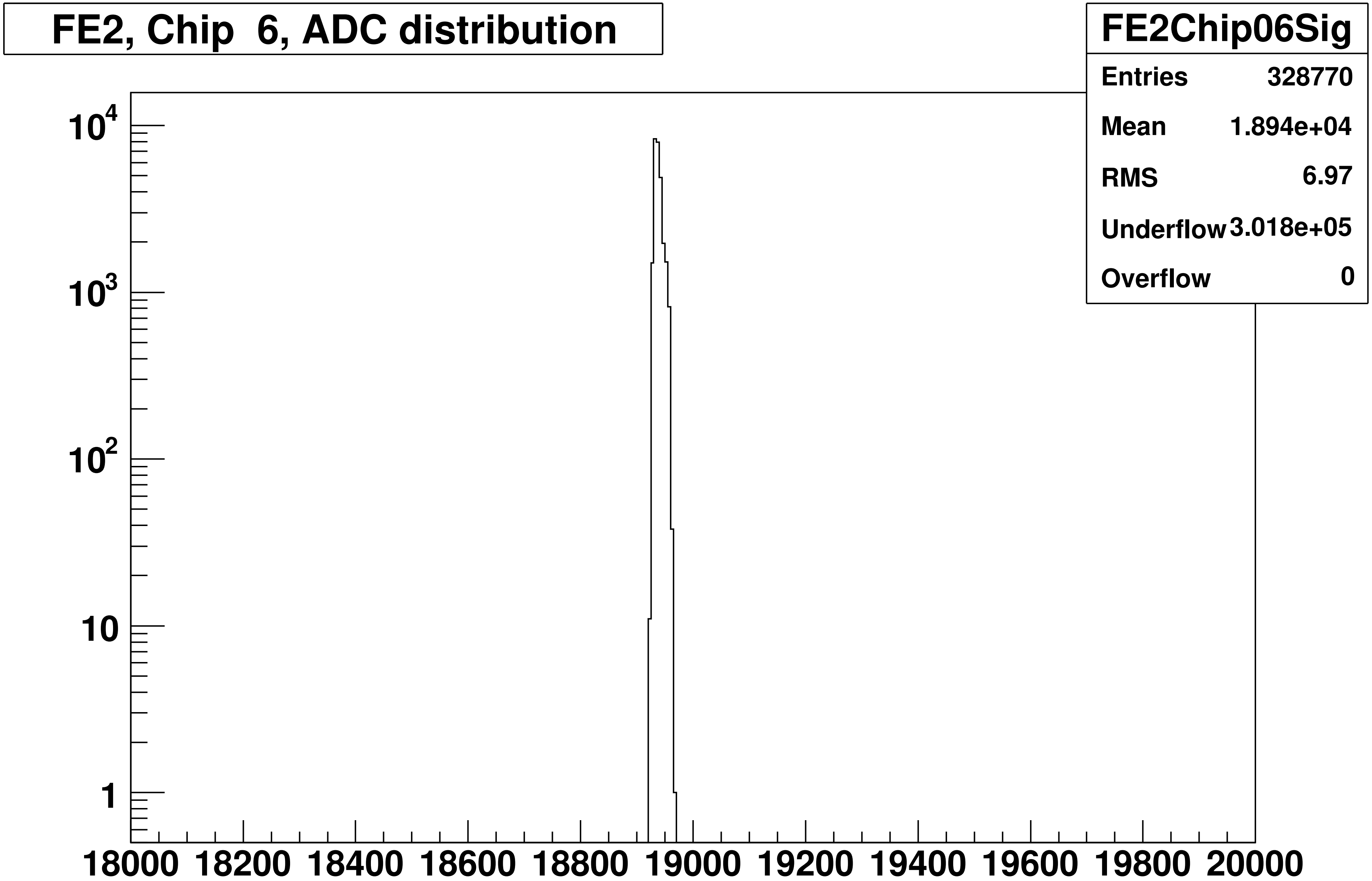

FE2, Chip 5, ADC distribution
FE2Chip05Sig
Entries 328770
Mean 1.885e+04
RMS 21.22
Underflow 3.009e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000

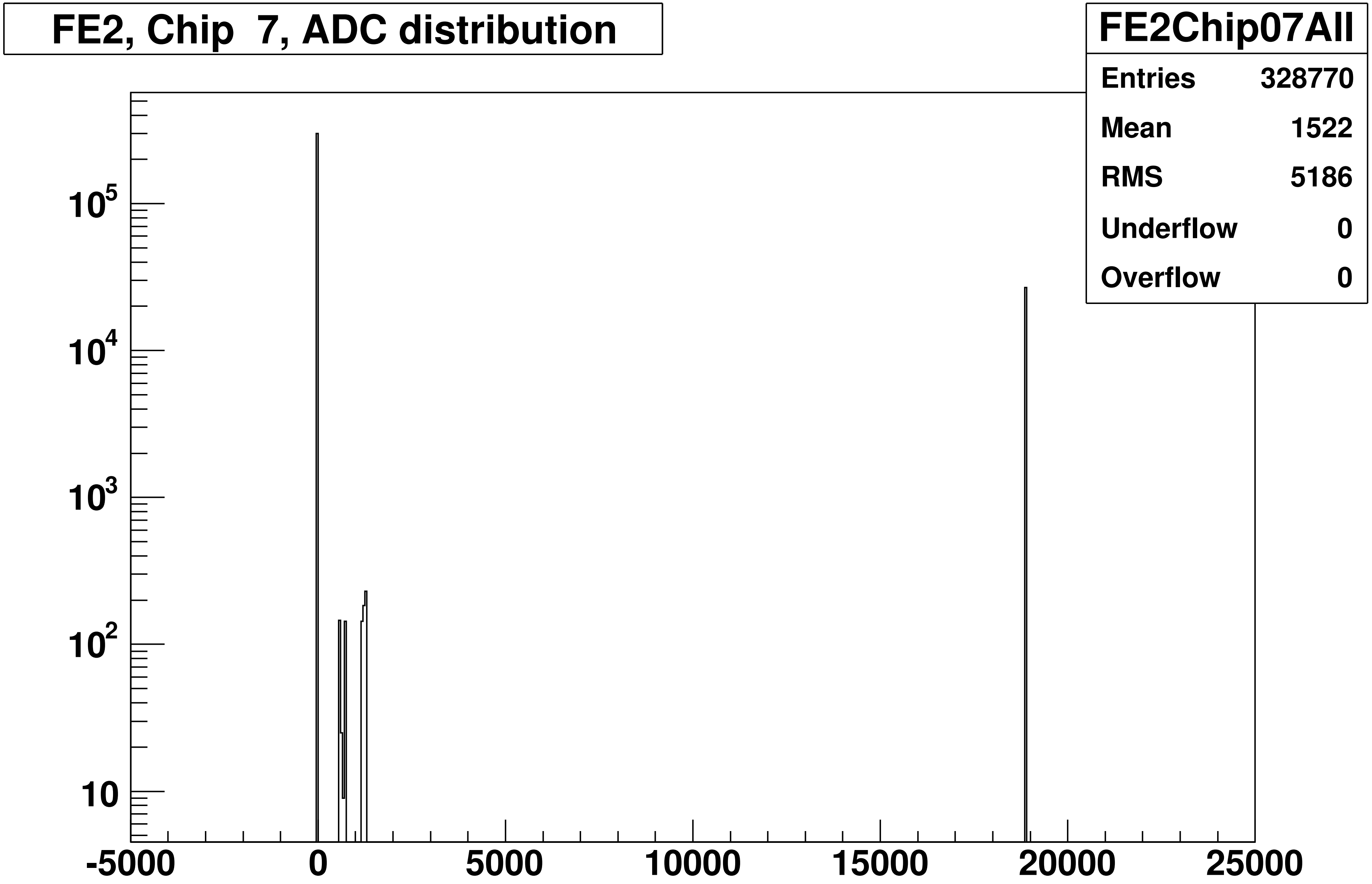


FE2, Chip 6, ADC distribution
FE2Chip06All
Entries 328770
Mean 1560
RMS 5194
Underflow 0
Overflow 0
10
10^2
10^3
10^4
10^5
-5000
0
5000
10000
15000
20000
25000

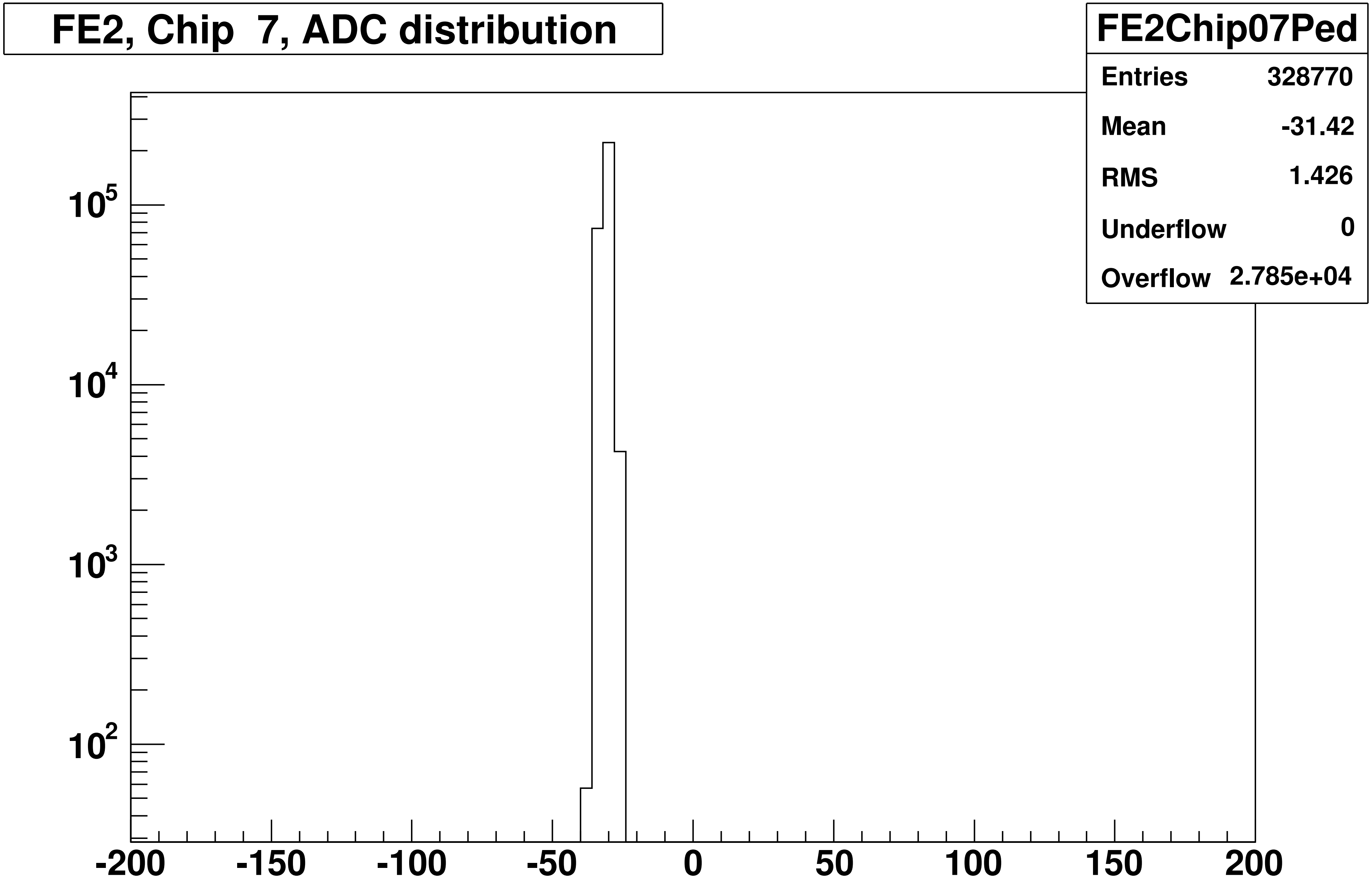


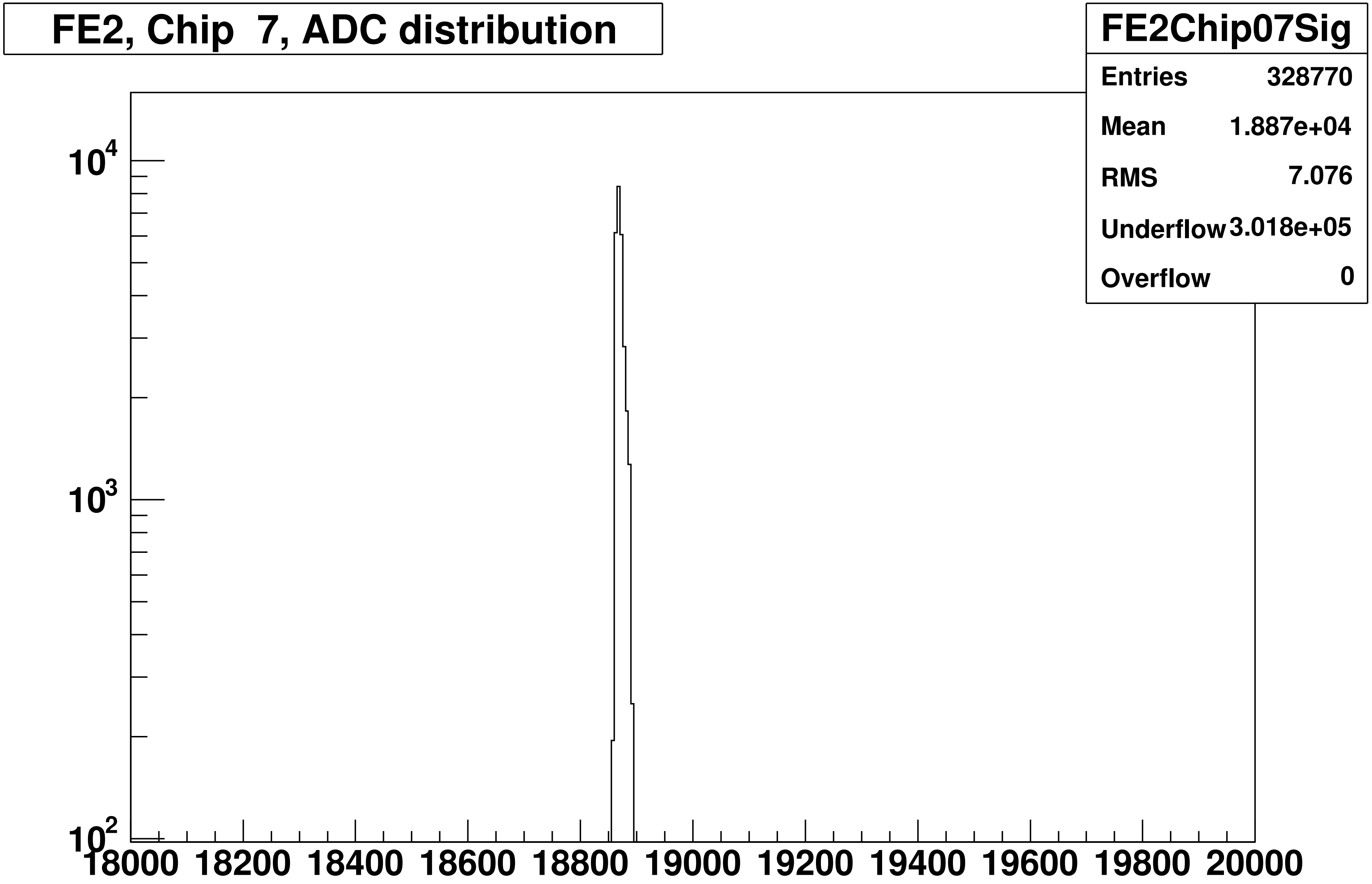
FE2, Chip 6, ADC distribution
FE2Chip06Ped
Entries 328770
Mean 7.581
RMS 1.351
Underflow 0
Overflow 2.698e+04
10^5
10^4
10^3
-200
-150
-100
-50
0
50
100
150
200


FE2, Chip 6, ADC distribution
FE2Chip06Sig
Entries 328770
Mean 1.894e+04
RMS 6.97
Underflow 3.018e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000

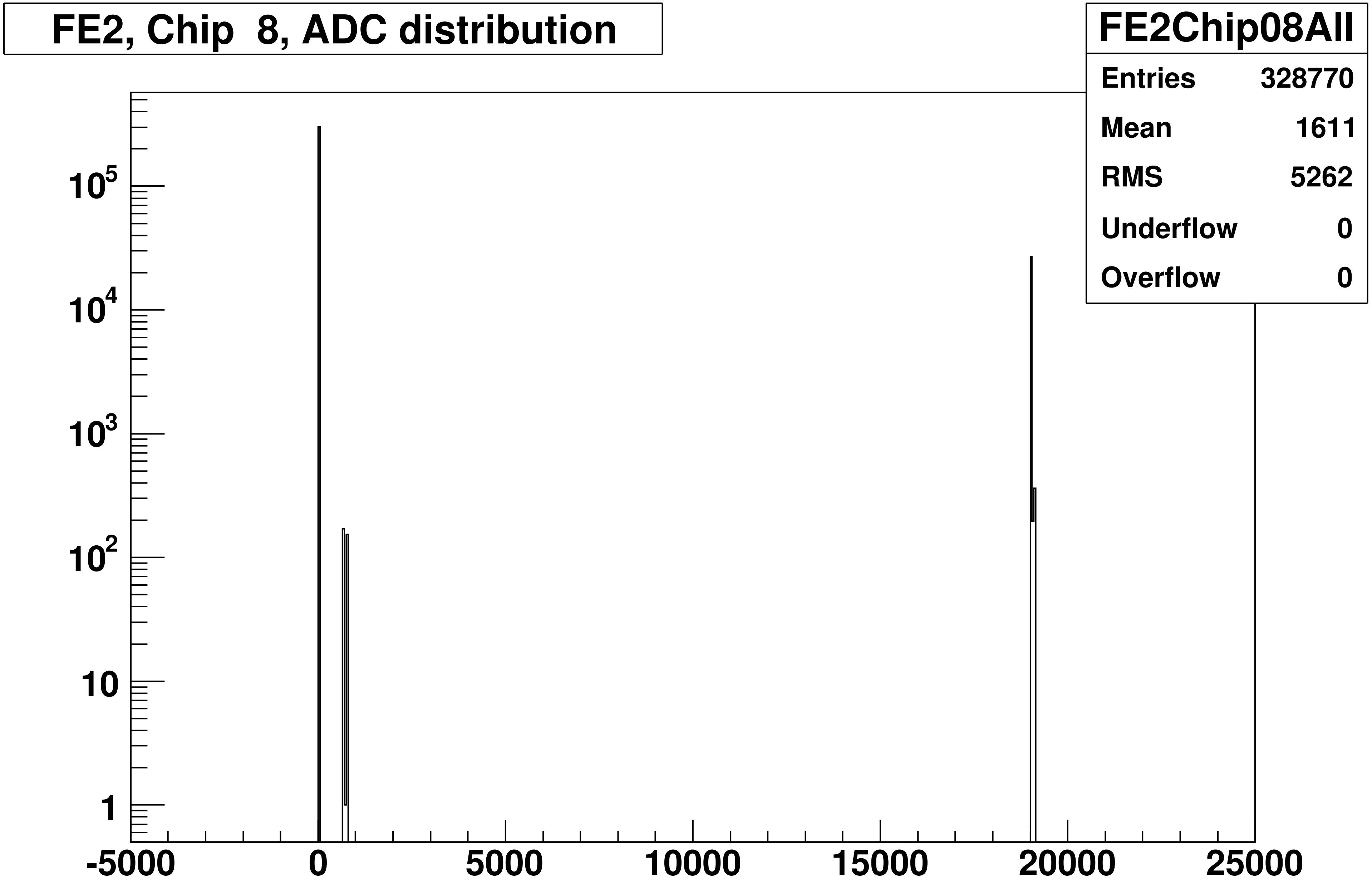


FE2, Chip 7, ADC distribution
FE2Chip07All
Entries 328770
Mean 1522
RMS 5186
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000

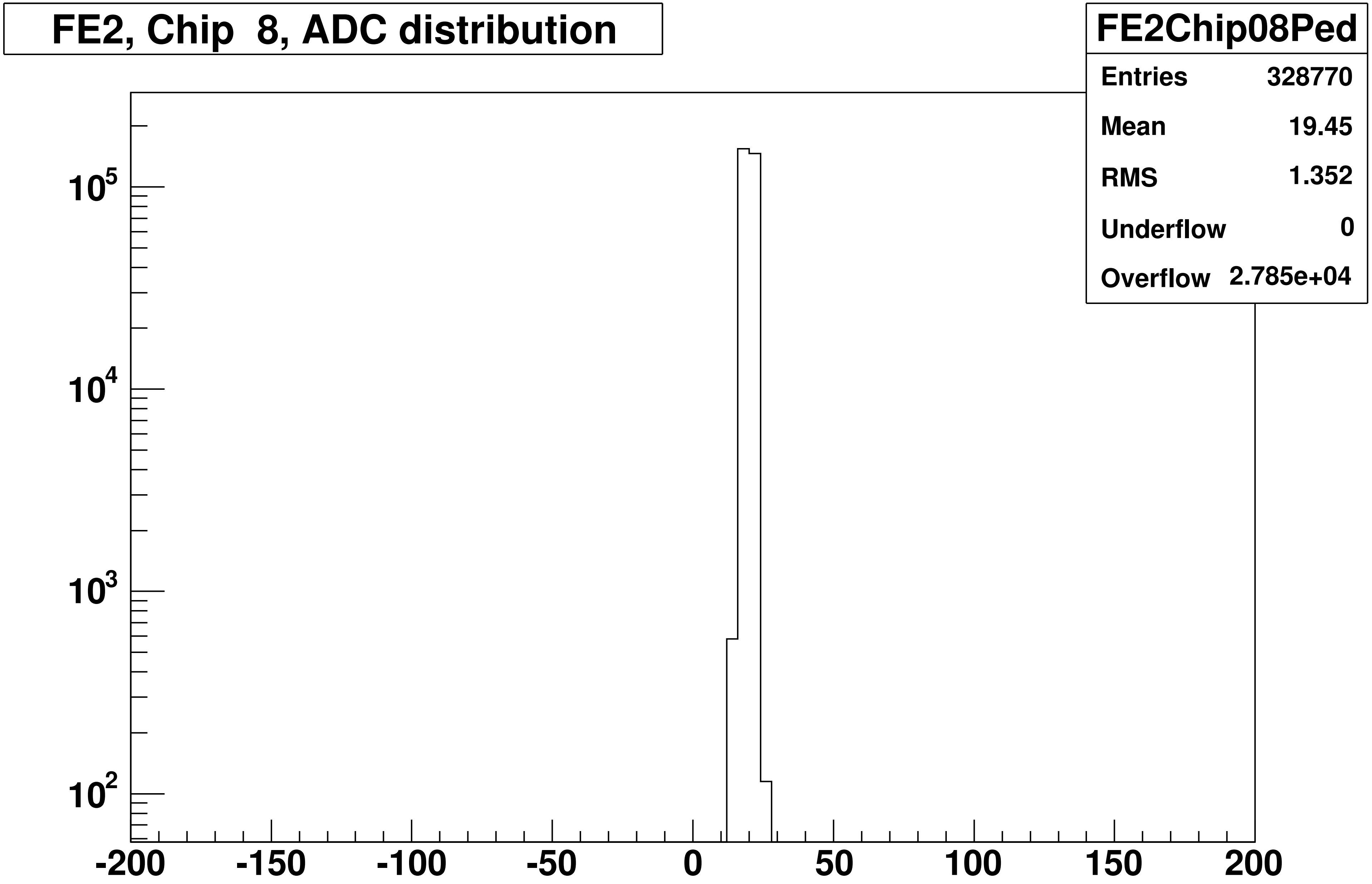

FE2, Chip 7, ADC distribution
FE2Chip07Ped
Entries 328770
Mean -31.42
RMS 1.426
Underflow 0
Overflow 2.785e+04
10^5
10^4
10^3
10^2
-200 -150 -100 -50 0 50 100 150 200

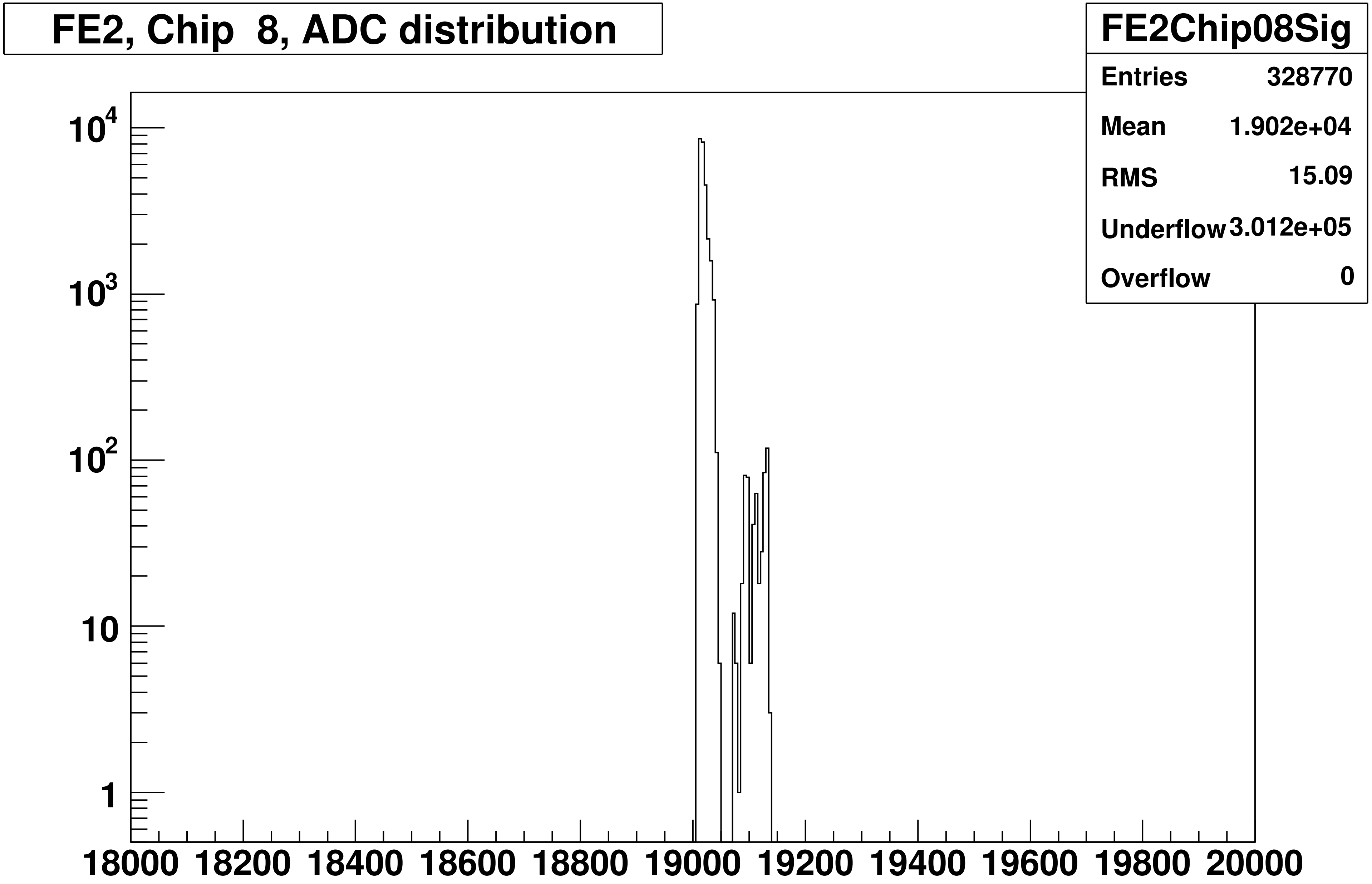


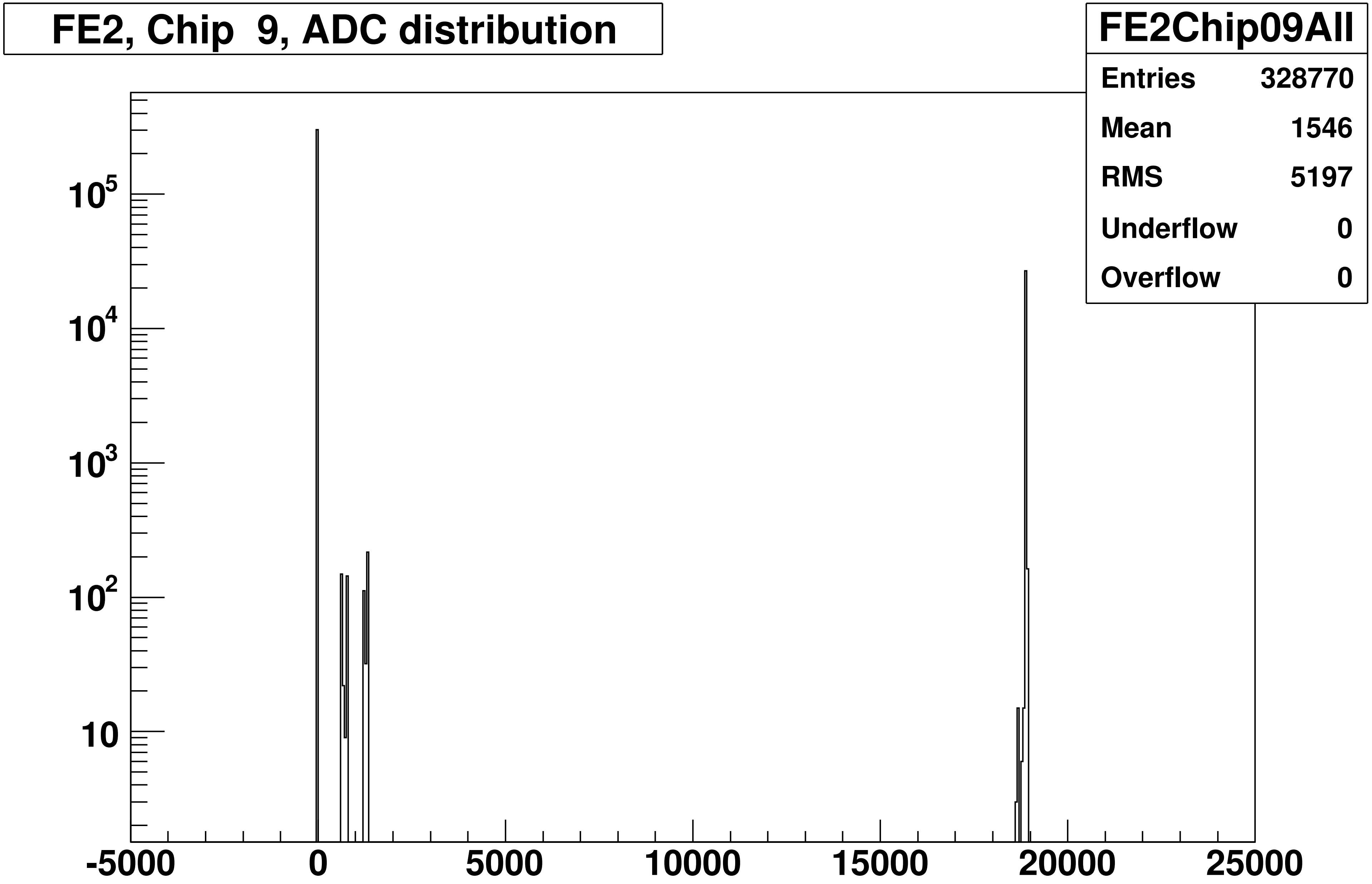
FE2, Chip 7, ADC distribution
FE2Chip07Sig
Entries 328770
Mean 1.887e+04
RMS 7.076
Underflow 3.018e+05
Overflow 0
10^4
10^3
10^2
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000



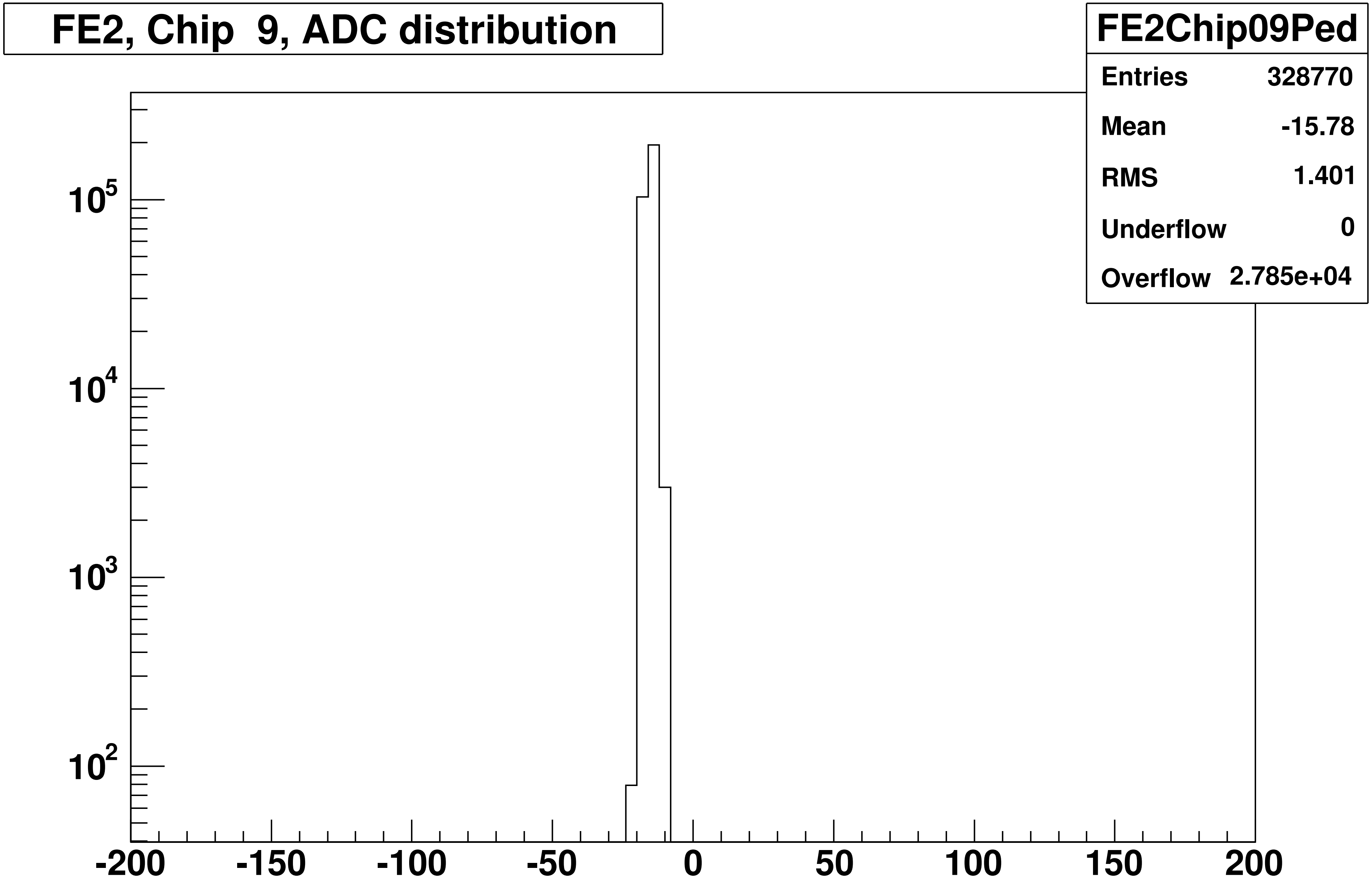
FE2, Chip 8, ADC distribution
FE2Chip08All
Entries 328770
Mean 1611
RMS 5262
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000

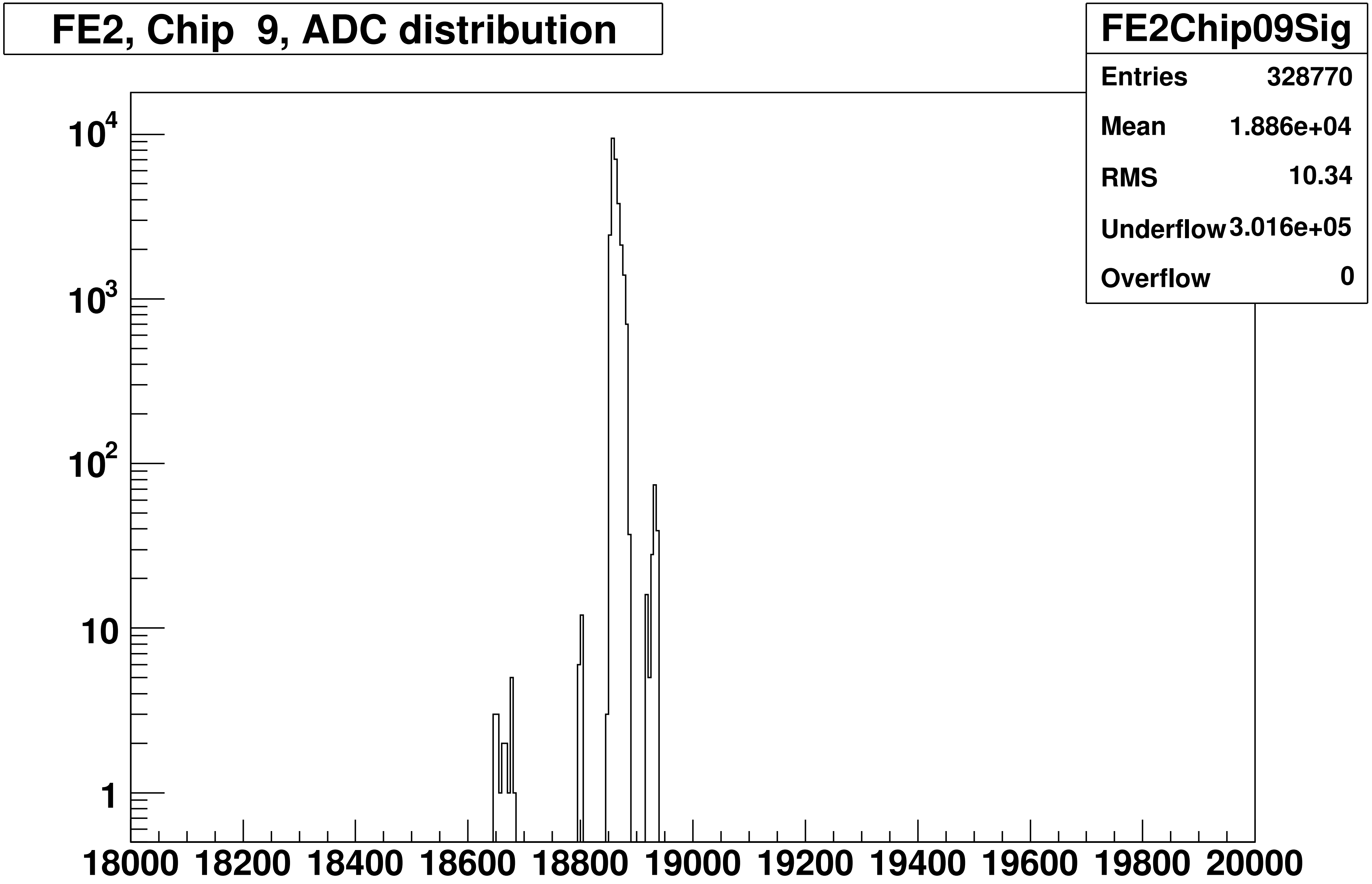

FE2, Chip 8, ADC distribution
FE2Chip08Ped
Entries 328770
Mean 19.45
RMS 1.352
Underflow 0
Overflow 2.785e+04
10^5
10^4
10^3
10^2
-200
-150
-100
-50
0
50
100
150
200


FE2, Chip 8, ADC distribution
FE2Chip08Sig
Entries 328770
Mean 1.902e+04
RMS 15.09
Underflow 3.012e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000

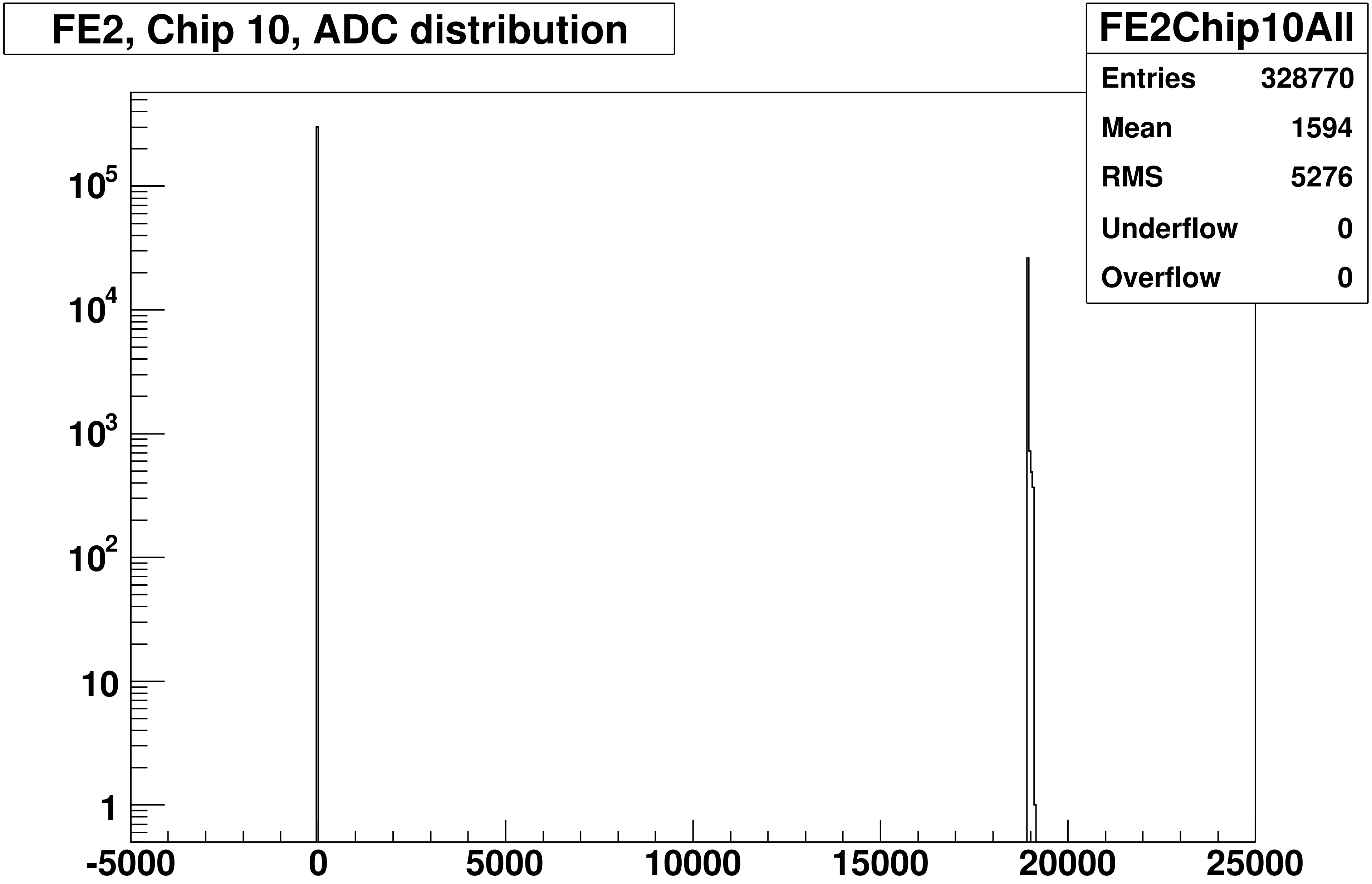


FE2, Chip 9, ADC distribution
FE2Chip09All
Entries 328770
Mean 1546
RMS 5197
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE2, Chip 9, ADC distribution
FE2Chip09Ped
Entries 328770
Mean -15.78
RMS 1.401
Underflow 0
Overflow 2.785e+04
10^5
10^4
10^3
10^2
-200
-150
-100
-50
0
50
100
150
200



FE2, Chip 9, ADC distribution
FE2Chip09Sig
Entries 328770
Mean 1.886e+04
RMS 10.34
Underflow 3.016e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000


FE2, Chip 10, ADC distribution
FE2Chip10All
Entries 328770
Mean 1594
RMS 5276
Underflow 0
Overflow 0
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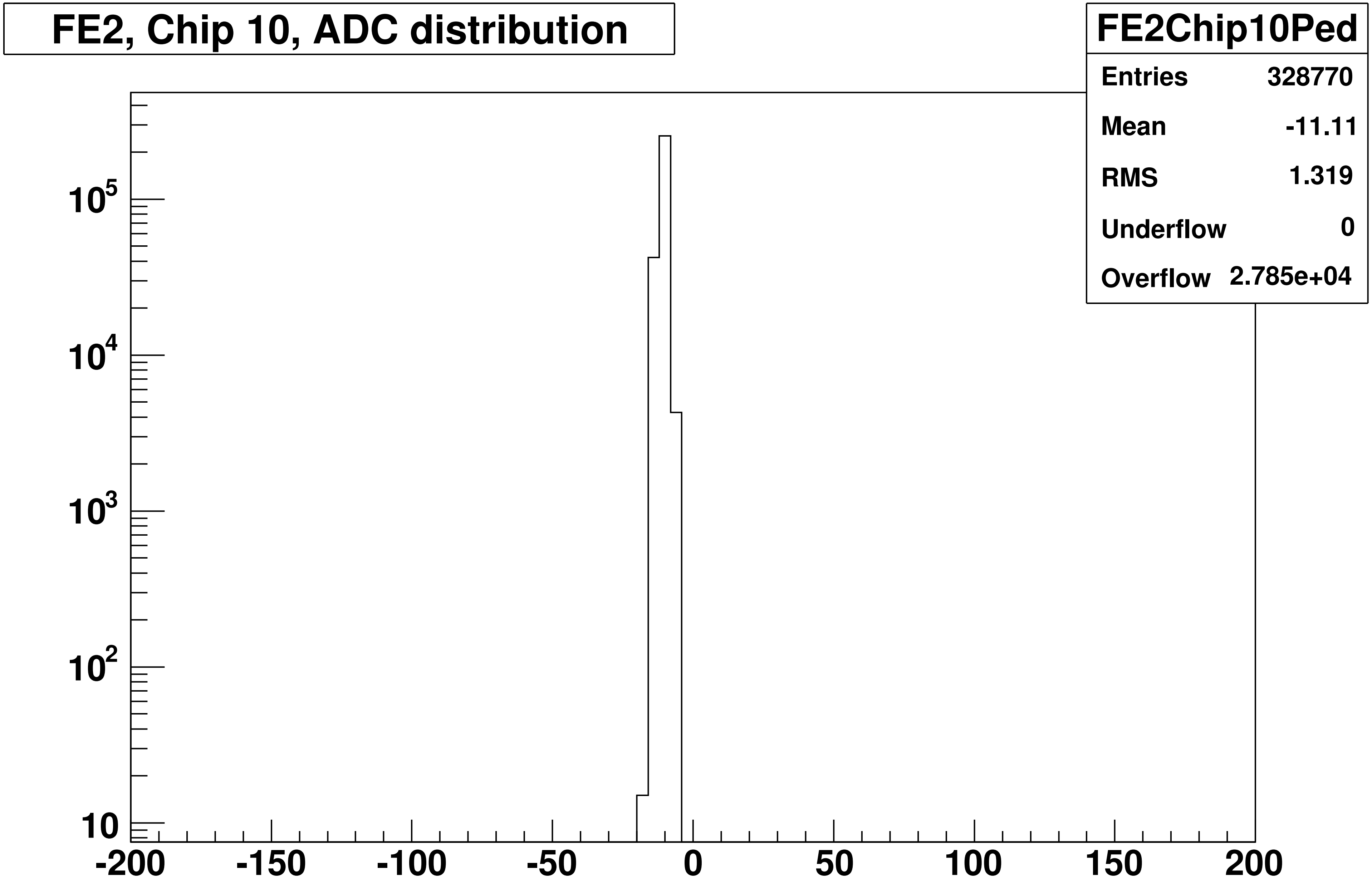
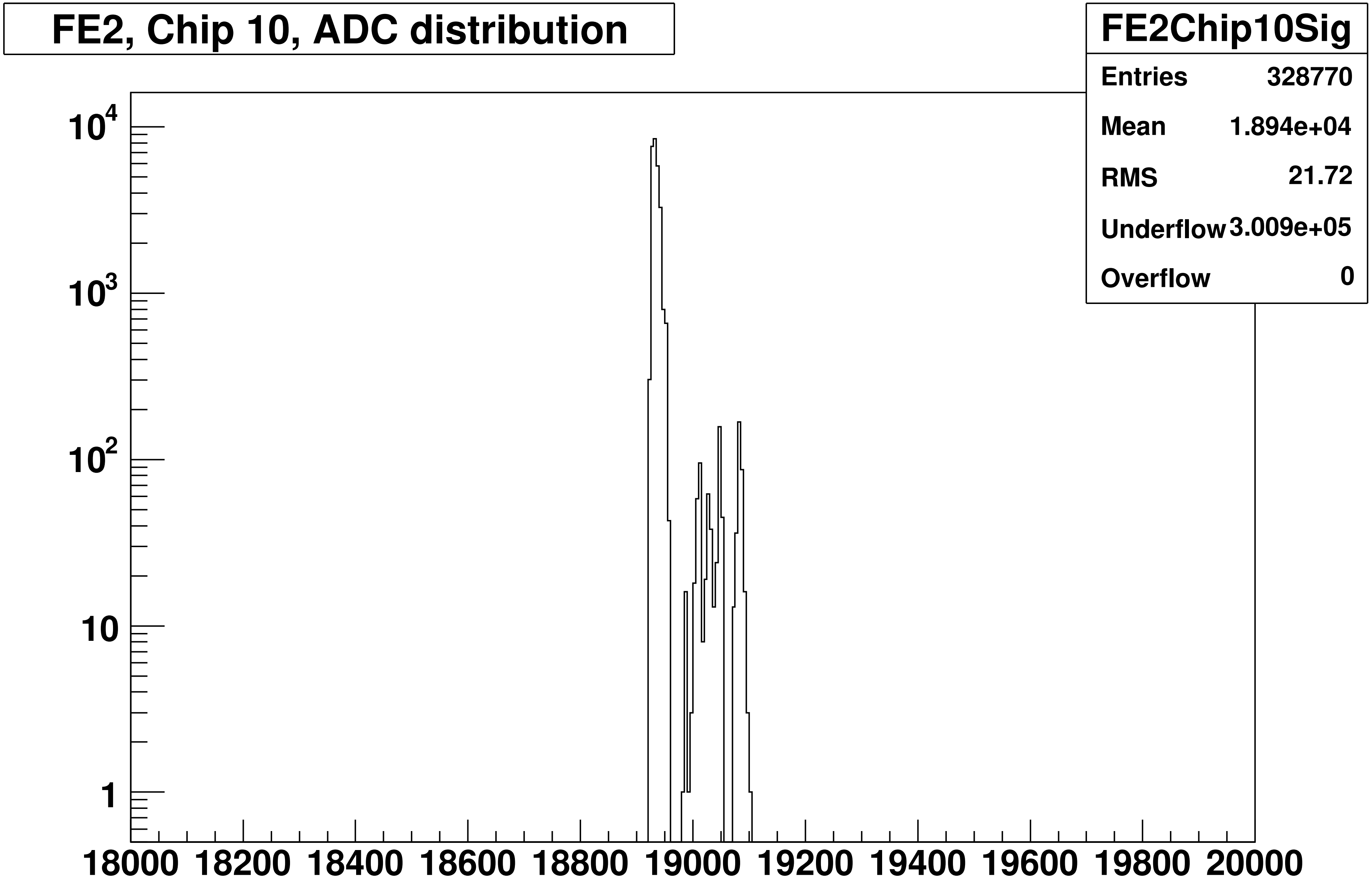
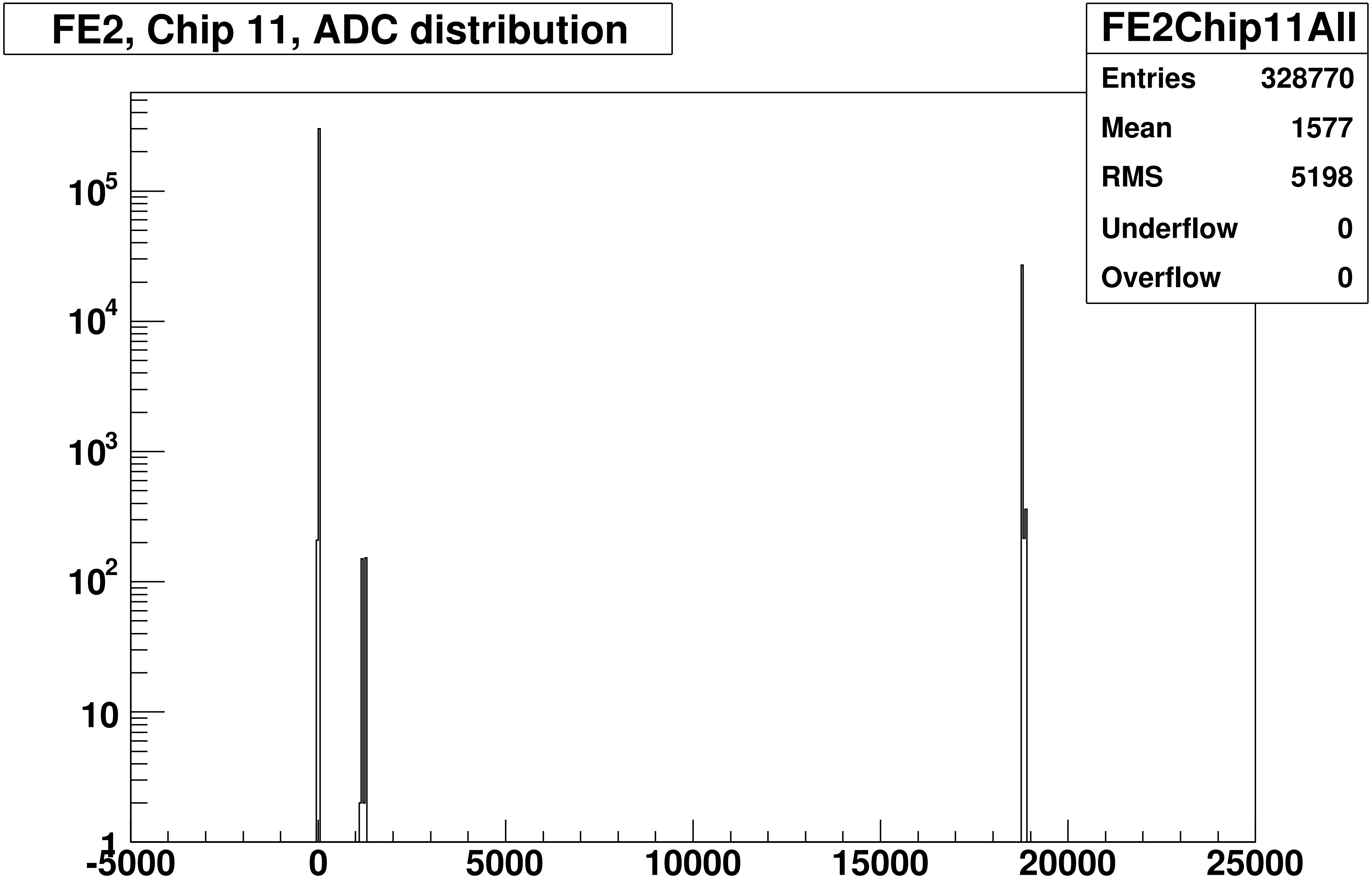
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE2, Chip 10, ADC distribution
FE2Chip10Ped
Entries 328770
Mean -11.11
RMS 1.319
Underflow 0
Overflow 2.785e+04
10
10^2
10^3
10^4
10^5
-200
-150
-100
-50
0
50
100
150
200



FE2, Chip 10, ADC distribution
FE2Chip10Sig
Entries 328770
Mean 1.894e+04
RMS 21.72
Underflow 3.009e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE2, Chip 11, ADC distribution
FE2Chip11All
Entries 328770
Mean 1577
RMS 5198
Underflow 0
Overflow 0
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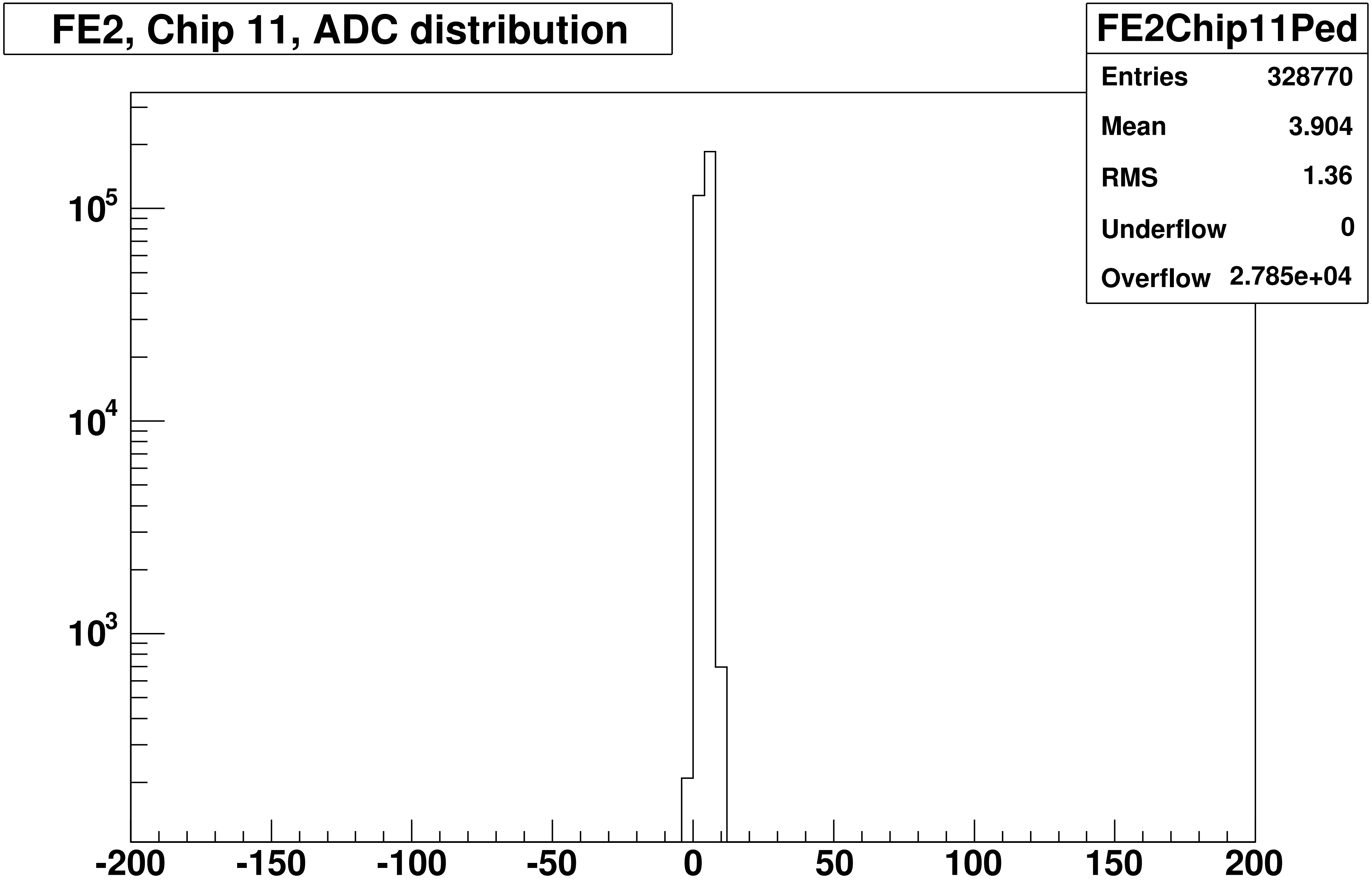
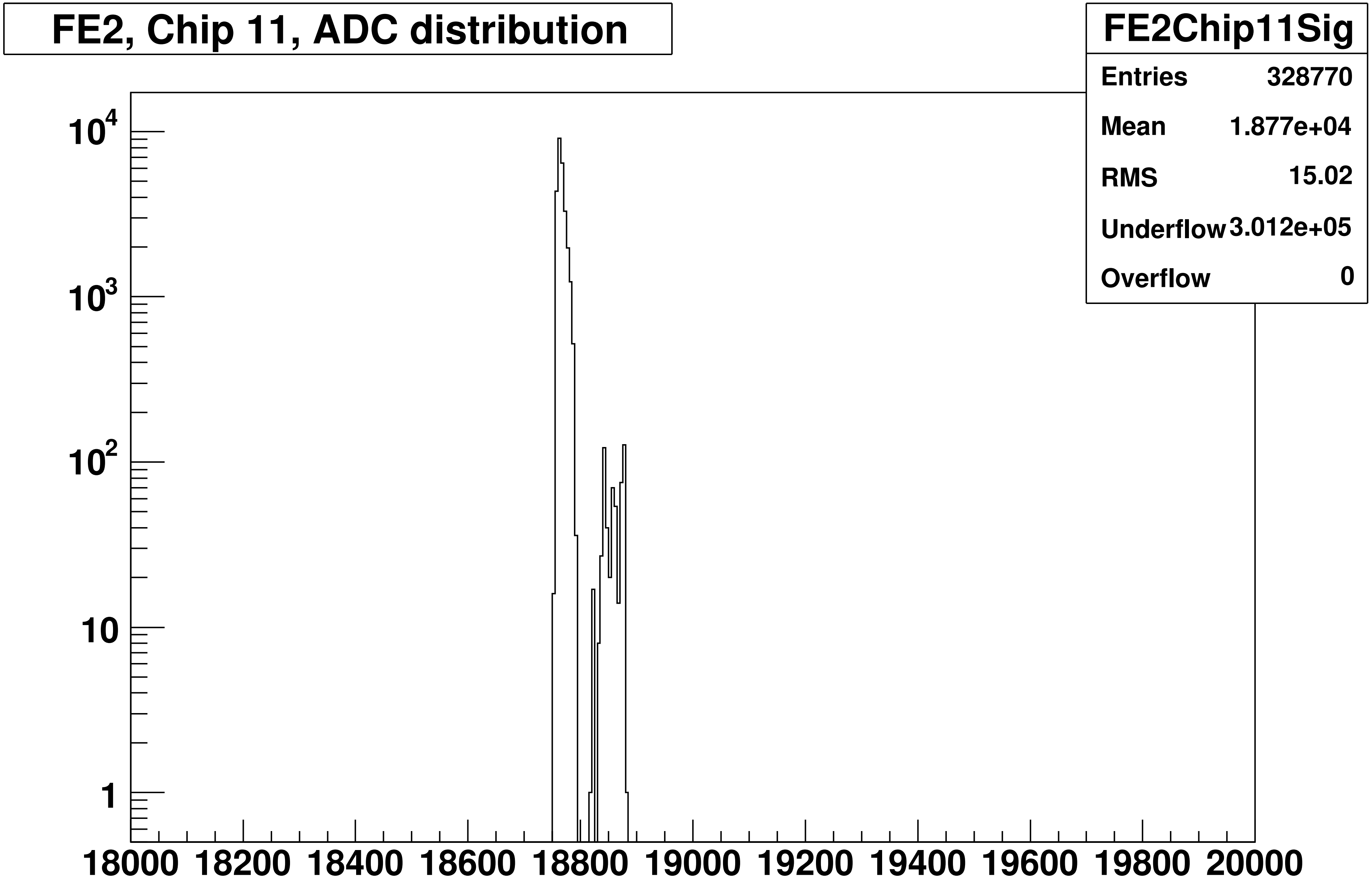
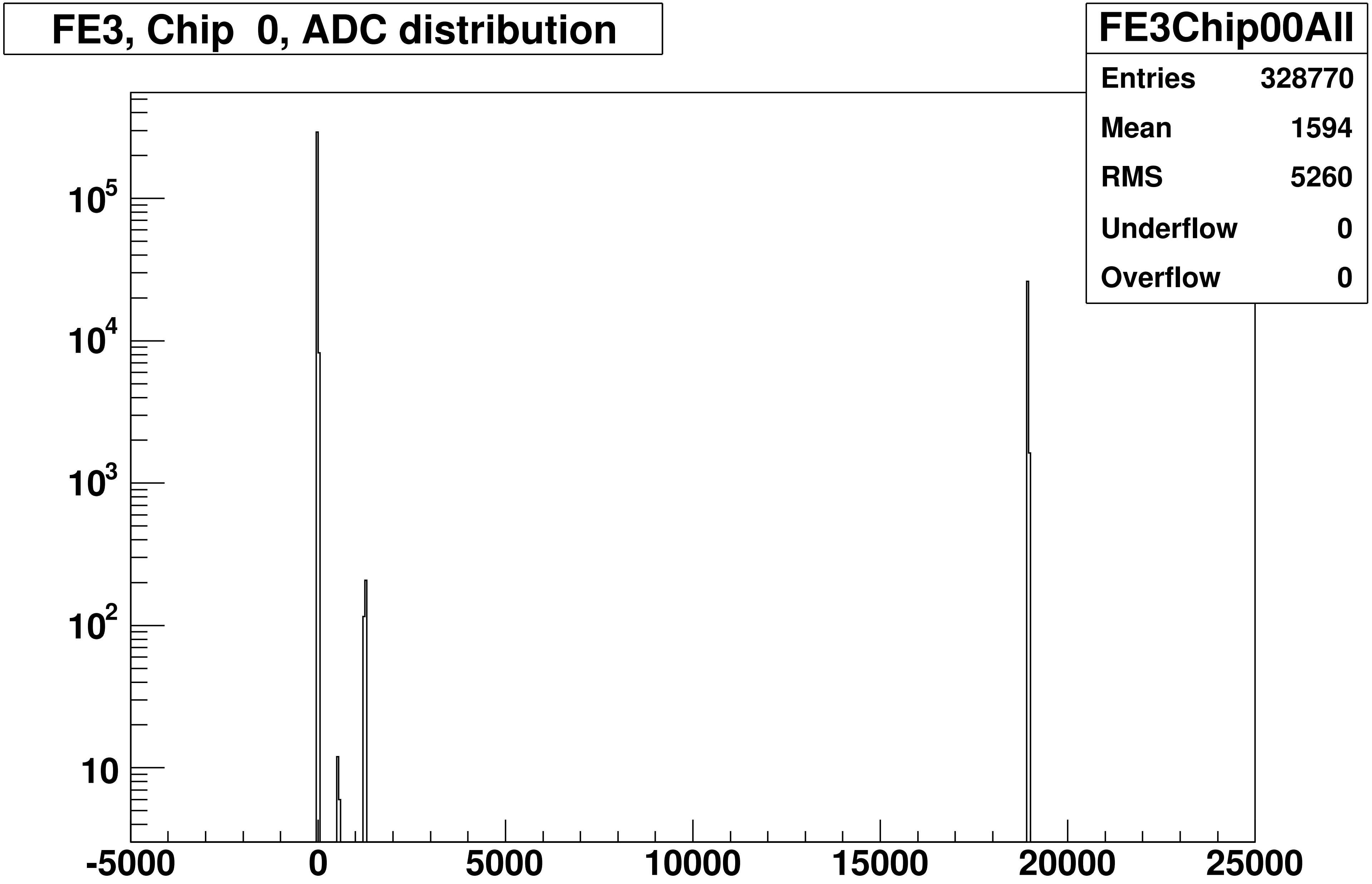
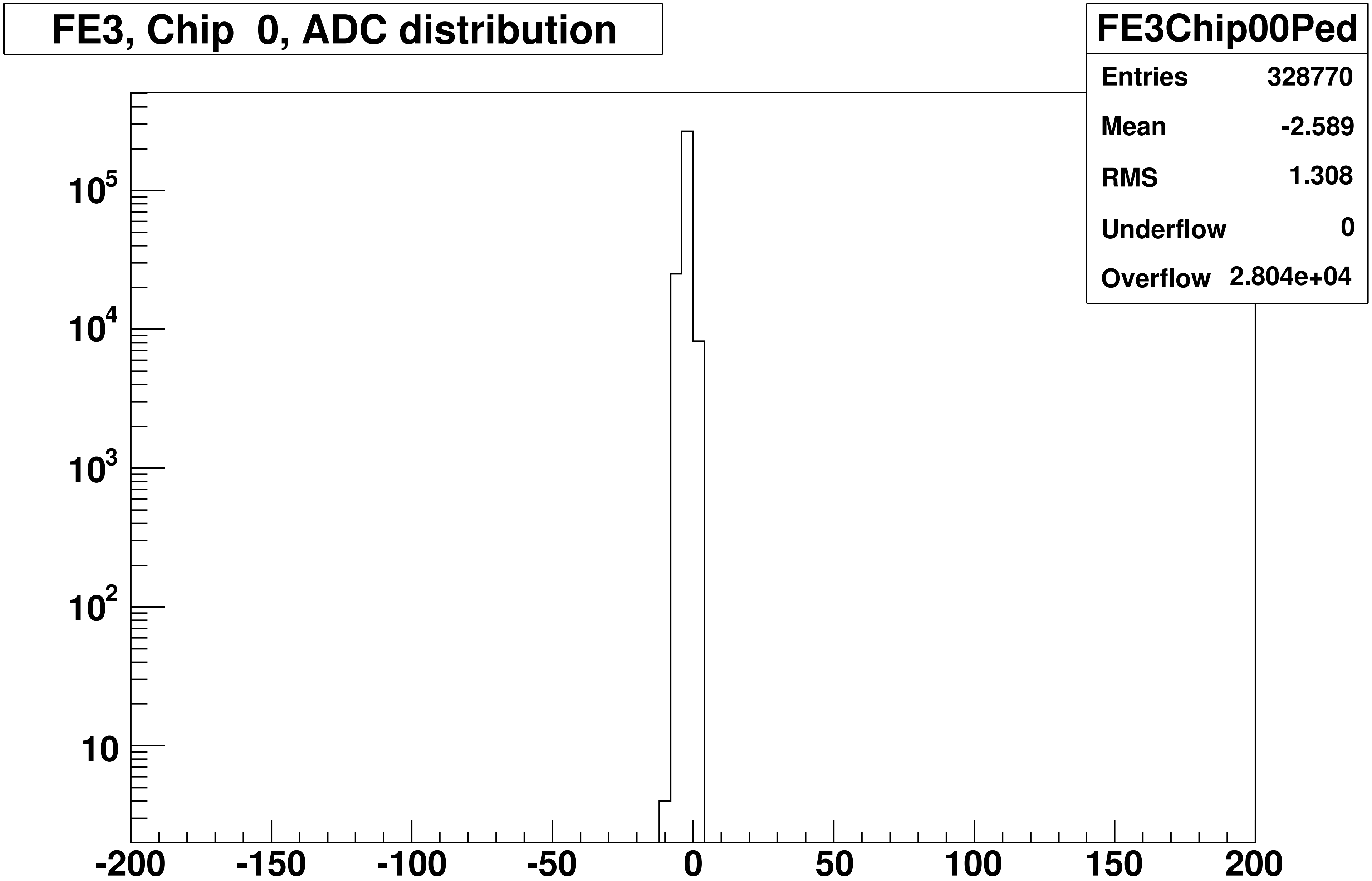
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000

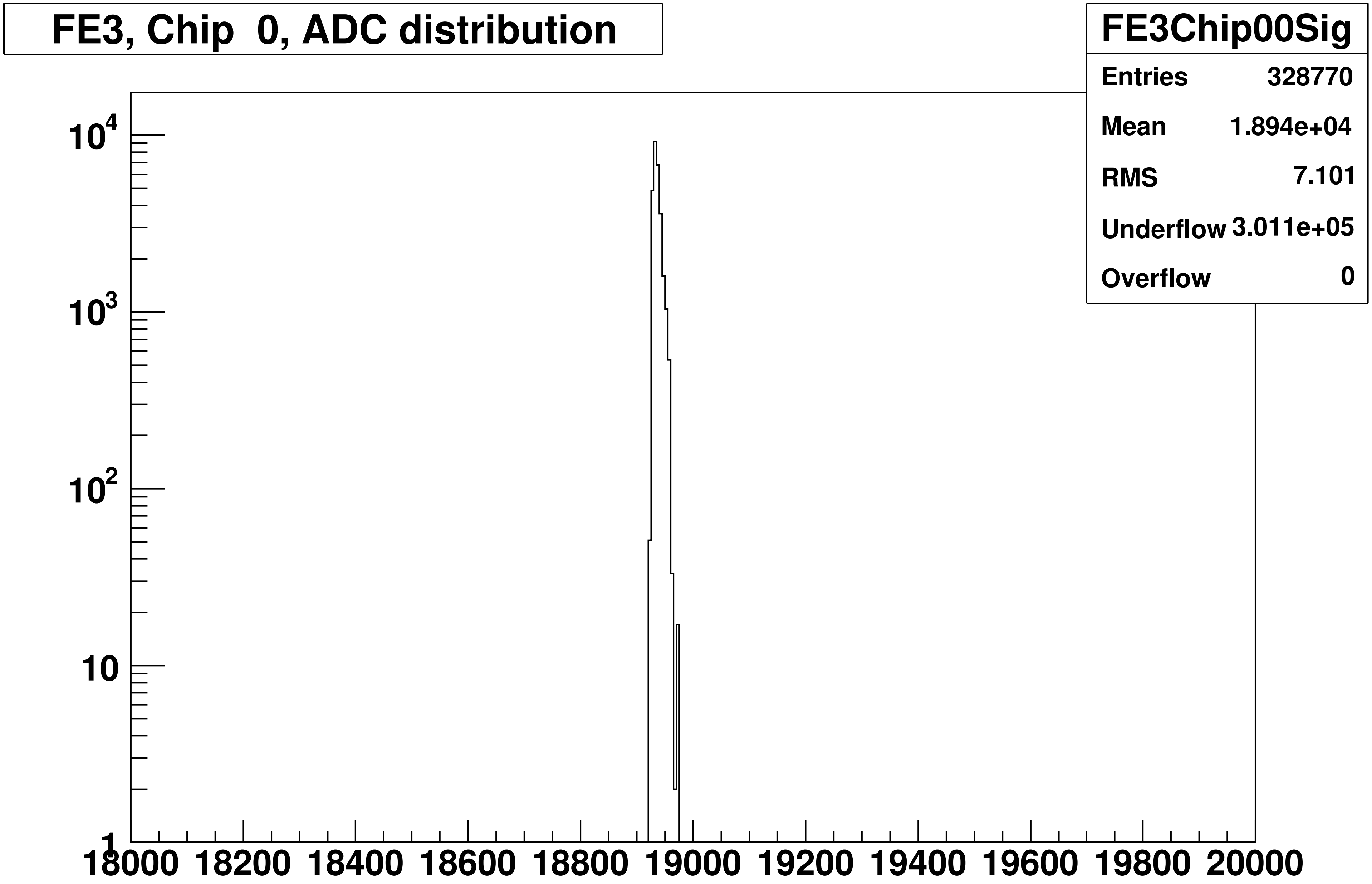

FE2, Chip 11, ADC distribution
FE2Chip11Ped
Entries 328770
Mean 3.904
RMS 1.36
Underflow 0
Overflow 2.785e+04
10^5
10^4
10^3
-200
-150
-100
-50
0
50
100
150
200

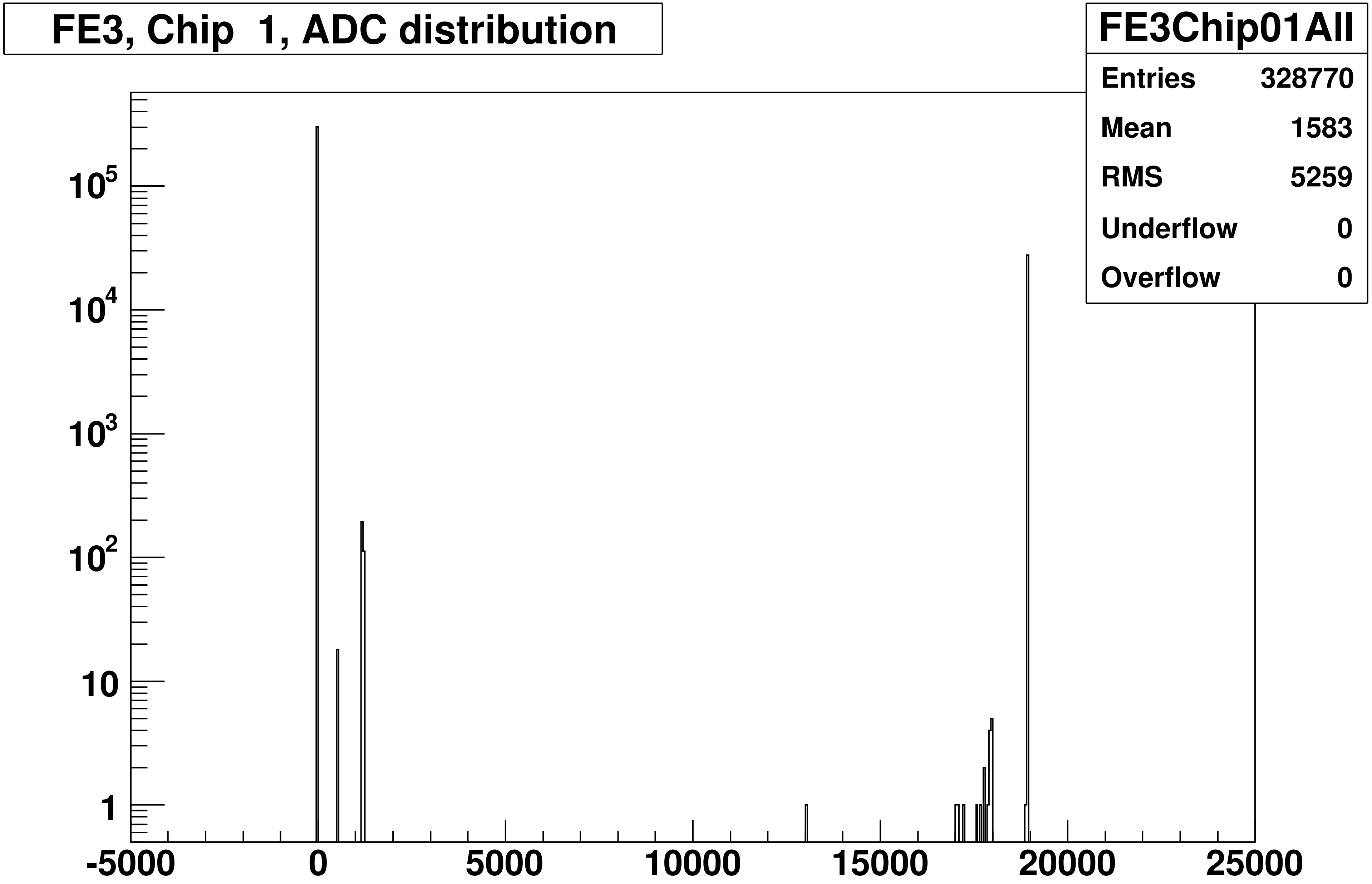

FE2, Chip 11, ADC distribution
FE2Chip11Sig
Entries 328770
Mean 1.877e+04
RMS 15.02
Underflow 3.012e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000


FE3, Chip 0, ADC distribution
FE3Chip00All
Entries 328770
Mean 1594
RMS 5260
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000



FE3, Chip 0, ADC distribution
FE3Chip00Ped
Entries 328770
Mean -2.589
RMS 1.308
Underflow 0
Overflow 2.804e+04
10^5
10^4
10^3
10^2
10
-200
-150
-100
-50
0
50
100
150
200


FE3, Chip 0, ADC distribution
FE3Chip00Sig
Entries 328770
Mean 1.894e+04
RMS 7.101
Underflow 3.011e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE3, Chip 1, ADC distribution
FE3Chip01All
Entries 328770
Mean 1583
RMS 5259
Underflow 0
Overflow 0
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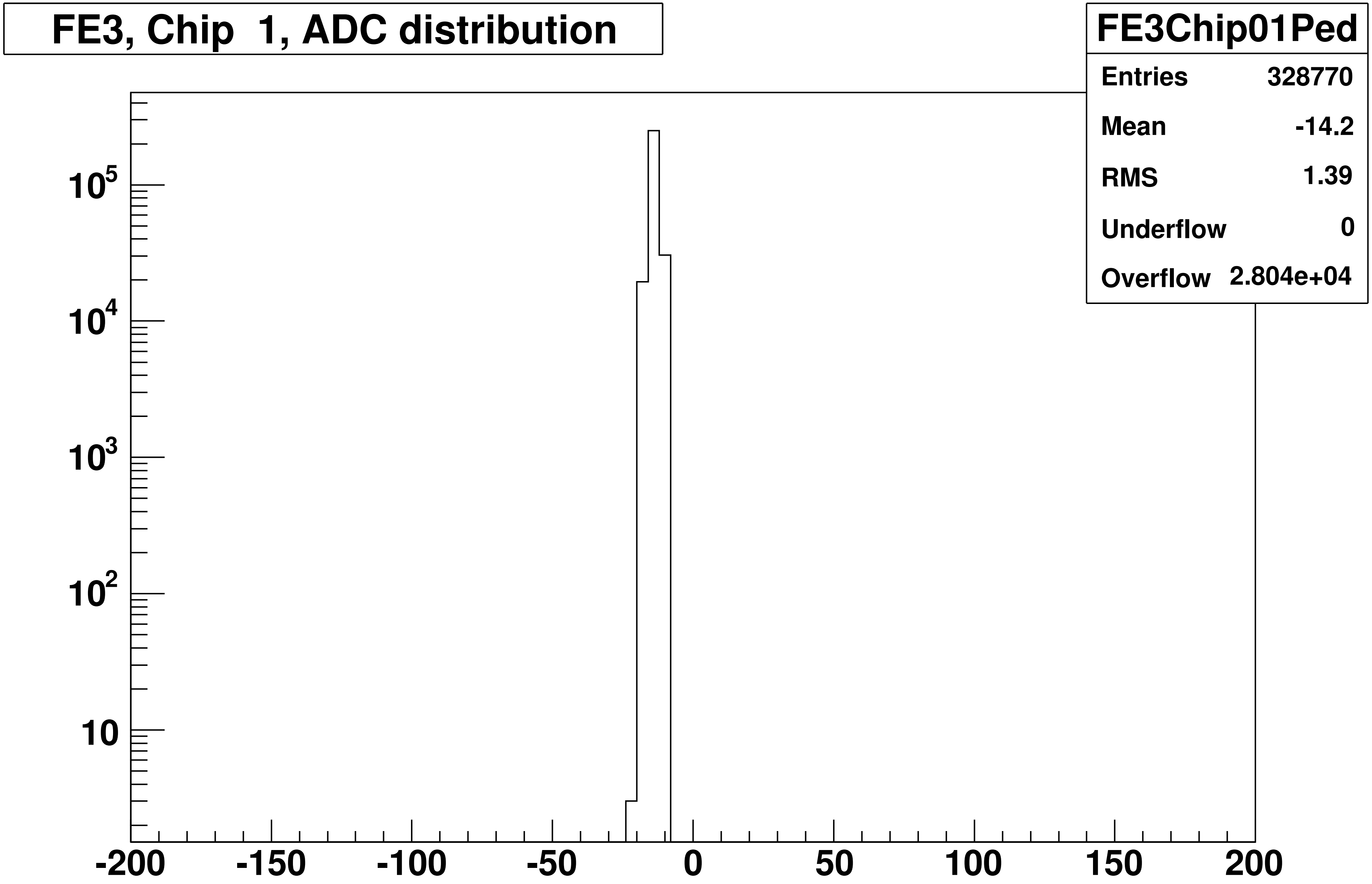
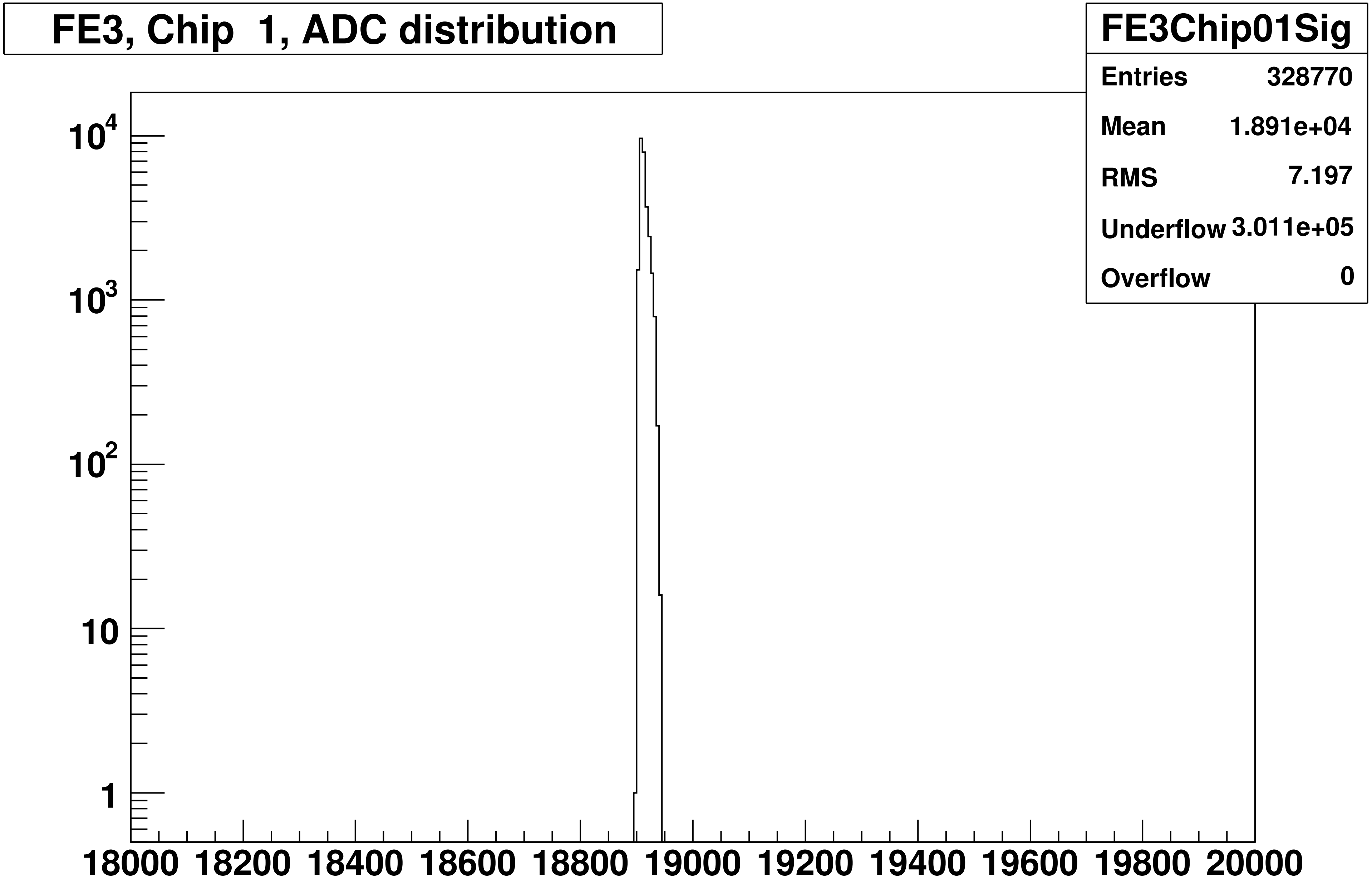
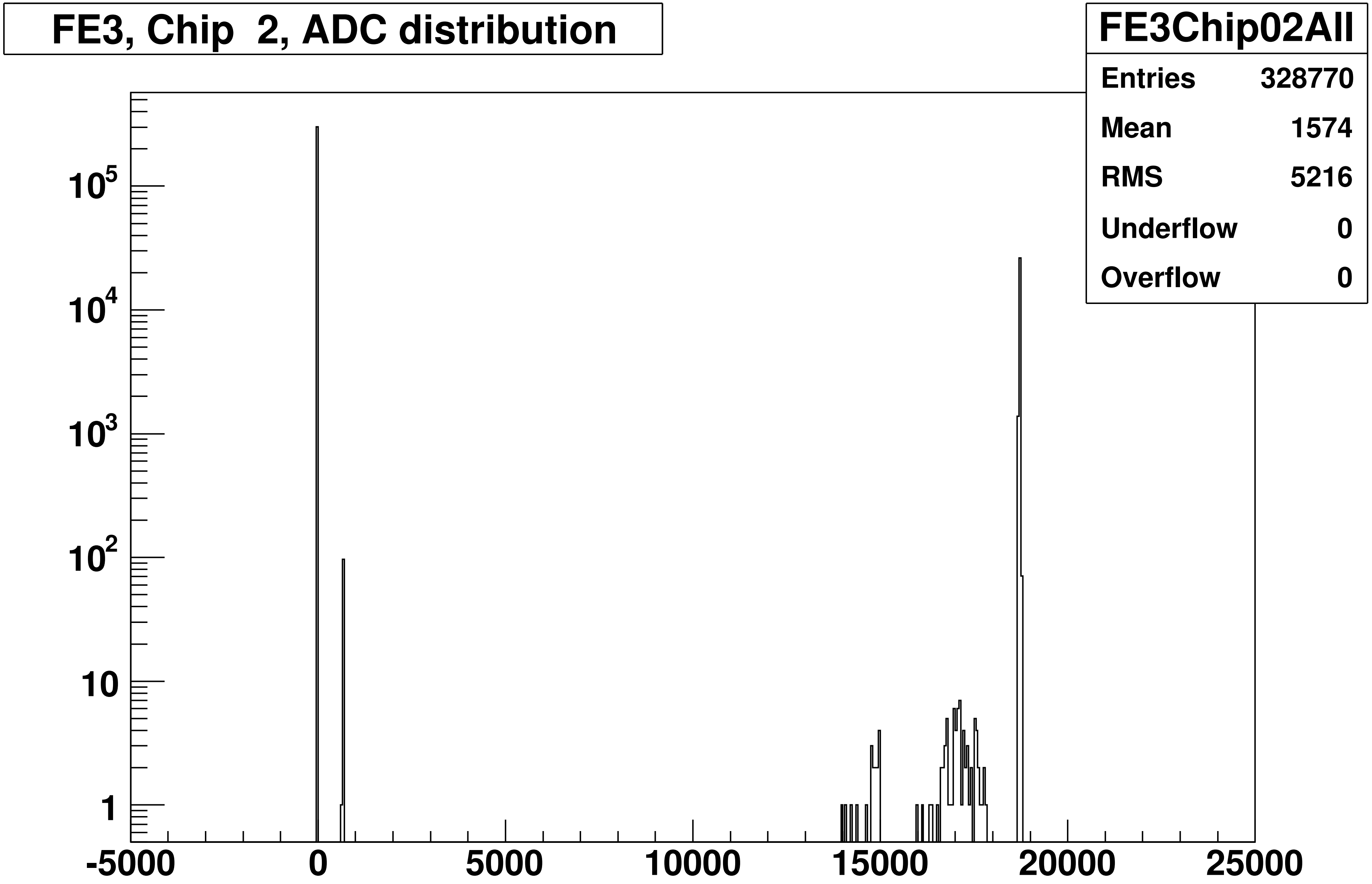
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE3, Chip 1, ADC distribution
FE3Chip01Ped
Entries 328770
Mean -14.2
RMS 1.39
Underflow 0
Overflow 2.804e+04
10
10^2
10^3
10^4
10^5
-200
-150
-100
-50
0
50
100
150
200


FE3, Chip 1, ADC distribution
FE3Chip01Sig
Entries 328770
Mean 1.891e+04
RMS 7.197
Underflow 3.011e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE3, Chip 2, ADC distribution
FE3Chip02All
Entries 328770
Mean 1574
RMS 5216
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
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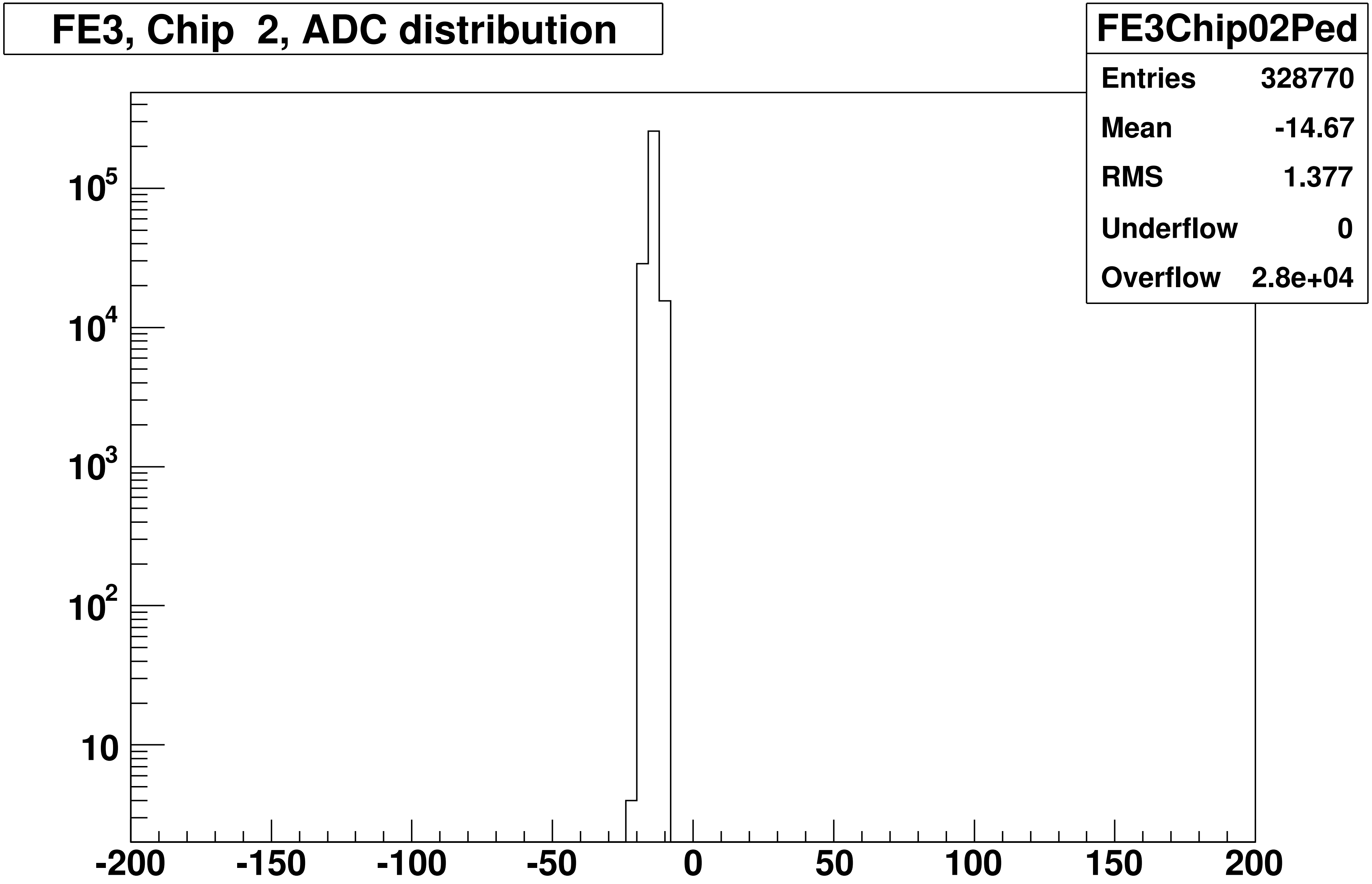
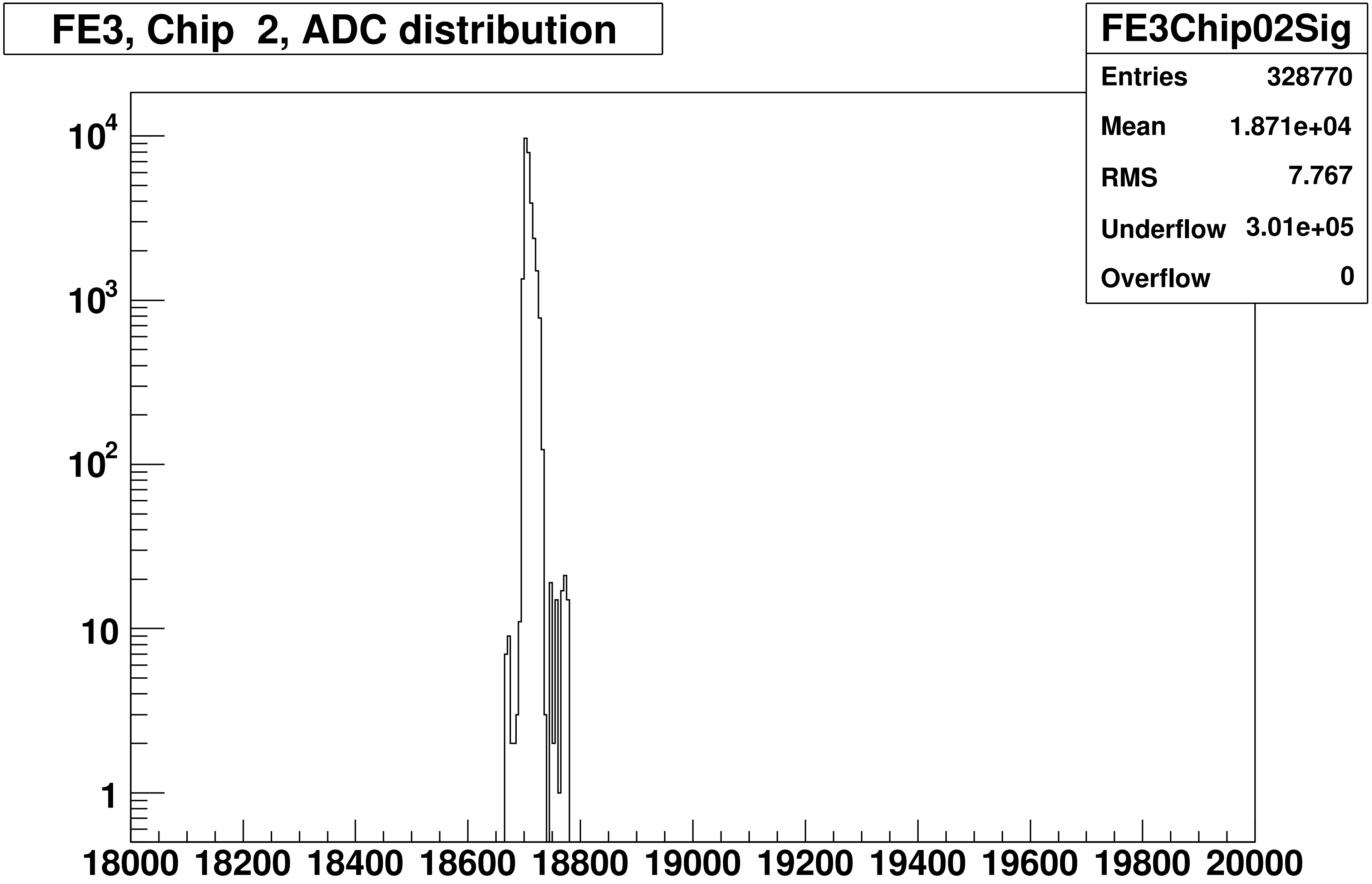
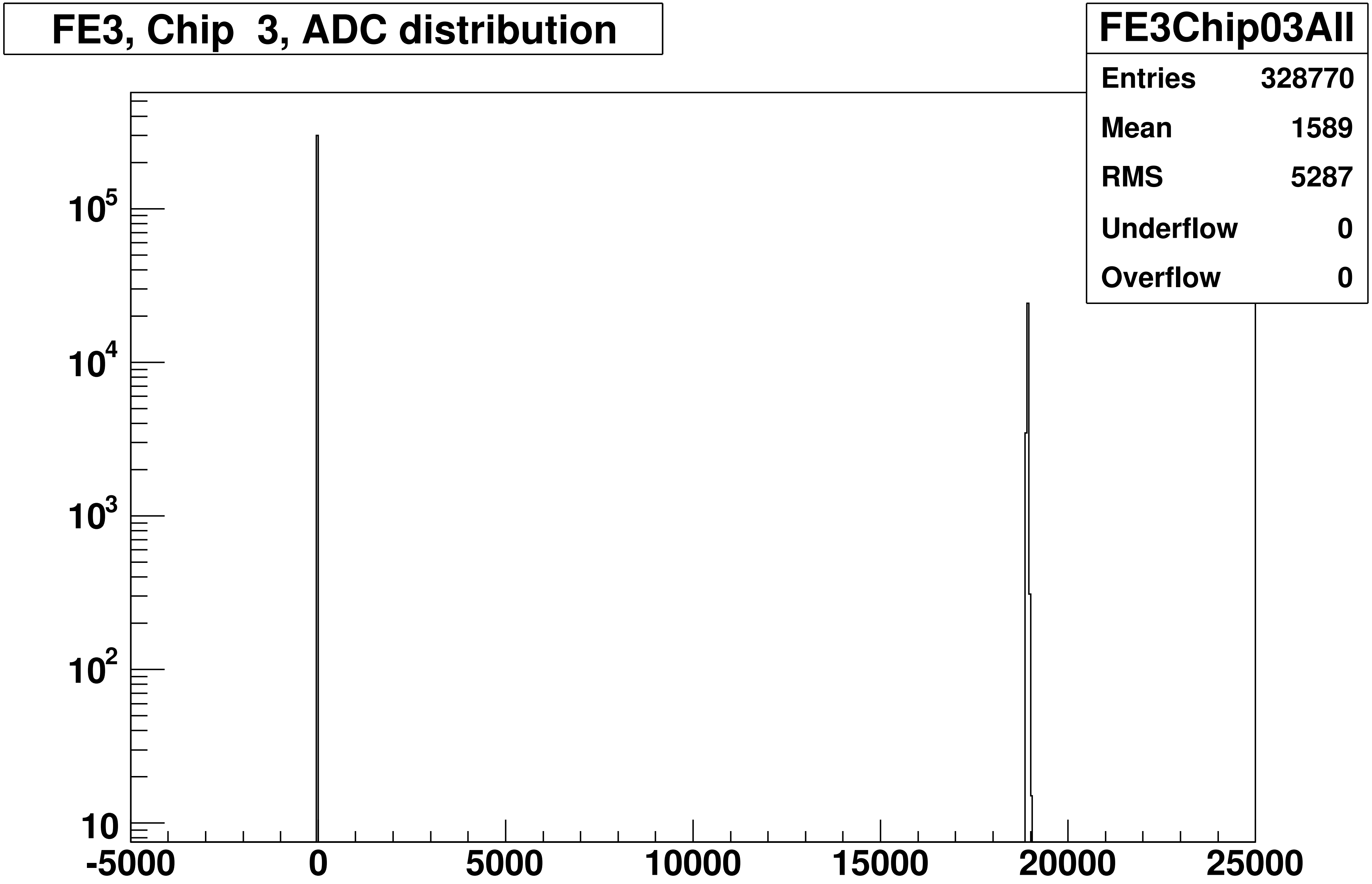
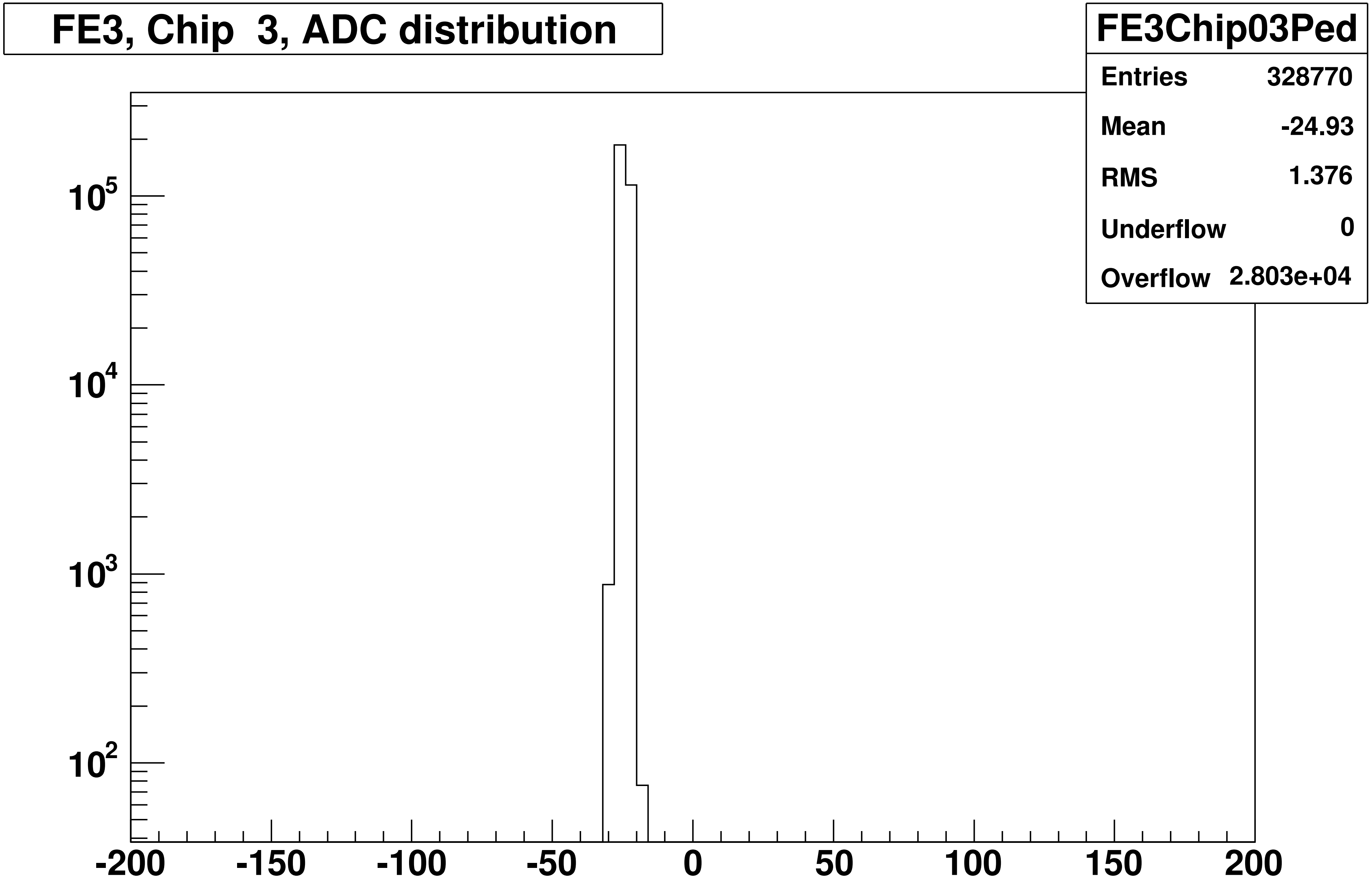
10000
15000
20000
25000


FE3, Chip 2, ADC distribution
FE3Chip02Ped
Entries 328770
Mean -14.67
RMS 1.377
Underflow 0
Overflow 2.8e+04
10
10^2
10^3
10^4
10^5
-200
-150
-100
-50
0
50
100
150
200



FE3, Chip 2, ADC distribution
FE3Chip02Sig
Entries 328770
Mean 1.871e+04
RMS 7.767
Underflow 3.01e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000


FE3, Chip 3, ADC distribution
FE3Chip03All
Entries 328770
Mean 1589
RMS 5287
Underflow 0
Overflow 0
10
10^2
10^3
10^4
10^5
-5000
0
5000
10000
15000
20000
25000



FE3, Chip 3, ADC distribution
FE3Chip03Ped
Entries 328770
Mean -24.93
RMS 1.376
Underflow 0
Overflow 2.803e+04
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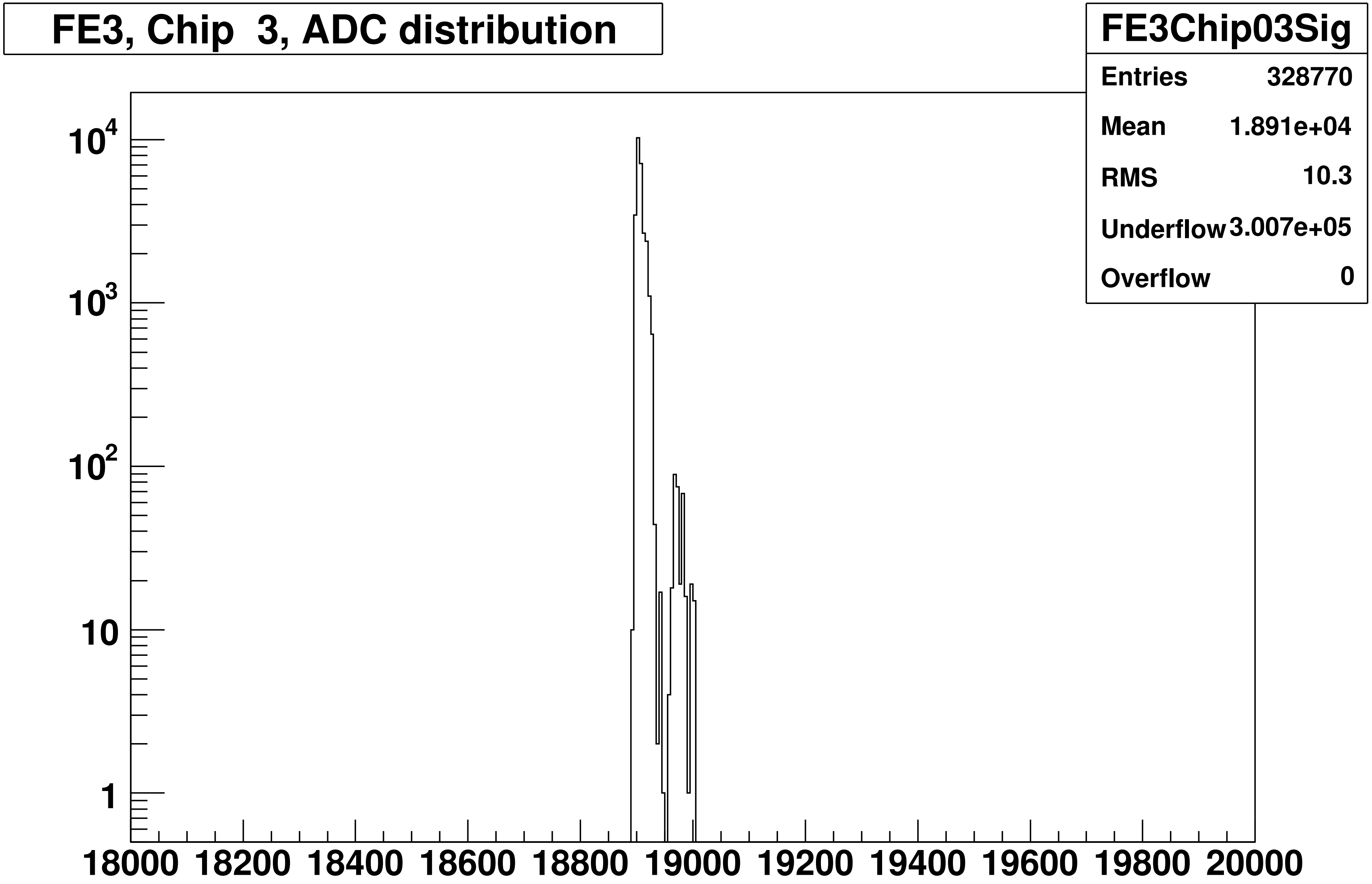
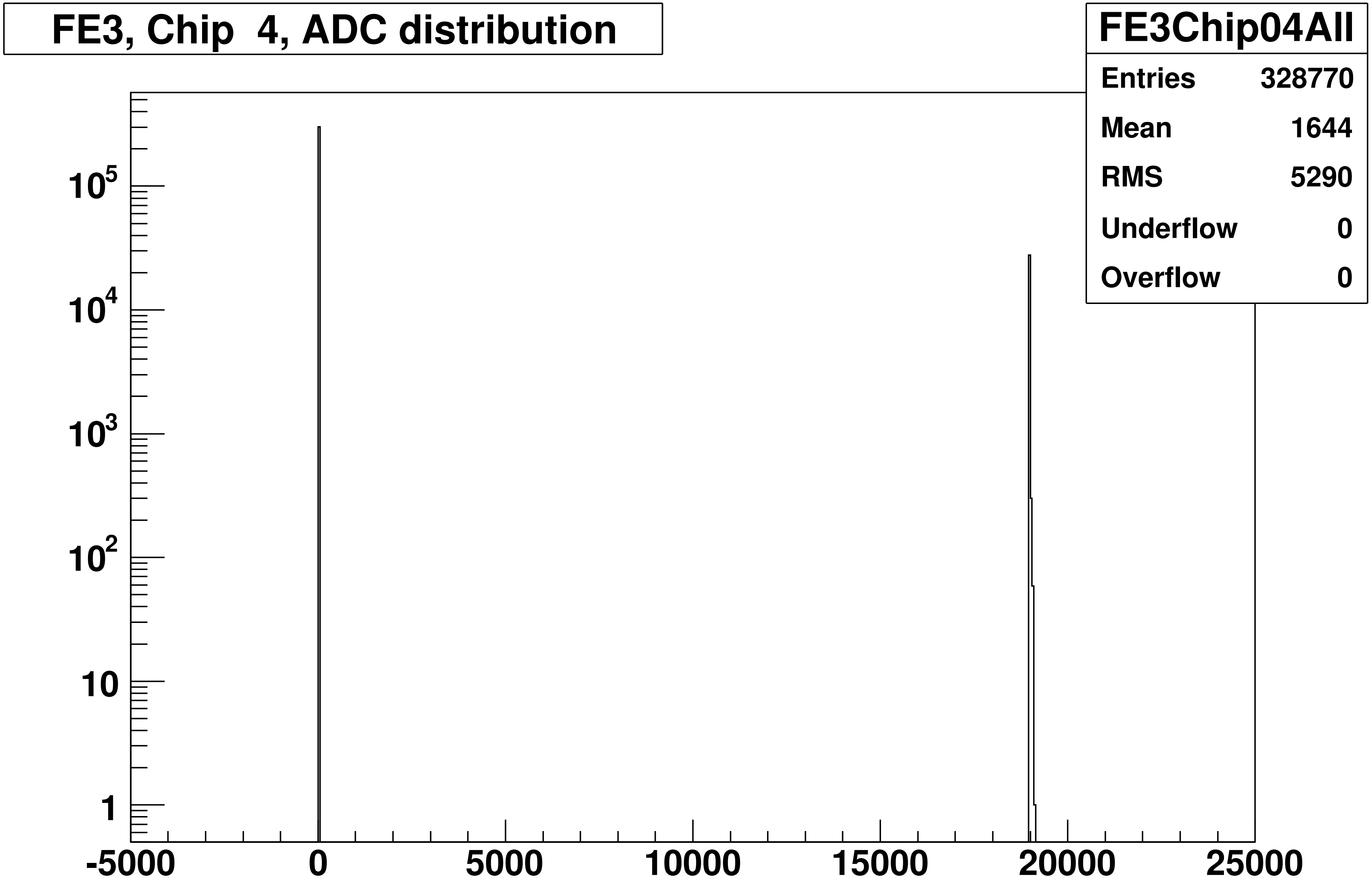
10^4
10^3
10^2
-200
-150
-100
-50
0
50
100
150
200


FE3, Chip 3, ADC distribution
FE3Chip03Sig
Entries 328770
Mean 1.891e+04
RMS 10.3
Underflow 3.007e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE3, Chip 4, ADC distribution
FE3Chip04All
Entries 328770
Mean 1644
RMS 5290
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
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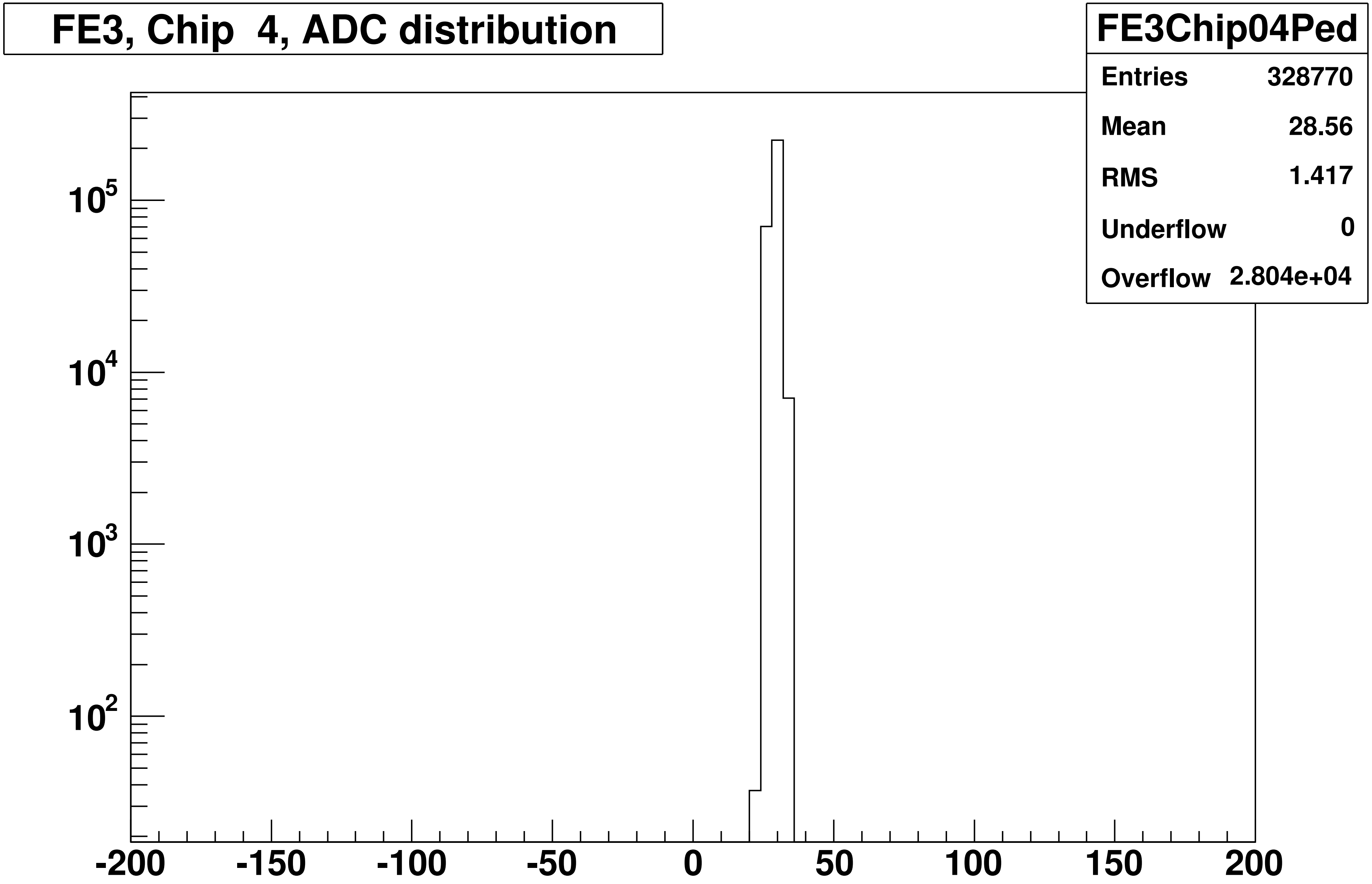
10000
15000
20000
25000


FE3, Chip 4, ADC distribution
FE3Chip04Ped
Entries 328770
Mean 28.56
RMS 1.417
Underflow 0
Overflow 2.804e+04
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10^4
10^3
10^2
-200
-150
-100
-50
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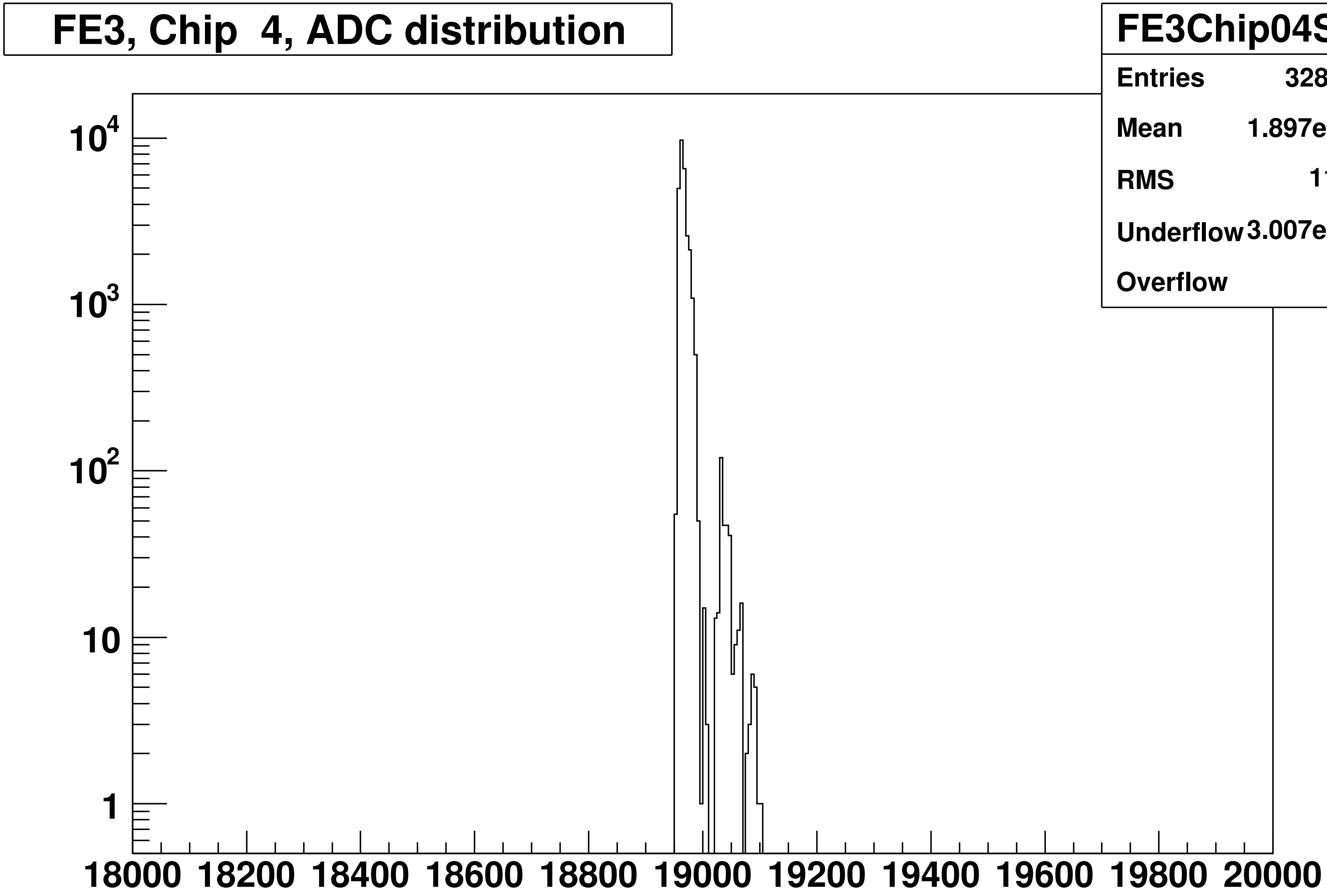
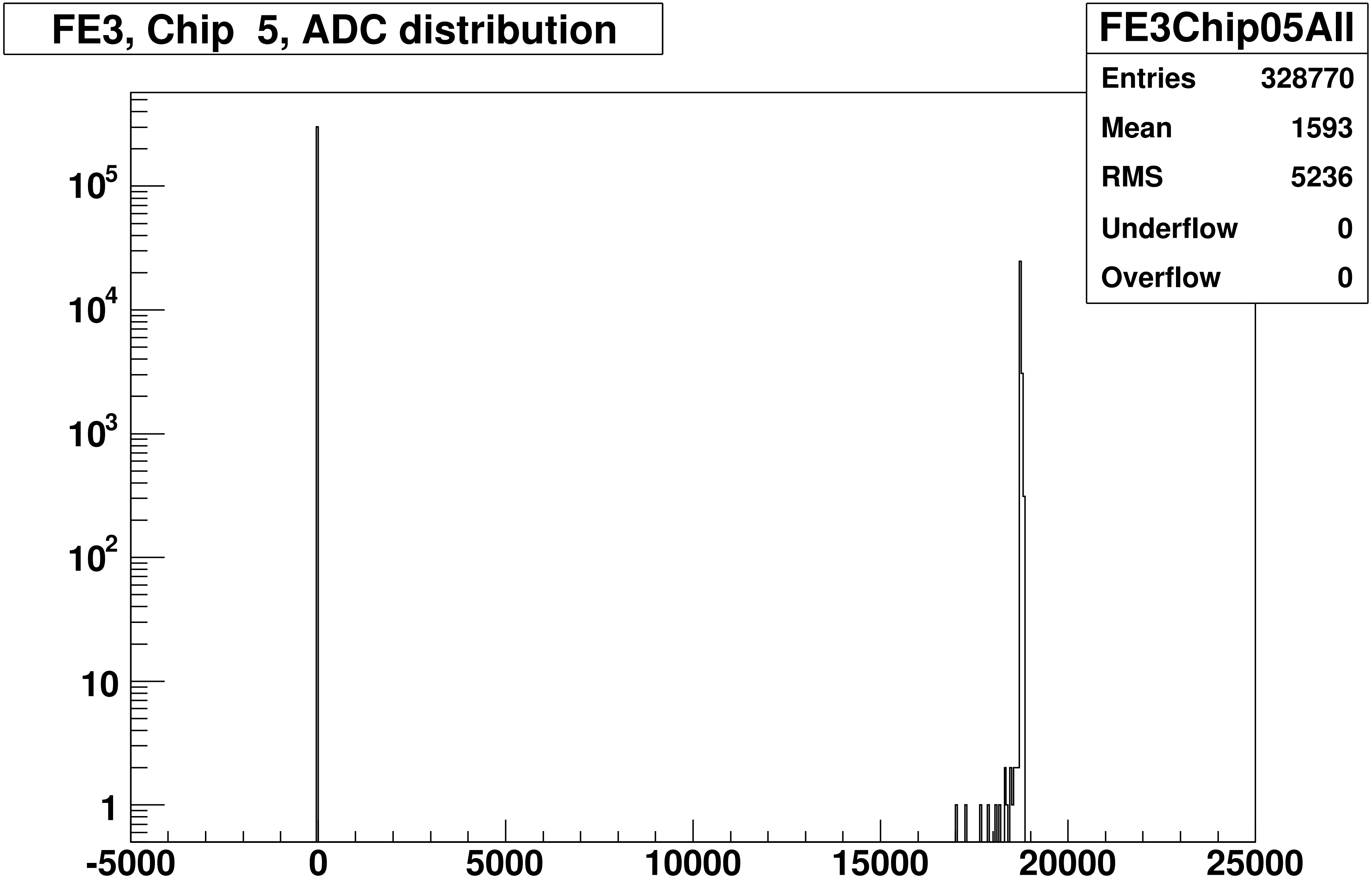
100
150
200



FE3, Chip 4, ADC distribution
FE3Chip04Sig
Entries 328770
Mean 1.897e+04
RMS 11.08
Underflow 3.007e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000


FE3, Chip 5, ADC distribution
FE3Chip05All
Entries 328770
Mean 1593
RMS 5236
Underflow 0
Overflow 0
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10^4
10^3
10^2
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-5000
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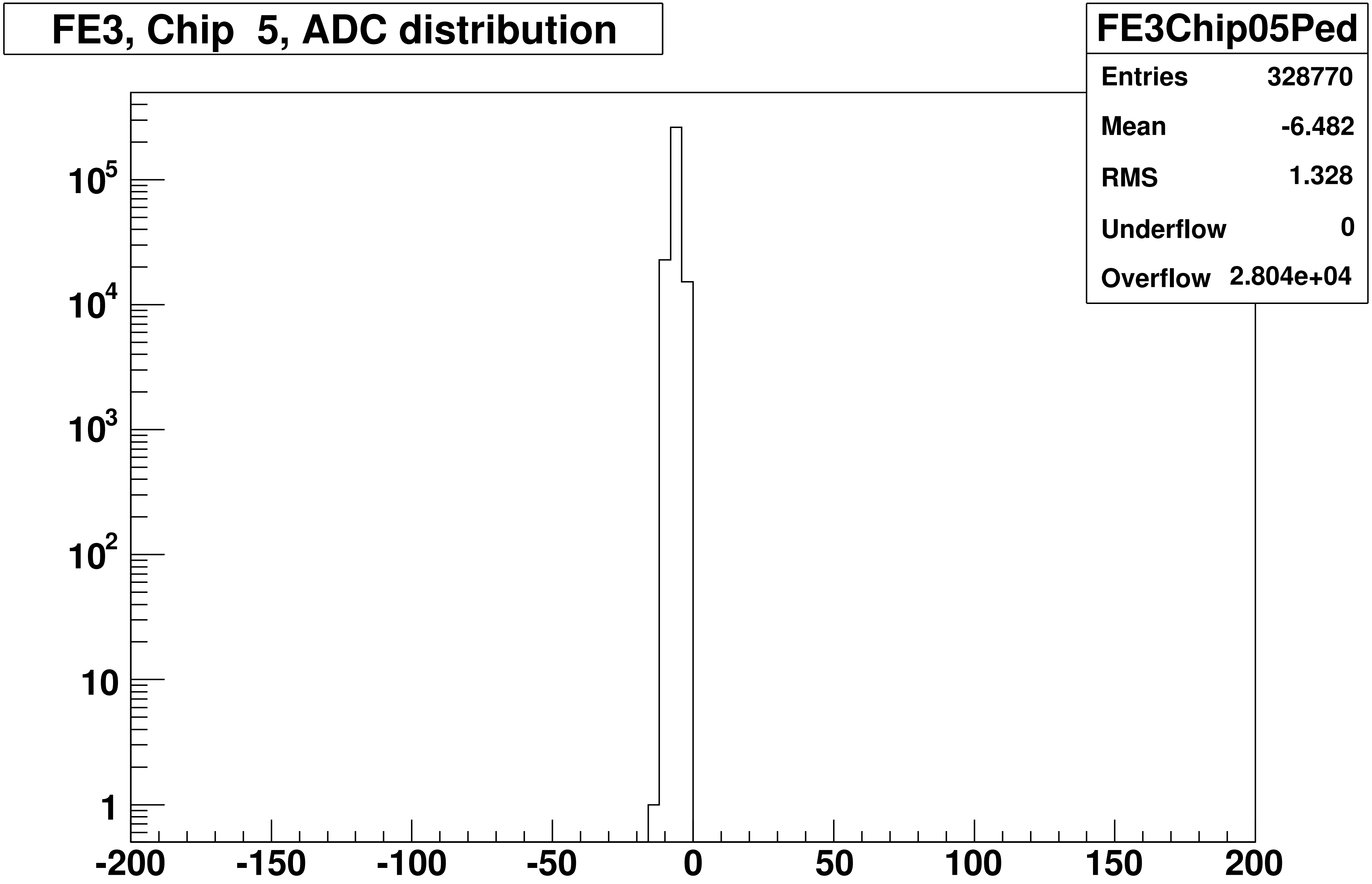
FE3, Chip 5, ADC distribution
FE3Chip05Ped
Entries 328770
Mean -6.482
RMS 1.328
Underflow 0
Overflow 2.804e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
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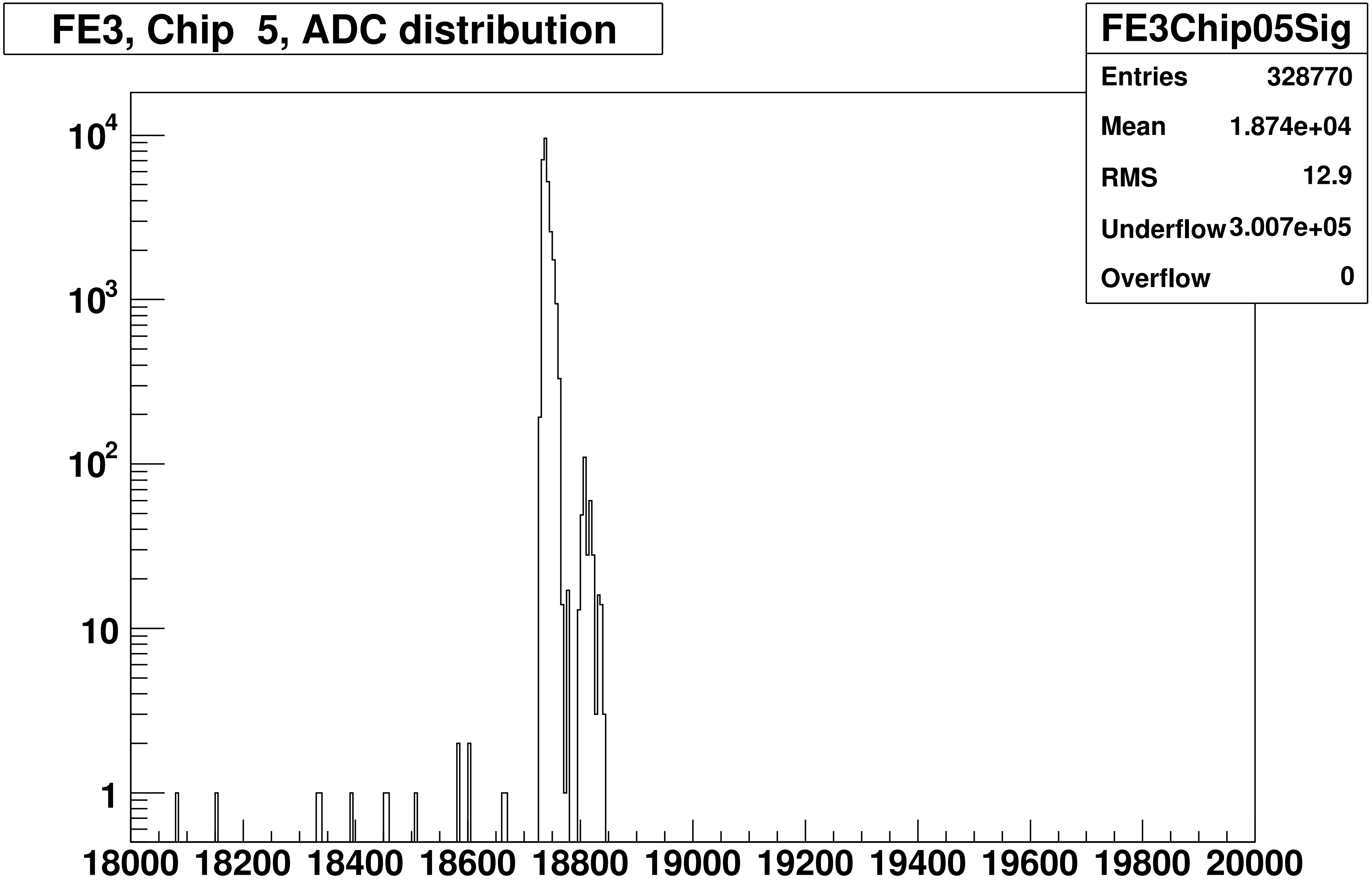
50
100
150
200



FE3, Chip 5, ADC distribution
FE3Chip05Sig
Entries 328770
Mean 1.874e+04
RMS 12.9
Underflow 3.007e+05
Overflow 0
10^4
10^3
10^2
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1
18000
18200
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18600
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19000
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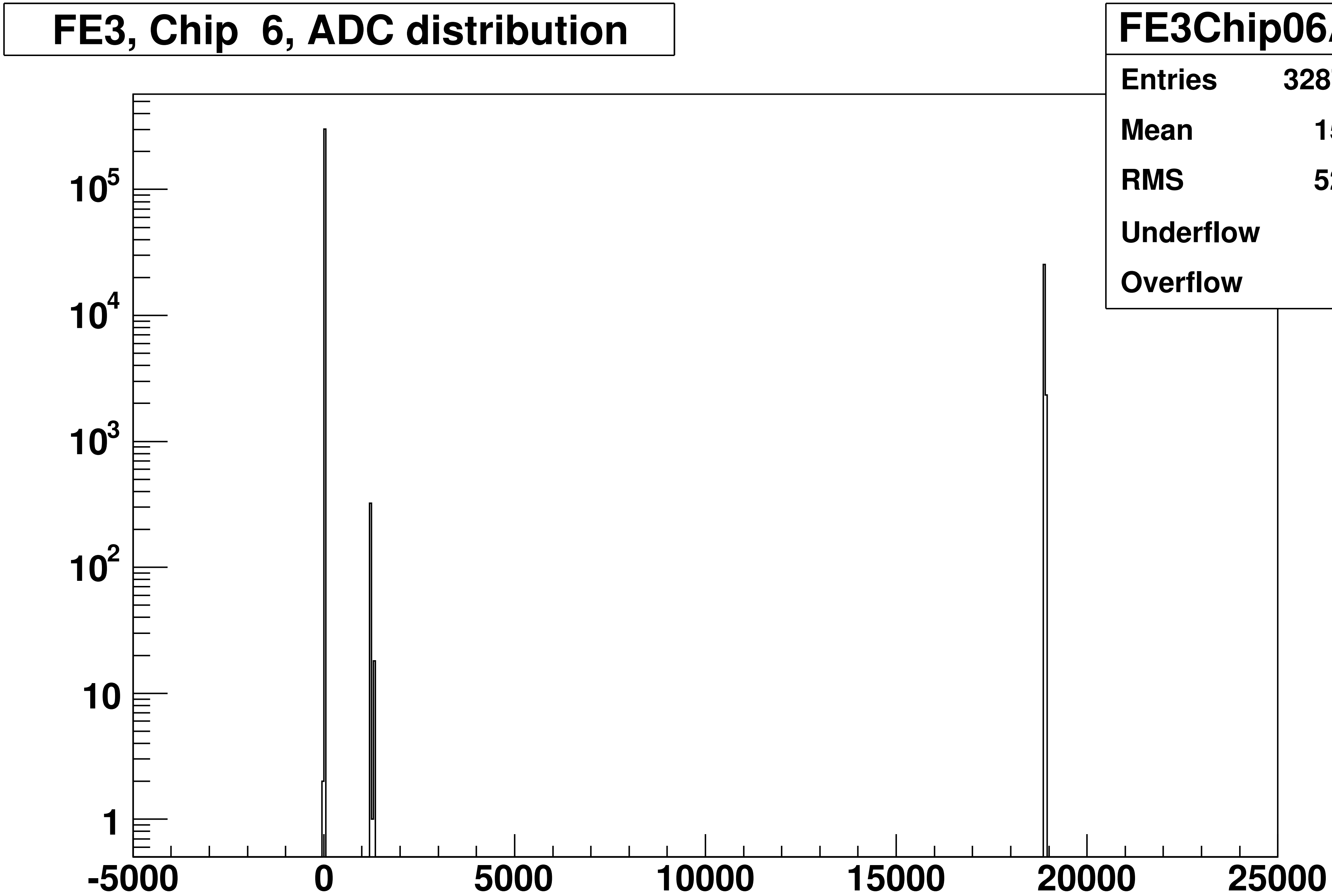
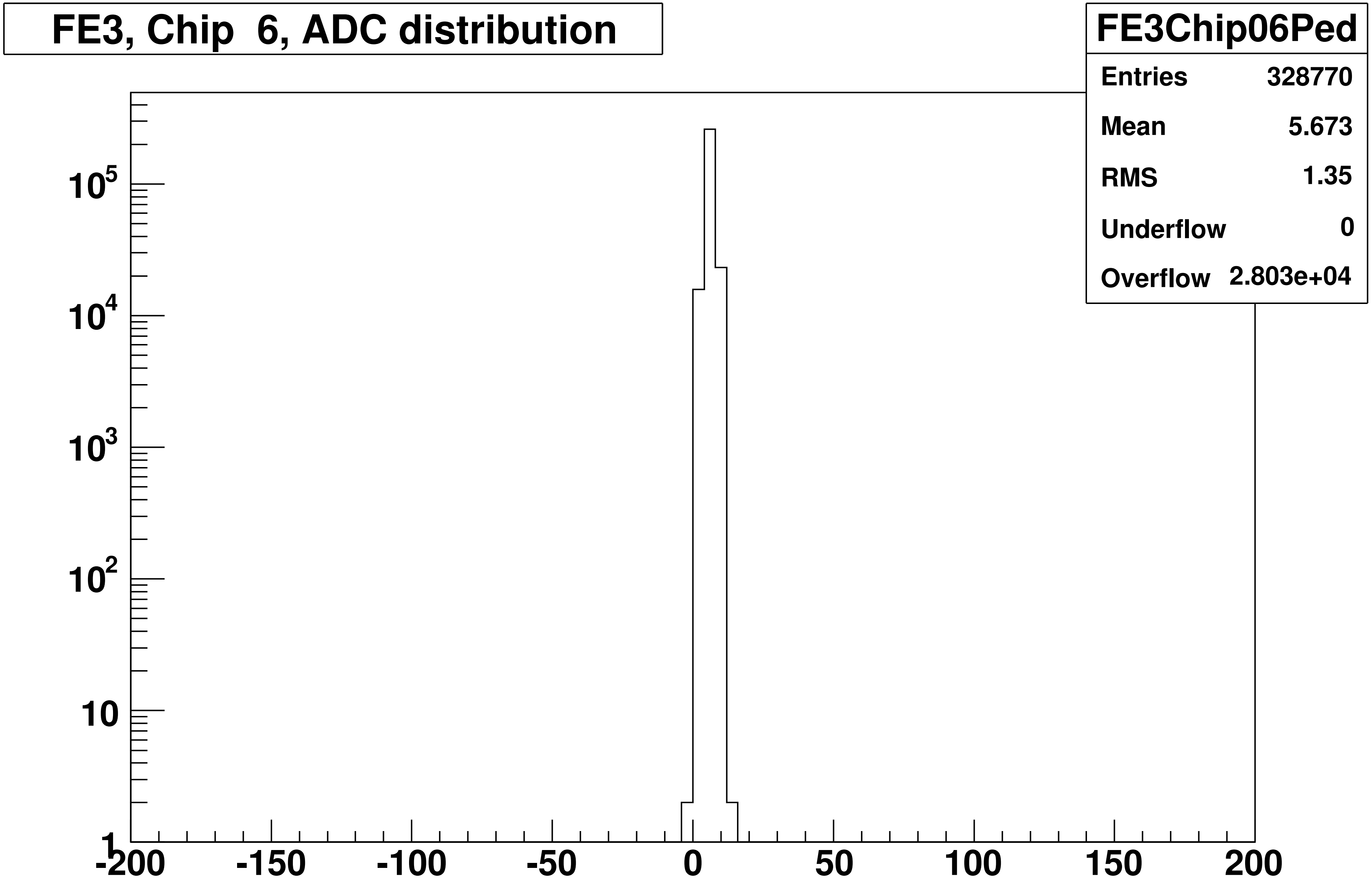
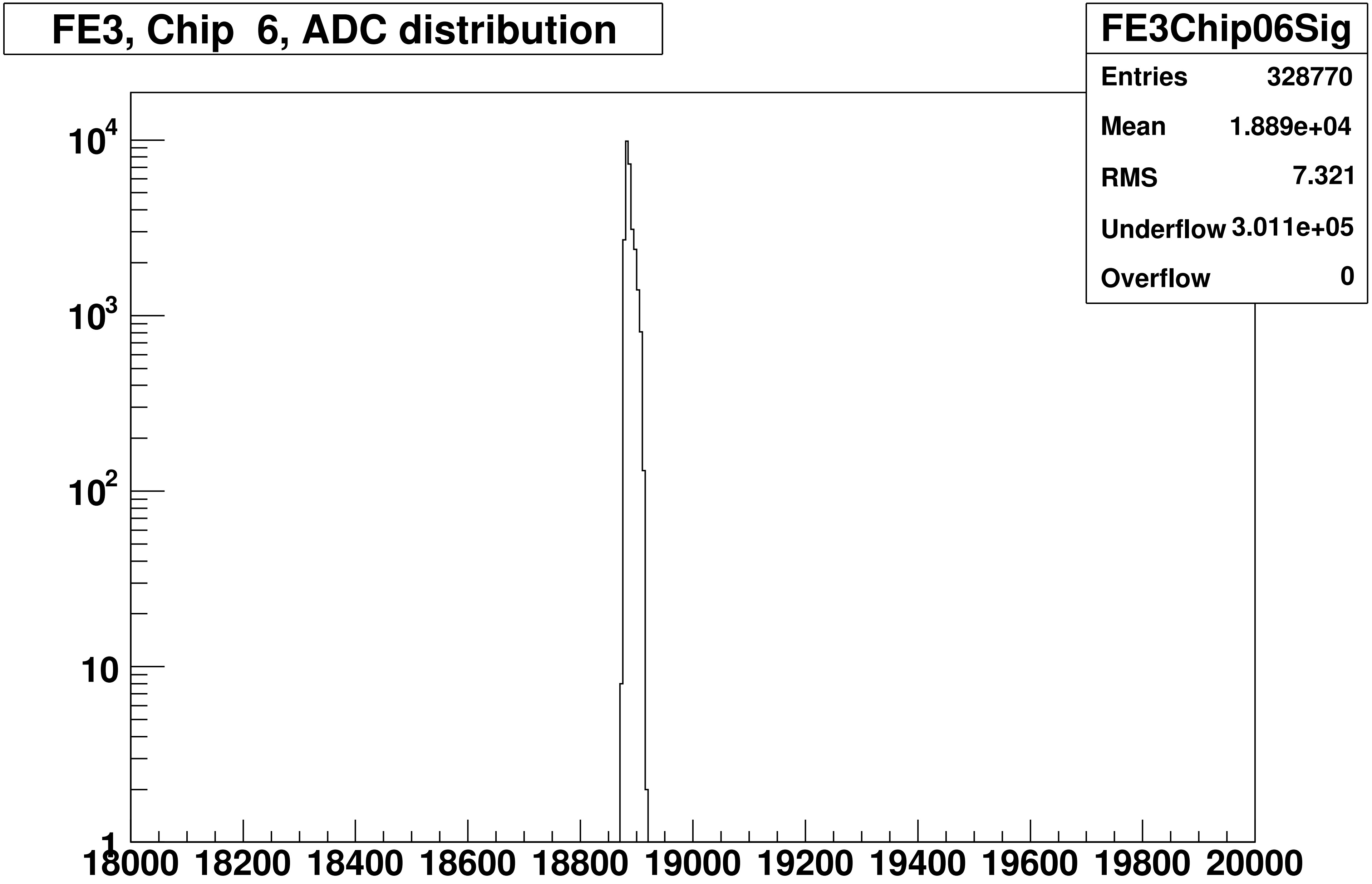
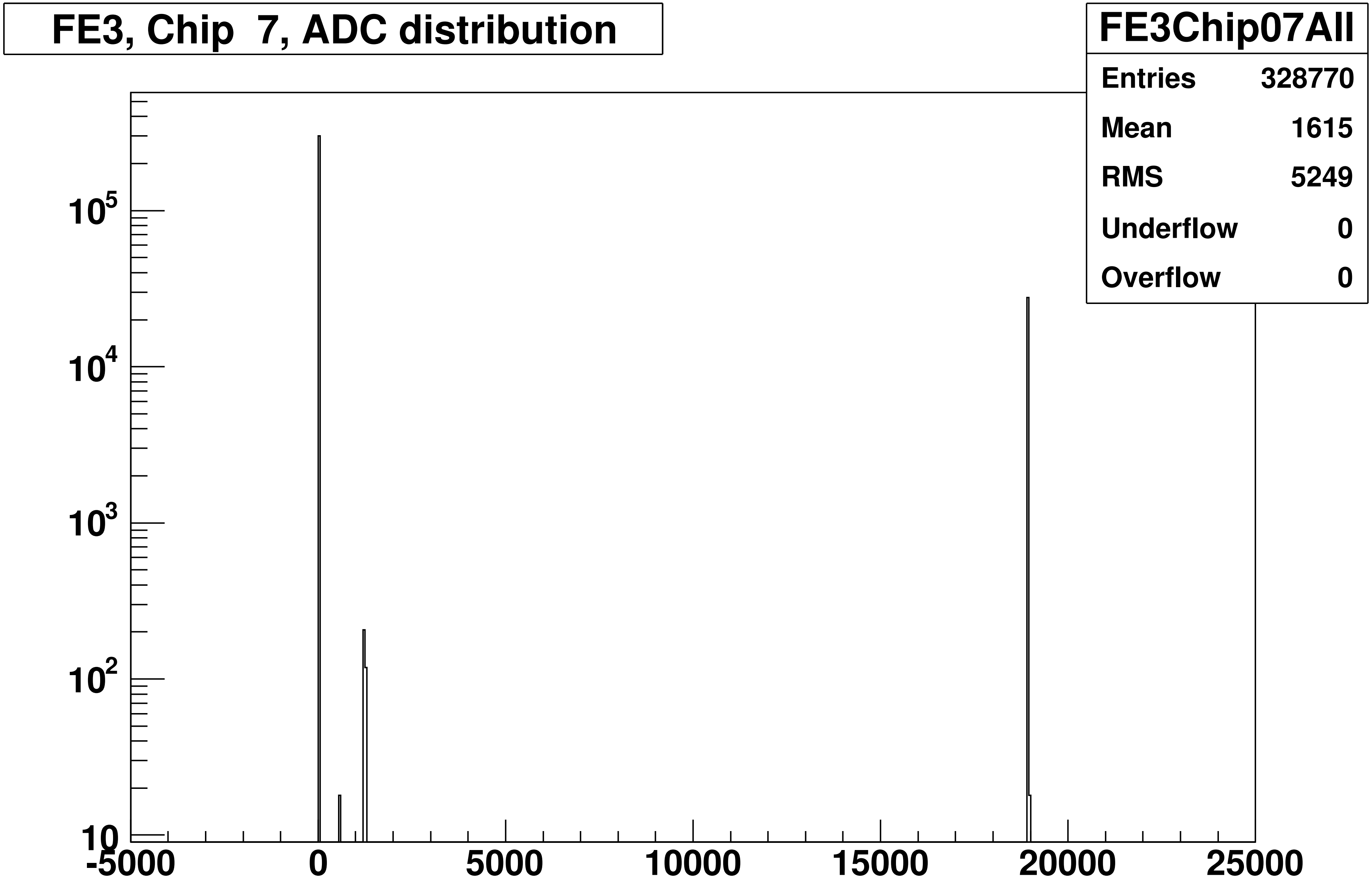

FE3, Chip 6, ADC distribution
FE3Chip06All
Entries 328770
Mean 1597
RMS 5243
Underflow 0
Overflow 0
1
10
10^2
10^3
10^4
10^5
-5000
0
5000
10000
15000
20000
25000

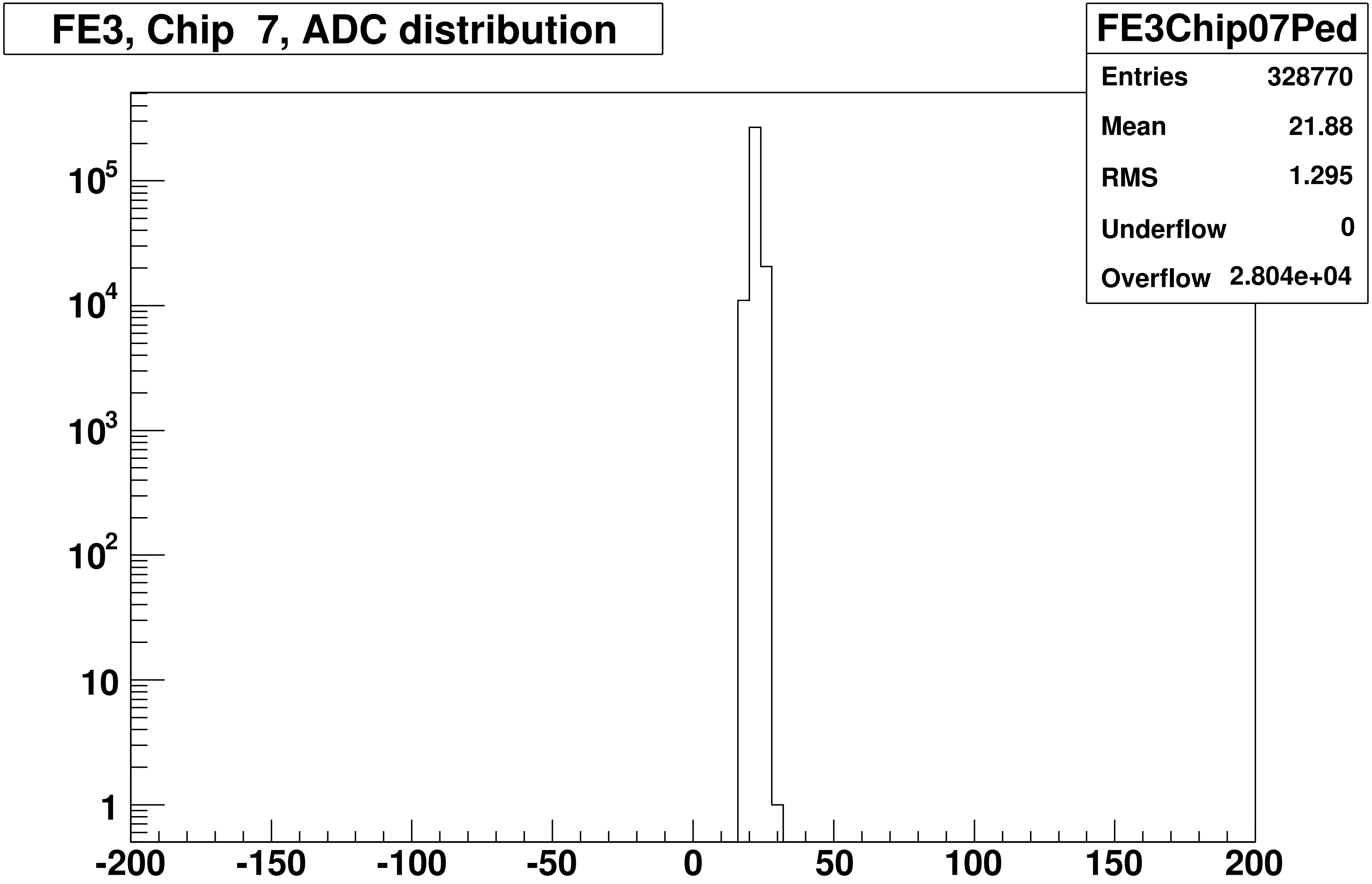


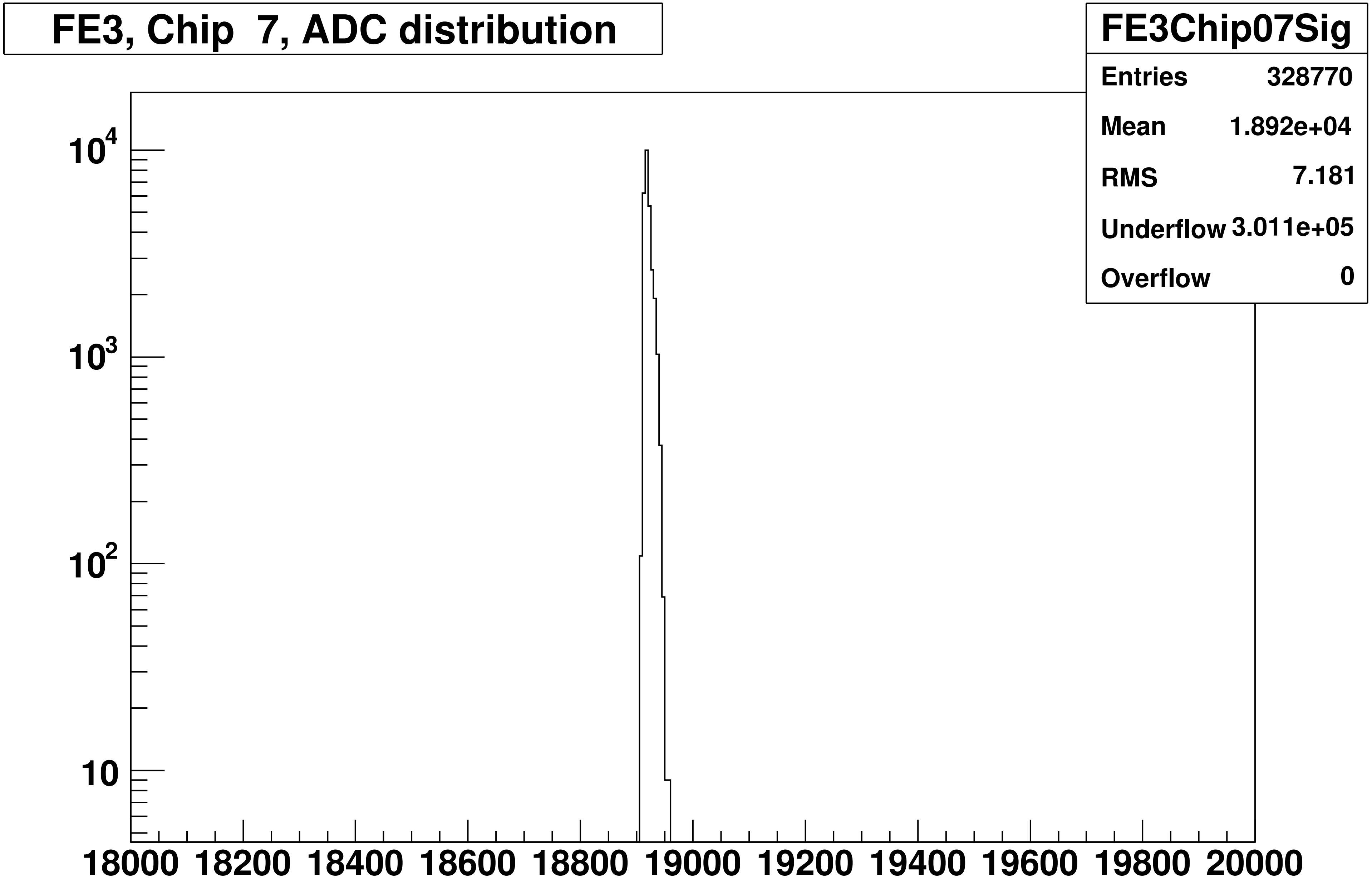
FE3, Chip 6, ADC distribution
FE3Chip06Ped
Entries 328770
Mean 5.673
RMS 1.35
Underflow 0
Overflow 2.803e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
200



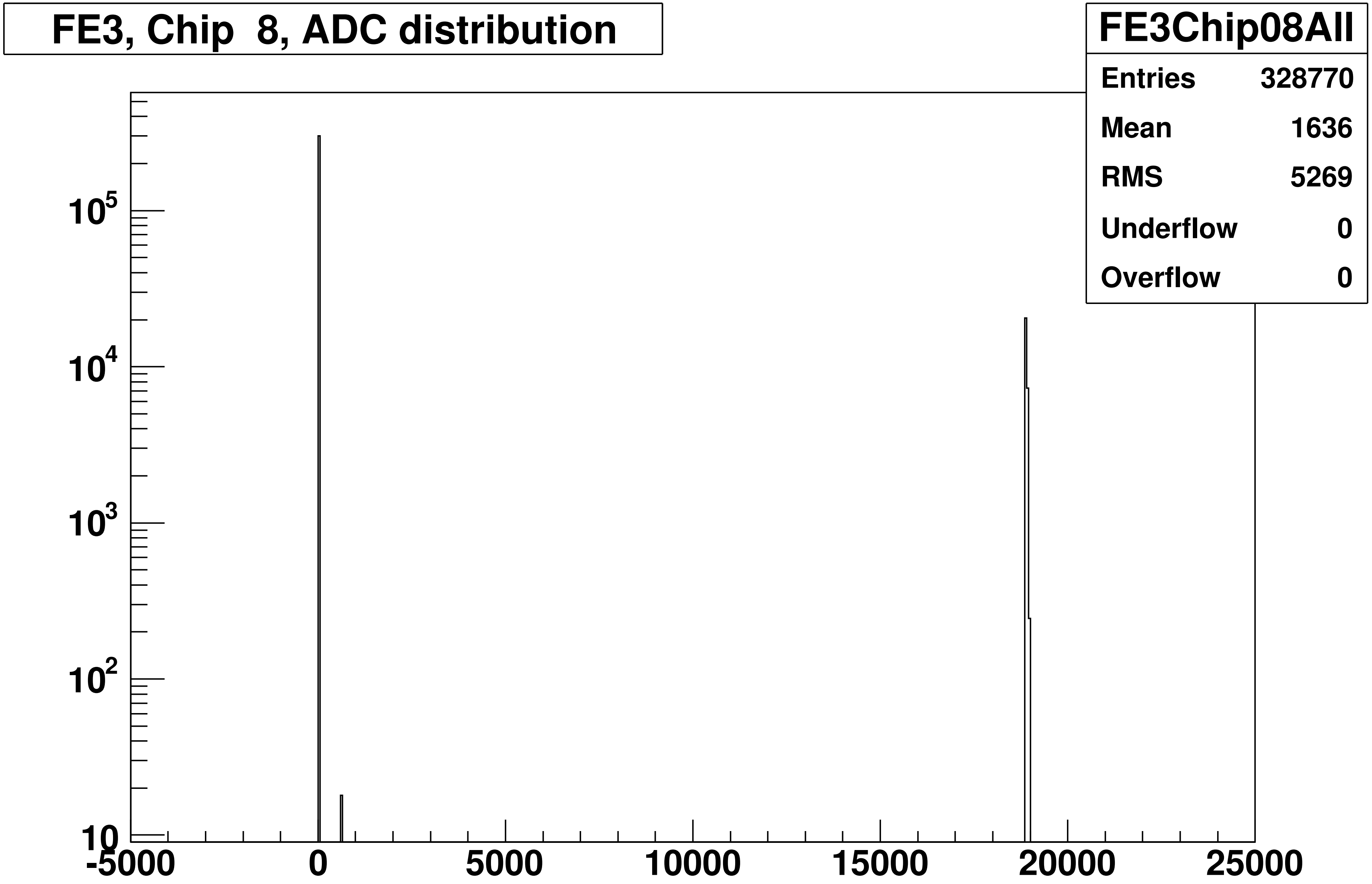
FE3, Chip 6, ADC distribution
FE3Chip06Sig
Entries 328770
Mean 1.889e+04
RMS 7.321
Underflow 3.011e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000

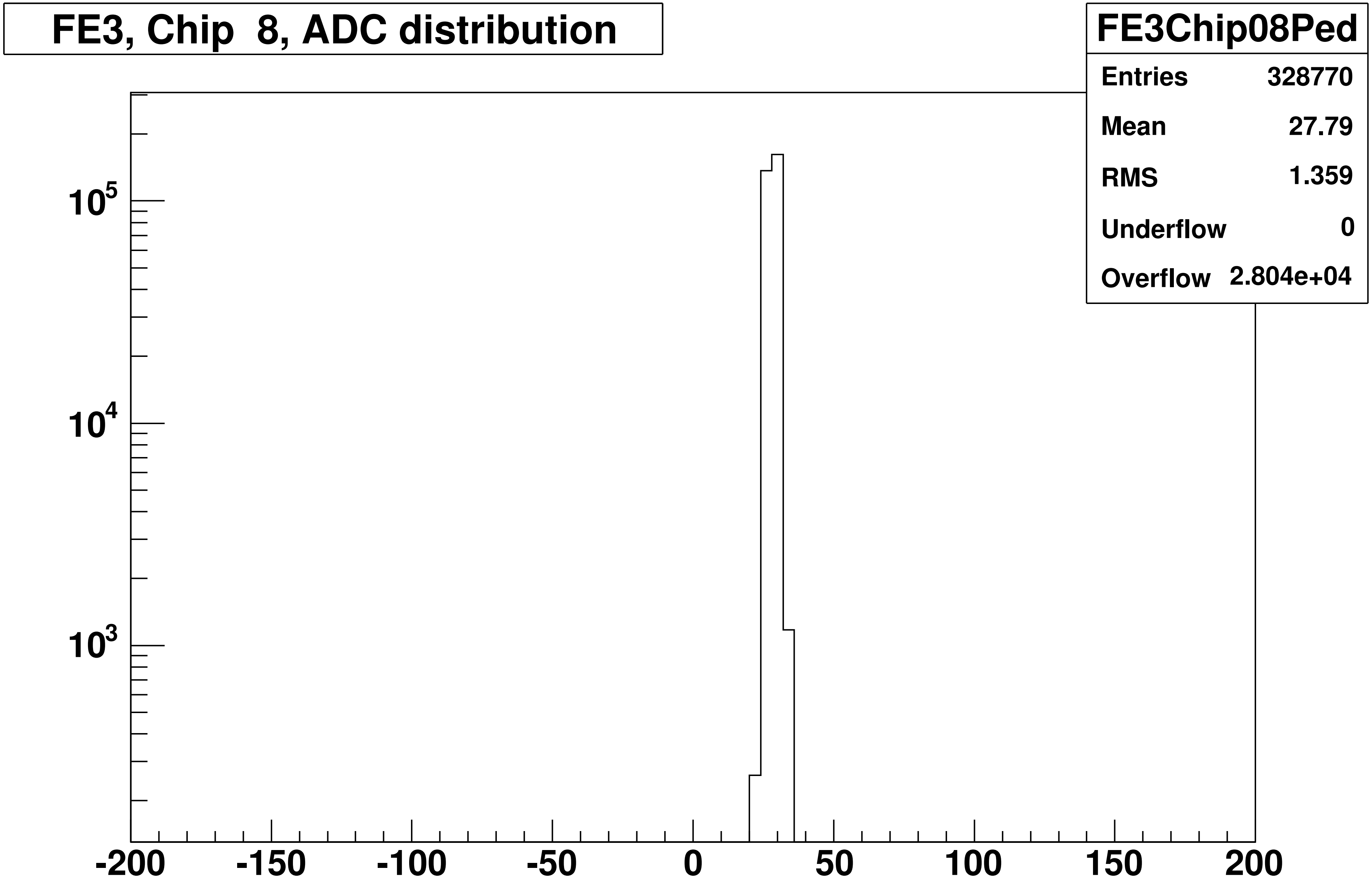

FE3, Chip 7, ADC distribution
FE3Chip07All
Entries 328770
Mean 1615
RMS 5249
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE3, Chip 7, ADC distribution
FE3Chip07Ped
Entries 328770
Mean 21.88
RMS 1.295
Underflow 0
Overflow 2.804e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
200



FE3, Chip 7, ADC distribution
FE3Chip07Sig
Entries 328770
Mean 1.892e+04
RMS 7.181
Underflow 3.011e+05
Overflow 0
10^4
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE3, Chip 8, ADC distribution
FE3Chip08All
Entries 328770
Mean 1636
RMS 5269
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE3, Chip 8, ADC distribution
FE3Chip08Ped
Entries 328770
Mean 27.79
RMS 1.359
Underflow 0
Overflow 2.804e+04
10^5
10^4
10^3
-200
-150
-100
-50
0
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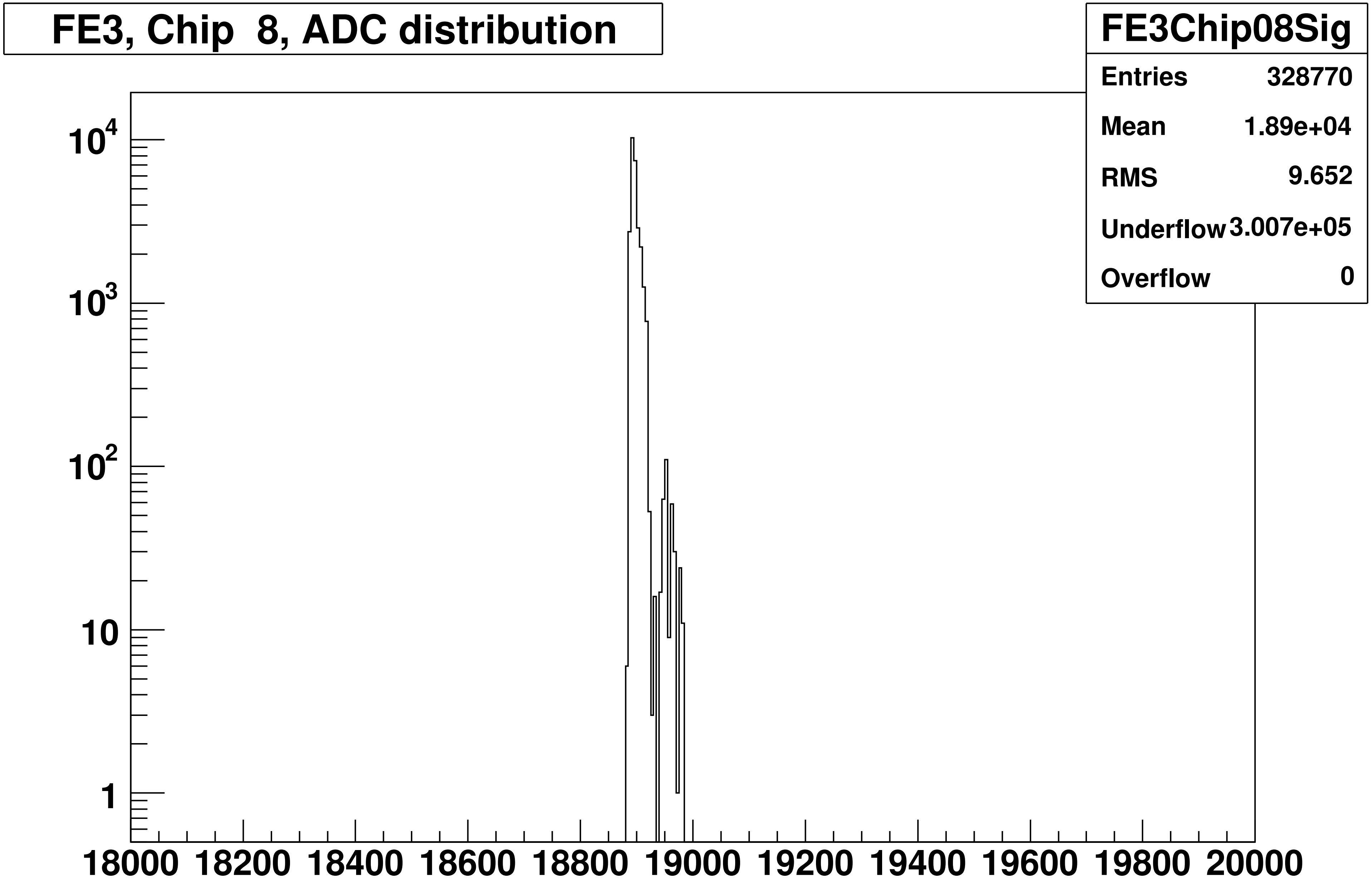
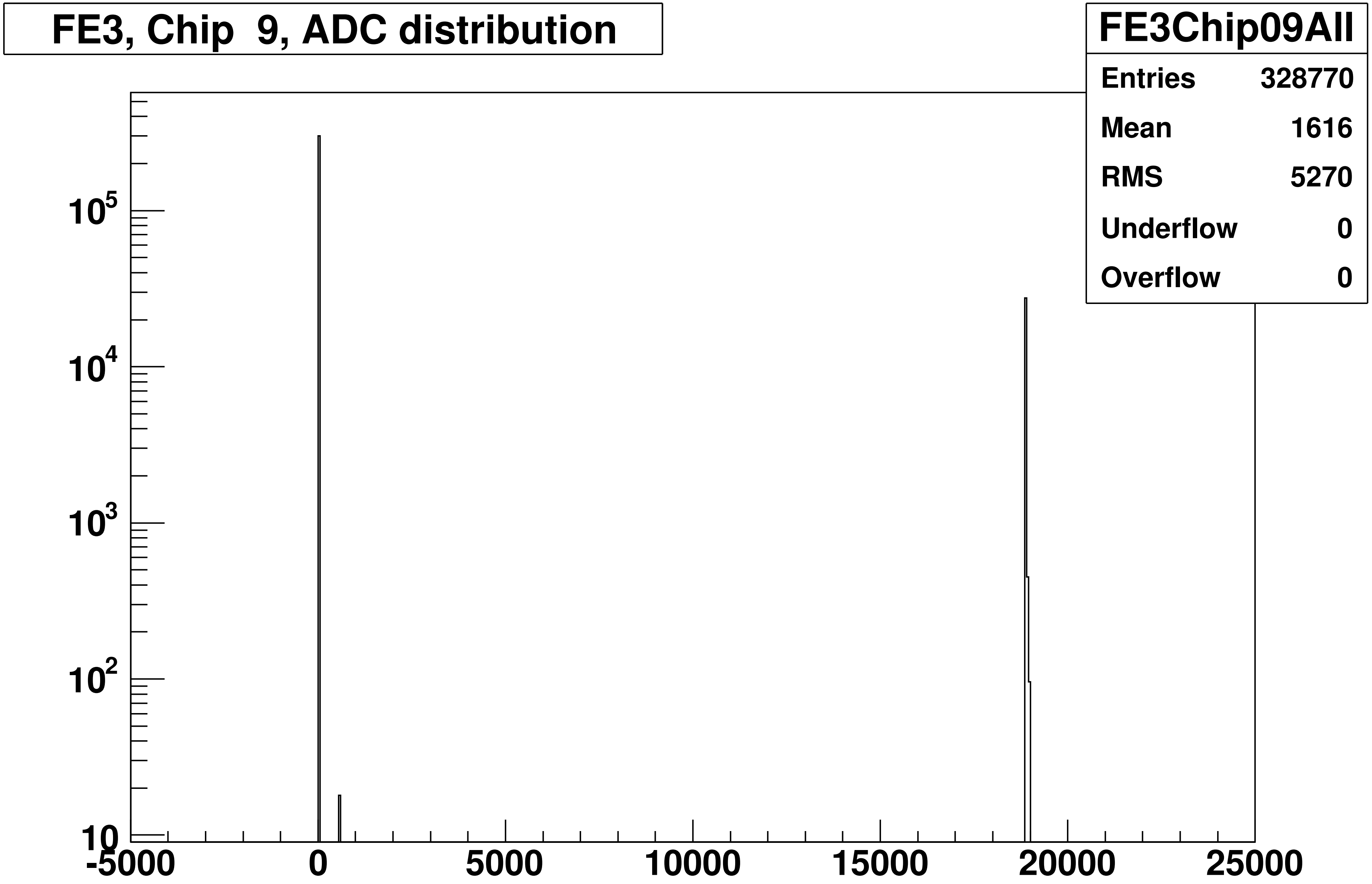
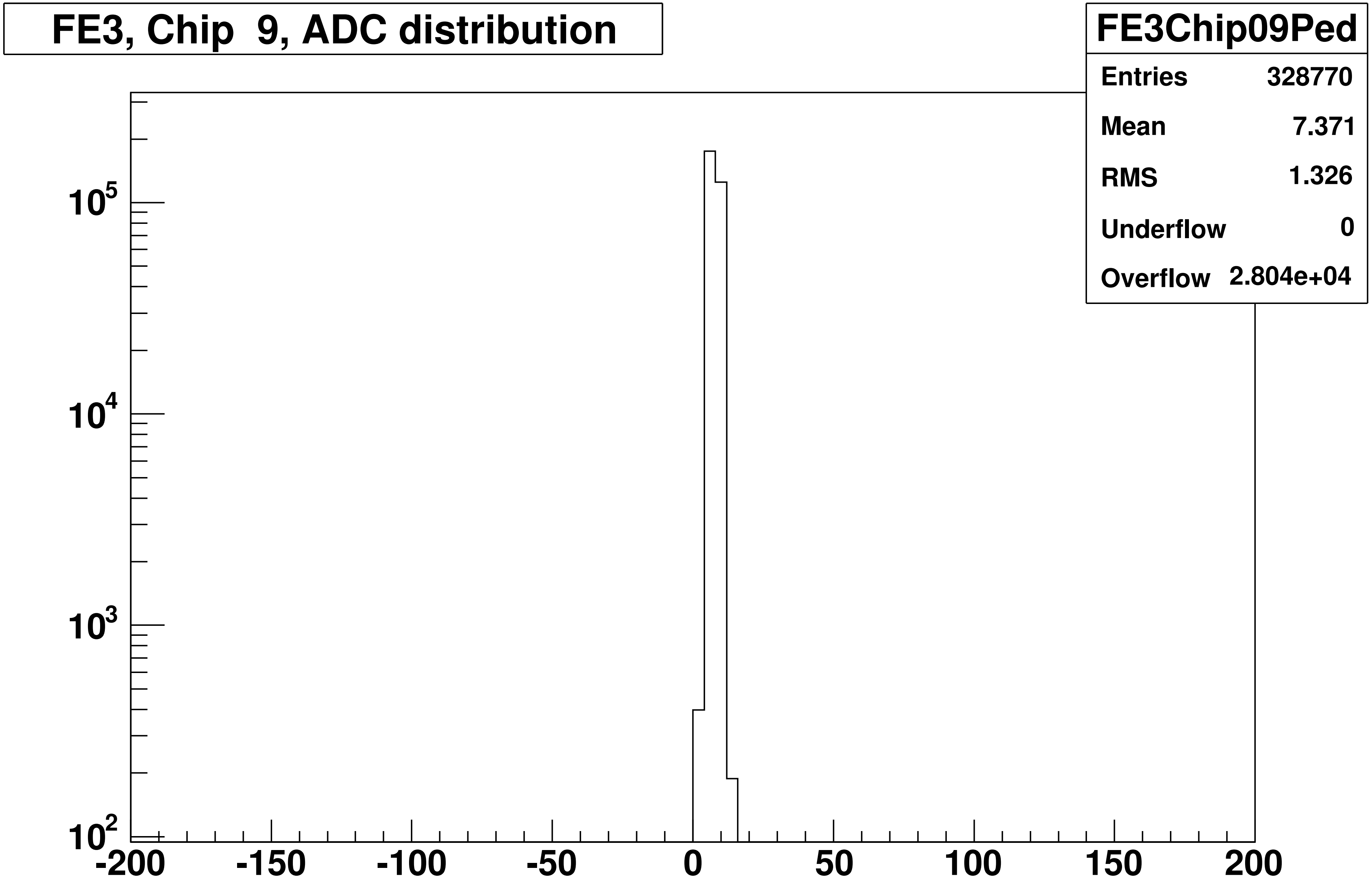
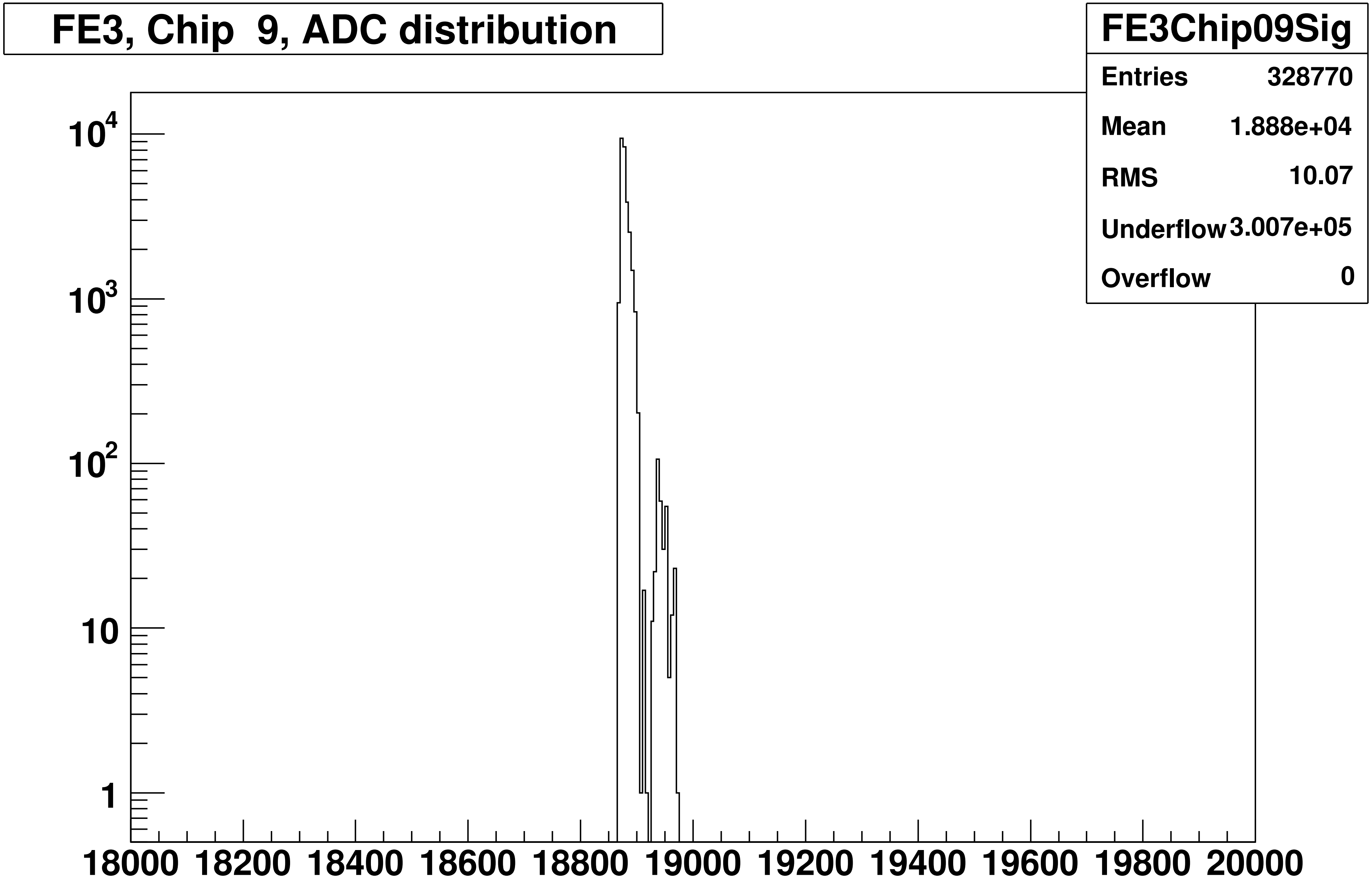
100
150
200

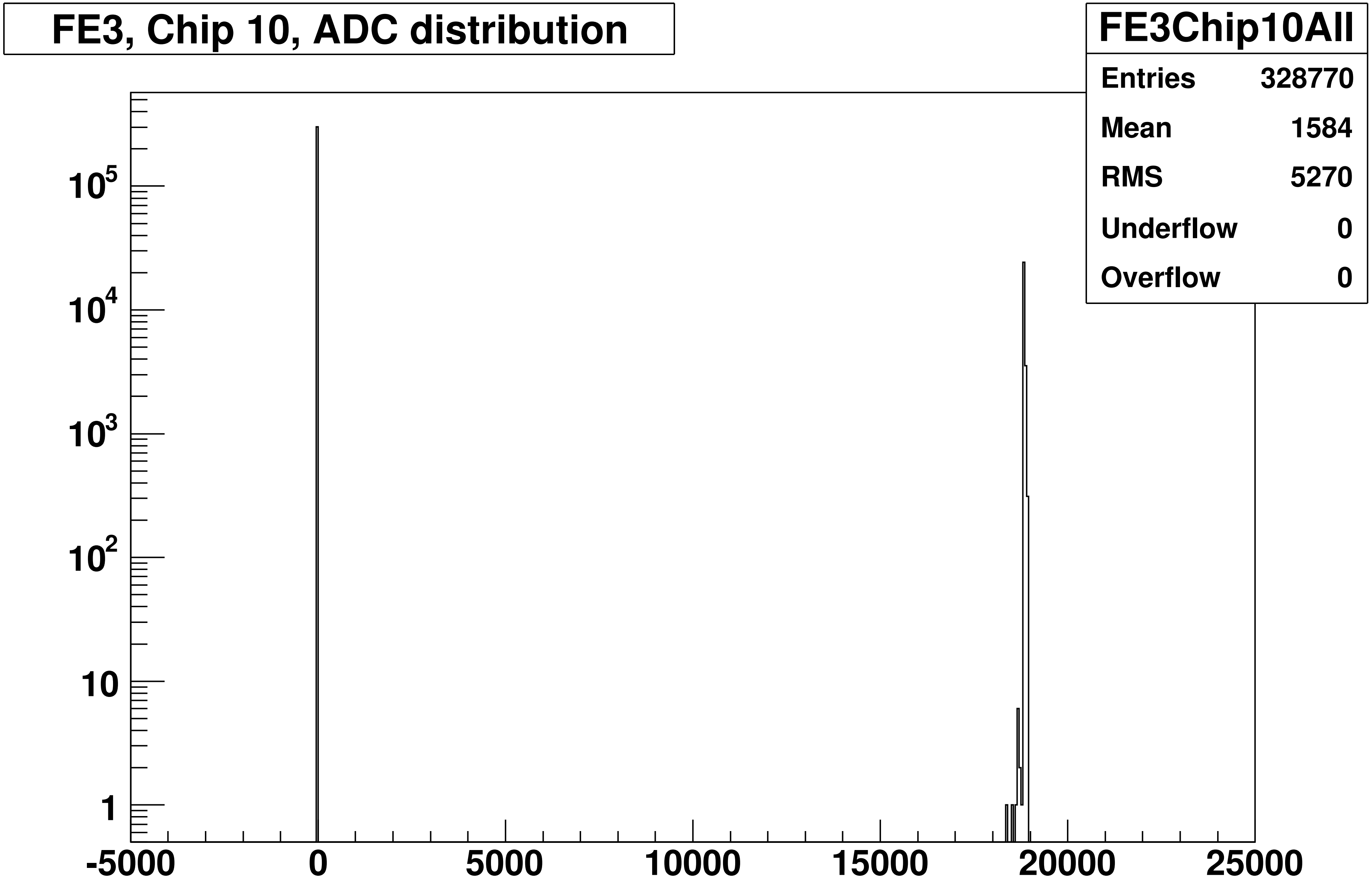

FE3, Chip 8, ADC distribution
FE3Chip08Sig
Entries 328770
Mean 1.89e+04
RMS 9.652
Underflow 3.007e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000

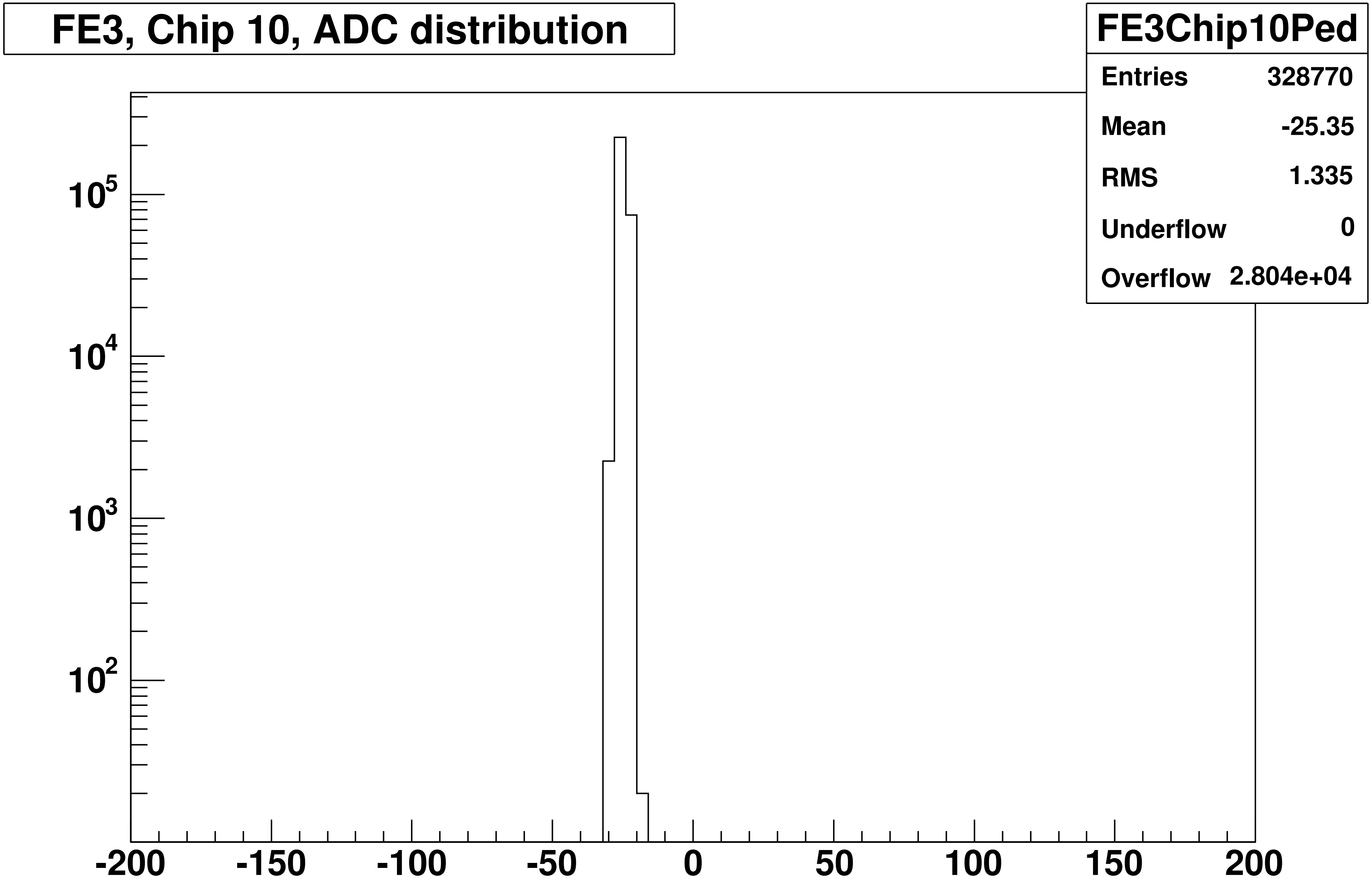

FE3, Chip 9, ADC distribution
FE3Chip09All
Entries 328770
Mean 1616
RMS 5270
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE3, Chip 9, ADC distribution
FE3Chip09Ped
Entries 328770
Mean 7.371
RMS 1.326
Underflow 0
Overflow 2.804e+04
10^5
10^4
10^3
10^2
-200
-150
-100
-50
0
50
100
150
200

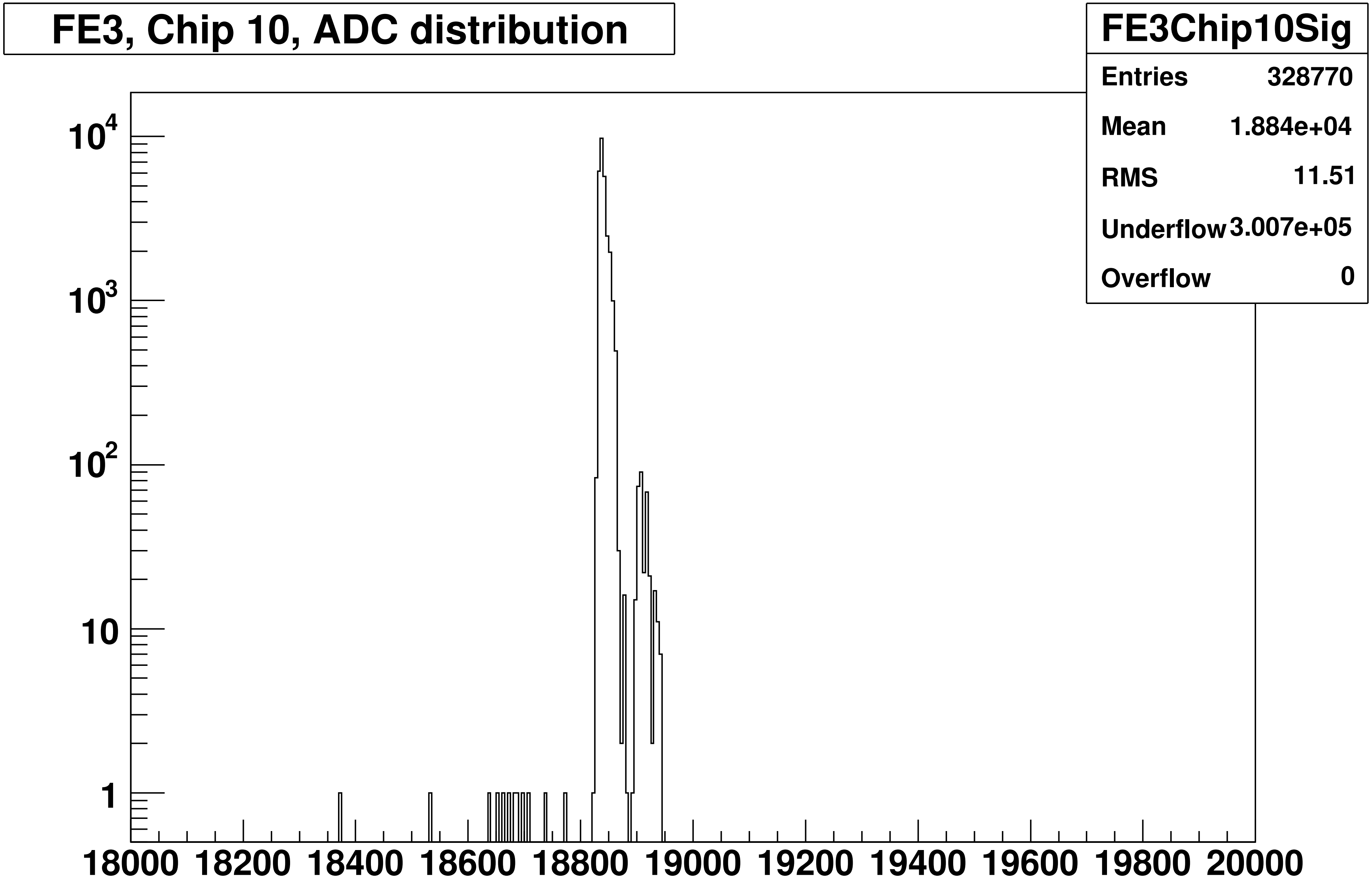


FE3, Chip 9, ADC distribution
FE3Chip09Sig
Entries 328770
Mean 1.888e+04
RMS 10.07
Underflow 3.007e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000

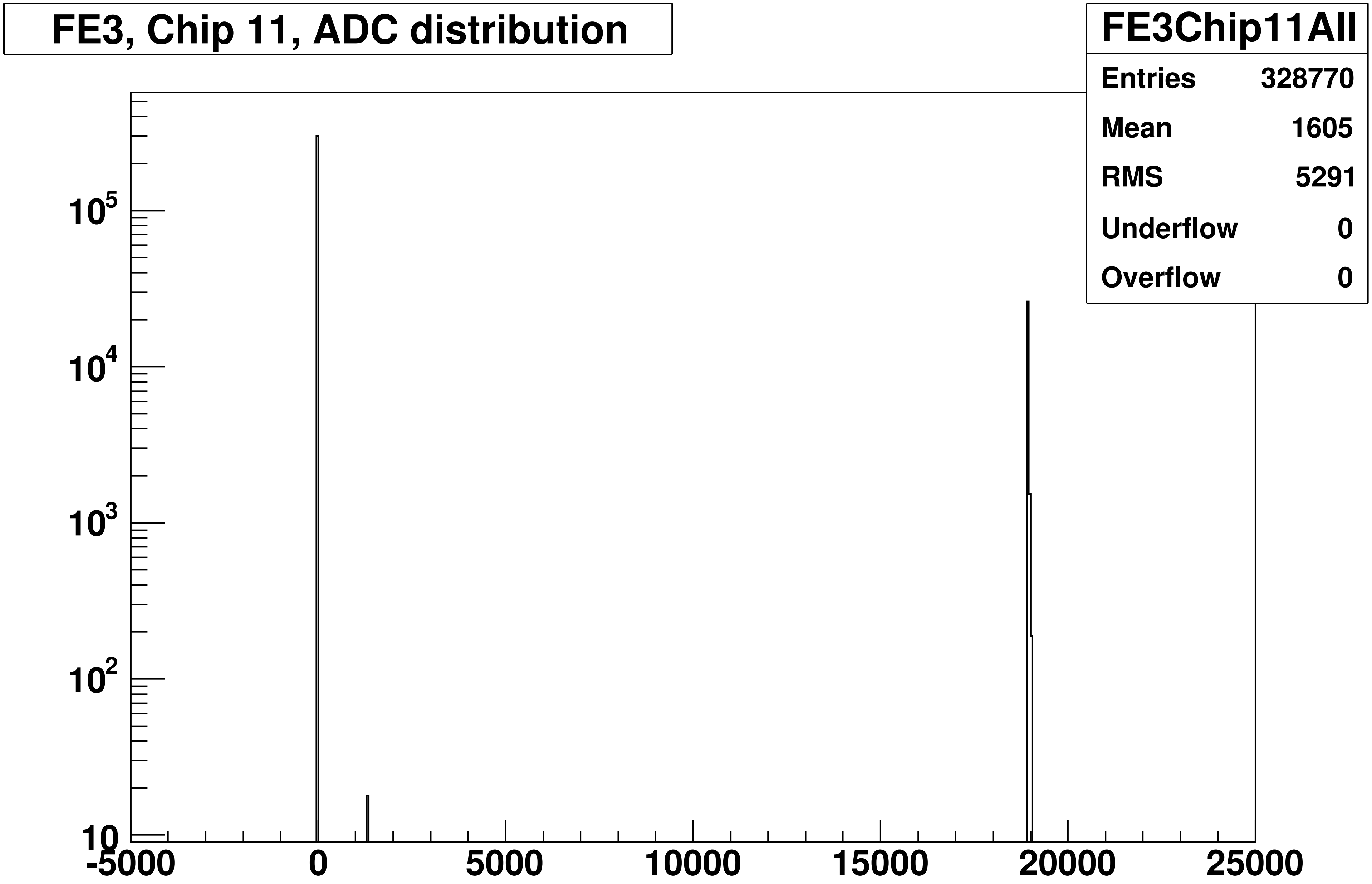

FE3, Chip 10, ADC distribution
FE3Chip10All
Entries 328770
Mean 1584
RMS 5270
Underflow 0
Overflow 0
1
10
10^2
10^3
10^4
10^5
-5000
0
5000
10000
15000
20000
25000

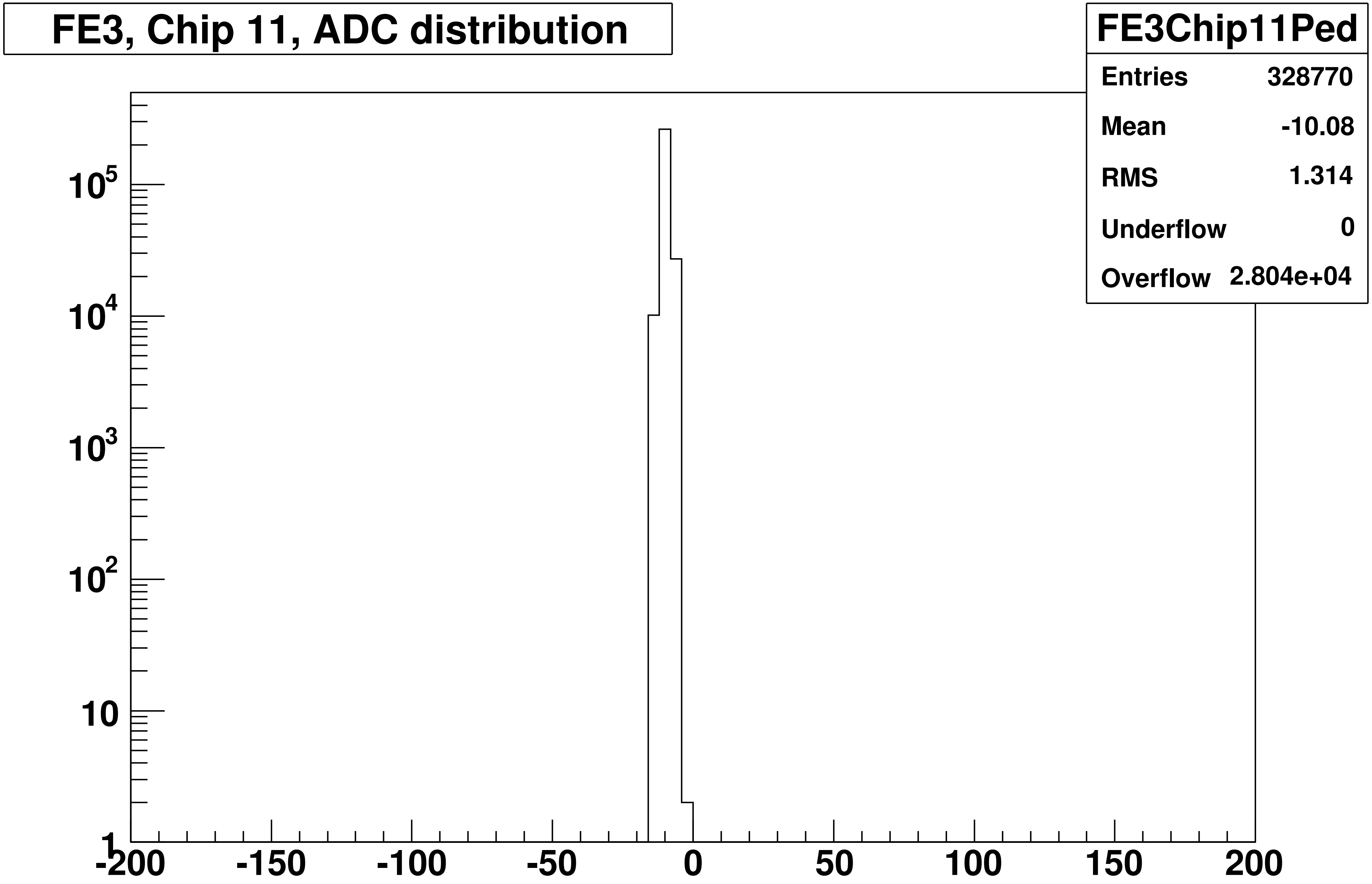


FE3, Chip 10, ADC distribution
FE3Chip10Ped
Entries 328770
Mean -25.35
RMS 1.335
Underflow 0
Overflow 2.804e+04
10^5
10^4
10^3
10^2
-200
-150
-100
-50
0
50
100
150
200



FE3, Chip 10, ADC distribution
FE3Chip10Sig
Entries 328770
Mean 1.884e+04
RMS 11.51
Underflow 3.007e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000


FE3, Chip 11, ADC distribution
FE3Chip11All
Entries 328770
Mean 1605
RMS 5291
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE3, Chip 11, ADC distribution
FE3Chip11Ped
Entries 328770
Mean -10.08
RMS 1.314
Underflow 0
Overflow 2.804e+04
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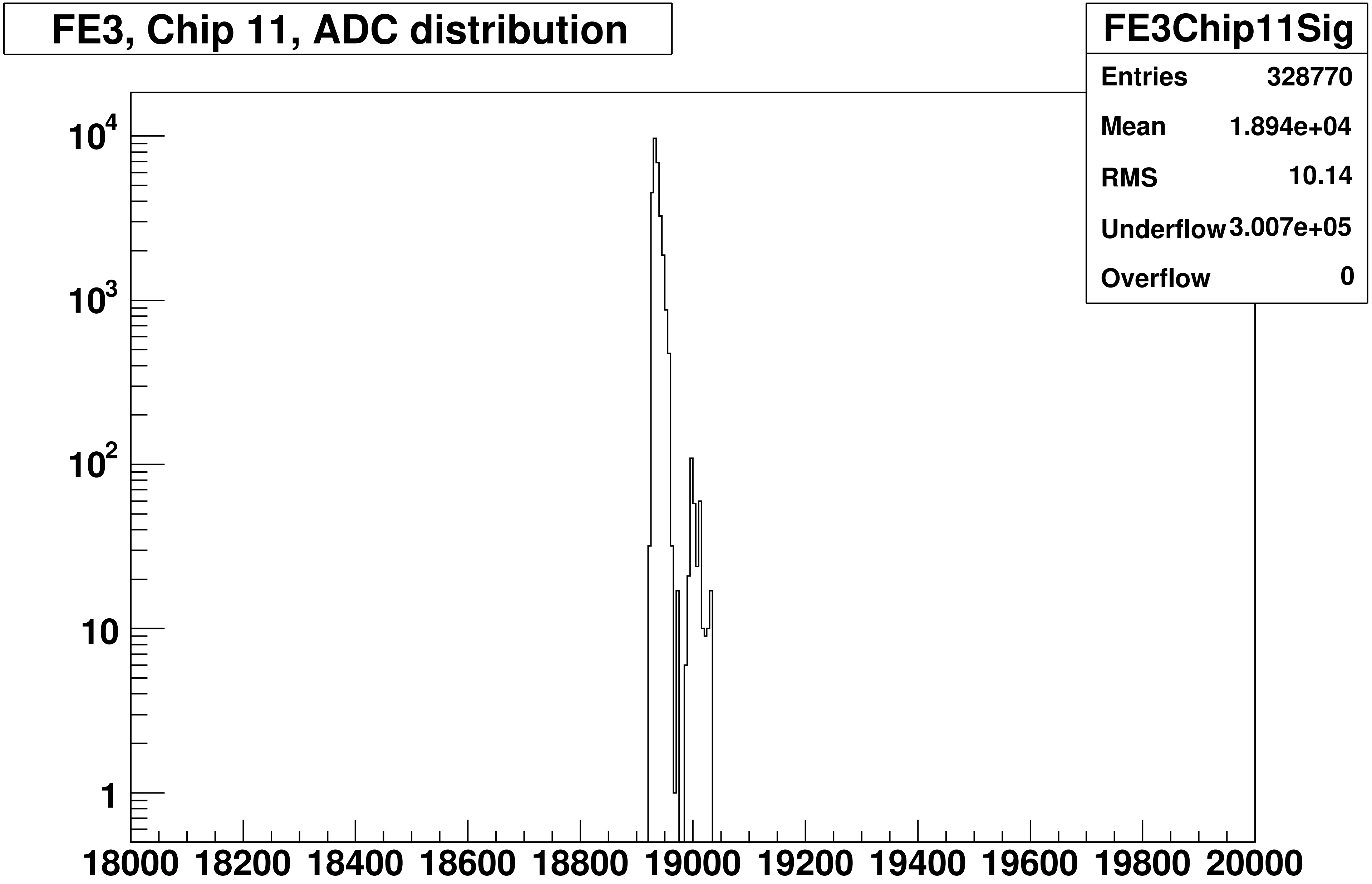
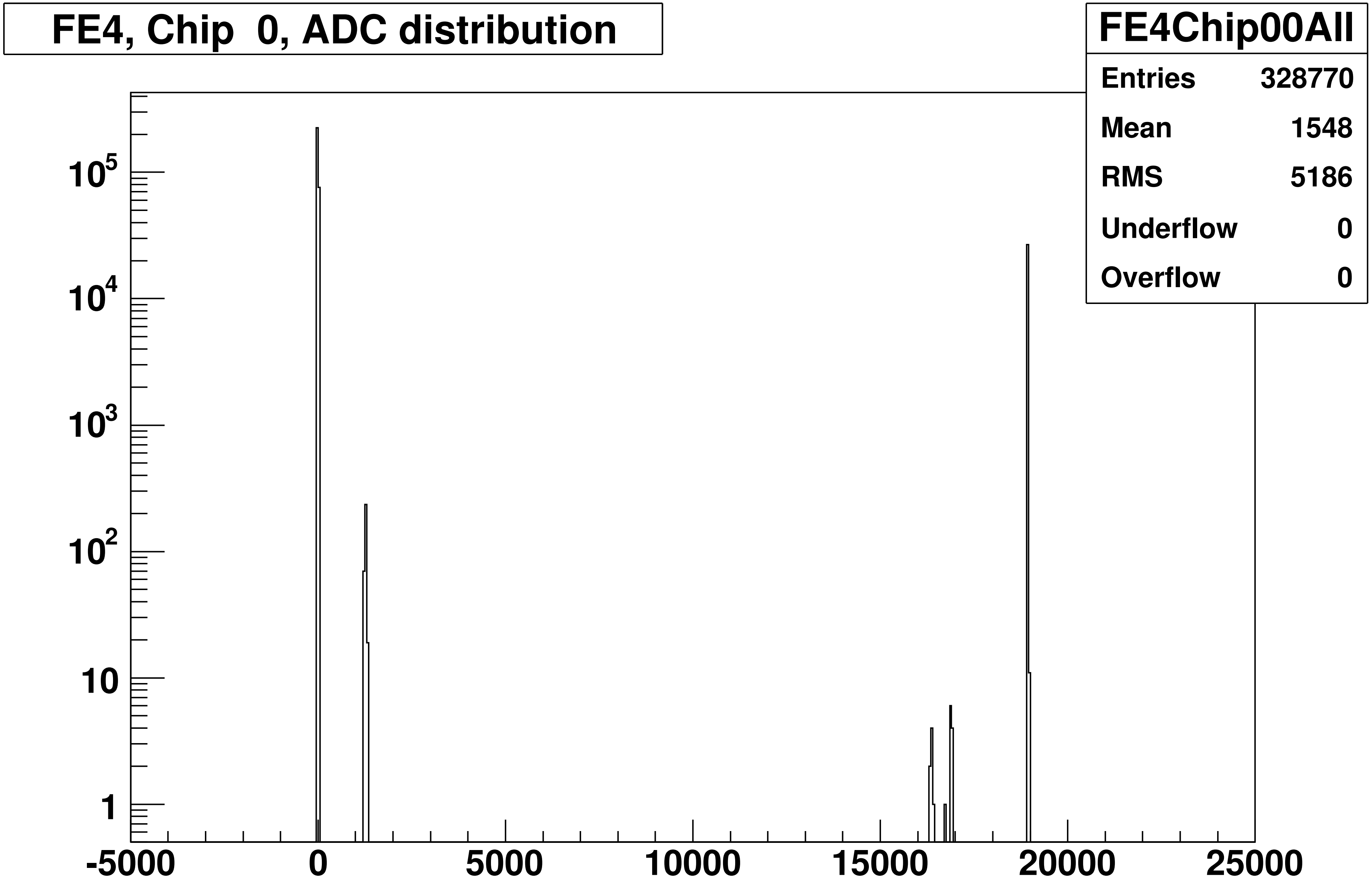
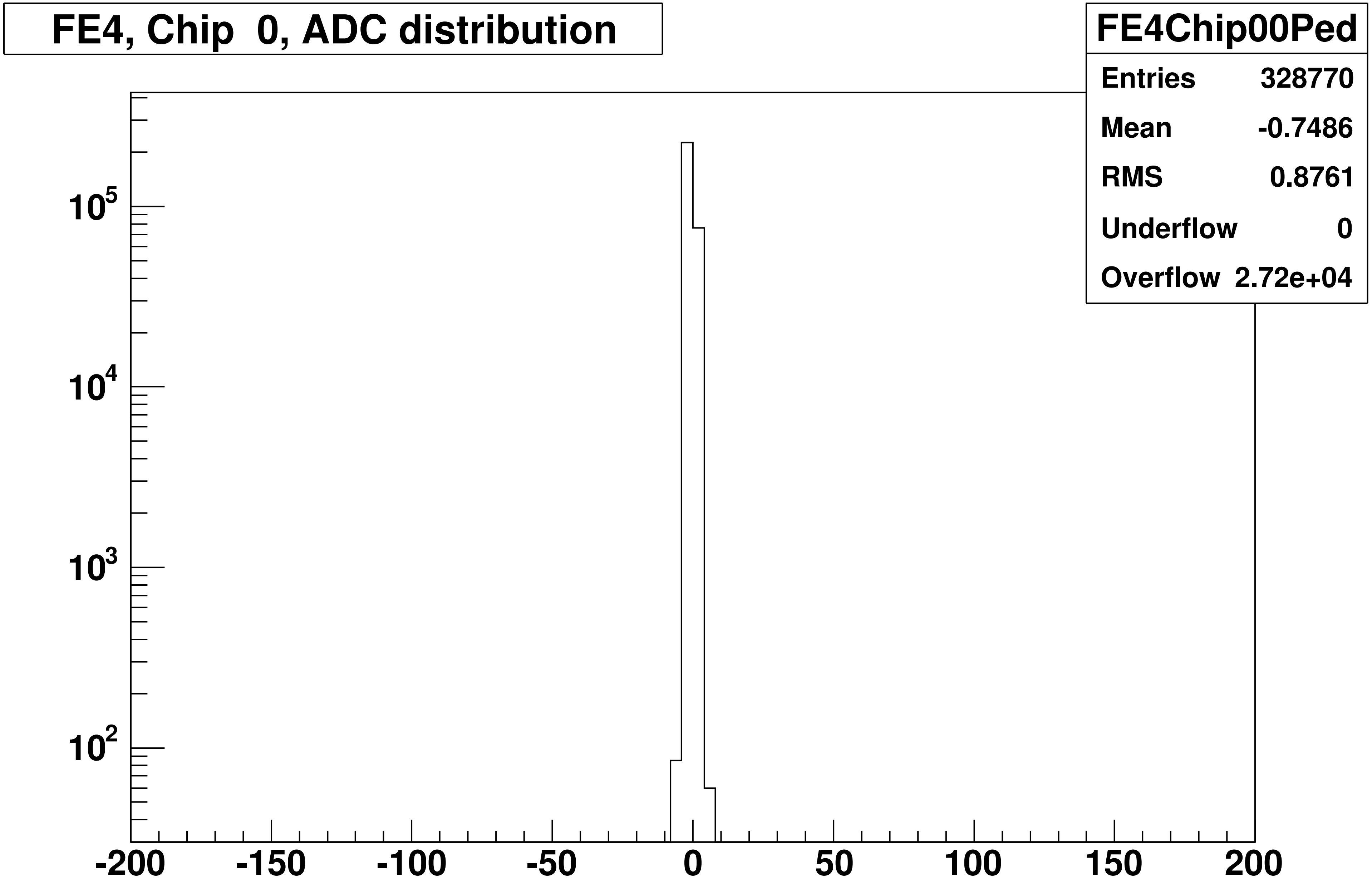
10
10^2
10^3
10^4
10^5
-200
-150
-100
-50
0
50
100
150
200


FE3, Chip 11, ADC distribution
FE3Chip11Sig
Entries 328770
Mean 1.894e+04
RMS 10.14
Underflow 3.007e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000



FE4, Chip 0, ADC distribution
FE4Chip00All
Entries 328770
Mean 1548
RMS 5186
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE4, Chip 0, ADC distribution
FE4Chip00Ped
Entries 328770
Mean -0.7486
RMS 0.8761
Underflow 0
Overflow 2.72e+04
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10^4
10^3
10^2
-200
-150
-100
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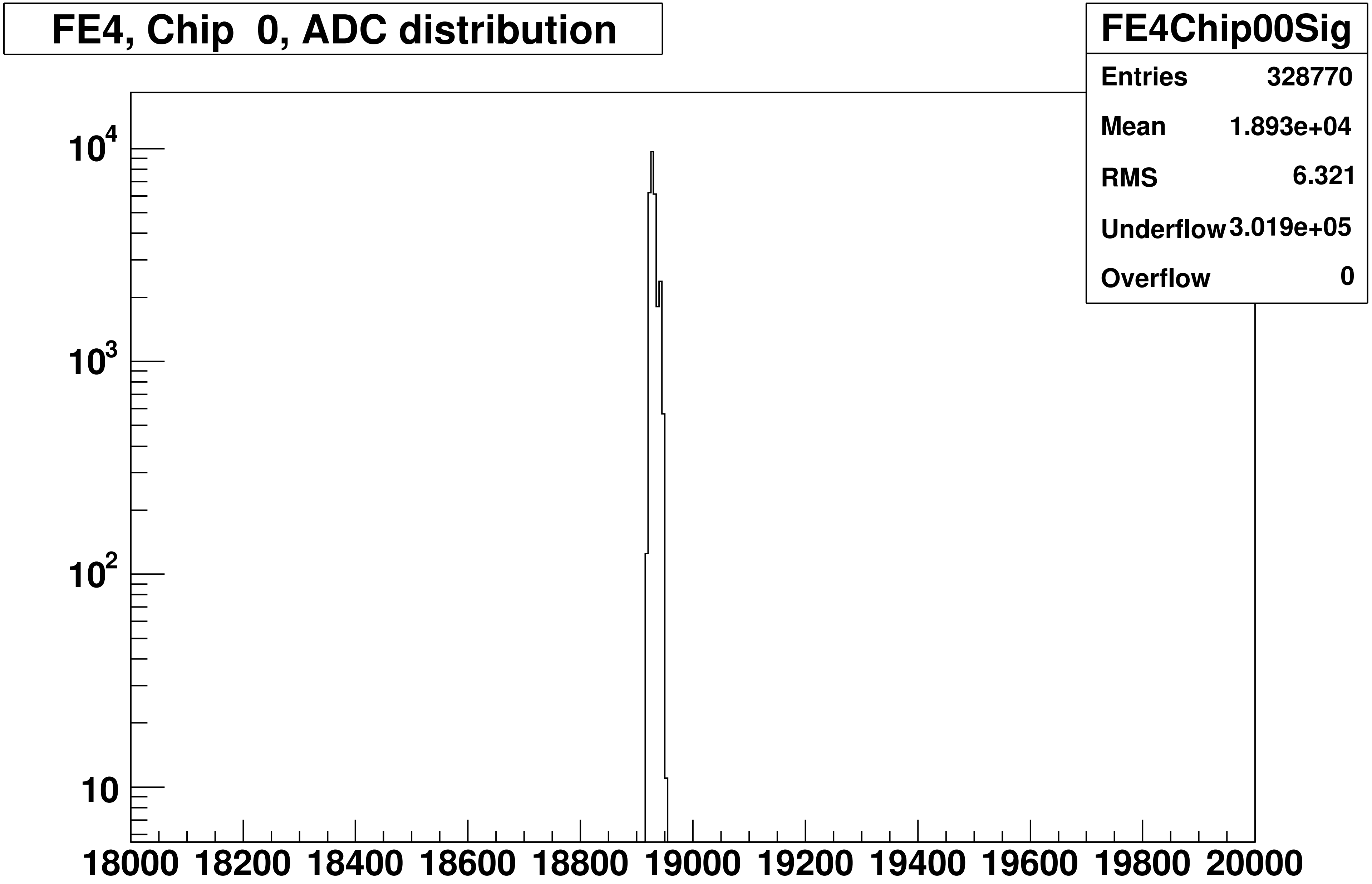
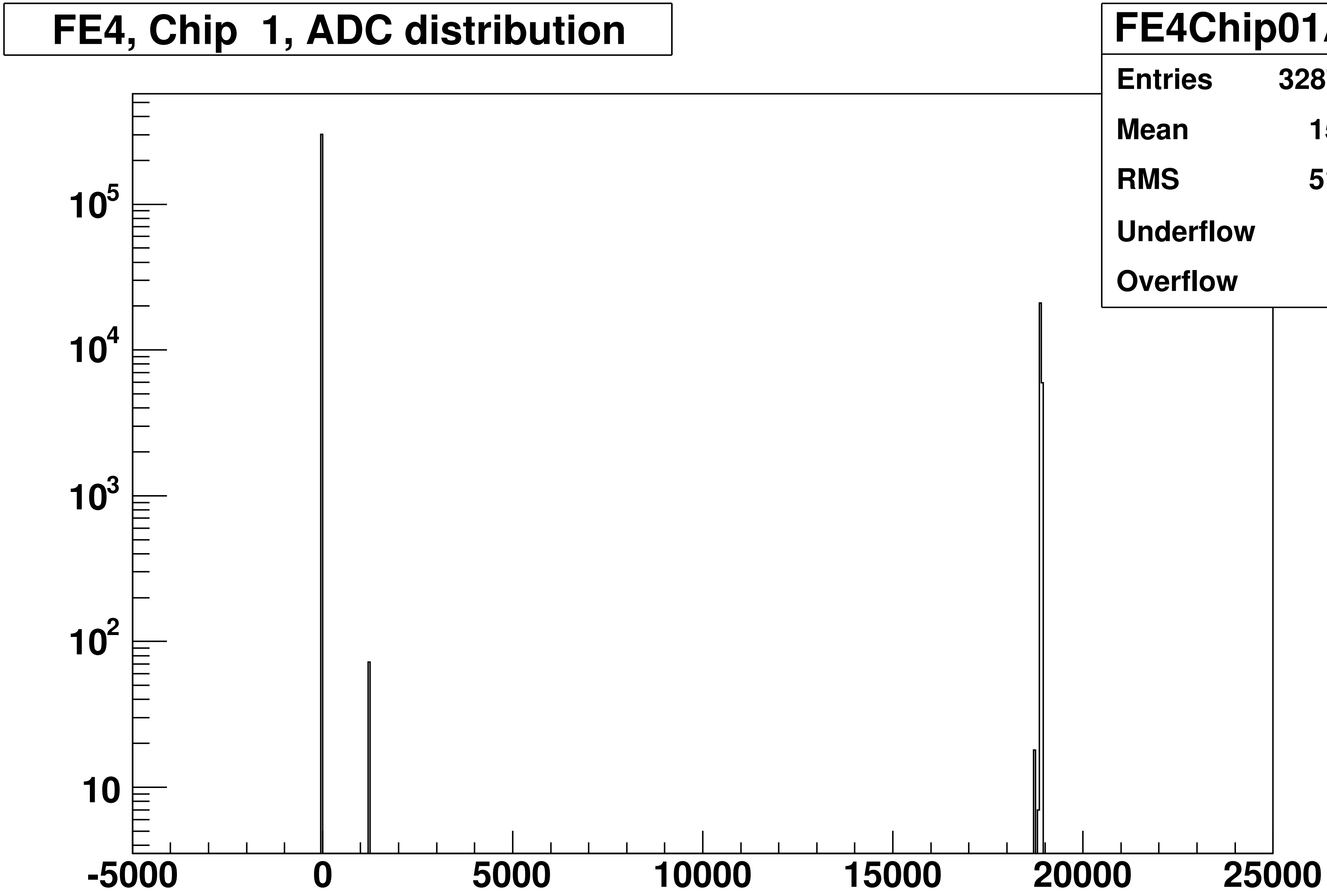
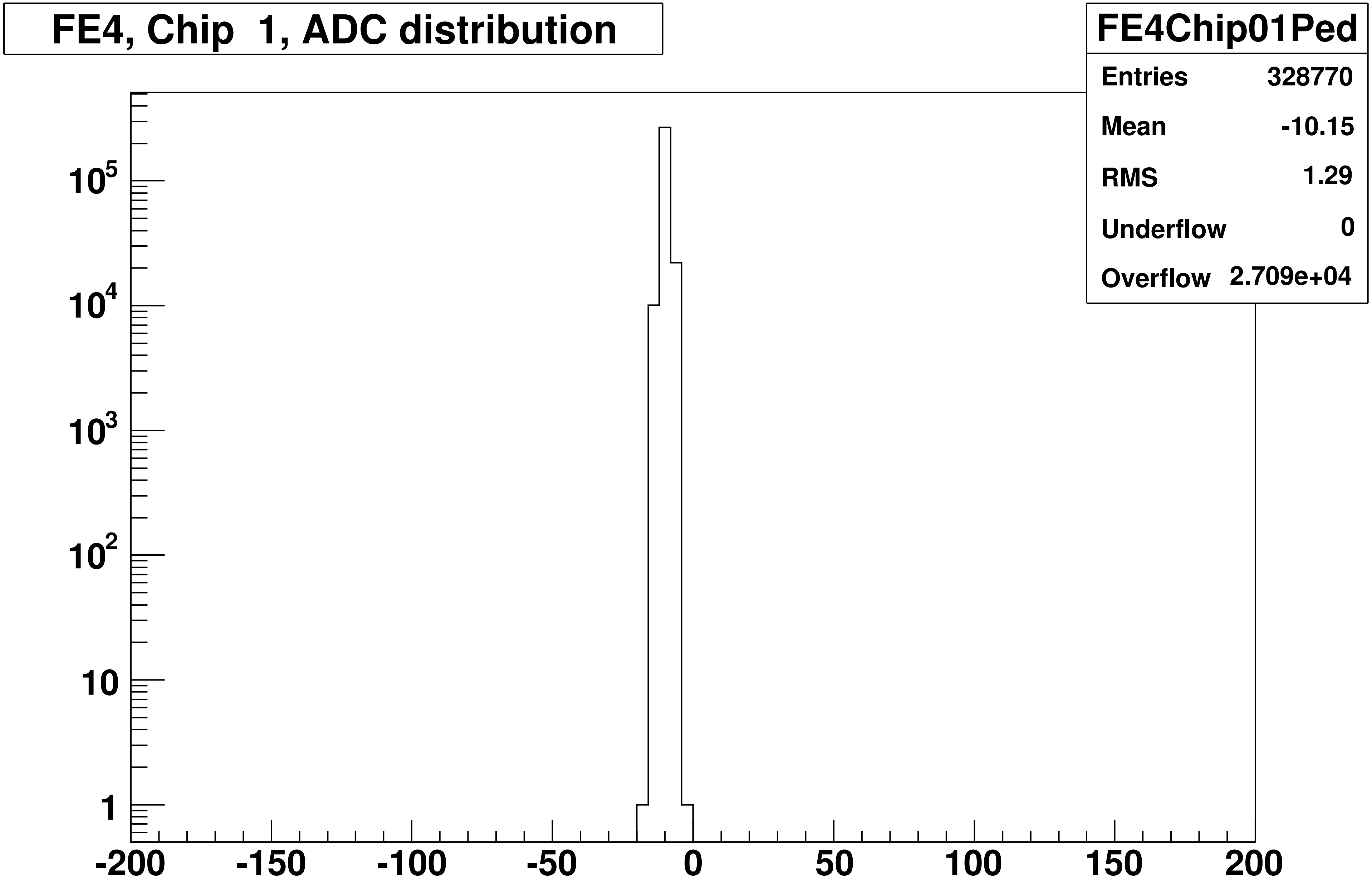
0
50
100
150
200

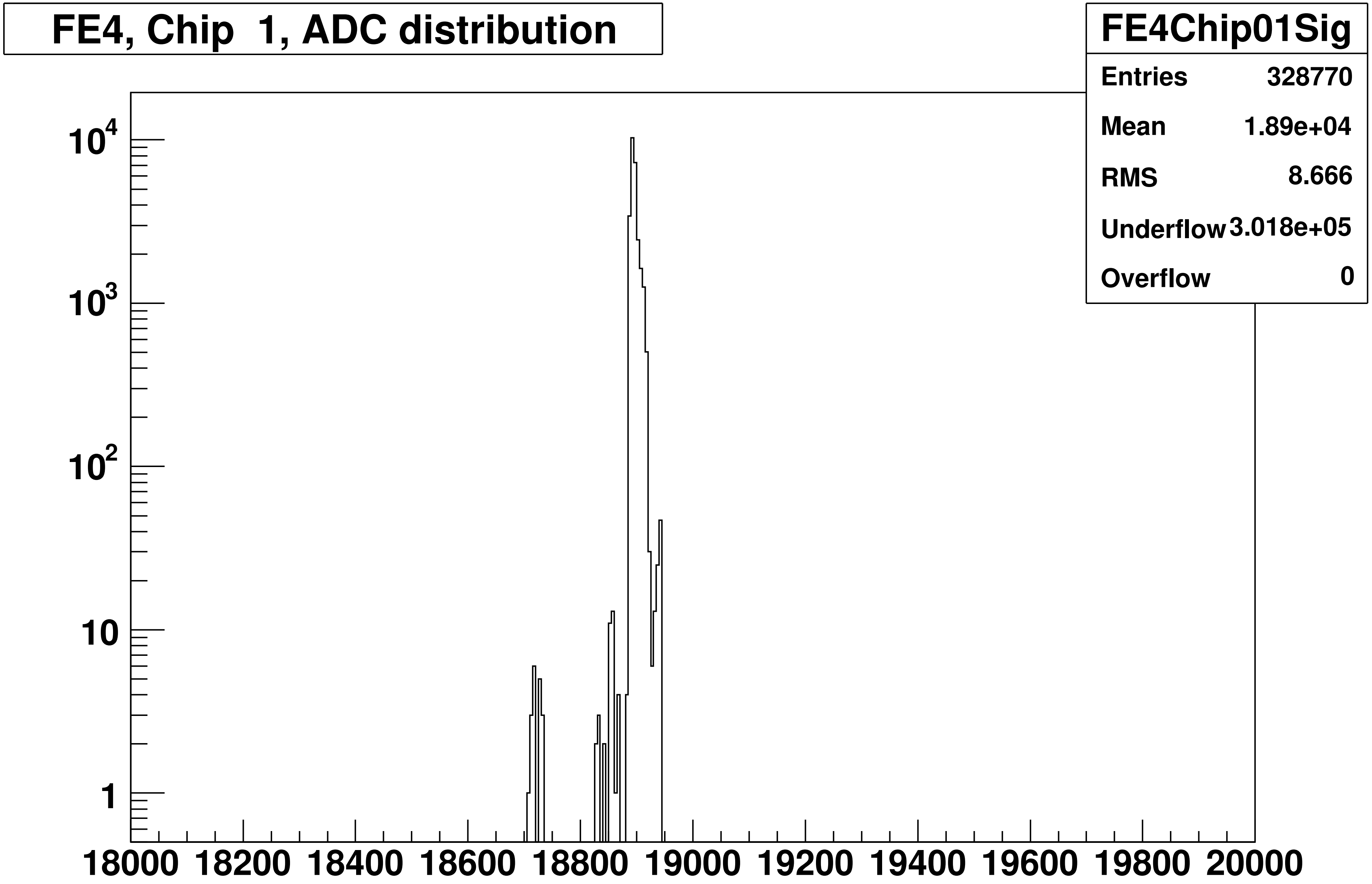


FE4, Chip 0, ADC distribution
FE4Chip00Sig
Entries 328770
Mean 1.893e+04
RMS 6.321
Underflow 3.019e+05
Overflow 0
10^4
10^3
10^2
10
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000

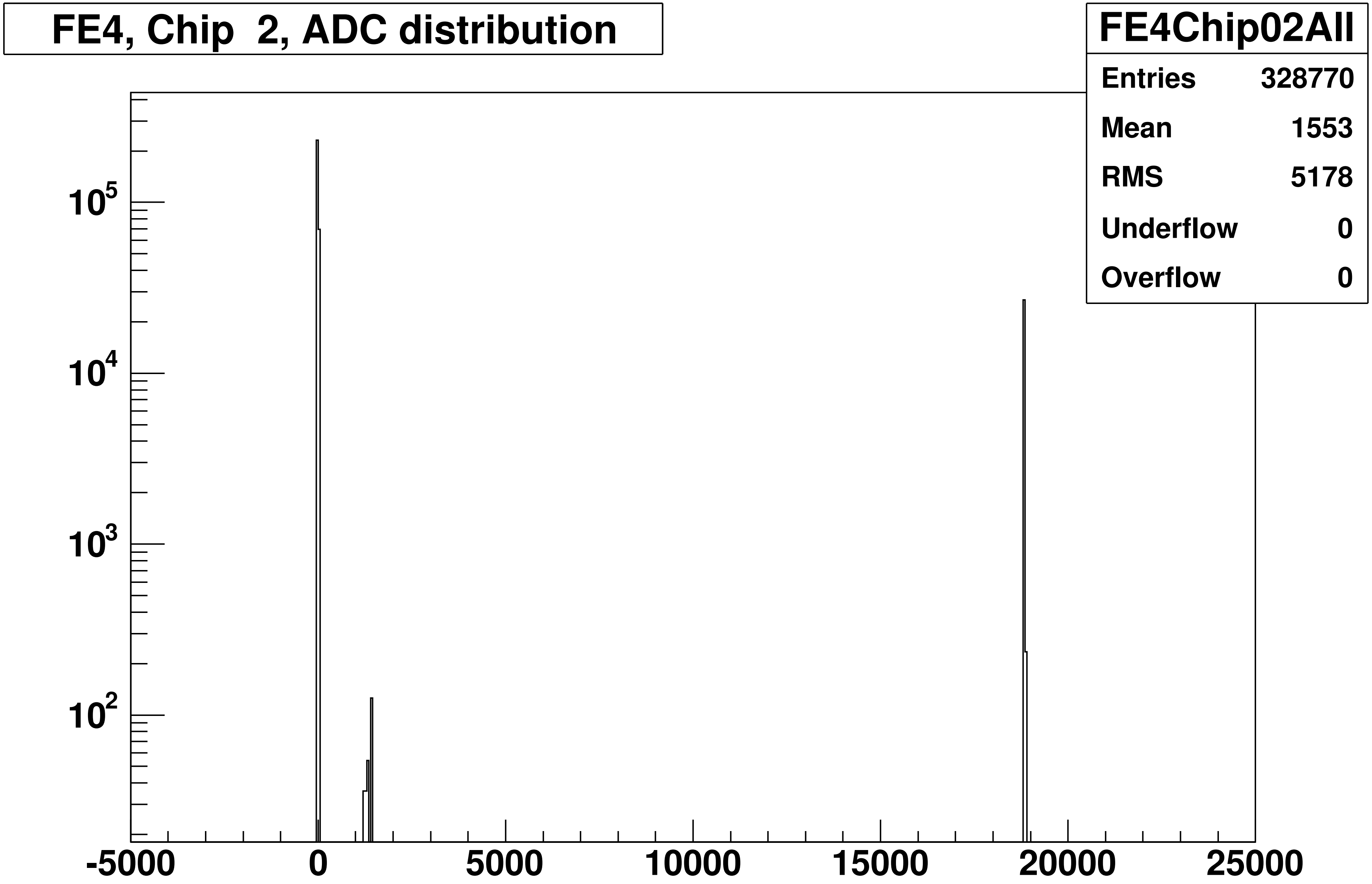


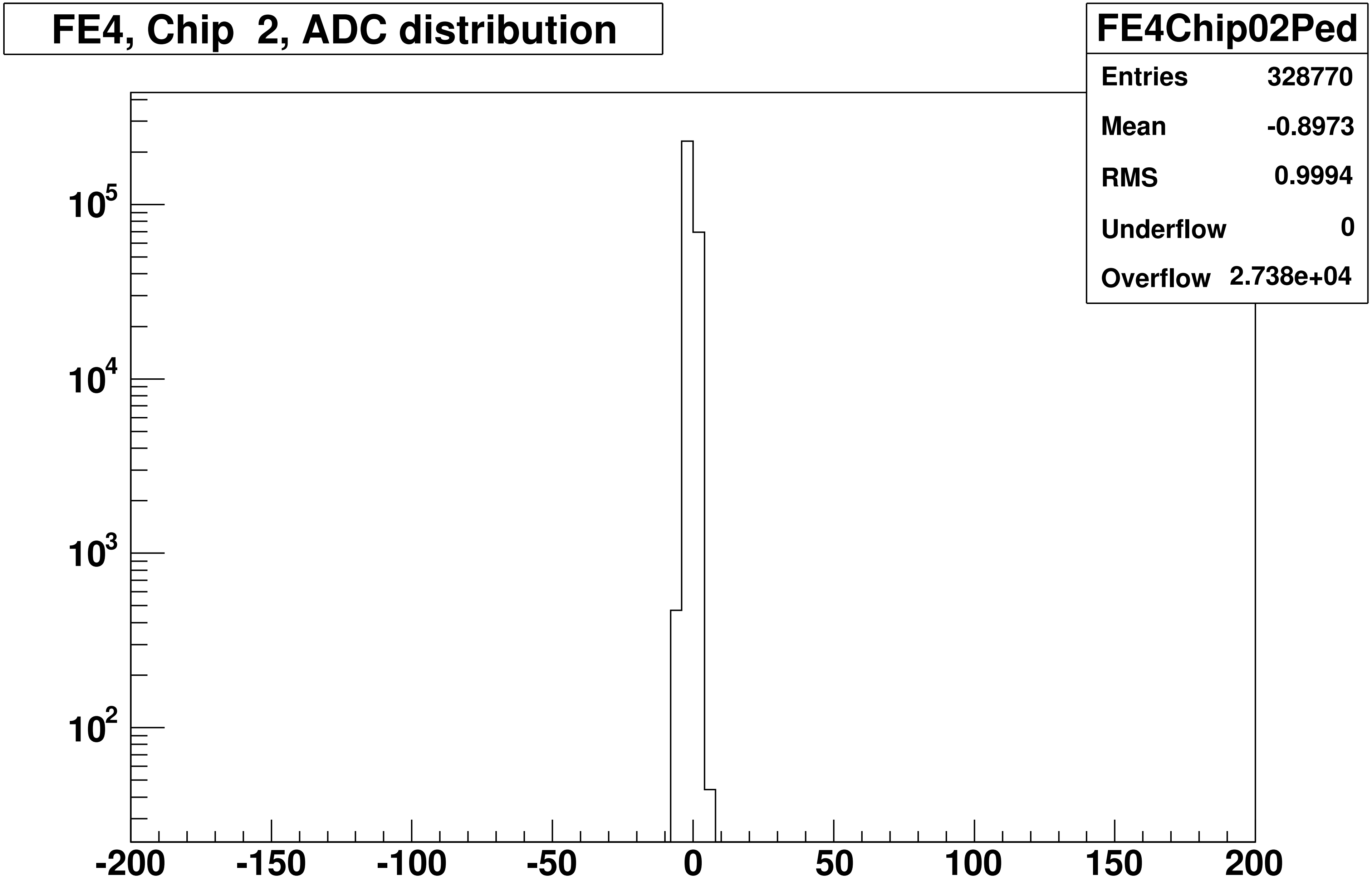
FE4, Chip 1, ADC distribution
FE4Chip01All
Entries 328770
Mean 1544
RMS 5192
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000

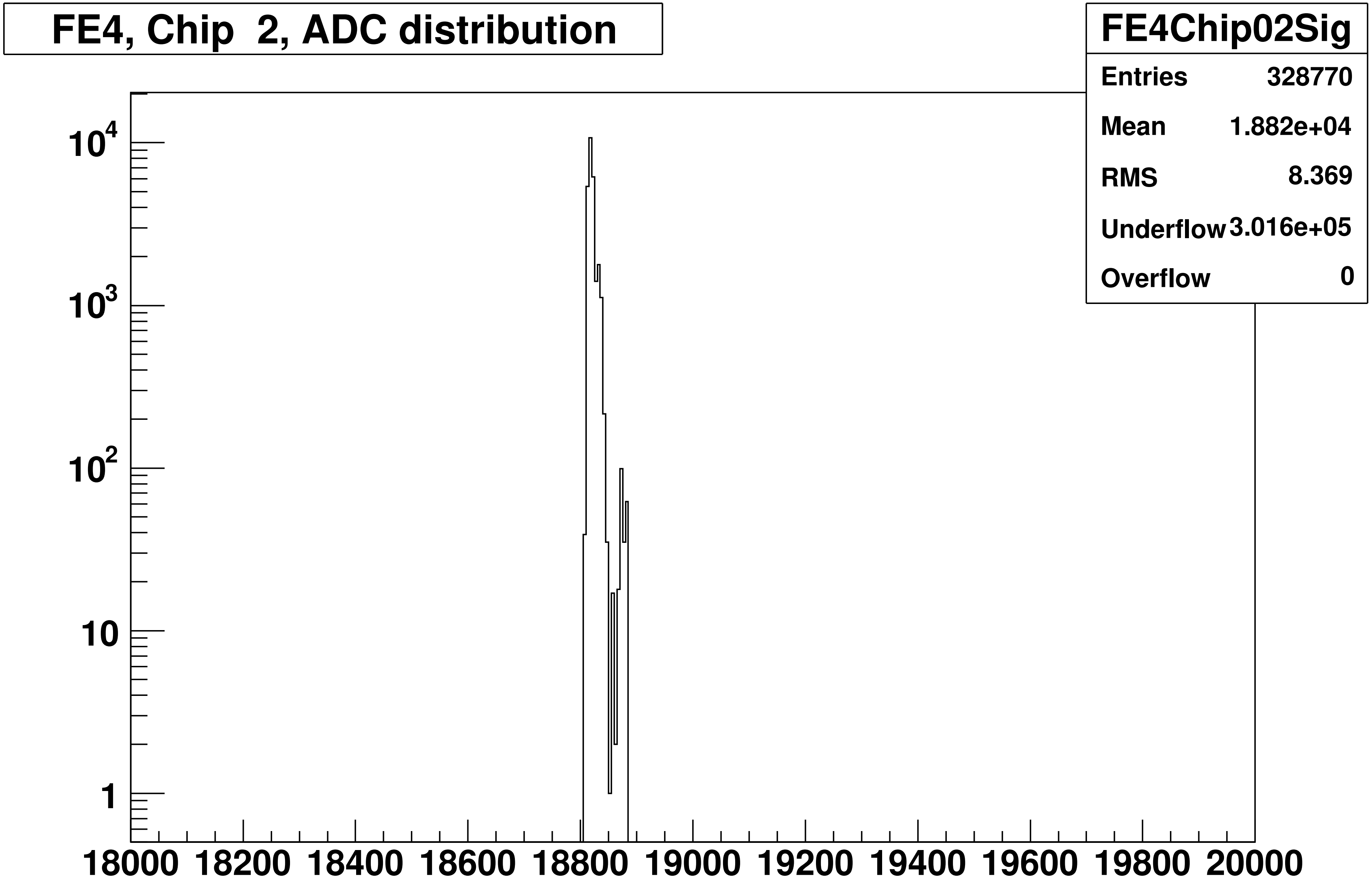

FE4, Chip 1, ADC distribution
FE4Chip01Ped
Entries 328770
Mean -10.15
RMS 1.29
Underflow 0
Overflow 2.709e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
200



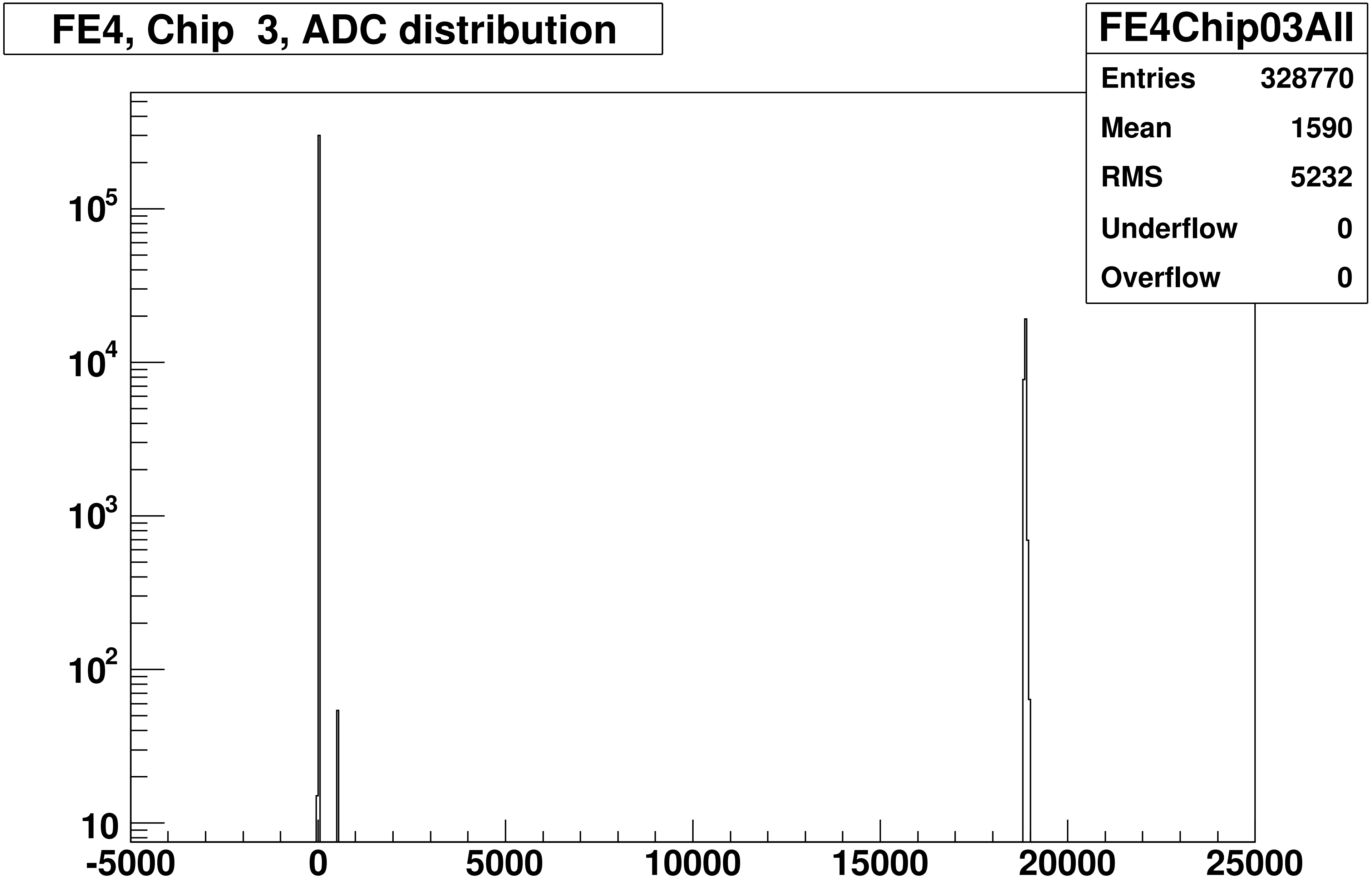
FE4, Chip 1, ADC distribution
FE4Chip01Sig
Entries 328770
Mean 1.89e+04
RMS 8.666
Underflow 3.018e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE4, Chip 2, ADC distribution
FE4Chip02All
Entries 328770
Mean 1553
RMS 5178
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000

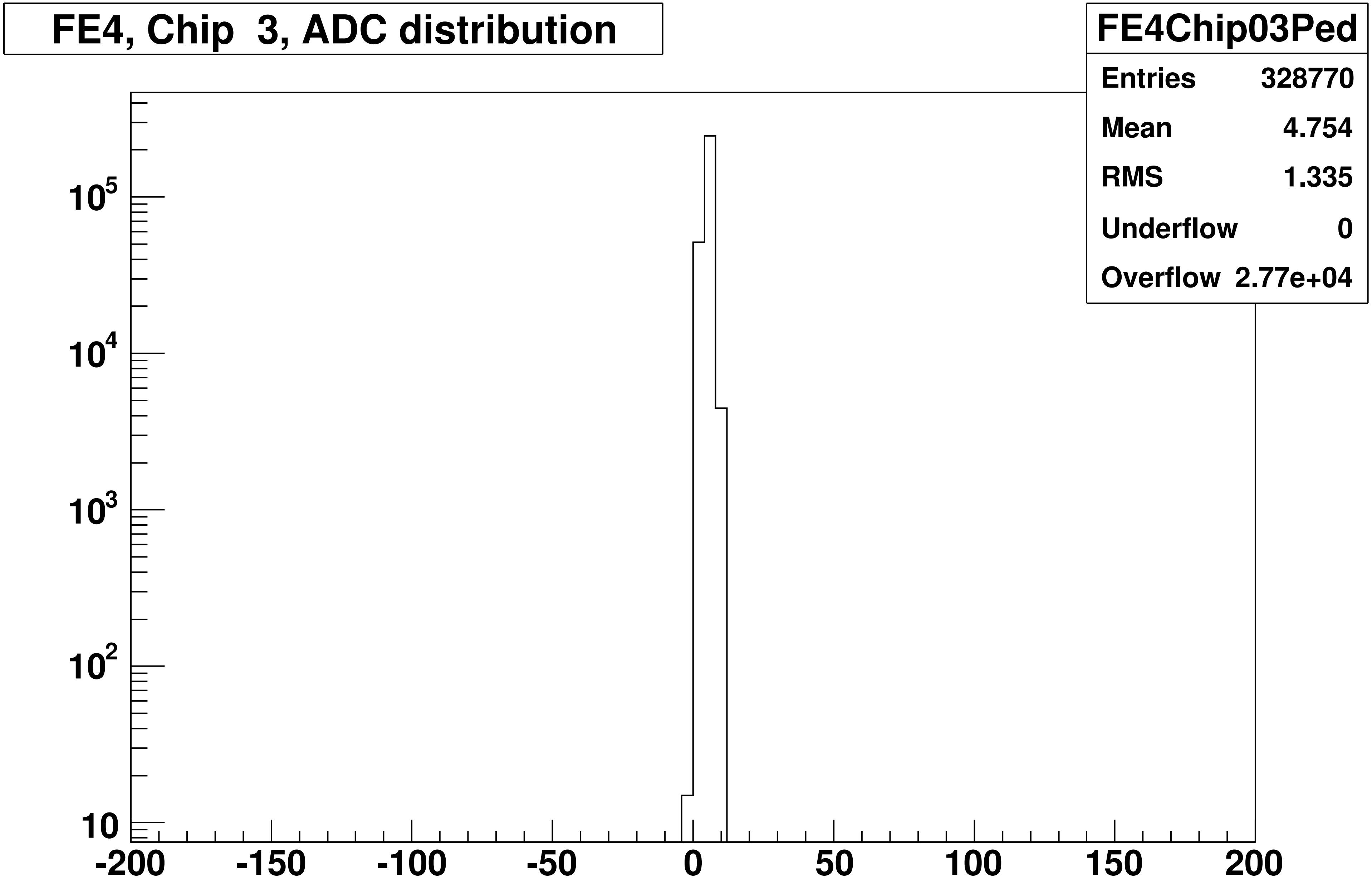

FE4, Chip 2, ADC distribution
FE4Chip02Ped
Entries 328770
Mean -0.8973
RMS 0.9994
Underflow 0
Overflow 2.738e+04
10^5
10^4
10^3
10^2
-200
-150
-100
-50
0
50
100
150
200

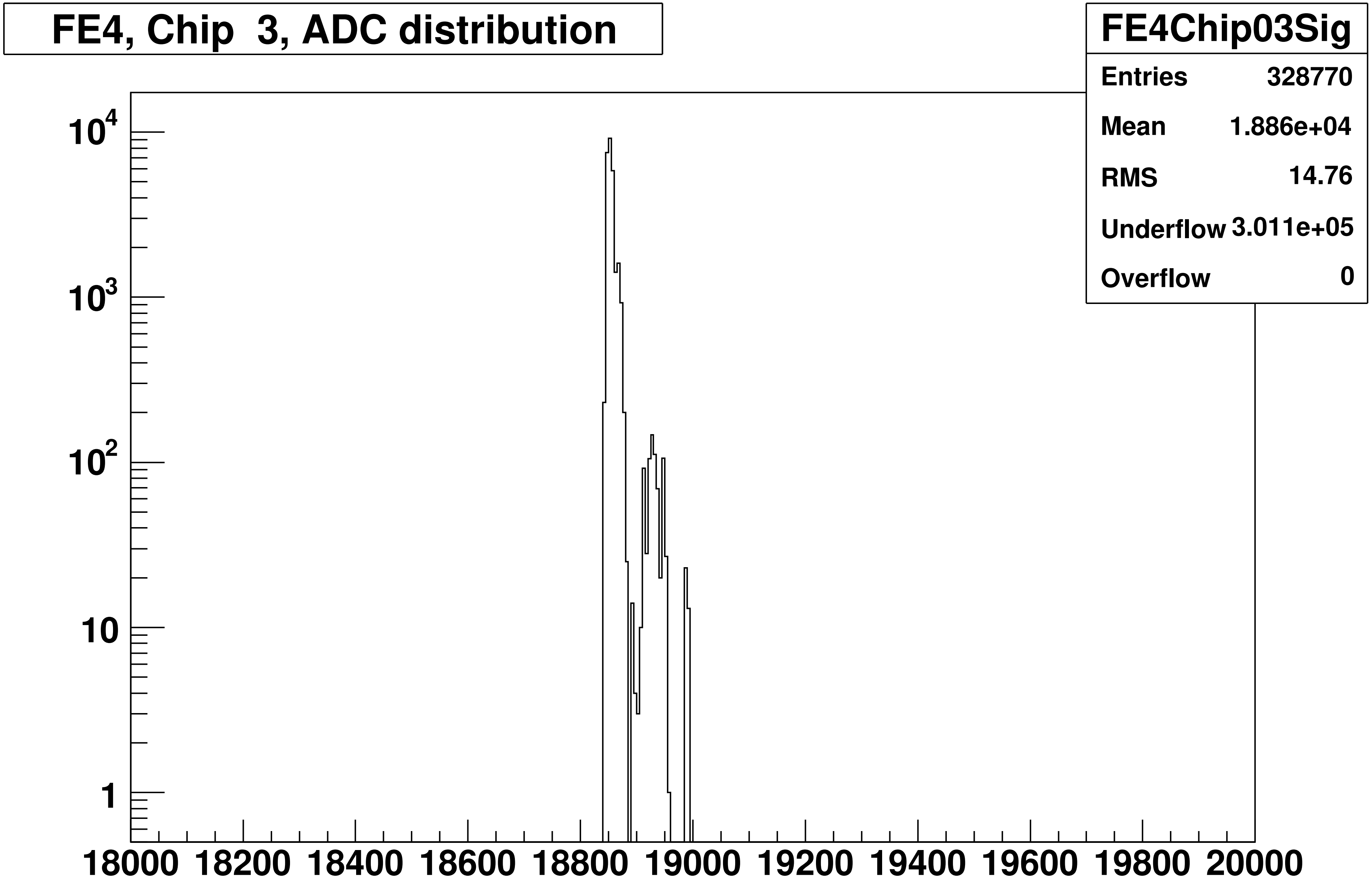


FE4, Chip 2, ADC distribution
FE4Chip02Sig
Entries 328770
Mean 1.882e+04
RMS 8.369
Underflow 3.016e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000

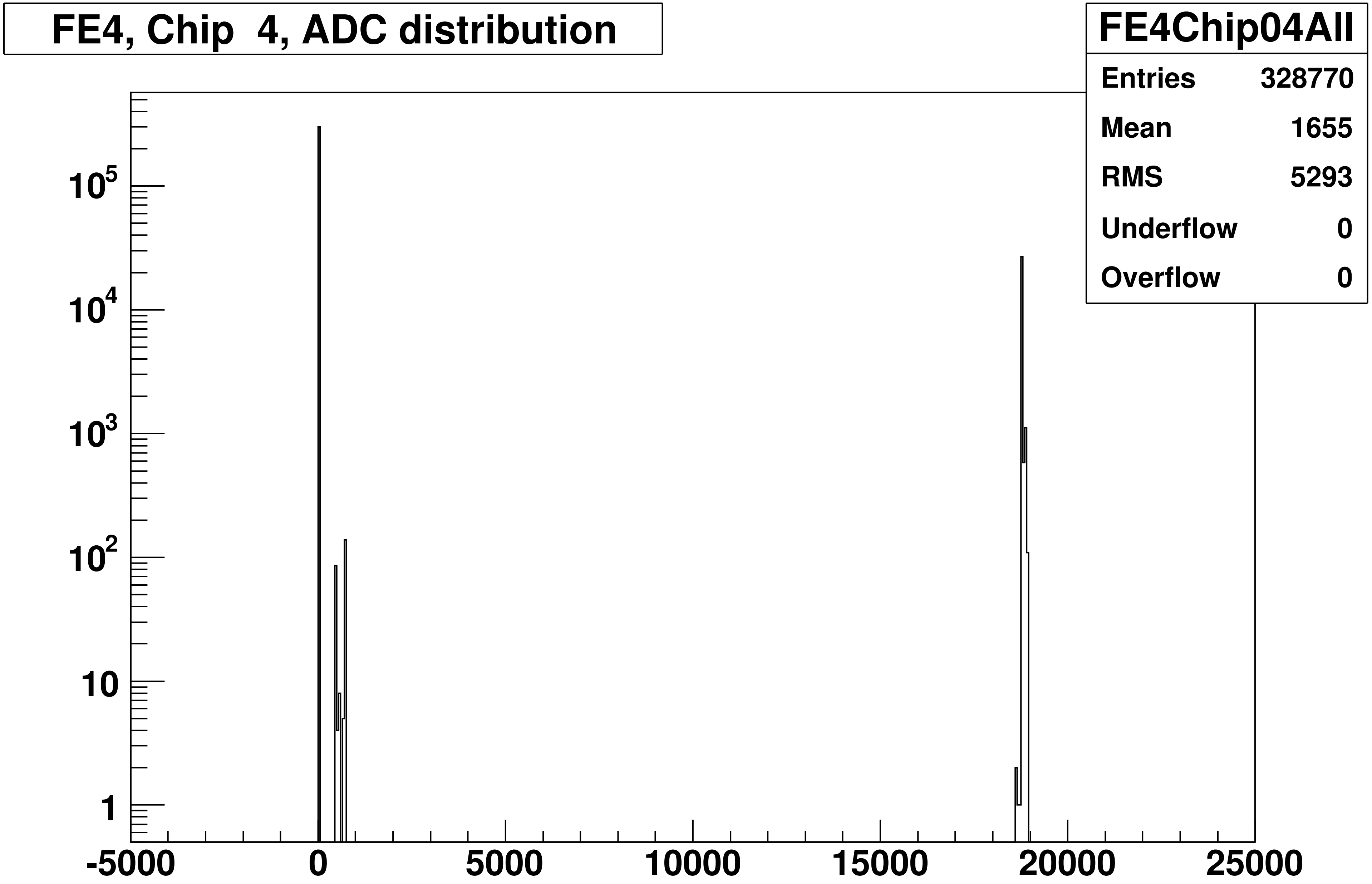


FE4, Chip 3, ADC distribution
FE4Chip03All
Entries 328770
Mean 1590
RMS 5232
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE4, Chip 3, ADC distribution
FE4Chip03Ped
Entries 328770
Mean 4.754
RMS 1.335
Underflow 0
Overflow 2.77e+04
10
10^2
10^3
10^4
10^5
-200
-150
-100
-50
0
50
100
150
200



FE4, Chip 3, ADC distribution
FE4Chip03Sig
Entries 328770
Mean 1.886e+04
RMS 14.76
Underflow 3.011e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000



FE4, Chip 4, ADC distribution
FE4Chip04All
Entries 328770
Mean 1655
RMS 5293
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
1
-5000
0
5000
10000
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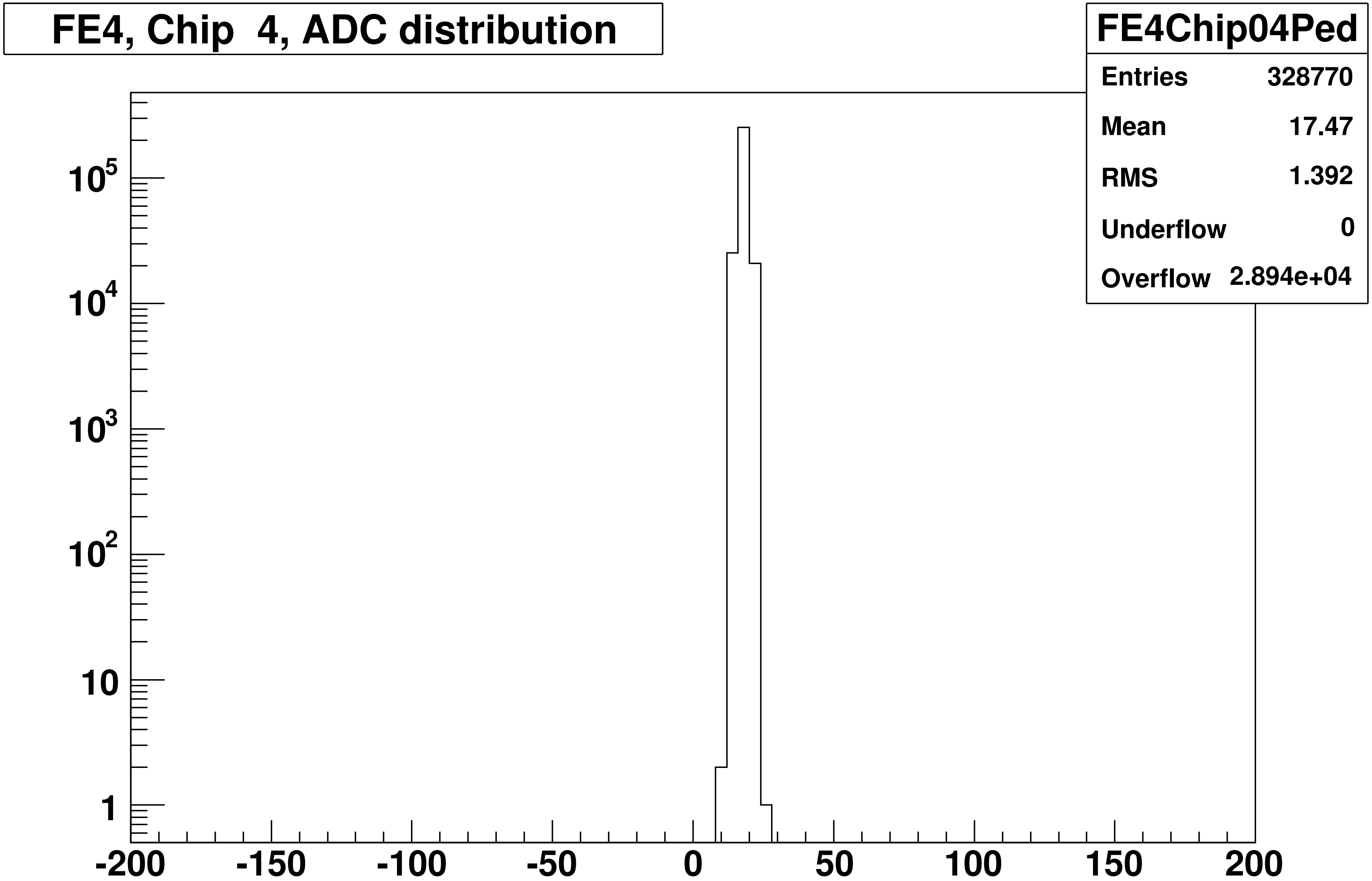
25000



FE4, Chip 4, ADC distribution
FE4Chip04Ped
Entries 328770
Mean 17.47
RMS 1.392
Underflow 0
Overflow 2.894e+04
10^5
10^4
10^3
10^2
10
1
-200
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-100
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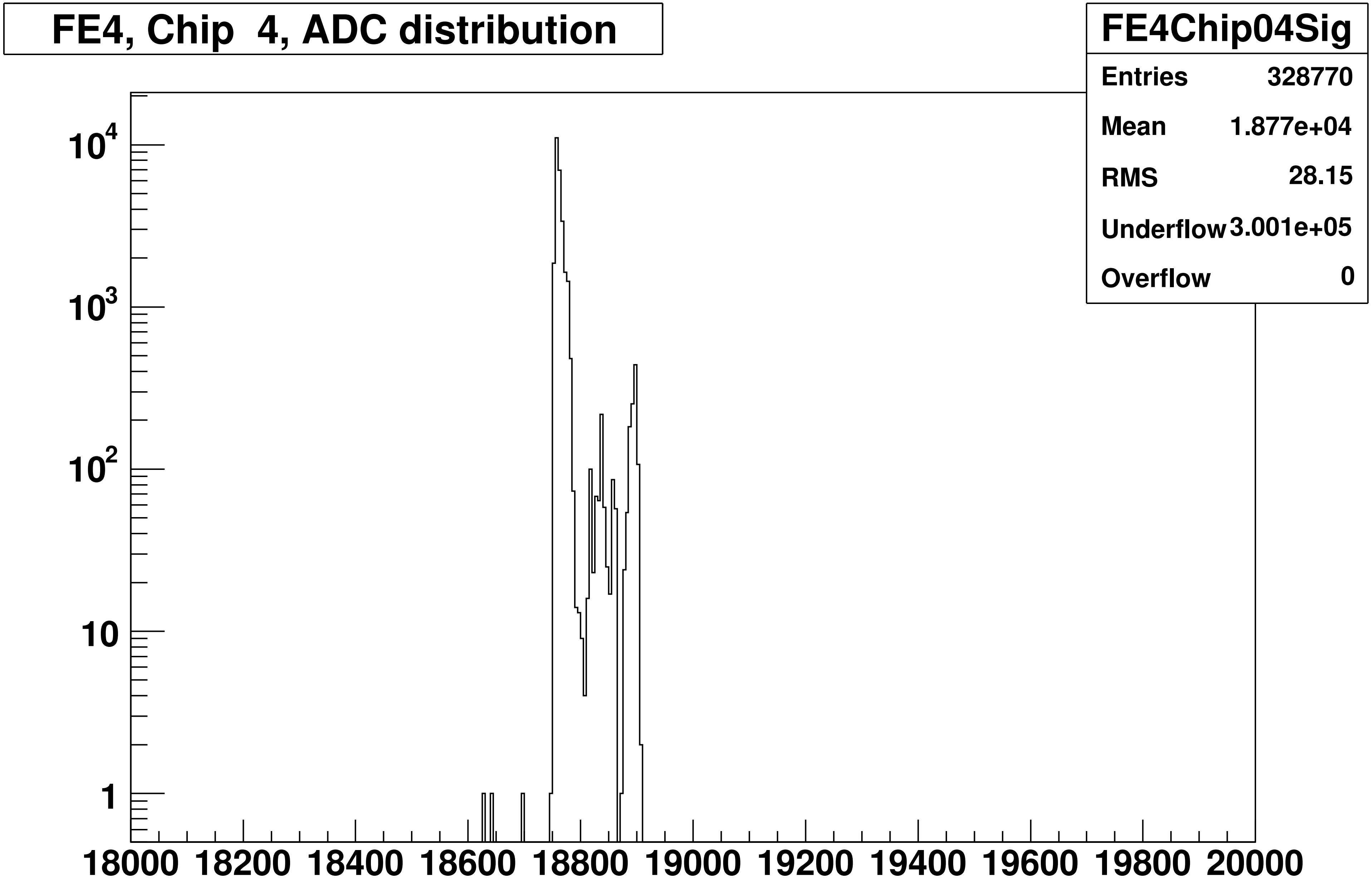
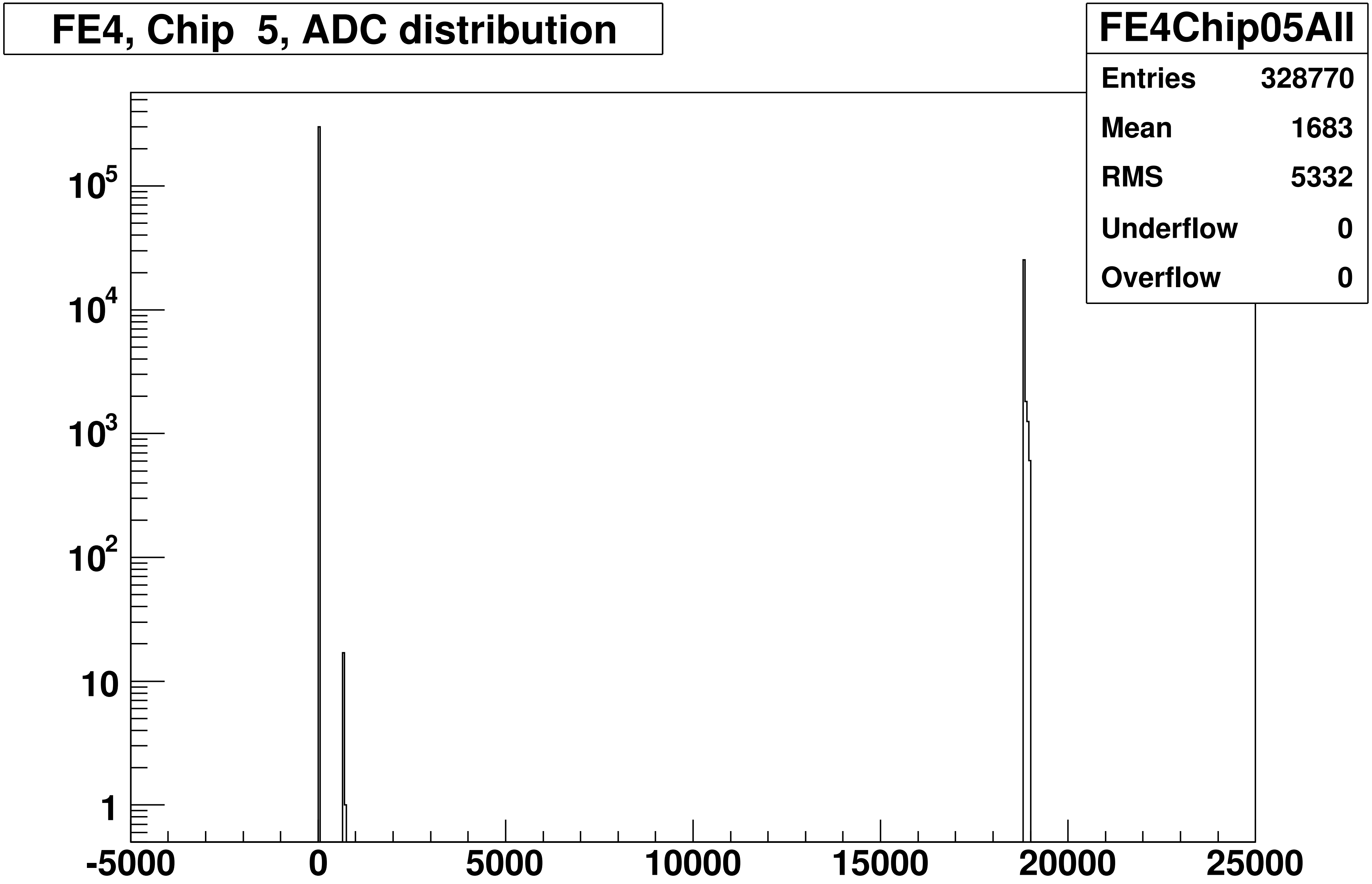
0
50
100
150
200



FE4, Chip 4, ADC distribution
FE4Chip04Sig
Entries 328770
Mean 1.877e+04
RMS 28.15
Underflow 3.001e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE4, Chip 5, ADC distribution
FE4Chip05All
Entries 328770
Mean 1683
RMS 5332
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
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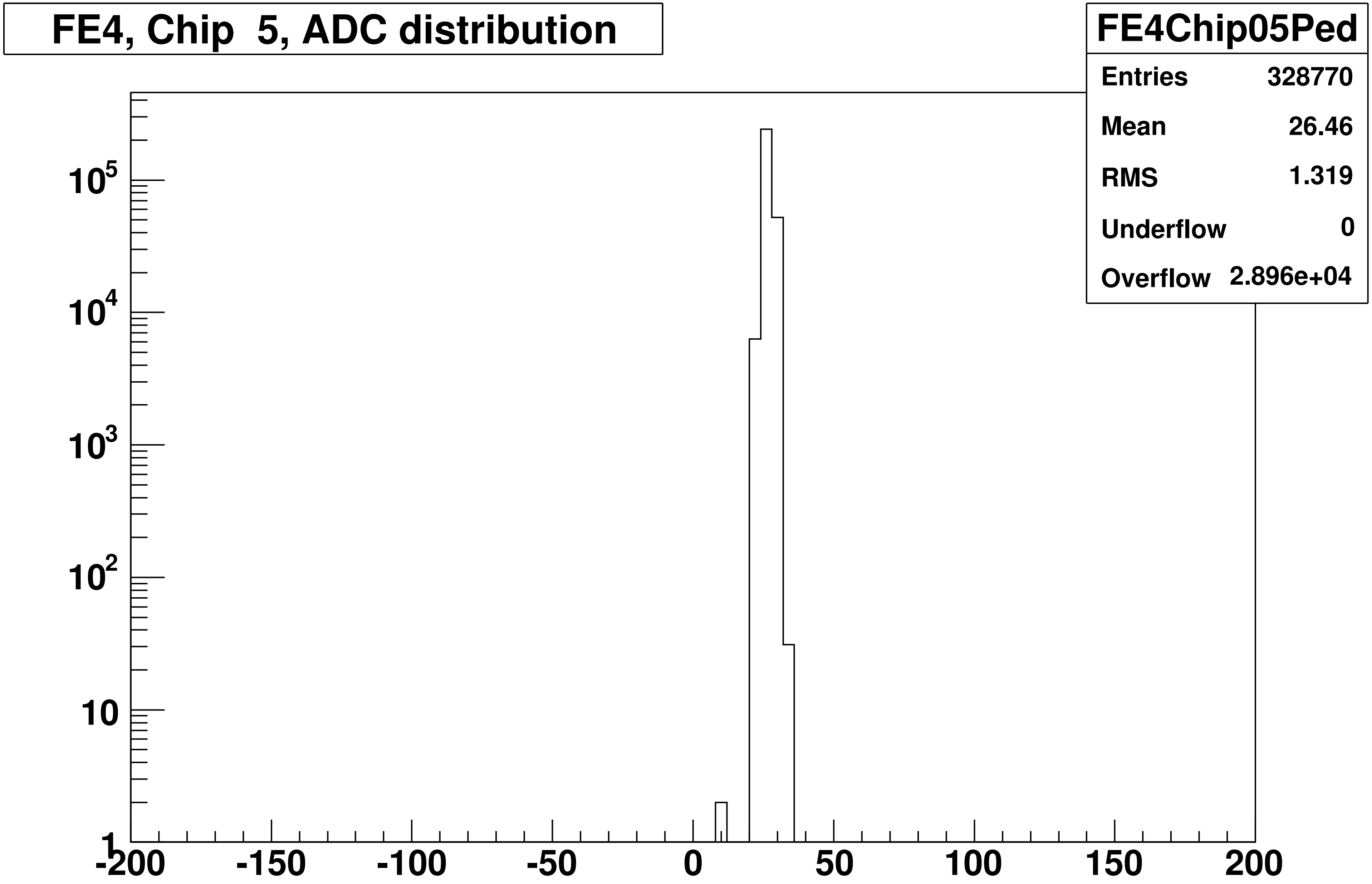
FE4, Chip 5, ADC distribution
FE4Chip05Ped
Entries 328770
Mean 26.46
RMS 1.319
Underflow 0
Overflow 2.896e+04
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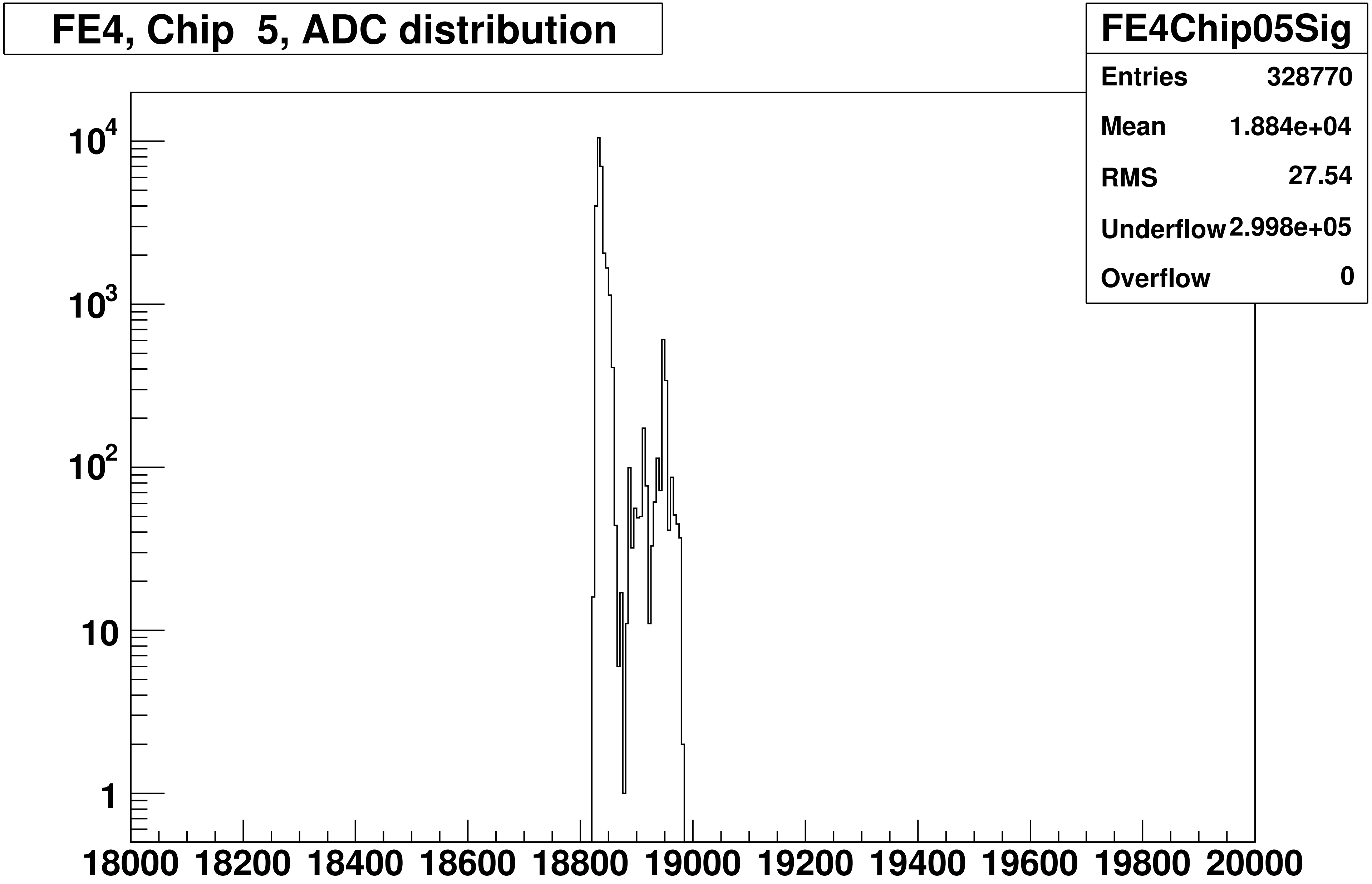
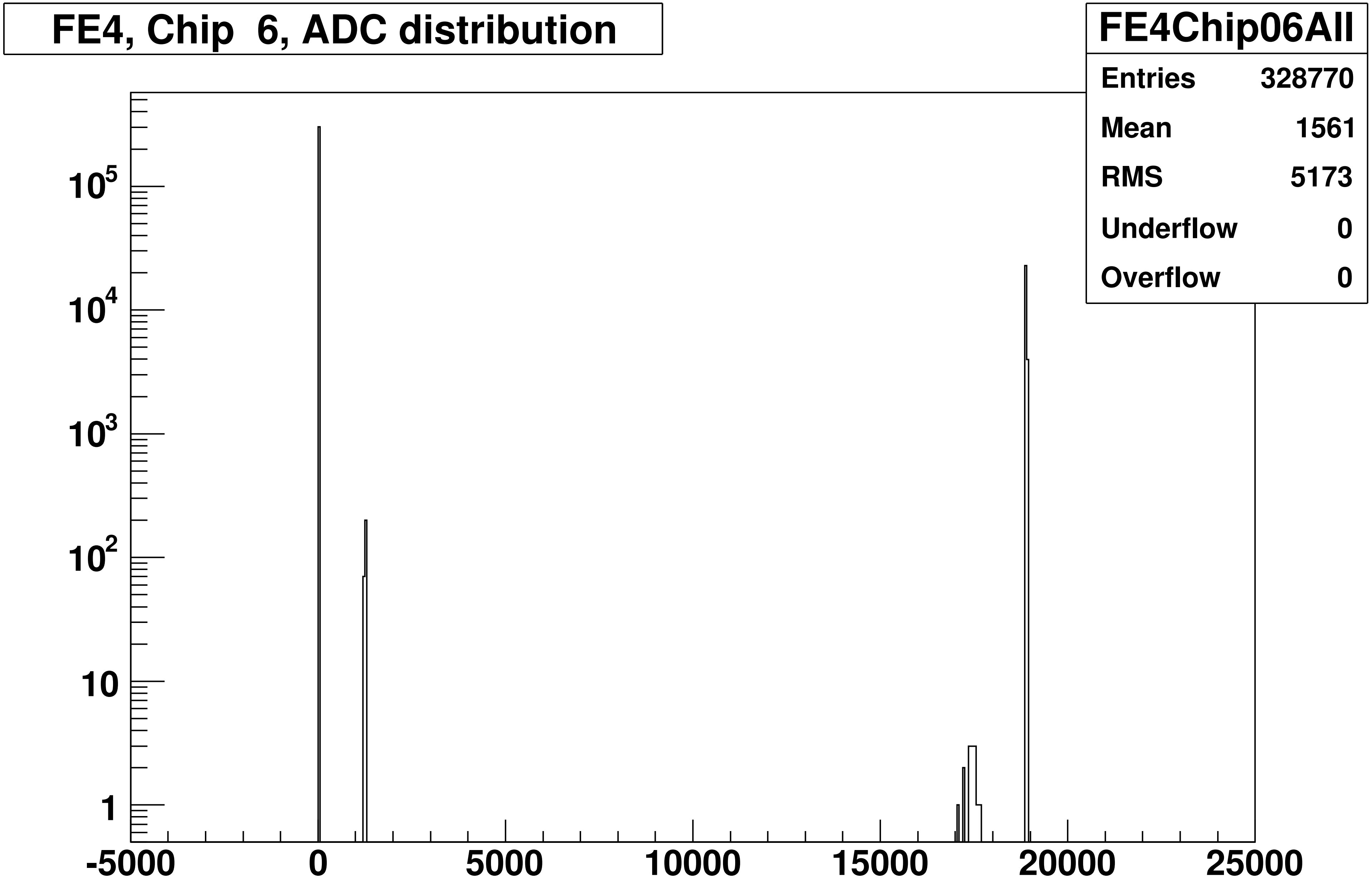

FE4, Chip 5, ADC distribution
FE4Chip05Sig
Entries 328770
Mean 1.884e+04
RMS 27.54
Underflow 2.998e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE4, Chip 6, ADC distribution
FE4Chip06All
Entries 328770
Mean 1561
RMS 5173
Underflow 0
Overflow 0
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10^4
10^3
10^2
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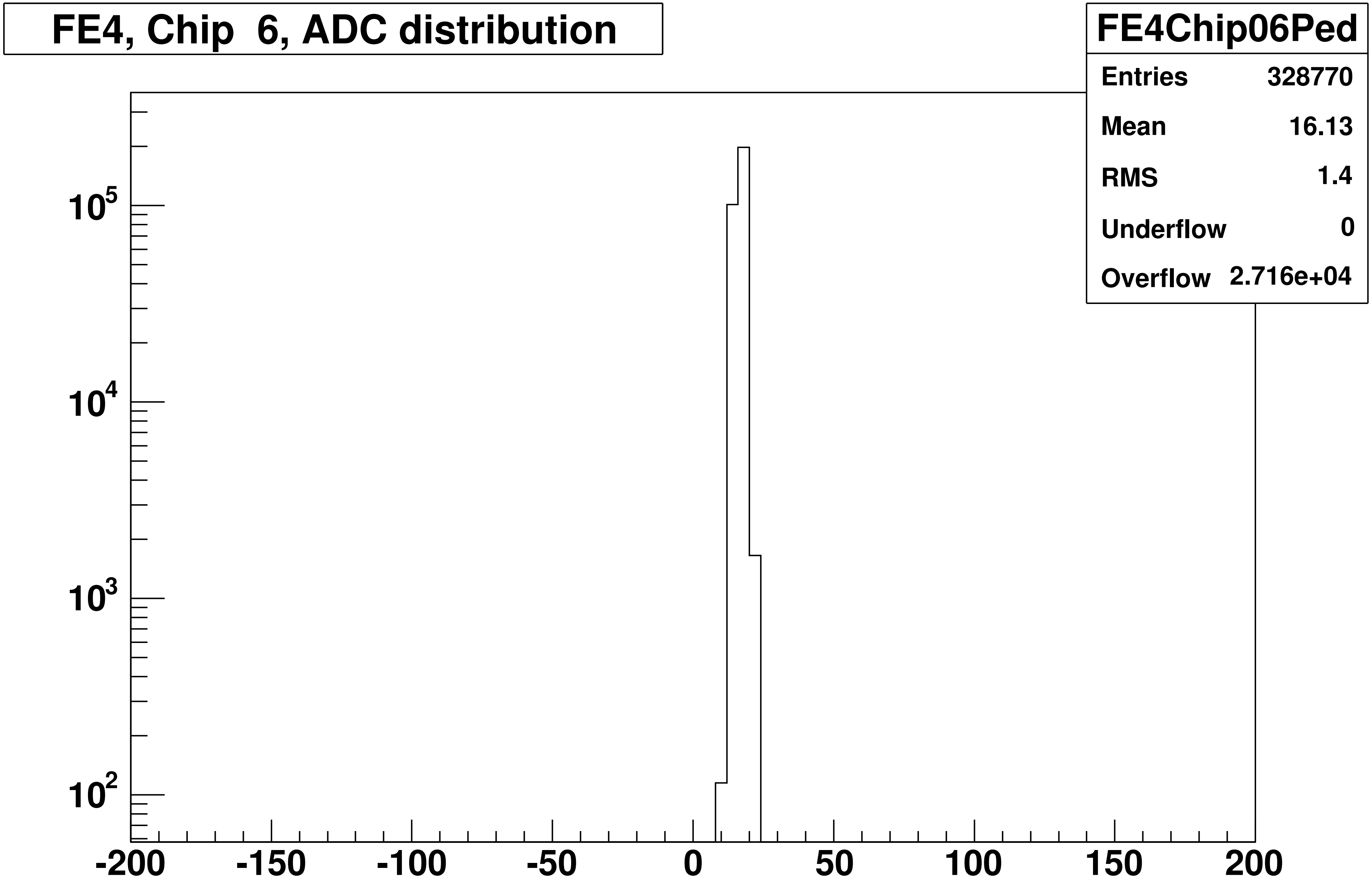

FE4, Chip 6, ADC distribution
FE4Chip06Ped
Entries 328770
Mean 16.13
RMS 1.4
Underflow 0
Overflow 2.716e+04
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10^3
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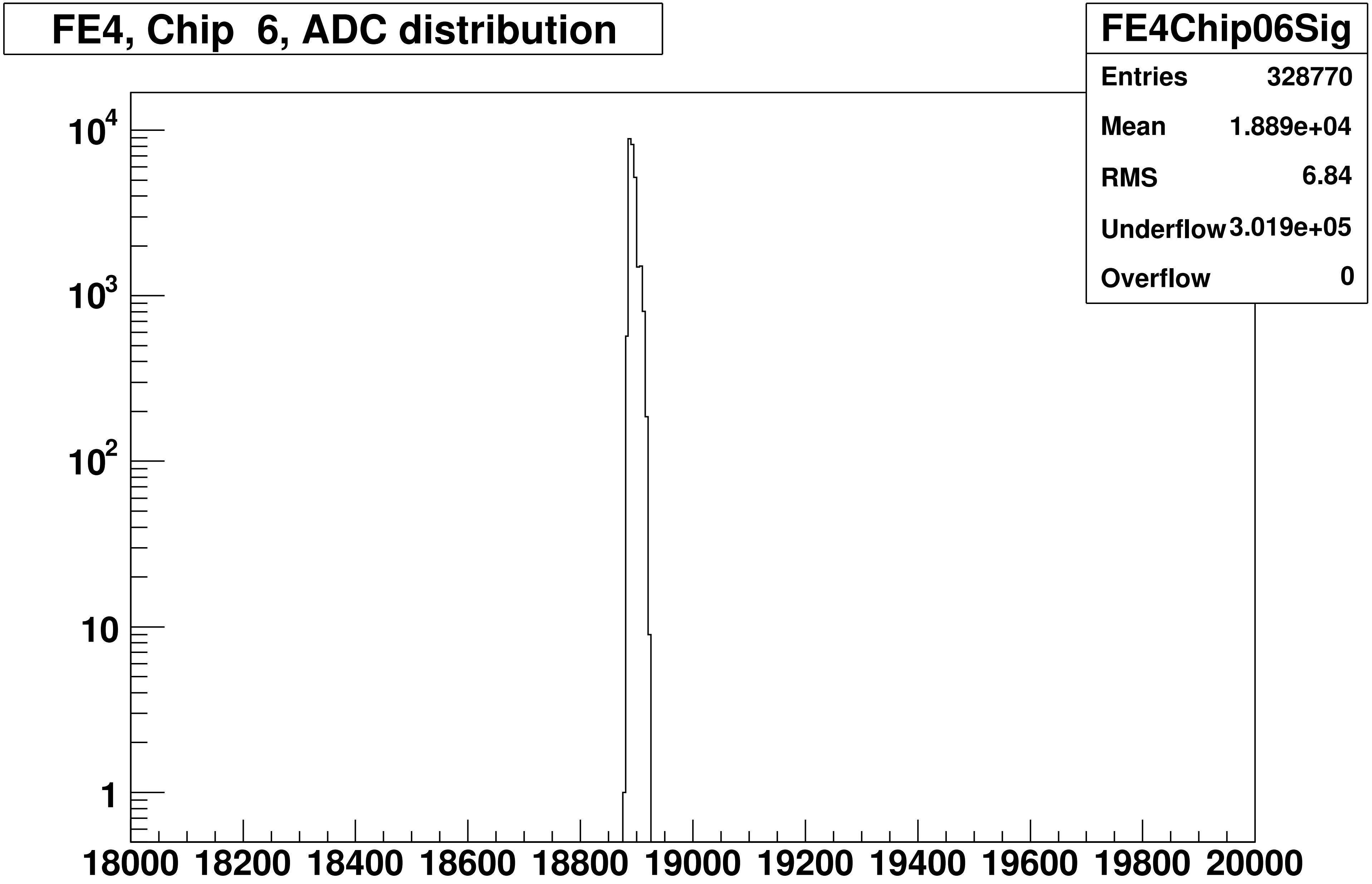
FE4, Chip 6, ADC distribution
FE4Chip06Sig
Entries 328770
Mean 1.889e+04
RMS 6.84
Underflow 3.019e+05
Overflow 0
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10^3
10^2
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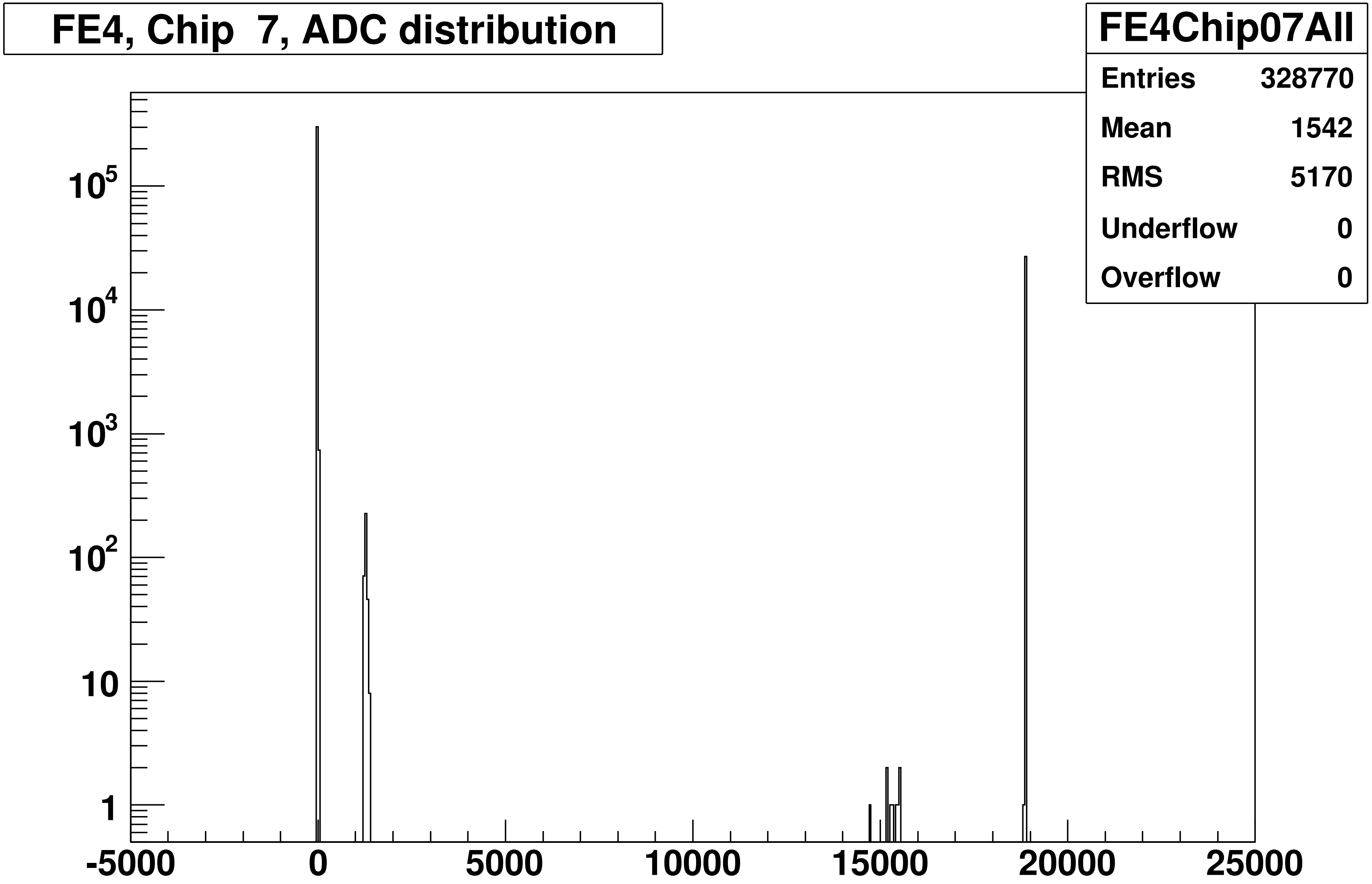
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE4, Chip 7, ADC distribution
FE4Chip07All
Entries 328770
Mean 1542
RMS 5170
Underflow 0
Overflow 0
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10^4
10^3
10^2
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10000
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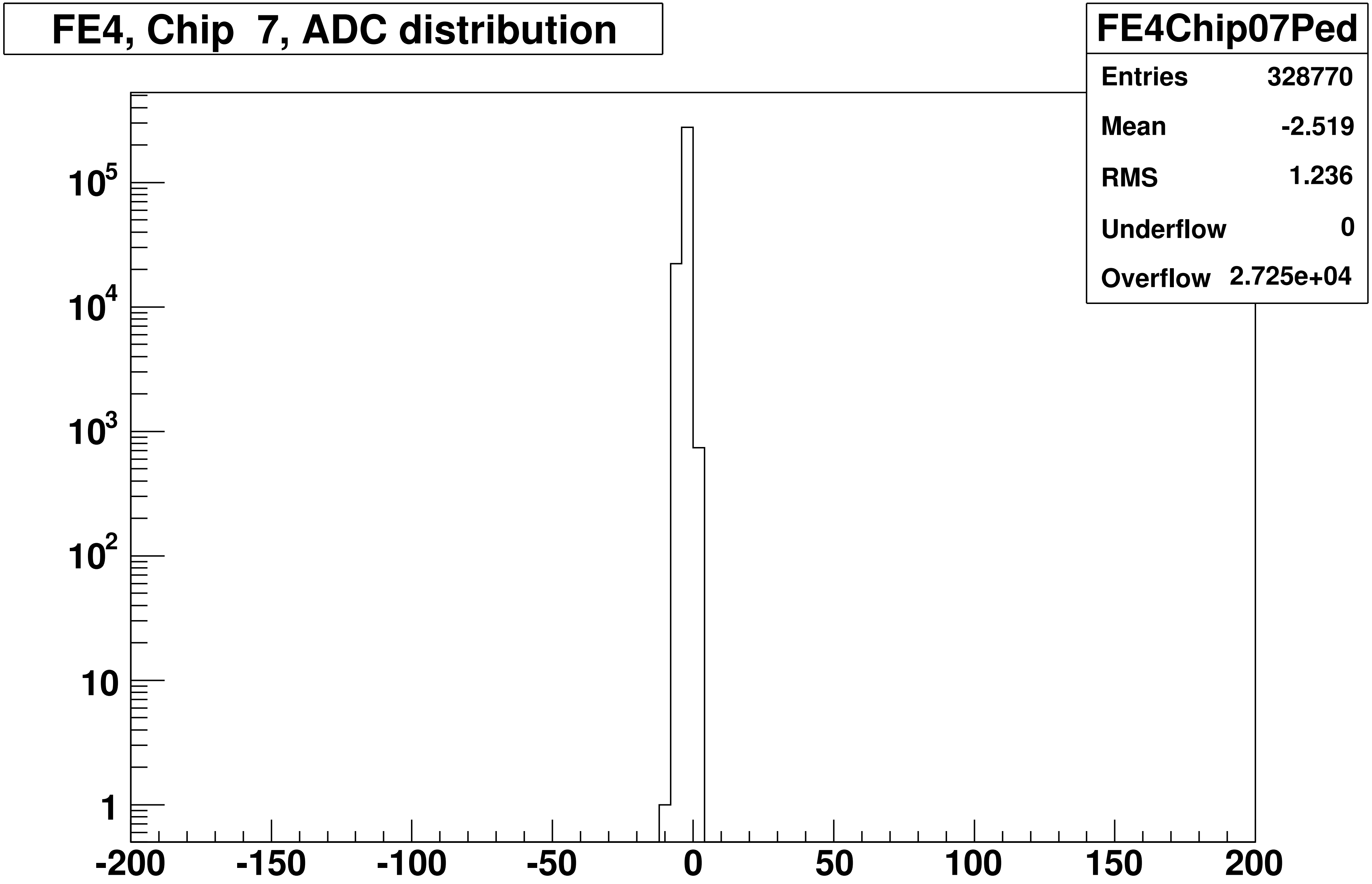
FE4, Chip 7, ADC distribution
FE4Chip07Ped
Entries 328770
Mean -2.519
RMS 1.236
Underflow 0
Overflow 2.725e+04
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10^2
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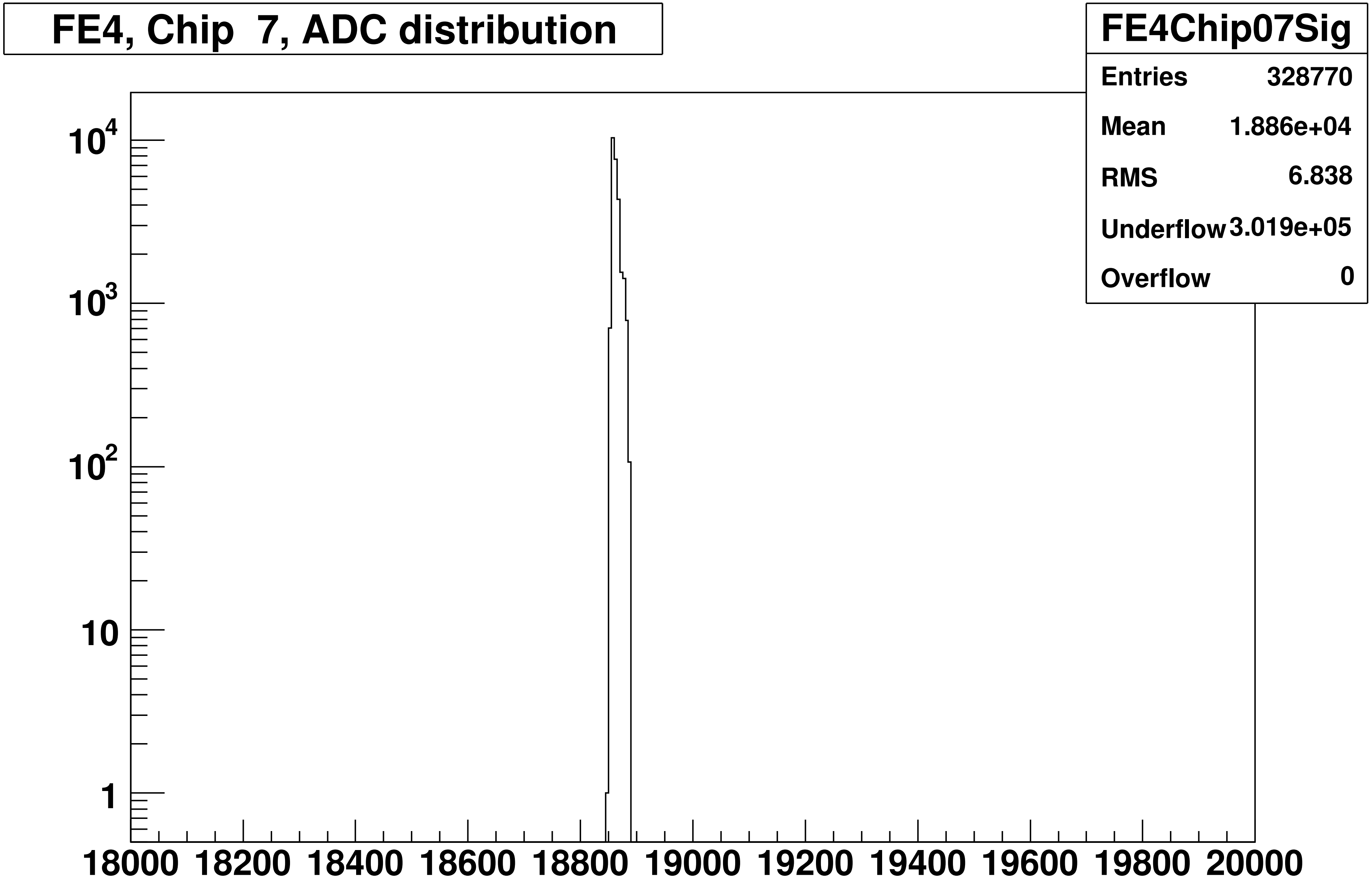
FE4, Chip 7, ADC distribution
FE4Chip07Sig
Entries 328770
Mean 1.886e+04
RMS 6.838
Underflow 3.019e+05
Overflow 0
10^4
10^3
10^2
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18200
18400
18600
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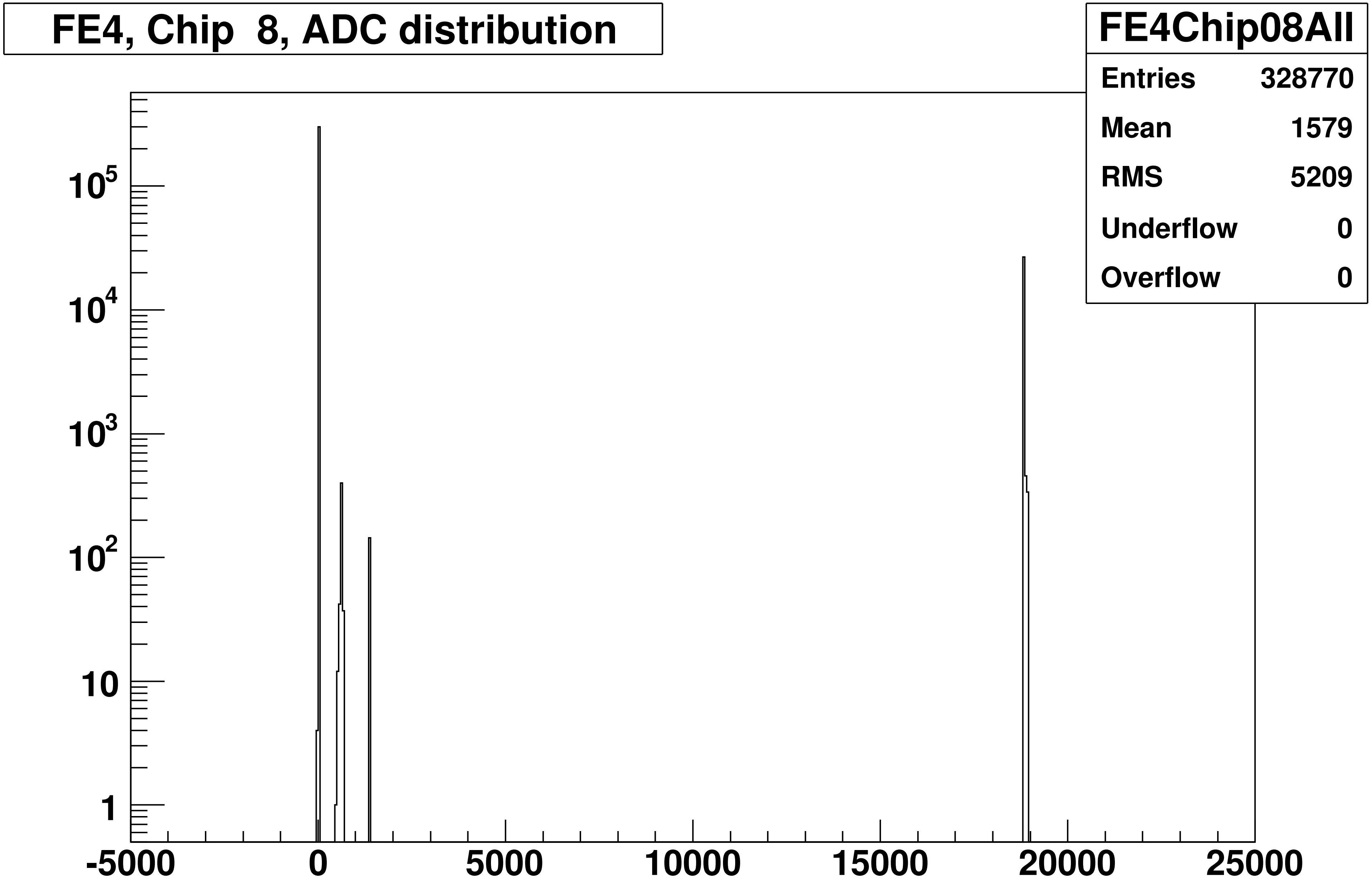
FE4, Chip 8, ADC distribution
FE4Chip08All
Entries 328770
Mean 1579
RMS 5209
Underflow 0
Overflow 0
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10^4
10^3
10^2
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1
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0
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10000
15000
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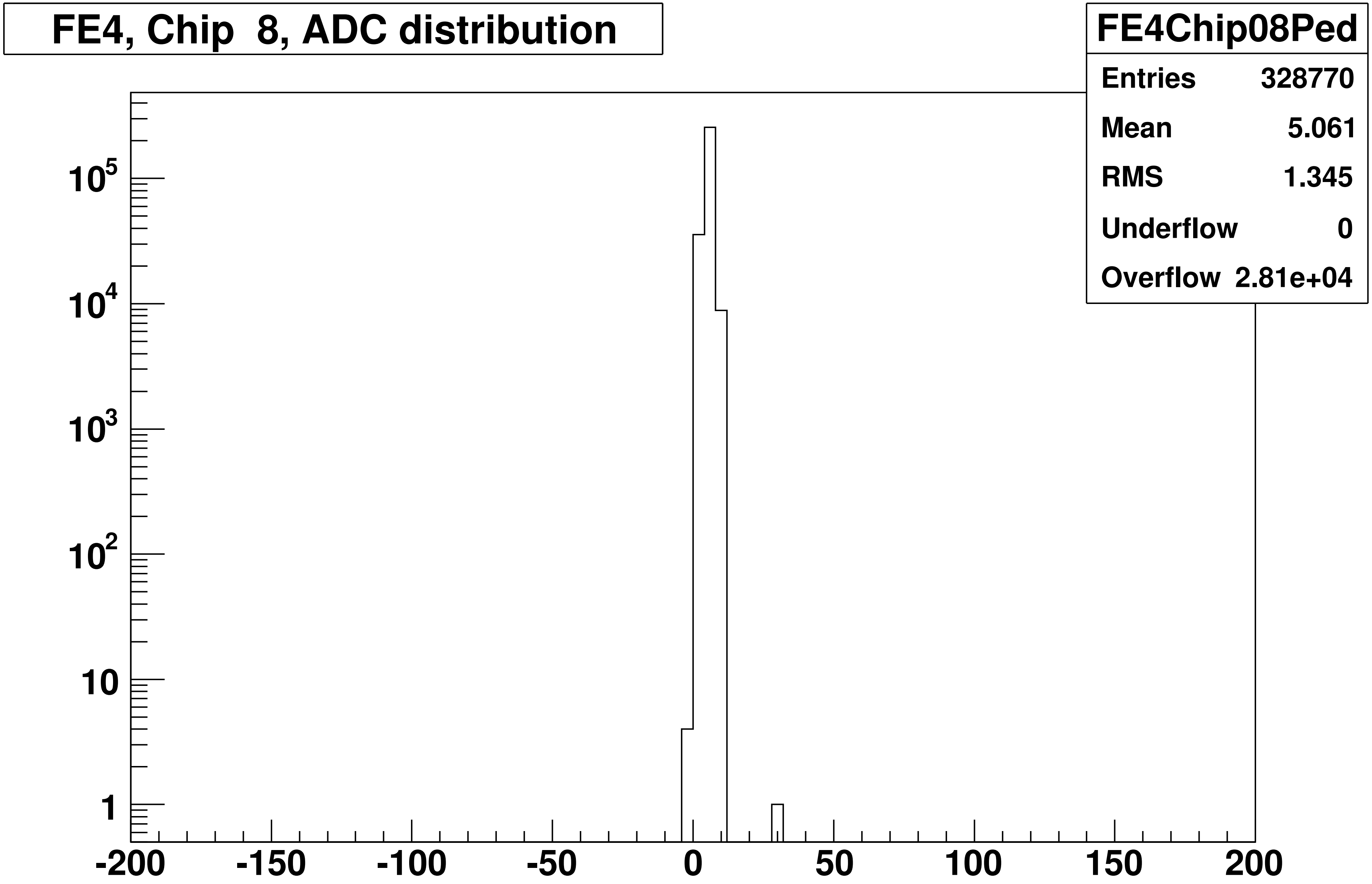
FE4, Chip 8, ADC distribution
FE4Chip08Ped
Entries 328770
Mean 5.061
RMS 1.345
Underflow 0
Overflow 2.81e+04
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10^4
10^3
10^2
10
1
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150
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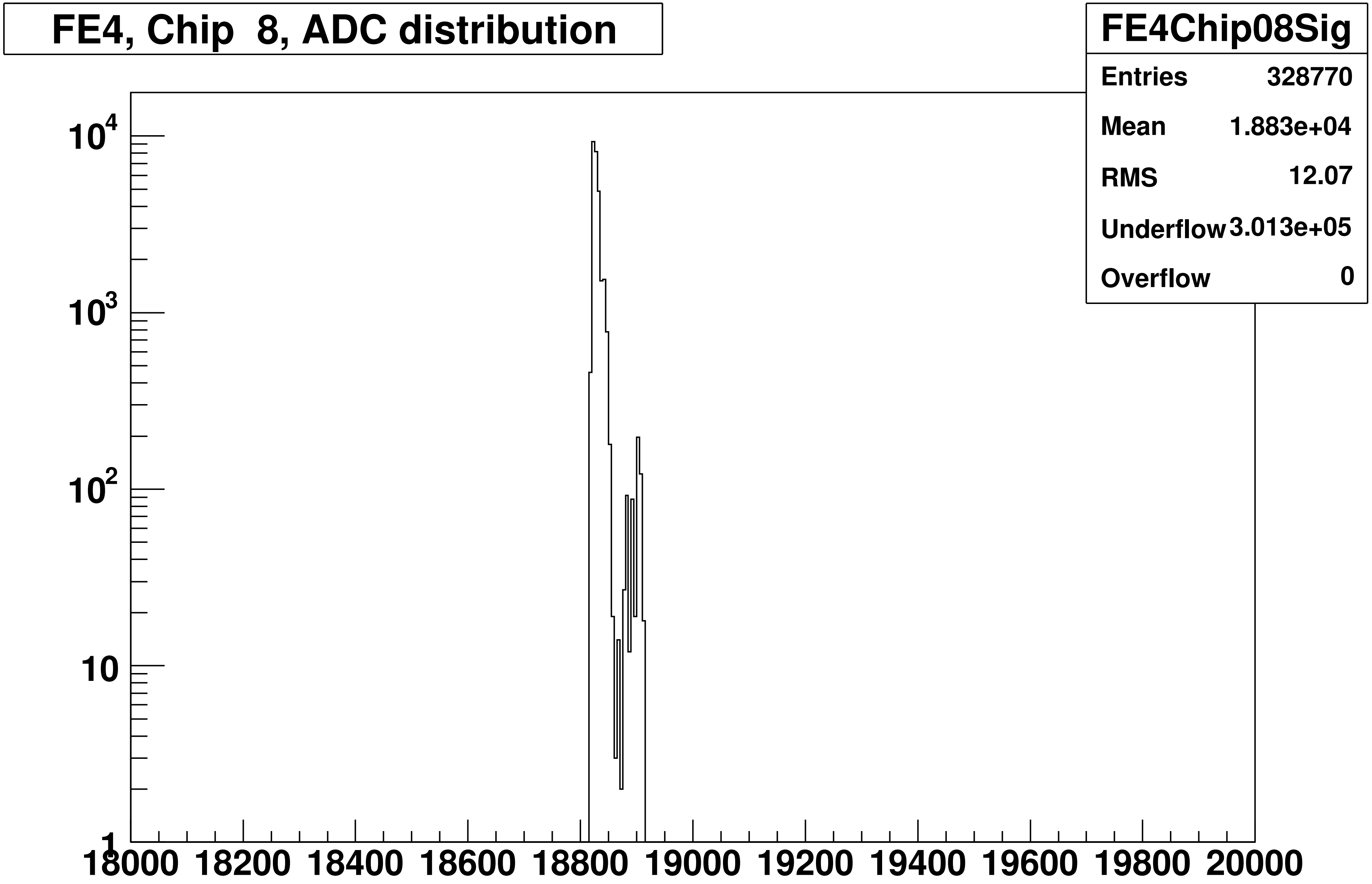

FE4, Chip 8, ADC distribution
FE4Chip08Sig
Entries 328770
Mean 1.883e+04
RMS 12.07
Underflow 3.013e+05
Overflow 0
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10^3
10^2
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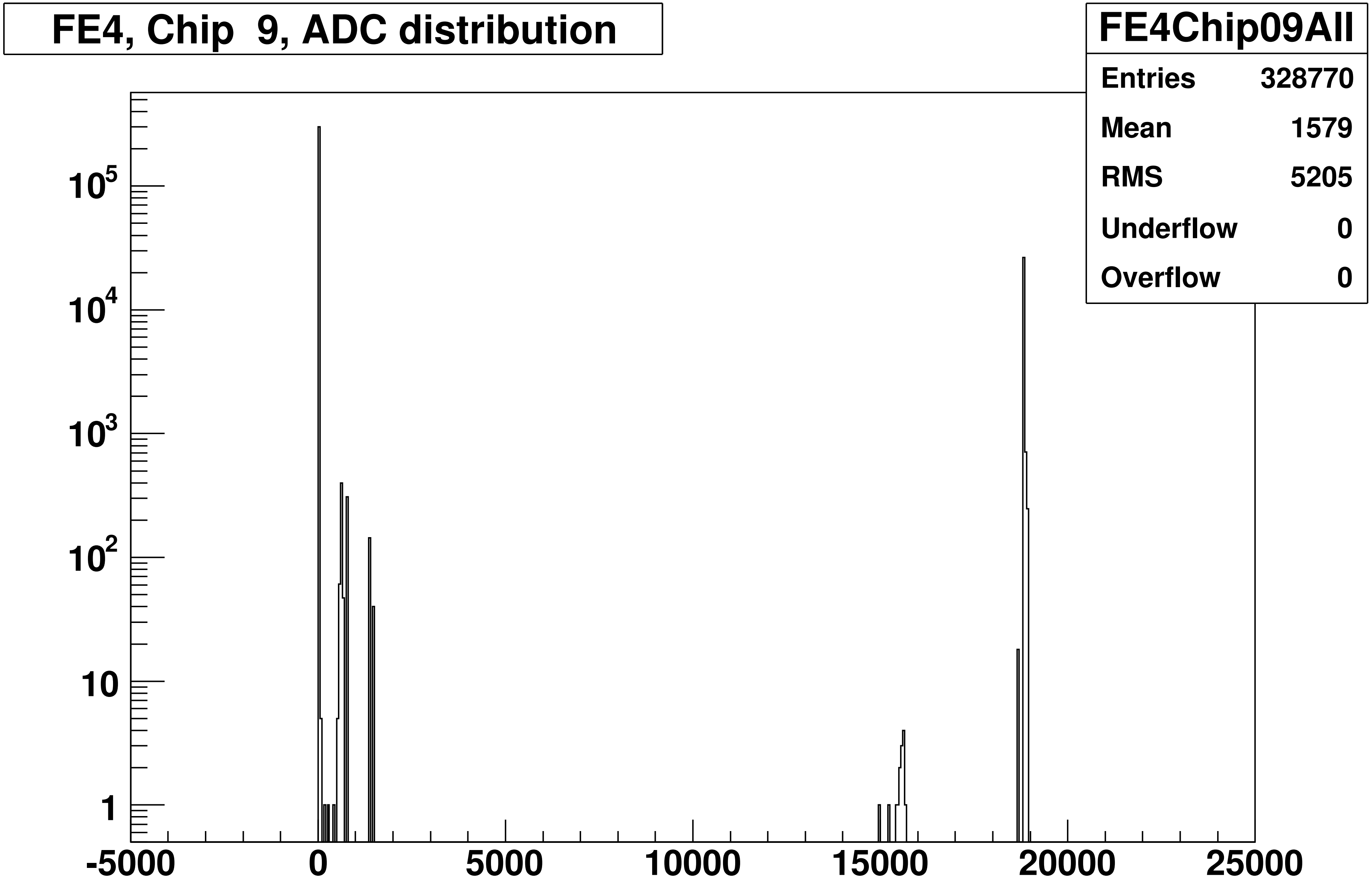
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE4, Chip 9, ADC distribution
FE4Chip09All
Entries 328770
Mean 1579
RMS 5205
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
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-5000
0
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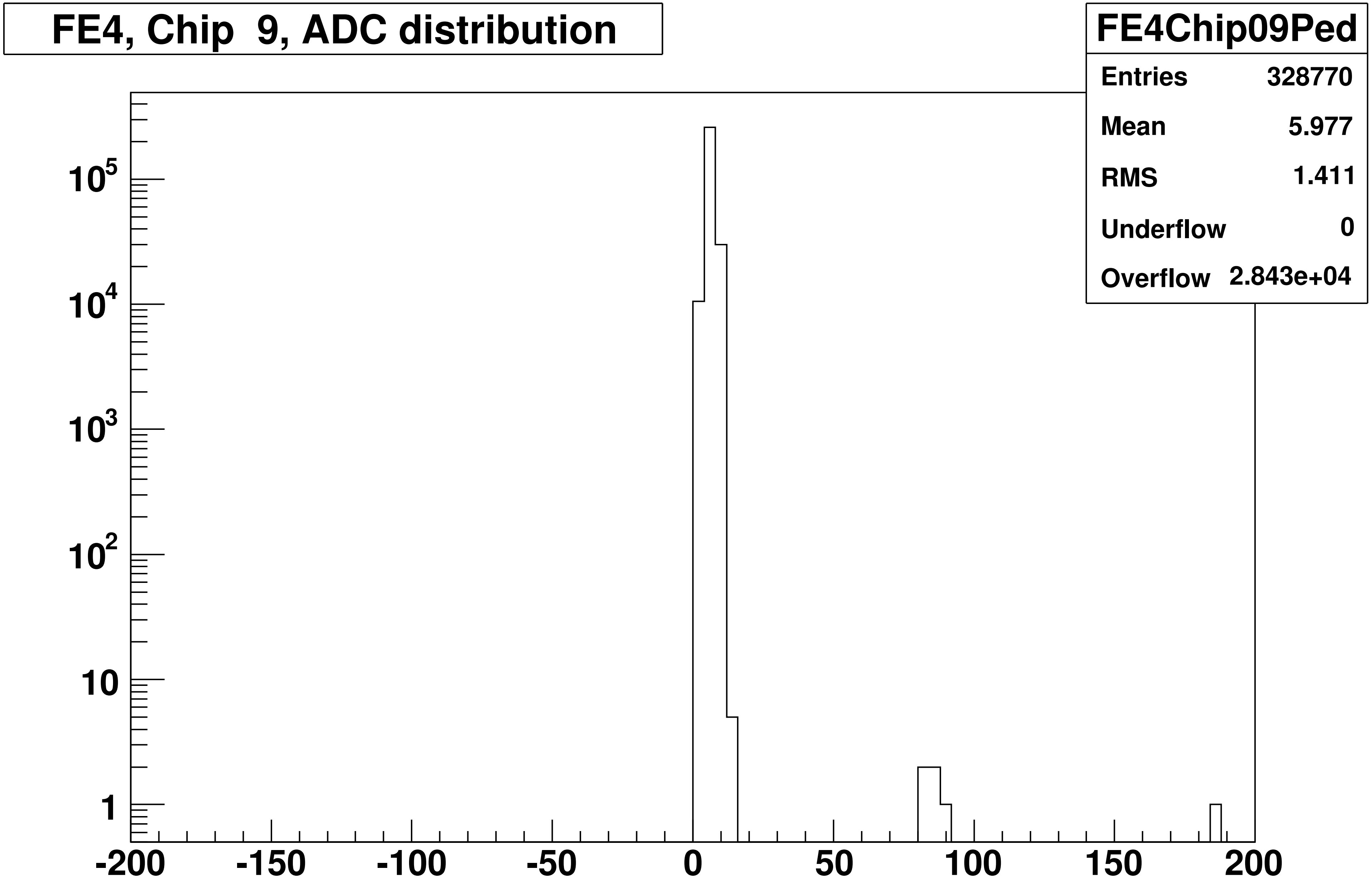
FE4, Chip 9, ADC distribution
FE4Chip09Ped
Entries 328770
Mean 5.977
RMS 1.411
Underflow 0
Overflow 2.843e+04
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10^4
10^3
10^2
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100
150
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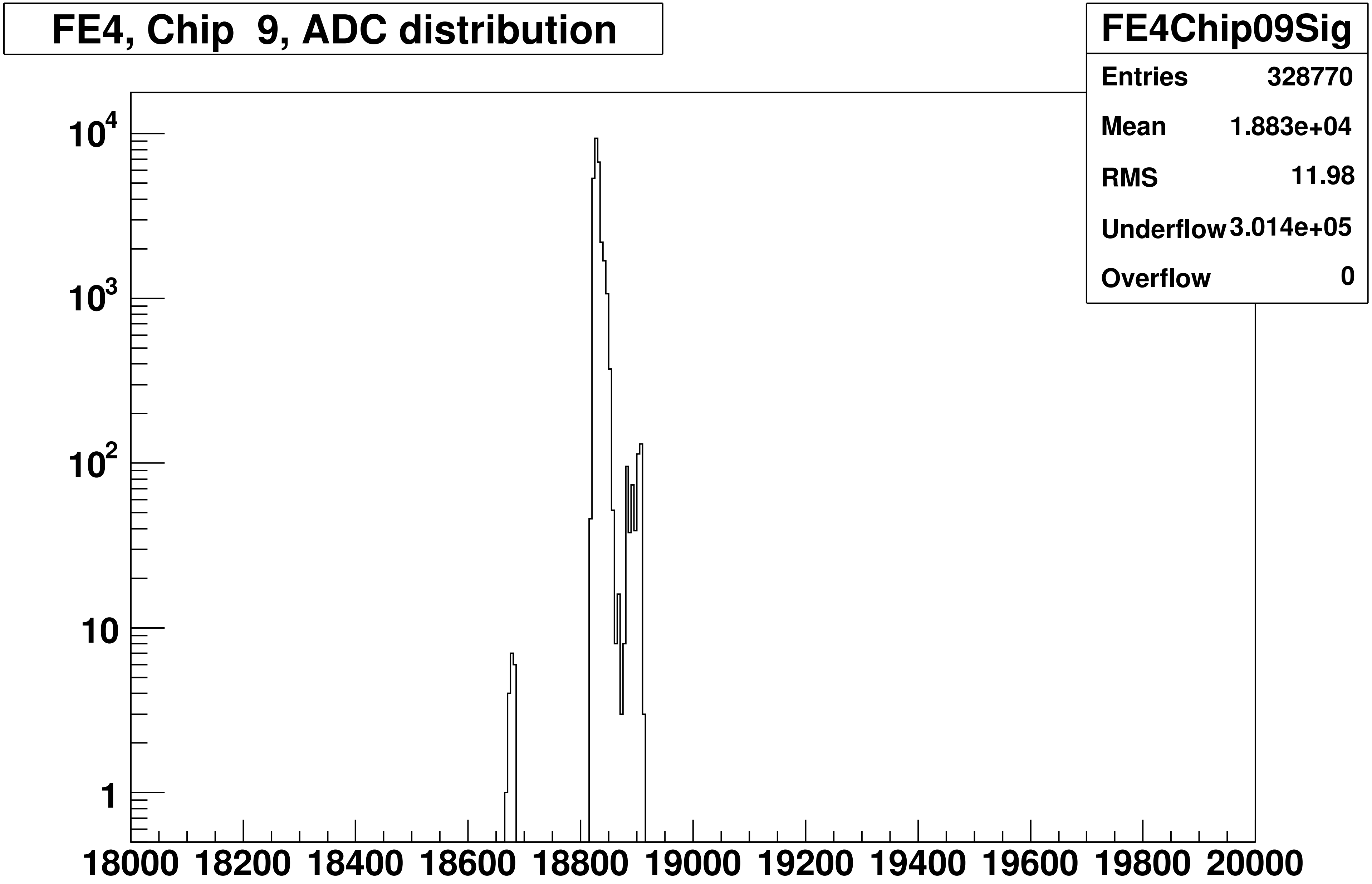
FE4, Chip 9, ADC distribution
FE4Chip09Sig
Entries 328770
Mean 1.883e+04
RMS 11.98
Underflow 3.014e+05
Overflow 0
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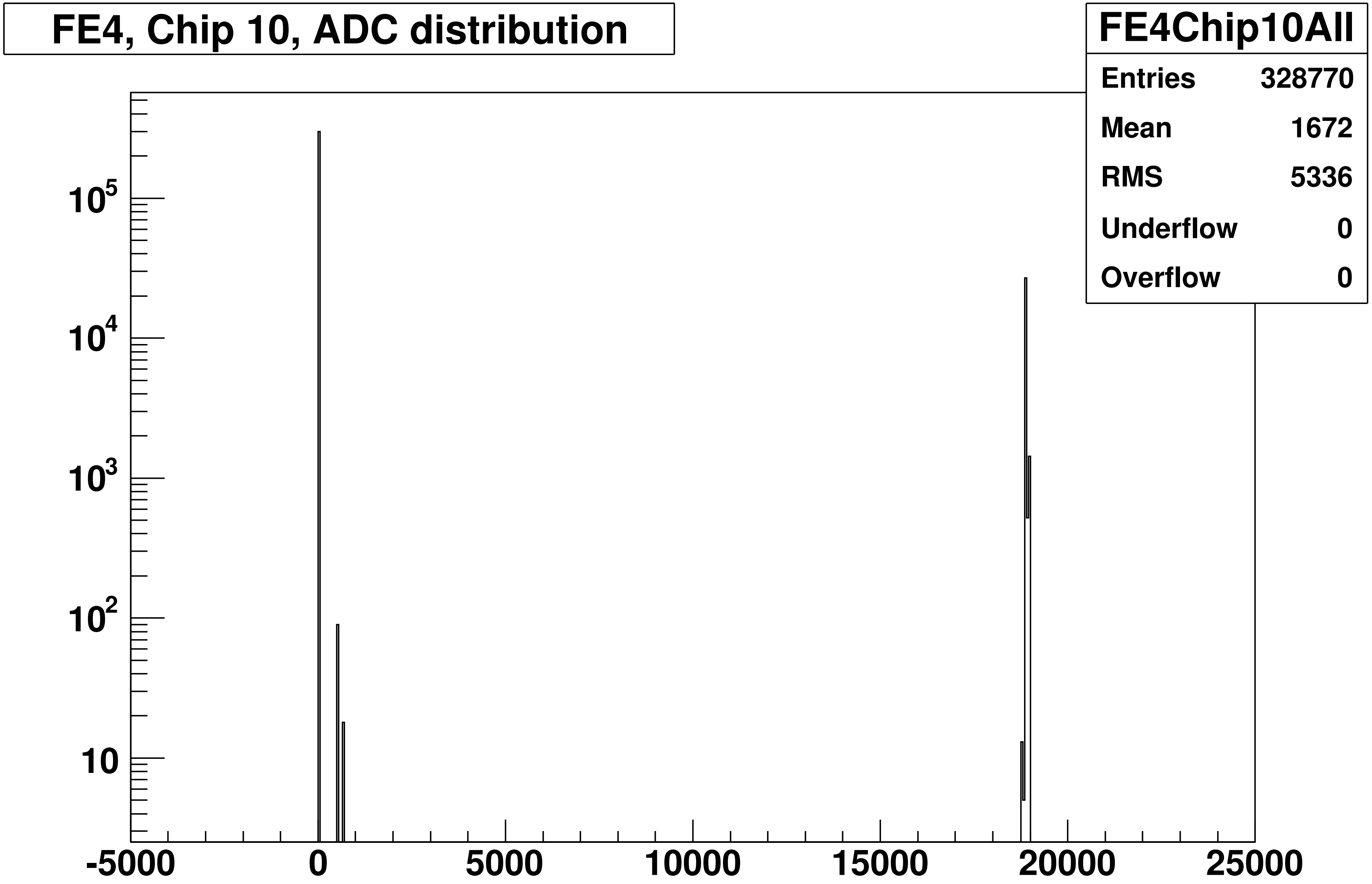
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE4, Chip 10, ADC distribution
FE4Chip10All
Entries 328770
Mean 1672
RMS 5336
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
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5000
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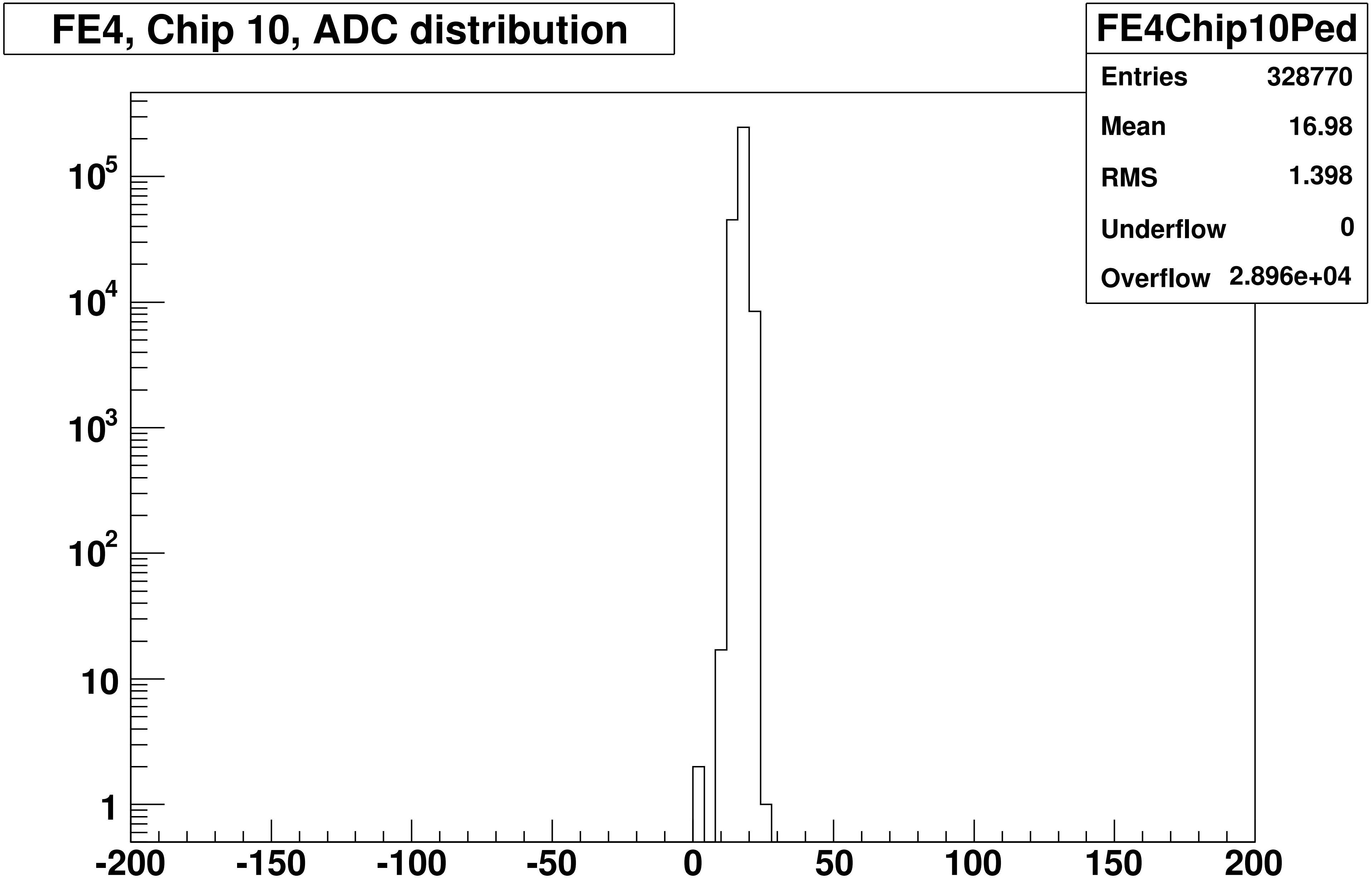
15000
20000
25000


FE4, Chip 10, ADC distribution
FE4Chip10Ped
Entries 328770
Mean 16.98
RMS 1.398
Underflow 0
Overflow 2.896e+04
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10^4
10^3
10^2
10
1
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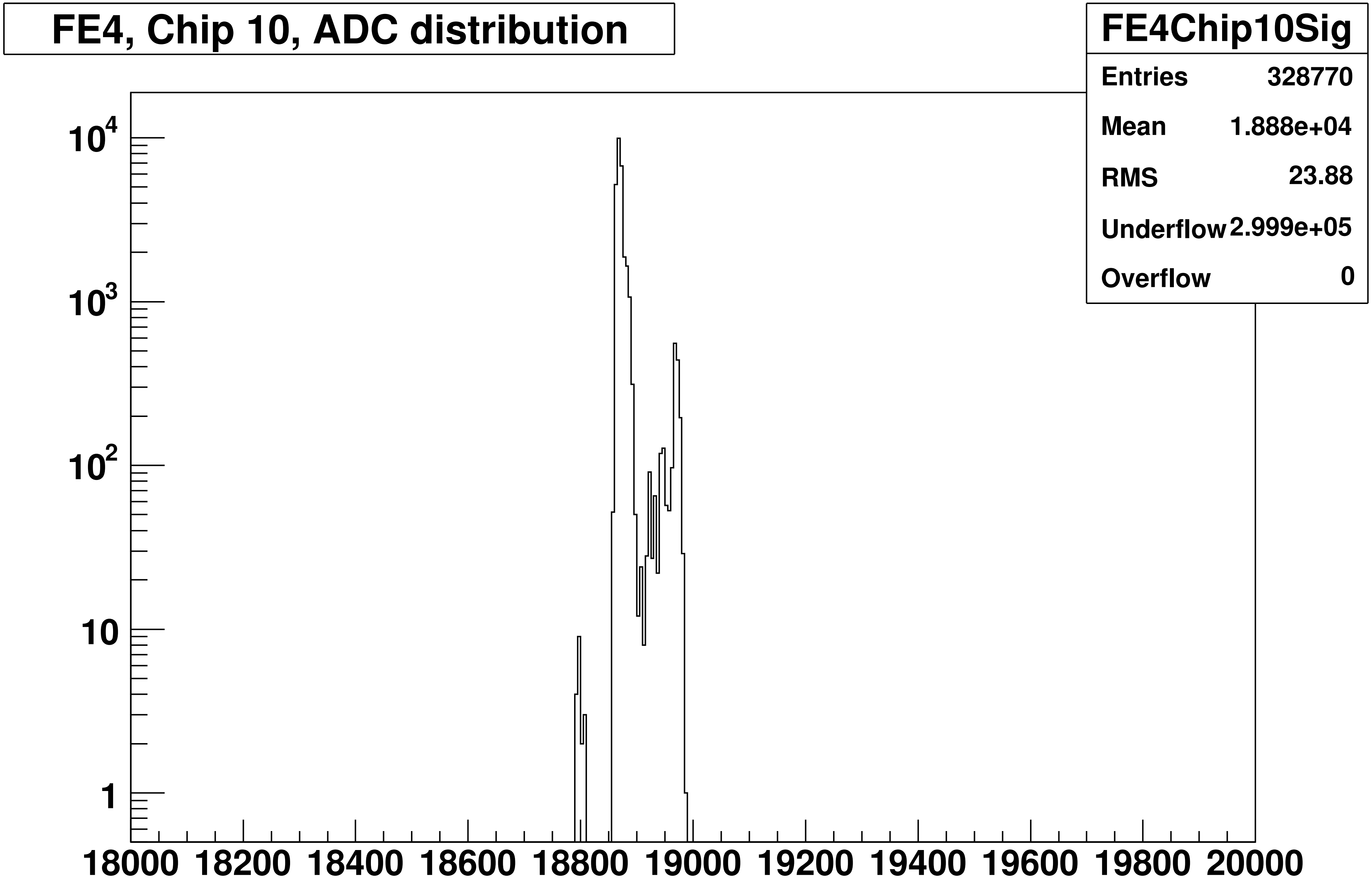
FE4, Chip 10, ADC distribution
FE4Chip10Sig
Entries 328770
Mean 1.888e+04
RMS 23.88
Underflow 2.999e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
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19000
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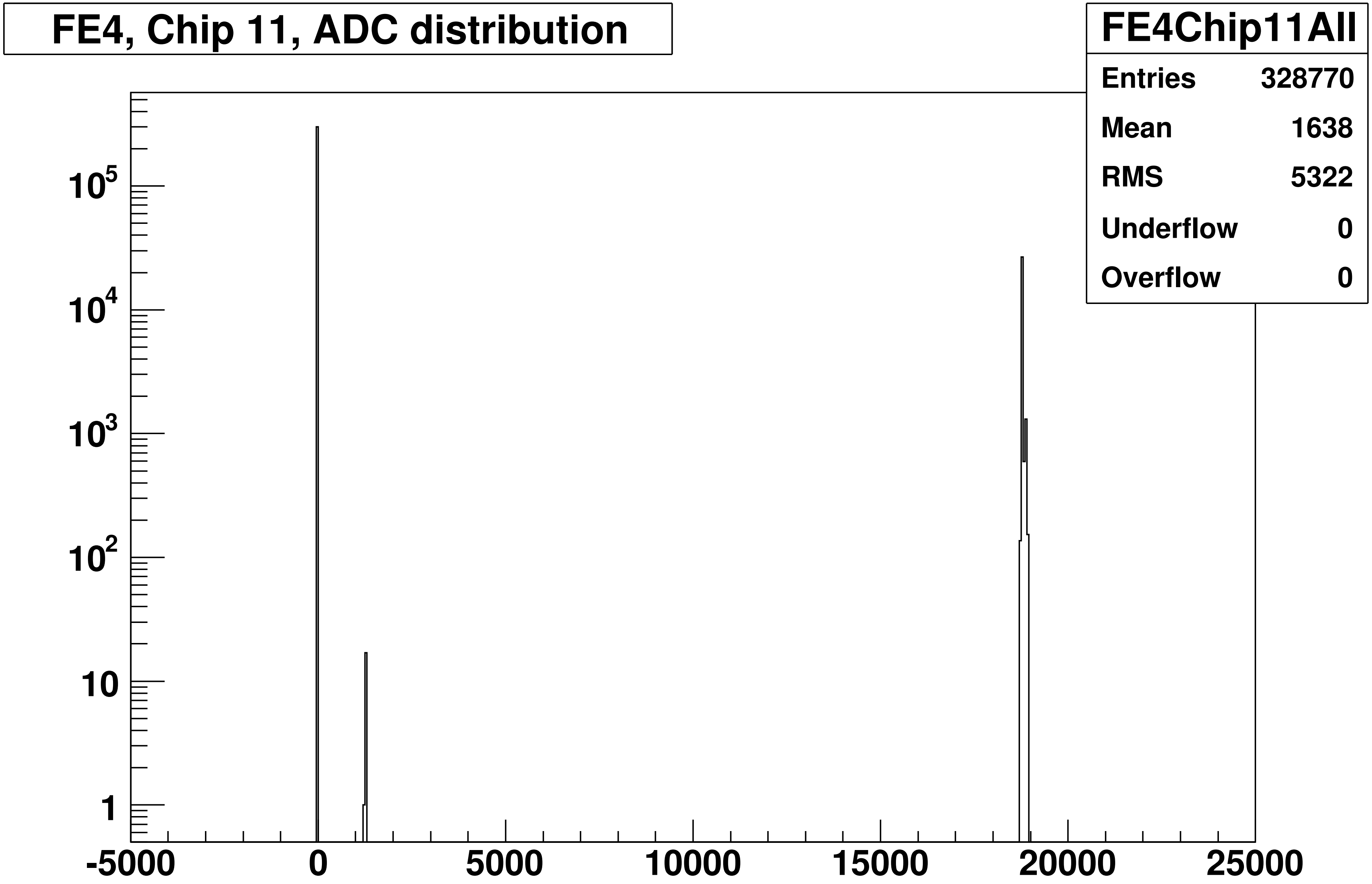
19800
20000



FE4, Chip 11, ADC distribution
FE4Chip11All
Entries 328770
Mean 1638
RMS 5322
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
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10000
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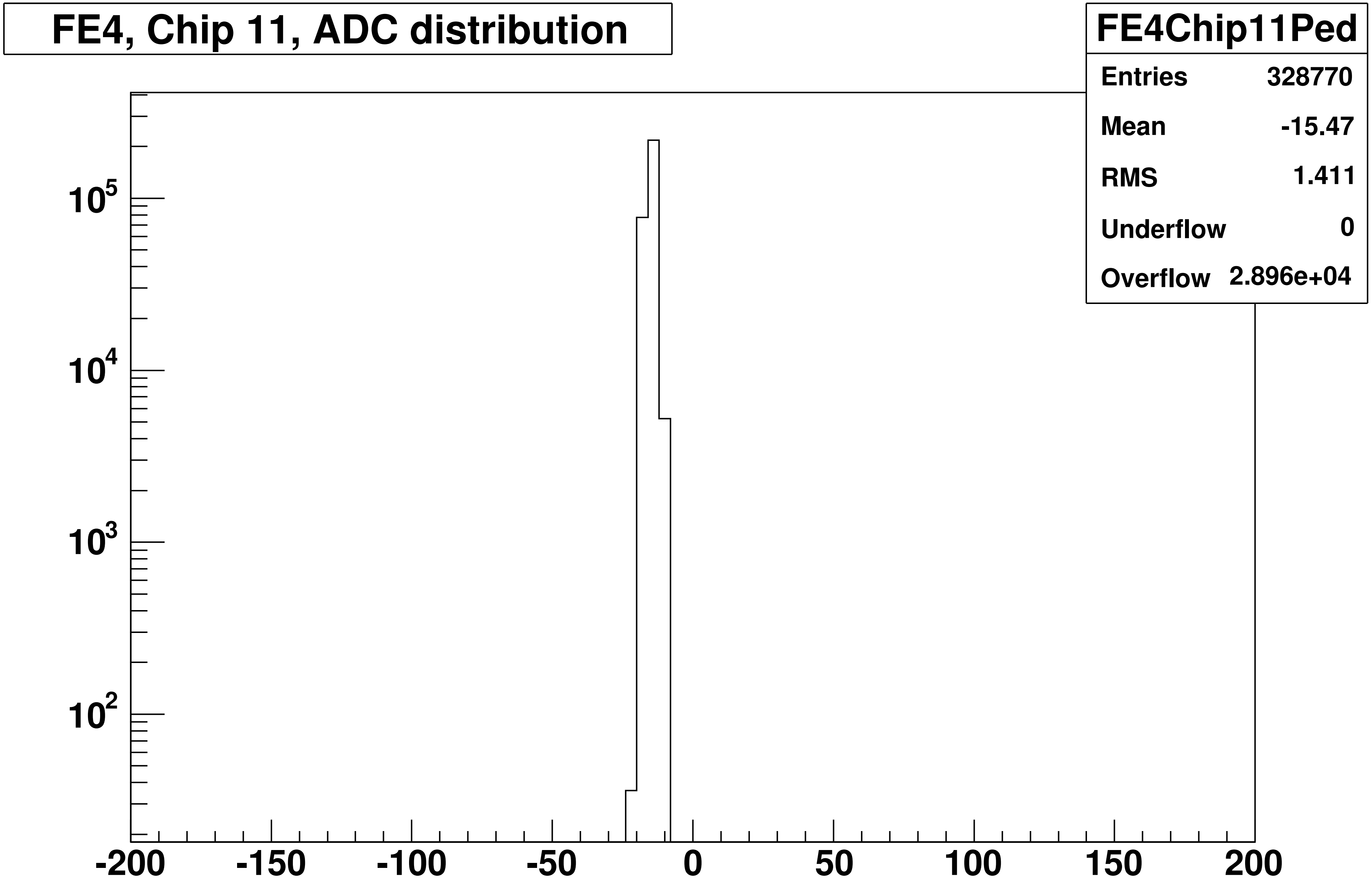
20000
25000


FE4, Chip 11, ADC distribution
FE4Chip11Ped
Entries 328770
Mean -15.47
RMS 1.411
Underflow 0
Overflow 2.896e+04
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10^4
10^3
10^2
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-100
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150
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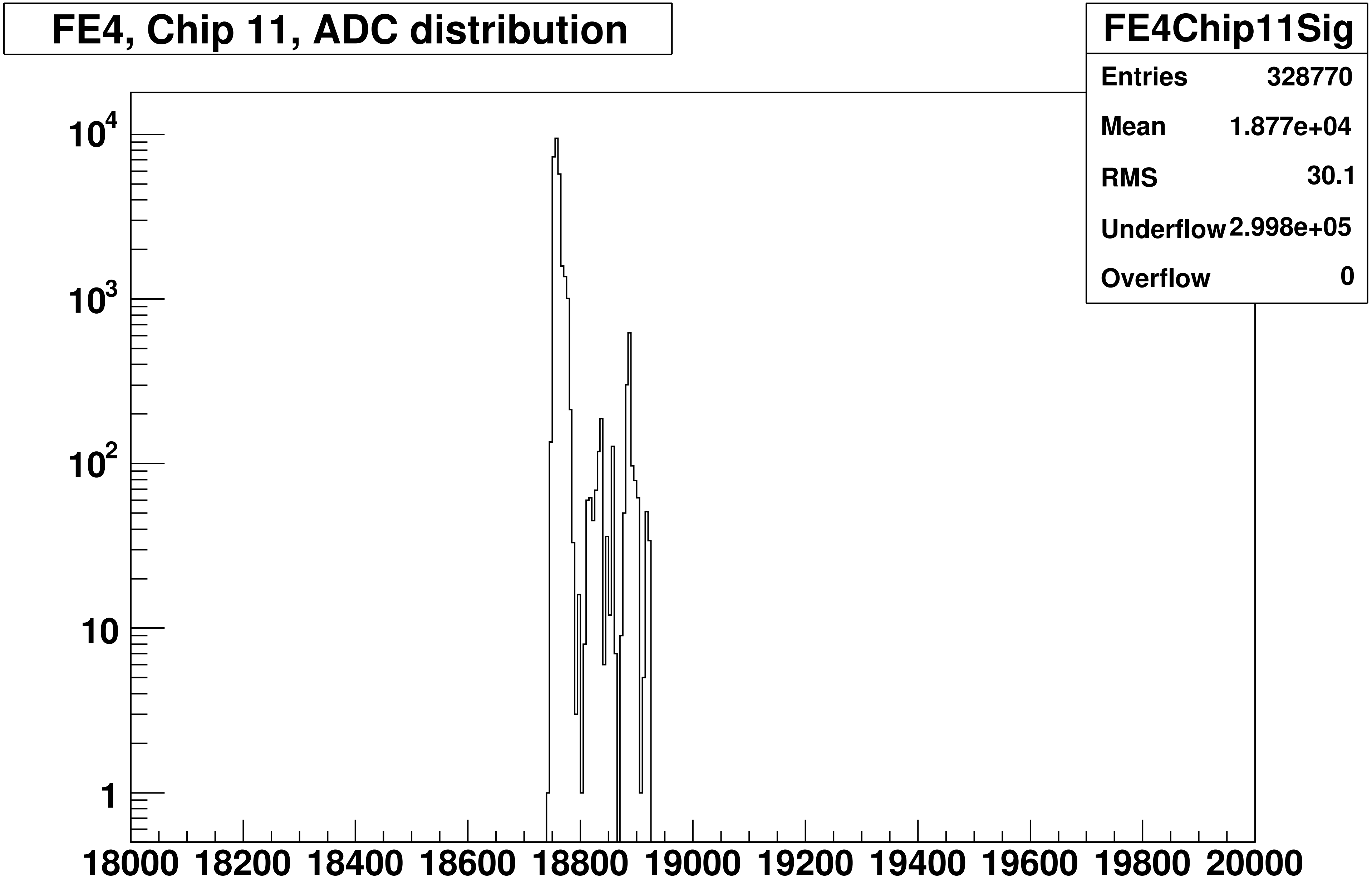
FE4, Chip 11, ADC distribution
FE4Chip11Sig
Entries 328770
Mean 1.877e+04
RMS 30.1
Underflow 2.998e+05
Overflow 0
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10^3
10^2
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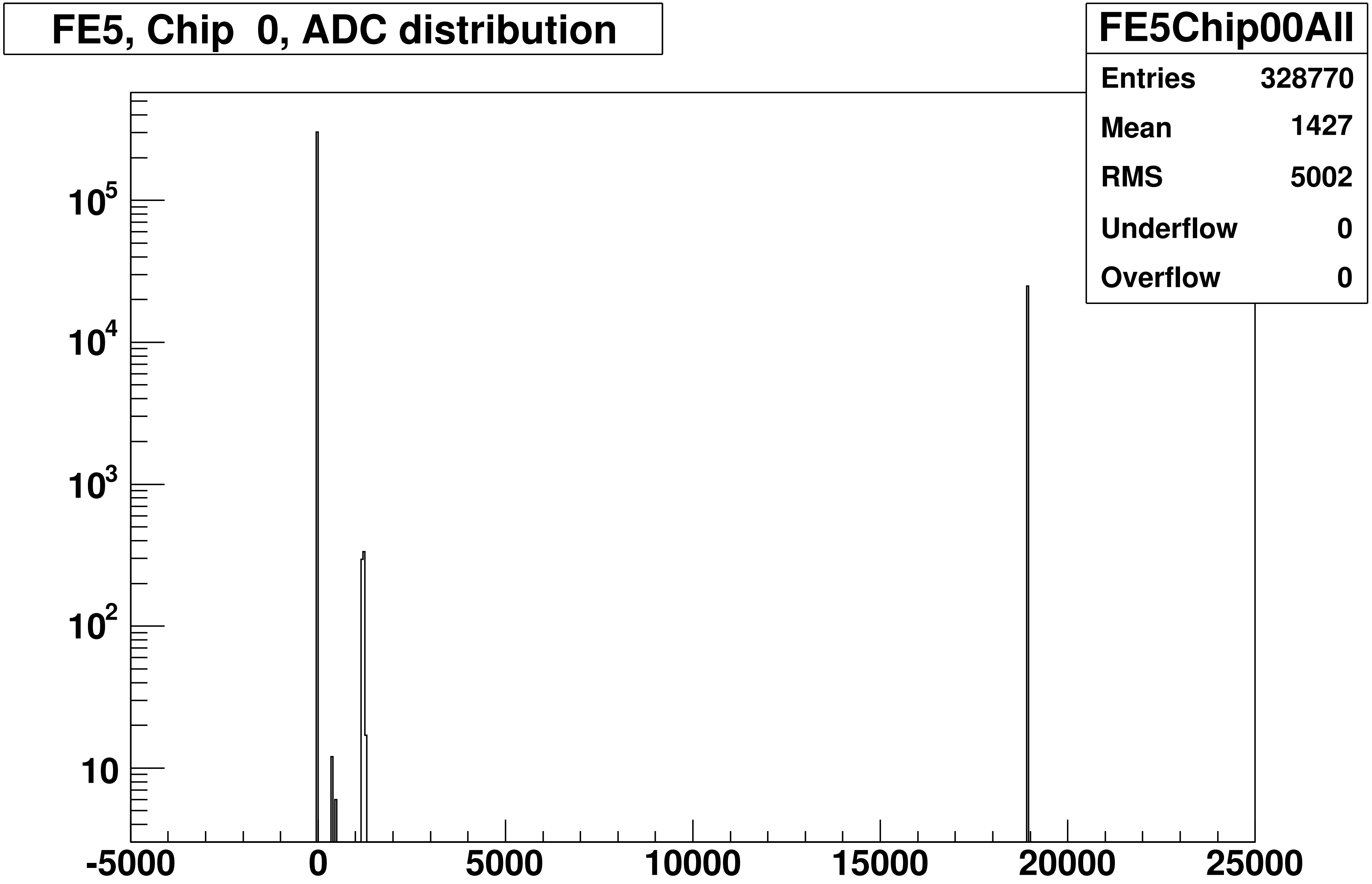
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE5, Chip 0, ADC distribution
FE5Chip00All
Entries 328770
Mean 1427
RMS 5002
Underflow 0
Overflow 0
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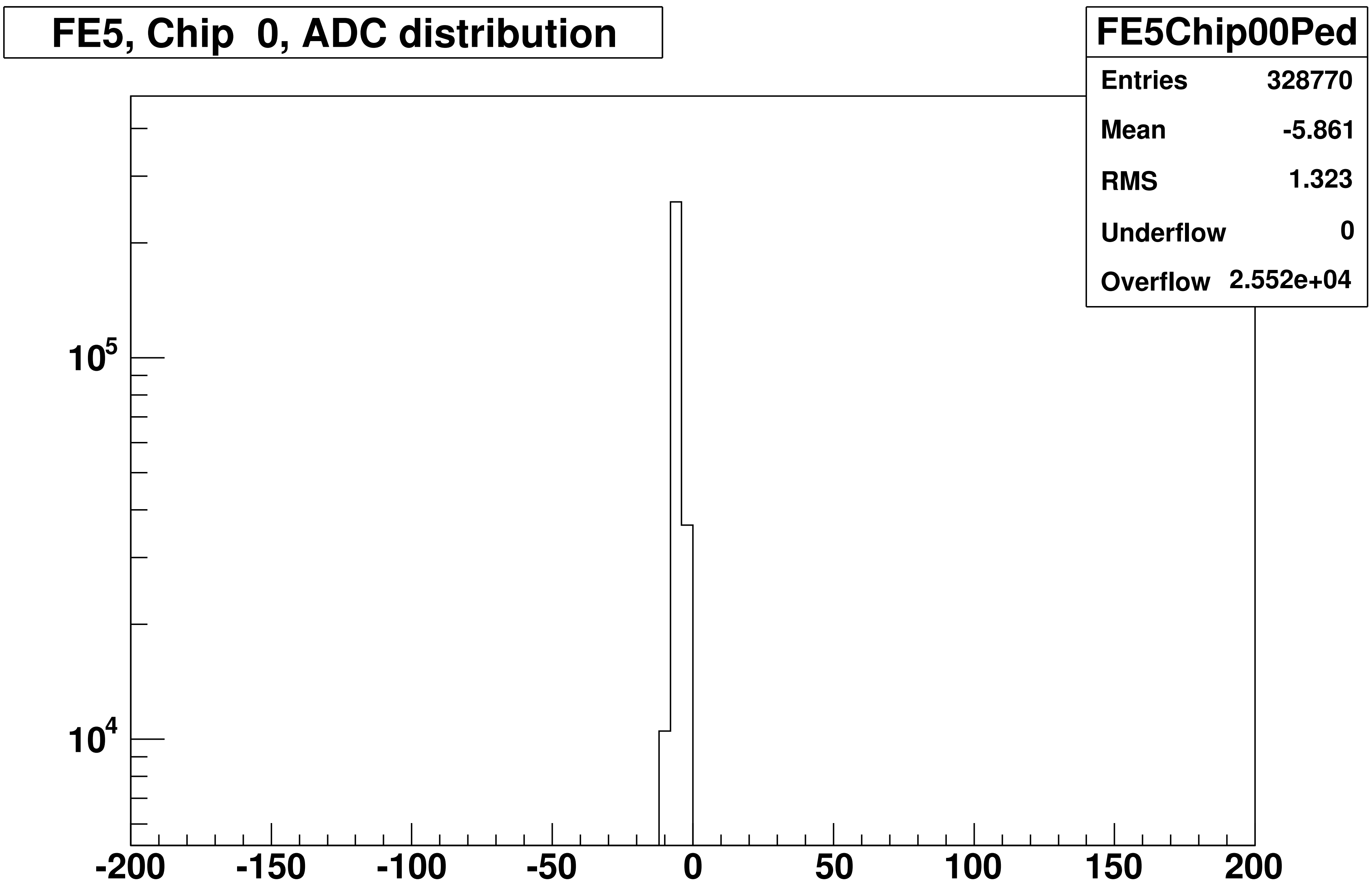
FE5, Chip 0, ADC distribution
FE5Chip00Ped
Entries 328770
Mean -5.861
RMS 1.323
Underflow 0
Overflow 2.552e+04
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10^4
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150
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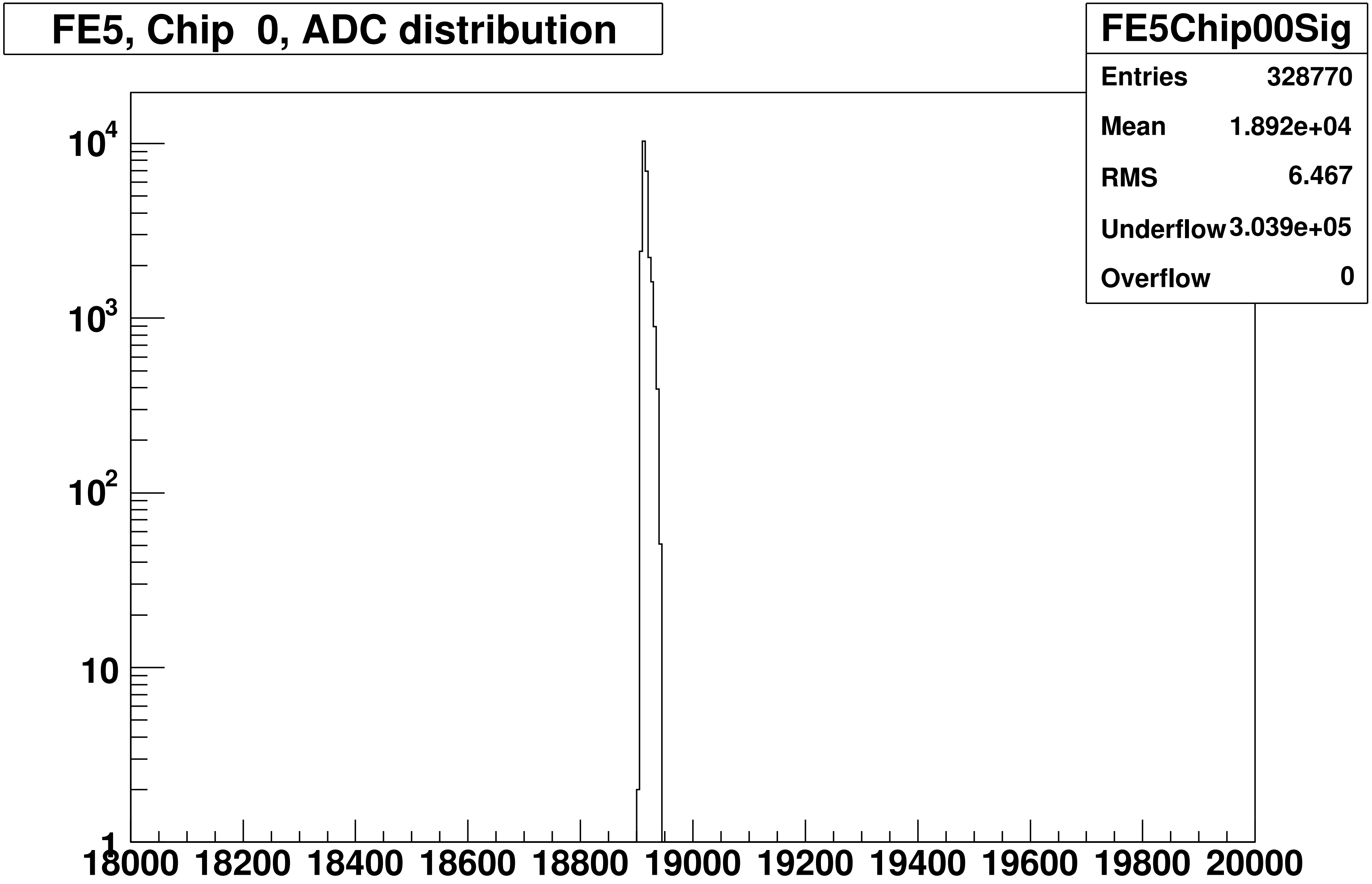

FE5, Chip 0, ADC distribution
FE5Chip00Sig
Entries 328770
Mean 1.892e+04
RMS 6.467
Underflow 3.039e+05
Overflow 0
10^4
10^3
10^2
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1
18000
18200
18400
18600
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19600
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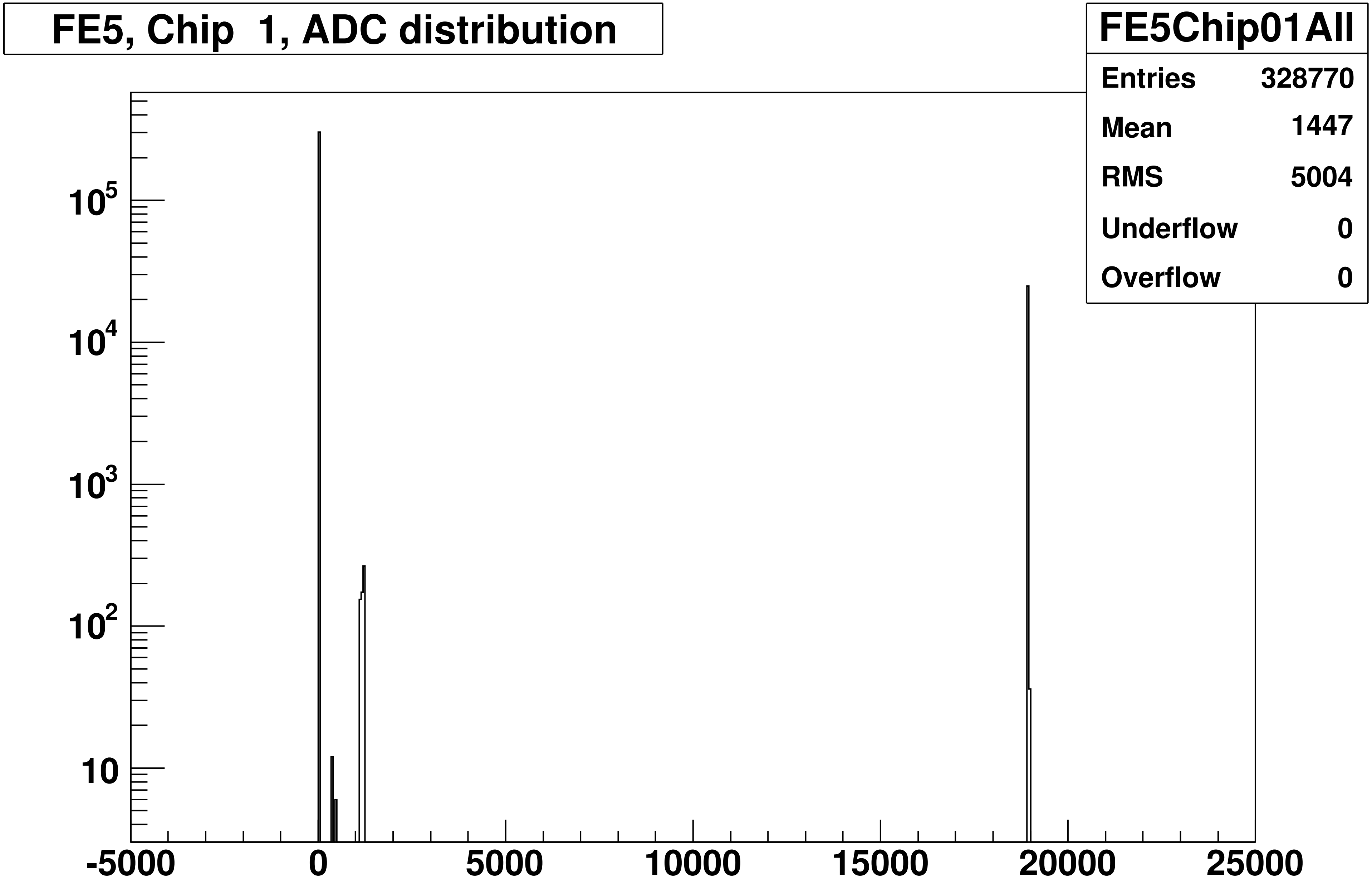

FE5, Chip 1, ADC distribution
FE5Chip01All
Entries 328770
Mean 1447
RMS 5004
Underflow 0
Overflow 0
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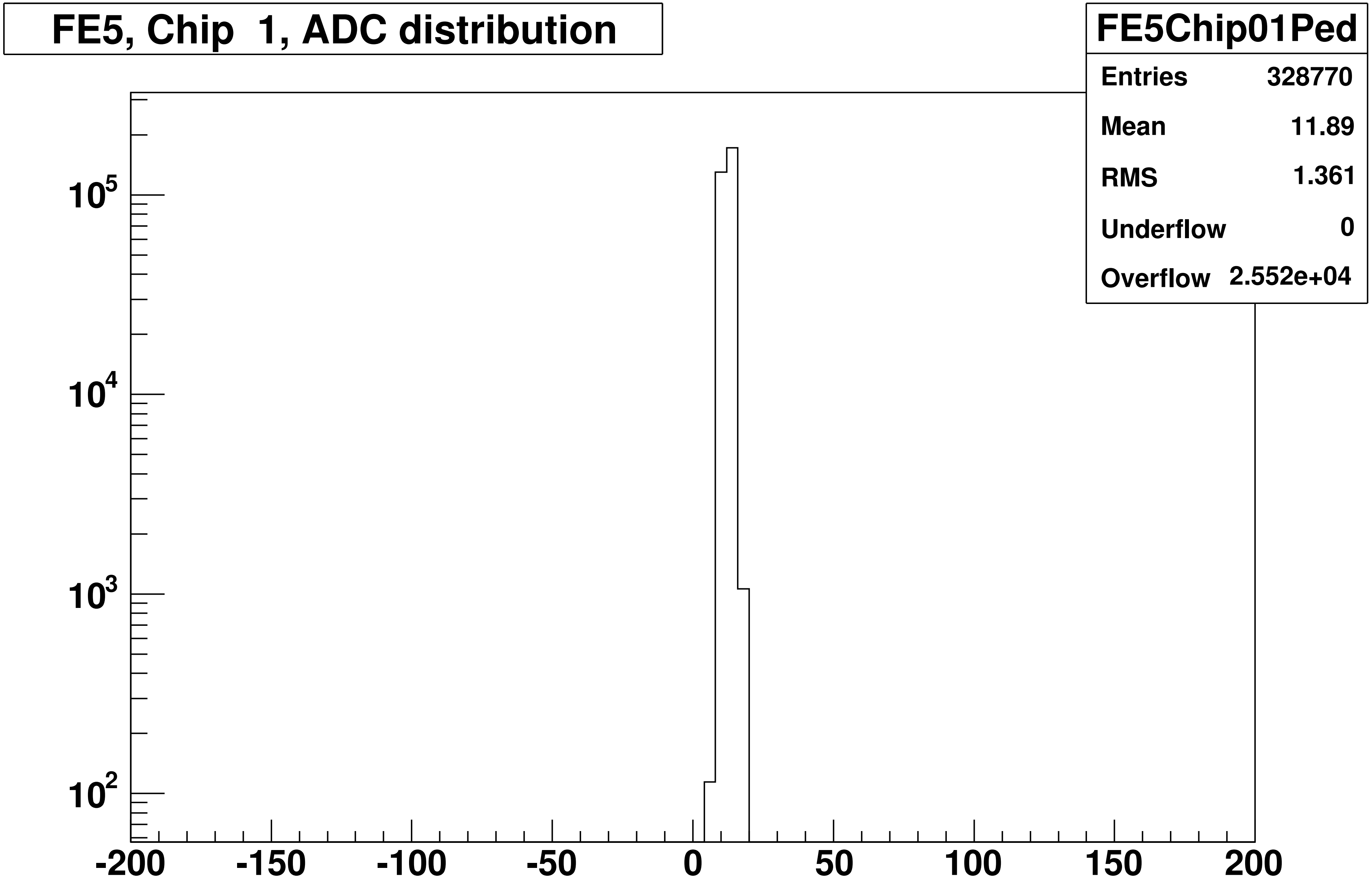

FE5, Chip 1, ADC distribution
FE5Chip01Ped
Entries 328770
Mean 11.89
RMS 1.361
Underflow 0
Overflow 2.552e+04
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10^3
10^2
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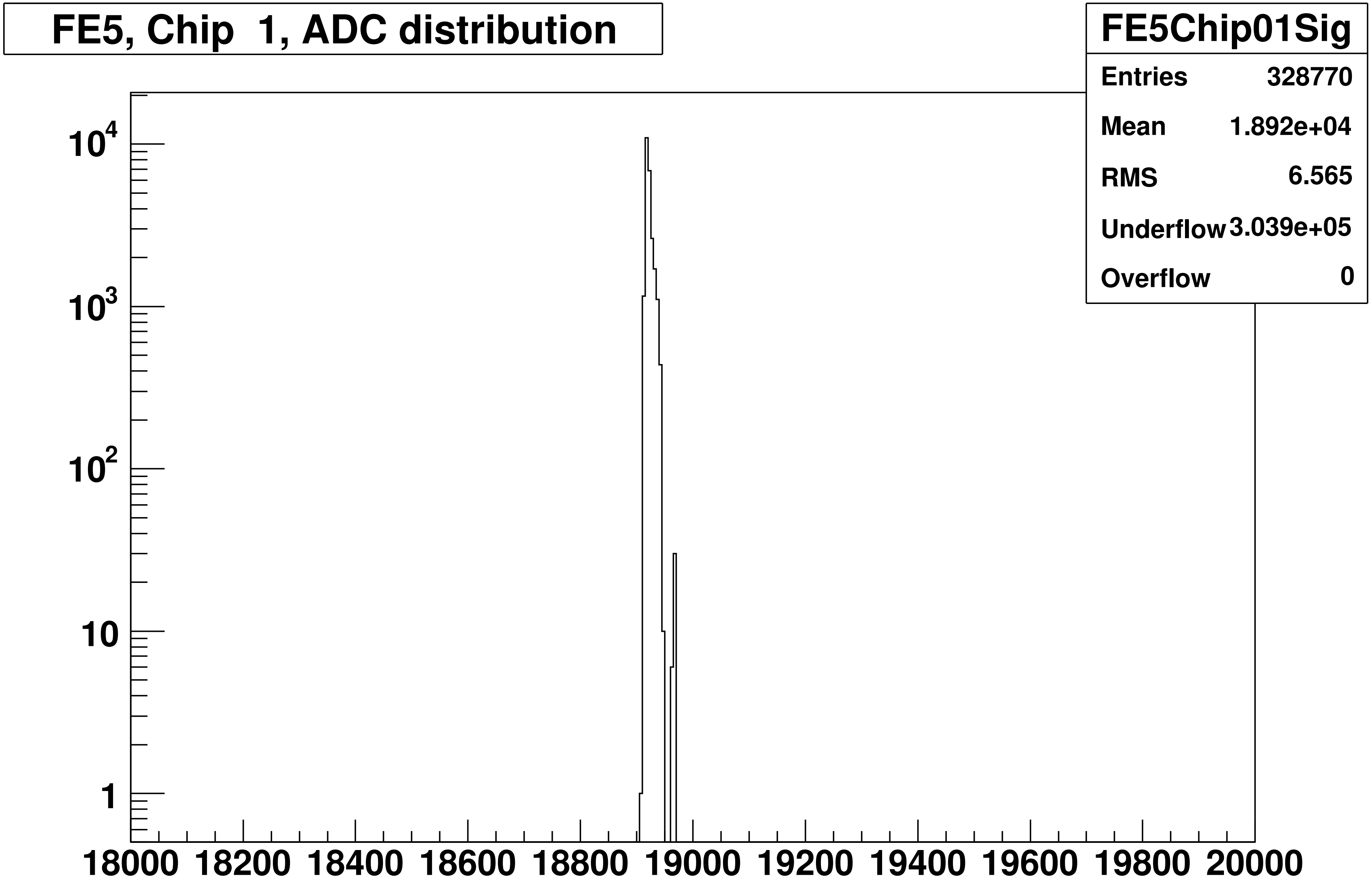
FE5, Chip 1, ADC distribution
FE5Chip01Sig
Entries 328770
Mean 1.892e+04
RMS 6.565
Underflow 3.039e+05
Overflow 0
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10^3
10^2
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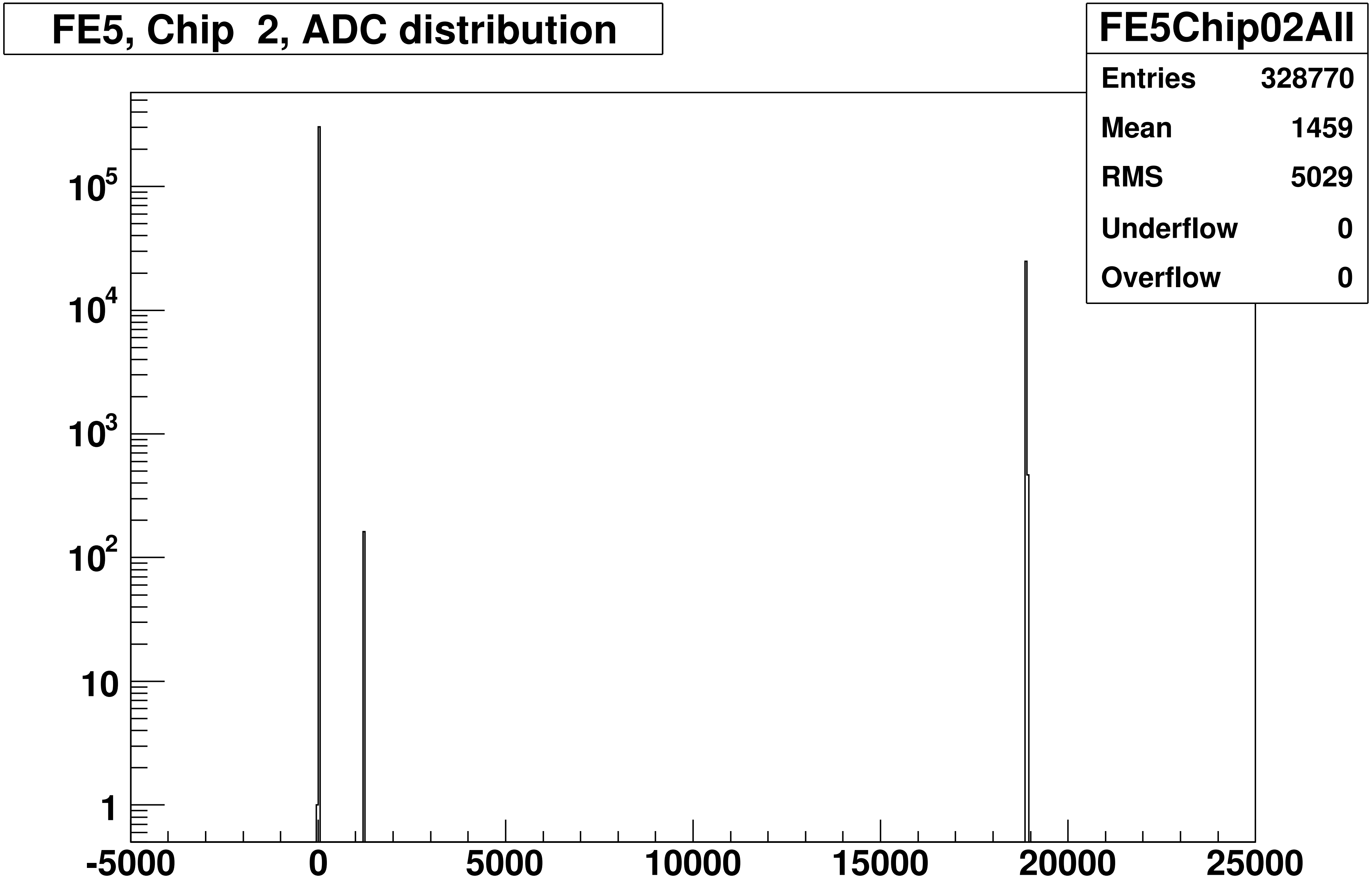
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE5, Chip 2, ADC distribution
FE5Chip02All
Entries 328770
Mean 1459
RMS 5029
Underflow 0
Overflow 0
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10^2
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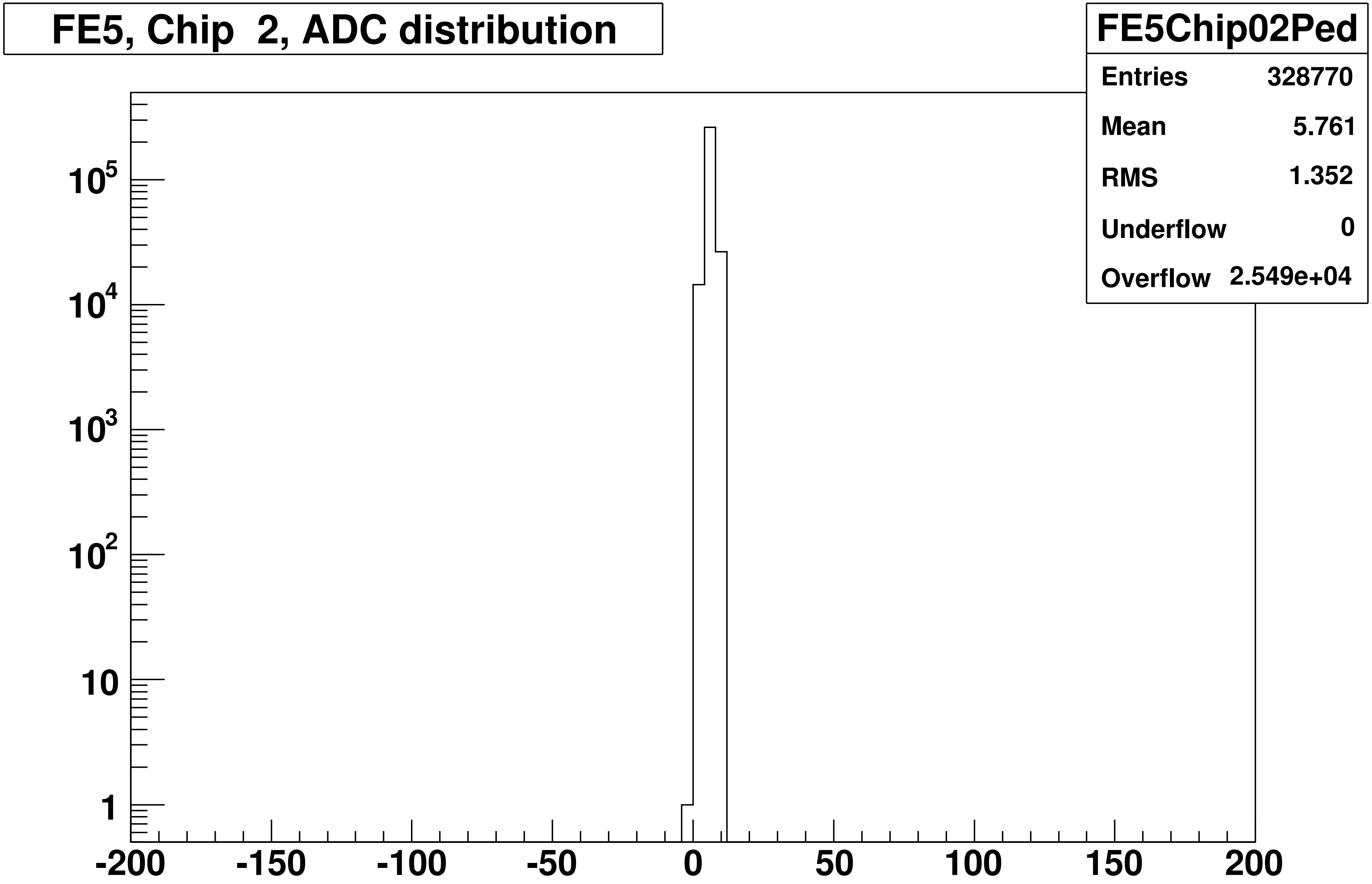
25000



FE5, Chip 2, ADC distribution
FE5Chip02Ped
Entries 328770
Mean 5.761
RMS 1.352
Underflow 0
Overflow 2.549e+04
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10^3
10^2
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150
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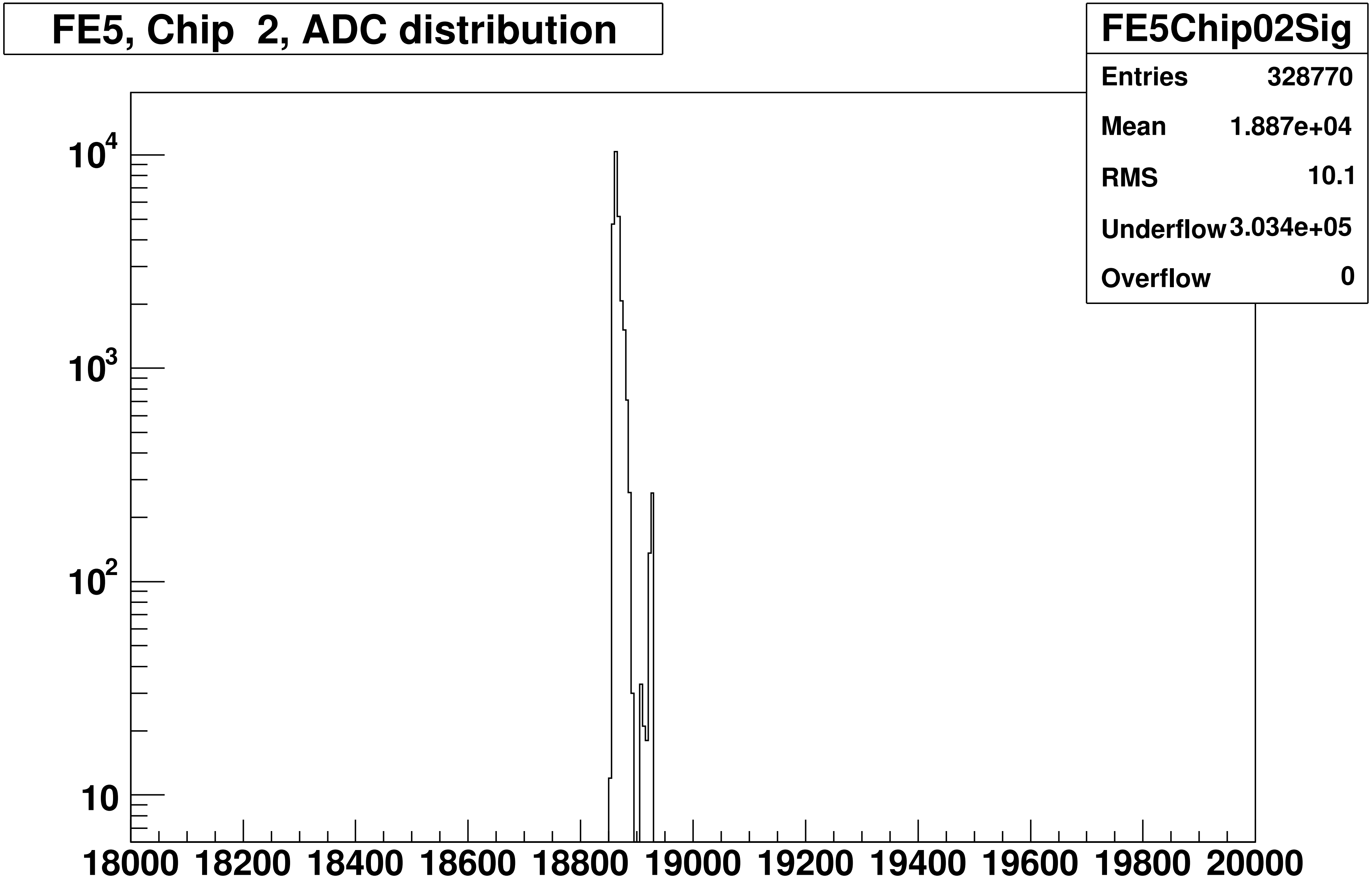

FE5, Chip 2, ADC distribution
FE5Chip02Sig
Entries 328770
Mean 1.887e+04
RMS 10.1
Underflow 3.034e+05
Overflow 0
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10^3
10^2
10
18000
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18400
18600
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19000
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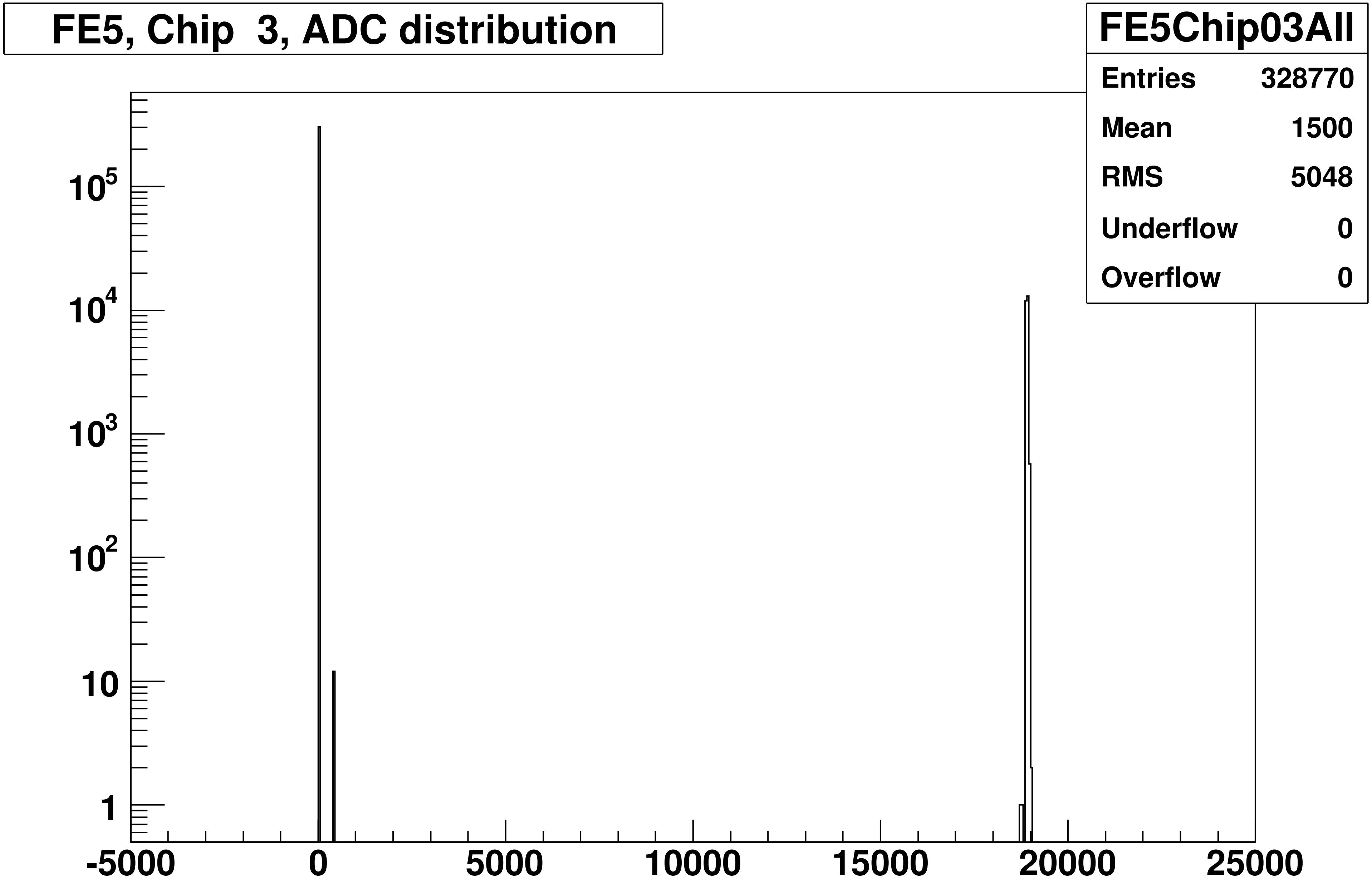
FE5, Chip 3, ADC distribution
FE5Chip03All
Entries 328770
Mean 1500
RMS 5048
Underflow 0
Overflow 0
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10^3
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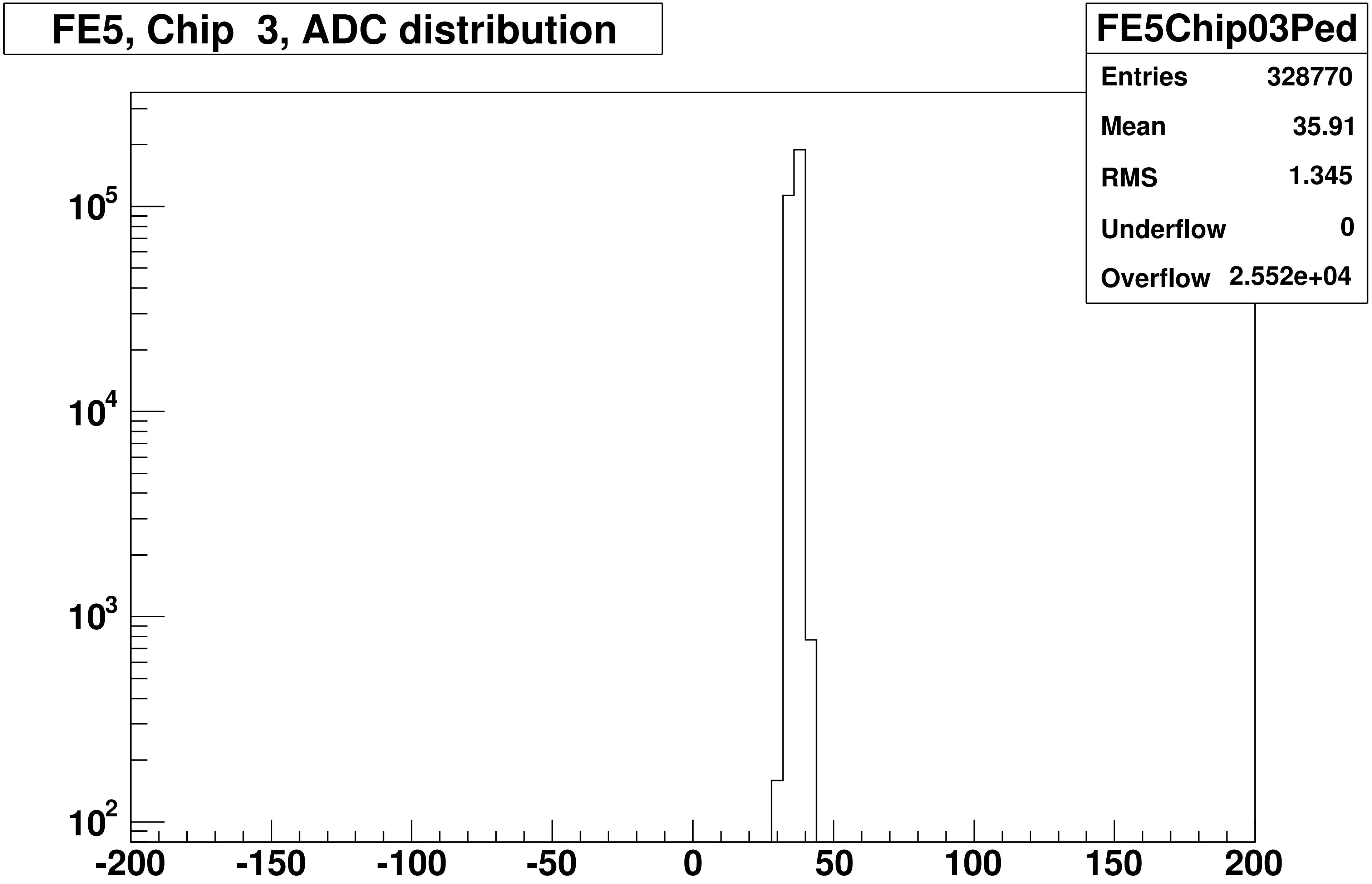
FE5, Chip 3, ADC distribution
FE5Chip03Ped
Entries 328770
Mean 35.91
RMS 1.345
Underflow 0
Overflow 2.552e+04
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10^4
10^3
10^2
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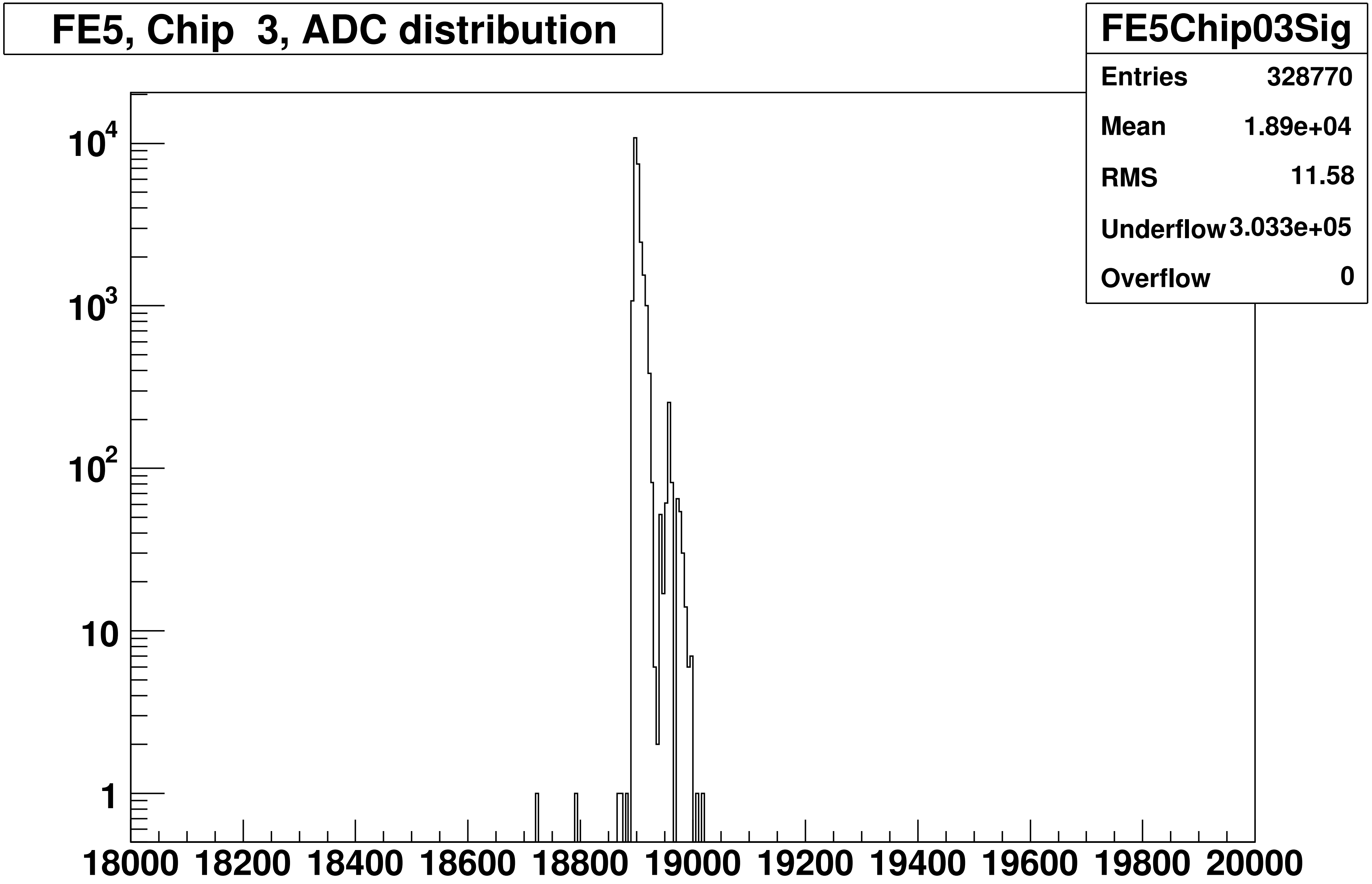
100
150
200


FE5, Chip 3, ADC distribution
FE5Chip03Sig
Entries 328770
Mean 1.89e+04
RMS 11.58
Underflow 3.033e+05
Overflow 0
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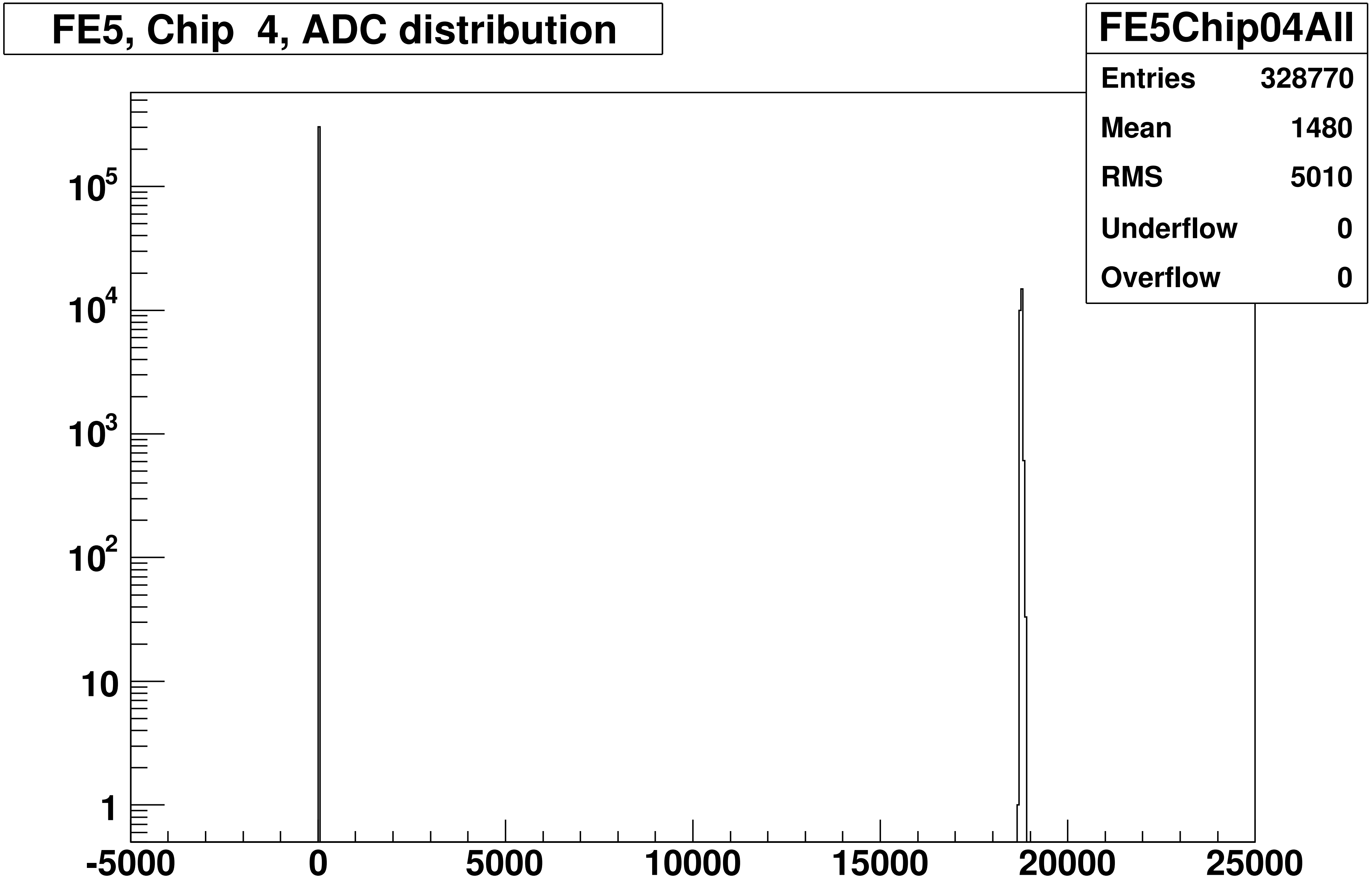
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE5, Chip 4, ADC distribution
FE5Chip04All
Entries 328770
Mean 1480
RMS 5010
Underflow 0
Overflow 0
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10^4
10^3
10^2
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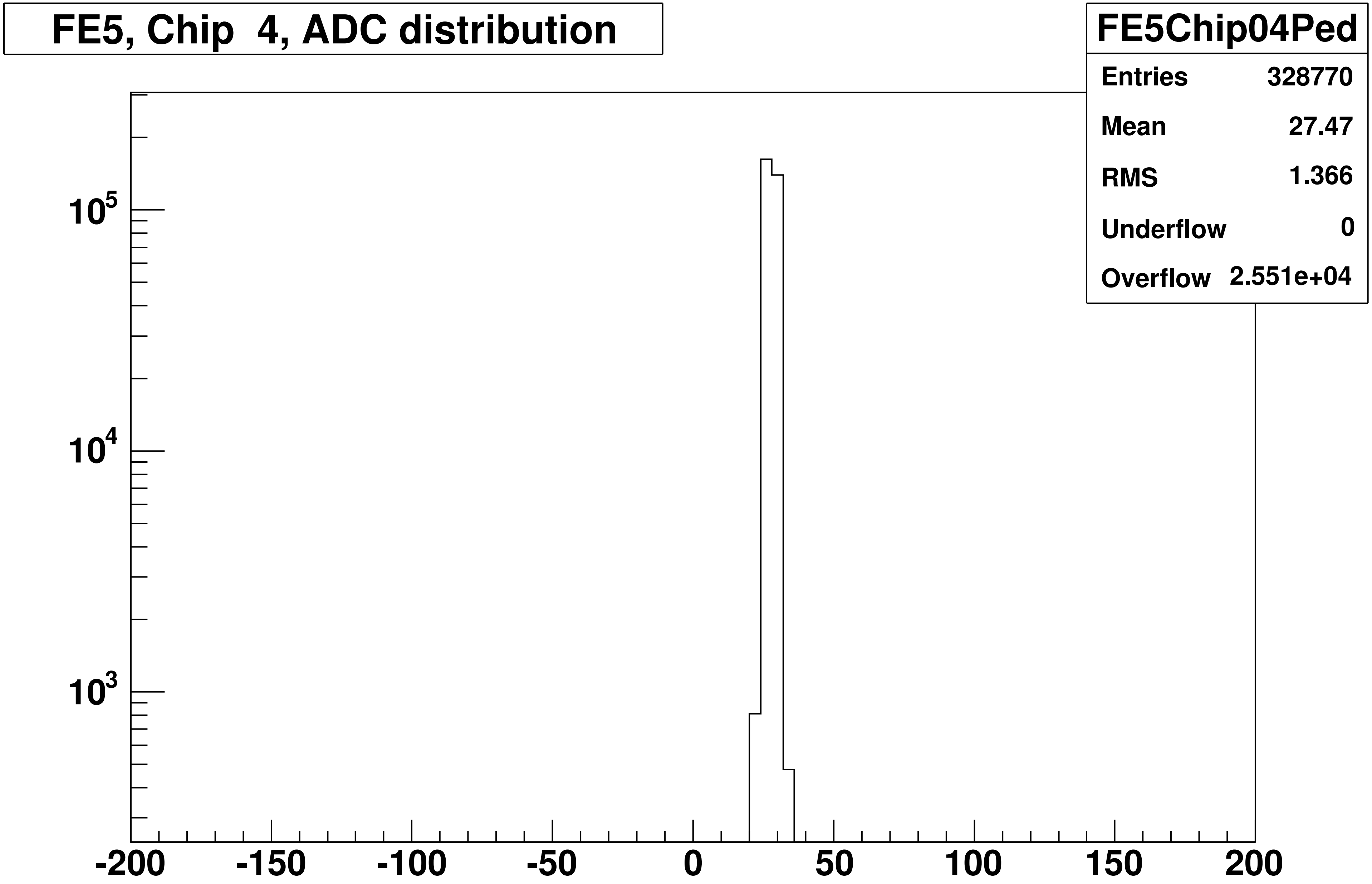
FE5, Chip 4, ADC distribution
FE5Chip04Ped
Entries 328770
Mean 27.47
RMS 1.366
Underflow 0
Overflow 2.551e+04
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10^4
10^3
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150
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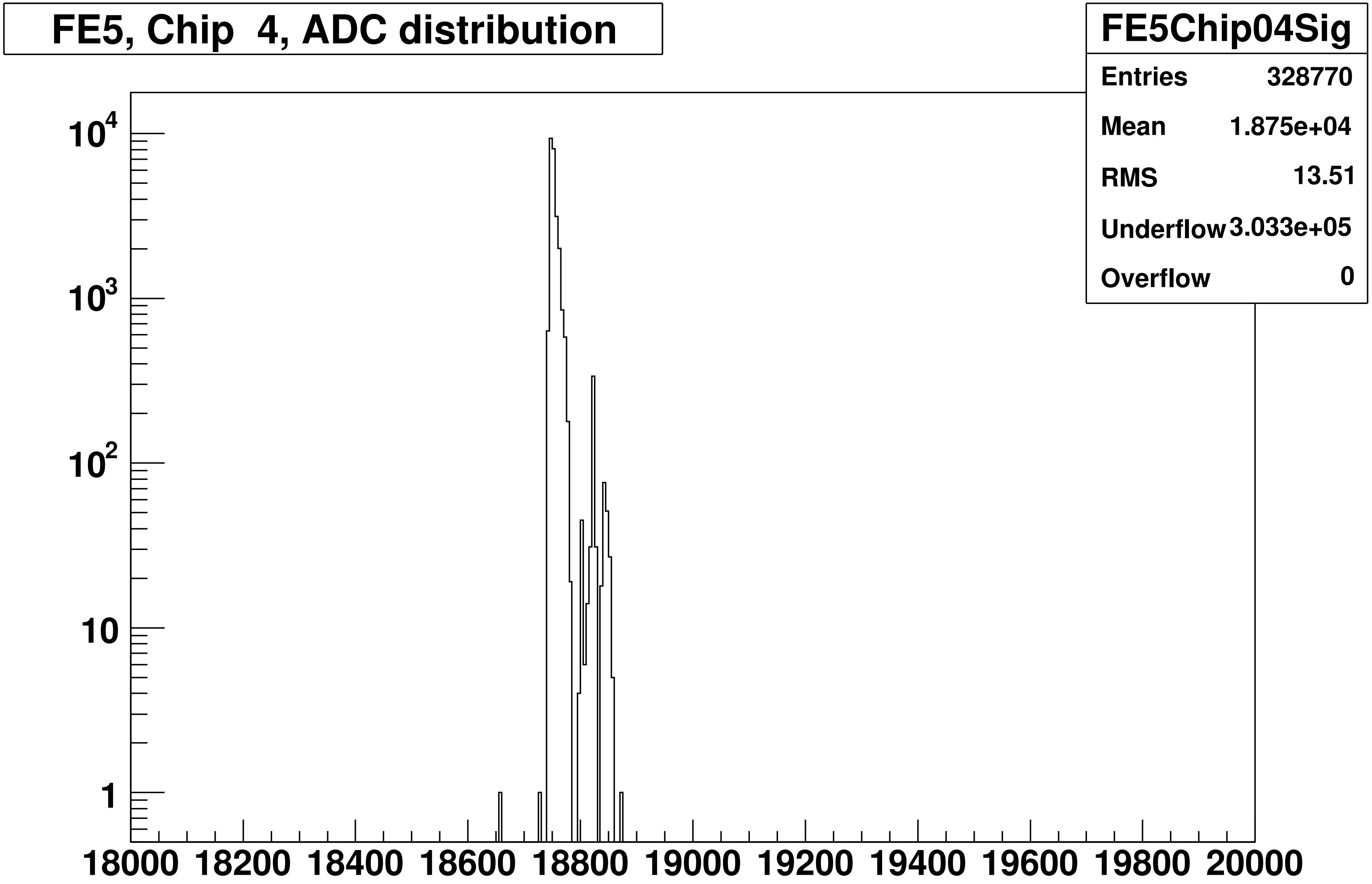
FE5, Chip 4, ADC distribution
FE5Chip04Sig
Entries 328770
Mean 1.875e+04
RMS 13.51
Underflow 3.033e+05
Overflow 0
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10^3
10^2
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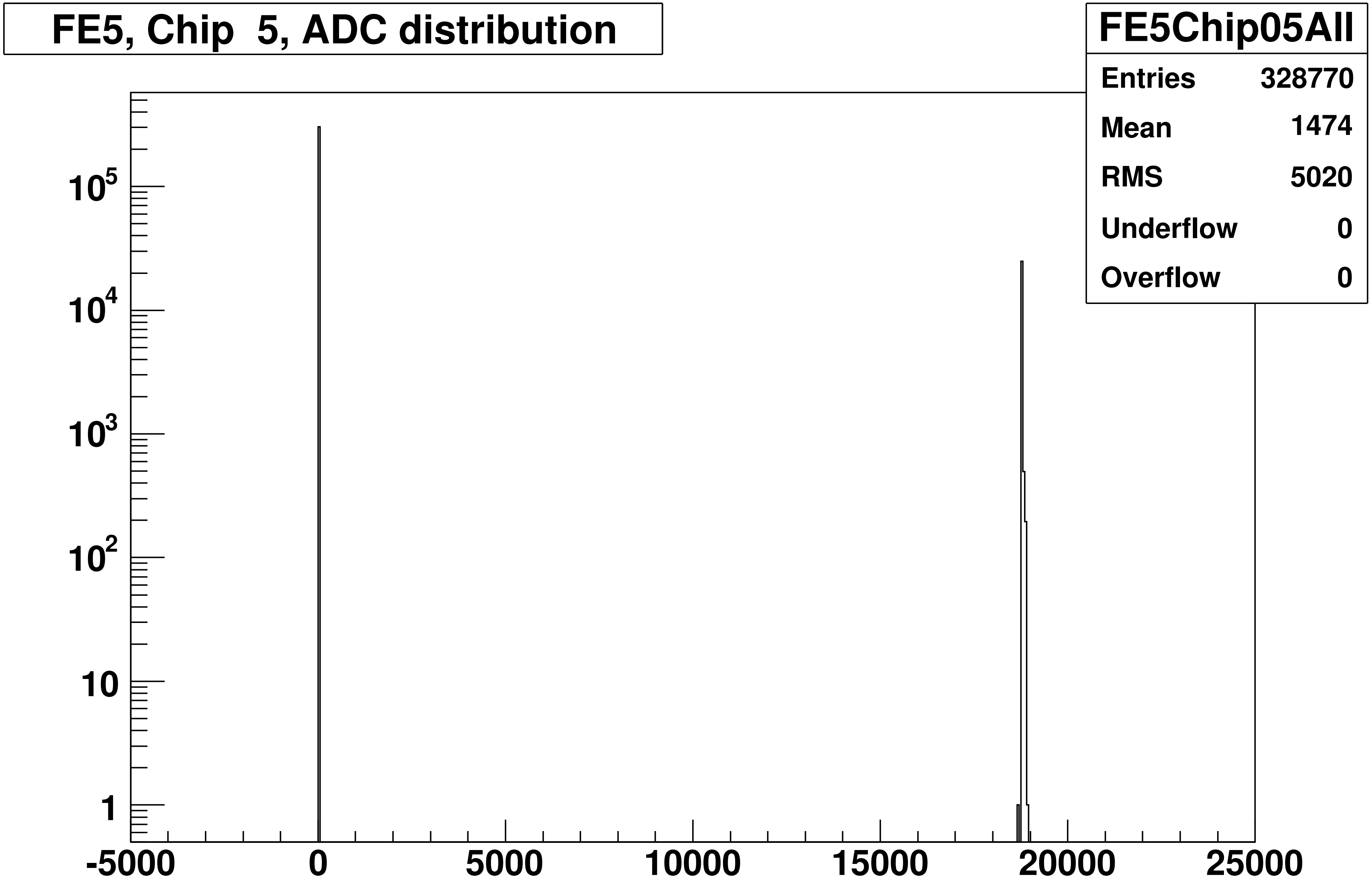
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE5, Chip 5, ADC distribution
FE5Chip05All
Entries 328770
Mean 1474
RMS 5020
Underflow 0
Overflow 0
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10^4
10^3
10^2
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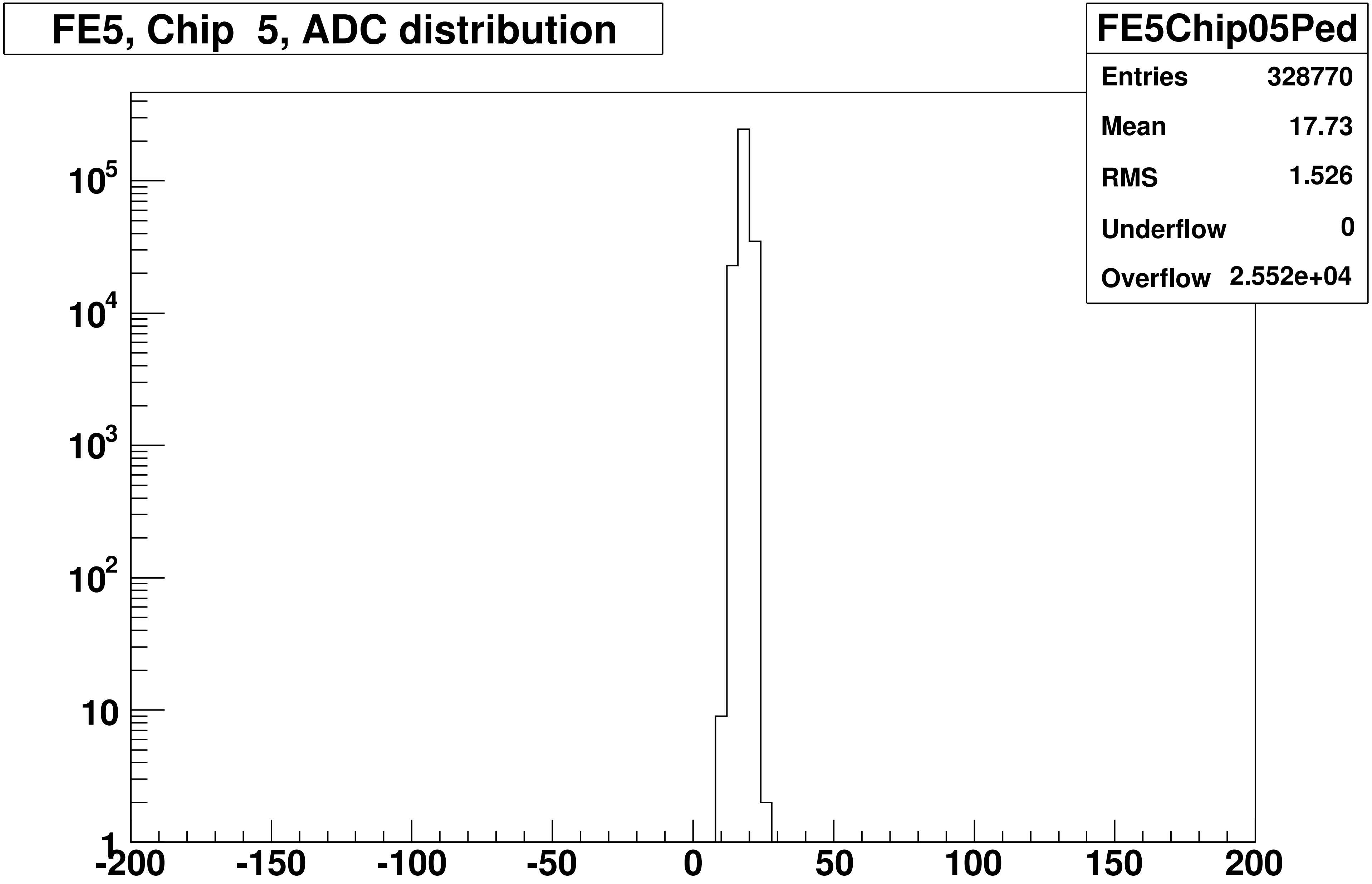
20000
25000



FE5, Chip 5, ADC distribution
FE5Chip05Ped
Entries 328770
Mean 17.73
RMS 1.526
Underflow 0
Overflow 2.552e+04
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10
10^2
10^3
10^4
10^5
-200
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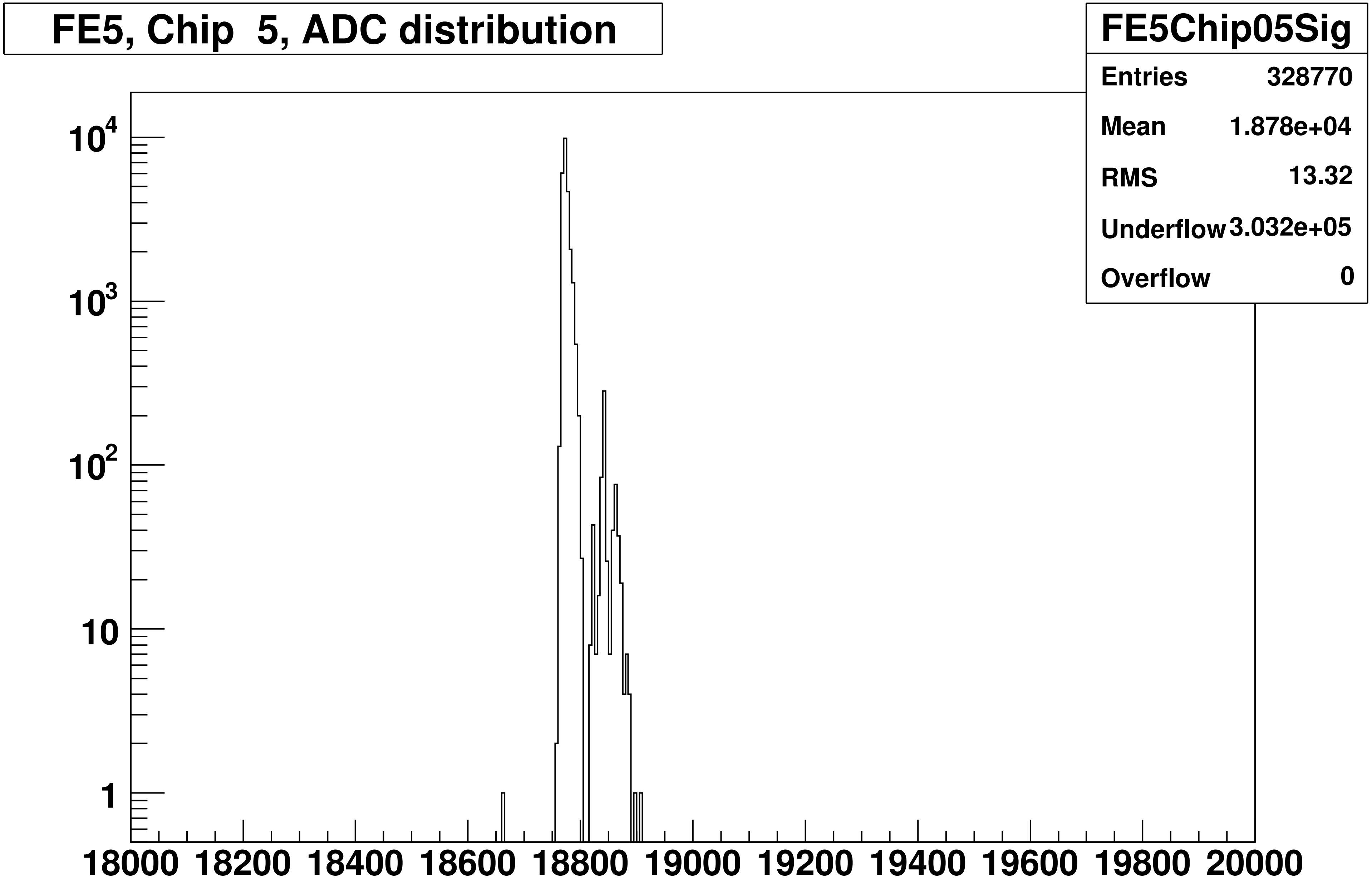
50
100
150
200


FE5, Chip 5, ADC distribution
FE5Chip05Sig
Entries 328770
Mean 1.878e+04
RMS 13.32
Underflow 3.032e+05
Overflow 0
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10^3
10^2
10
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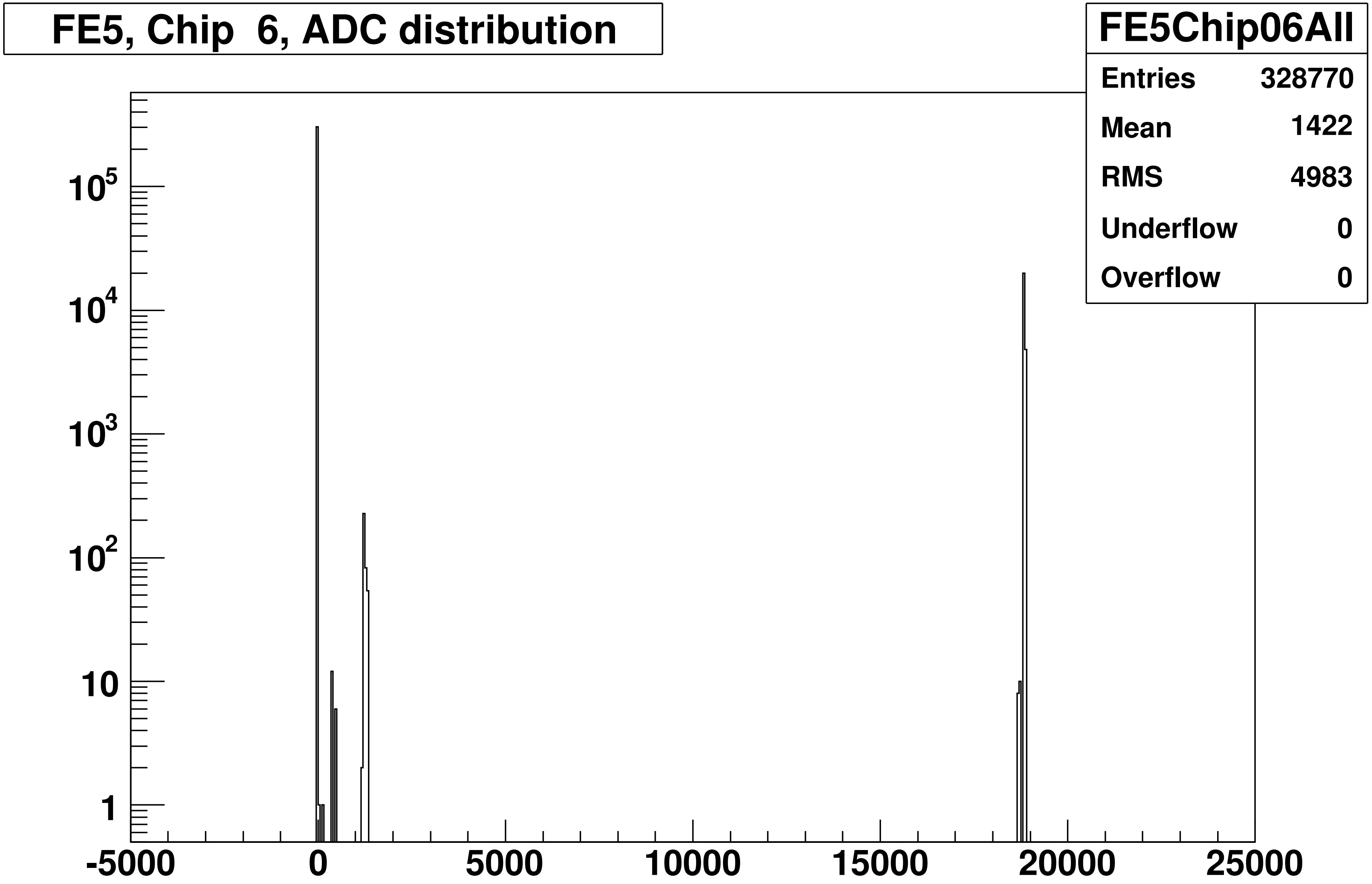
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE5, Chip 6, ADC distribution
FE5Chip06All
Entries 328770
Mean 1422
RMS 4983
Underflow 0
Overflow 0
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10^3
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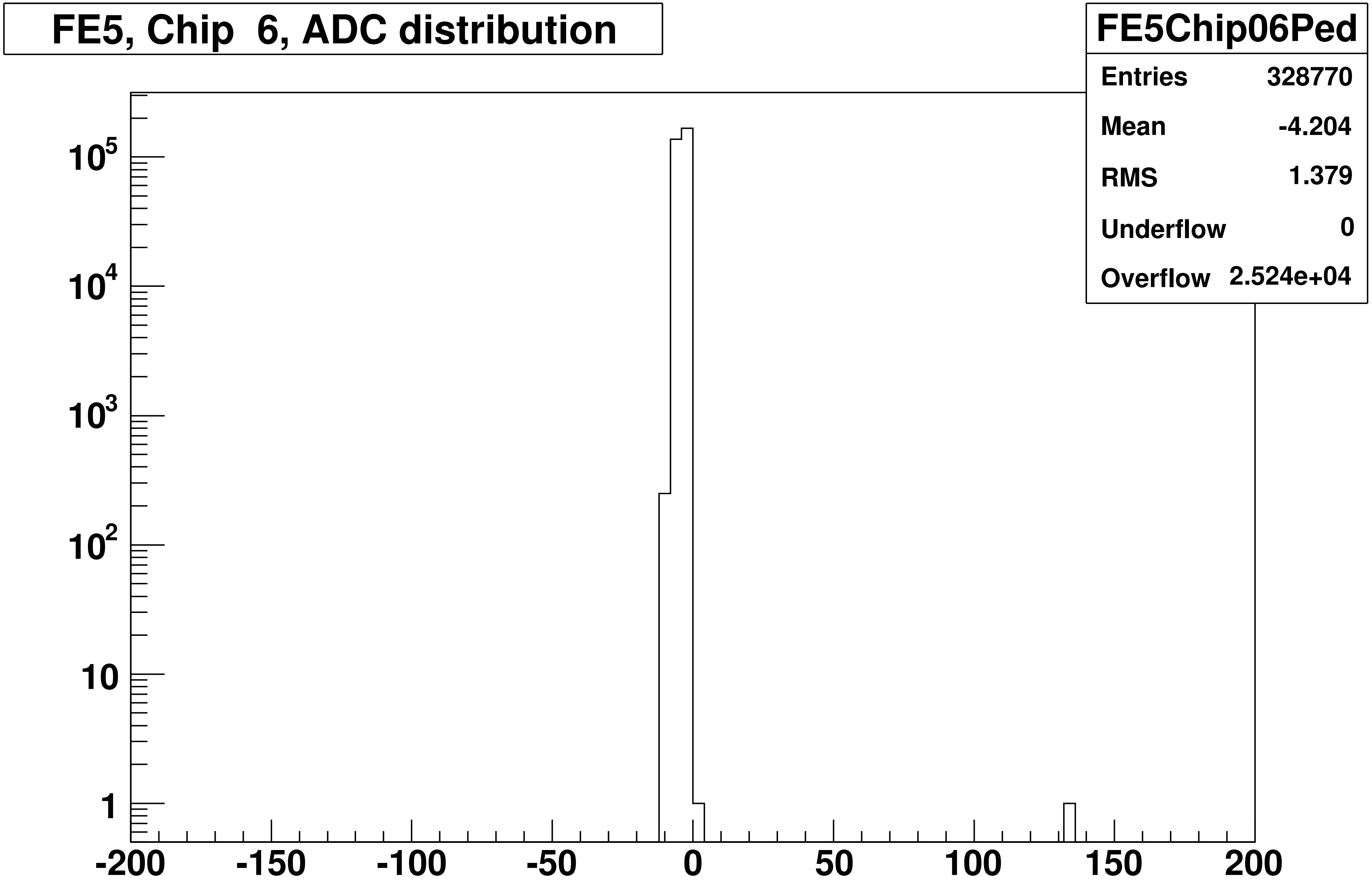
20000
25000


FE5, Chip 6, ADC distribution
FE5Chip06Ped
Entries 328770
Mean -4.204
RMS 1.379
Underflow 0
Overflow 2.524e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
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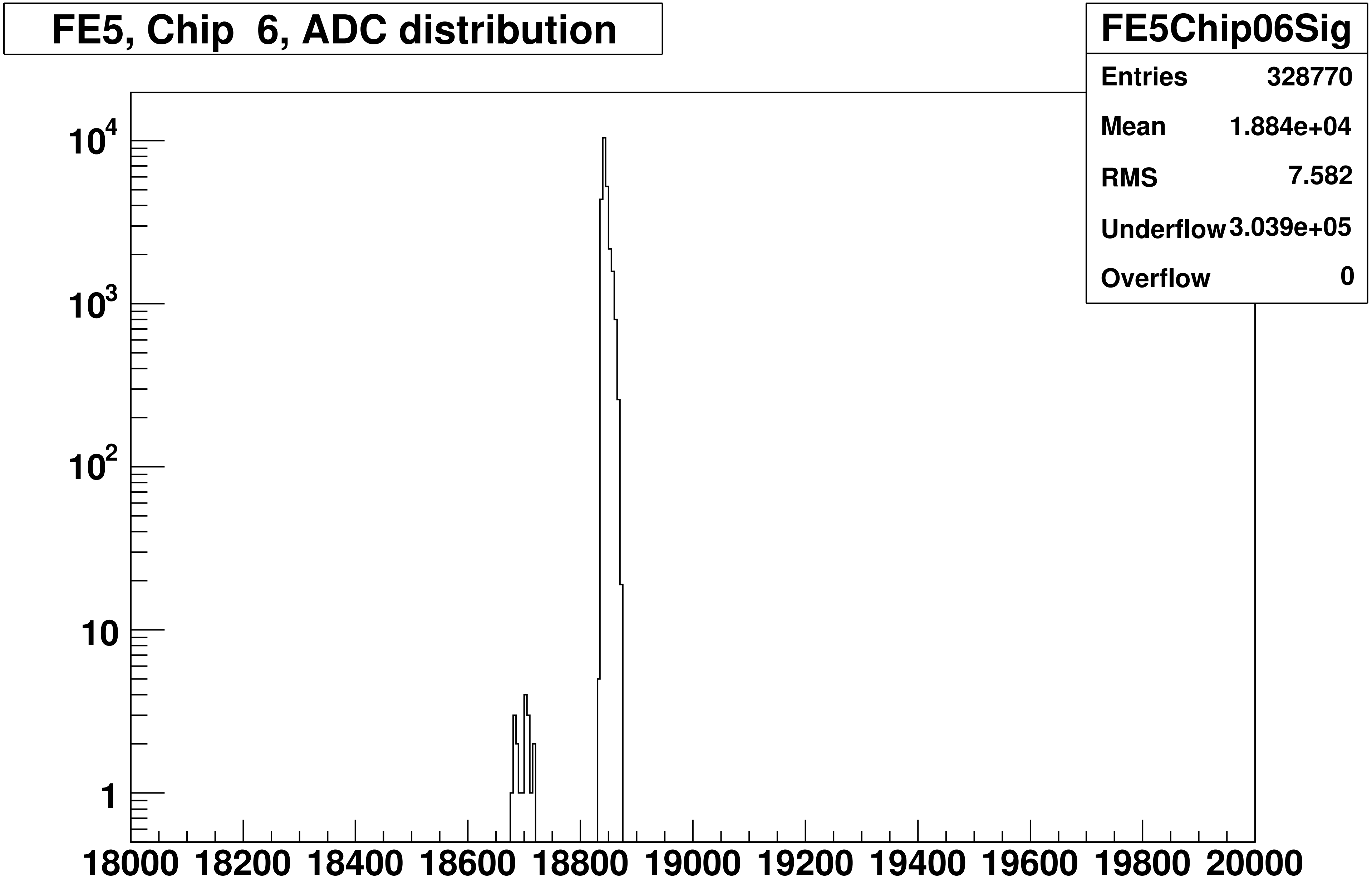
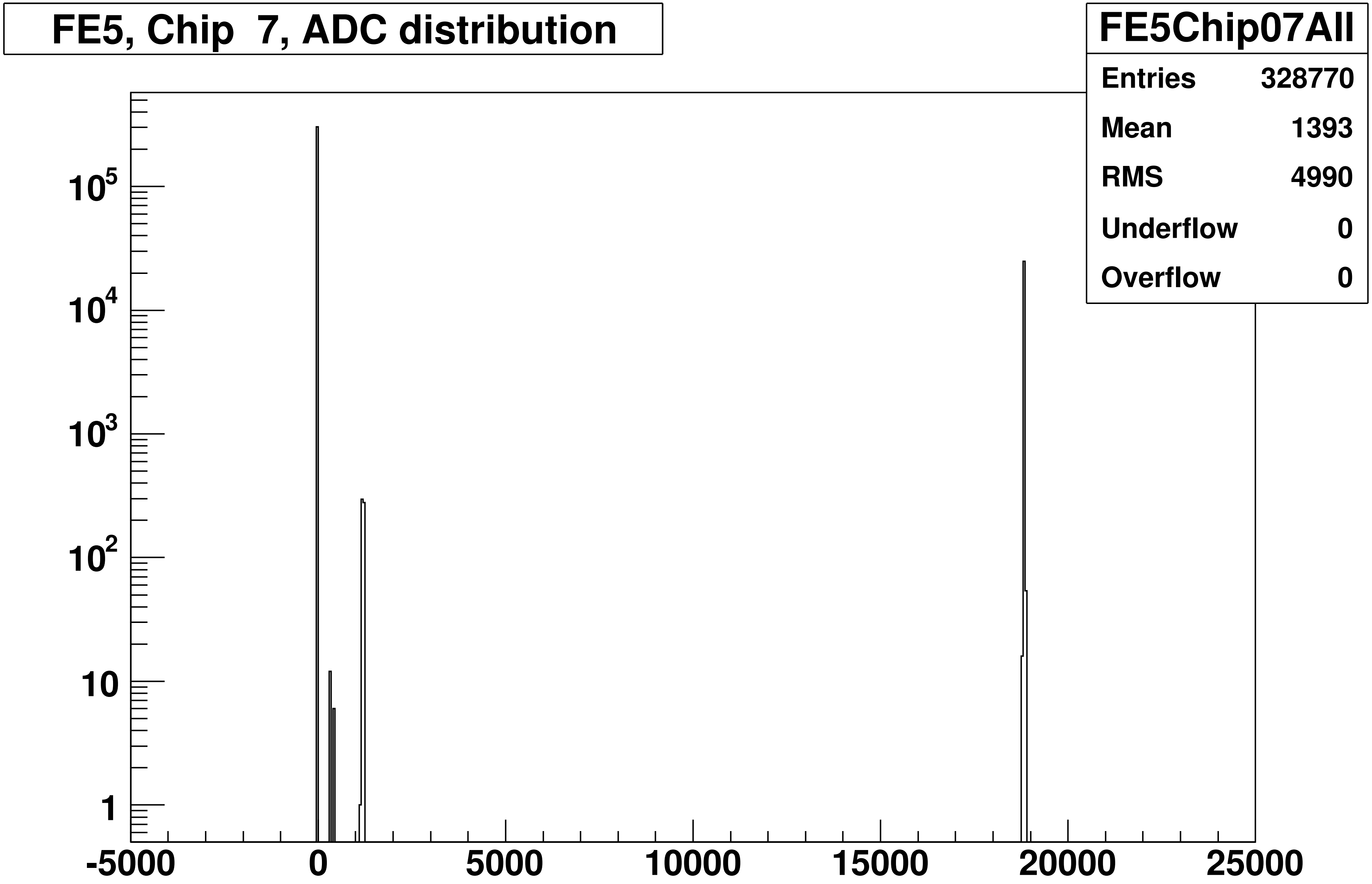
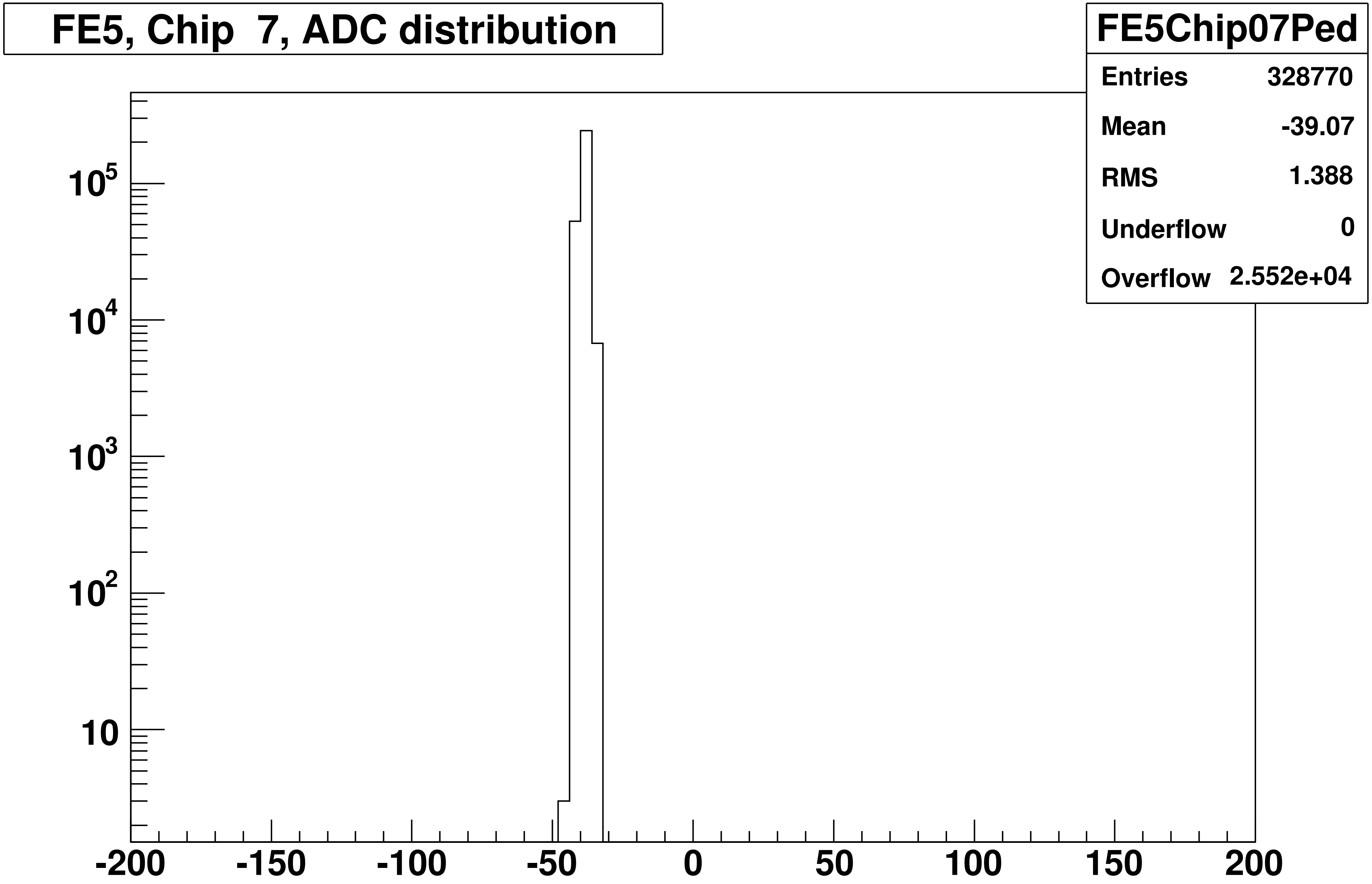
0
50
100
150
200


FE5, Chip 6, ADC distribution
FE5Chip06Sig
Entries 328770
Mean 1.884e+04
RMS 7.582
Underflow 3.039e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000


FE5, Chip 7, ADC distribution
FE5Chip07All
Entries 328770
Mean 1393
RMS 4990
Underflow 0
Overflow 0
1
10
10^2
10^3
10^4
10^5
-5000
0
5000
10000
15000
20000
25000


FE5, Chip 7, ADC distribution
FE5Chip07Ped
Entries 328770
Mean -39.07
RMS 1.388
Underflow 0
Overflow 2.552e+04
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10^2
10^3
10^4
10^5
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-150
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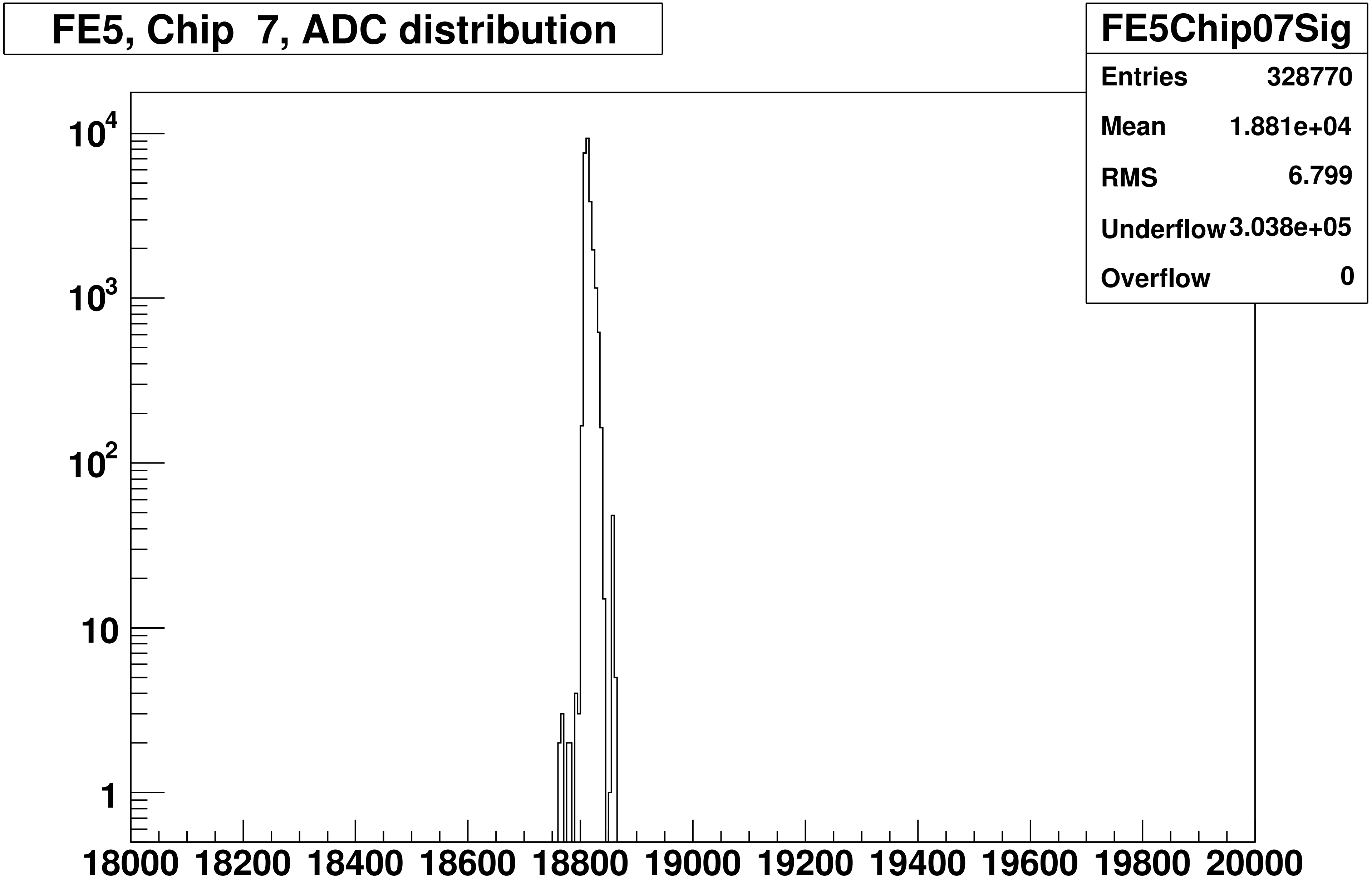
0
50
100
150
200



FE5, Chip 7, ADC distribution
FE5Chip07Sig
Entries 328770
Mean 1.881e+04
RMS 6.799
Underflow 3.038e+05
Overflow 0
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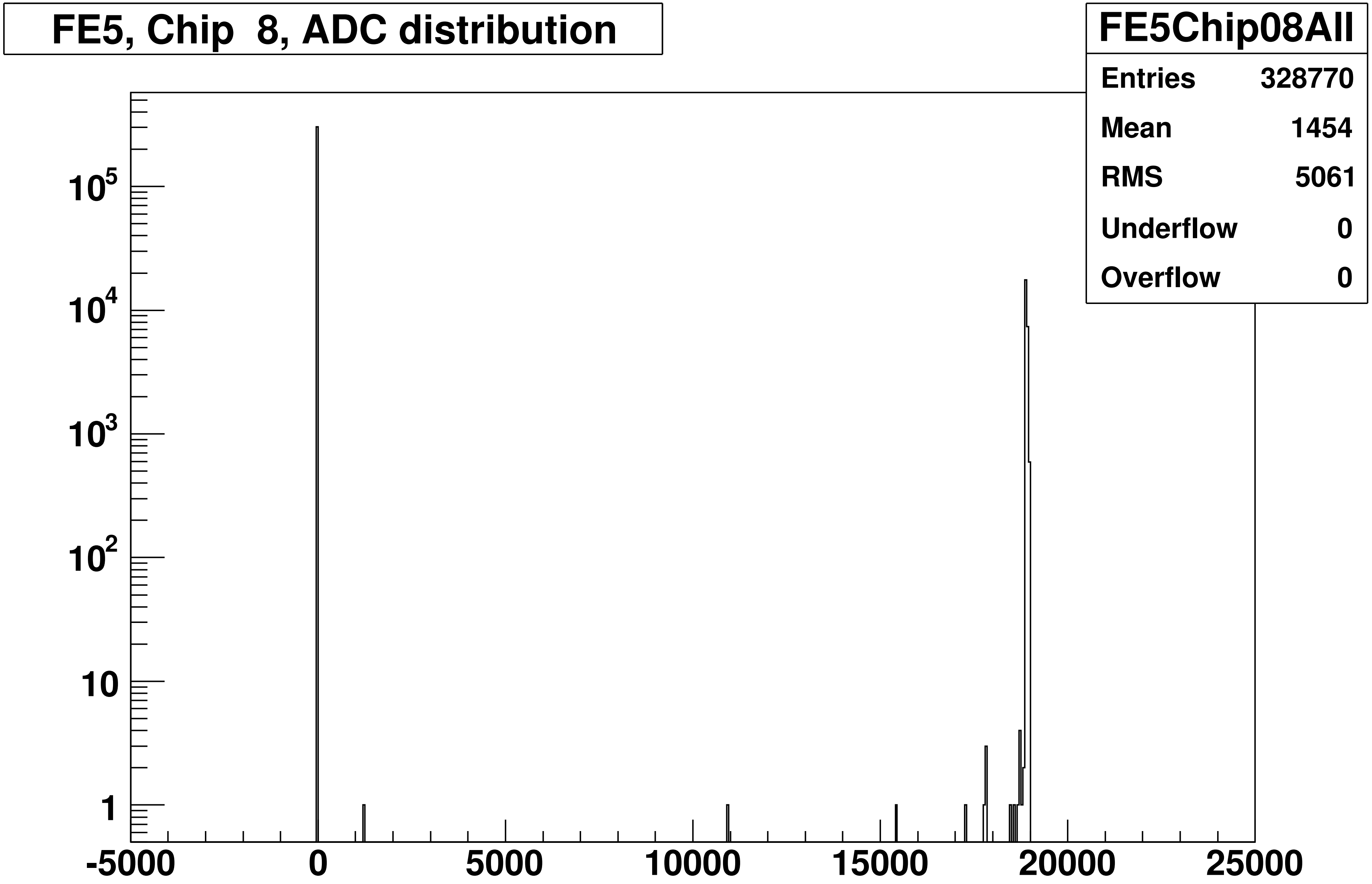
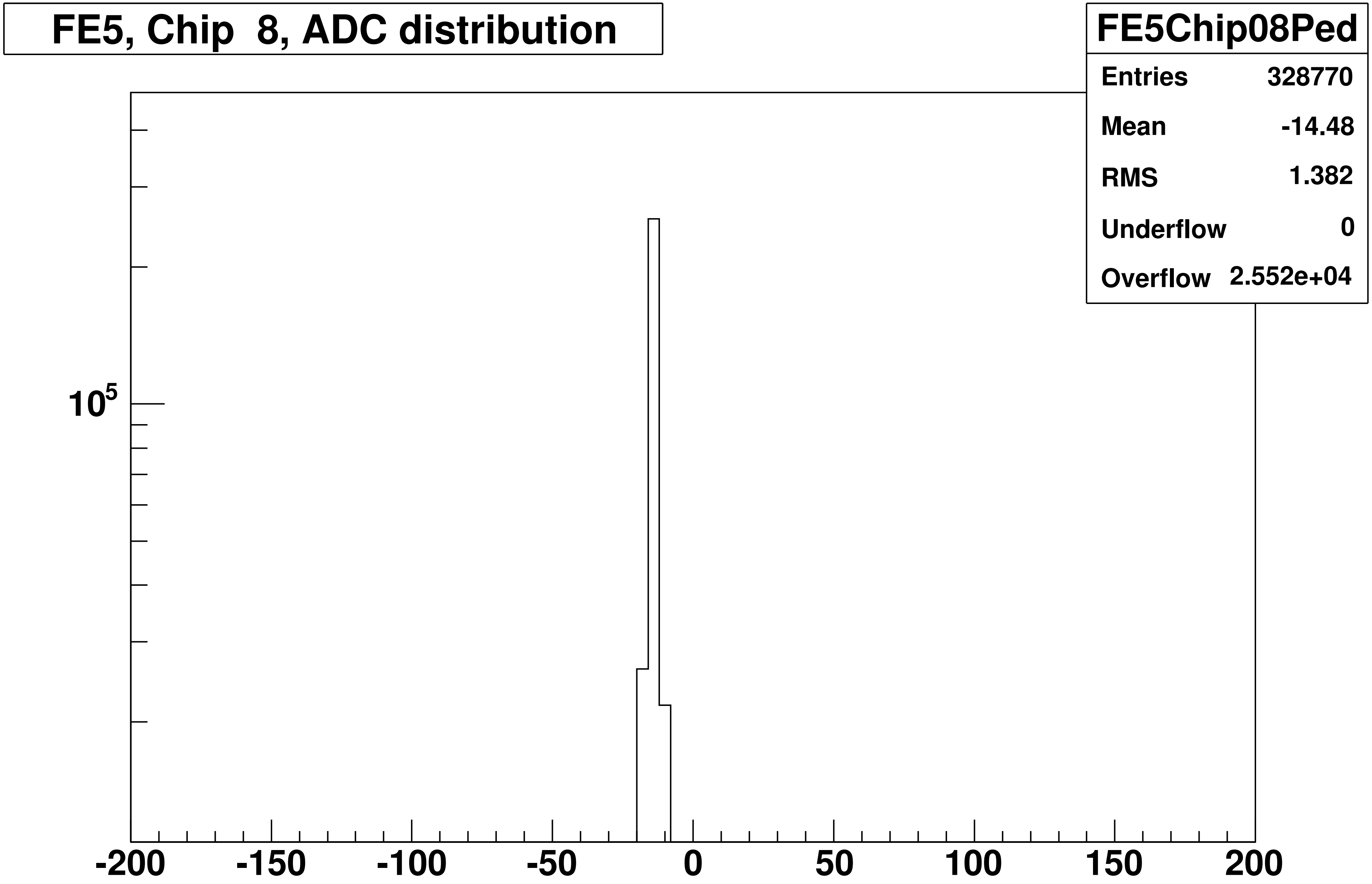
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE5, Chip 8, ADC distribution
FE5Chip08All
Entries 328770
Mean 1454
RMS 5061
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE5, Chip 8, ADC distribution
FE5Chip08Ped
Entries 328770
Mean -14.48
RMS 1.382
Underflow 0
Overflow 2.552e+04
10^5
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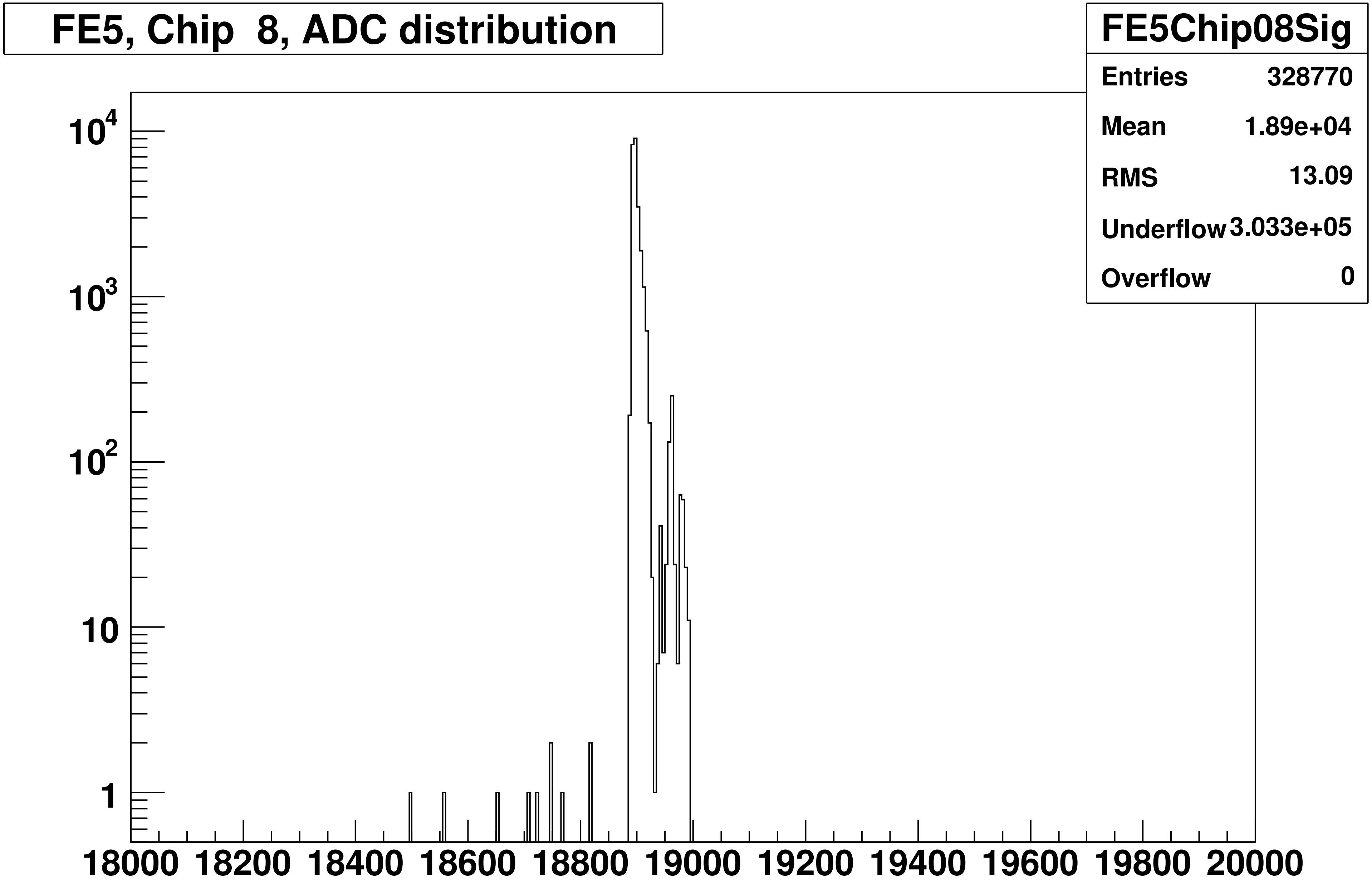
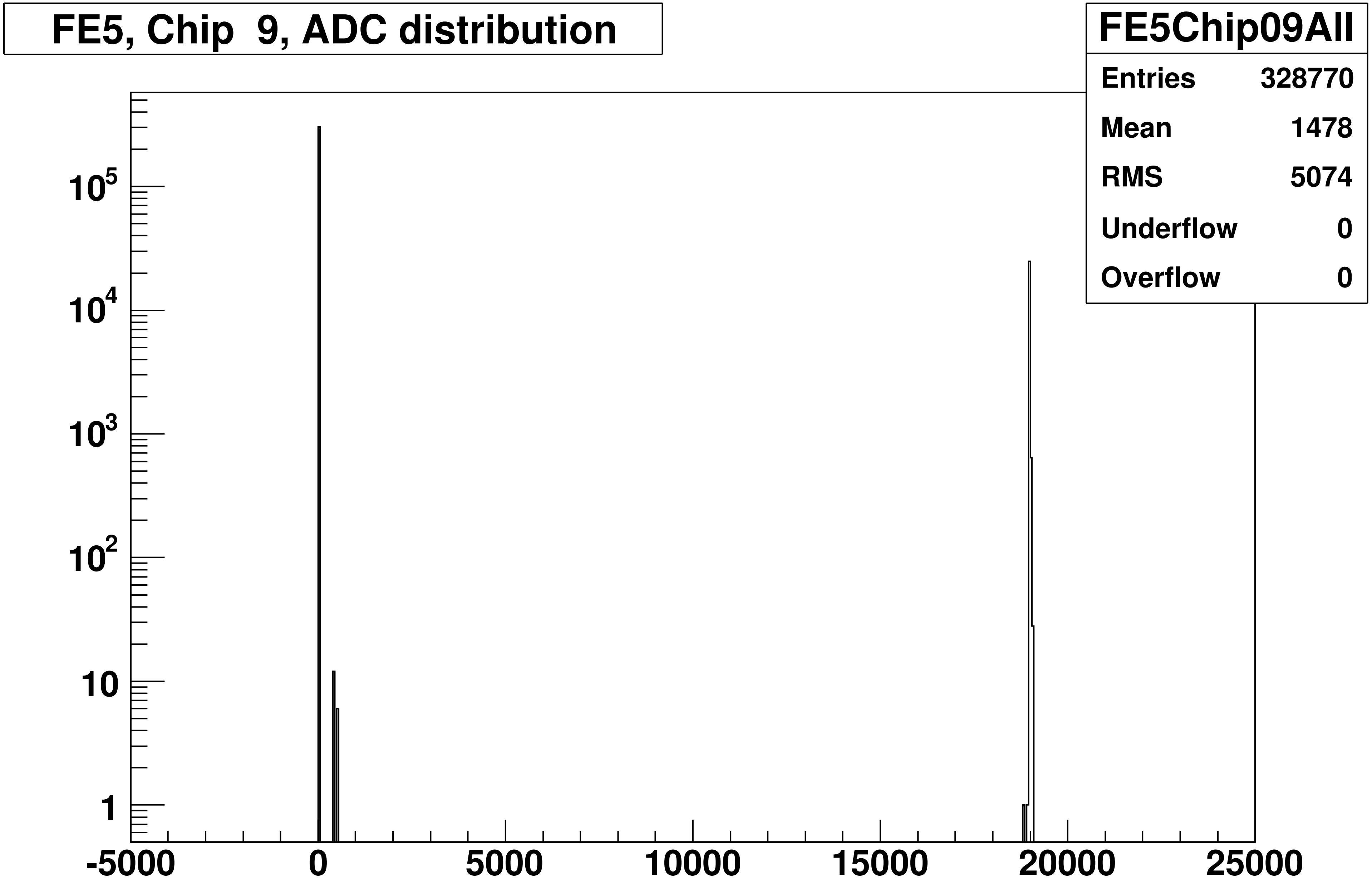
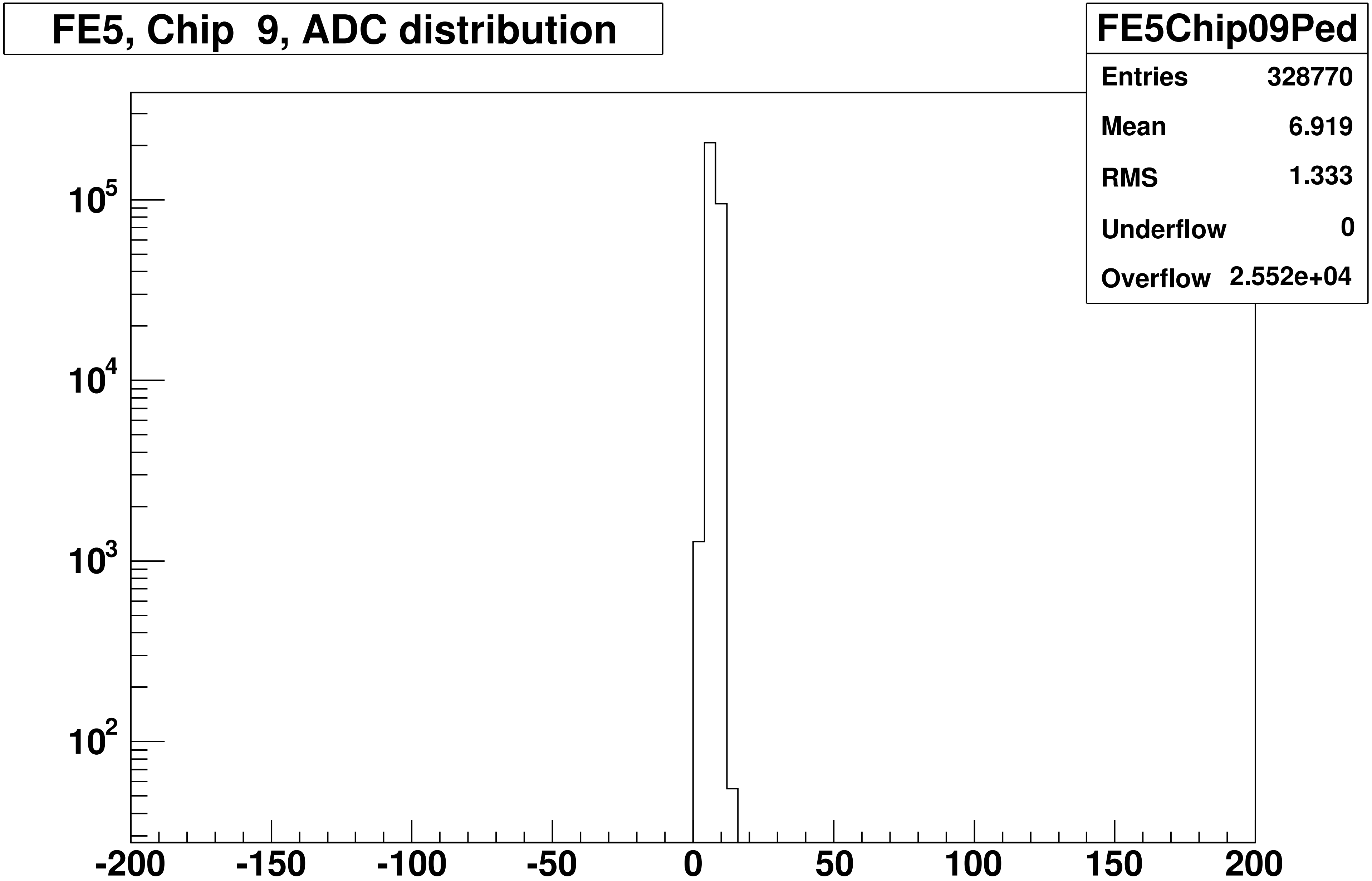
-50
0
50
100
150
200


FE5, Chip 8, ADC distribution
FE5Chip08Sig
Entries 328770
Mean 1.89e+04
RMS 13.09
Underflow 3.033e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE5, Chip 9, ADC distribution
FE5Chip09All
Entries 328770
Mean 1478
RMS 5074
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE5, Chip 9, ADC distribution
FE5Chip09Ped
Entries 328770
Mean 6.919
RMS 1.333
Underflow 0
Overflow 2.552e+04
10^5
10^4
10^3
10^2
-200
-150
-100
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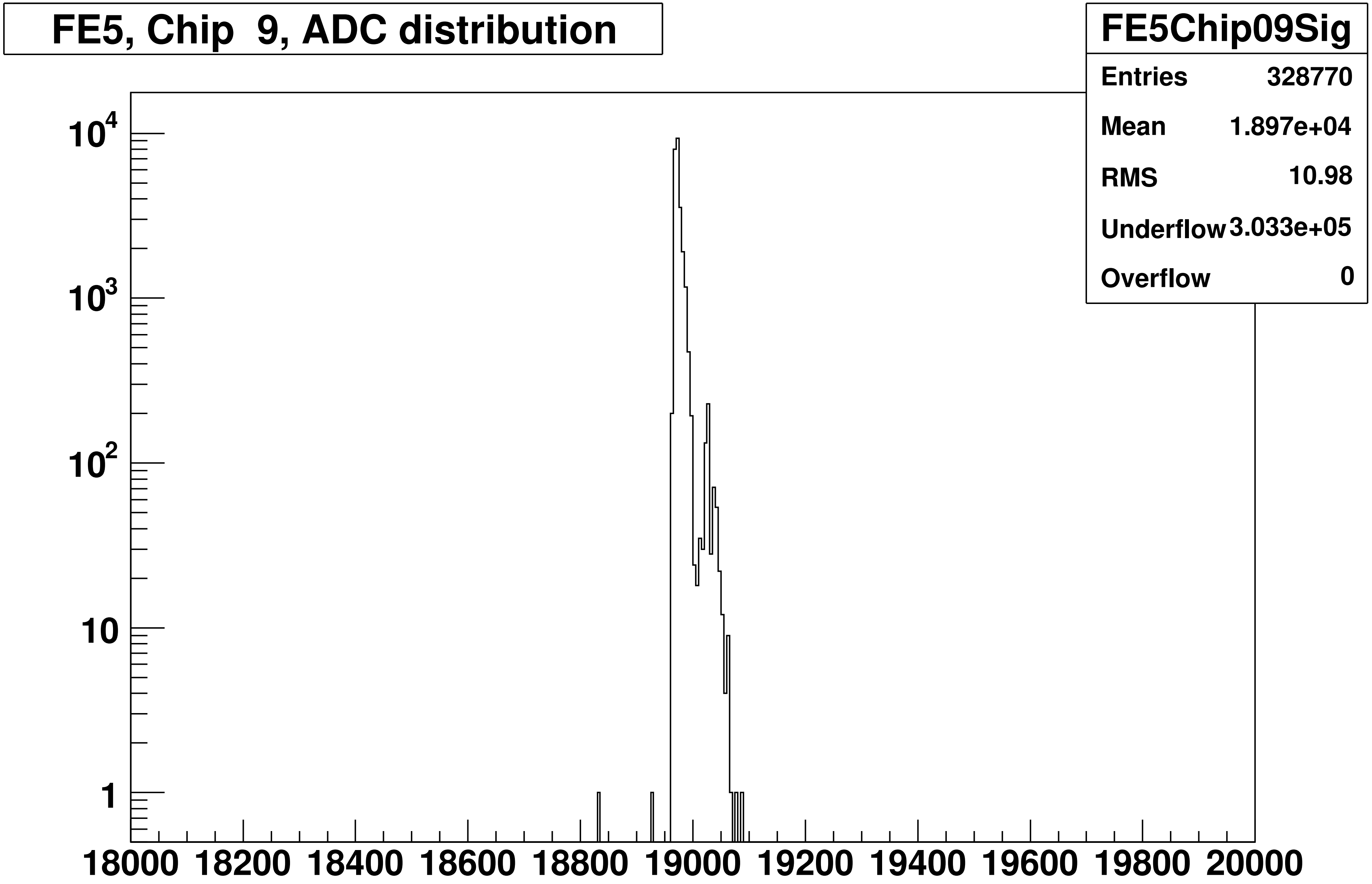
0
50
100
150
200



FE5, Chip 9, ADC distribution
FE5Chip09Sig
Entries 328770
Mean 1.897e+04
RMS 10.98
Underflow 3.033e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
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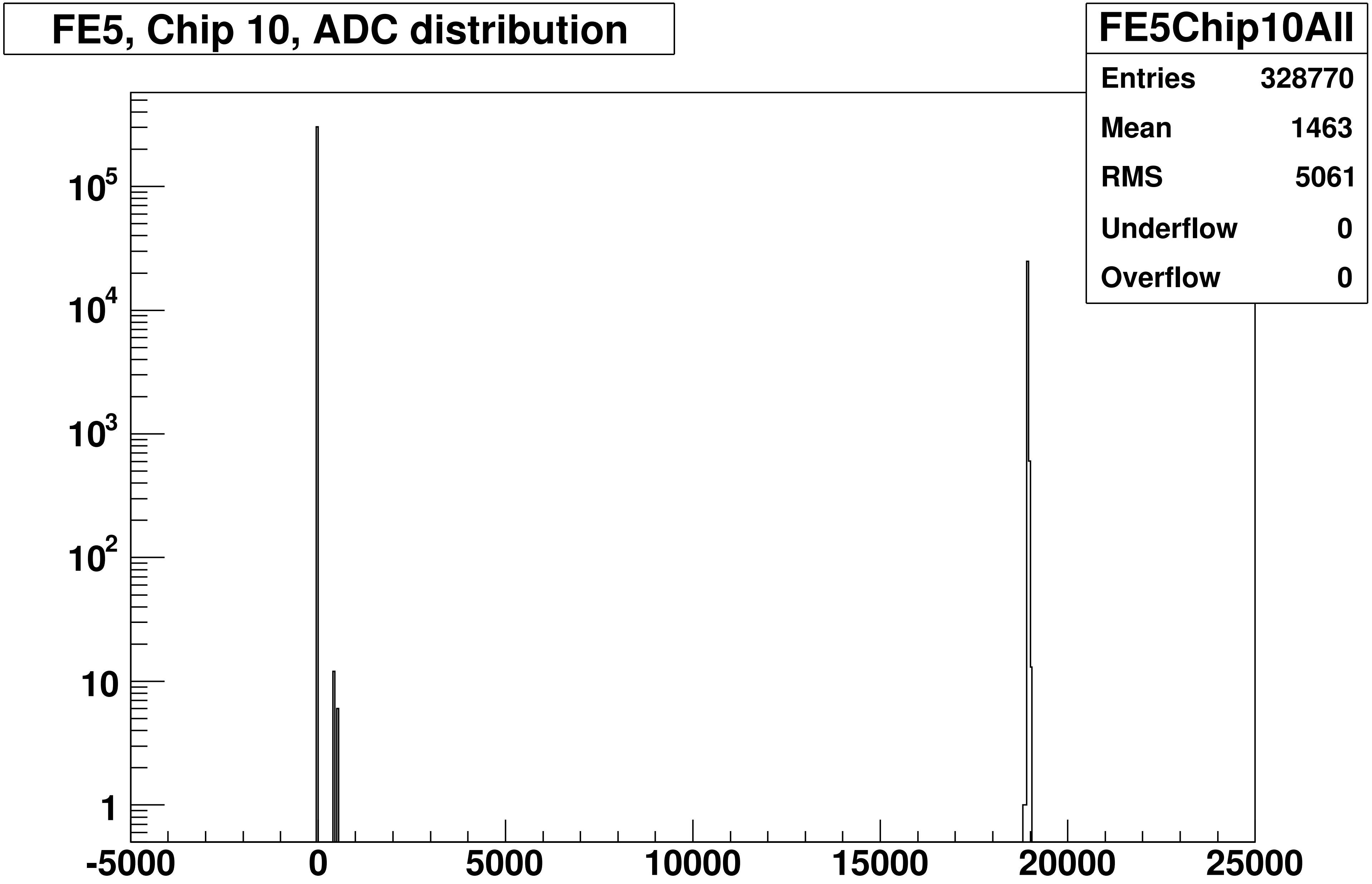
19400
19600
19800
20000



FE5, Chip 10, ADC distribution
FE5Chip10All
Entries 328770
Mean 1463
RMS 5061
Underflow 0
Overflow 0
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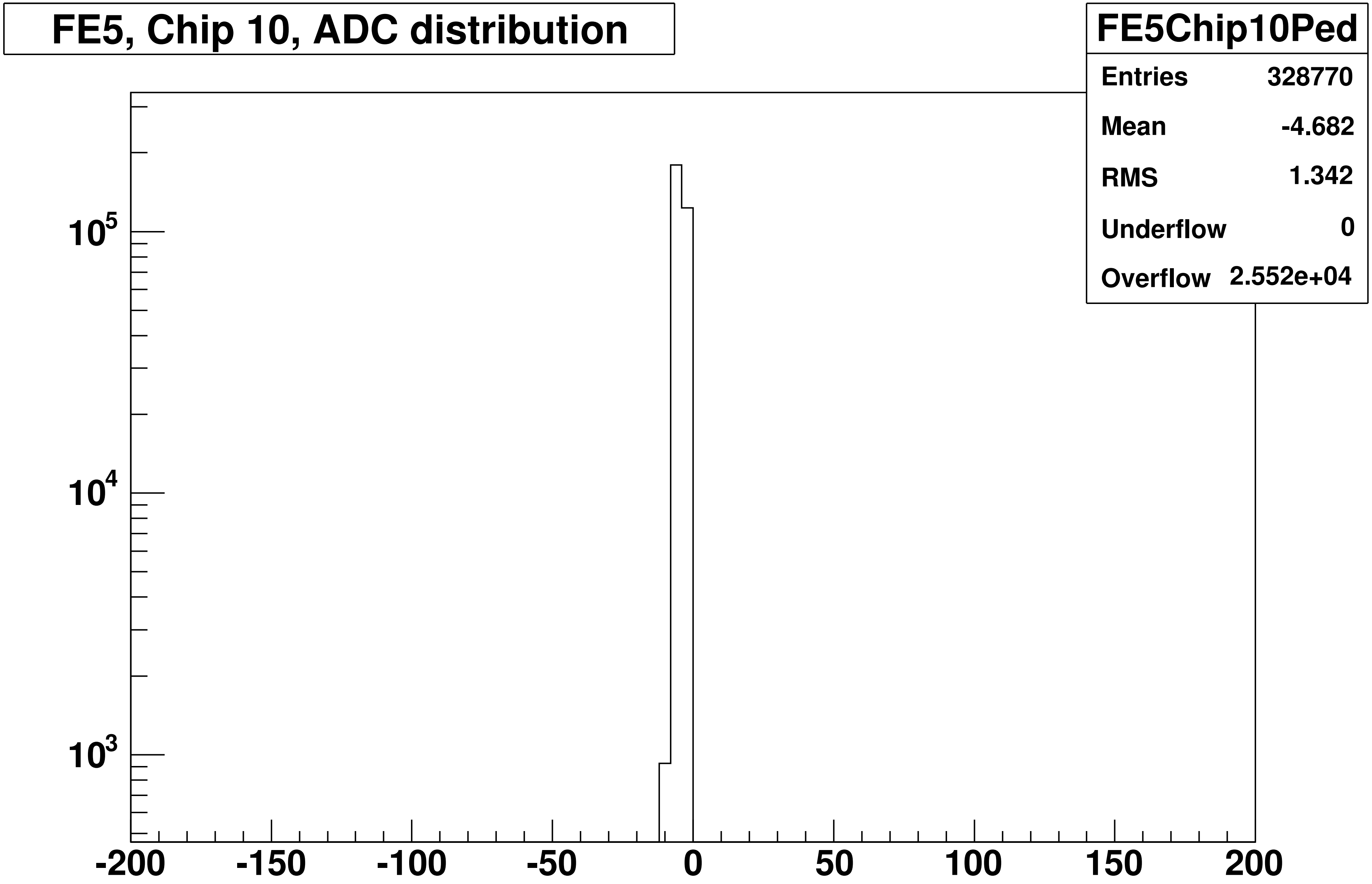
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE5, Chip 10, ADC distribution
FE5Chip10Ped
Entries 328770
Mean -4.682
RMS 1.342
Underflow 0
Overflow 2.552e+04
10^5
10^4
10^3
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-100
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0
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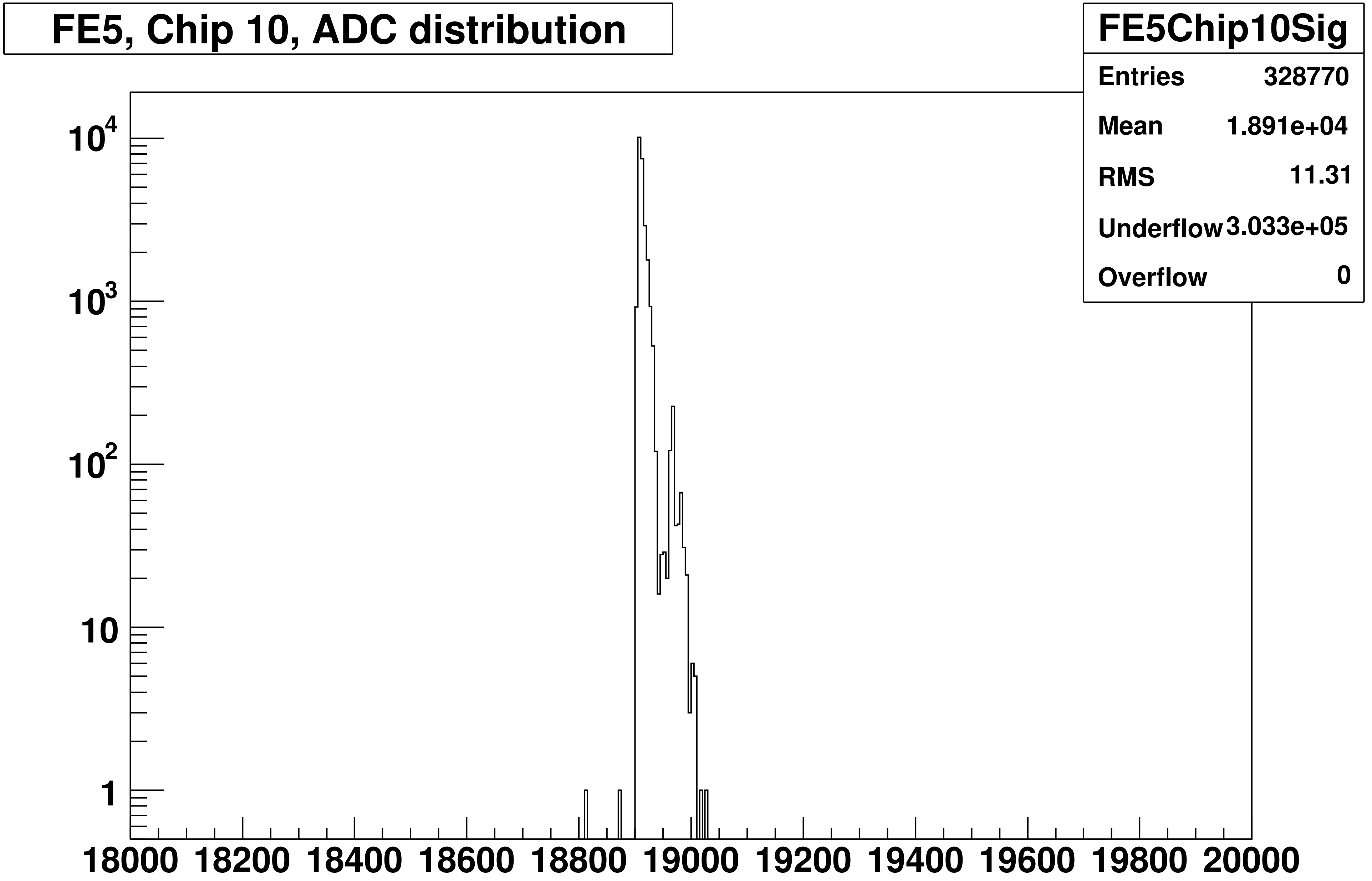
100
150
200


FE5, Chip 10, ADC distribution
FE5Chip10Sig
Entries 328770
Mean 1.891e+04
RMS 11.31
Underflow 3.033e+05
Overflow 0
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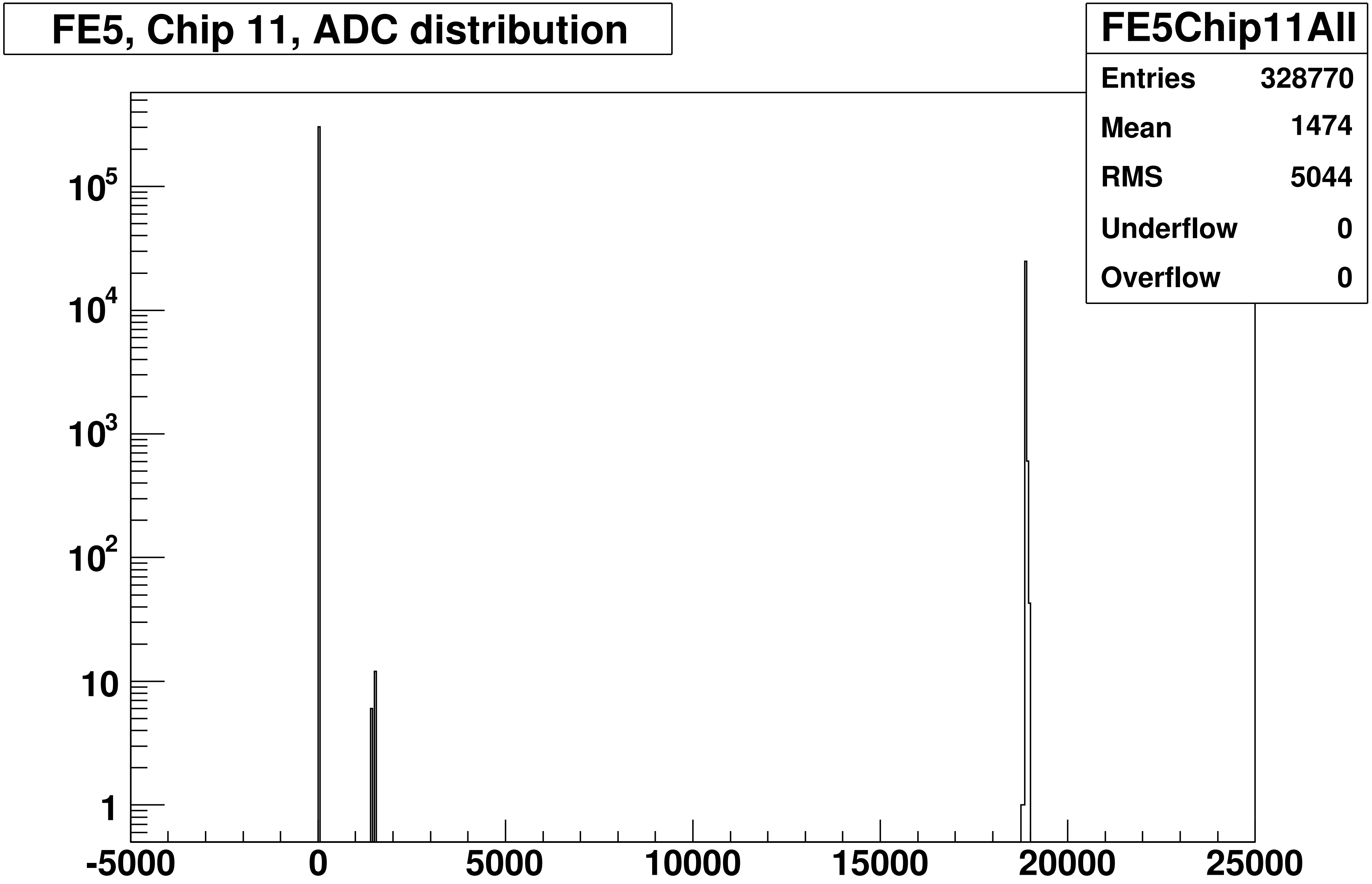
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE5, Chip 11, ADC distribution
FE5Chip11All
Entries 328770
Mean 1474
RMS 5044
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
1
-5000
0
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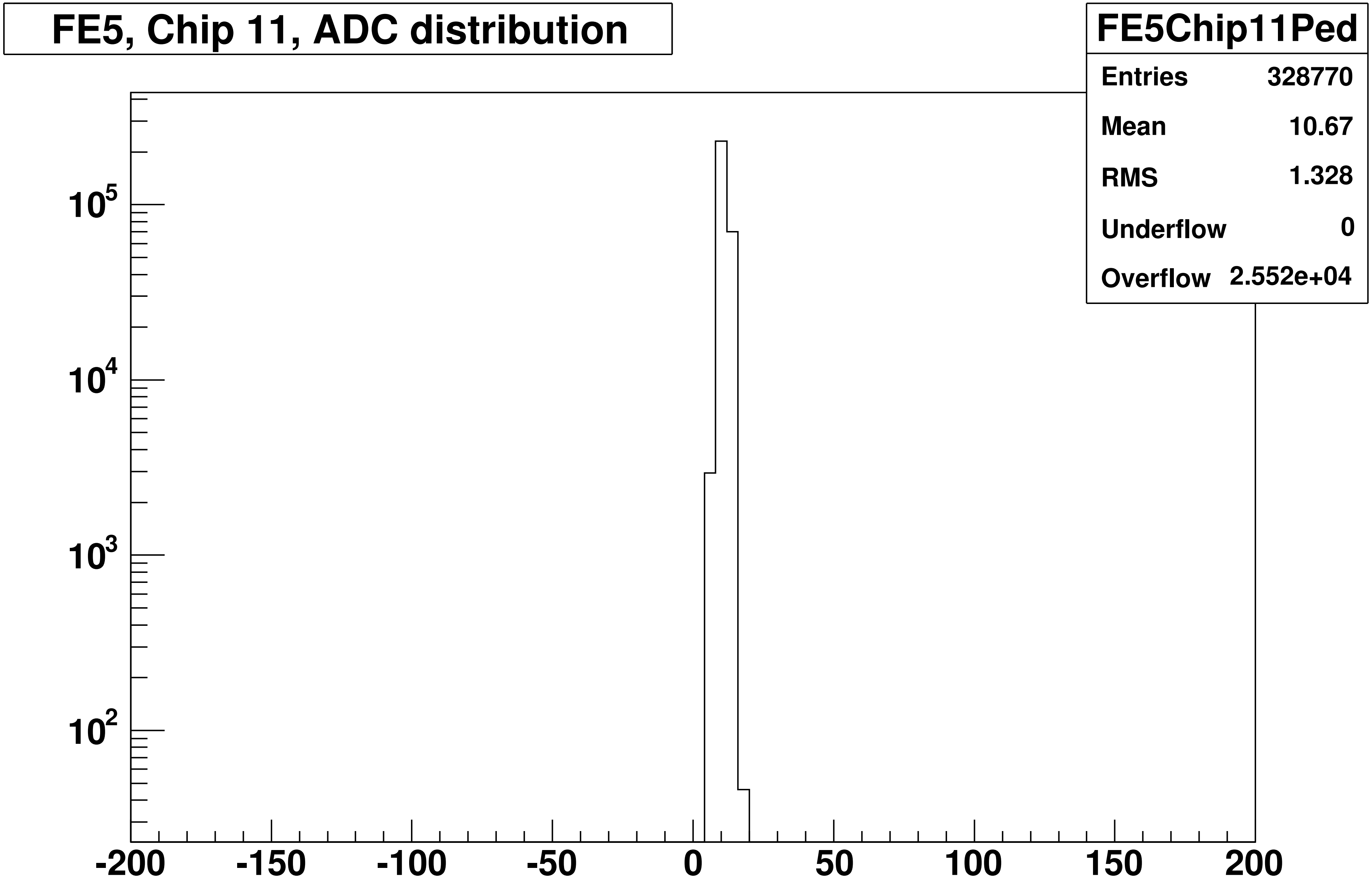
10000
15000
20000
25000



FE5, Chip 11, ADC distribution
FE5Chip11Ped
Entries 328770
Mean 10.67
RMS 1.328
Underflow 0
Overflow 2.552e+04
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10^4
10^3
10^2
-200
-150
-100
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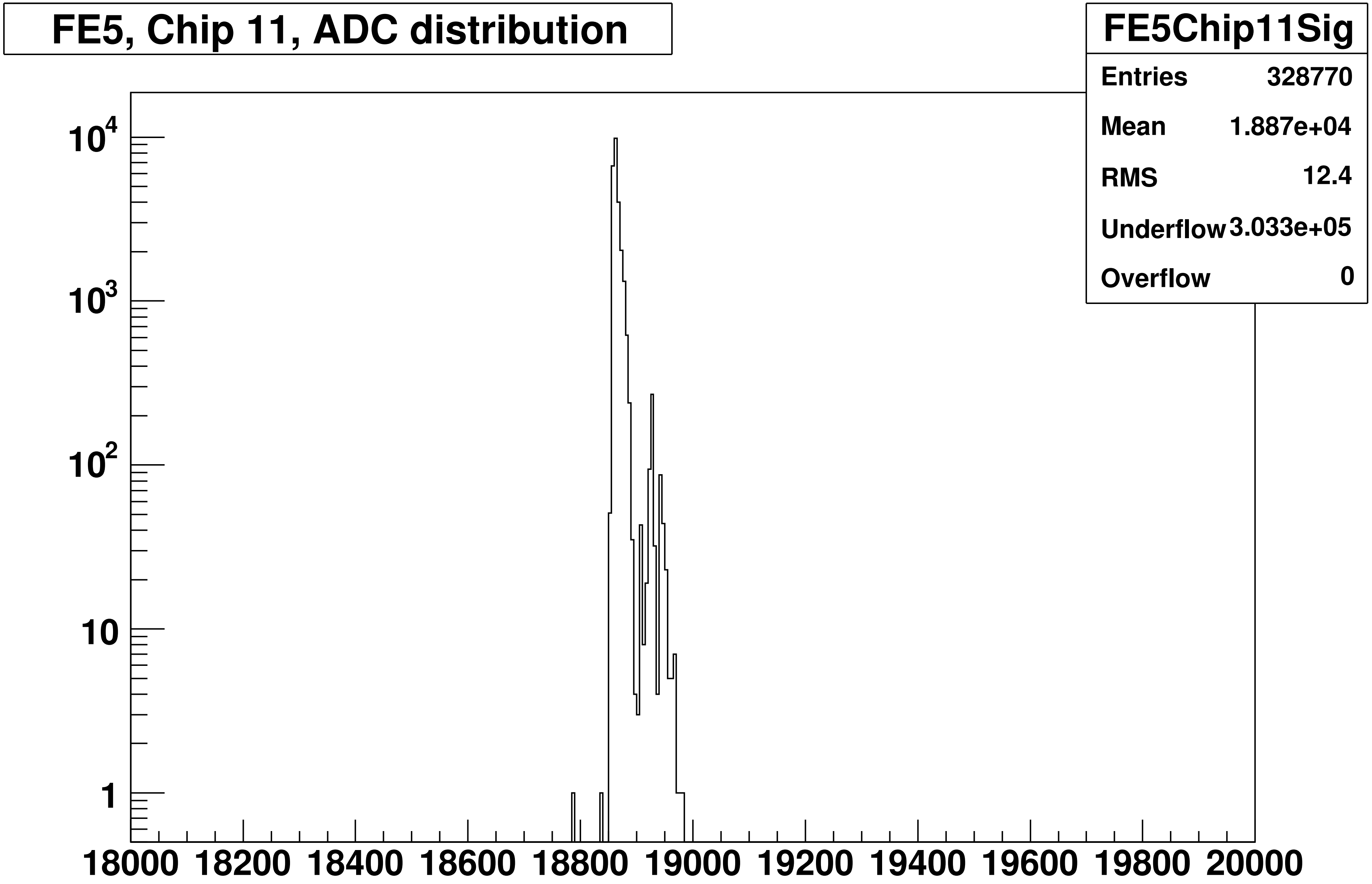
0
50
100
150
200


FE5, Chip 11, ADC distribution
FE5Chip11Sig
Entries 328770
Mean 1.887e+04
RMS 12.4
Underflow 3.033e+05
Overflow 0
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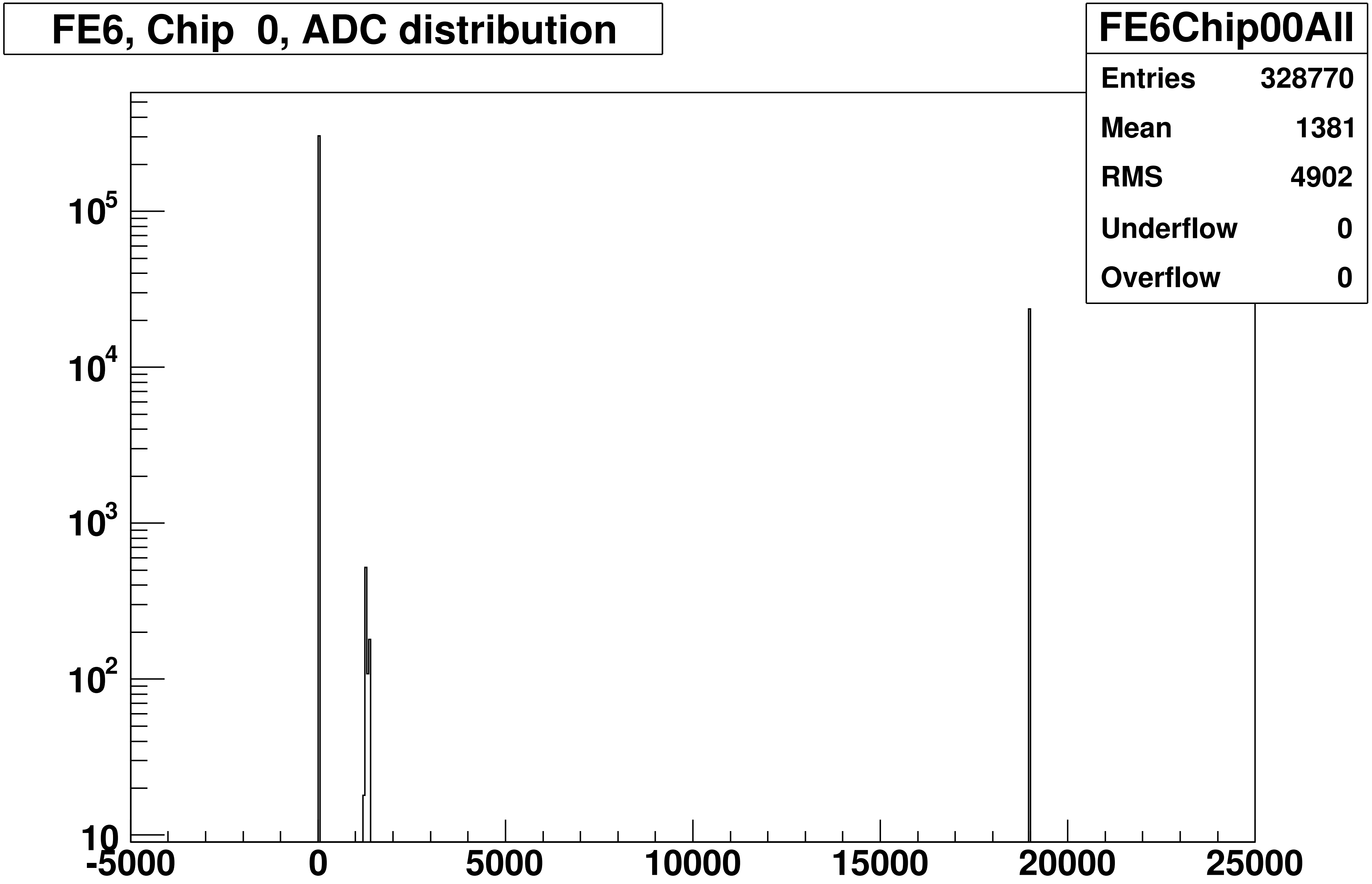
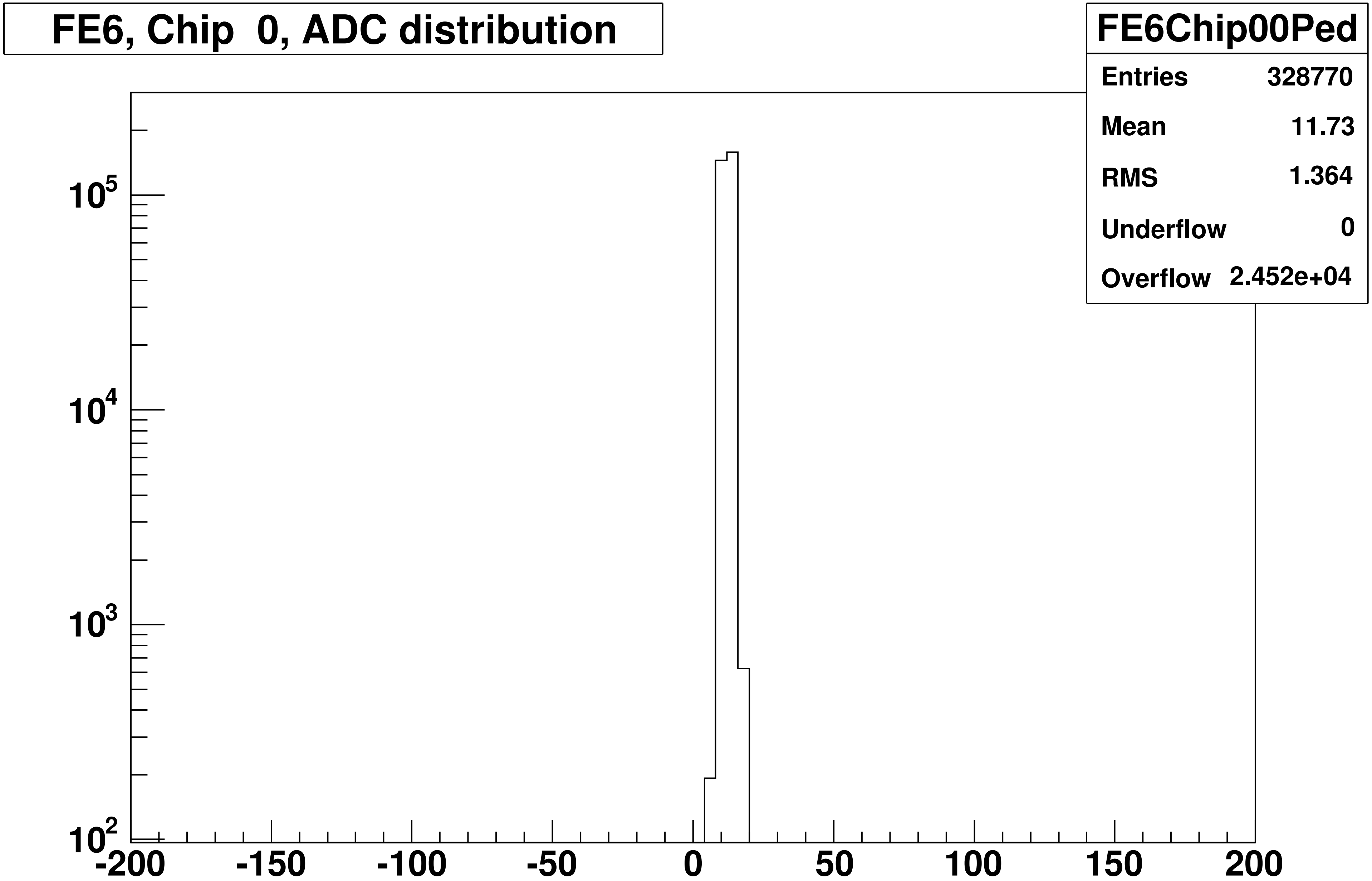
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE6, Chip 0, ADC distribution
FE6Chip00All
Entries 328770
Mean 1381
RMS 4902
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE6, Chip 0, ADC distribution
FE6Chip00Ped
Entries 328770
Mean 11.73
RMS 1.364
Underflow 0
Overflow 2.452e+04
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10^4
10^3
10^2
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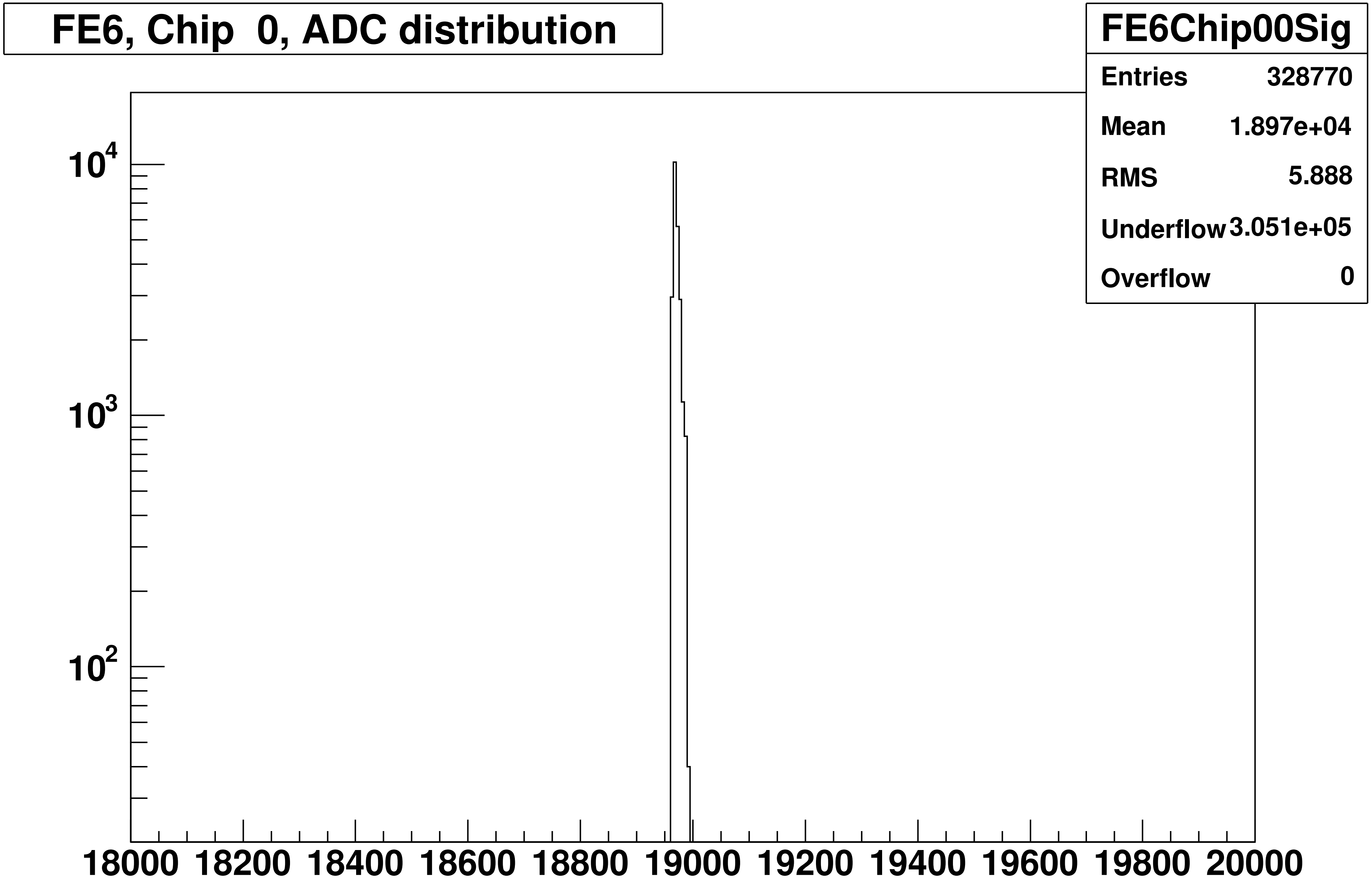
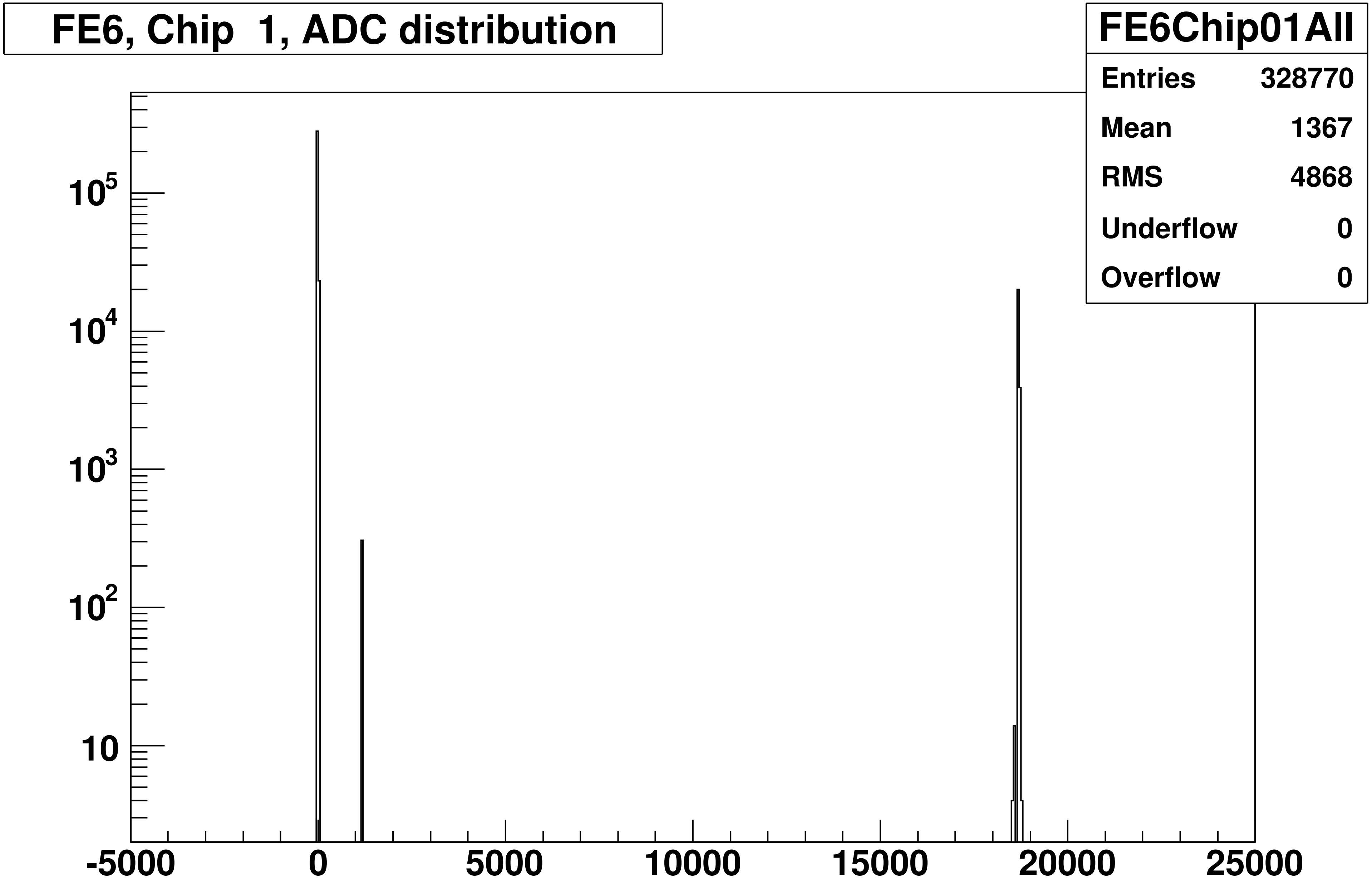
-150
-100
-50
0
50
100
150
200


FE6, Chip 0, ADC distribution
FE6Chip00Sig
Entries 328770
Mean 1.897e+04
RMS 5.888
Underflow 3.051e+05
Overflow 0
10^4
10^3
10^2
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE6, Chip 1, ADC distribution
FE6Chip01All
Entries 328770
Mean 1367
RMS 4868
Underflow 0
Overflow 0
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10^4
10^3
10^2
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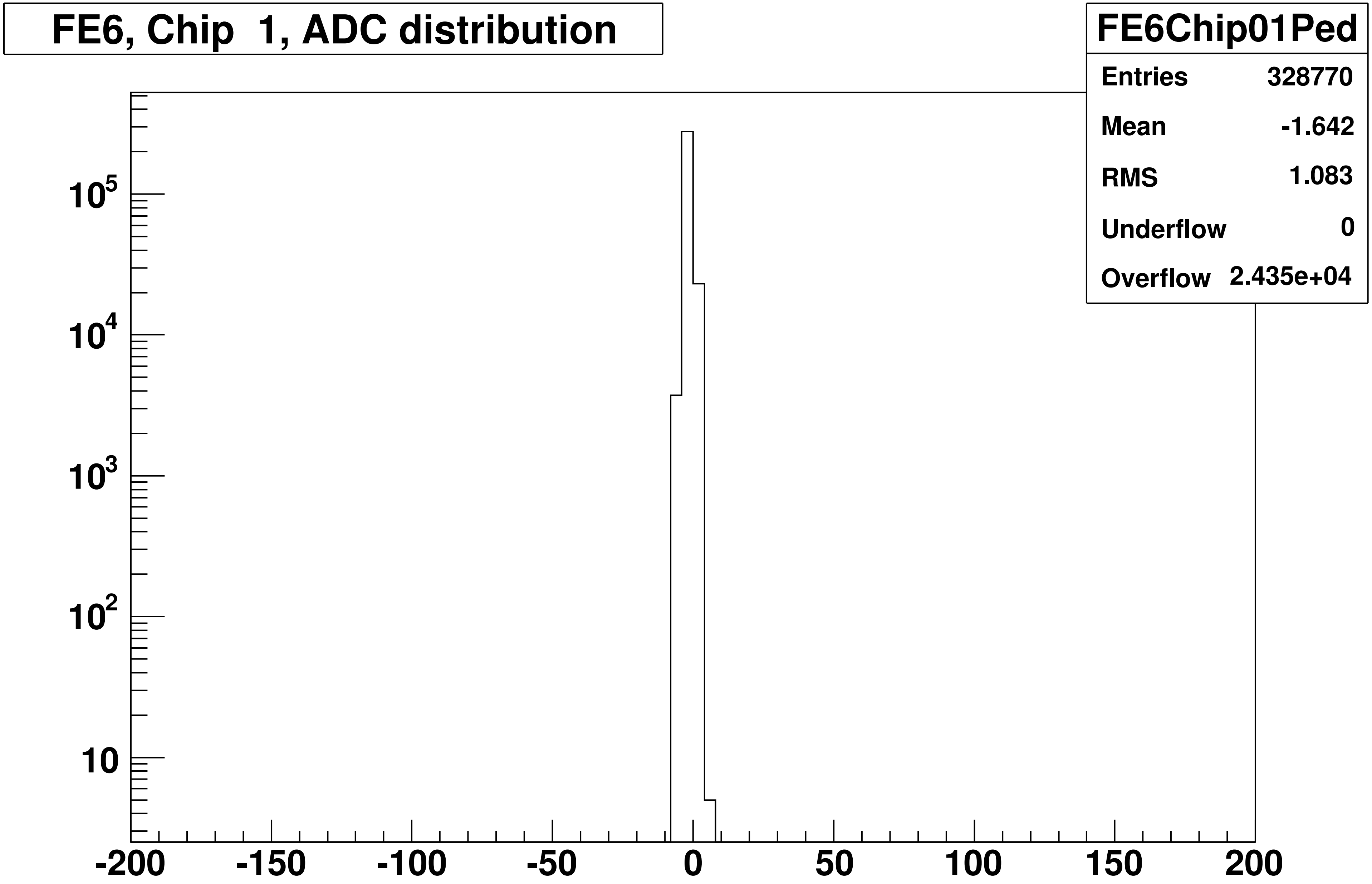
20000
25000


FE6, Chip 1, ADC distribution
FE6Chip01Ped
Entries 328770
Mean -1.642
RMS 1.083
Underflow 0
Overflow 2.435e+04
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10^4
10^3
10^2
10
-200
-150
-100
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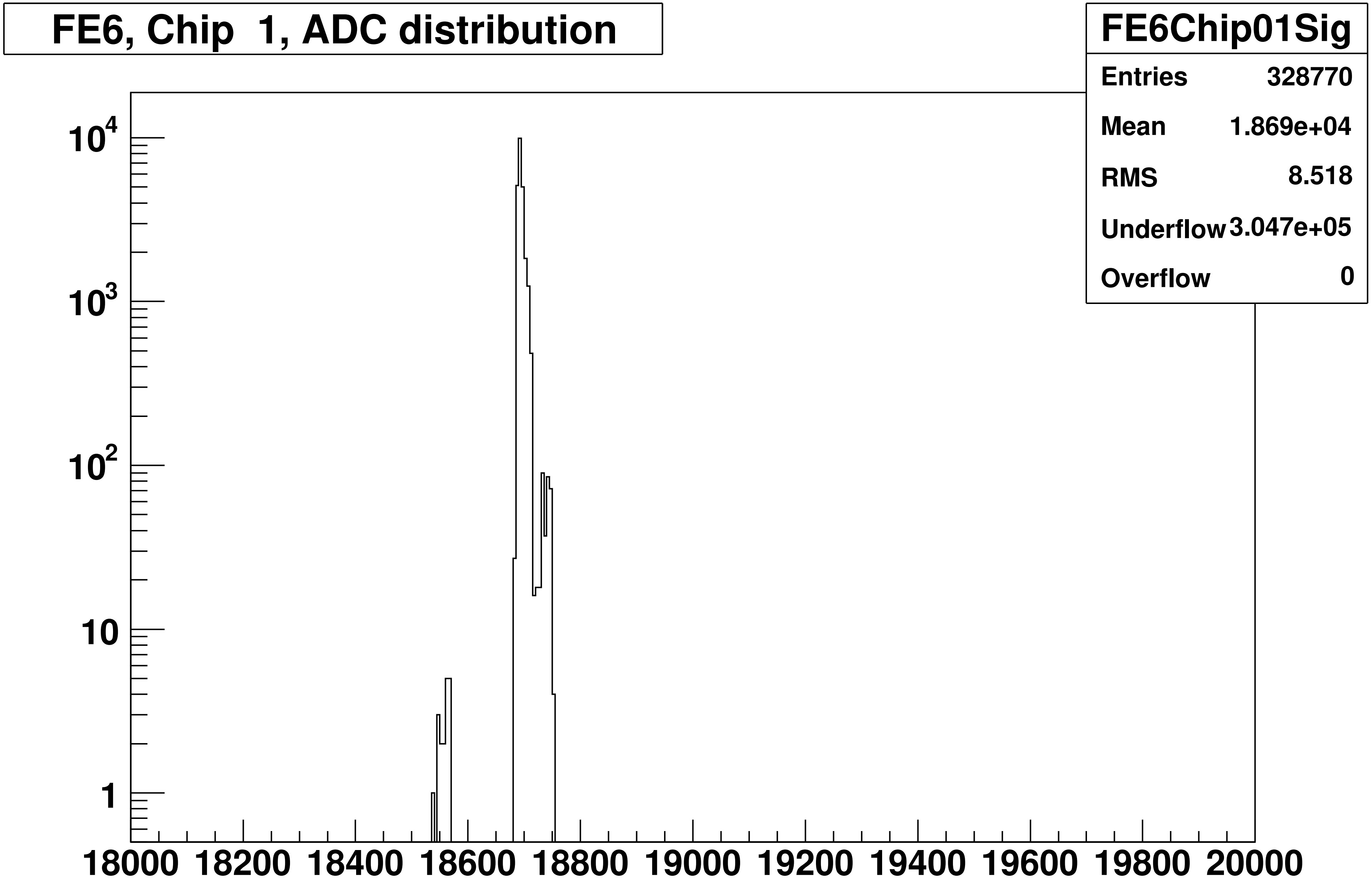
50
100
150
200


FE6, Chip 1, ADC distribution
FE6Chip01Sig
Entries 328770
Mean 1.869e+04
RMS 8.518
Underflow 3.047e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
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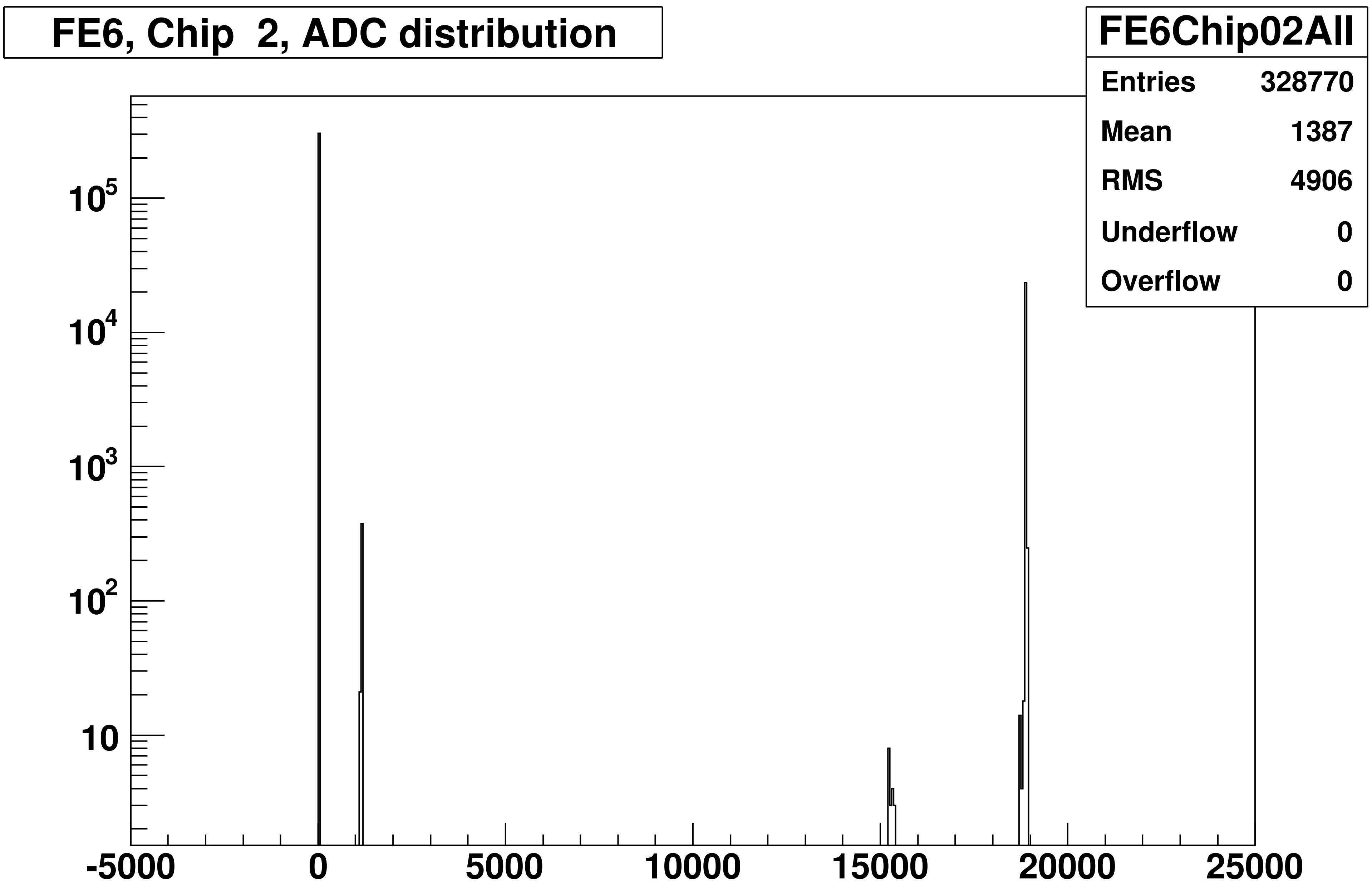
19400
19600
19800
20000



FE6, Chip 2, ADC distribution
FE6Chip02All
Entries 328770
Mean 1387
RMS 4906
Underflow 0
Overflow 0
10
10^2
10^3
10^4
10^5
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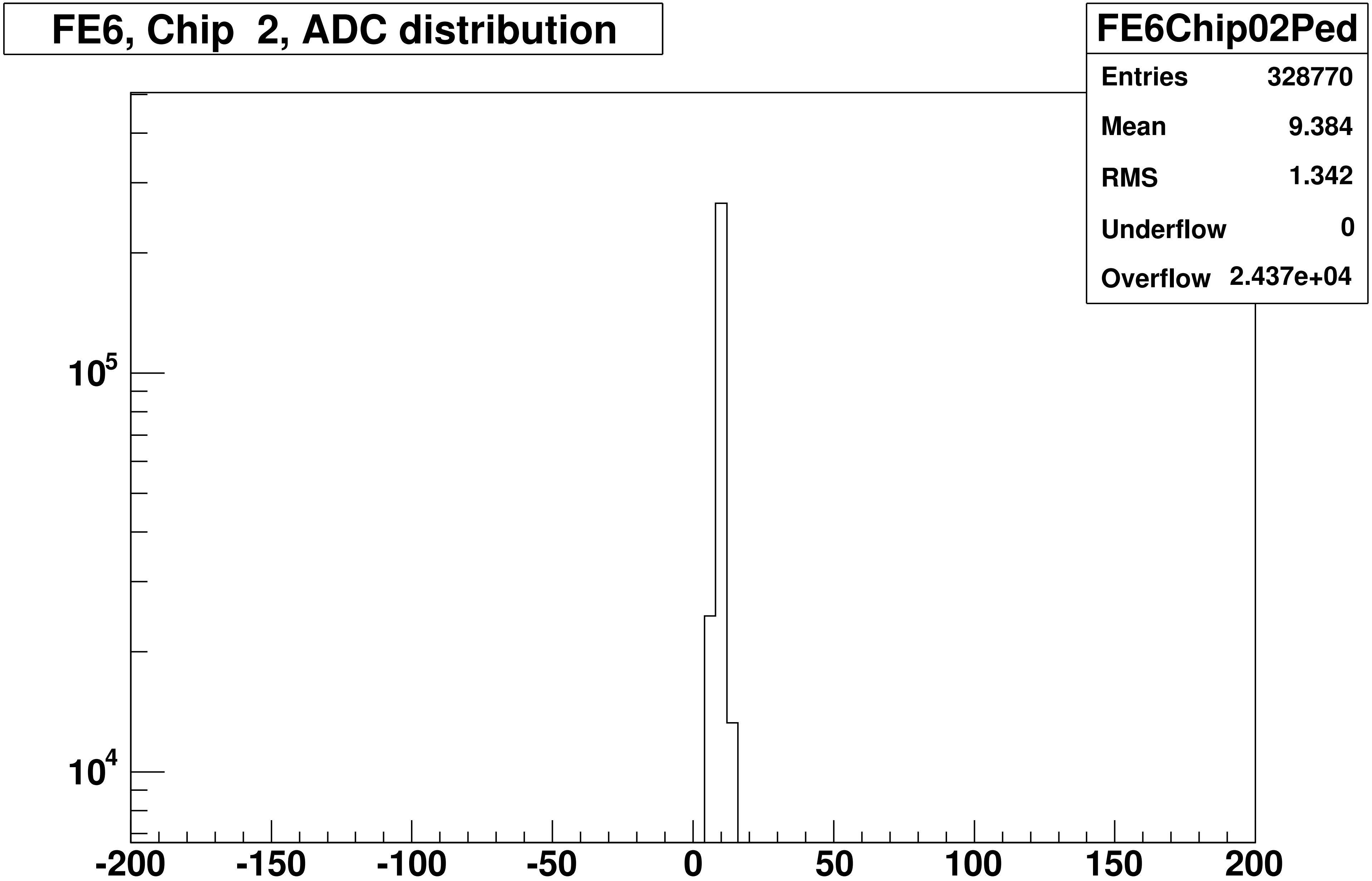
0
5000
10000
15000
20000
25000


FE6, Chip 2, ADC distribution
FE6Chip02Ped
Entries 328770
Mean 9.384
RMS 1.342
Underflow 0
Overflow 2.437e+04
10^5
10^4
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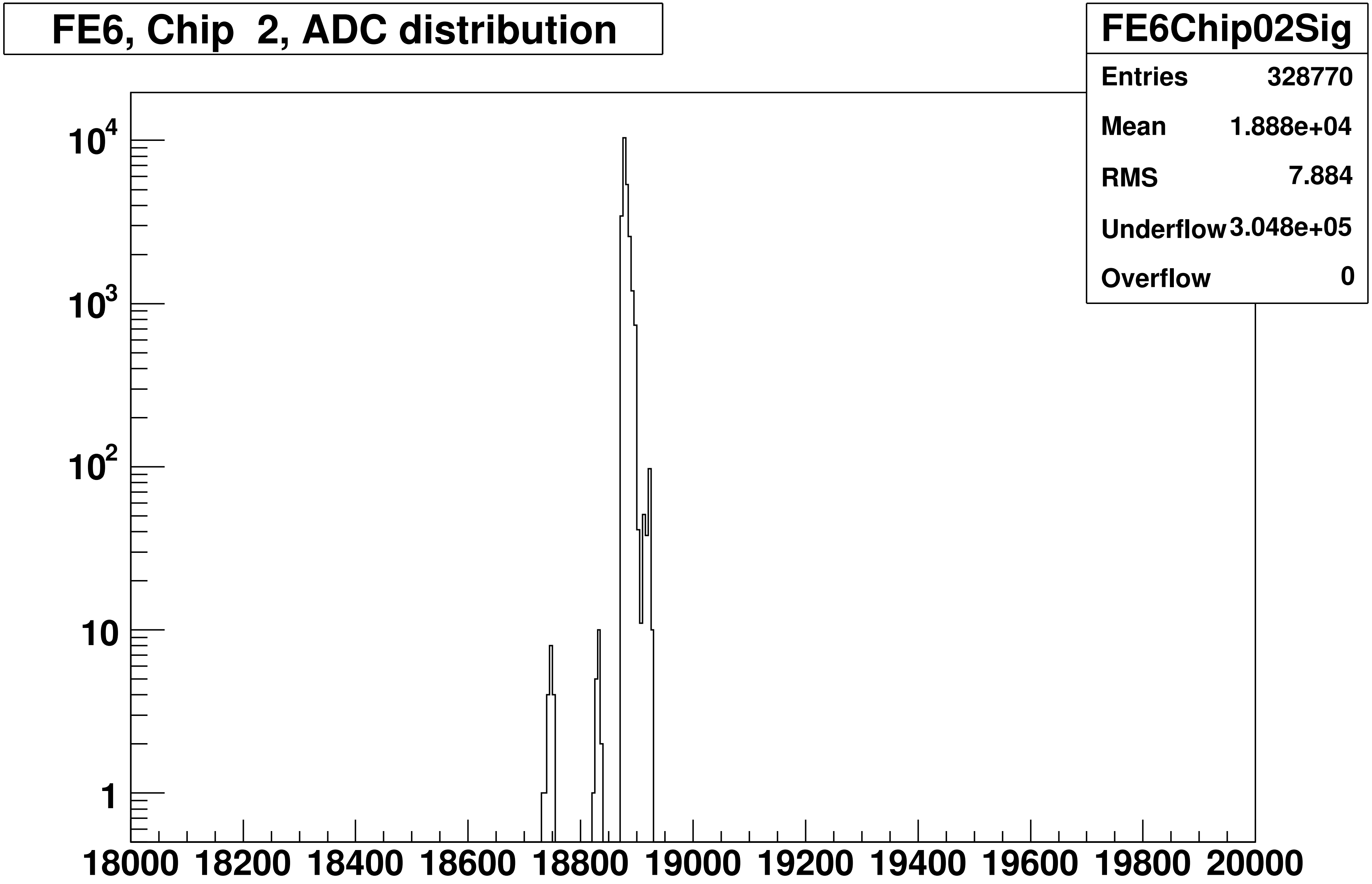
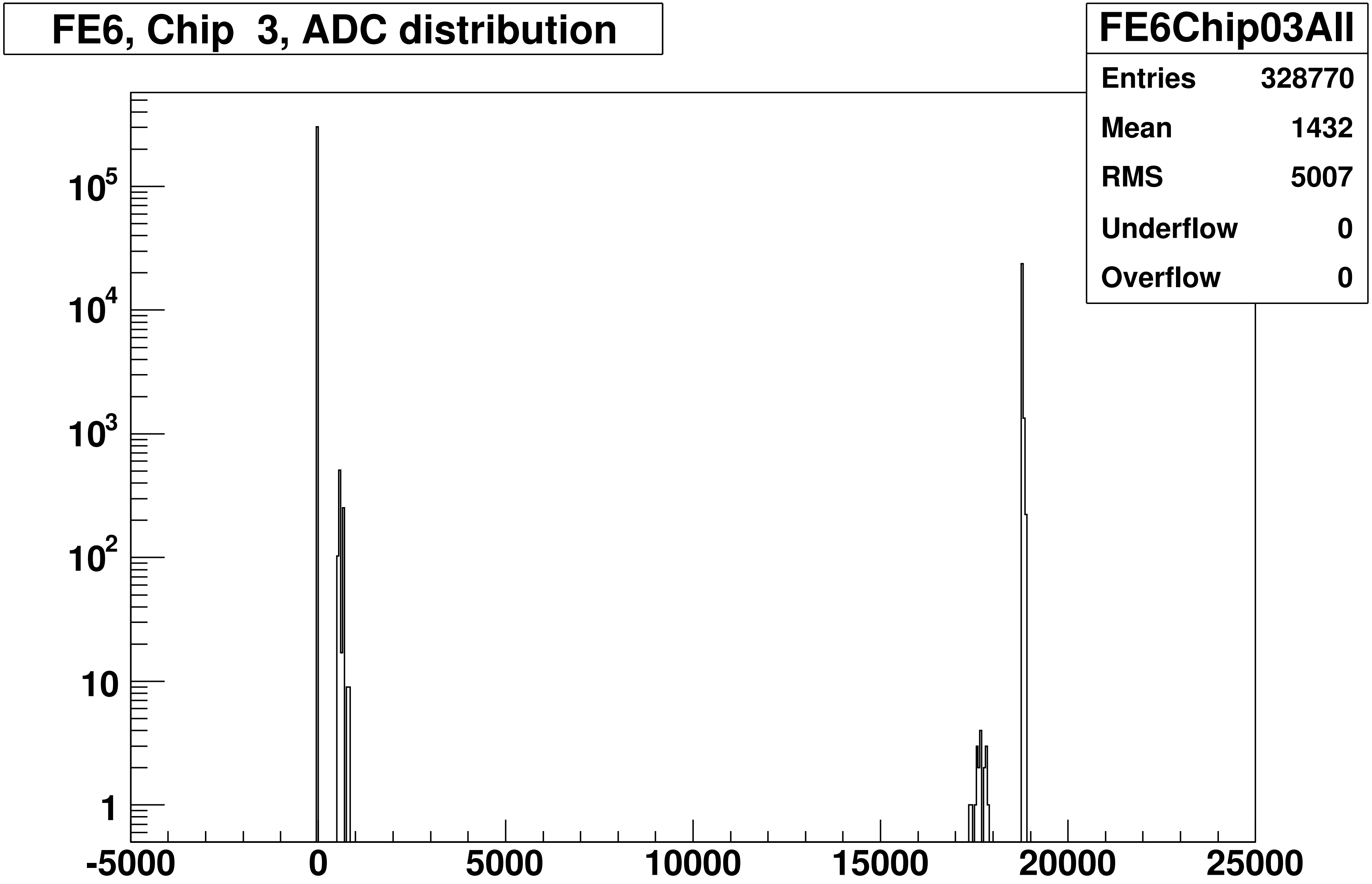
-150
-100
-50
0
50
100
150
200


FE6, Chip 2, ADC distribution
FE6Chip02Sig
Entries 328770
Mean 1.888e+04
RMS 7.884
Underflow 3.048e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE6, Chip 3, ADC distribution
FE6Chip03All
Entries 328770
Mean 1432
RMS 5007
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
1
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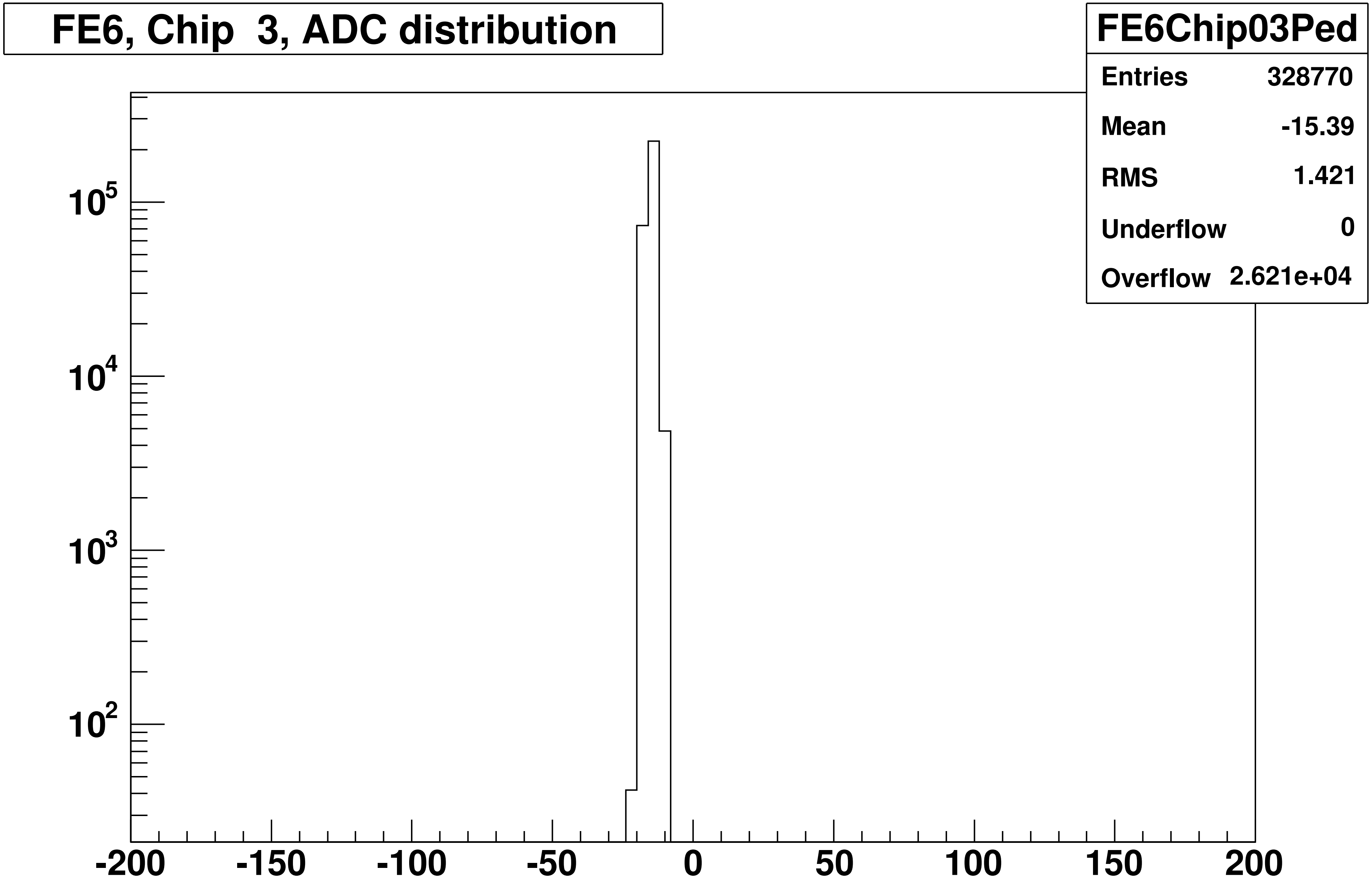
25000


FE6, Chip 3, ADC distribution
FE6Chip03Ped
Entries 328770
Mean -15.39
RMS 1.421
Underflow 0
Overflow 2.621e+04
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10^4
10^3
10^2
-200
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-100
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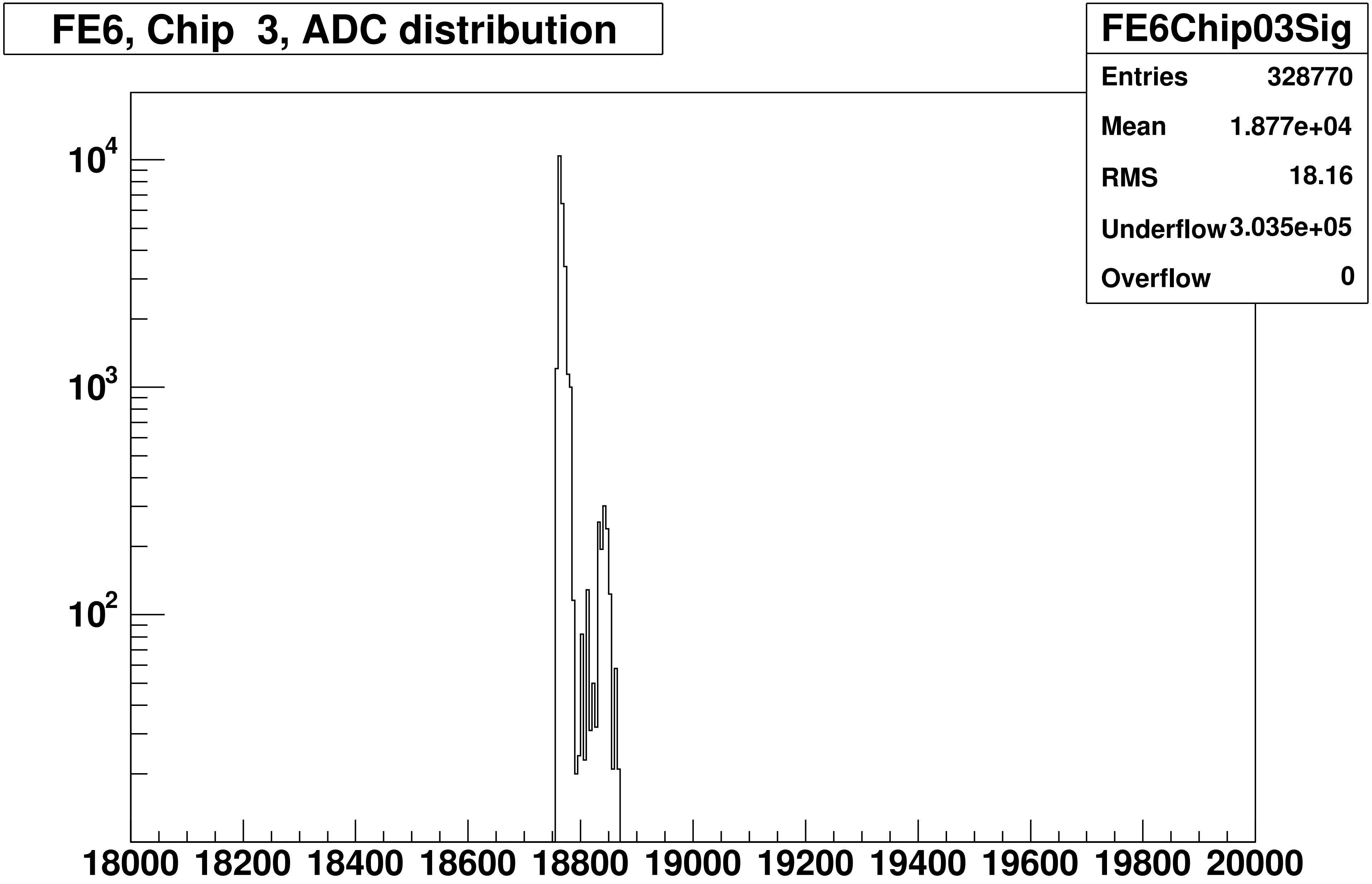
150
200


FE6, Chip 3, ADC distribution
FE6Chip03Sig
Entries 328770
Mean 1.877e+04
RMS 18.16
Underflow 3.035e+05
Overflow 0
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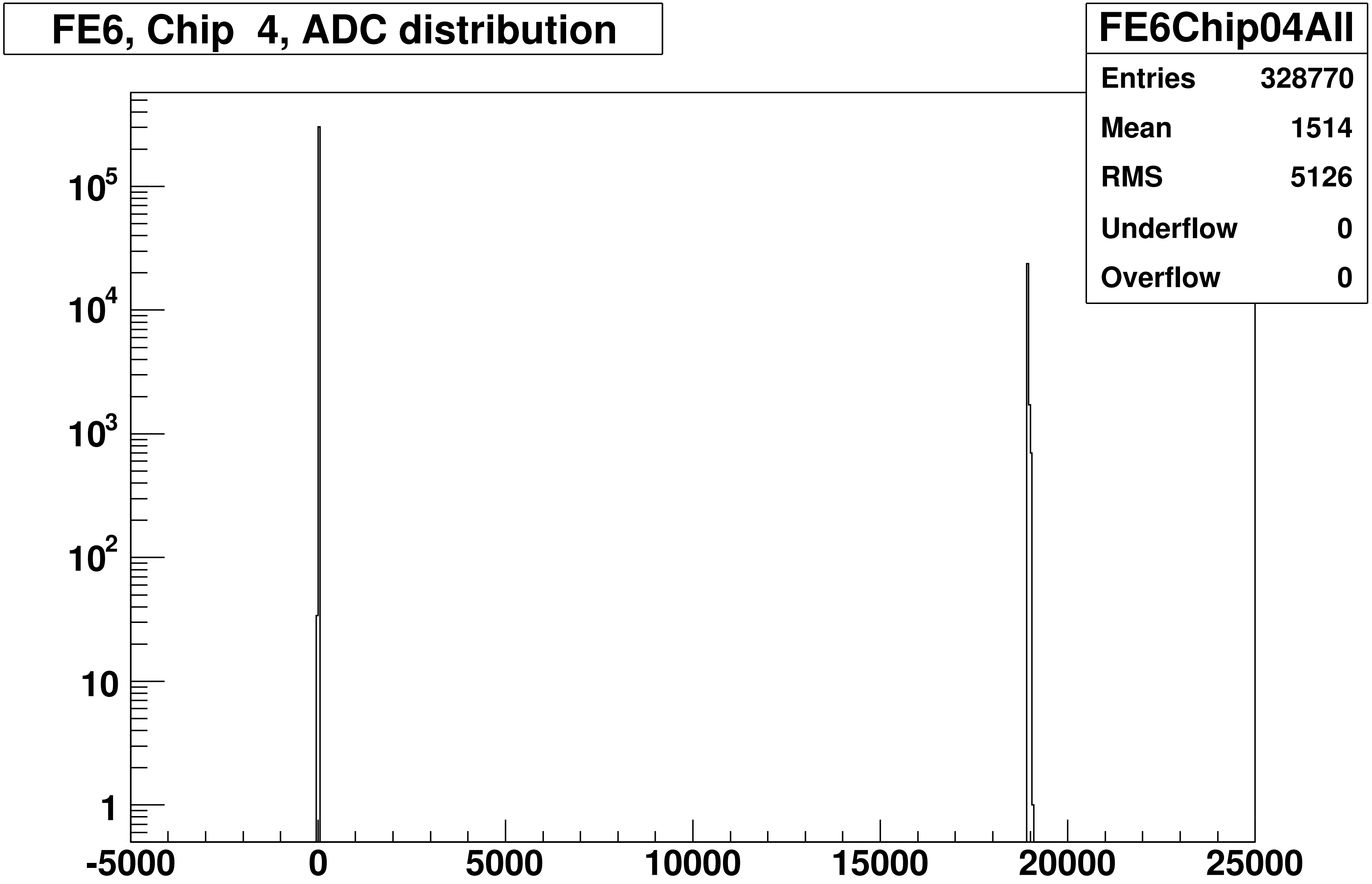
10^3
10^2
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE6, Chip 4, ADC distribution
FE6Chip04All
Entries 328770
Mean 1514
RMS 5126
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
1
-5000
0
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20000
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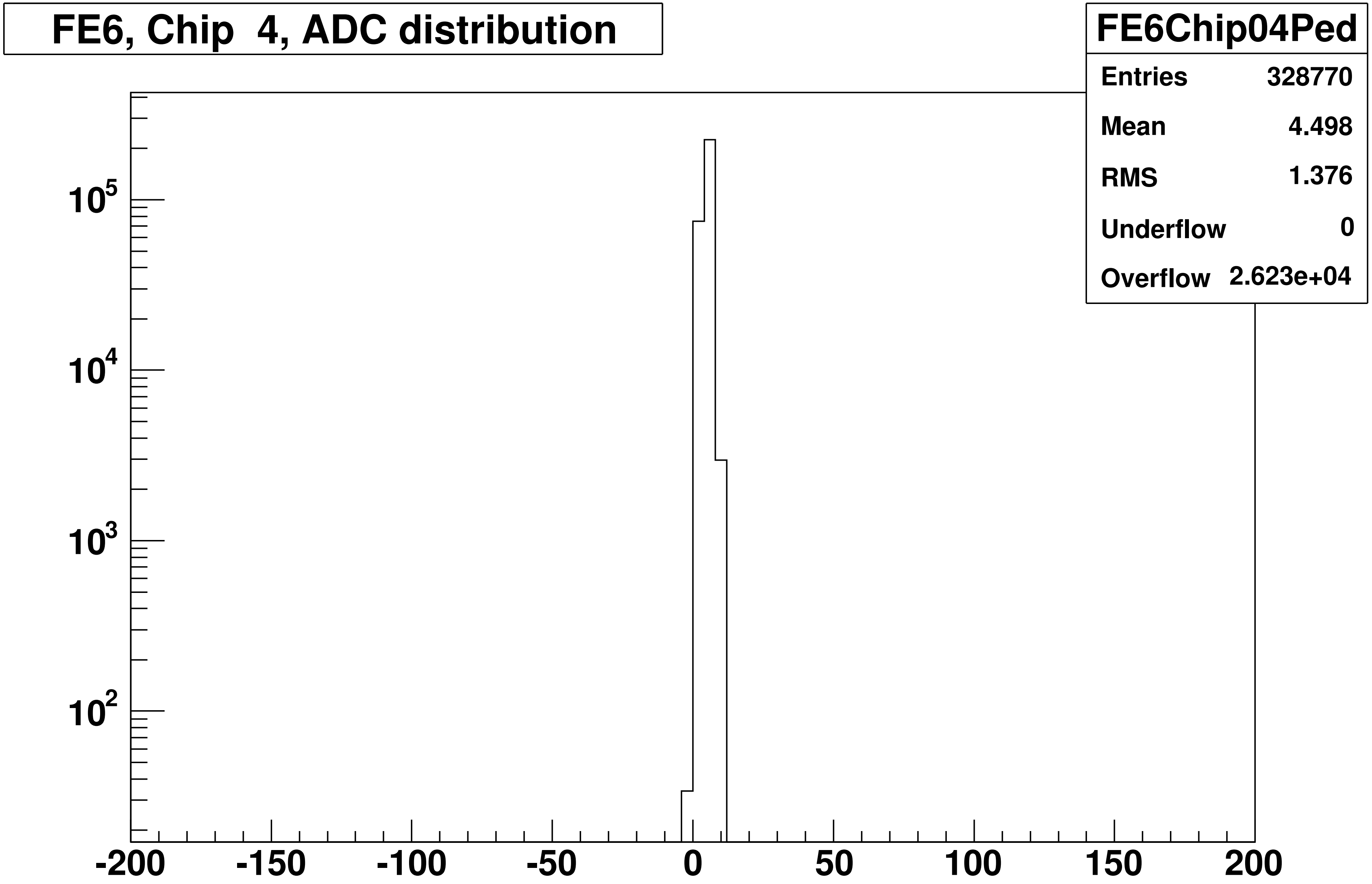
FE6, Chip 4, ADC distribution
FE6Chip04Ped
Entries 328770
Mean 4.498
RMS 1.376
Underflow 0
Overflow 2.623e+04
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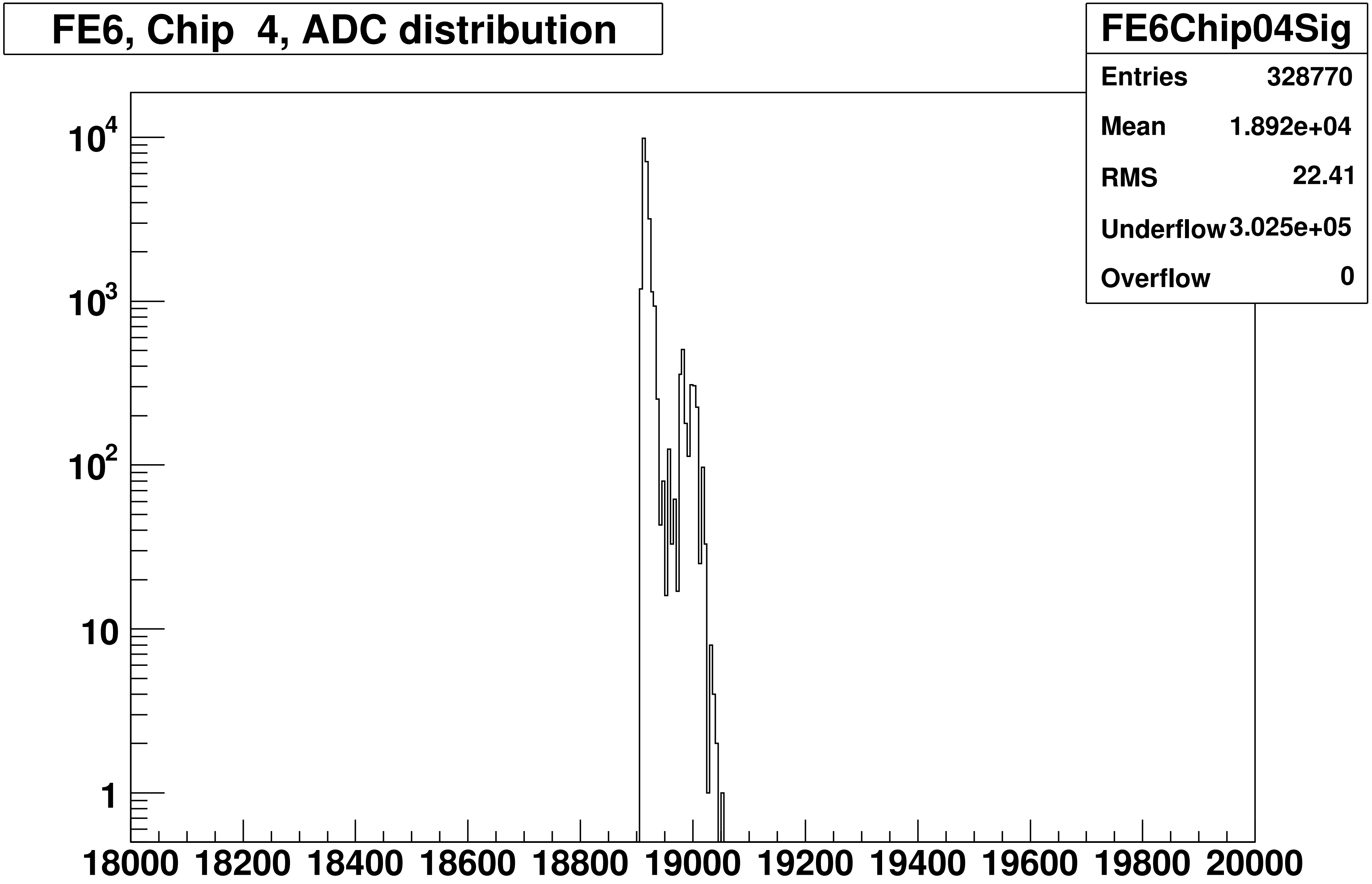
10^4
10^3
10^2
-200
-150
-100
-50
0
50
100
150
200


FE6, Chip 4, ADC distribution
FE6Chip04Sig
Entries 328770
Mean 1.892e+04
RMS 22.41
Underflow 3.025e+05
Overflow 0
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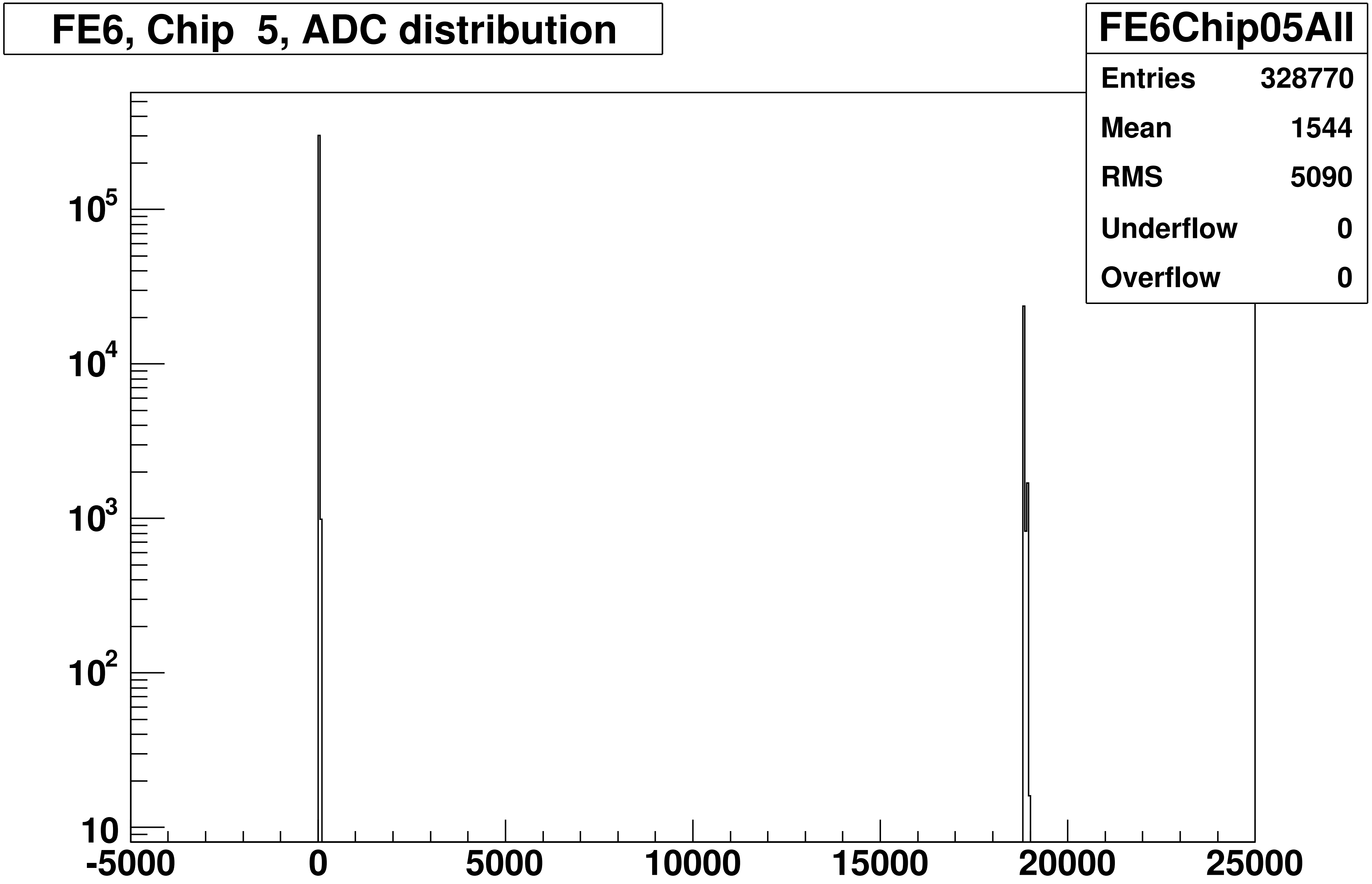
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE6, Chip 5, ADC distribution
FE6Chip05All
Entries 328770
Mean 1544
RMS 5090
Underflow 0
Overflow 0
10
10^2
10^3
10^4
10^5
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0
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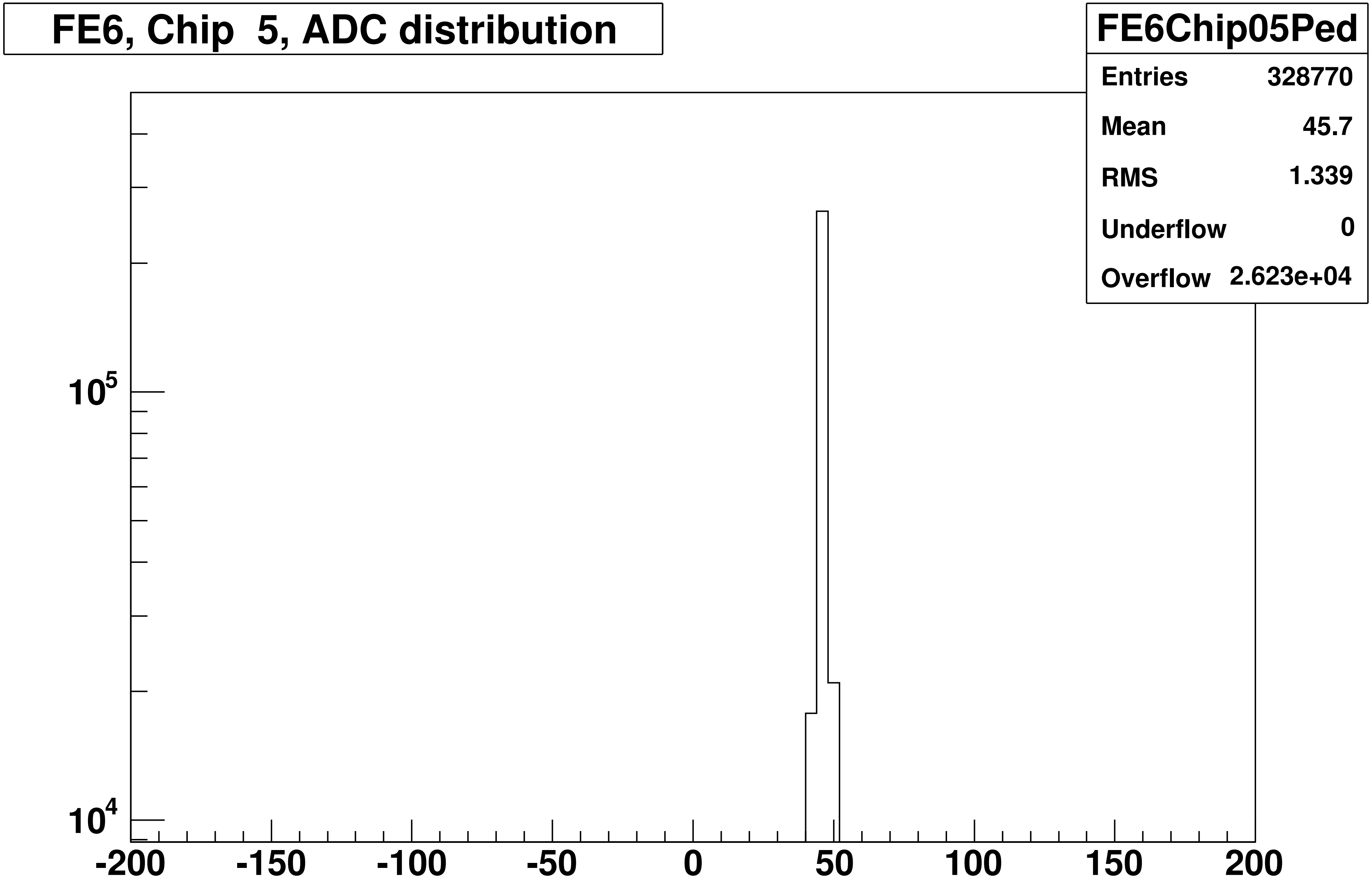
20000
25000



FE6, Chip 5, ADC distribution
FE6Chip05Ped
Entries 328770
Mean 45.7
RMS 1.339
Underflow 0
Overflow 2.623e+04
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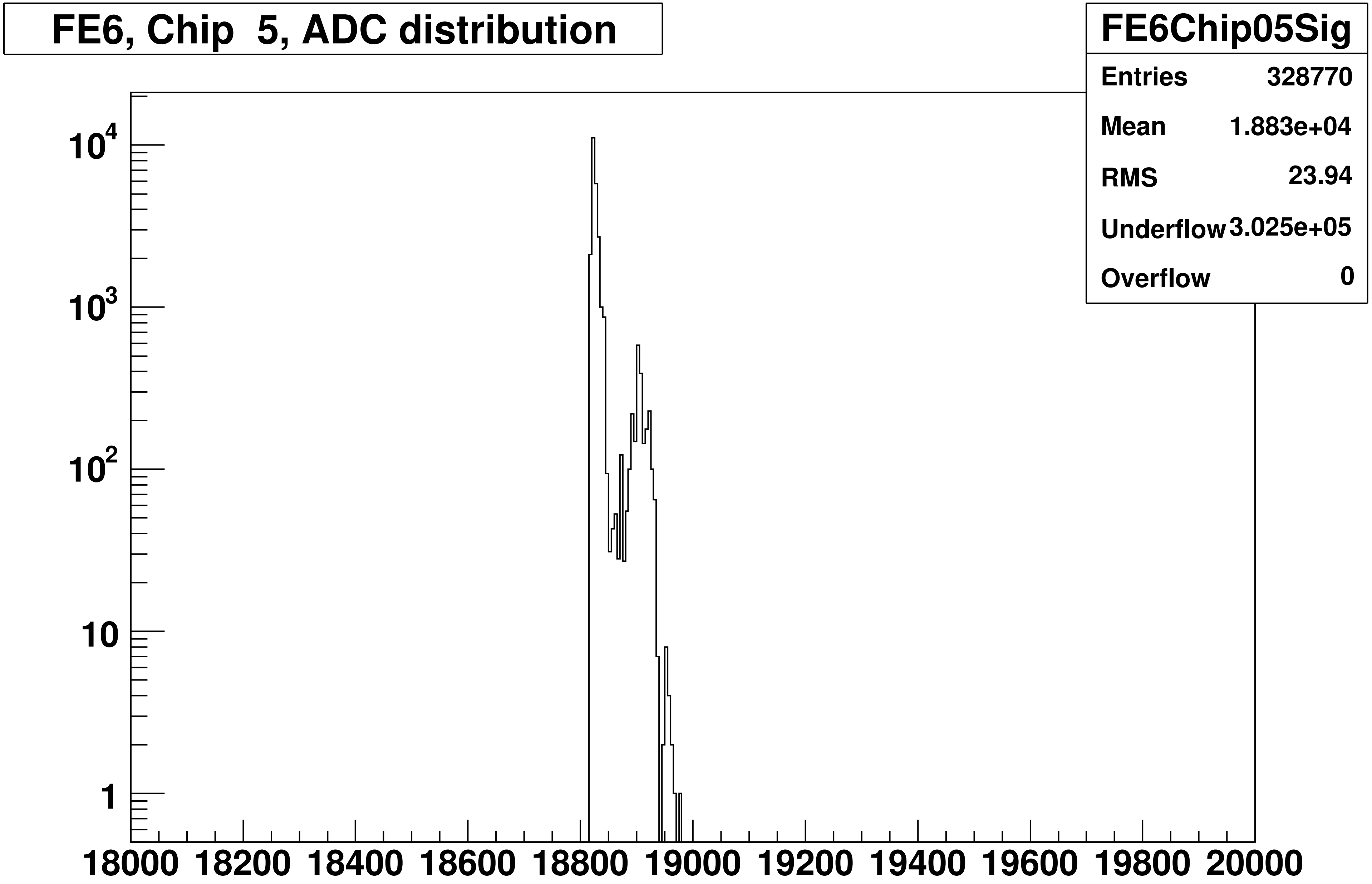
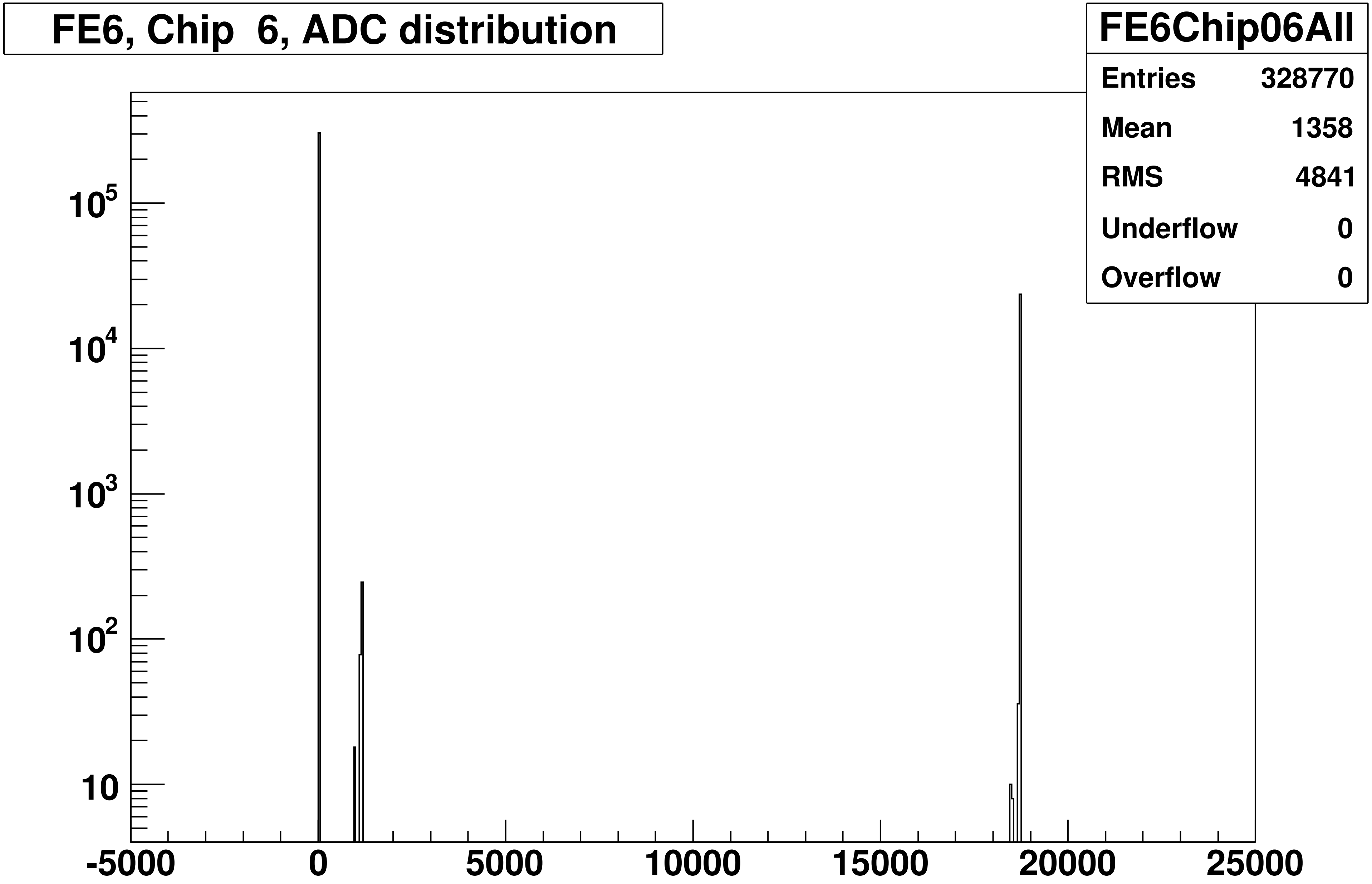
10^4
-200
-150
-100
-50
0
50
100
150
200



FE6, Chip 5, ADC distribution
FE6Chip05Sig
Entries 328770
Mean 1.883e+04
RMS 23.94
Underflow 3.025e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE6, Chip 6, ADC distribution
FE6Chip06All
Entries 328770
Mean 1358
RMS 4841
Underflow 0
Overflow 0
10^5
10^4
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10^2
10
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0
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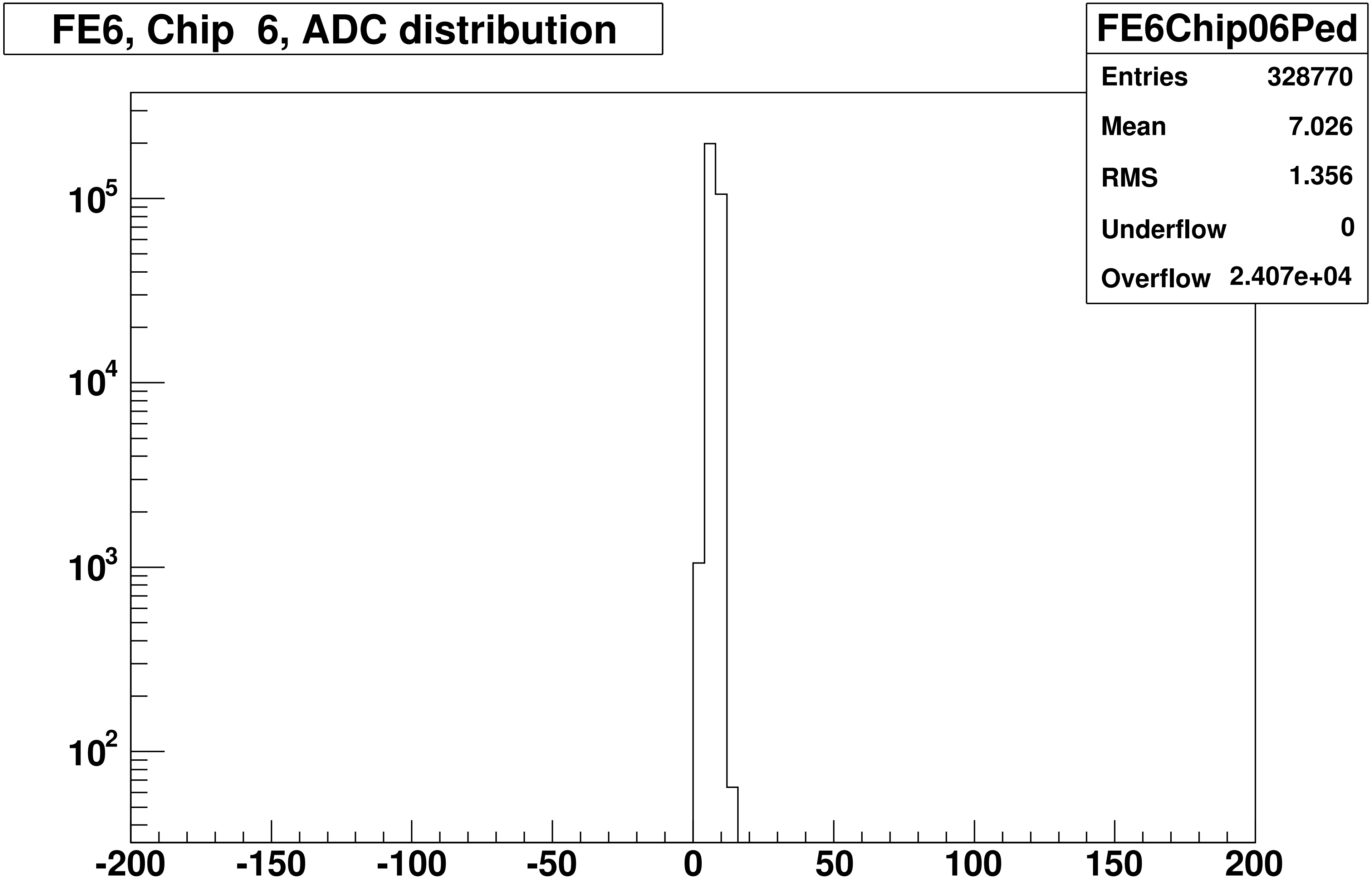
15000
20000
25000



FE6, Chip 6, ADC distribution
FE6Chip06Ped
Entries 328770
Mean 7.026
RMS 1.356
Underflow 0
Overflow 2.407e+04
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10^4
10^3
10^2
-200
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-100
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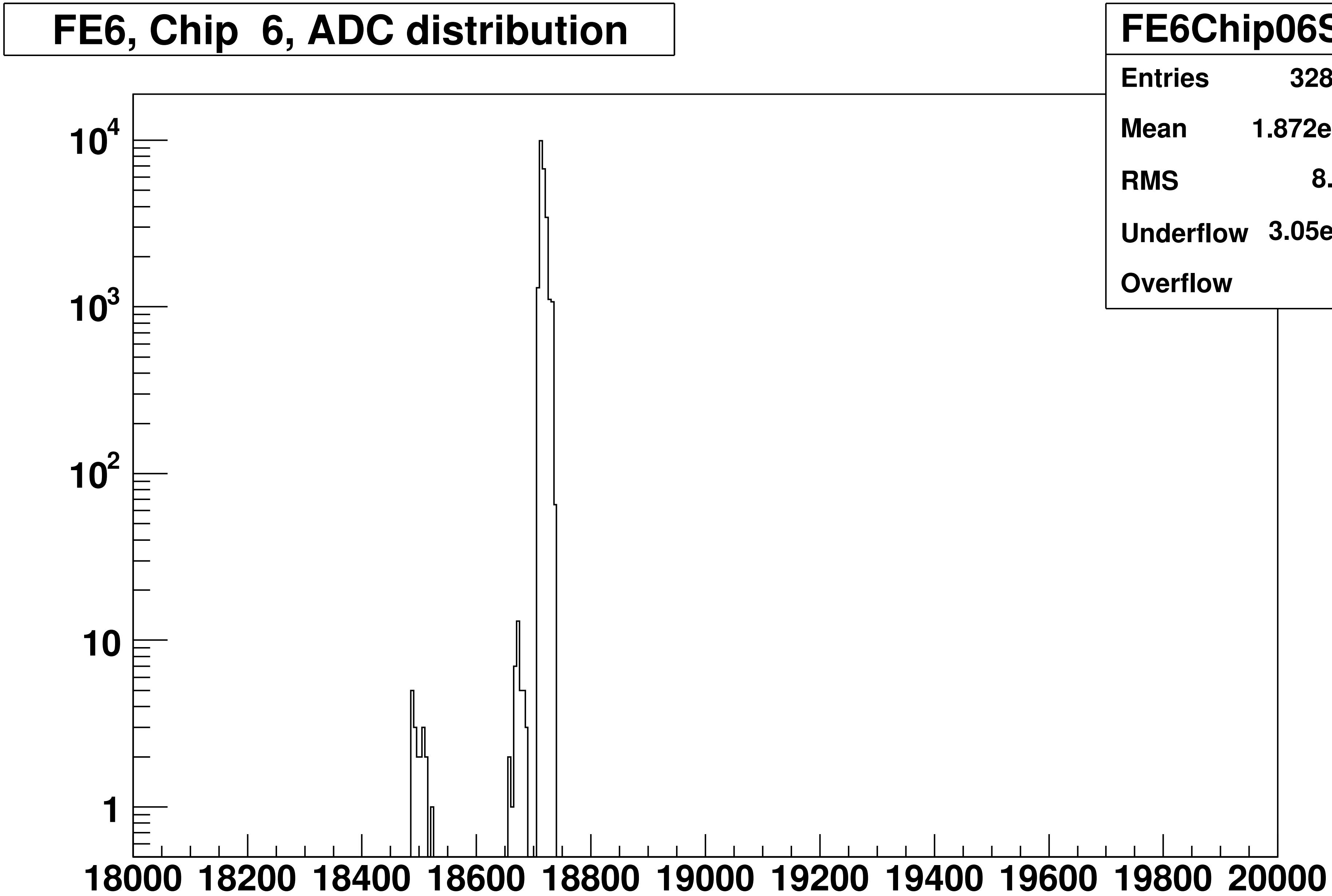
0
50
100
150
200


FE6, Chip 6, ADC distribution
FE6Chip06Sig
Entries 328770
Mean 1.872e+04
RMS 8.529
Underflow 3.05e+05
Overflow 0
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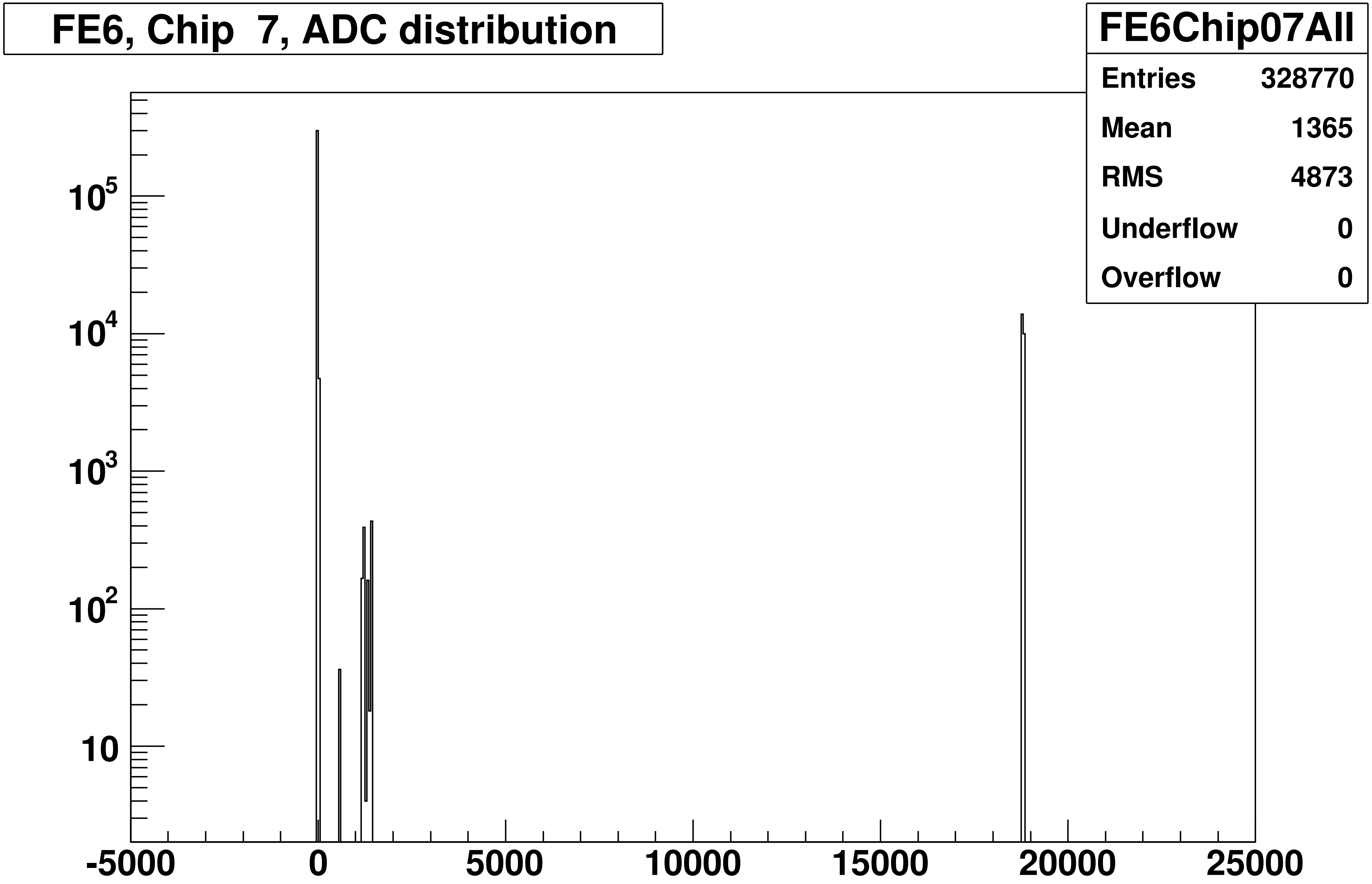
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE6, Chip 7, ADC distribution
FE6Chip07All
Entries 328770
Mean 1365
RMS 4873
Underflow 0
Overflow 0
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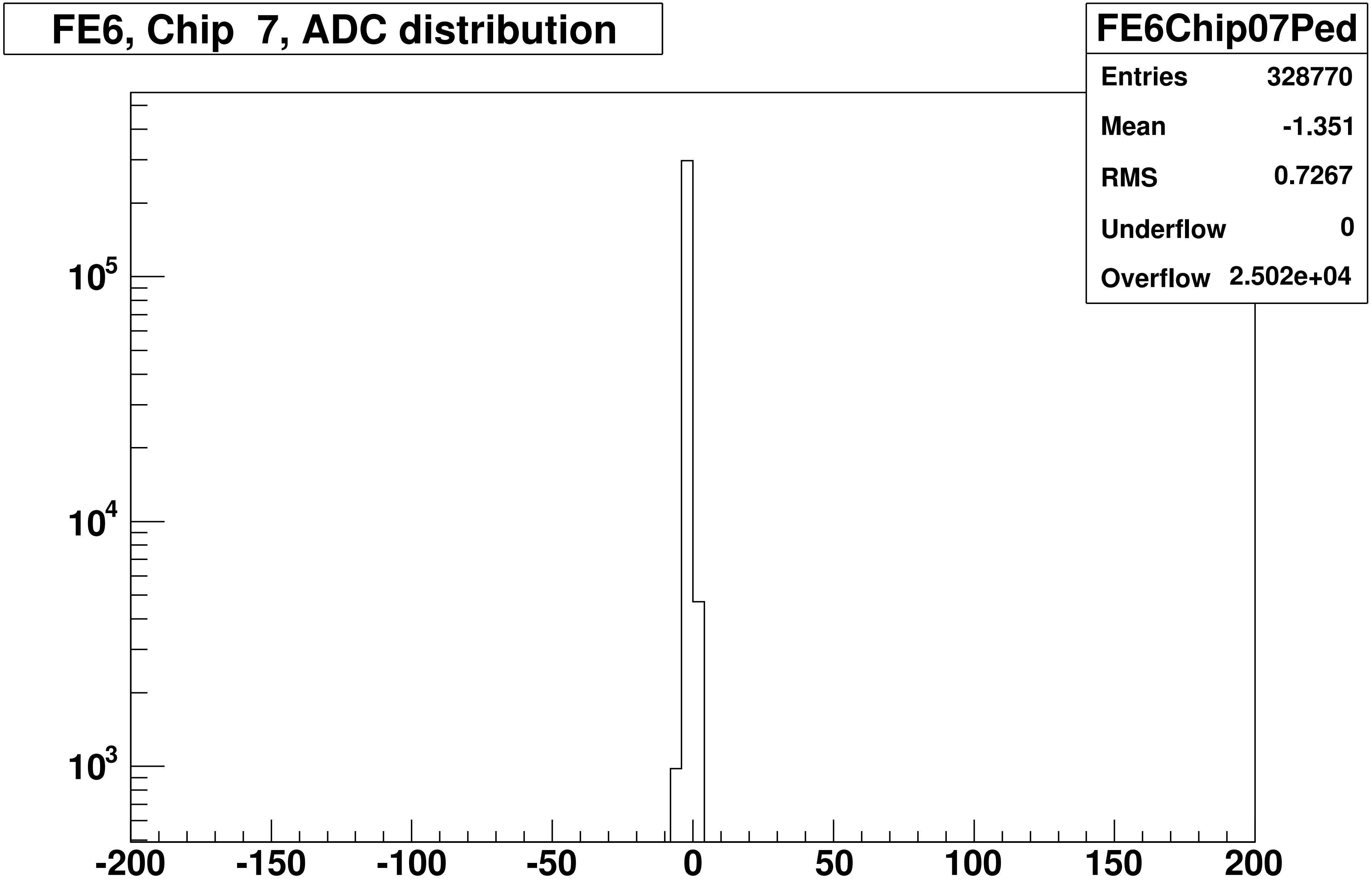
10^2
10^3
10^4
10^5
-5000
0
5000
10000
15000
20000
25000



FE6, Chip 7, ADC distribution
FE6Chip07Ped
Entries 328770
Mean -1.351
RMS 0.7267
Underflow 0
Overflow 2.502e+04
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10^4
10^3
-200
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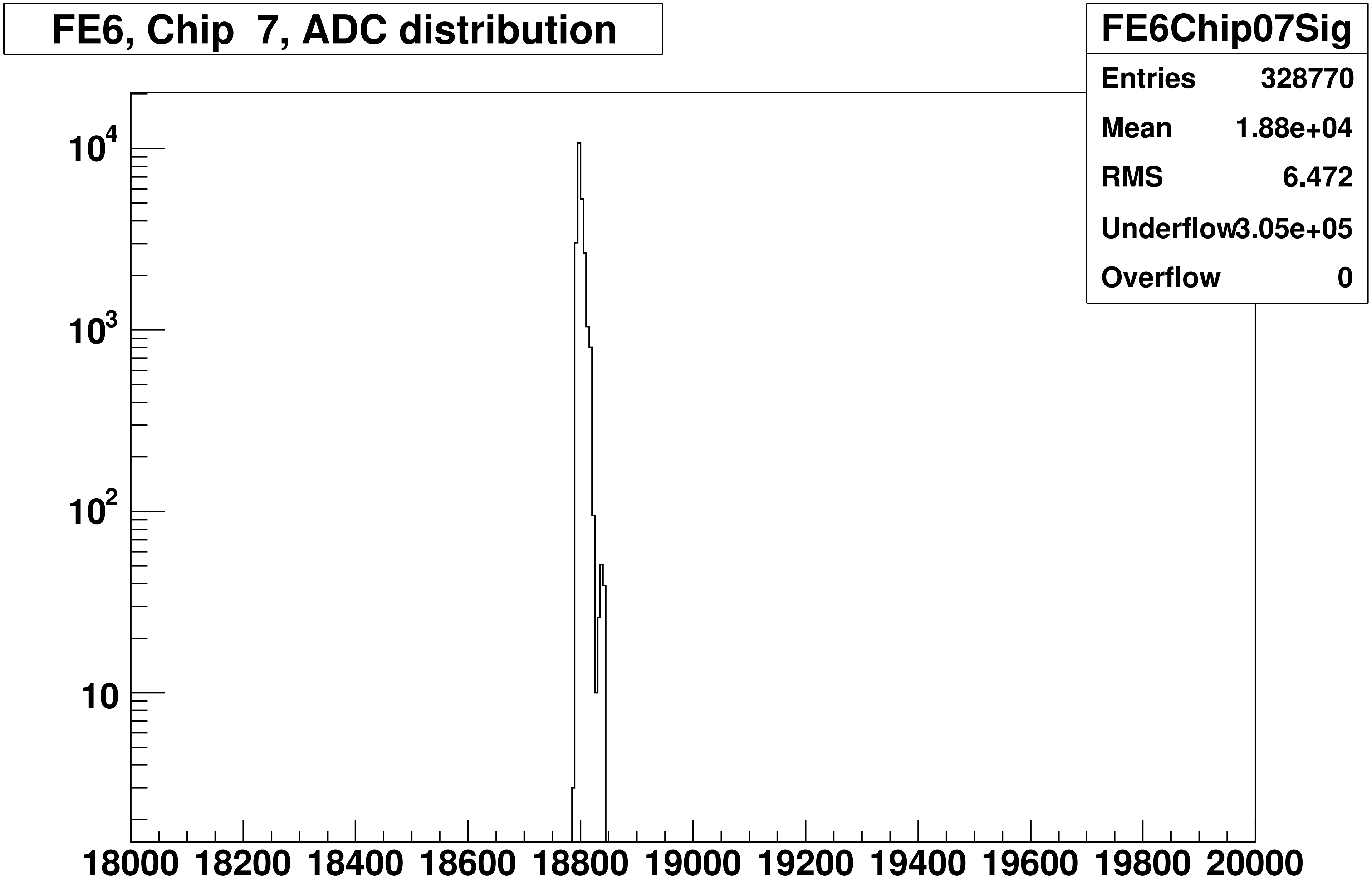
-100
-50
0
50
100
150
200


FE6, Chip 7, ADC distribution
FE6Chip07Sig
Entries 328770
Mean 1.88e+04
RMS 6.472
Underflow 3.05e+05
Overflow 0
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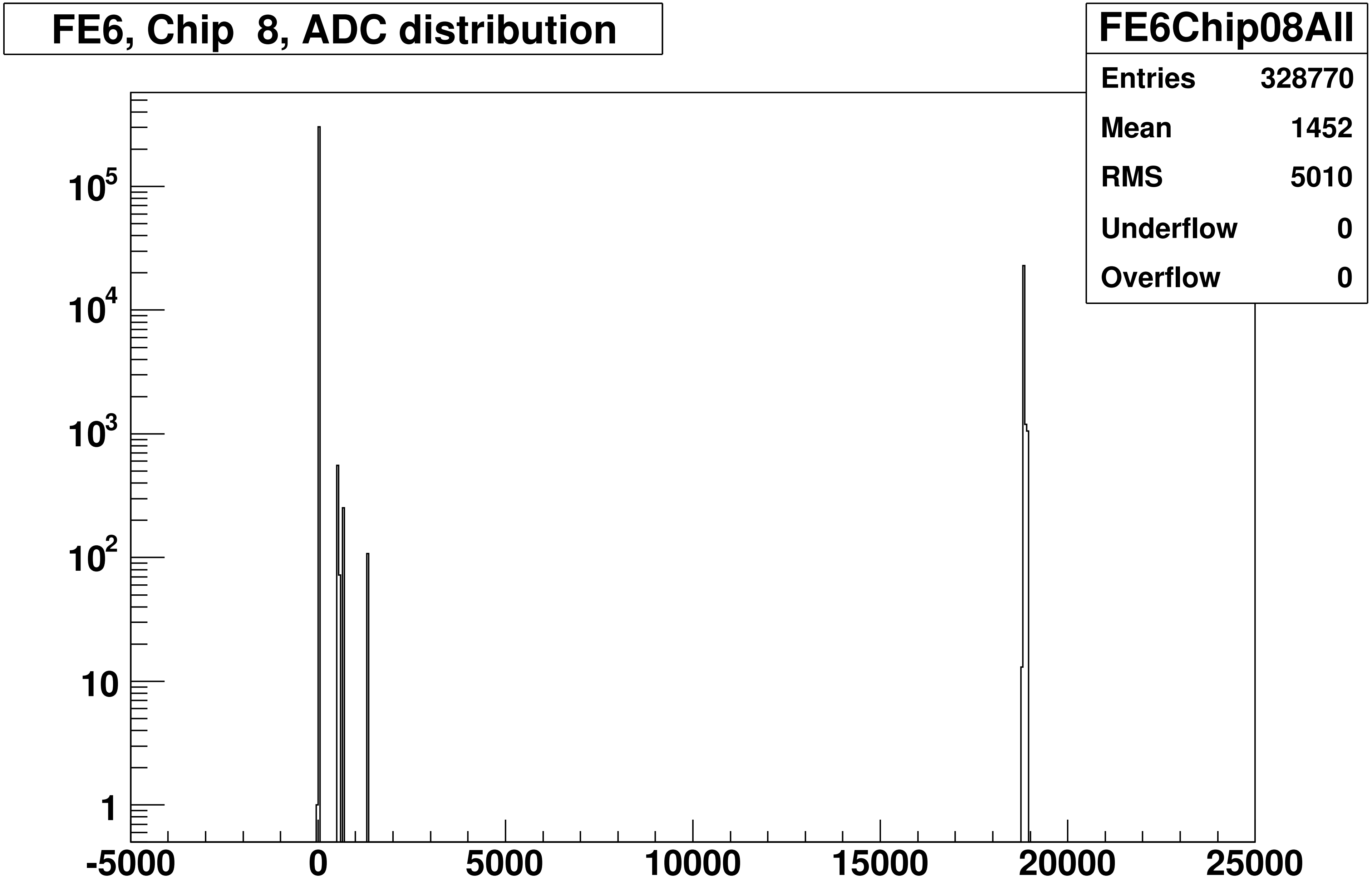
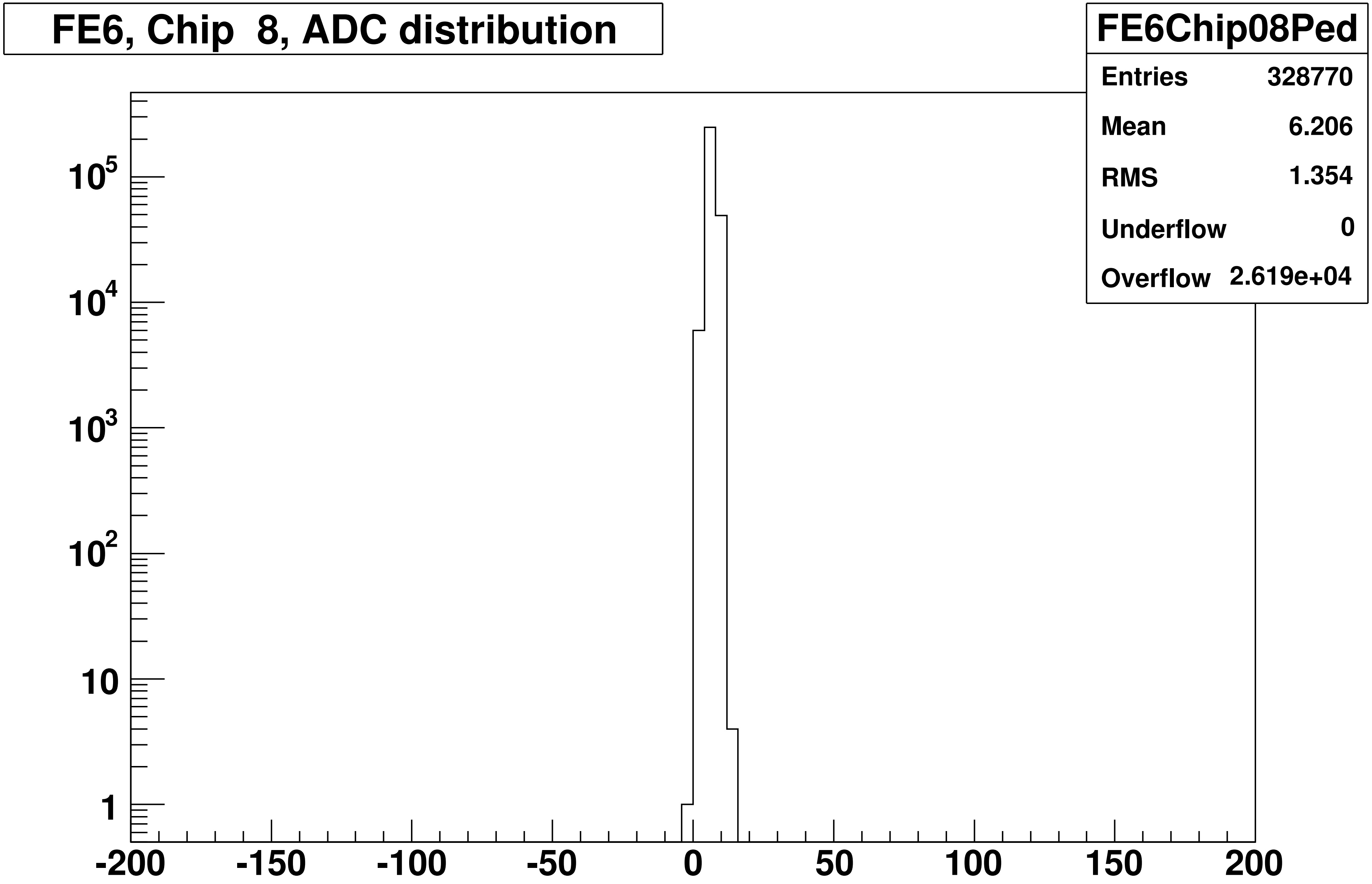
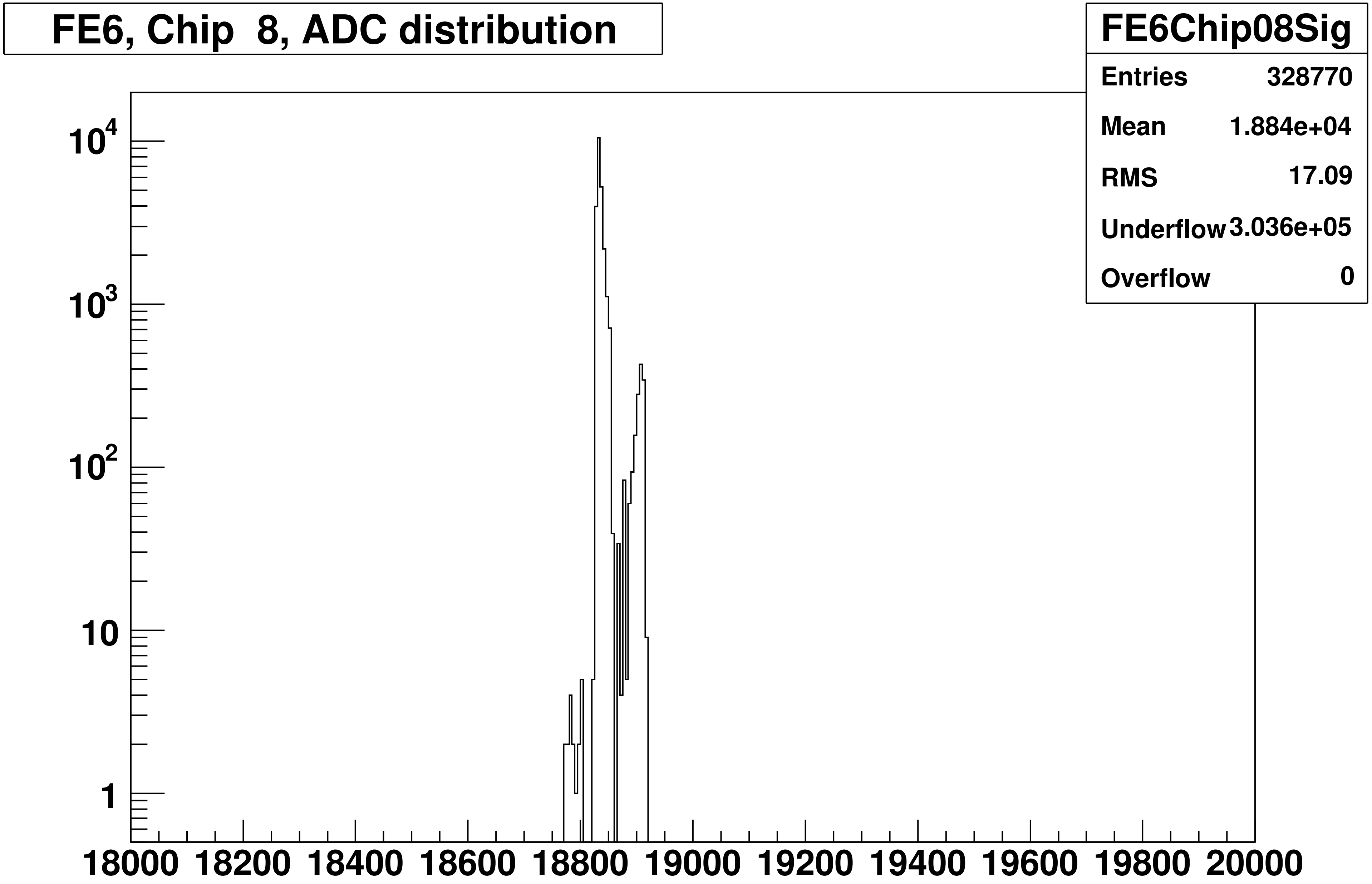
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000

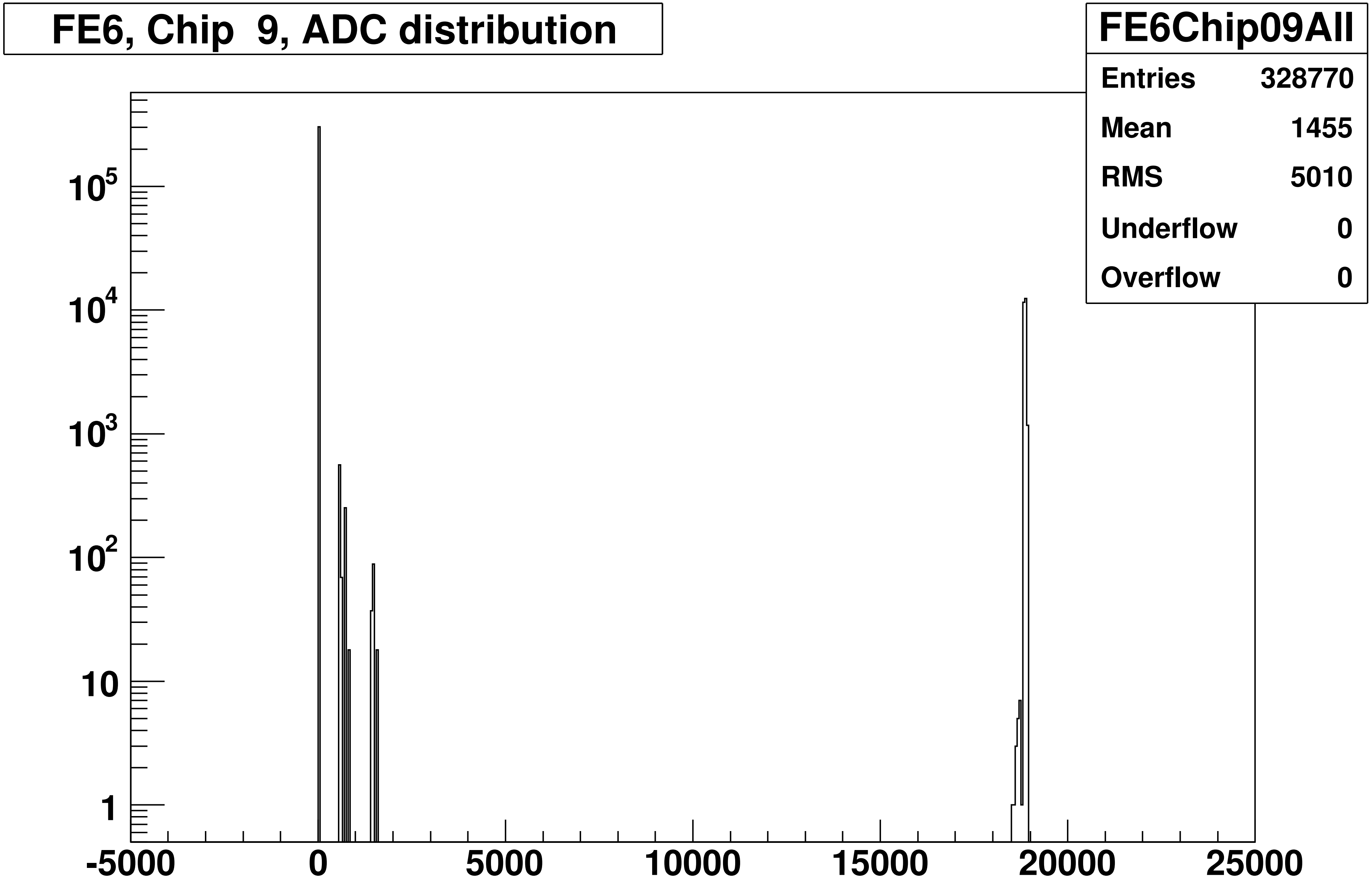


FE6, Chip 8, ADC distribution
FE6Chip08All
Entries 328770
Mean 1452
RMS 5010
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE6, Chip 8, ADC distribution
FE6Chip08Ped
Entries 328770
Mean 6.206
RMS 1.354
Underflow 0
Overflow 2.619e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
200



FE6, Chip 8, ADC distribution
FE6Chip08Sig
Entries 328770
Mean 1.884e+04
RMS 17.09
Underflow 3.036e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE6, Chip 9, ADC distribution
FE6Chip09All
Entries 328770
Mean 1455
RMS 5010
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
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1
-5000
0
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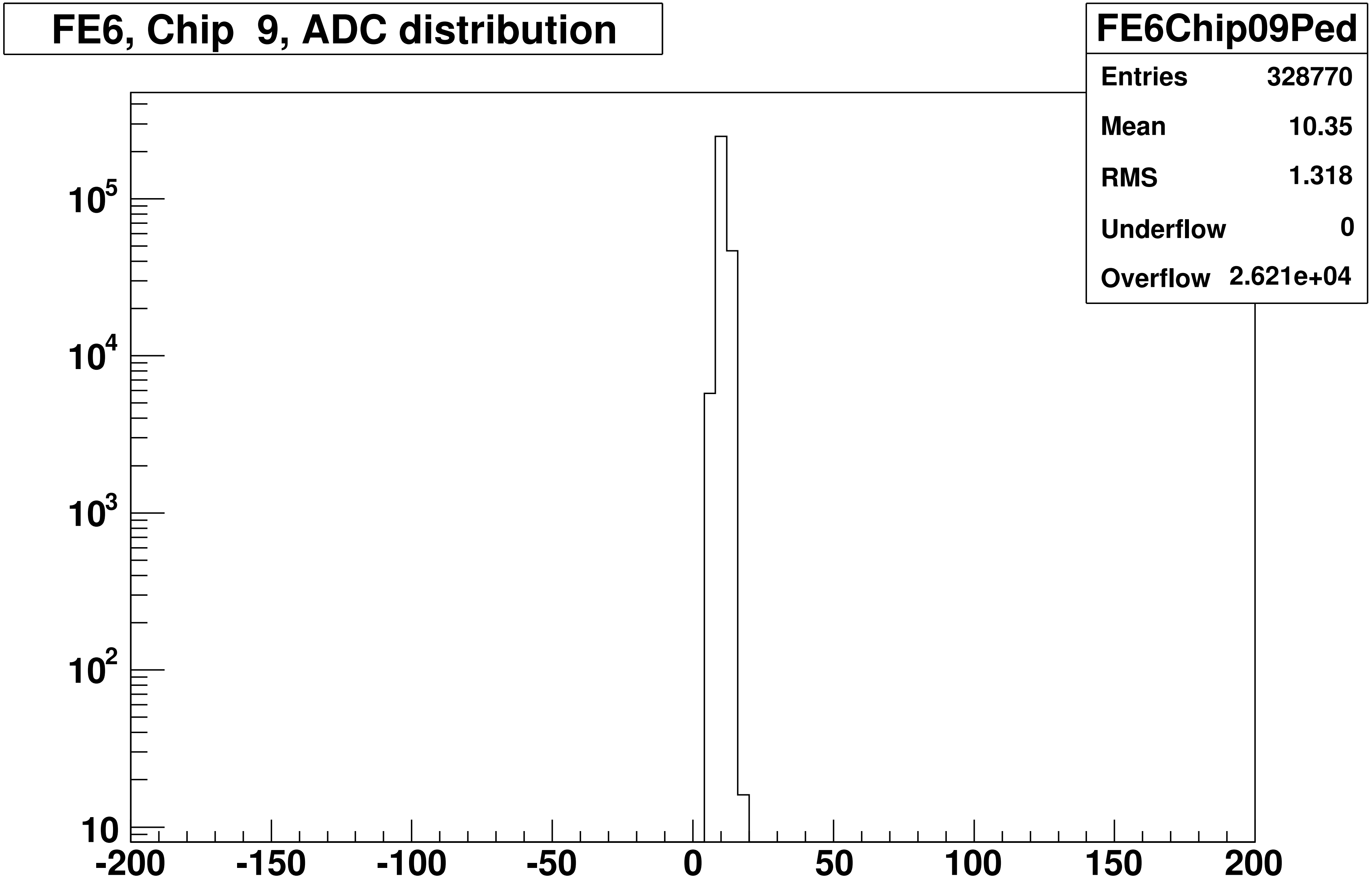
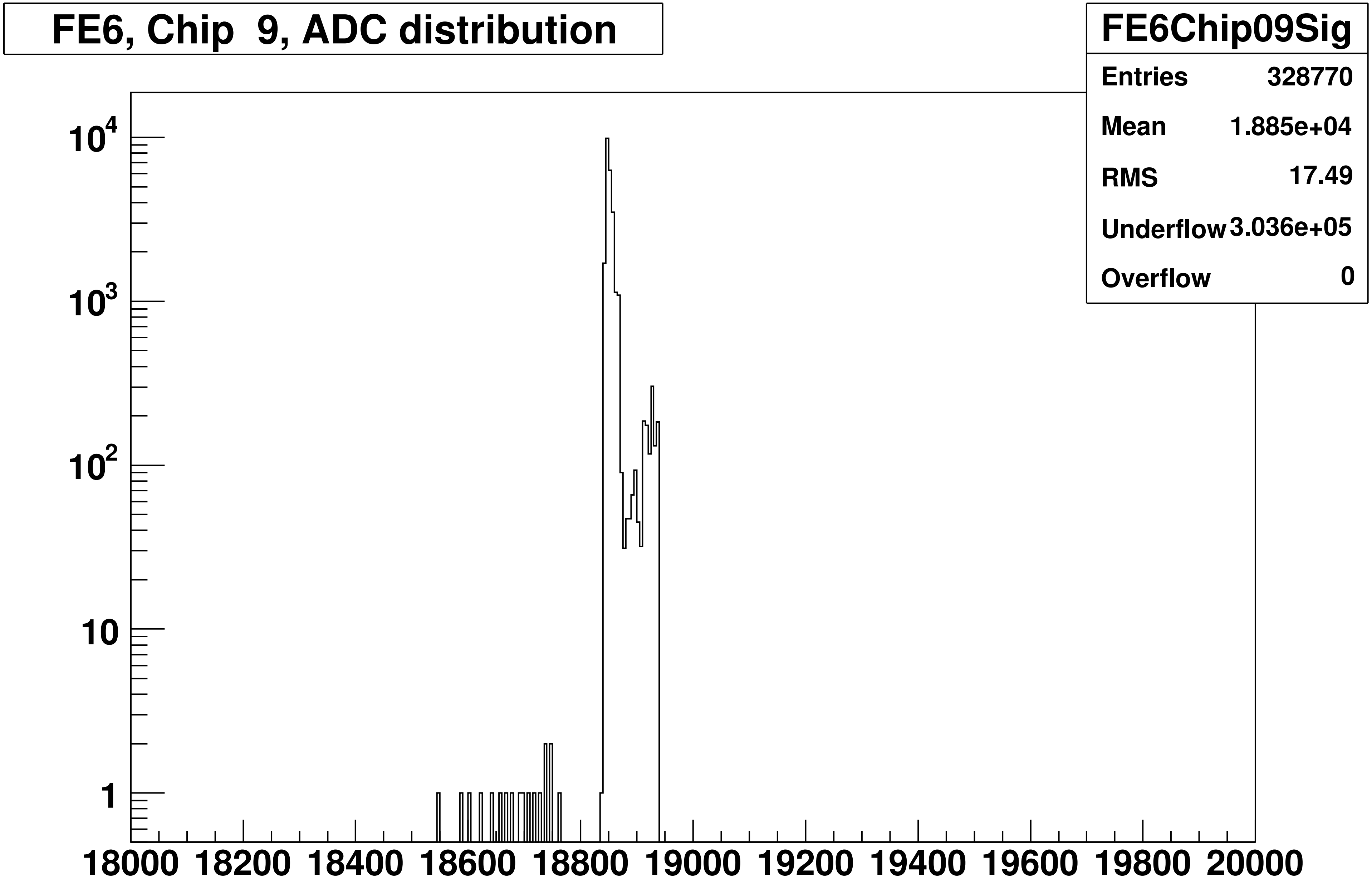
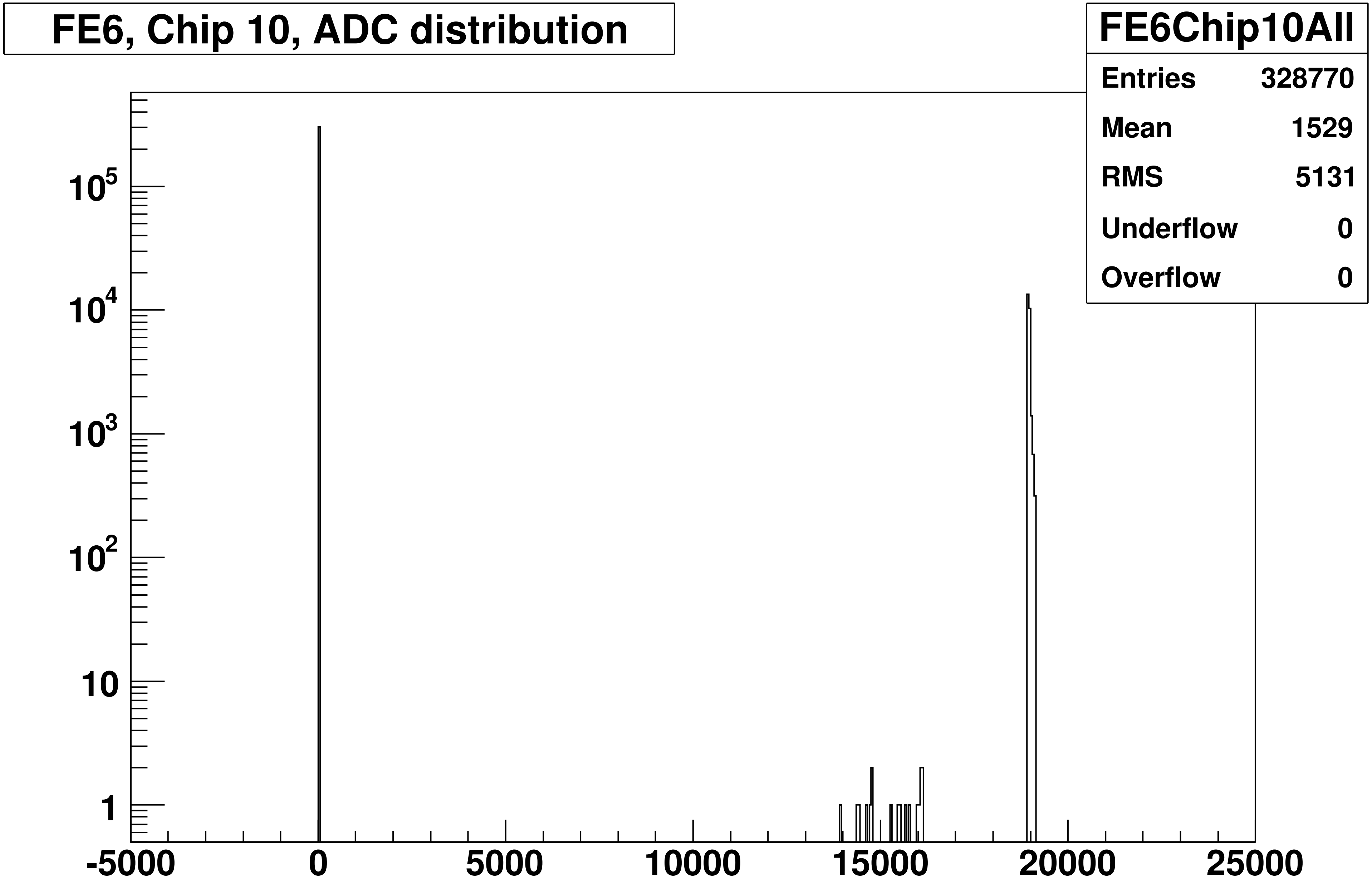
10000
15000
20000
25000

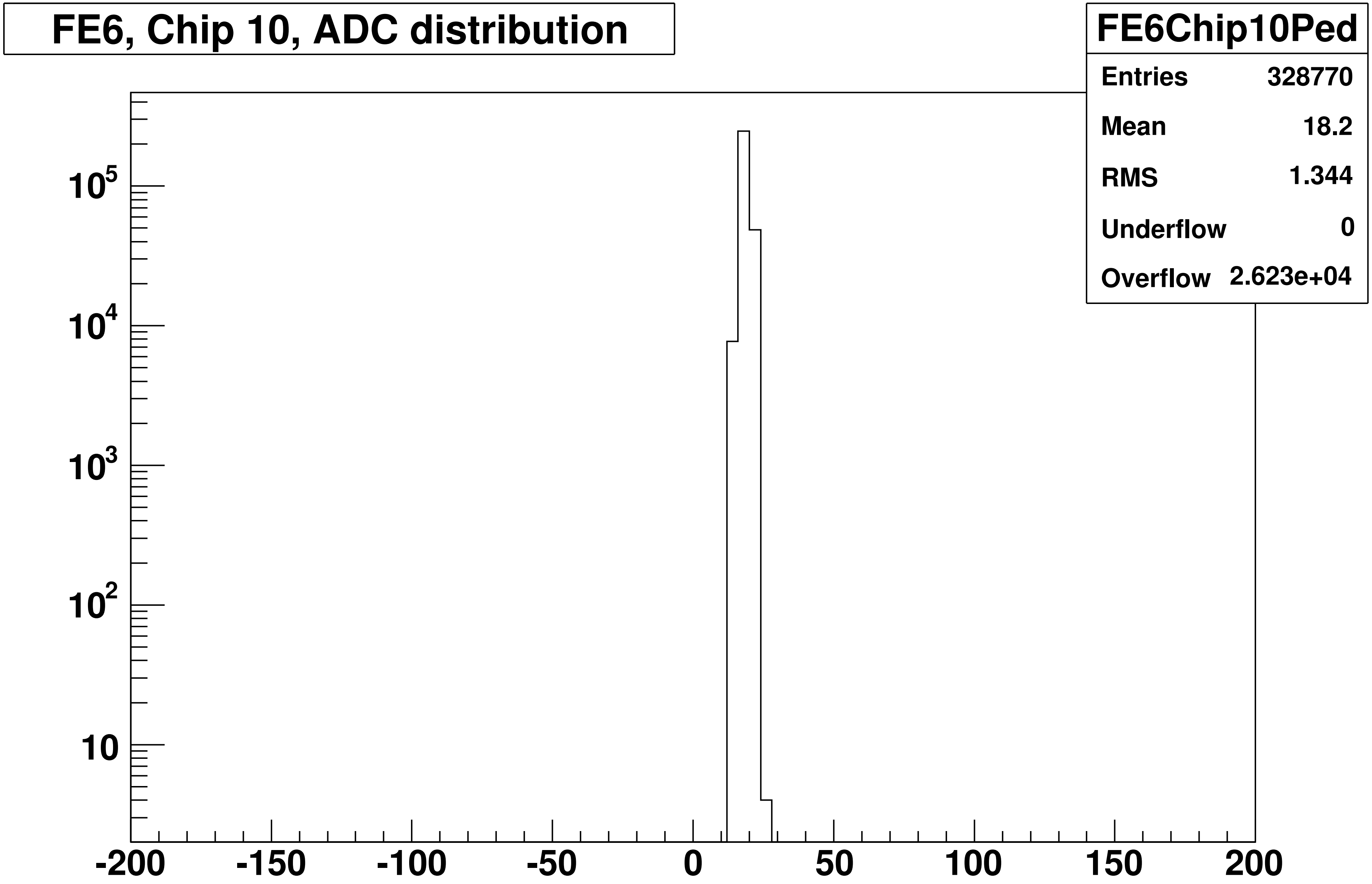


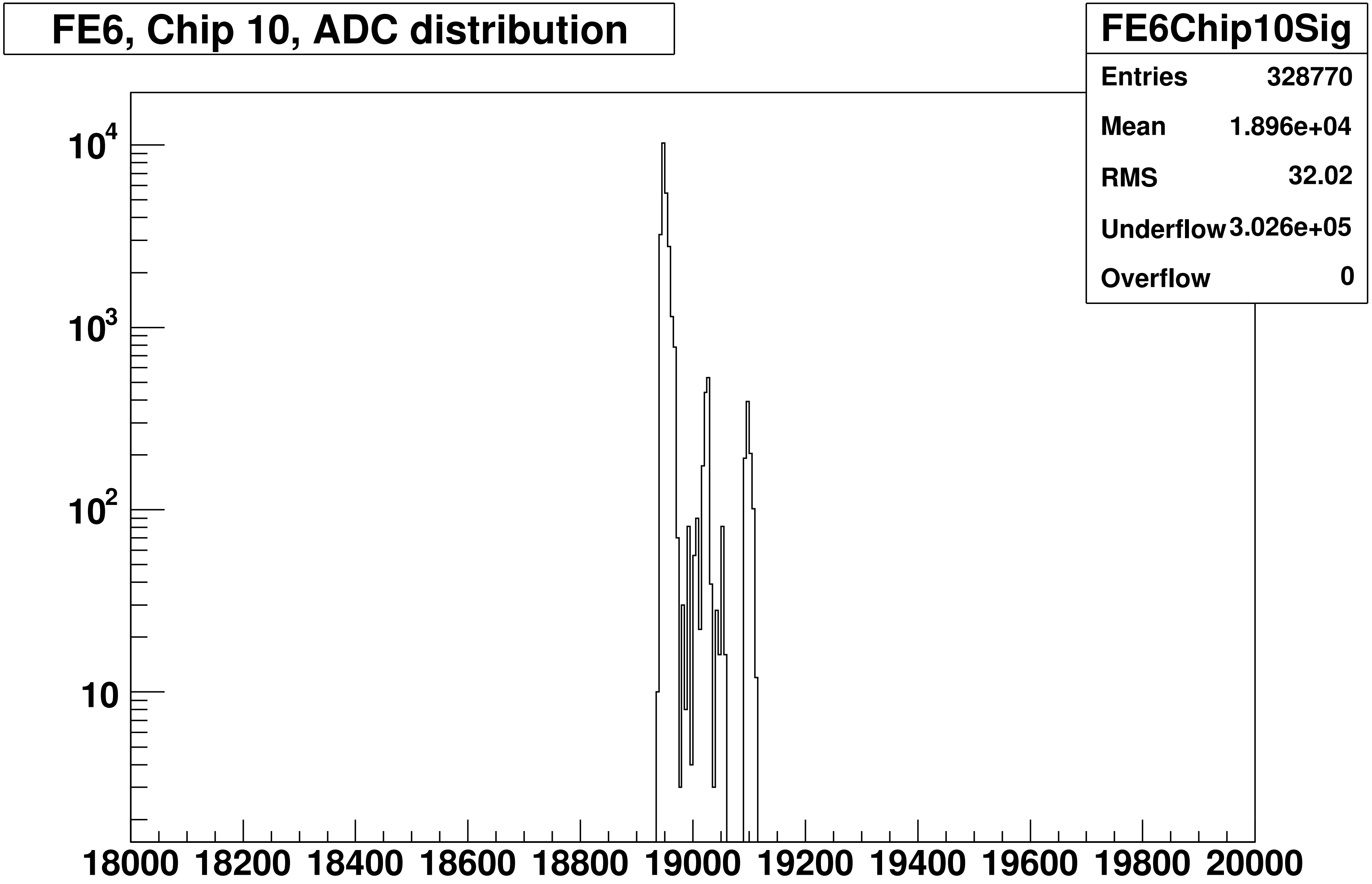
FE6, Chip 9, ADC distribution
FE6Chip09Ped
Entries 328770
Mean 10.35
RMS 1.318
Underflow 0
Overflow 2.621e+04
10^5
10^4
10^3
10^2
10
-200
-150
-100
-50
0
50
100
150
200



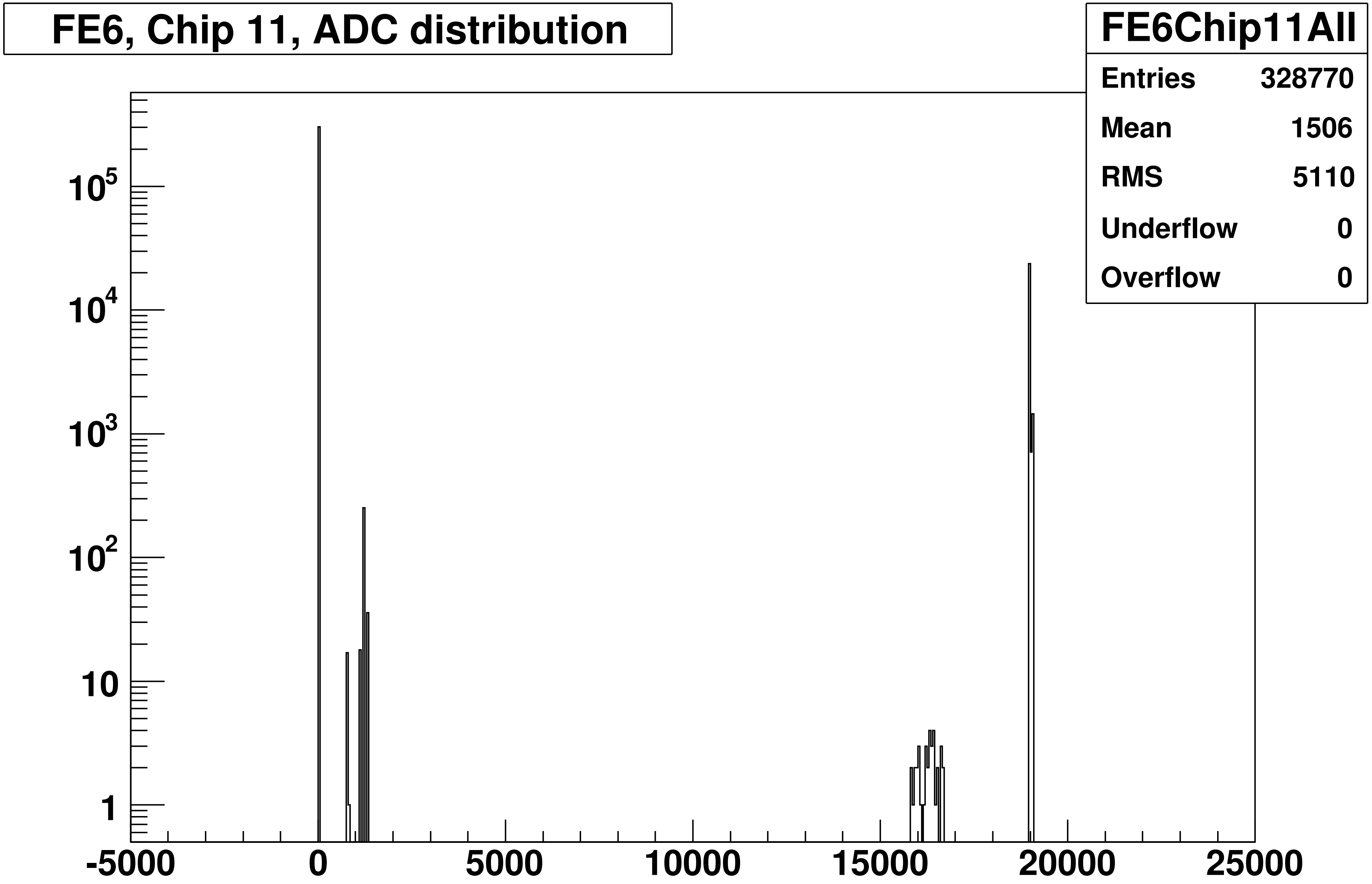
FE6, Chip 9, ADC distribution
FE6Chip09Sig
Entries 328770
Mean 1.885e+04
RMS 17.49
Underflow 3.036e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000


FE6, Chip 10, ADC distribution
FE6Chip10All
Entries 328770
Mean 1529
RMS 5131
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000

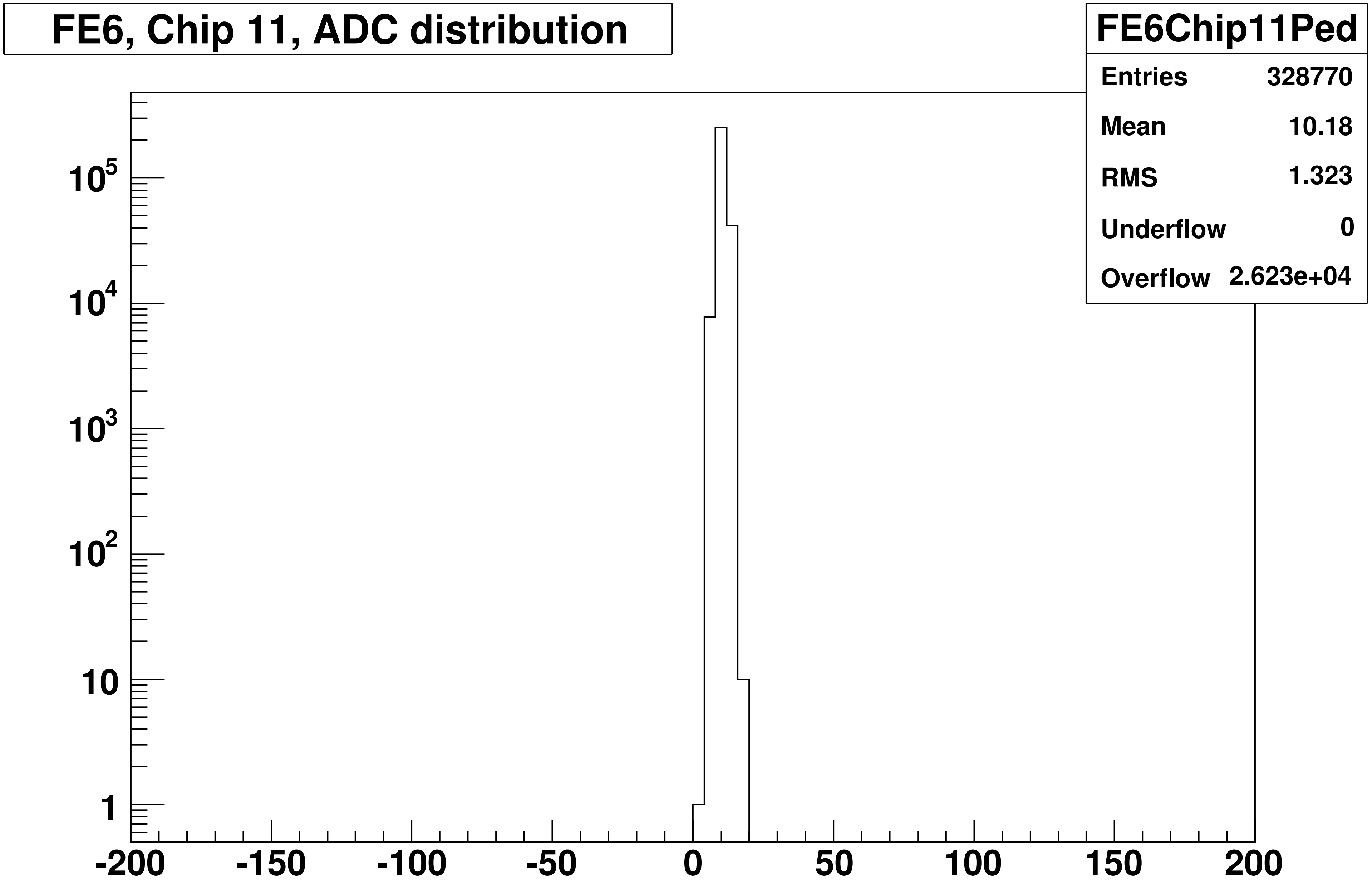

FE6, Chip 10, ADC distribution
FE6Chip10Ped
Entries 328770
Mean 18.2
RMS 1.344
Underflow 0
Overflow 2.623e+04
10^5
10^4
10^3
10^2
10
-200
-150
-100
-50
0
50
100
150
200



FE6, Chip 10, ADC distribution
FE6Chip10Sig
Entries 328770
Mean 1.896e+04
RMS 32.02
Underflow 3.026e+05
Overflow 0
10^4
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE6, Chip 11, ADC distribution
FE6Chip11All
Entries 328770
Mean 1506
RMS 5110
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE6, Chip 11, ADC distribution
FE6Chip11Ped
Entries 328770
Mean 10.18
RMS 1.323
Underflow 0
Overflow 2.623e+04
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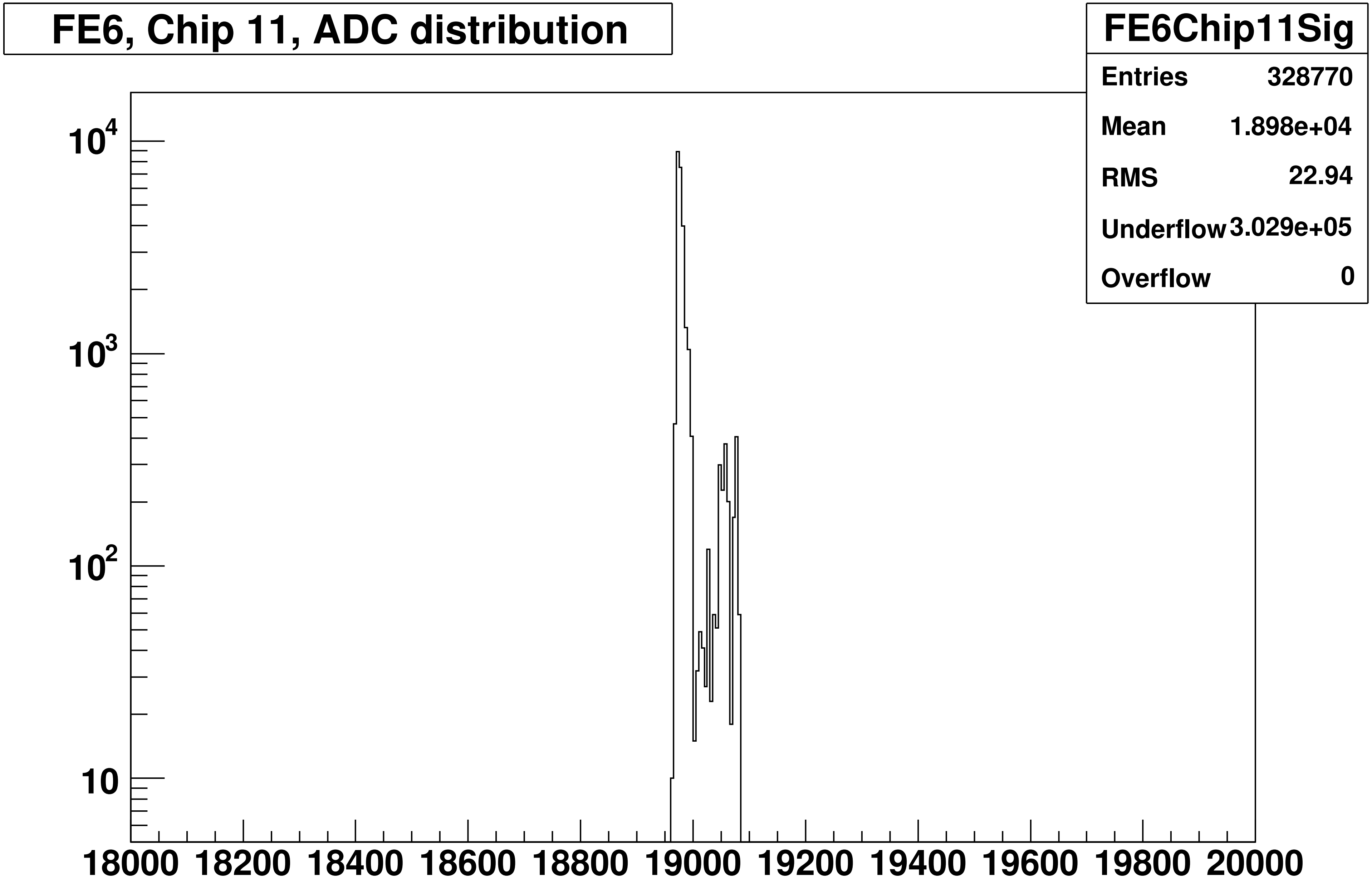
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
200


FE6, Chip 11, ADC distribution
FE6Chip11Sig
Entries 328770
Mean 1.898e+04
RMS 22.94
Underflow 3.029e+05
Overflow 0
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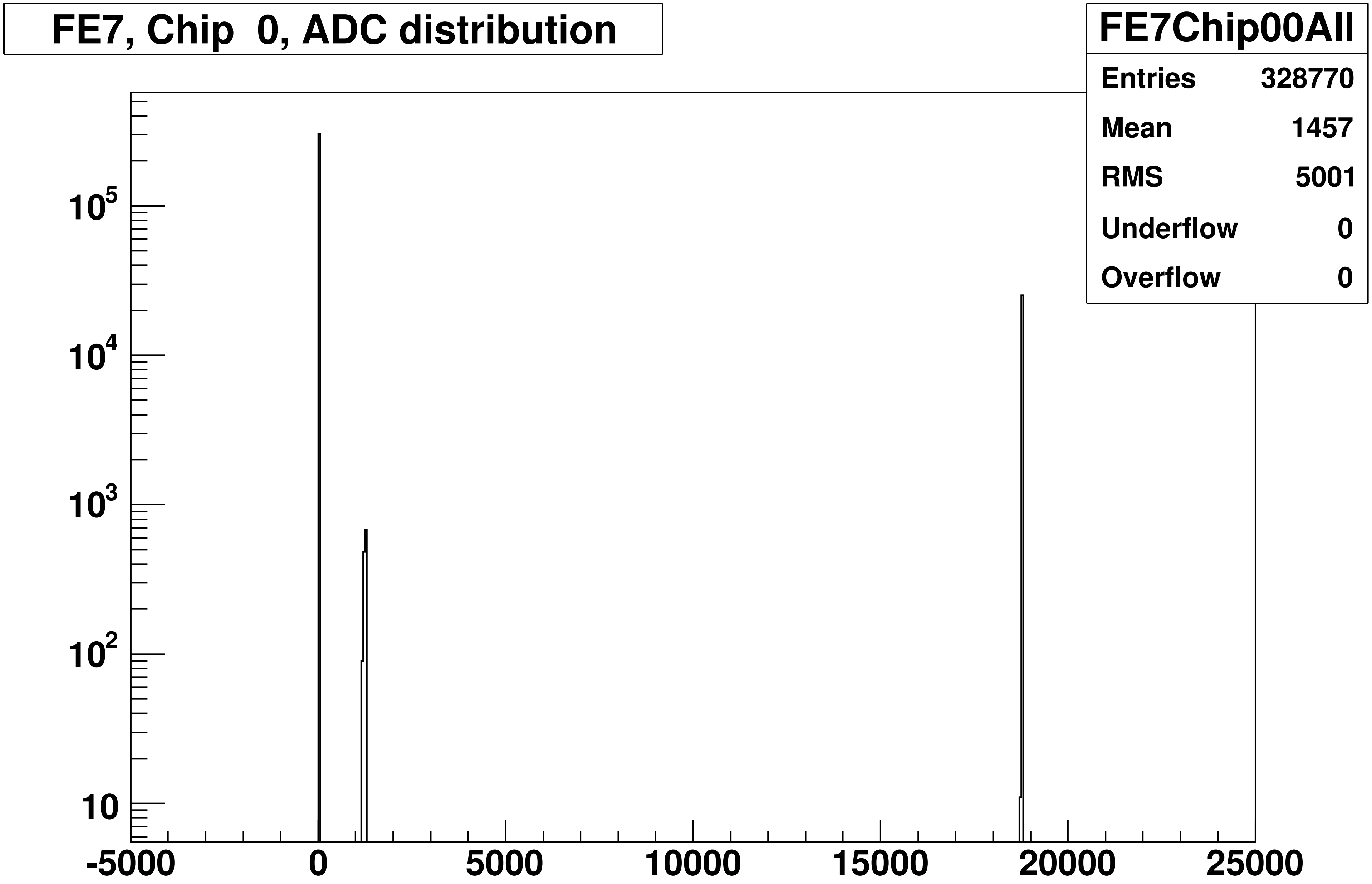
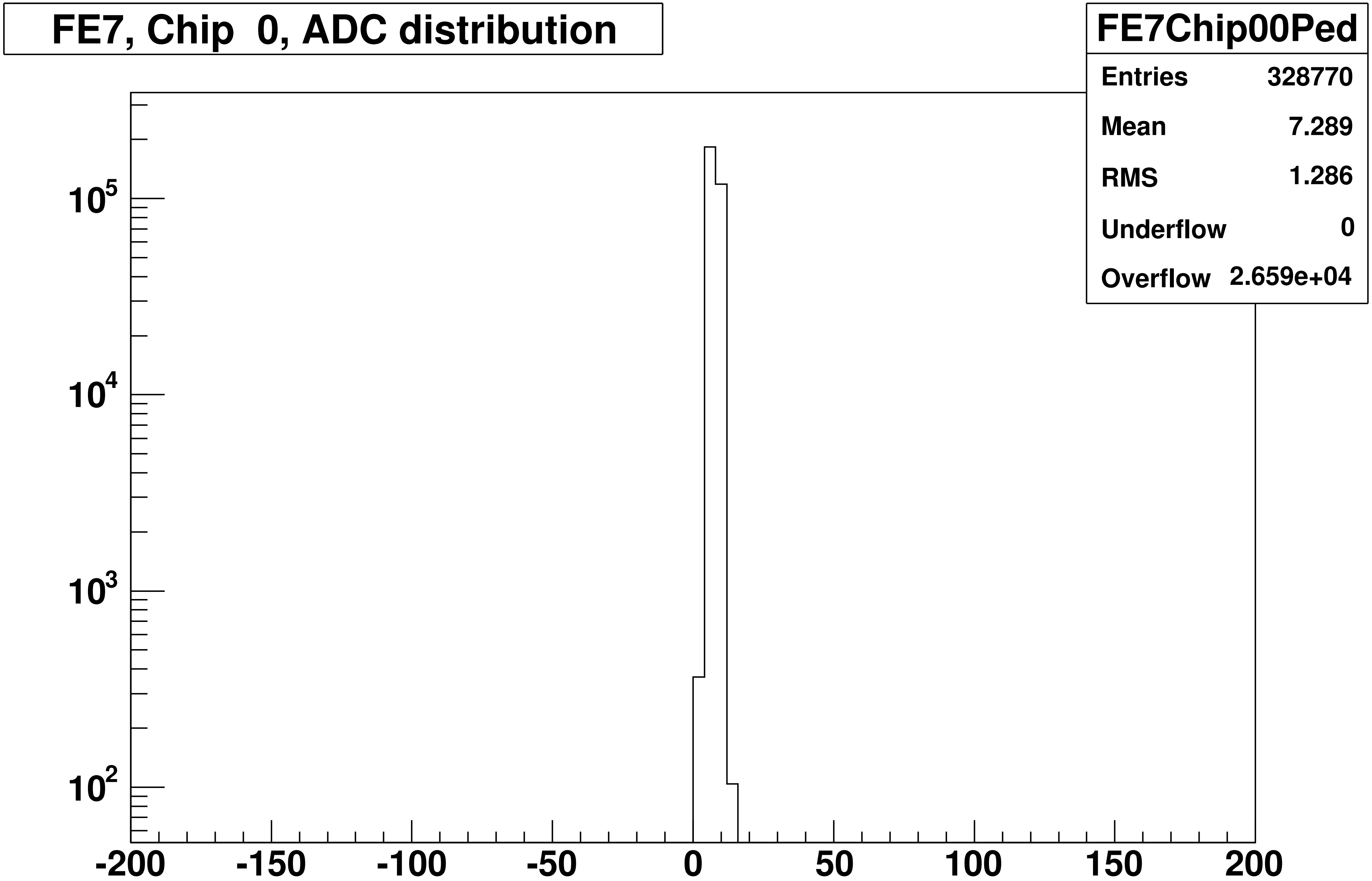
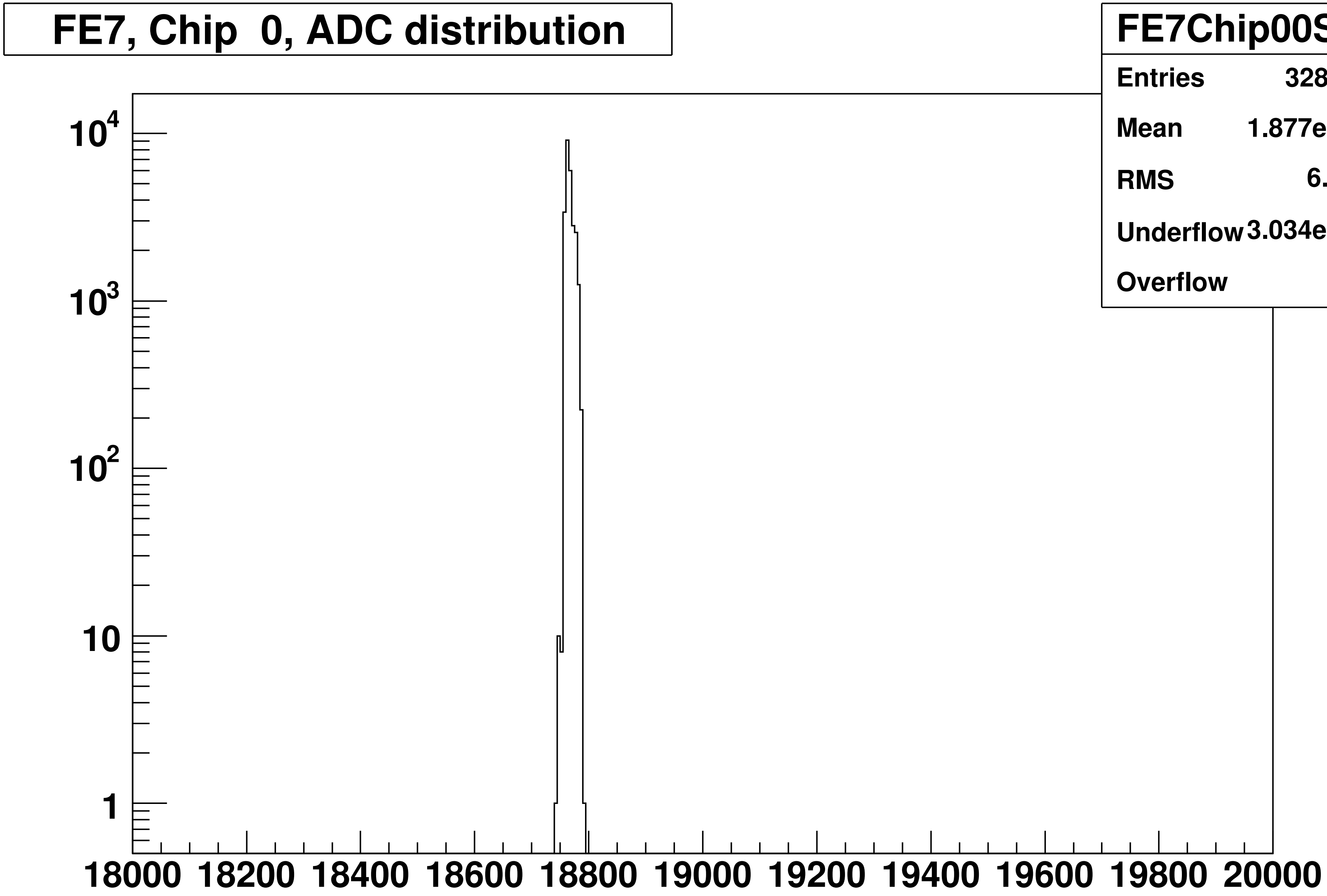
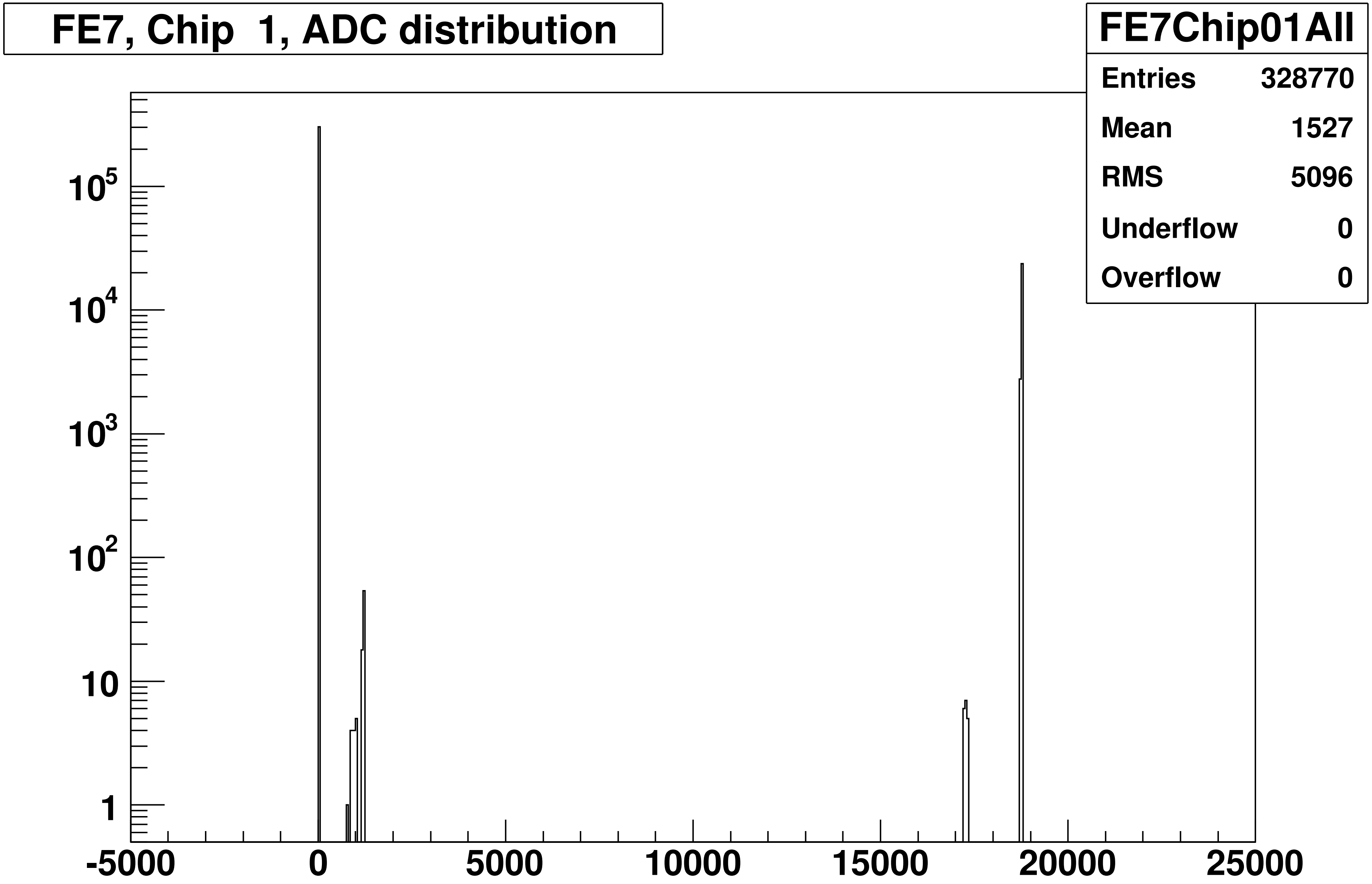
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE7, Chip 0, ADC distribution
FE7Chip00All
Entries 328770
Mean 1457
RMS 5001
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000

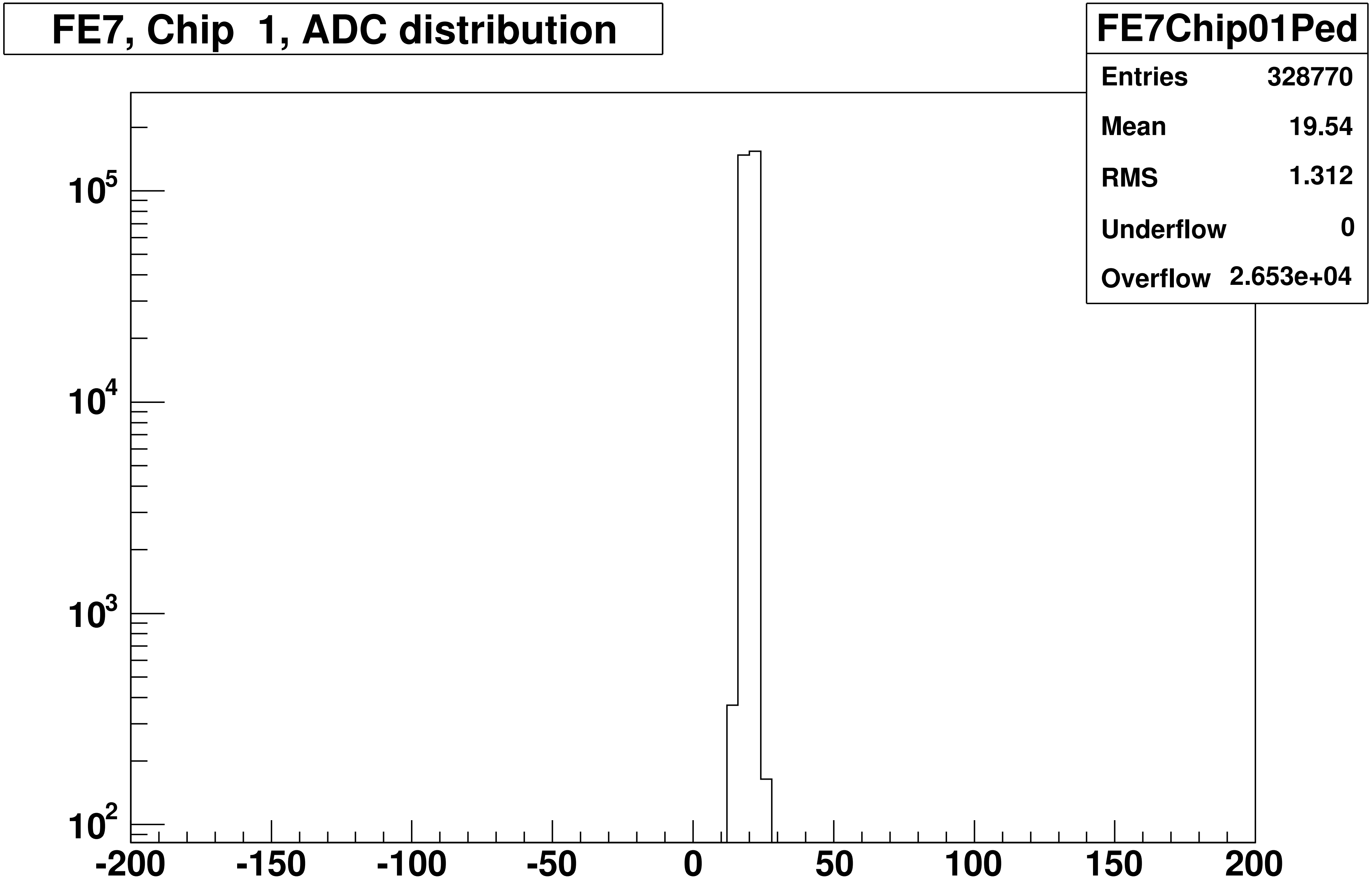


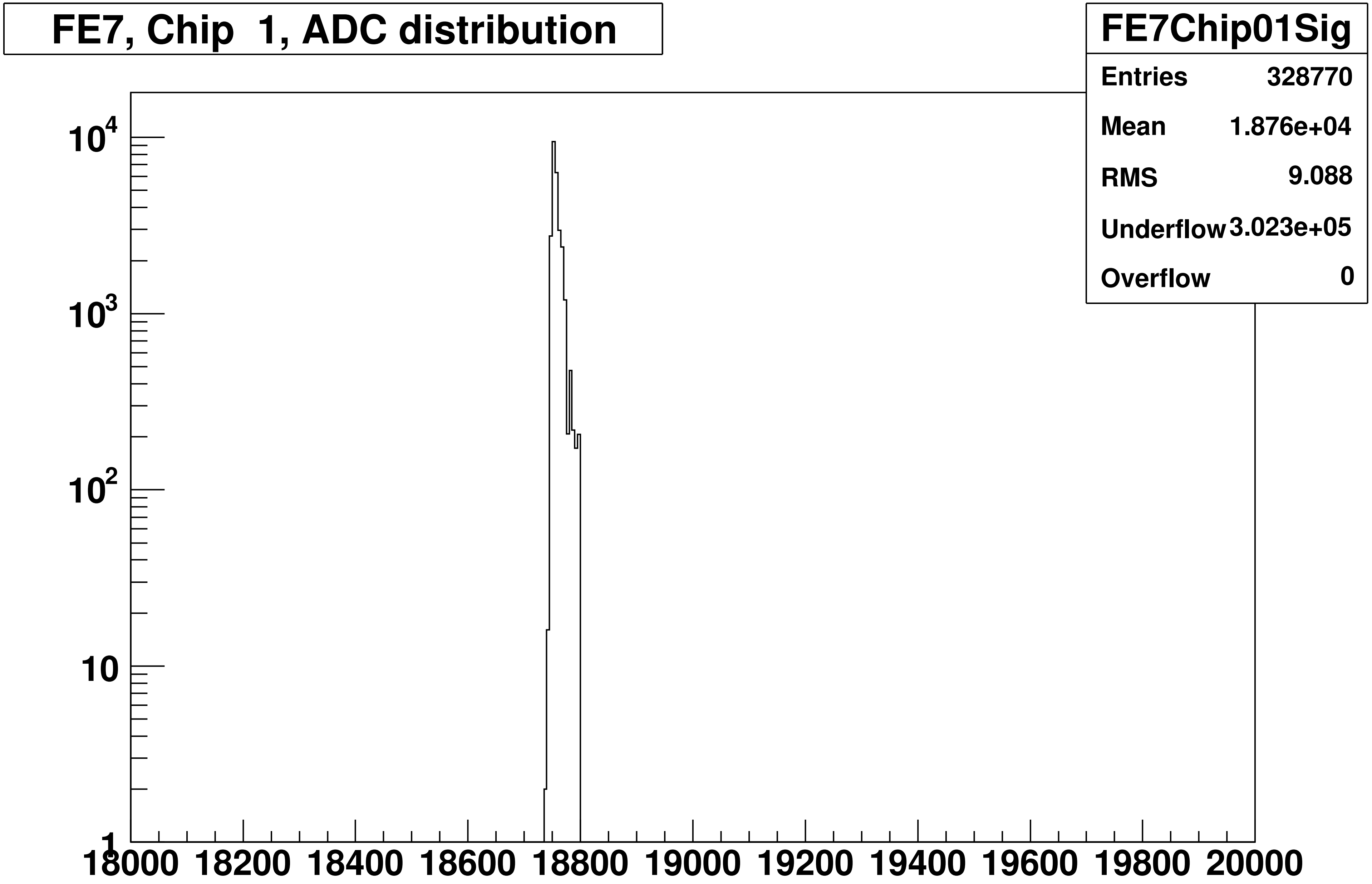
FE7, Chip 0, ADC distribution
FE7Chip00Ped
Entries 328770
Mean 7.289
RMS 1.286
Underflow 0
Overflow 2.659e+04
10^5
10^4
10^3
10^2
-200
-150
-100
-50
0
50
100
150
200


FE7, Chip 0, ADC distribution
FE7Chip00Sig
Entries 328770
Mean 1.877e+04
RMS 6.838
Underflow 3.034e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000

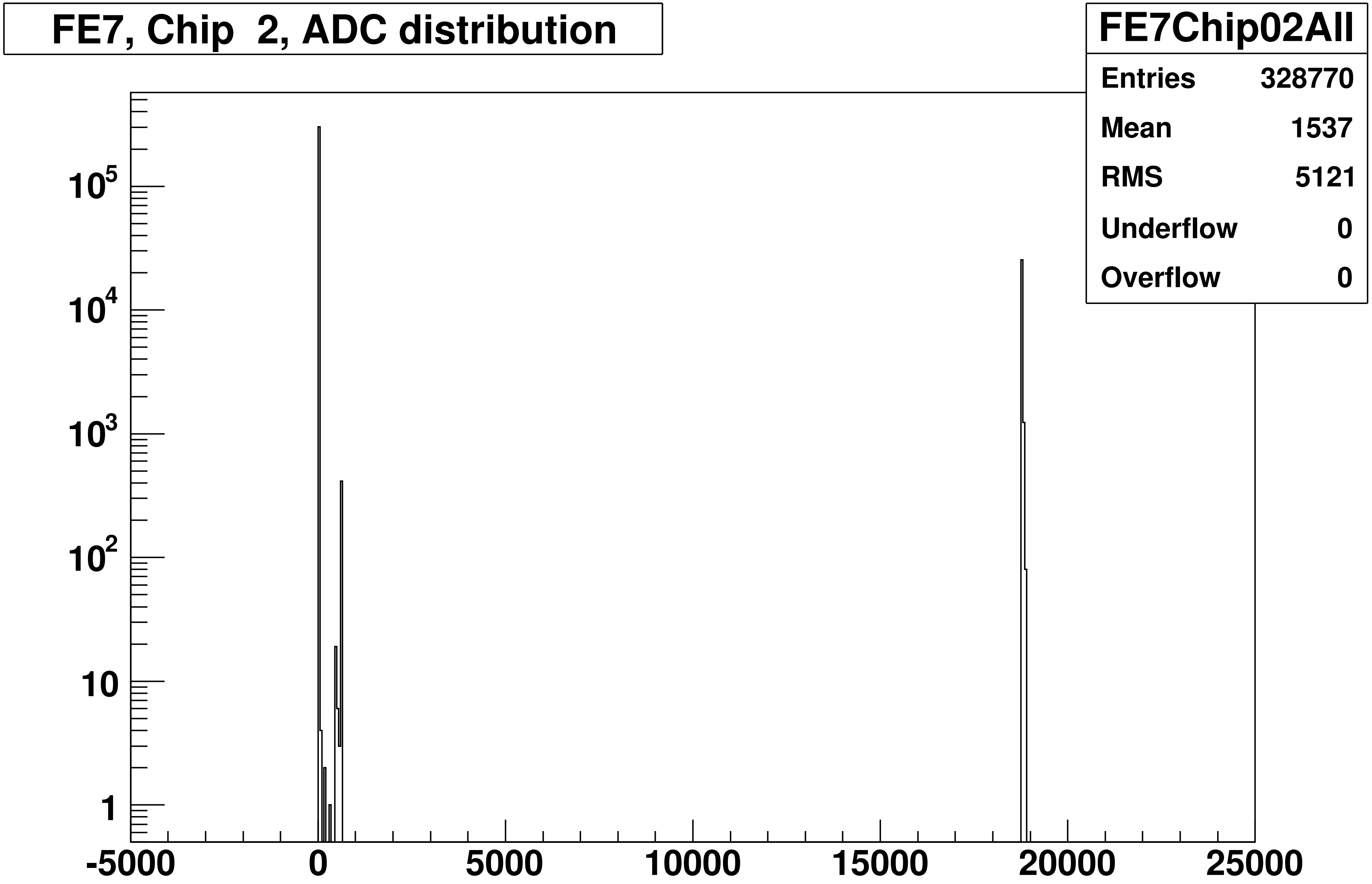


FE7, Chip 1, ADC distribution
FE7Chip01All
Entries 328770
Mean 1527
RMS 5096
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000

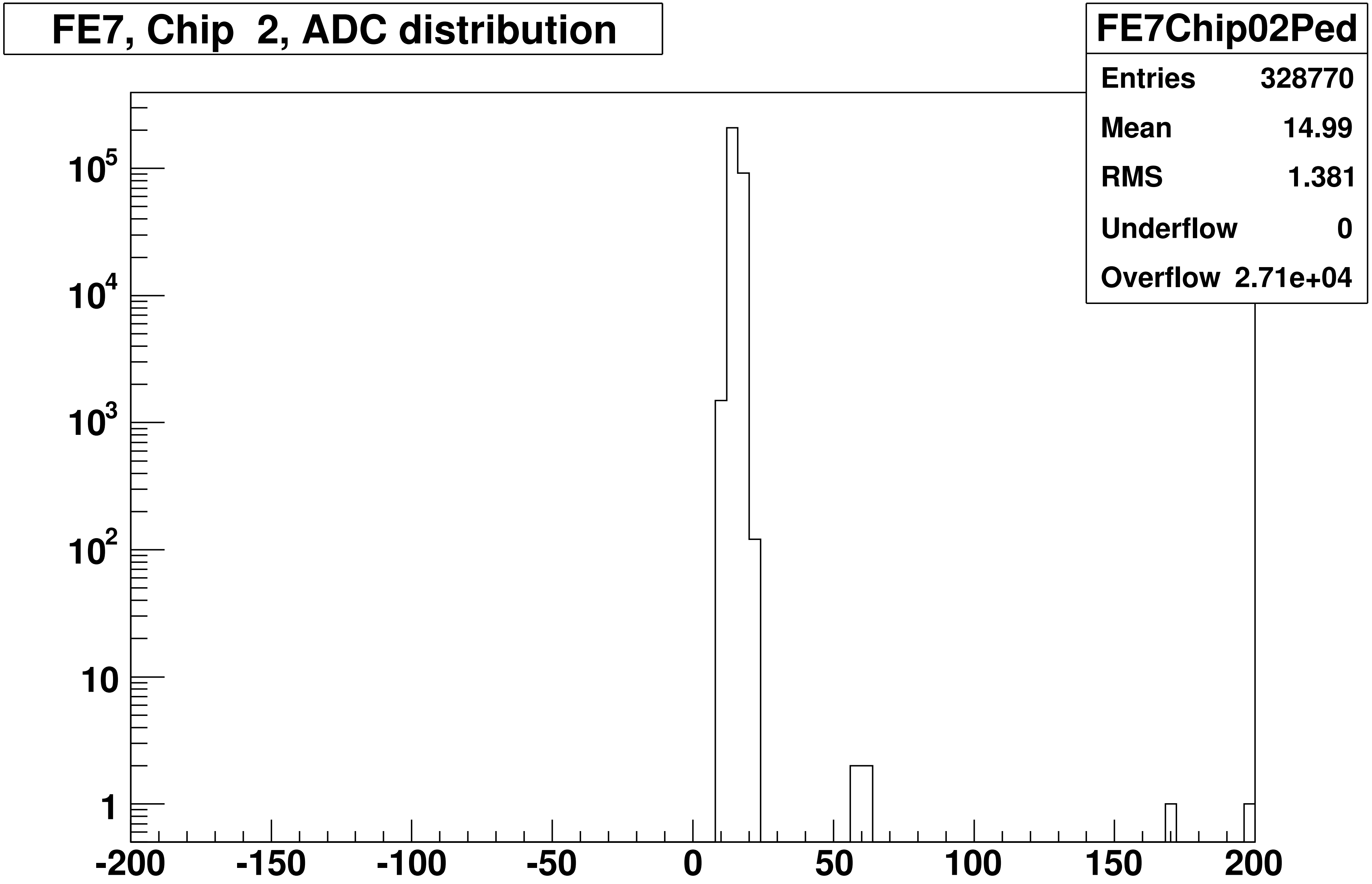

FE7, Chip 1, ADC distribution
FE7Chip01Ped
Entries 328770
Mean 19.54
RMS 1.312
Underflow 0
Overflow 2.653e+04
10^5
10^4
10^3
10^2
-200
-150
-100
-50
0
50
100
150
200



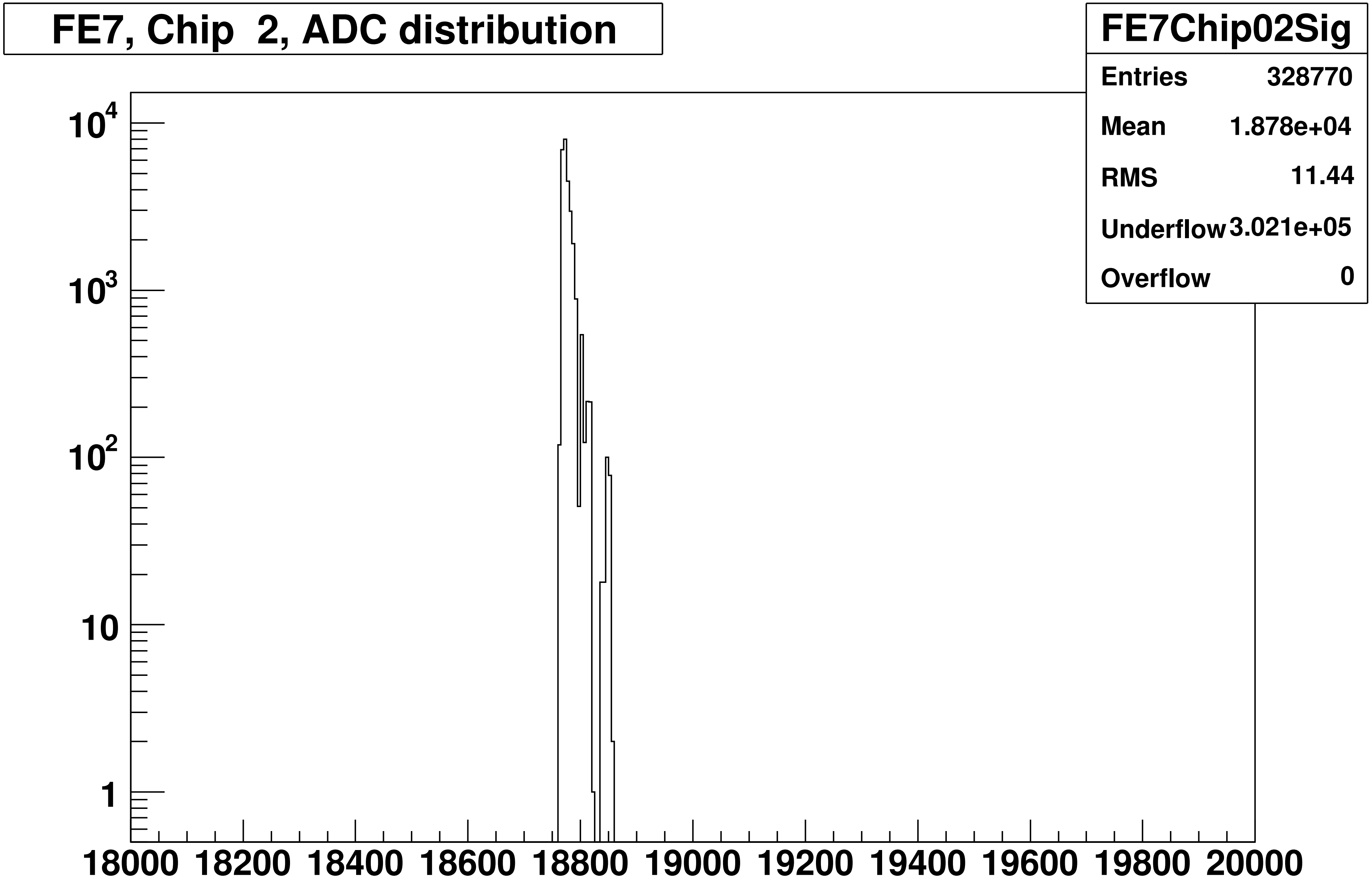
FE7, Chip 1, ADC distribution
FE7Chip01Sig
Entries 328770
Mean 1.876e+04
RMS 9.088
Underflow 3.023e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



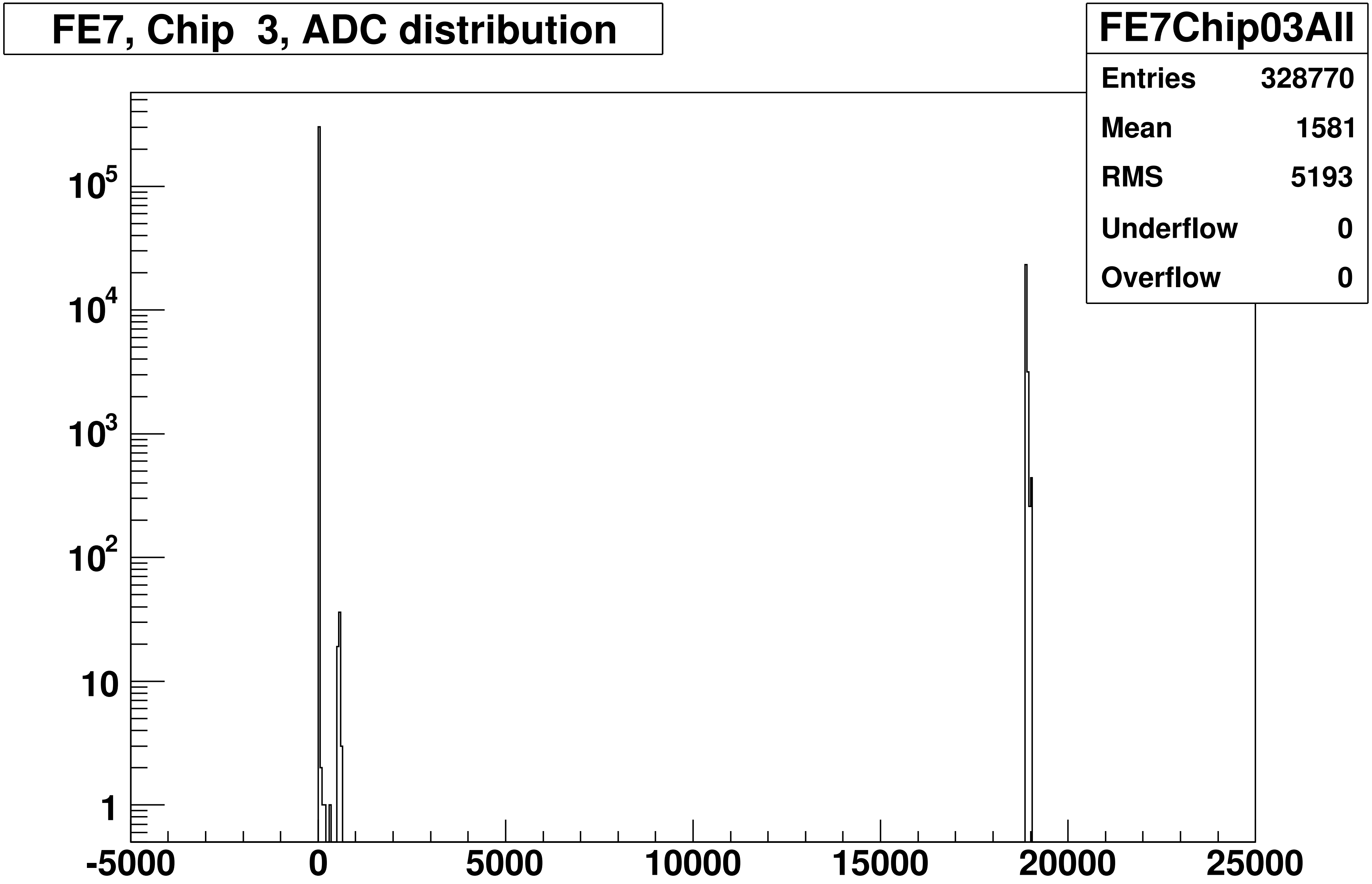
FE7, Chip 2, ADC distribution
FE7Chip02All
Entries 328770
Mean 1537
RMS 5121
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



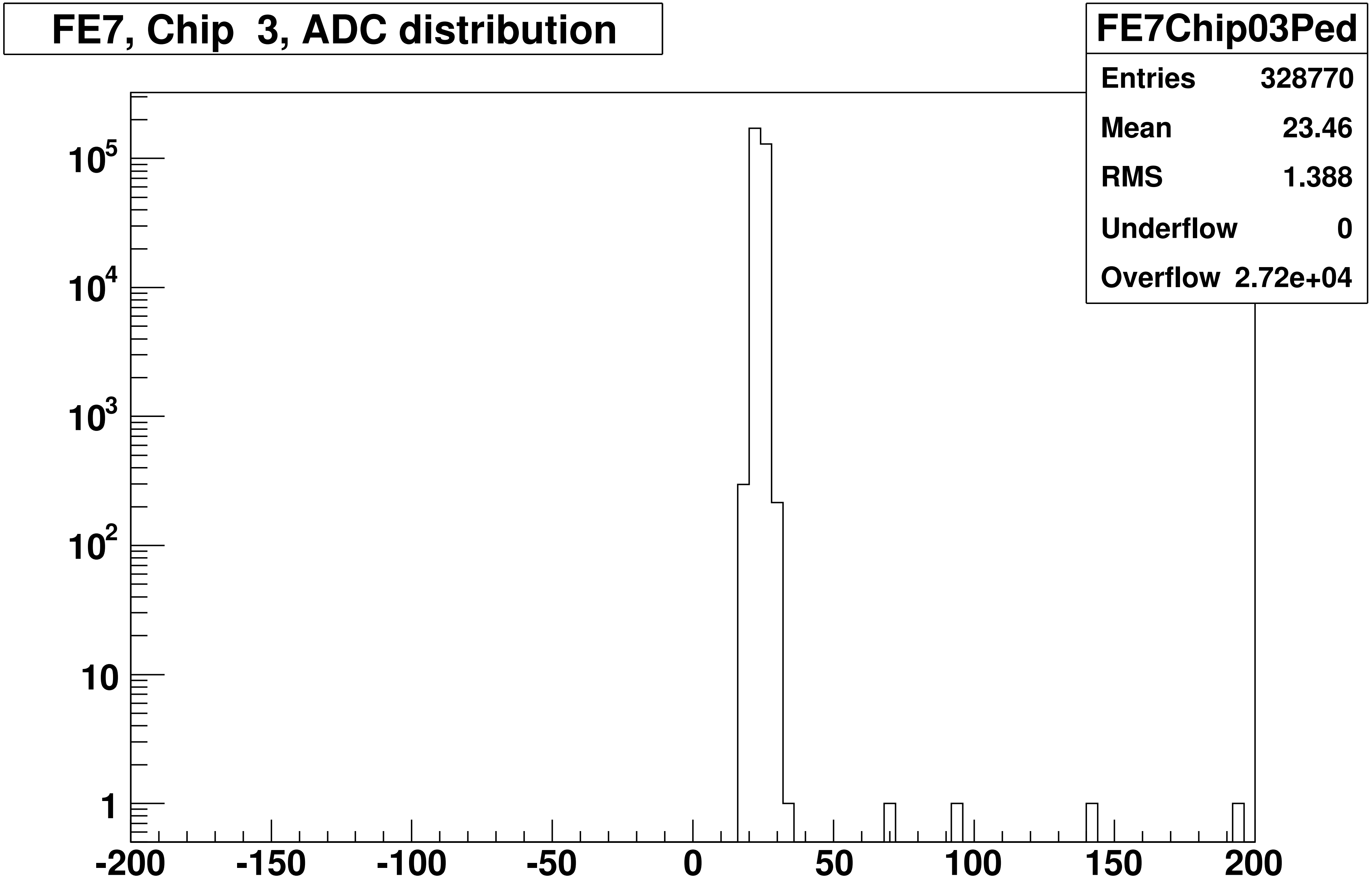
FE7, Chip 2, ADC distribution
FE7Chip02Ped
Entries 328770
Mean 14.99
RMS 1.381
Underflow 0
Overflow 2.71e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
200

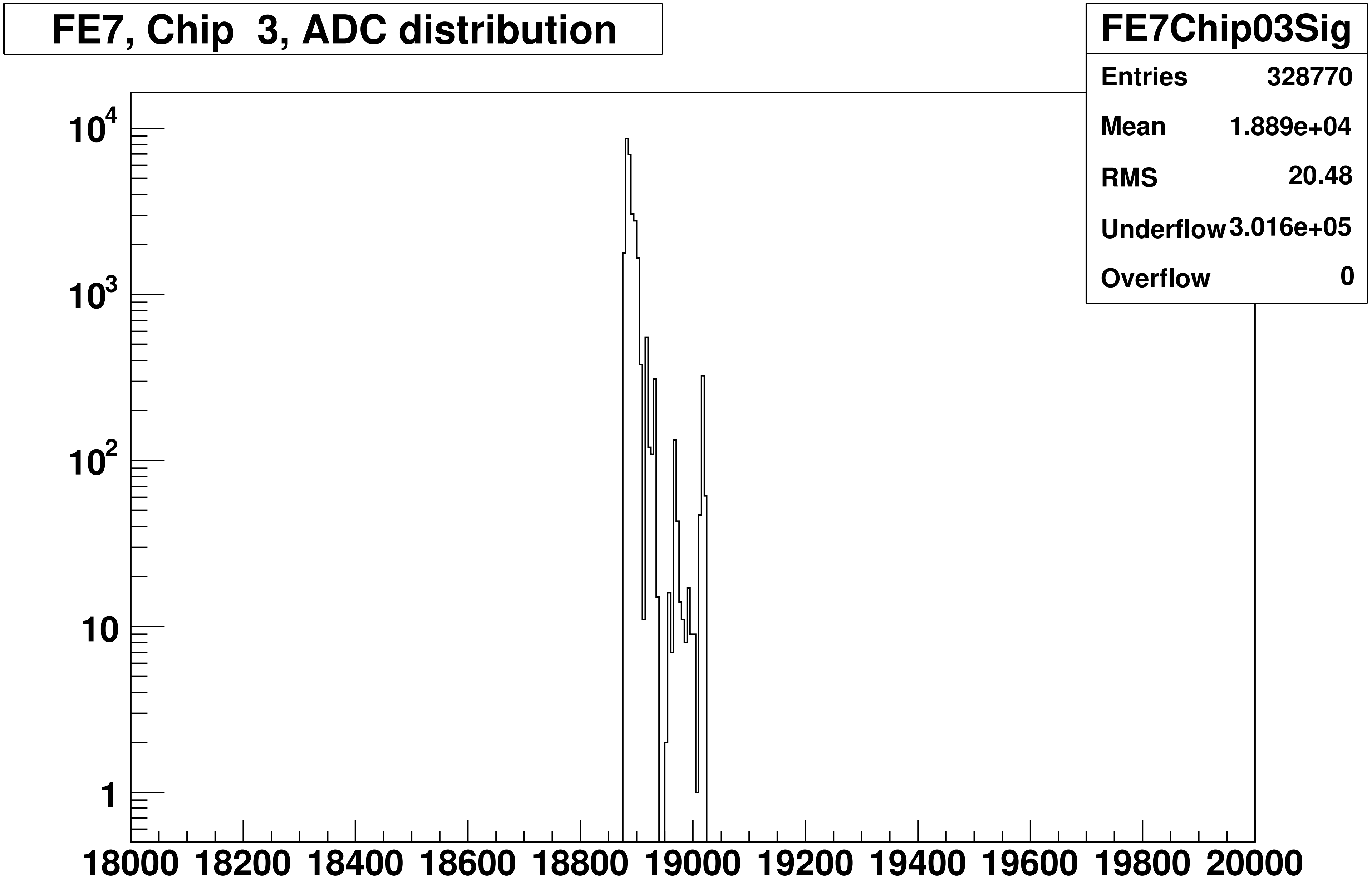


FE7, Chip 2, ADC distribution
FE7Chip02Sig
Entries 328770
Mean 1.878e+04
RMS 11.44
Underflow 3.021e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000

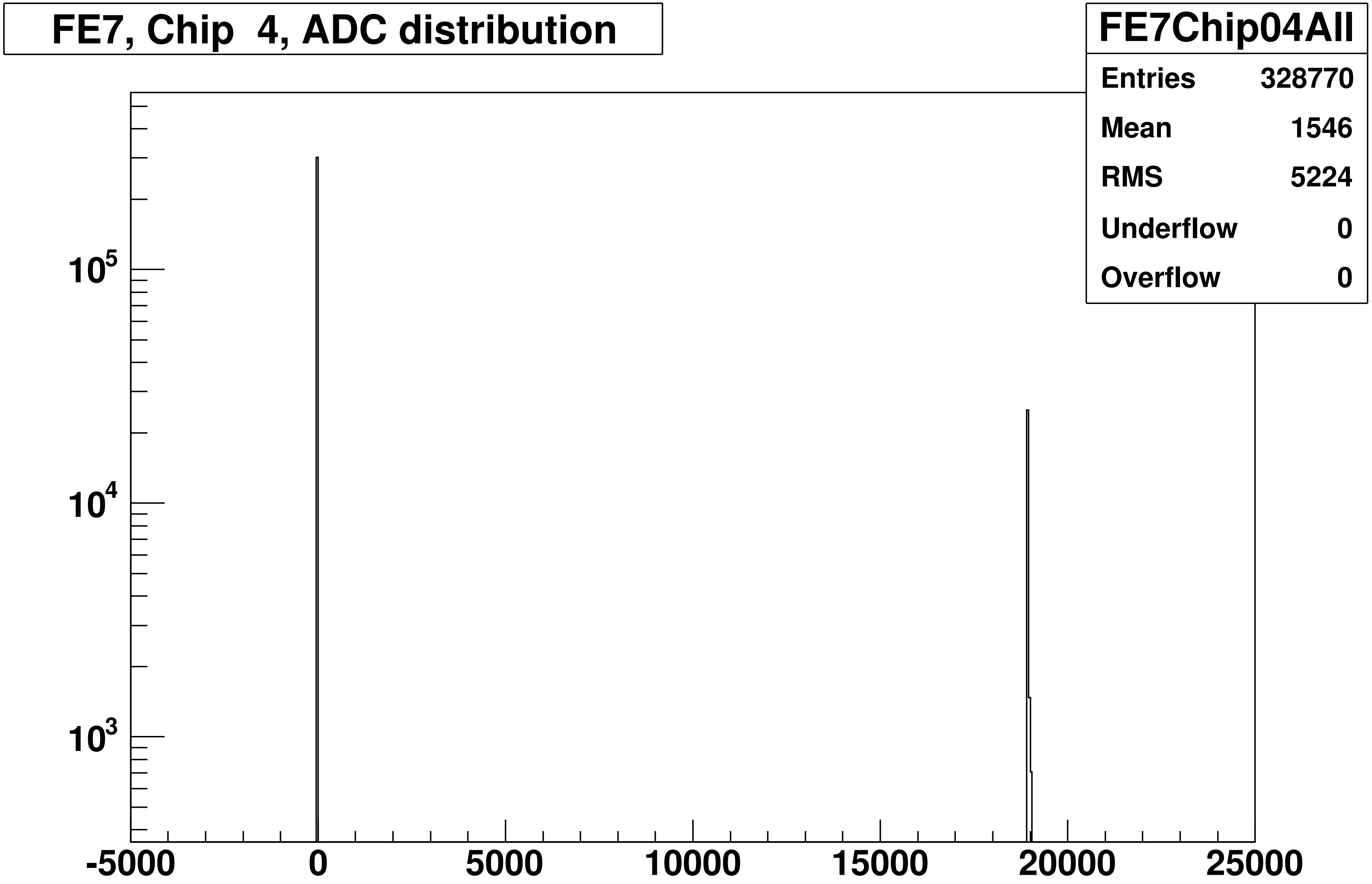


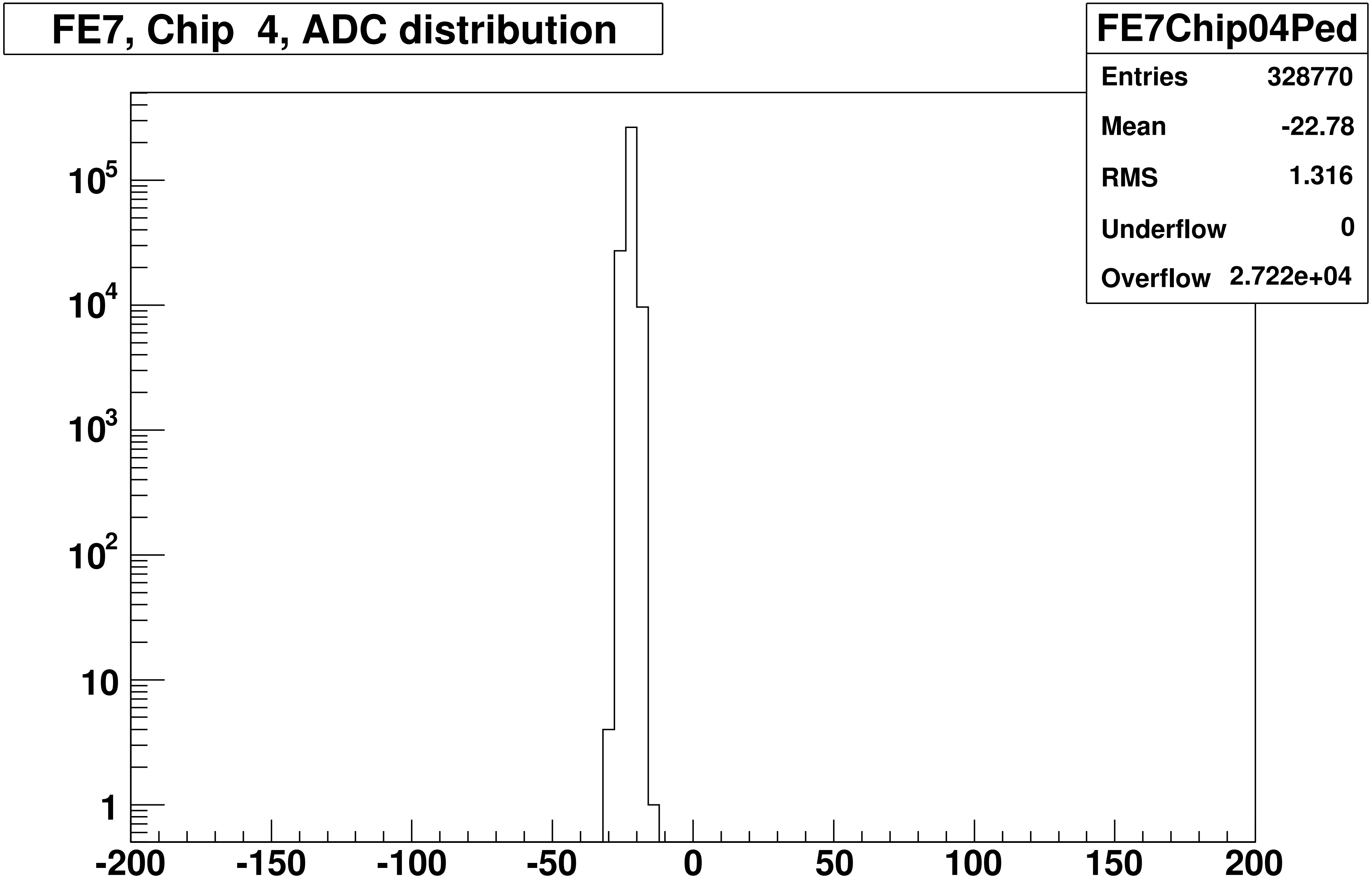
FE7, Chip 3, ADC distribution
FE7Chip03All
Entries 328770
Mean 1581
RMS 5193
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000

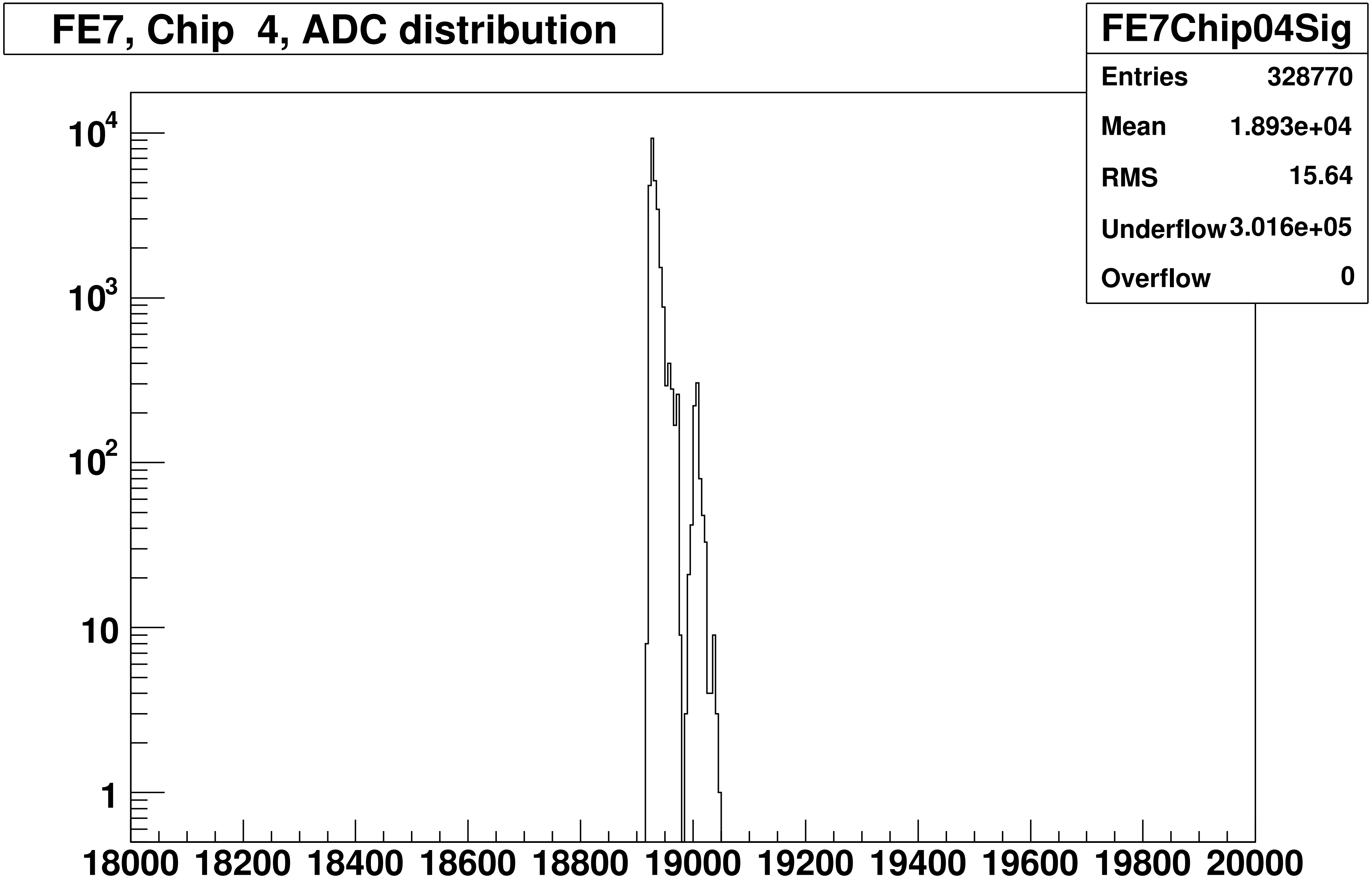

FE7, Chip 3, ADC distribution
FE7Chip03Ped
Entries 328770
Mean 23.46
RMS 1.388
Underflow 0
Overflow 2.72e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
200

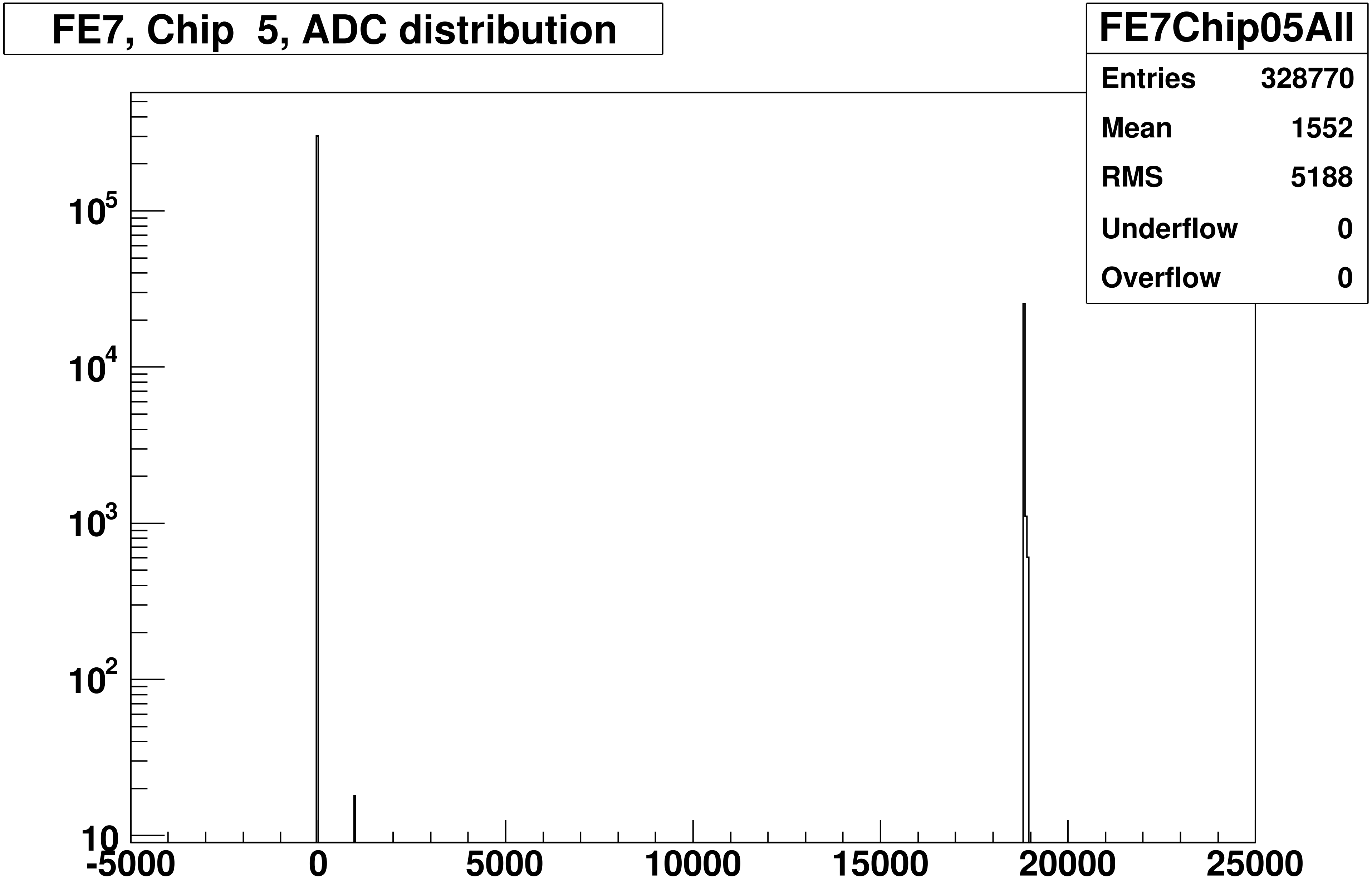


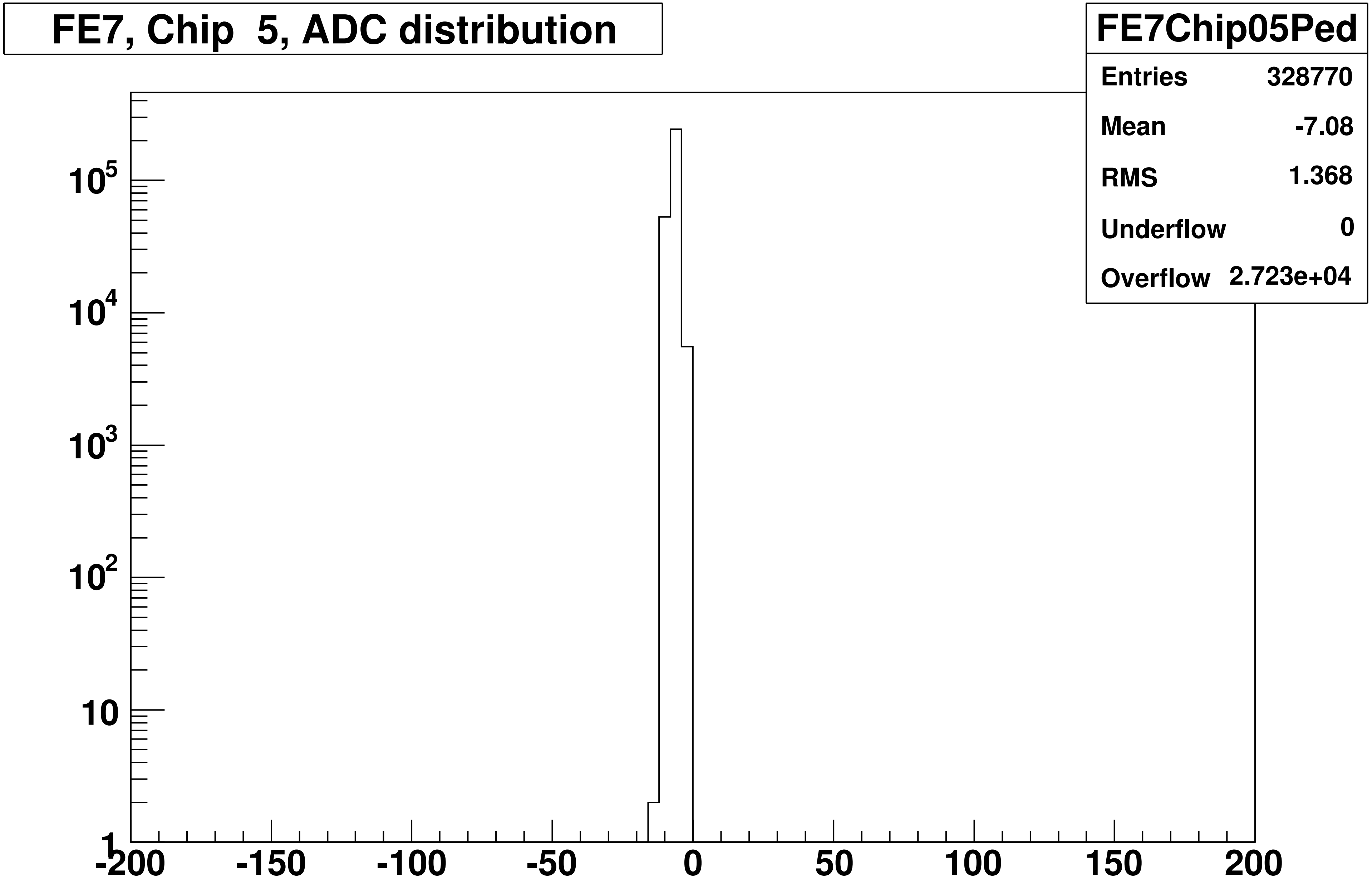
FE7, Chip 3, ADC distribution
FE7Chip03Sig
Entries 328770
Mean 1.889e+04
RMS 20.48
Underflow 3.016e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000

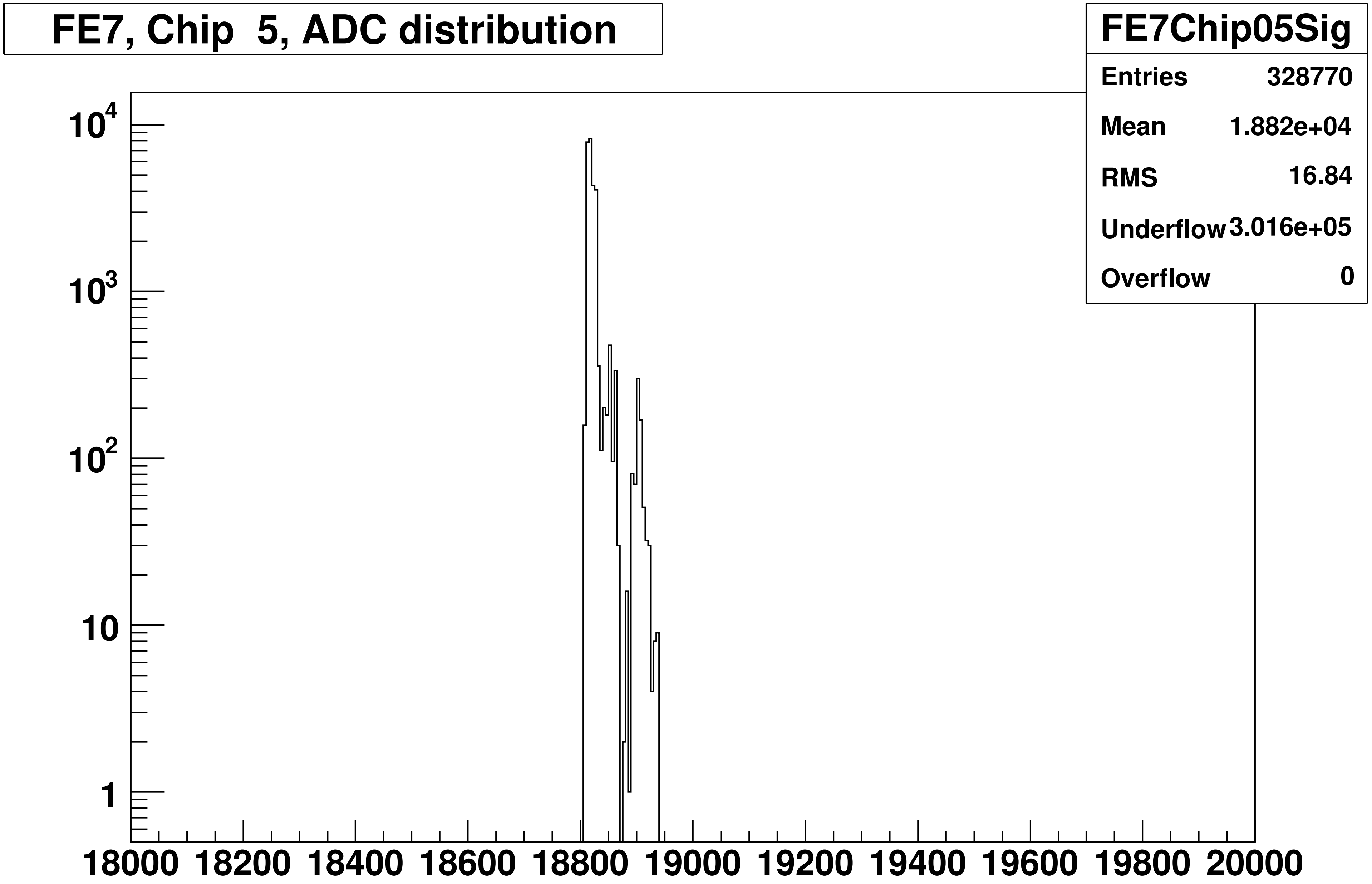

FE7, Chip 4, ADC distribution
FE7Chip04All
Entries 328770
Mean 1546
RMS 5224
Underflow 0
Overflow 0
10^5
10^4
10^3
-5000
0
5000
10000
15000
20000
25000


FE7, Chip 4, ADC distribution
FE7Chip04Ped
Entries 328770
Mean -22.78
RMS 1.316
Underflow 0
Overflow 2.722e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
200


FE7, Chip 4, ADC distribution
FE7Chip04Sig
Entries 328770
Mean 1.893e+04
RMS 15.64
Underflow 3.016e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE7, Chip 5, ADC distribution
FE7Chip05All
Entries 328770
Mean 1552
RMS 5188
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE7, Chip 5, ADC distribution
FE7Chip05Ped
Entries 328770
Mean -7.08
RMS 1.368
Underflow 0
Overflow 2.723e+04
1
10
10^2
10^3
10^4
10^5
-200
-150
-100
-50
0
50
100
150
200


FE7, Chip 5, ADC distribution
FE7Chip05Sig
Entries 328770
Mean 1.882e+04
RMS 16.84
Underflow 3.016e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
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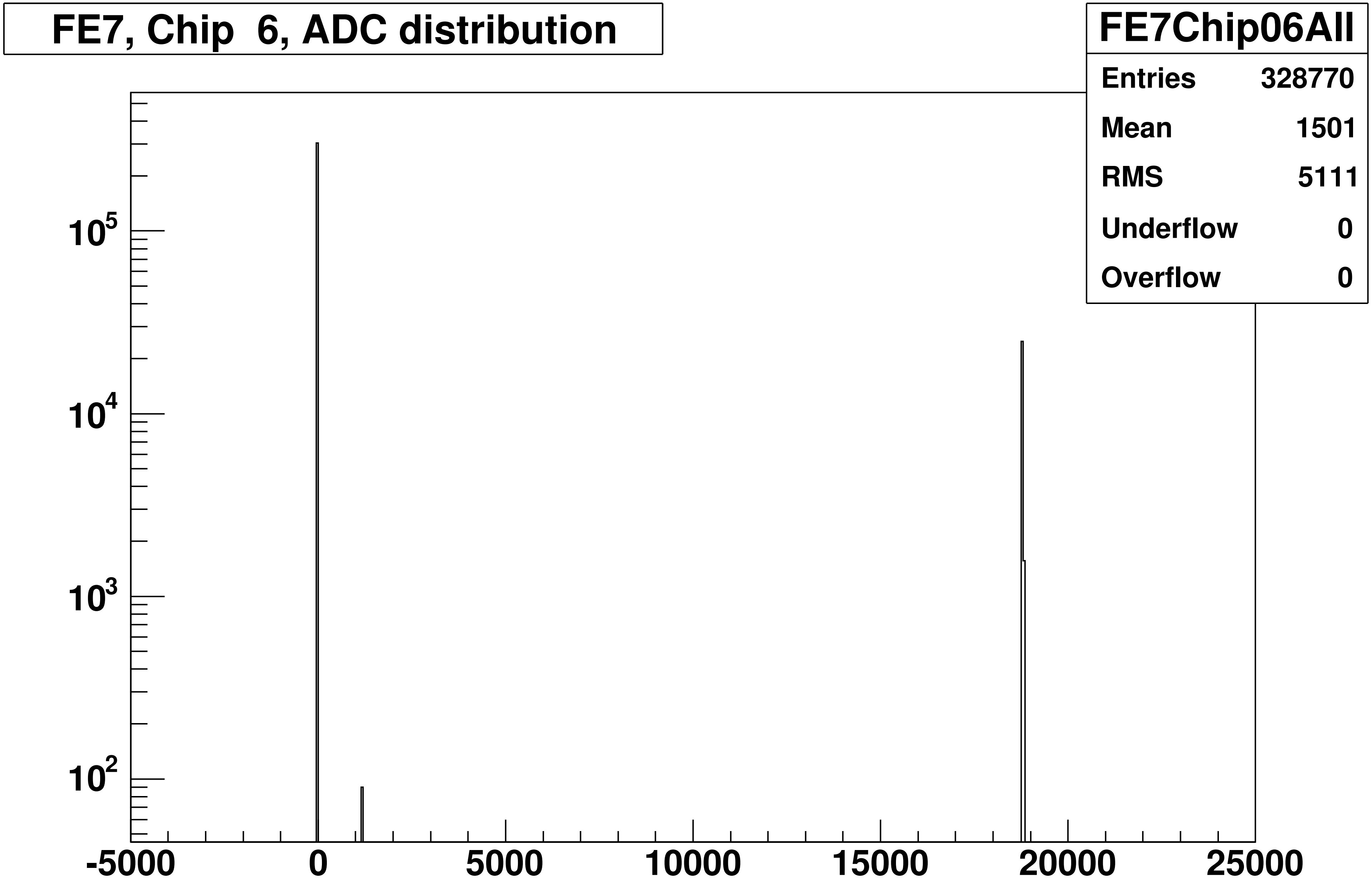
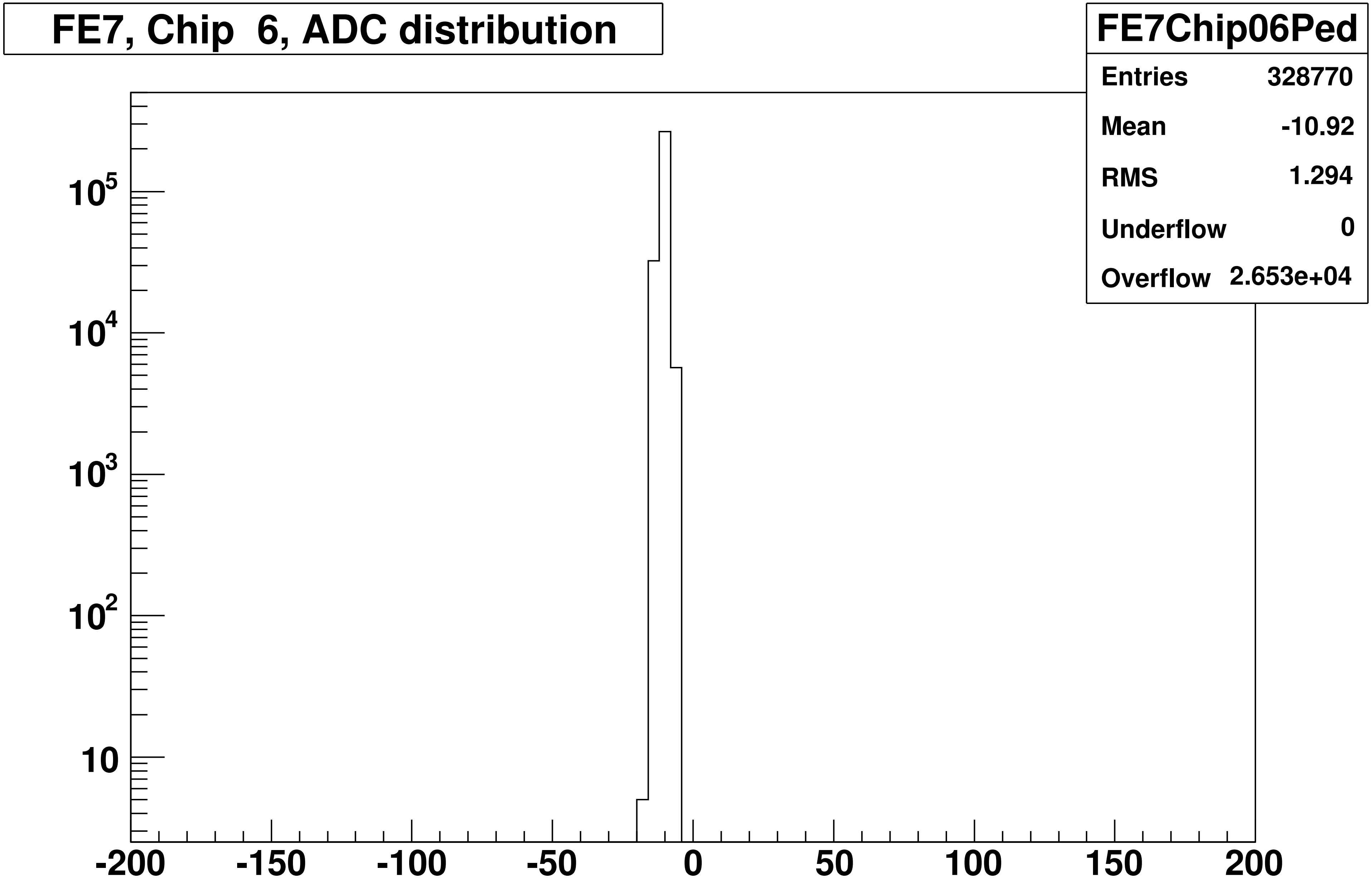
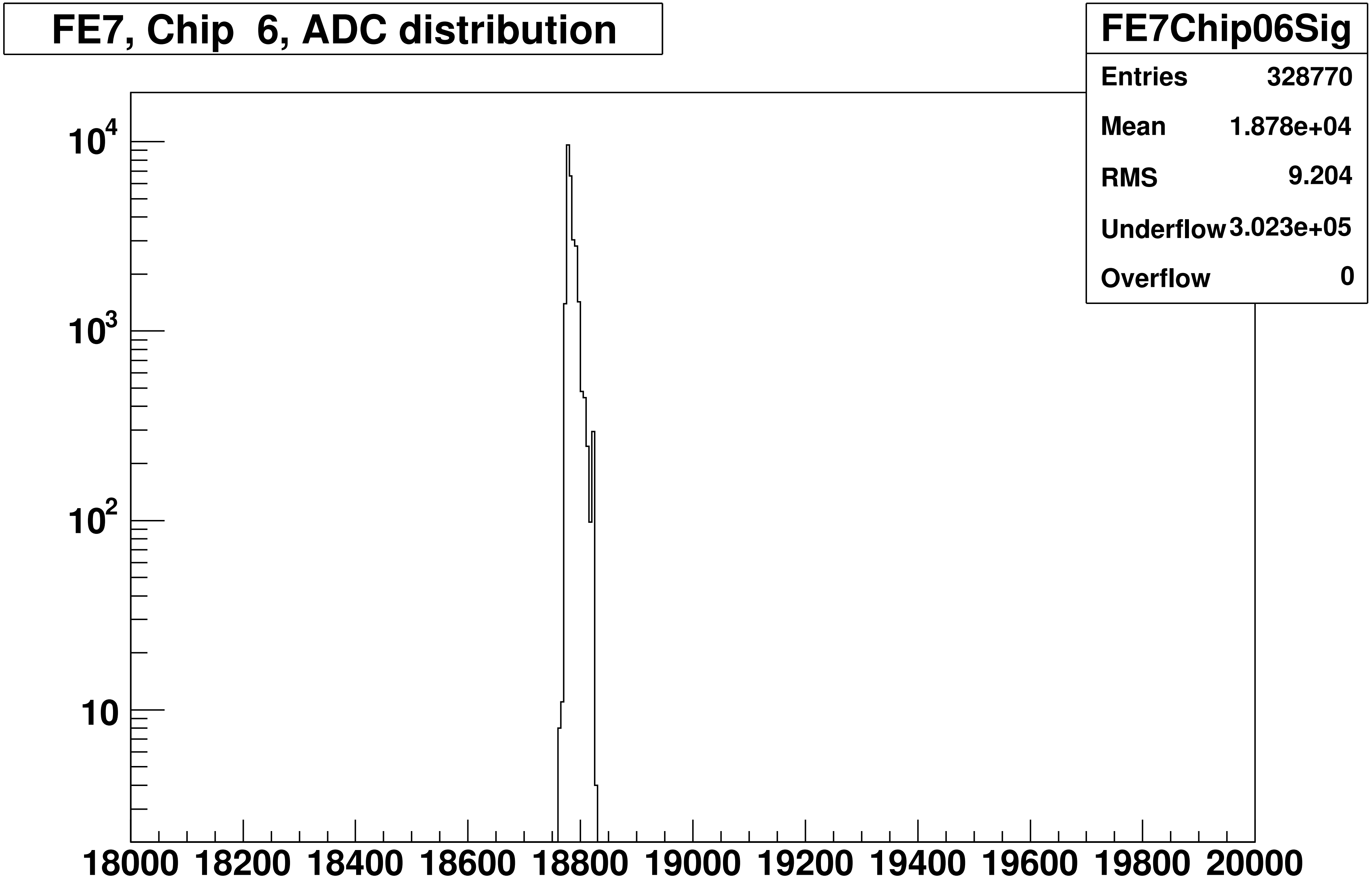
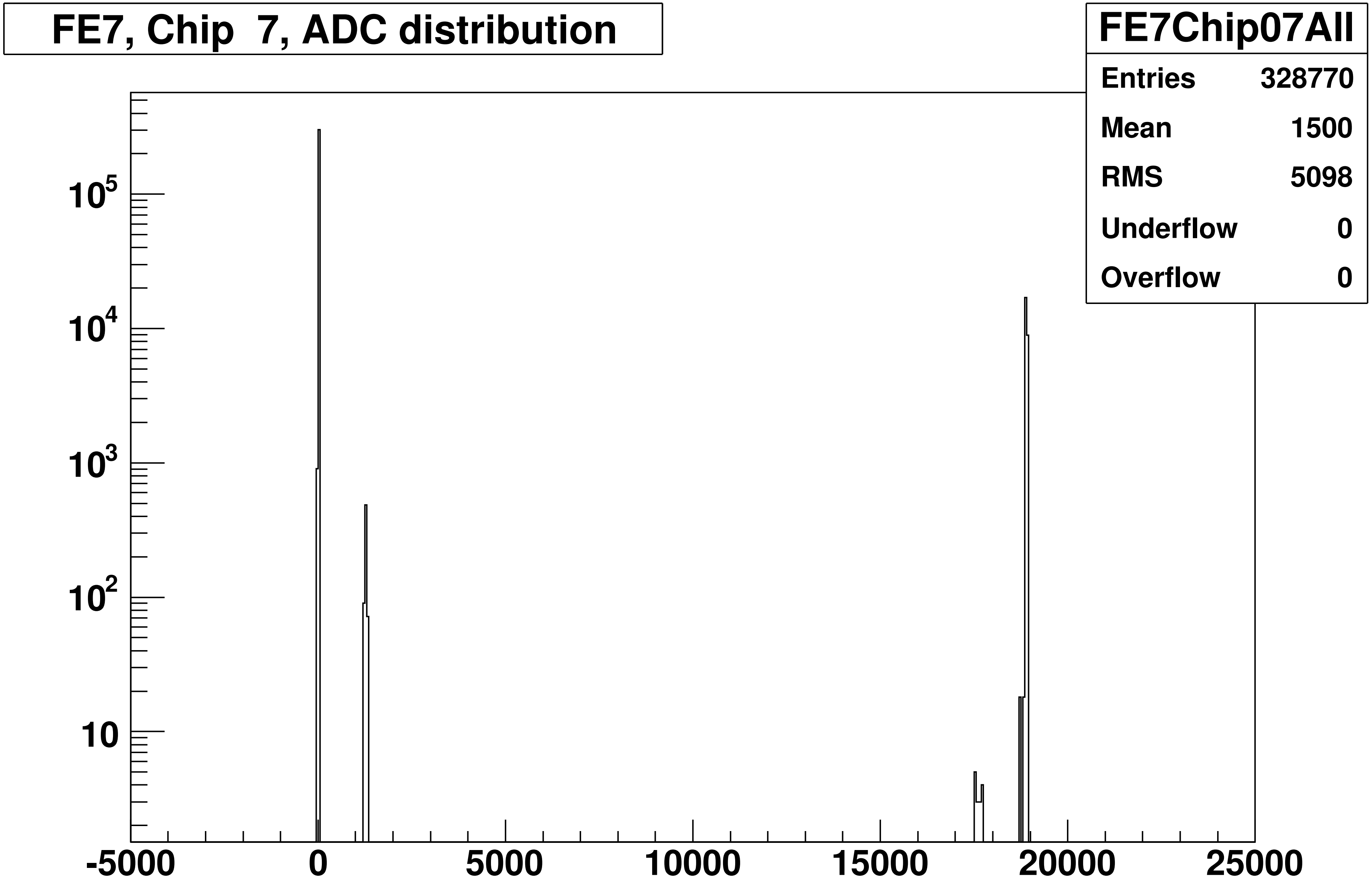
19800
20000


FE7, Chip 6, ADC distribution
FE7Chip06All
Entries 328770
Mean 1501
RMS 5111
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000

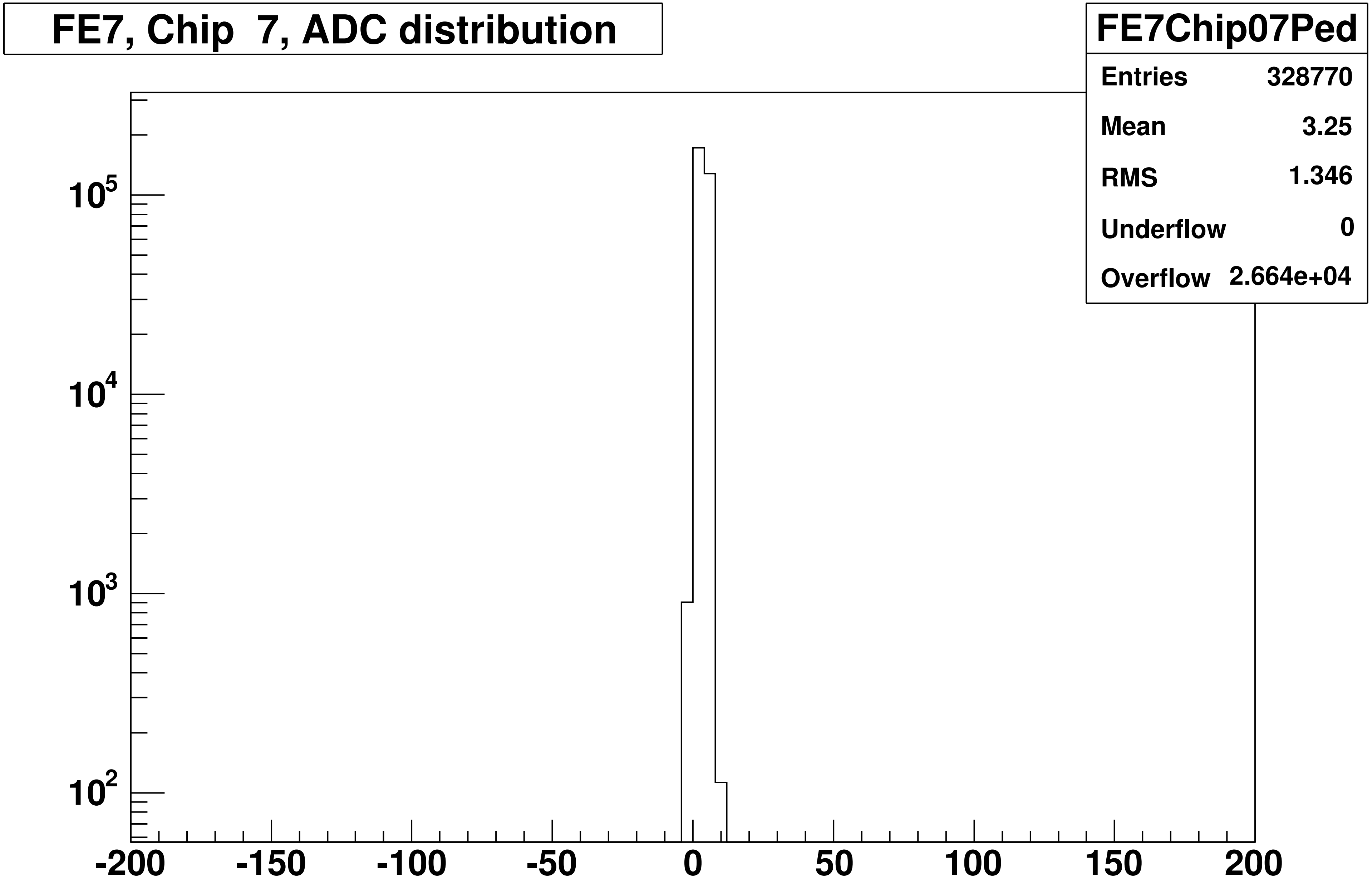

FE7, Chip 6, ADC distribution
FE7Chip06Ped
Entries 328770
Mean -10.92
RMS 1.294
Underflow 0
Overflow 2.653e+04
10^5
10^4
10^3
10^2
10
-200
-150
-100
-50
0
50
100
150
200

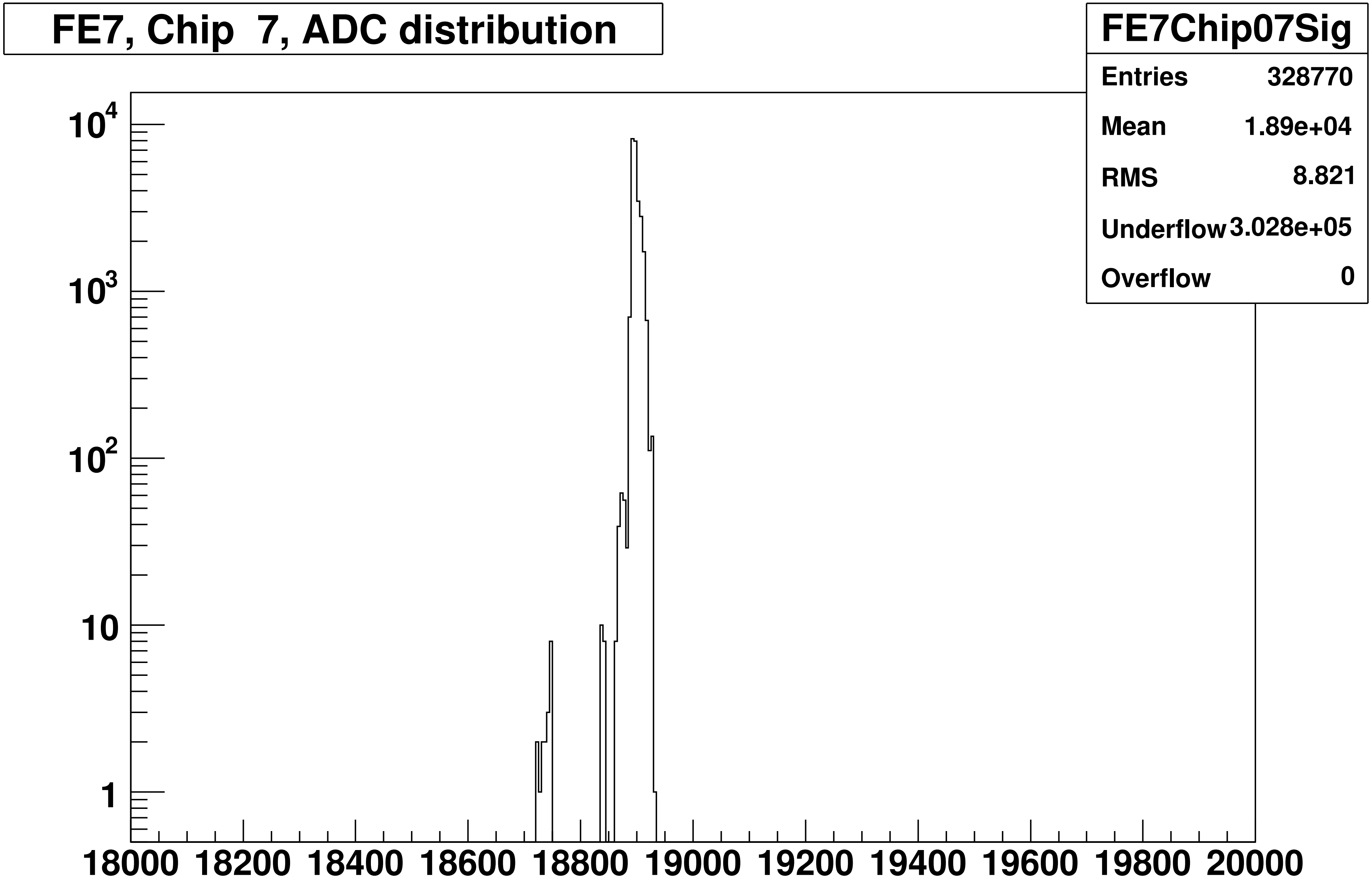


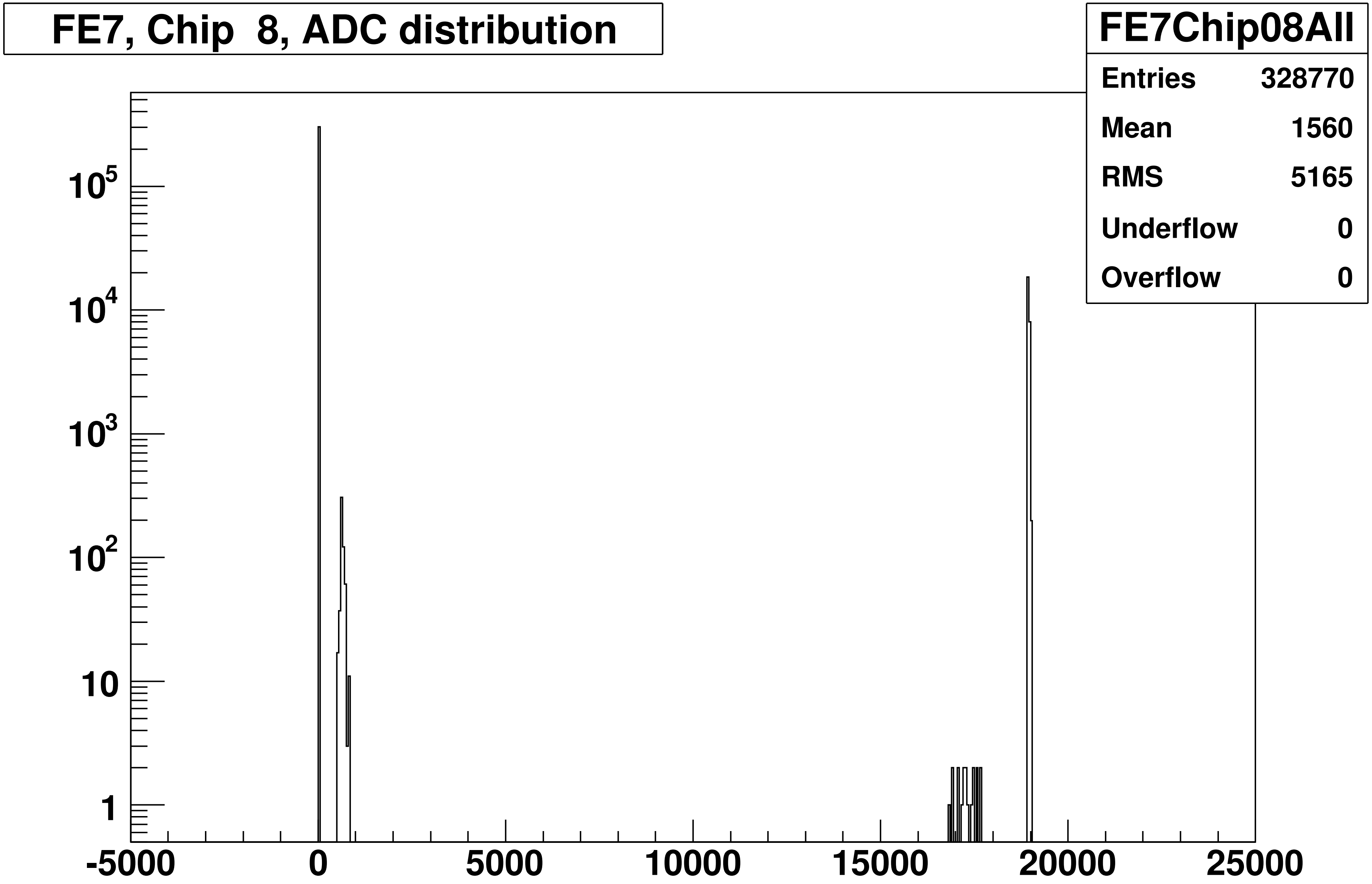
FE7, Chip 6, ADC distribution
FE7Chip06Sig
Entries 328770
Mean 1.878e+04
RMS 9.204
Underflow 3.023e+05
Overflow 0
10^4
10^3
10^2
10
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000



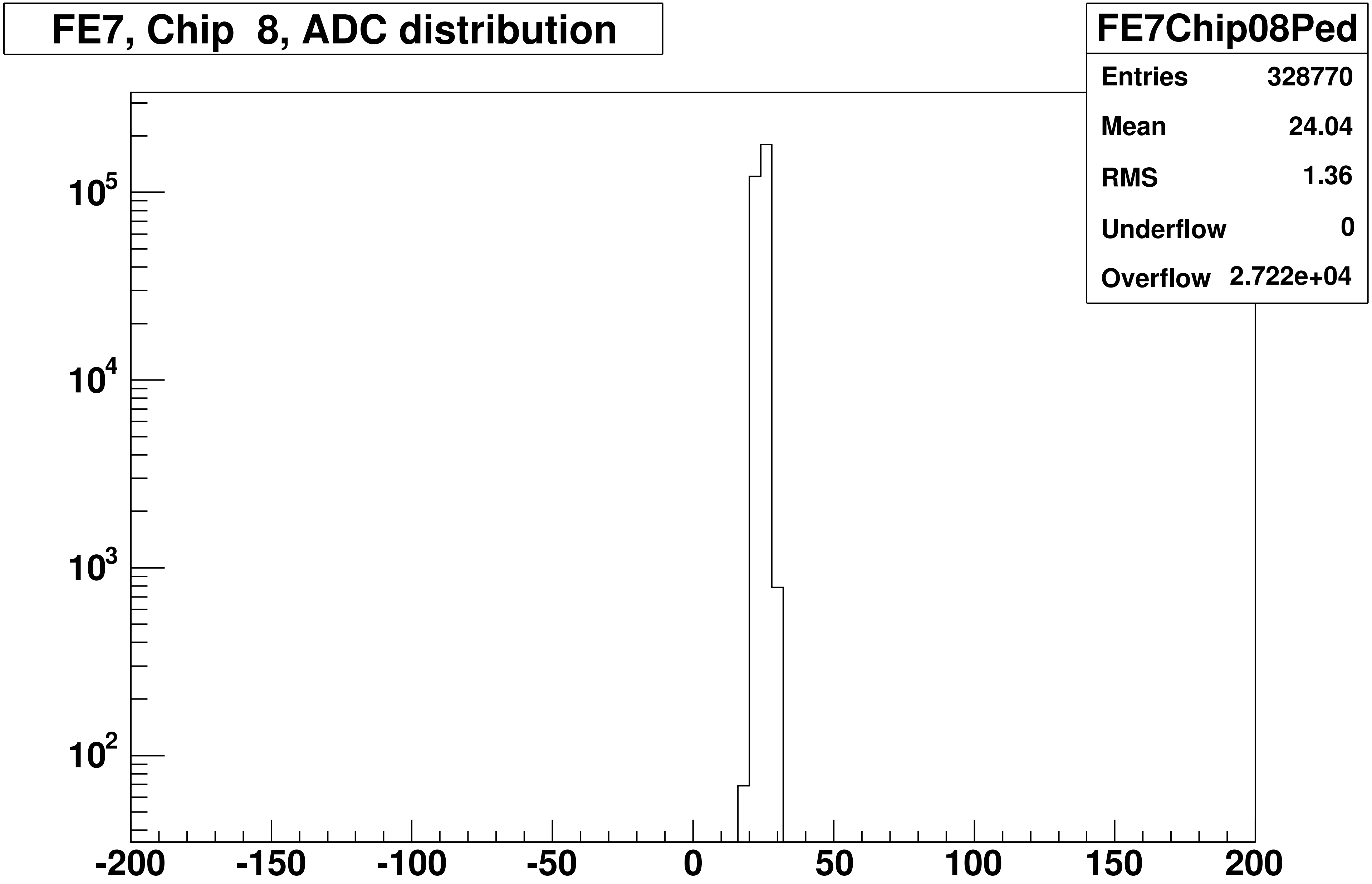
FE7, Chip 7, ADC distribution
FE7Chip07All
Entries 328770
Mean 1500
RMS 5098
Underflow 0
Overflow 0
10
10^2
10^3
10^4
10^5
-5000
0
5000
10000
15000
20000
25000


FE7, Chip 7, ADC distribution
FE7Chip07Ped
Entries 328770
Mean 3.25
RMS 1.346
Underflow 0
Overflow 2.664e+04
10^5
10^4
10^3
10^2
-200
-150
-100
-50
0
50
100
150
200

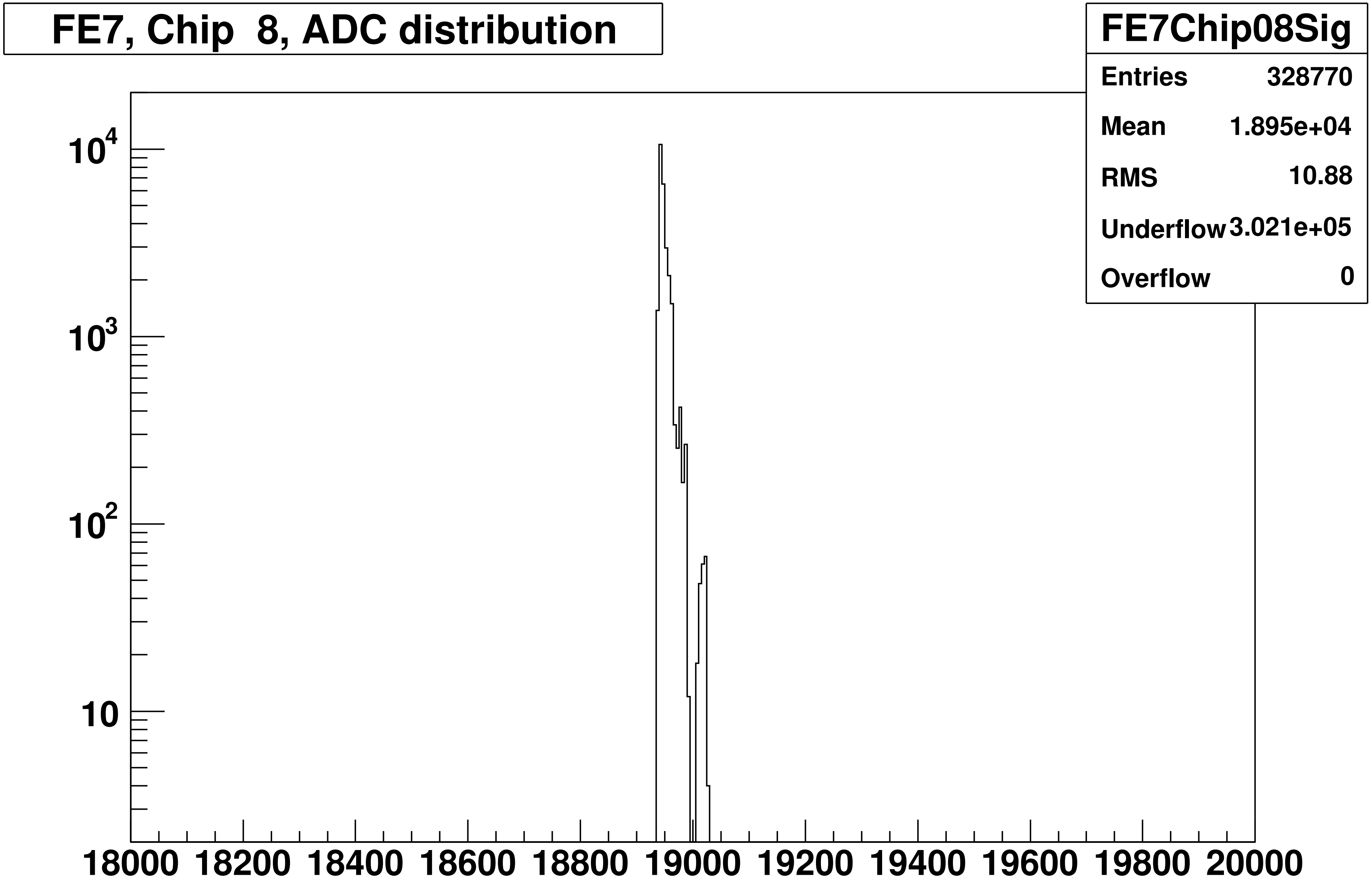

FE7, Chip 7, ADC distribution
FE7Chip07Sig
Entries 328770
Mean 1.89e+04
RMS 8.821
Underflow 3.028e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000

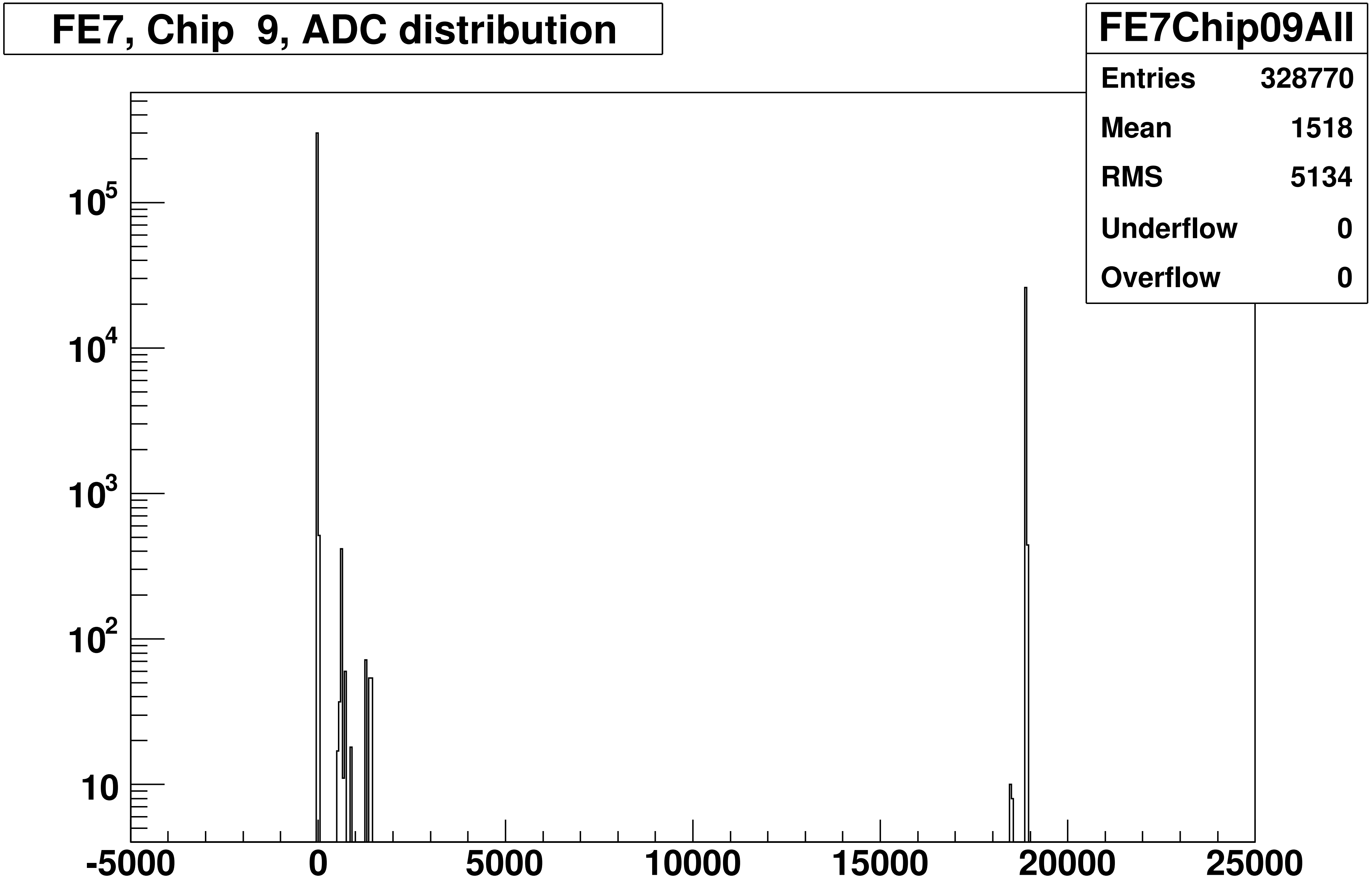


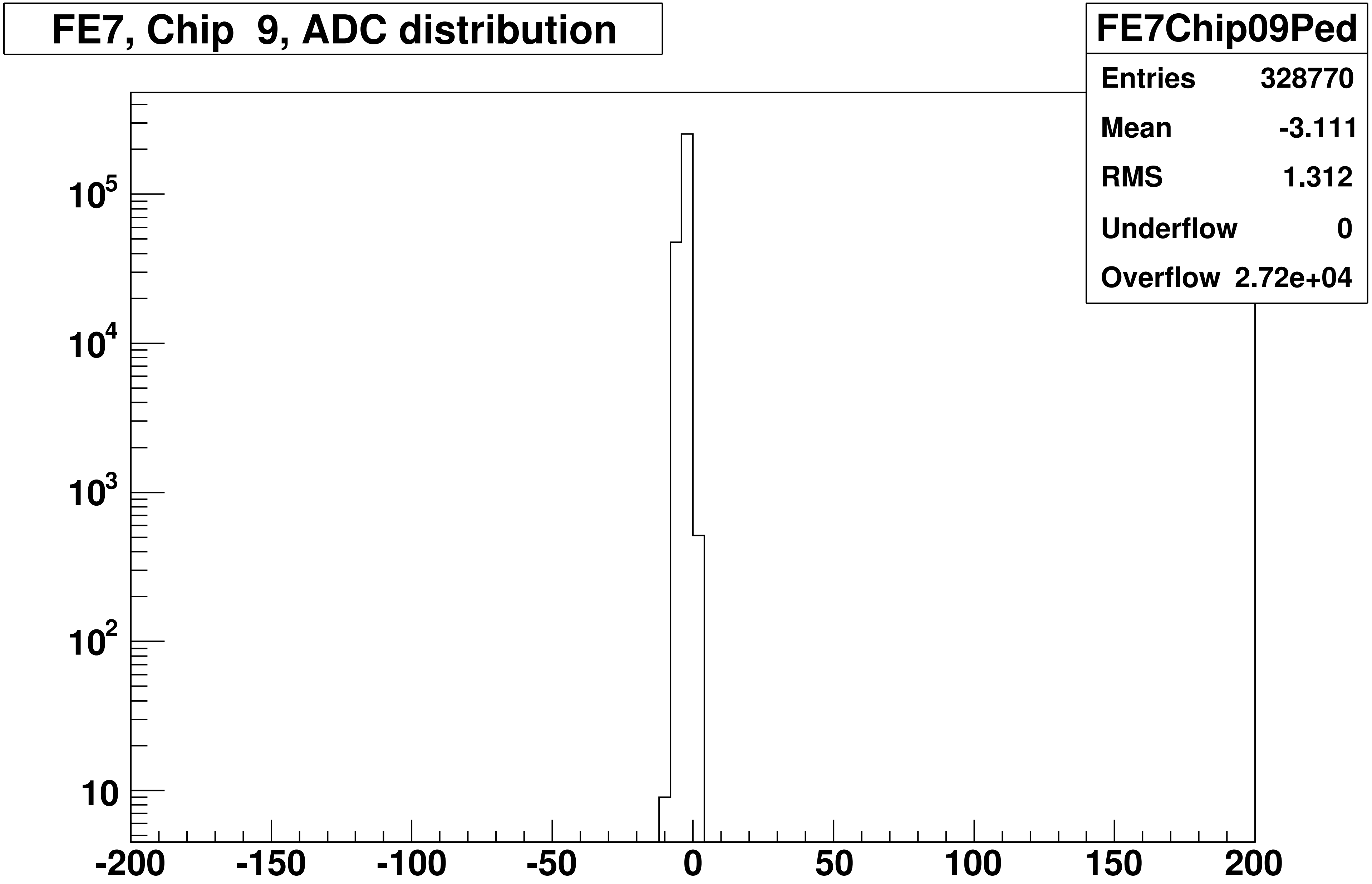
FE7, Chip 8, ADC distribution
FE7Chip08All
Entries 328770
Mean 1560
RMS 5165
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000

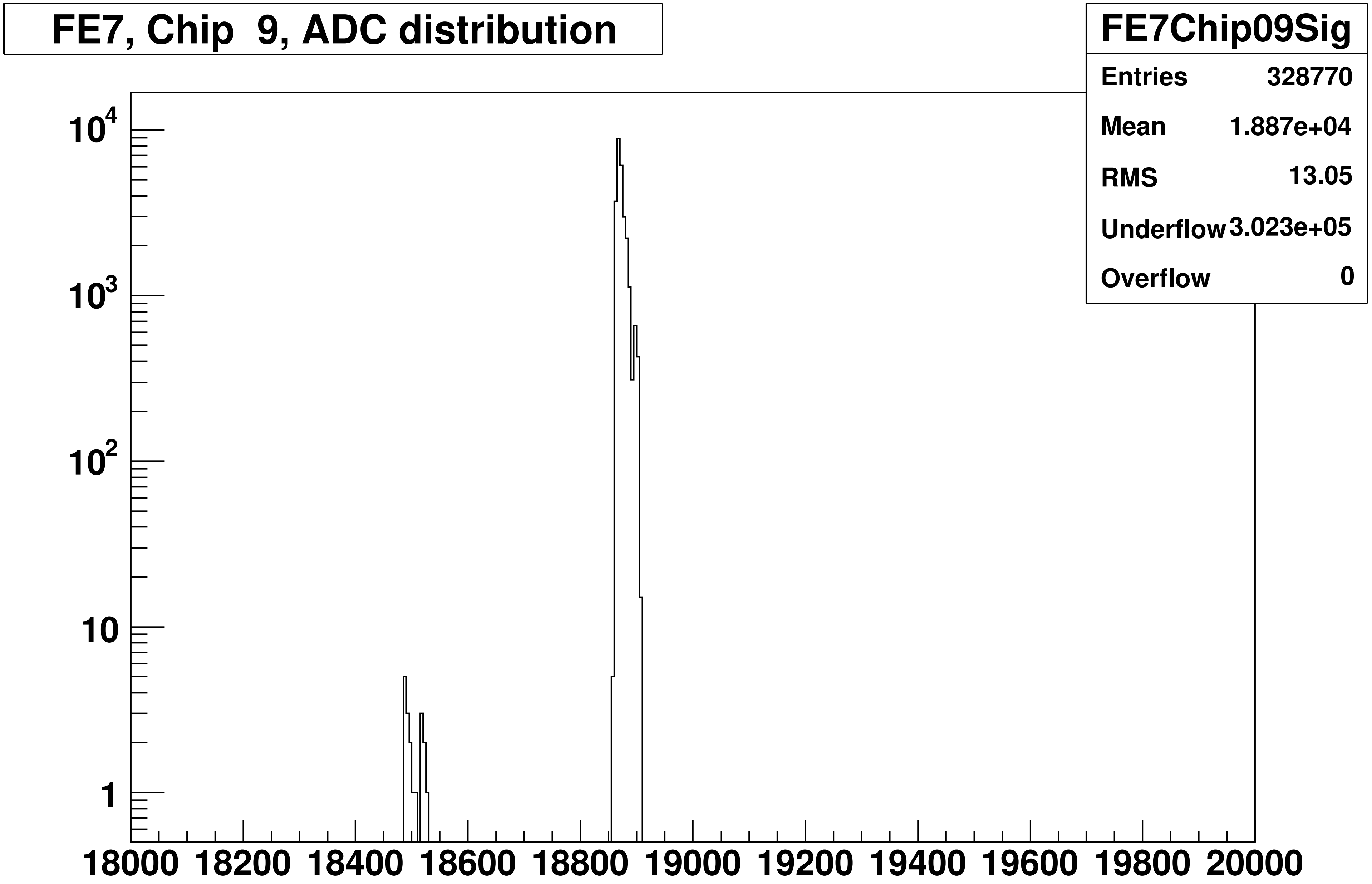


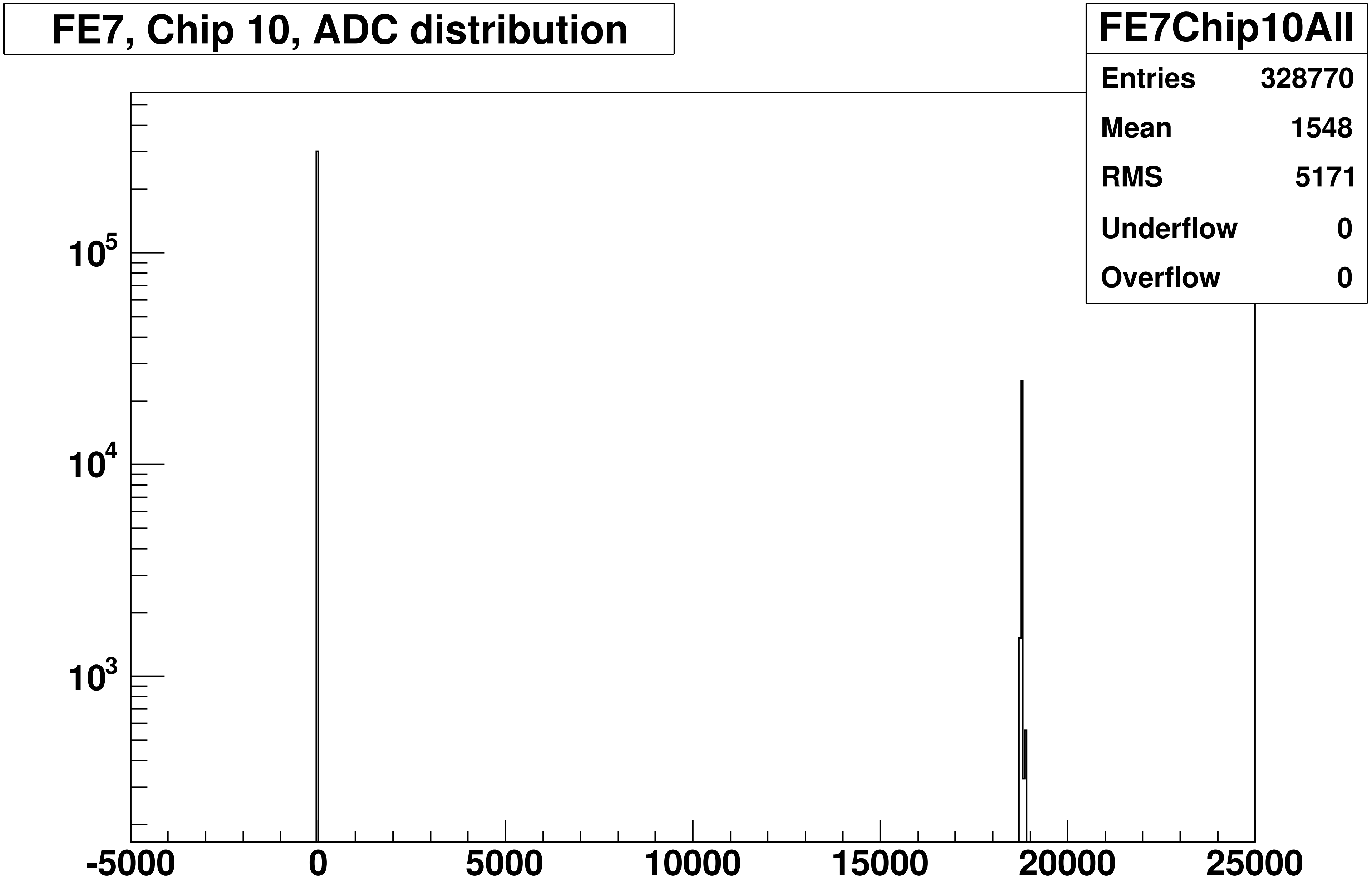
FE7, Chip 8, ADC distribution
FE7Chip08Ped
Entries 328770
Mean 24.04
RMS 1.36
Underflow 0
Overflow 2.722e+04
10^5
10^4
10^3
10^2
-200
-150
-100
-50
0
50
100
150
200


FE7, Chip 8, ADC distribution
FE7Chip08Sig
Entries 328770
Mean 1.895e+04
RMS 10.88
Underflow 3.021e+05
Overflow 0
10^4
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000

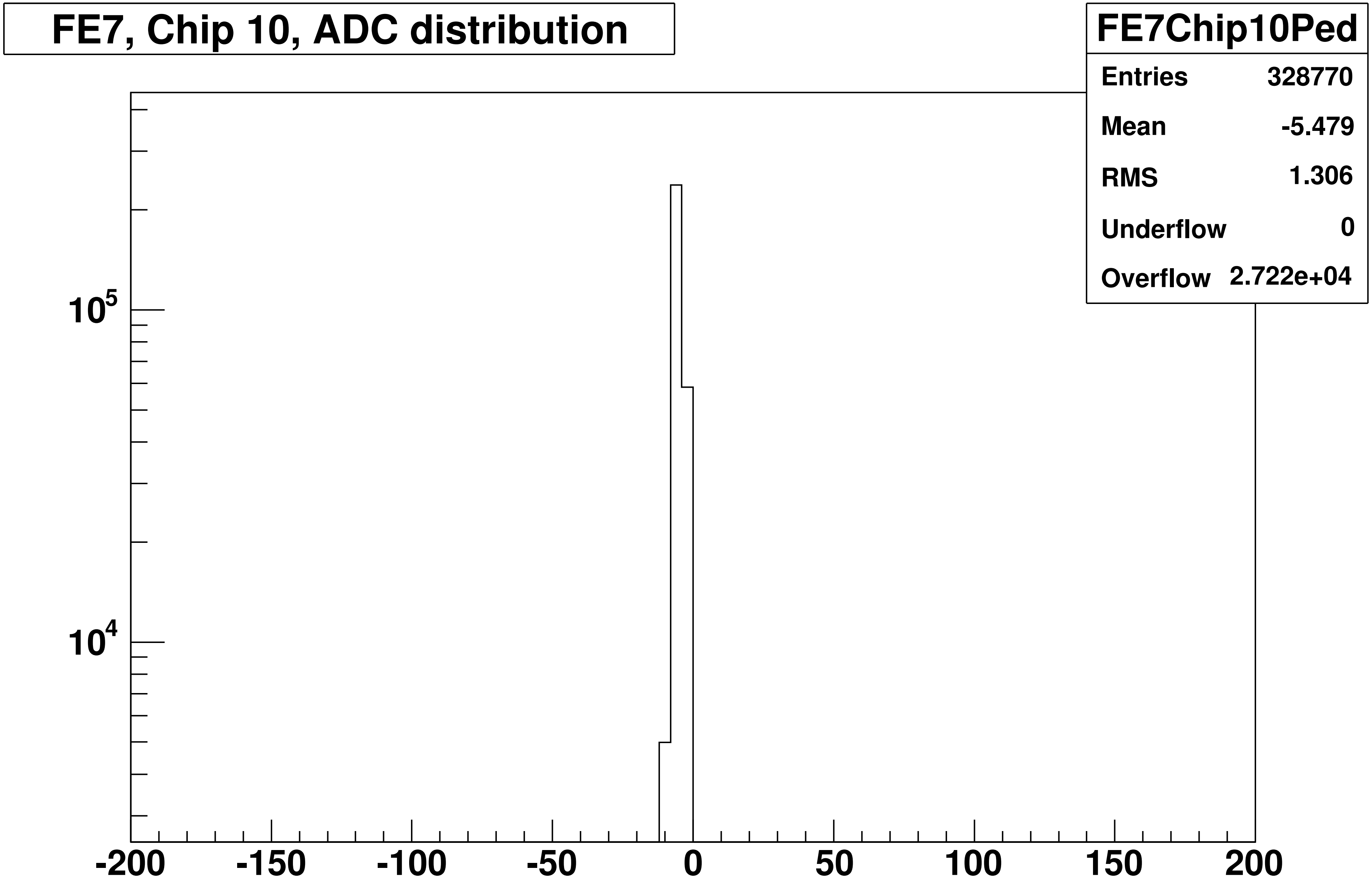

FE7, Chip 9, ADC distribution
FE7Chip09All
Entries 328770
Mean 1518
RMS 5134
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000

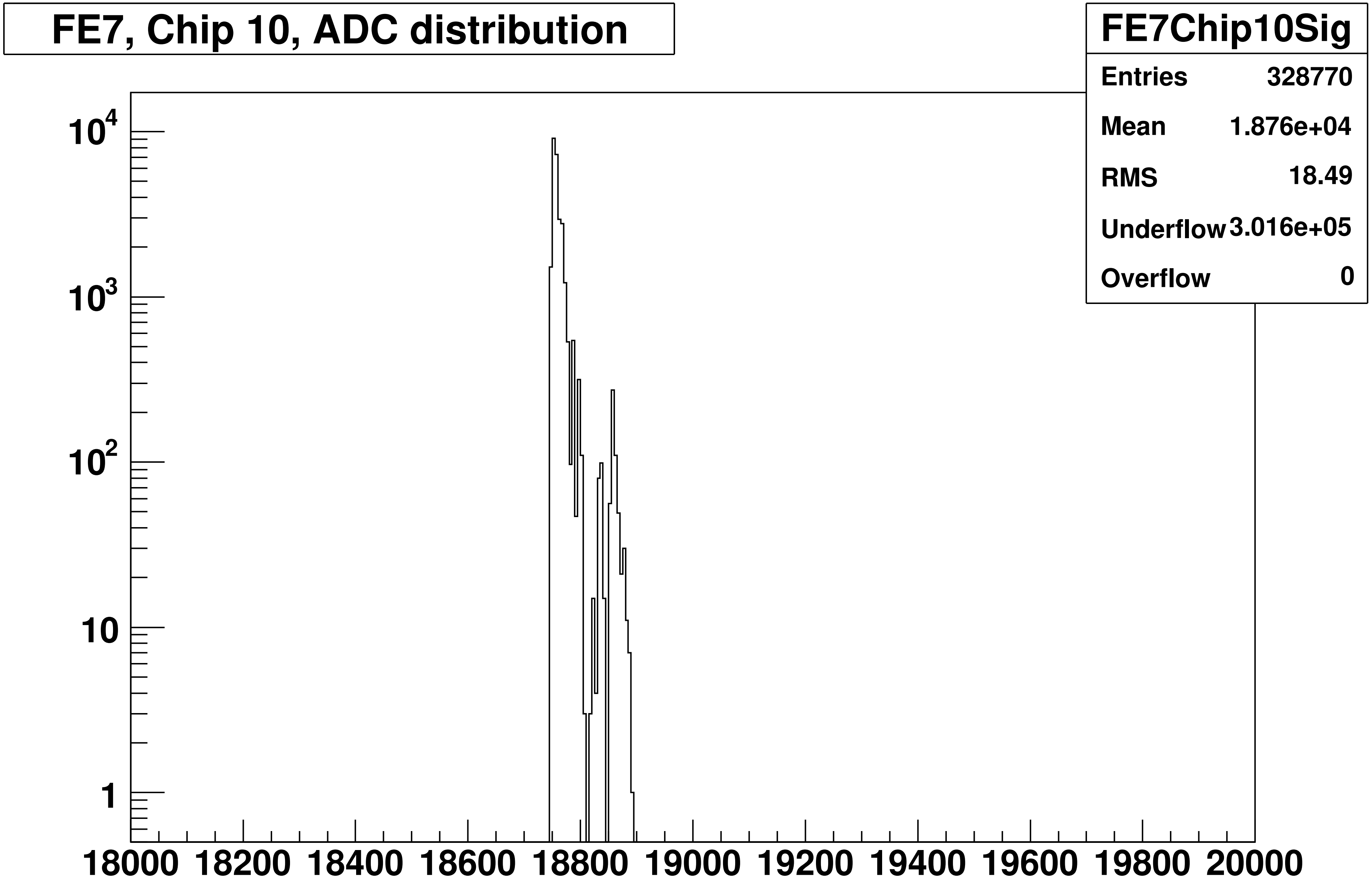

FE7, Chip 9, ADC distribution
FE7Chip09Ped
Entries 328770
Mean -3.111
RMS 1.312
Underflow 0
Overflow 2.72e+04
10^5
10^4
10^3
10^2
10
-200
-150
-100
-50
0
50
100
150
200


FE7, Chip 9, ADC distribution
FE7Chip09Sig
Entries 328770
Mean 1.887e+04
RMS 13.05
Underflow 3.023e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000

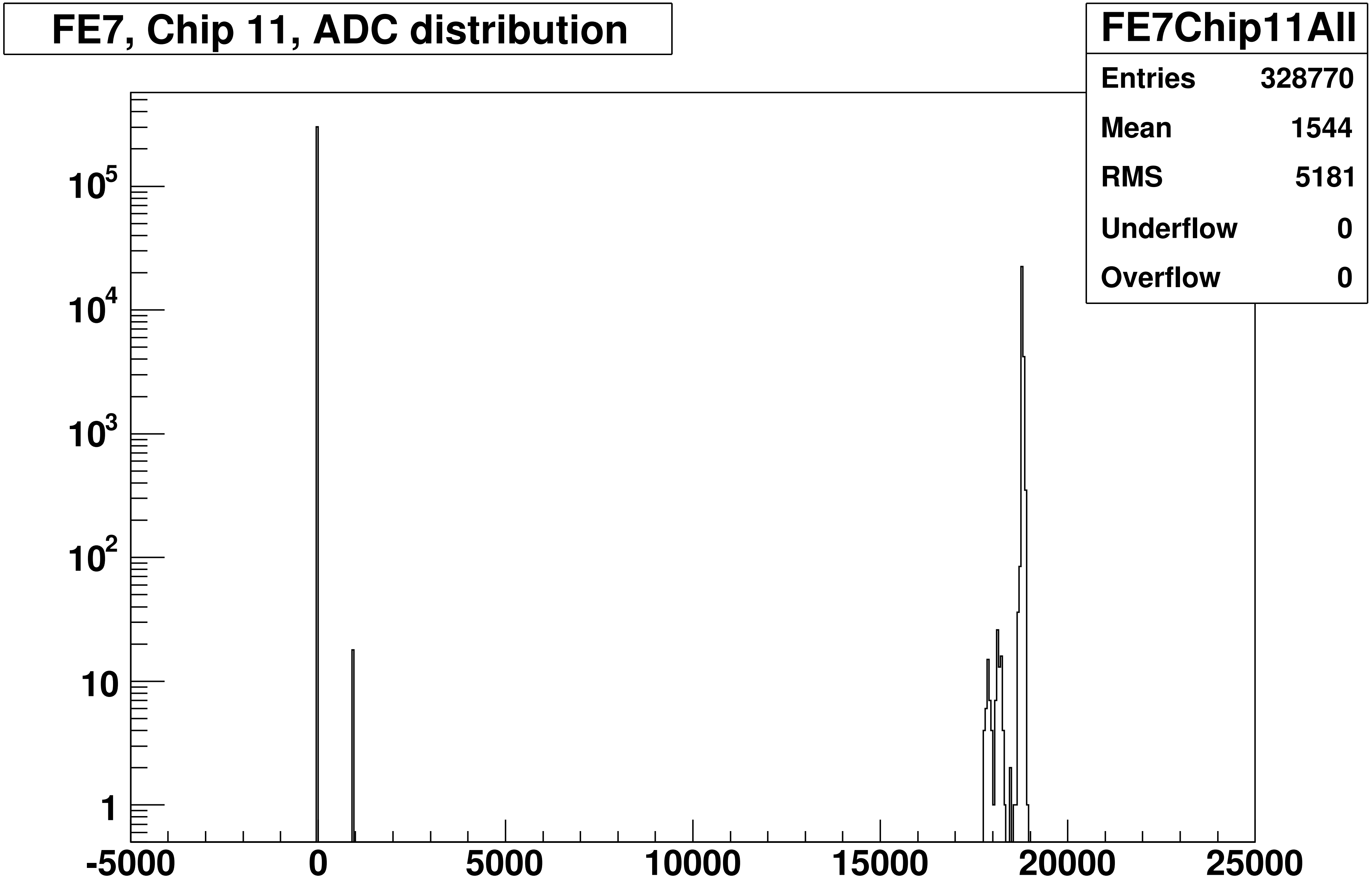


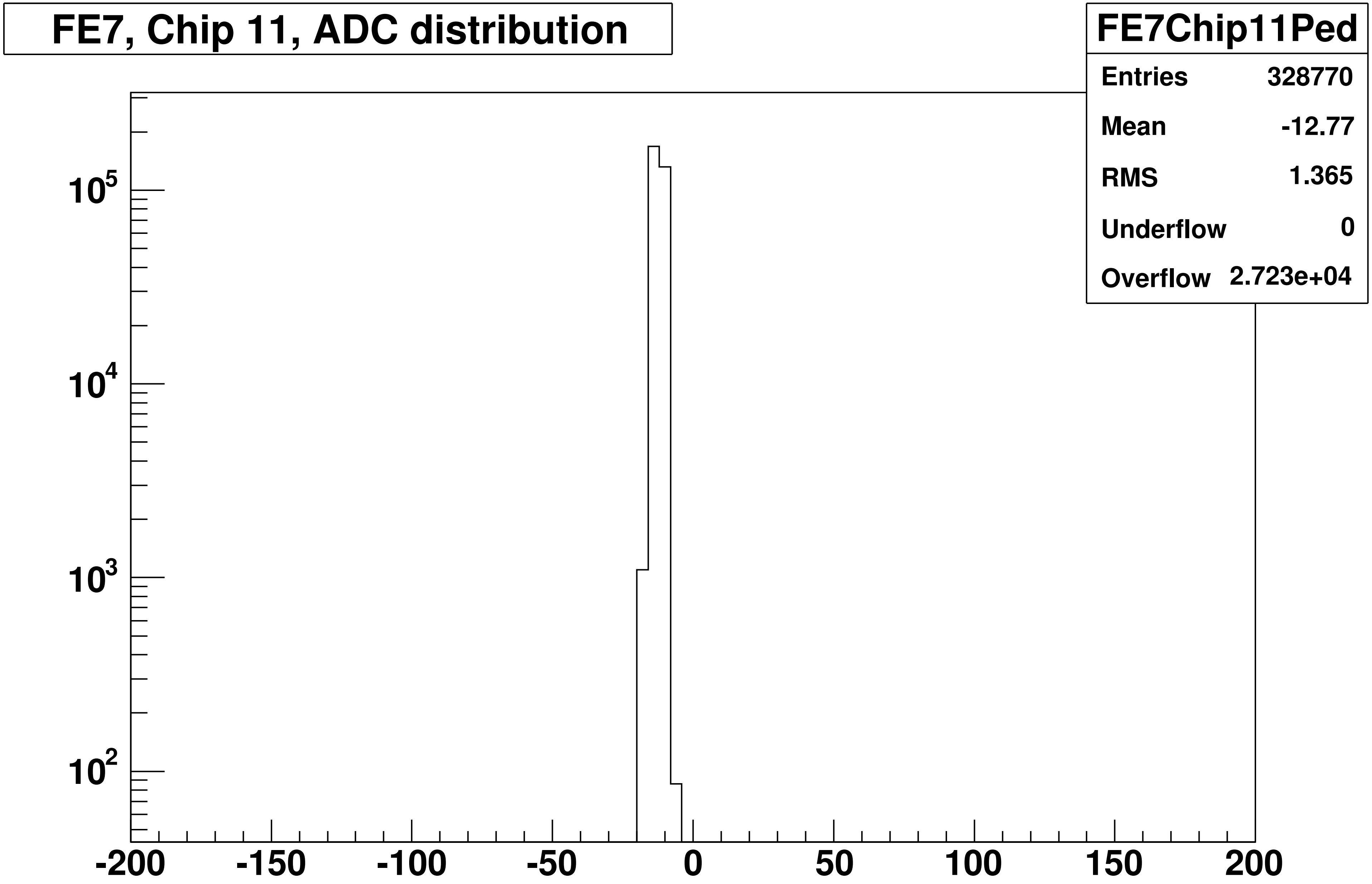
FE7, Chip 10, ADC distribution
FE7Chip10All
Entries 328770
Mean 1548
RMS 5171
Underflow 0
Overflow 0
10^5
10^4
10^3
-5000
0
5000
10000
15000
20000
25000

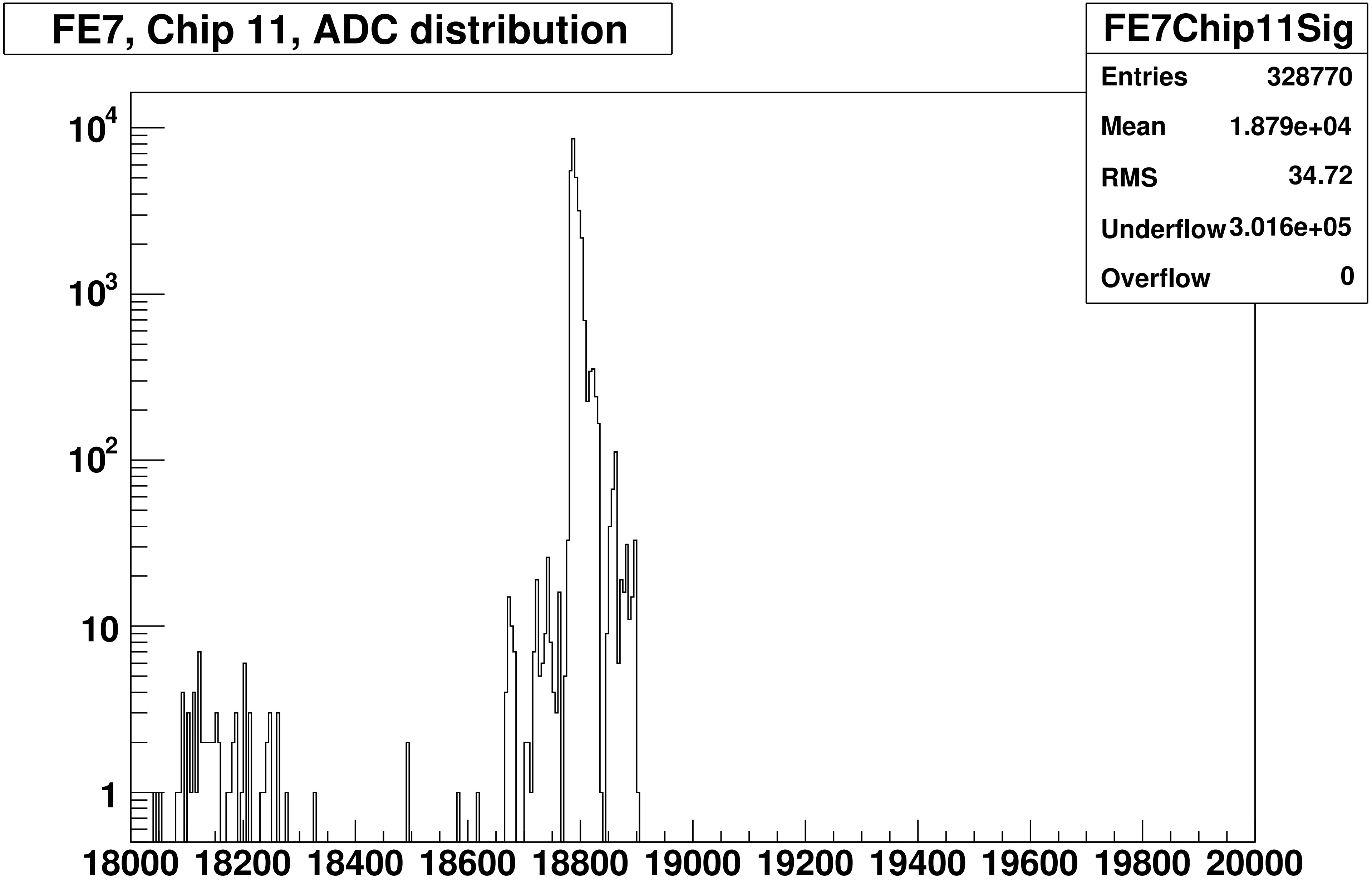

FE7, Chip 10, ADC distribution
FE7Chip10Ped
Entries 328770
Mean -5.479
RMS 1.306
Underflow 0
Overflow 2.722e+04
10^5
10^4
-200
-150
-100
-50
0
50
100
150
200



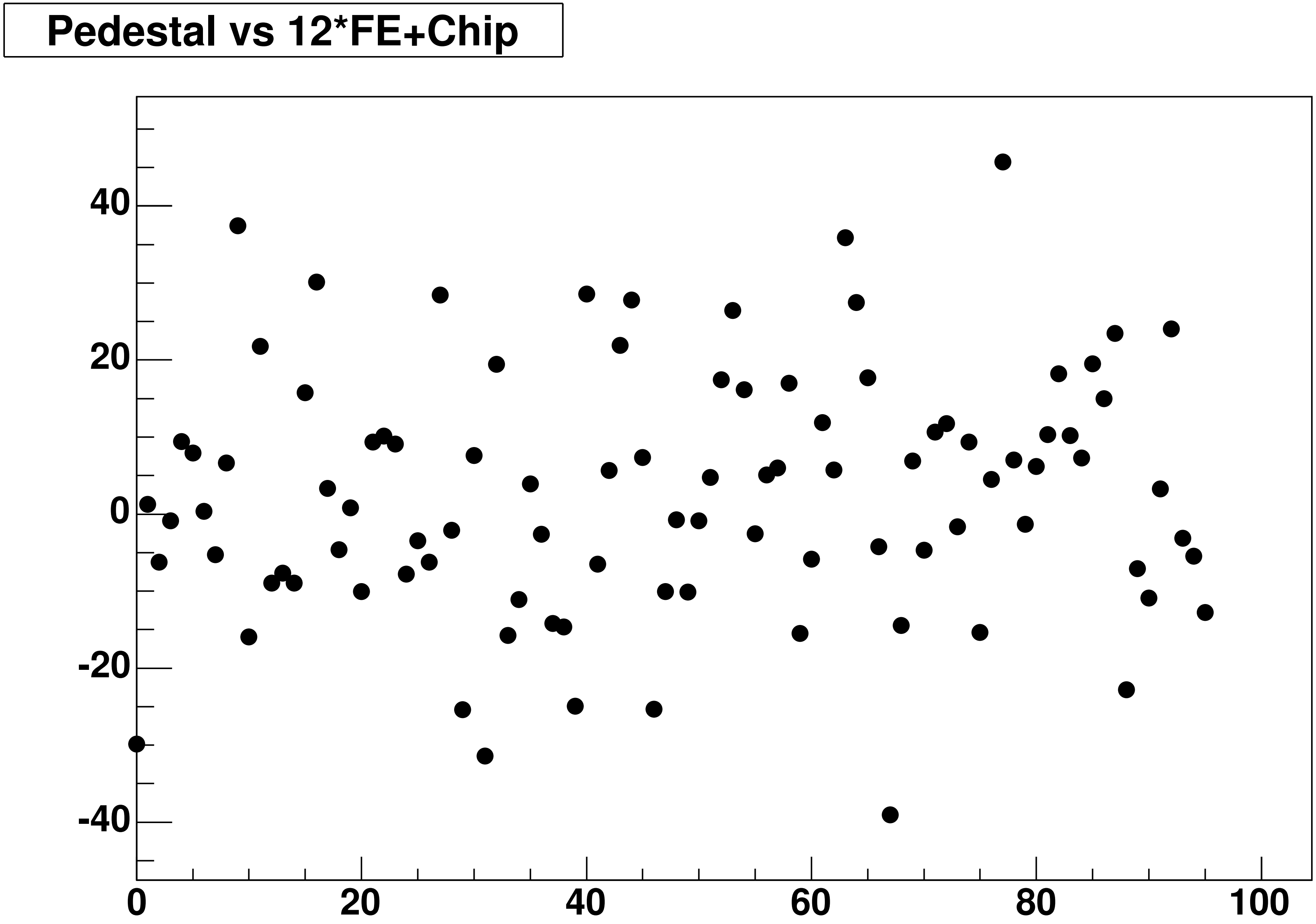
FE7, Chip 10, ADC distribution
FE7Chip10Sig
Entries 328770
Mean 1.876e+04
RMS 18.49
Underflow 3.016e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000

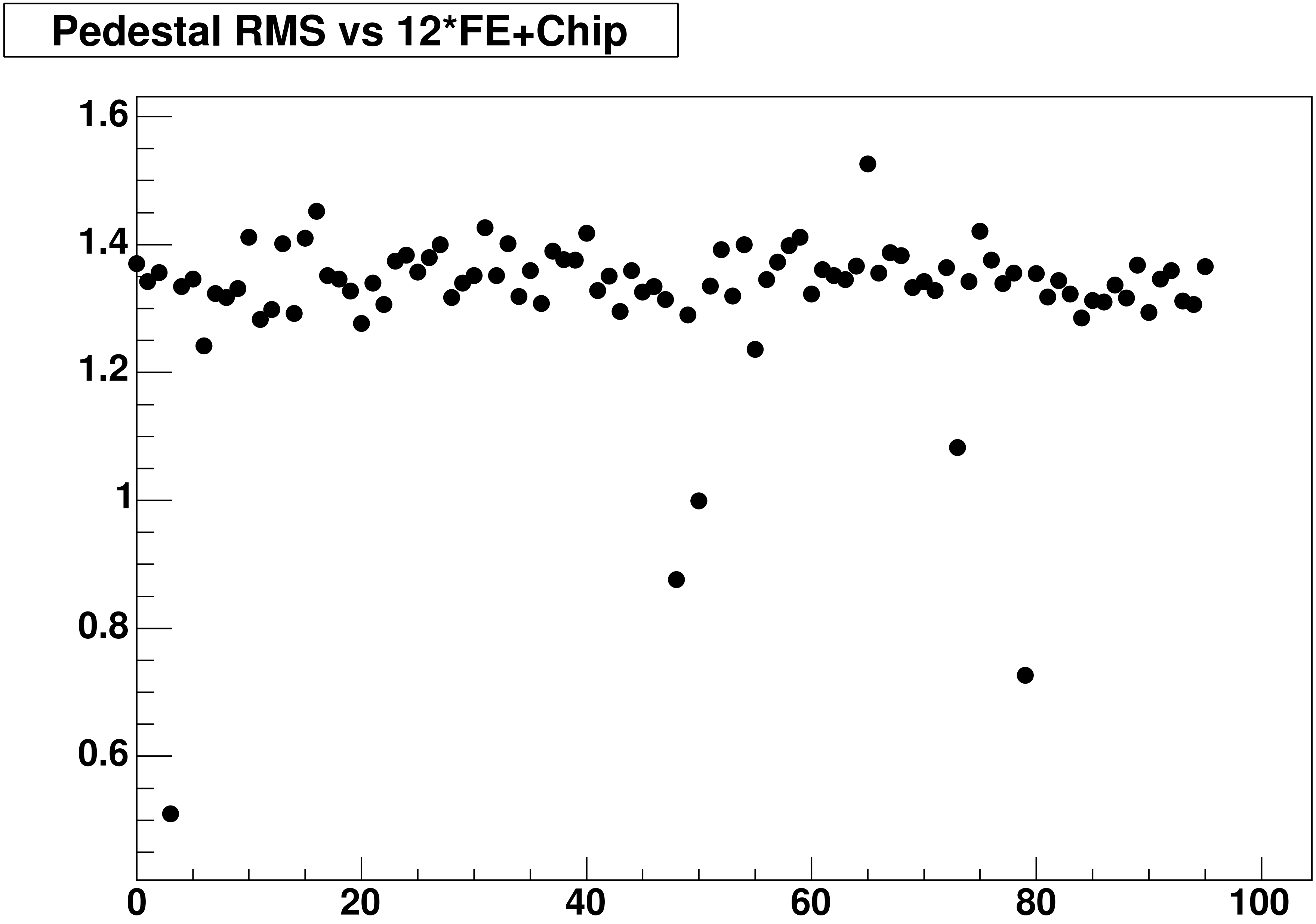

FE7, Chip 11, ADC distribution
FE7Chip11All
Entries 328770
Mean 1544
RMS 5181
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000

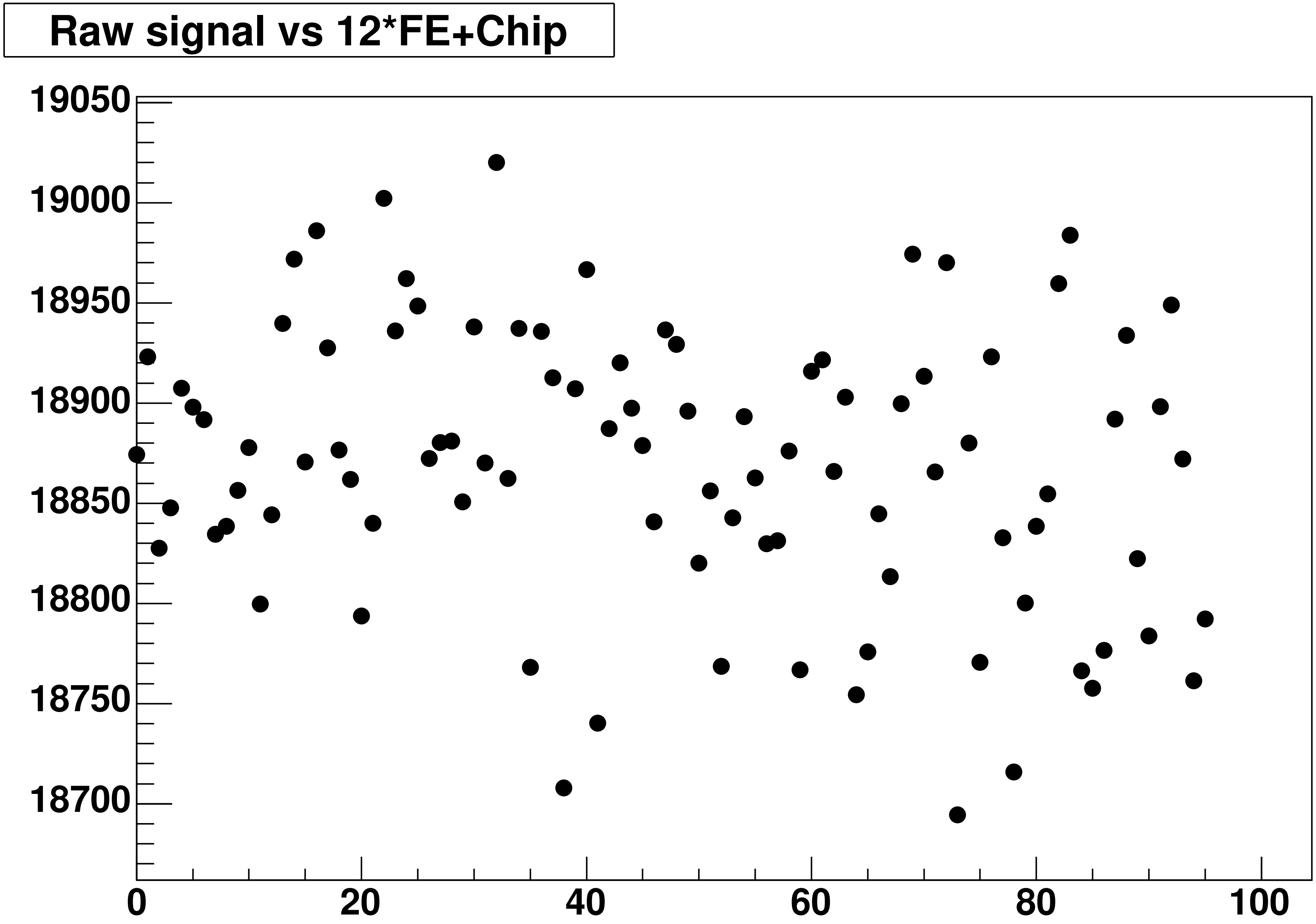

FE7, Chip 11, ADC distribution
FE7Chip11Ped
Entries 328770
Mean -12.77
RMS 1.365
Underflow 0
Overflow 2.723e+04
10^5
10^4
10^3
10^2
-200 -150 -100 -50 0 50 100 150 200

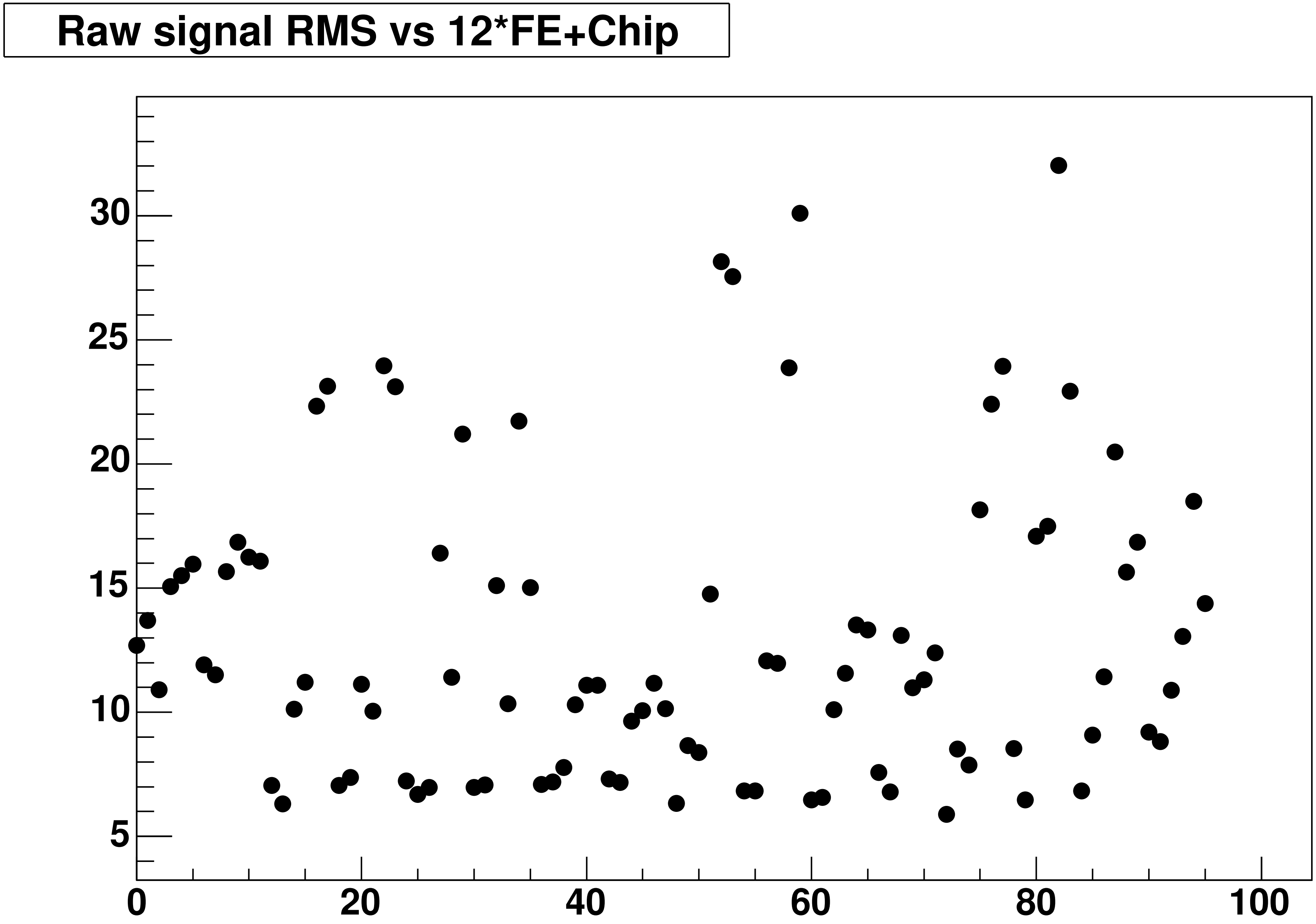


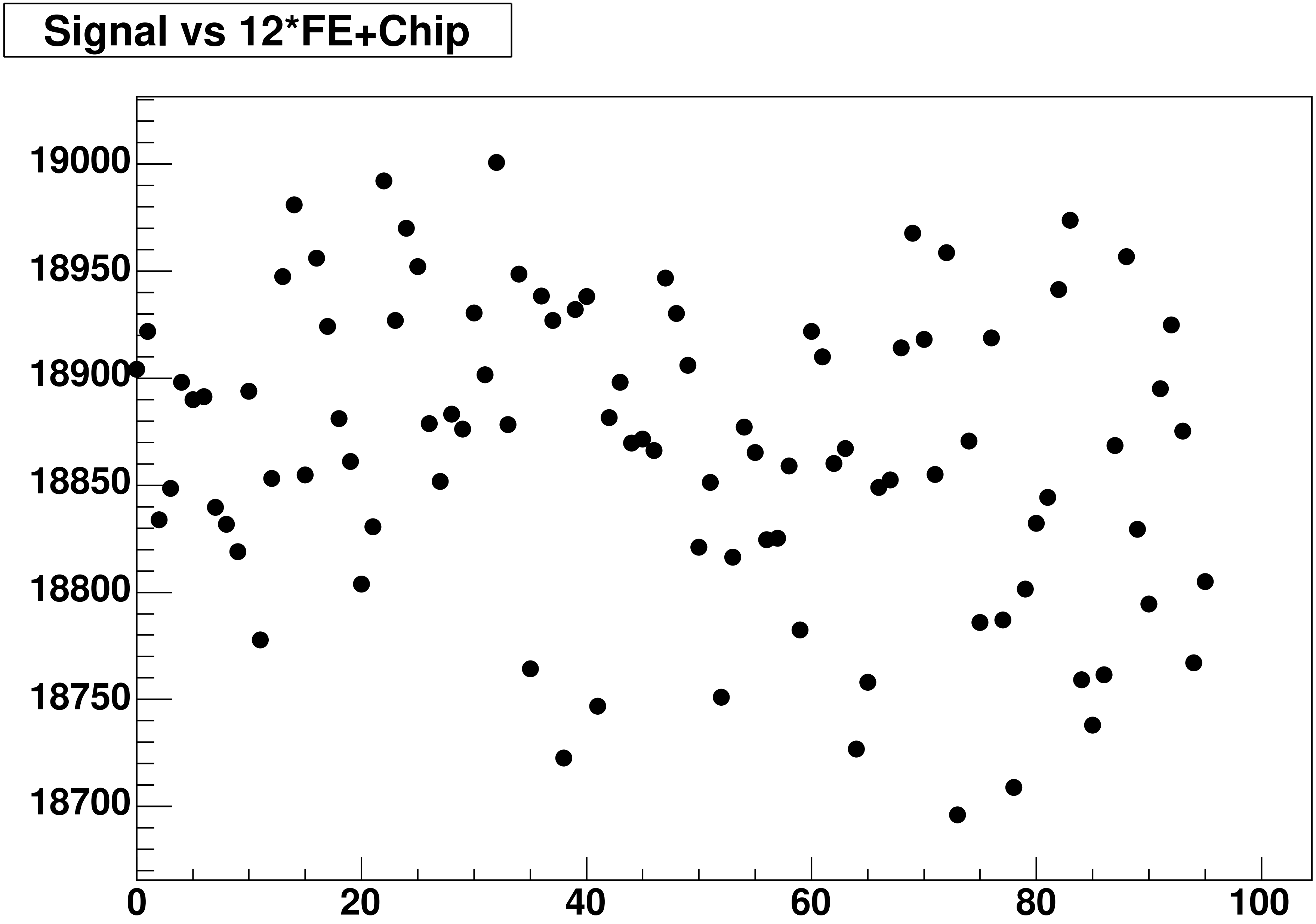
FE7, Chip 11, ADC distribution
FE7Chip11Sig
Entries 328770
Mean 1.879e+04
RMS 34.72
Underflow 3.016e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000


Pedestal vs 12*FE+Chip
40
20
0
-20
-40
0
20
40
60
80
100

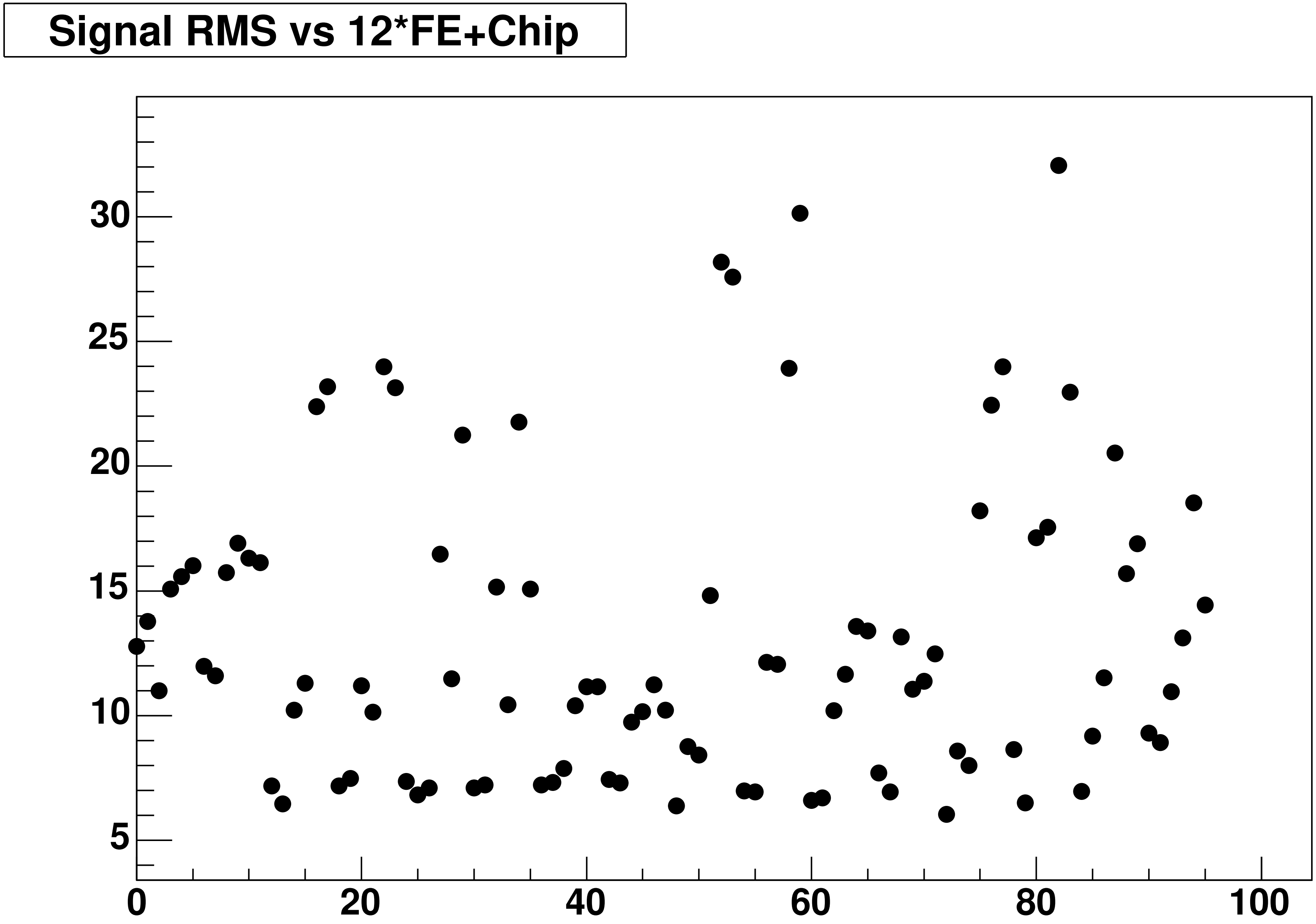

Pedestal RMS vs 12*FE+Chip
1.6
1.4
1.2
1
0.8
0.6
0
20
40
60
80
100


Raw signal vs 12*FE+Chip
19050
19000
18950
18900
18850
18800
18750
18700
0
20
40
60
80
100


Raw signal RMS vs 12*FE+Chip
5
10
15
20
25
30
0
20
40
60
80
100



Signal vs 12*FE+Chip
19000
18950
18900
18850
18800
18750
18700
0
20
40
60
80
100


Signal RMS vs 12*FE+Chip
5
10
15
20
25
30
0
20
40
60
80
100