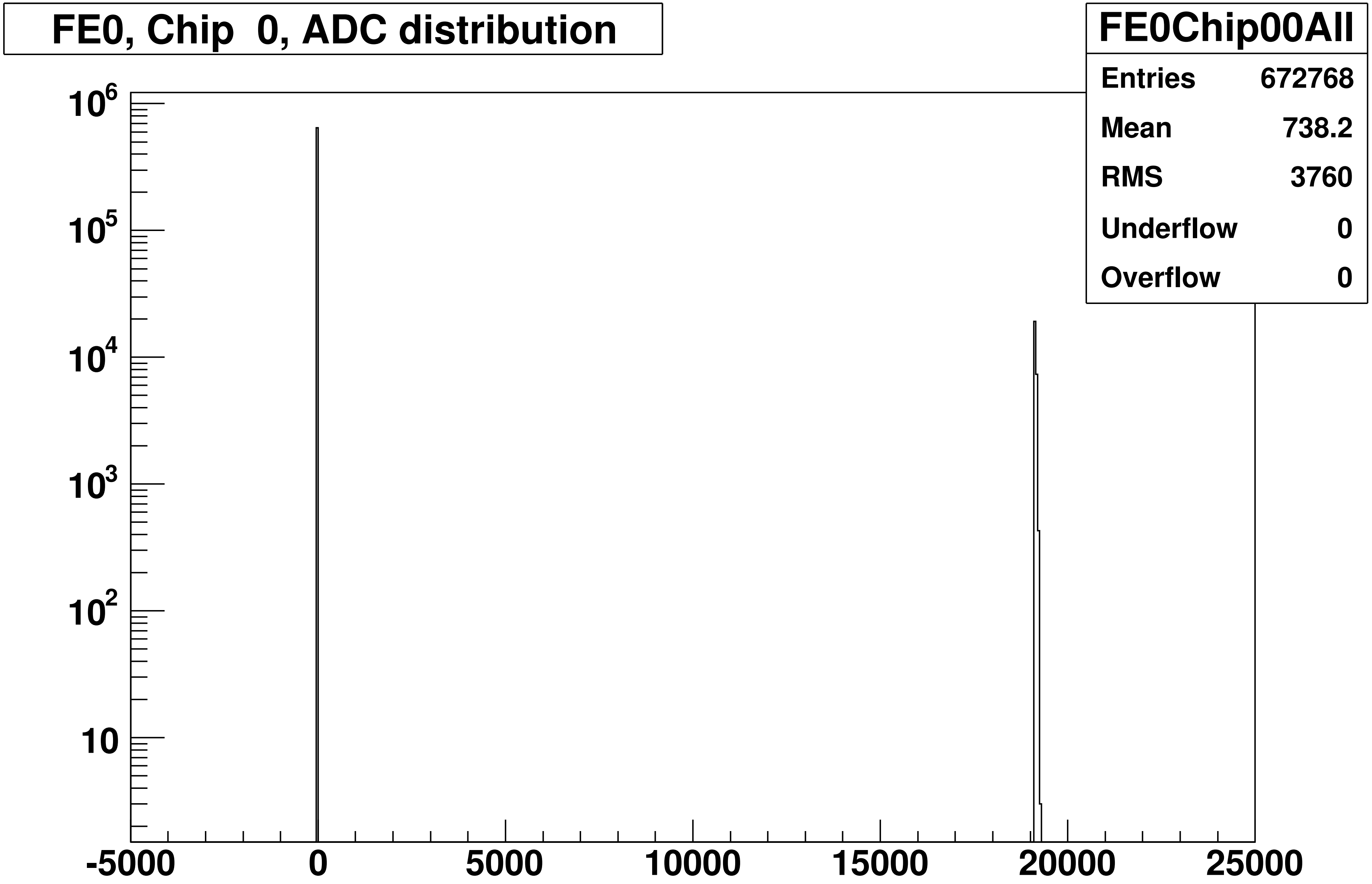

FE0, Chip 0, ADC distribution
FE0Chip00All
Entries 672768
Mean 738.2
RMS 3760
Underflow 0
Overflow 0
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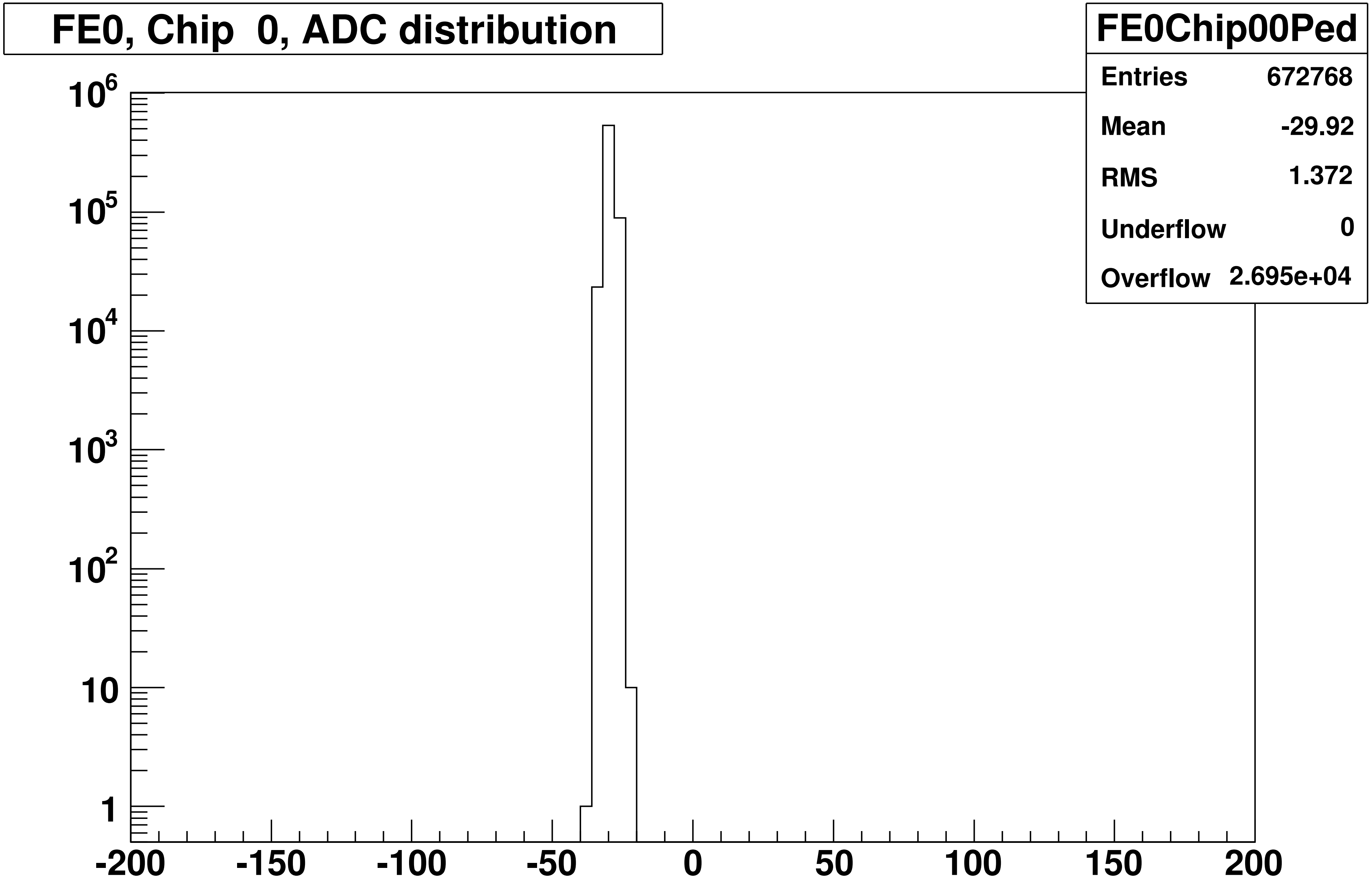
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE0, Chip 0, ADC distribution
FE0Chip00Ped
Entries 672768
Mean -29.92
RMS 1.372
Underflow 0
Overflow 2.695e+04
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10^5
10^4
10^3
10^2
10
1
-200
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-100
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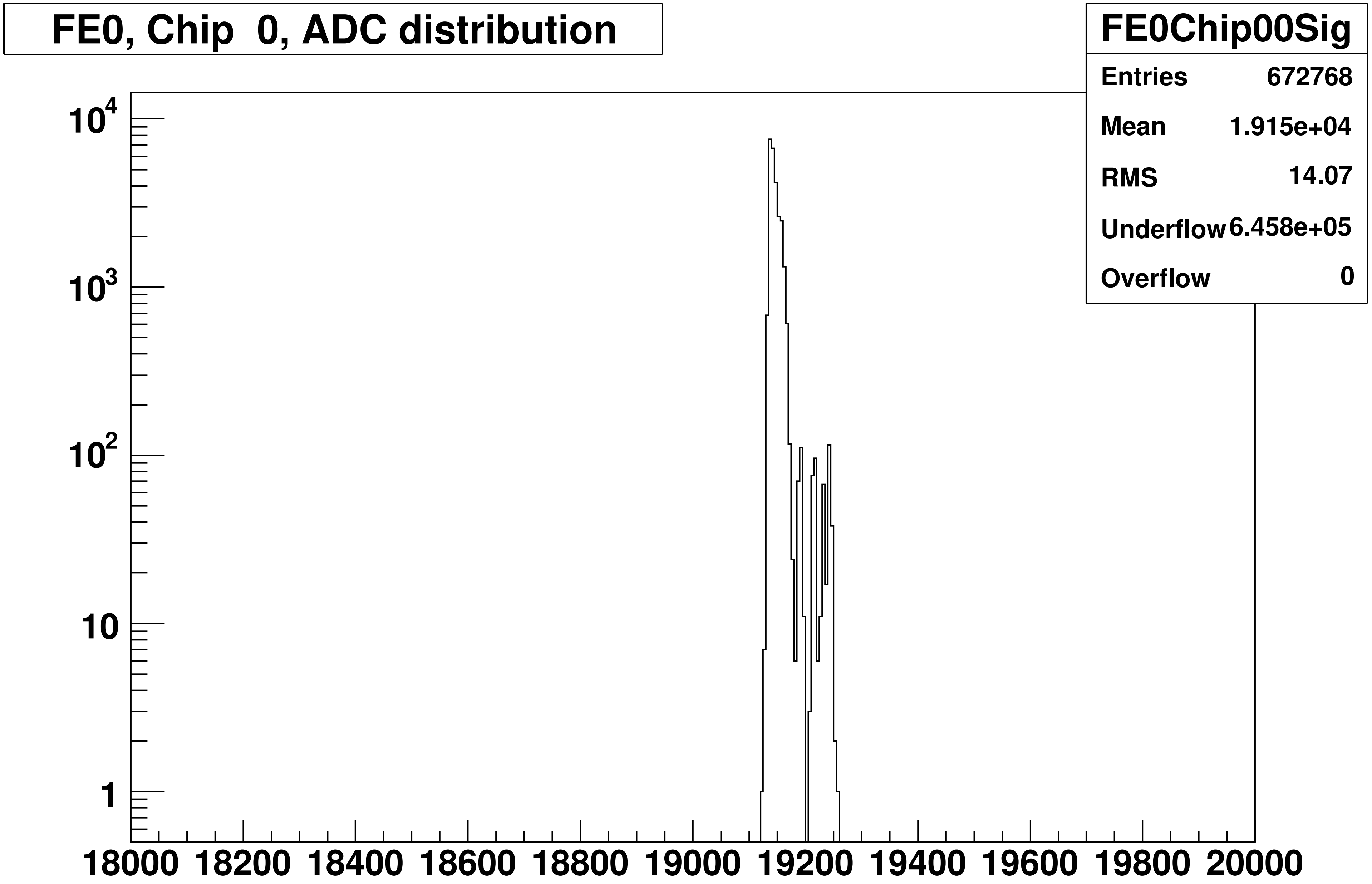
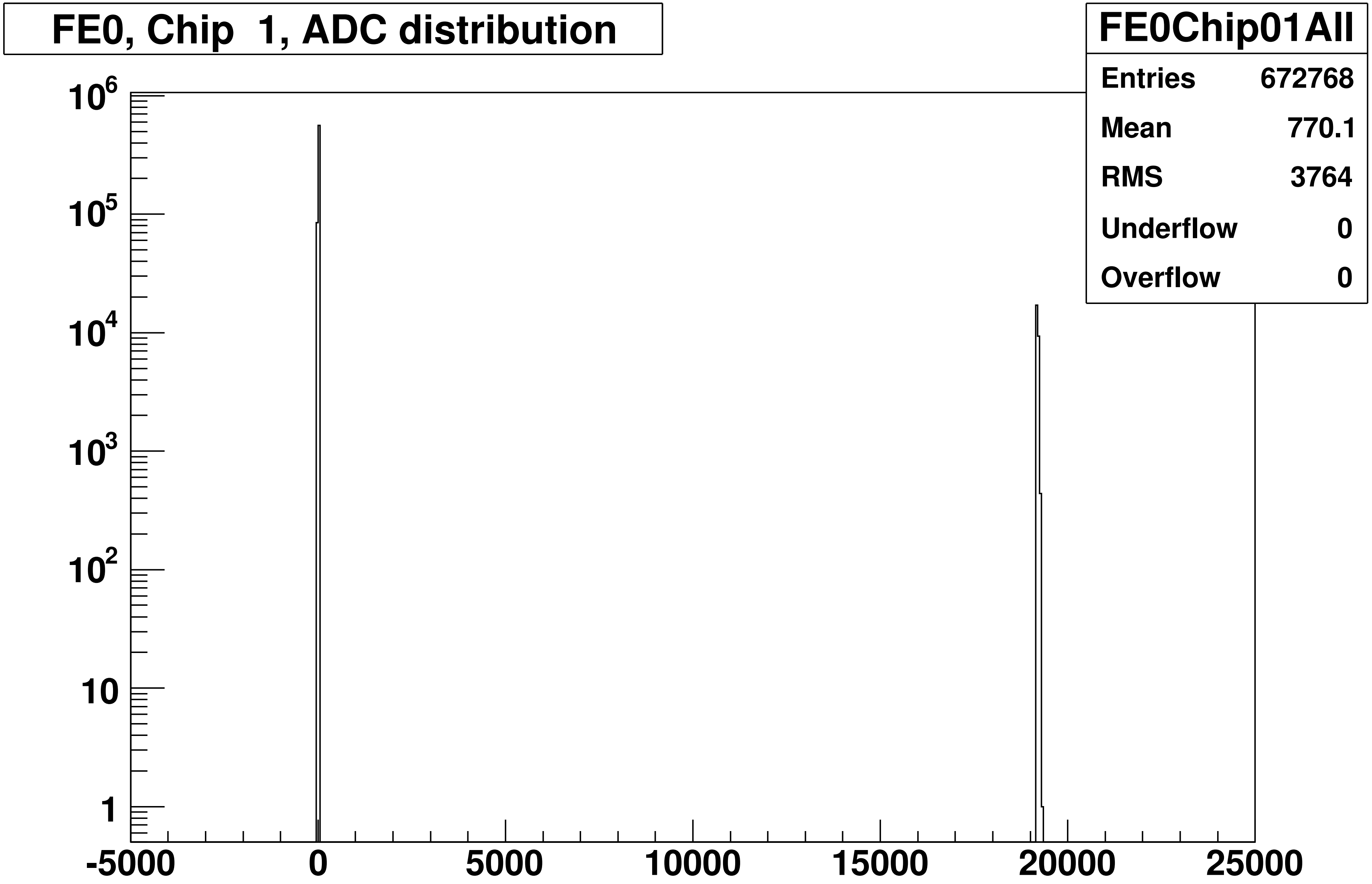
100
150
200


FE0, Chip 0, ADC distribution
FE0Chip00Sig
Entries 672768
Mean 1.915e+04
RMS 14.07
Underflow 6.458e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE0, Chip 1, ADC distribution
FE0Chip01All
Entries 672768
Mean 770.1
RMS 3764
Underflow 0
Overflow 0
1
10
10^2
10^3
10^4
10^5
10^6
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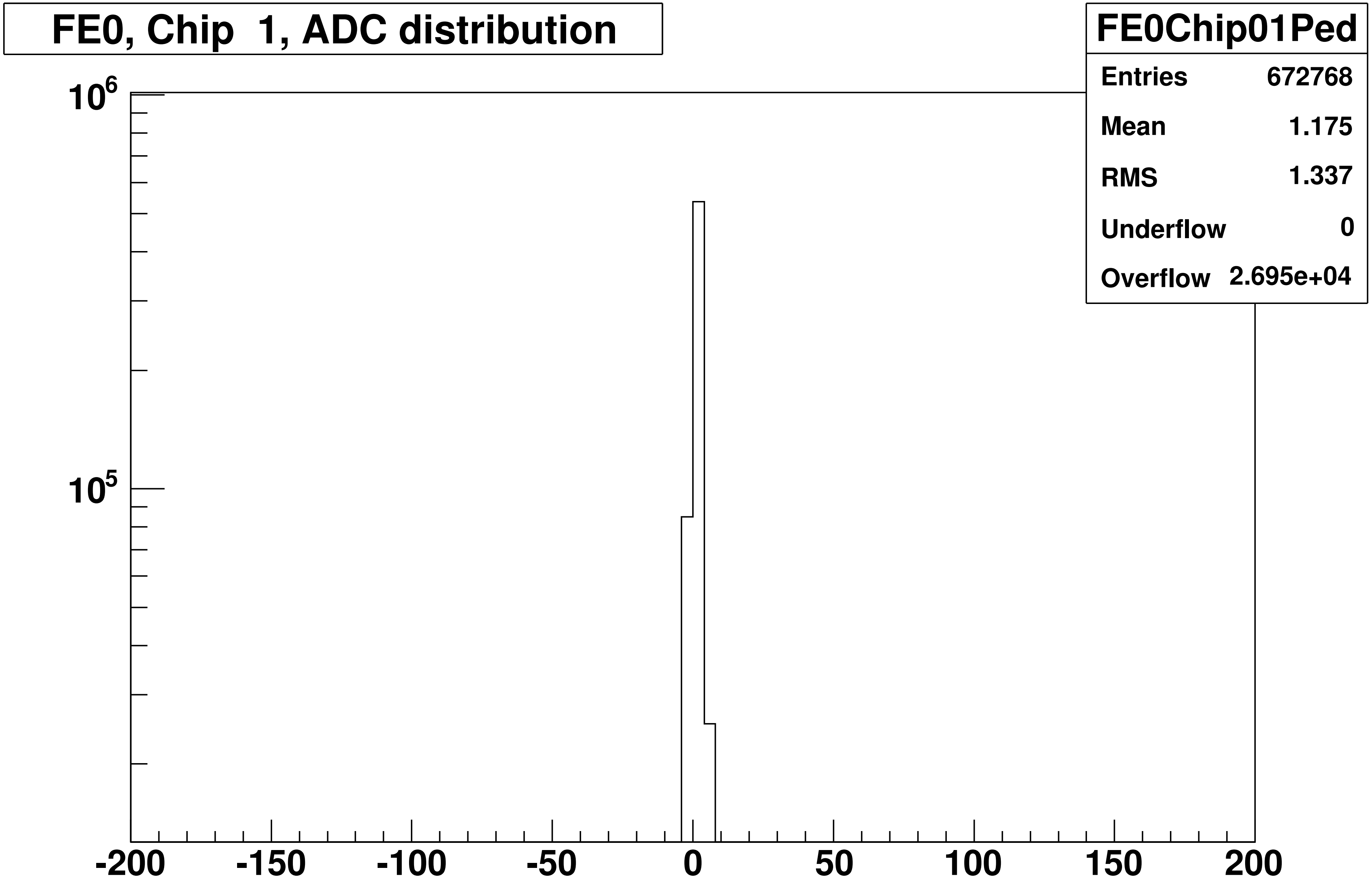
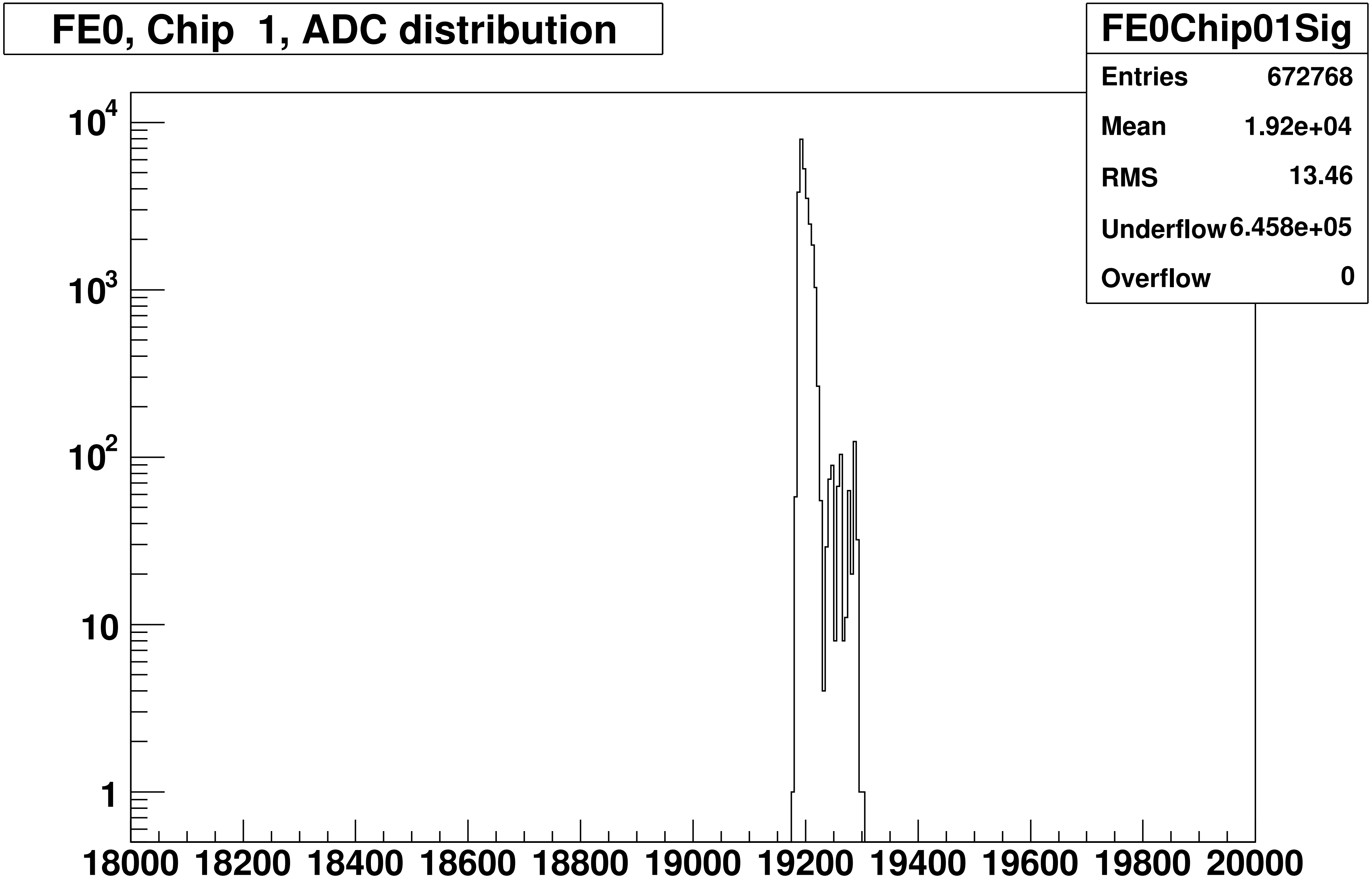
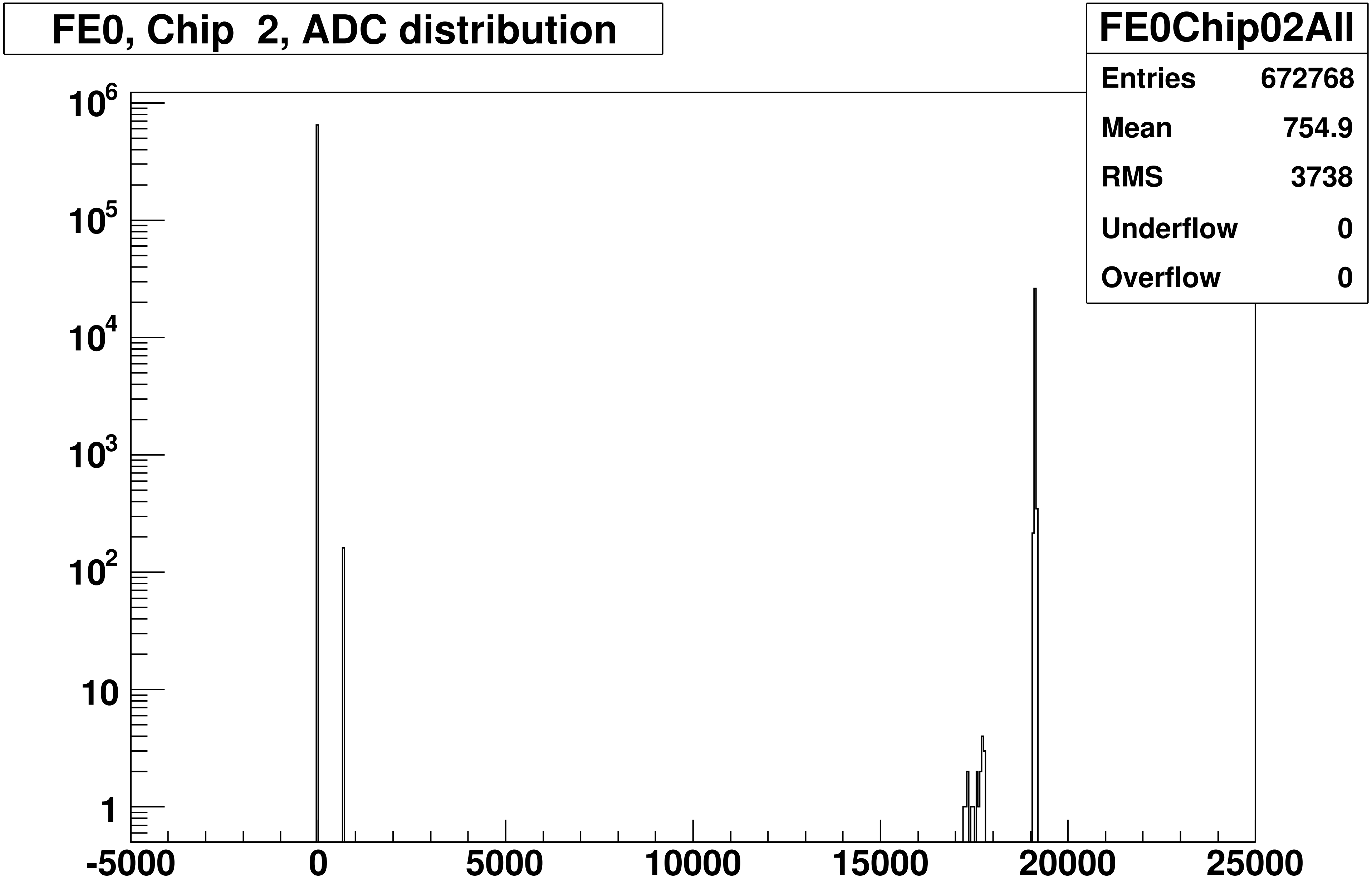

FE0, Chip 1, ADC distribution
FE0Chip01Ped
Entries 672768
Mean 1.175
RMS 1.337
Underflow 0
Overflow 2.695e+04
10^6
10^5
-200
-150
-100
-50
0
50
100
150
200


FE0, Chip 1, ADC distribution
FE0Chip01Sig
Entries 672768
Mean 1.92e+04
RMS 13.46
Underflow 6.458e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE0, Chip 2, ADC distribution
FE0Chip02All
Entries 672768
Mean 754.9
RMS 3738
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
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10000
15000
20000
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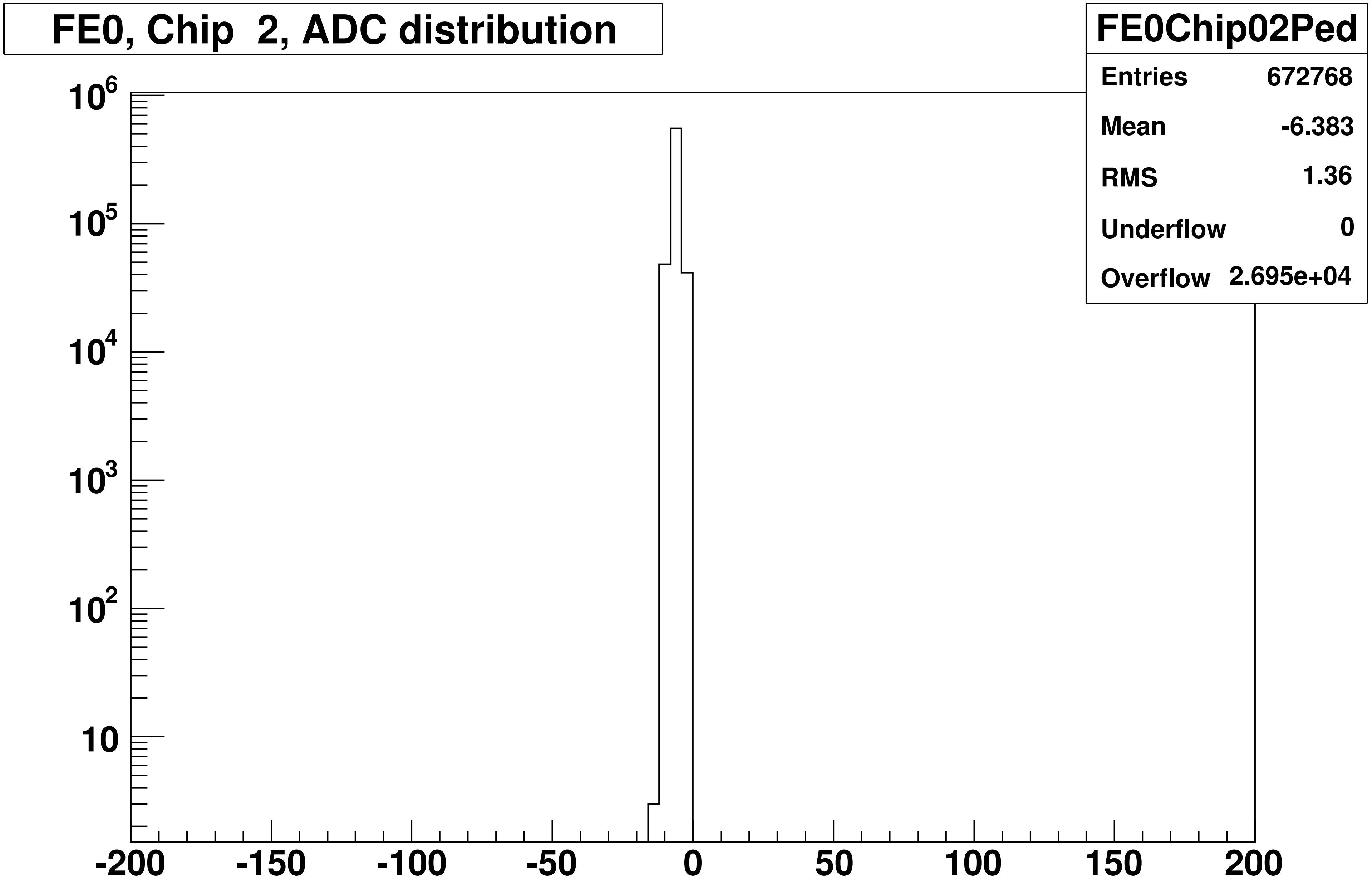
FE0, Chip 2, ADC distribution
FE0Chip02Ped
Entries 672768
Mean -6.383
RMS 1.36
Underflow 0
Overflow 2.695e+04
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10^5
10^4
10^3
10^2
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-100
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100
150
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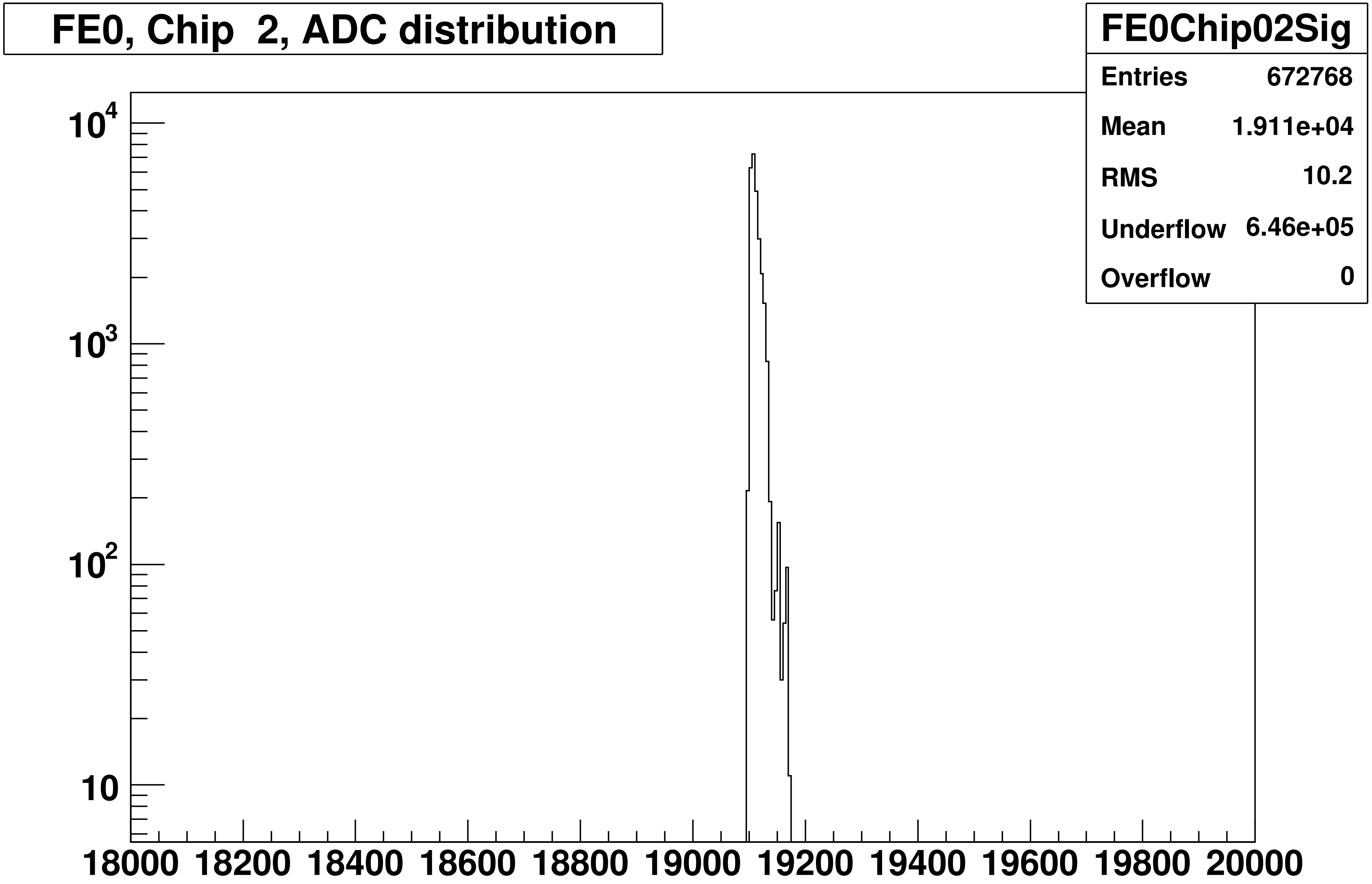

FE0, Chip 2, ADC distribution
FE0Chip02Sig
Entries 672768
Mean 1.911e+04
RMS 10.2
Underflow 6.46e+05
Overflow 0
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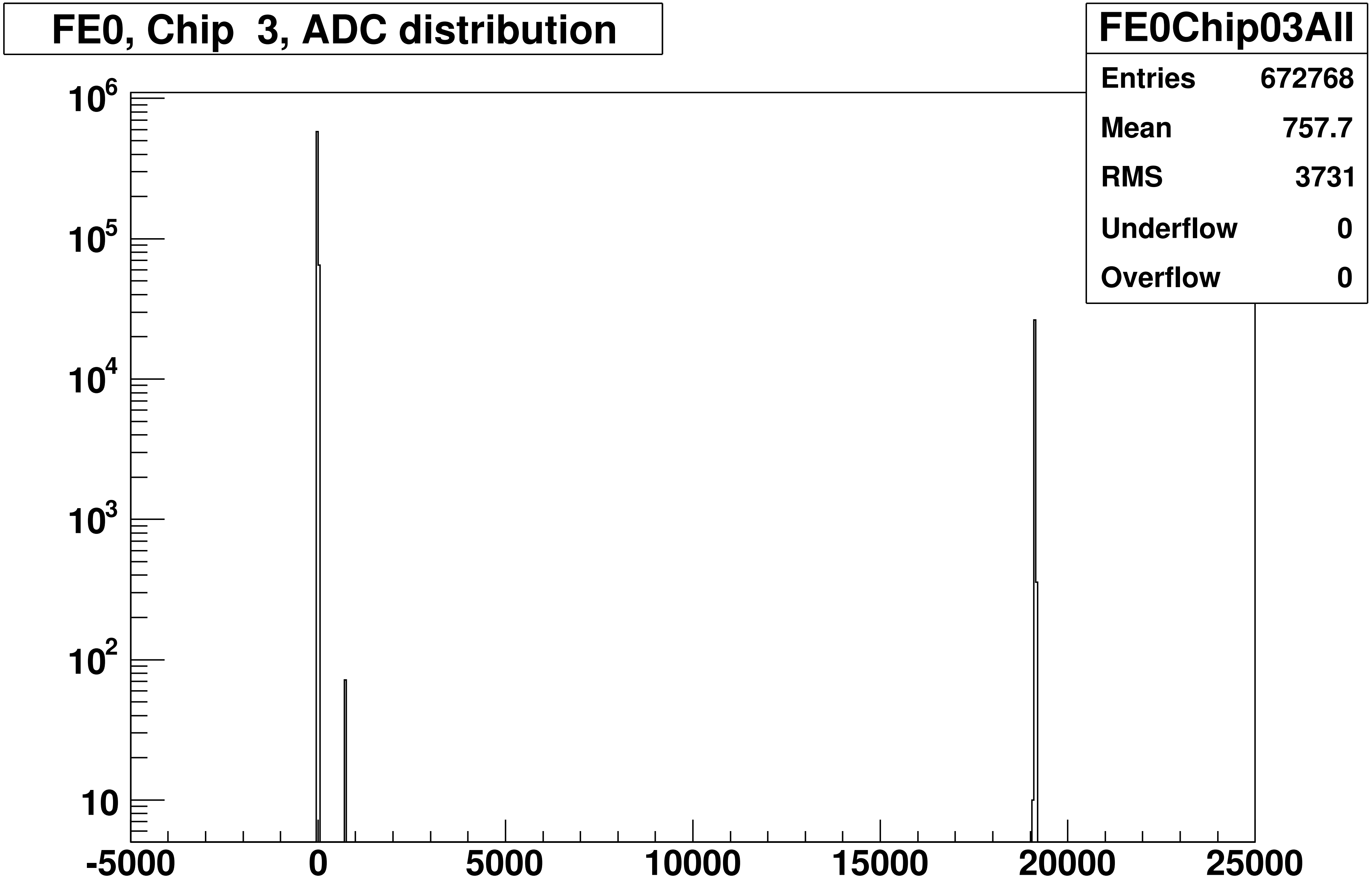
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE0, Chip 3, ADC distribution
FE0Chip03All
Entries 672768
Mean 757.7
RMS 3731
Underflow 0
Overflow 0
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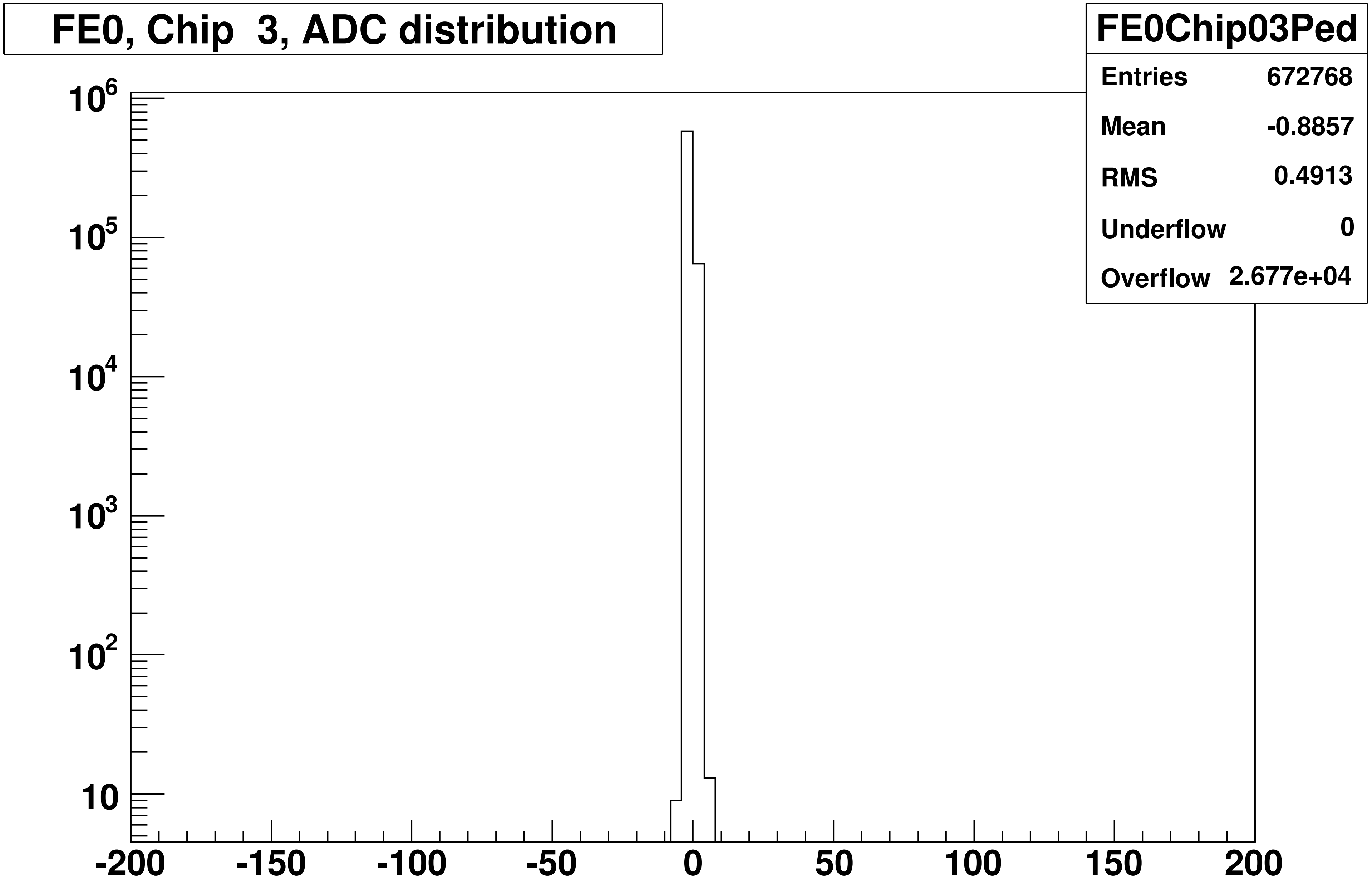
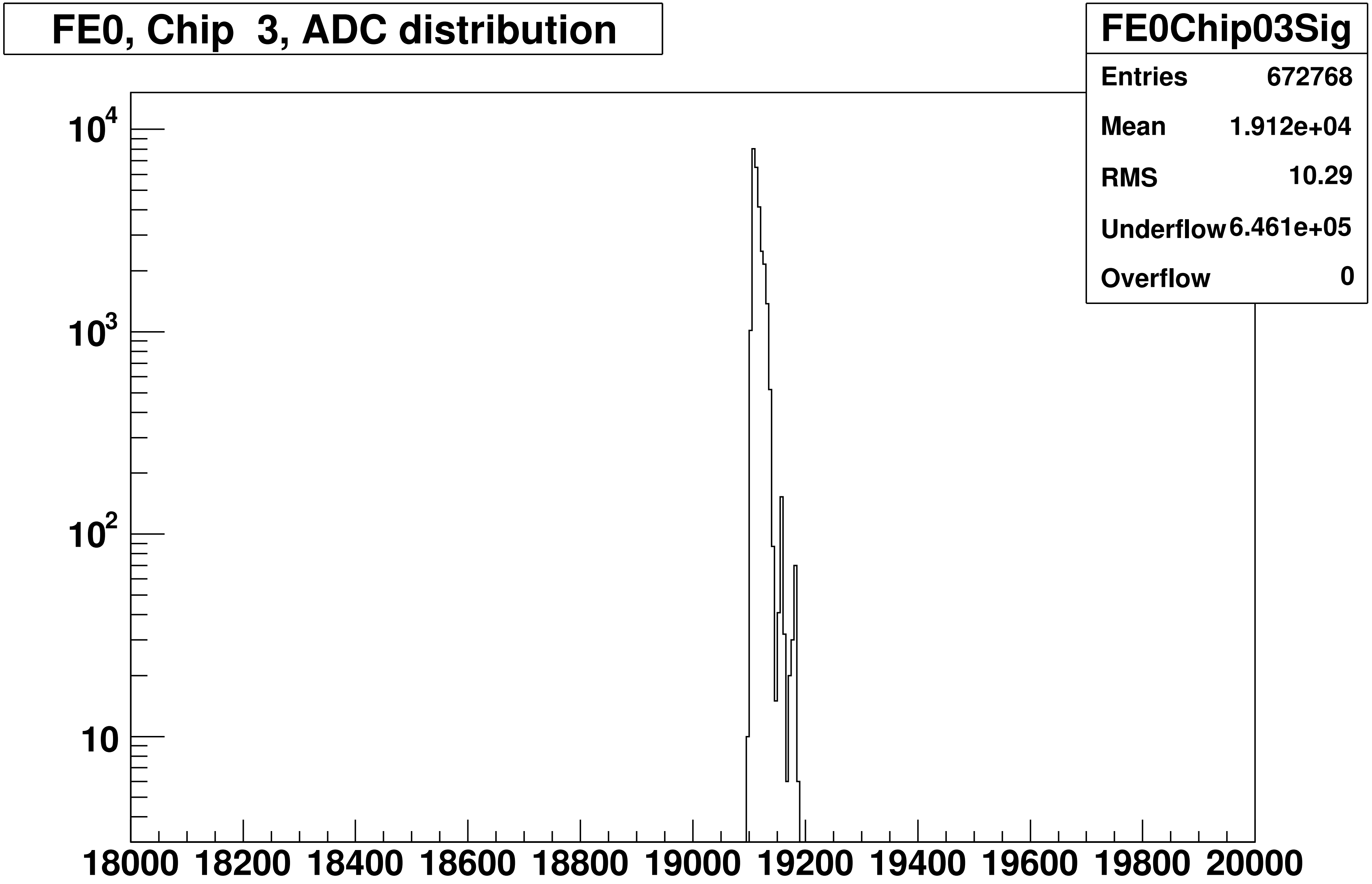
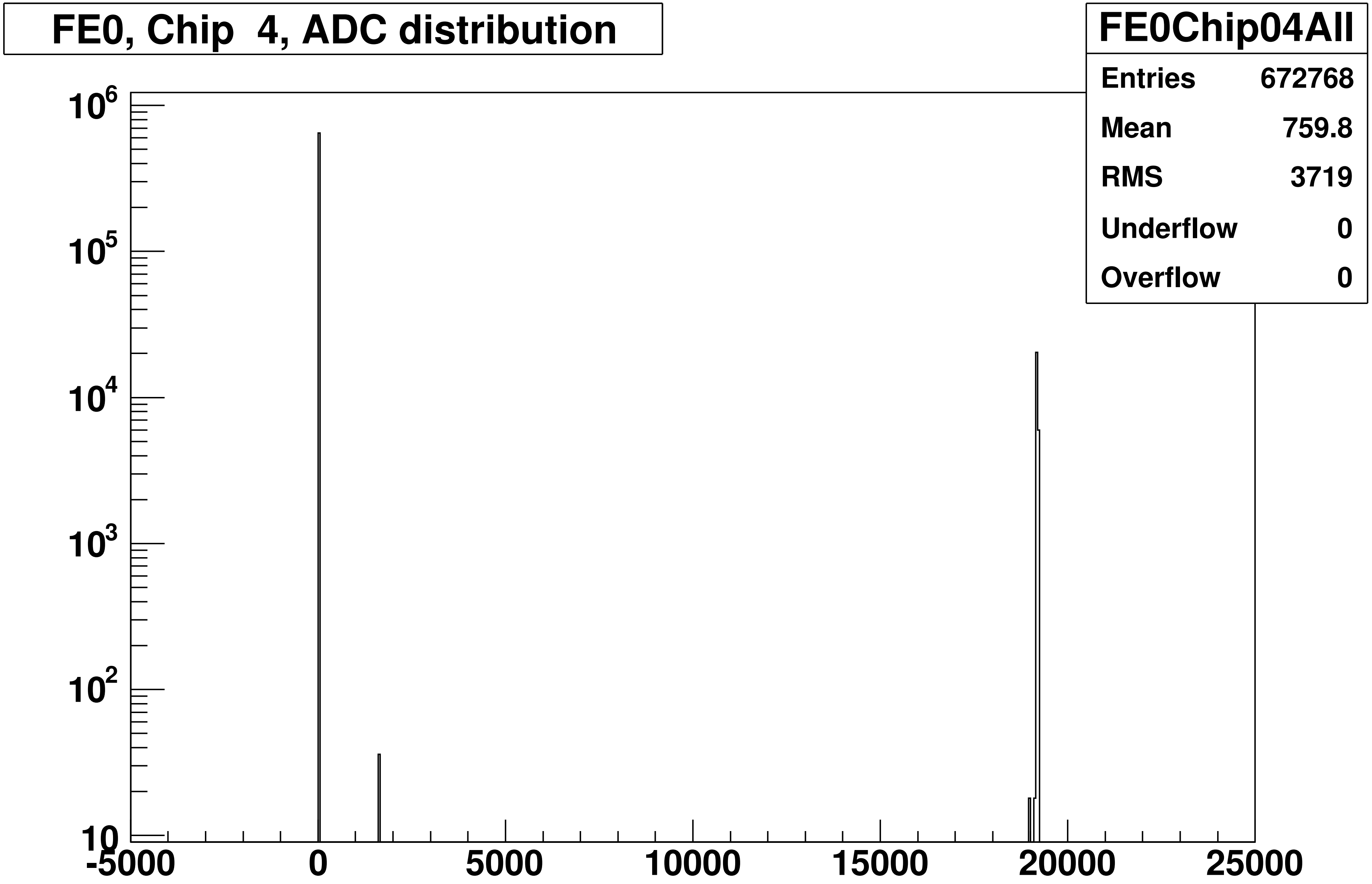
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000

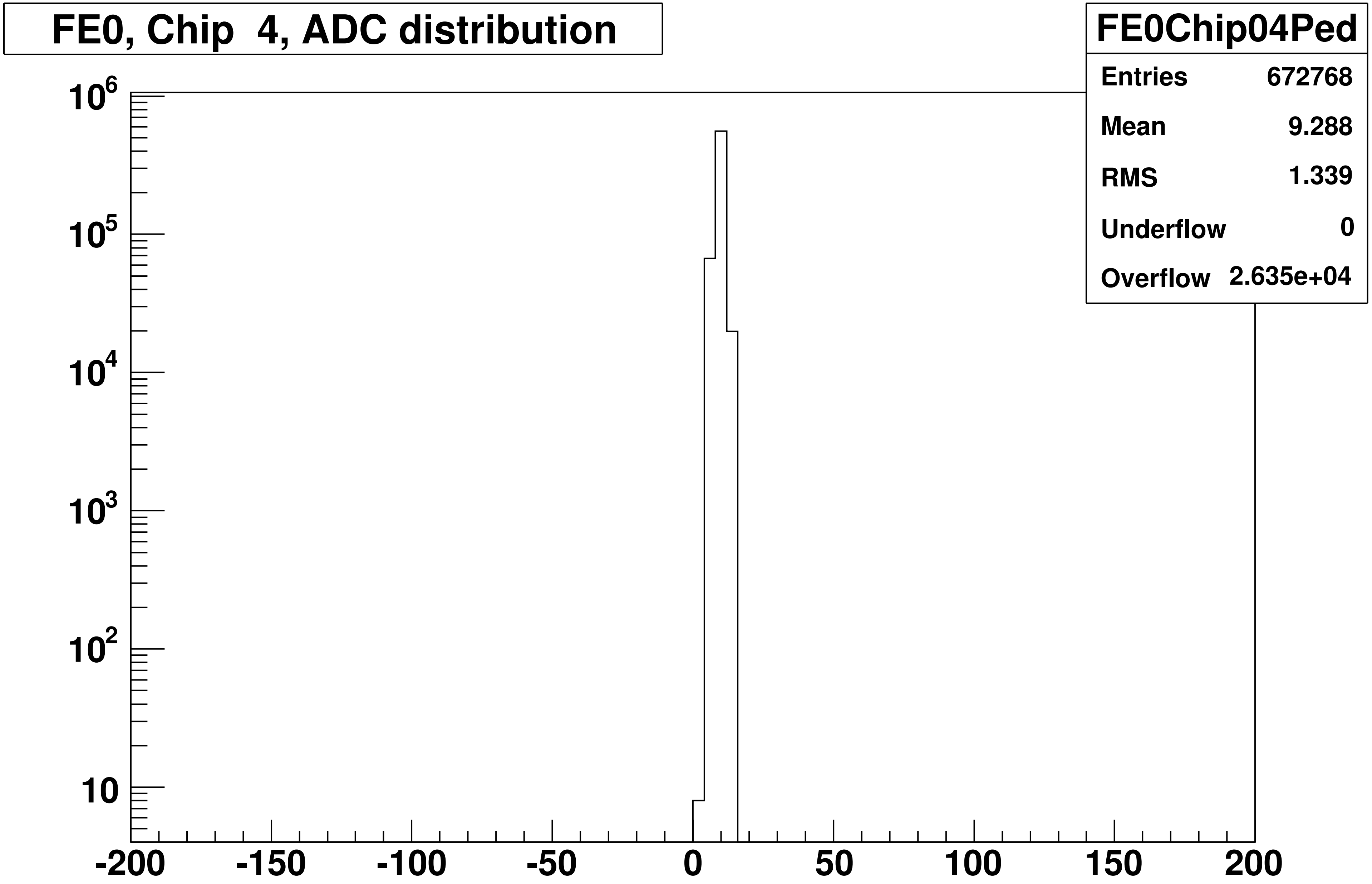

FE0, Chip 3, ADC distribution
FE0Chip03Ped
Entries 672768
Mean -0.8857
RMS 0.4913
Underflow 0
Overflow 2.677e+04
10^6
10^5
10^4
10^3
10^2
10
-200
-150
-100
-50
0
50
100
150
200



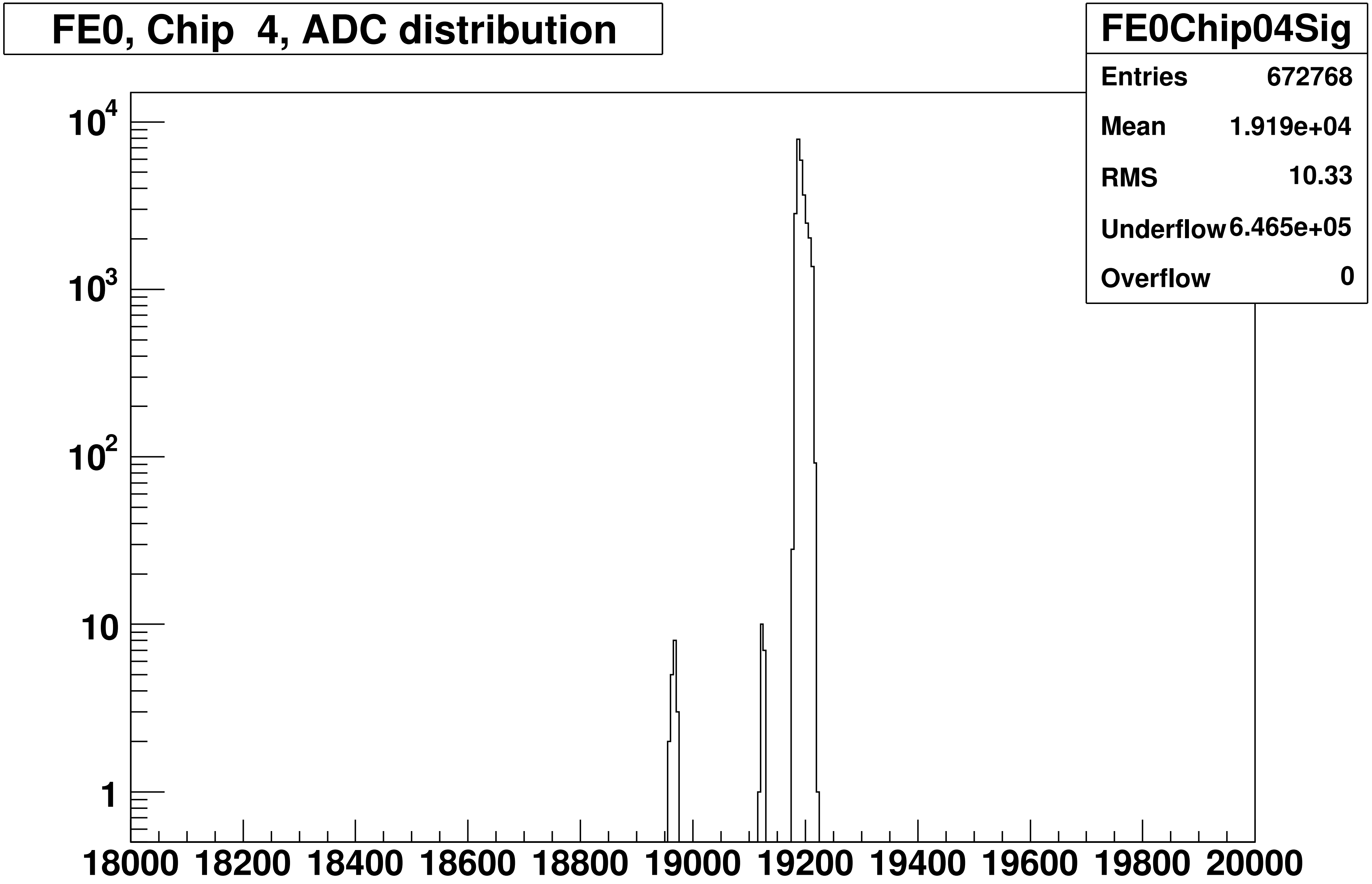
FE0, Chip 3, ADC distribution
FE0Chip03Sig
Entries 672768
Mean 1.912e+04
RMS 10.29
Underflow 6.461e+05
Overflow 0
10^4
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000

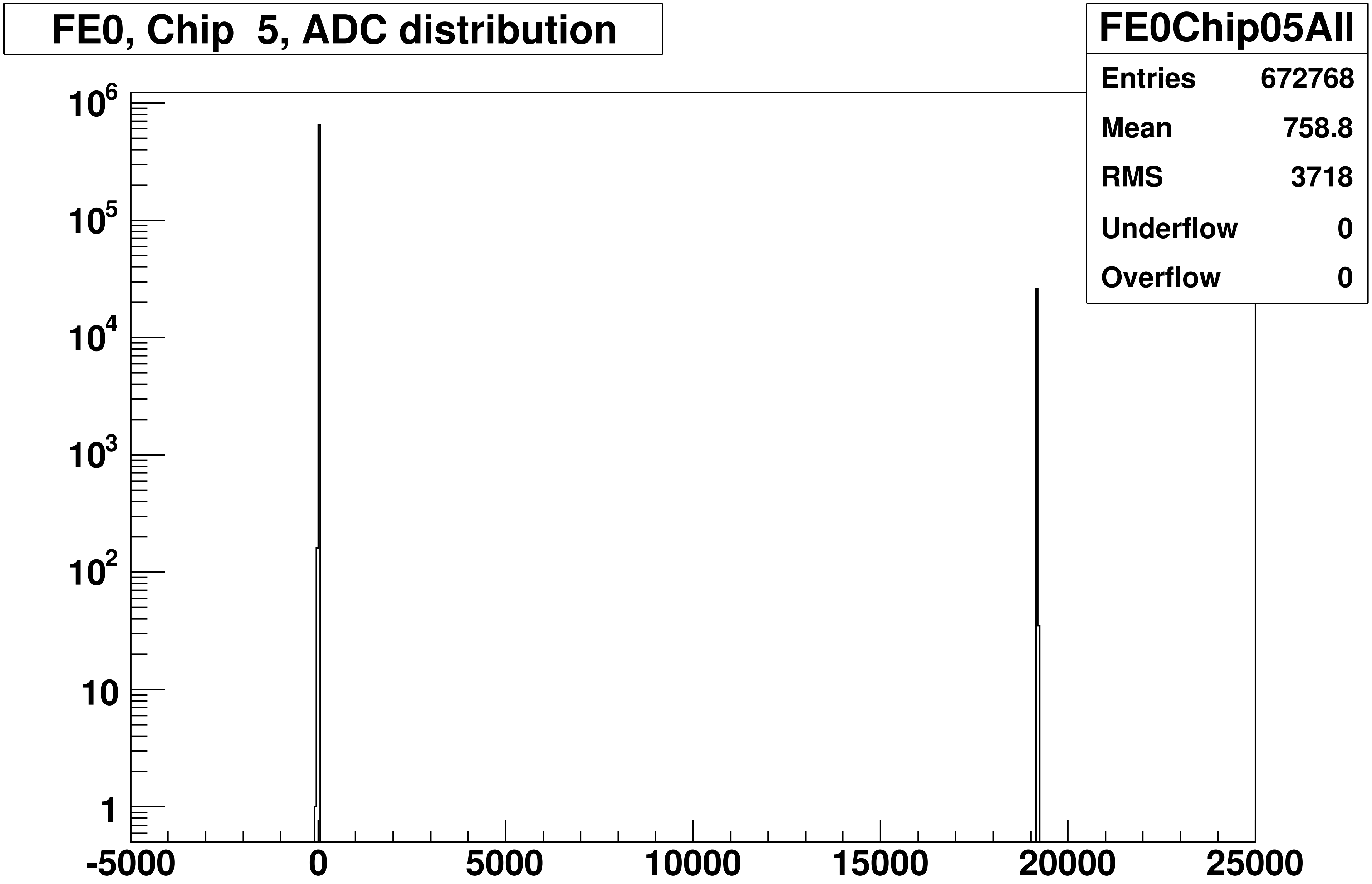


FE0, Chip 4, ADC distribution
FE0Chip04All
Entries 672768
Mean 759.8
RMS 3719
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000

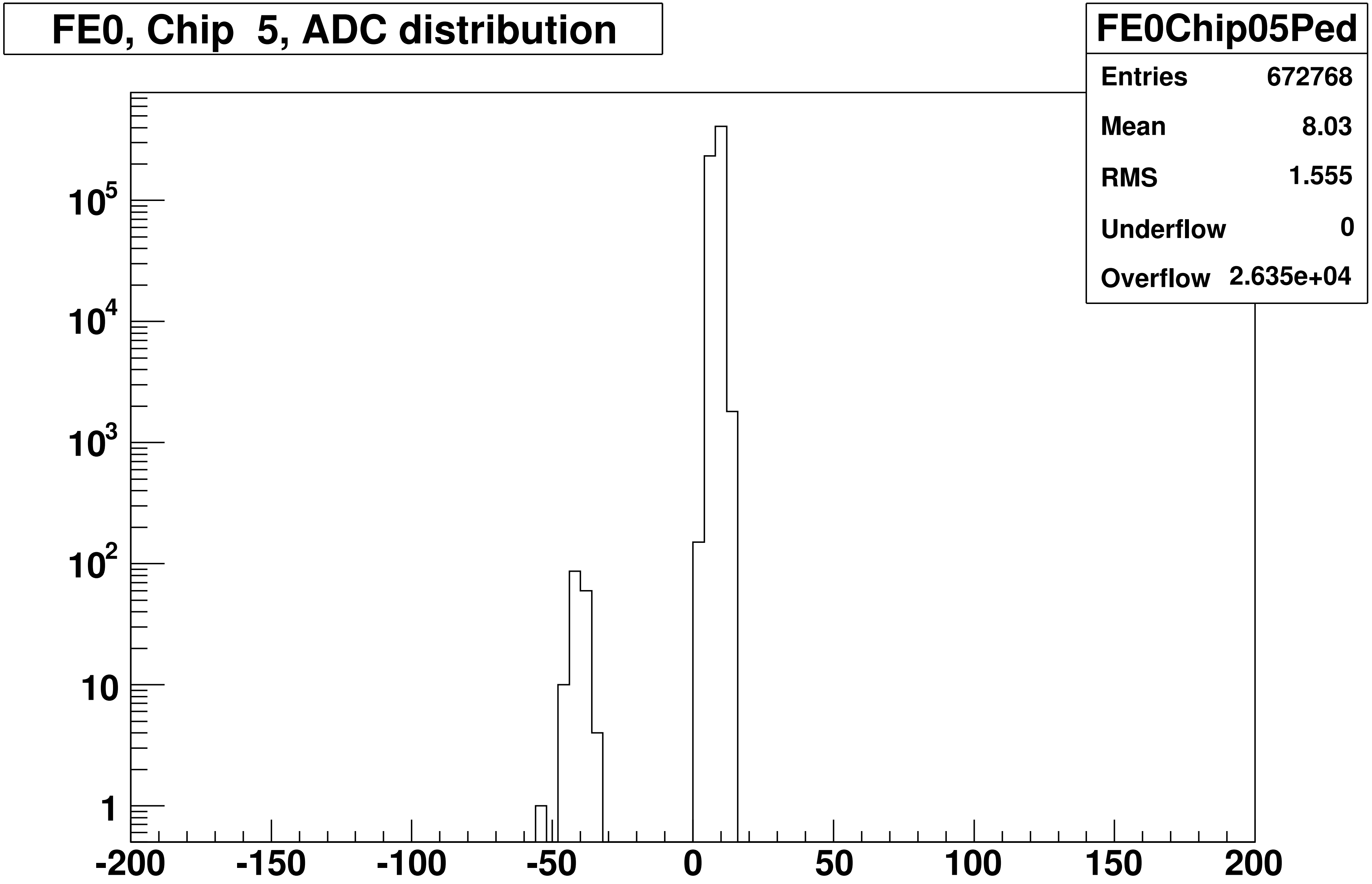


FE0, Chip 4, ADC distribution
FE0Chip04Ped
Entries 672768
Mean 9.288
RMS 1.339
Underflow 0
Overflow 2.635e+04
10^6
10^5
10^4
10^3
10^2
10
-200
-150
-100
-50
0
50
100
150
200

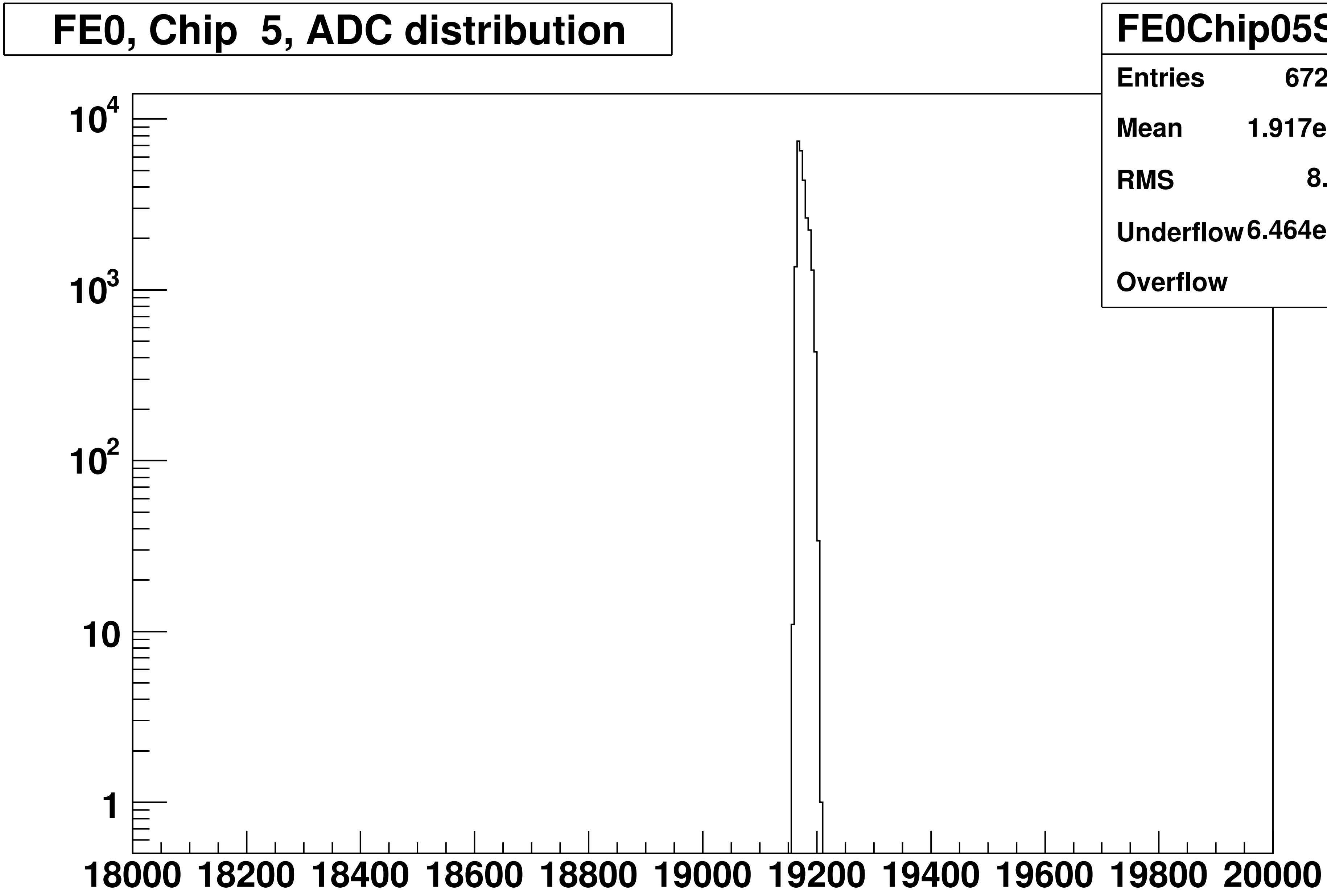

FE0, Chip 4, ADC distribution
FE0Chip04Sig
Entries 672768
Mean 1.919e+04
RMS 10.33
Underflow 6.465e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000

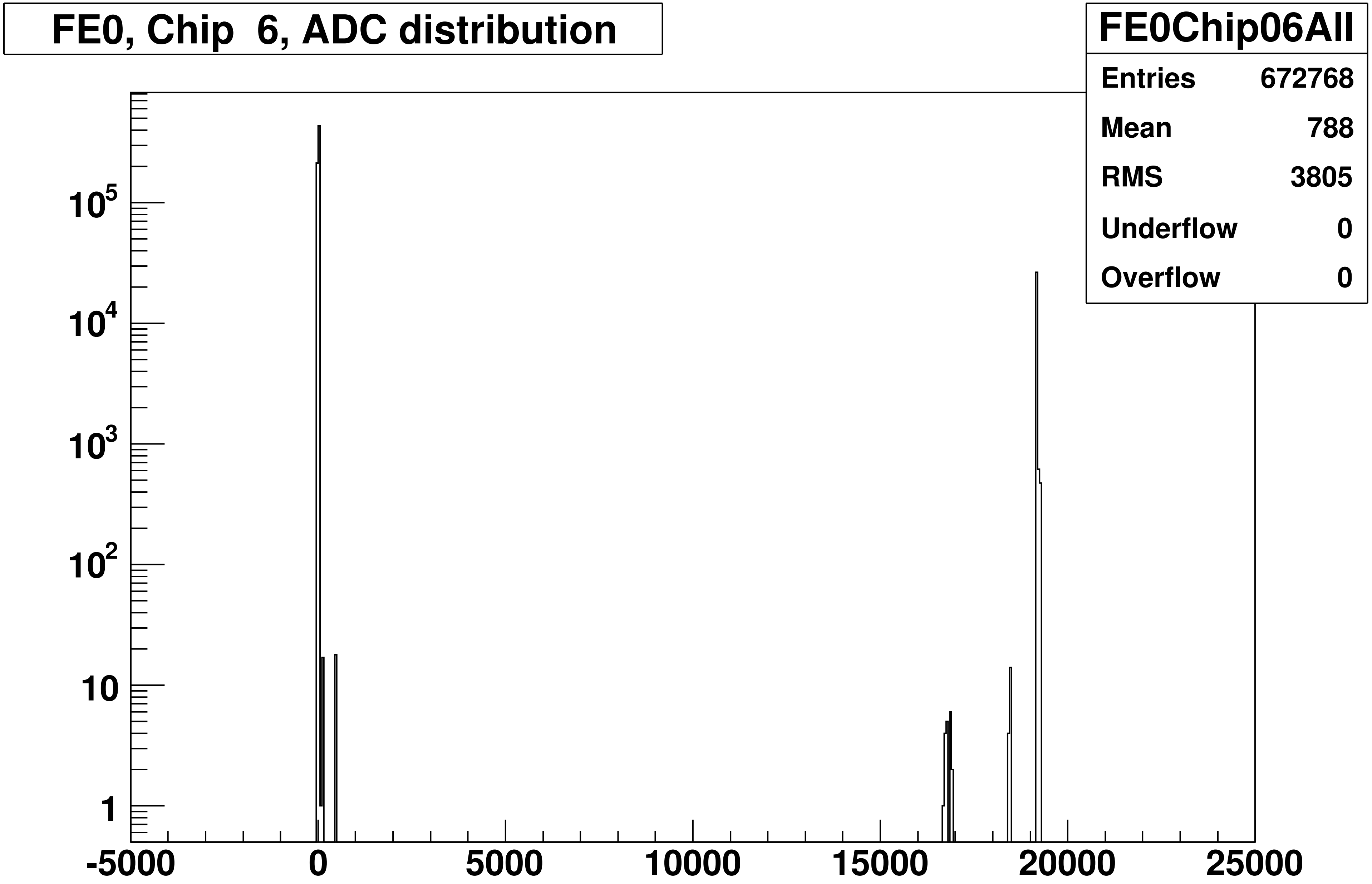


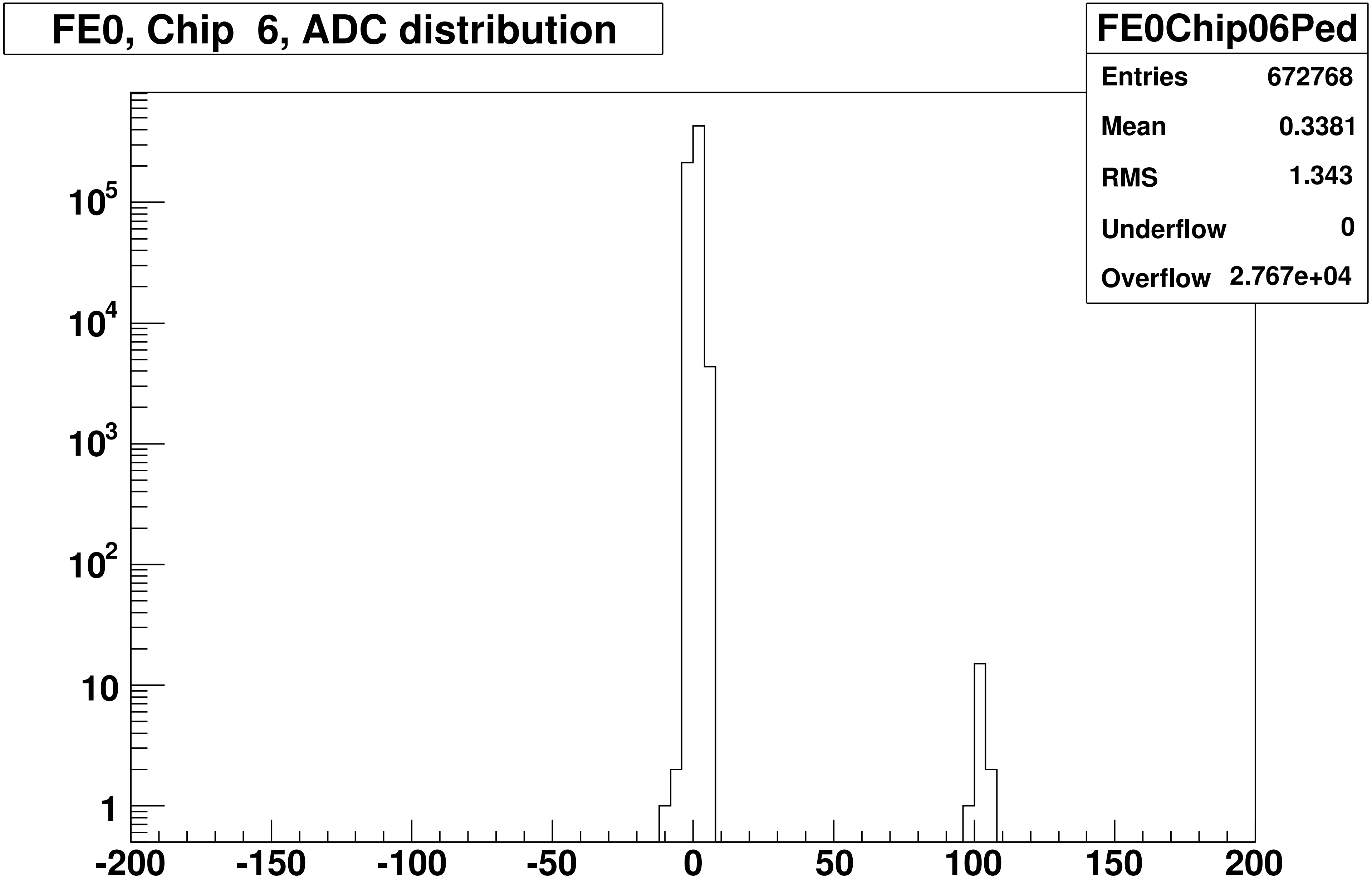
FE0, Chip 5, ADC distribution
FE0Chip05All
Entries 672768
Mean 758.8
RMS 3718
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



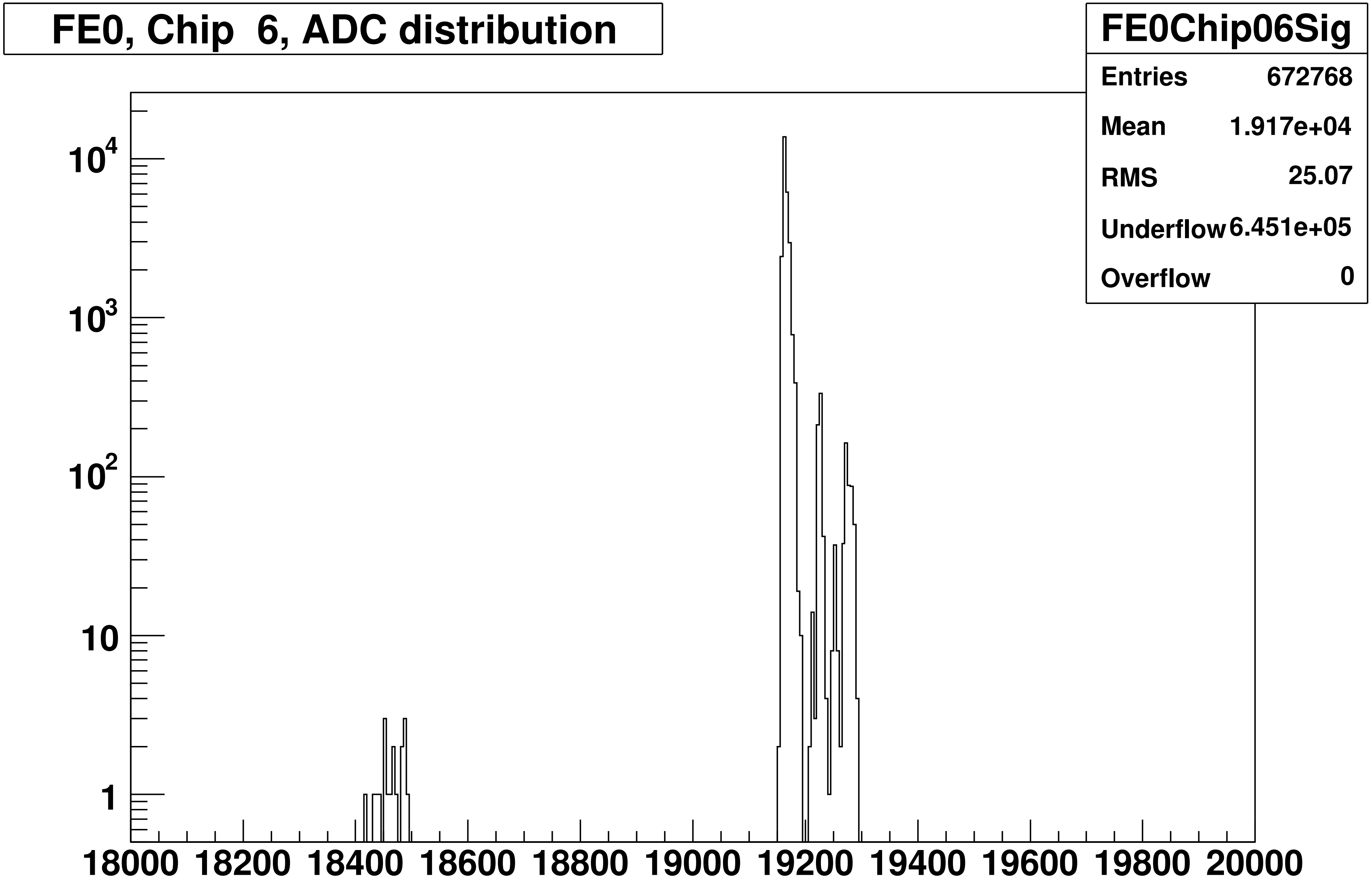
FE0, Chip 5, ADC distribution
FE0Chip05Ped
Entries 672768
Mean 8.03
RMS 1.555
Underflow 0
Overflow 2.635e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
200


FE0, Chip 5, ADC distribution
FE0Chip05Sig
Entries 672768
Mean 1.917e+04
RMS 8.277
Underflow 6.464e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000

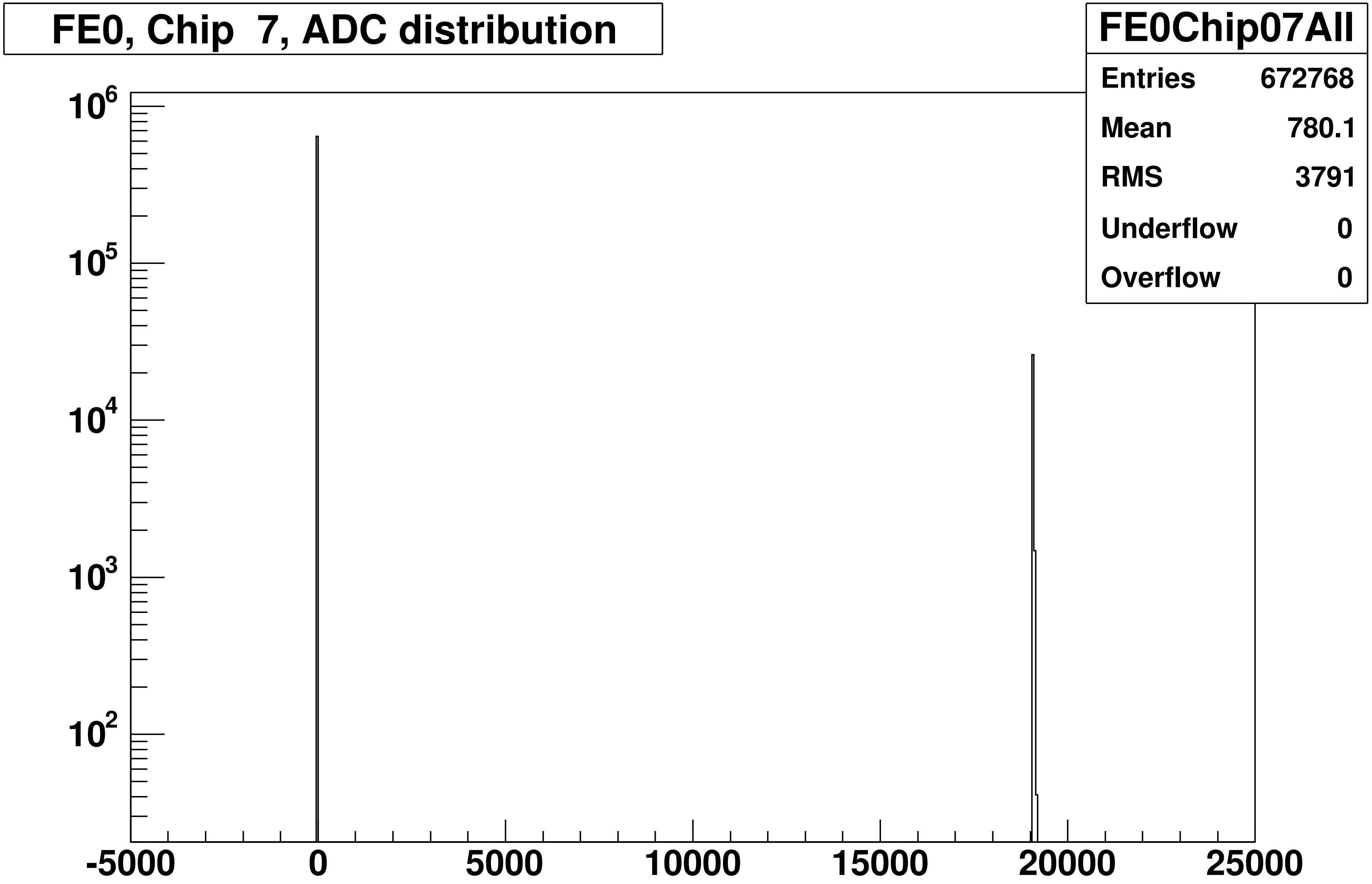

FE0, Chip 6, ADC distribution
FE0Chip06All
Entries 672768
Mean 788
RMS 3805
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE0, Chip 6, ADC distribution
FE0Chip06Ped
Entries 672768
Mean 0.3381
RMS 1.343
Underflow 0
Overflow 2.767e+04
10^5
10^4
10^3
10^2
10
1
-200 -150 -100 -50 0 50 100 150 200



FE0, Chip 6, ADC distribution
FE0Chip06Sig
Entries 672768
Mean 1.917e+04
RMS 25.07
Underflow 6.451e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE0, Chip 7, ADC distribution
FE0Chip07All
Entries 672768
Mean 780.1
RMS 3791
Underflow 0
Overflow 0
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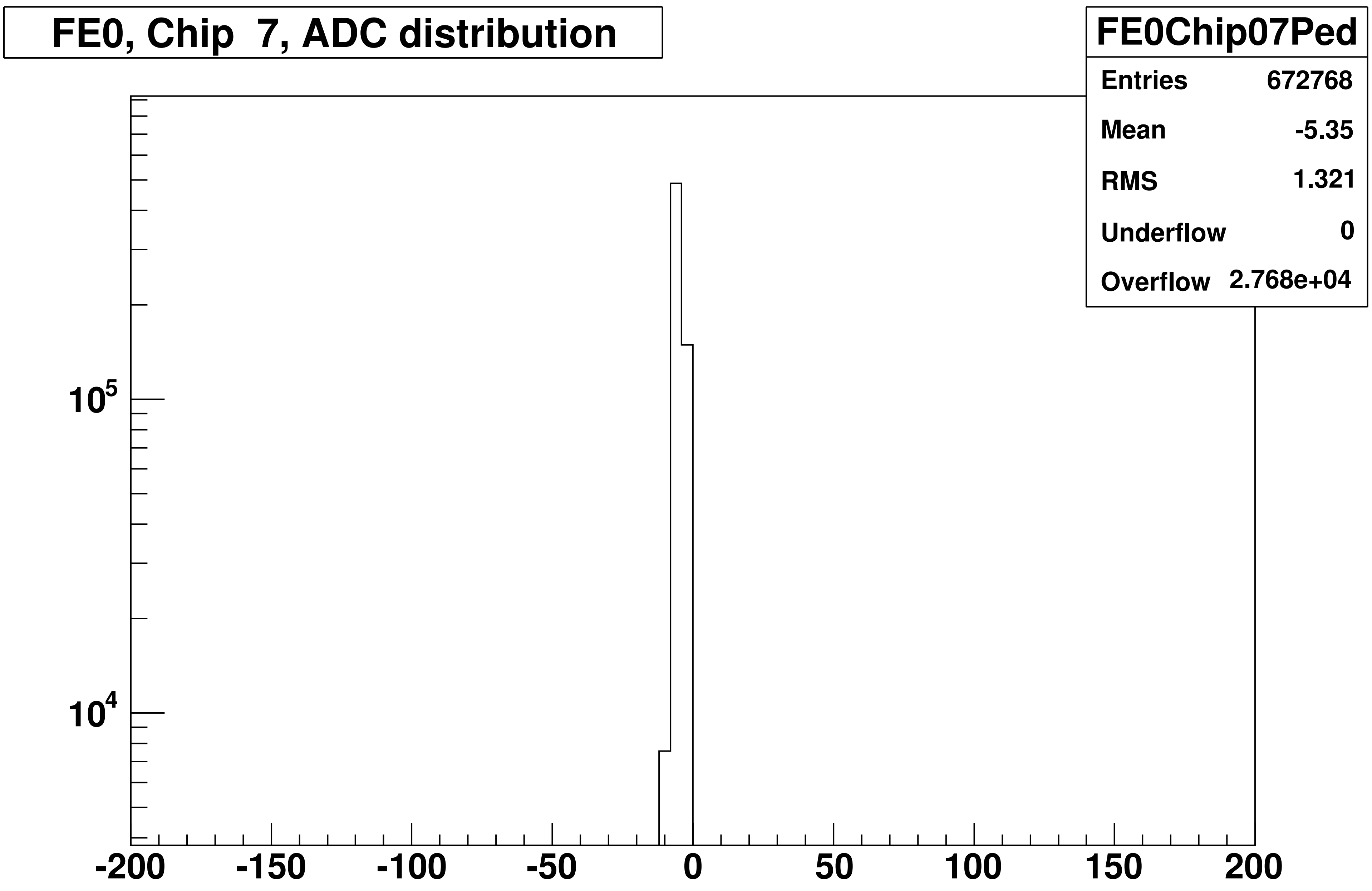
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000


FE0, Chip 7, ADC distribution
FE0Chip07Ped
Entries 672768
Mean -5.35
RMS 1.321
Underflow 0
Overflow 2.768e+04
10^5
10^4
-200
-150
-100
-50
0
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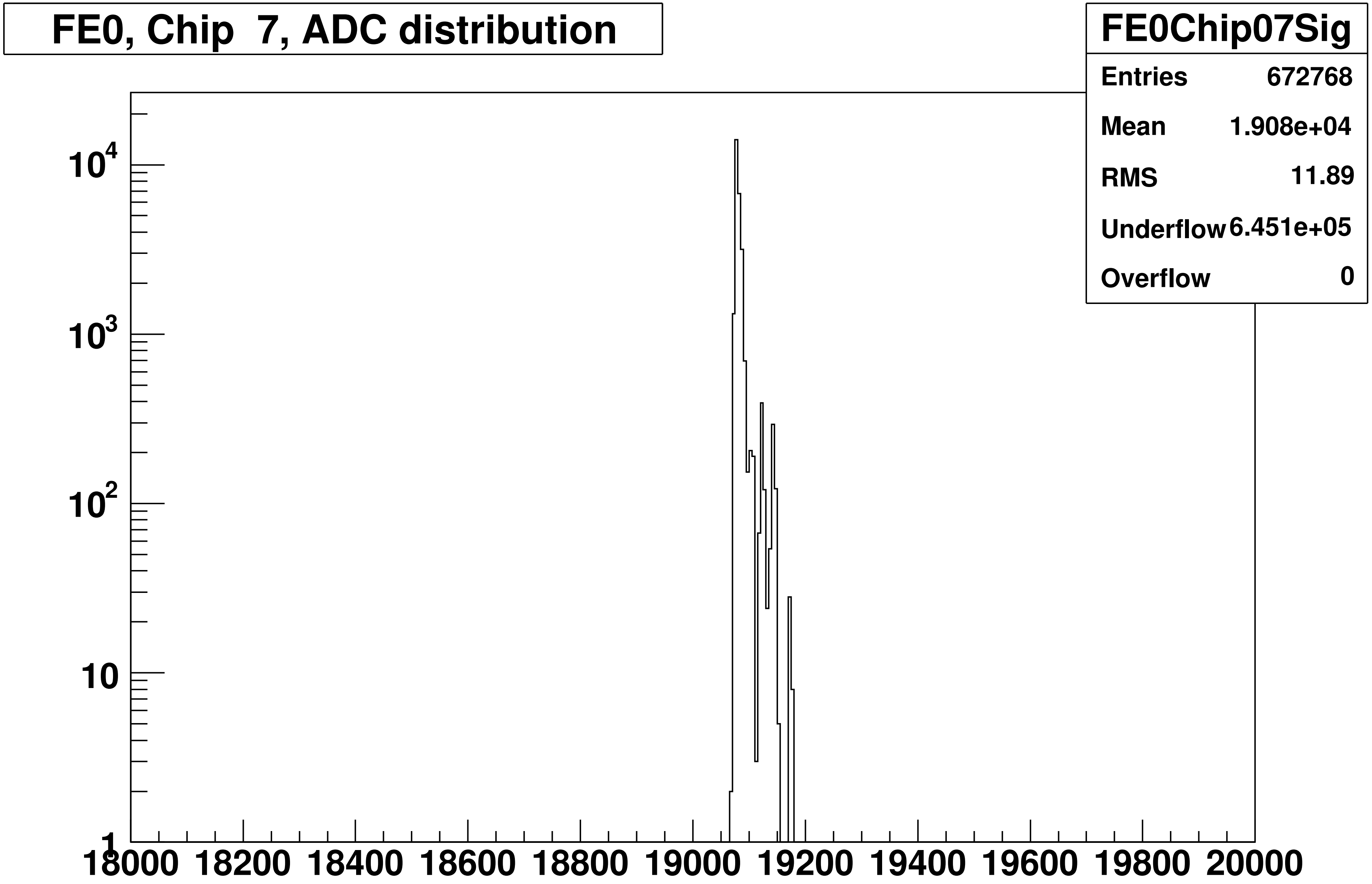
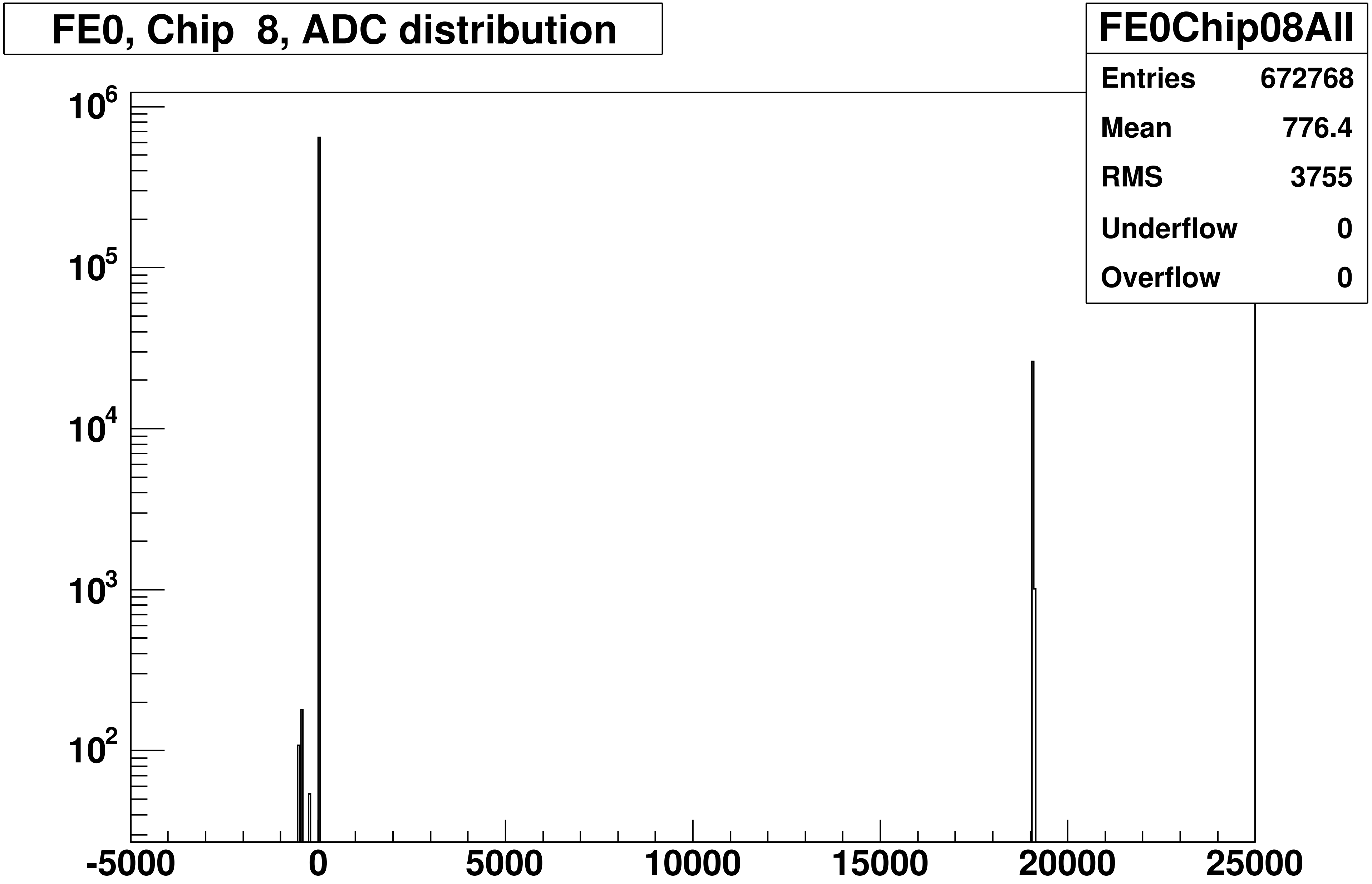
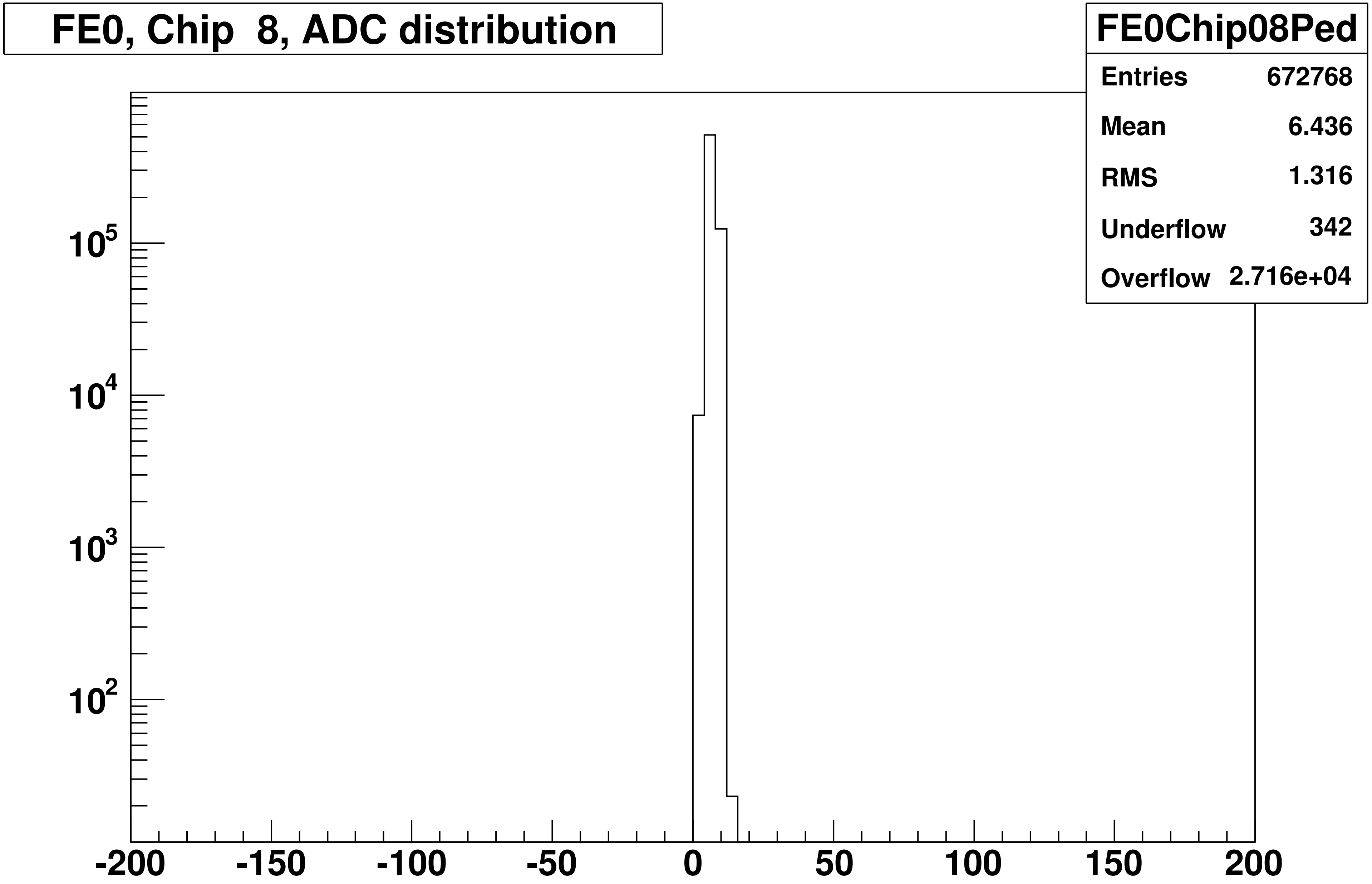
100
150
200

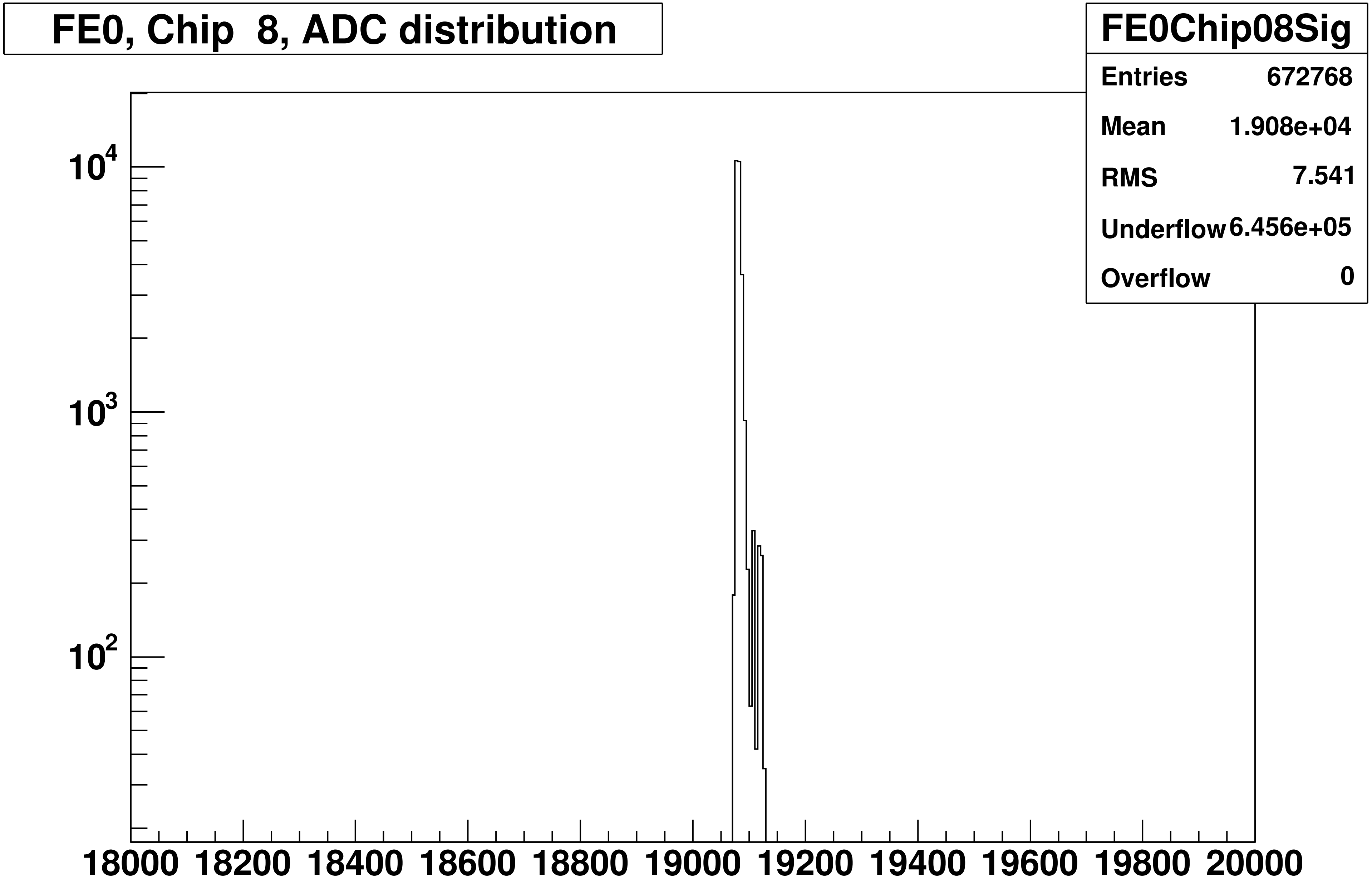


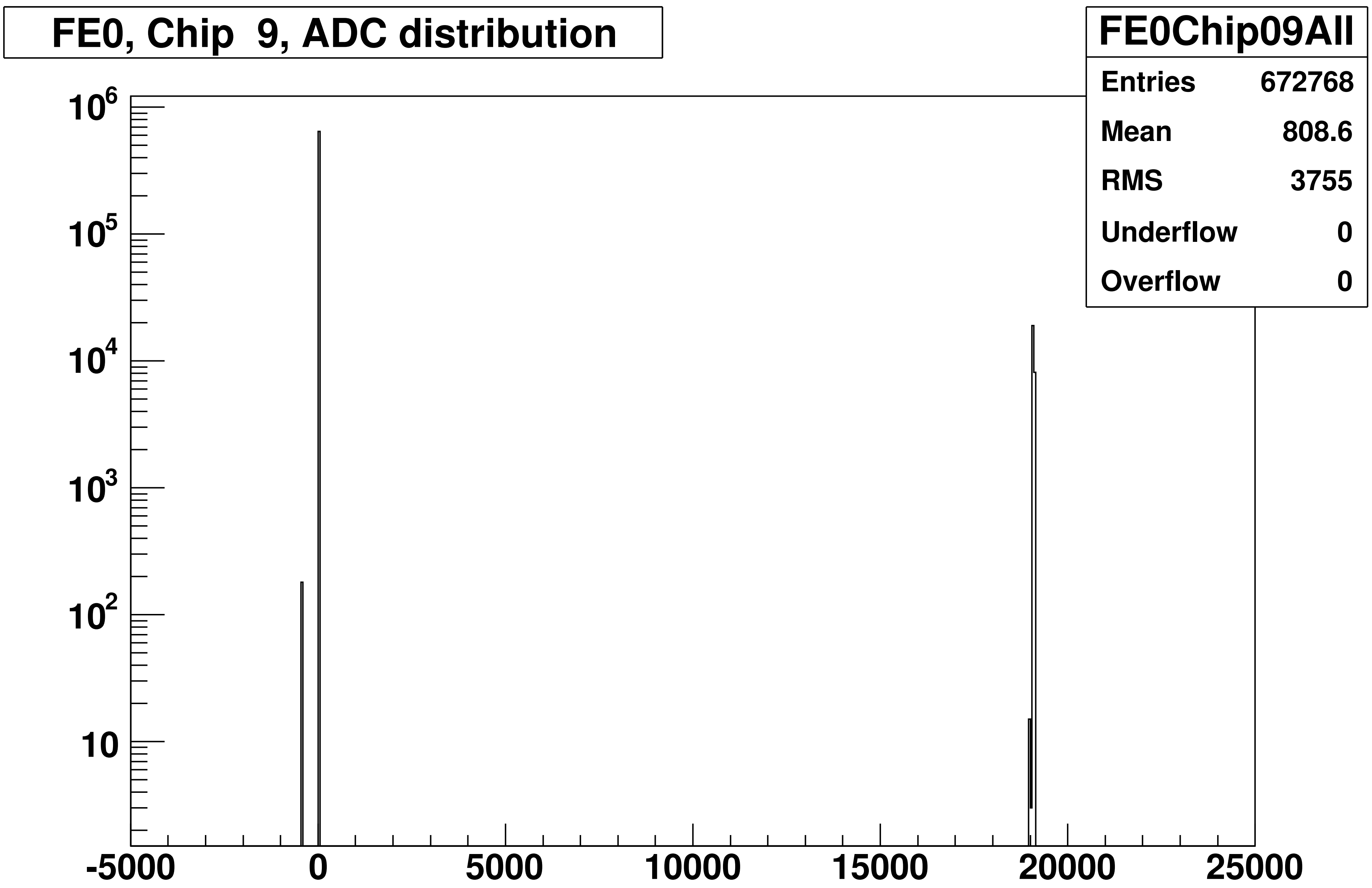
FE0, Chip 7, ADC distribution
FE0Chip07Sig
Entries 672768
Mean 1.908e+04
RMS 11.89
Underflow 6.451e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE0, Chip 8, ADC distribution
FE0Chip08All
Entries 672768
Mean 776.4
RMS 3755
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000


FE0, Chip 8, ADC distribution
FE0Chip08Ped
Entries 672768
Mean 6.436
RMS 1.316
Underflow 342
Overflow 2.716e+04
10^5
10^4
10^3
10^2
-200 -150 -100 -50 0 50 100 150 200


FE0, Chip 8, ADC distribution
FE0Chip08Sig
Entries 672768
Mean 1.908e+04
RMS 7.541
Underflow 6.456e+05
Overflow 0
10^4
10^3
10^2
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000


FE0, Chip 9, ADC distribution
FE0Chip09All
Entries 672768
Mean 808.6
RMS 3755
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
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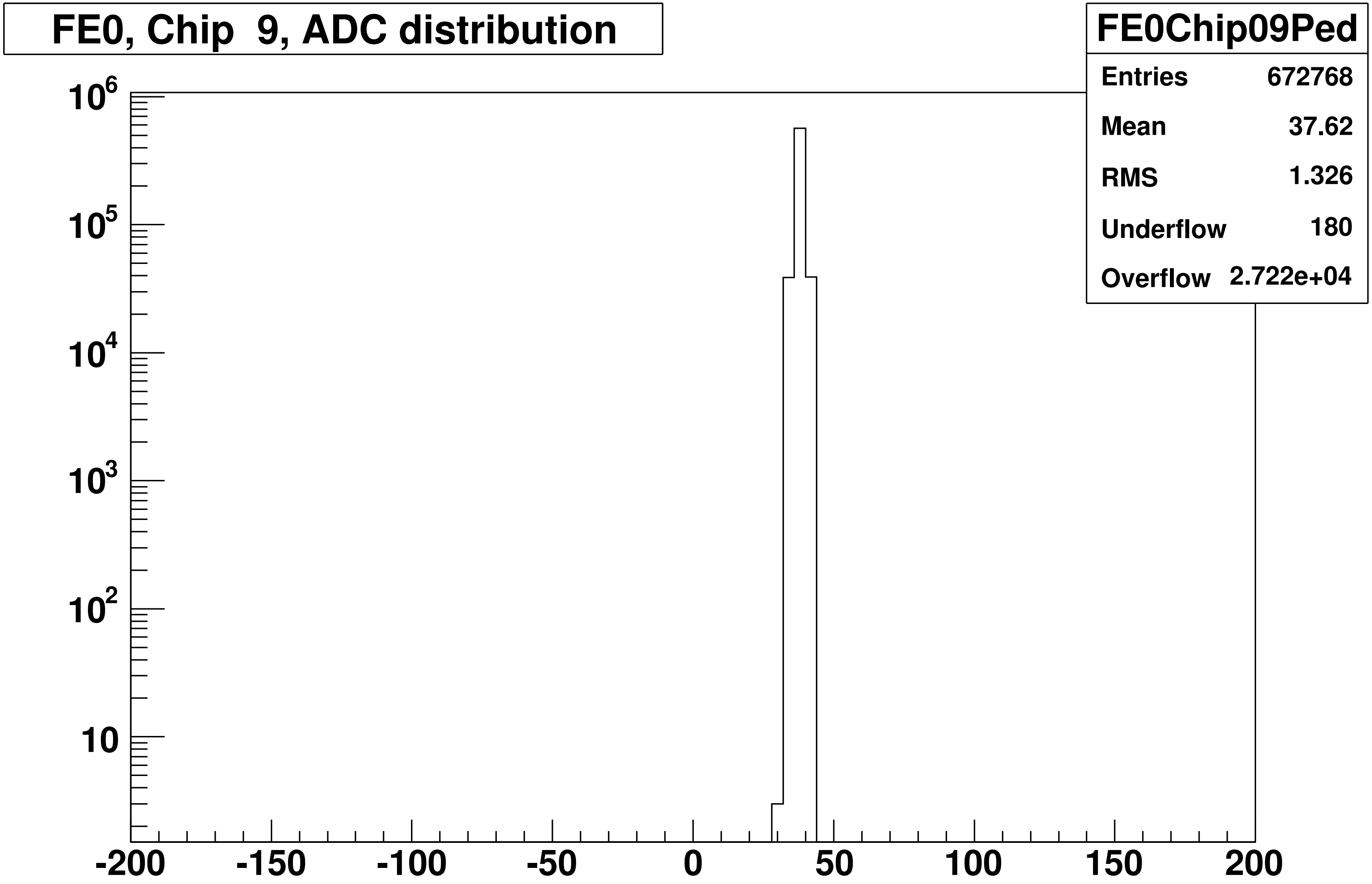
20000
25000


FE0, Chip 9, ADC distribution
FE0Chip09Ped
Entries 672768
Mean 37.62
RMS 1.326
Underflow 180
Overflow 2.722e+04
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10^5
10^4
10^3
10^2
10
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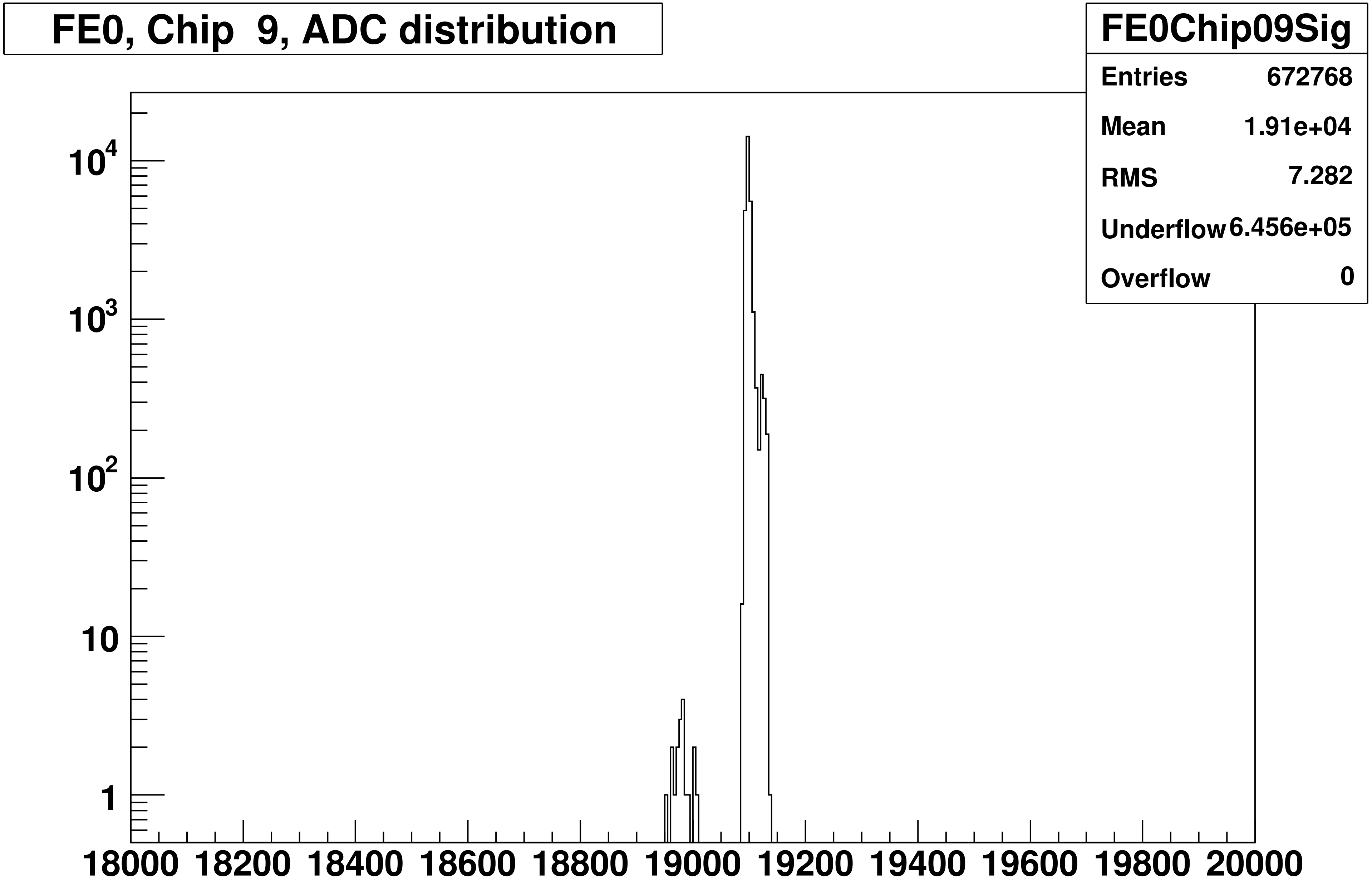
150
200


FE0, Chip 9, ADC distribution
FE0Chip09Sig
Entries 672768
Mean 1.91e+04
RMS 7.282
Underflow 6.456e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
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19000
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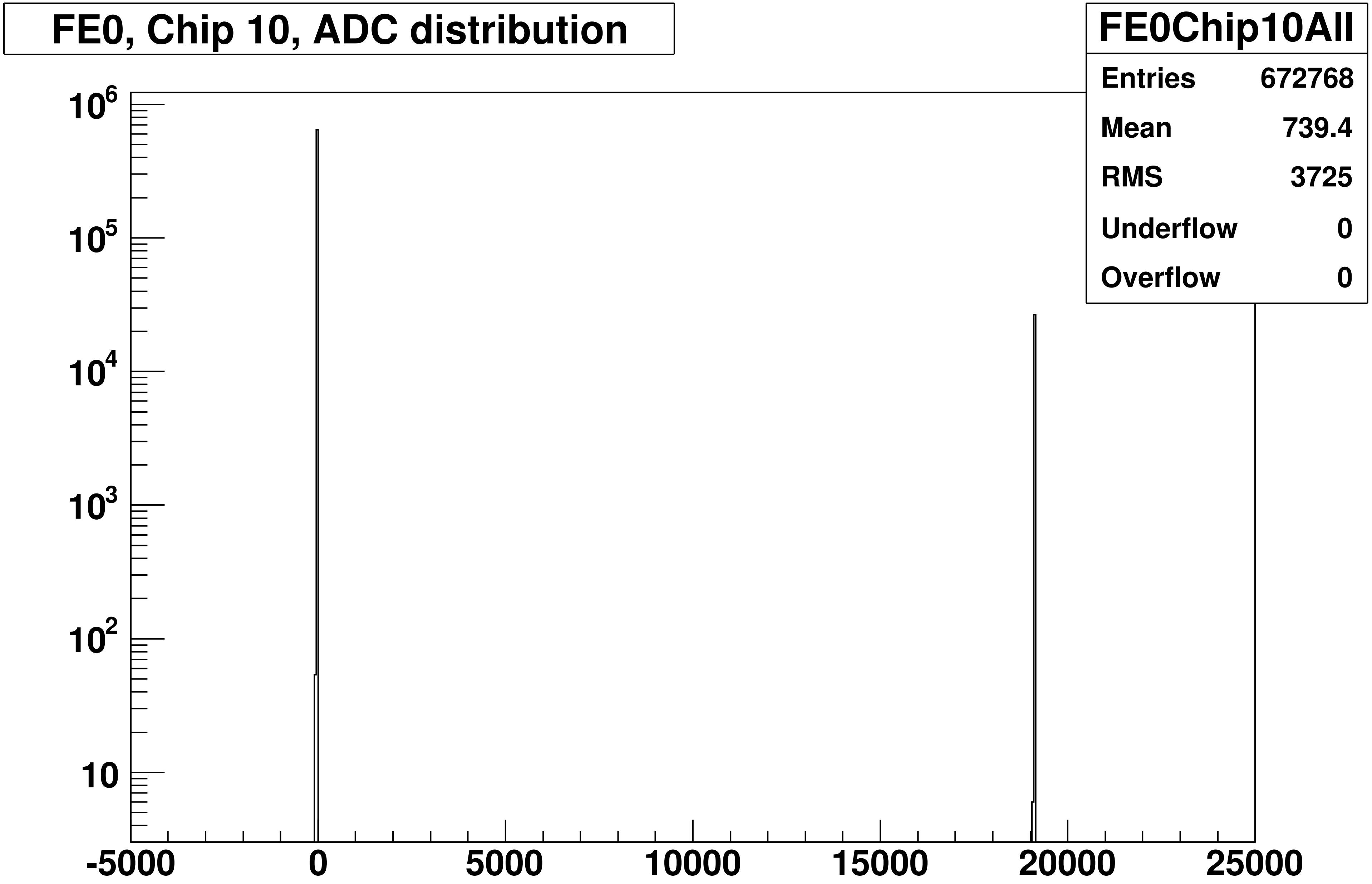
19400
19600
19800
20000



FE0, Chip 10, ADC distribution
FE0Chip10All
Entries 672768
Mean 739.4
RMS 3725
Underflow 0
Overflow 0
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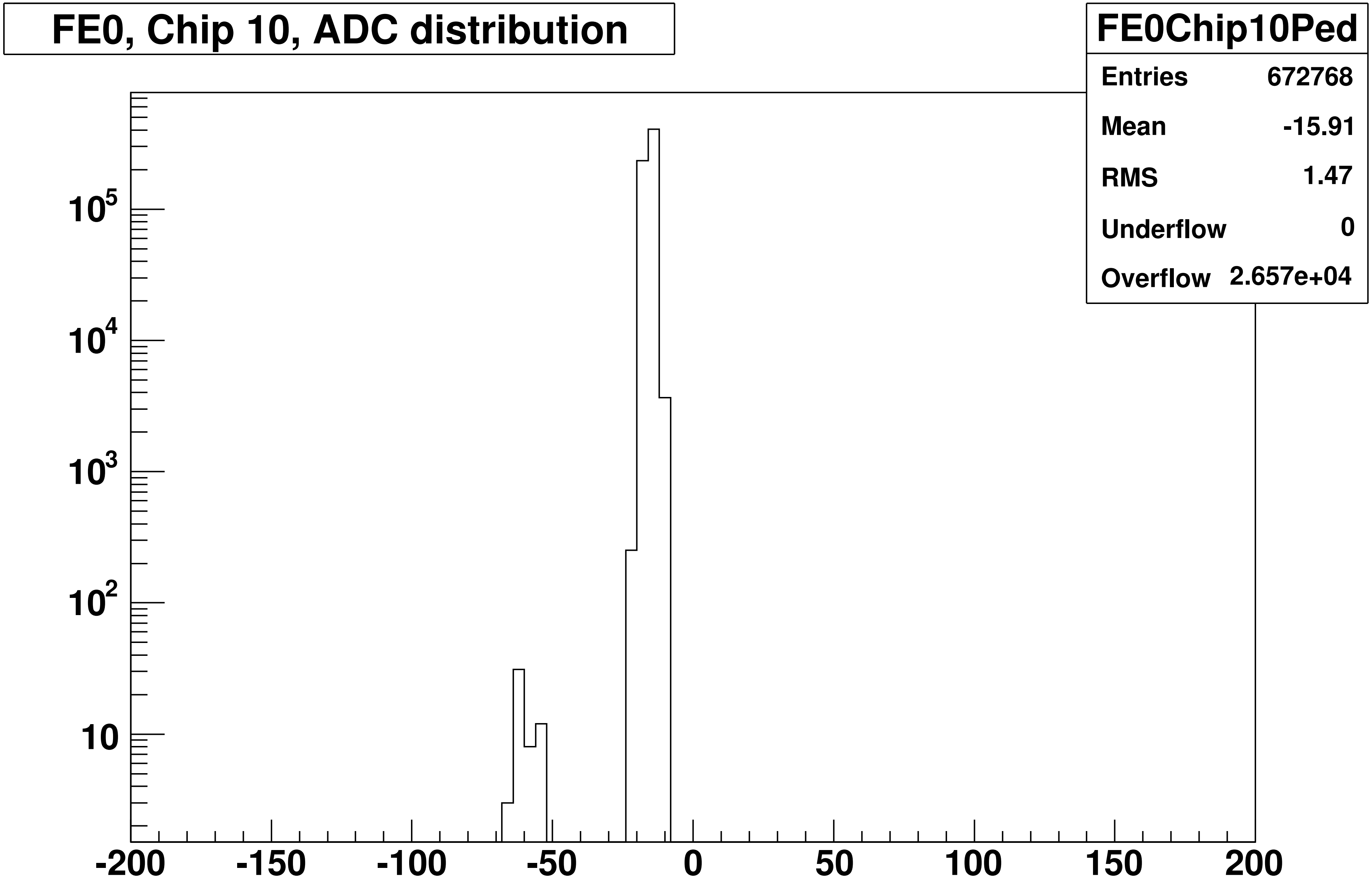
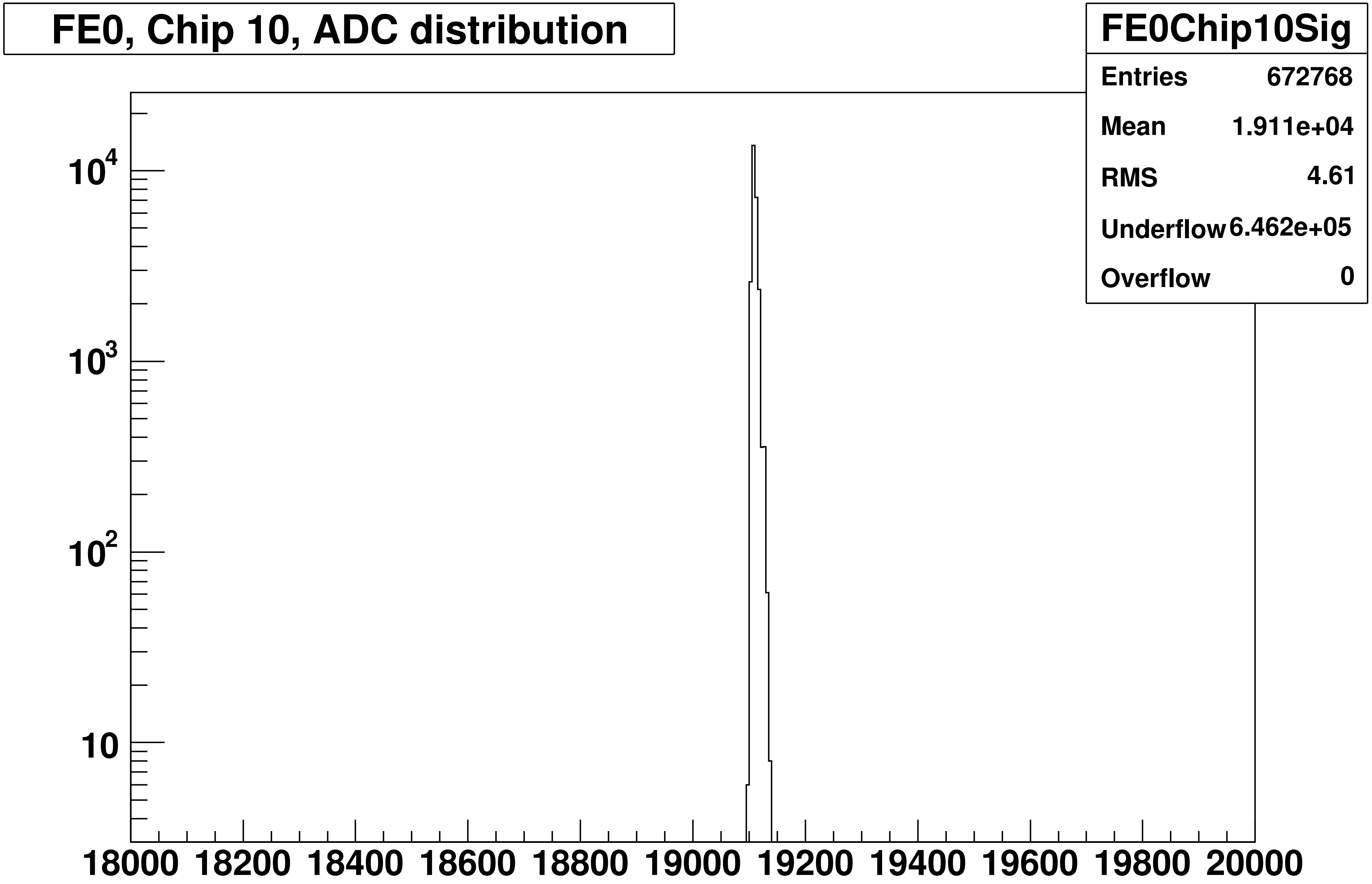
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000



FE0, Chip 10, ADC distribution
FE0Chip10Ped
Entries 672768
Mean -15.91
RMS 1.47
Underflow 0
Overflow 2.657e+04
10
10^2
10^3
10^4
10^5
-200
-150
-100
-50
0
50
100
150
200


FE0, Chip 10, ADC distribution
FE0Chip10Sig
Entries 672768
Mean 1.911e+04
RMS 4.61
Underflow 6.462e+05
Overflow 0
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10^3
10^2
10
18000
18200
18400
18600
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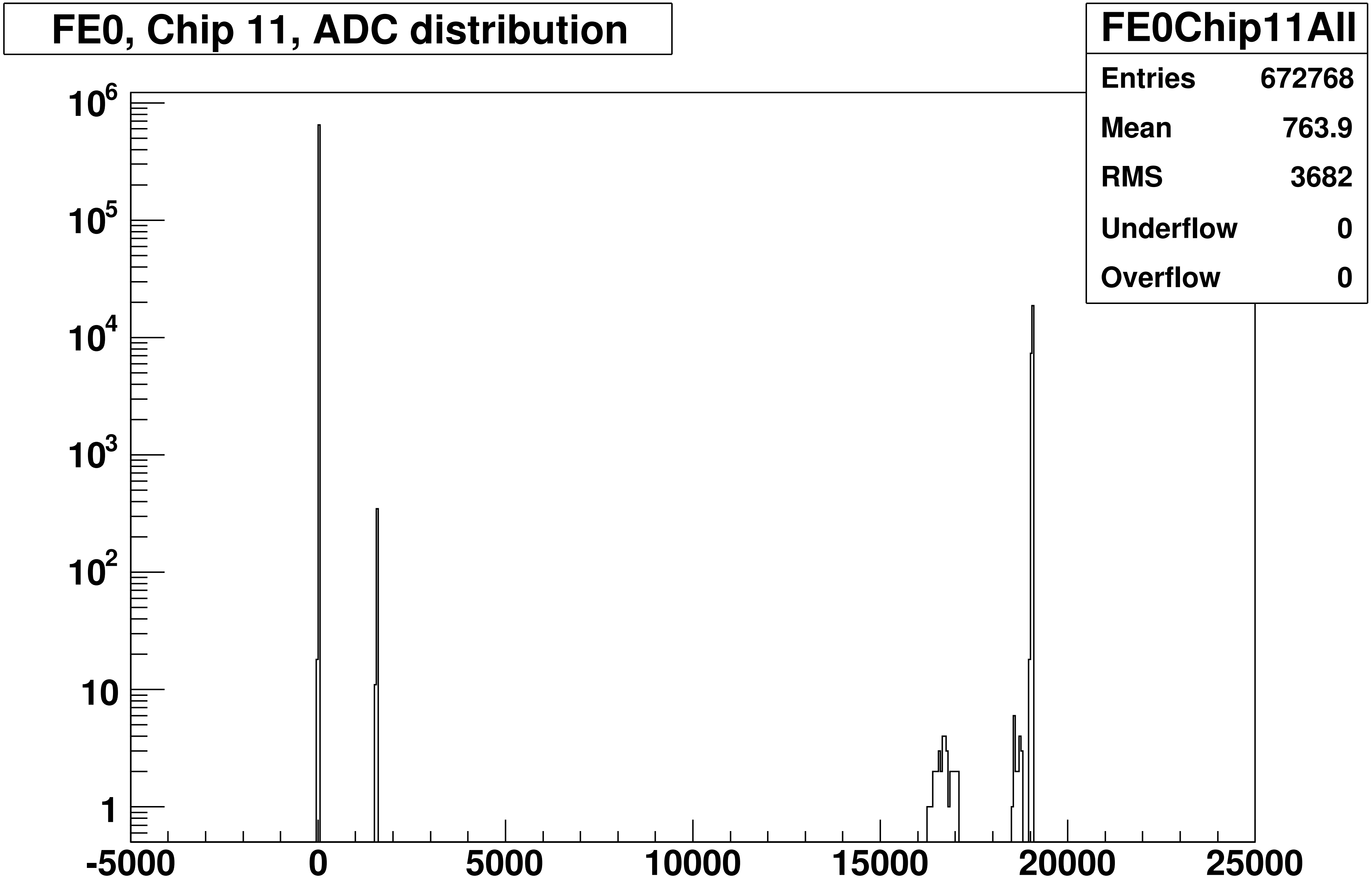
19000
19200
19400
19600
19800
20000



FE0, Chip 11, ADC distribution
FE0Chip11All
Entries 672768
Mean 763.9
RMS 3682
Underflow 0
Overflow 0
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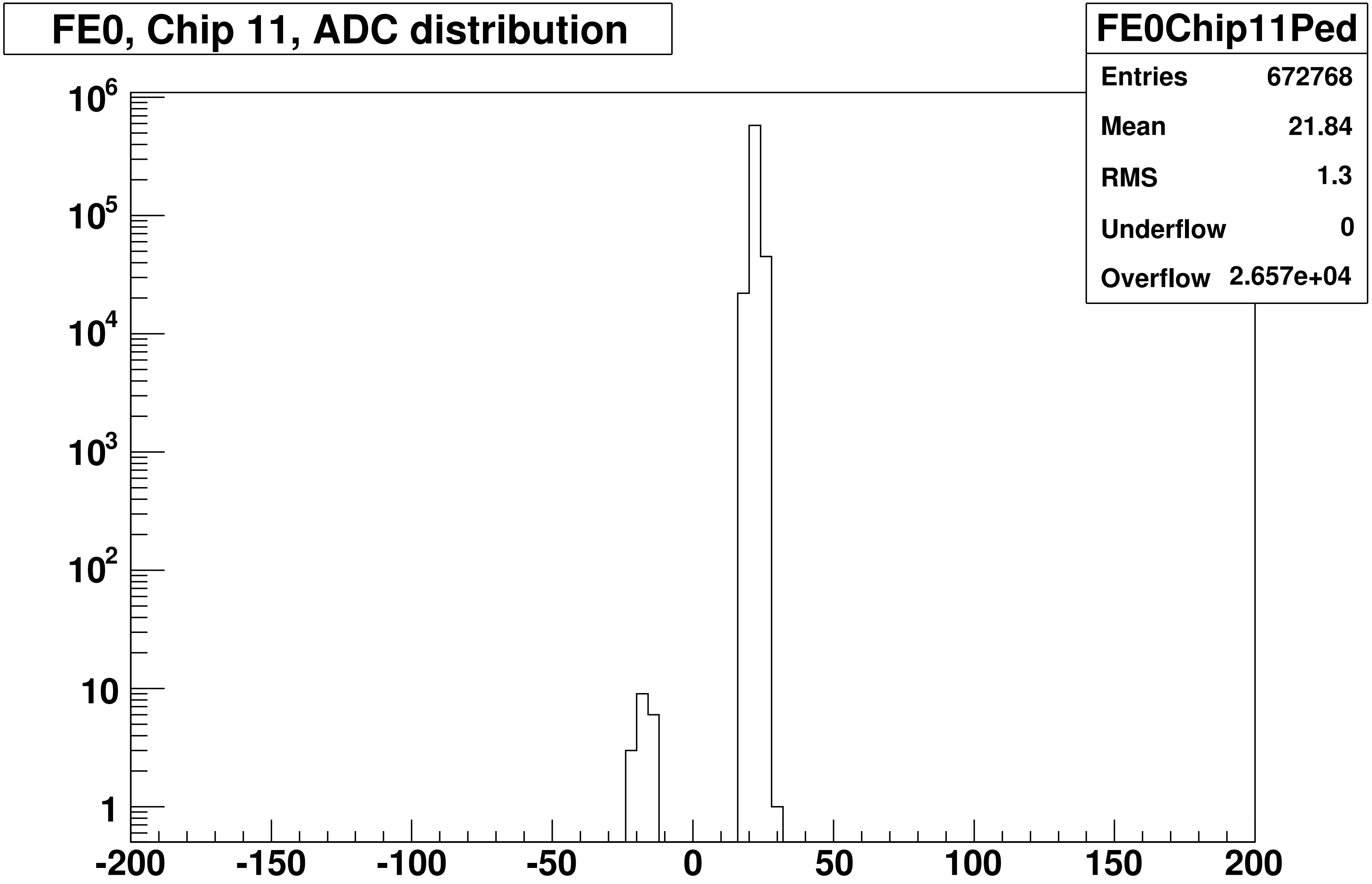
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE0, Chip 11, ADC distribution
FE0Chip11Ped
Entries 672768
Mean 21.84
RMS 1.3
Underflow 0
Overflow 2.657e+04
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10^4
10^3
10^2
10
1
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-100
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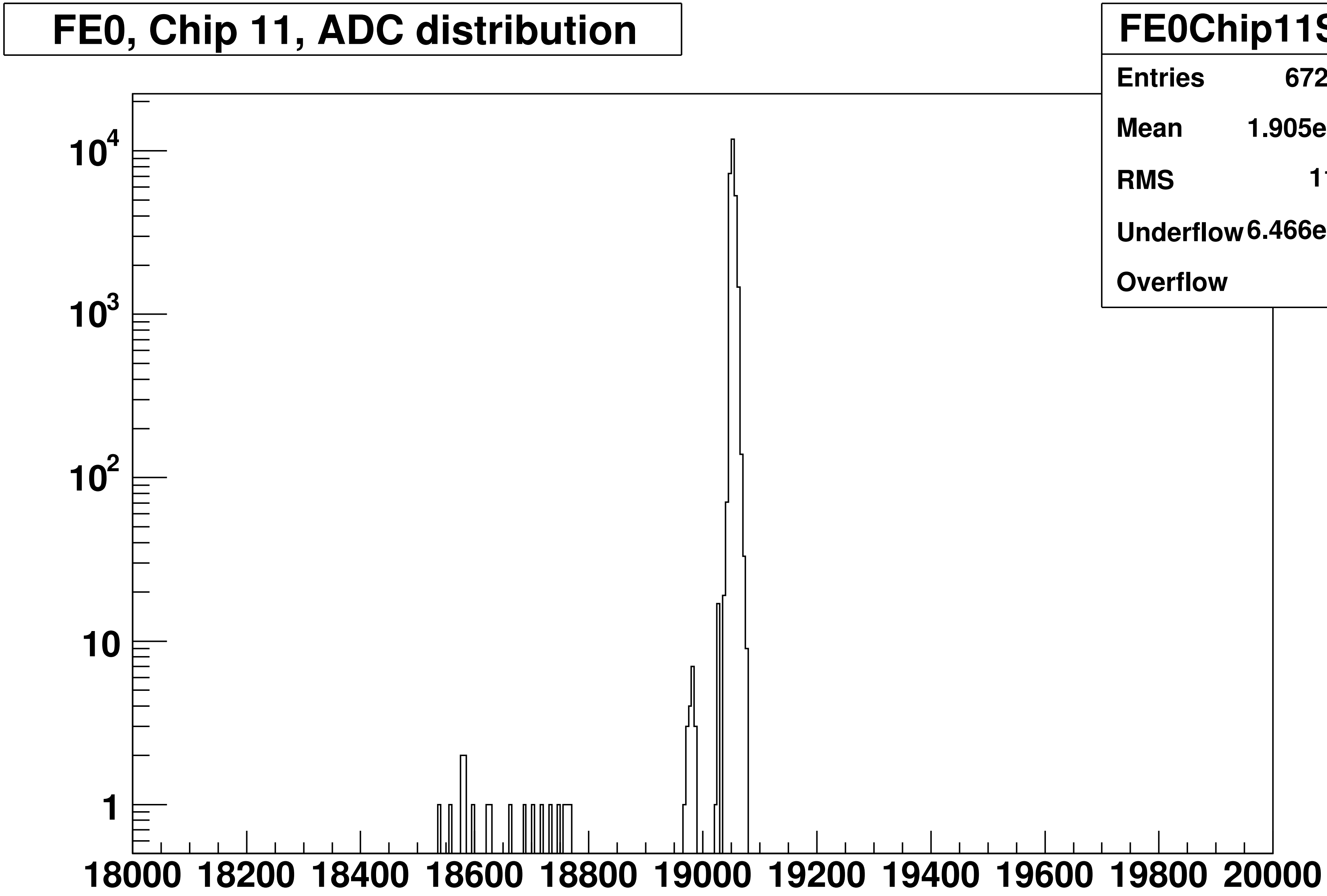
50
100
150
200


FE0, Chip 11, ADC distribution
FE0Chip11Sig
Entries 672768
Mean 1.905e+04
RMS 11.57
Underflow 6.466e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
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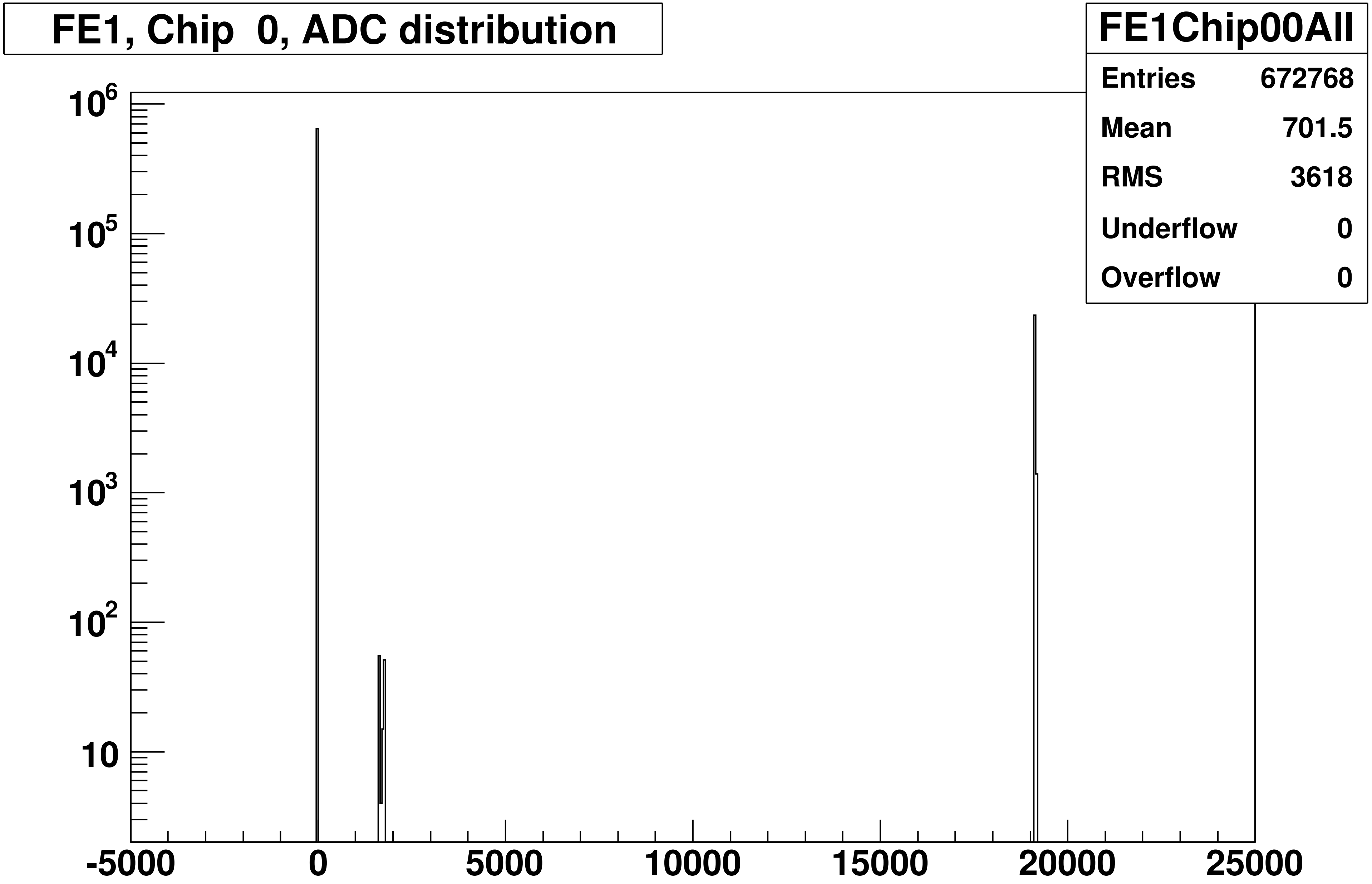
19600
19800
20000


FE1, Chip 0, ADC distribution
FE1Chip00All
Entries 672768
Mean 701.5
RMS 3618
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
-5000
0
5000
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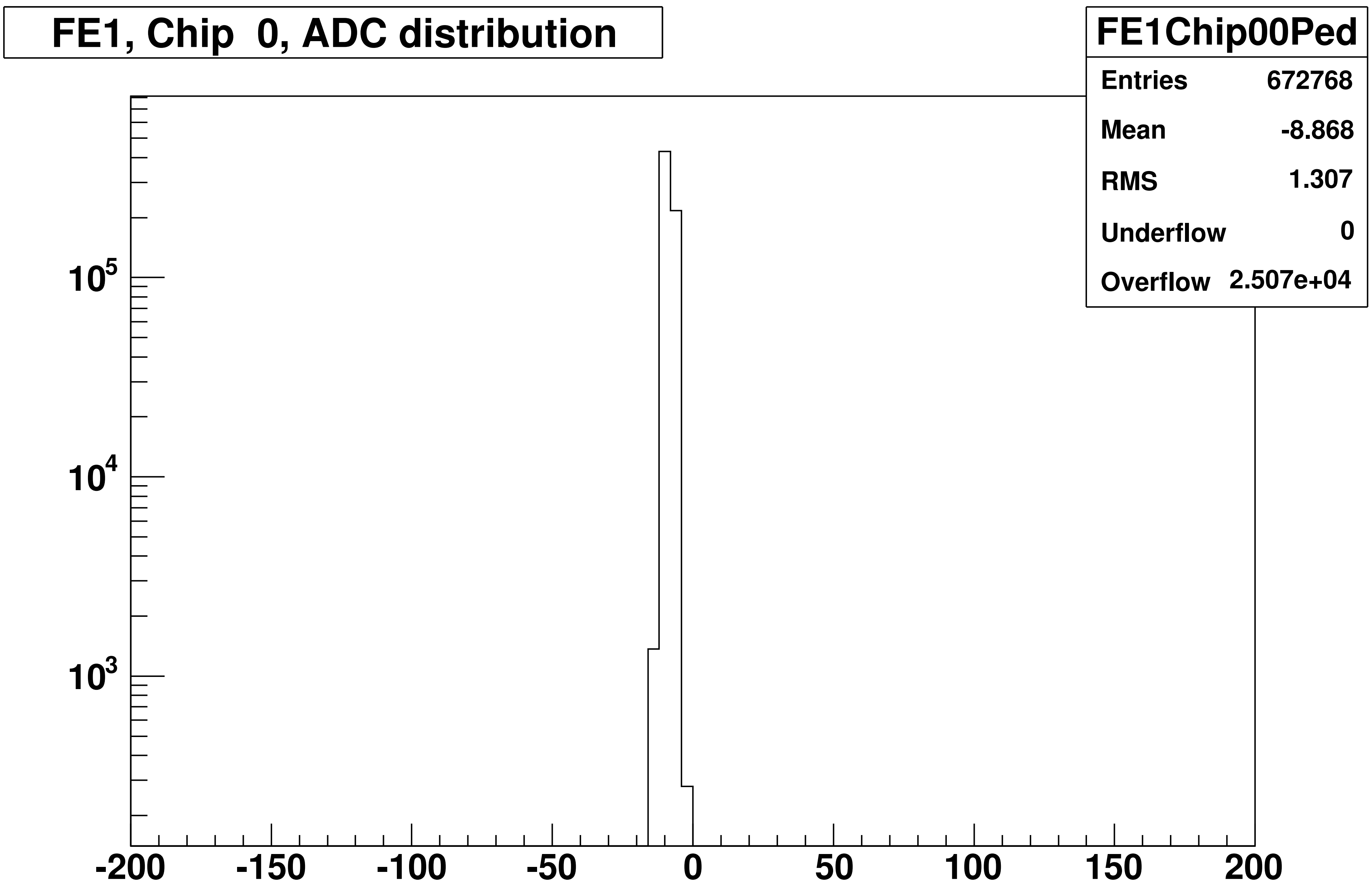
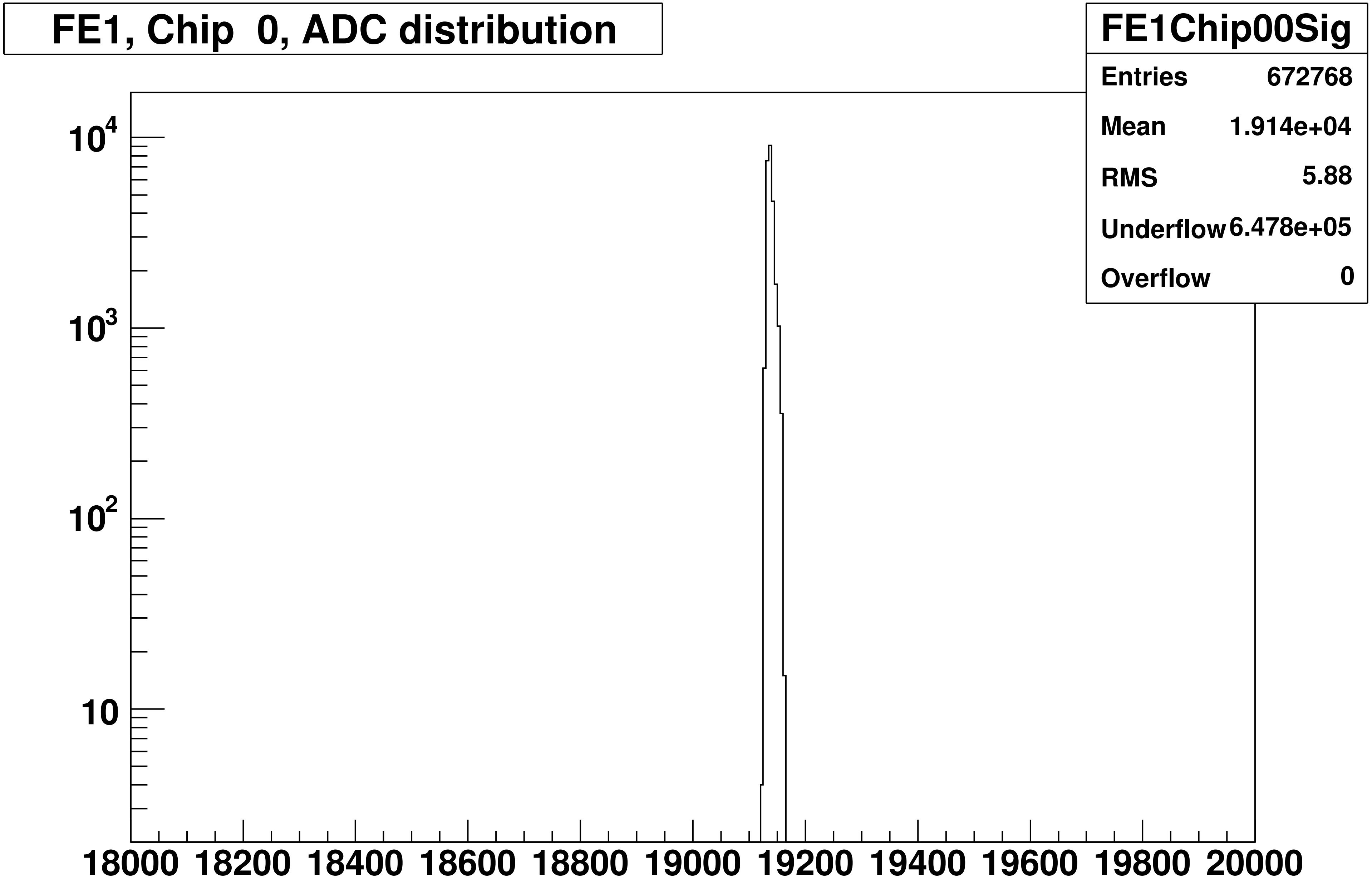
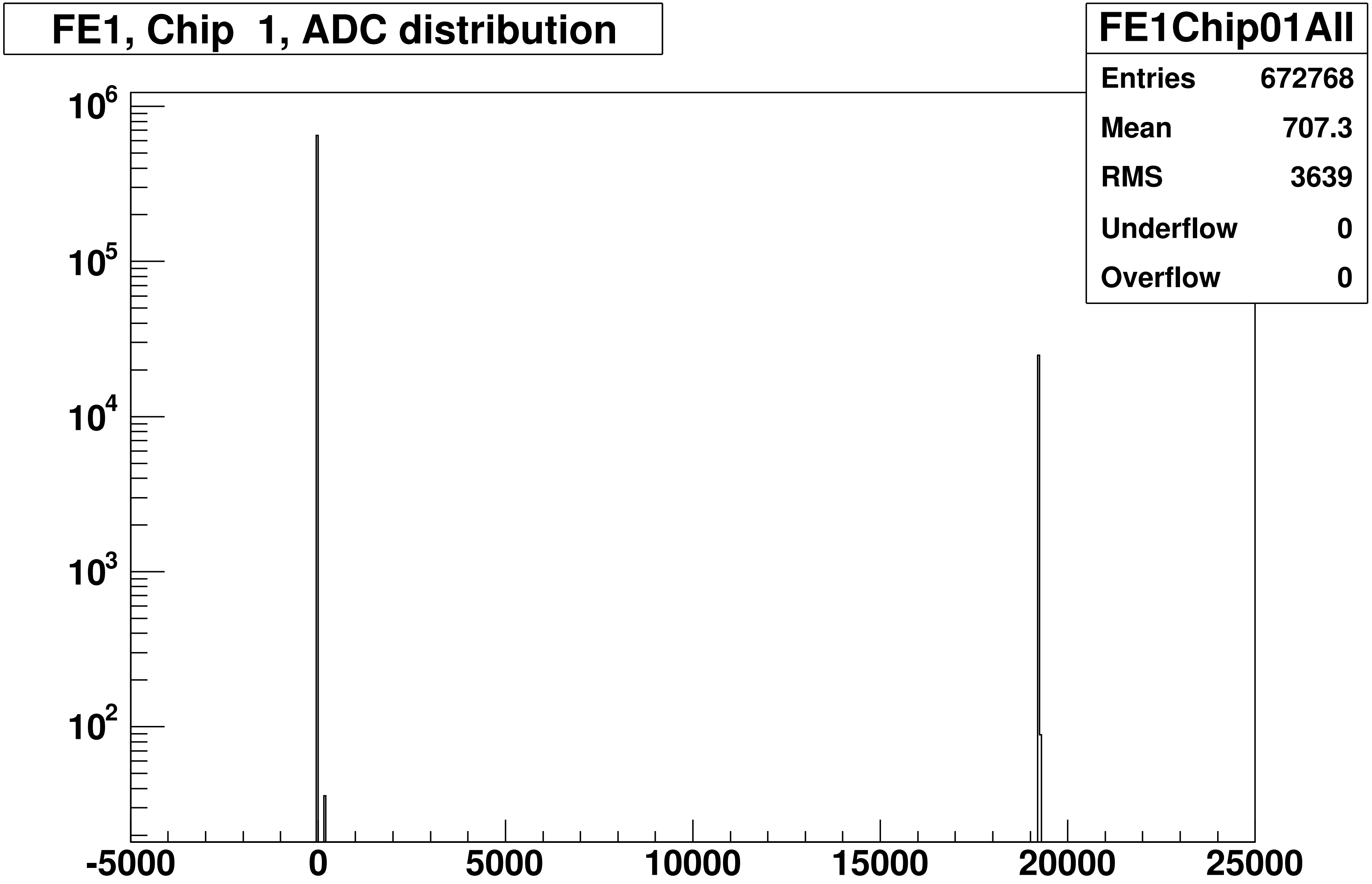
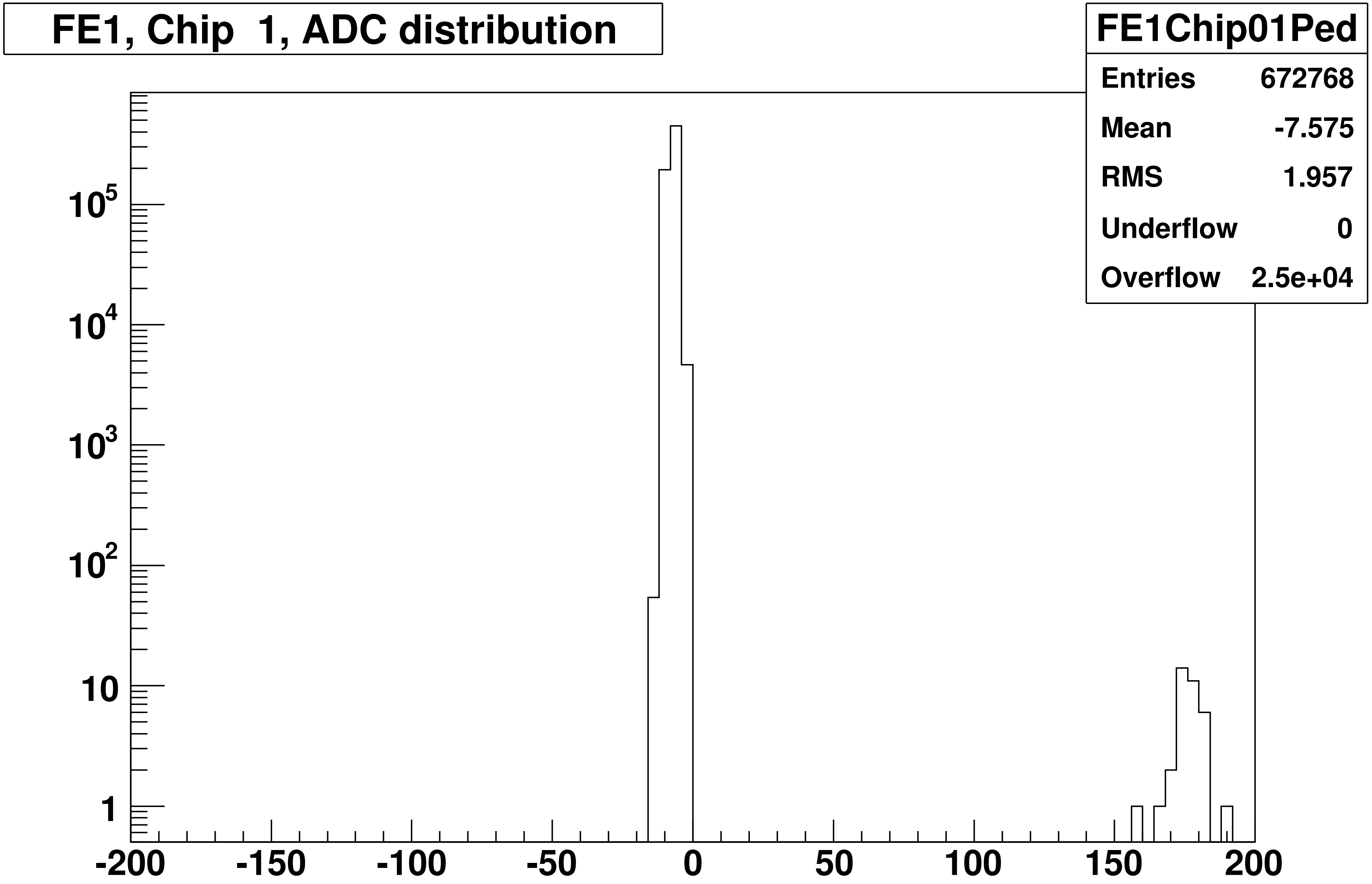

FE1, Chip 0, ADC distribution
FE1Chip00Ped
Entries 672768
Mean -8.868
RMS 1.307
Underflow 0
Overflow 2.507e+04
10^5
10^4
10^3
-200
-150
-100
-50
0
50
100
150
200

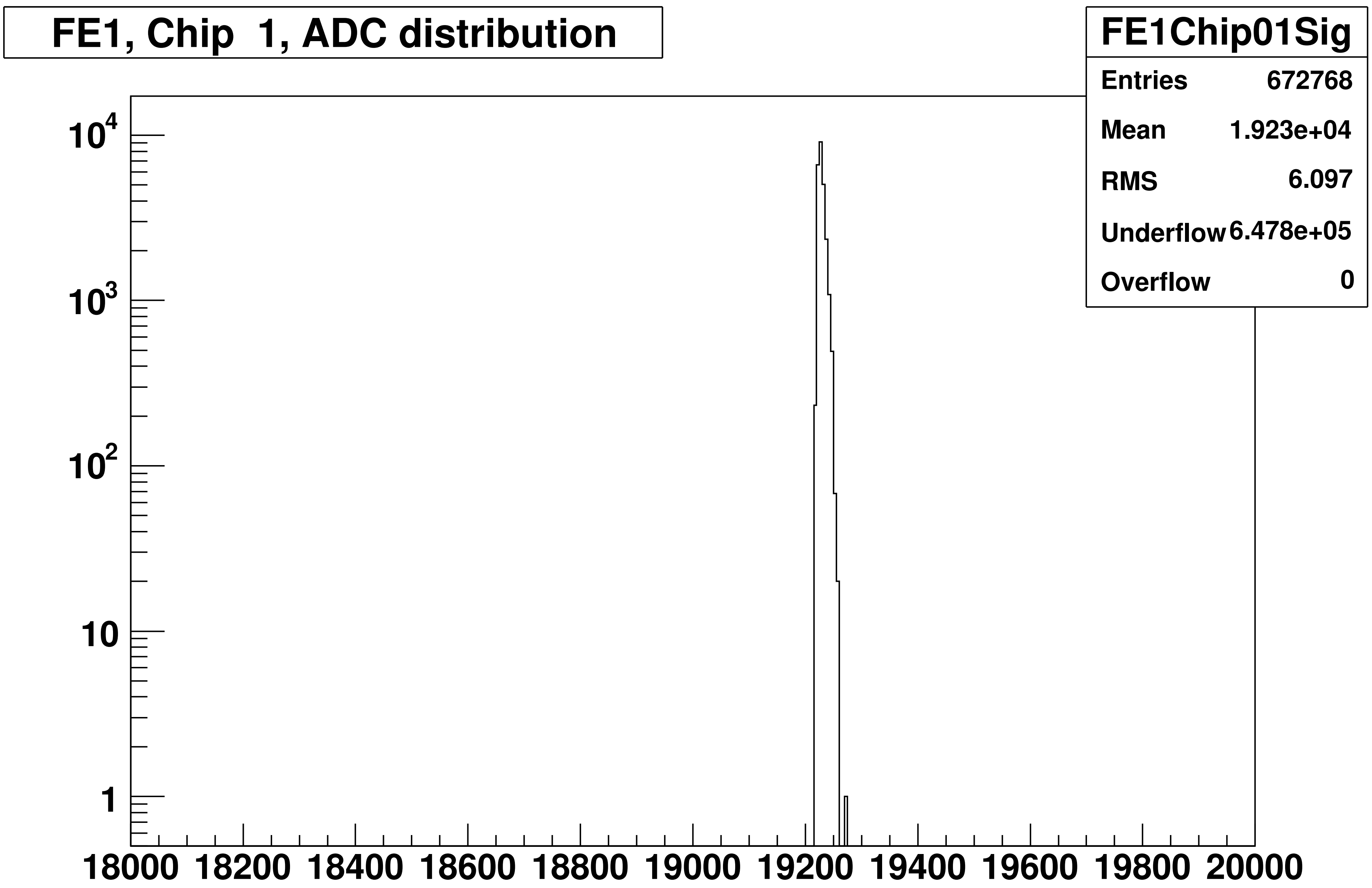

FE1, Chip 0, ADC distribution
FE1Chip00Sig
Entries 672768
Mean 1.914e+04
RMS 5.88
Underflow 6.478e+05
Overflow 0
10^4
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000

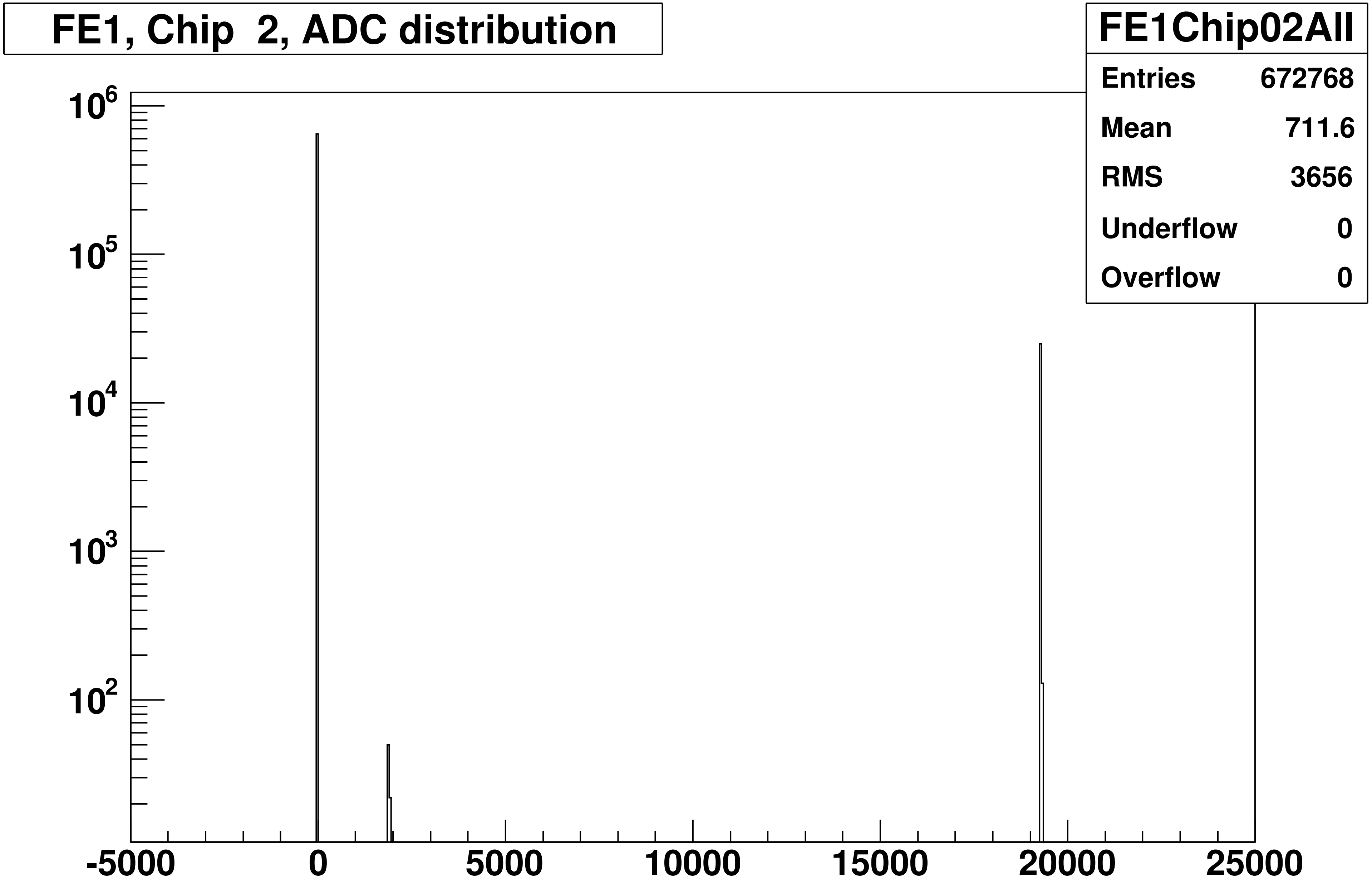


FE1, Chip 1, ADC distribution
FE1Chip01All
Entries 672768
Mean 707.3
RMS 3639
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000



FE1, Chip 1, ADC distribution
FE1Chip01Ped
Entries 672768
Mean -7.575
RMS 1.957
Underflow 0
Overflow 2.5e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
200


FE1, Chip 1, ADC distribution
FE1Chip01Sig
Entries 672768
Mean 1.923e+04
RMS 6.097
Underflow 6.478e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE1, Chip 2, ADC distribution
FE1Chip02All
Entries 672768
Mean 711.6
RMS 3656
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
-5000
0
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10000
15000
20000
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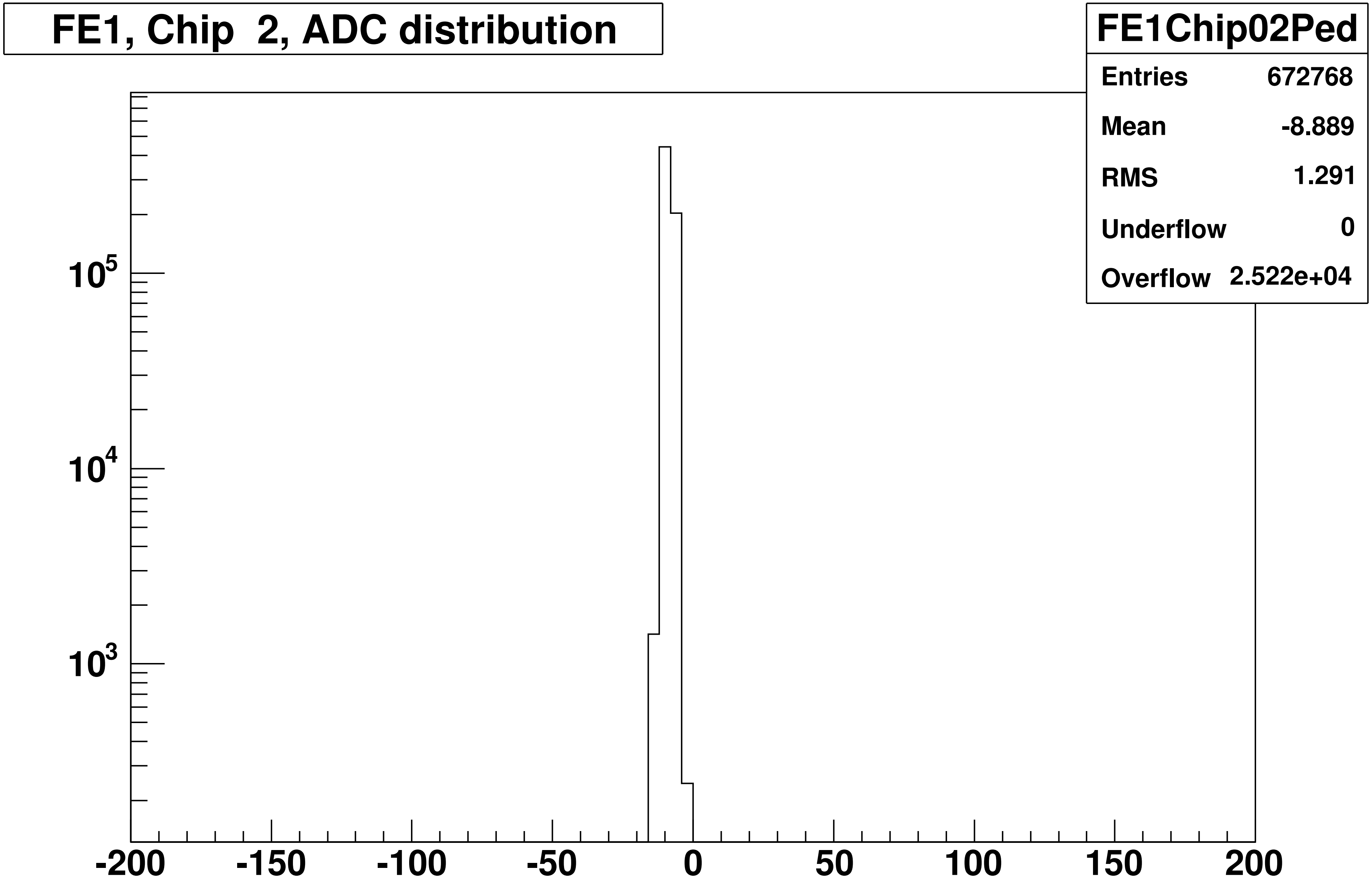
FE1, Chip 2, ADC distribution
FE1Chip02Ped
Entries 672768
Mean -8.889
RMS 1.291
Underflow 0
Overflow 2.522e+04
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10^4
10^3
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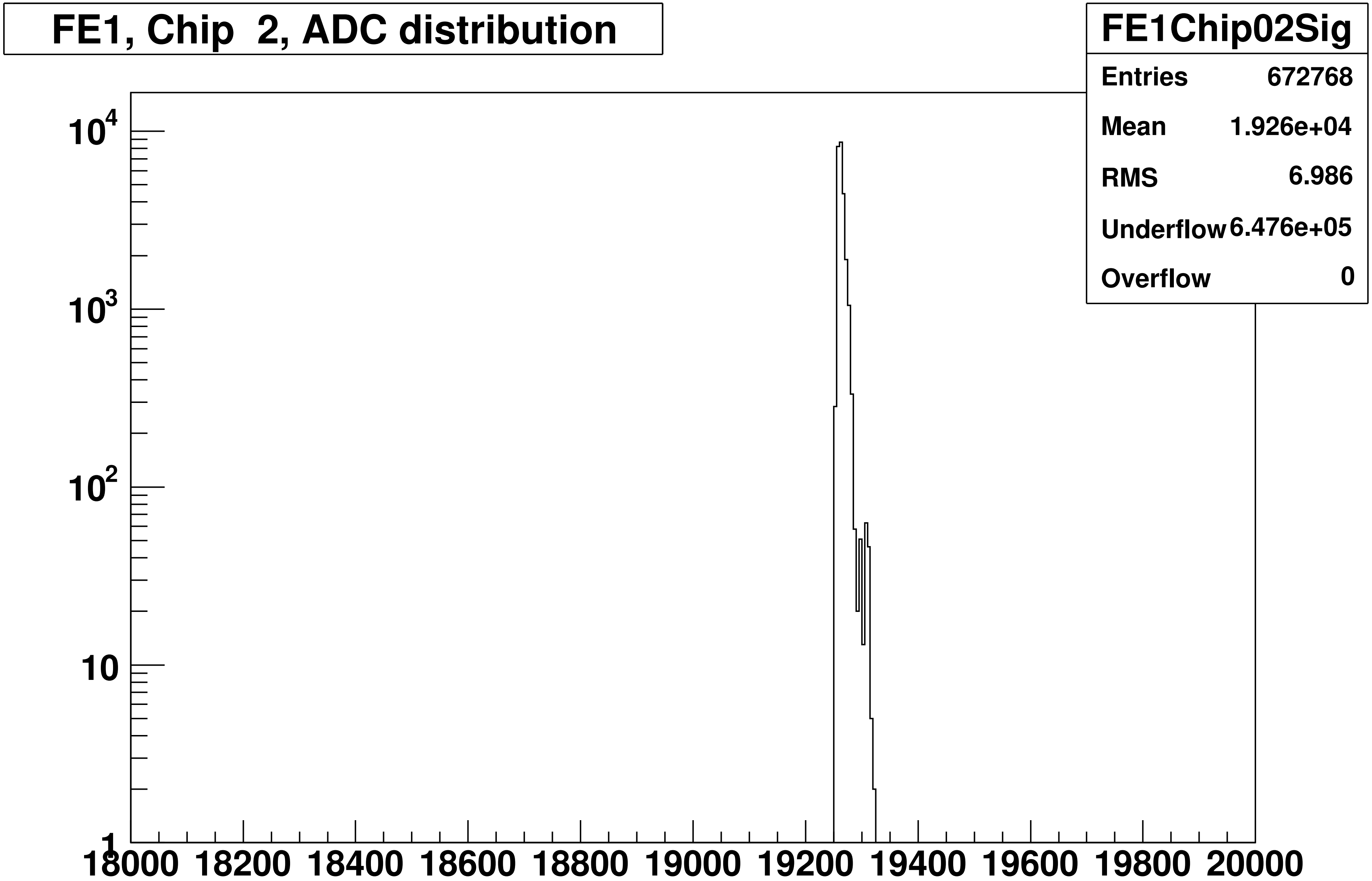
FE1, Chip 2, ADC distribution
FE1Chip02Sig
Entries 672768
Mean 1.926e+04
RMS 6.986
Underflow 6.476e+05
Overflow 0
10^4
10^3
10^2
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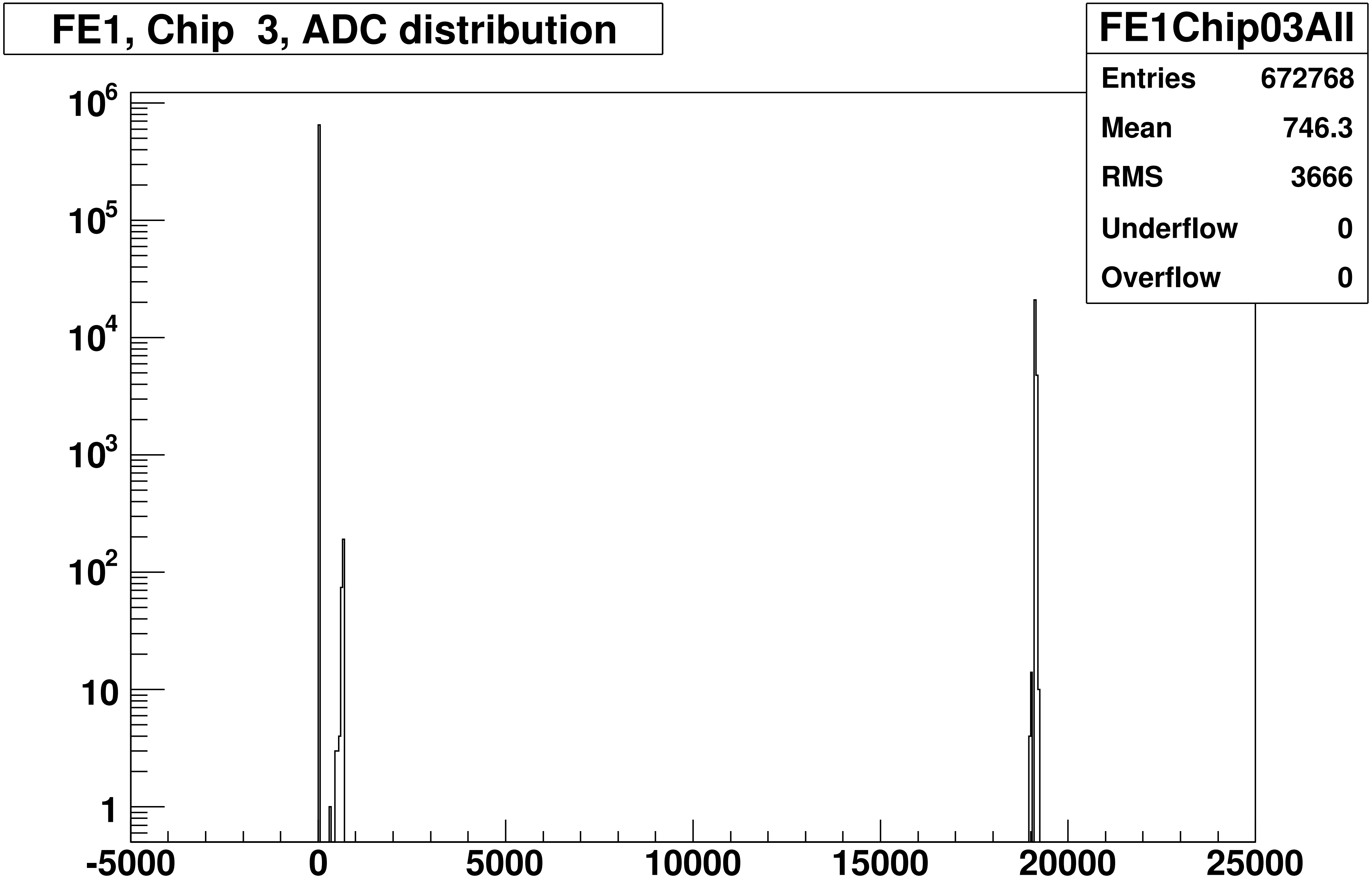
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE1, Chip 3, ADC distribution
FE1Chip03All
Entries 672768
Mean 746.3
RMS 3666
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
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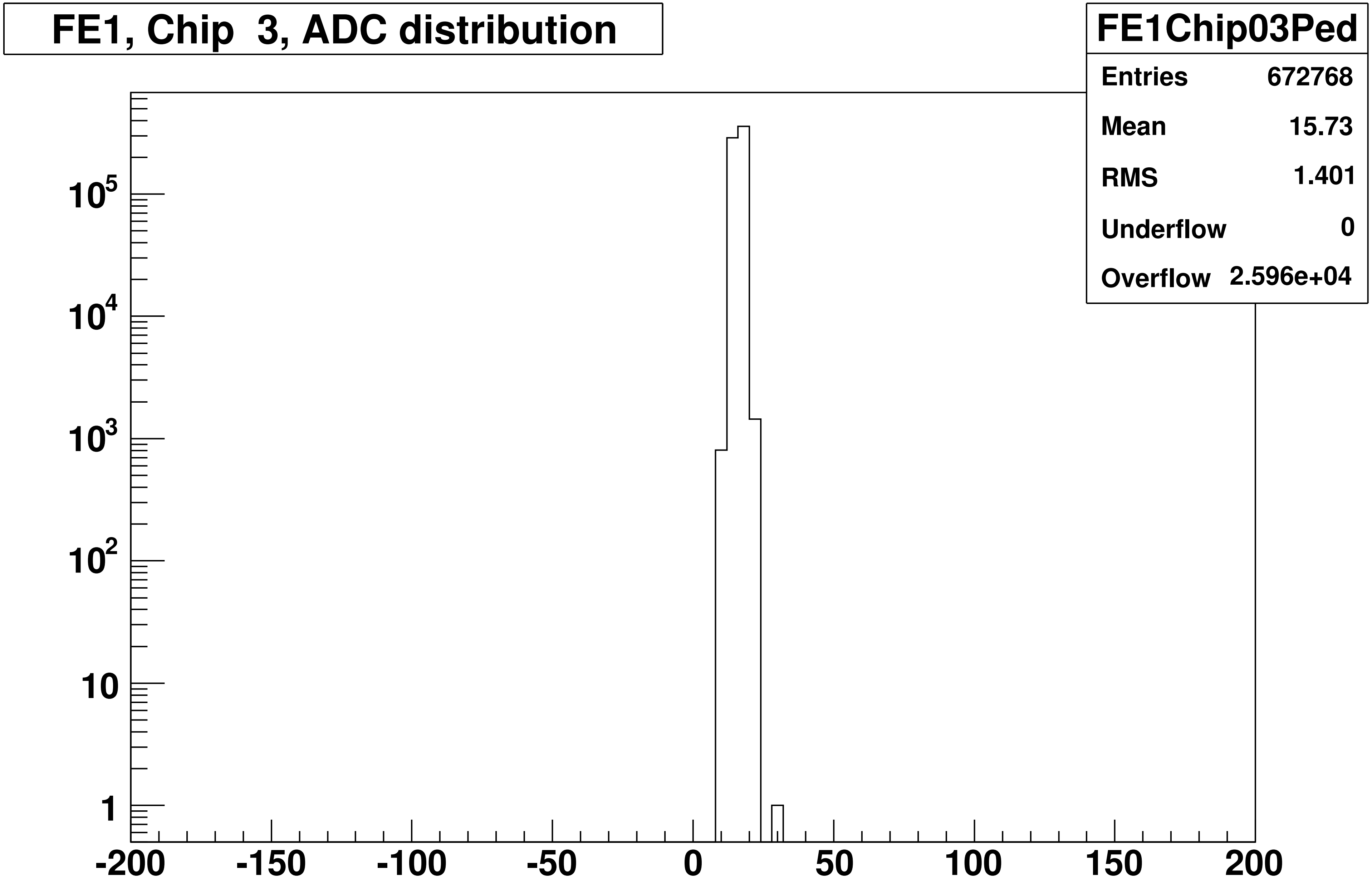
FE1, Chip 3, ADC distribution
FE1Chip03Ped
Entries 672768
Mean 15.73
RMS 1.401
Underflow 0
Overflow 2.596e+04
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10^3
10^2
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100
150
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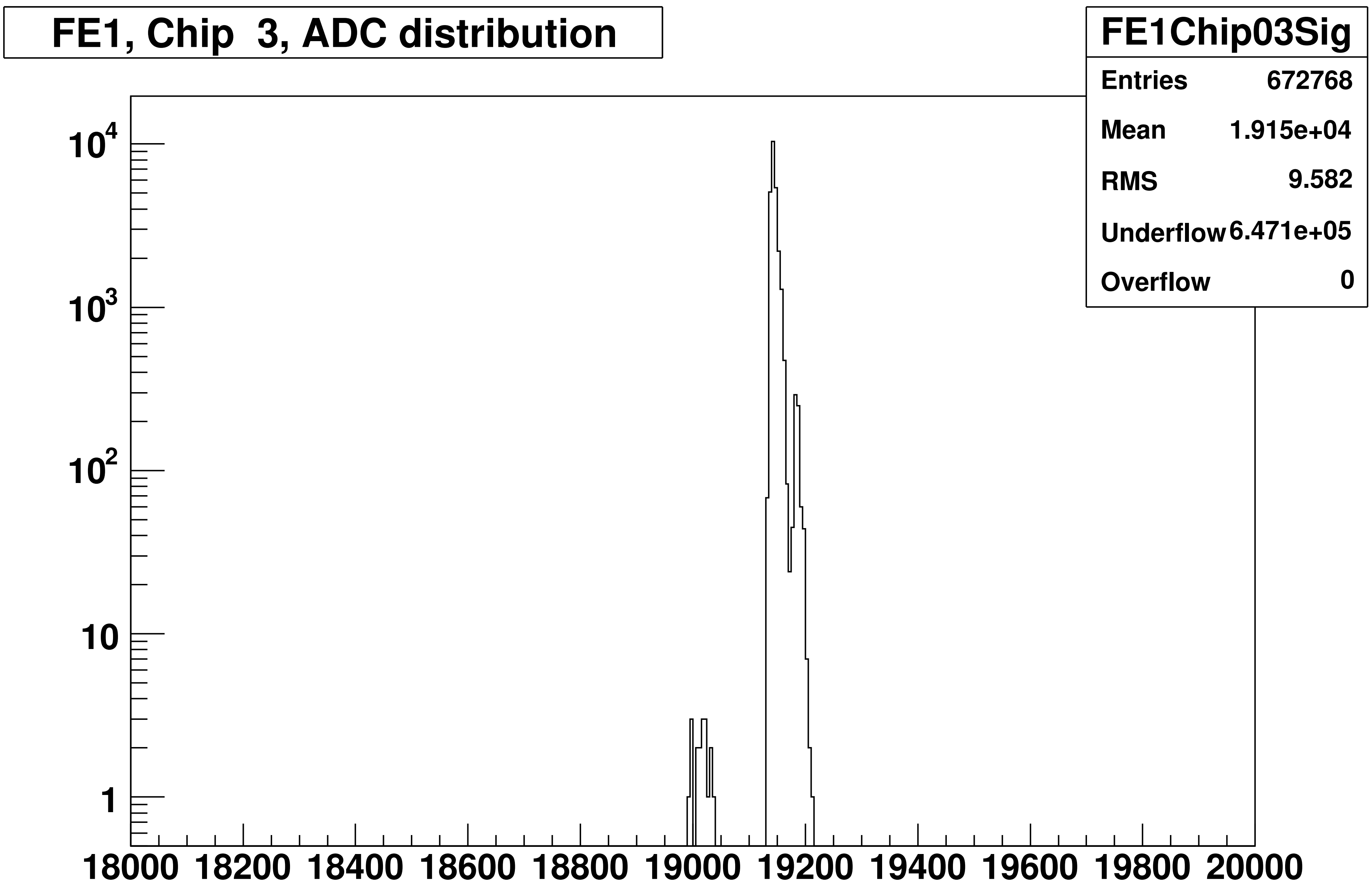
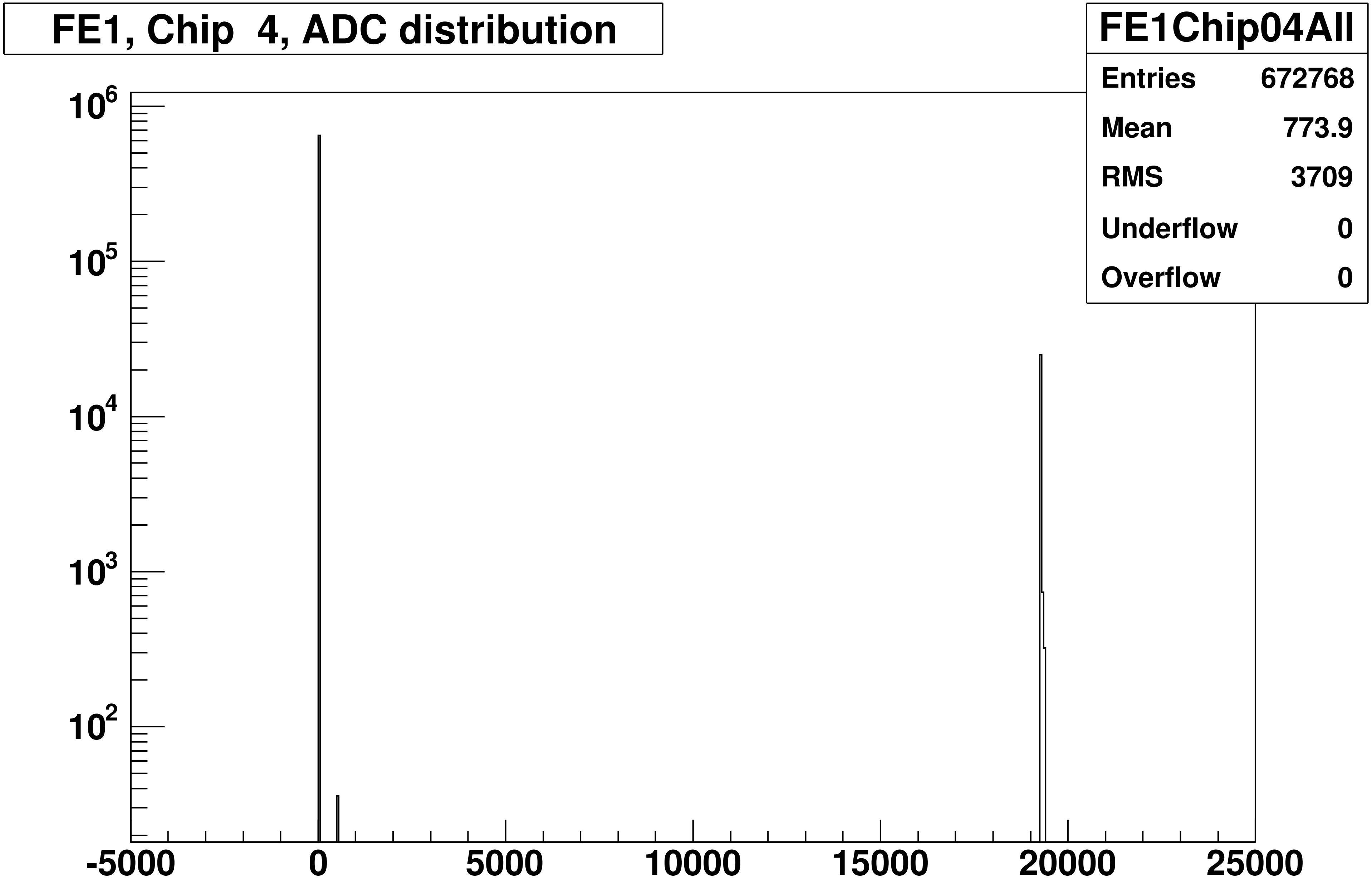


FE1, Chip 3, ADC distribution
FE1Chip03Sig
Entries 672768
Mean 1.915e+04
RMS 9.582
Underflow 6.471e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE1, Chip 4, ADC distribution
FE1Chip04All
Entries 672768
Mean 773.9
RMS 3709
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
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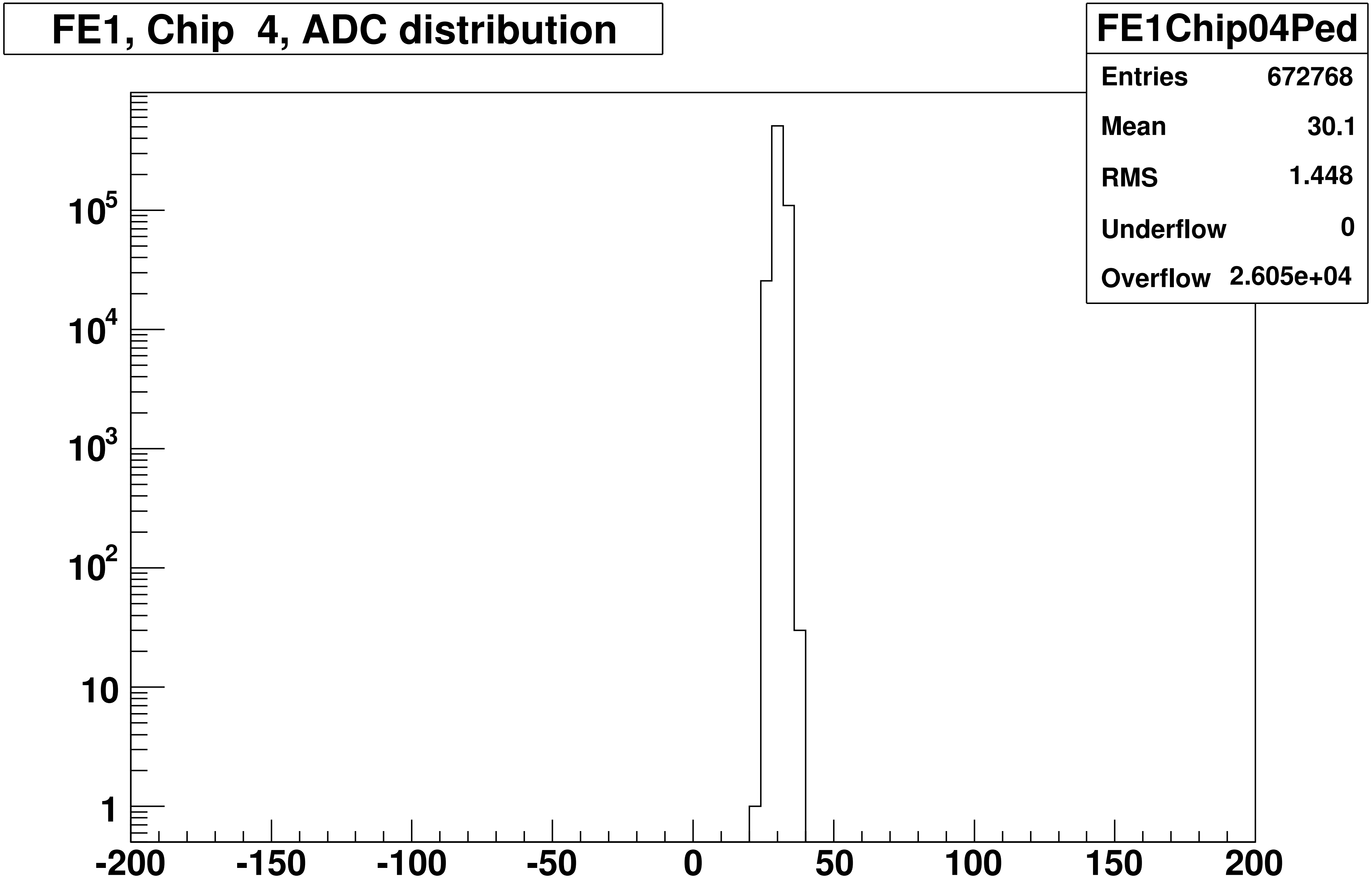

FE1, Chip 4, ADC distribution
FE1Chip04Ped
Entries 672768
Mean 30.1
RMS 1.448
Underflow 0
Overflow 2.605e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
-50
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50
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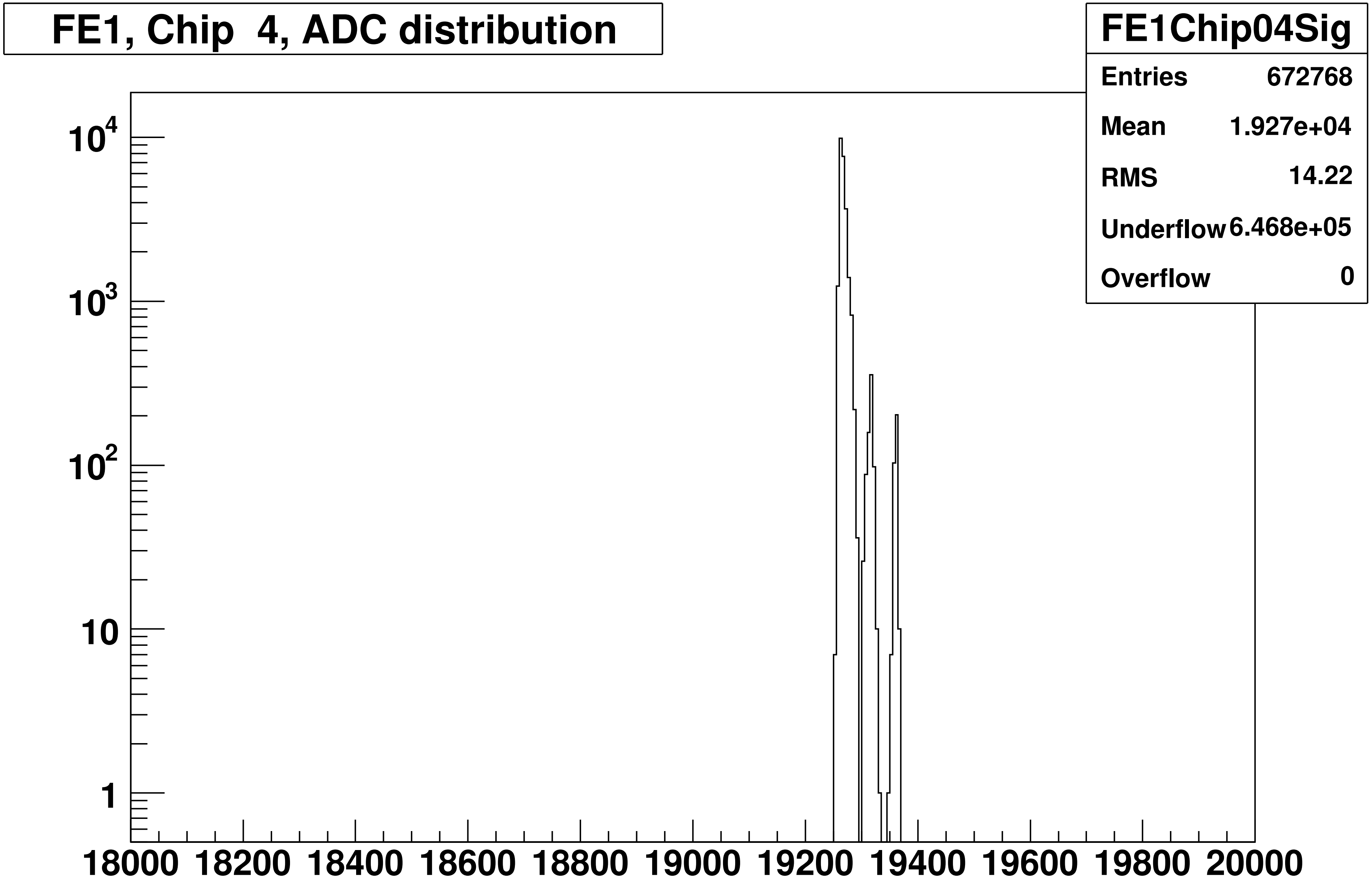
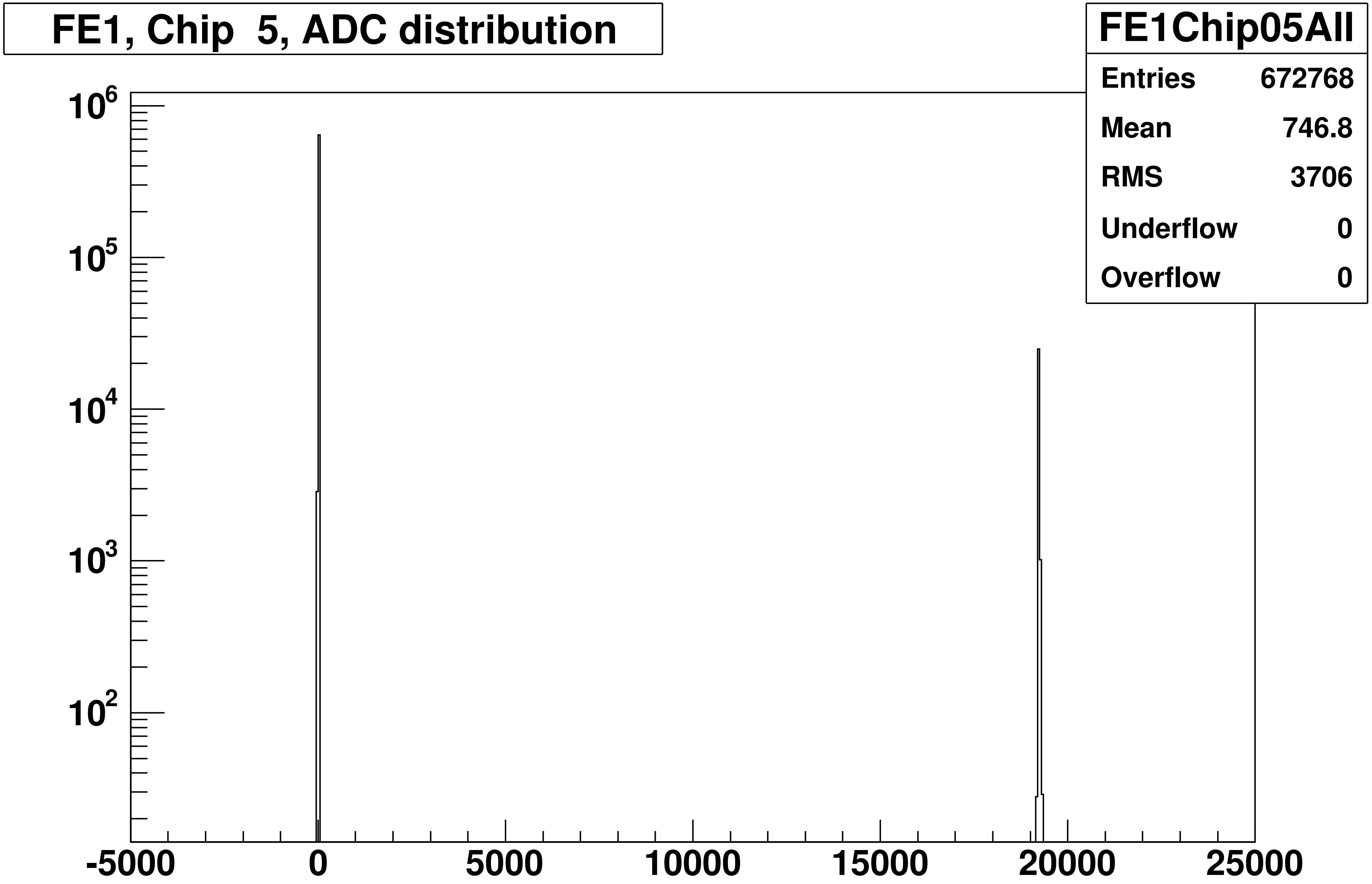
150
200



FE1, Chip 4, ADC distribution
FE1Chip04Sig
Entries 672768
Mean 1.927e+04
RMS 14.22
Underflow 6.468e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE1, Chip 5, ADC distribution
FE1Chip05All
Entries 672768
Mean 746.8
RMS 3706
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
-5000
0
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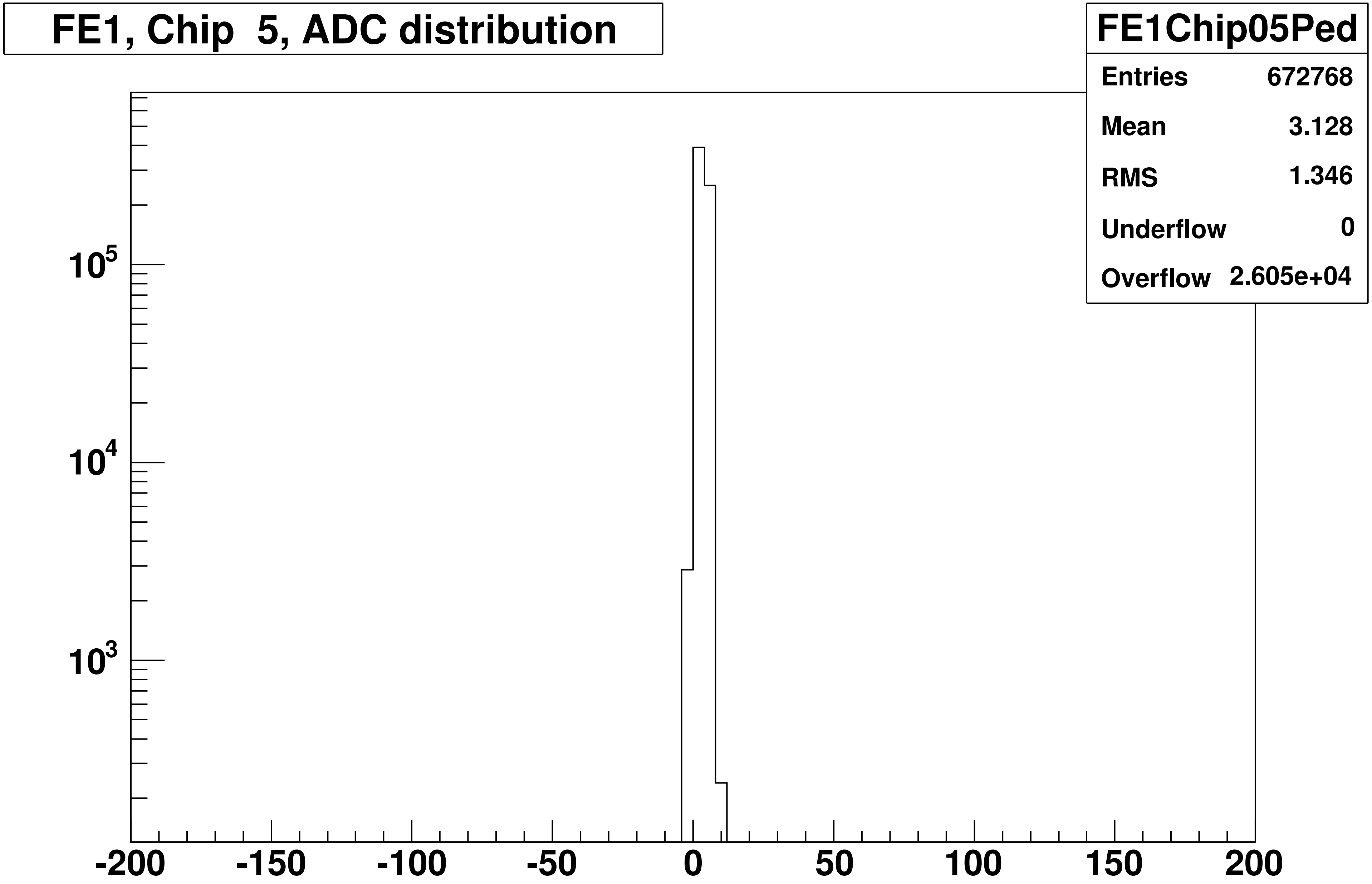
10000
15000
20000
25000



FE1, Chip 5, ADC distribution
FE1Chip05Ped
Entries 672768
Mean 3.128
RMS 1.346
Underflow 0
Overflow 2.605e+04
10^5
10^4
10^3
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-150
-100
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0
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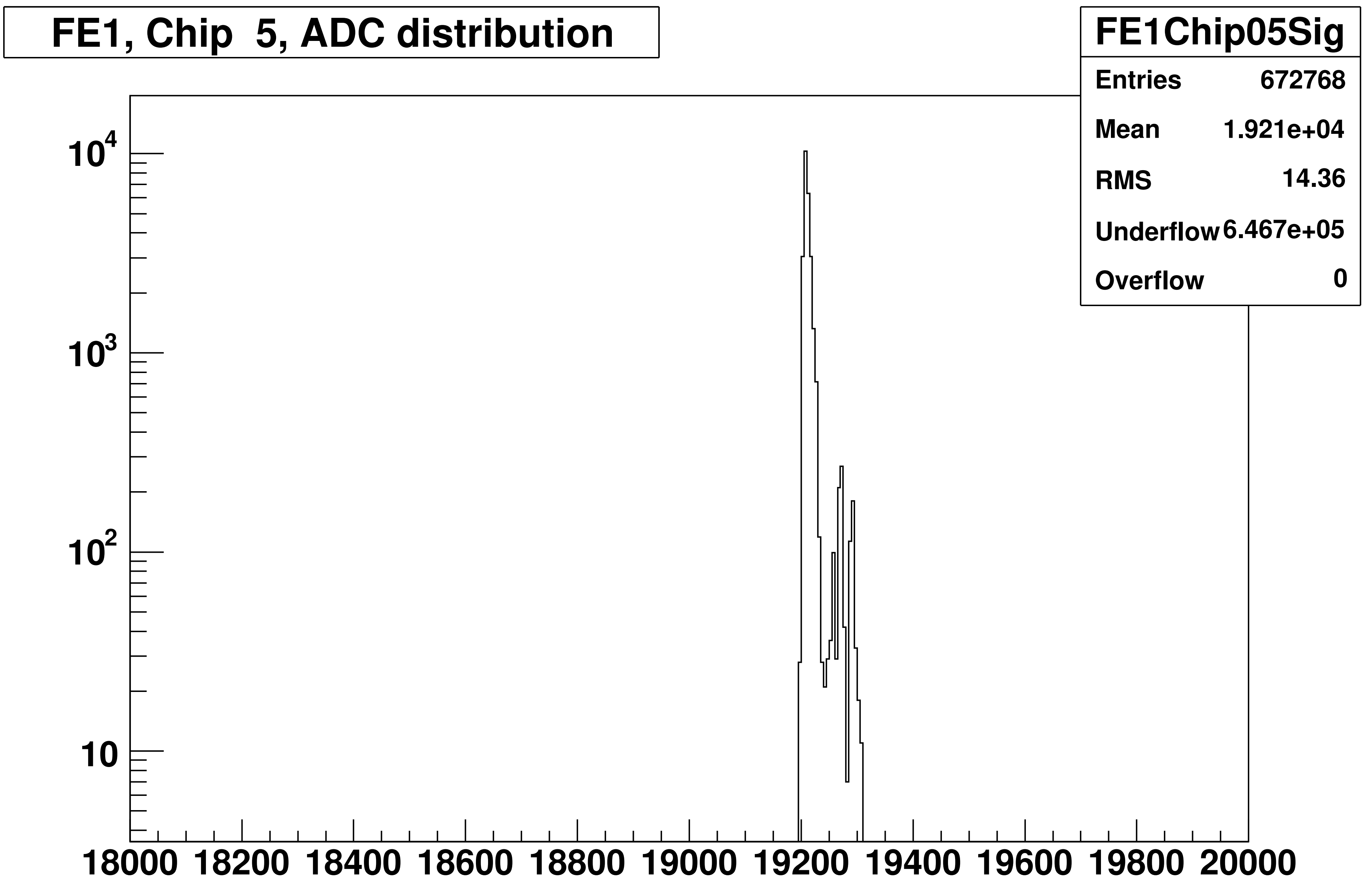
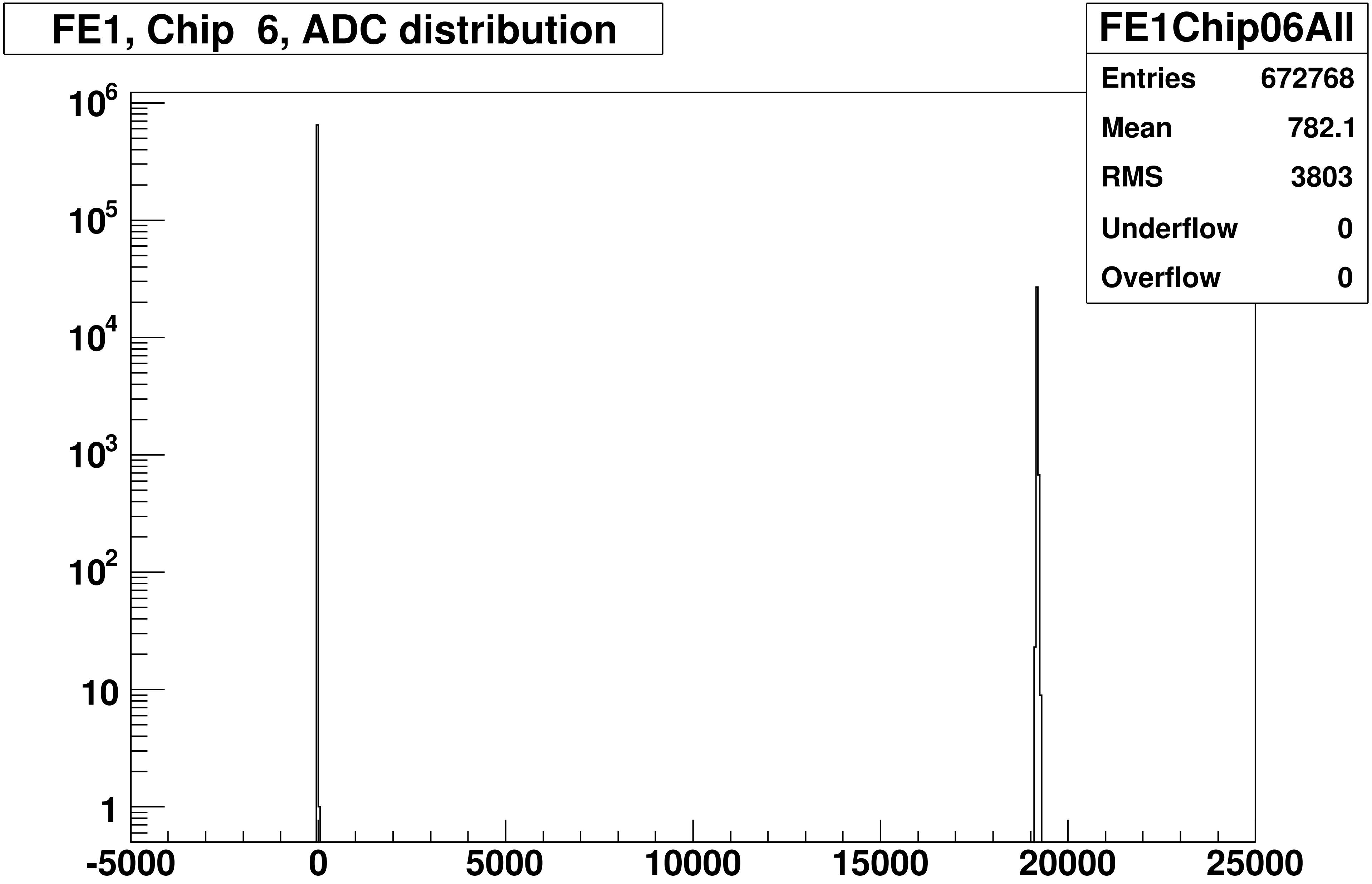
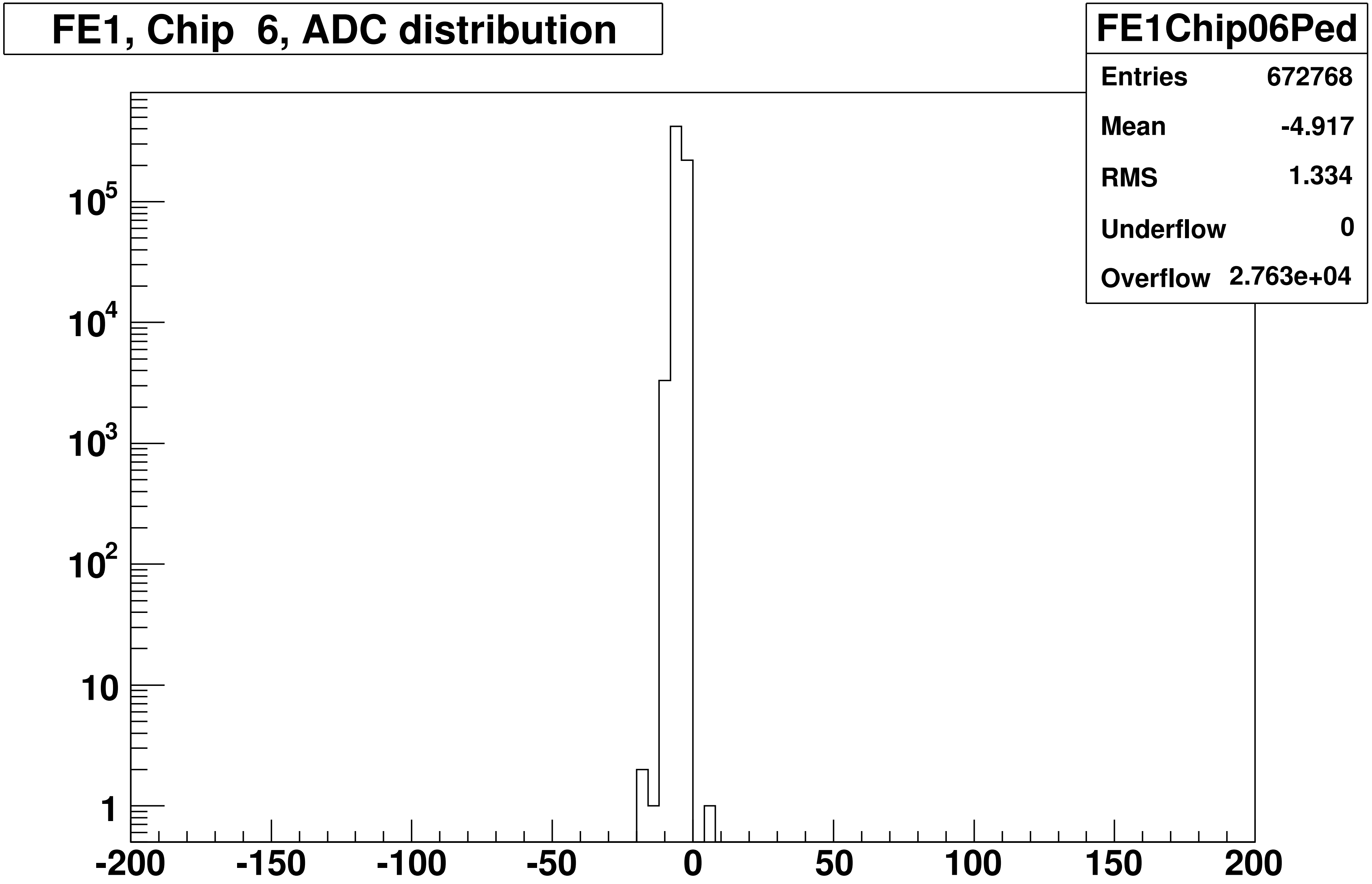
100
150
200



FE1, Chip 5, ADC distribution
FE1Chip05Sig
Entries 672768
Mean 1.921e+04
RMS 14.36
Underflow 6.467e+05
Overflow 0
10^4
10^3
10^2
10
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000



FE1, Chip 6, ADC distribution
FE1Chip06All
Entries 672768
Mean 782.1
RMS 3803
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE1, Chip 6, ADC distribution
FE1Chip06Ped
Entries 672768
Mean -4.917
RMS 1.334
Underflow 0
Overflow 2.763e+04
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10^4
10^3
10^2
10
1
-200
-150
-100
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0
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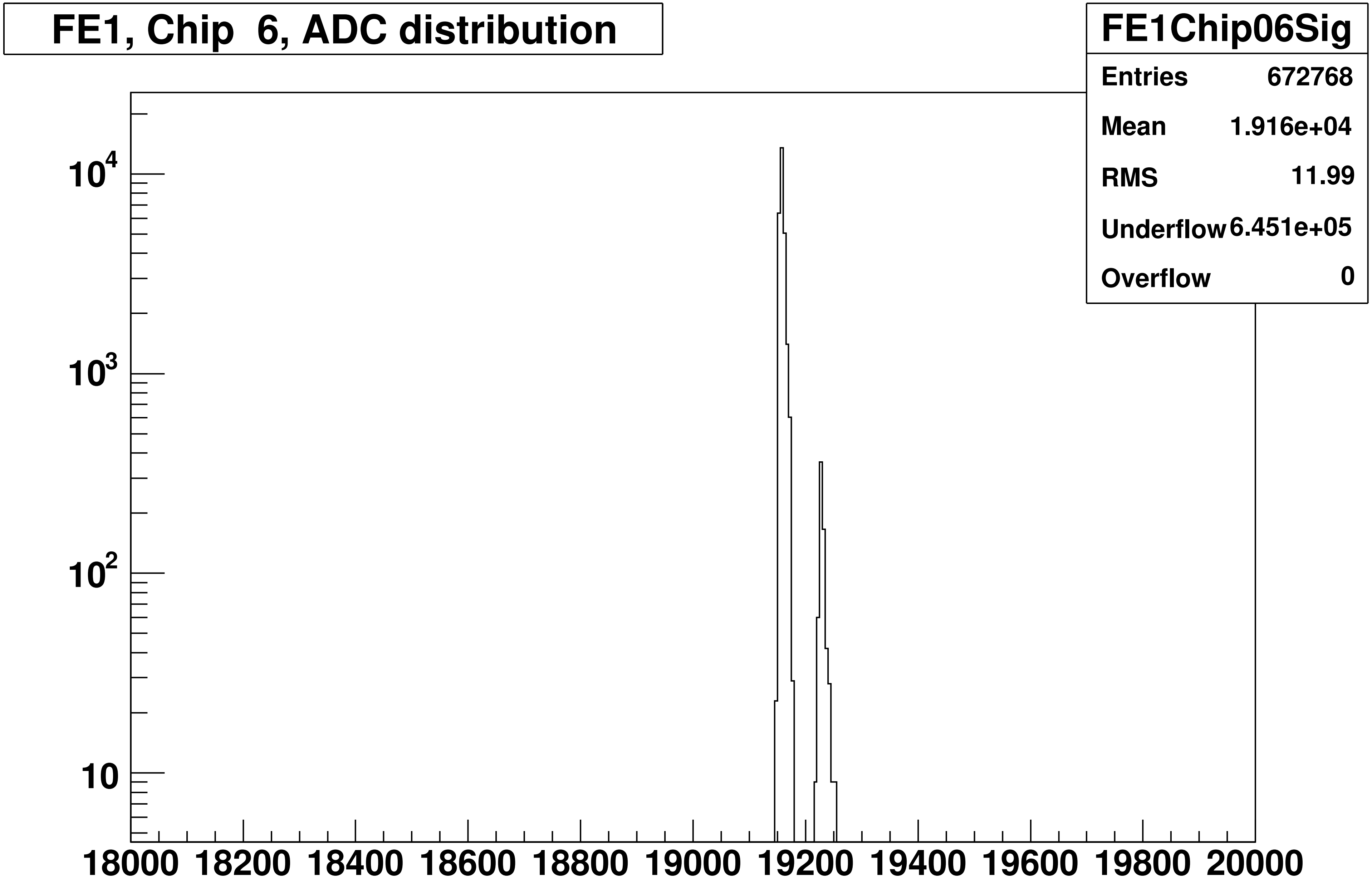
100
150
200



FE1, Chip 6, ADC distribution
FE1Chip06Sig
Entries 672768
Mean 1.916e+04
RMS 11.99
Underflow 6.451e+05
Overflow 0
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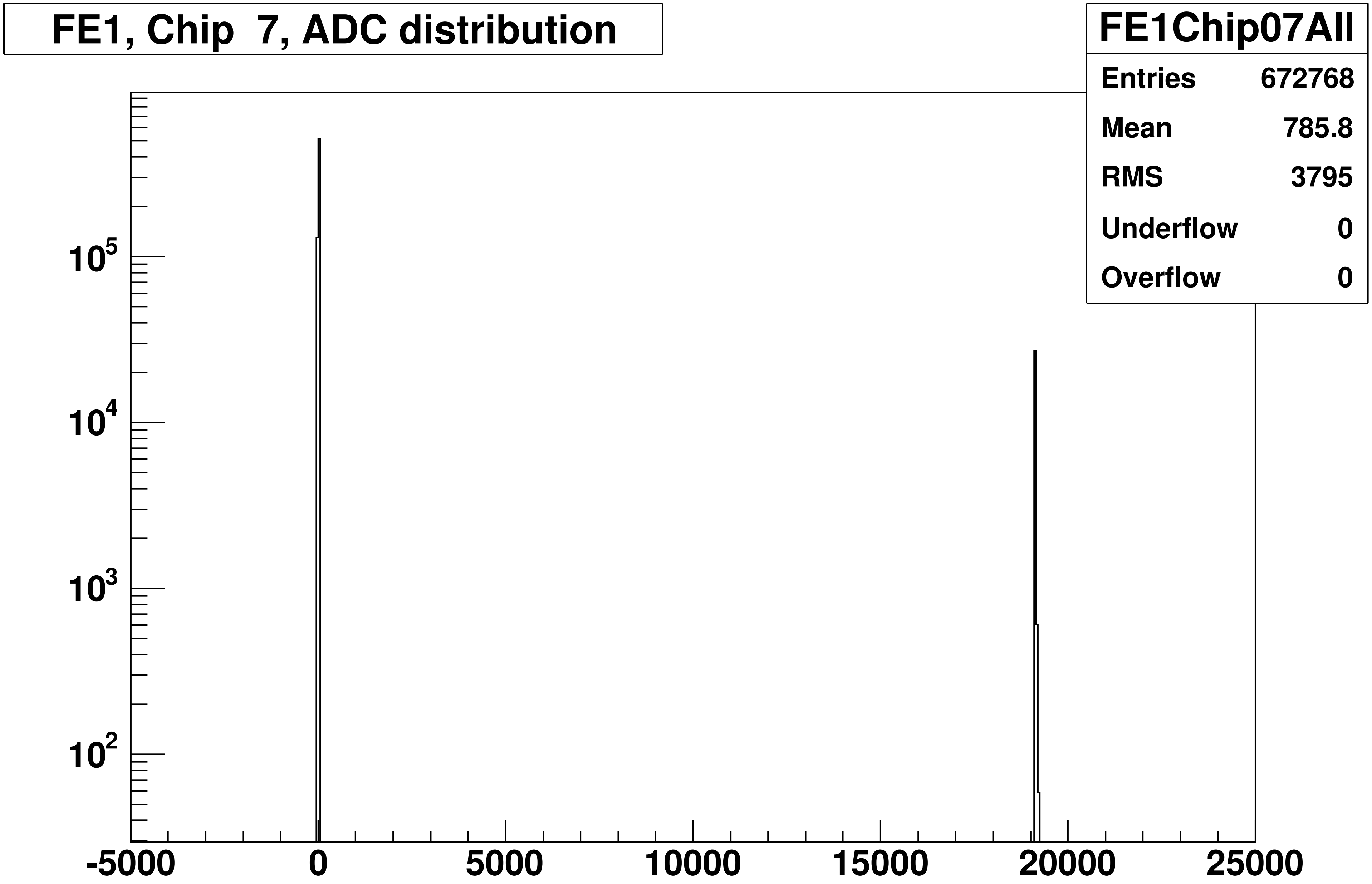
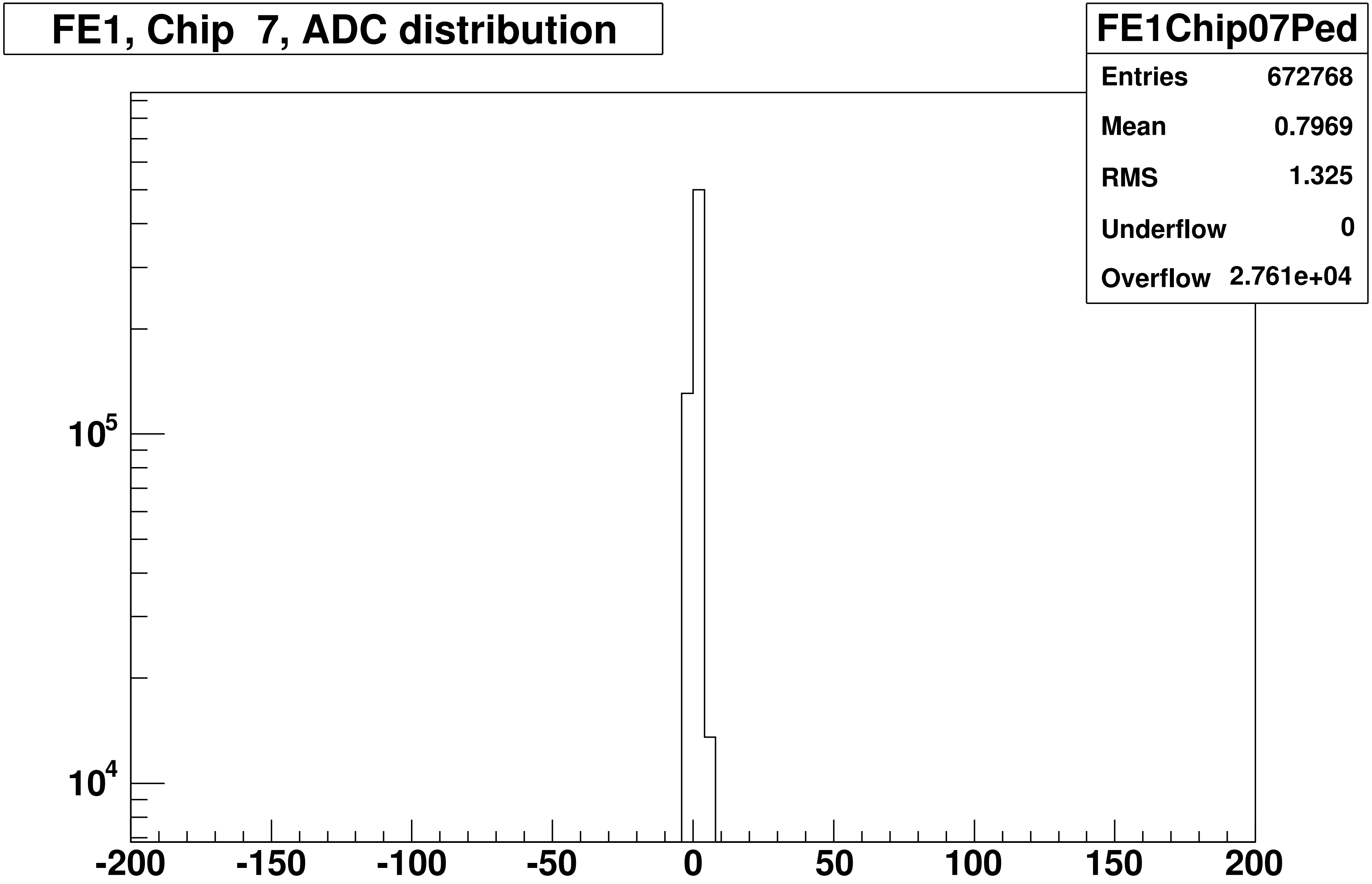
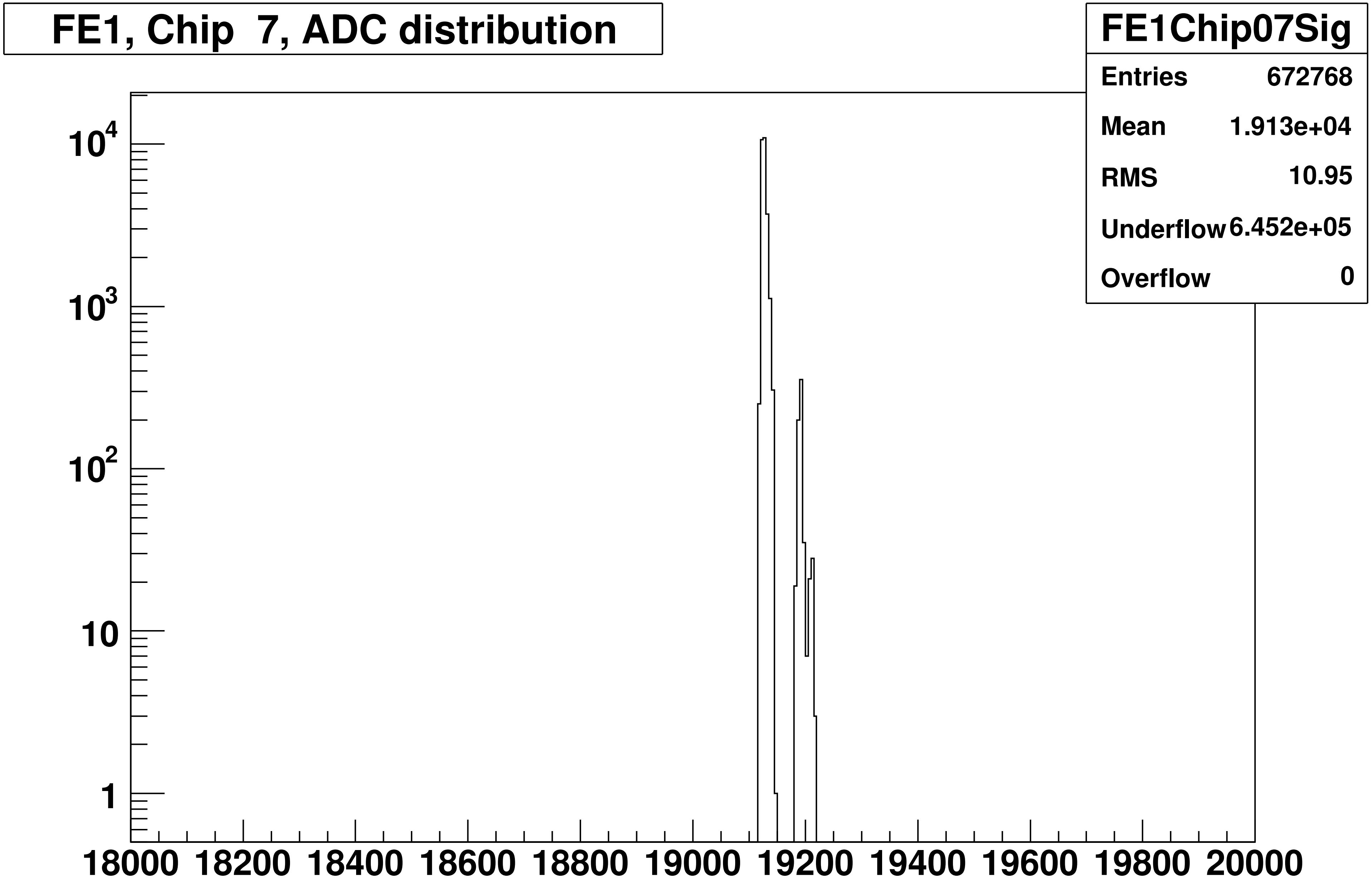
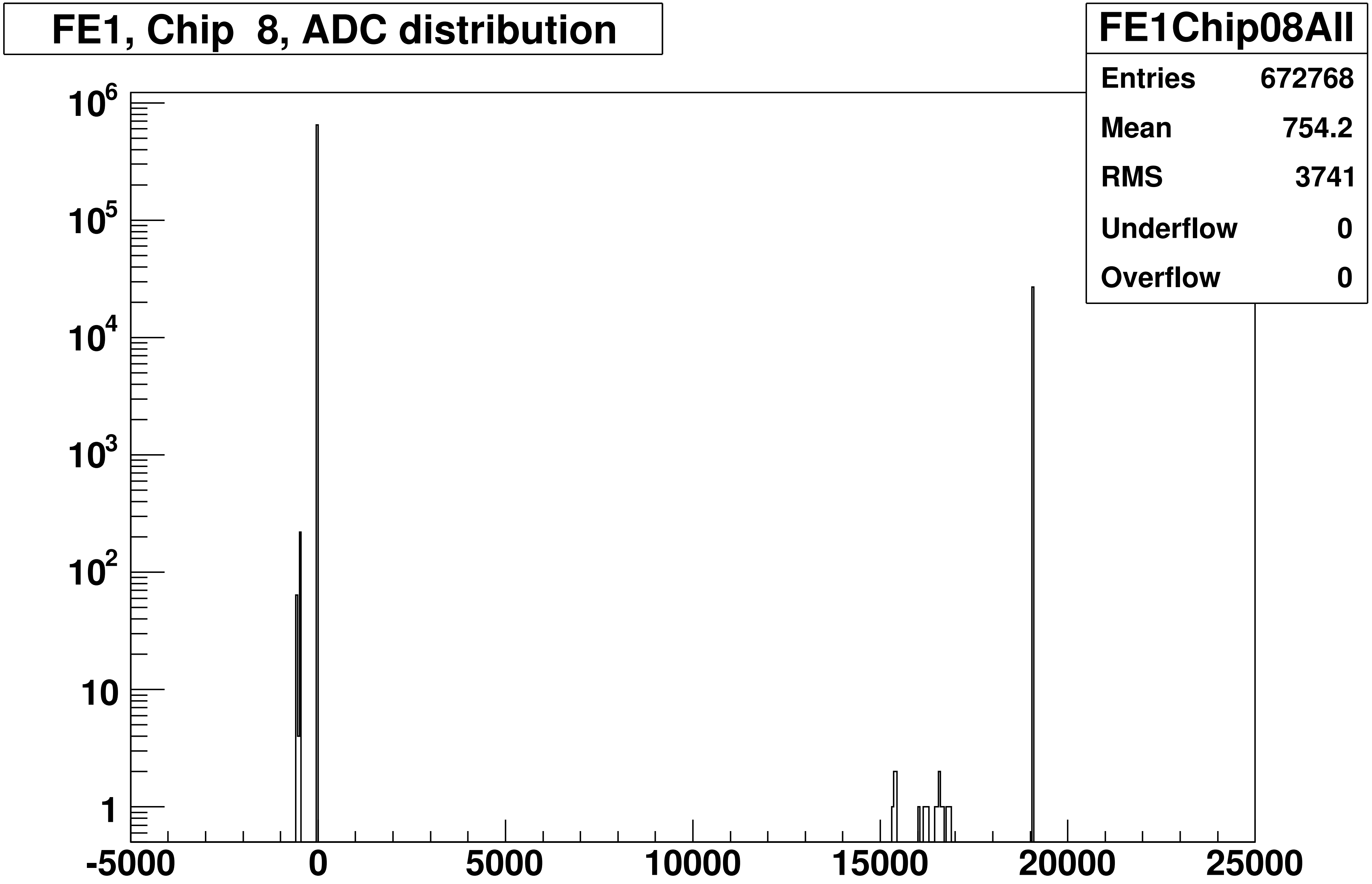
10^3
10^2
10
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000


FE1, Chip 7, ADC distribution
FE1Chip07All
Entries 672768
Mean 785.8
RMS 3795
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000


FE1, Chip 7, ADC distribution
FE1Chip07Ped
Entries 672768
Mean 0.7969
RMS 1.325
Underflow 0
Overflow 2.761e+04
10^5
10^4
-200
-150
-100
-50
0
50
100
150
200



FE1, Chip 7, ADC distribution
FE1Chip07Sig
Entries 672768
Mean 1.913e+04
RMS 10.95
Underflow 6.452e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE1, Chip 8, ADC distribution
FE1Chip08All
Entries 672768
Mean 754.2
RMS 3741
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
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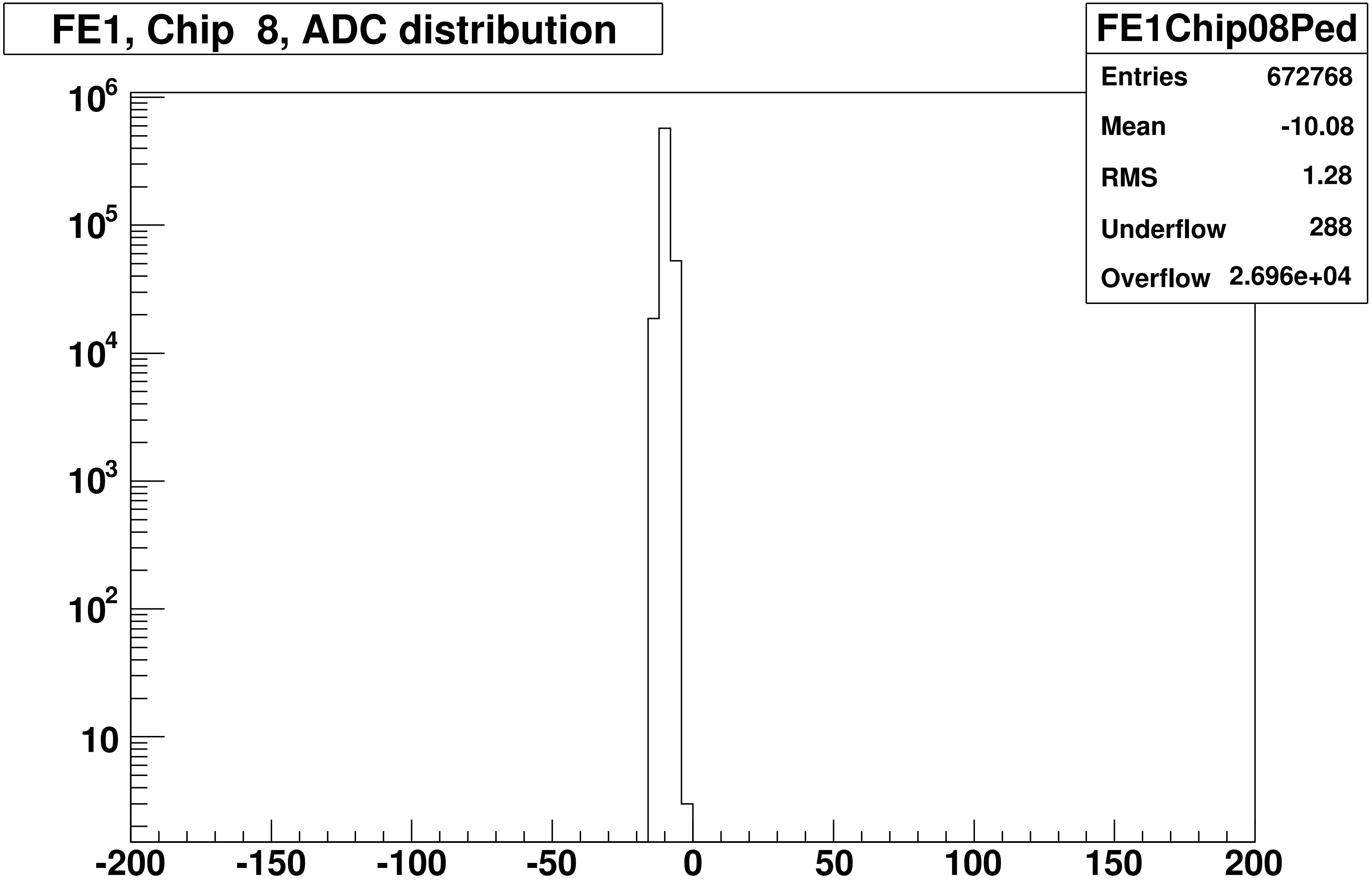
10000
15000
20000
25000


FE1, Chip 8, ADC distribution
FE1Chip08Ped
Entries 672768
Mean -10.08
RMS 1.28
Underflow 288
Overflow 2.696e+04
10^6
10^5
10^4
10^3
10^2
10
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-100
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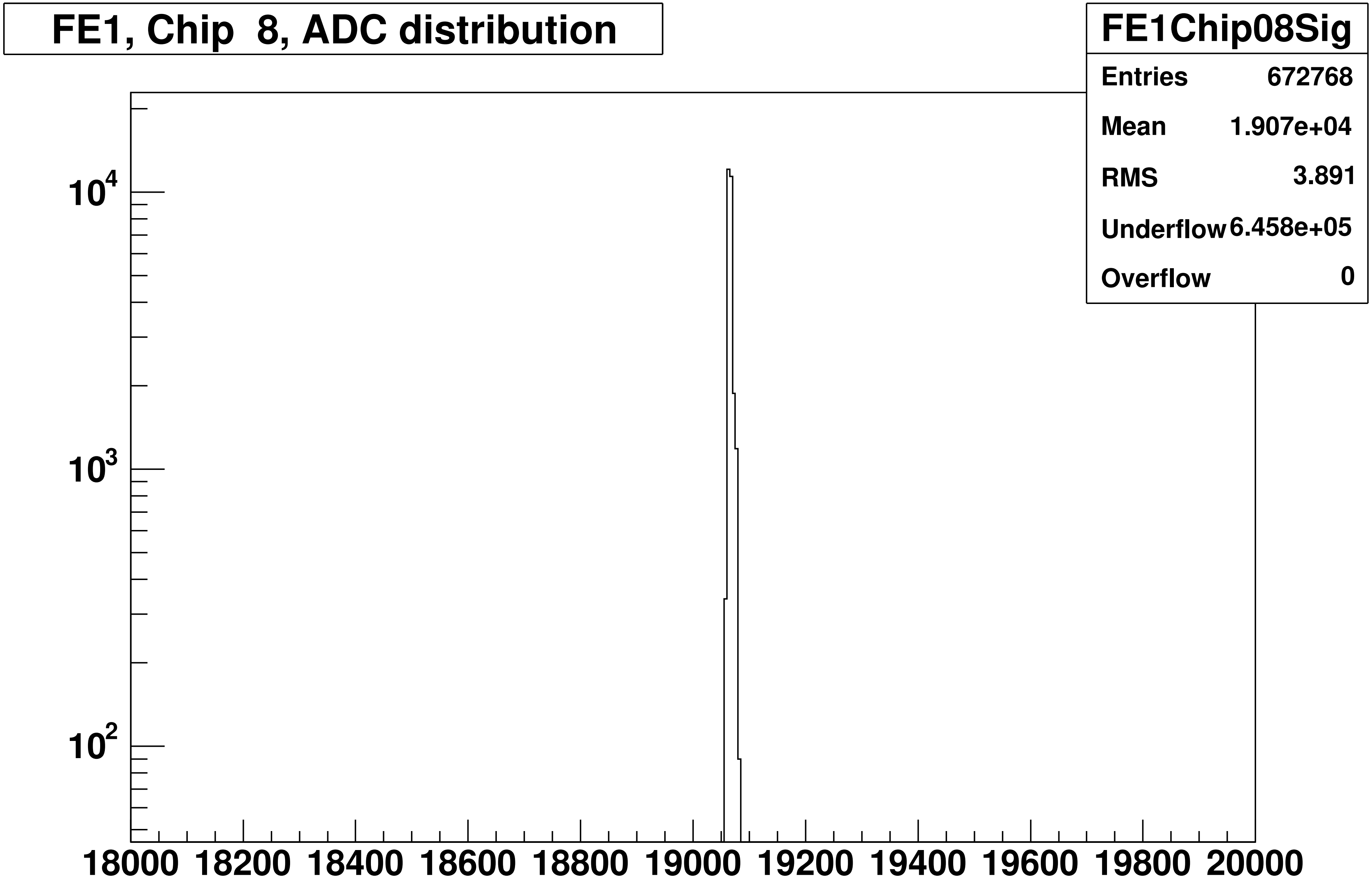
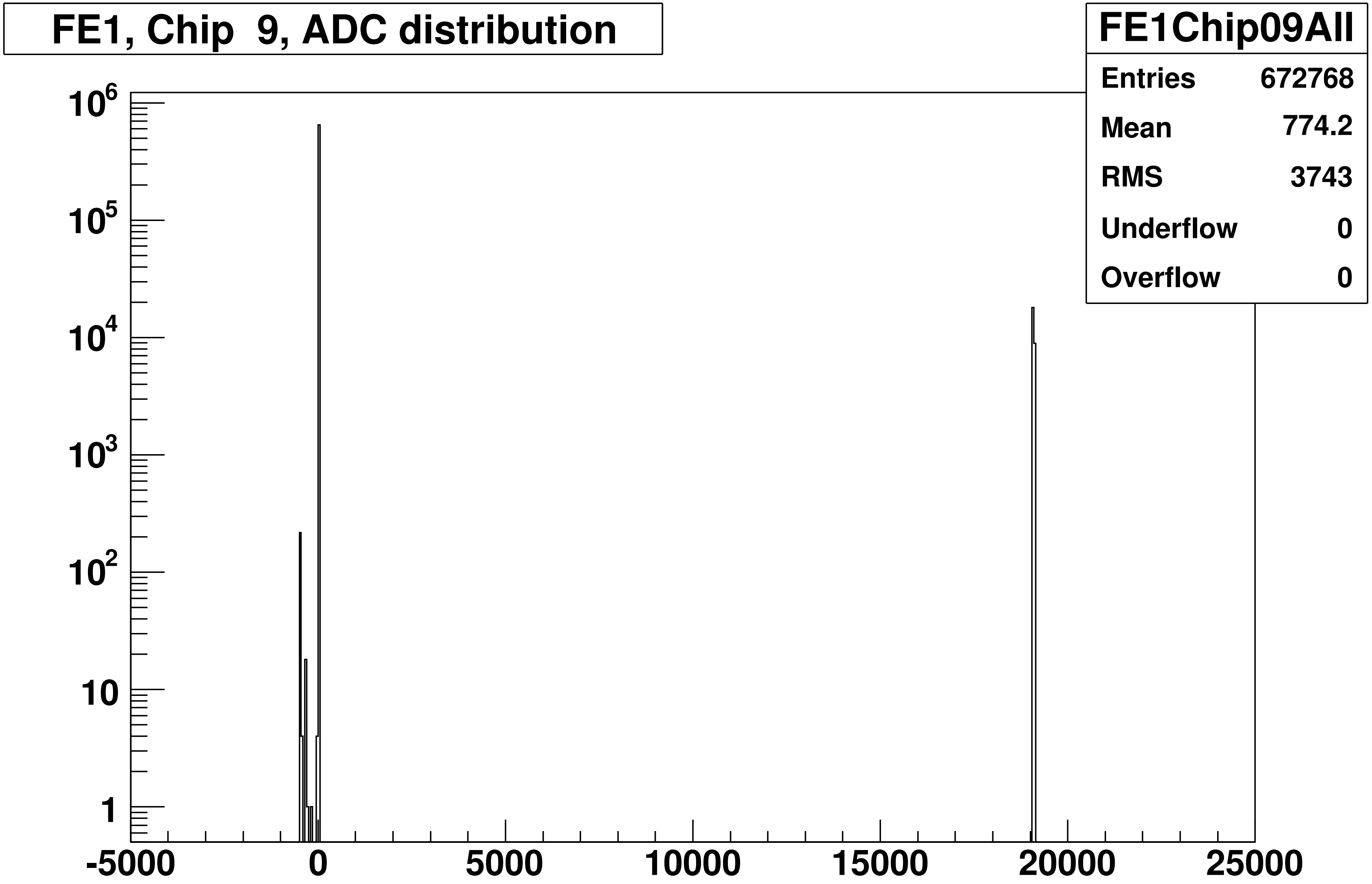
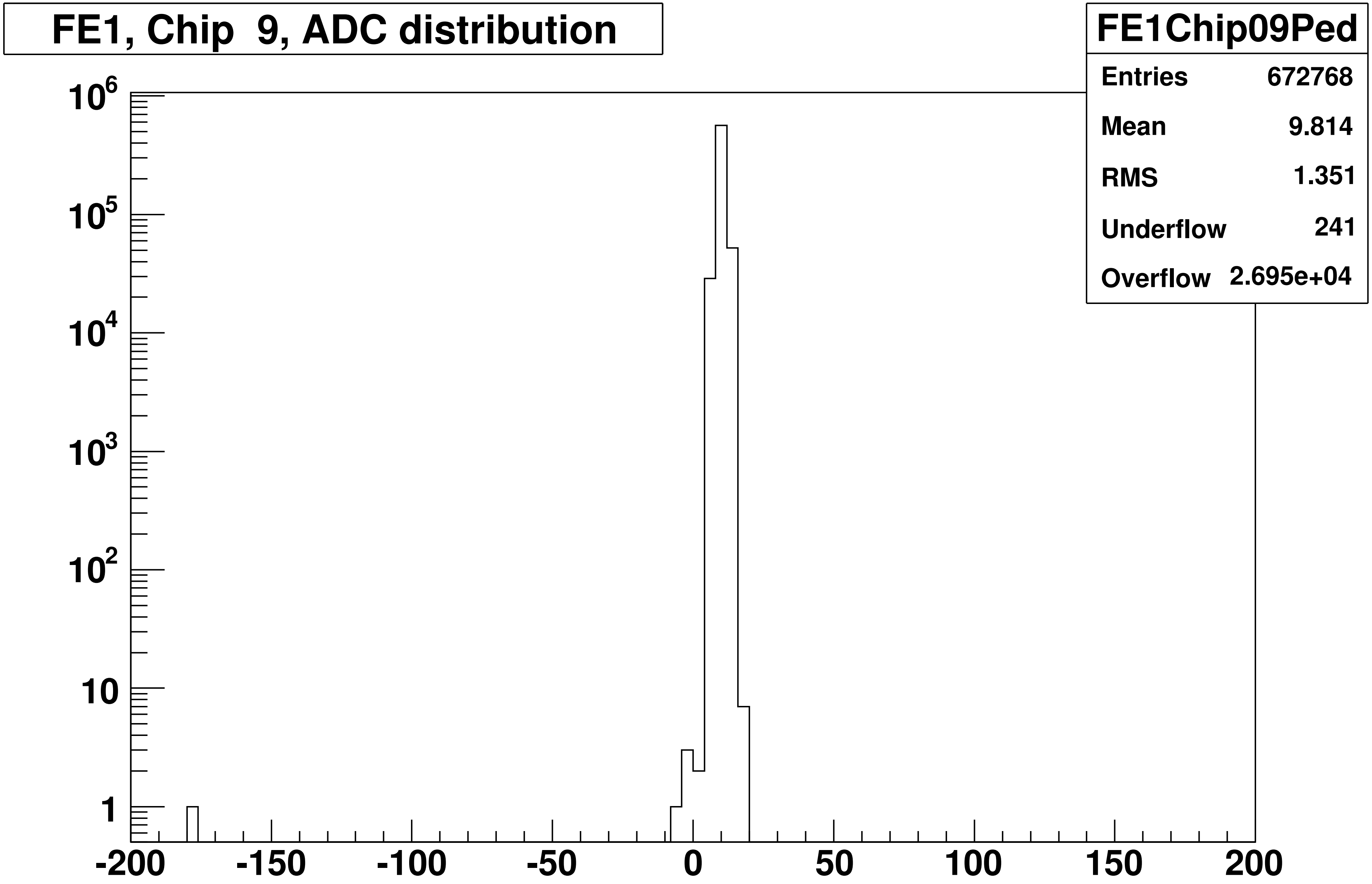
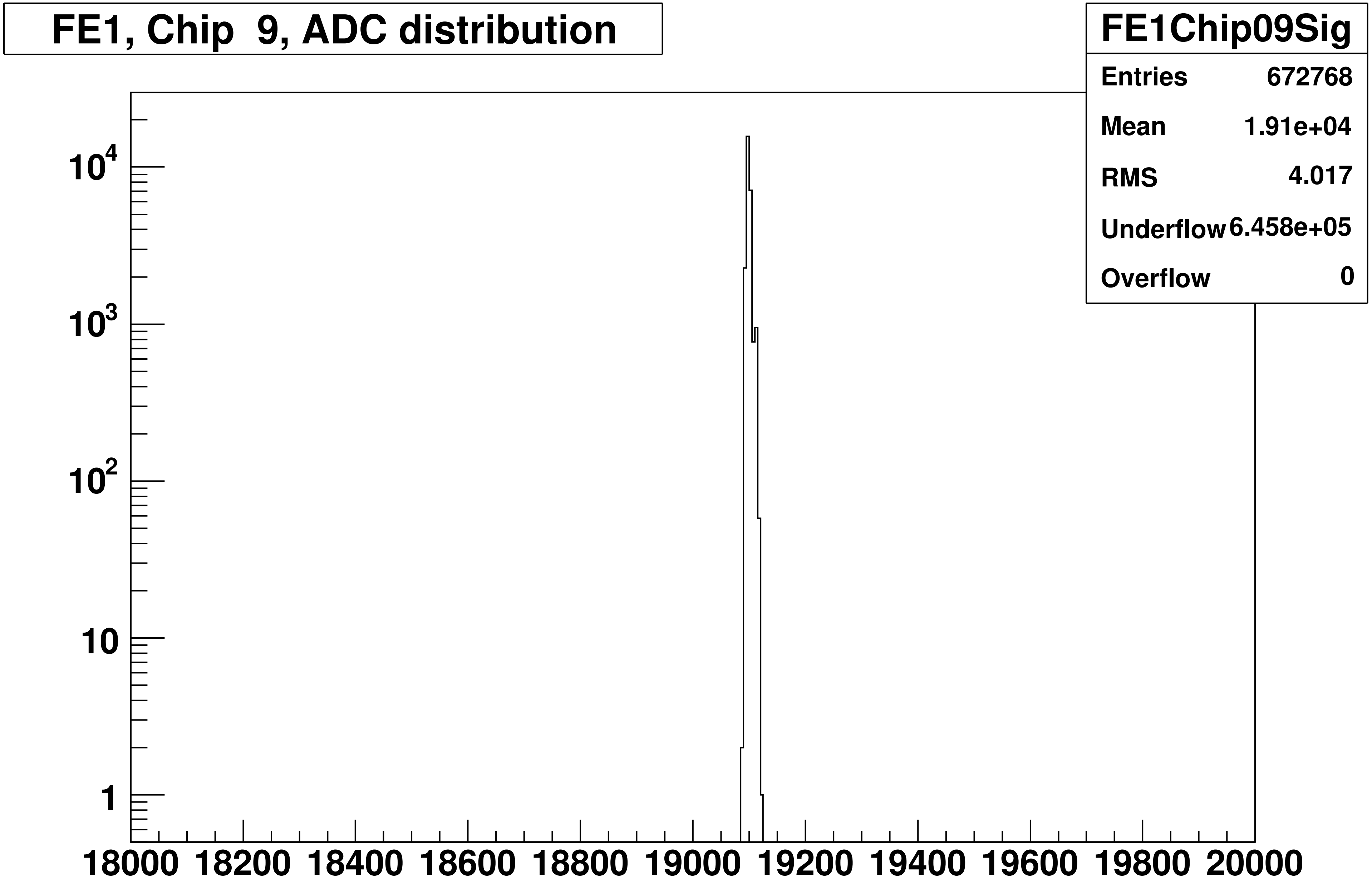
100
150
200


FE1, Chip 8, ADC distribution
FE1Chip08Sig
Entries 672768
Mean 1.907e+04
RMS 3.891
Underflow 6.458e+05
Overflow 0
10^4
10^3
10^2
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE1, Chip 9, ADC distribution
FE1Chip09All
Entries 672768
Mean 774.2
RMS 3743
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE1, Chip 9, ADC distribution
FE1Chip09Ped
Entries 672768
Mean 9.814
RMS 1.351
Underflow 241
Overflow 2.695e+04
10^6
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
200


FE1, Chip 9, ADC distribution
FE1Chip09Sig
Entries 672768
Mean 1.91e+04
RMS 4.017
Underflow 6.458e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
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19000
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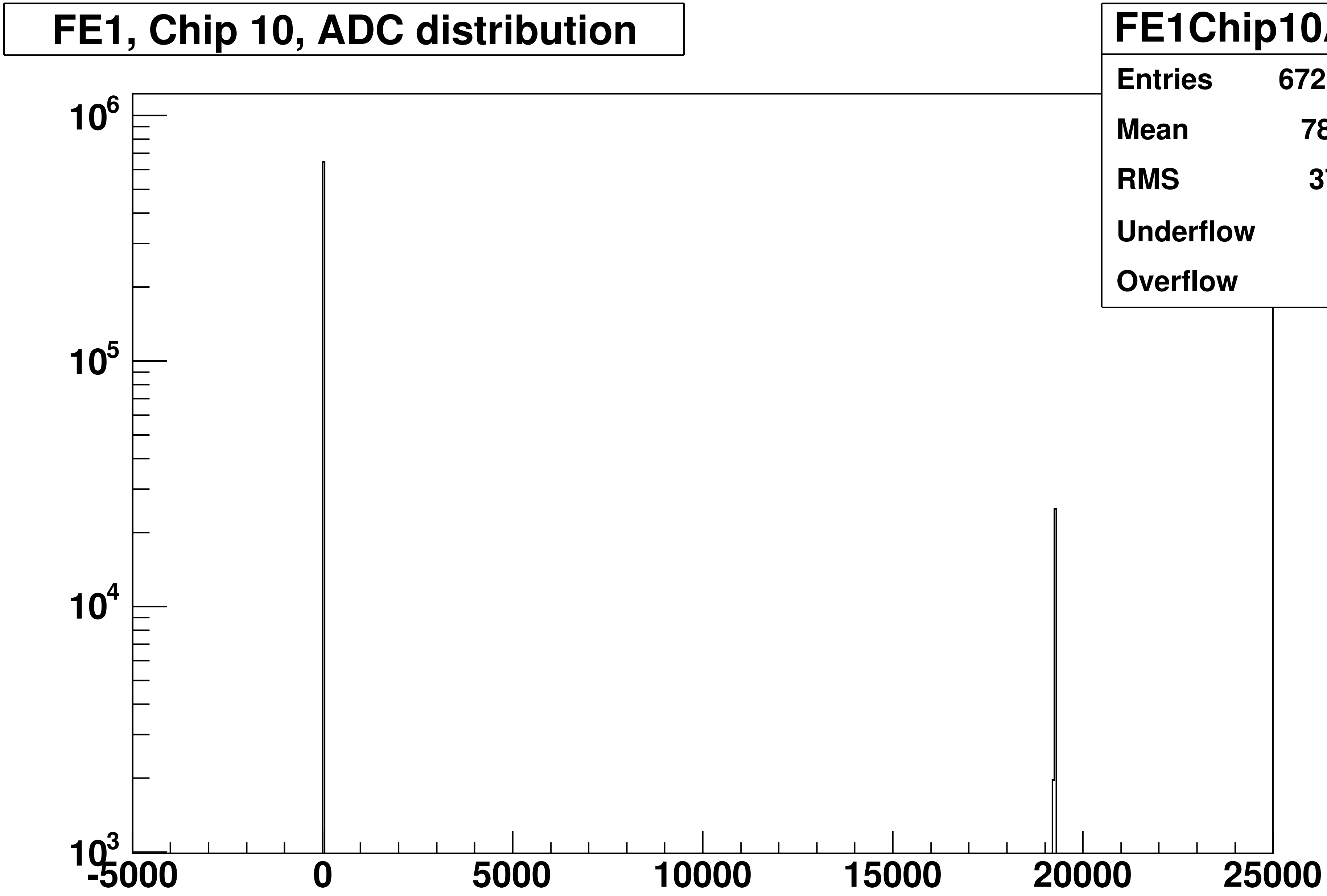
19400
19600
19800
20000


FE1, Chip 10, ADC distribution
FE1Chip10All
Entries 672768
Mean 780.9
RMS 3773
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
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0
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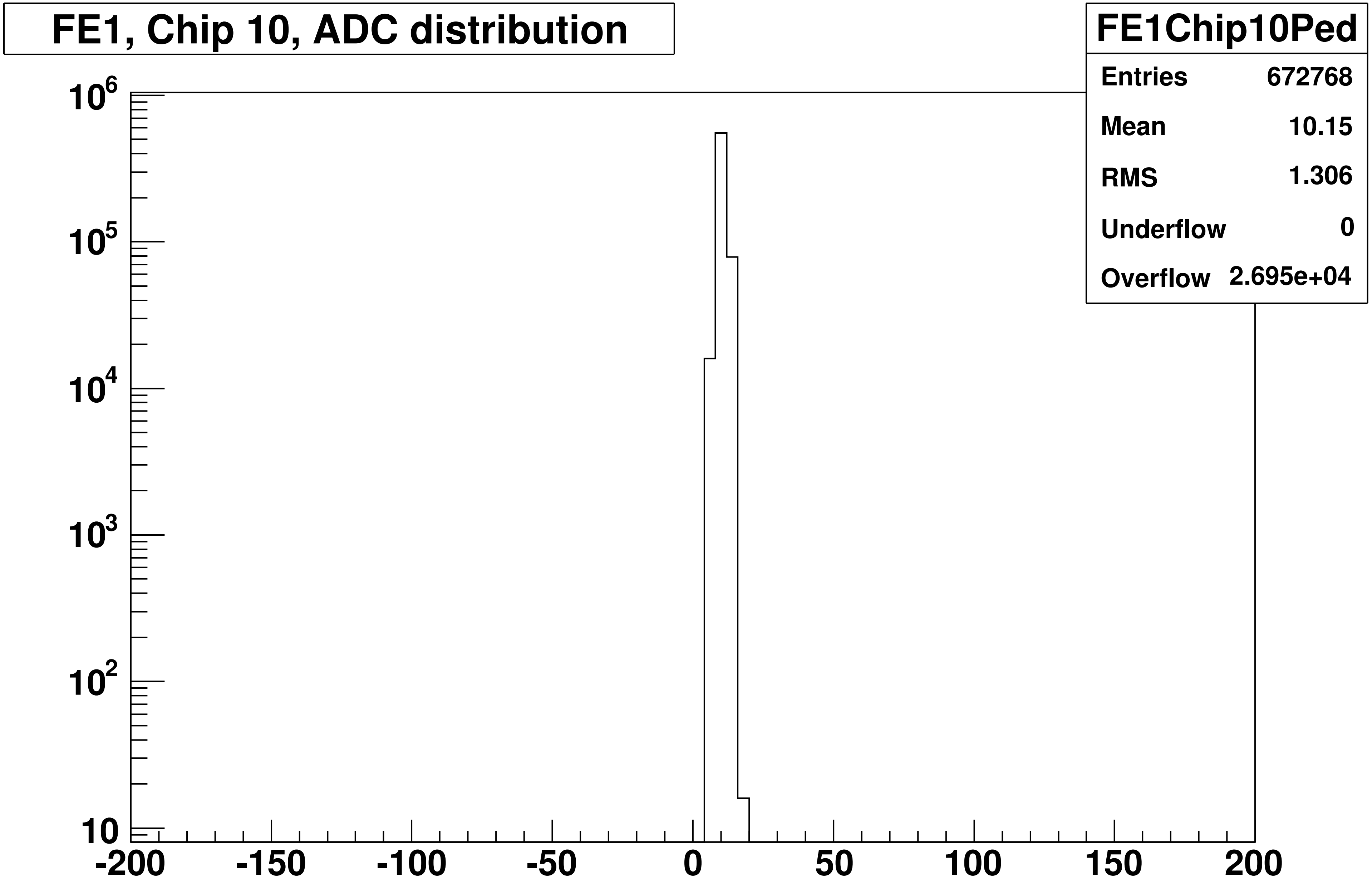
10000
15000
20000
25000



FE1, Chip 10, ADC distribution
FE1Chip10Ped
Entries 672768
Mean 10.15
RMS 1.306
Underflow 0
Overflow 2.695e+04
10^6
10^5
10^4
10^3
10^2
10
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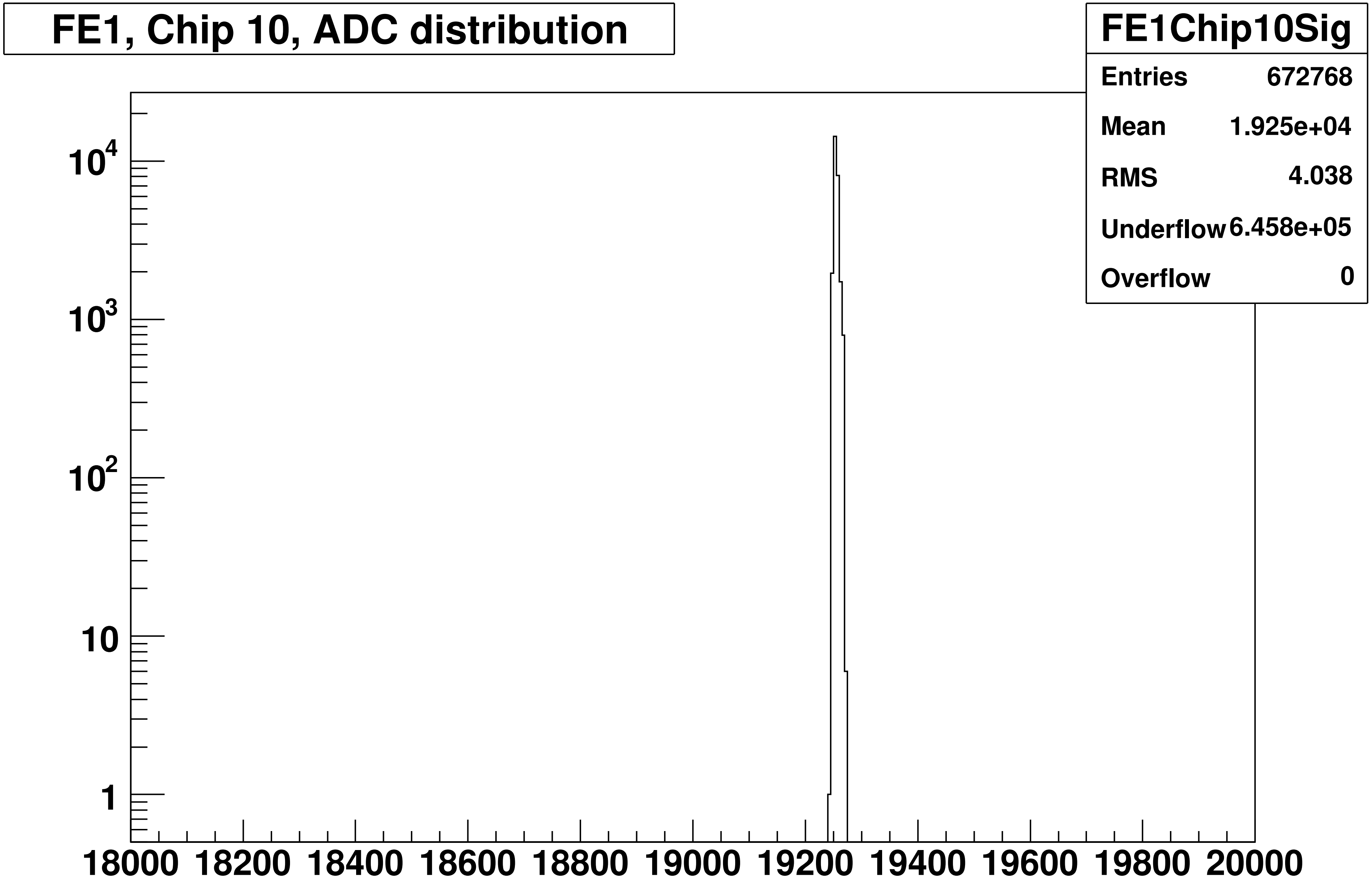
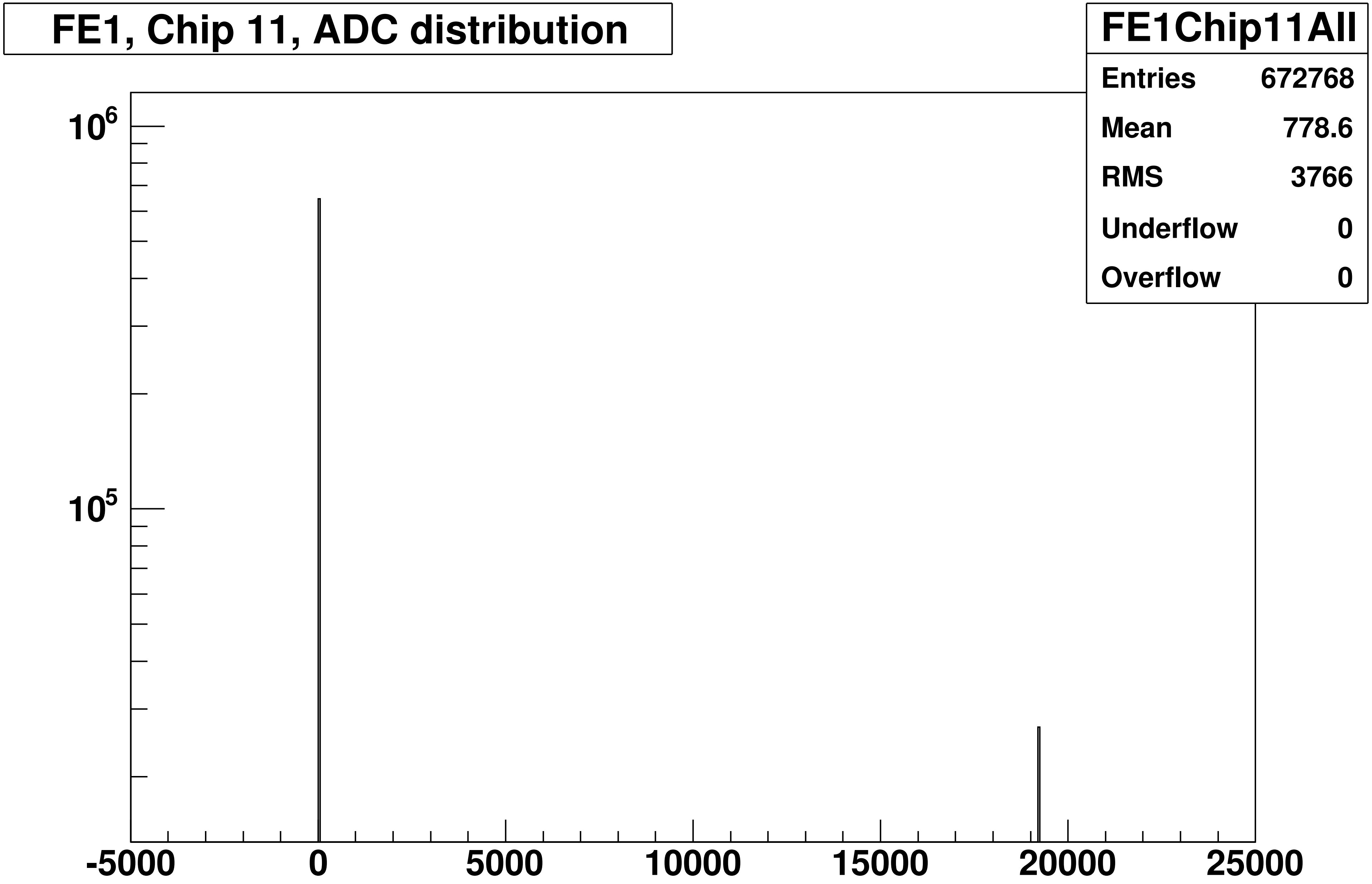
100
150
200


FE1, Chip 10, ADC distribution
FE1Chip10Sig
Entries 672768
Mean 1.925e+04
RMS 4.038
Underflow 6.458e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE1, Chip 11, ADC distribution
FE1Chip11All
Entries 672768
Mean 778.6
RMS 3766
Underflow 0
Overflow 0
10^6
10^5
-5000
0
5000
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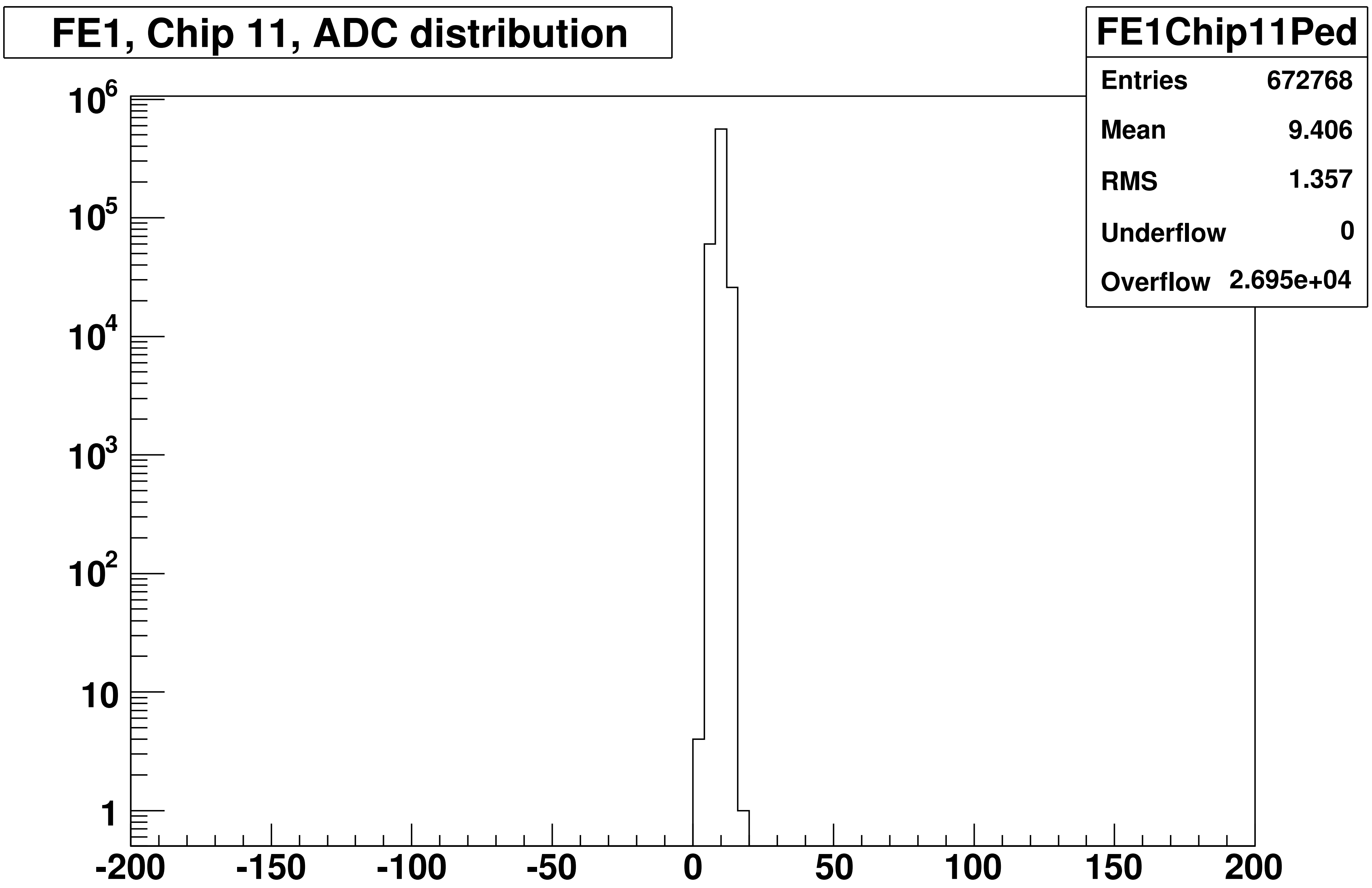
15000
20000
25000


FE1, Chip 11, ADC distribution
FE1Chip11Ped
Entries 672768
Mean 9.406
RMS 1.357
Underflow 0
Overflow 2.695e+04
10^6
10^5
10^4
10^3
10^2
10
1
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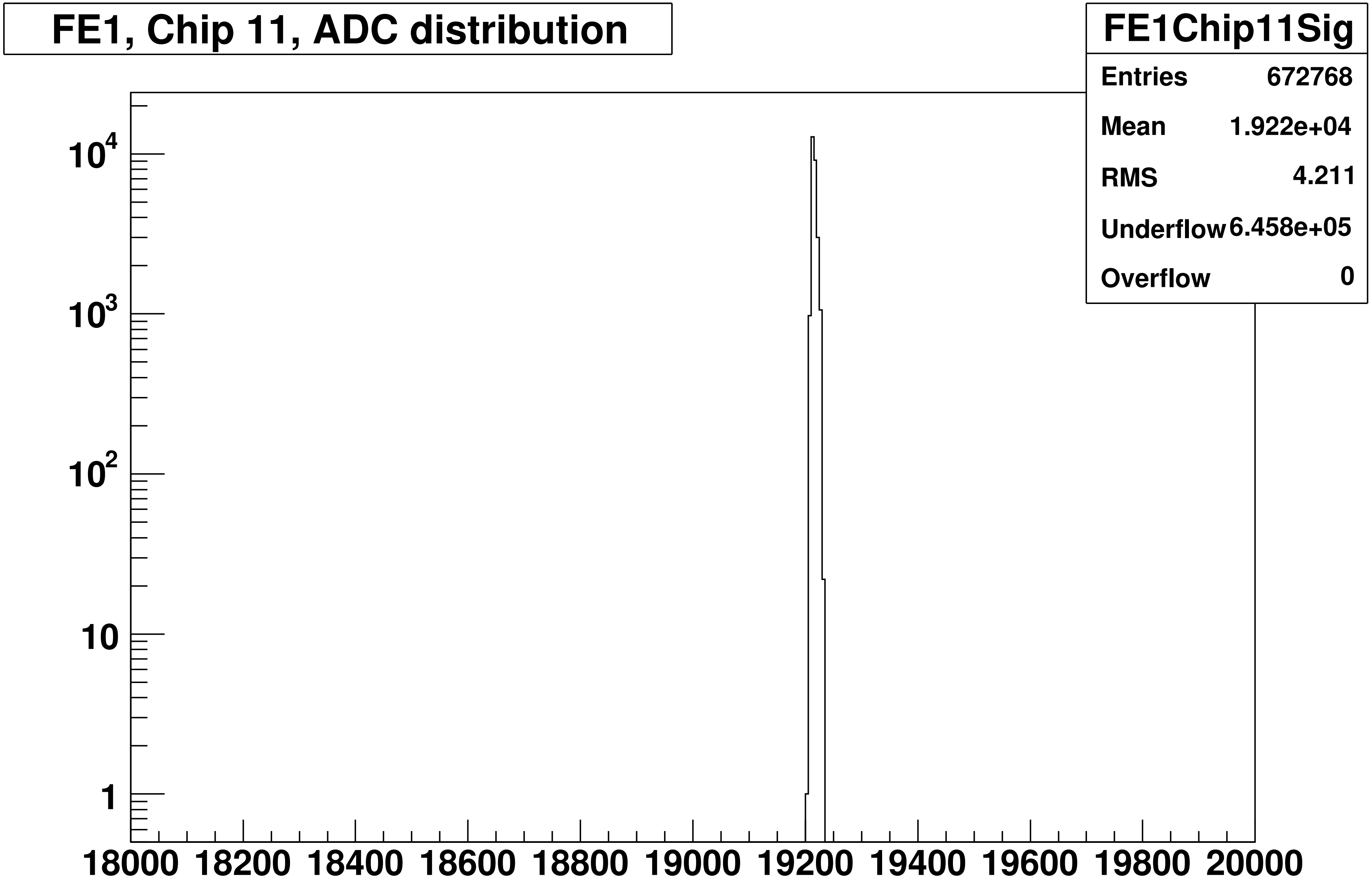
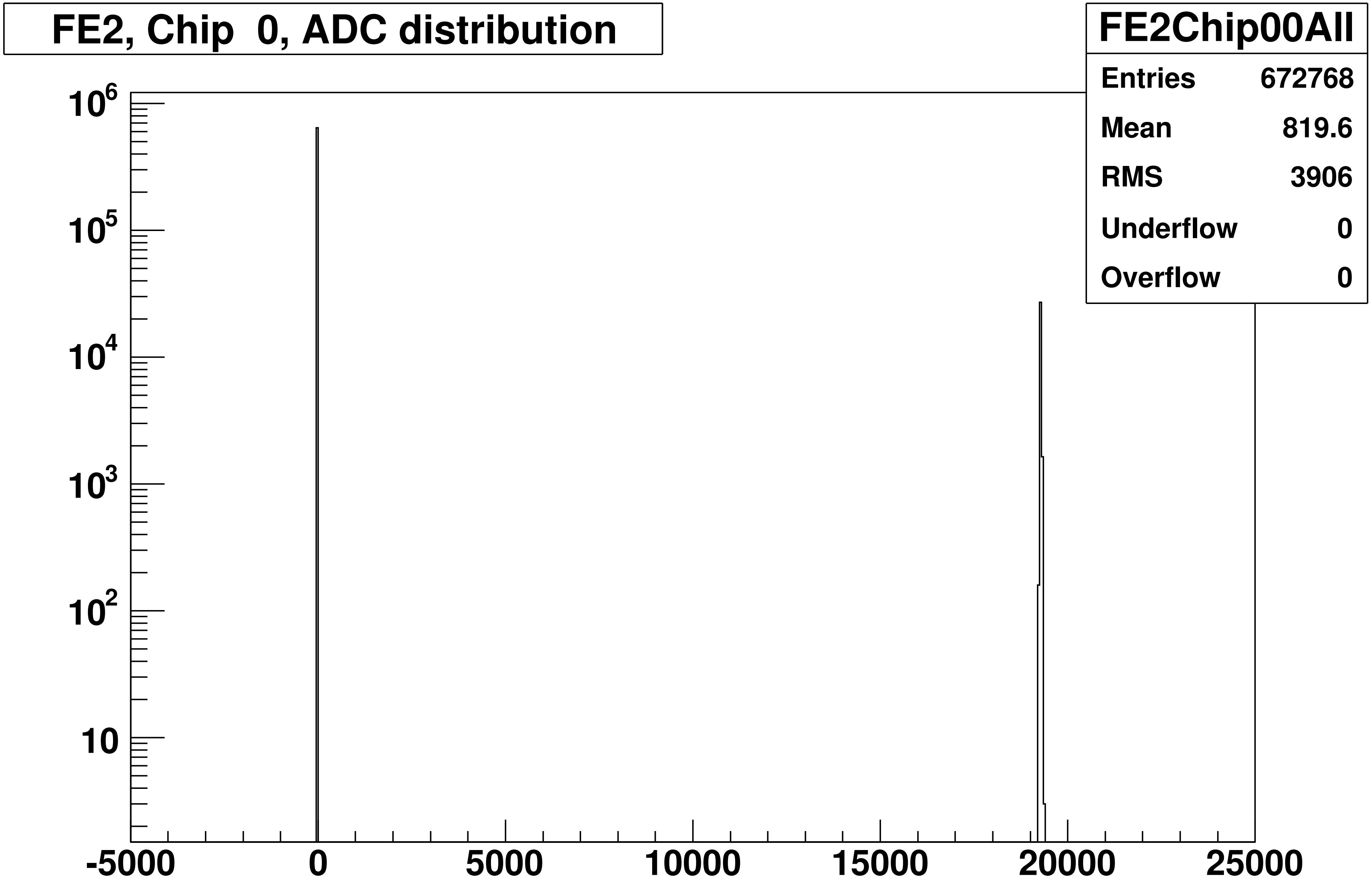
100
150
200



FE1, Chip 11, ADC distribution
FE1Chip11Sig
Entries 672768
Mean 1.922e+04
RMS 4.211
Underflow 6.458e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE2, Chip 0, ADC distribution
FE2Chip00All
Entries 672768
Mean 819.6
RMS 3906
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
-5000
0
5000
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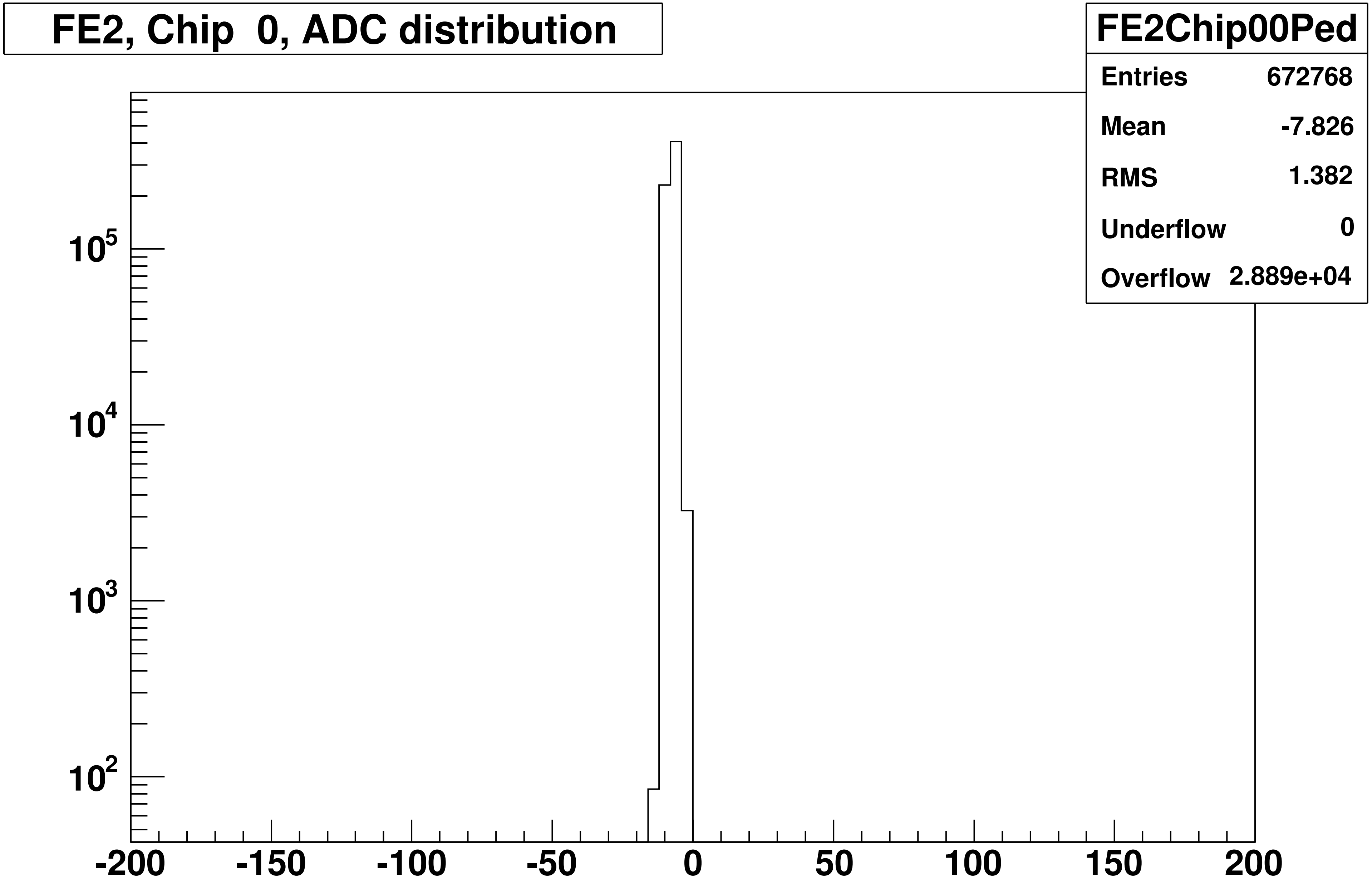
FE2, Chip 0, ADC distribution
FE2Chip00Ped
Entries 672768
Mean -7.826
RMS 1.382
Underflow 0
Overflow 2.889e+04
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10^4
10^3
10^2
-200
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-100
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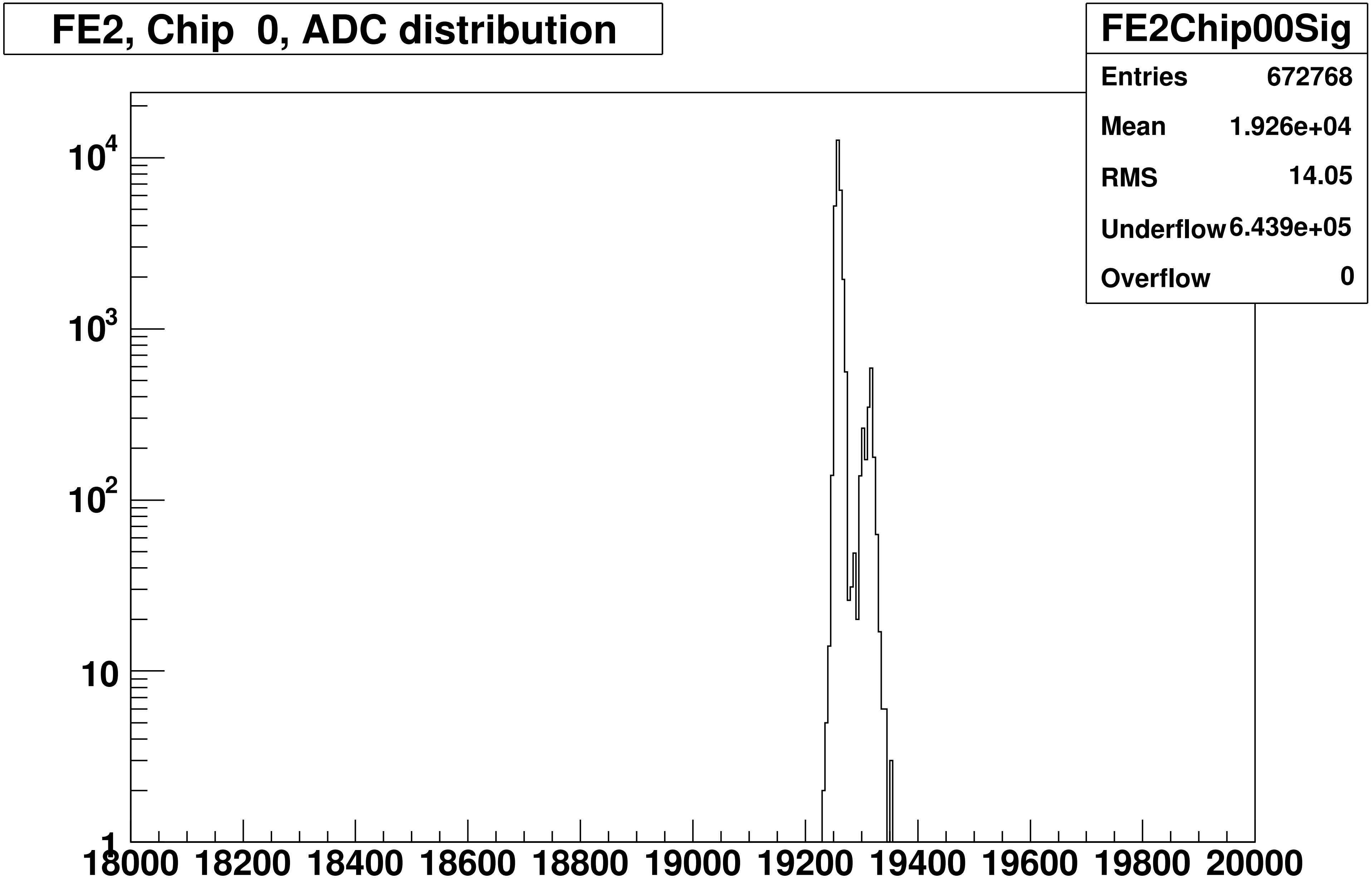
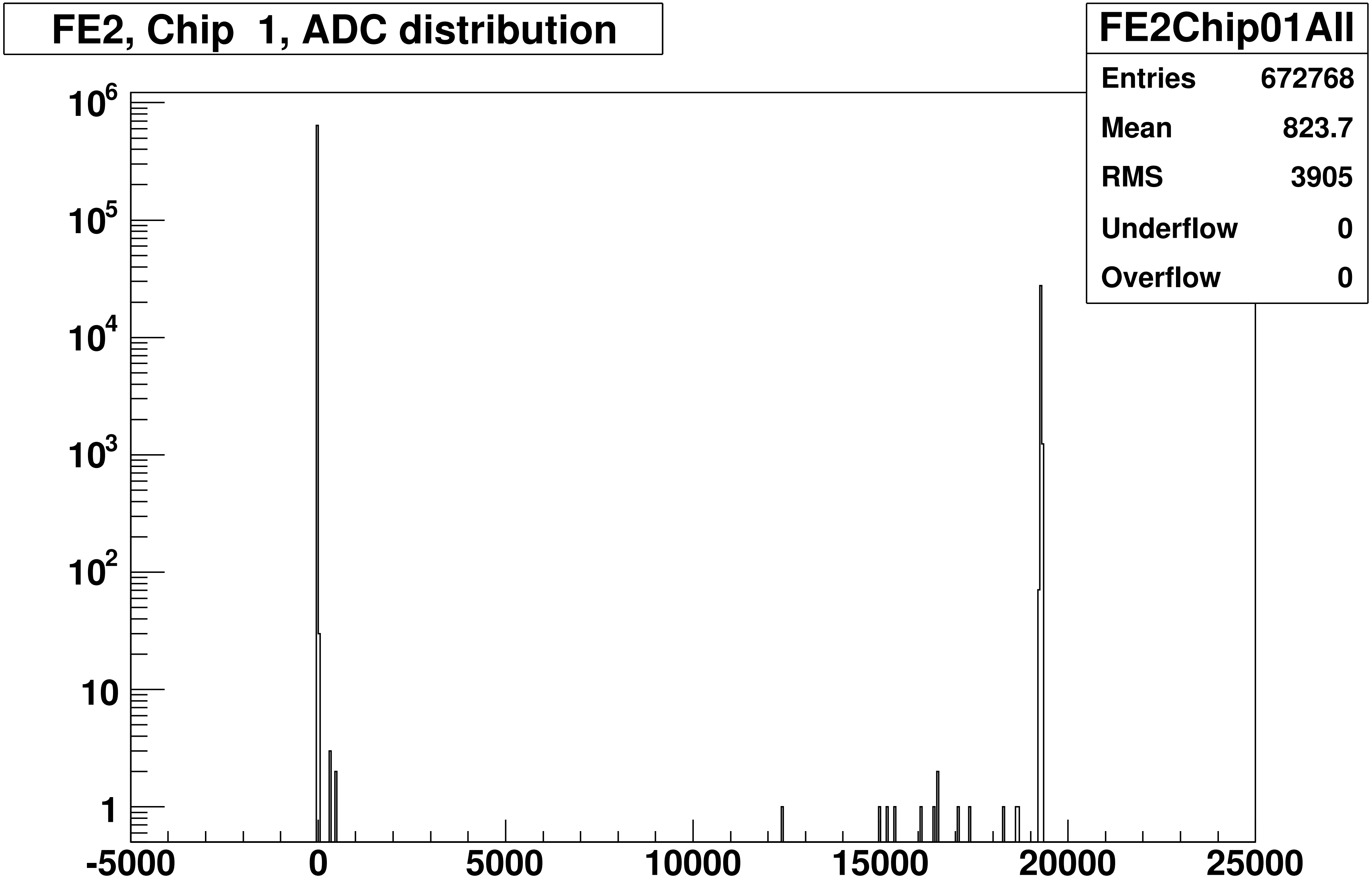
100
150
200



FE2, Chip 0, ADC distribution
FE2Chip00Sig
Entries 672768
Mean 1.926e+04
RMS 14.05
Underflow 6.439e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE2, Chip 1, ADC distribution
FE2Chip01All
Entries 672768
Mean 823.7
RMS 3905
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
1
-5000
0
5000
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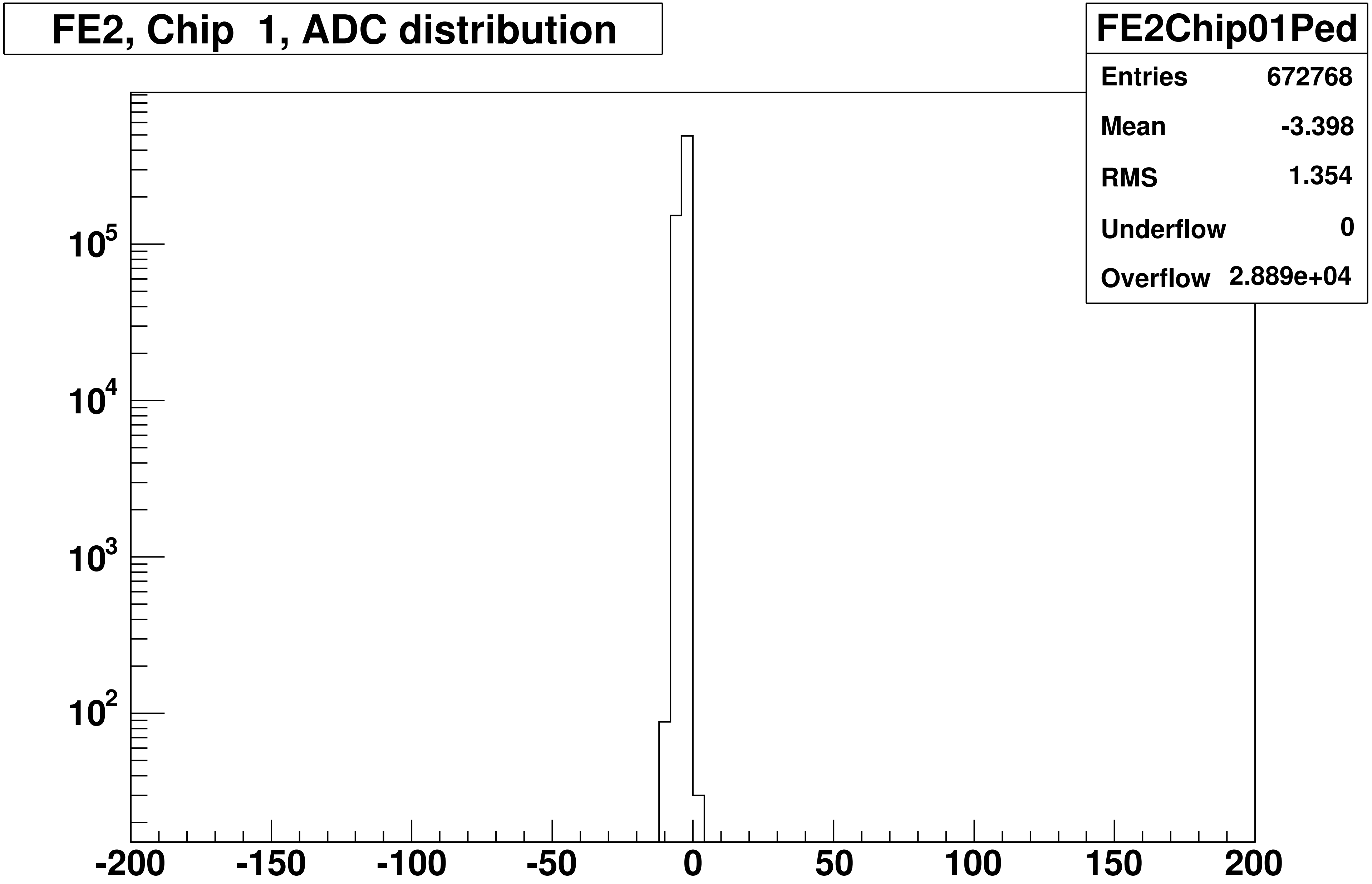
25000


FE2, Chip 1, ADC distribution
FE2Chip01Ped
Entries 672768
Mean -3.398
RMS 1.354
Underflow 0
Overflow 2.889e+04
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10^4
10^3
10^2
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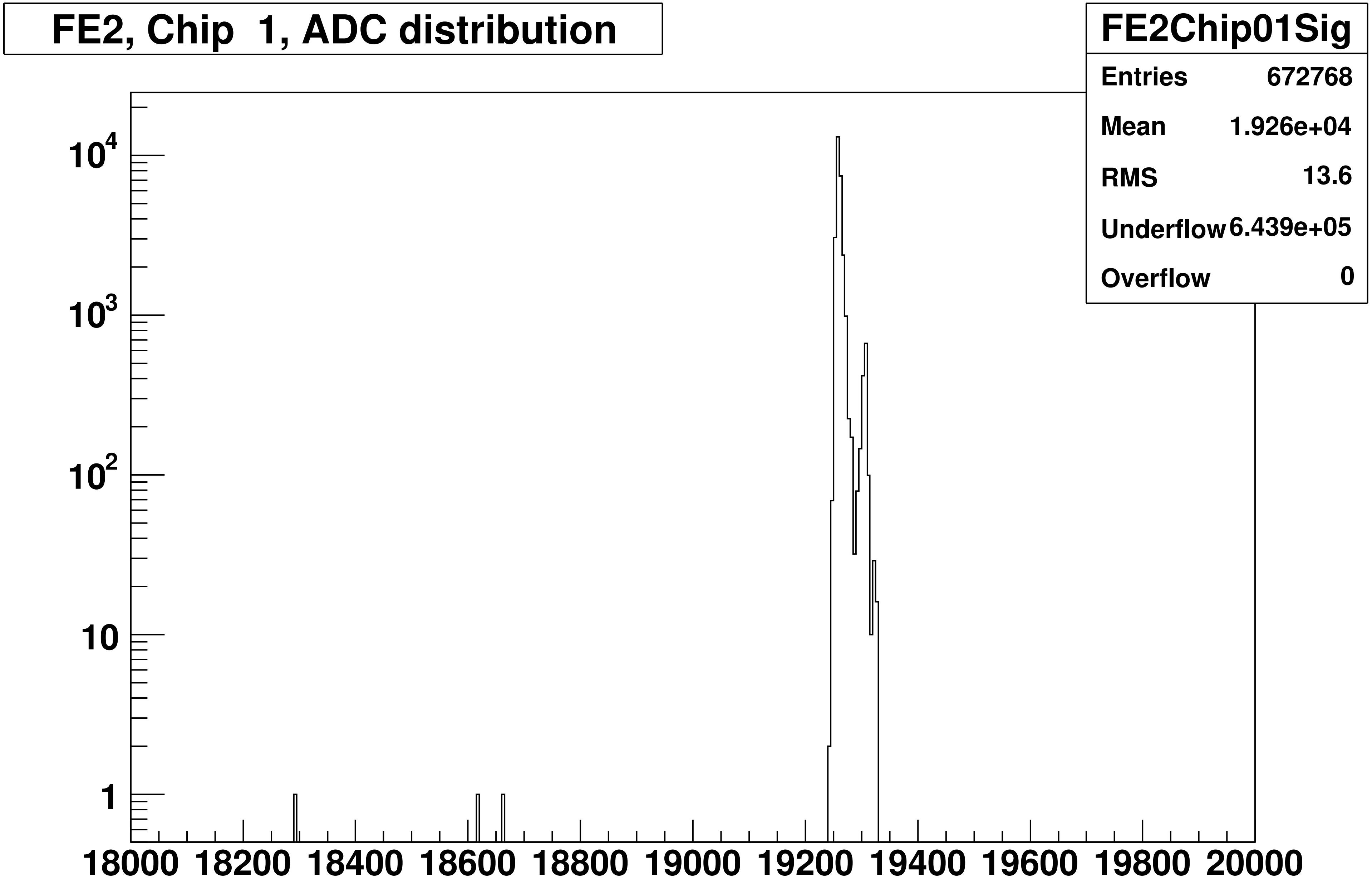
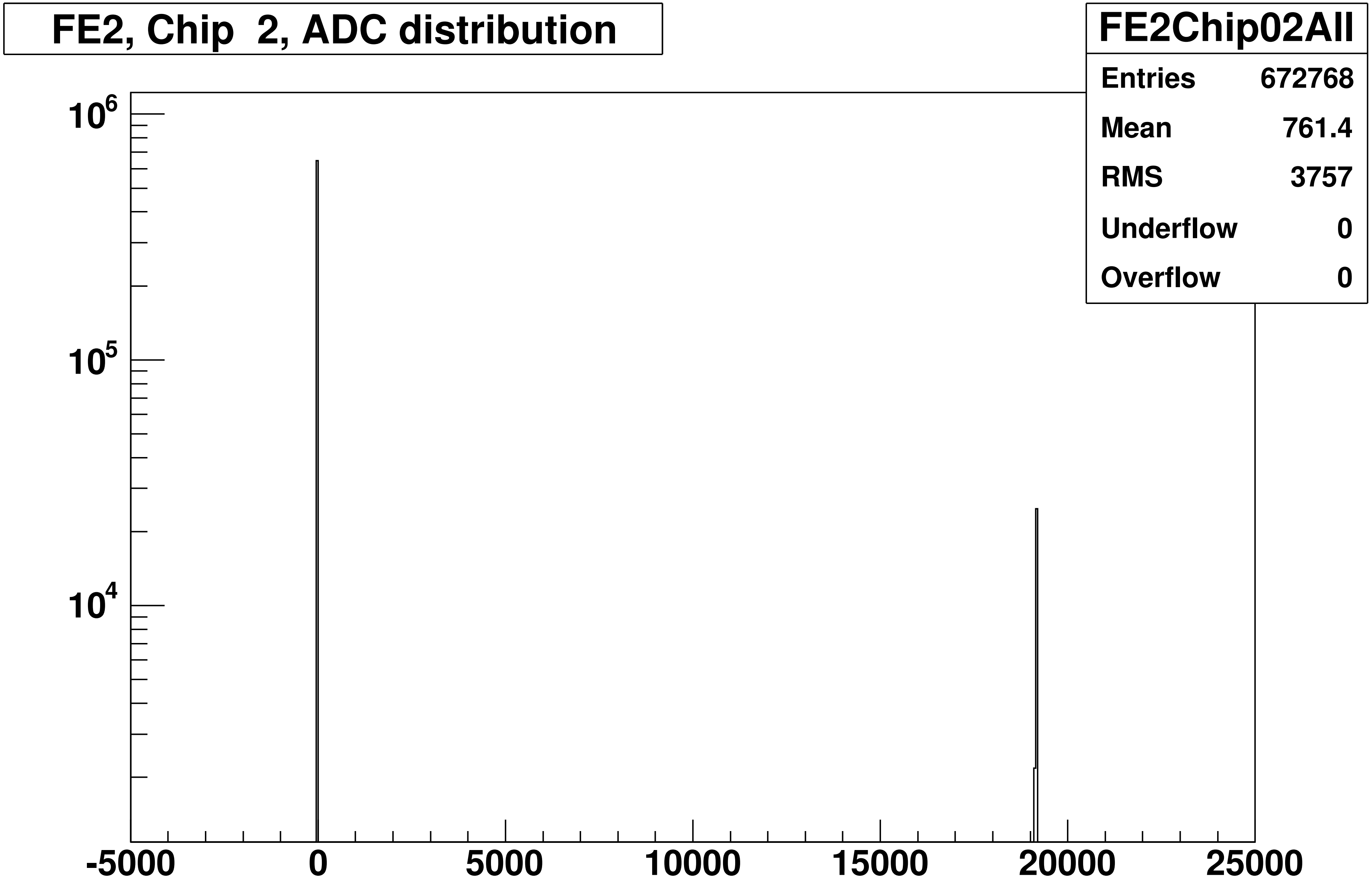
150
200


FE2, Chip 1, ADC distribution
FE2Chip01Sig
Entries 672768
Mean 1.926e+04
RMS 13.6
Underflow 6.439e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE2, Chip 2, ADC distribution
FE2Chip02All
Entries 672768
Mean 761.4
RMS 3757
Underflow 0
Overflow 0
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10^5
10^4
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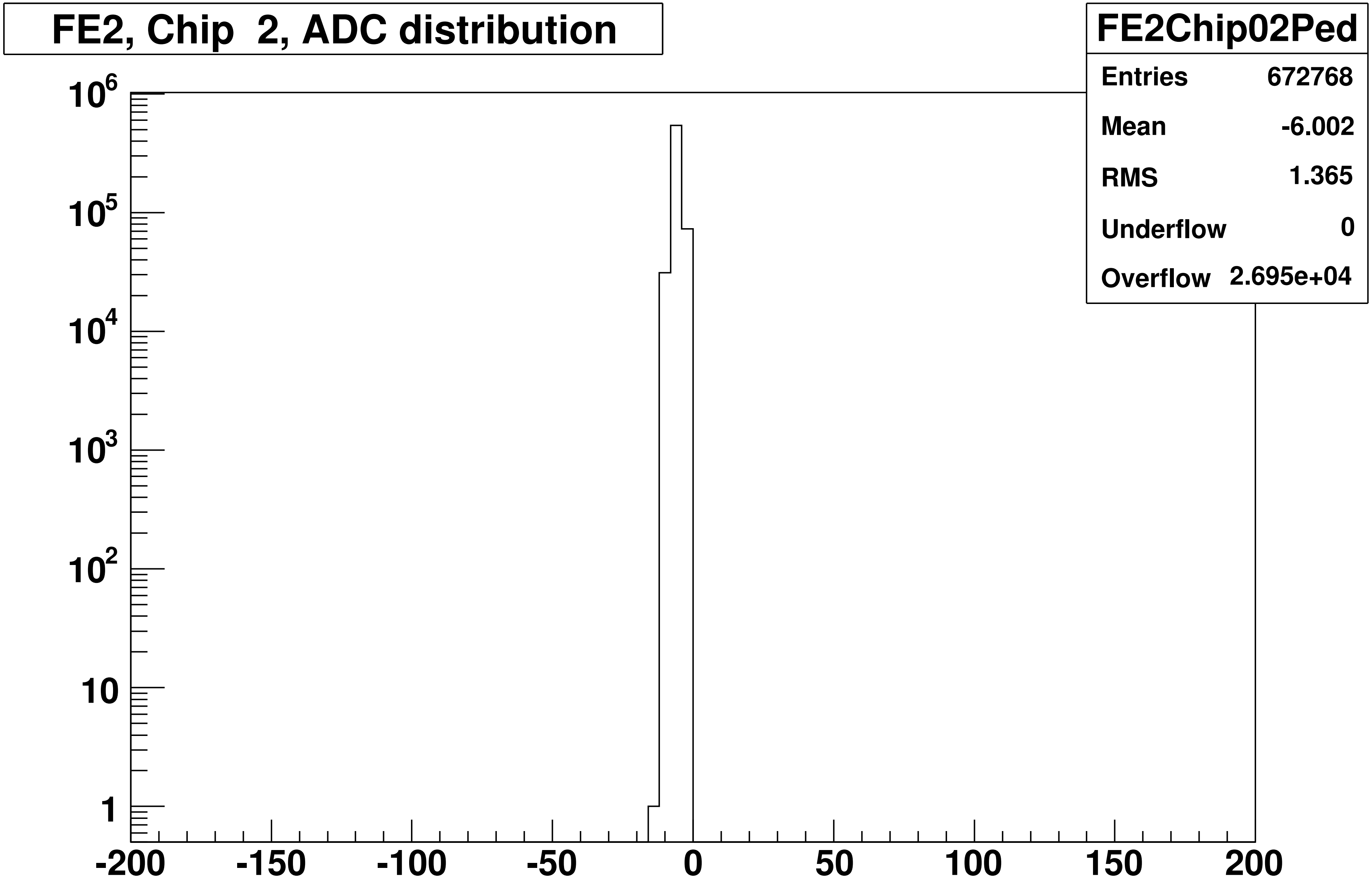
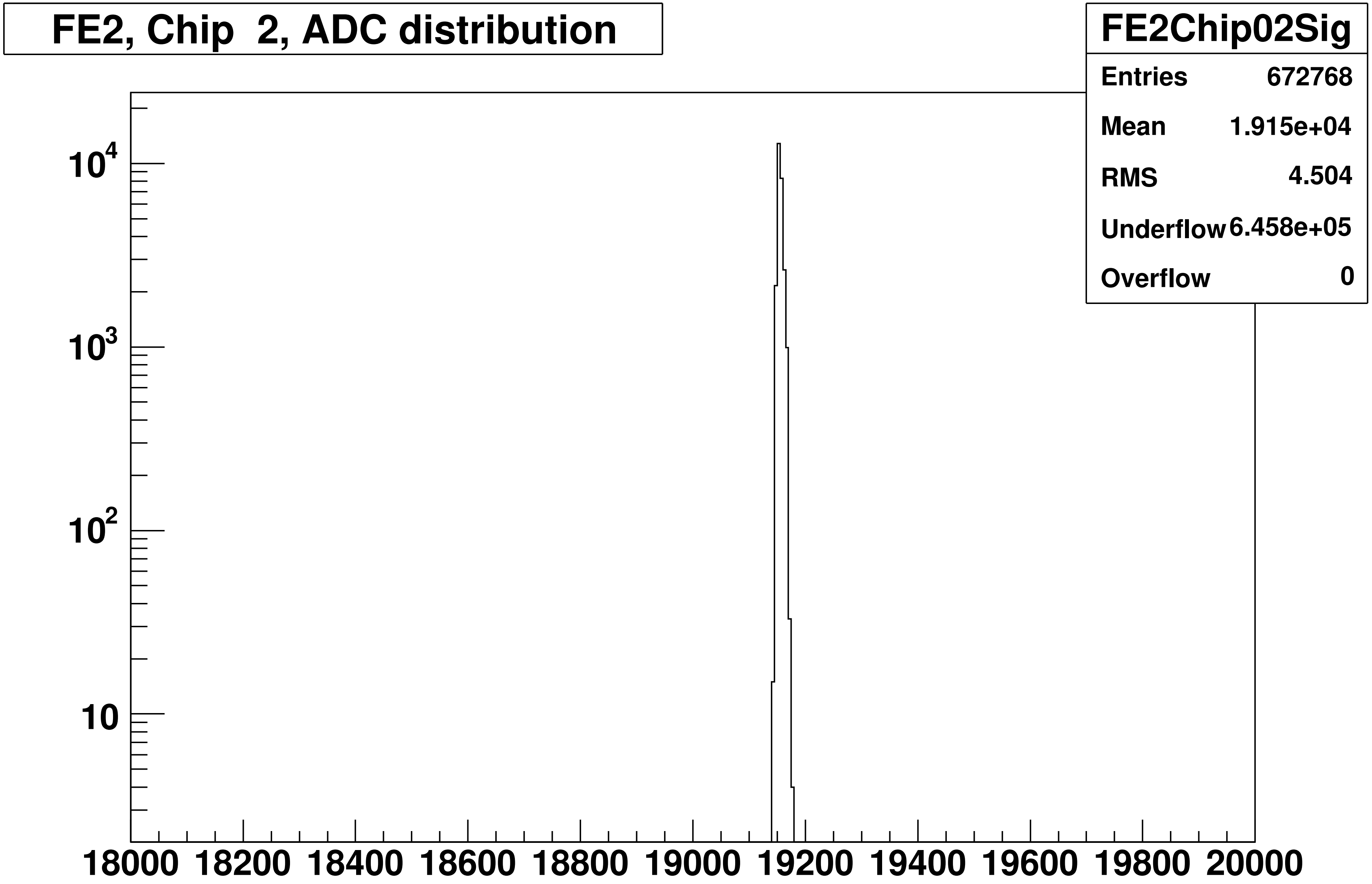
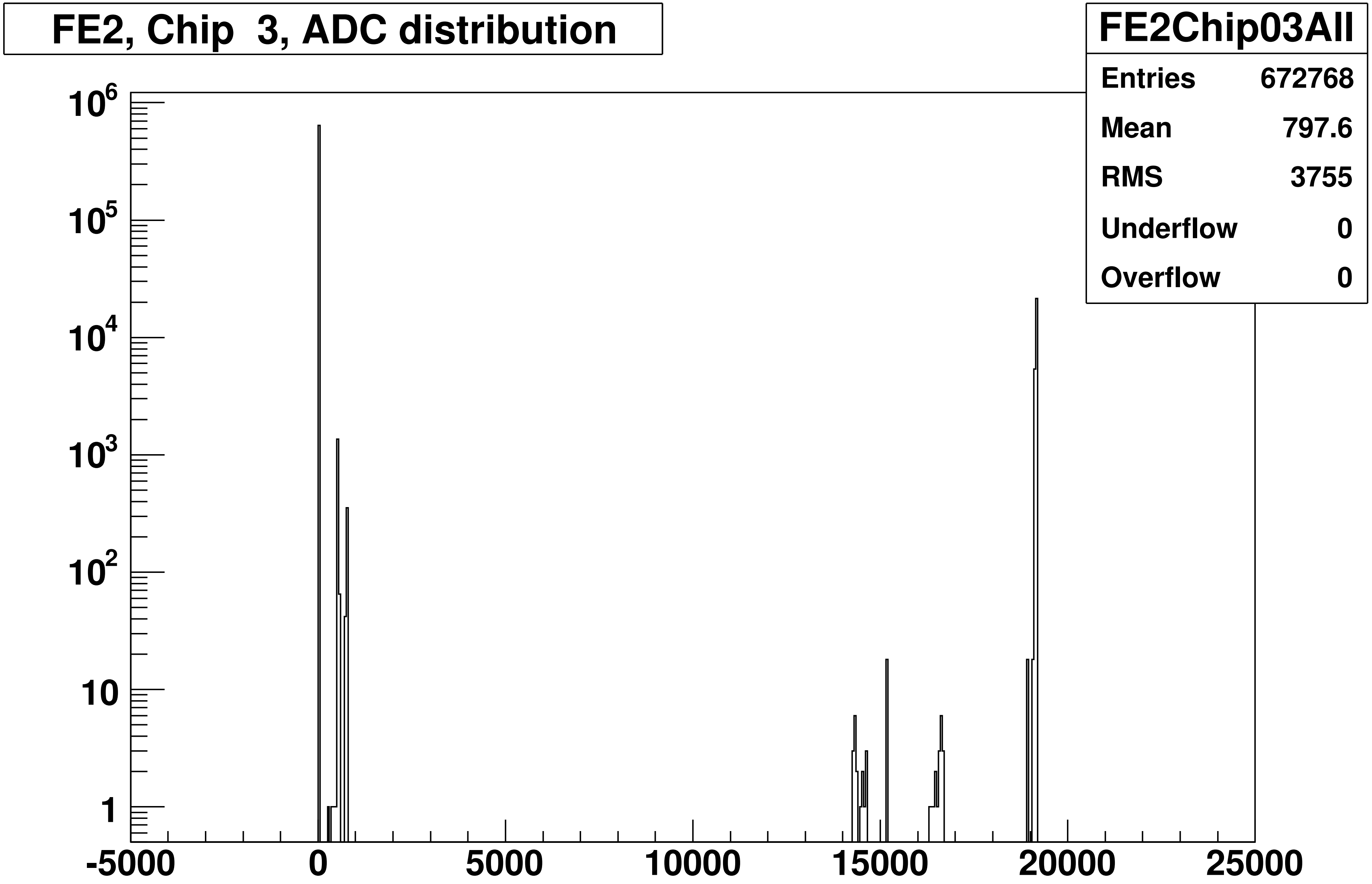
10000
15000
20000
25000



FE2, Chip 2, ADC distribution
FE2Chip02Ped
Entries 672768
Mean -6.002
RMS 1.365
Underflow 0
Overflow 2.695e+04



FE2, Chip 2, ADC distribution
FE2Chip02Sig
Entries 672768
Mean 1.915e+04
RMS 4.504
Underflow 6.458e+05
Overflow 0
10^4
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE2, Chip 3, ADC distribution
FE2Chip03All
Entries 672768
Mean 797.6
RMS 3755
Underflow 0
Overflow 0
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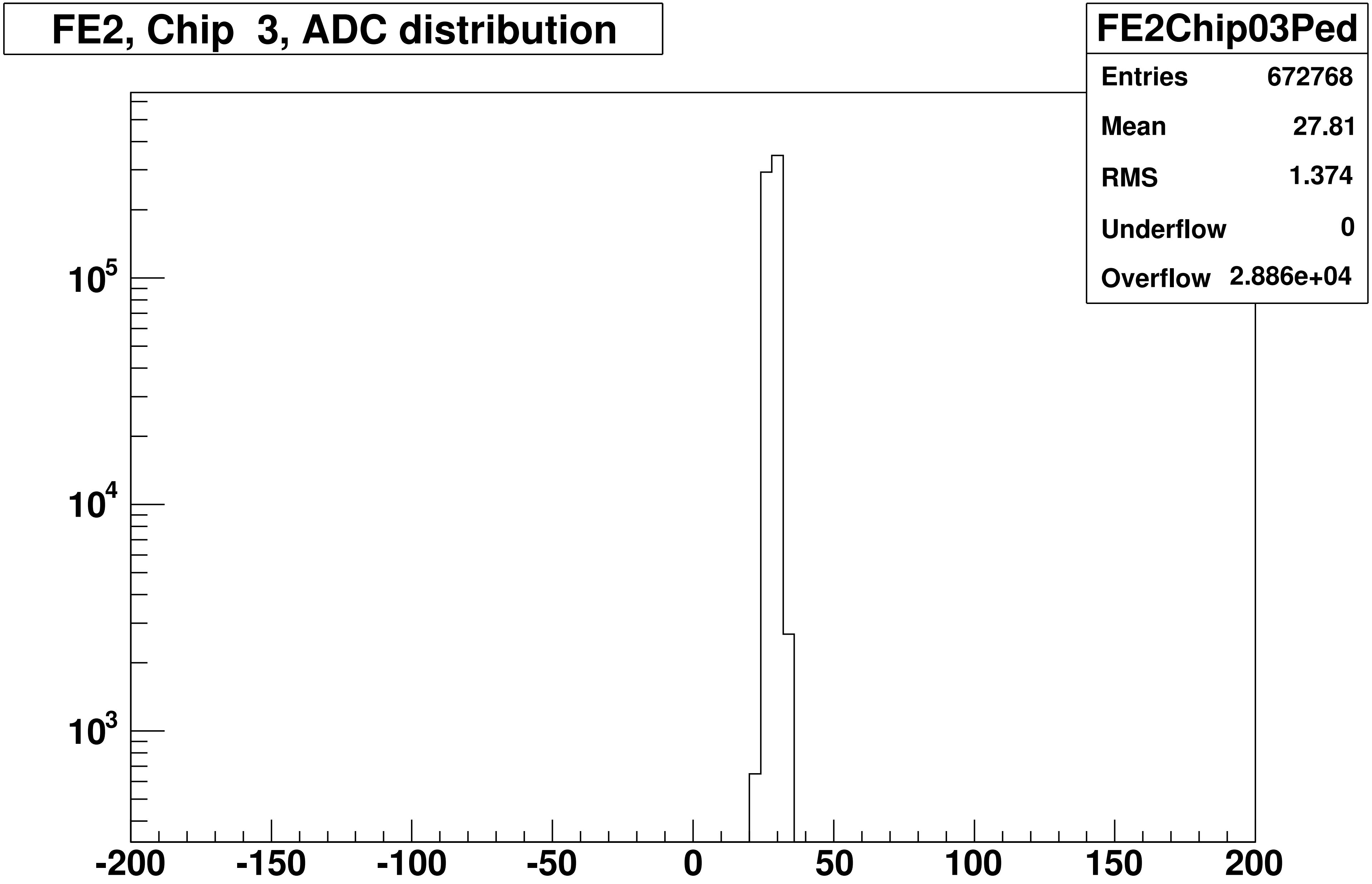
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE2, Chip 3, ADC distribution
FE2Chip03Ped
Entries 672768
Mean 27.81
RMS 1.374
Underflow 0
Overflow 2.886e+04
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10^4
10^3
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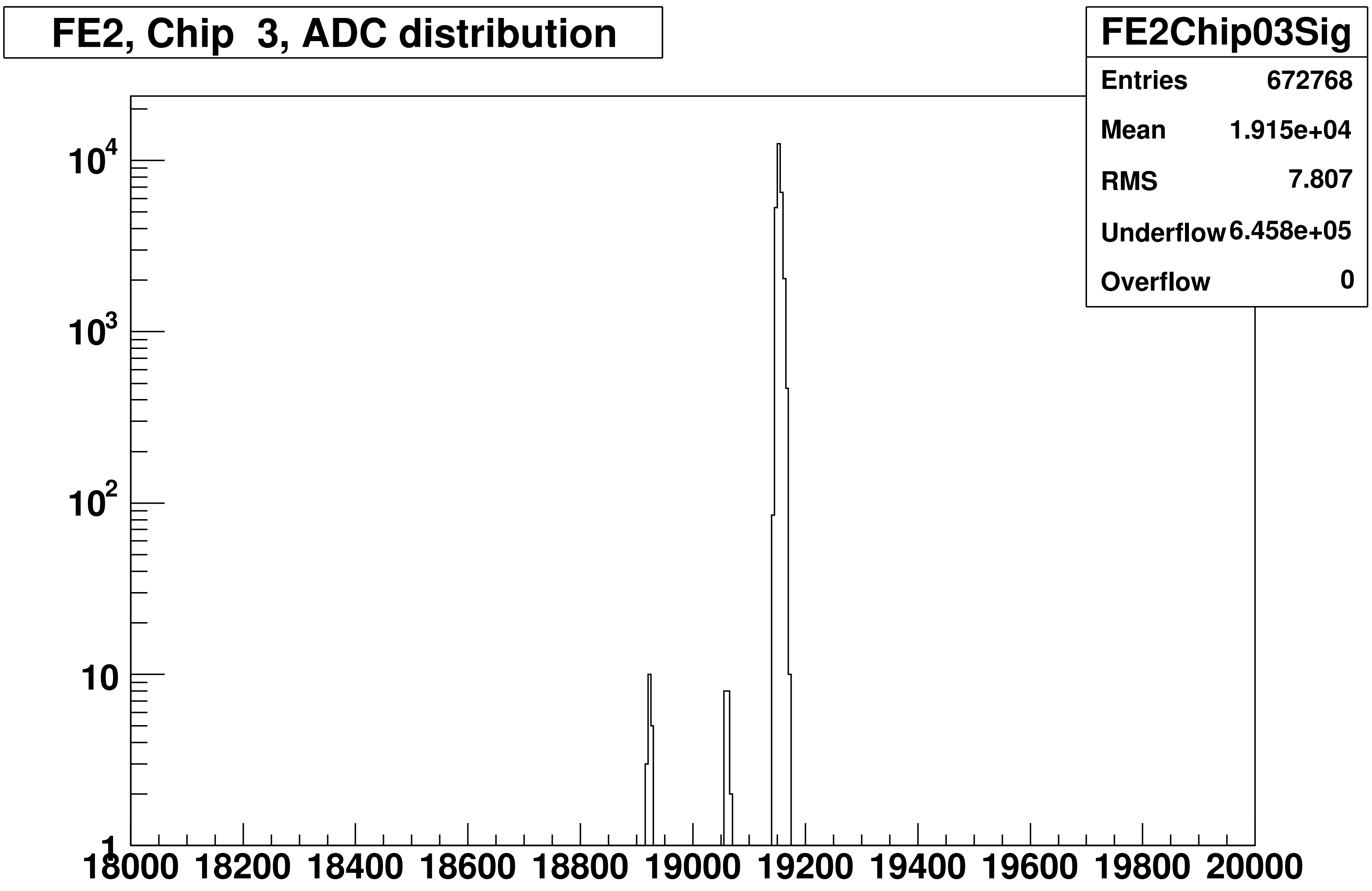
0
50
100
150
200


FE2, Chip 3, ADC distribution
FE2Chip03Sig
Entries 672768
Mean 1.915e+04
RMS 7.807
Underflow 6.458e+05
Overflow 0
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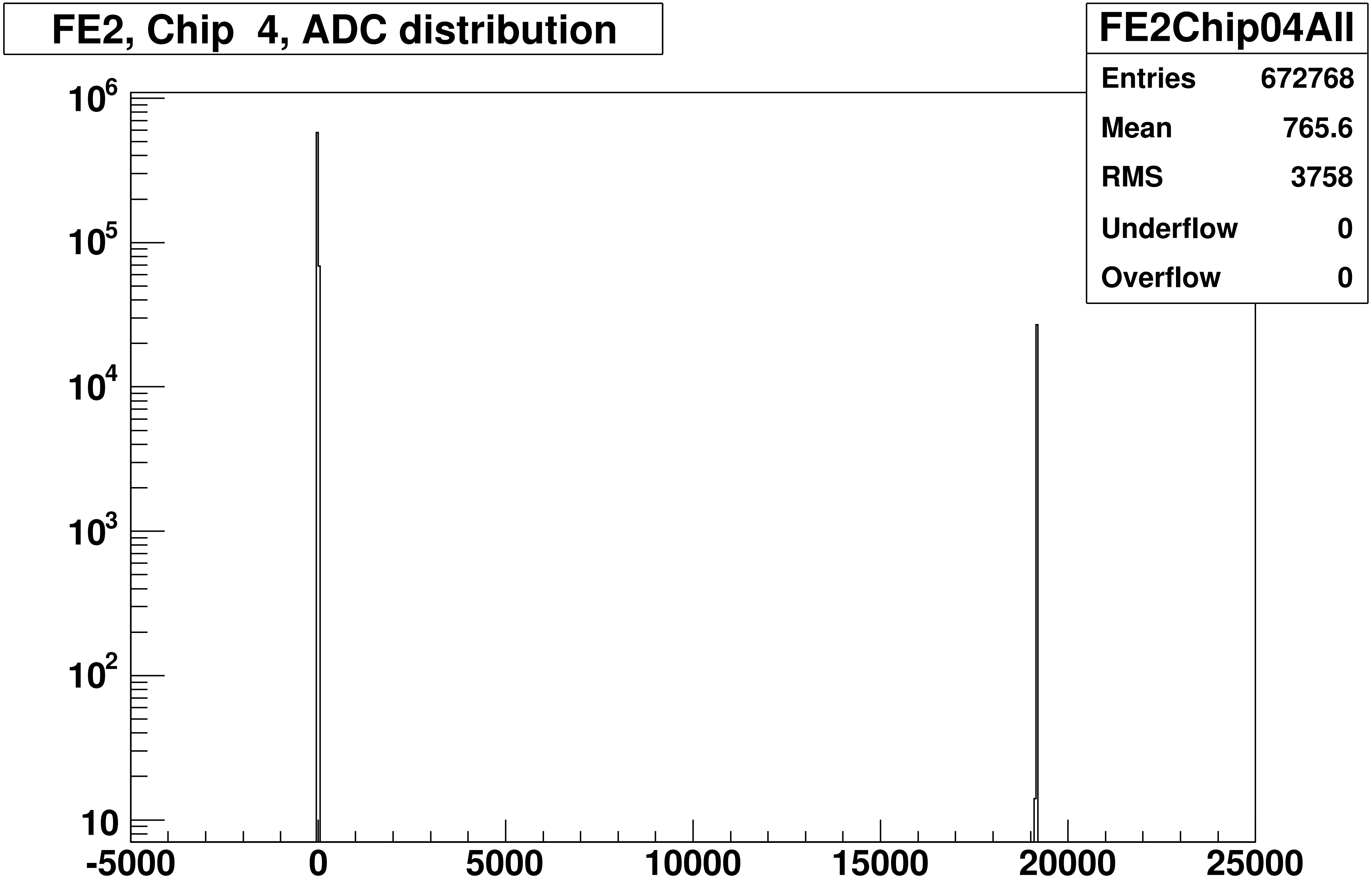
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE2, Chip 4, ADC distribution
FE2Chip04All
Entries 672768
Mean 765.6
RMS 3758
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
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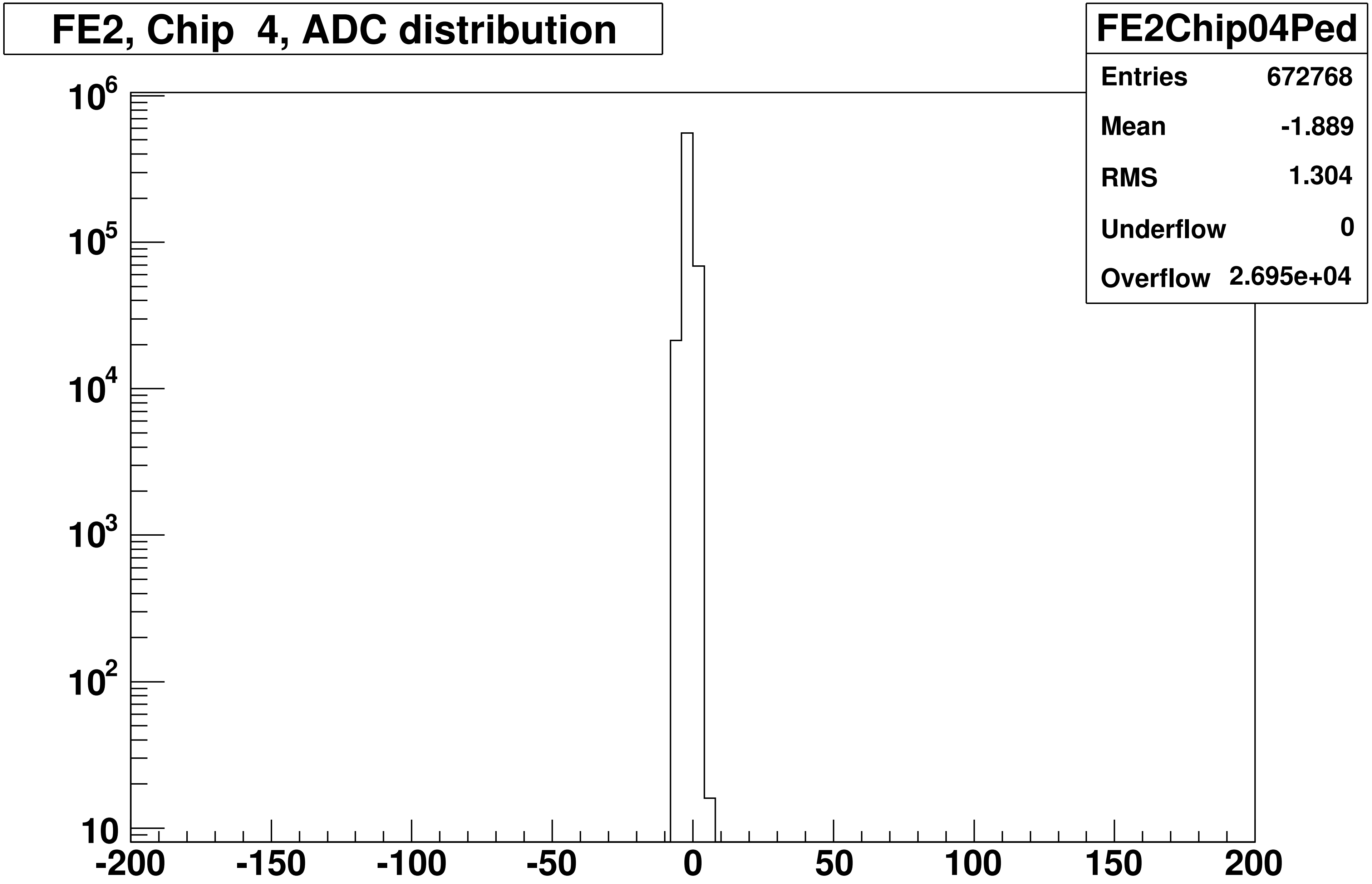
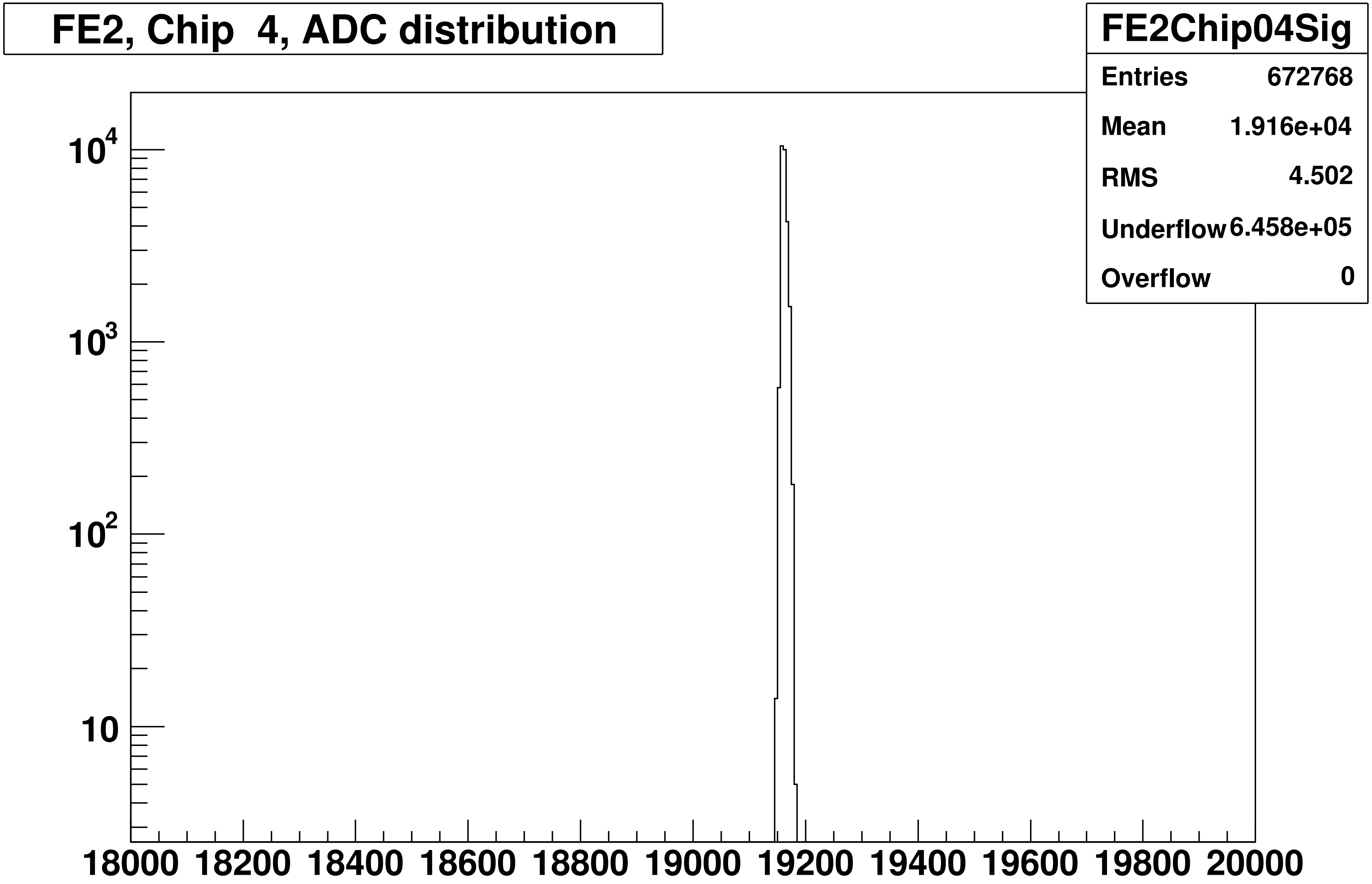
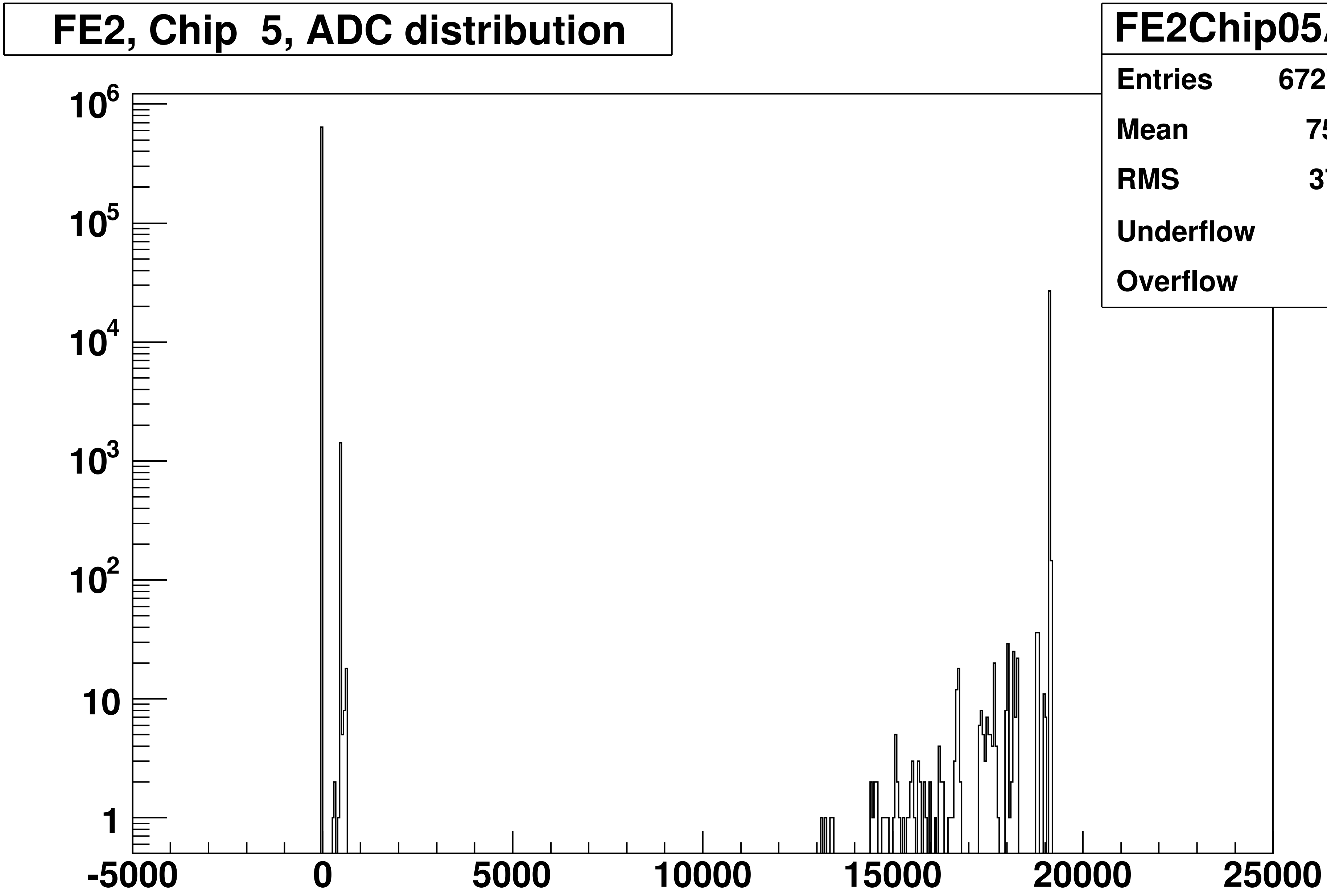
5000
10000
15000
20000
25000



FE2, Chip 4, ADC distribution
FE2Chip04Ped
Entries 672768
Mean -1.889
RMS 1.304
Underflow 0
Overflow 2.695e+04
10^6
10^5
10^4
10^3
10^2
10
-200
-150
-100
-50
0
50
100
150
200



FE2, Chip 4, ADC distribution
FE2Chip04Sig
Entries 672768
Mean 1.916e+04
RMS 4.502
Underflow 6.458e+05
Overflow 0
10^4
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE2, Chip 5, ADC distribution
FE2Chip05All
Entries 672768
Mean 756.1
RMS 3785
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
1
-5000
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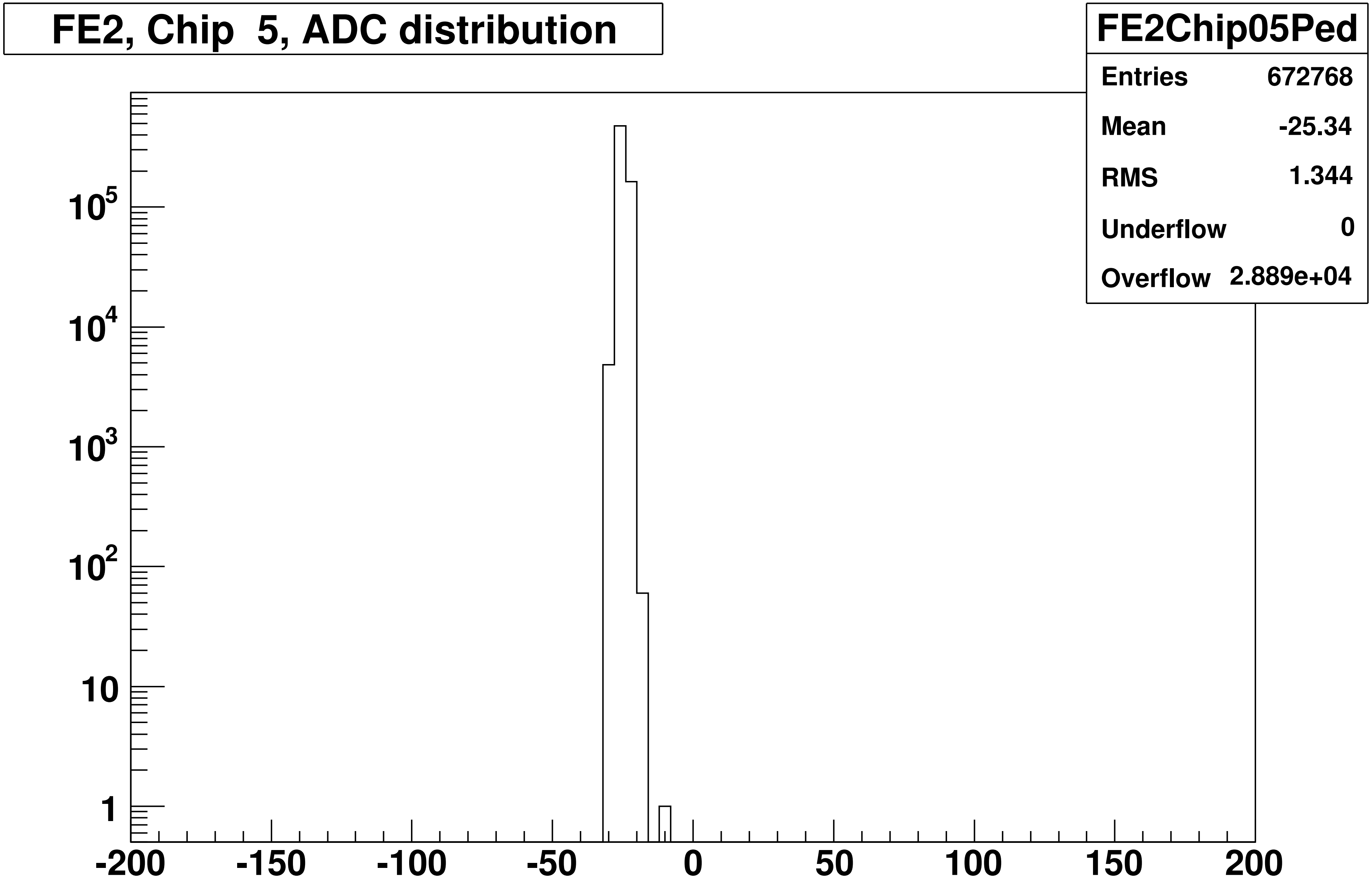
5000
10000
15000
20000
25000


FE2, Chip 5, ADC distribution
FE2Chip05Ped
Entries 672768
Mean -25.34
RMS 1.344
Underflow 0
Overflow 2.889e+04
10^5
10^4
10^3
10^2
10
1
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-150
-100
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0
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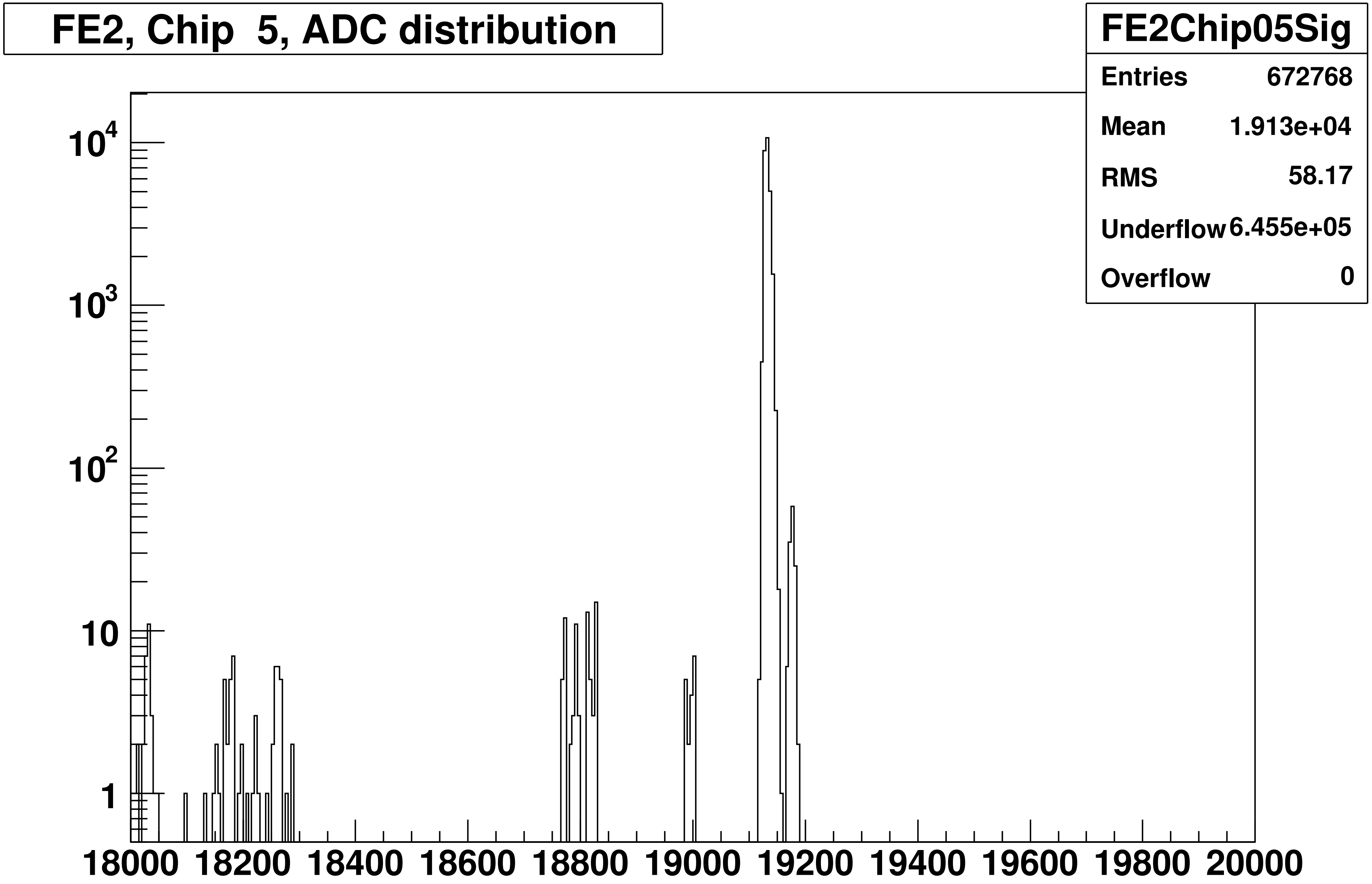
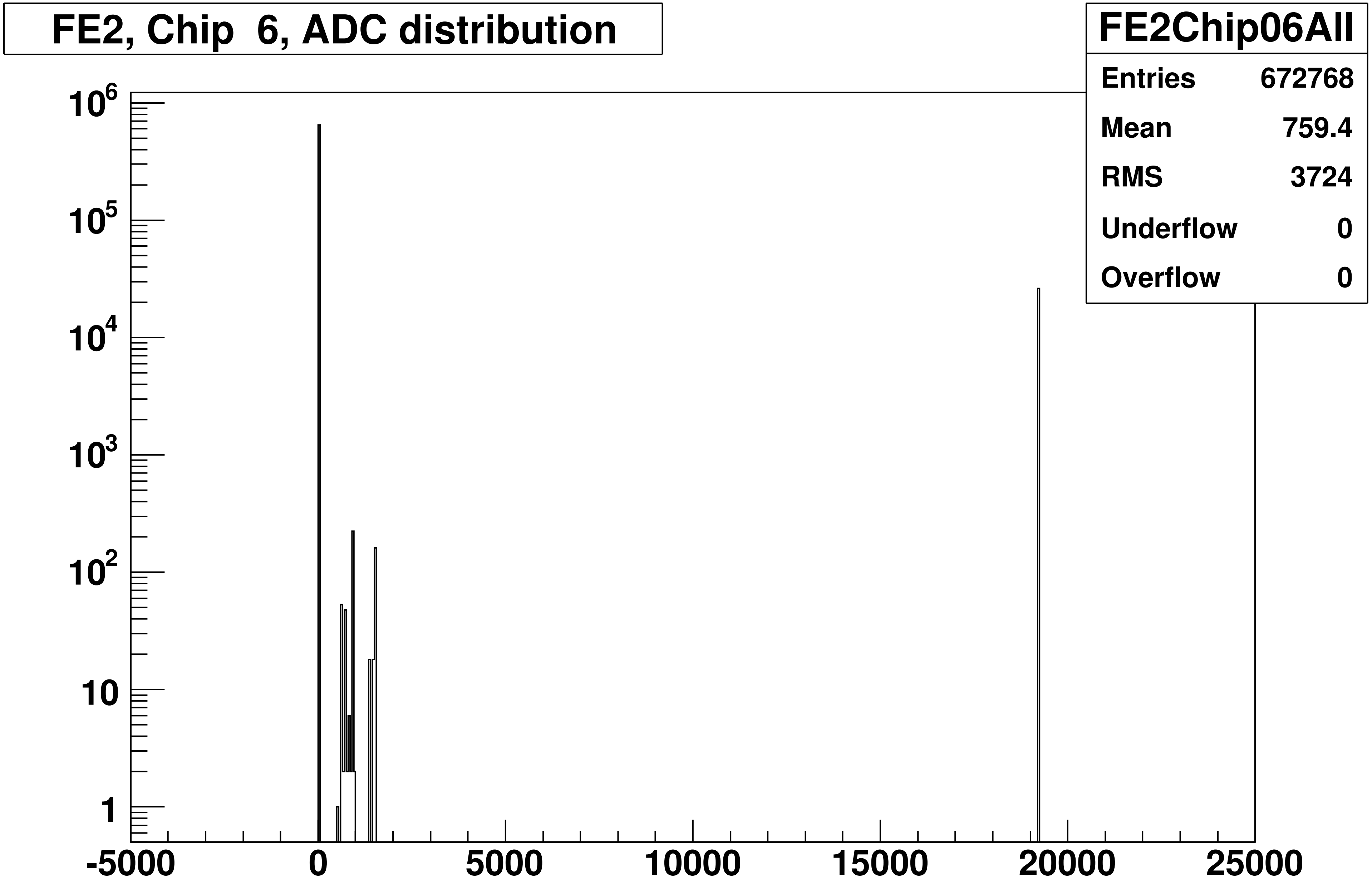
100
150
200



FE2, Chip 5, ADC distribution
FE2Chip05Sig
Entries 672768
Mean 1.913e+04
RMS 58.17
Underflow 6.455e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE2, Chip 6, ADC distribution
FE2Chip06All
Entries 672768
Mean 759.4
RMS 3724
Underflow 0
Overflow 0
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10^4
10^3
10^2
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10000
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20000
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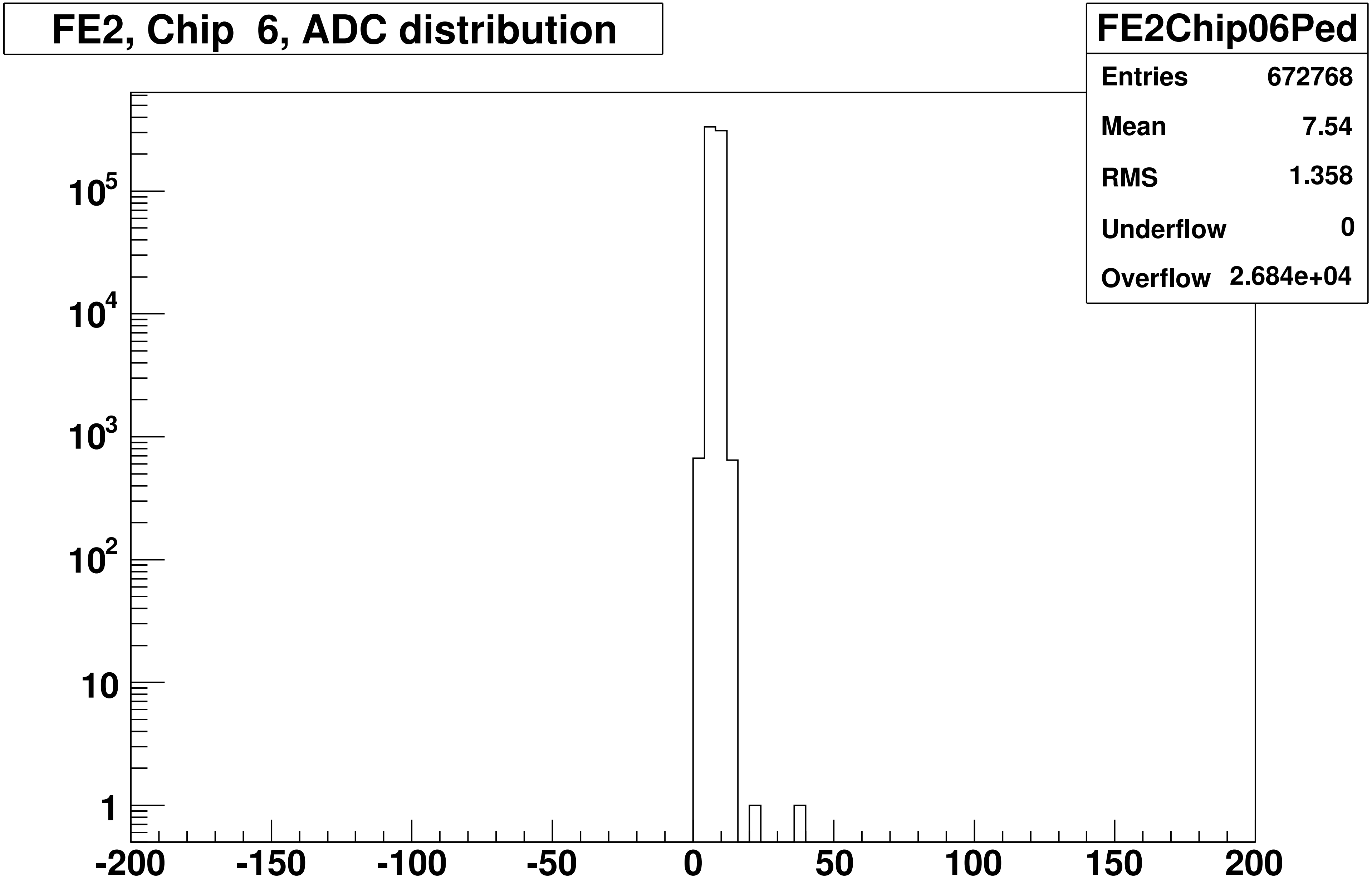
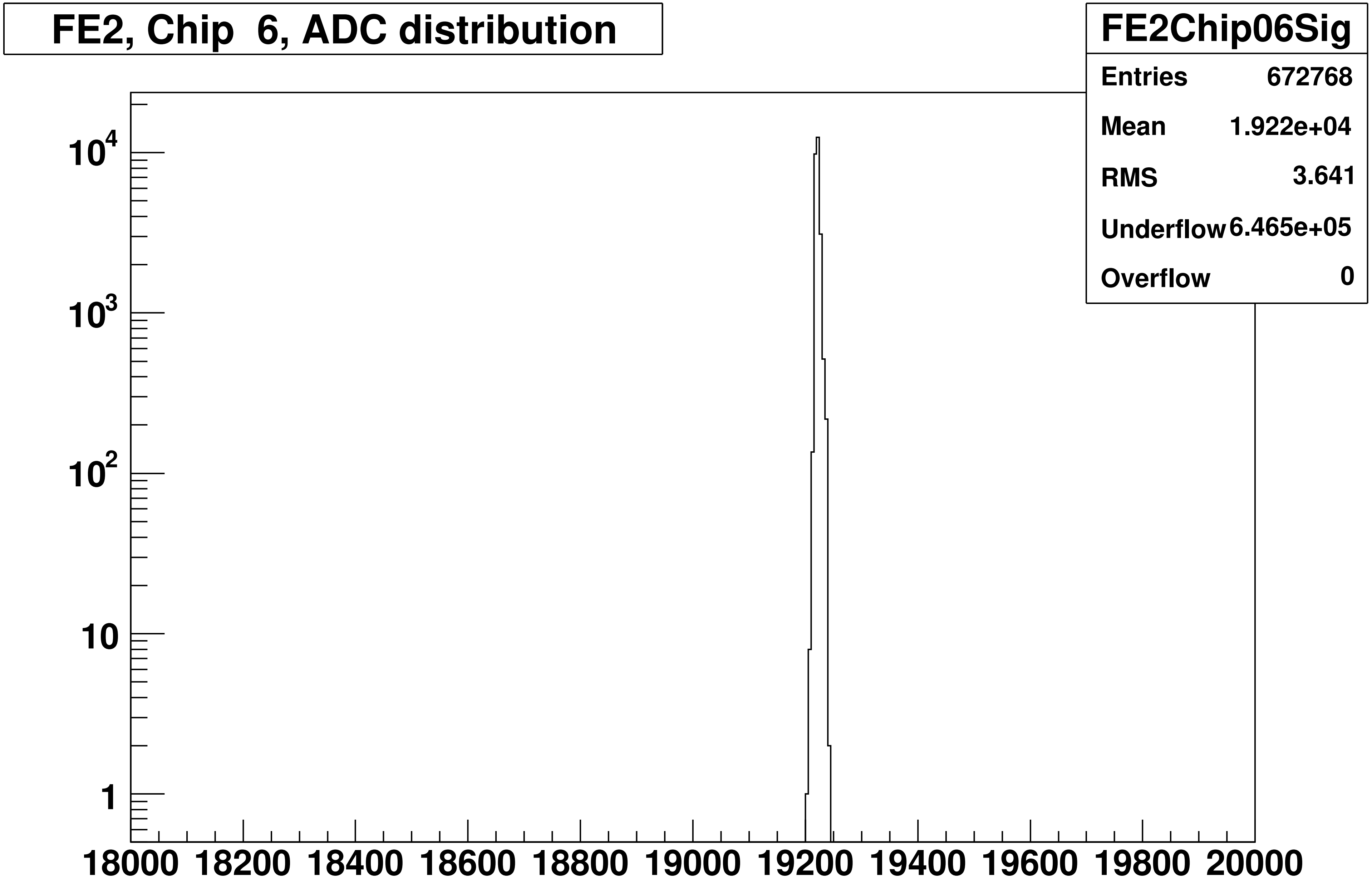
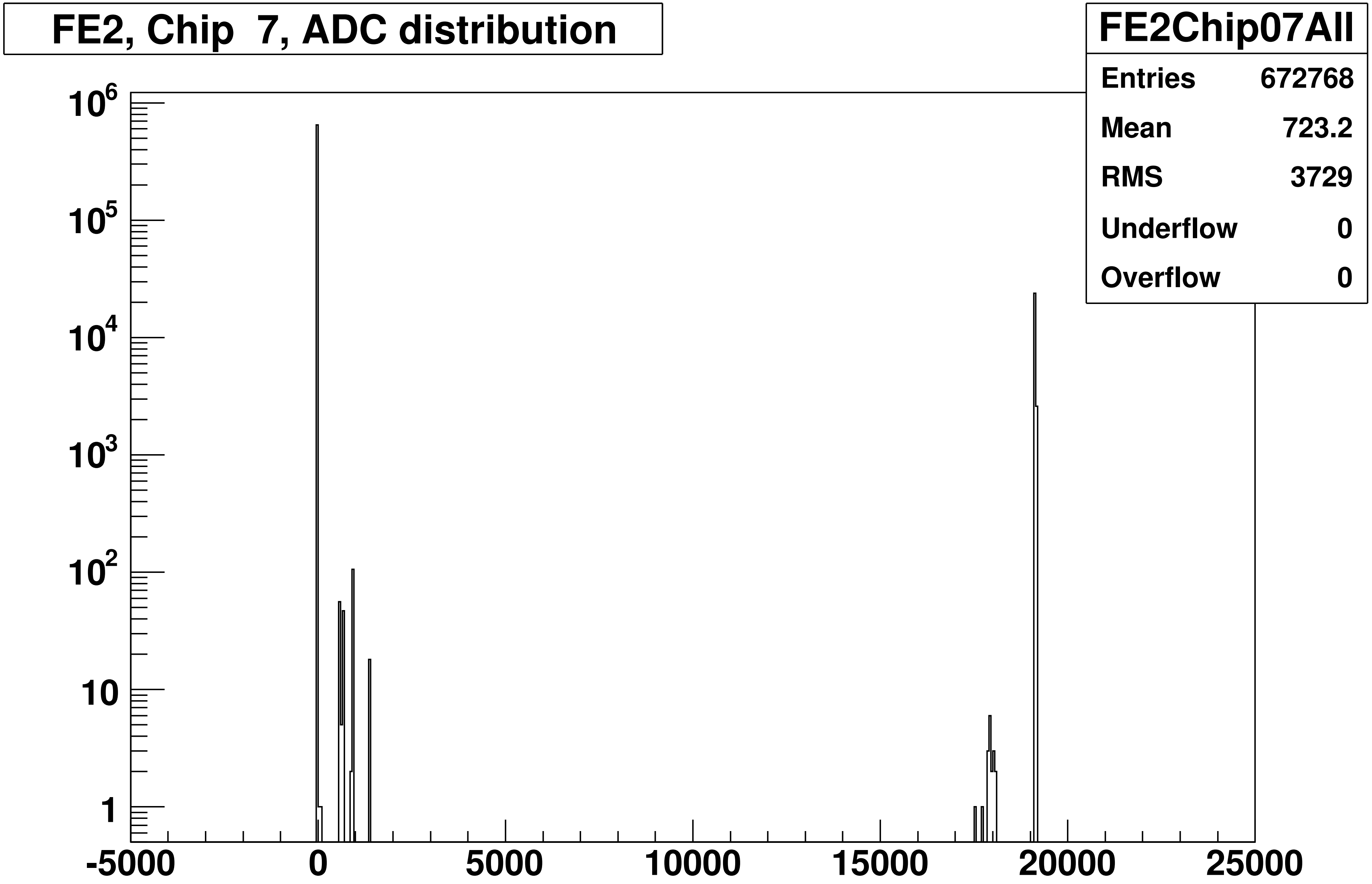


FE2, Chip 6, ADC distribution
FE2Chip06Ped
Entries 672768
Mean 7.54
RMS 1.358
Underflow 0
Overflow 2.684e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
200



FE2, Chip 6, ADC distribution
FE2Chip06Sig
Entries 672768
Mean 1.922e+04
RMS 3.641
Underflow 6.465e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000



FE2, Chip 7, ADC distribution
FE2Chip07All
Entries 672768
Mean 723.2
RMS 3729
Underflow 0
Overflow 0
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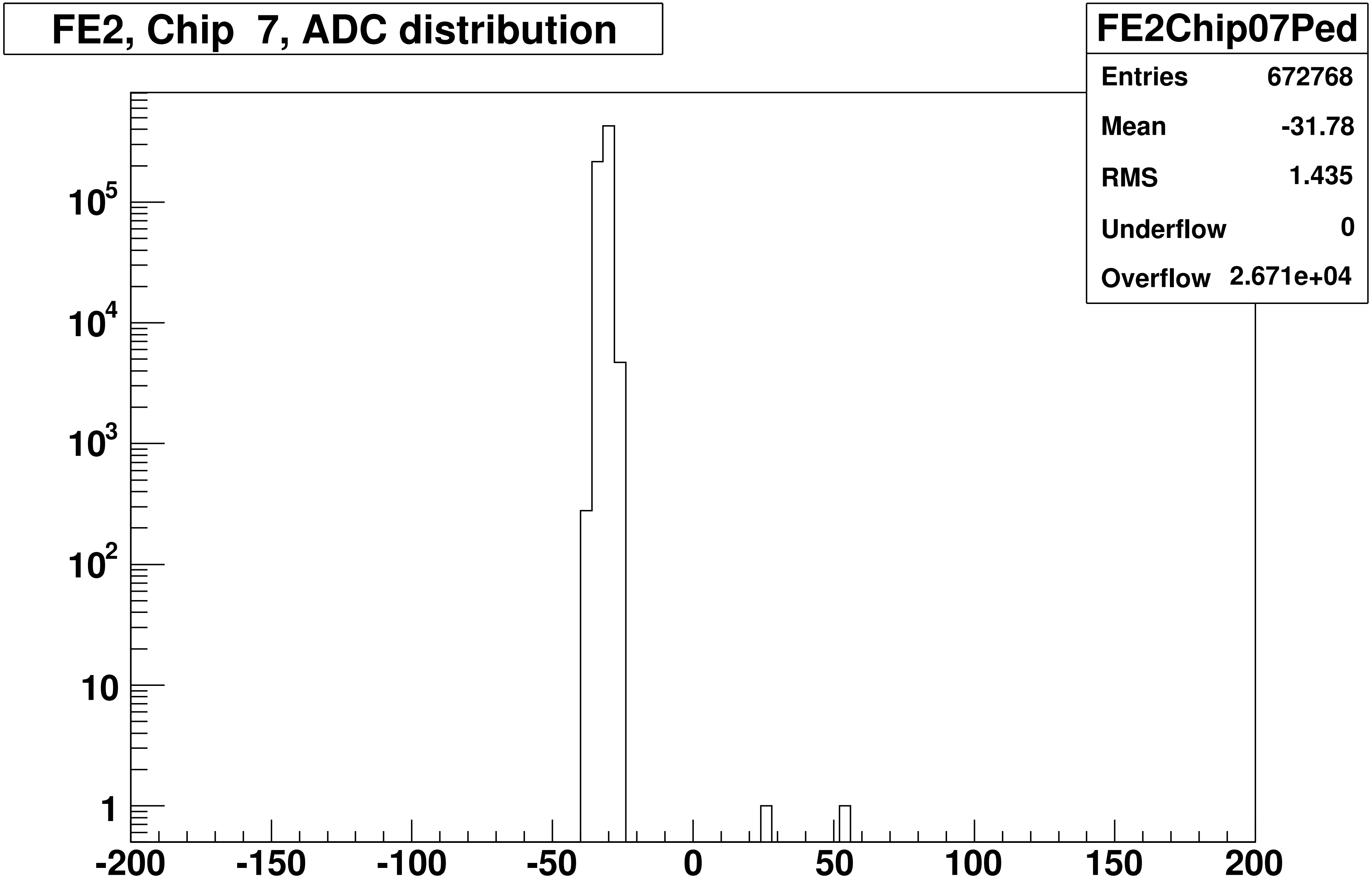
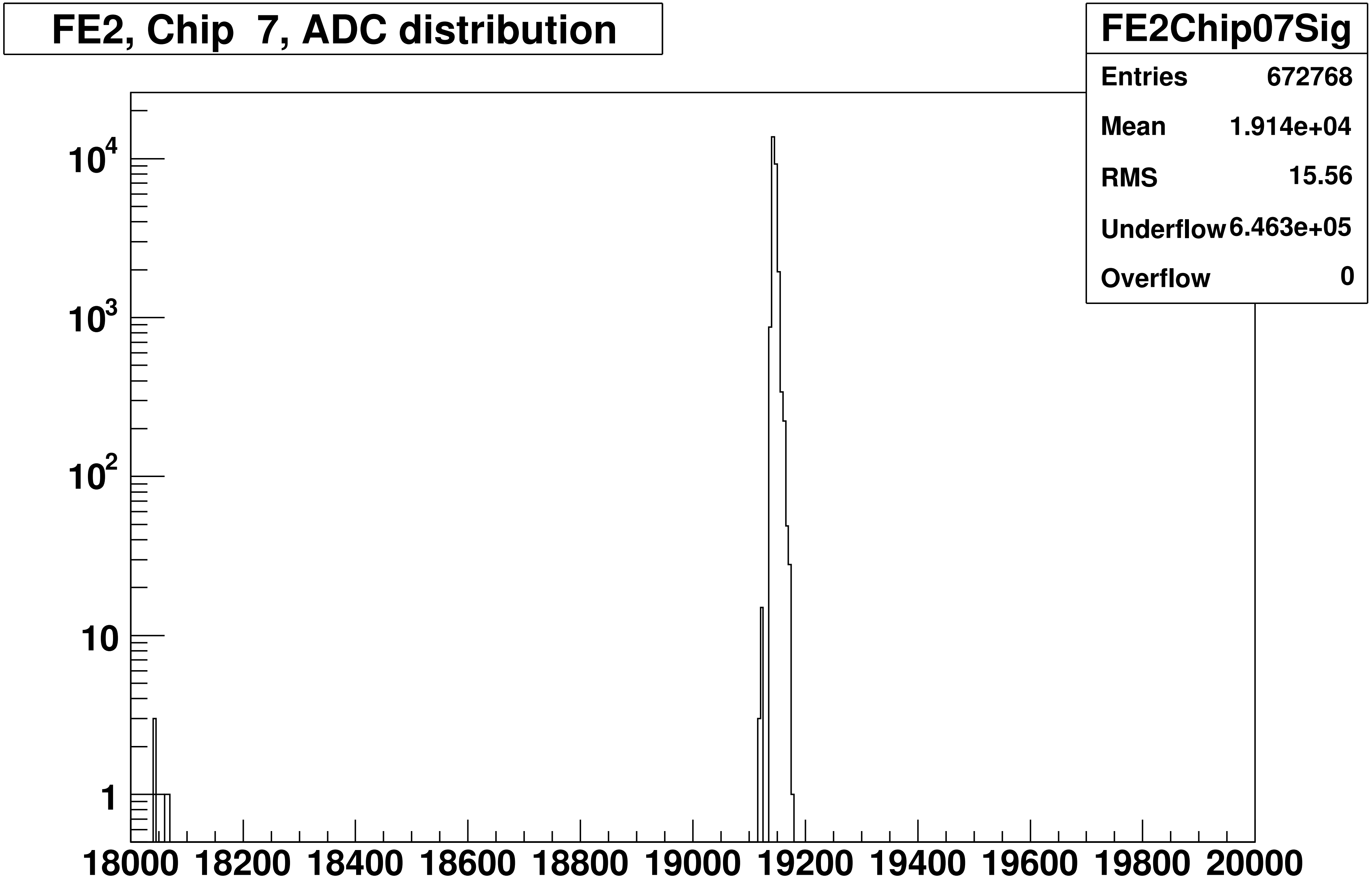
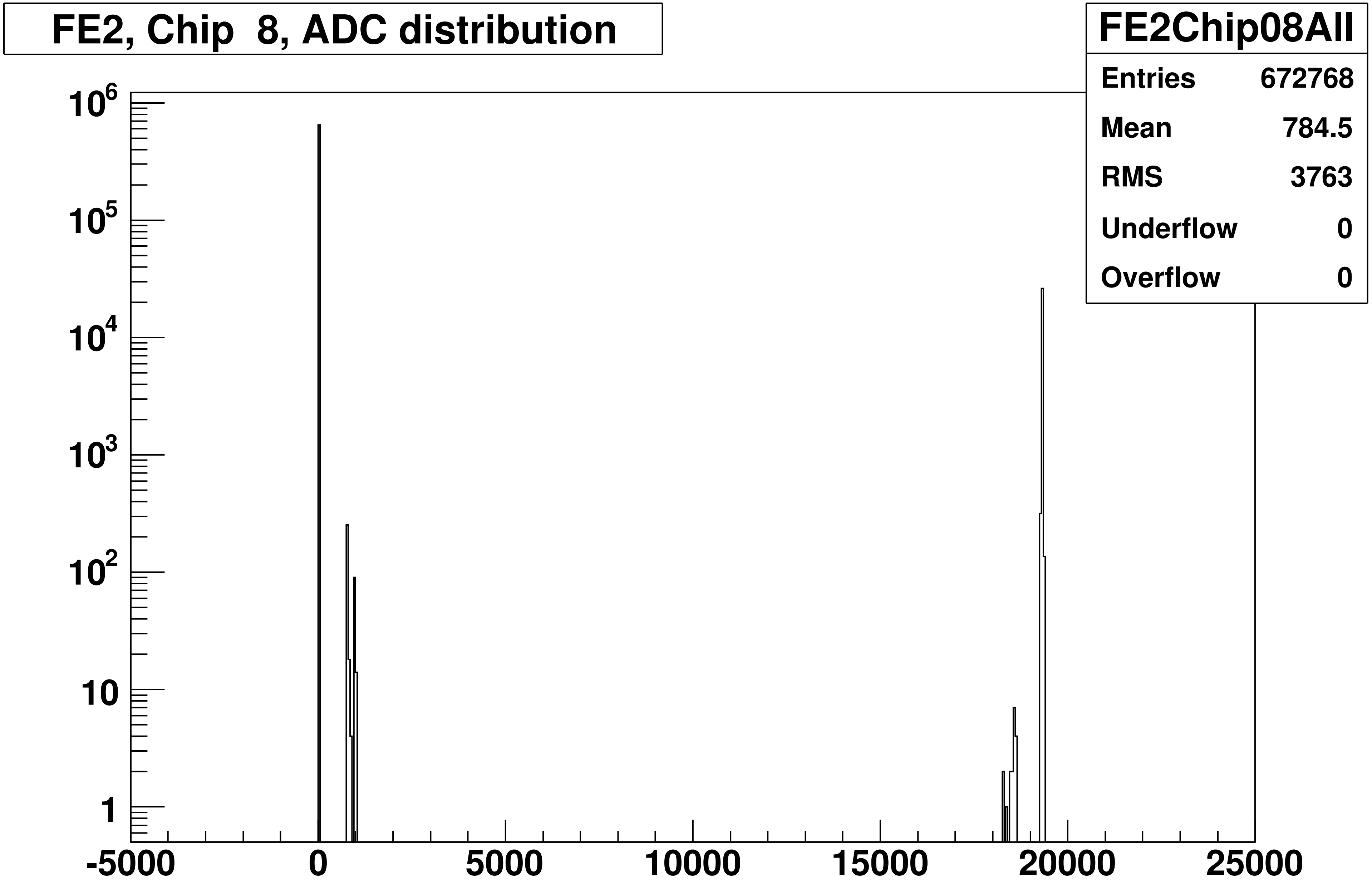
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000

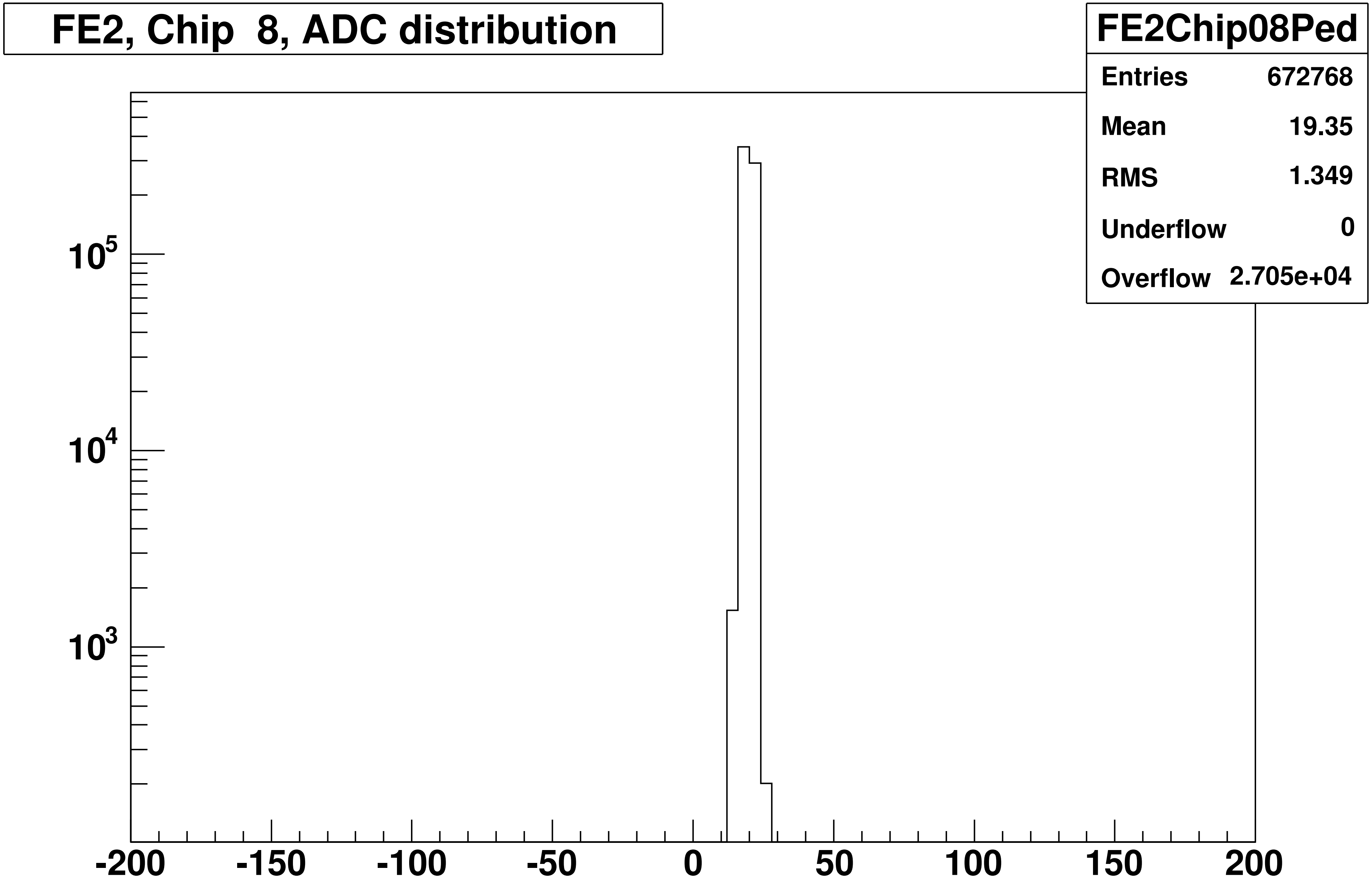


FE2, Chip 7, ADC distribution
FE2Chip07Ped
Entries 672768
Mean -31.78
RMS 1.435
Underflow 0
Overflow 2.671e+04
10^5
10^4
10^3
10^2
10
1
-200 -150 -100 -50 0 50 100 150 200

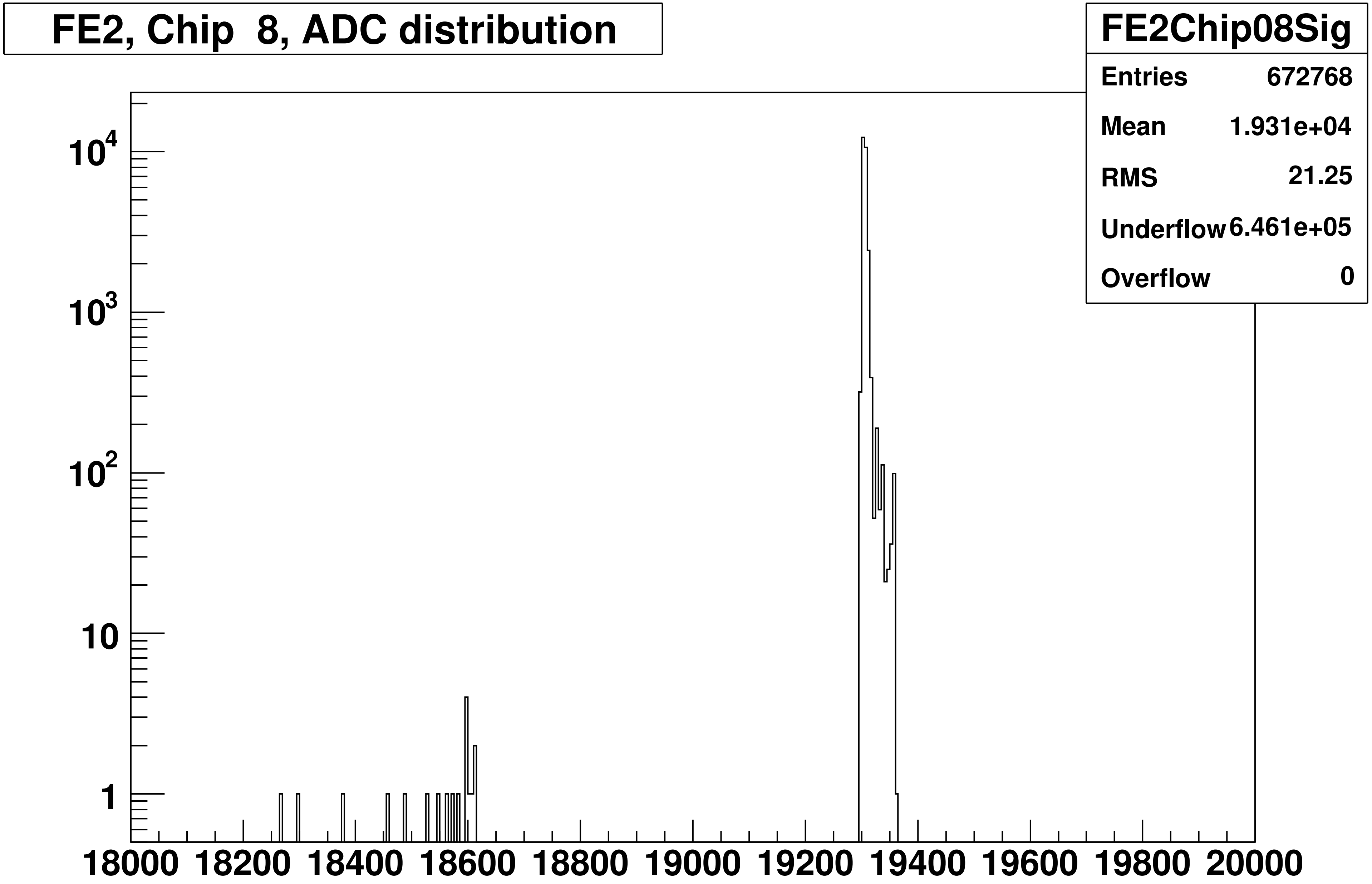


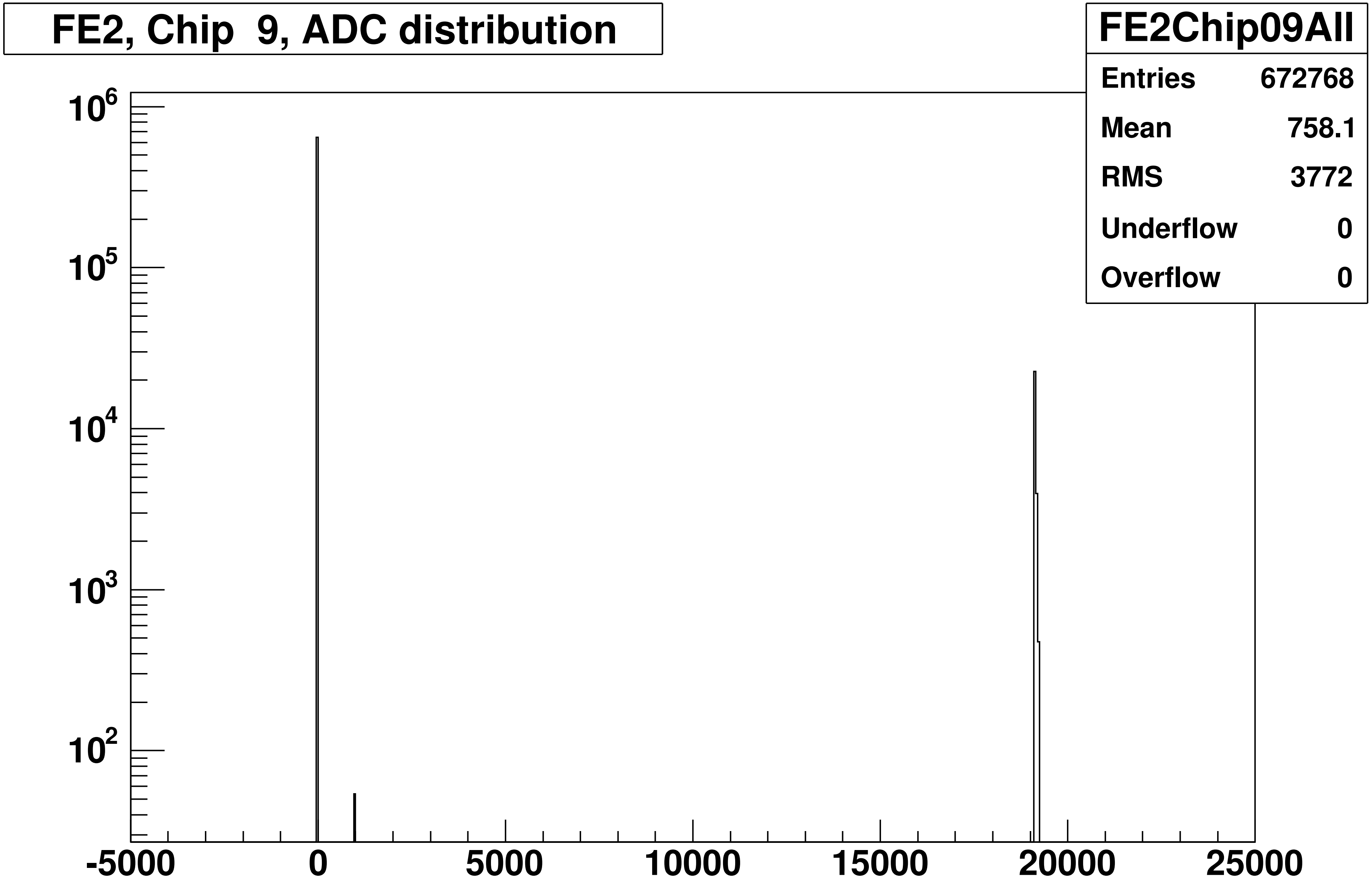
FE2, Chip 7, ADC distribution
FE2Chip07Sig
Entries 672768
Mean 1.914e+04
RMS 15.56
Underflow 6.463e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE2, Chip 8, ADC distribution
FE2Chip08All
Entries 672768
Mean 784.5
RMS 3763
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000

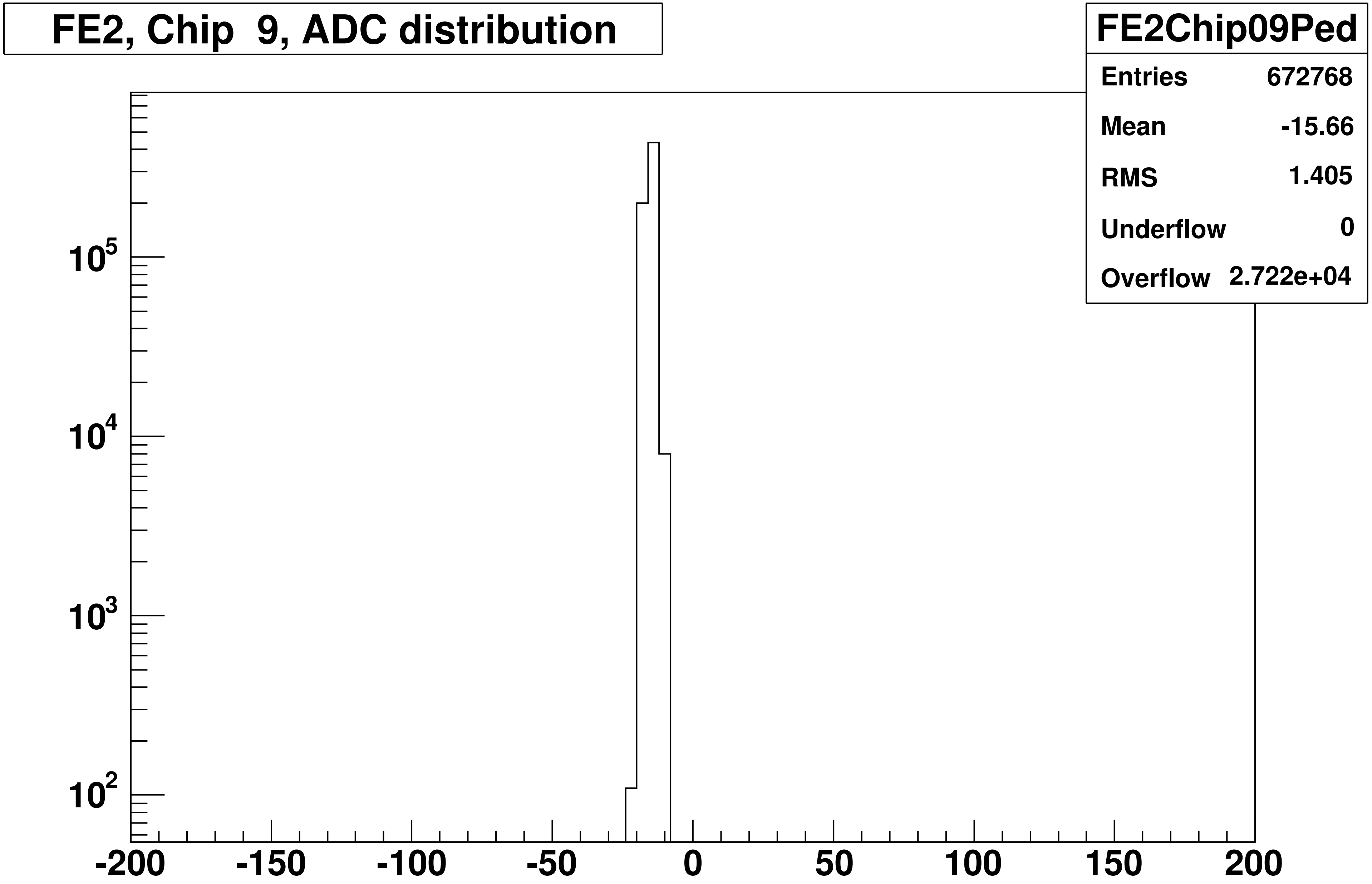


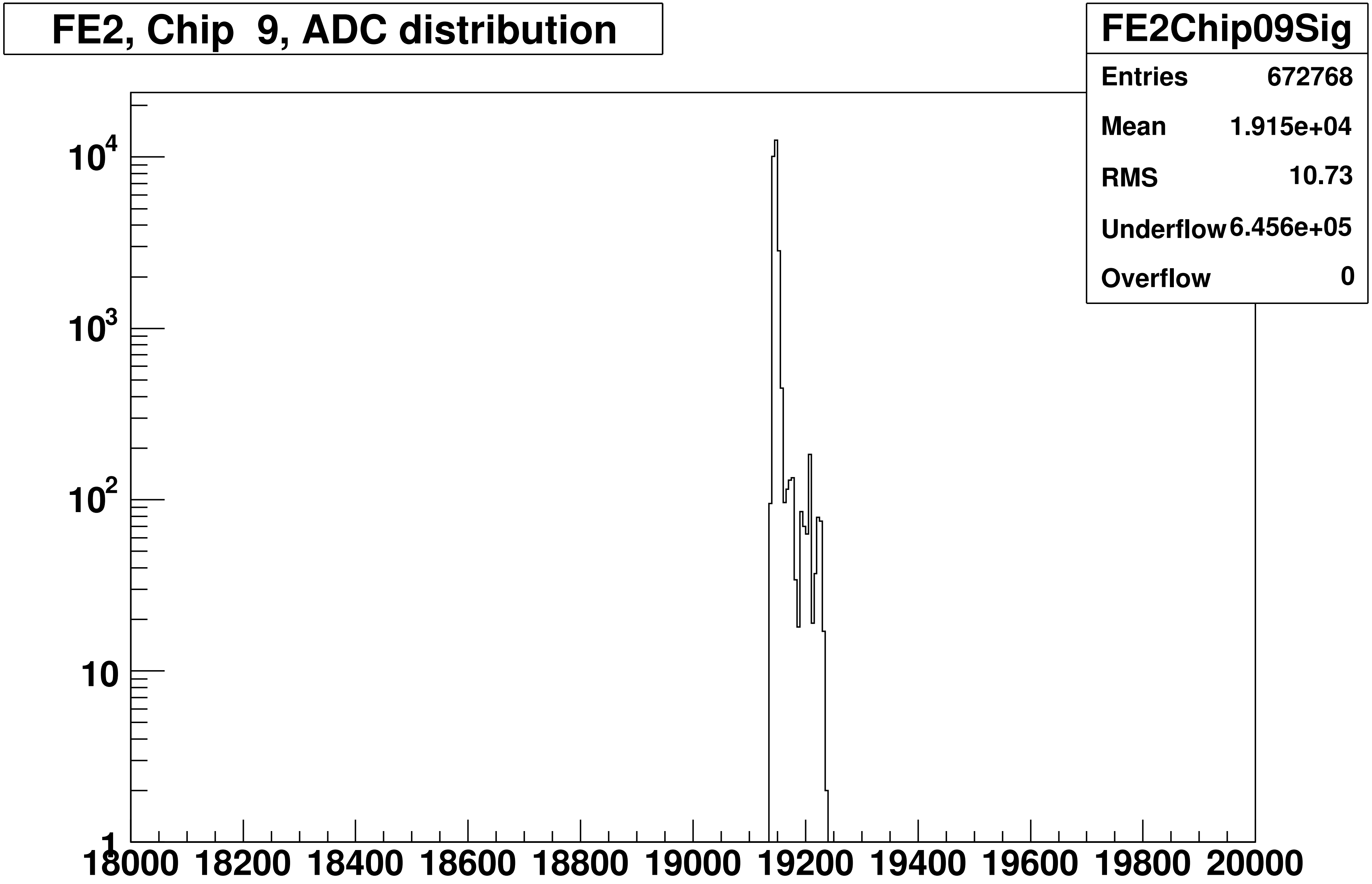
FE2, Chip 8, ADC distribution
FE2Chip08Ped
Entries 672768
Mean 19.35
RMS 1.349
Underflow 0
Overflow 2.705e+04
10^5
10^4
10^3
-200
-150
-100
-50
0
50
100
150
200


FE2, Chip 8, ADC distribution
FE2Chip08Sig
Entries 672768
Mean 1.931e+04
RMS 21.25
Underflow 6.461e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000

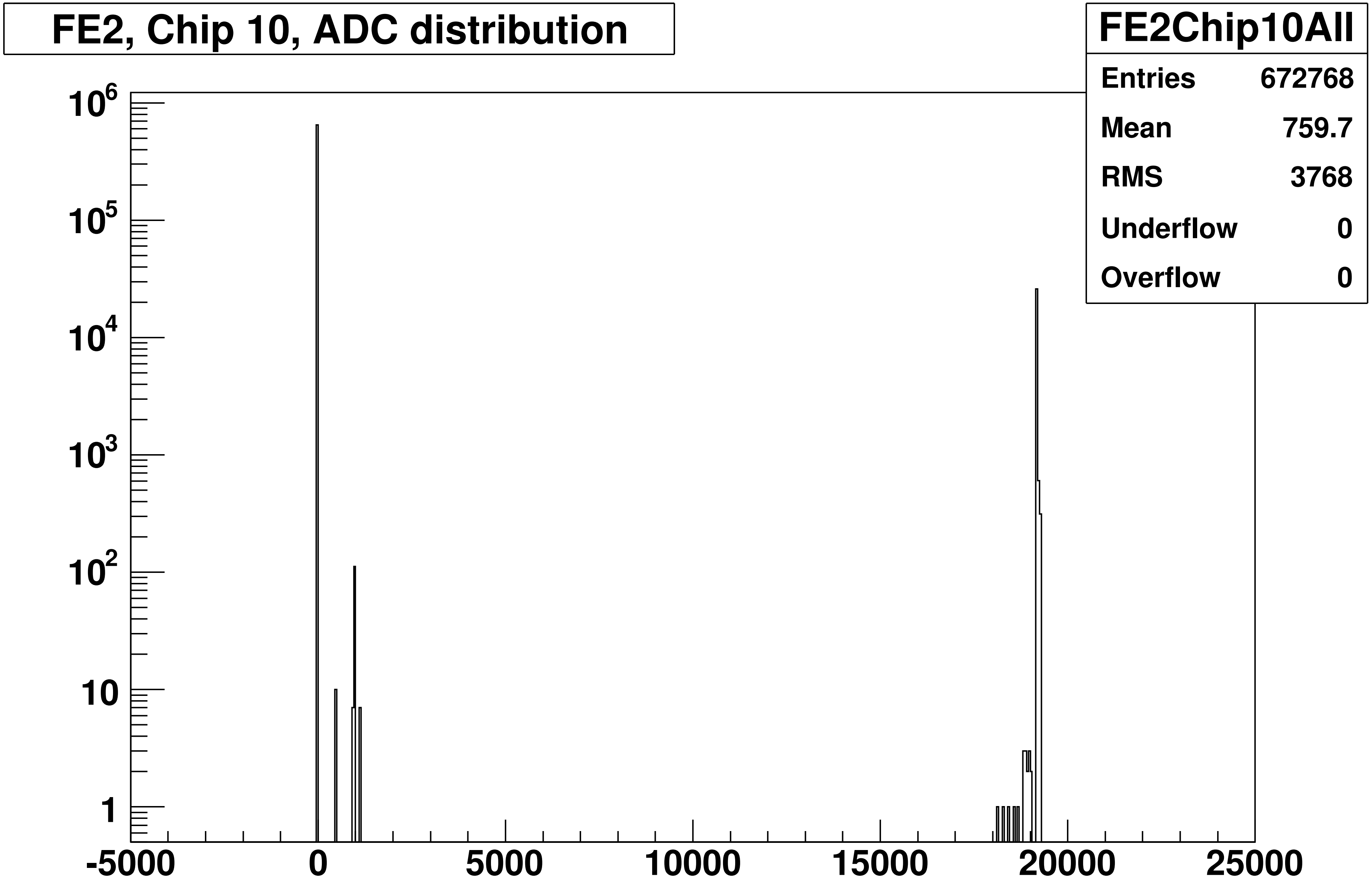


FE2, Chip 9, ADC distribution
FE2Chip09All
Entries 672768
Mean 758.1
RMS 3772
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000

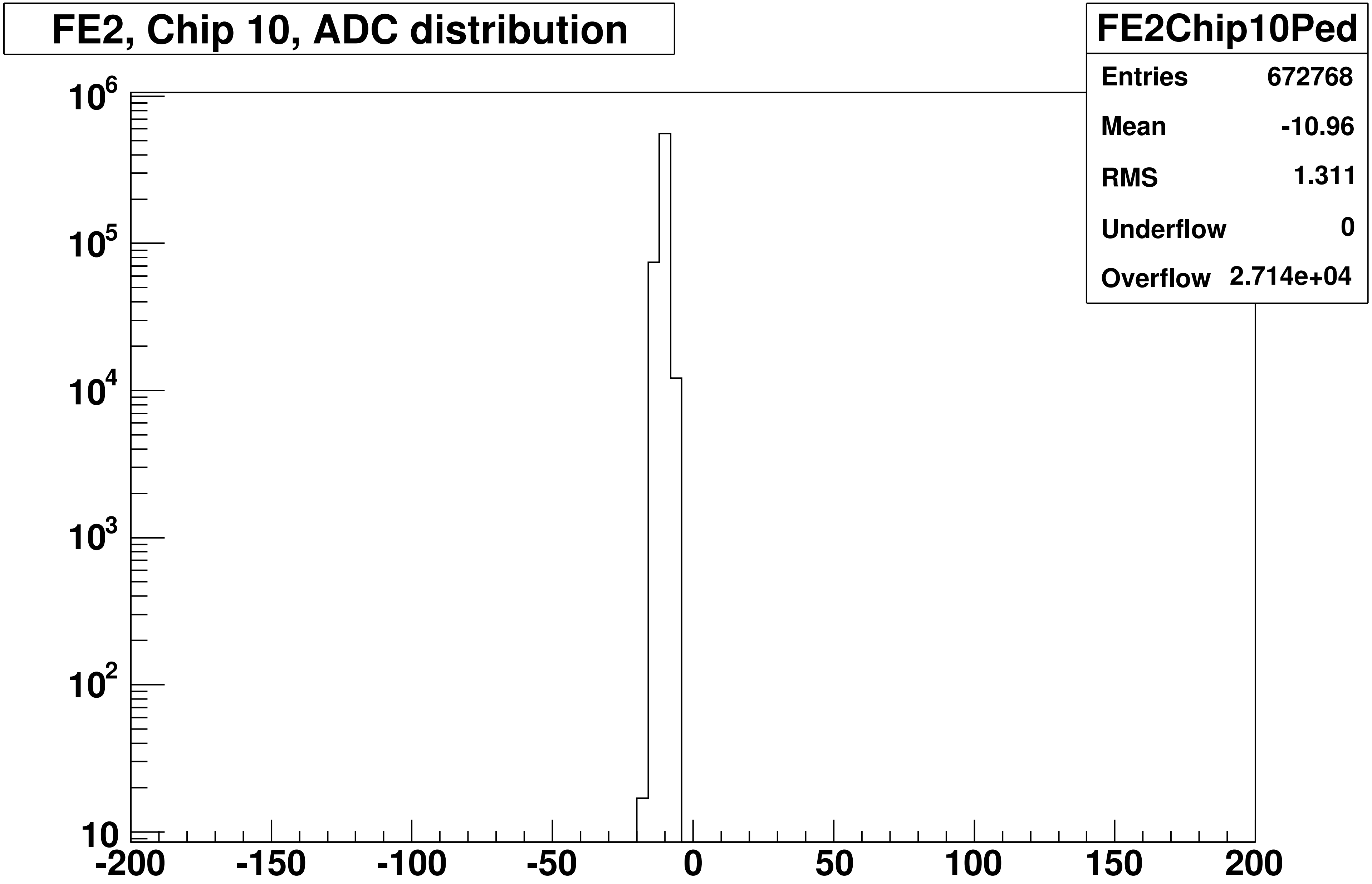

FE2, Chip 9, ADC distribution
FE2Chip09Ped
Entries 672768
Mean -15.66
RMS 1.405
Underflow 0
Overflow 2.722e+04
10^5
10^4
10^3
10^2
-200 -150 -100 -50 0 50 100 150 200



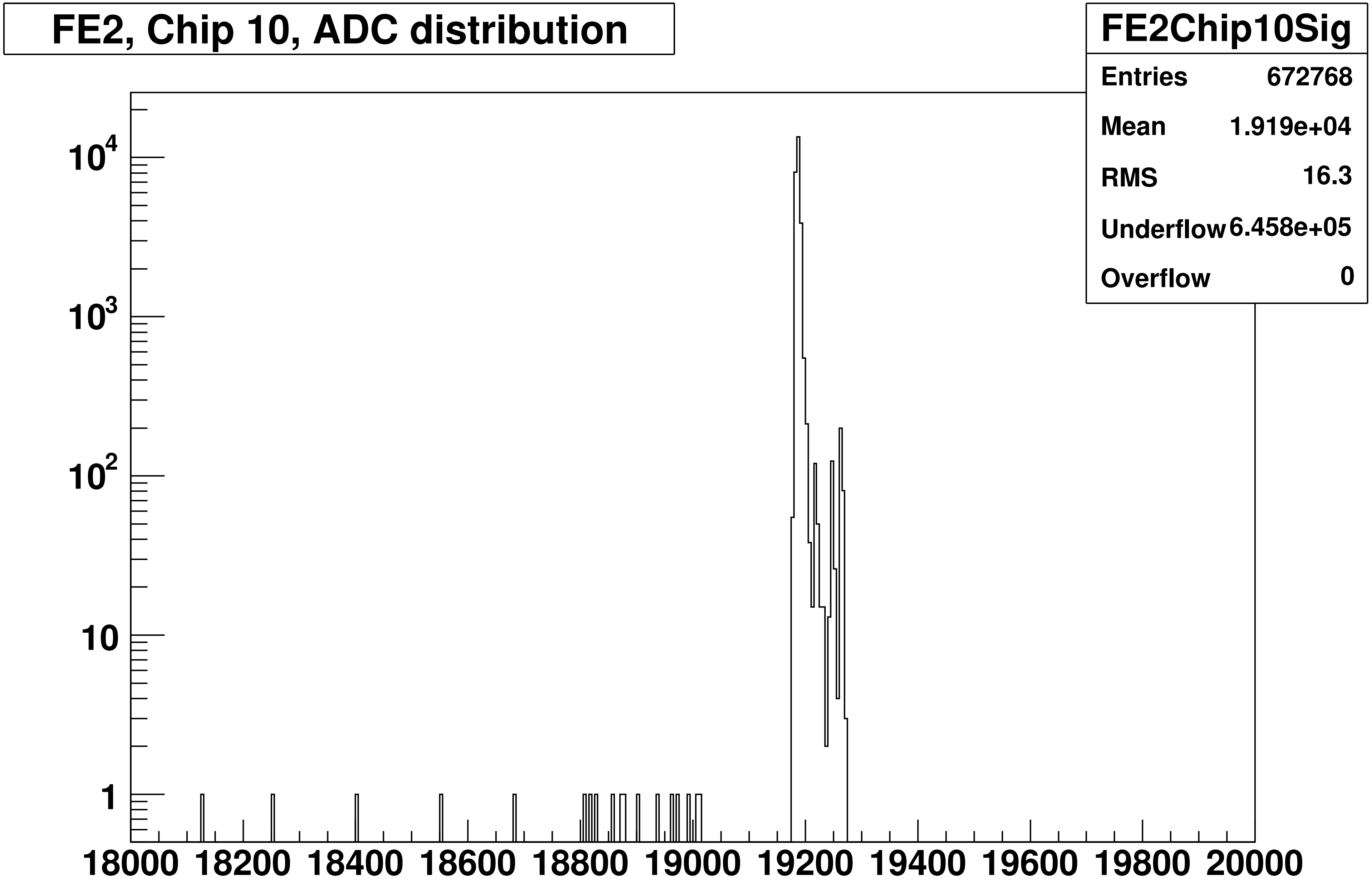
FE2, Chip 9, ADC distribution
FE2Chip09Sig
Entries 672768
Mean 1.915e+04
RMS 10.73
Underflow 6.456e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000

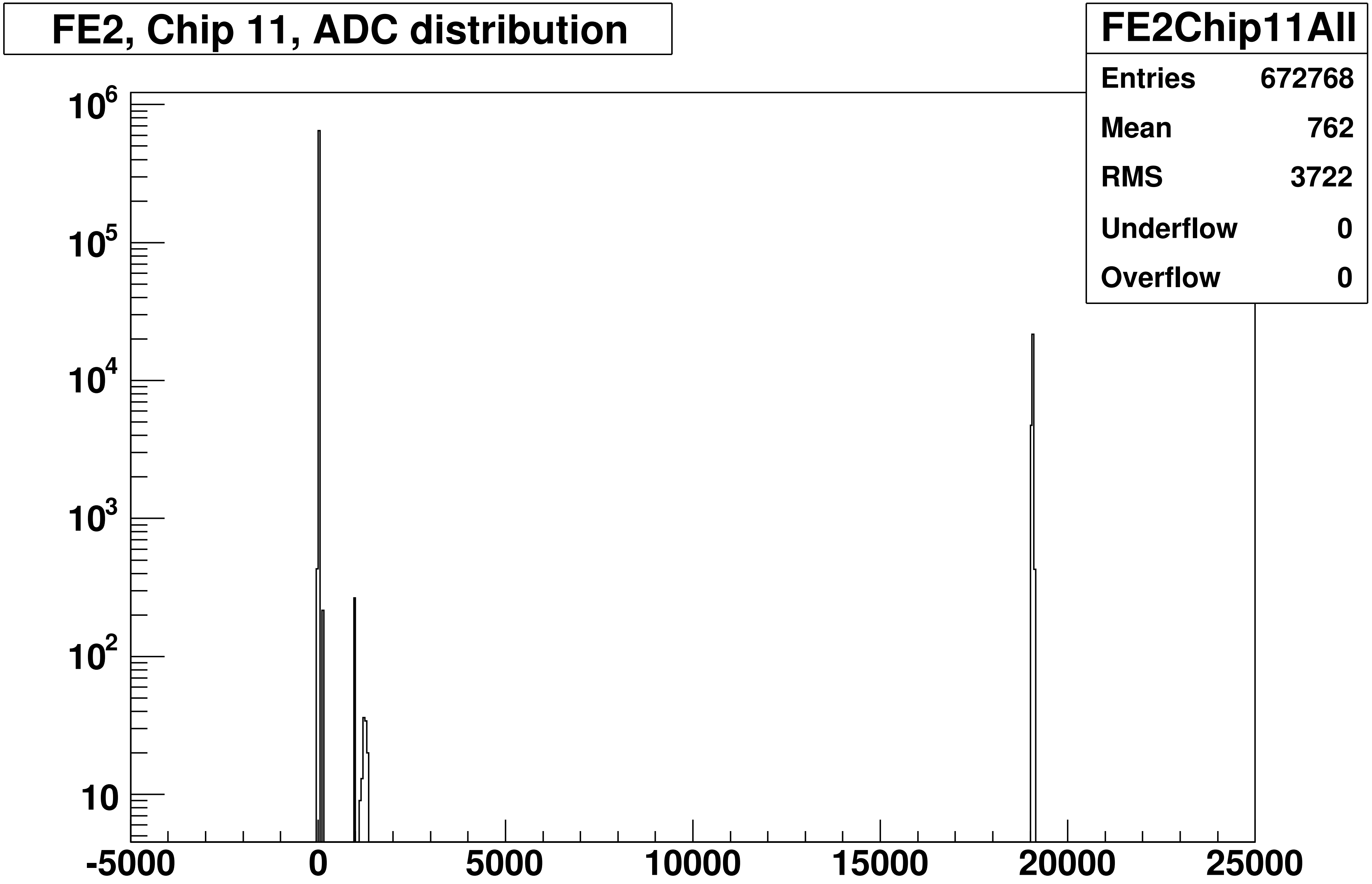


FE2, Chip 10, ADC distribution
FE2Chip10All
Entries 672768
Mean 759.7
RMS 3768
Underflow 0
Overflow 0

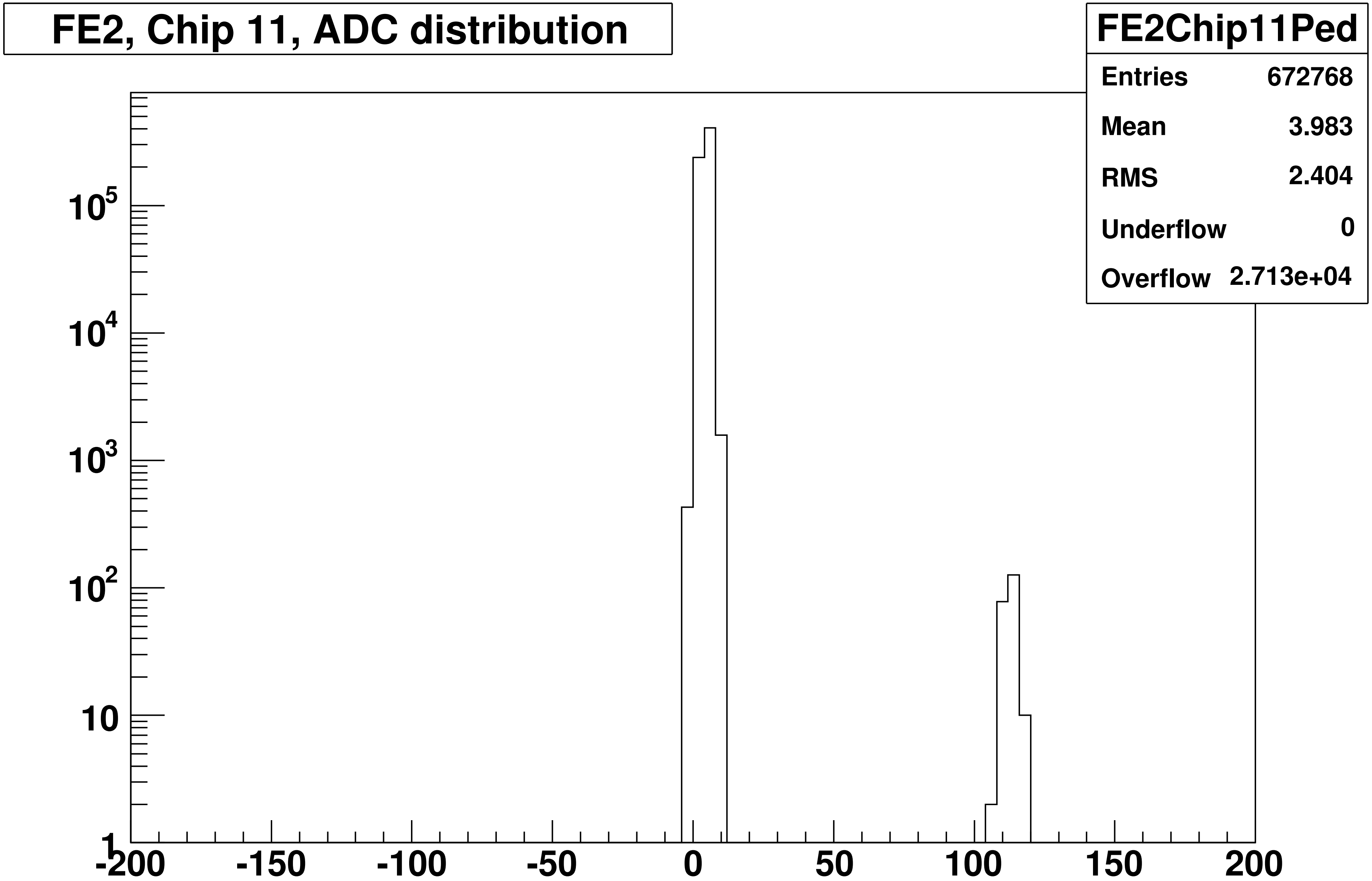


FE2, Chip 10, ADC distribution
FE2Chip10Ped
Entries 672768
Mean -10.96
RMS 1.311
Underflow 0
Overflow 2.714e+04
10^6
10^5
10^4
10^3
10^2
10
-200
-150
-100
-50
0
50
100
150
200


FE2, Chip 10, ADC distribution
FE2Chip10Sig
Entries 672768
Mean 1.919e+04
RMS 16.3
Underflow 6.458e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000



FE2, Chip 11, ADC distribution
FE2Chip11All
Entries 672768
Mean 762
RMS 3722
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000



FE2, Chip 11, ADC distribution
FE2Chip11Ped
Entries 672768
Mean 3.983
RMS 2.404
Underflow 0
Overflow 2.713e+04
1
10
10^2
10^3
10^4
10^5
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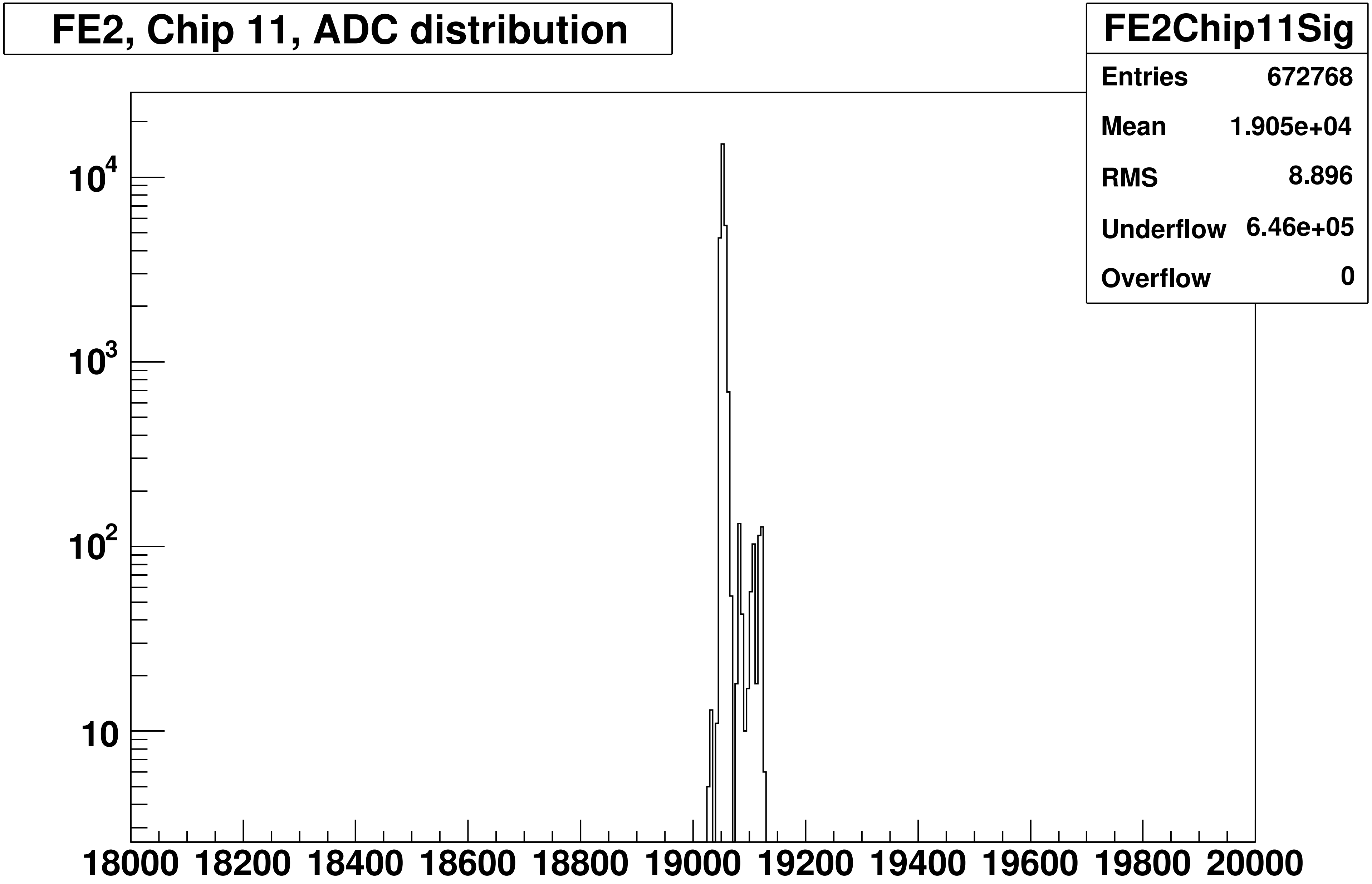
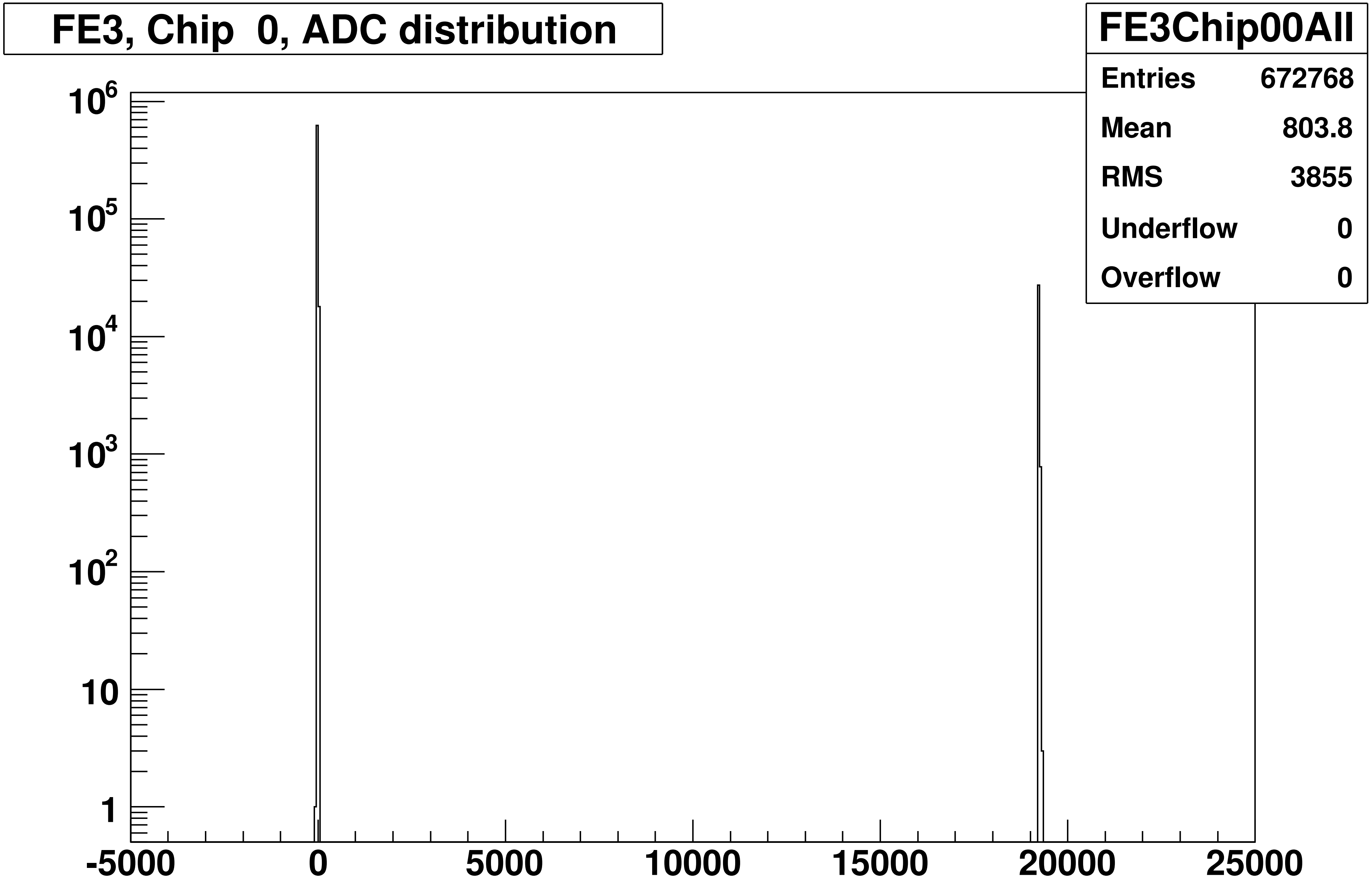
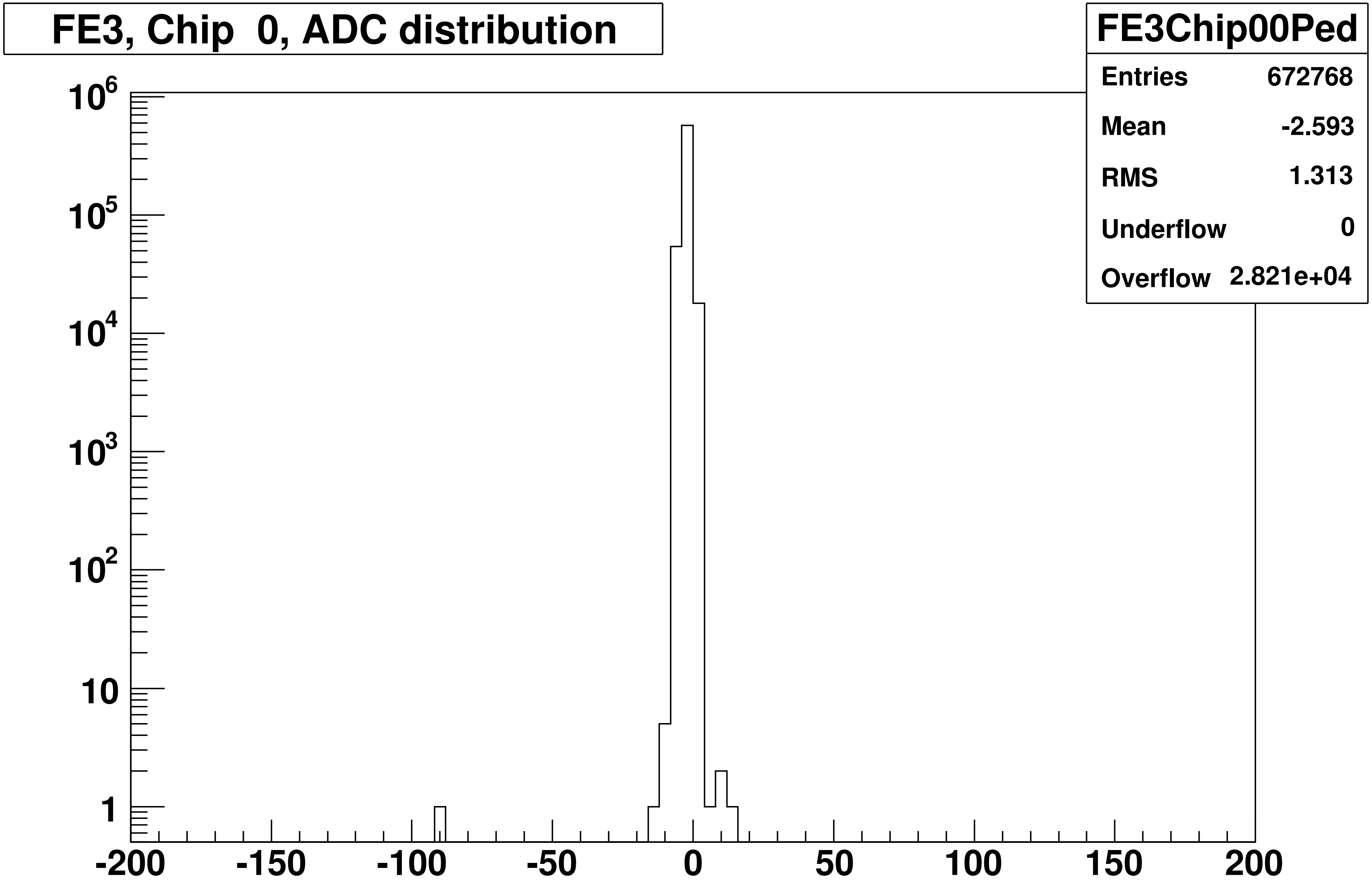
-150
-100
-50
0
50
100
150
200



FE2, Chip 11, ADC distribution
FE2Chip11Sig
Entries 672768
Mean 1.905e+04
RMS 8.896
Underflow 6.46e+05
Overflow 0
10^4
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE3, Chip 0, ADC distribution
FE3Chip00All
Entries 672768
Mean 803.8
RMS 3855
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE3, Chip 0, ADC distribution
FE3Chip00Ped
Entries 672768
Mean -2.593
RMS 1.313
Underflow 0
Overflow 2.821e+04
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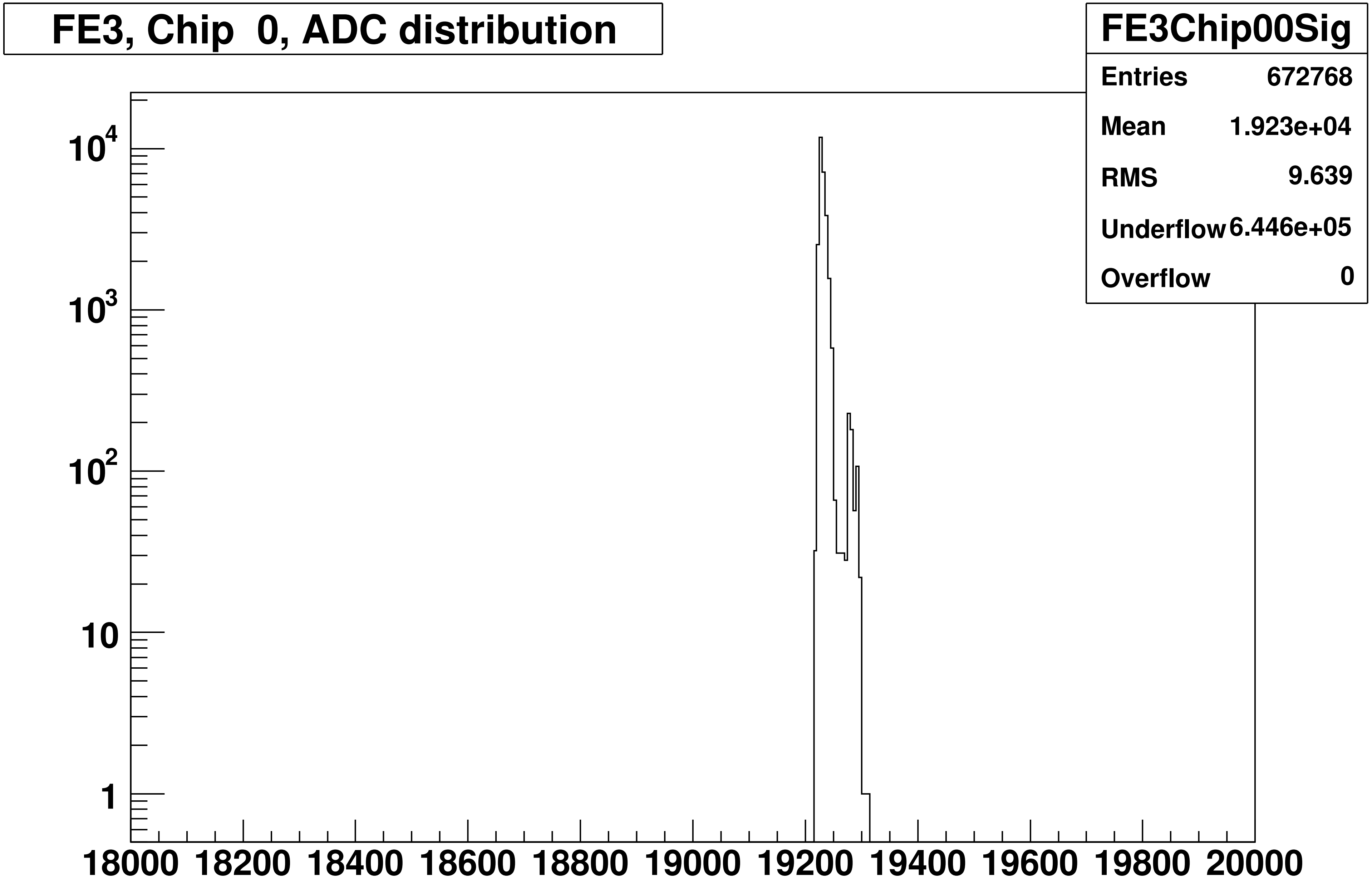
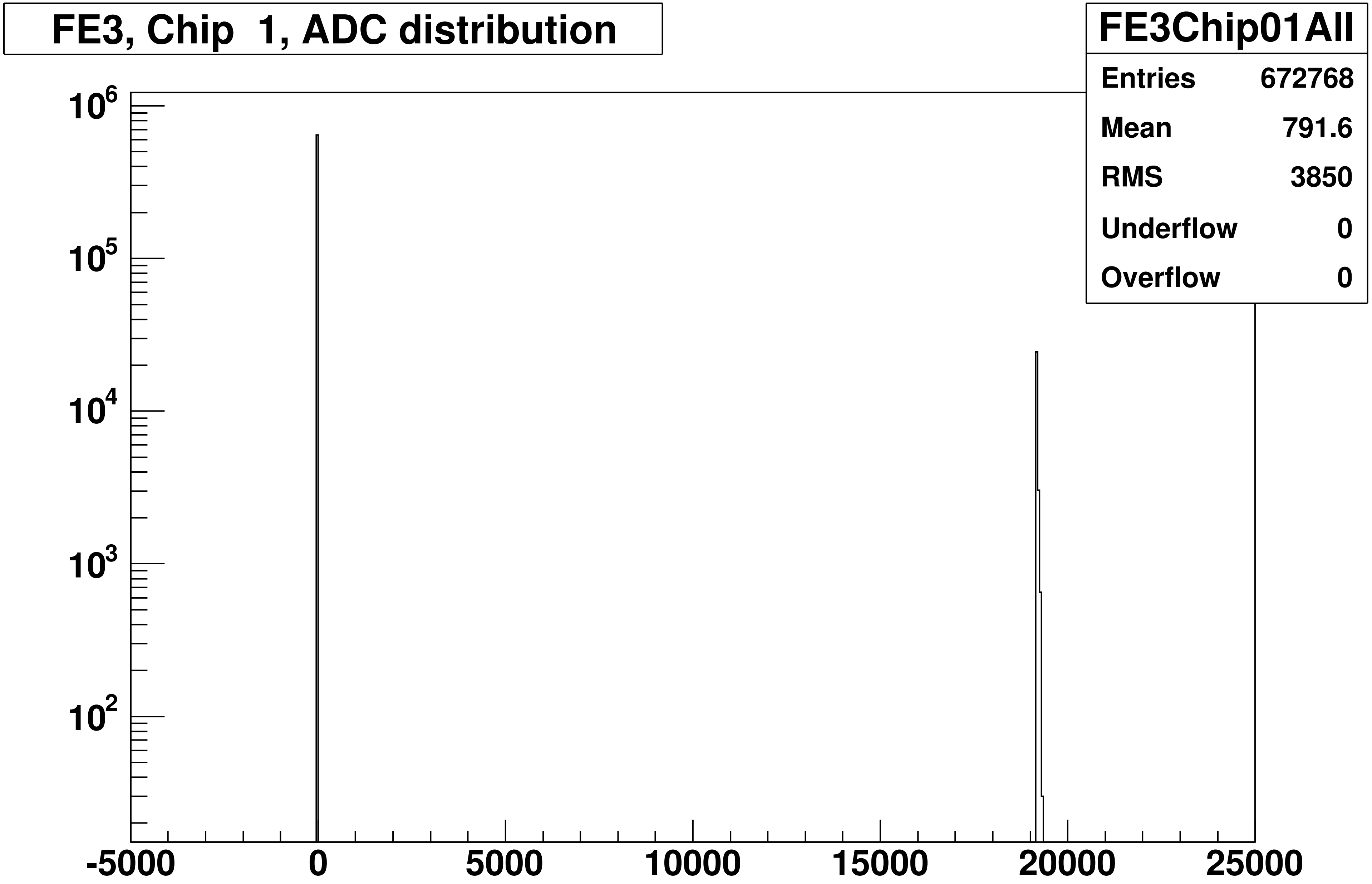
10^5
10^4
10^3
10^2
10
1
-200 -150 -100 -50 0 50 100 150 200


FE3, Chip 0, ADC distribution
FE3Chip00Sig
Entries 672768
Mean 1.923e+04
RMS 9.639
Underflow 6.446e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000


FE3, Chip 1, ADC distribution
FE3Chip01All
Entries 672768
Mean 791.6
RMS 3850
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
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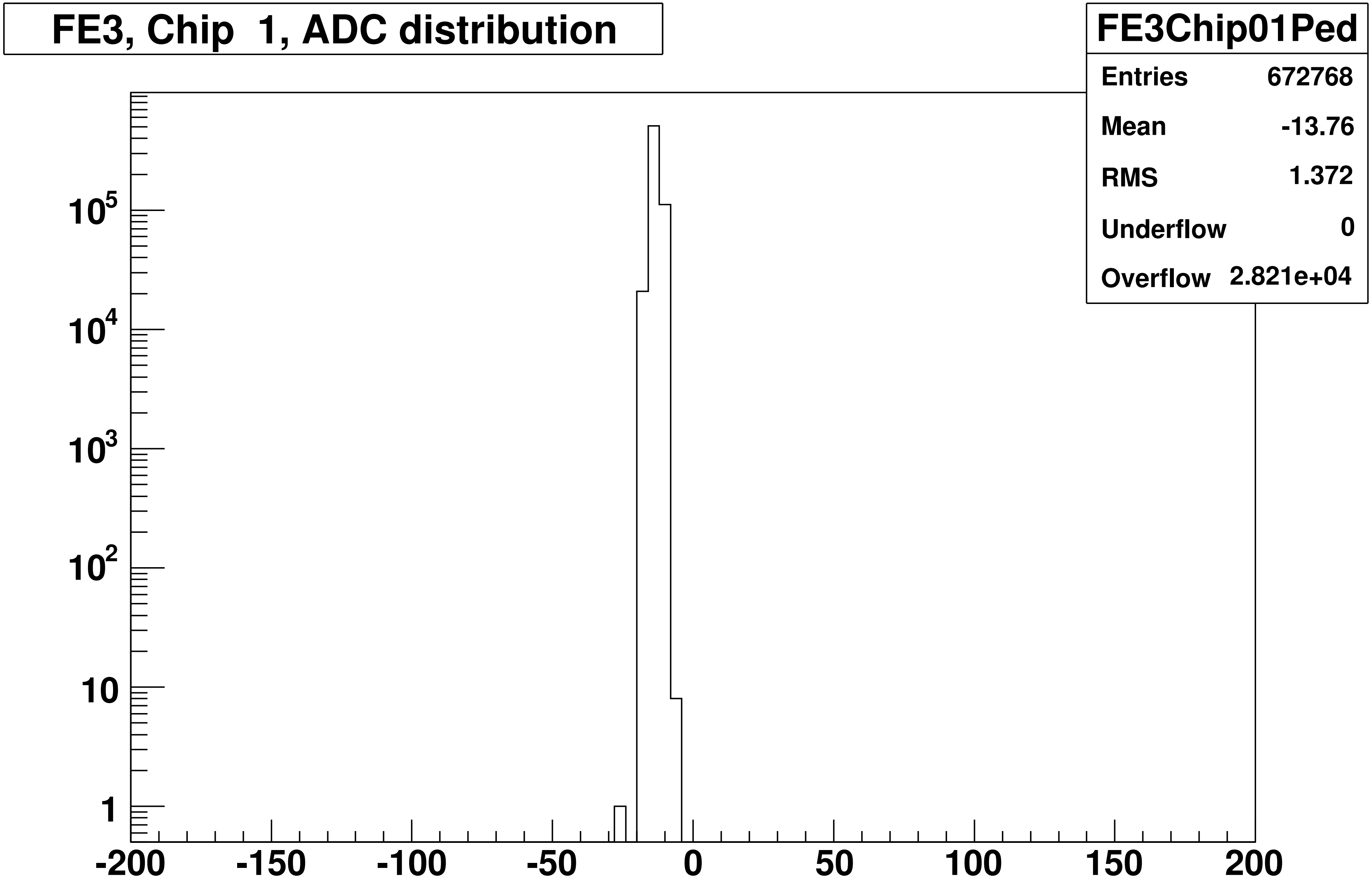
FE3, Chip 1, ADC distribution
FE3Chip01Ped
Entries 672768
Mean -13.76
RMS 1.372
Underflow 0
Overflow 2.821e+04
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10^4
10^3
10^2
10
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-100
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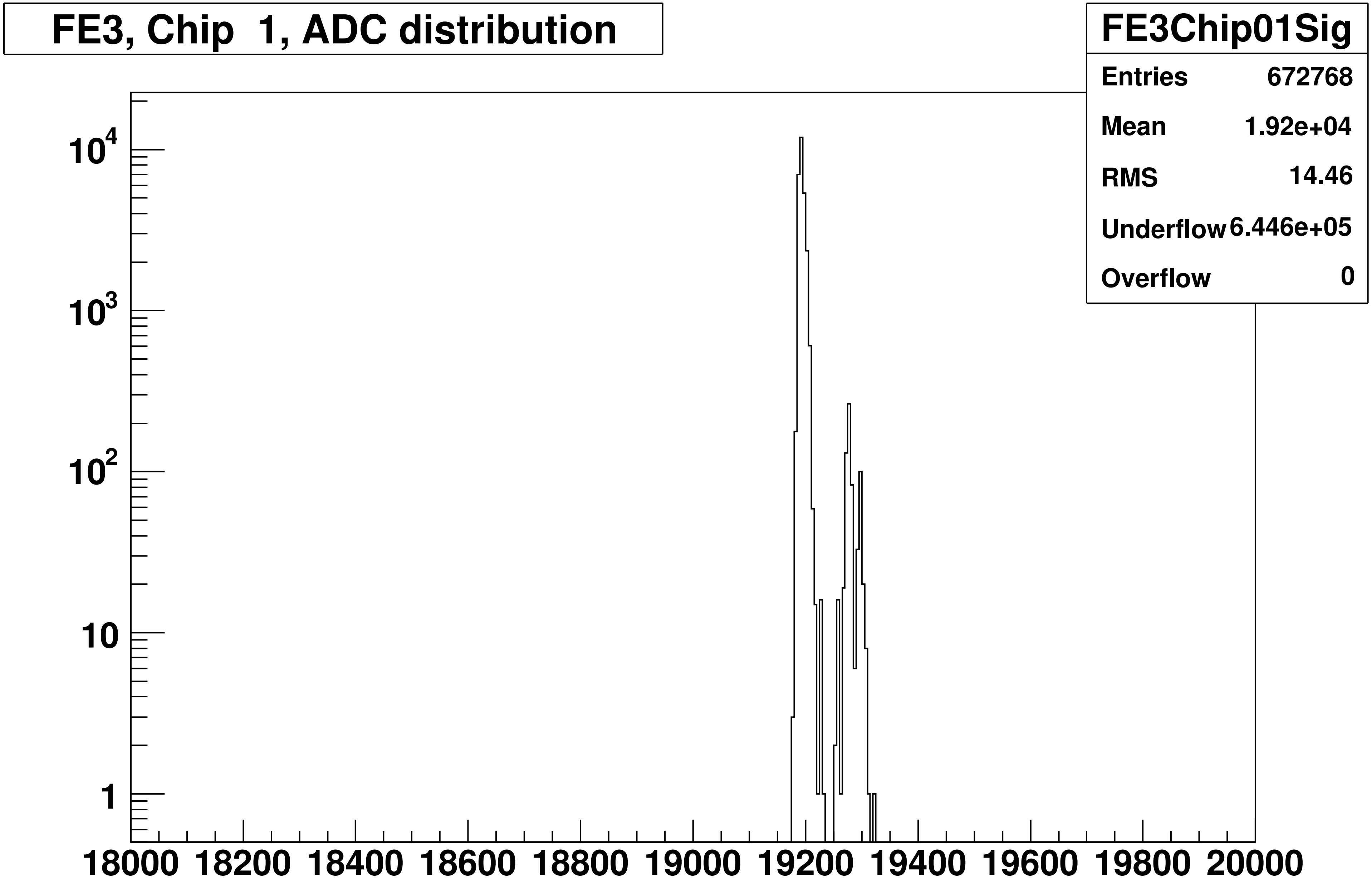
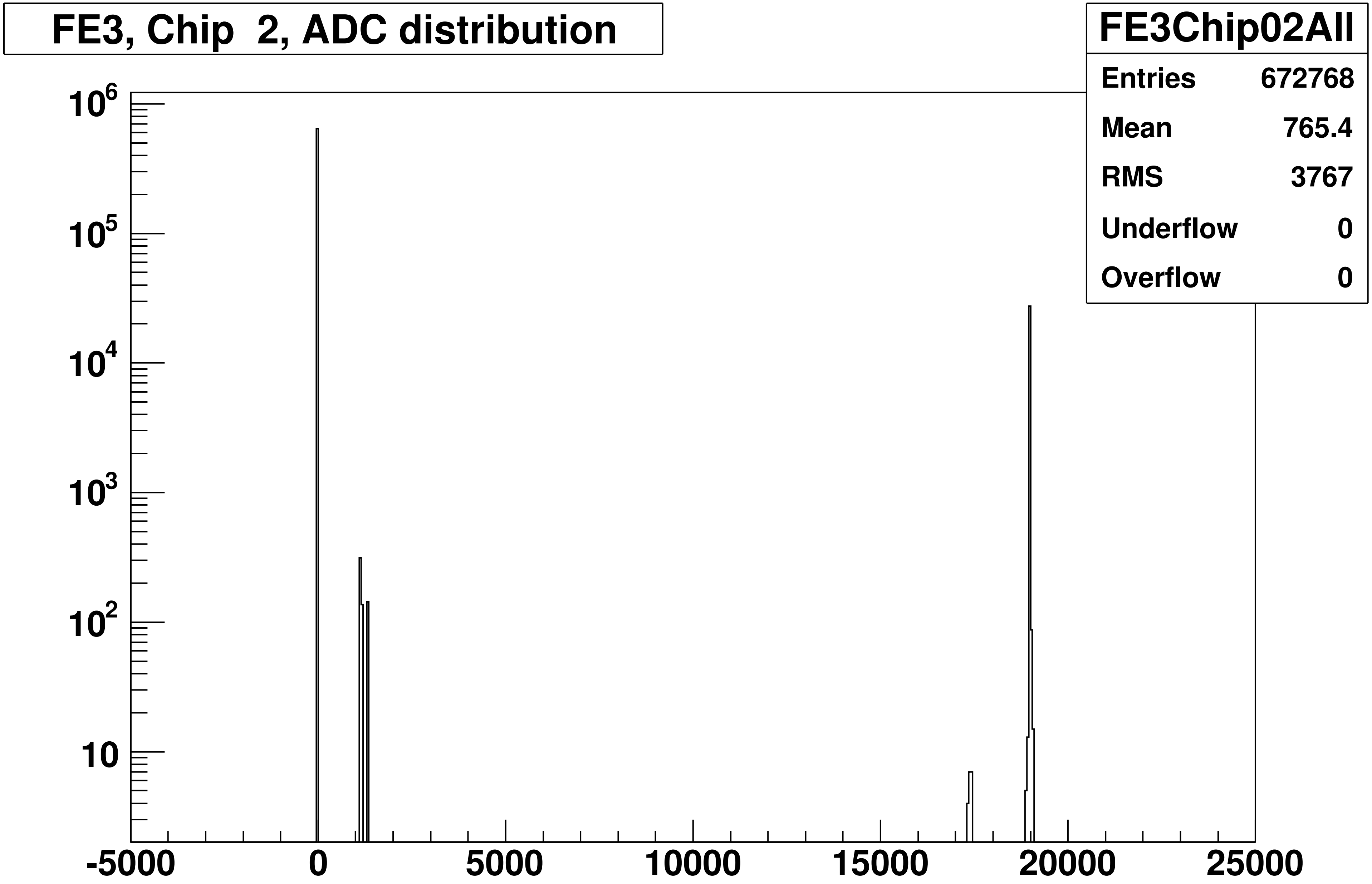
0
50
100
150
200


FE3, Chip 1, ADC distribution
FE3Chip01Sig
Entries 672768
Mean 1.92e+04
RMS 14.46
Underflow 6.446e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE3, Chip 2, ADC distribution
FE3Chip02All
Entries 672768
Mean 765.4
RMS 3767
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
-5000
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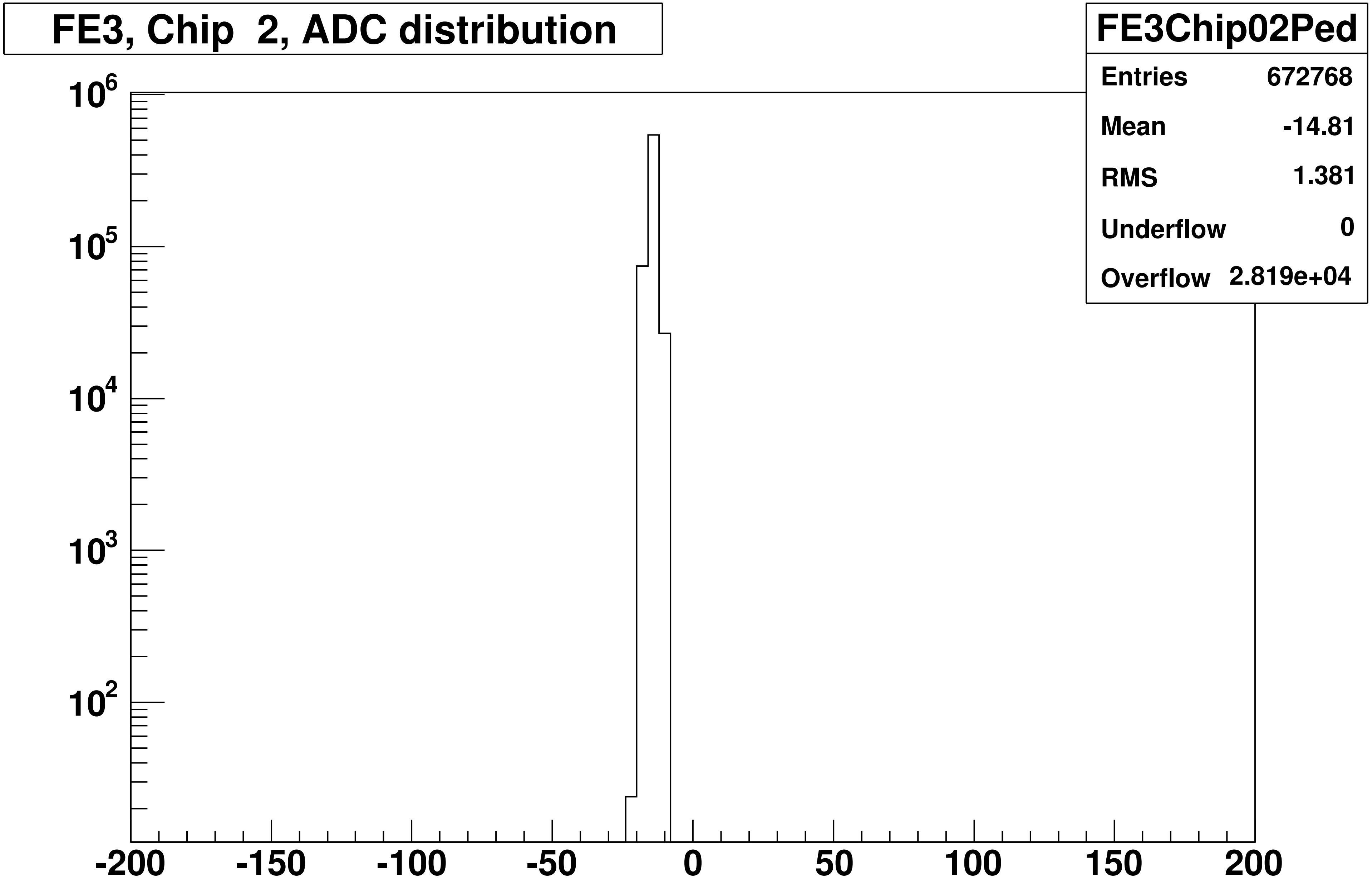
FE3, Chip 2, ADC distribution
FE3Chip02Ped
Entries 672768
Mean -14.81
RMS 1.381
Underflow 0
Overflow 2.819e+04
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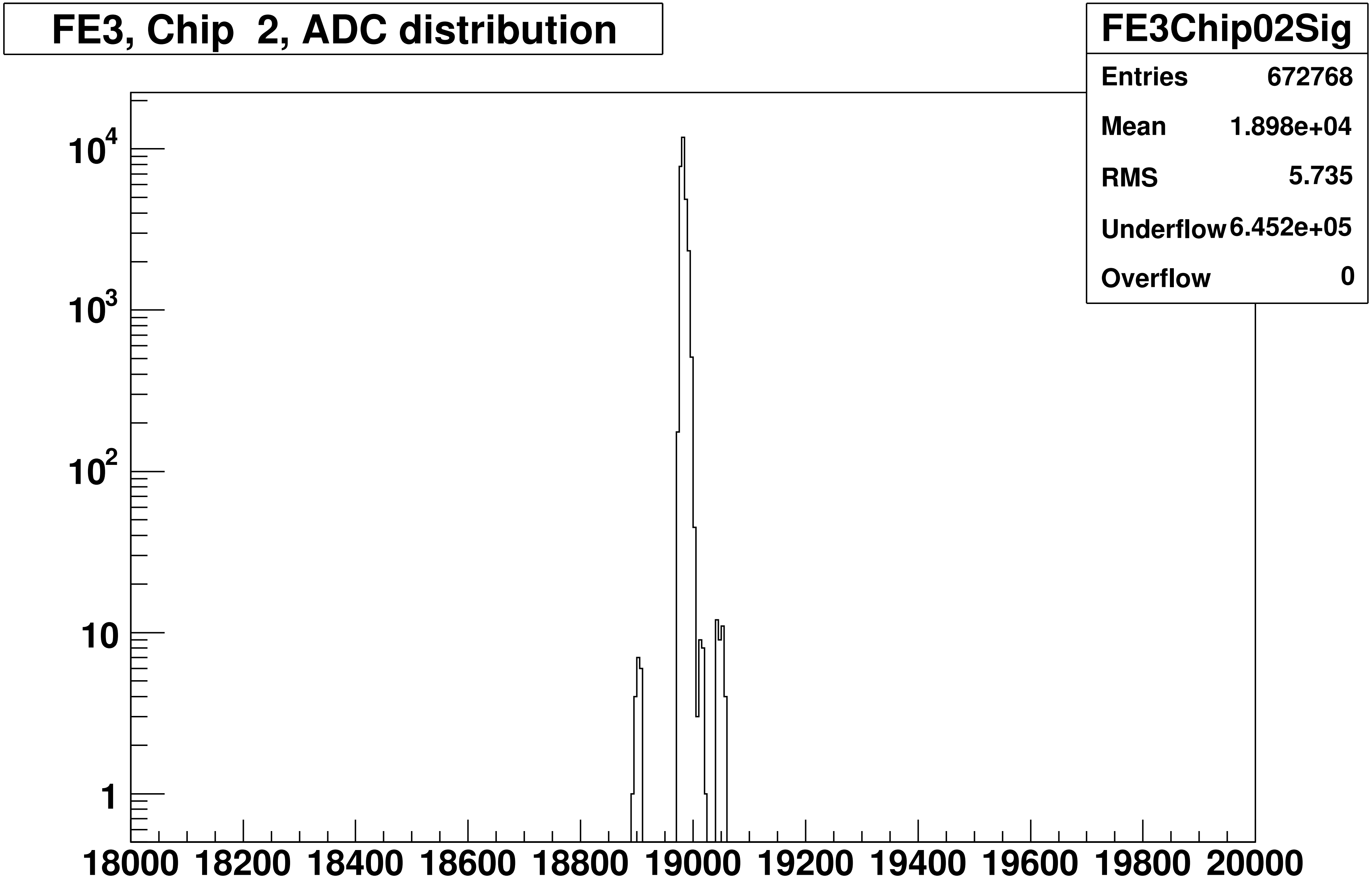
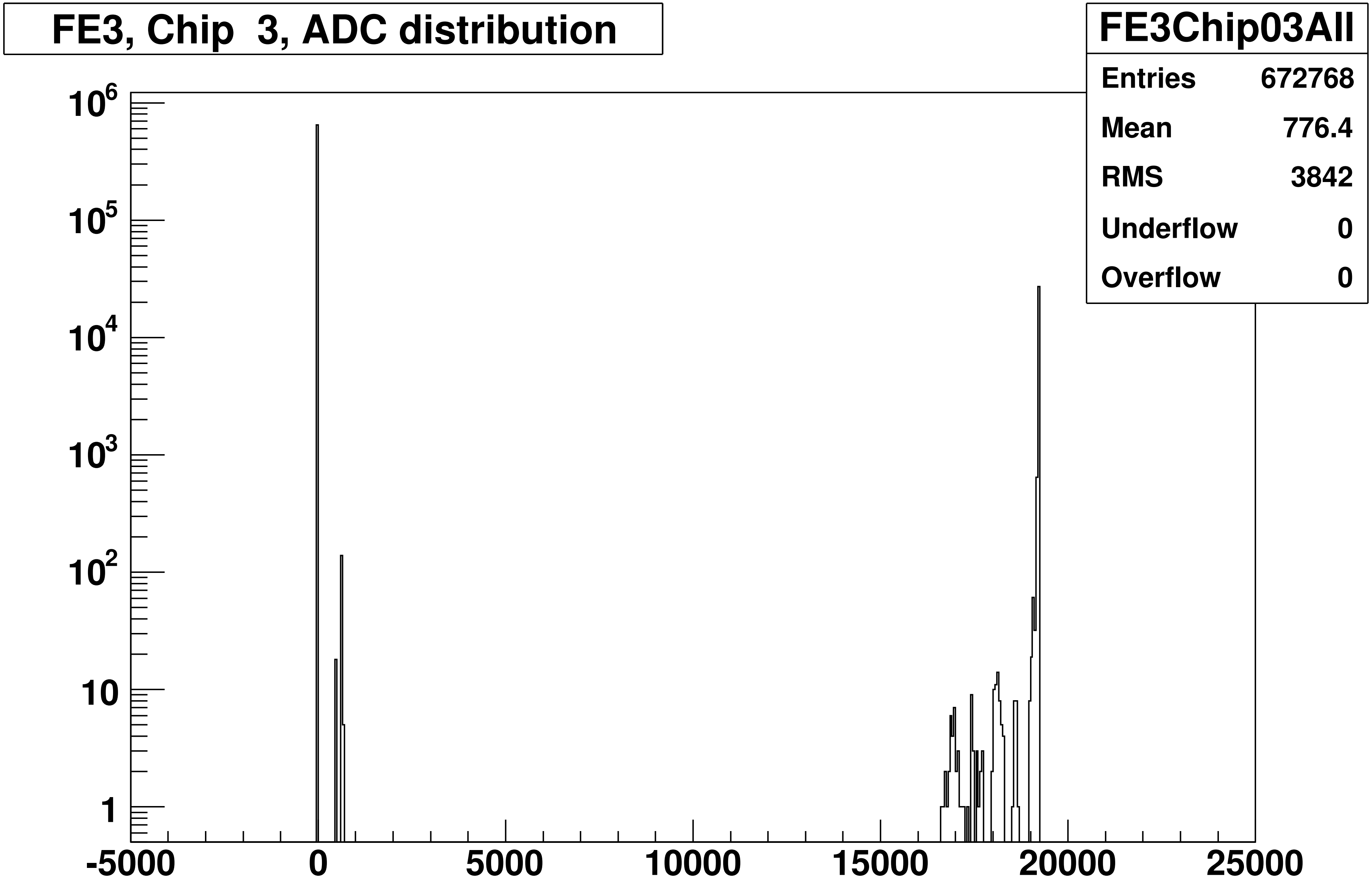
10^5
10^4
10^3
10^2
-200 -150 -100 -50 0 50 100 150 200



FE3, Chip 2, ADC distribution
FE3Chip02Sig
Entries 672768
Mean 1.898e+04
RMS 5.735
Underflow 6.452e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE3, Chip 3, ADC distribution
FE3Chip03All
Entries 672768
Mean 776.4
RMS 3842
Underflow 0
Overflow 0
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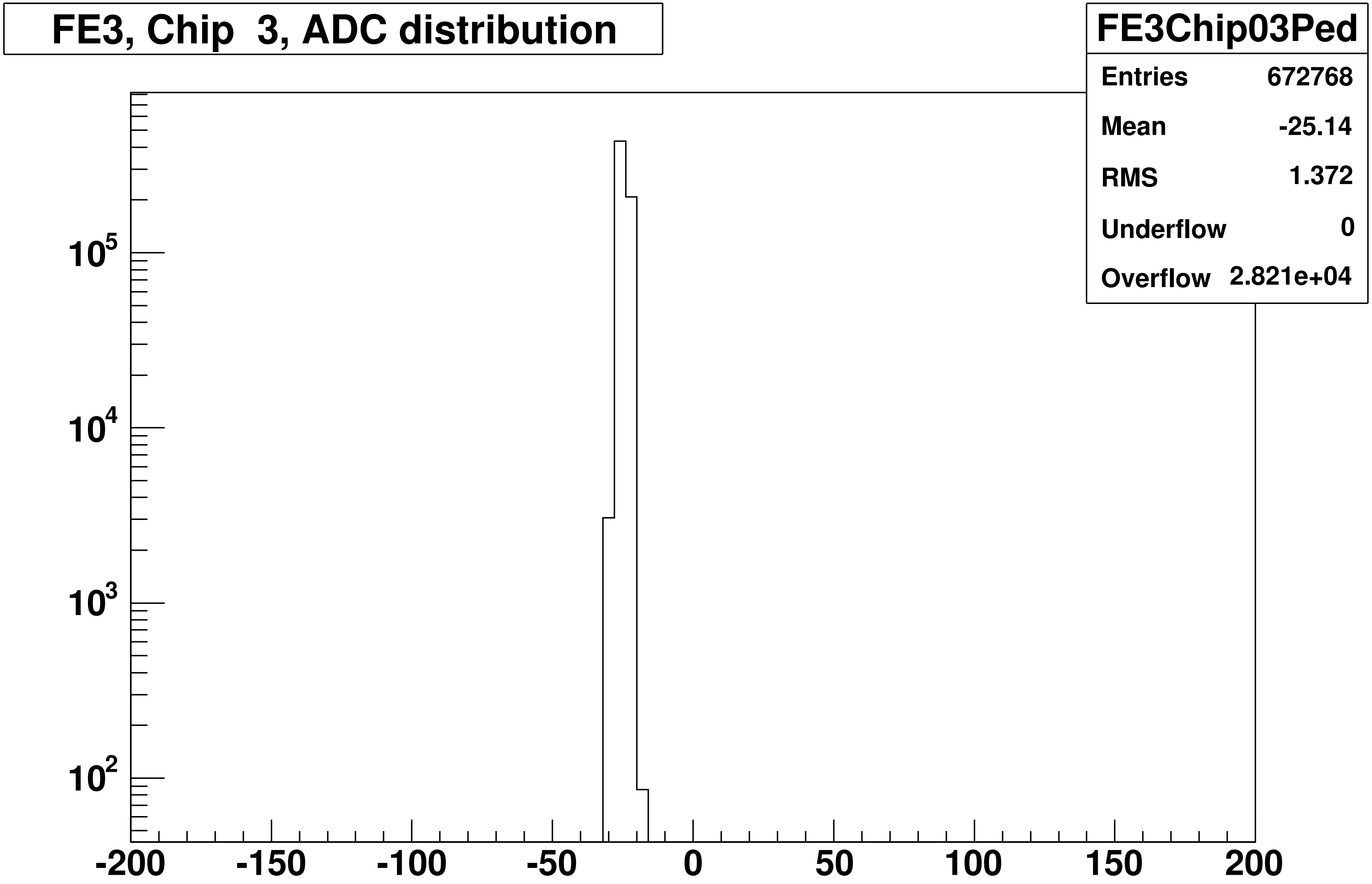
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE3, Chip 3, ADC distribution
FE3Chip03Ped
Entries 672768
Mean -25.14
RMS 1.372
Underflow 0
Overflow 2.821e+04
10^5
10^4
10^3
10^2
-200
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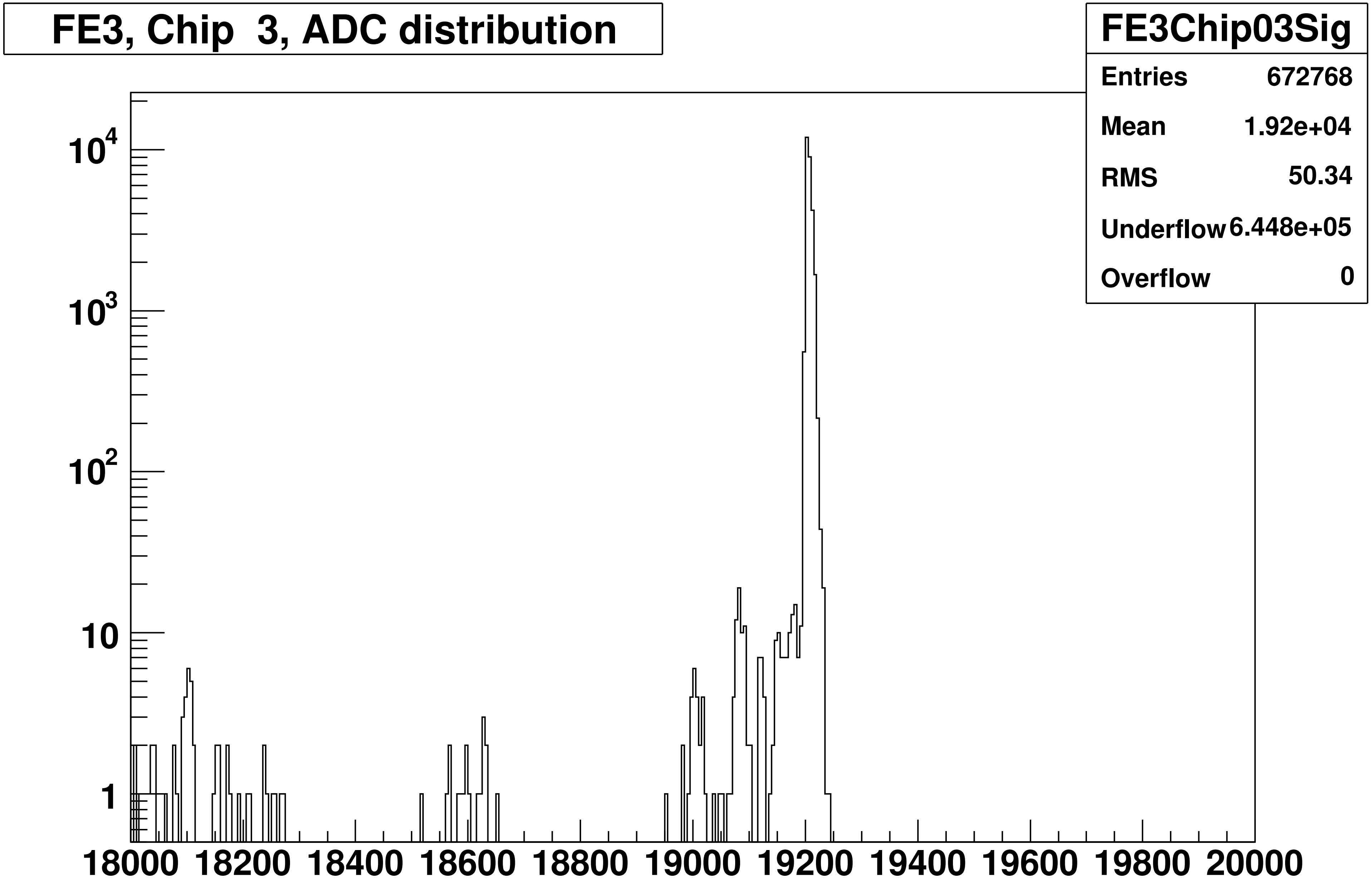
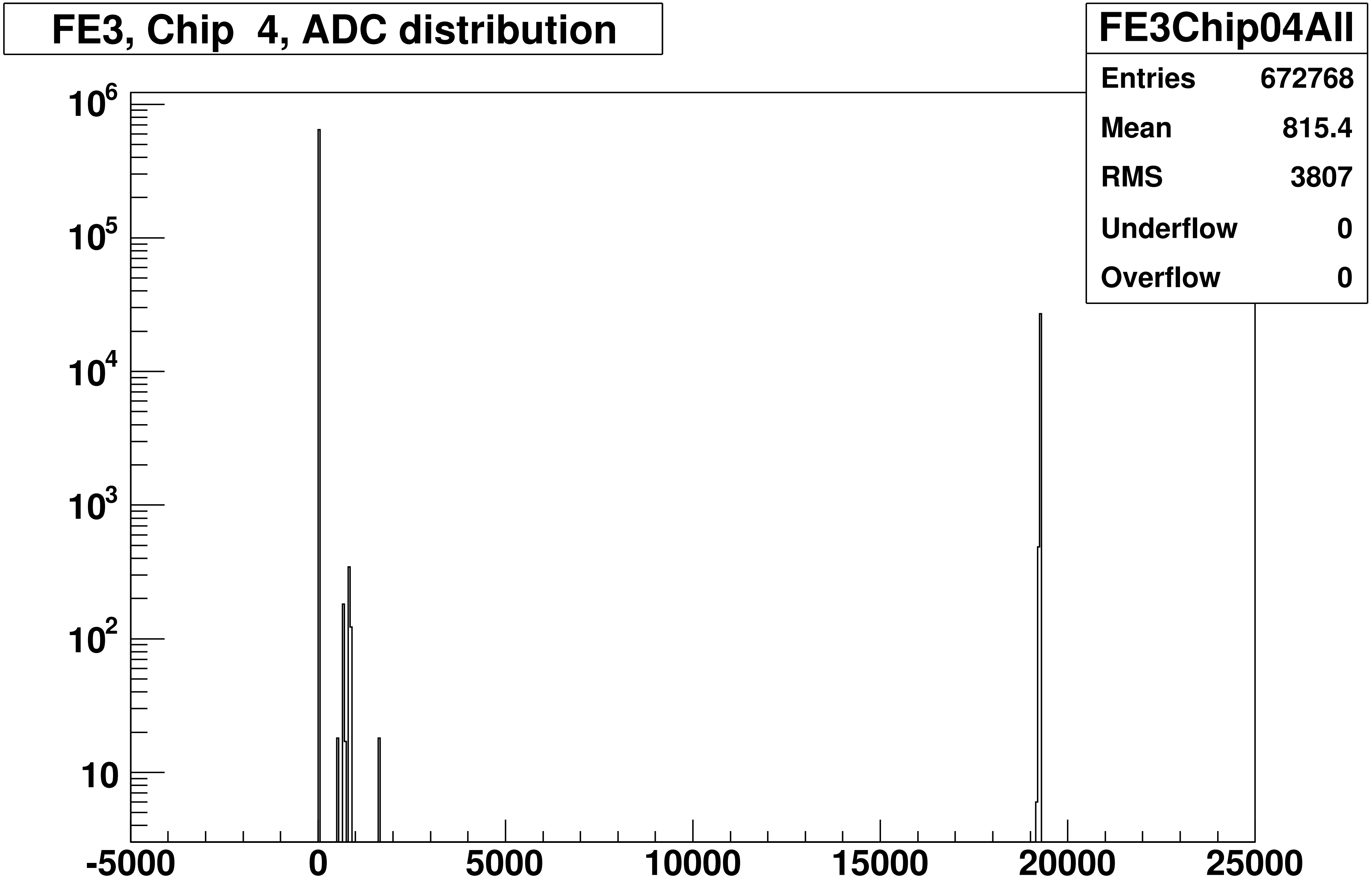
-100
-50
0
50
100
150
200


FE3, Chip 3, ADC distribution
FE3Chip03Sig
Entries 672768
Mean 1.92e+04
RMS 50.34
Underflow 6.448e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000


FE3, Chip 4, ADC distribution
FE3Chip04All
Entries 672768
Mean 815.4
RMS 3807
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
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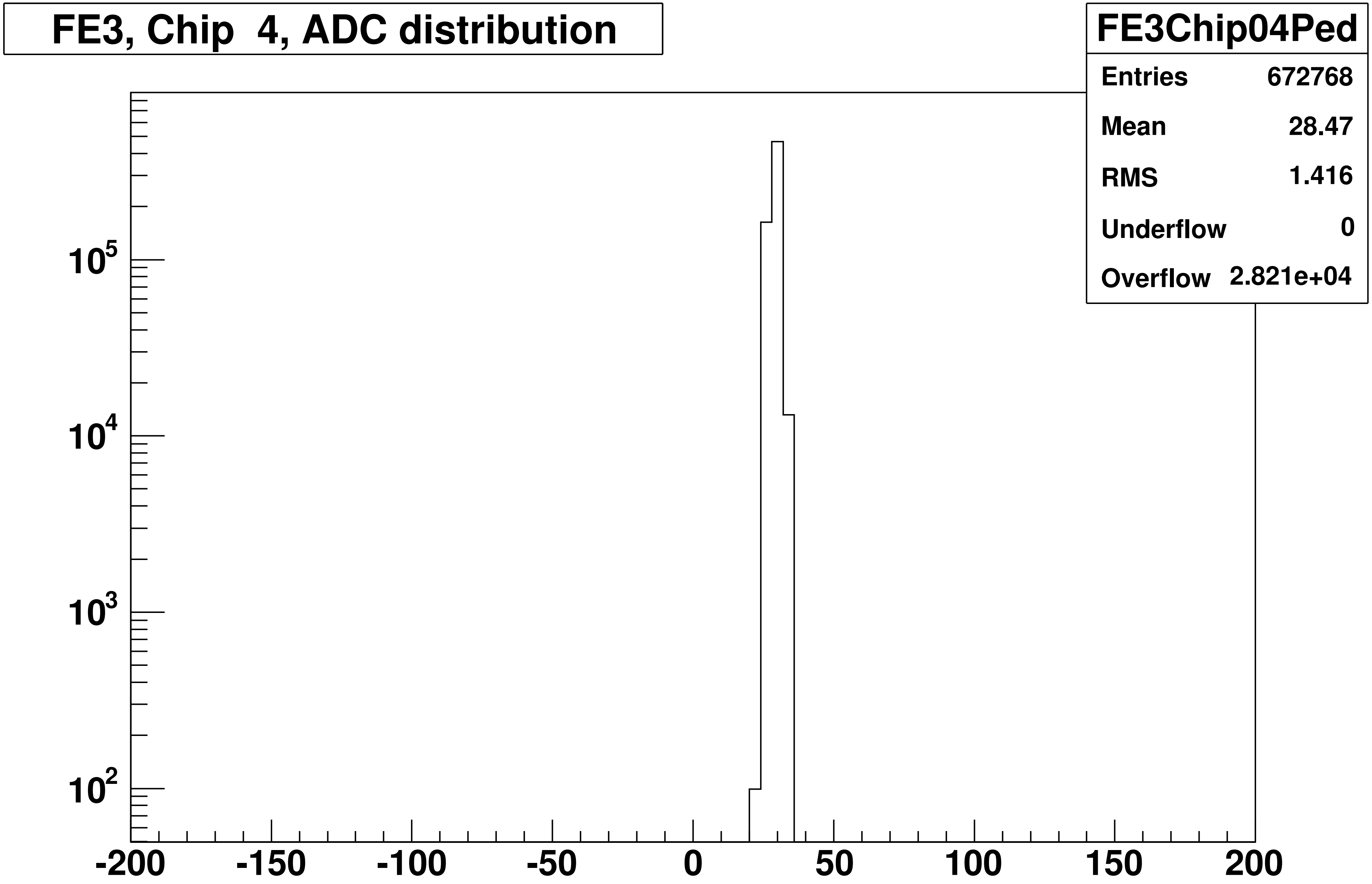

FE3, Chip 4, ADC distribution
FE3Chip04Ped
Entries 672768
Mean 28.47
RMS 1.416
Underflow 0
Overflow 2.821e+04
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10^4
10^3
10^2
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150
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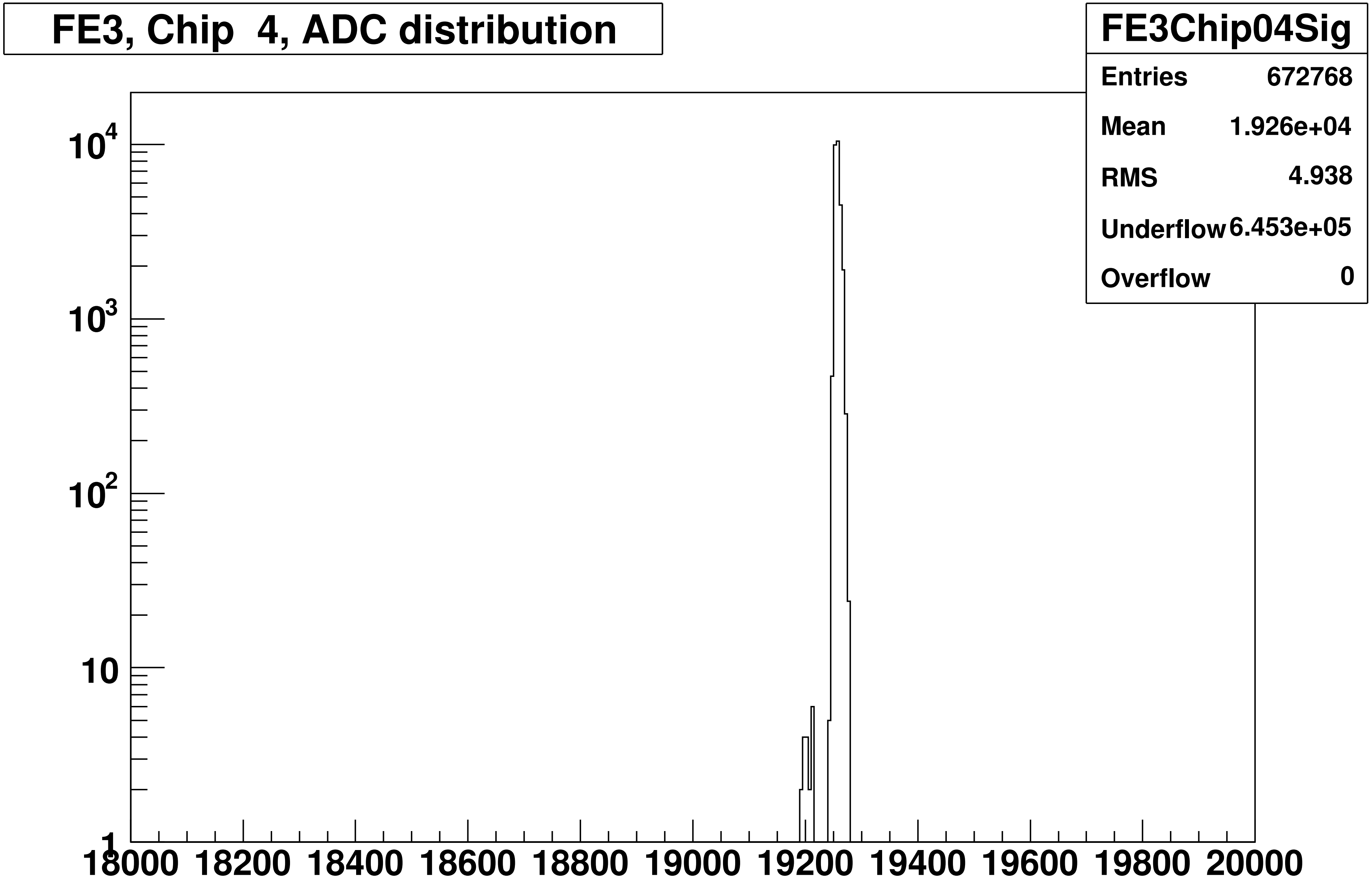

FE3, Chip 4, ADC distribution
FE3Chip04Sig
Entries 672768
Mean 1.926e+04
RMS 4.938
Underflow 6.453e+05
Overflow 0
10^4
10^3
10^2
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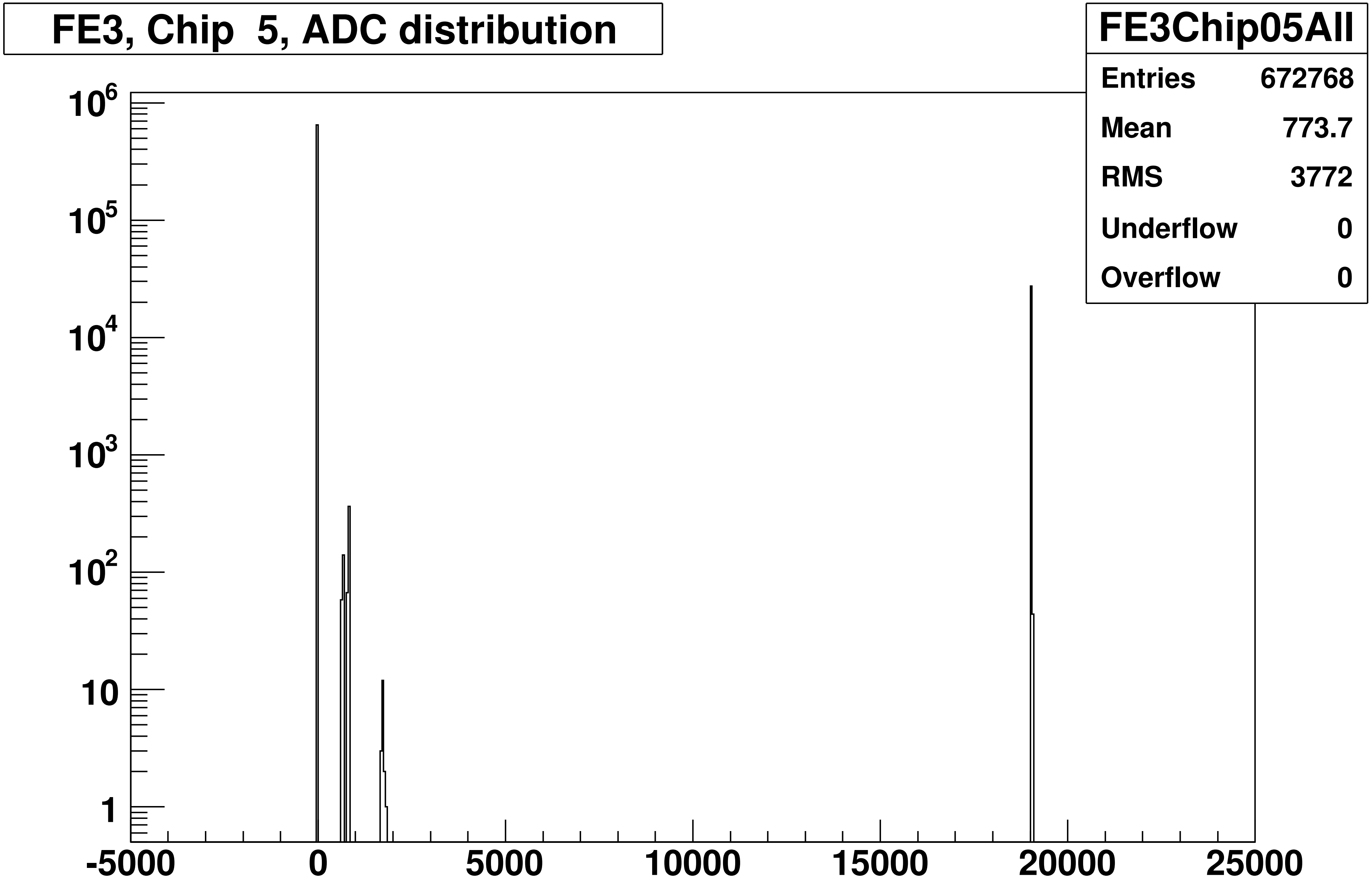
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE3, Chip 5, ADC distribution
FE3Chip05All
Entries 672768
Mean 773.7
RMS 3772
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
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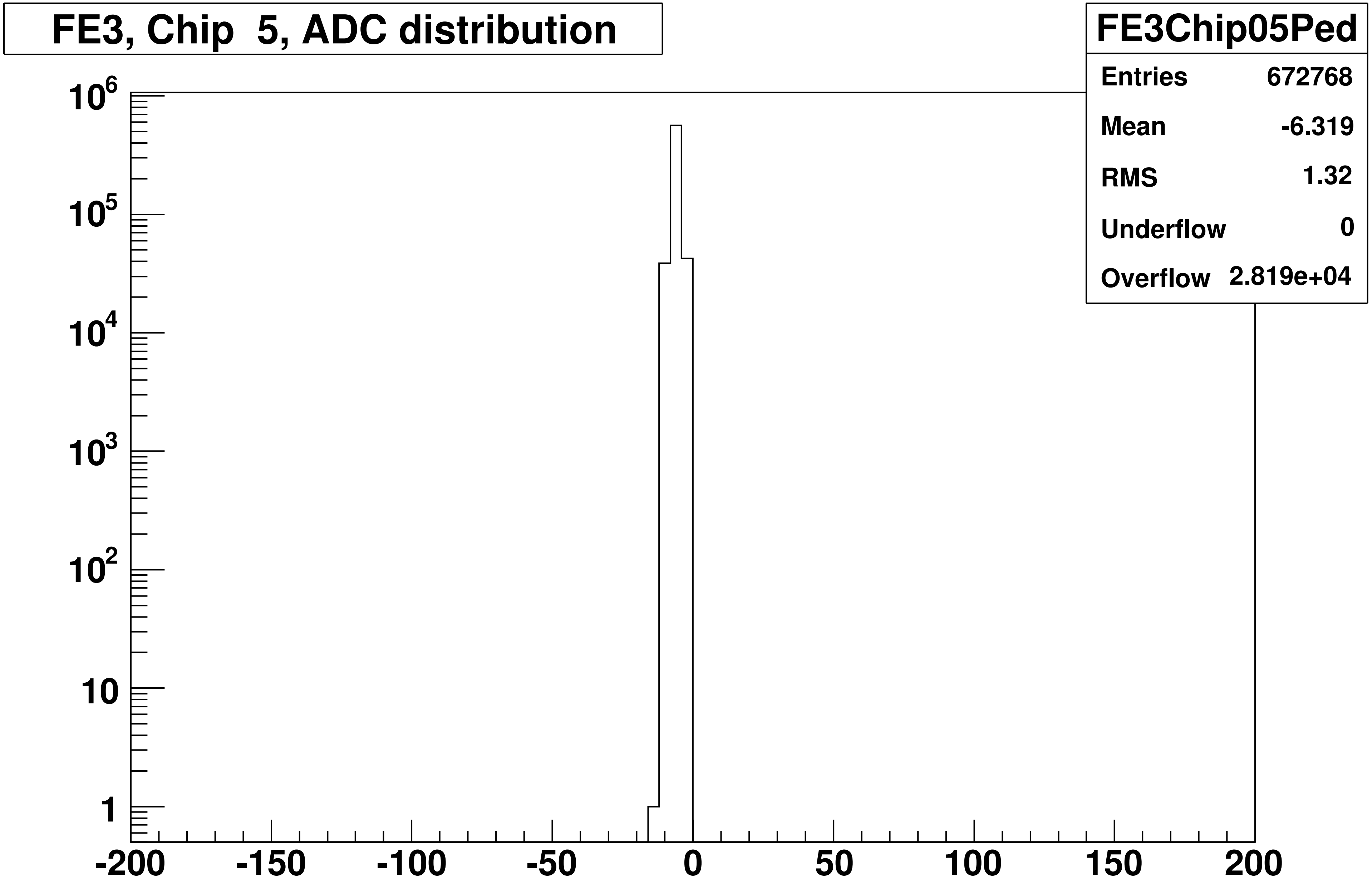

FE3, Chip 5, ADC distribution
FE3Chip05Ped
Entries 672768
Mean -6.319
RMS 1.32
Underflow 0
Overflow 2.819e+04
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10^5
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10^3
10^2
10
1
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100
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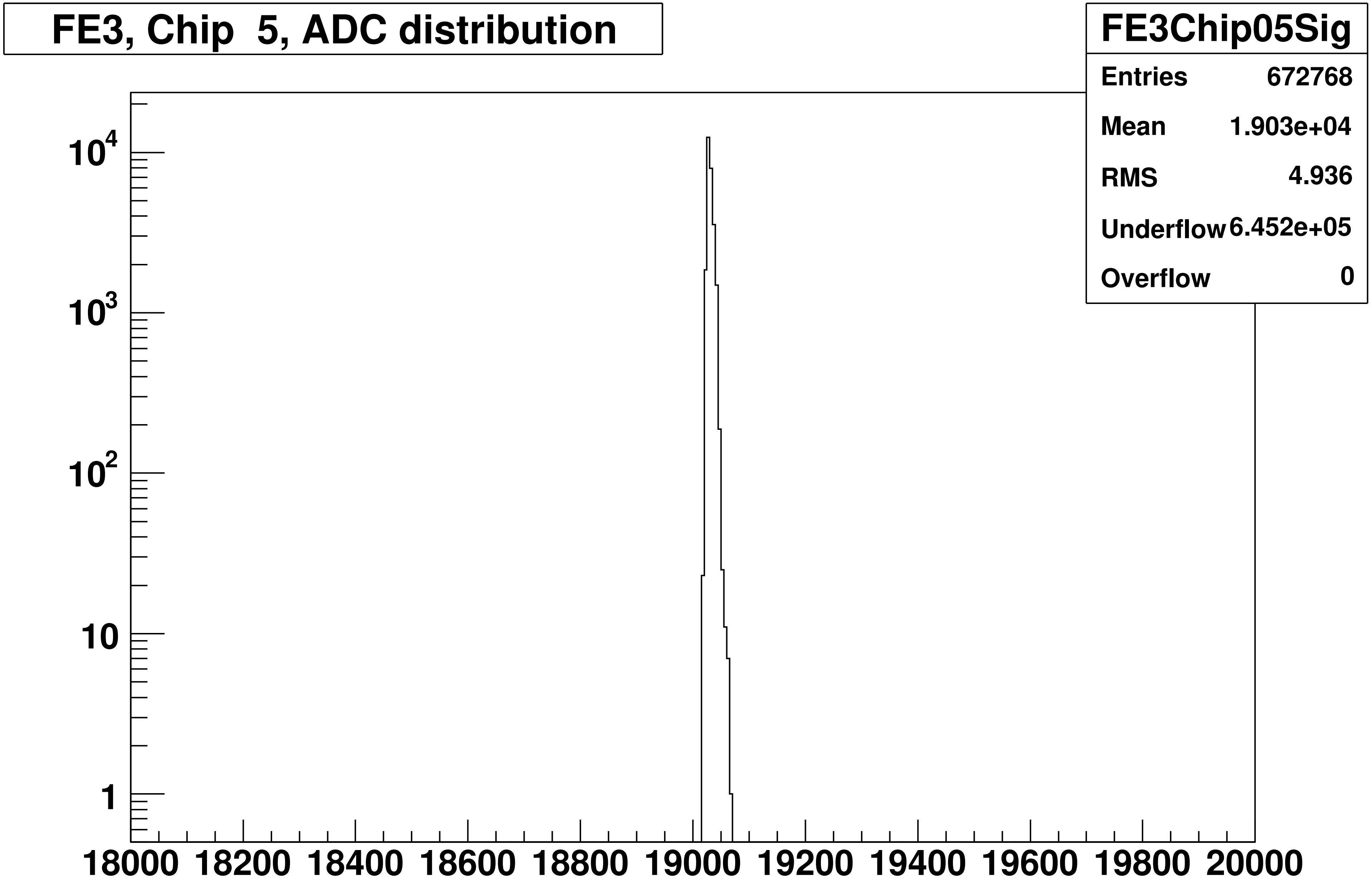
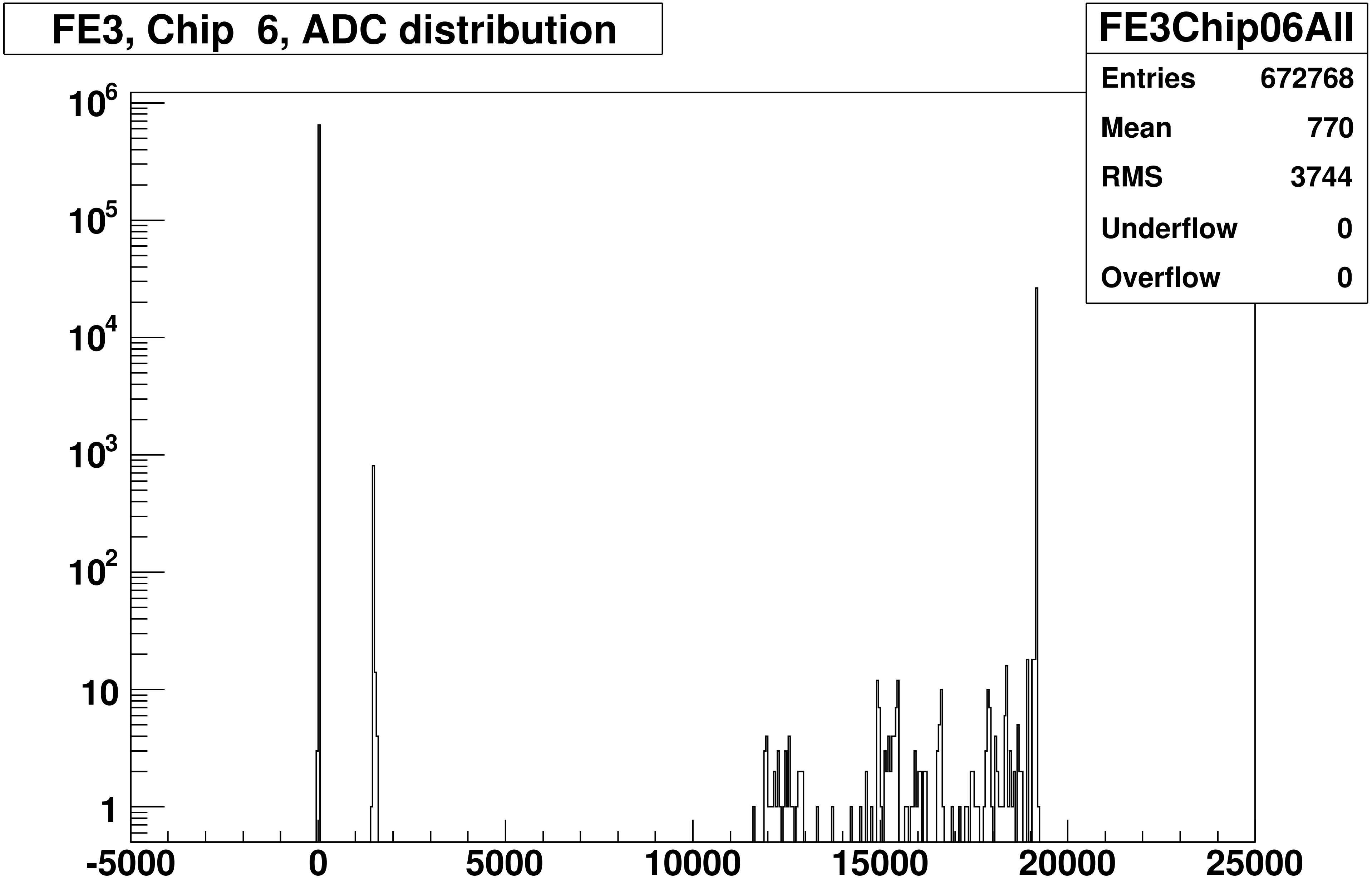

FE3, Chip 5, ADC distribution
FE3Chip05Sig
Entries 672768
Mean 1.903e+04
RMS 4.936
Underflow 6.452e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE3, Chip 6, ADC distribution
FE3Chip06All
Entries 672768
Mean 770
RMS 3744
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
1
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0
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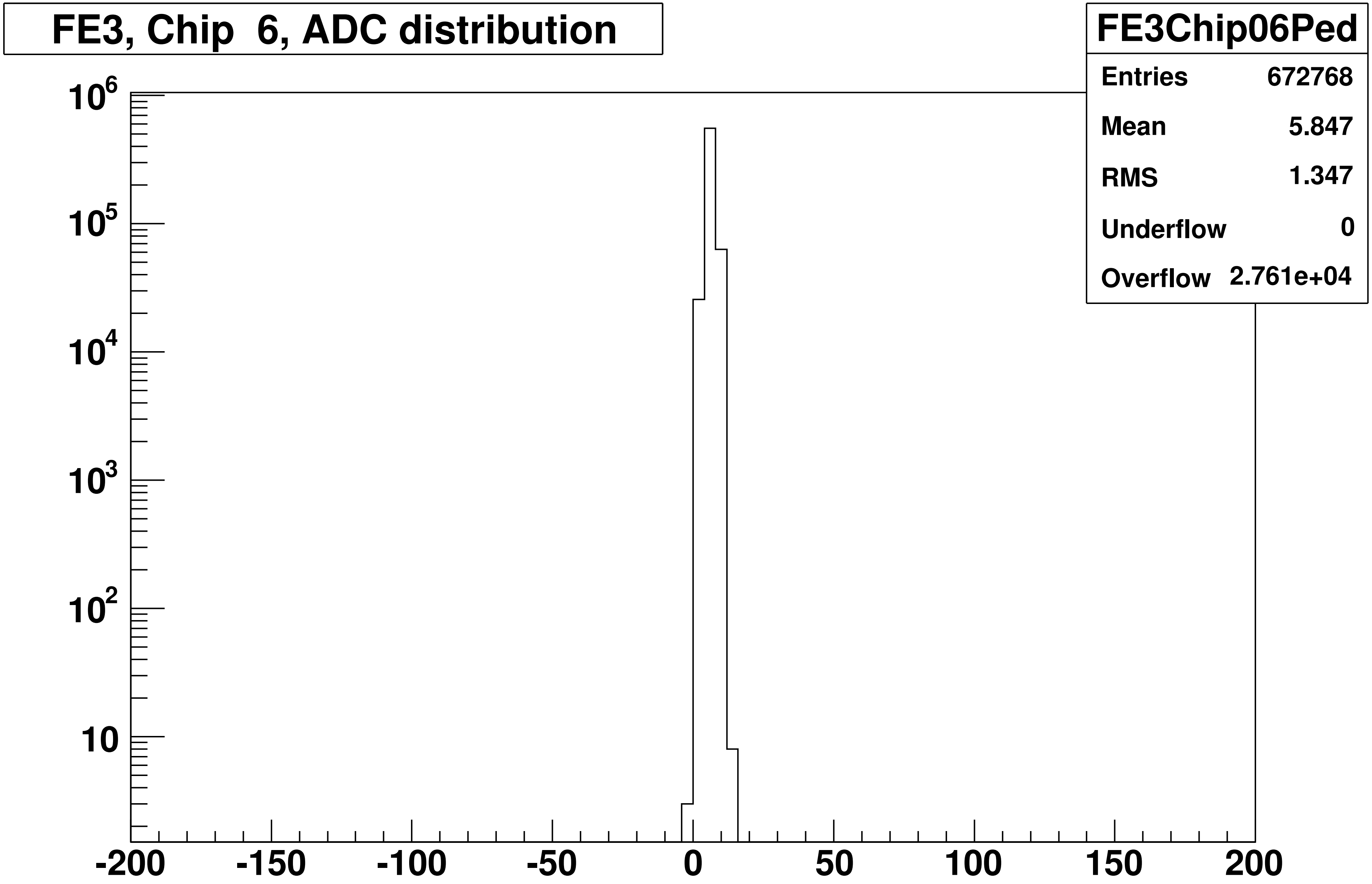
FE3, Chip 6, ADC distribution
FE3Chip06Ped
Entries 672768
Mean 5.847
RMS 1.347
Underflow 0
Overflow 2.761e+04
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10^5
10^4
10^3
10^2
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150
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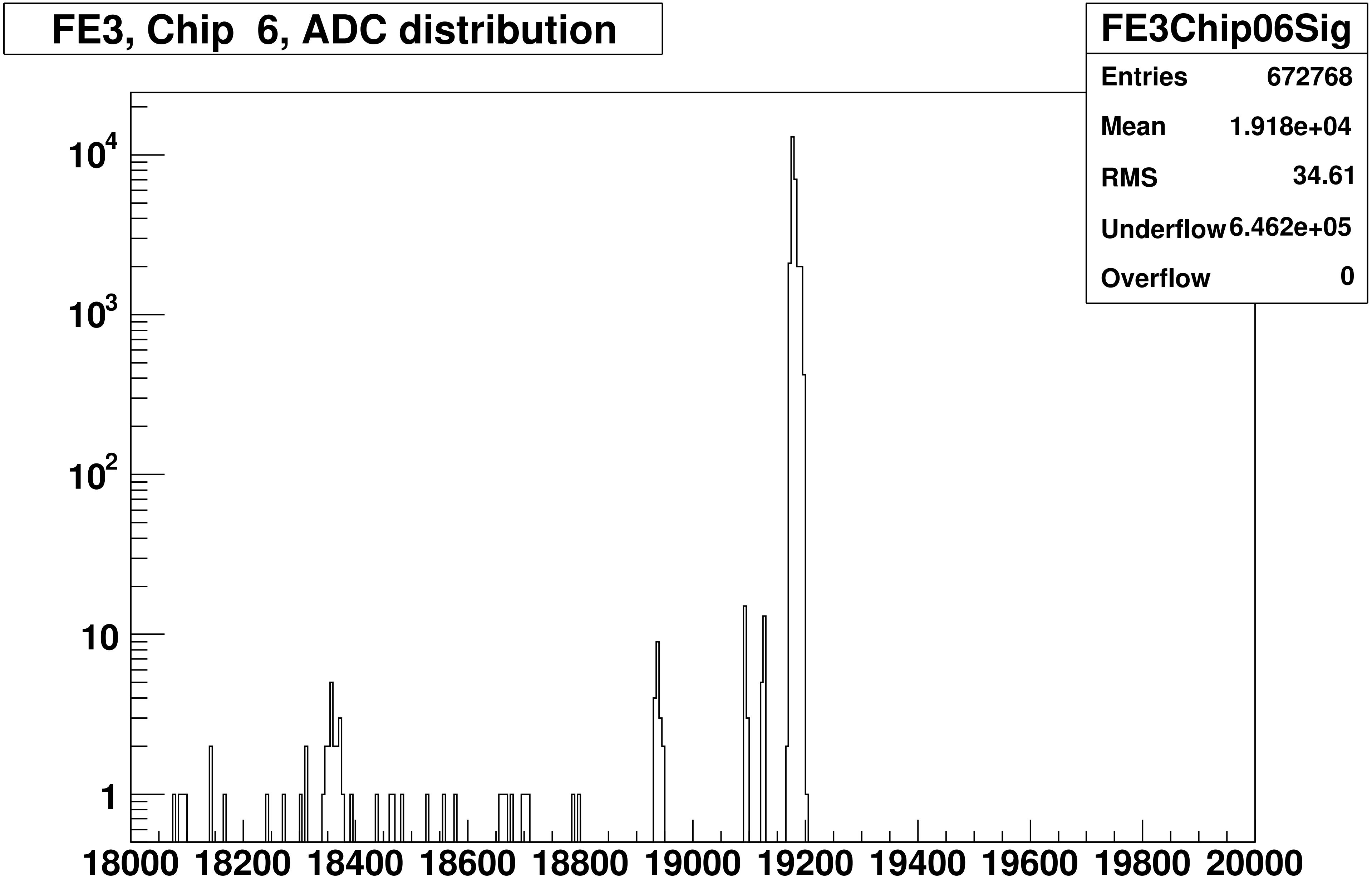
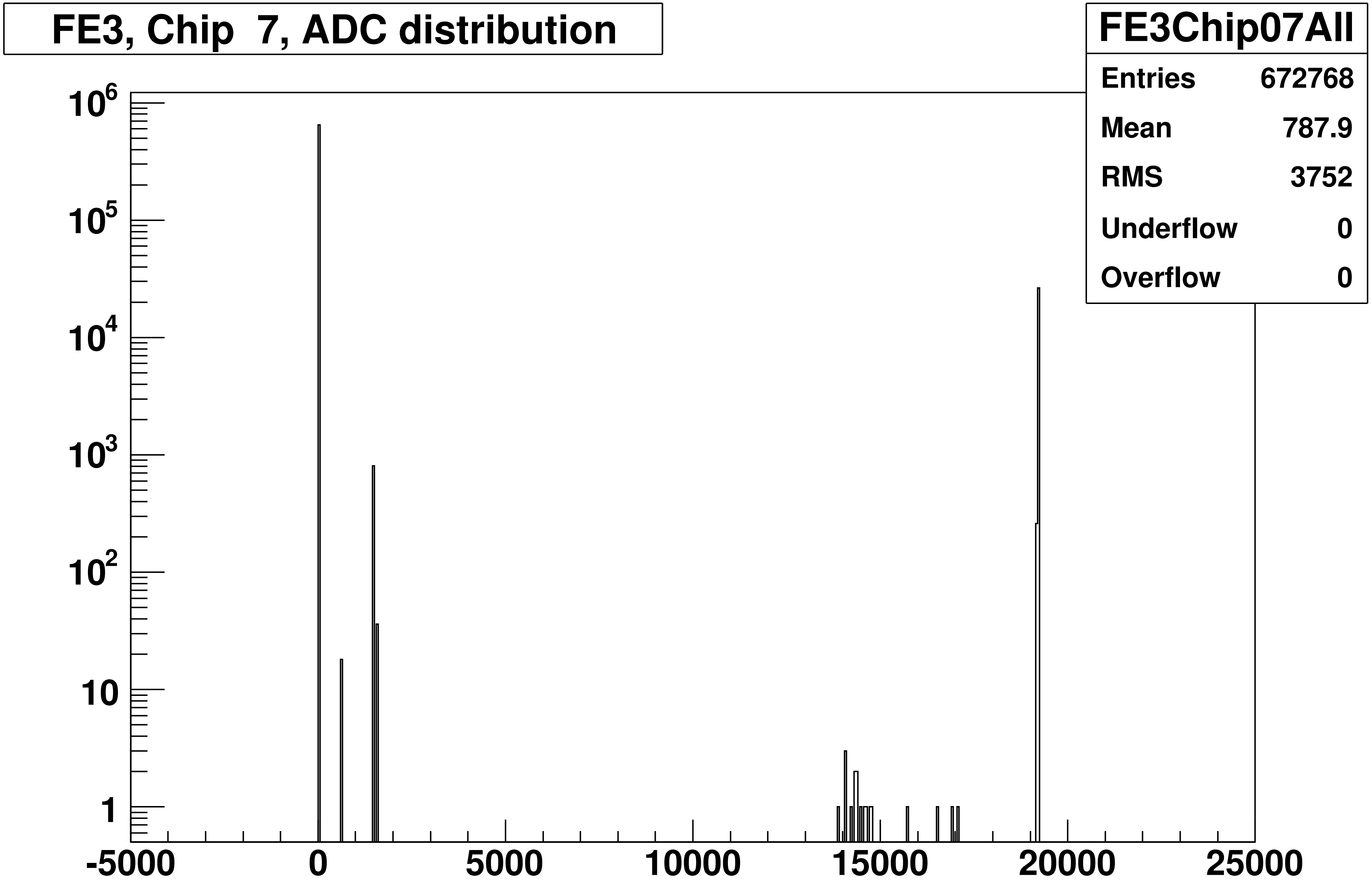

FE3, Chip 6, ADC distribution
FE3Chip06Sig
Entries 672768
Mean 1.918e+04
RMS 34.61
Underflow 6.462e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE3, Chip 7, ADC distribution
FE3Chip07All
Entries 672768
Mean 787.9
RMS 3752
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
1
-5000
0
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10000
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20000
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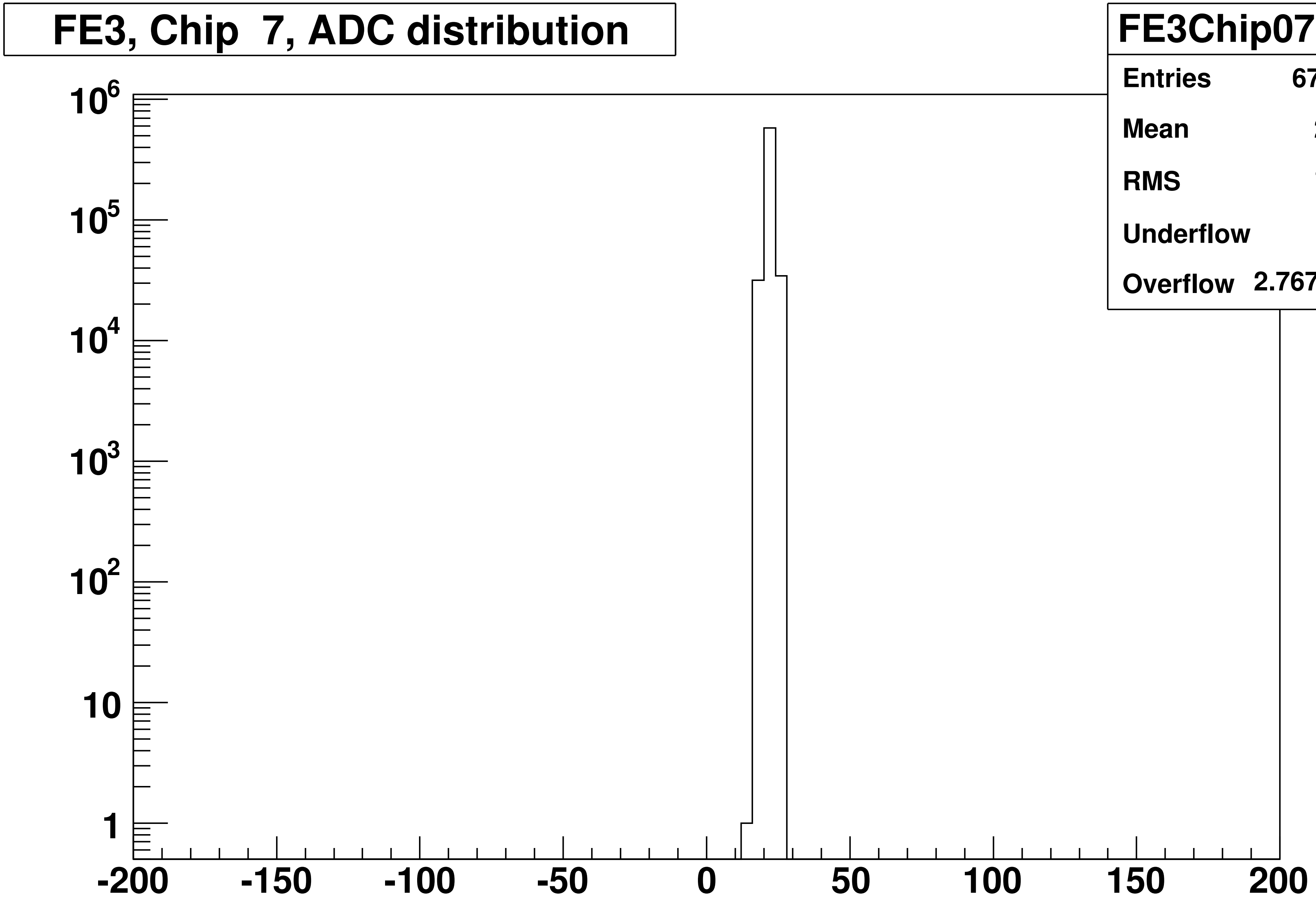
FE3, Chip 7, ADC distribution
FE3Chip07Ped
Entries 672768
Mean 21.72
RMS 1.306
Underflow 0
Overflow 2.767e+04
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10^5
10^4
10^3
10^2
10
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150
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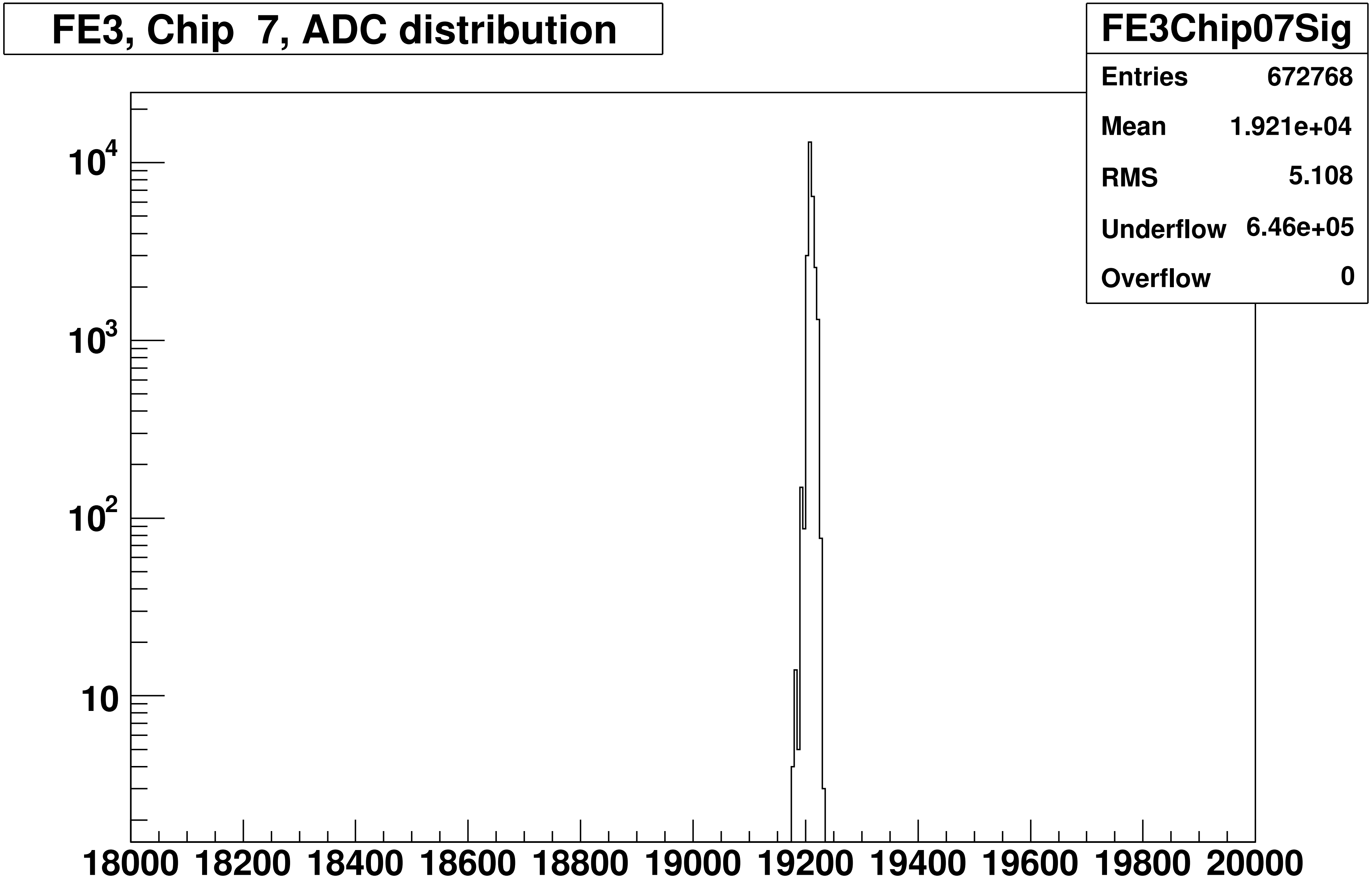

FE3, Chip 7, ADC distribution
FE3Chip07Sig
Entries 672768
Mean 1.921e+04
RMS 5.108
Underflow 6.46e+05
Overflow 0
10^4
10^3
10^2
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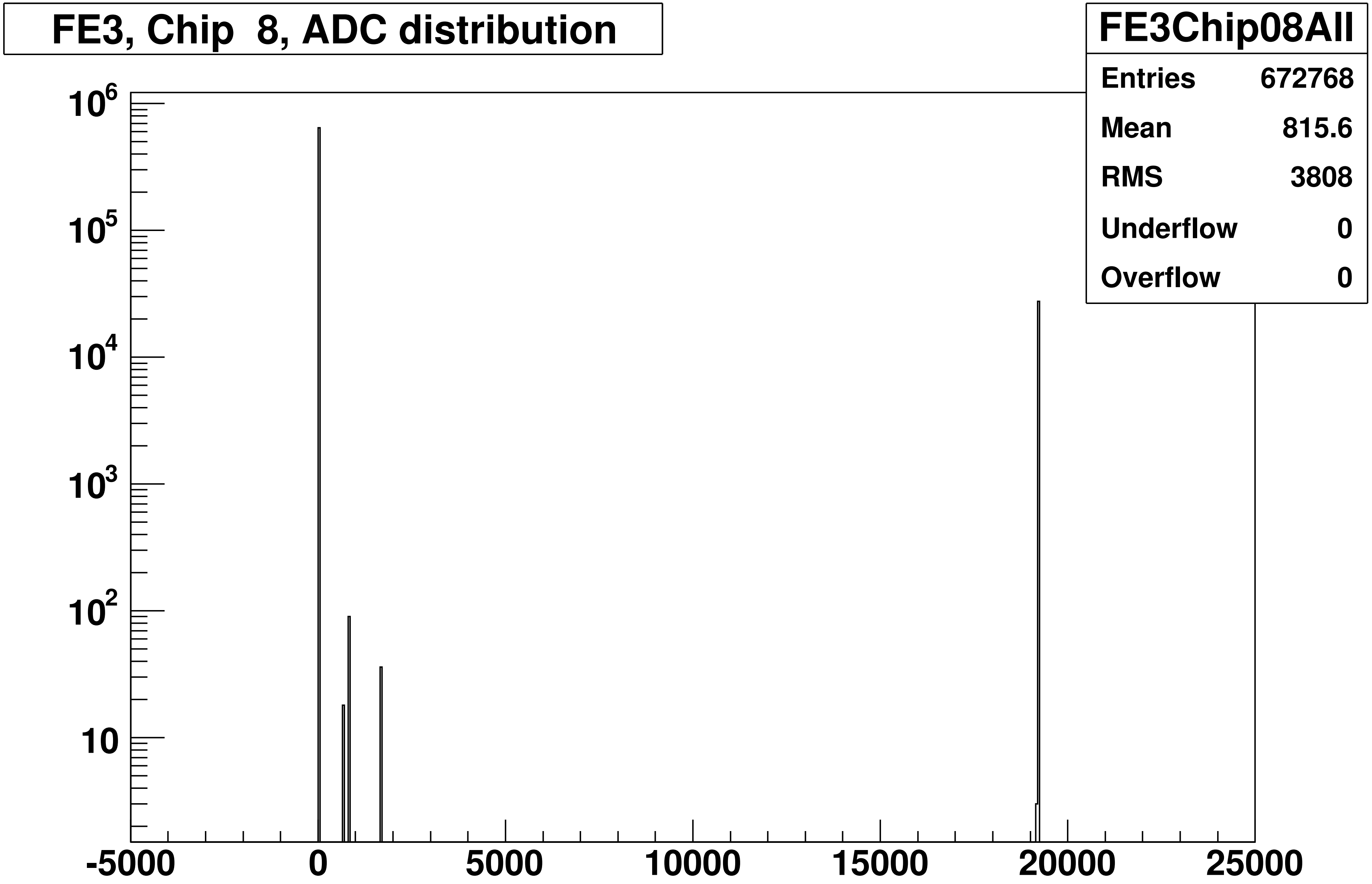
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE3, Chip 8, ADC distribution
FE3Chip08All
Entries 672768
Mean 815.6
RMS 3808
Underflow 0
Overflow 0
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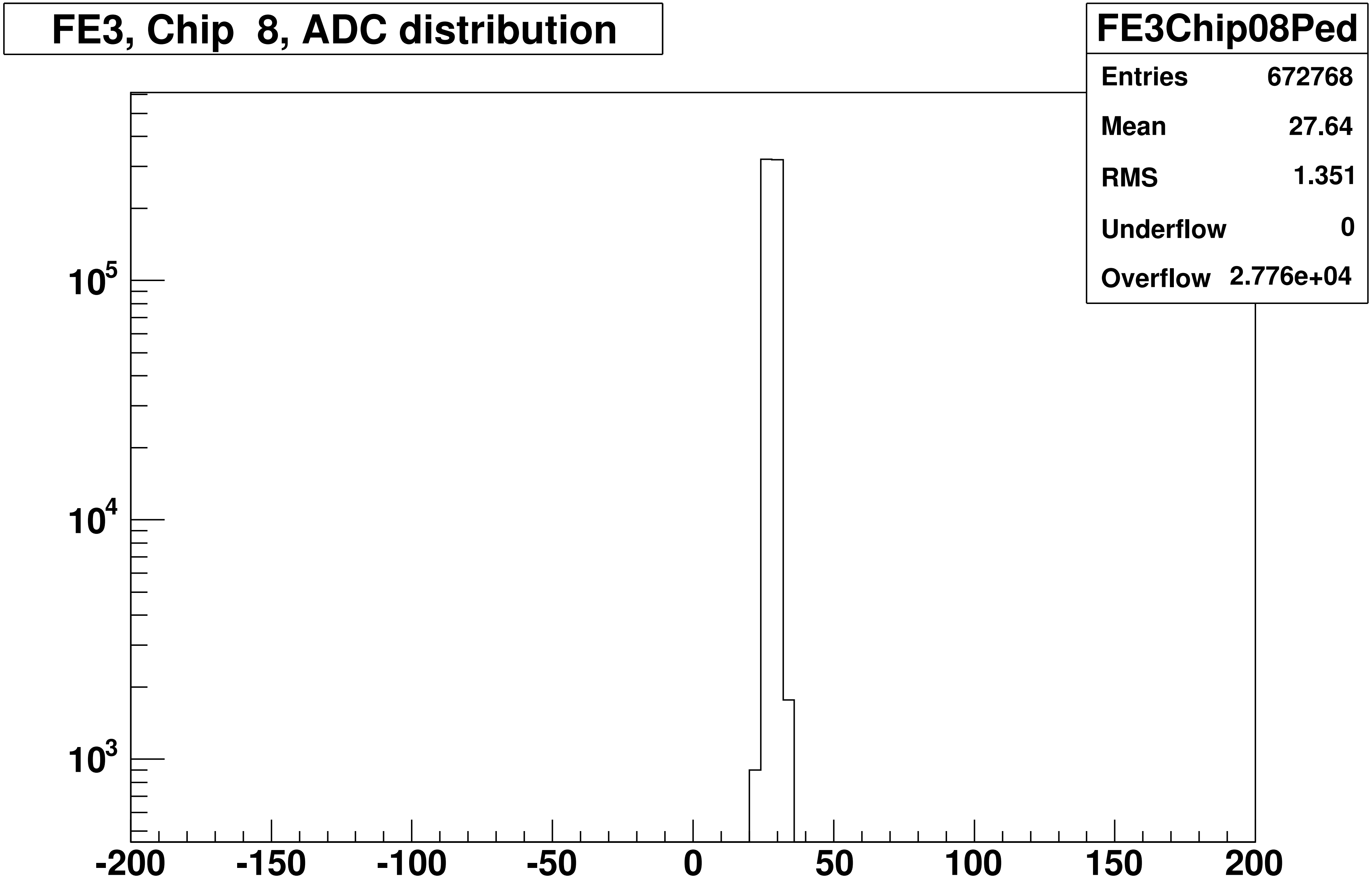
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE3, Chip 8, ADC distribution
FE3Chip08Ped
Entries 672768
Mean 27.64
RMS 1.351
Underflow 0
Overflow 2.776e+04
10^5
10^4
10^3
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-150
-100
-50
0
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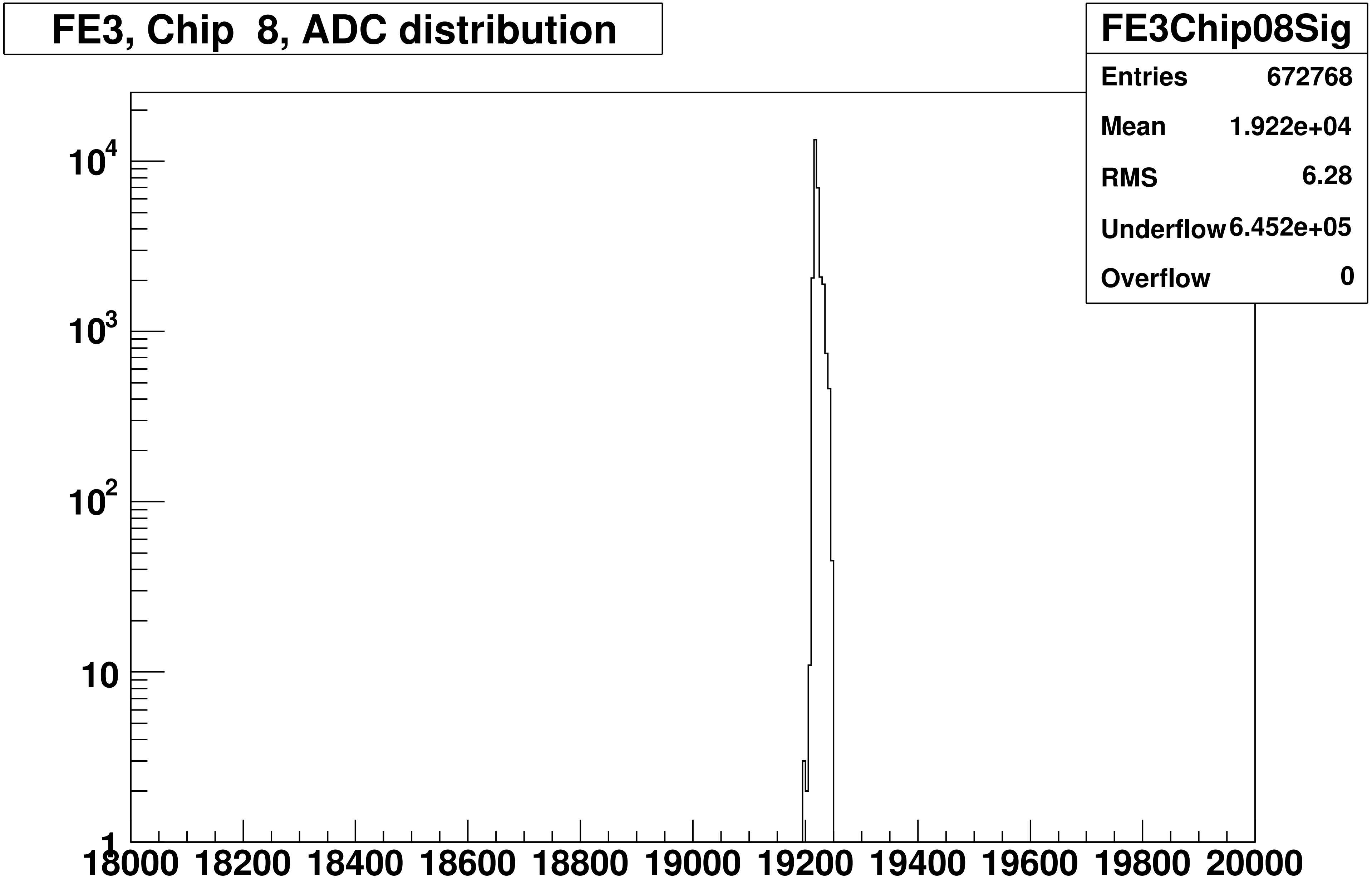
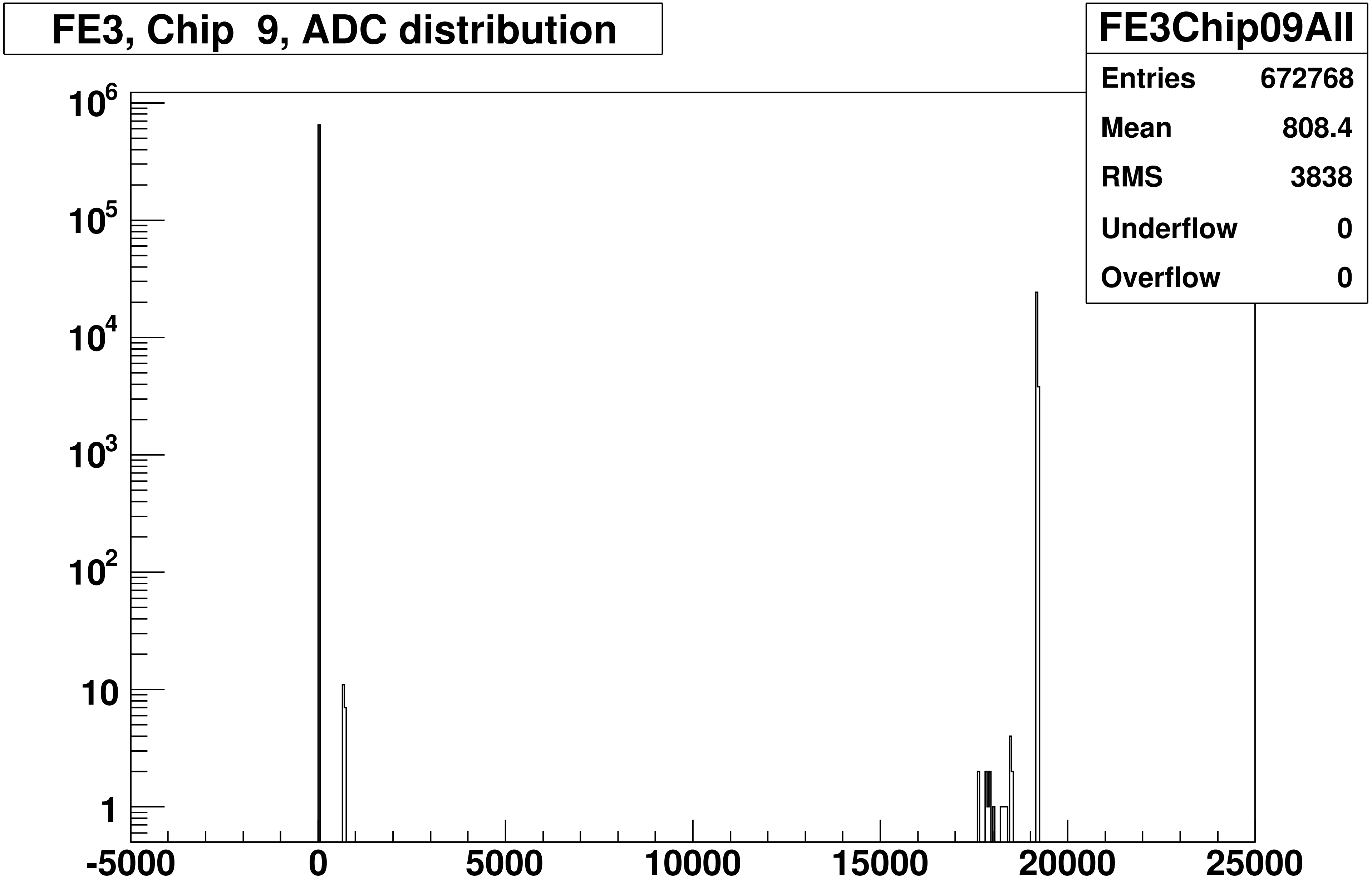
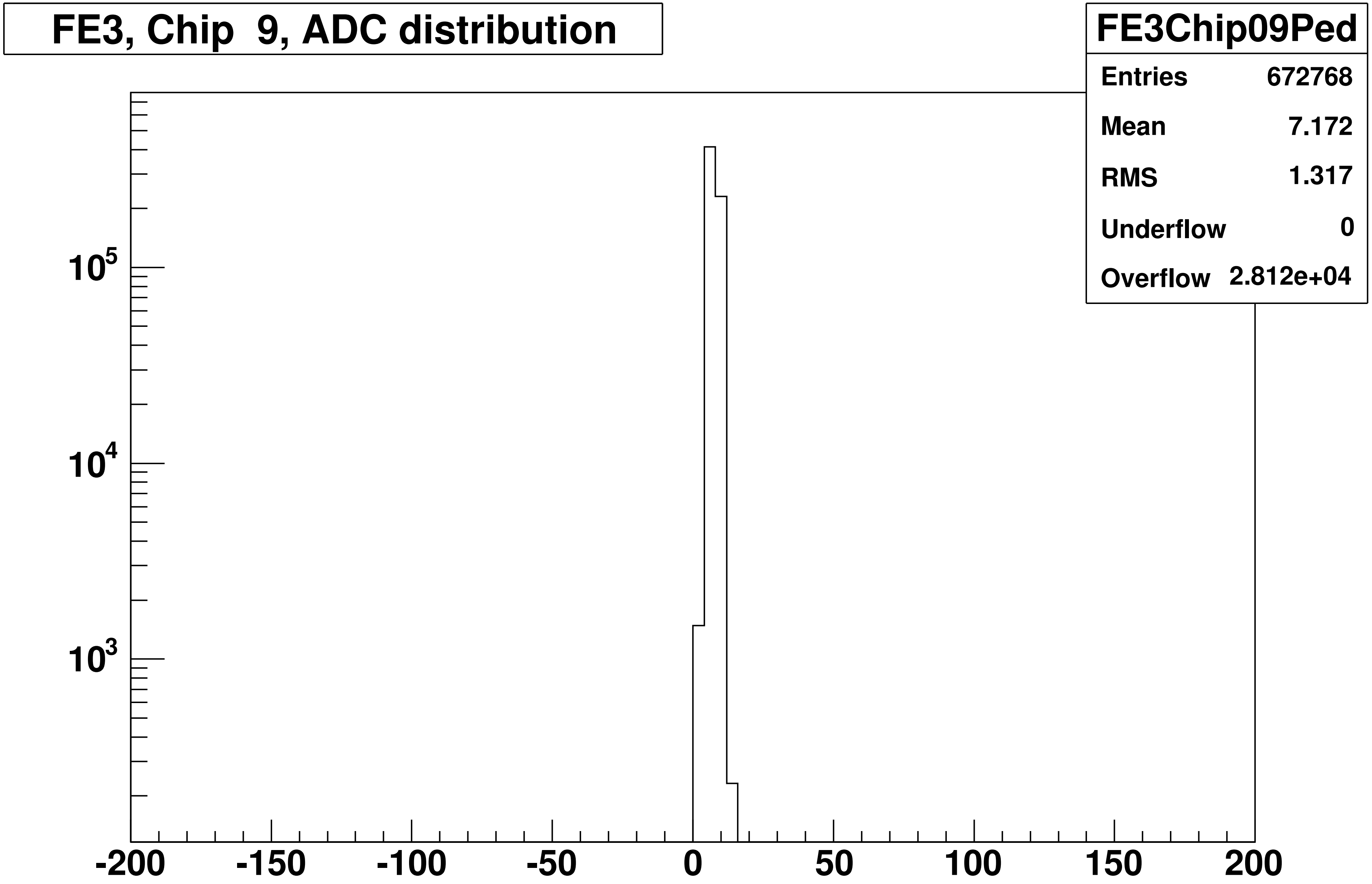
100
150
200

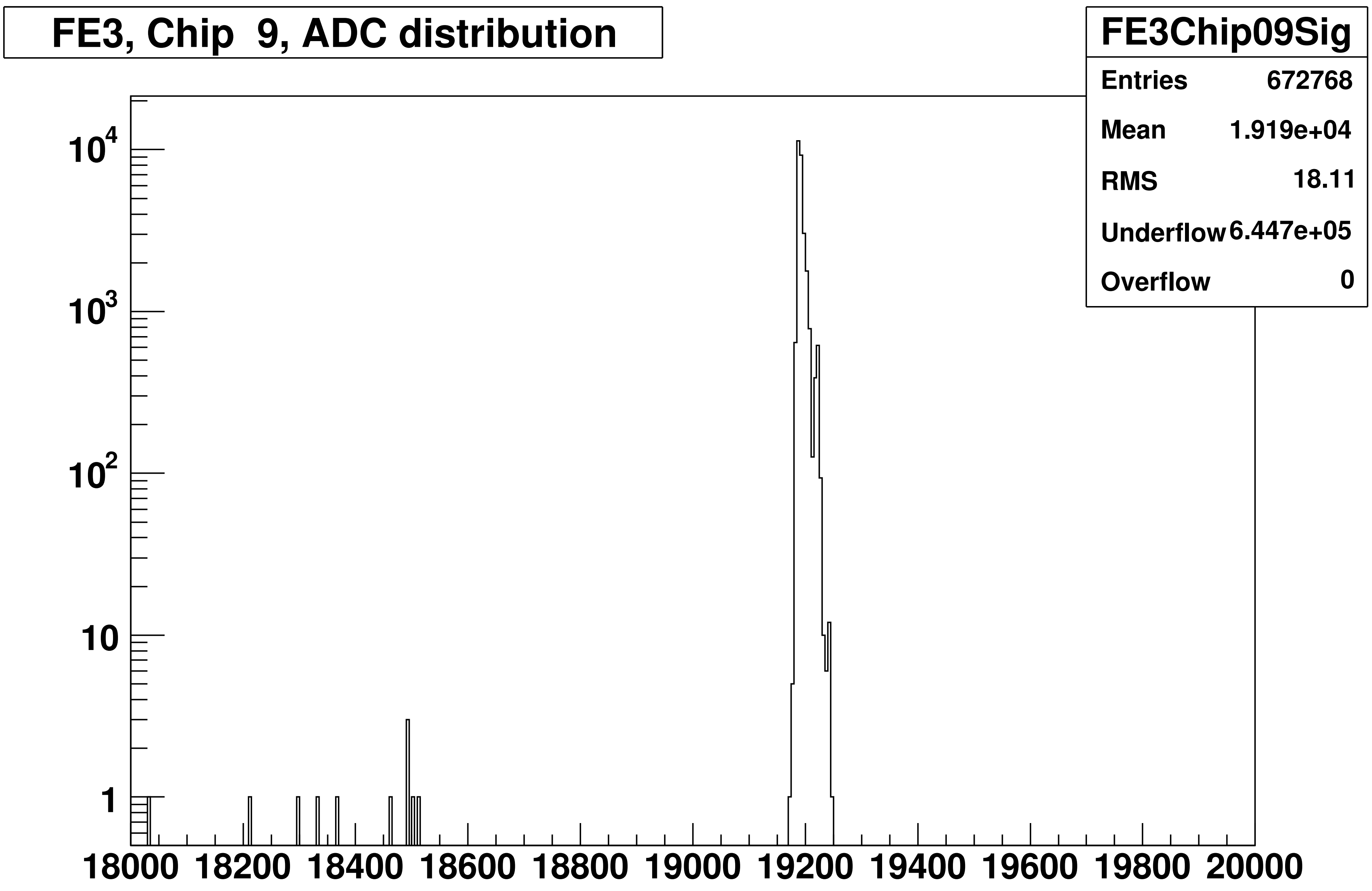


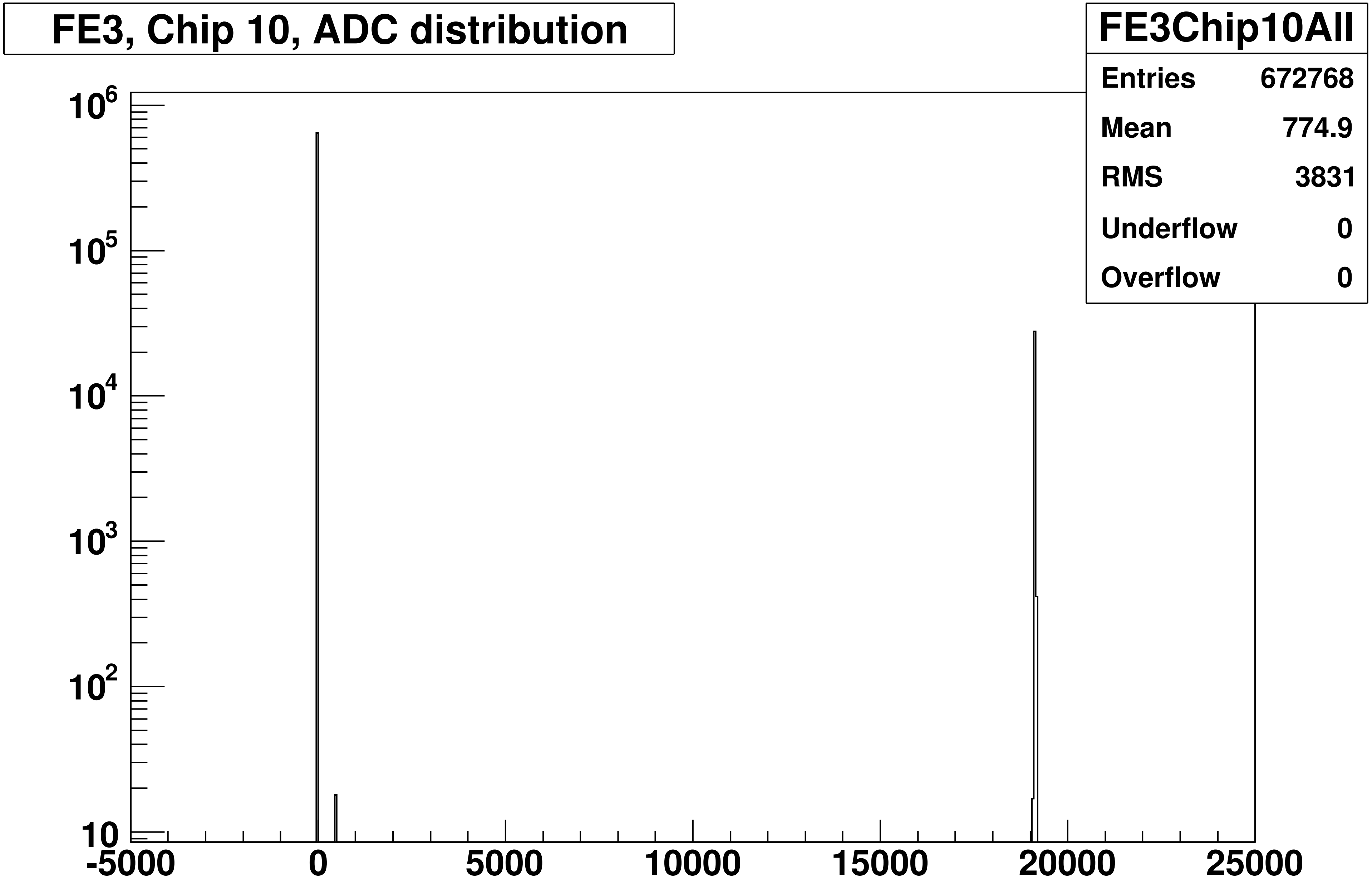
FE3, Chip 8, ADC distribution
FE3Chip08Sig
Entries 672768
Mean 1.922e+04
RMS 6.28
Underflow 6.452e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000



FE3, Chip 9, ADC distribution
FE3Chip09All
Entries 672768
Mean 808.4
RMS 3838
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE3, Chip 9, ADC distribution
FE3Chip09Ped
Entries 672768
Mean 7.172
RMS 1.317
Underflow 0
Overflow 2.812e+04
10^5
10^4
10^3
-200
-150
-100
-50
0
50
100
150
200


FE3, Chip 9, ADC distribution
FE3Chip09Sig
Entries 672768
Mean 1.919e+04
RMS 18.11
Underflow 6.447e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE3, Chip 10, ADC distribution
FE3Chip10All
Entries 672768
Mean 774.9
RMS 3831
Underflow 0
Overflow 0
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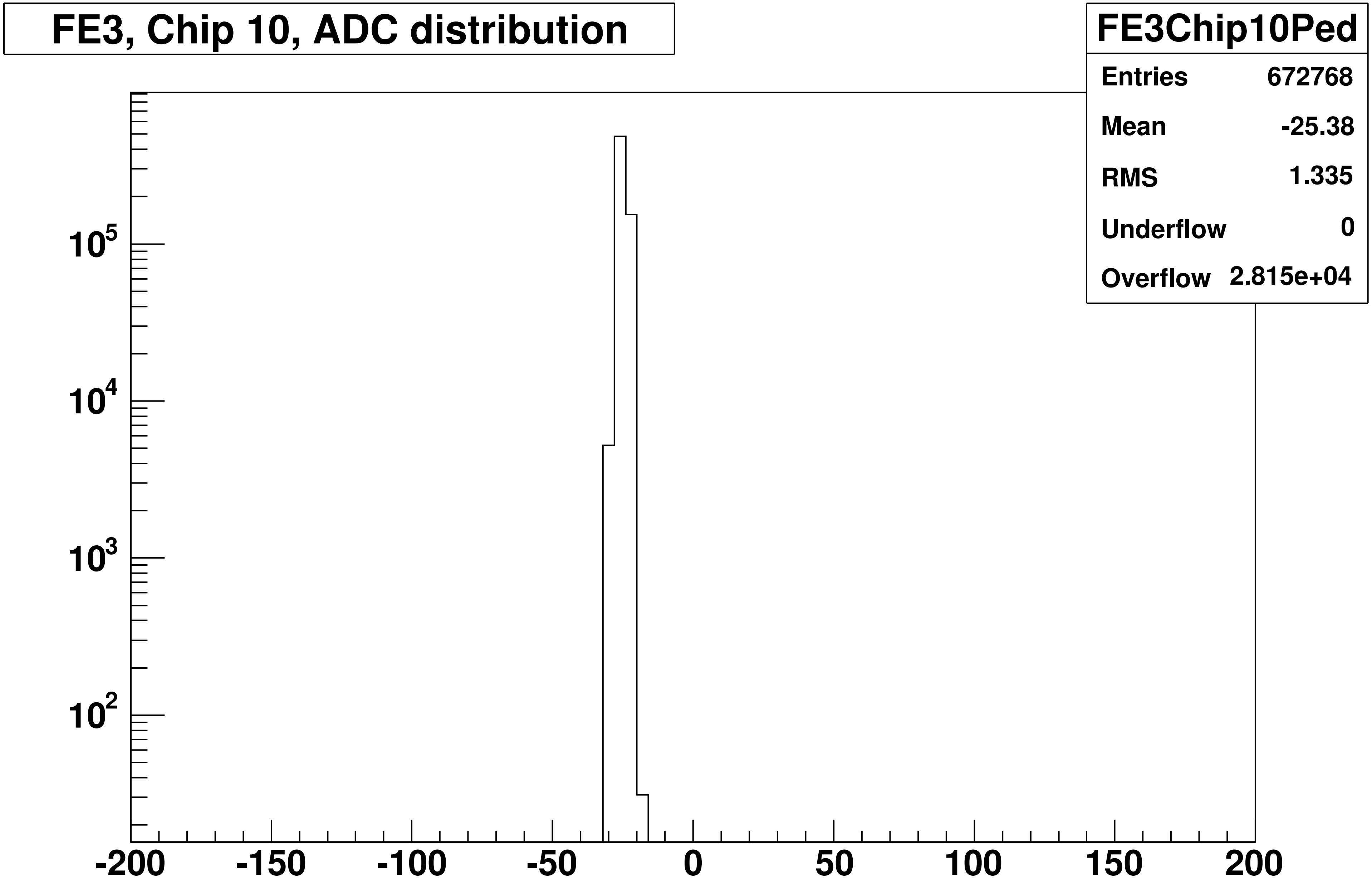
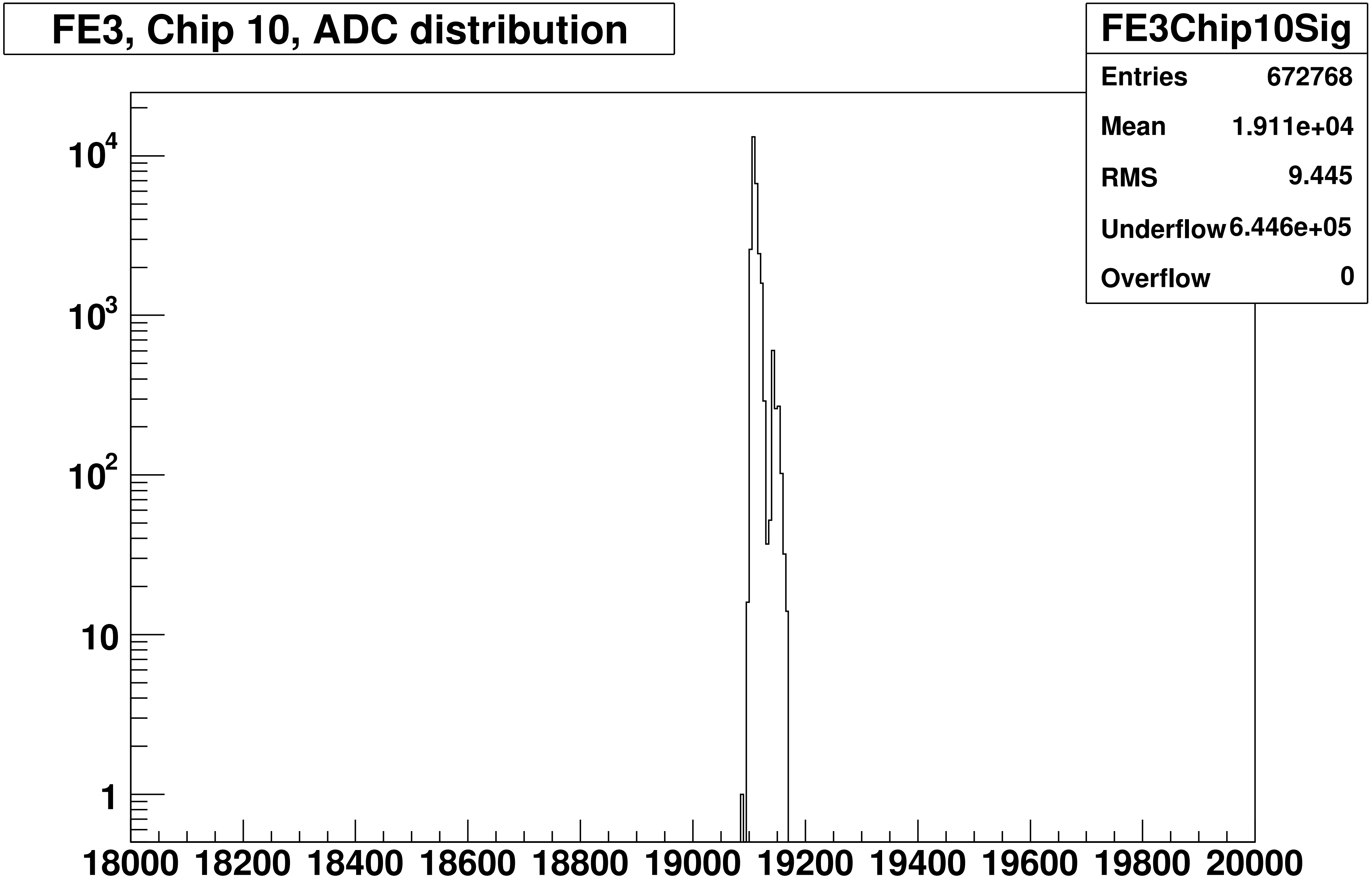
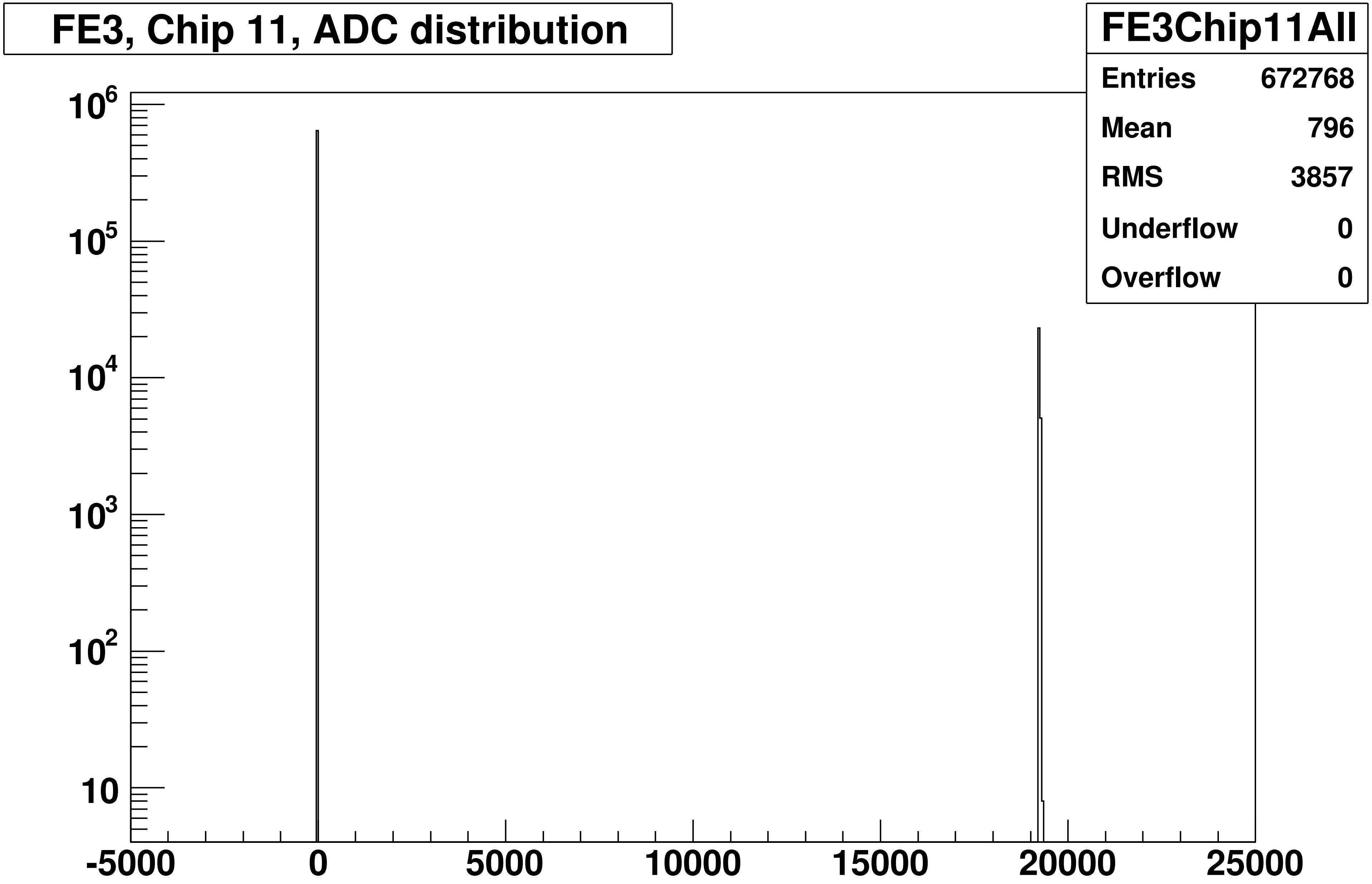
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000



FE3, Chip 10, ADC distribution
FE3Chip10Ped
Entries 672768
Mean -25.38
RMS 1.335
Underflow 0
Overflow 2.815e+04
10^5
10^4
10^3
10^2
-200 -150 -100 -50 0 50 100 150 200



FE3, Chip 10, ADC distribution
FE3Chip10Sig
Entries 672768
Mean 1.911e+04
RMS 9.445
Underflow 6.446e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE3, Chip 11, ADC distribution
FE3Chip11All
Entries 672768
Mean 796
RMS 3857
Underflow 0
Overflow 0
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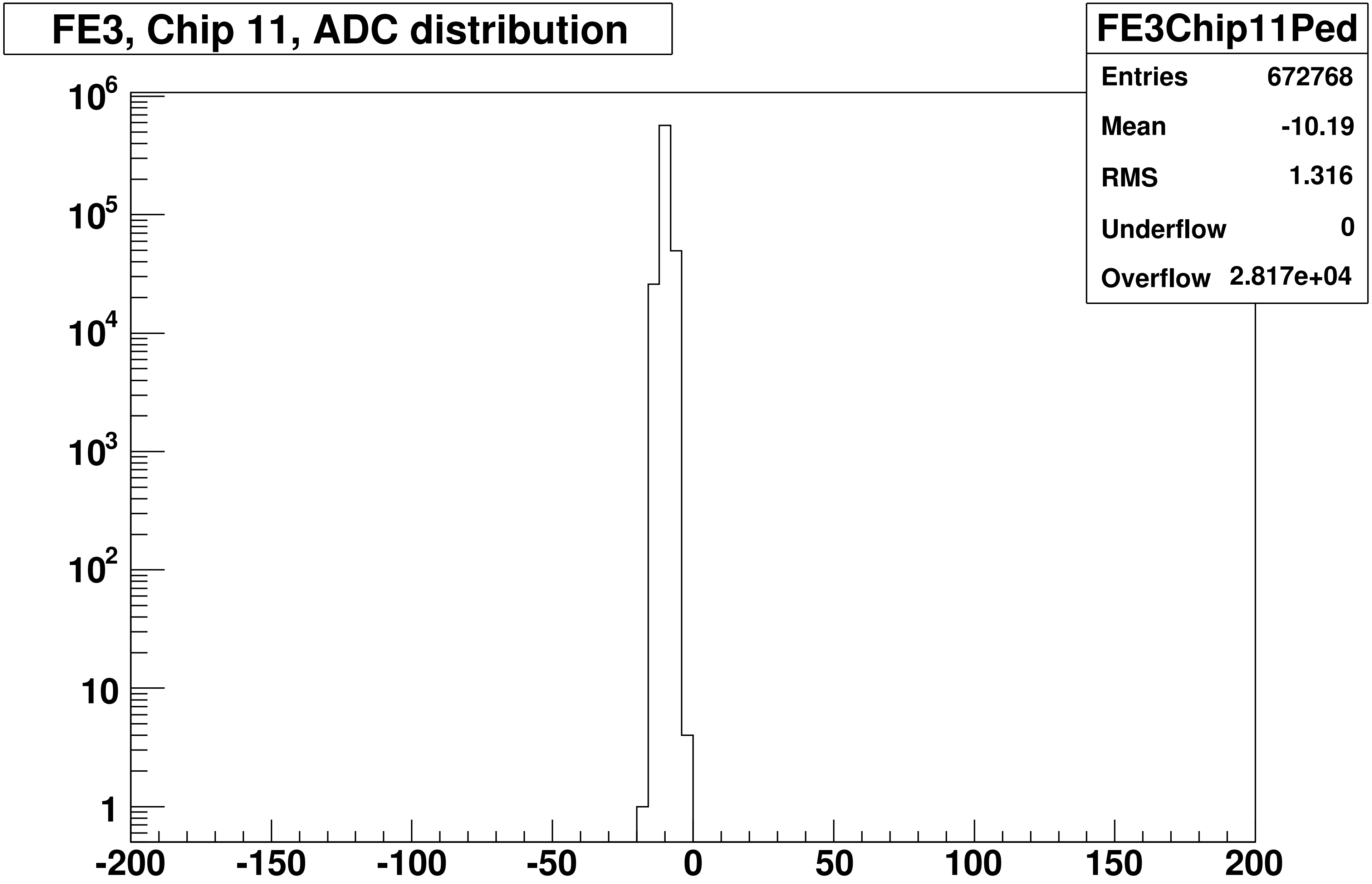
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE3, Chip 11, ADC distribution
FE3Chip11Ped
Entries 672768
Mean -10.19
RMS 1.316
Underflow 0
Overflow 2.817e+04
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10^5
10^4
10^3
10^2
10
1
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-100
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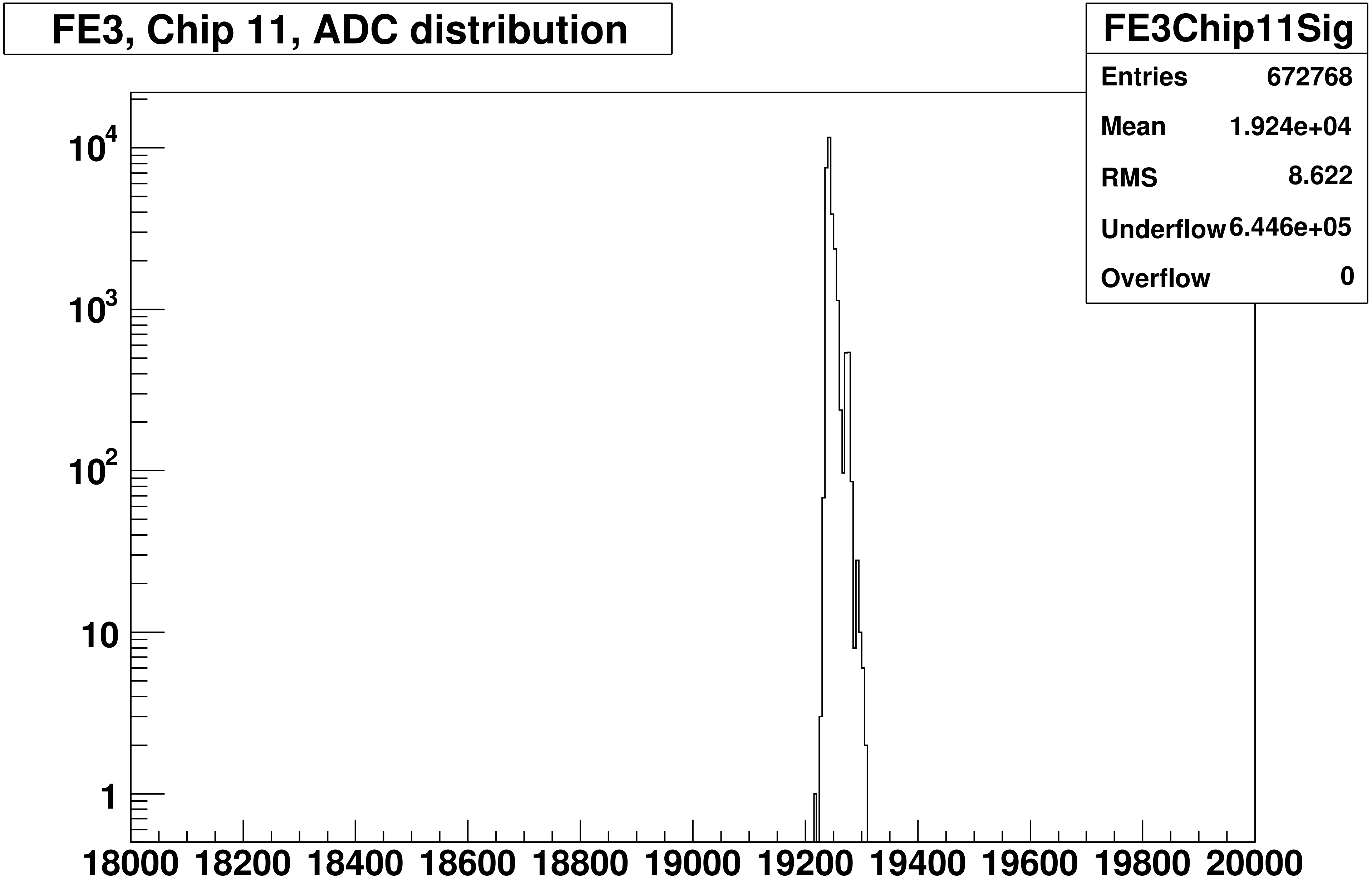
0
50
100
150
200


FE3, Chip 11, ADC distribution
FE3Chip11Sig
Entries 672768
Mean 1.924e+04
RMS 8.622
Underflow 6.446e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
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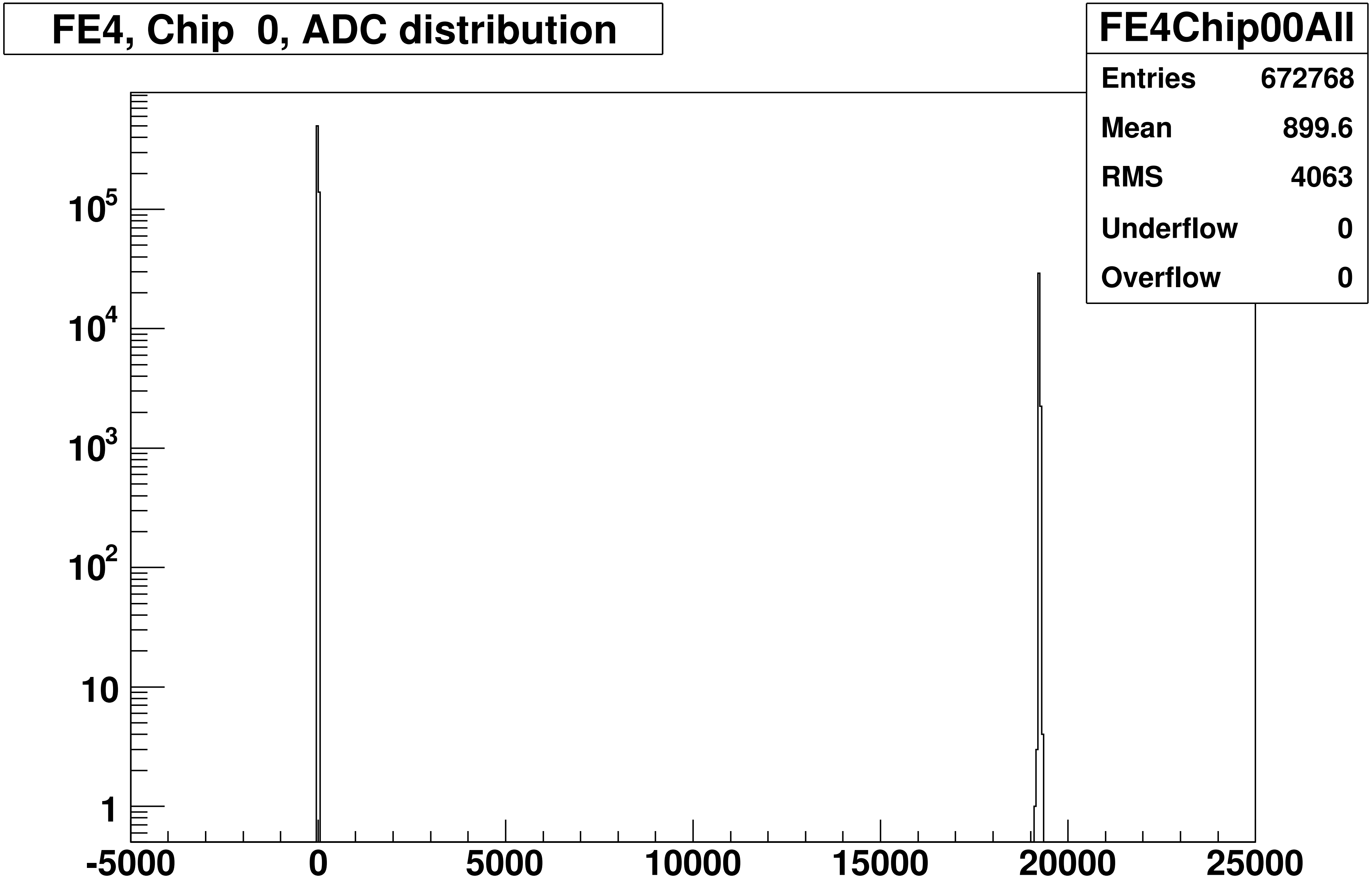
FE4, Chip 0, ADC distribution
FE4Chip00All
Entries 672768
Mean 899.6
RMS 4063
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
1
-5000
0
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20000
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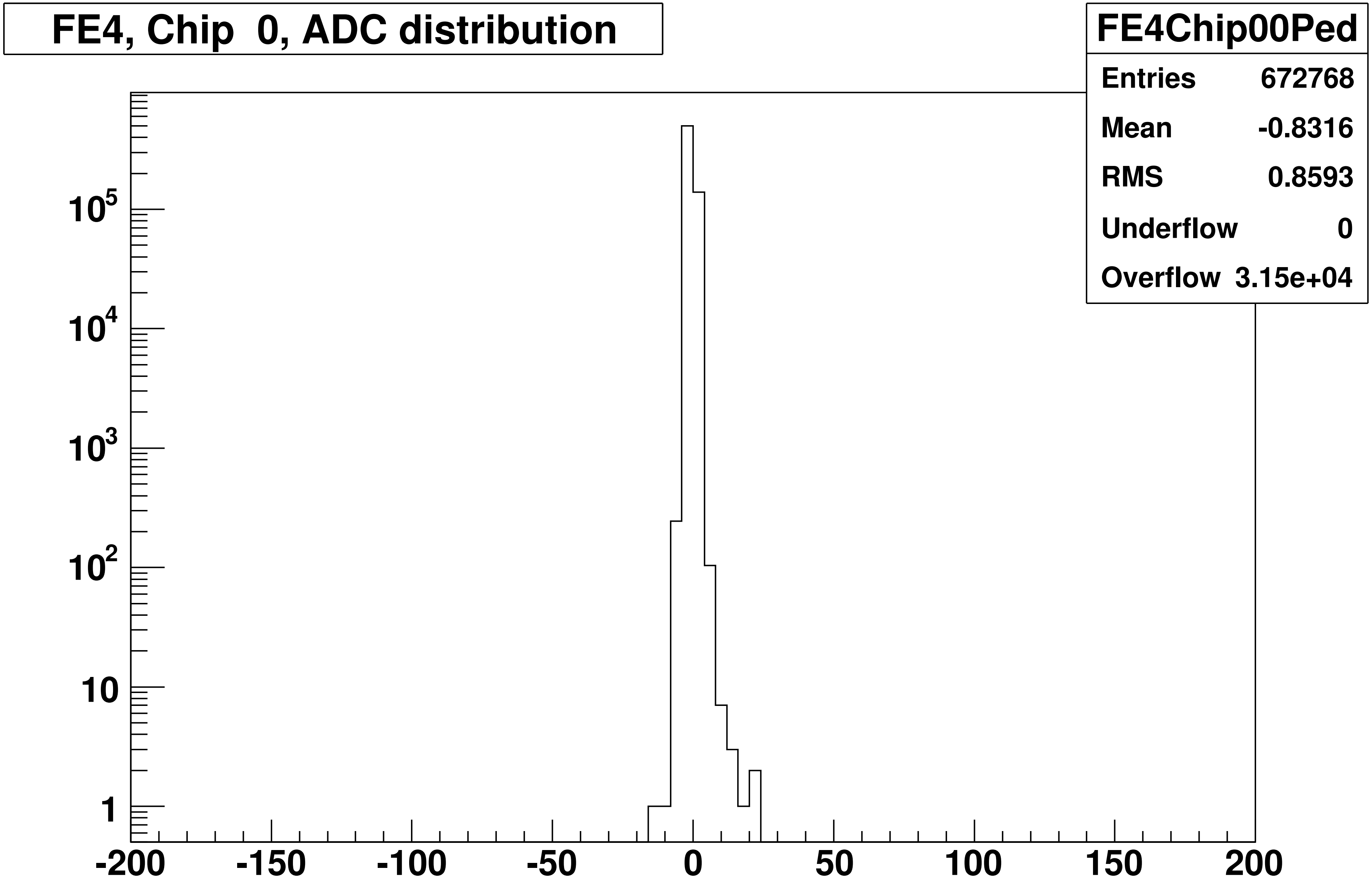

FE4, Chip 0, ADC distribution
FE4Chip00Ped
Entries 672768
Mean -0.8316
RMS 0.8593
Underflow 0
Overflow 3.15e+04
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10^4
10^3
10^2
10
1
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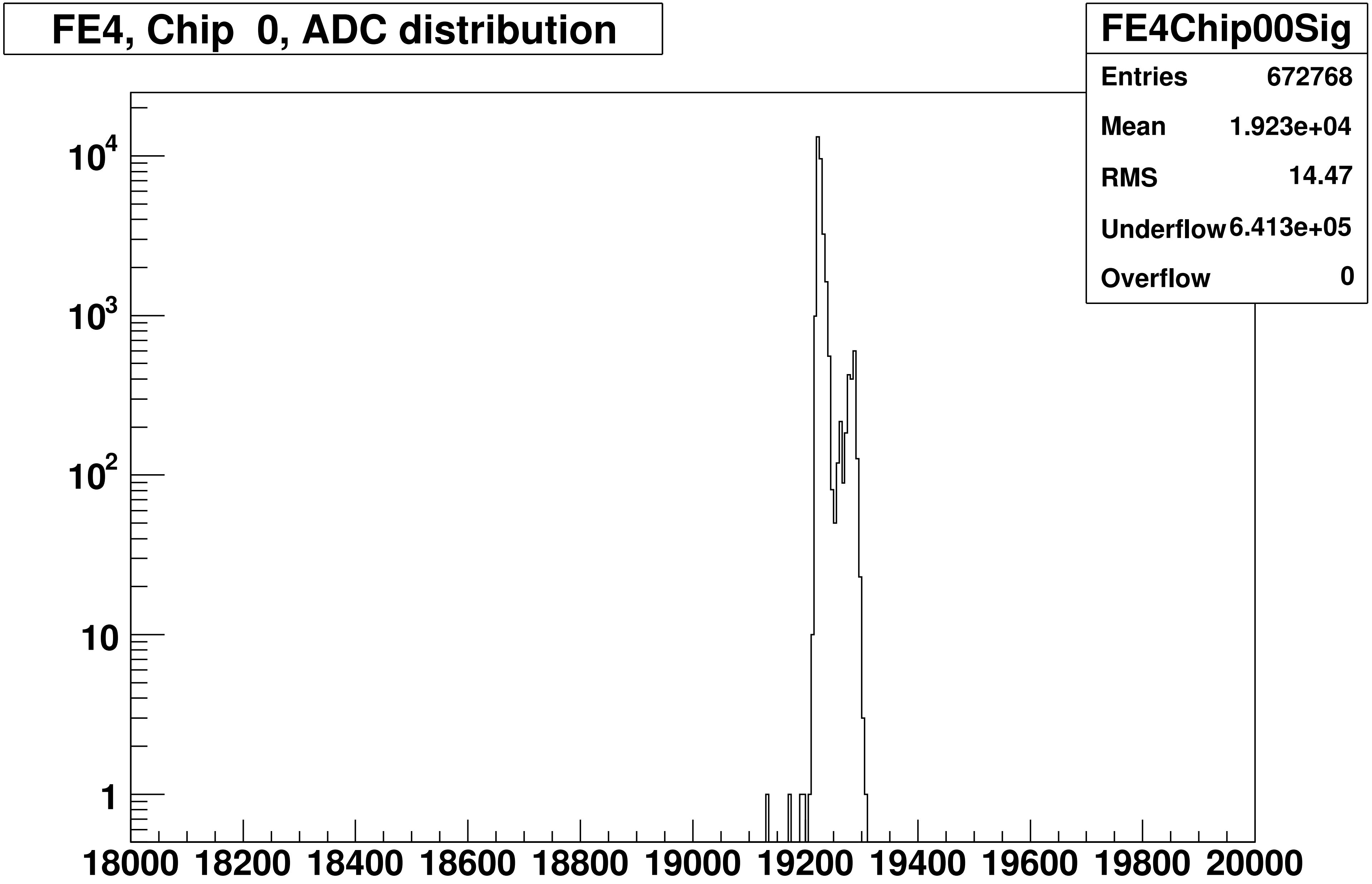
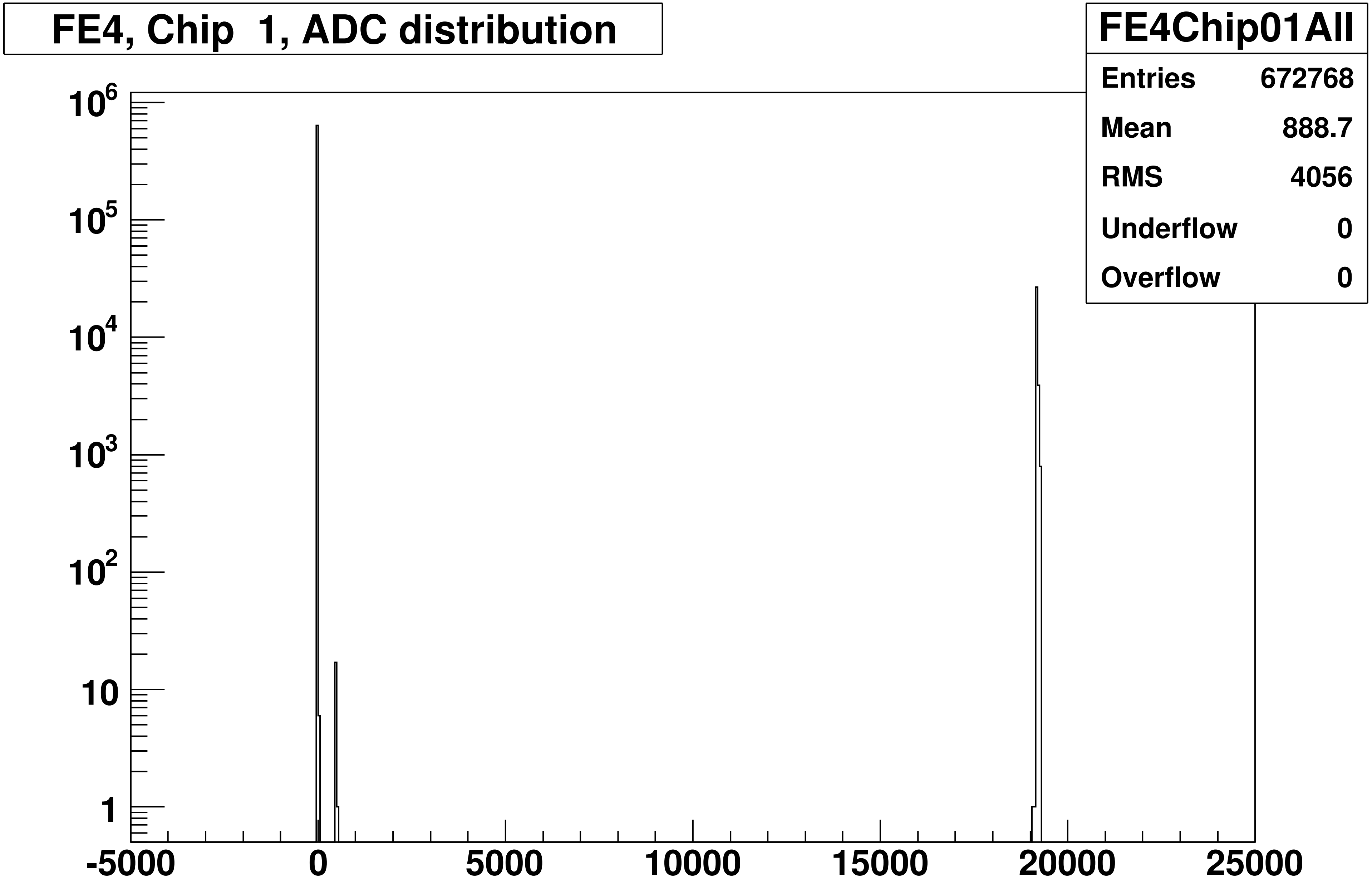


FE4, Chip 0, ADC distribution
FE4Chip00Sig
Entries 672768
Mean 1.923e+04
RMS 14.47
Underflow 6.413e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE4, Chip 1, ADC distribution
FE4Chip01All
Entries 672768
Mean 888.7
RMS 4056
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
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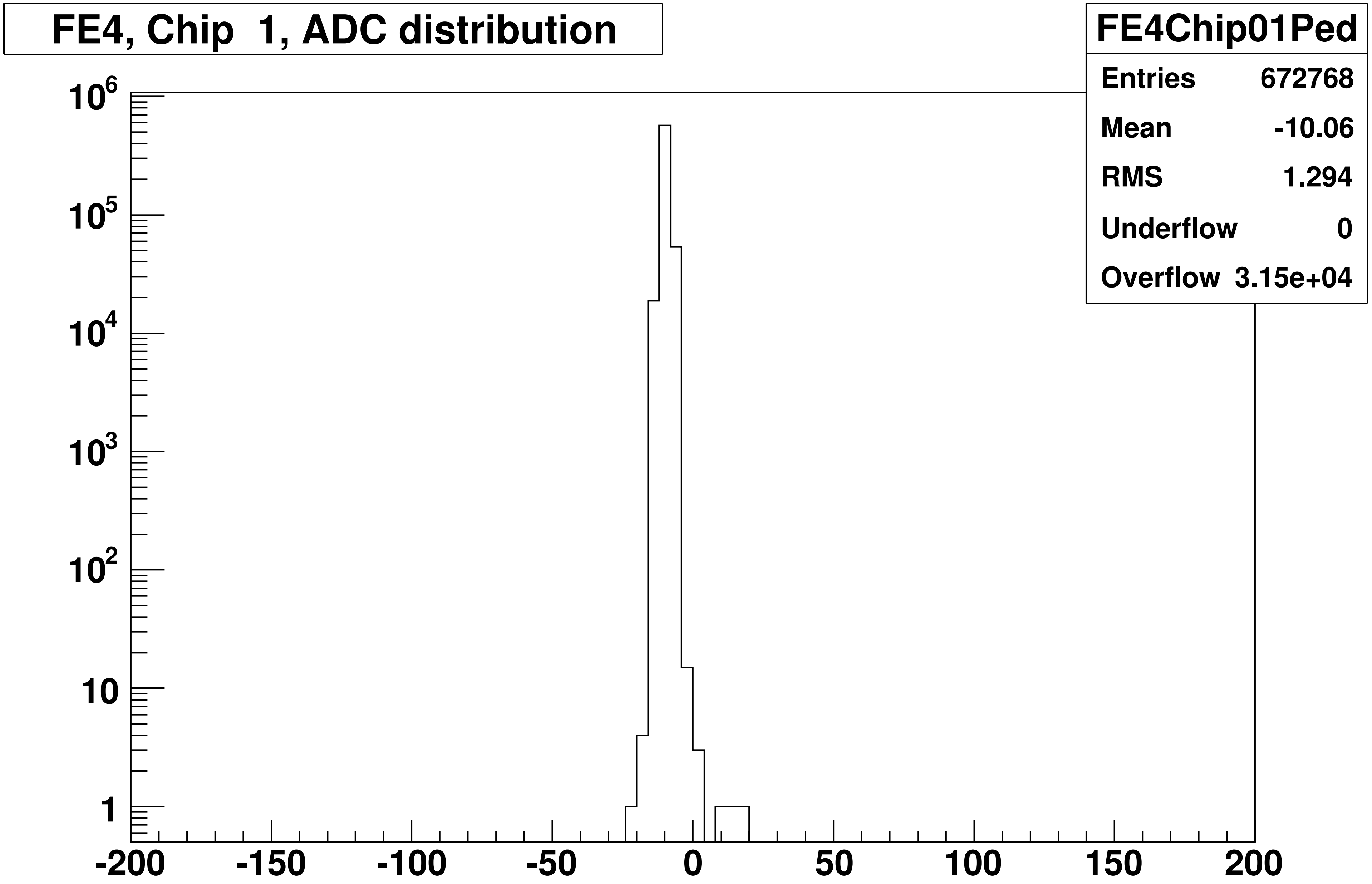
20000
25000


FE4, Chip 1, ADC distribution
FE4Chip01Ped
Entries 672768
Mean -10.06
RMS 1.294
Underflow 0
Overflow 3.15e+04
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10^5
10^4
10^3
10^2
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-100
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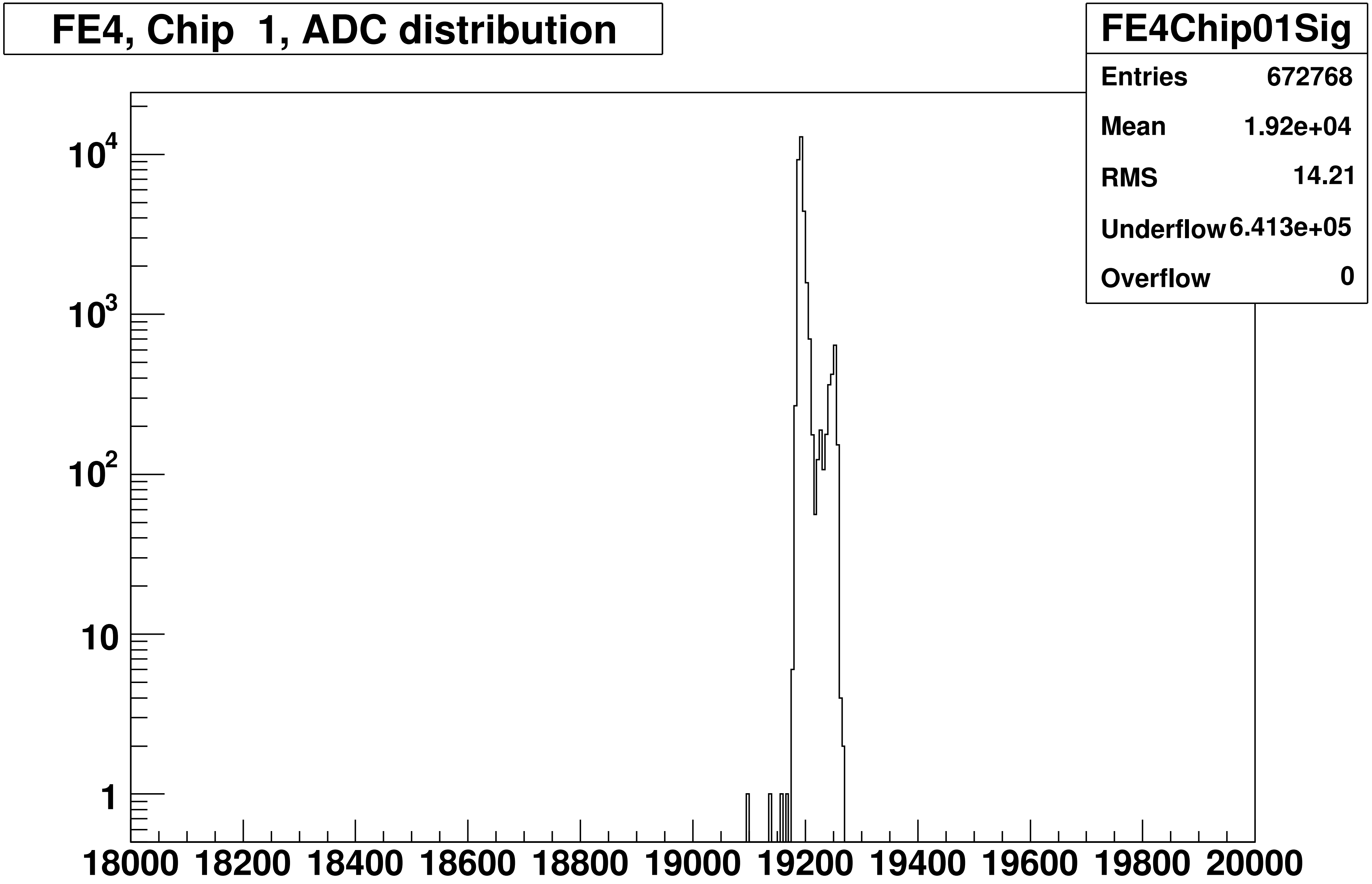
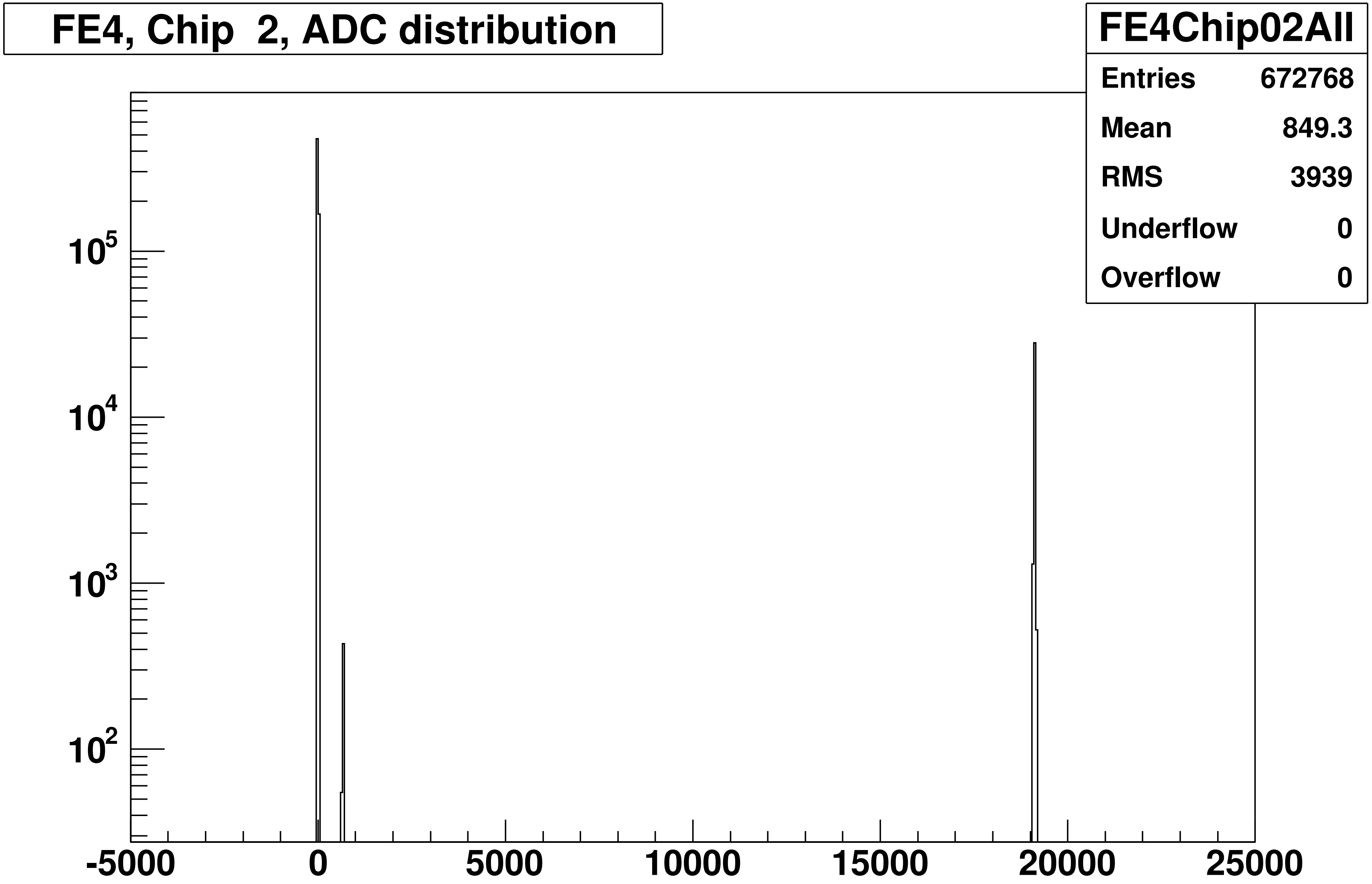
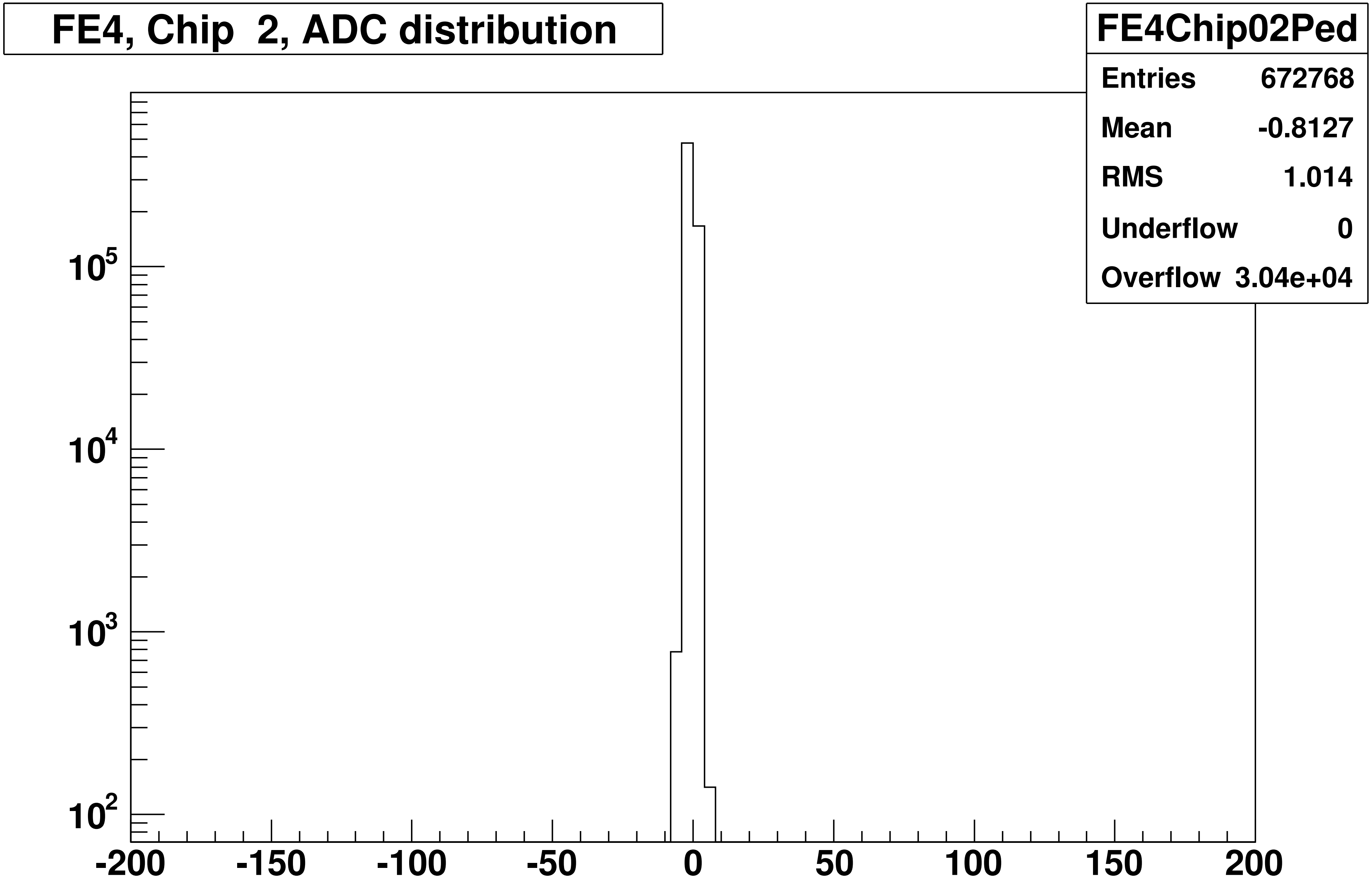
50
100
150
200



FE4, Chip 1, ADC distribution
FE4Chip01Sig
Entries 672768
Mean 1.92e+04
RMS 14.21
Underflow 6.413e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000



FE4, Chip 2, ADC distribution
FE4Chip02All
Entries 672768
Mean 849.3
RMS 3939
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000



FE4, Chip 2, ADC distribution
FE4Chip02Ped
Entries 672768
Mean -0.8127
RMS 1.014
Underflow 0
Overflow 3.04e+04
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10^4
10^3
10^2
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-100
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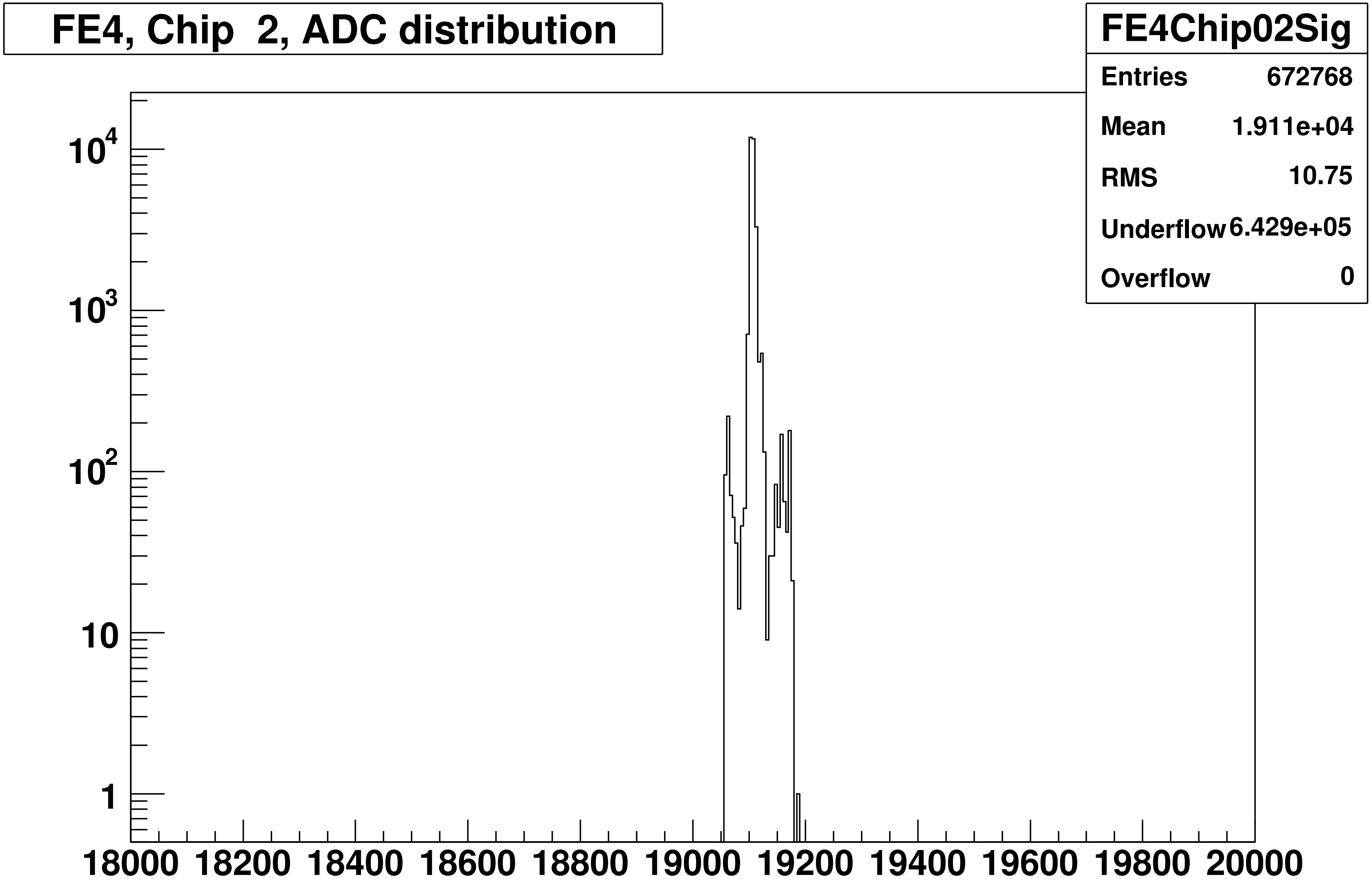
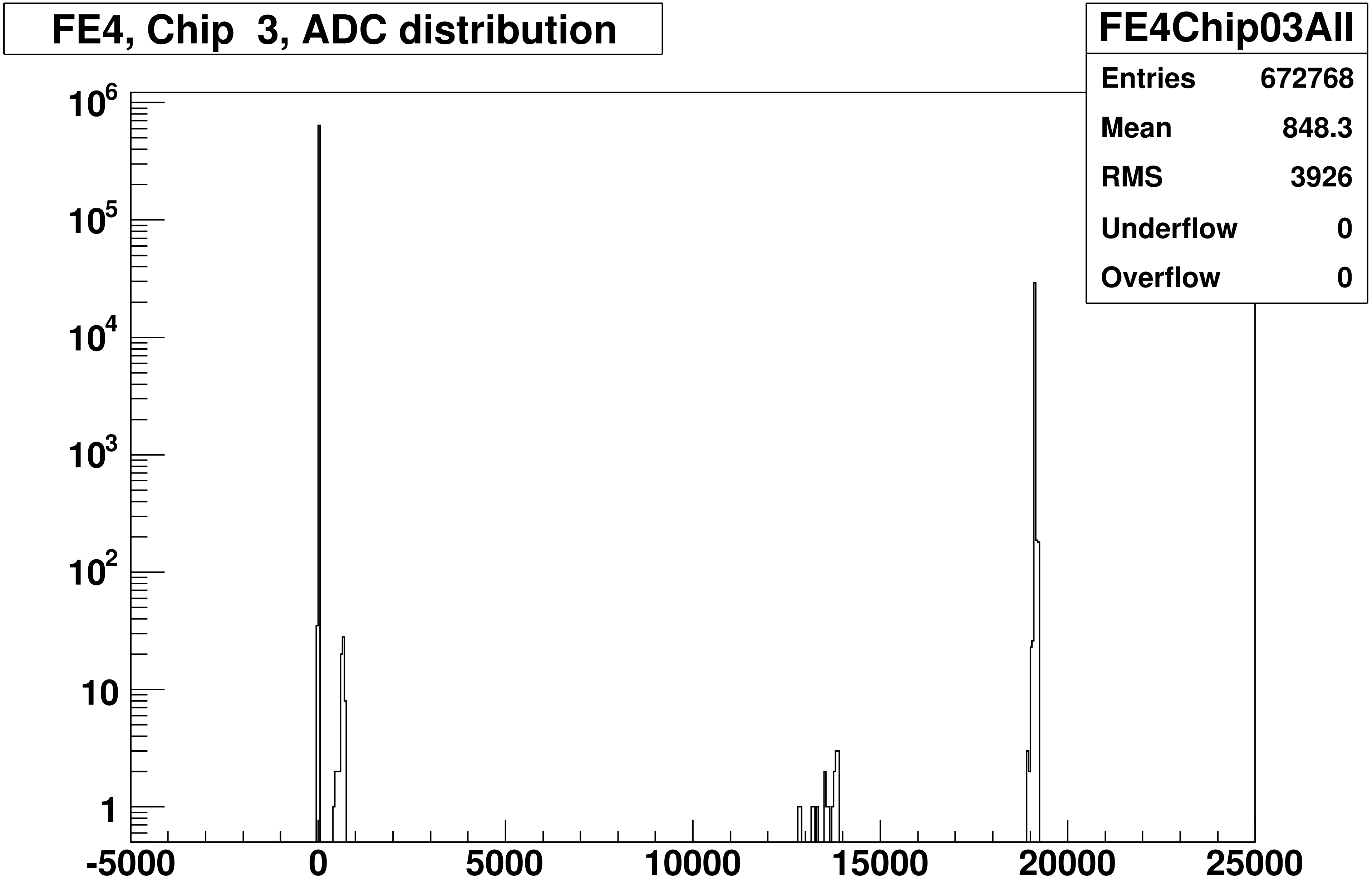
100
150
200



FE4, Chip 2, ADC distribution
FE4Chip02Sig
Entries 672768
Mean 1.911e+04
RMS 10.75
Underflow 6.429e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE4, Chip 3, ADC distribution
FE4Chip03All
Entries 672768
Mean 848.3
RMS 3926
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
1
-5000
0
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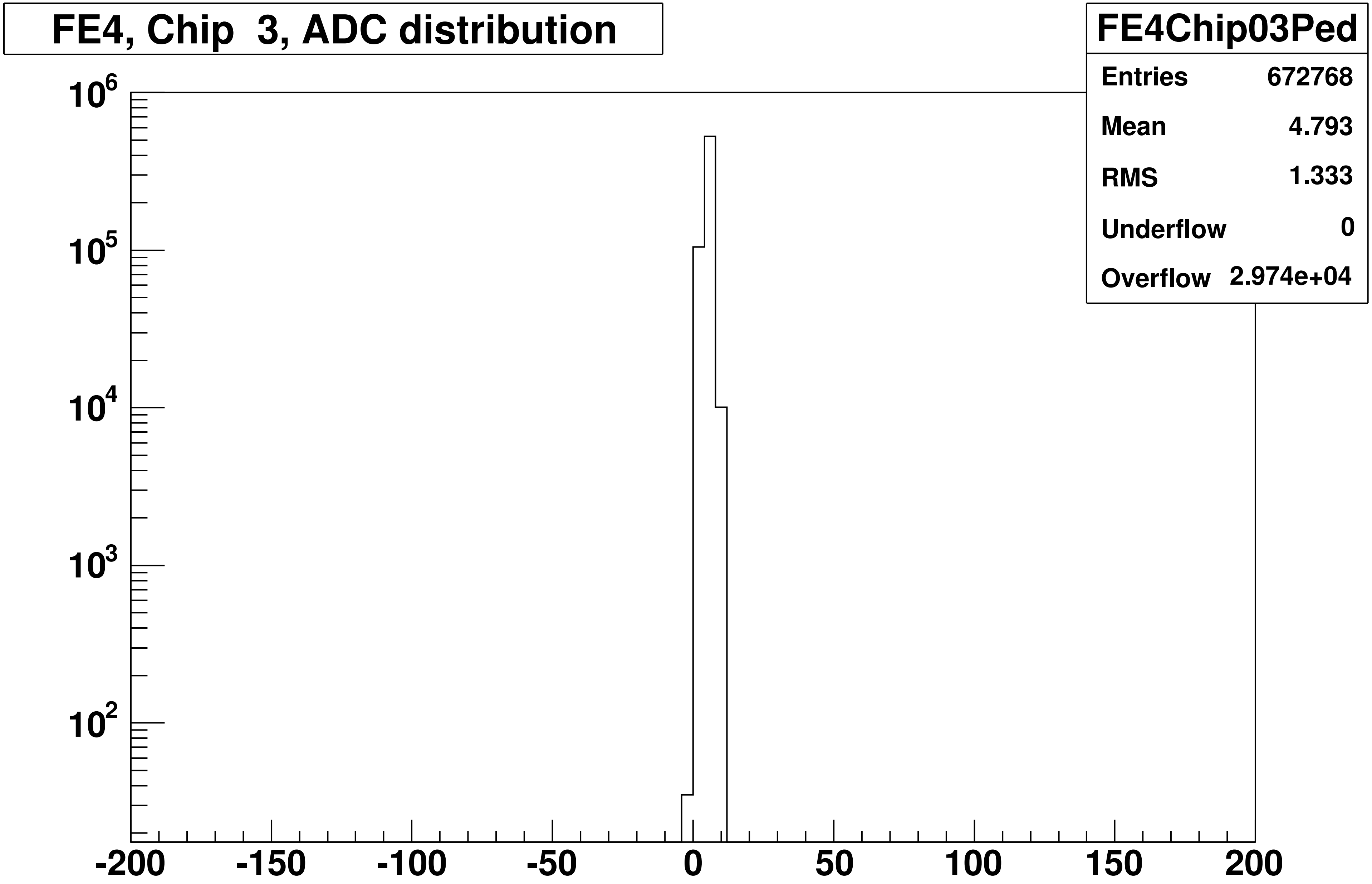
10000
15000
20000
25000



FE4, Chip 3, ADC distribution
FE4Chip03Ped
Entries 672768
Mean 4.793
RMS 1.333
Underflow 0
Overflow 2.974e+04
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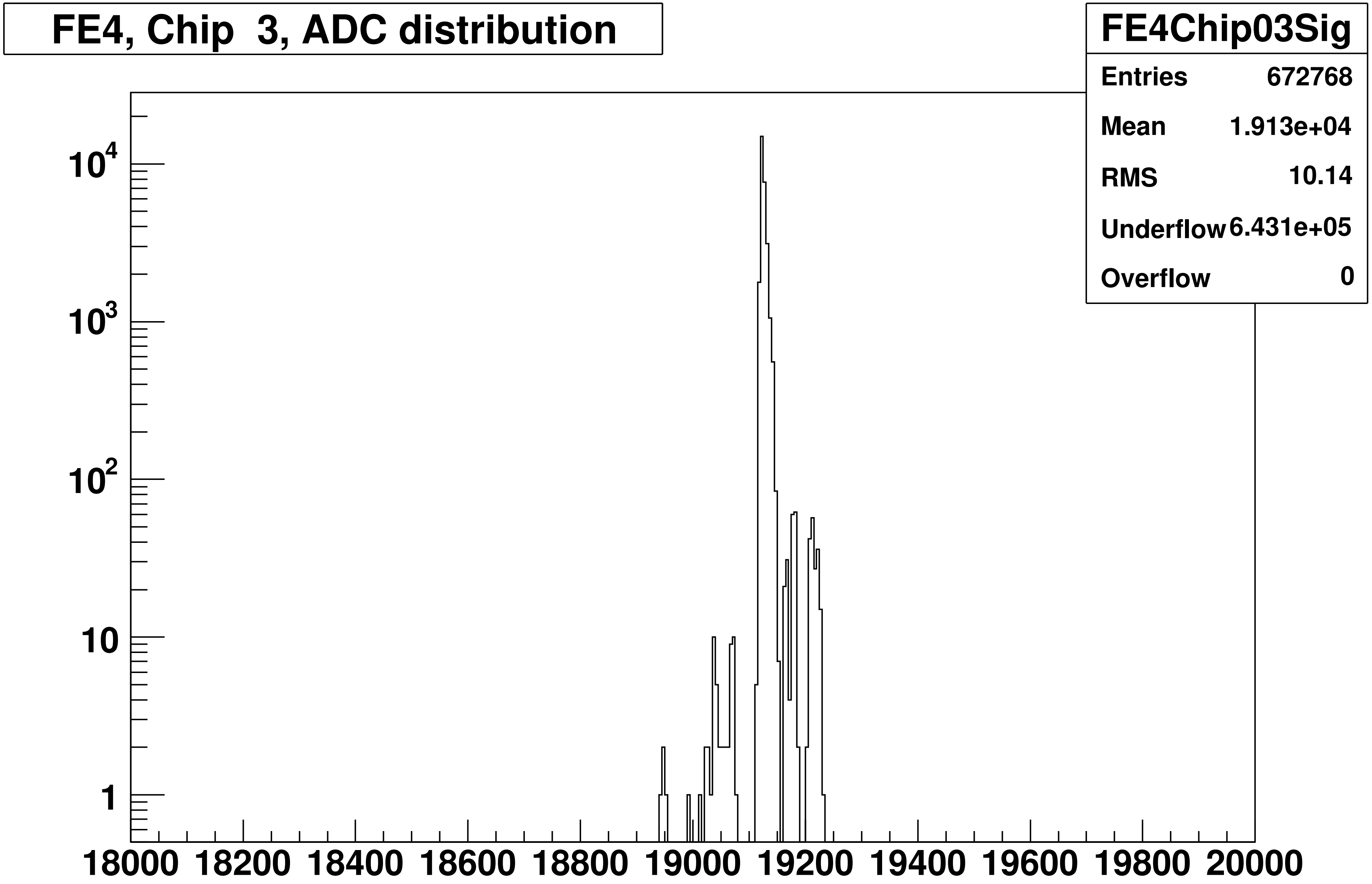
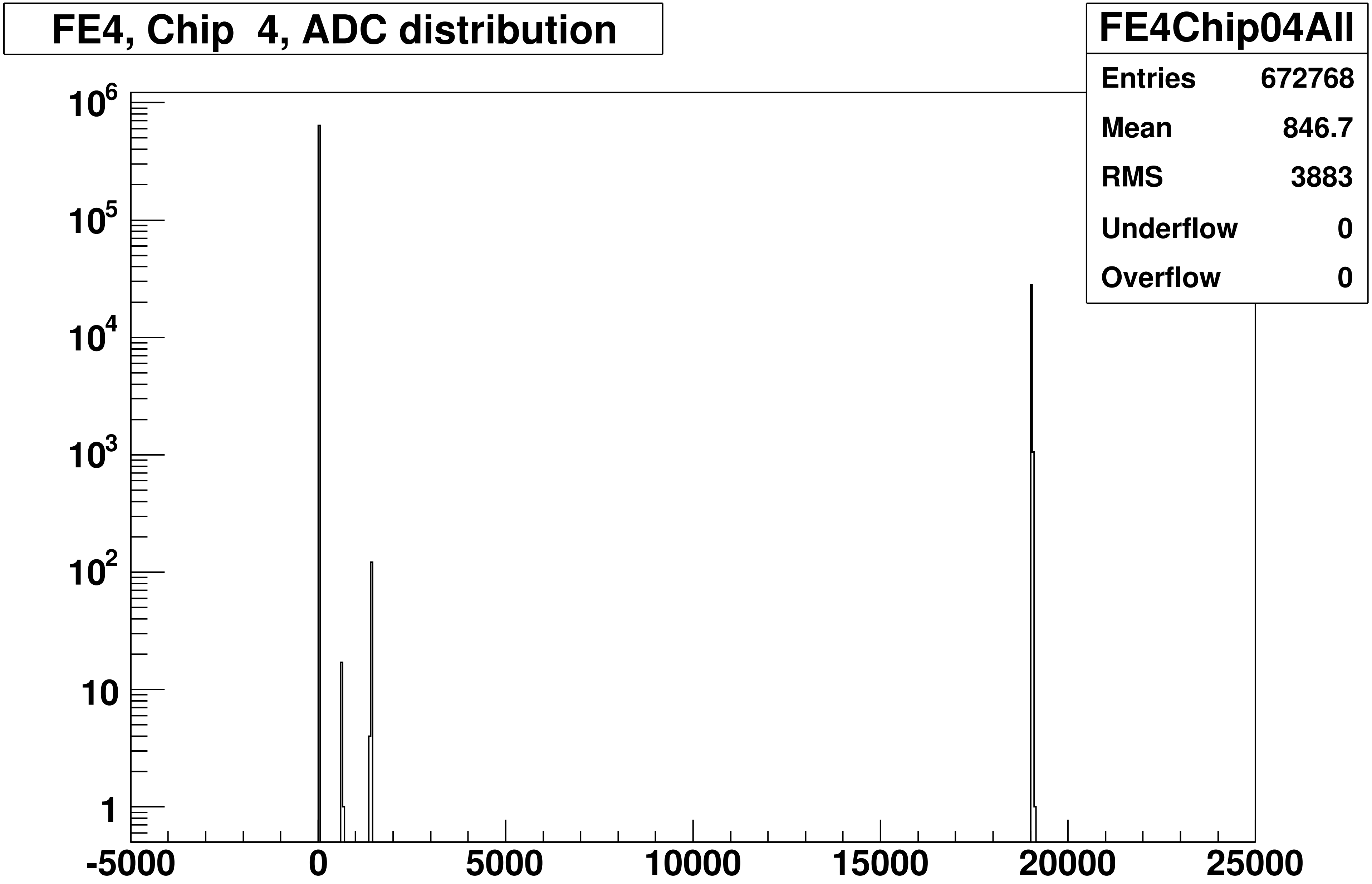
10^5
10^4
10^3
10^2
-200
-150
-100
-50
0
50
100
150
200



FE4, Chip 3, ADC distribution
FE4Chip03Sig
Entries 672768
Mean 1.913e+04
RMS 10.14
Underflow 6.431e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE4, Chip 4, ADC distribution
FE4Chip04All
Entries 672768
Mean 846.7
RMS 3883
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
1
-5000
0
5000
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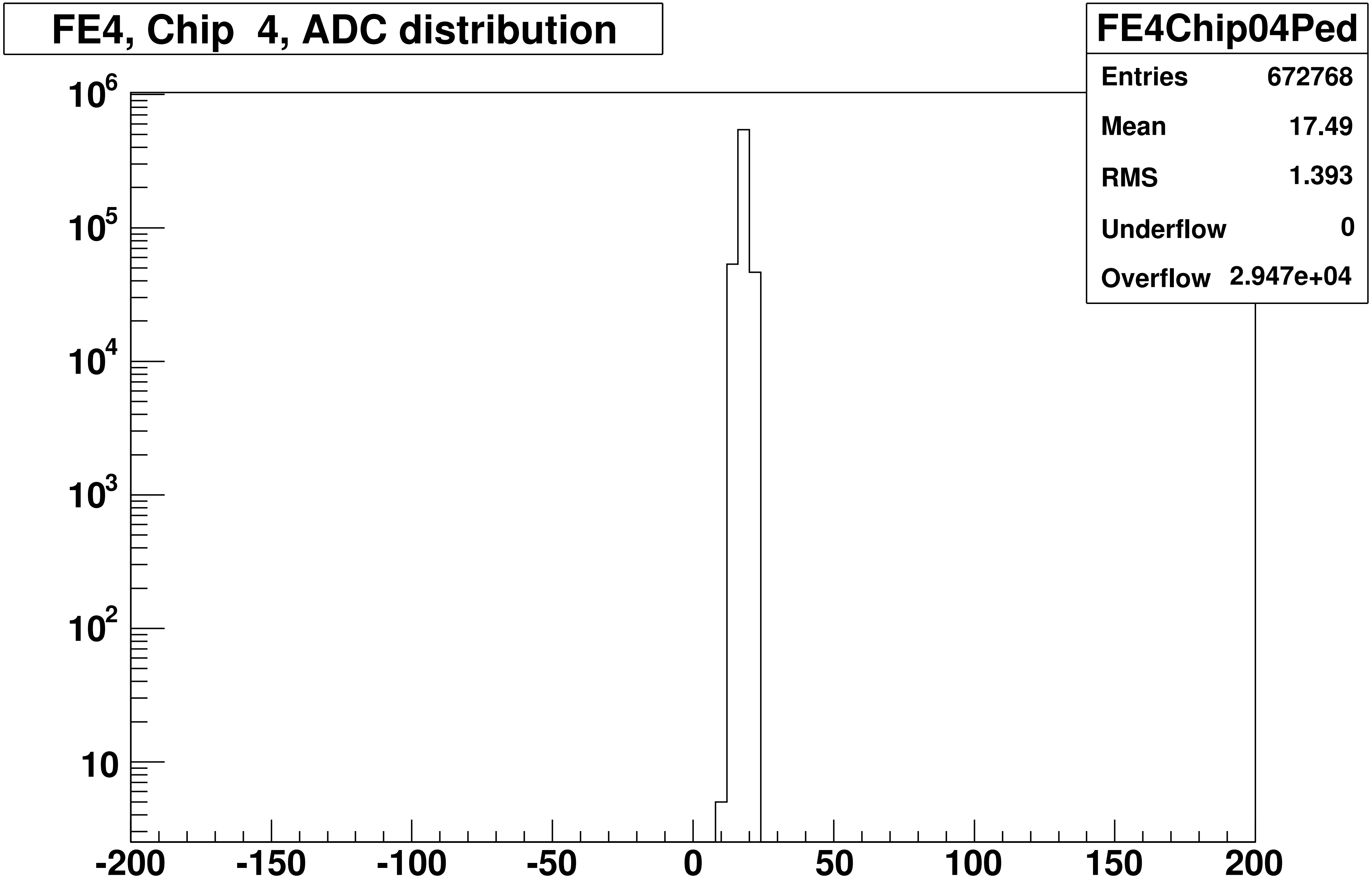
15000
20000
25000


FE4, Chip 4, ADC distribution
FE4Chip04Ped
Entries 672768
Mean 17.49
RMS 1.393
Underflow 0
Overflow 2.947e+04
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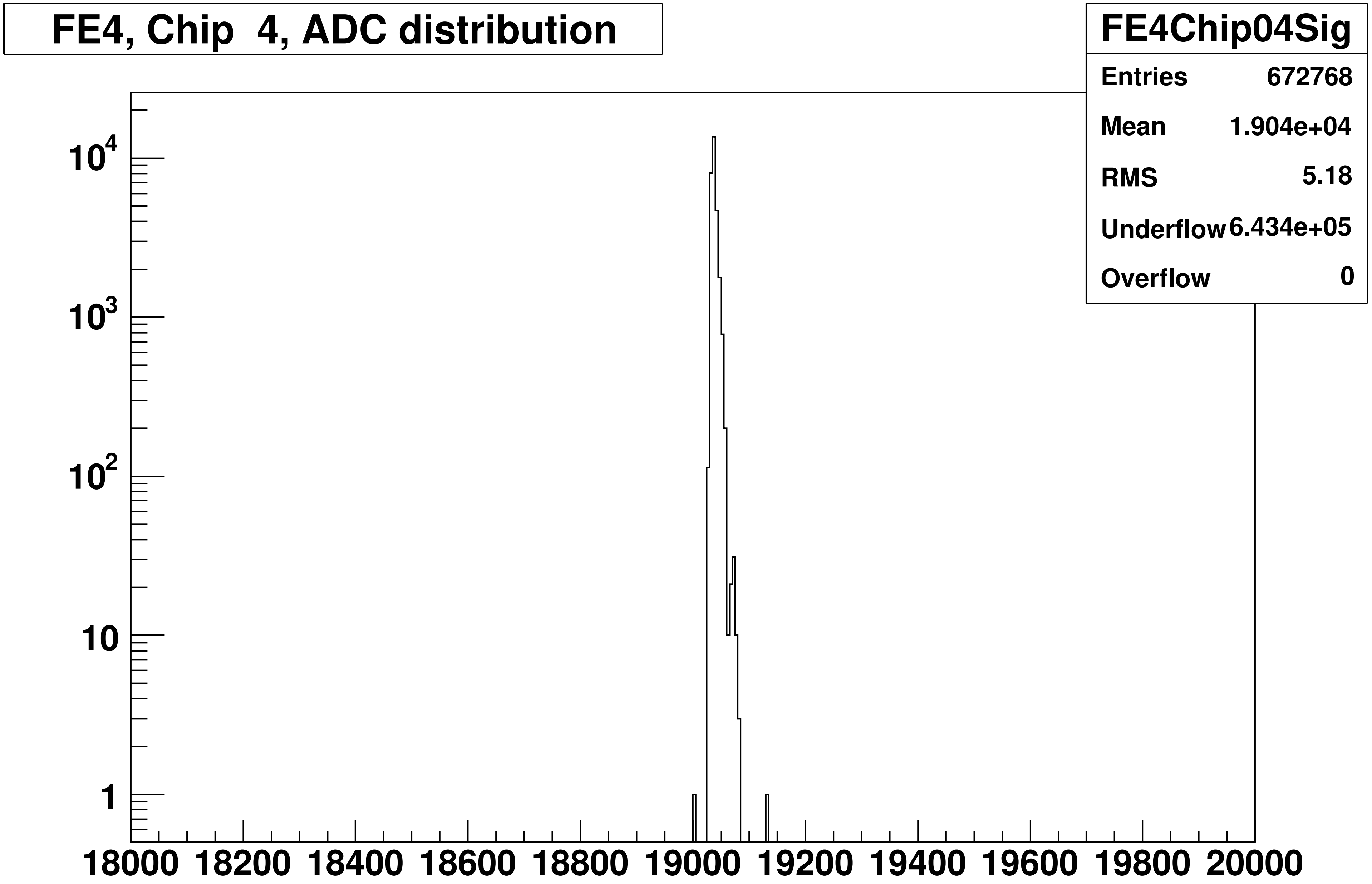
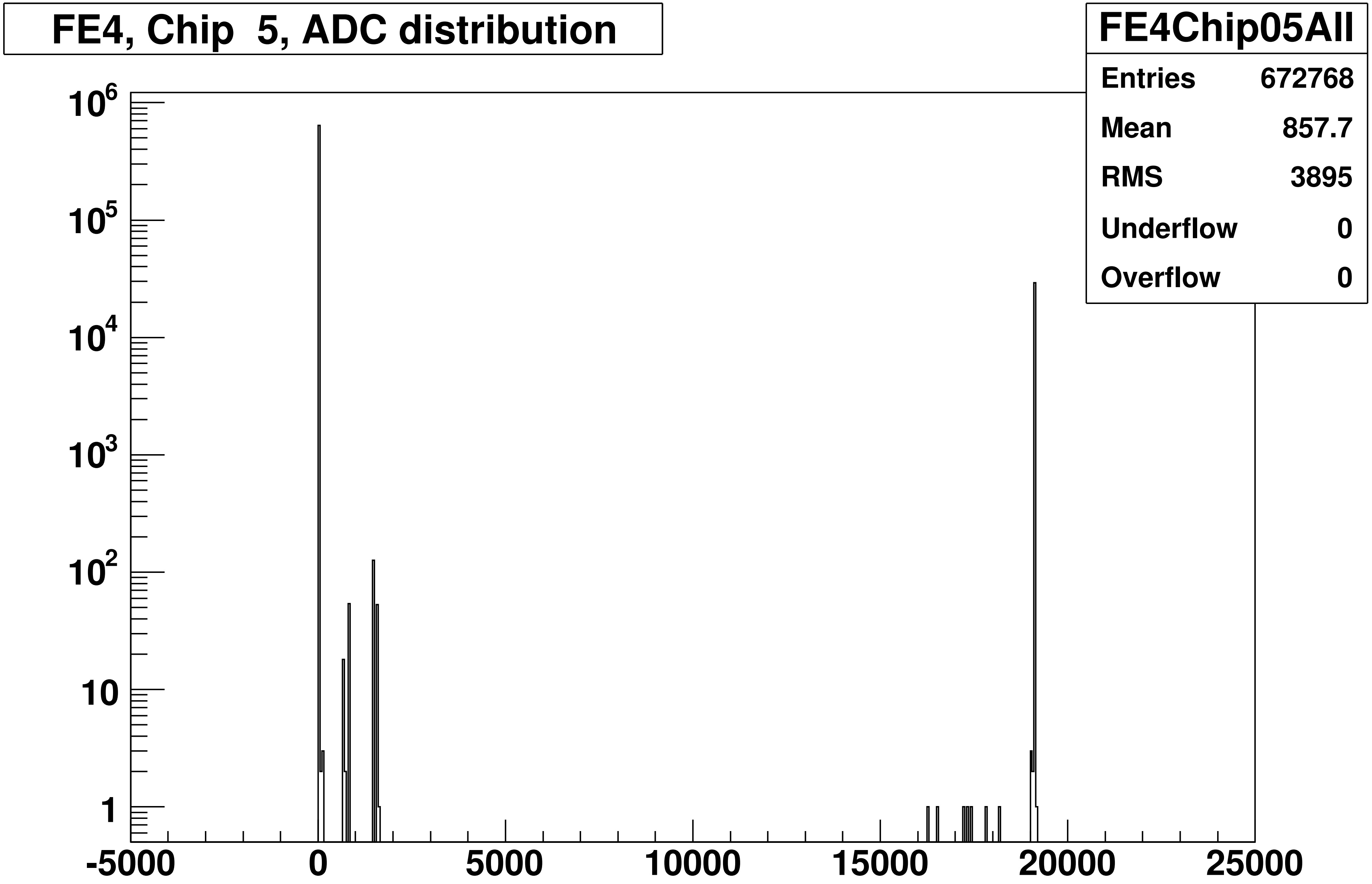
0
50
100
150
200


FE4, Chip 4, ADC distribution
FE4Chip04Sig
Entries 672768
Mean 1.904e+04
RMS 5.18
Underflow 6.434e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE4, Chip 5, ADC distribution
FE4Chip05All
Entries 672768
Mean 857.7
RMS 3895
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
1
-5000
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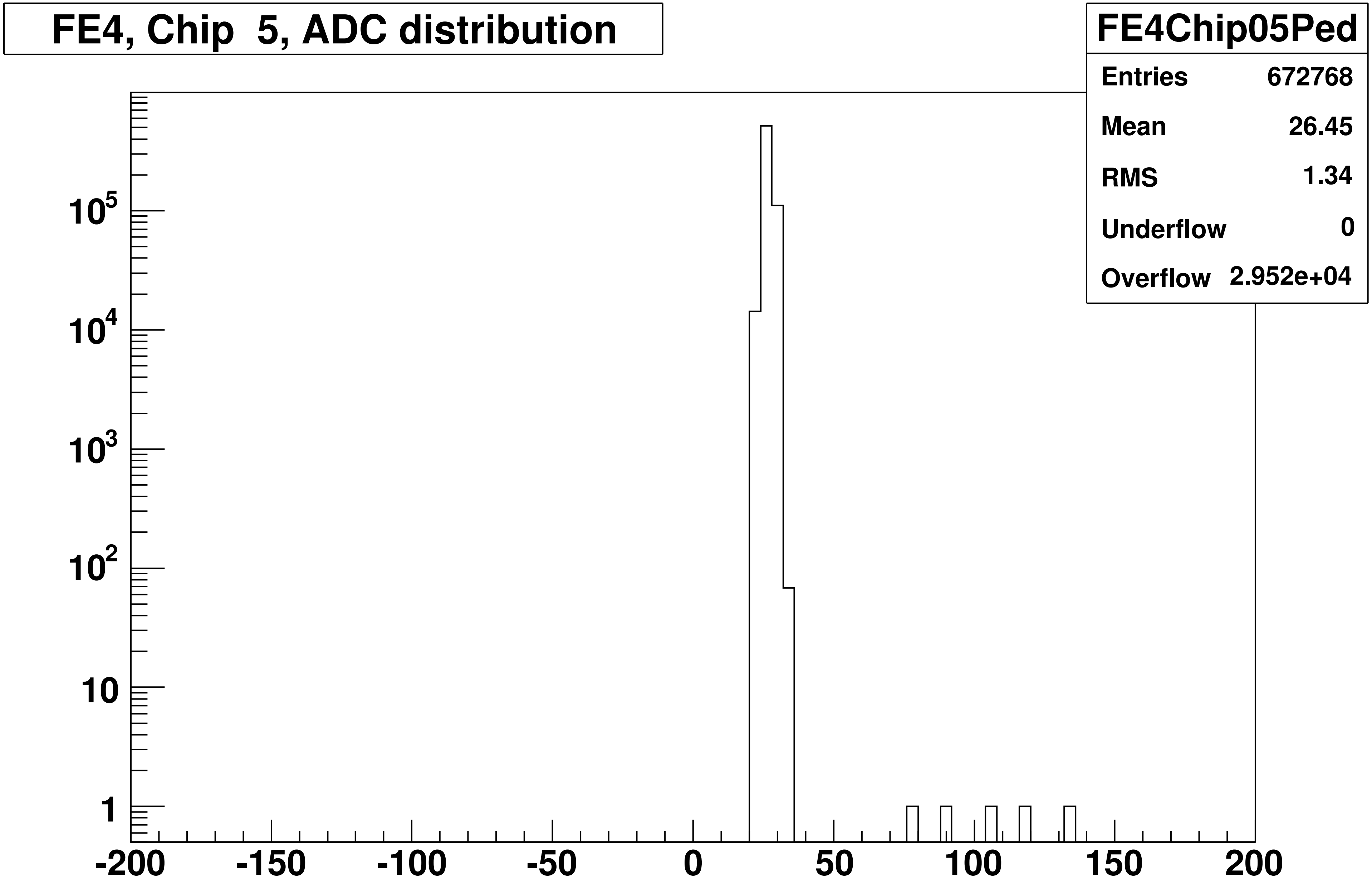
FE4, Chip 5, ADC distribution
FE4Chip05Ped
Entries 672768
Mean 26.45
RMS 1.34
Underflow 0
Overflow 2.952e+04
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10^3
10^2
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-150
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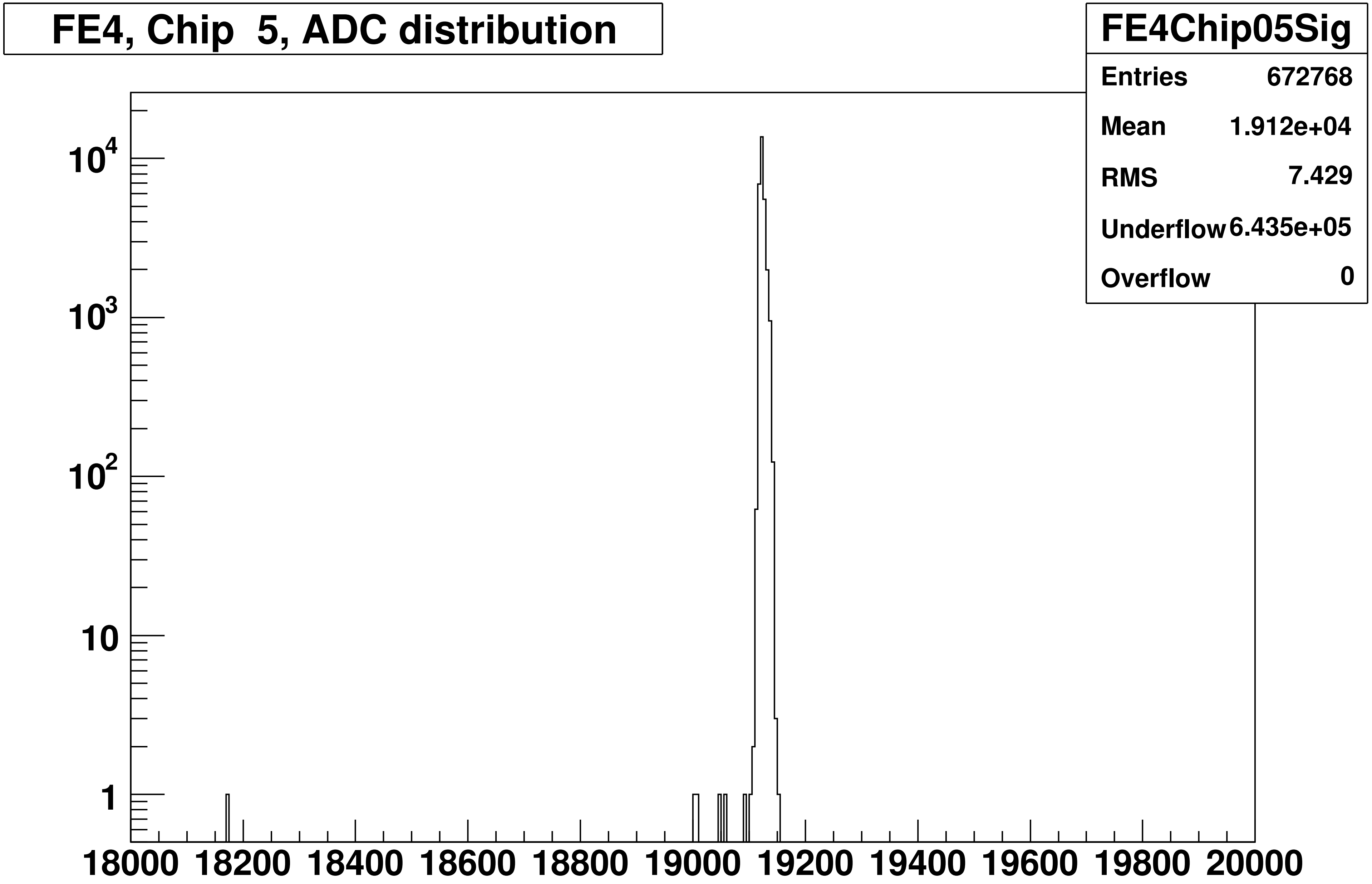
FE4, Chip 5, ADC distribution
FE4Chip05Sig
Entries 672768
Mean 1.912e+04
RMS 7.429
Underflow 6.435e+05
Overflow 0
10^4
10^3
10^2
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18400
18600
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19000
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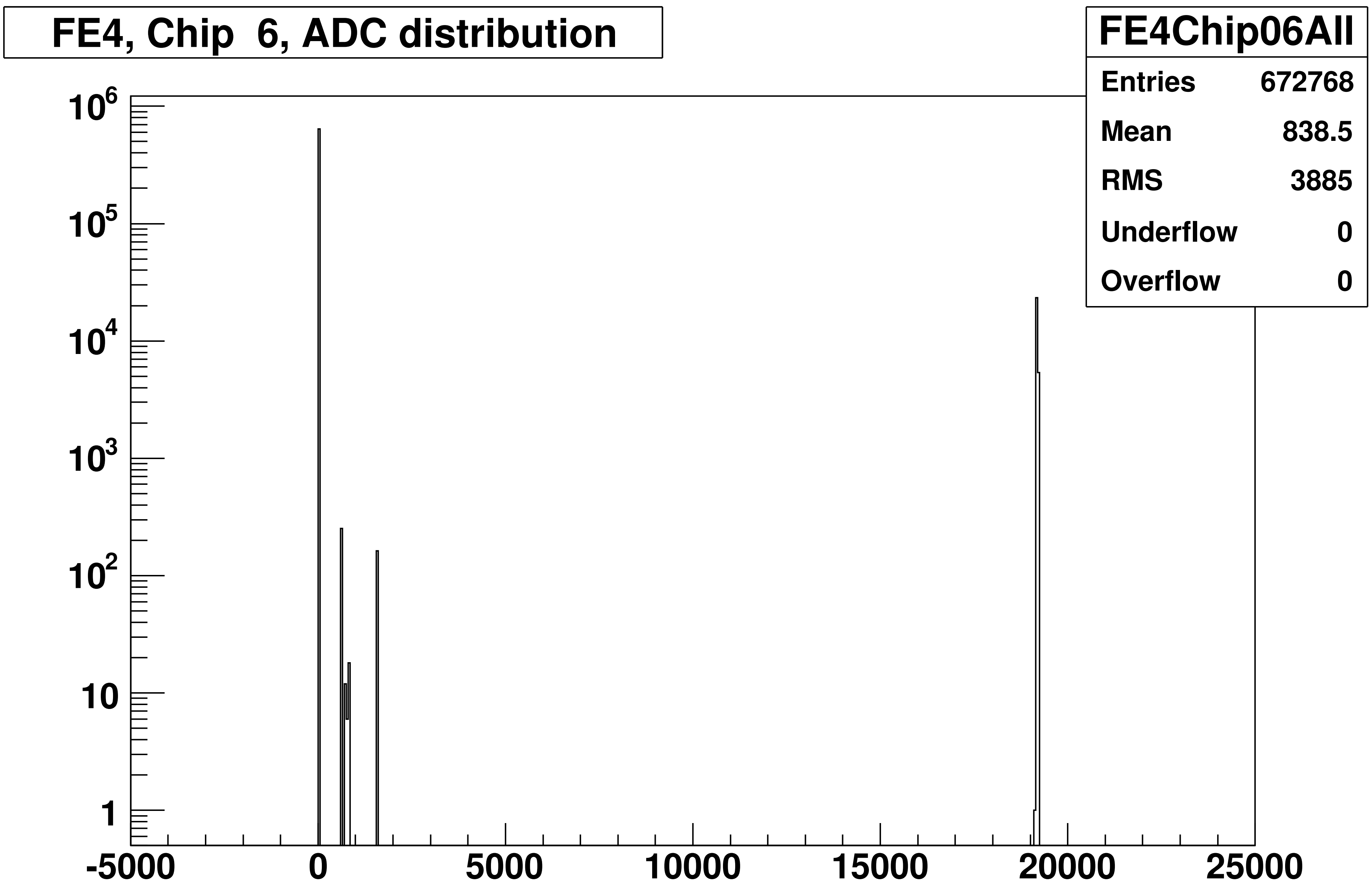

FE4, Chip 6, ADC distribution
FE4Chip06All
Entries 672768
Mean 838.5
RMS 3885
Underflow 0
Overflow 0
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10^4
10^3
10^2
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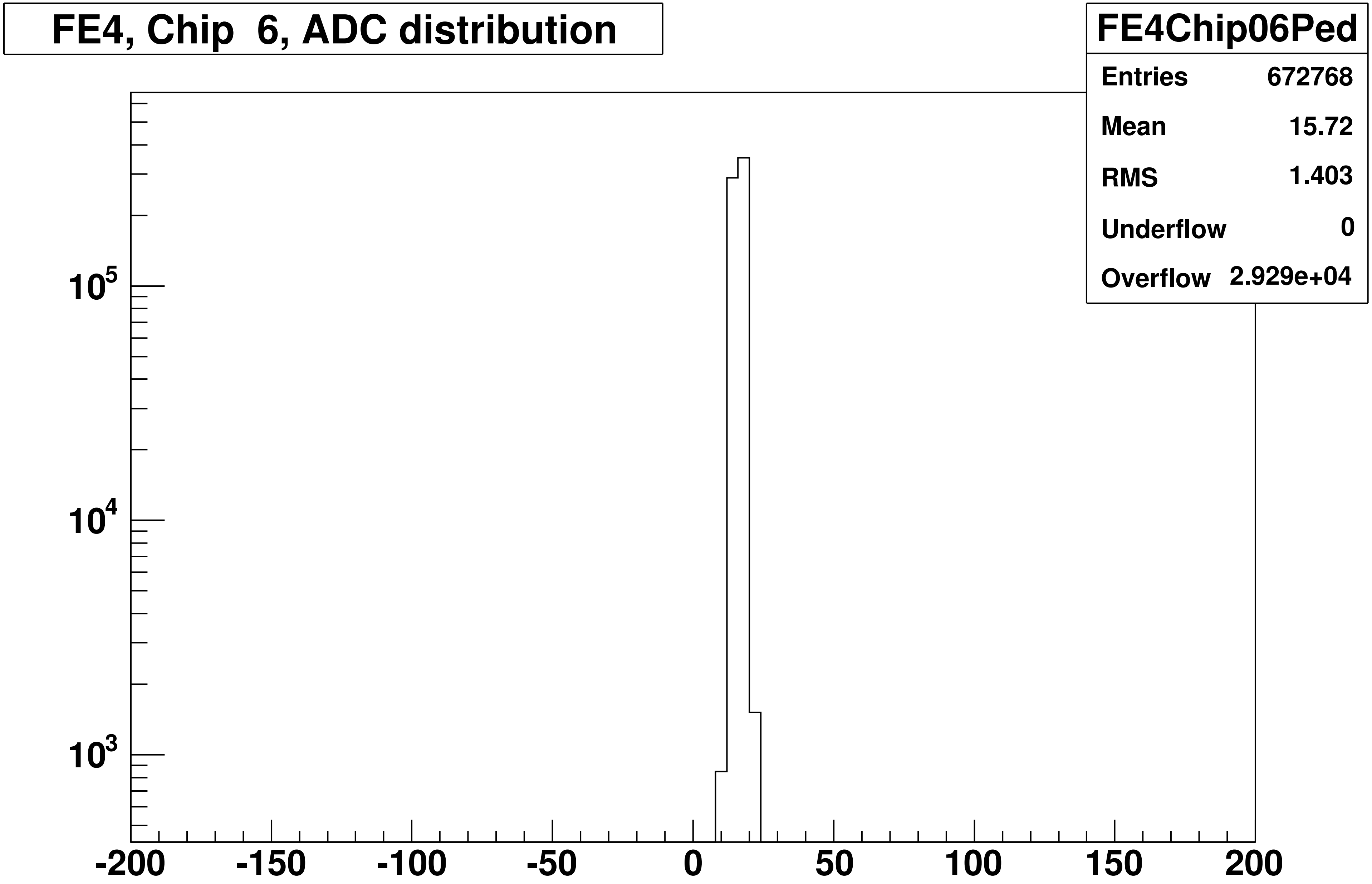

FE4, Chip 6, ADC distribution
FE4Chip06Ped
Entries 672768
Mean 15.72
RMS 1.403
Underflow 0
Overflow 2.929e+04
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10^4
10^3
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0
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150
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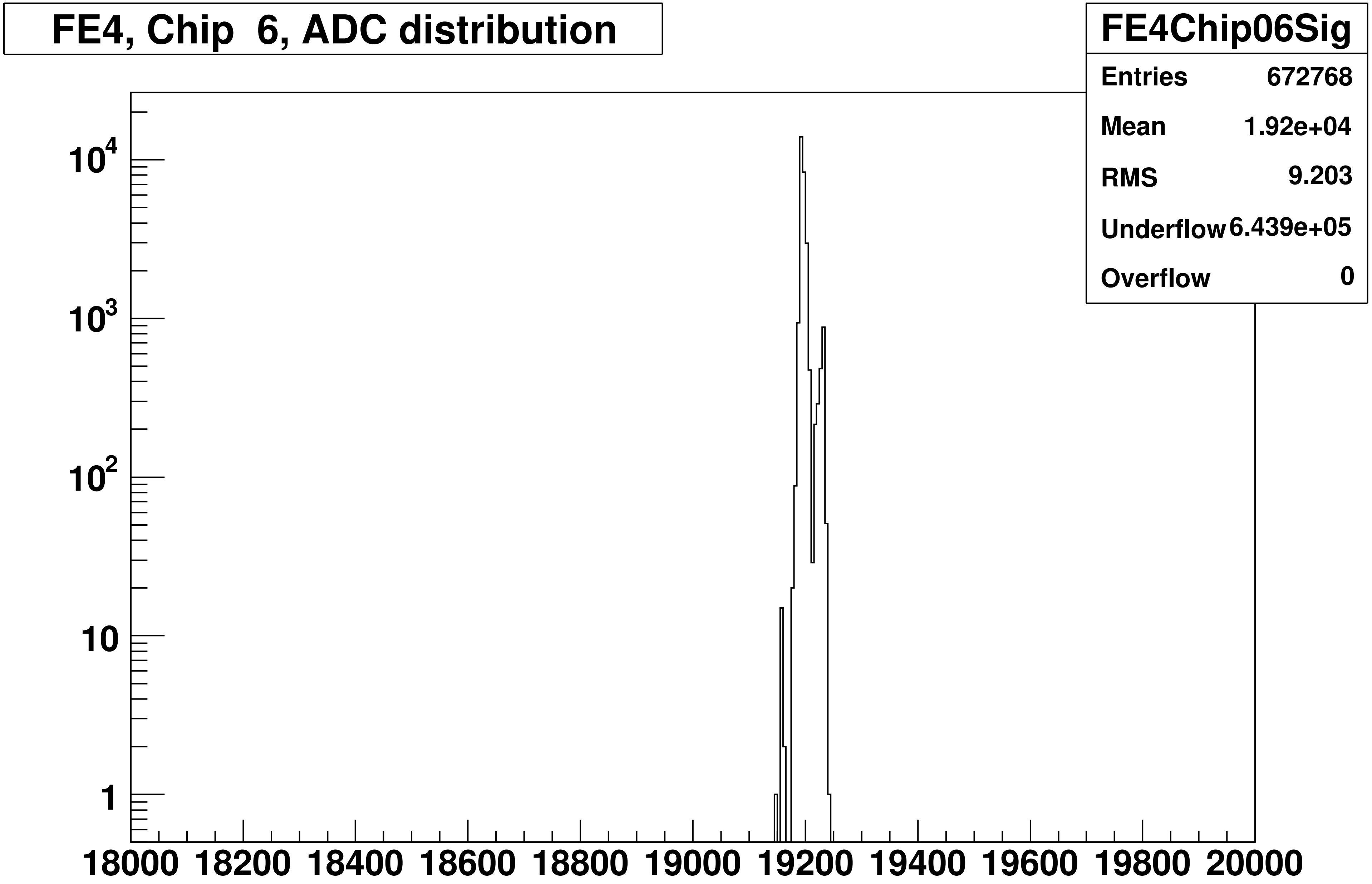
FE4, Chip 6, ADC distribution
FE4Chip06Sig
Entries 672768
Mean 1.92e+04
RMS 9.203
Underflow 6.439e+05
Overflow 0
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10^3
10^2
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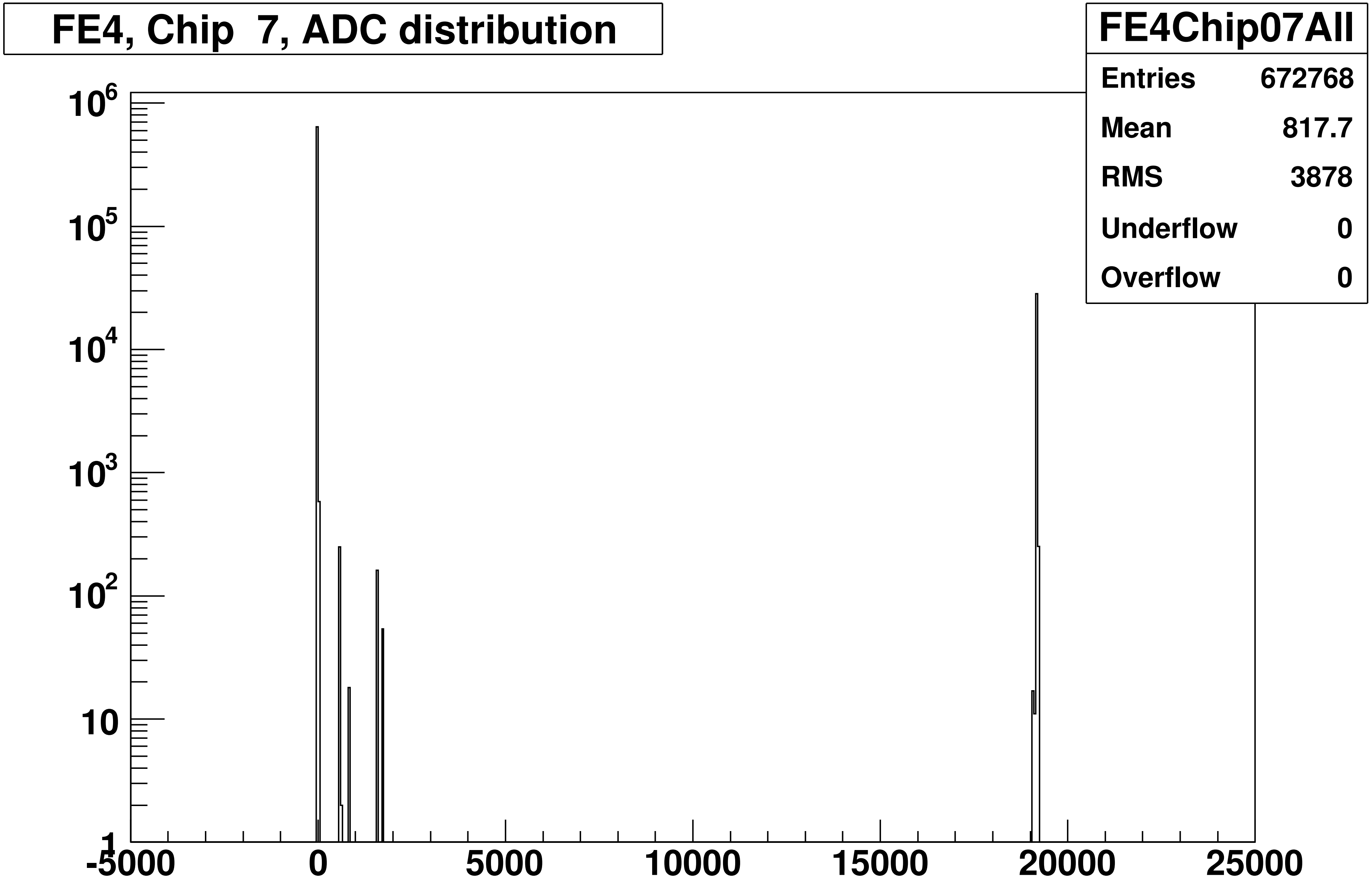
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE4, Chip 7, ADC distribution
FE4Chip07All
Entries 672768
Mean 817.7
RMS 3878
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
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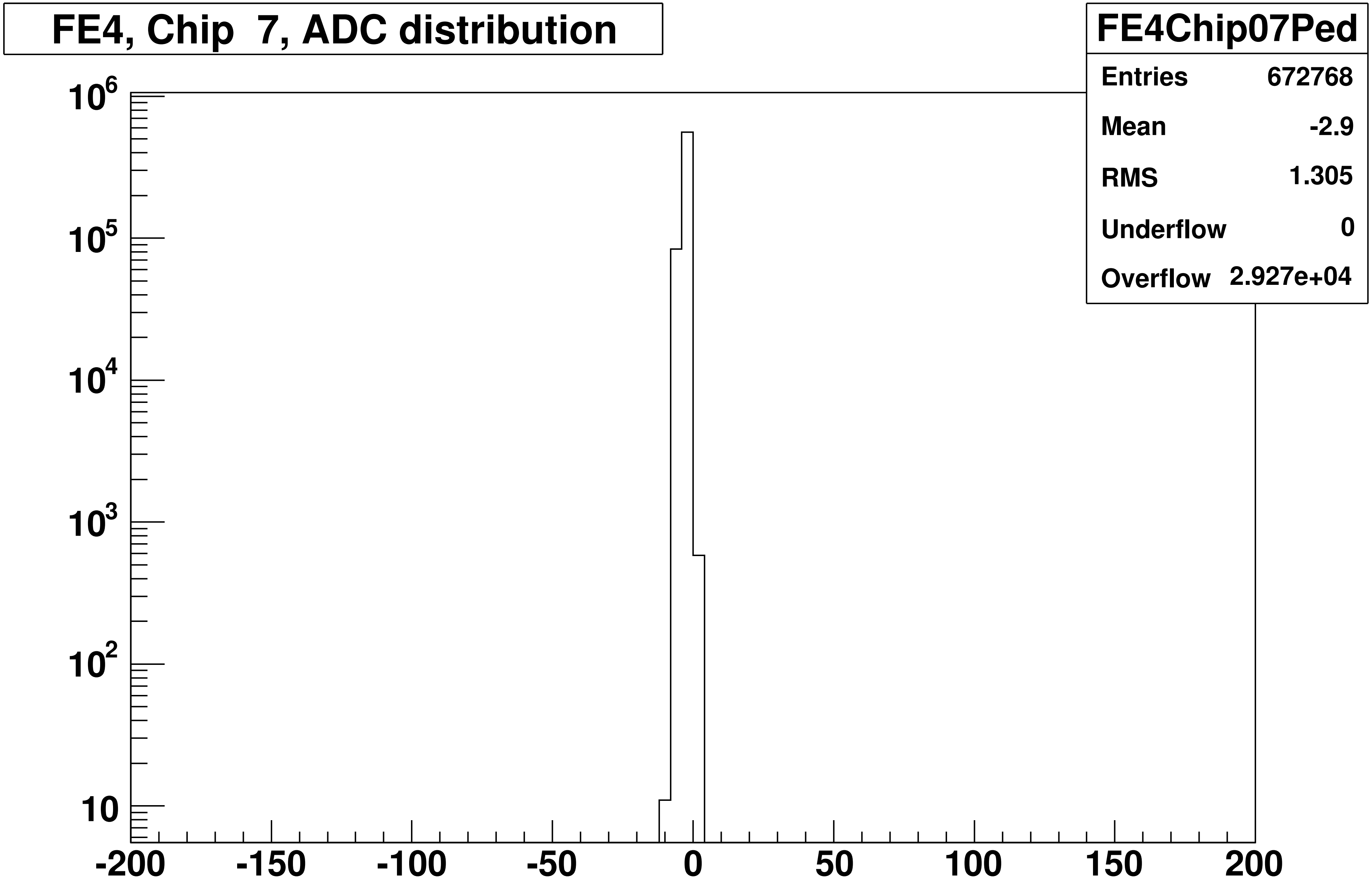

FE4, Chip 7, ADC distribution
FE4Chip07Ped
Entries 672768
Mean -2.9
RMS 1.305
Underflow 0
Overflow 2.927e+04
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10^5
10^4
10^3
10^2
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100
150
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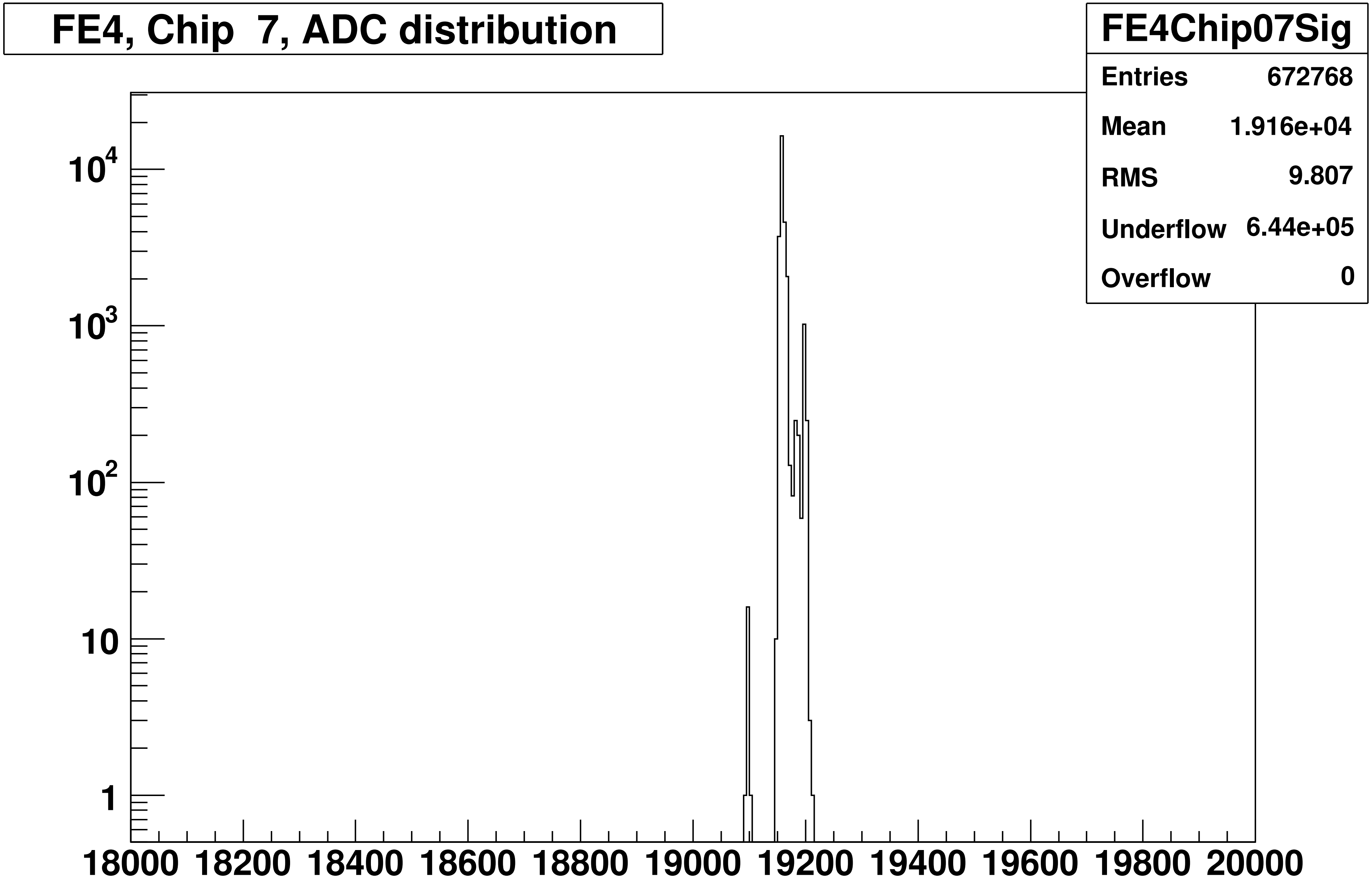
FE4, Chip 7, ADC distribution
FE4Chip07Sig
Entries 672768
Mean 1.916e+04
RMS 9.807
Underflow 6.44e+05
Overflow 0
10^4
10^3
10^2
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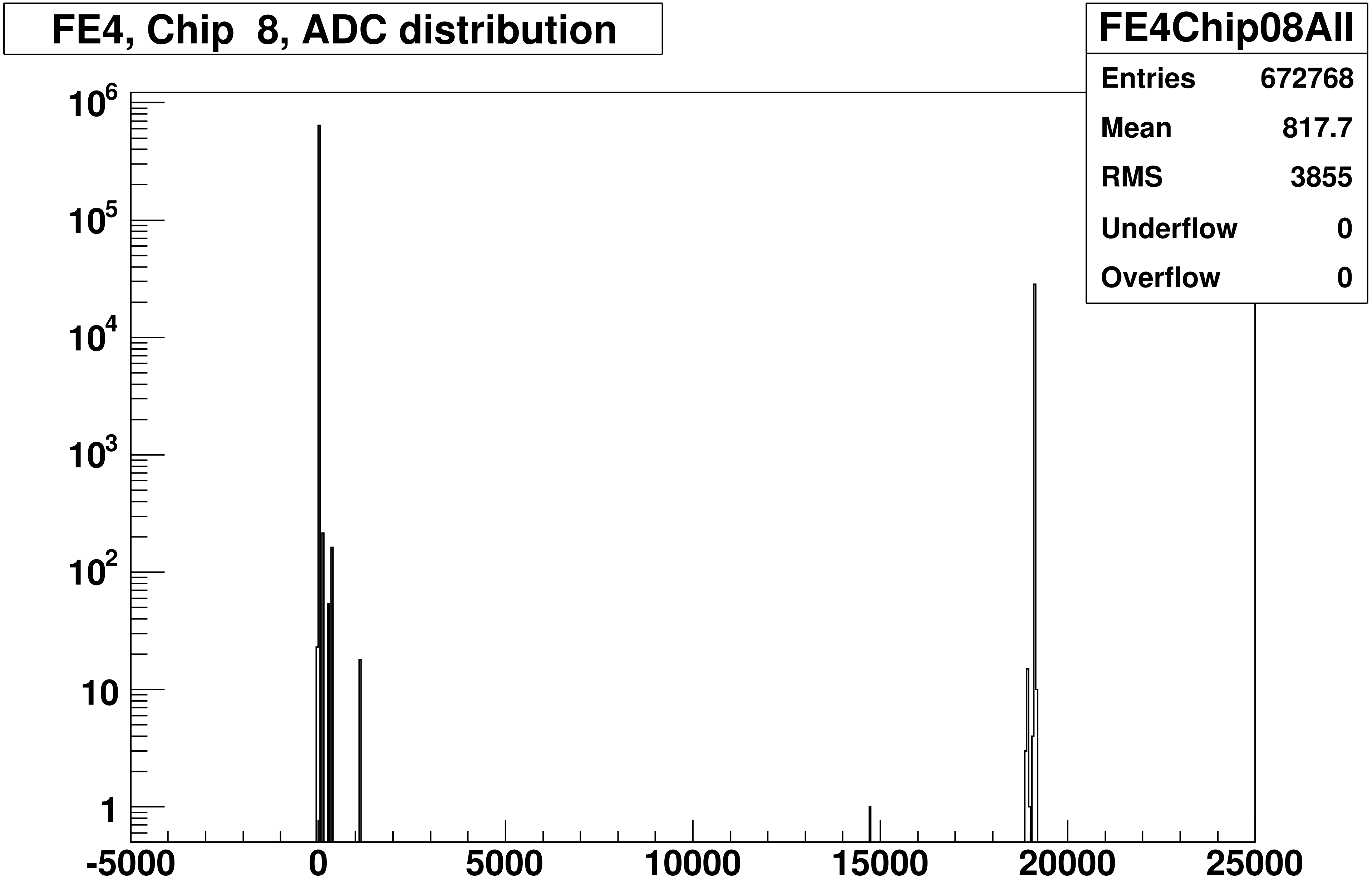
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE4, Chip 8, ADC distribution
FE4Chip08All
Entries 672768
Mean 817.7
RMS 3855
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
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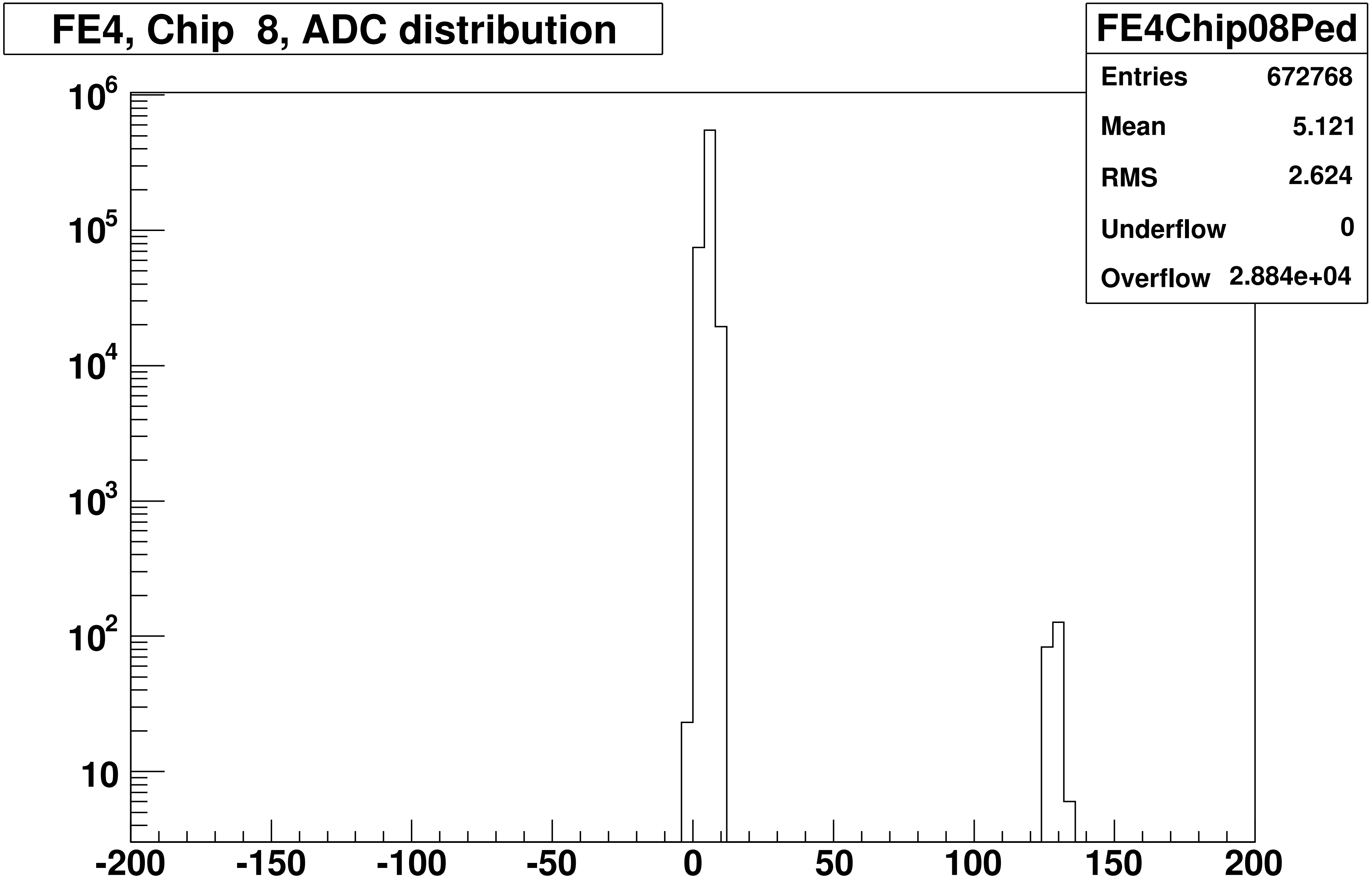
FE4, Chip 8, ADC distribution
FE4Chip08Ped
Entries 672768
Mean 5.121
RMS 2.624
Underflow 0
Overflow 2.884e+04
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10^5
10^4
10^3
10^2
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-200
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0
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100
150
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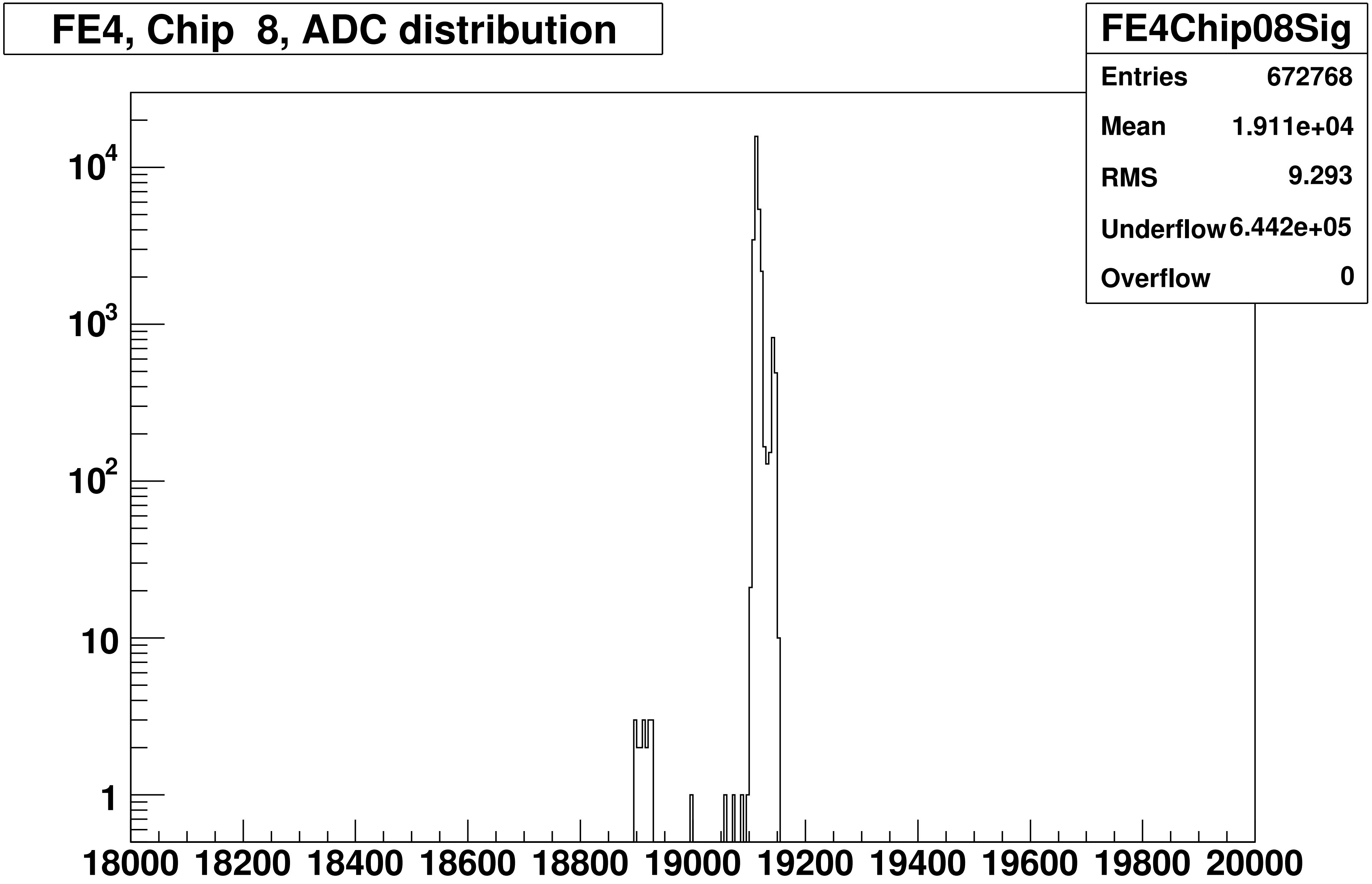
FE4, Chip 8, ADC distribution
FE4Chip08Sig
Entries 672768
Mean 1.911e+04
RMS 9.293
Underflow 6.442e+05
Overflow 0
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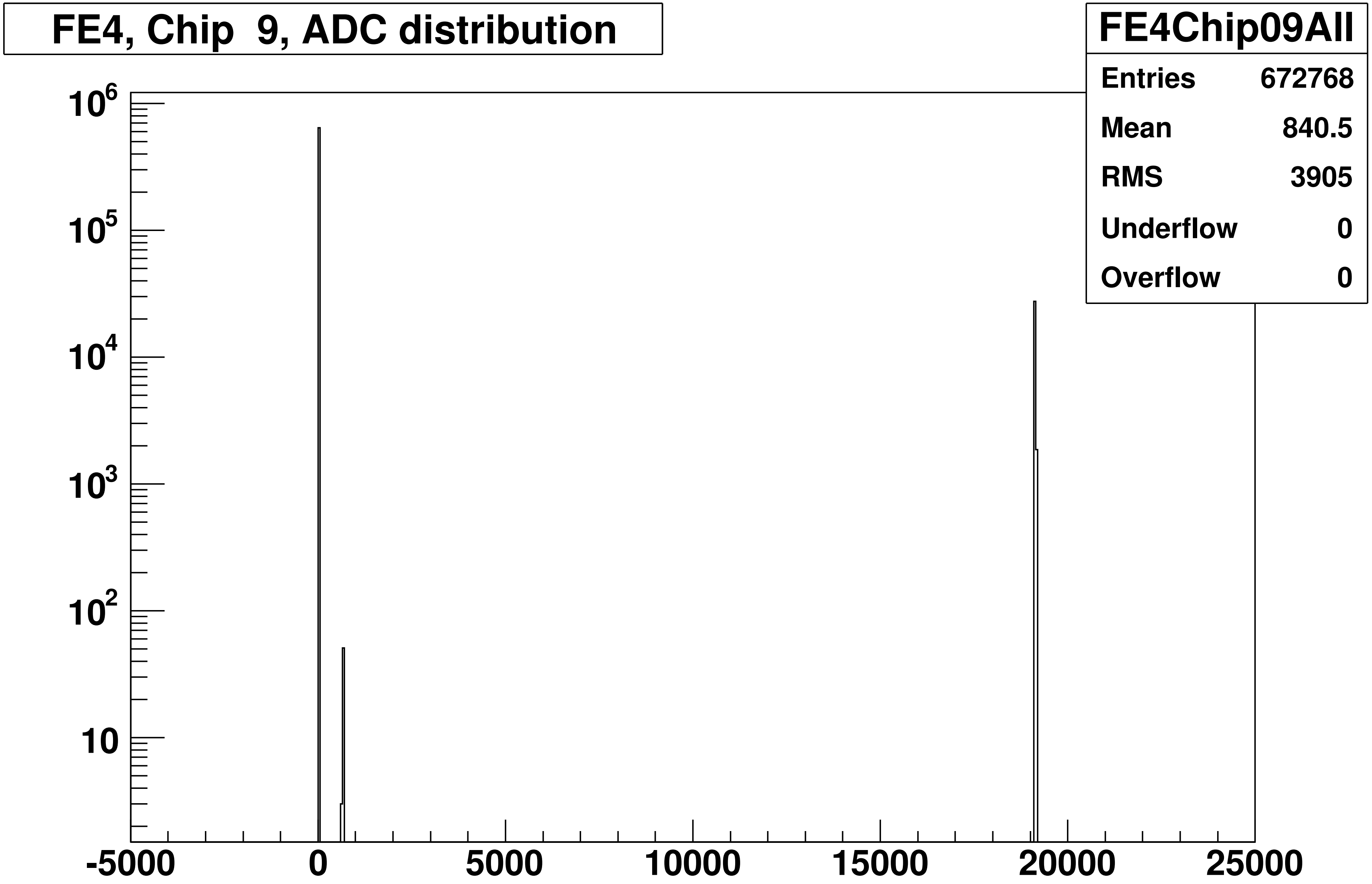
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE4, Chip 9, ADC distribution
FE4Chip09All
Entries 672768
Mean 840.5
RMS 3905
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
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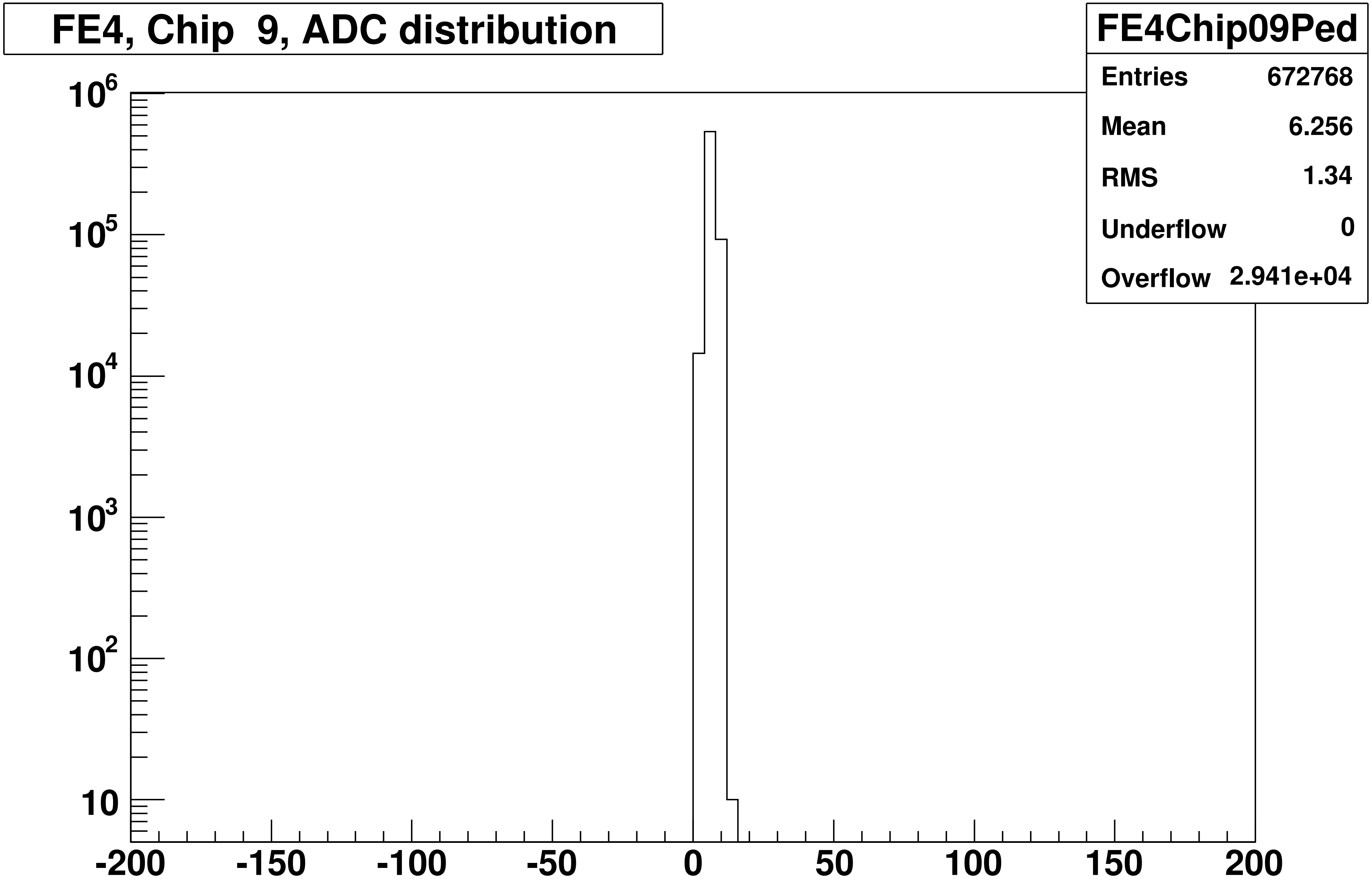

FE4, Chip 9, ADC distribution
FE4Chip09Ped
Entries 672768
Mean 6.256
RMS 1.34
Underflow 0
Overflow 2.941e+04
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10^4
10^3
10^2
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100
150
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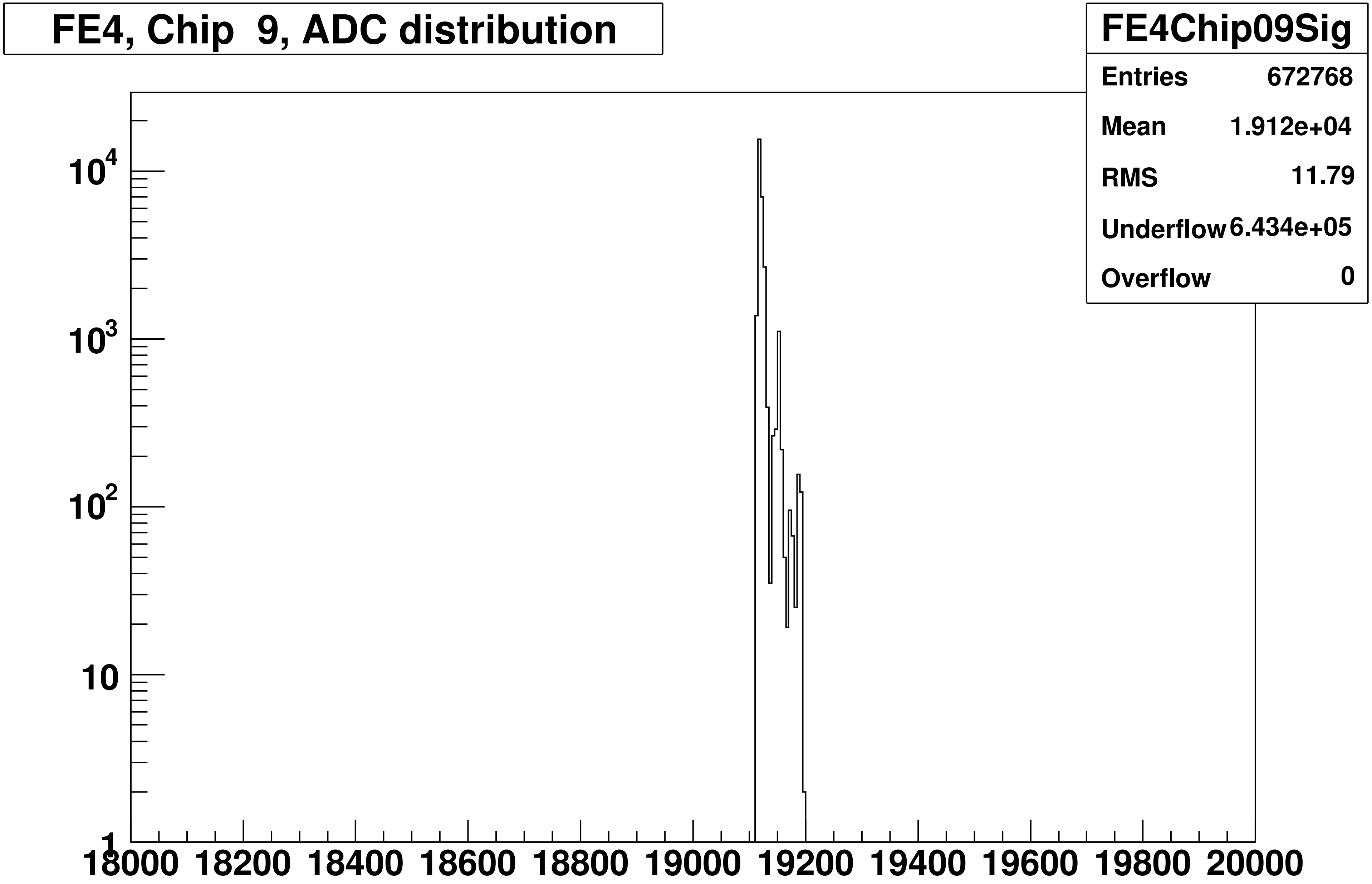
FE4, Chip 9, ADC distribution
FE4Chip09Sig
Entries 672768
Mean 1.912e+04
RMS 11.79
Underflow 6.434e+05
Overflow 0
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10^3
10^2
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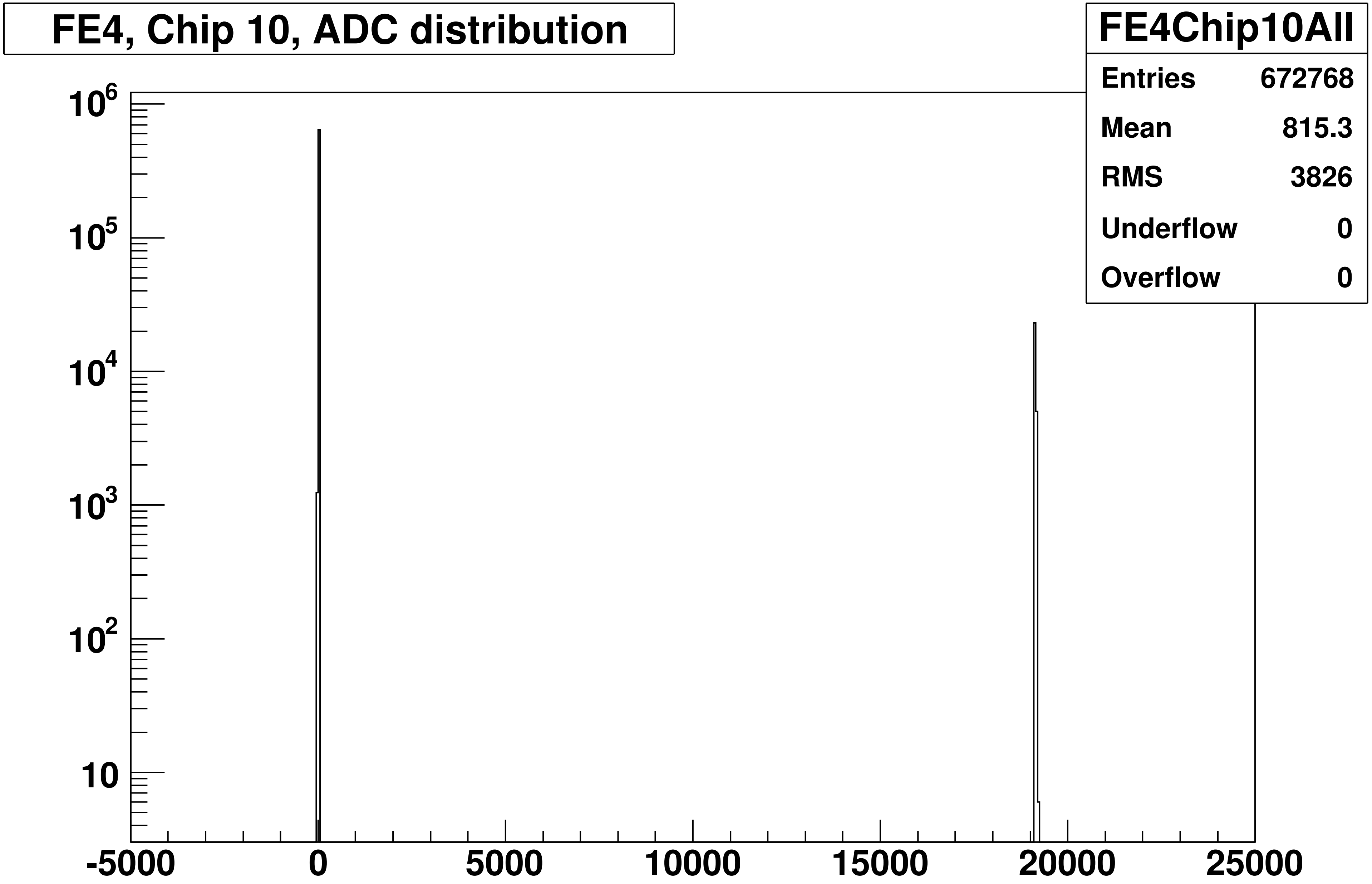
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE4, Chip 10, ADC distribution
FE4Chip10All
Entries 672768
Mean 815.3
RMS 3826
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
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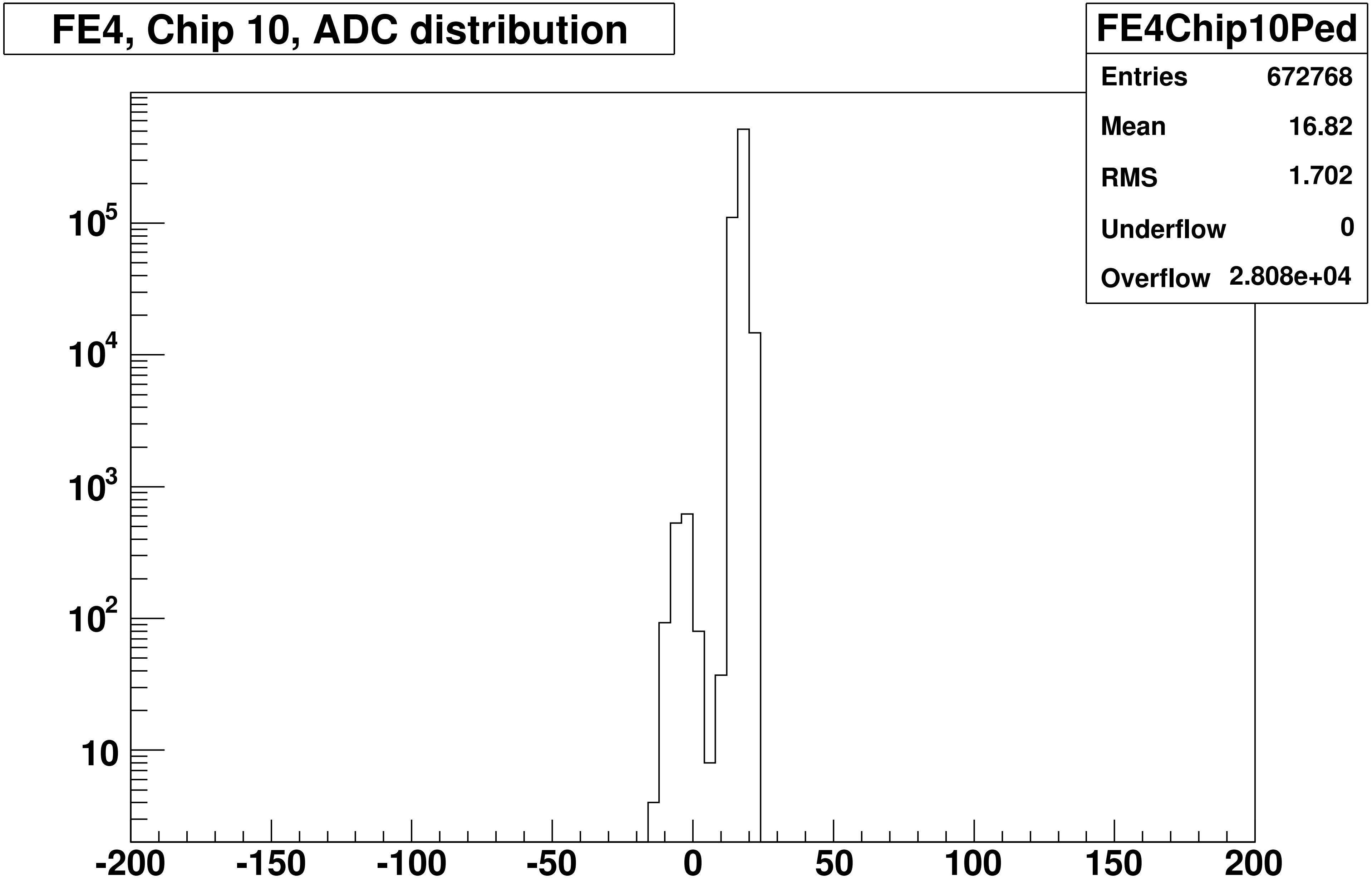
FE4, Chip 10, ADC distribution
FE4Chip10Ped
Entries 672768
Mean 16.82
RMS 1.702
Underflow 0
Overflow 2.808e+04
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10^4
10^3
10^2
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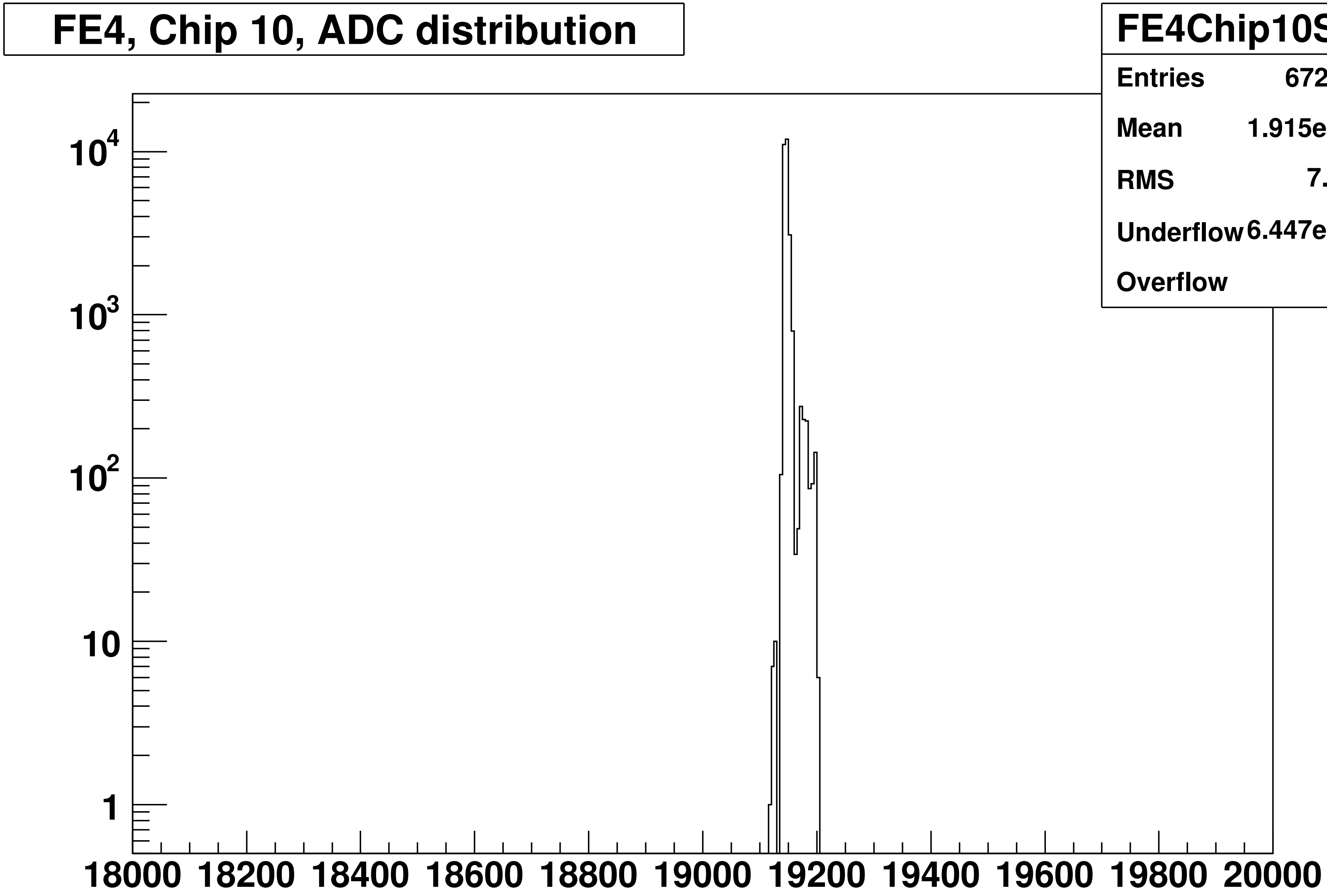

FE4, Chip 10, ADC distribution
FE4Chip10Sig
Entries 672768
Mean 1.915e+04
RMS 7.898
Underflow 6.447e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
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19000
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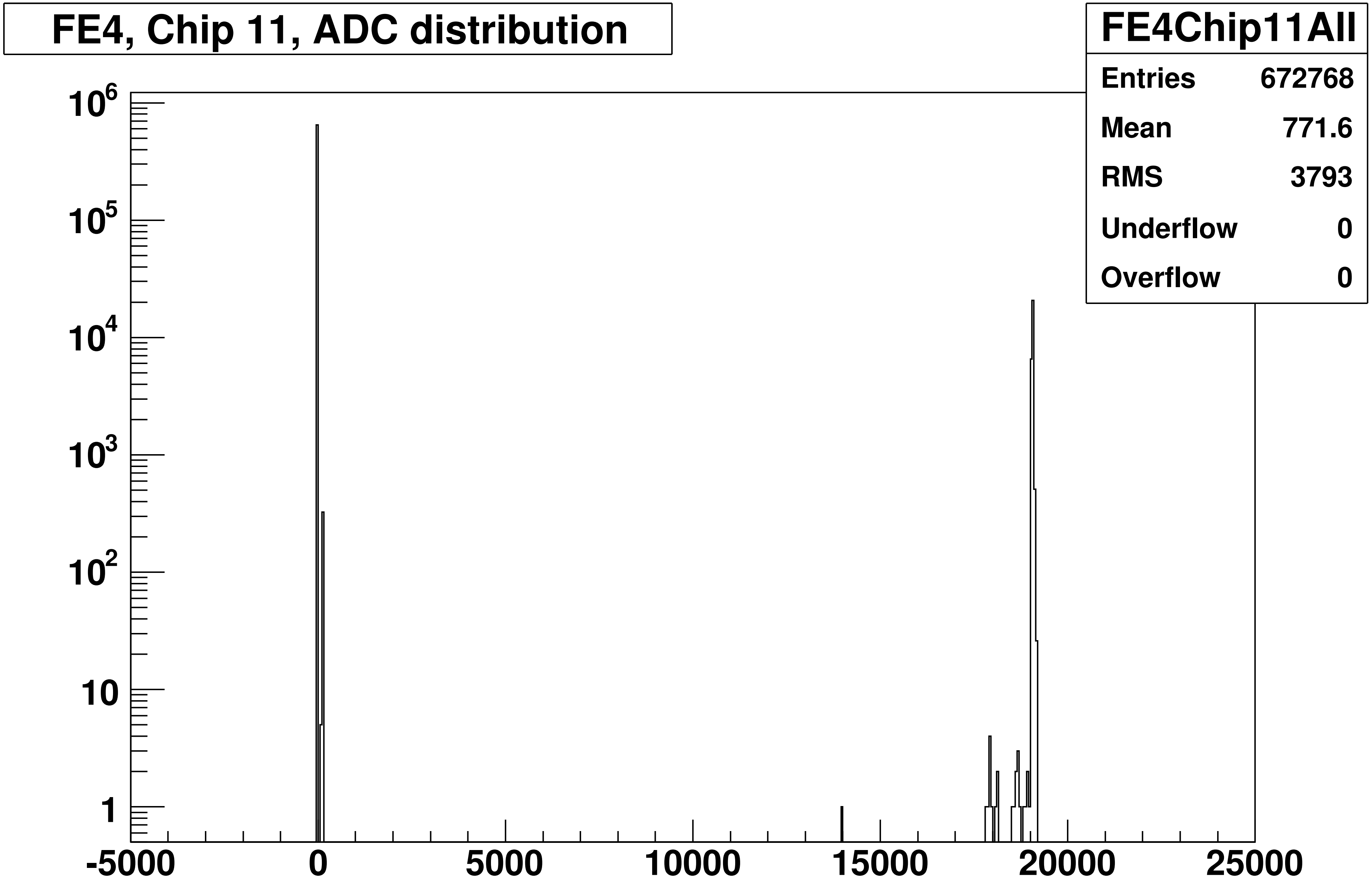

FE4, Chip 11, ADC distribution
FE4Chip11All
Entries 672768
Mean 771.6
RMS 3793
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
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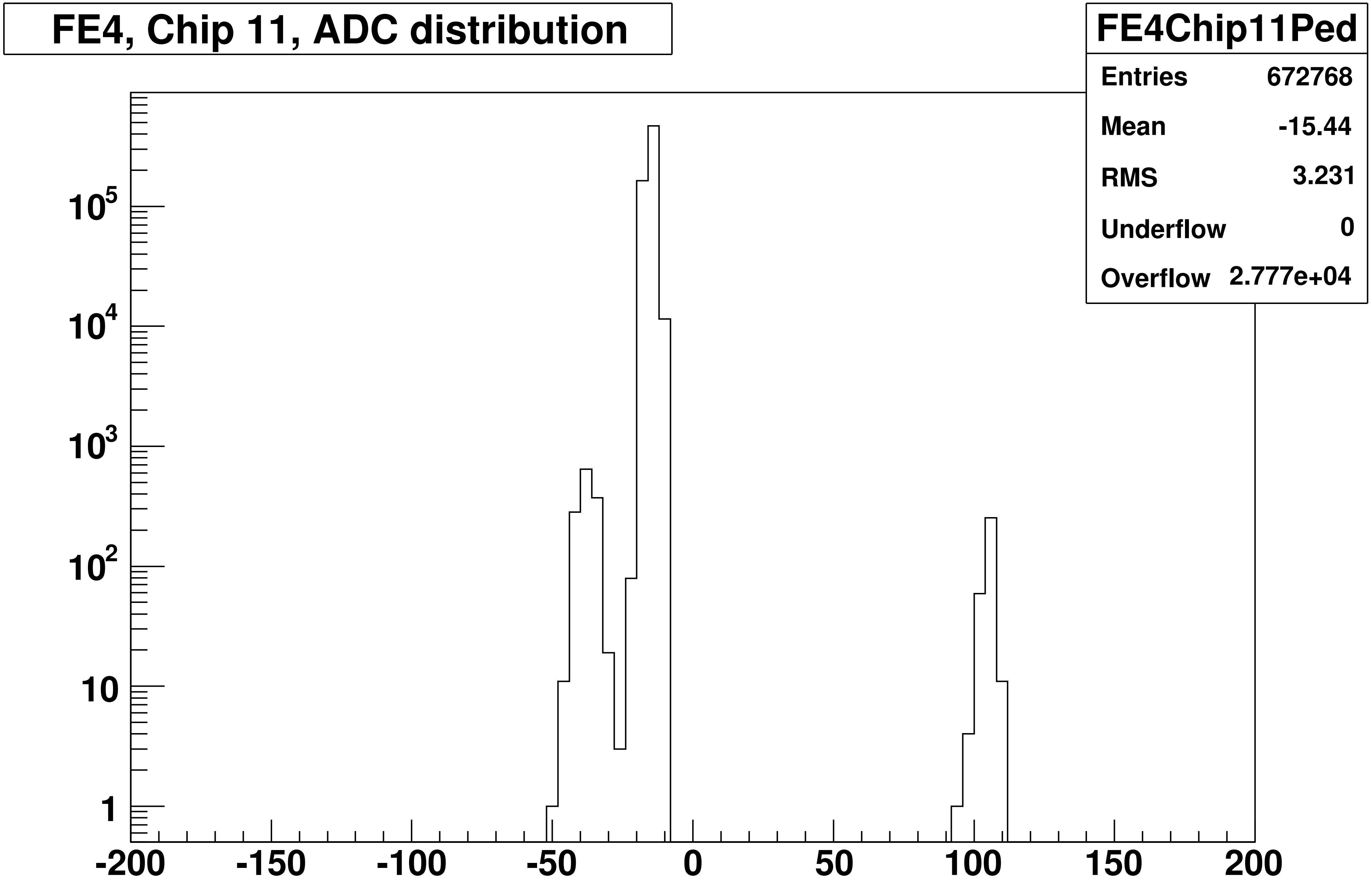
20000
25000


FE4, Chip 11, ADC distribution
FE4Chip11Ped
Entries 672768
Mean -15.44
RMS 3.231
Underflow 0
Overflow 2.777e+04
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10^3
10^2
10
1
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50
100
150
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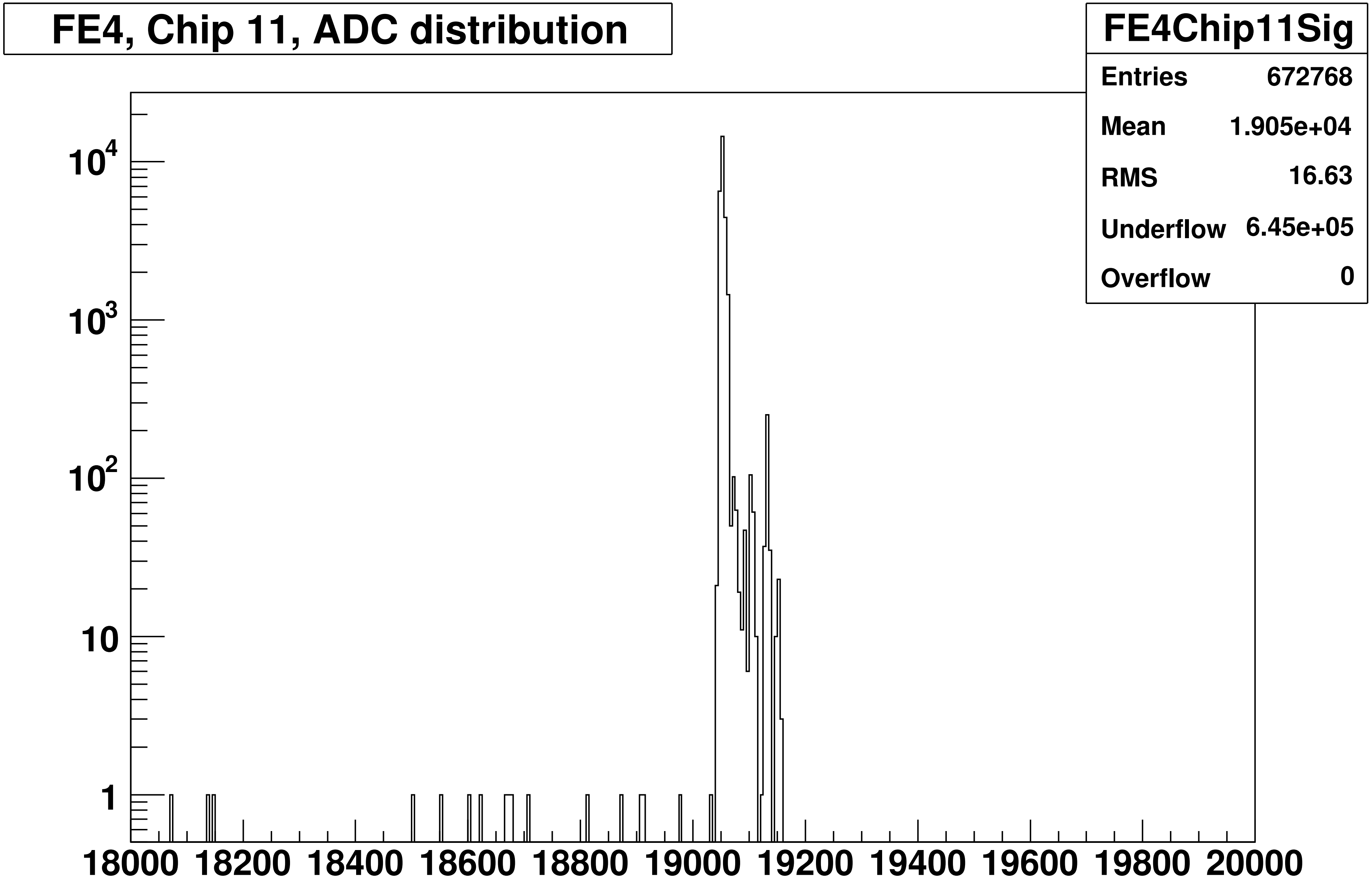

FE4, Chip 11, ADC distribution
FE4Chip11Sig
Entries 672768
Mean 1.905e+04
RMS 16.63
Underflow 6.45e+05
Overflow 0
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10^3
10^2
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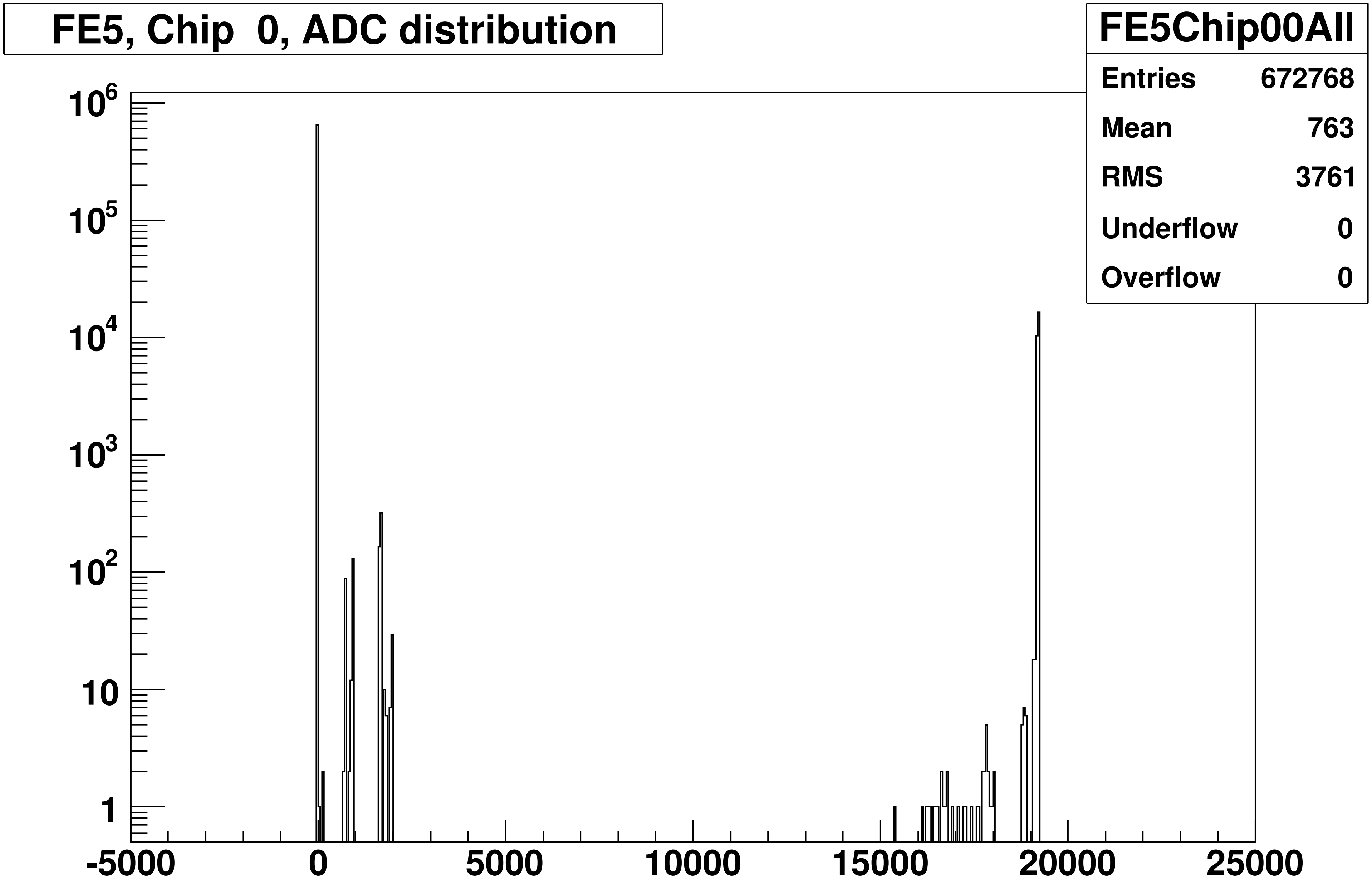
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE5, Chip 0, ADC distribution
FE5Chip00All
Entries 672768
Mean 763
RMS 3761
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
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0
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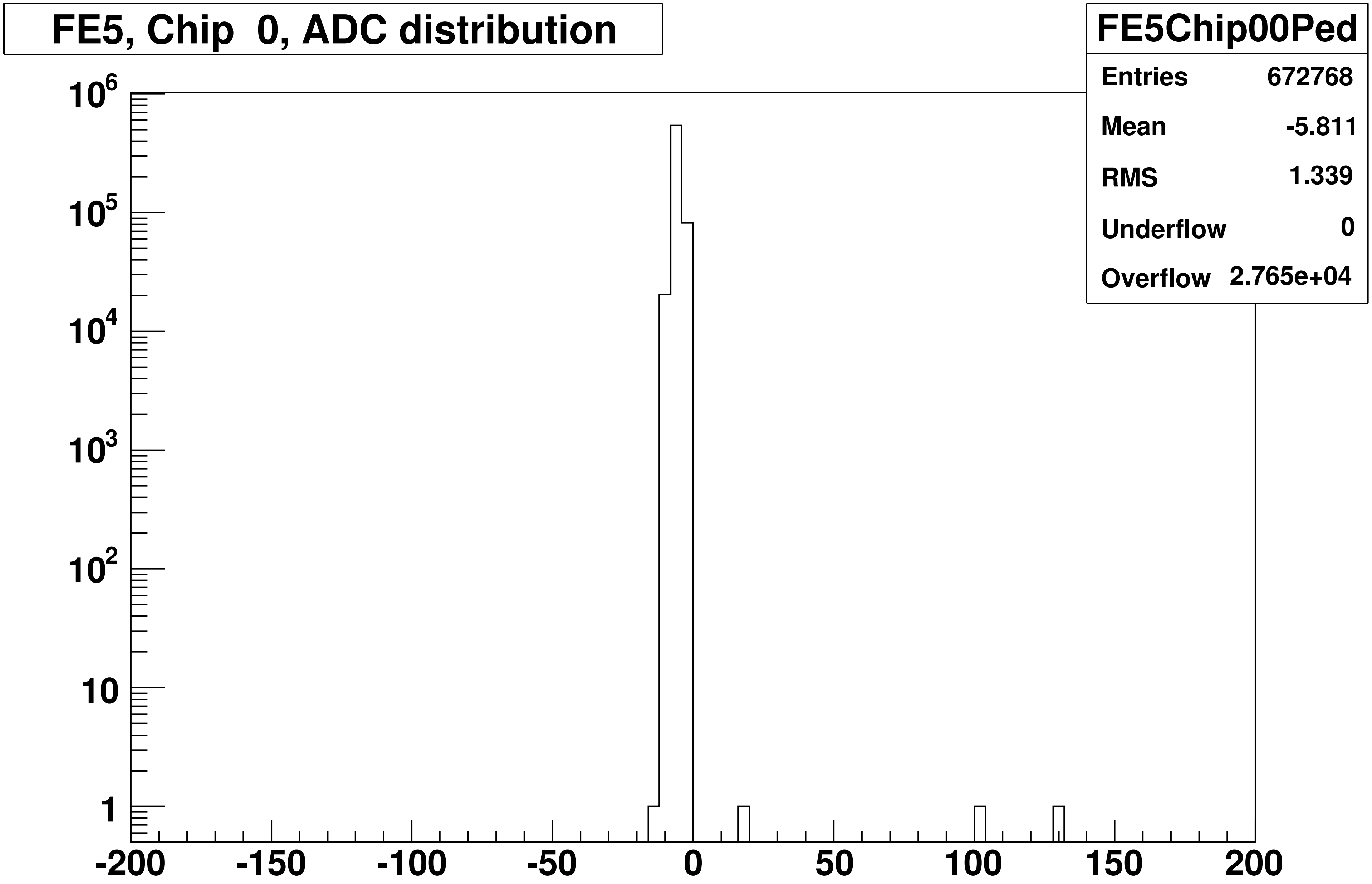
10000
15000
20000
25000


FE5, Chip 0, ADC distribution
FE5Chip00Ped
Entries 672768
Mean -5.811
RMS 1.339
Underflow 0
Overflow 2.765e+04
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10^4
10^3
10^2
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1
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100
150
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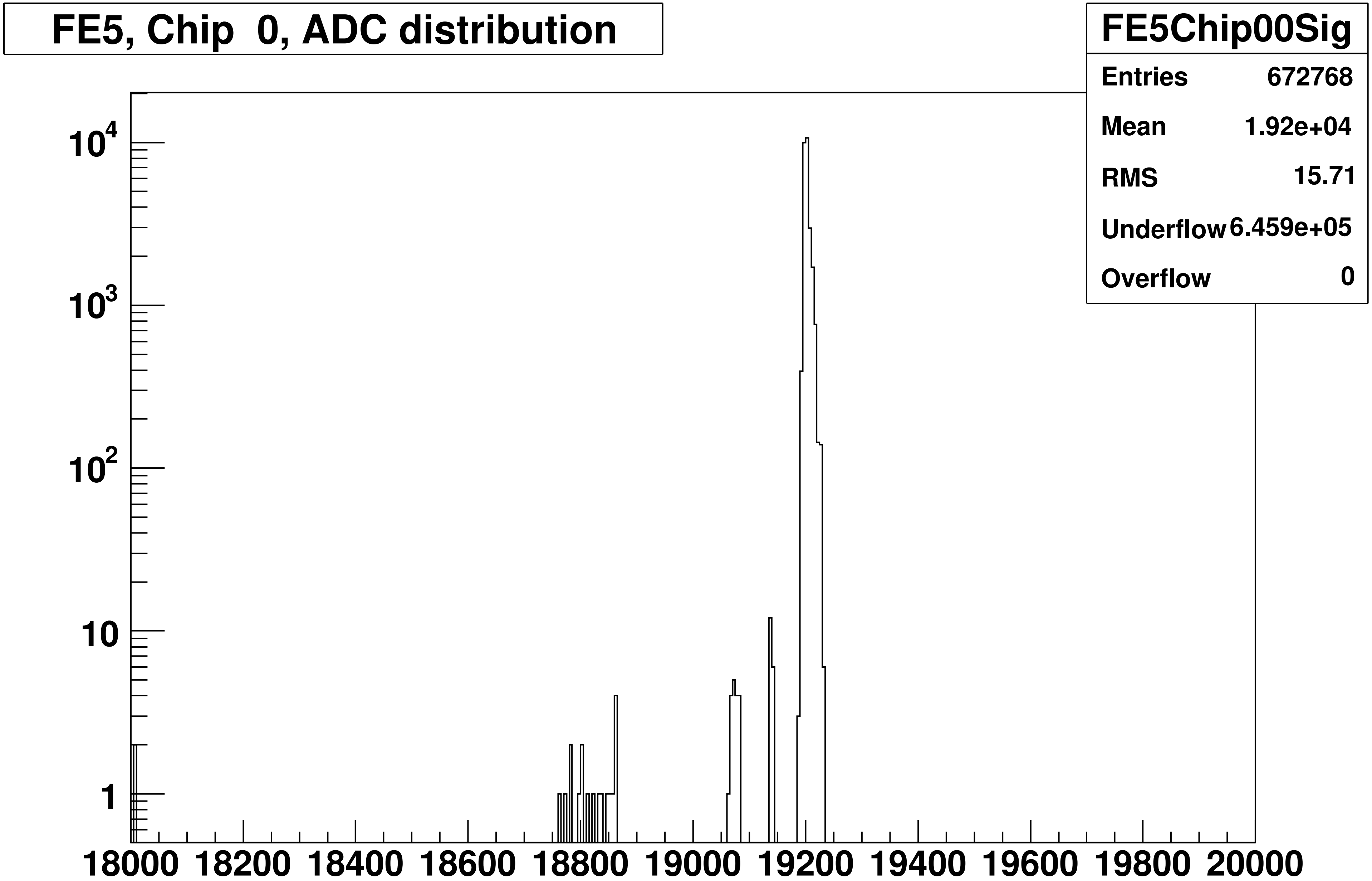
FE5, Chip 0, ADC distribution
FE5Chip00Sig
Entries 672768
Mean 1.92e+04
RMS 15.71
Underflow 6.459e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
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19000
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19800
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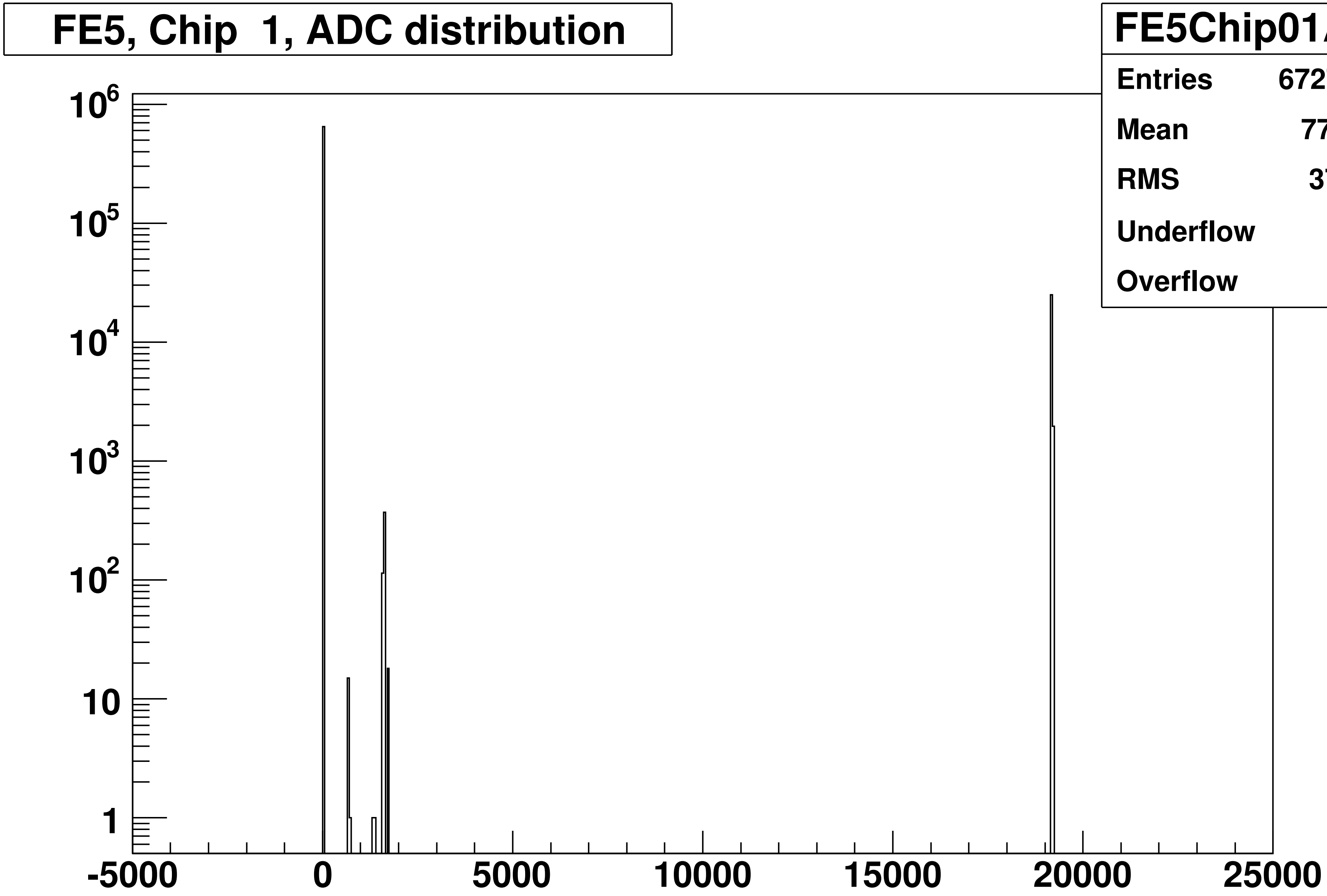
FE5, Chip 1, ADC distribution
FE5Chip01All
Entries 672768
Mean 778.5
RMS 3755
Underflow 0
Overflow 0
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10^4
10^3
10^2
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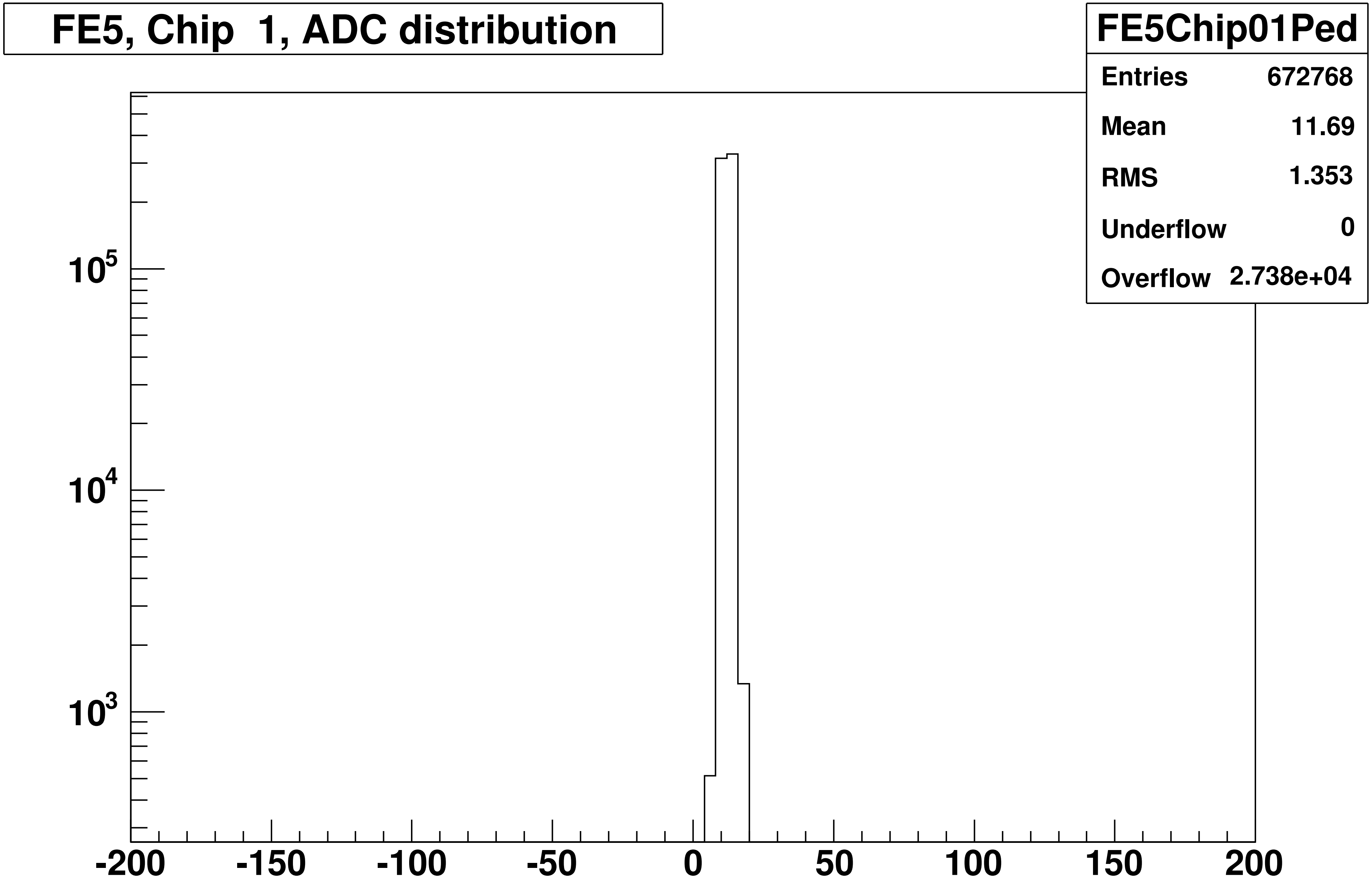
FE5, Chip 1, ADC distribution
FE5Chip01Ped
Entries 672768
Mean 11.69
RMS 1.353
Underflow 0
Overflow 2.738e+04
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10^3
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150
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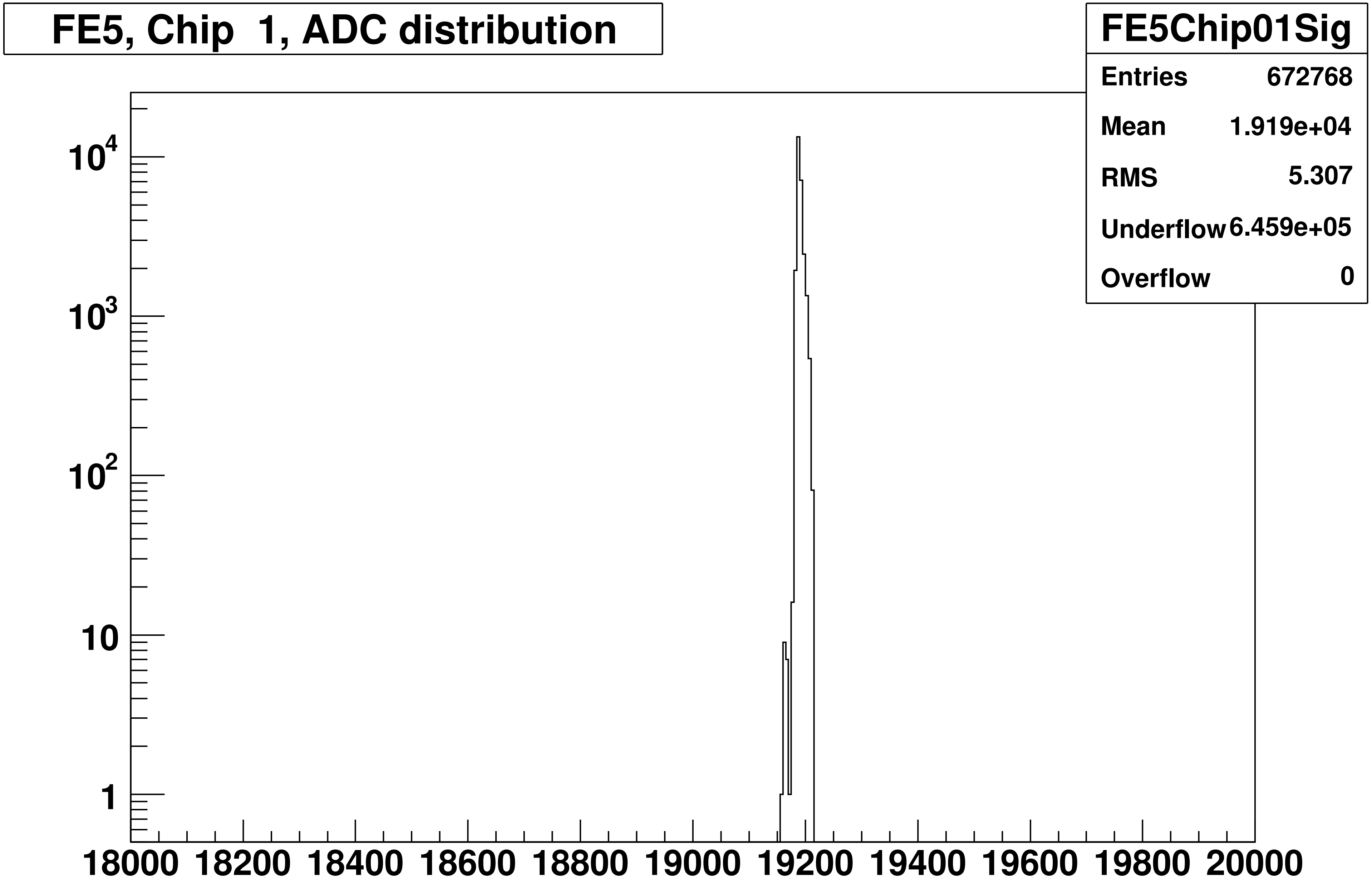
FE5, Chip 1, ADC distribution
FE5Chip01Sig
Entries 672768
Mean 1.919e+04
RMS 5.307
Underflow 6.459e+05
Overflow 0
10^4
10^3
10^2
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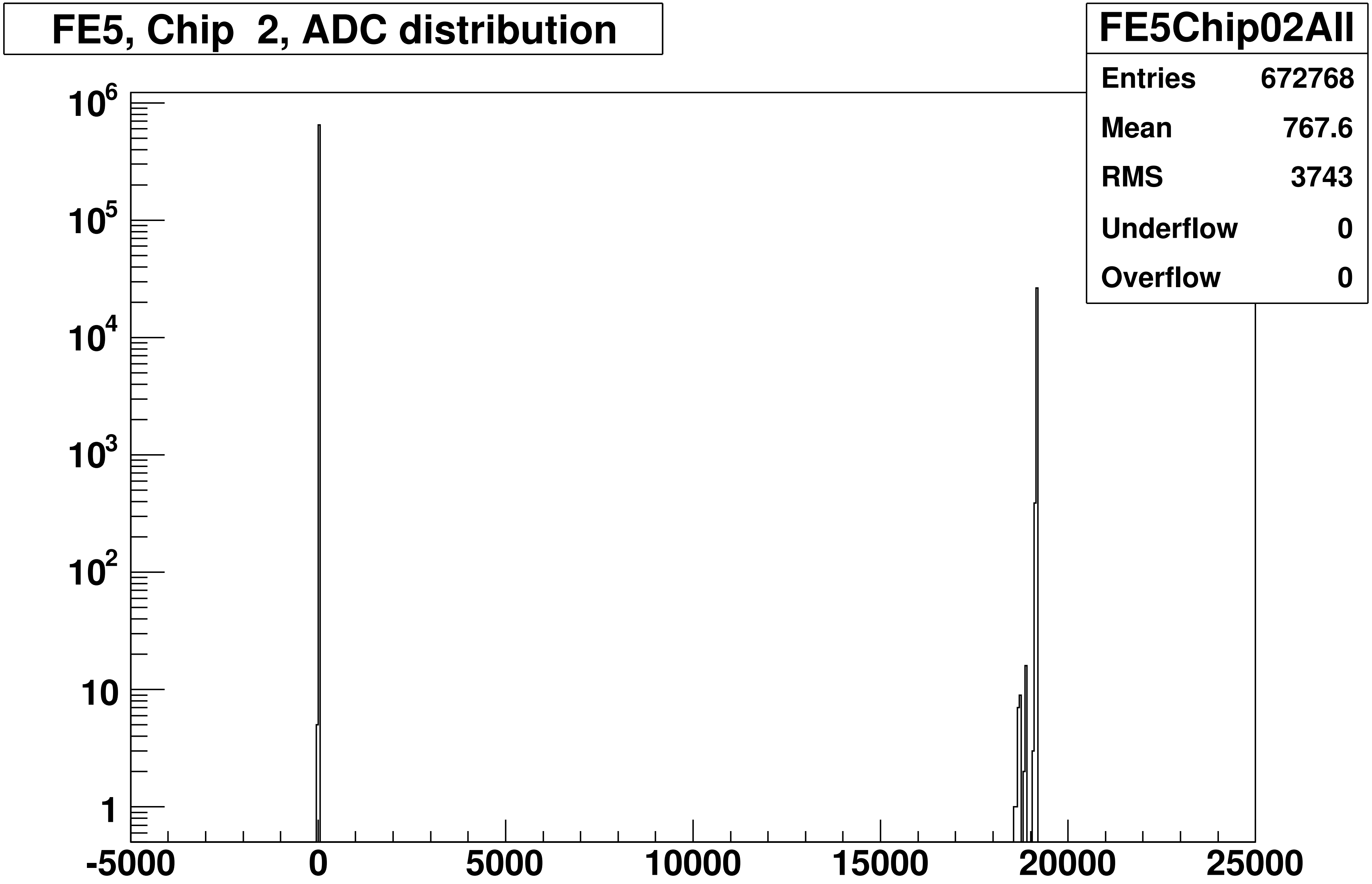
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE5, Chip 2, ADC distribution
FE5Chip02All
Entries 672768
Mean 767.6
RMS 3743
Underflow 0
Overflow 0
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10^4
10^3
10^2
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0
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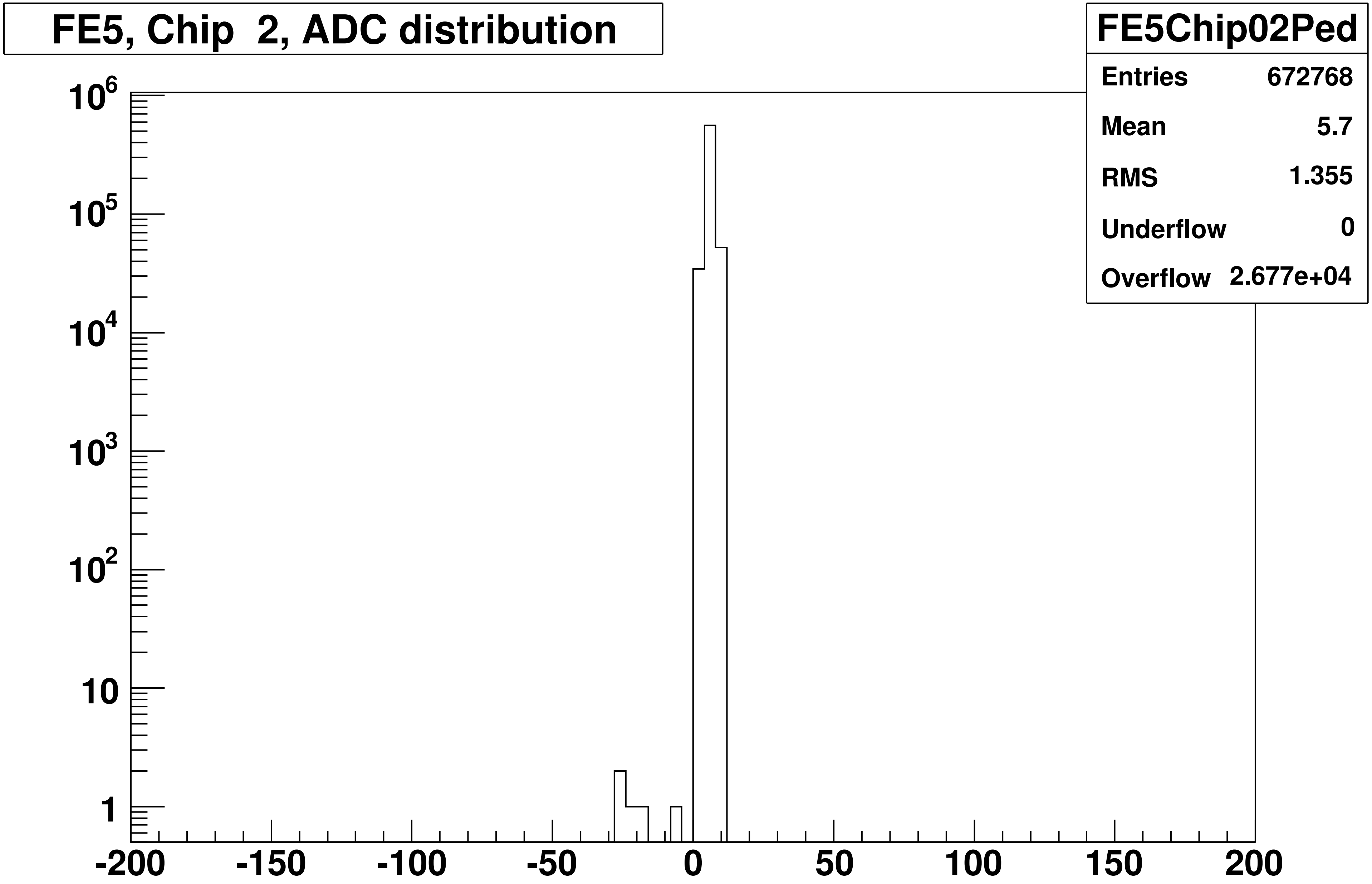
20000
25000


FE5, Chip 2, ADC distribution
FE5Chip02Ped
Entries 672768
Mean 5.7
RMS 1.355
Underflow 0
Overflow 2.677e+04
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10^5
10^4
10^3
10^2
10
1
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-100
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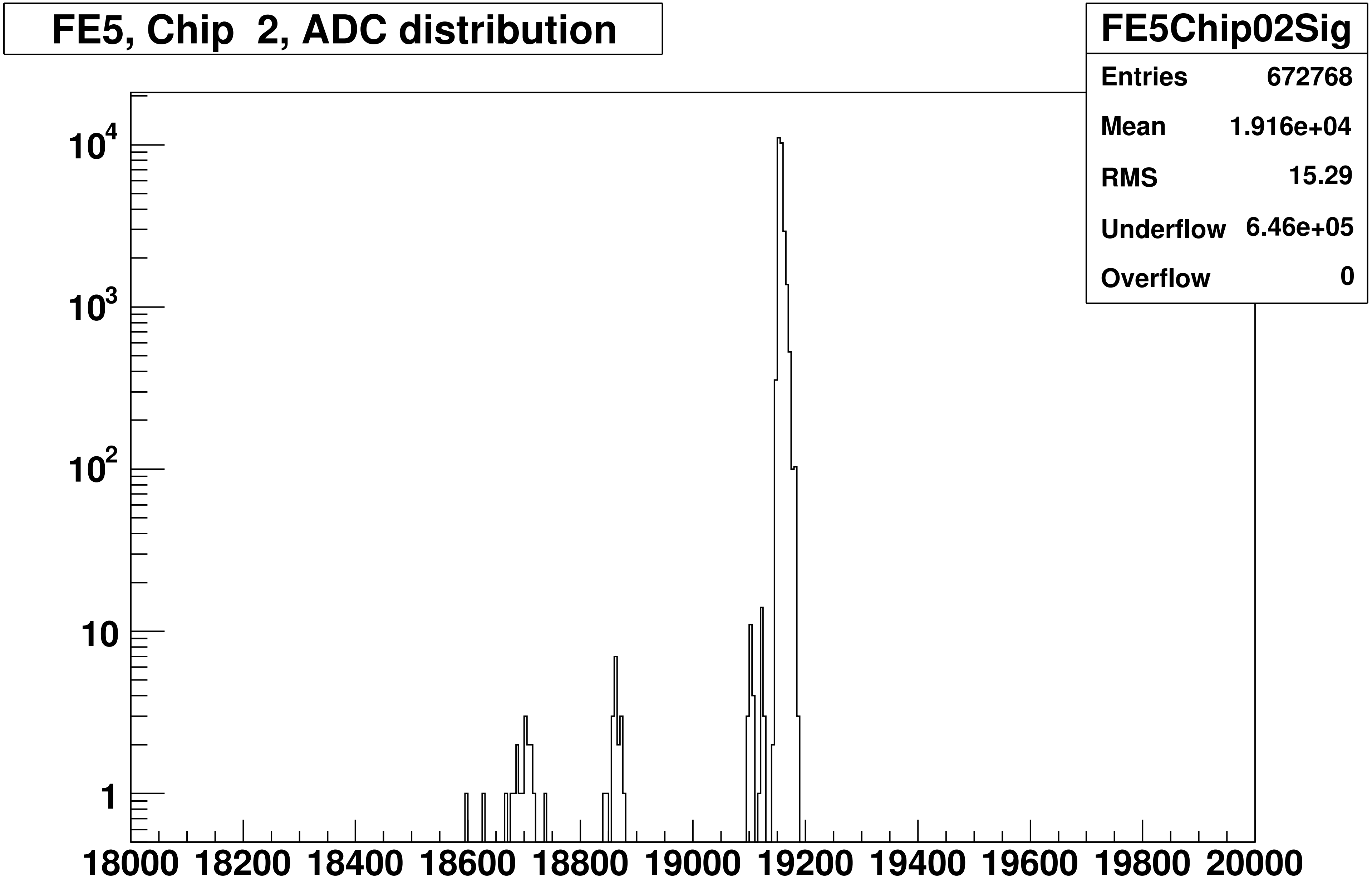
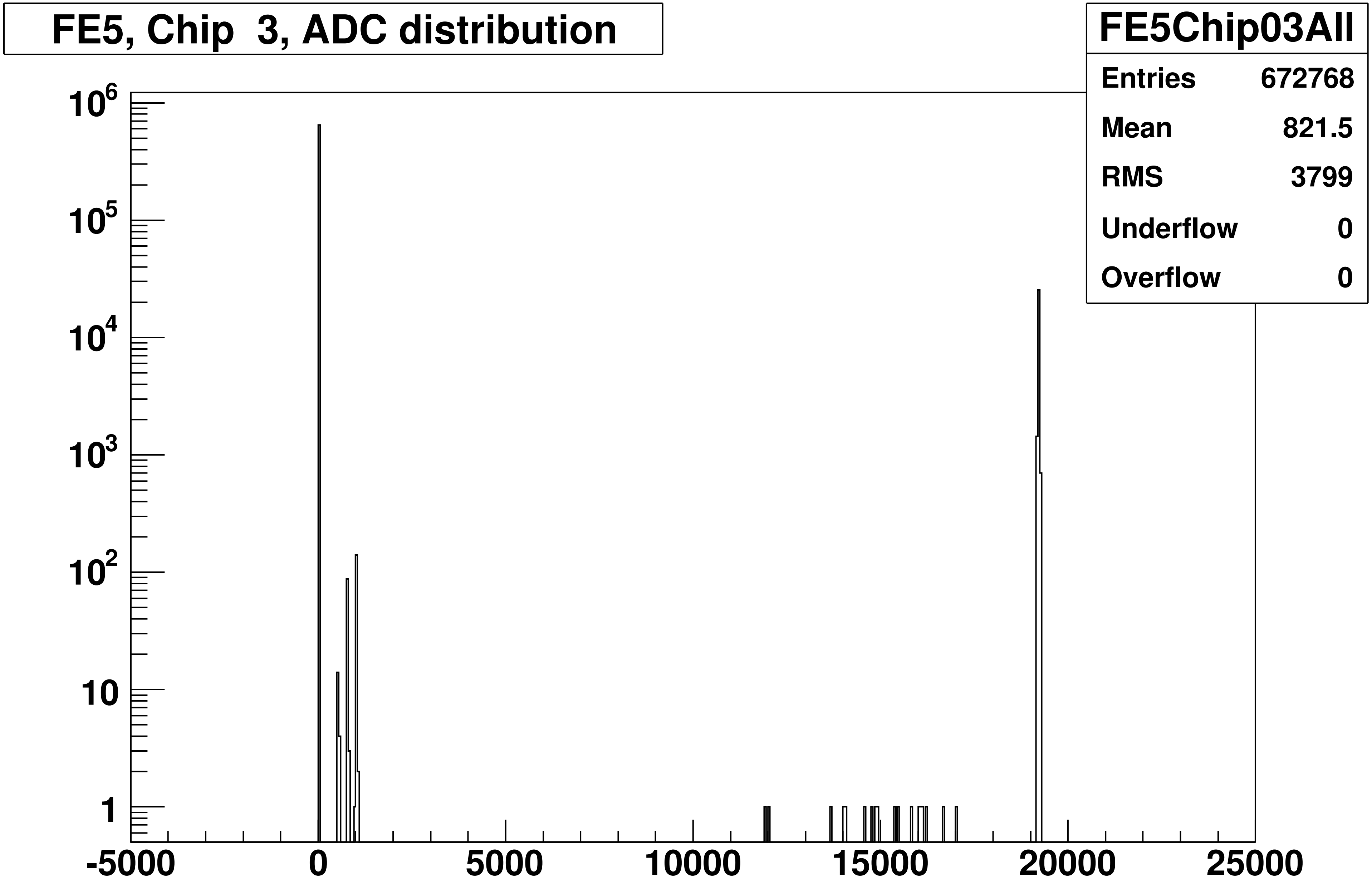
0
50
100
150
200



FE5, Chip 2, ADC distribution
FE5Chip02Sig
Entries 672768
Mean 1.916e+04
RMS 15.29
Underflow 6.46e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE5, Chip 3, ADC distribution
FE5Chip03All
Entries 672768
Mean 821.5
RMS 3799
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
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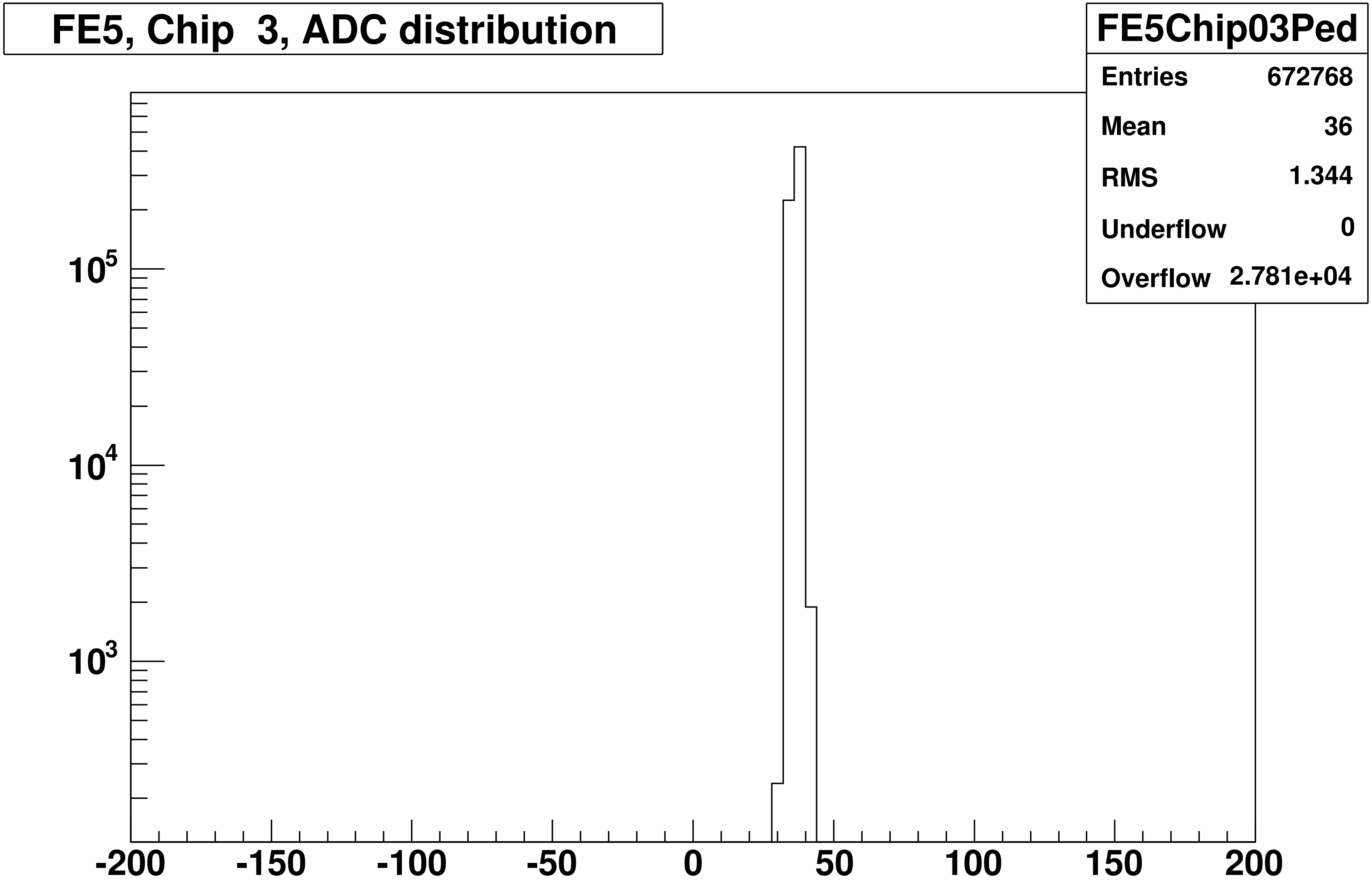

FE5, Chip 3, ADC distribution
FE5Chip03Ped
Entries 672768
Mean 36
RMS 1.344
Underflow 0
Overflow 2.781e+04
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10^4
10^3
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-100
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0
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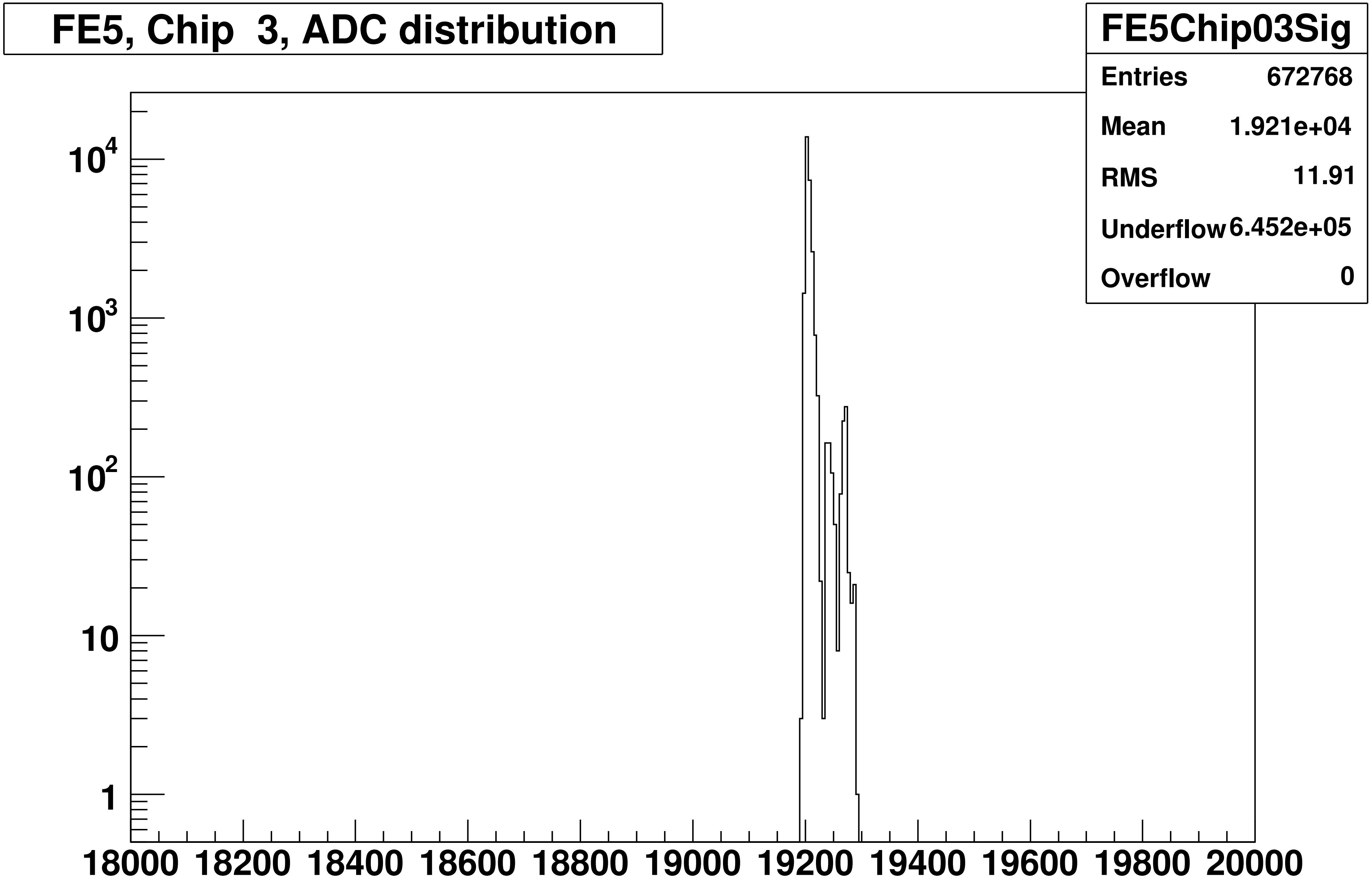
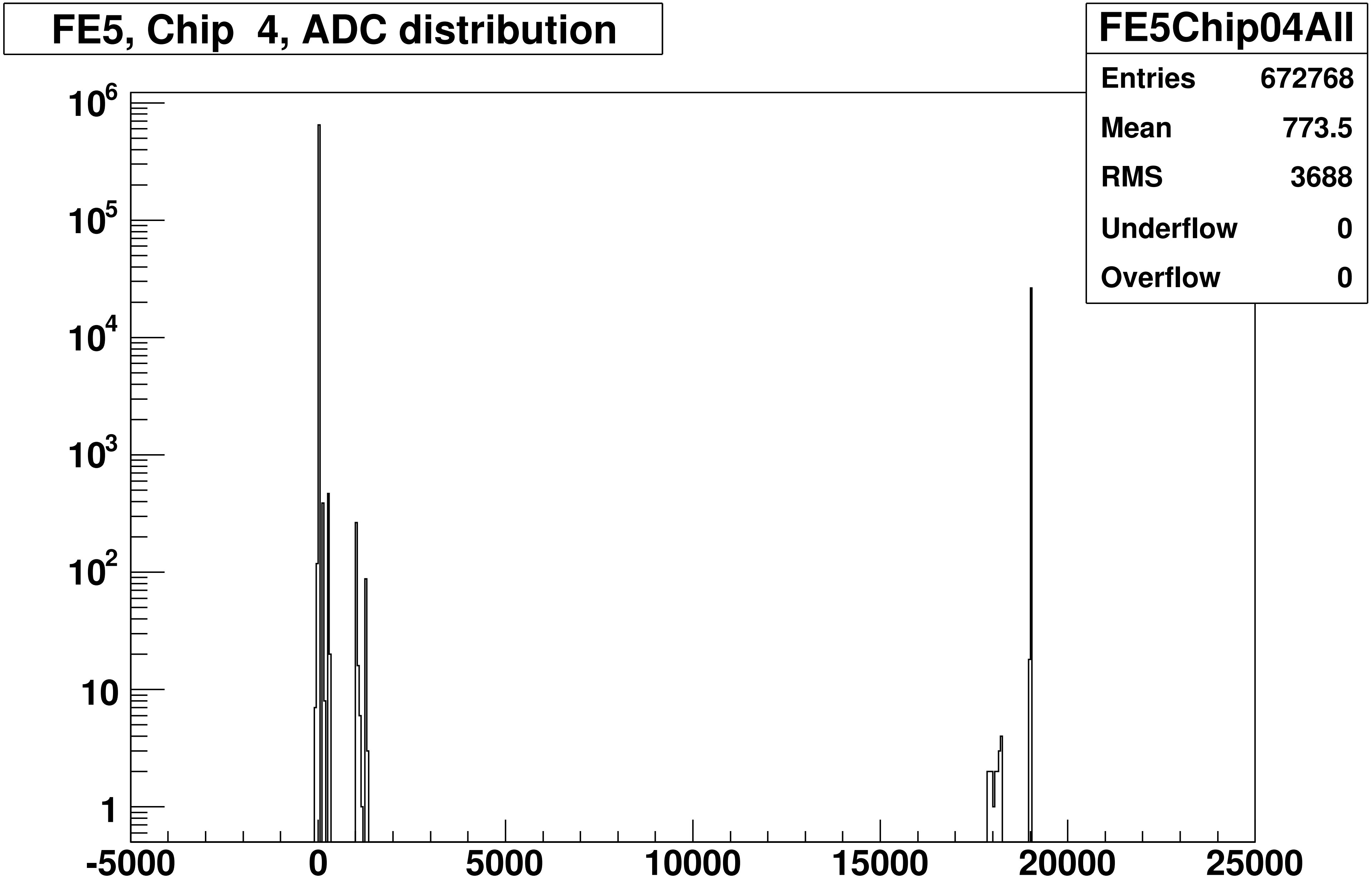
150
200


FE5, Chip 3, ADC distribution
FE5Chip03Sig
Entries 672768
Mean 1.921e+04
RMS 11.91
Underflow 6.452e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE5, Chip 4, ADC distribution
FE5Chip04All
Entries 672768
Mean 773.5
RMS 3688
Underflow 0
Overflow 0
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10^4
10^3
10^2
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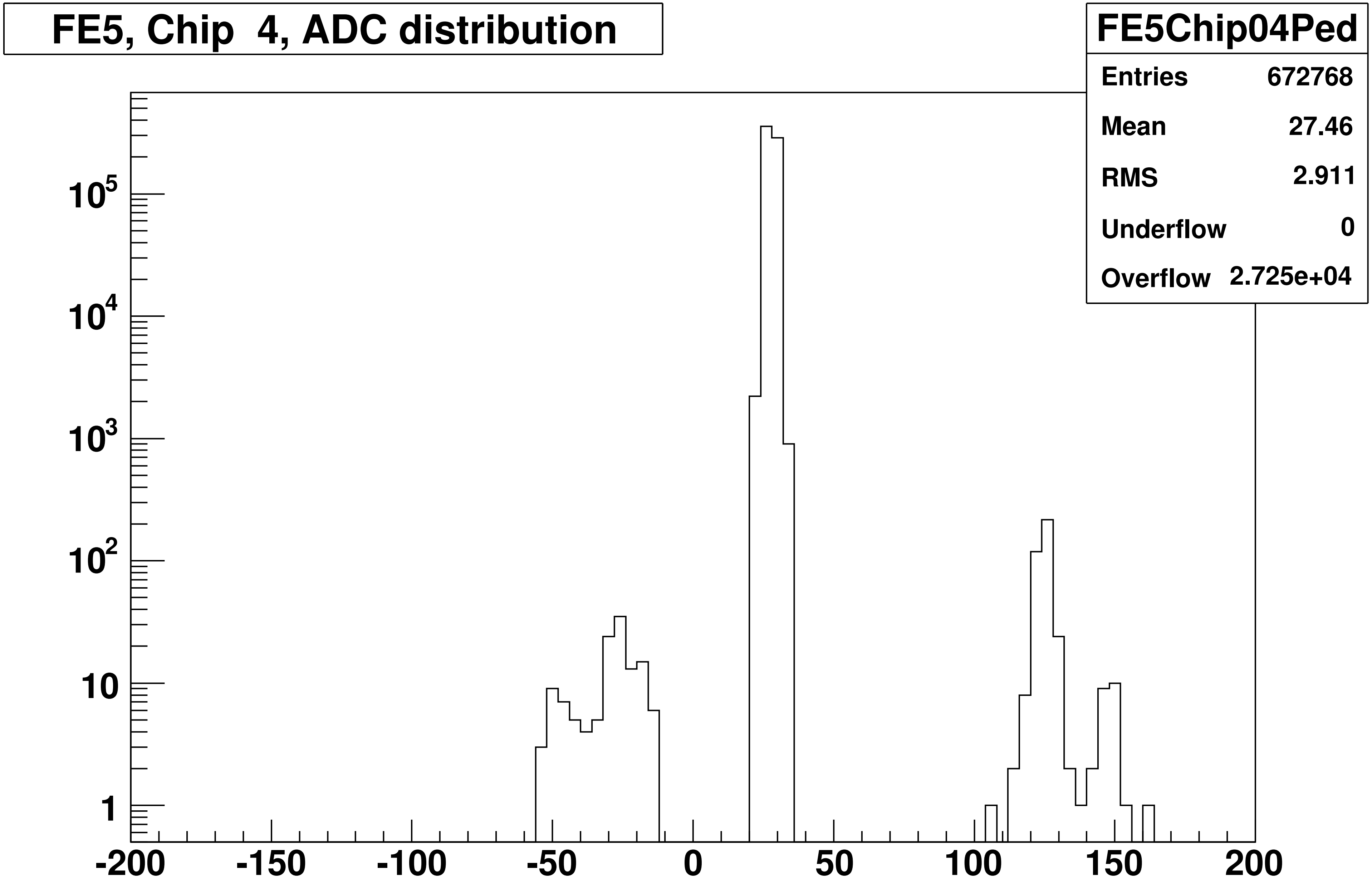

FE5, Chip 4, ADC distribution
FE5Chip04Ped
Entries 672768
Mean 27.46
RMS 2.911
Underflow 0
Overflow 2.725e+04
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10^4
10^3
10^2
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1
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-100
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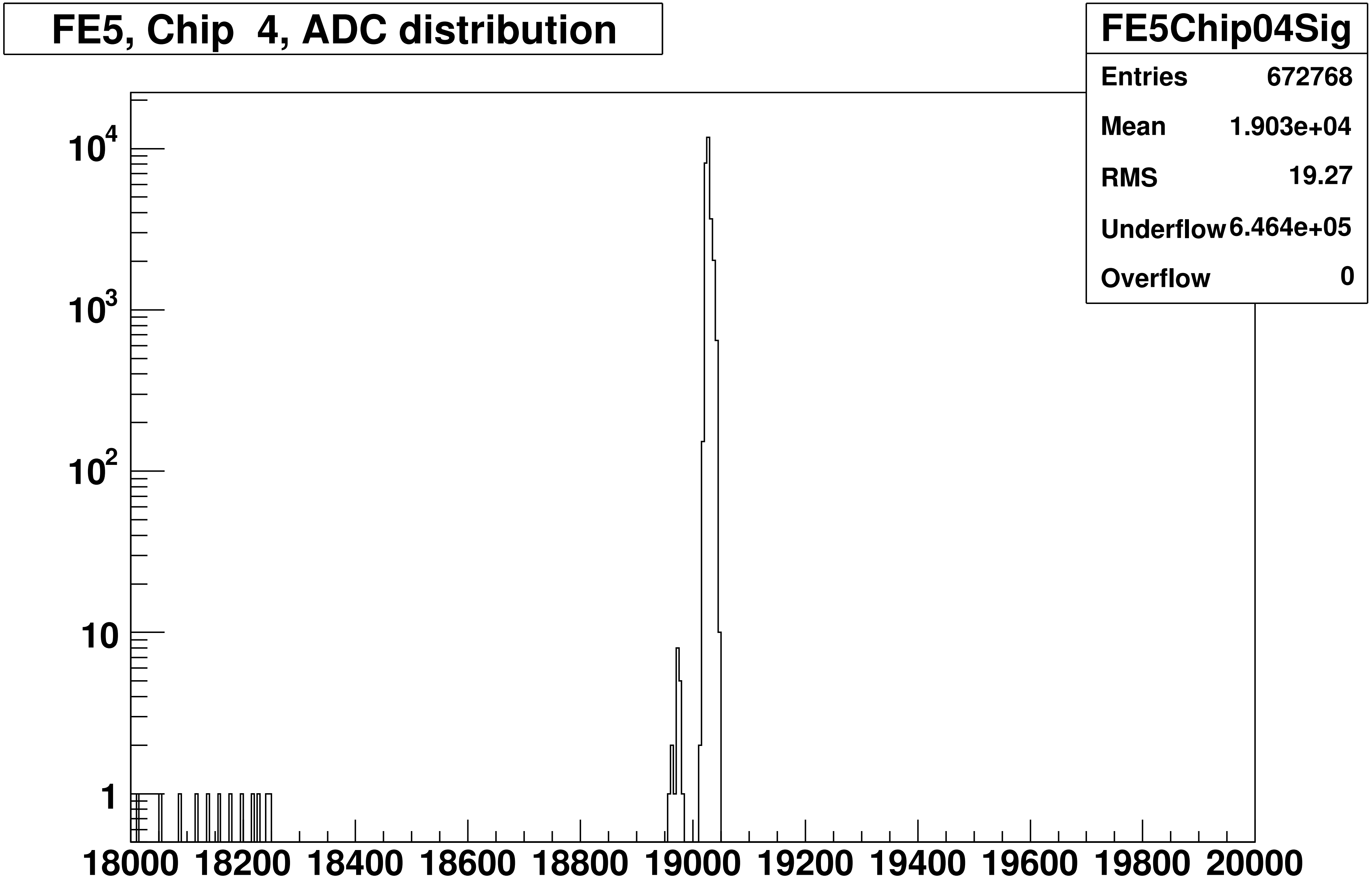
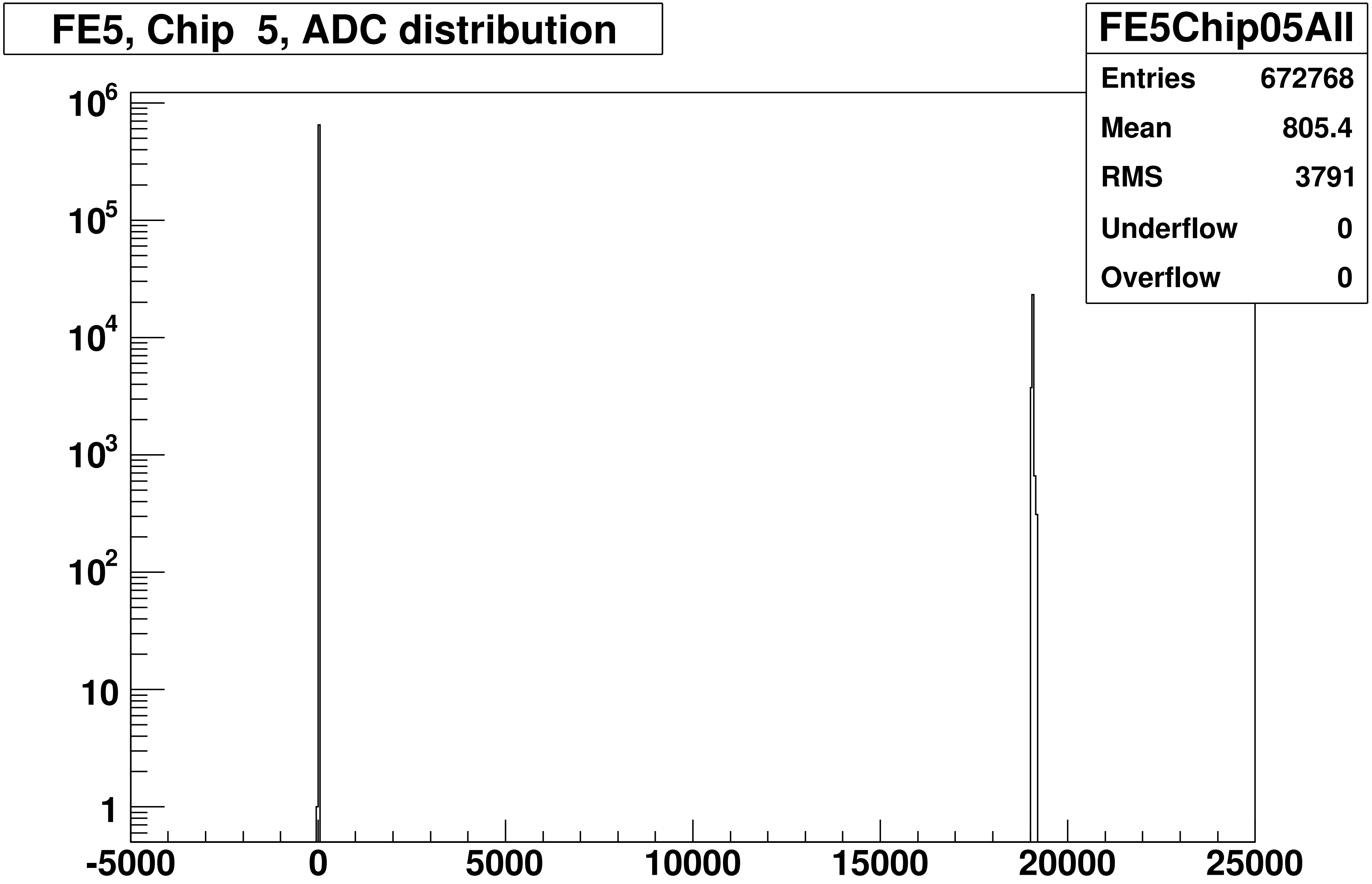
100
150
200


FE5, Chip 4, ADC distribution
FE5Chip04Sig
Entries 672768
Mean 1.903e+04
RMS 19.27
Underflow 6.464e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE5, Chip 5, ADC distribution
FE5Chip05All
Entries 672768
Mean 805.4
RMS 3791
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
1
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5000
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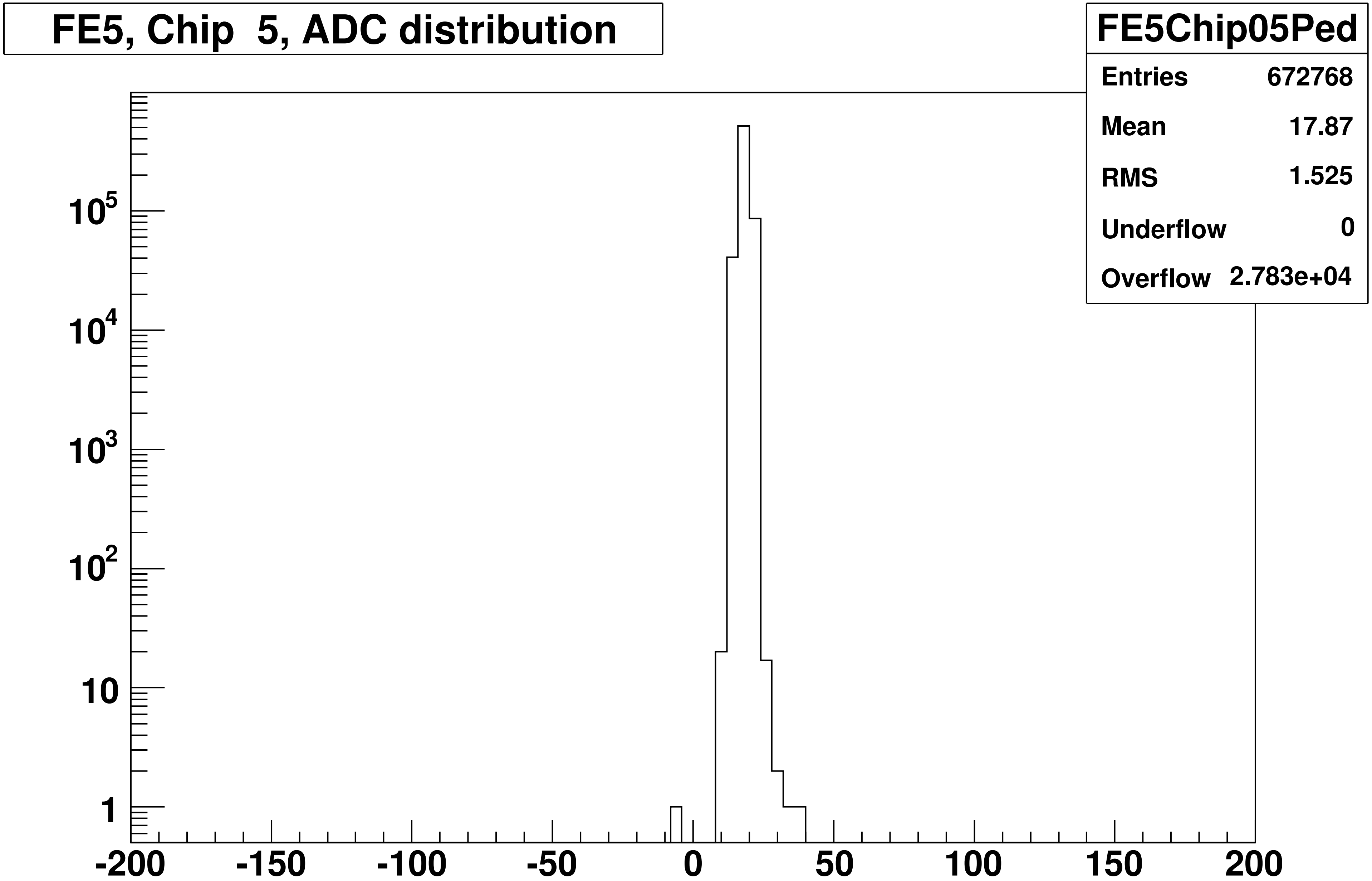
20000
25000


FE5, Chip 5, ADC distribution
FE5Chip05Ped
Entries 672768
Mean 17.87
RMS 1.525
Underflow 0
Overflow 2.783e+04
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10^4
10^3
10^2
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50
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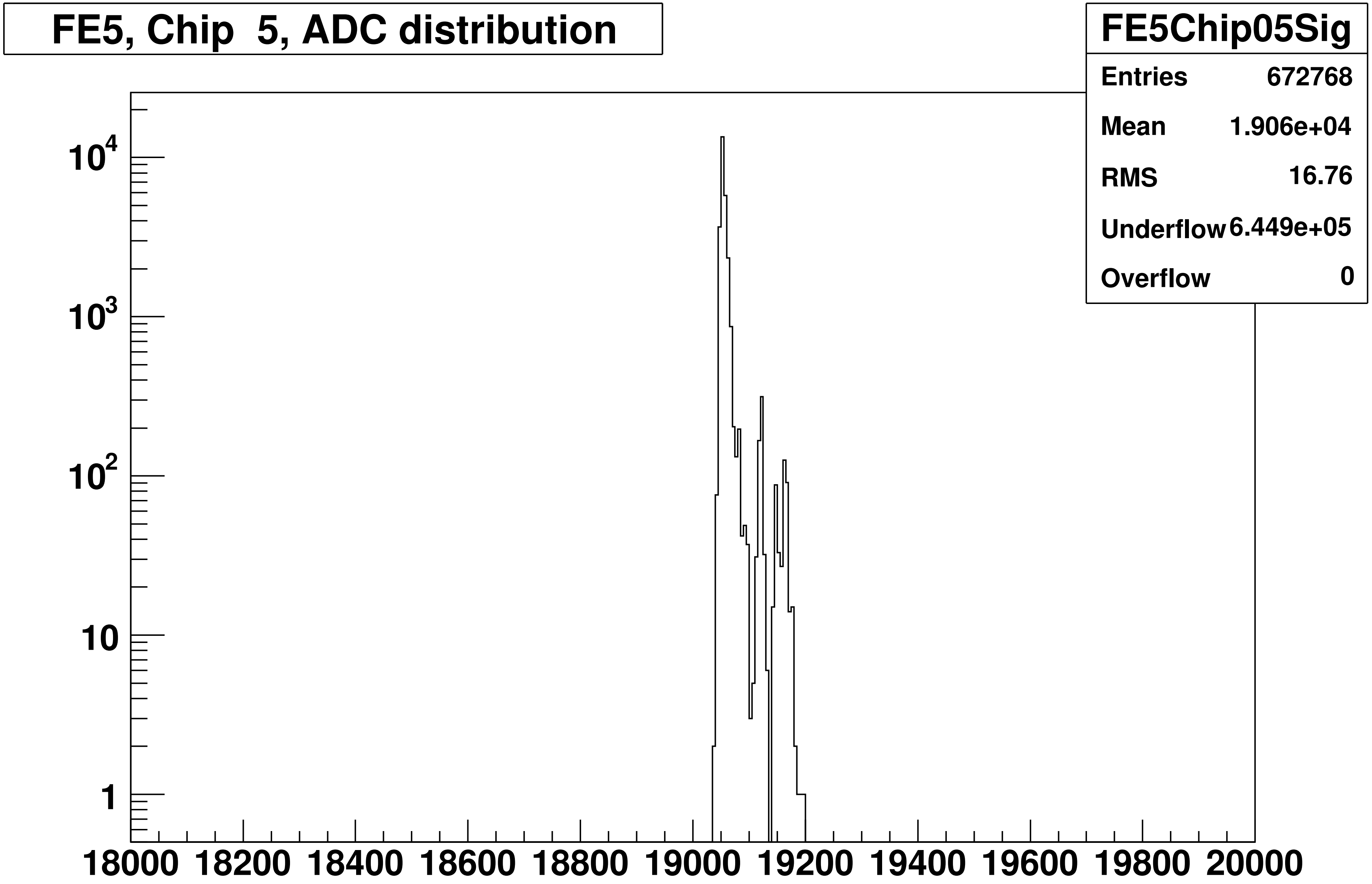
150
200



FE5, Chip 5, ADC distribution
FE5Chip05Sig
Entries 672768
Mean 1.906e+04
RMS 16.76
Underflow 6.449e+05
Overflow 0
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10^3
10^2
10
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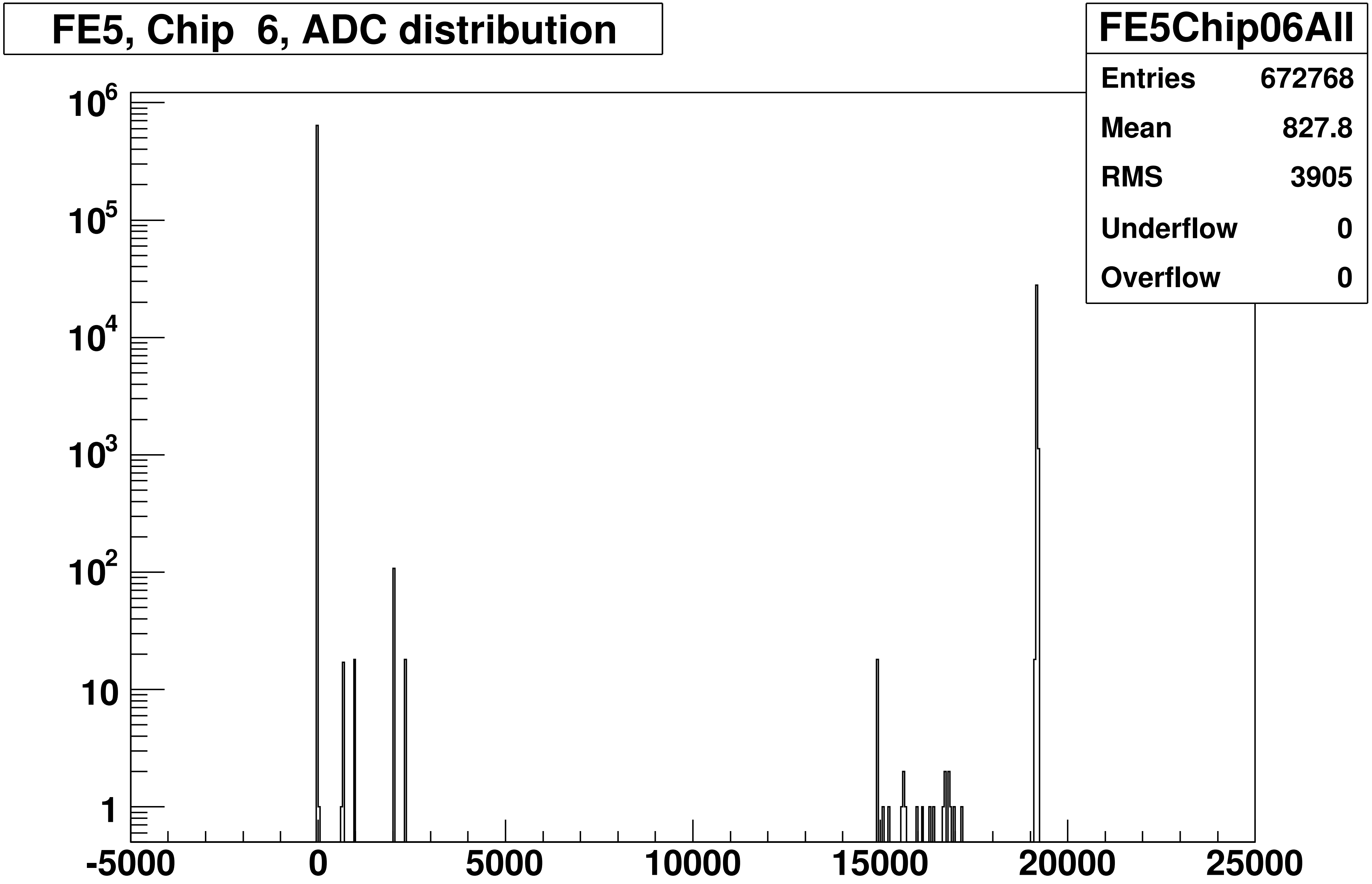
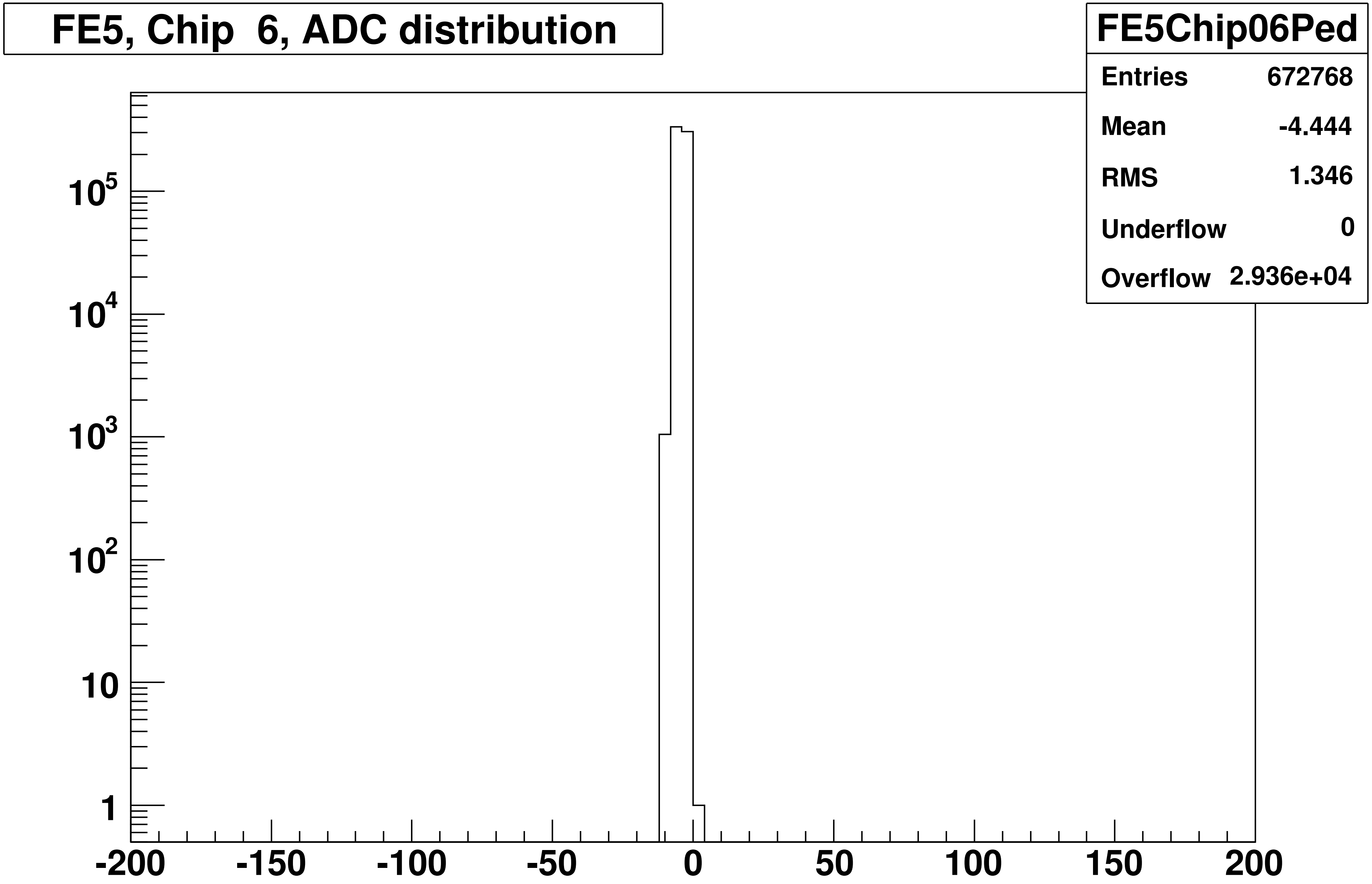
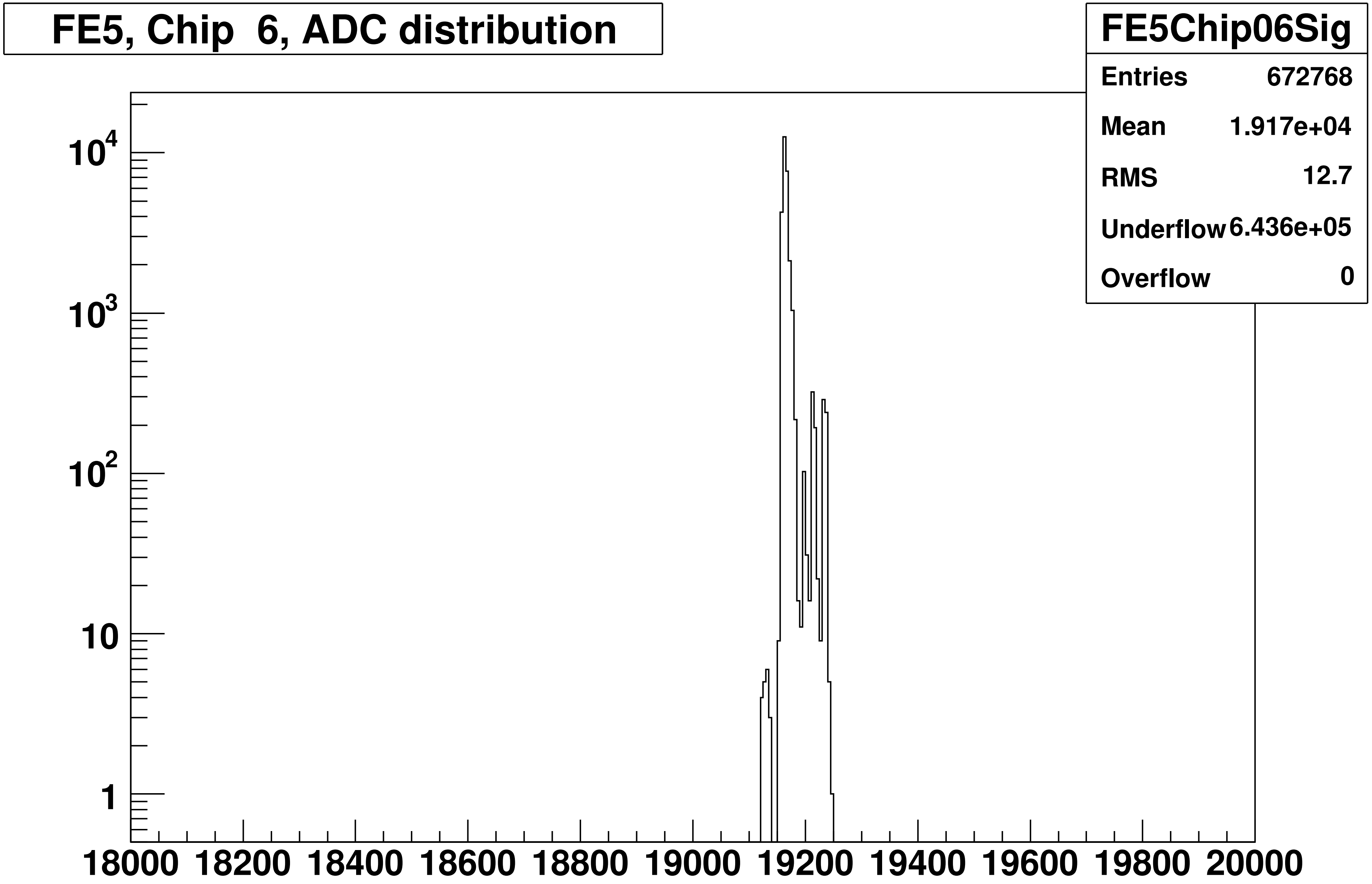
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



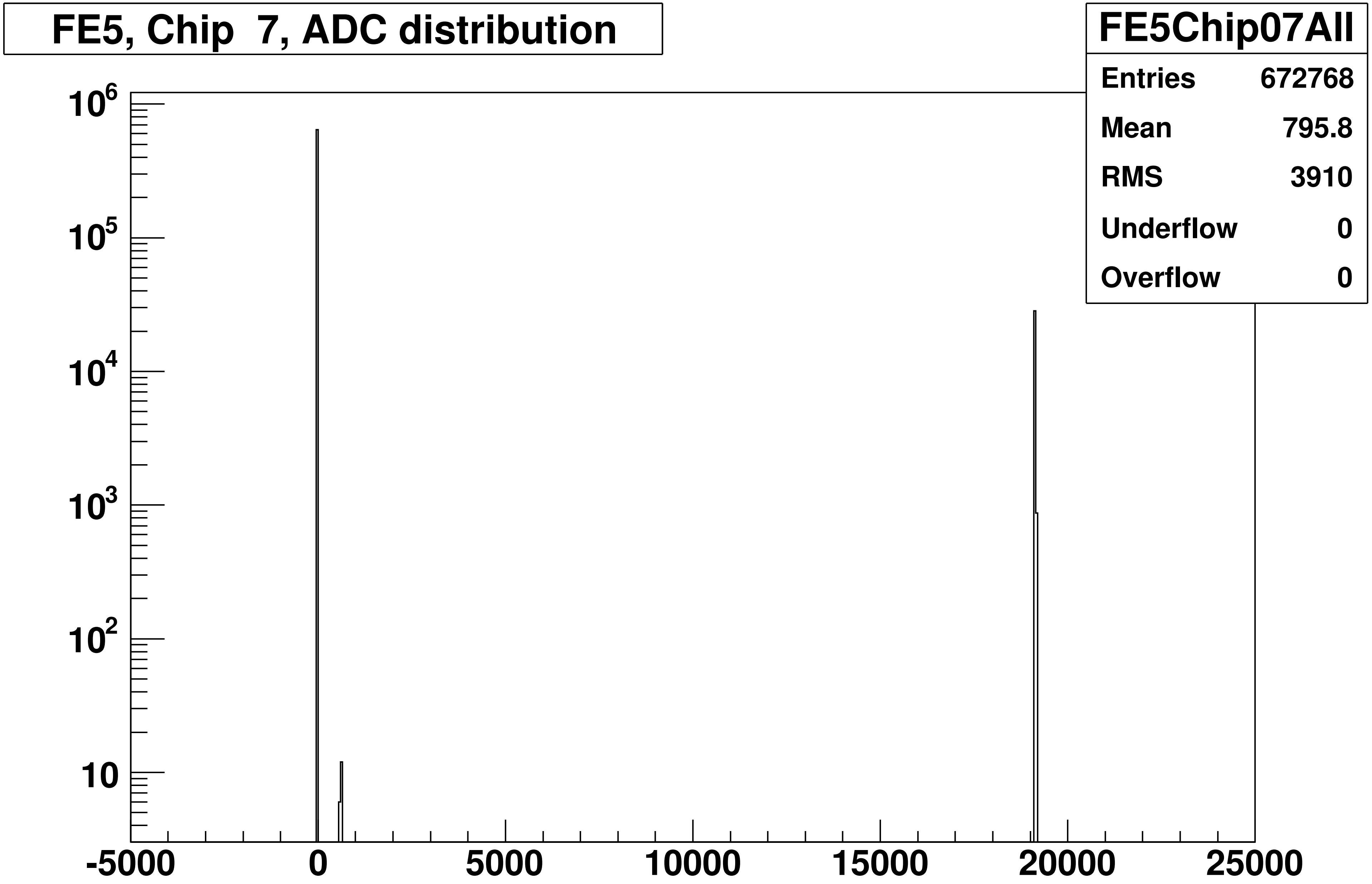
FE5, Chip 6, ADC distribution
FE5Chip06All
Entries 672768
Mean 827.8
RMS 3905
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE5, Chip 6, ADC distribution
FE5Chip06Ped
Entries 672768
Mean -4.444
RMS 1.346
Underflow 0
Overflow 2.936e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
200



FE5, Chip 6, ADC distribution
FE5Chip06Sig
Entries 672768
Mean 1.917e+04
RMS 12.7
Underflow 6.436e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE5, Chip 7, ADC distribution
FE5Chip07All
Entries 672768
Mean 795.8
RMS 3910
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
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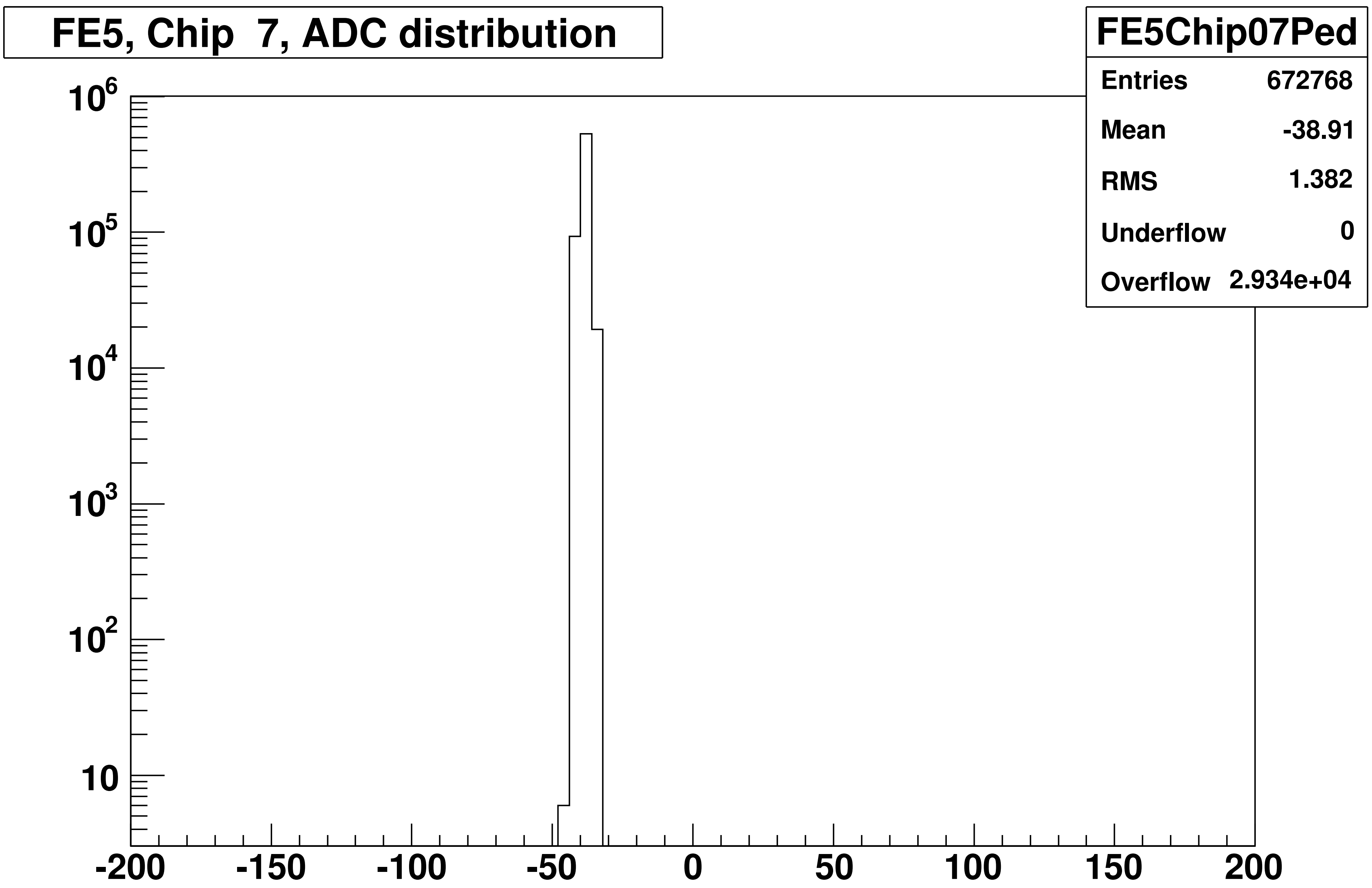
FE5, Chip 7, ADC distribution
FE5Chip07Ped
Entries 672768
Mean -38.91
RMS 1.382
Underflow 0
Overflow 2.934e+04
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10^2
10^3
10^4
10^5
10^6
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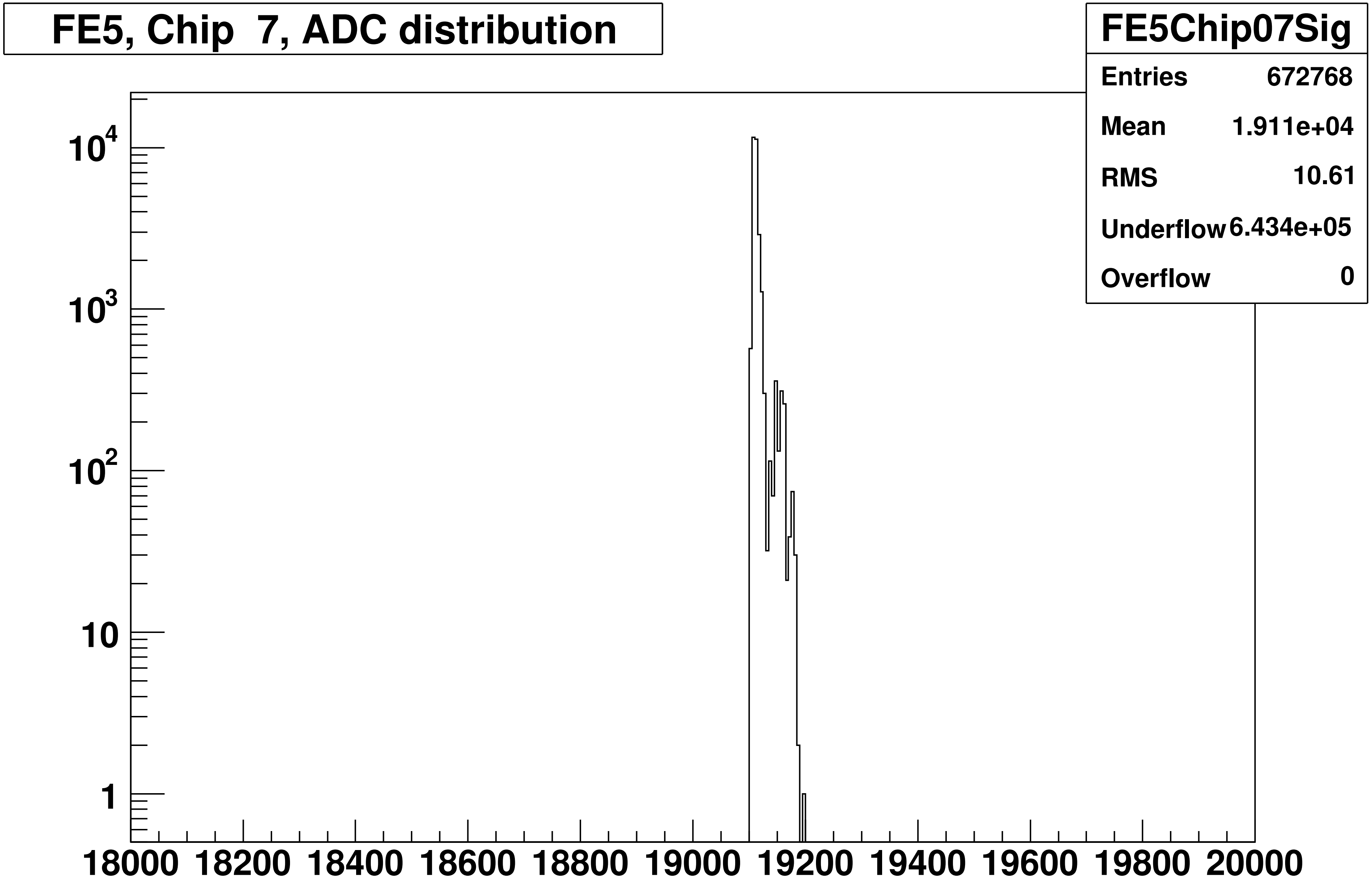
FE5, Chip 7, ADC distribution
FE5Chip07Sig
Entries 672768
Mean 1.911e+04
RMS 10.61
Underflow 6.434e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
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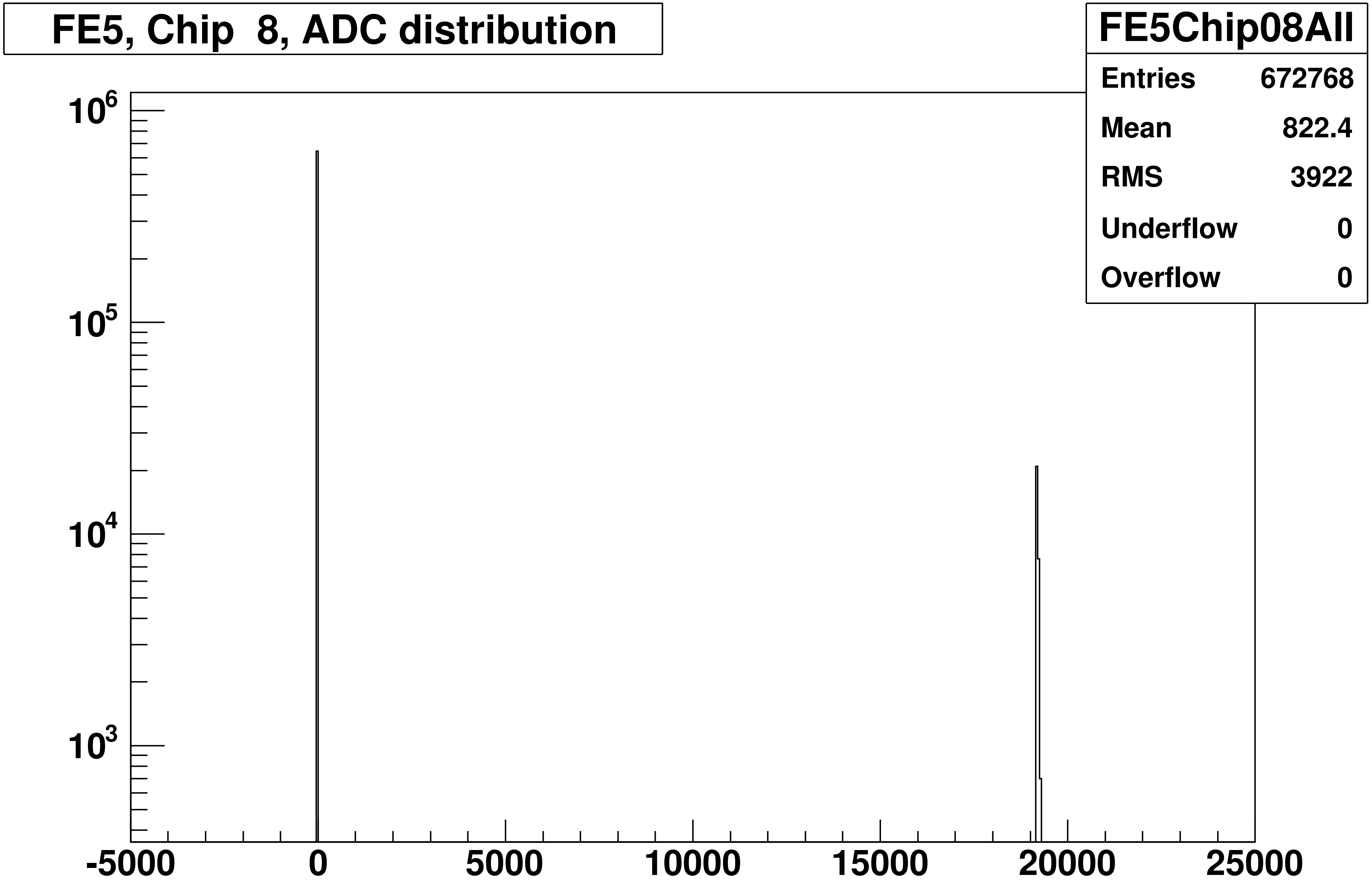
19800
20000


FE5, Chip 8, ADC distribution
FE5Chip08All
Entries 672768
Mean 822.4
RMS 3922
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
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0
5000
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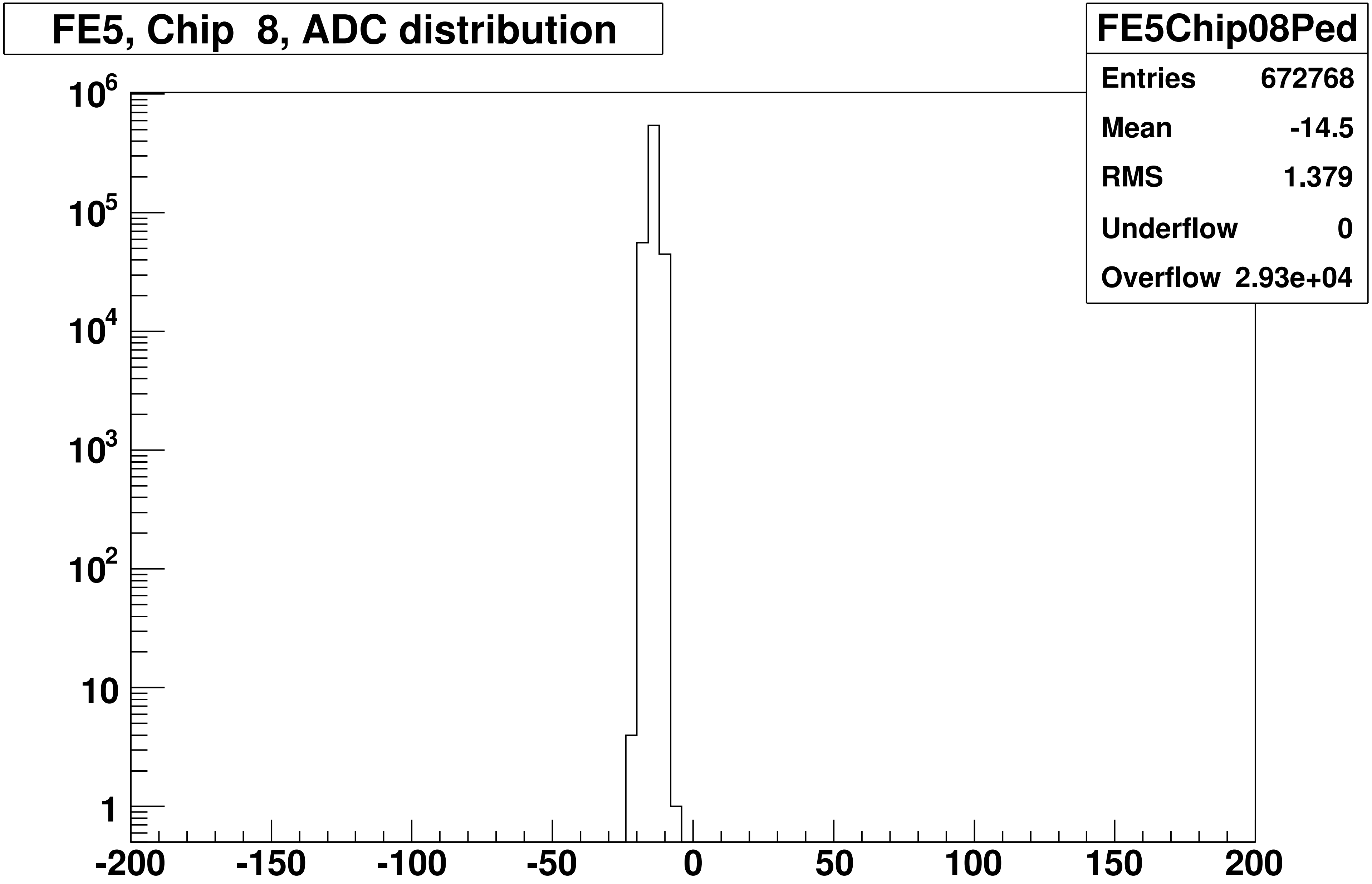
15000
20000
25000



FE5, Chip 8, ADC distribution
FE5Chip08Ped
Entries 672768
Mean -14.5
RMS 1.379
Underflow 0
Overflow 2.93e+04
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10^5
10^4
10^3
10^2
10
1
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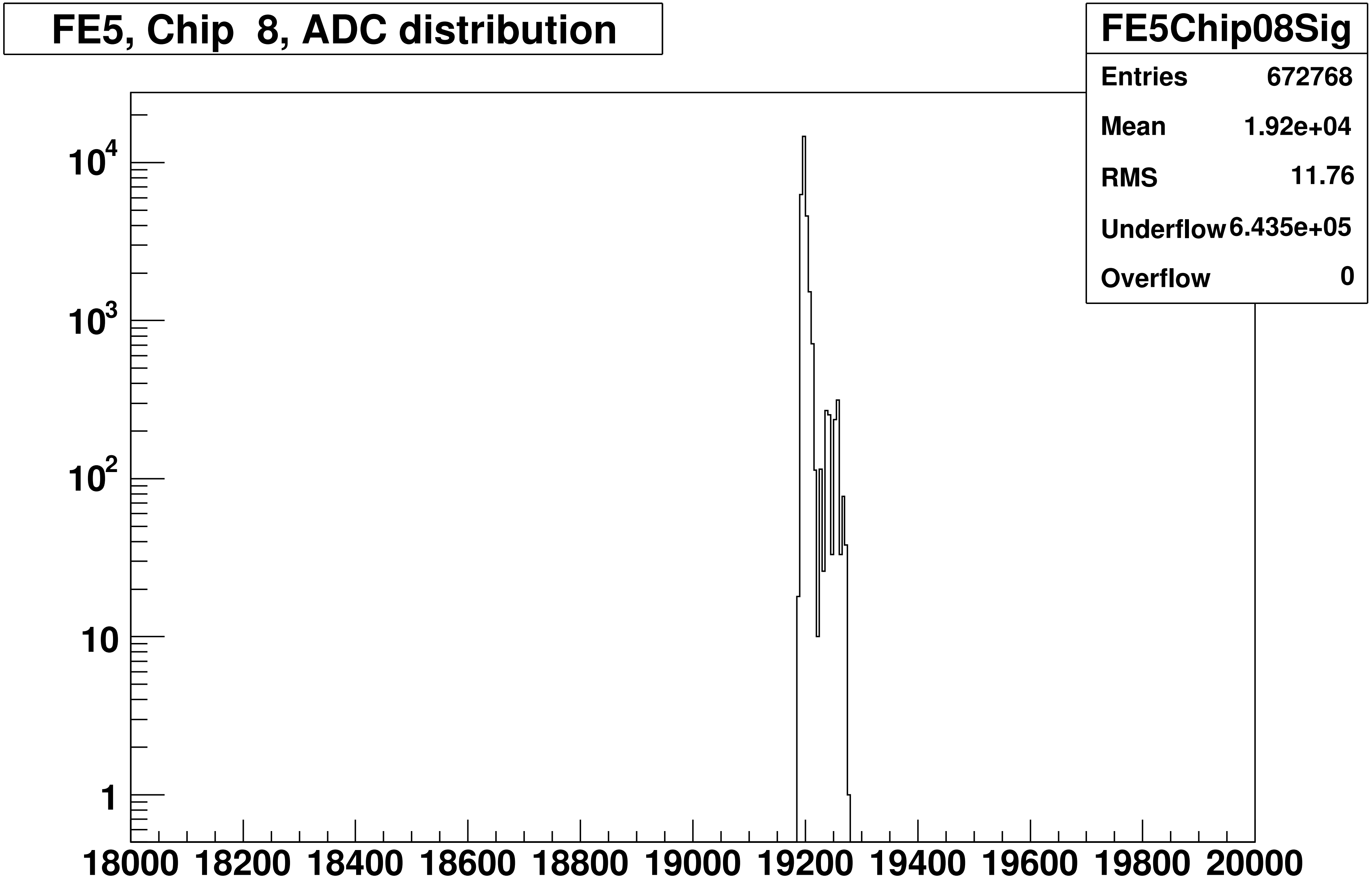

FE5, Chip 8, ADC distribution
FE5Chip08Sig
Entries 672768
Mean 1.92e+04
RMS 11.76
Underflow 6.435e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
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19000
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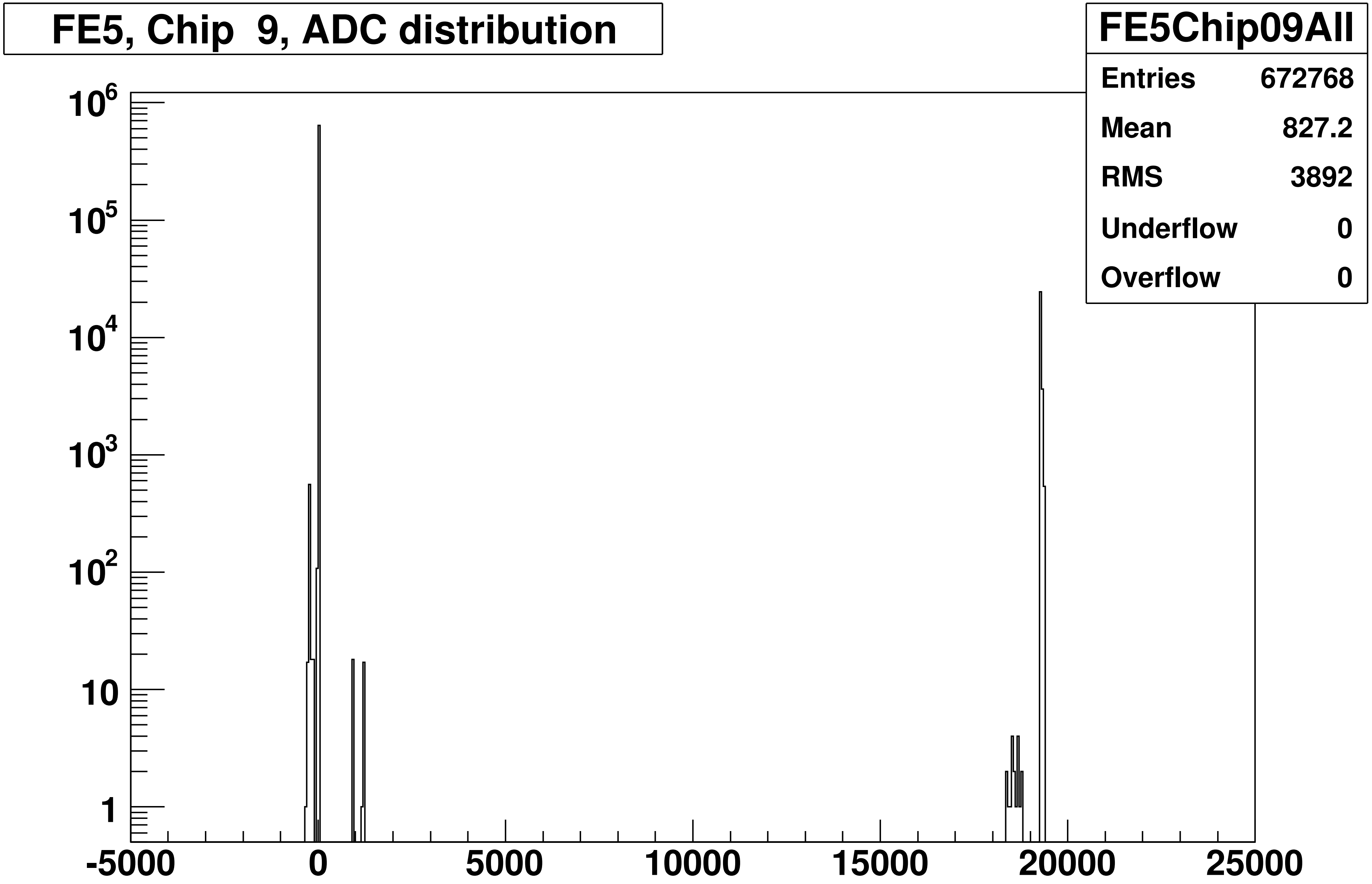
FE5, Chip 9, ADC distribution
FE5Chip09All
Entries 672768
Mean 827.2
RMS 3892
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
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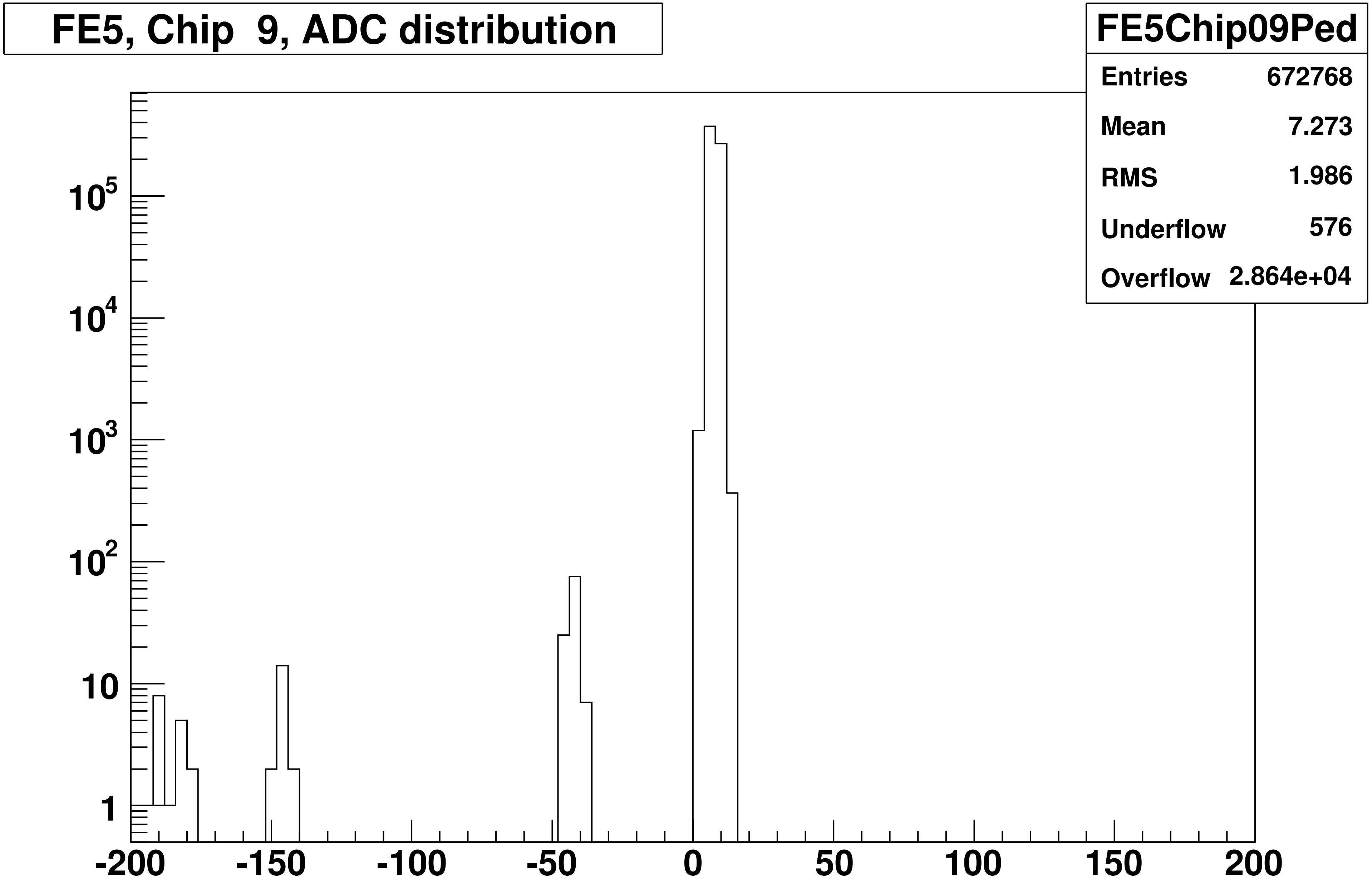
FE5, Chip 9, ADC distribution
FE5Chip09Ped
Entries 672768
Mean 7.273
RMS 1.986
Underflow 576
Overflow 2.864e+04
10^5
10^4
10^3
10^2
10
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150
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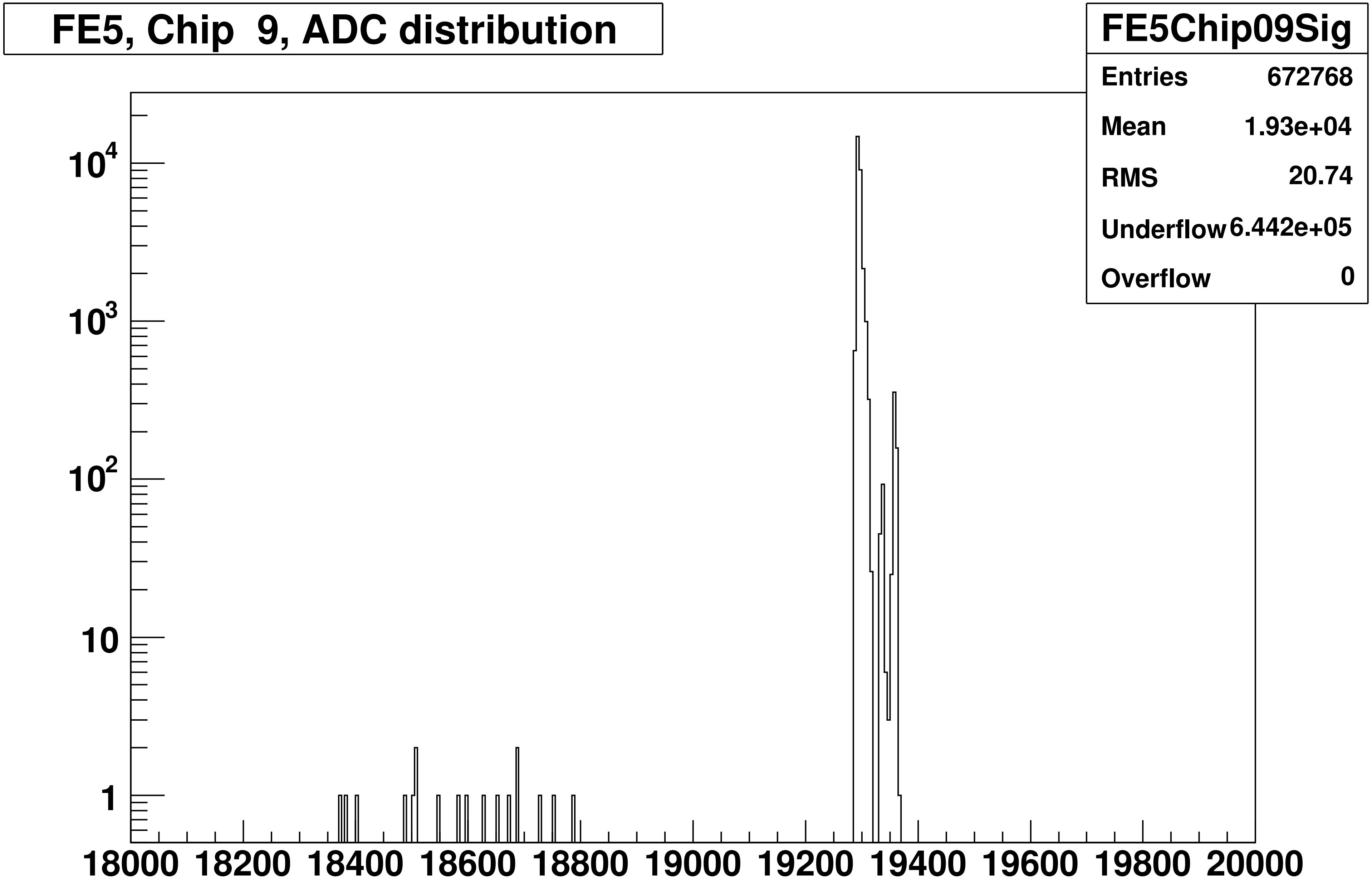

FE5, Chip 9, ADC distribution
FE5Chip09Sig
Entries 672768
Mean 1.93e+04
RMS 20.74
Underflow 6.442e+05
Overflow 0
1
10
10^2
10^3
10^4
18000
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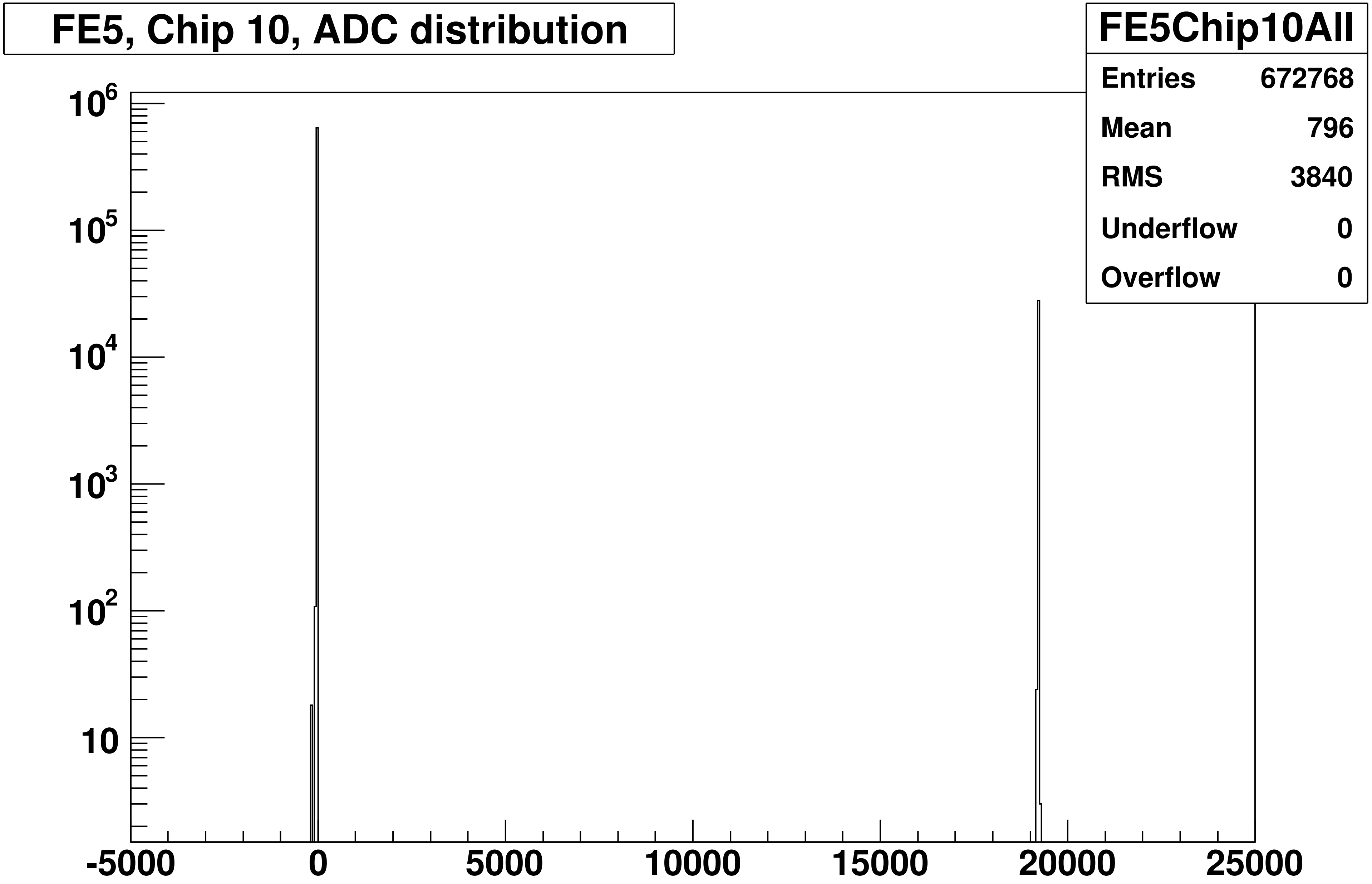
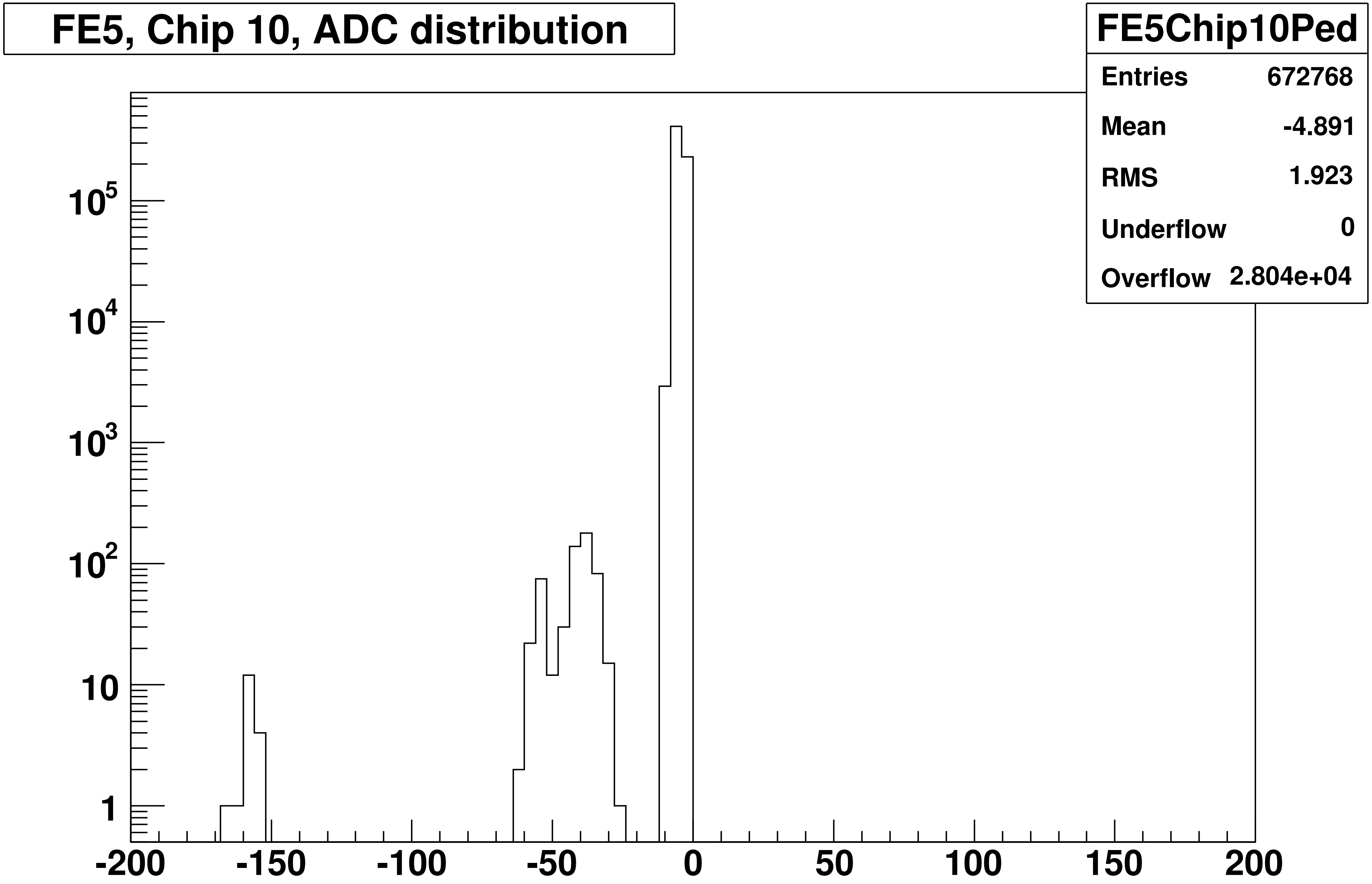
19400
19600
19800
20000


FE5, Chip 10, ADC distribution
FE5Chip10All
Entries 672768
Mean 796
RMS 3840
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE5, Chip 10, ADC distribution
FE5Chip10Ped
Entries 672768
Mean -4.891
RMS 1.923
Underflow 0
Overflow 2.804e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
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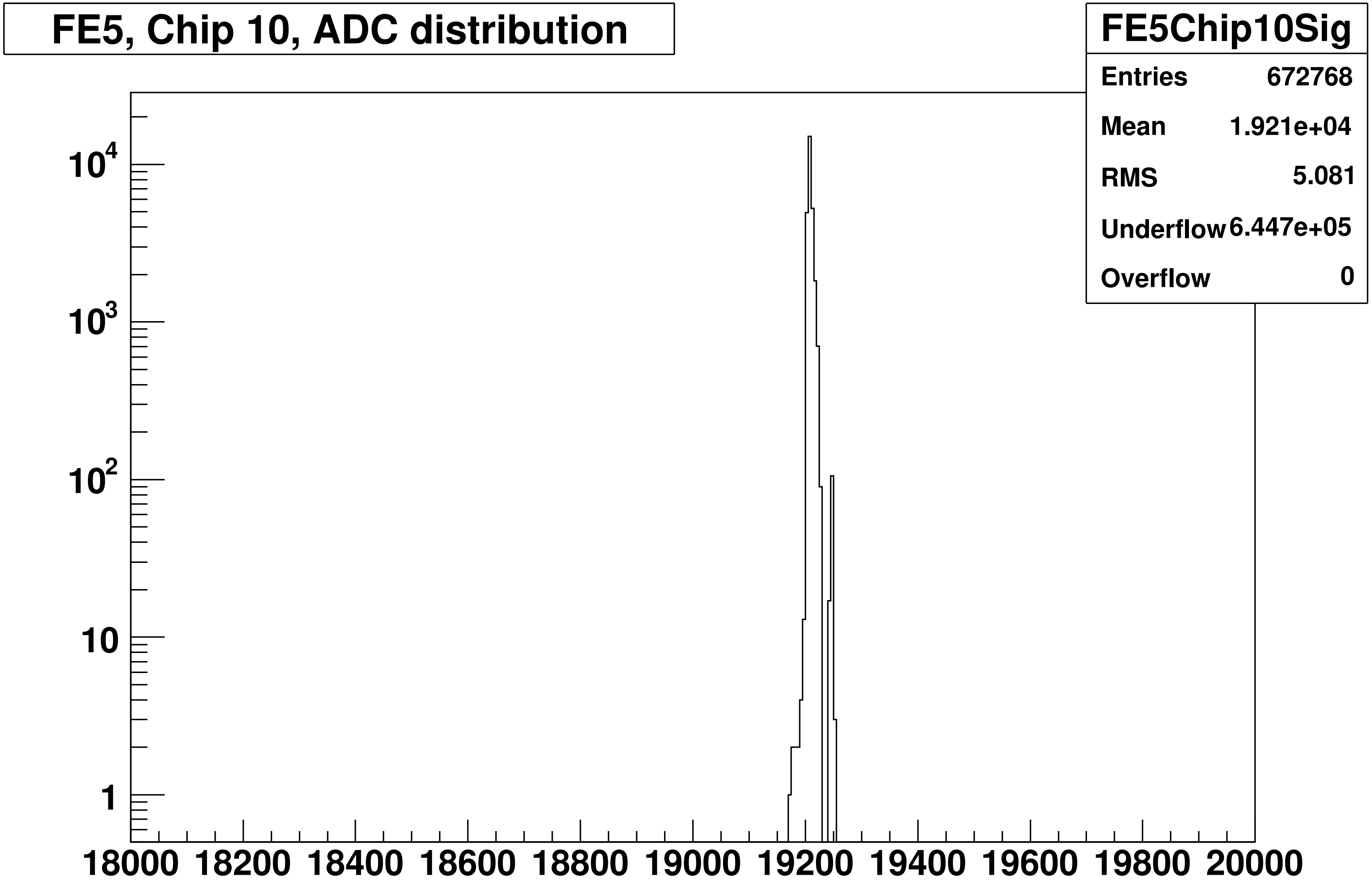
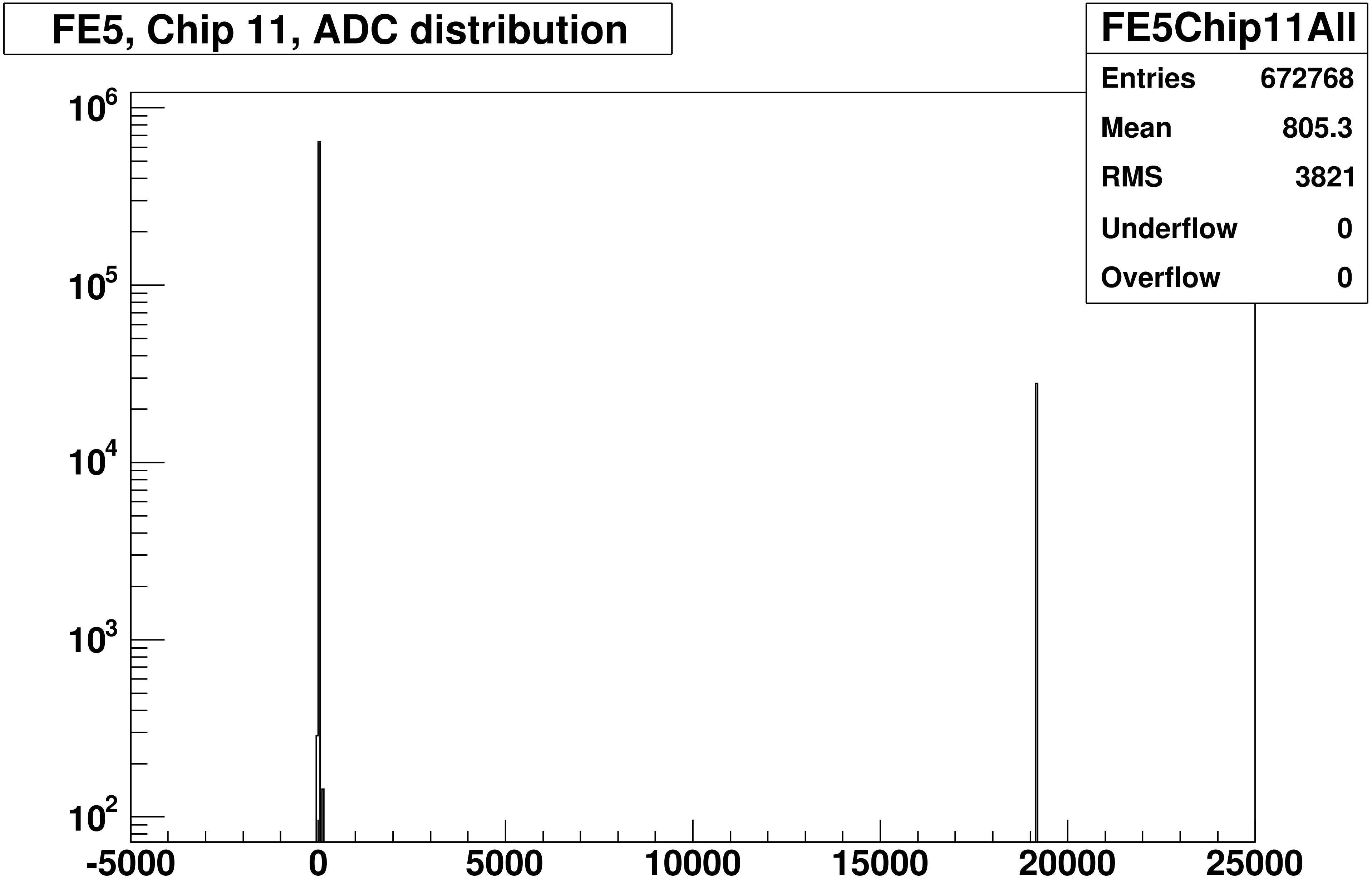
0
50
100
150
200


FE5, Chip 10, ADC distribution
FE5Chip10Sig
Entries 672768
Mean 1.921e+04
RMS 5.081
Underflow 6.447e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE5, Chip 11, ADC distribution
FE5Chip11All
Entries 672768
Mean 805.3
RMS 3821
Underflow 0
Overflow 0
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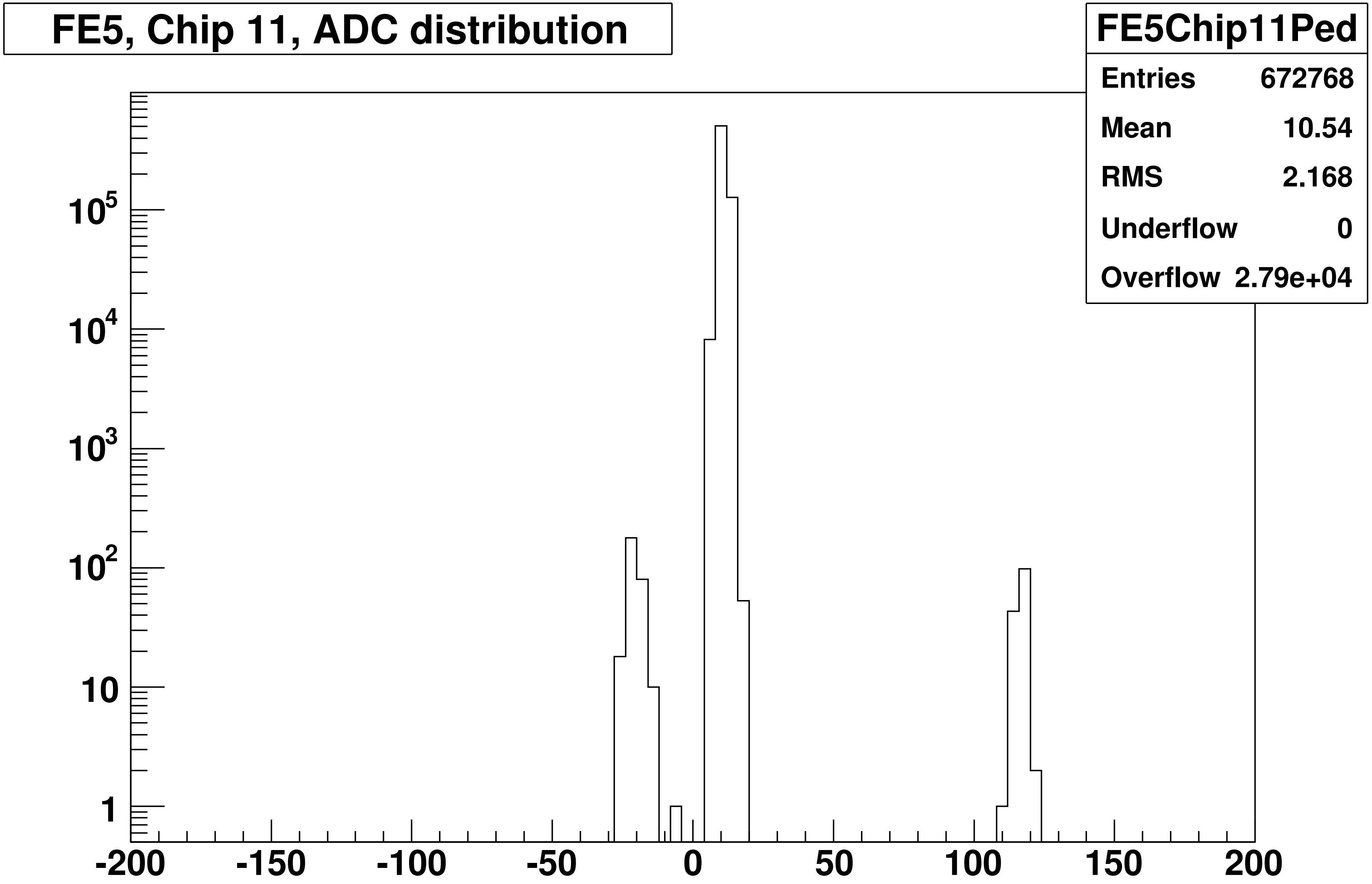
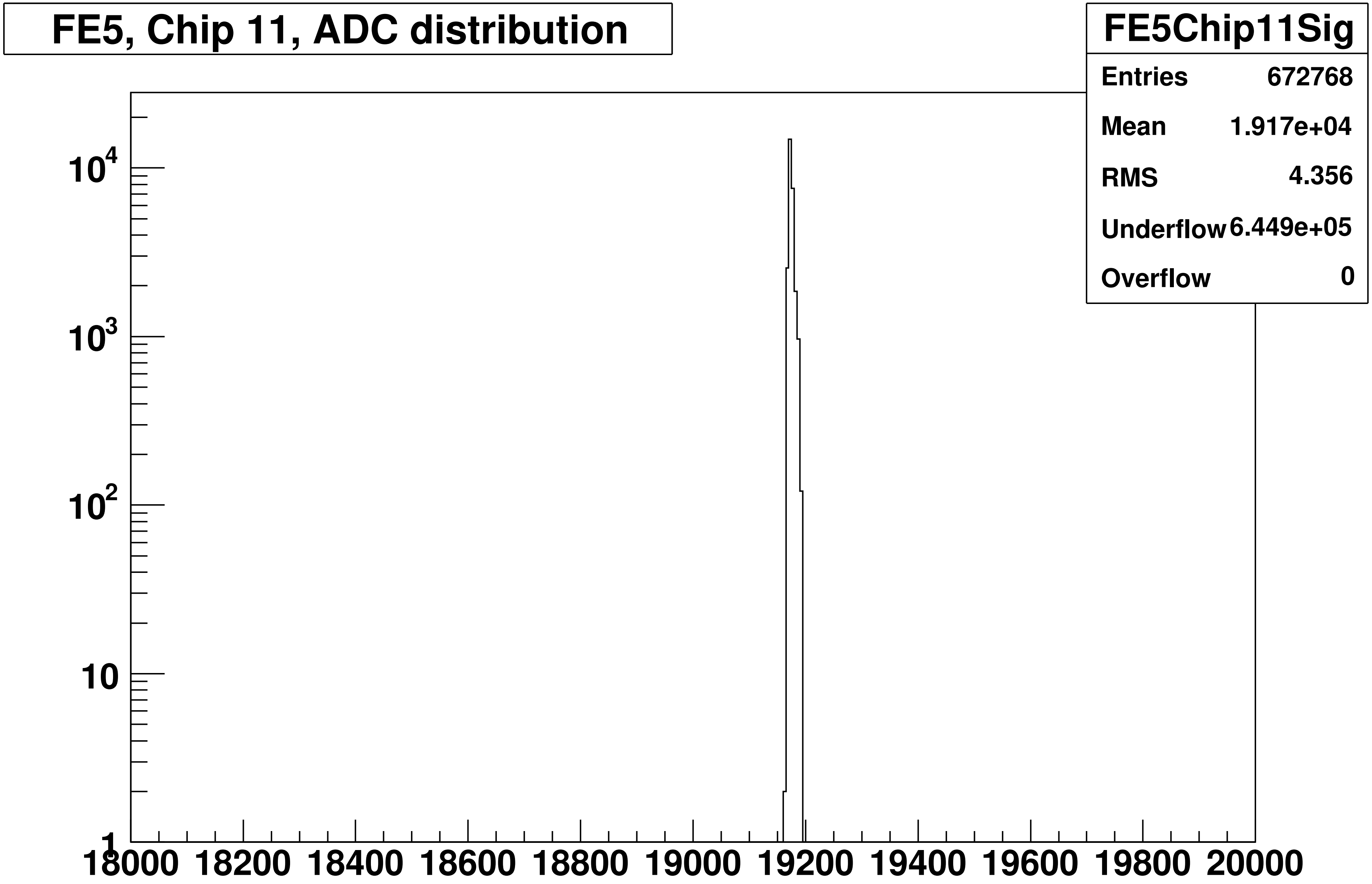
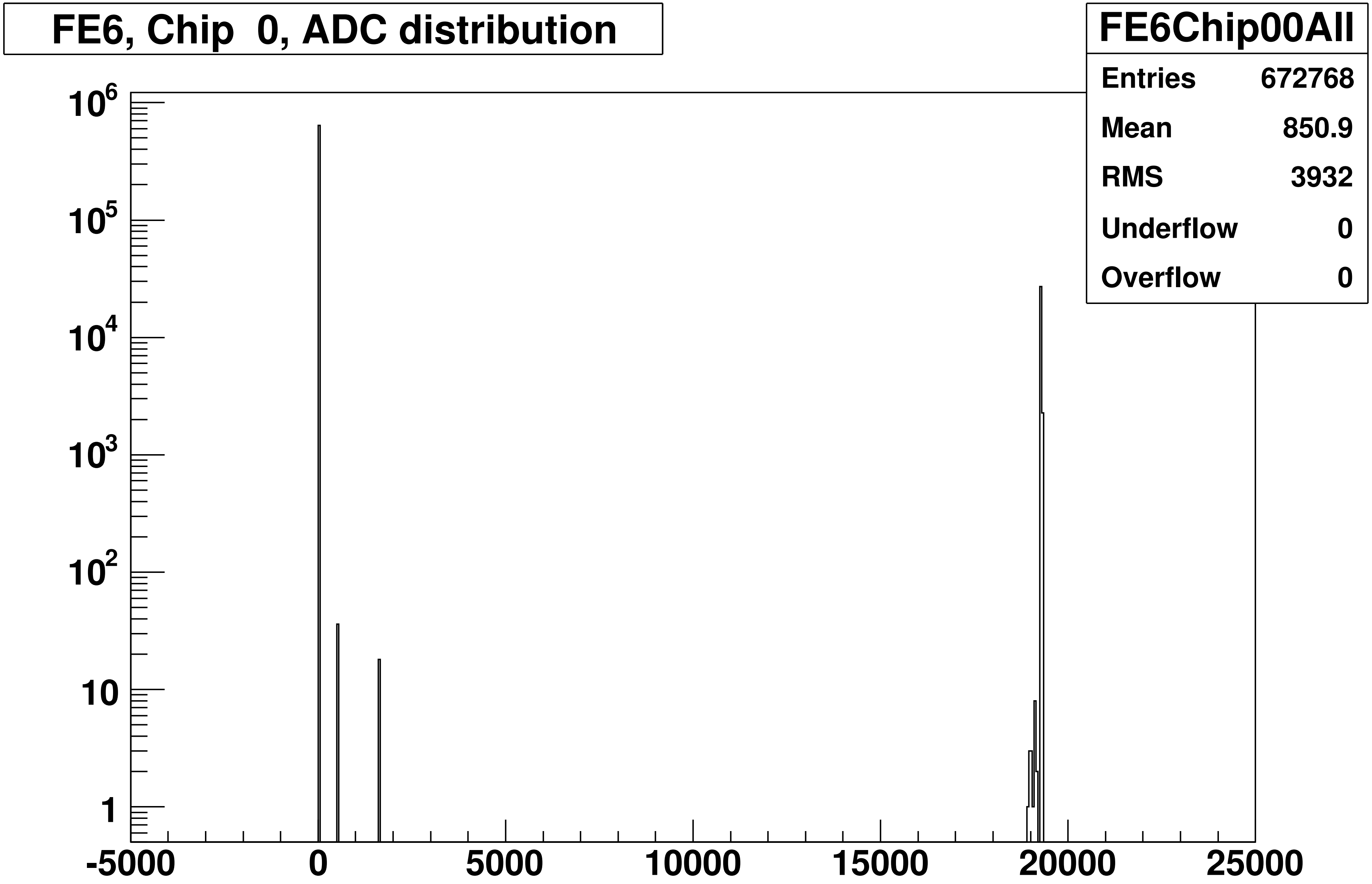
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000


FE5, Chip 11, ADC distribution
FE5Chip11Ped
Entries 672768
Mean 10.54
RMS 2.168
Underflow 0
Overflow 2.79e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
200



FE5, Chip 11, ADC distribution
FE5Chip11Sig
Entries 672768
Mean 1.917e+04
RMS 4.356
Underflow 6.449e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE6, Chip 0, ADC distribution
FE6Chip00All
Entries 672768
Mean 850.9
RMS 3932
Underflow 0
Overflow 0
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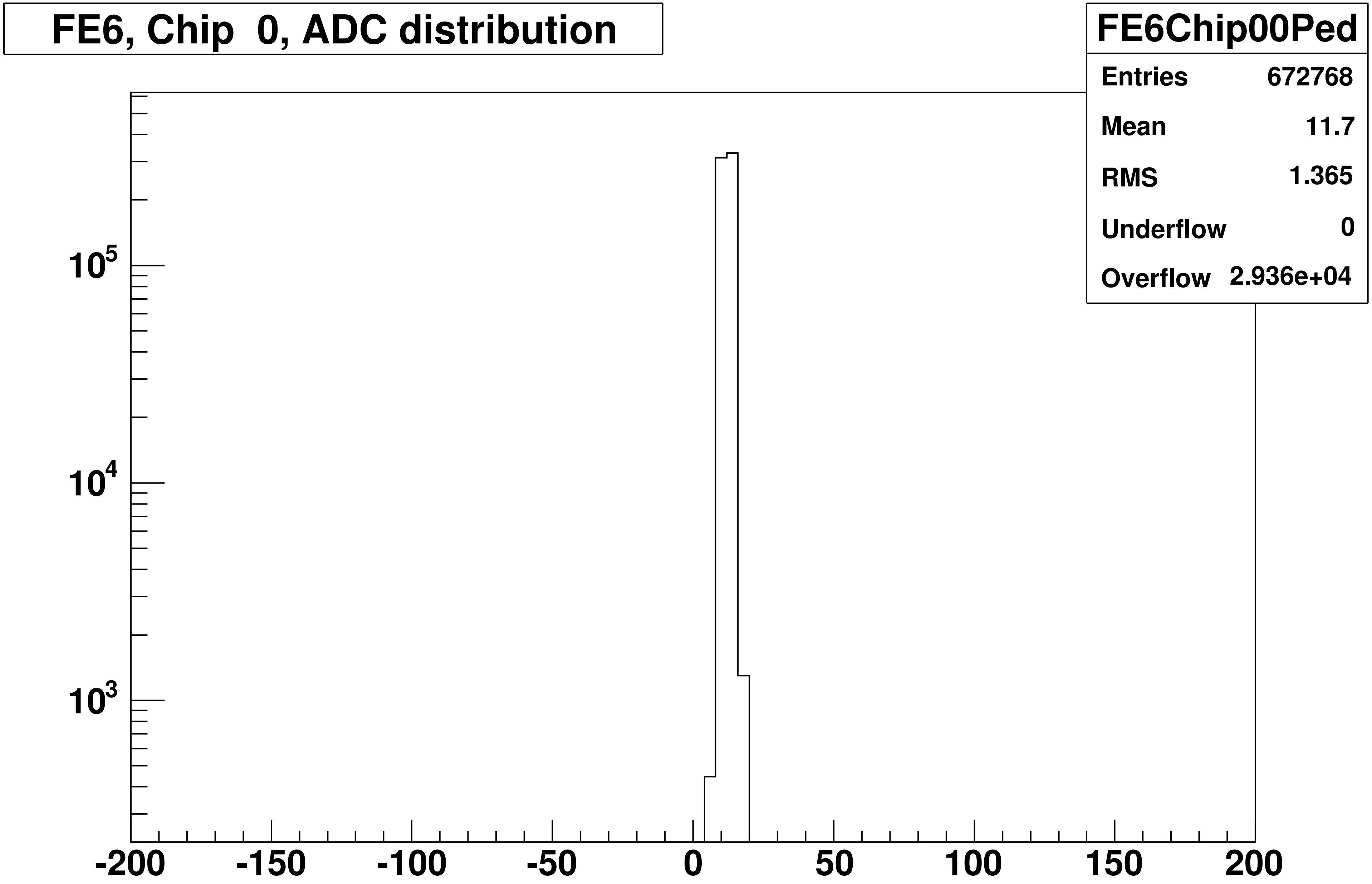
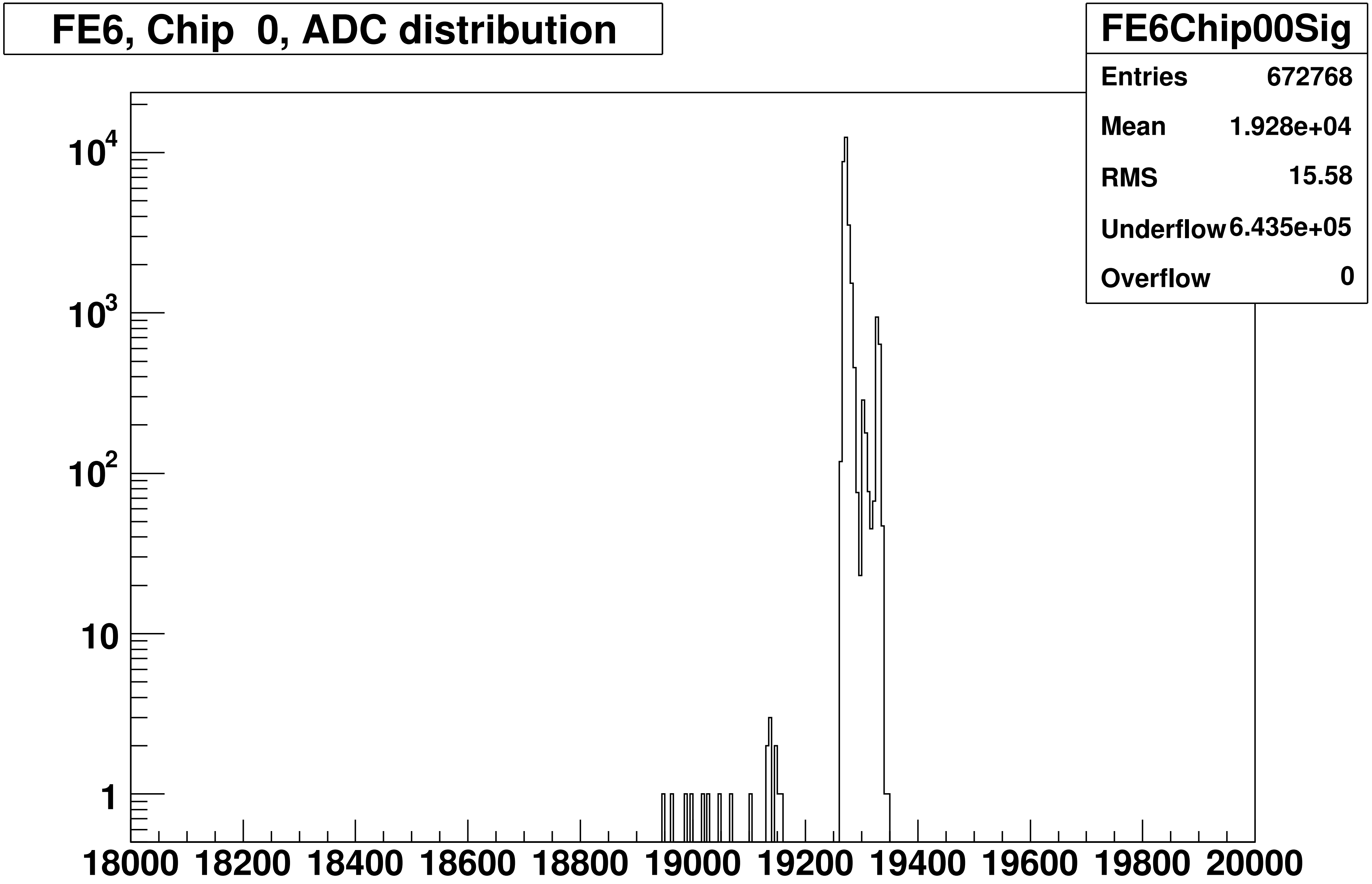
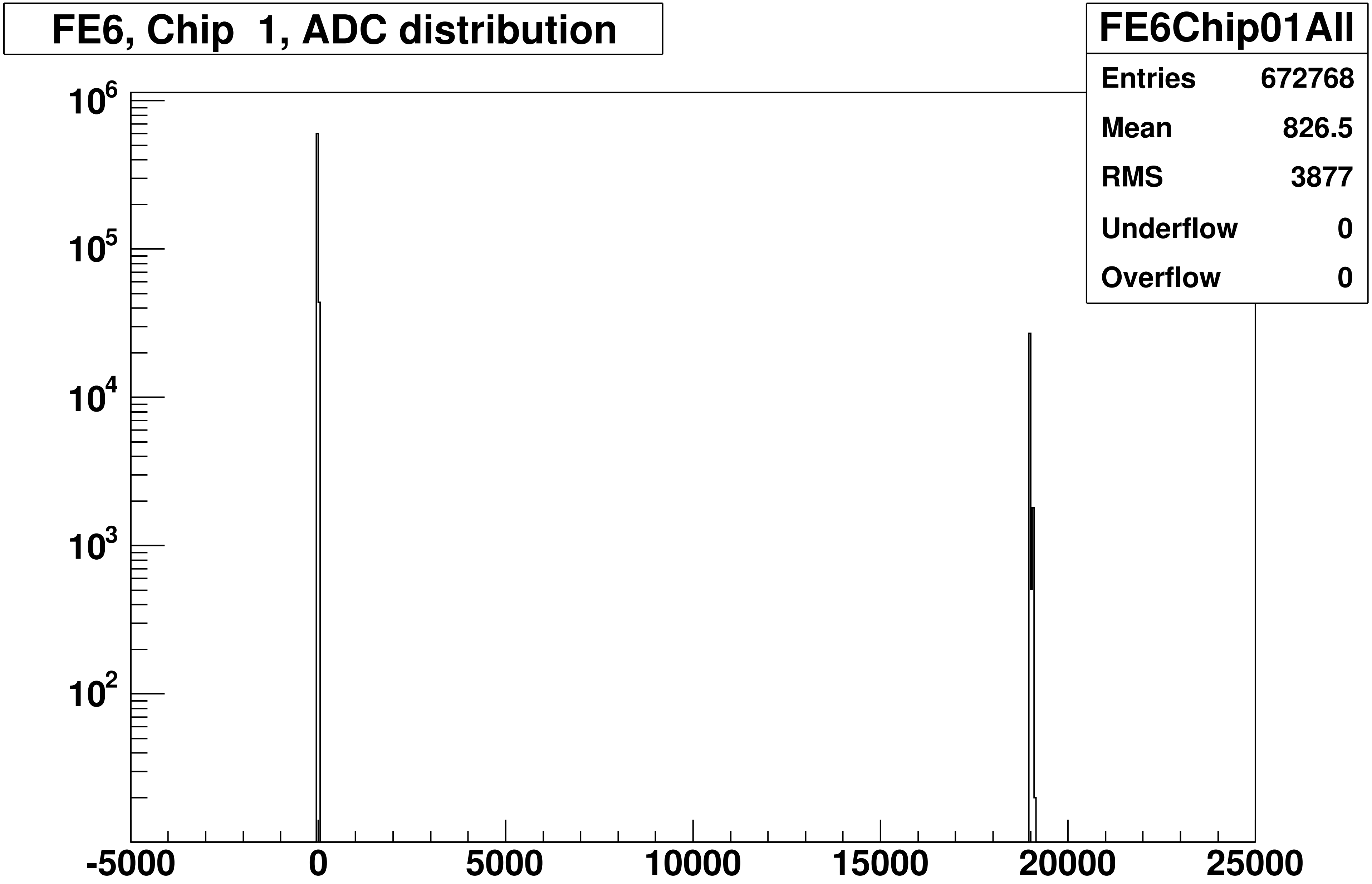
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE6, Chip 0, ADC distribution
FE6Chip00Ped
Entries 672768
Mean 11.7
RMS 1.365
Underflow 0
Overflow 2.936e+04
10^5
10^4
10^3
-200
-150
-100
-50
0
50
100
150
200


FE6, Chip 0, ADC distribution
FE6Chip00Sig
Entries 672768
Mean 1.928e+04
RMS 15.58
Underflow 6.435e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE6, Chip 1, ADC distribution
FE6Chip01All
Entries 672768
Mean 826.5
RMS 3877
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
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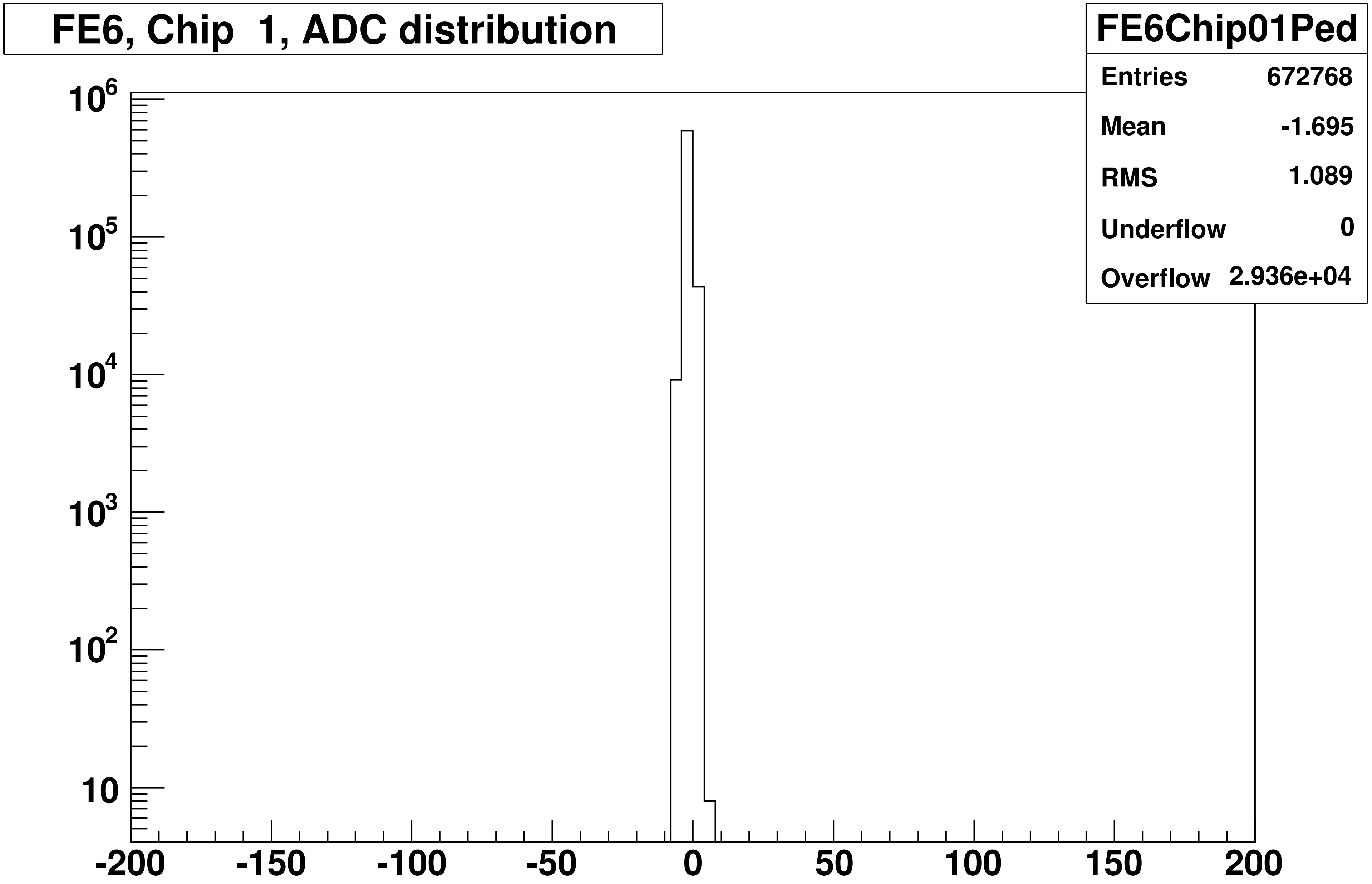
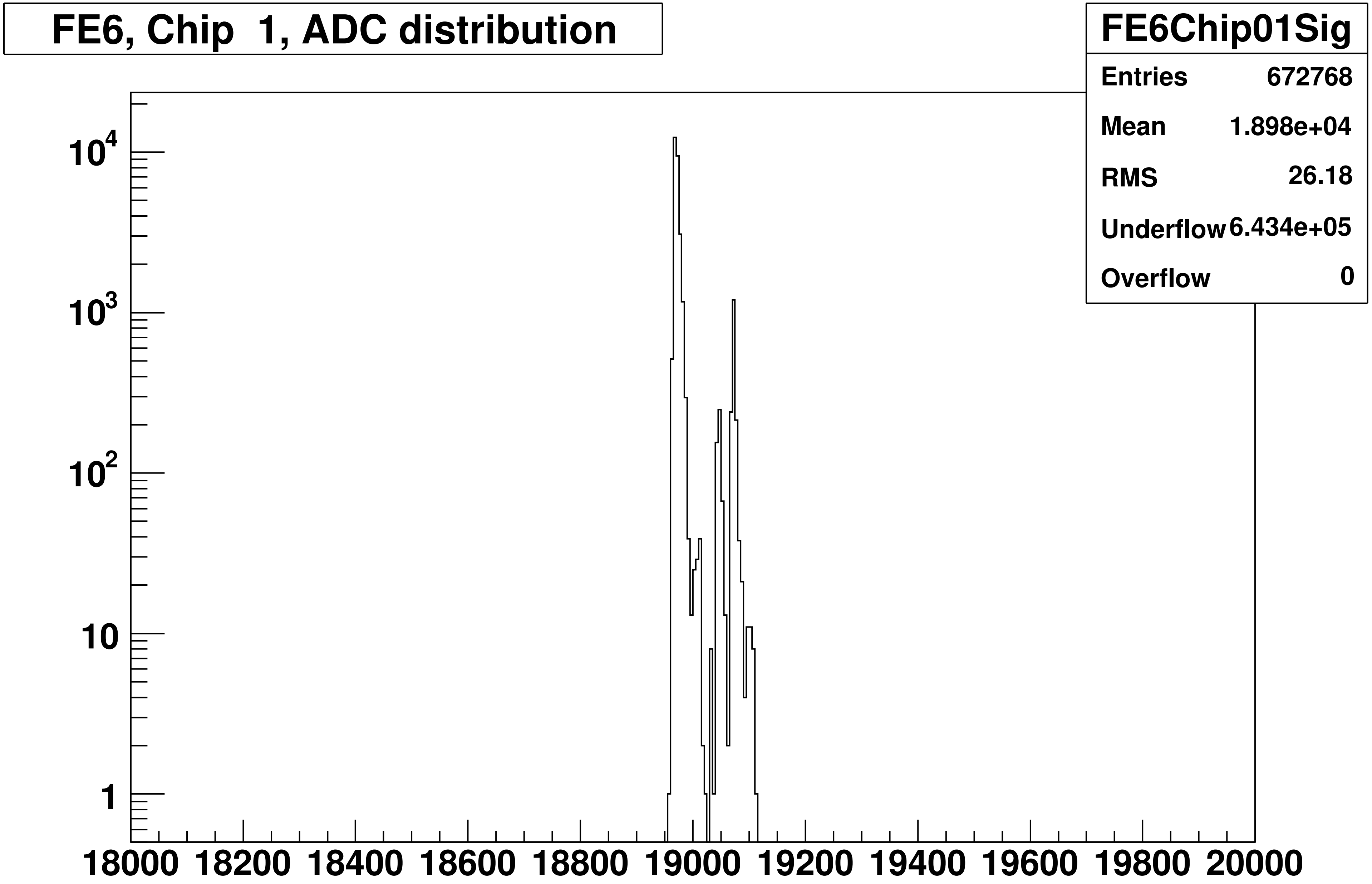
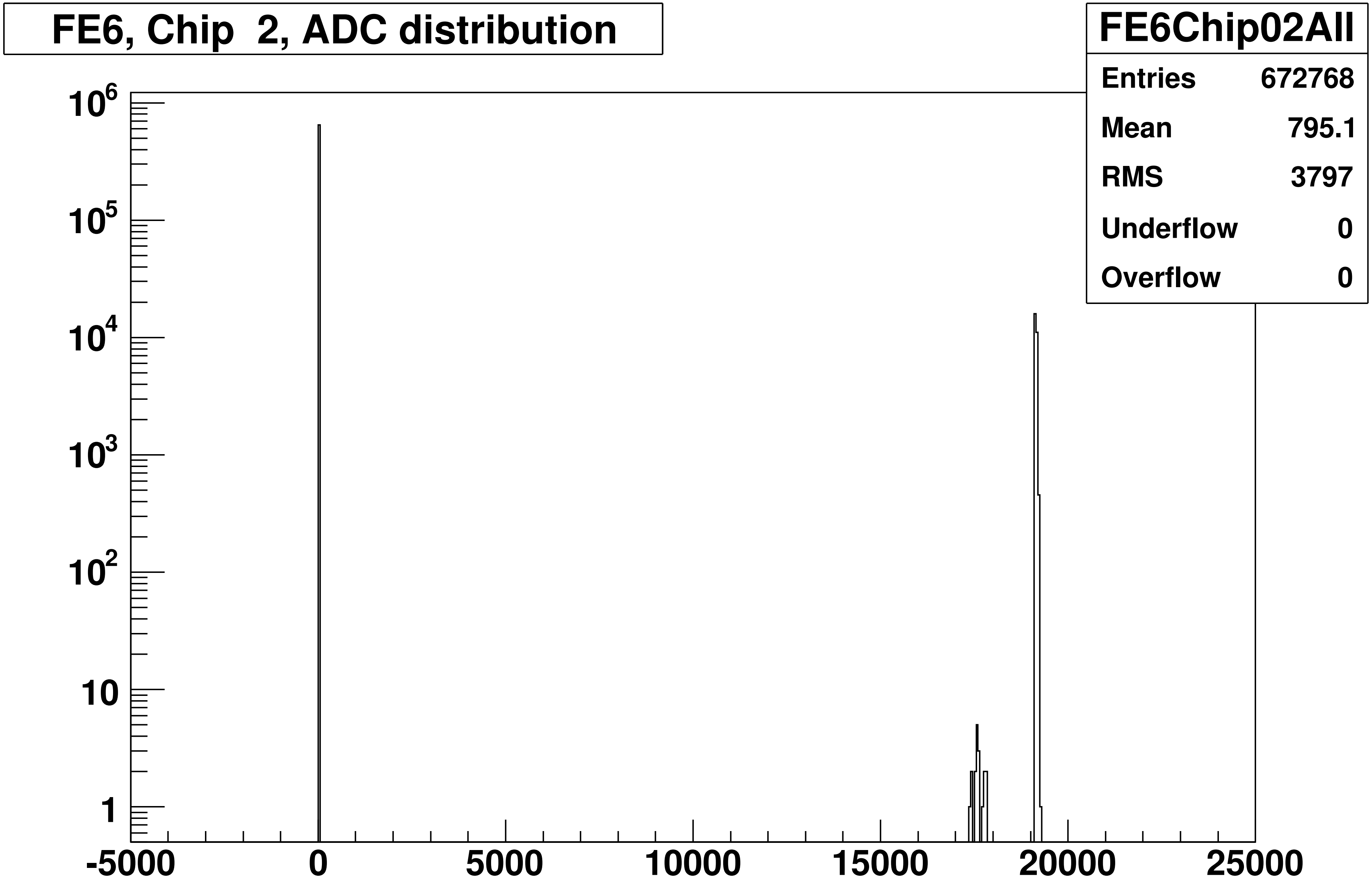
0
5000
10000
15000
20000
25000



FE6, Chip 1, ADC distribution
FE6Chip01Ped
Entries 672768
Mean -1.695
RMS 1.089
Underflow 0
Overflow 2.936e+04
10^6
10^5
10^4
10^3
10^2
10
-200
-150
-100
-50
0
50
100
150
200



FE6, Chip 1, ADC distribution
FE6Chip01Sig
Entries 672768
Mean 1.898e+04
RMS 26.18
Underflow 6.434e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000


FE6, Chip 2, ADC distribution
FE6Chip02All
Entries 672768
Mean 795.1
RMS 3797
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
1
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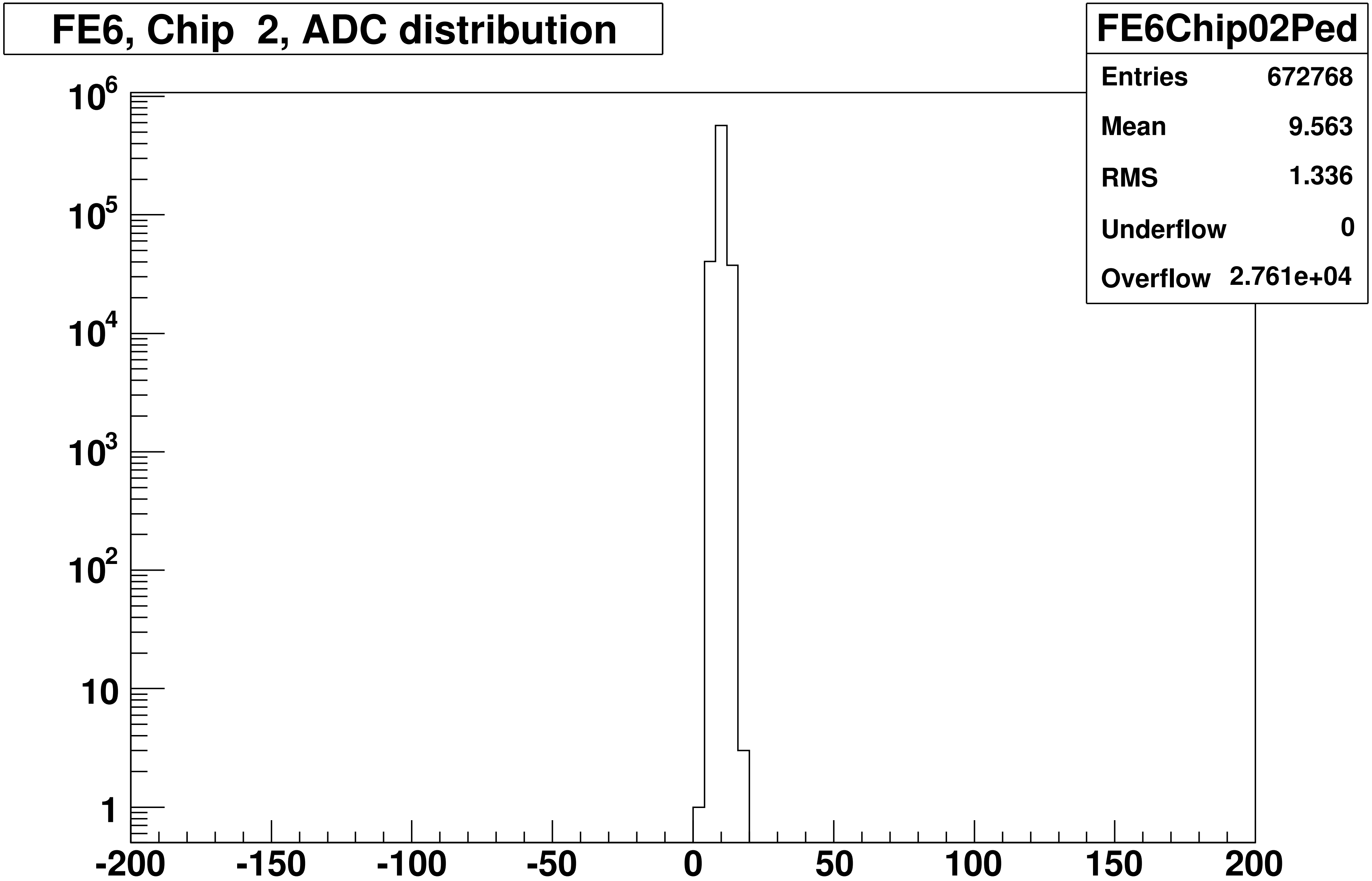
0
5000
10000
15000
20000
25000


FE6, Chip 2, ADC distribution
FE6Chip02Ped
Entries 672768
Mean 9.563
RMS 1.336
Underflow 0
Overflow 2.761e+04
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10^5
10^4
10^3
10^2
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1
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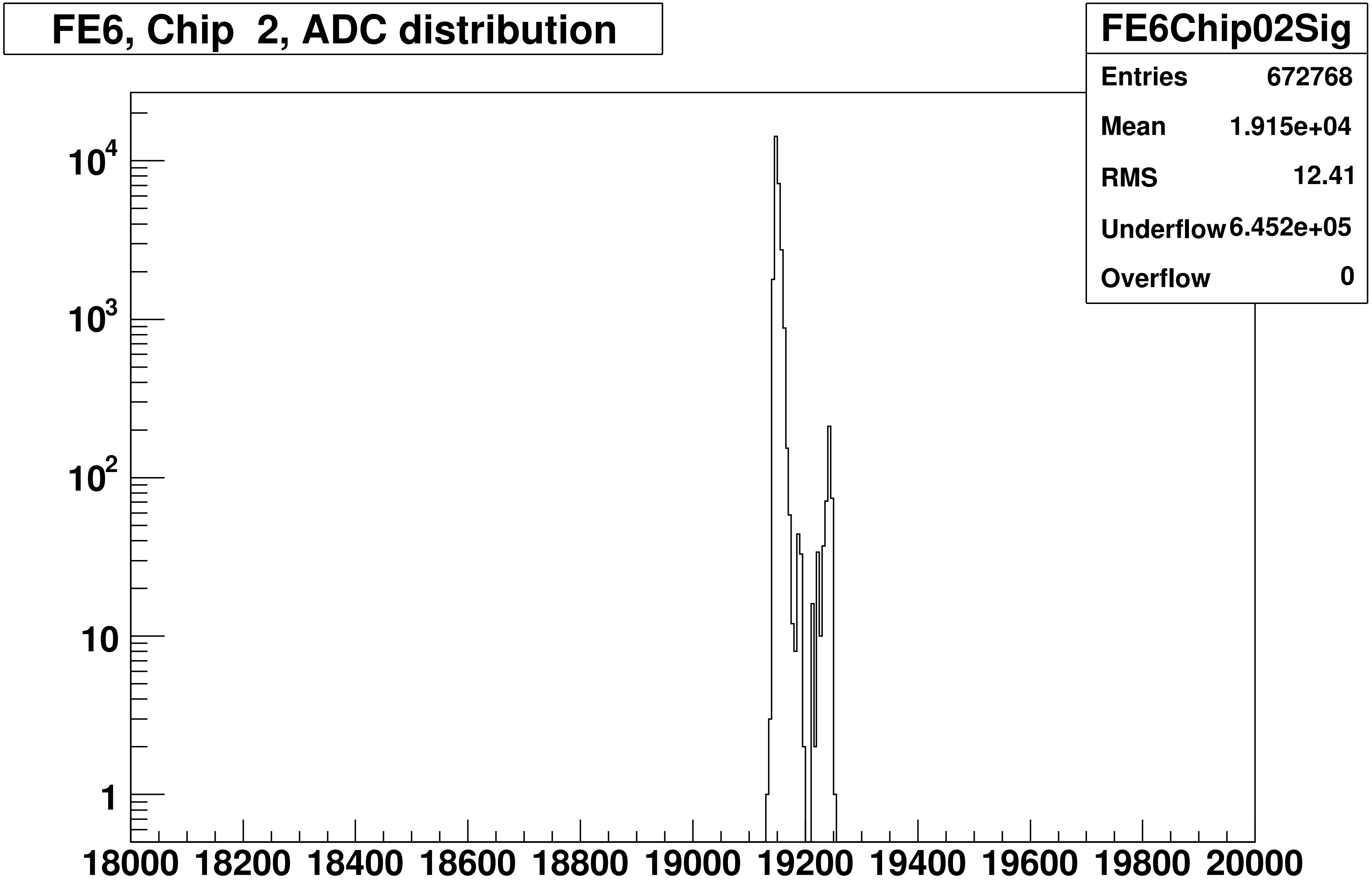
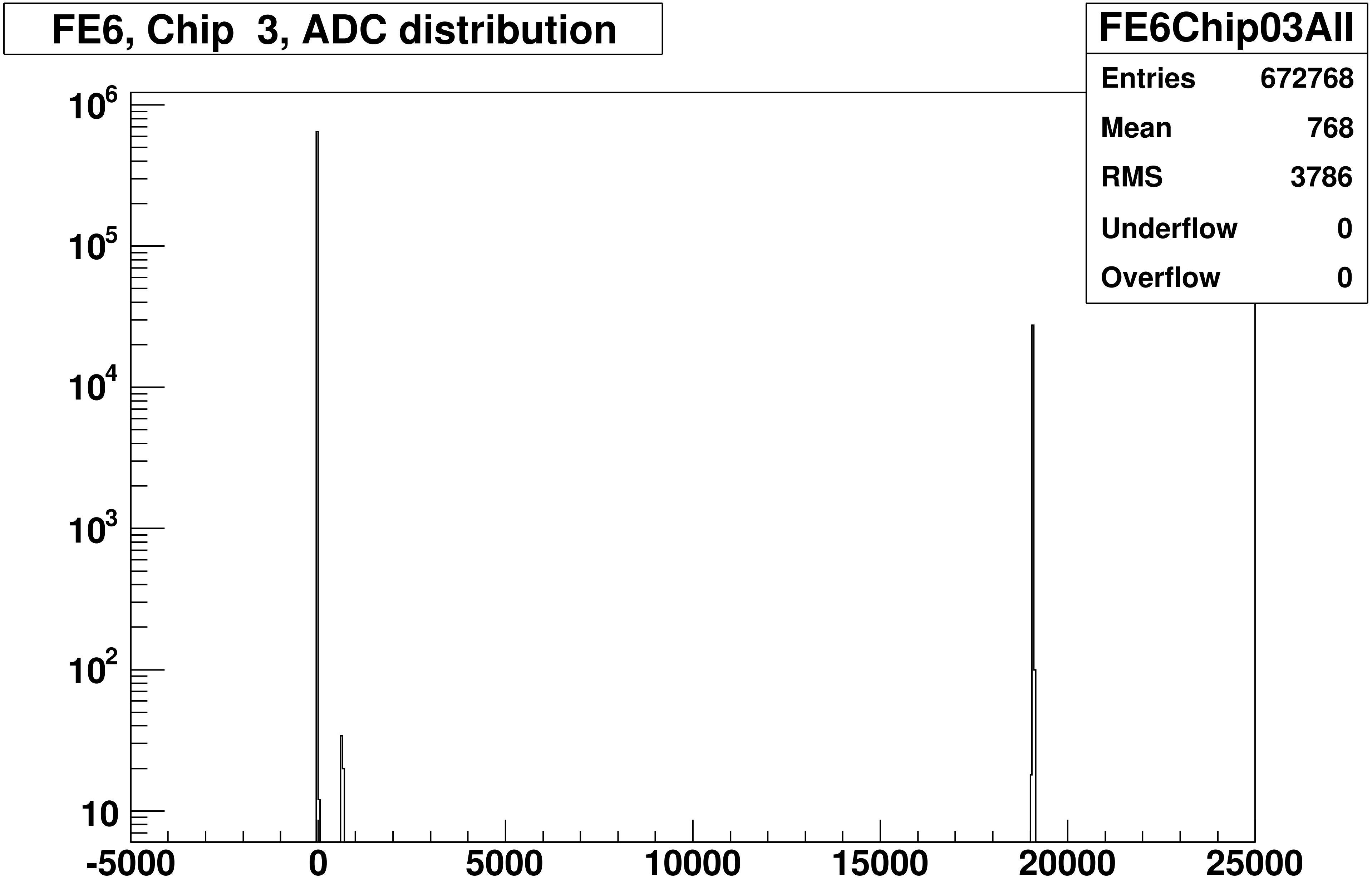

FE6, Chip 2, ADC distribution
FE6Chip02Sig
Entries 672768
Mean 1.915e+04
RMS 12.41
Underflow 6.452e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000


FE6, Chip 3, ADC distribution
FE6Chip03All
Entries 672768
Mean 768
RMS 3786
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
-5000
0
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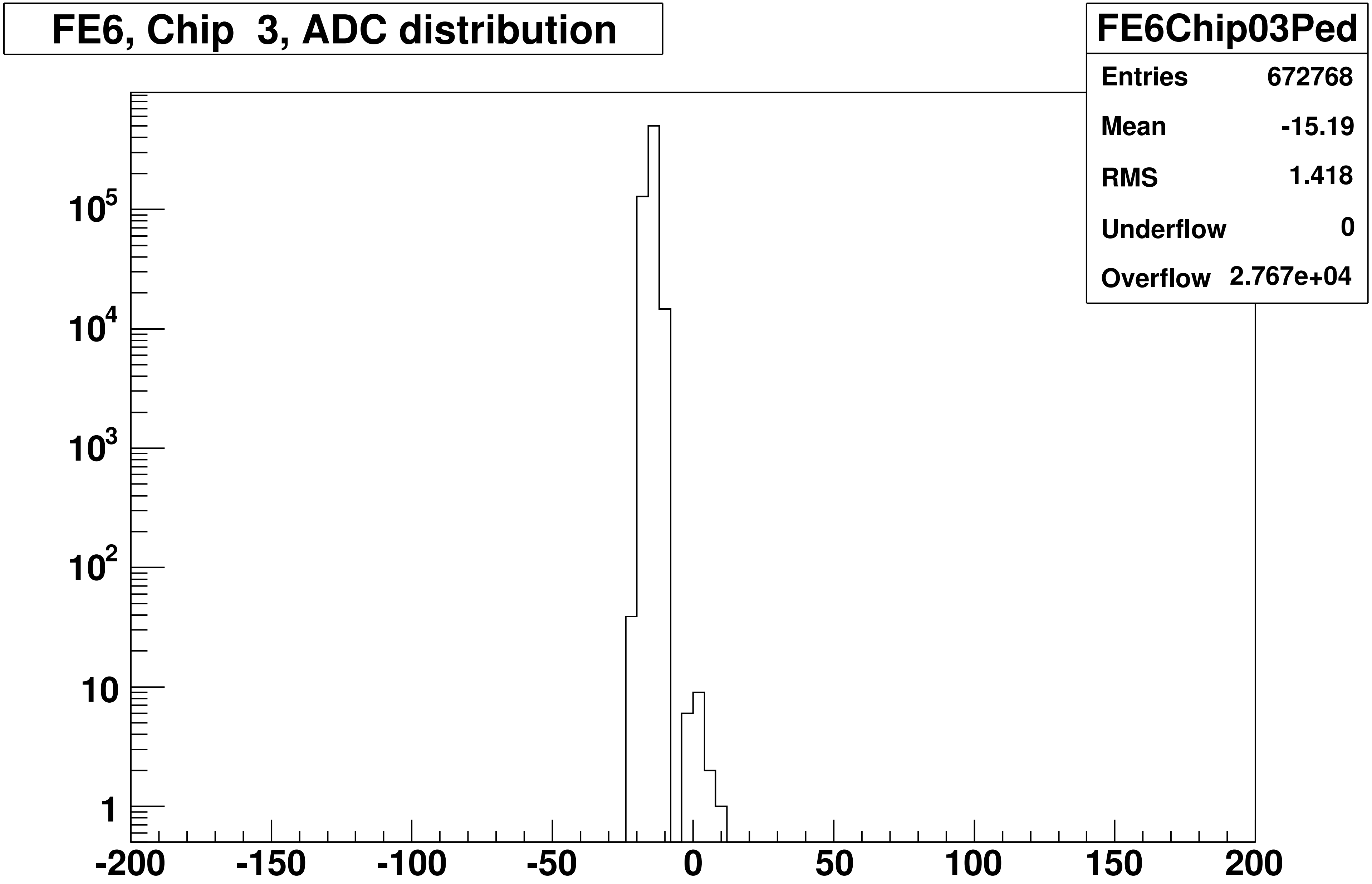
20000
25000



FE6, Chip 3, ADC distribution
FE6Chip03Ped
Entries 672768
Mean -15.19
RMS 1.418
Underflow 0
Overflow 2.767e+04
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10^4
10^3
10^2
10
1
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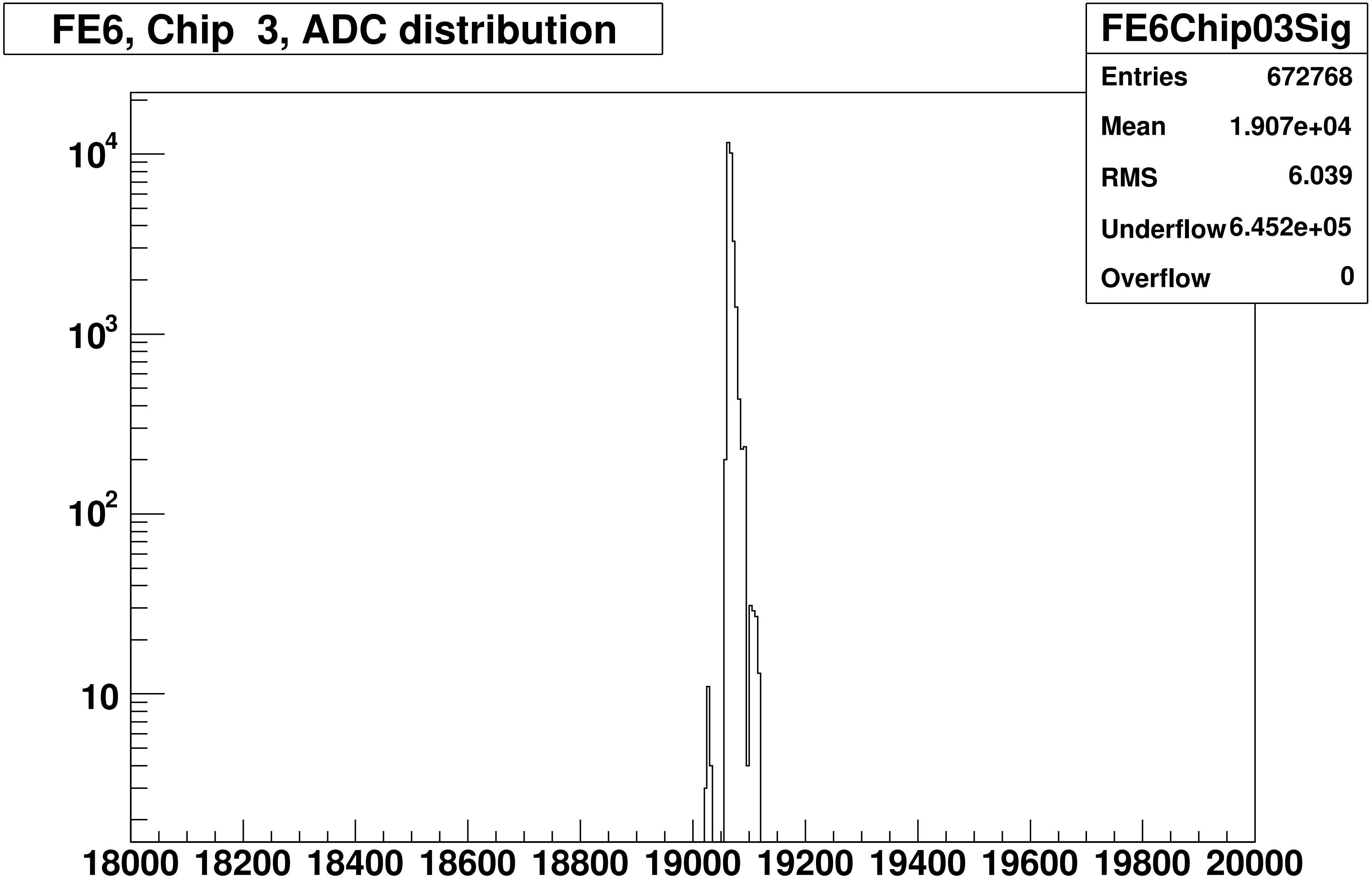
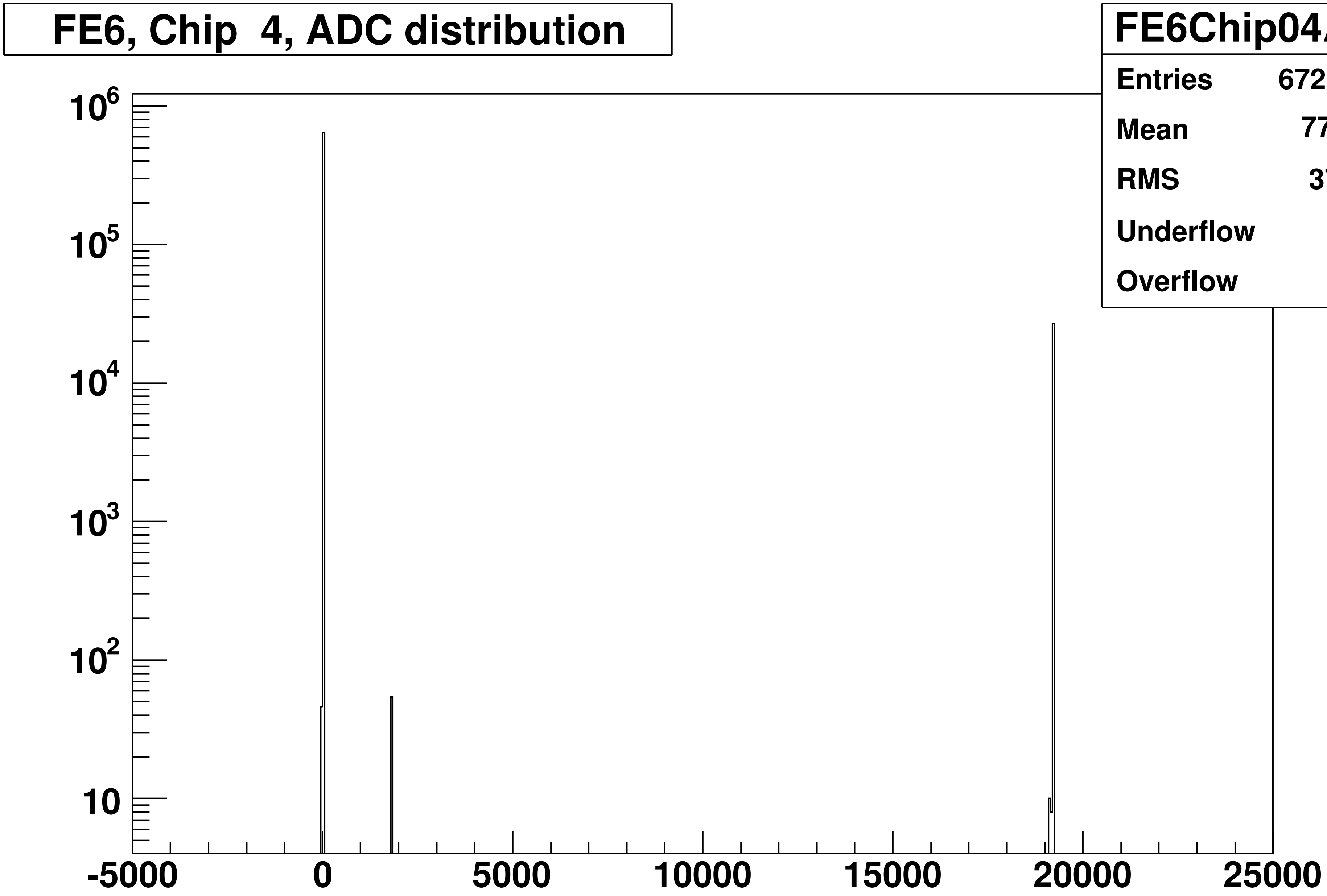
150
200


FE6, Chip 3, ADC distribution
FE6Chip03Sig
Entries 672768
Mean 1.907e+04
RMS 6.039
Underflow 6.452e+05
Overflow 0
10^4
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE6, Chip 4, ADC distribution
FE6Chip04All
Entries 672768
Mean 777.4
RMS 3776
Underflow 0
Overflow 0
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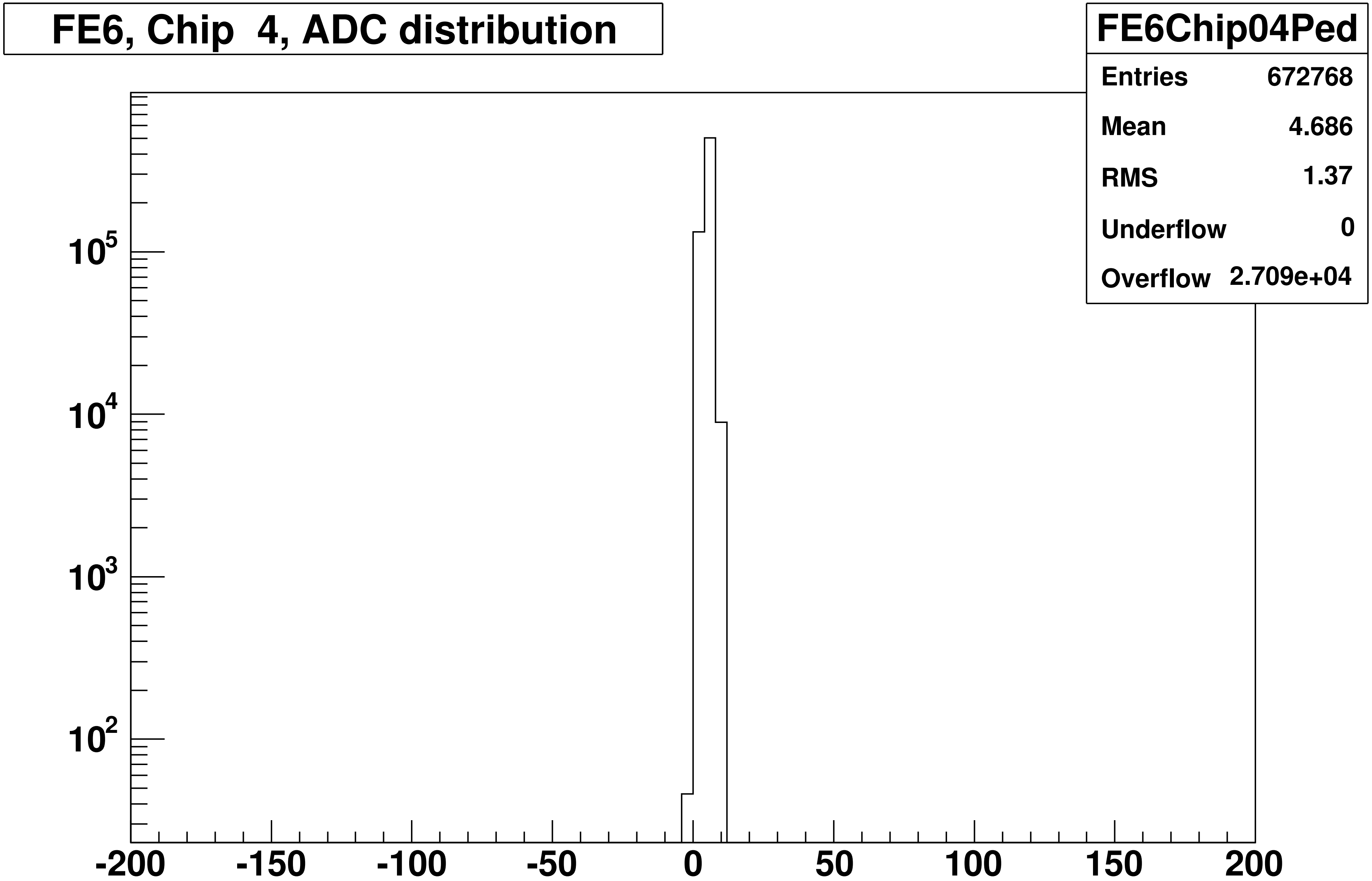
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000



FE6, Chip 4, ADC distribution
FE6Chip04Ped
Entries 672768
Mean 4.686
RMS 1.37
Underflow 0
Overflow 2.709e+04
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10^4
10^3
10^2
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-100
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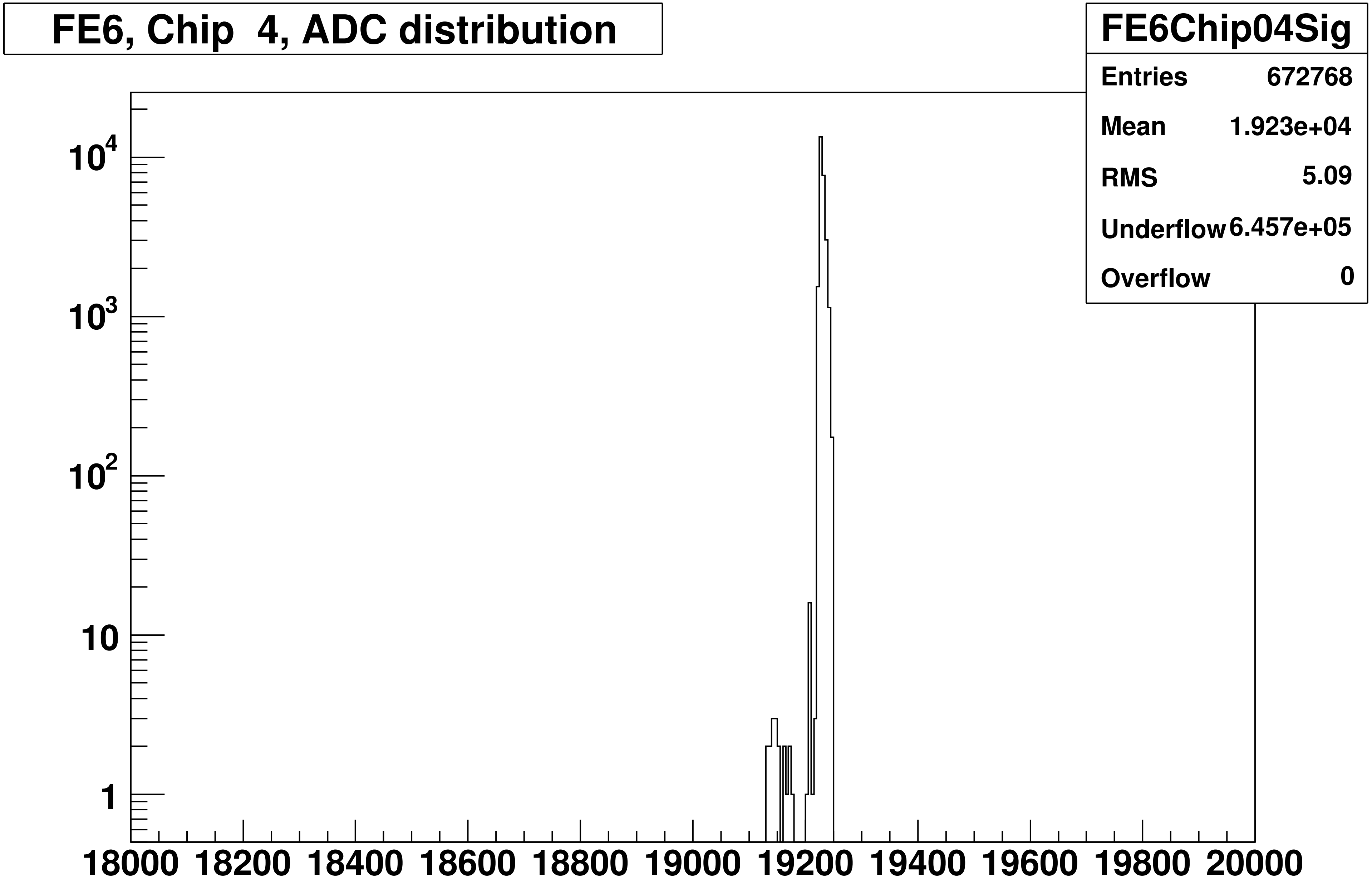
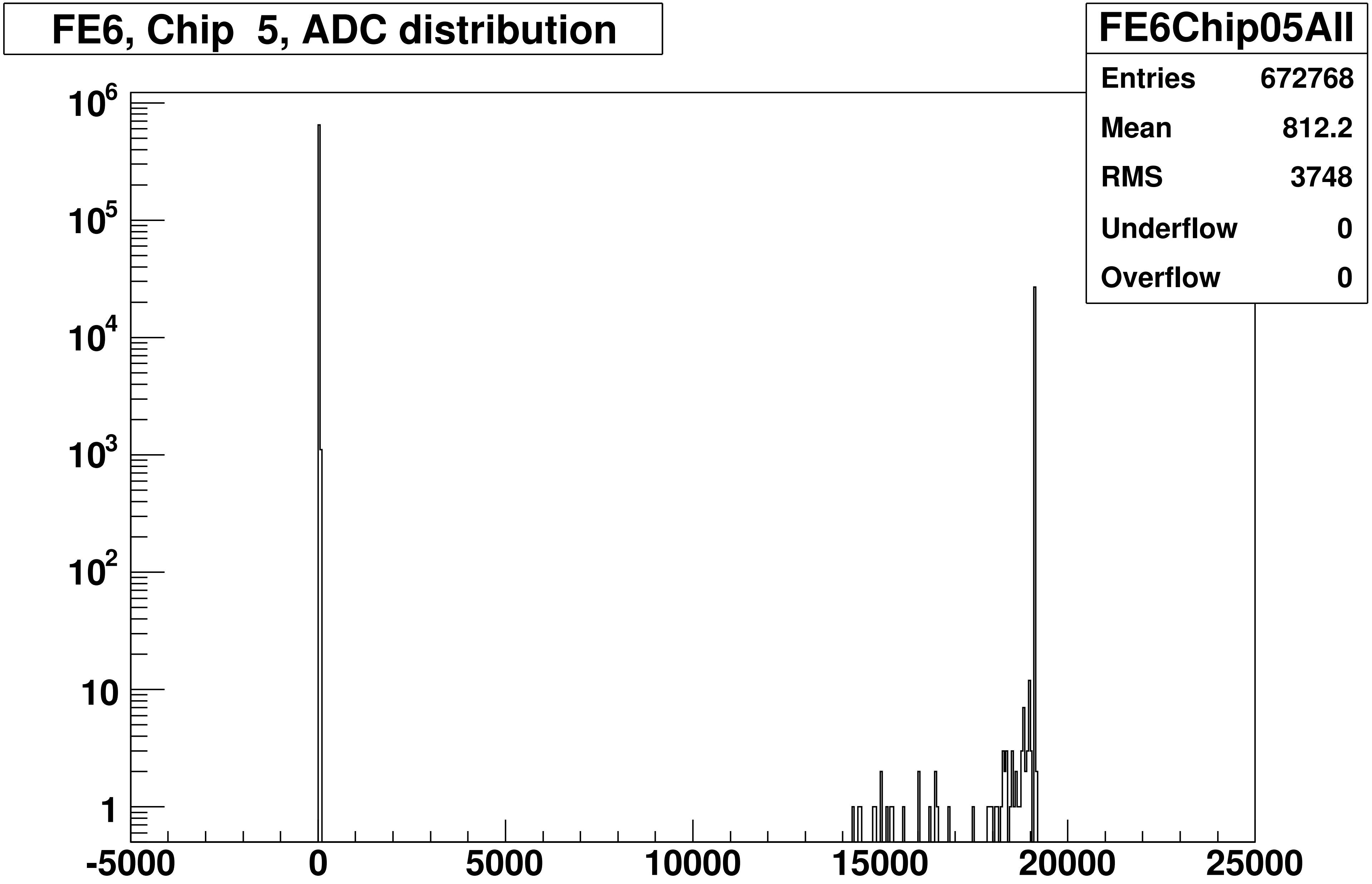
100
150
200



FE6, Chip 4, ADC distribution
FE6Chip04Sig
Entries 672768
Mean 1.923e+04
RMS 5.09
Underflow 6.457e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE6, Chip 5, ADC distribution
FE6Chip05All
Entries 672768
Mean 812.2
RMS 3748
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
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1
-5000
0
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15000
20000
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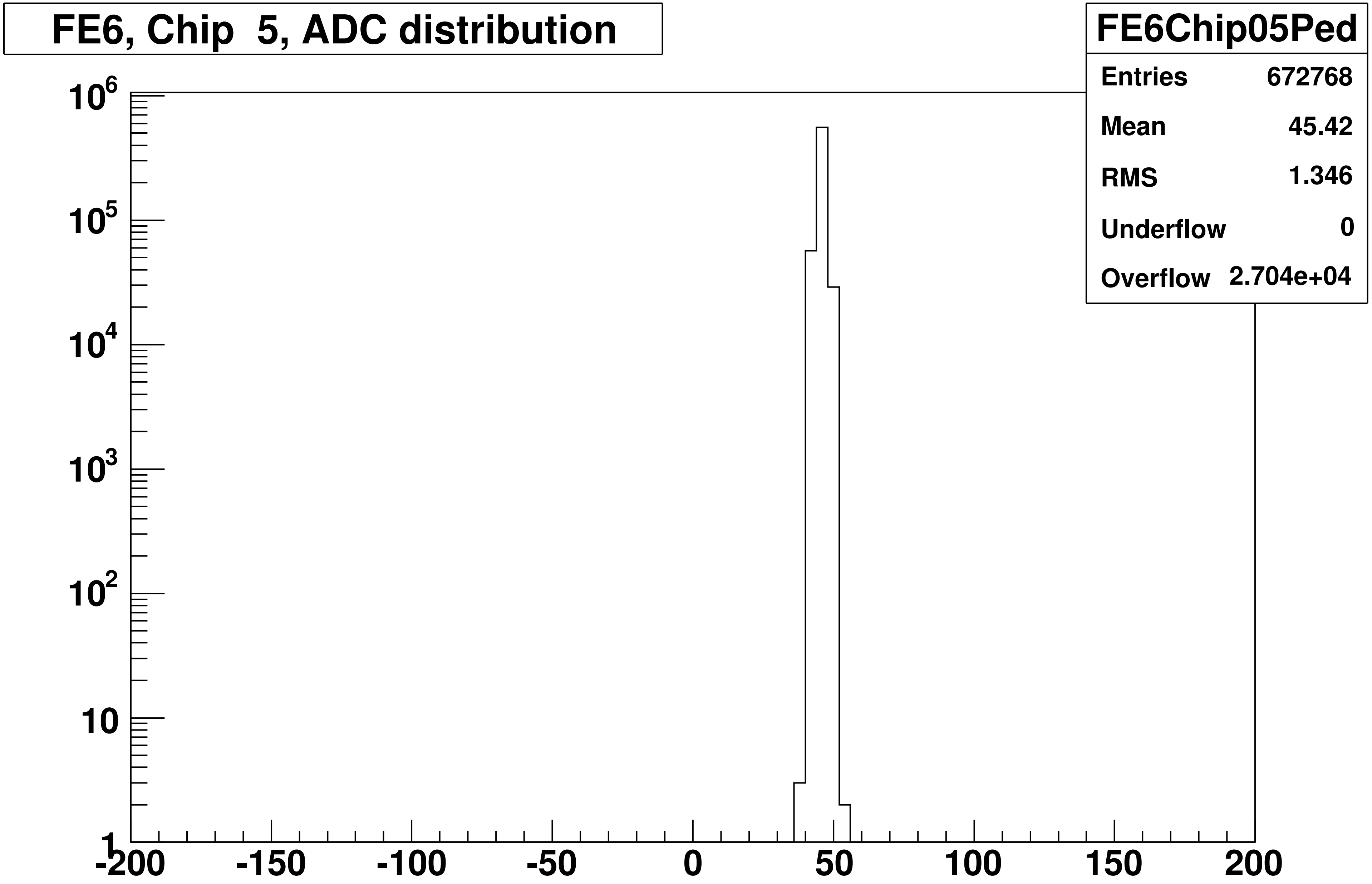

FE6, Chip 5, ADC distribution
FE6Chip05Ped
Entries 672768
Mean 45.42
RMS 1.346
Underflow 0
Overflow 2.704e+04
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10^5
10^4
10^3
10^2
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1
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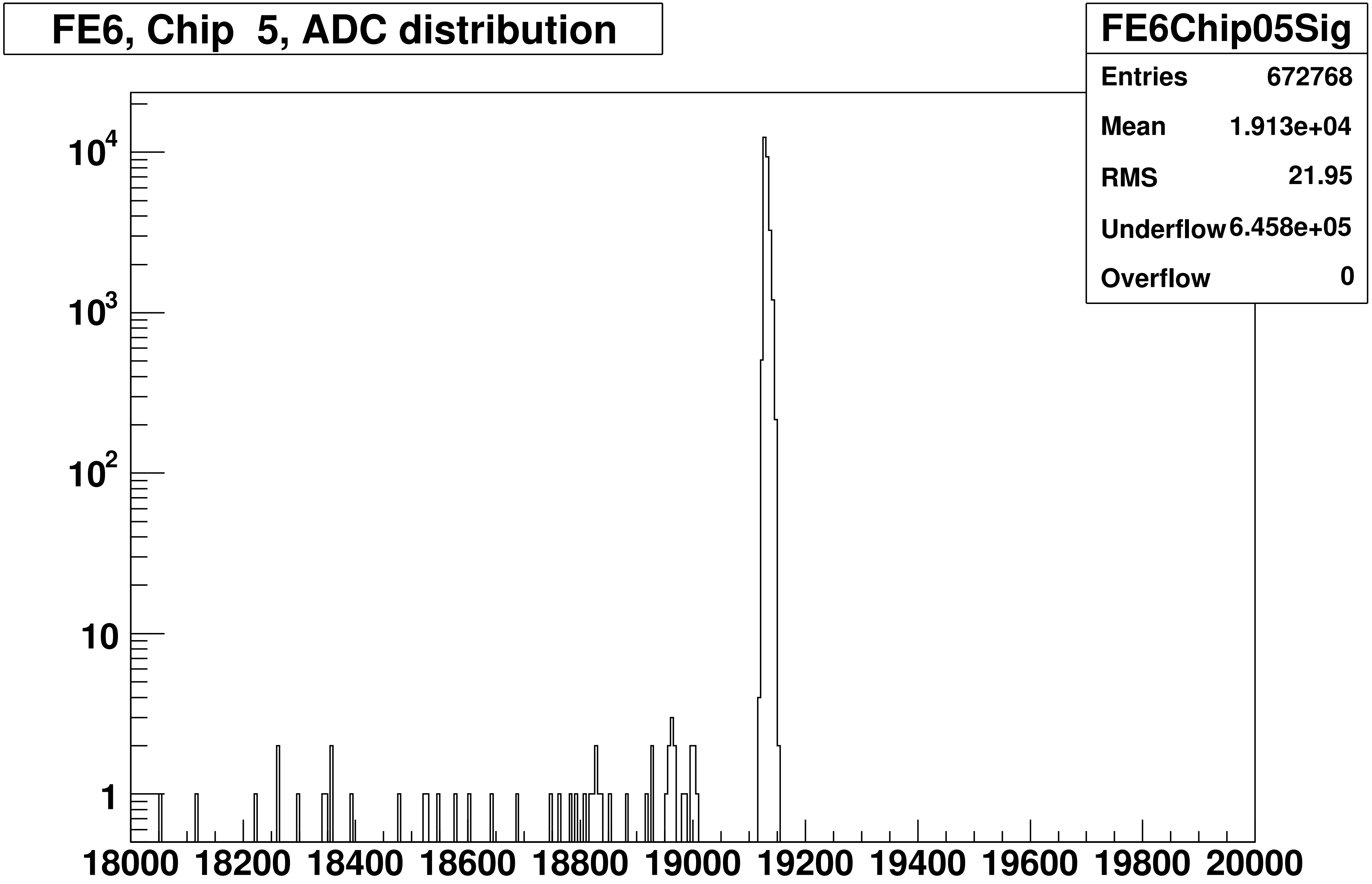
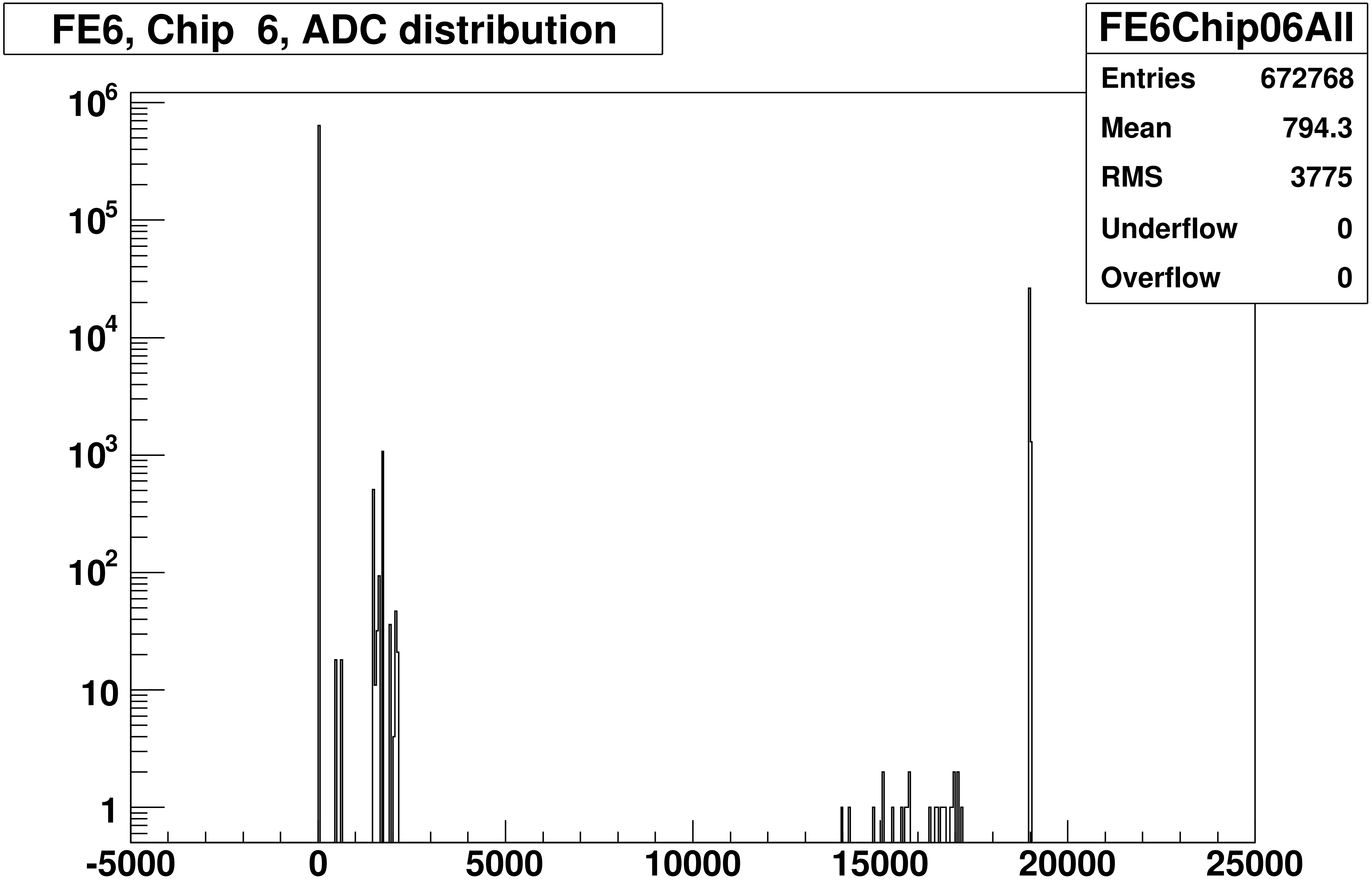
-100
-50
0
50
100
150
200


FE6, Chip 5, ADC distribution
FE6Chip05Sig
Entries 672768
Mean 1.913e+04
RMS 21.95
Underflow 6.458e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE6, Chip 6, ADC distribution
FE6Chip06All
Entries 672768
Mean 794.3
RMS 3775
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
1
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0
5000
10000
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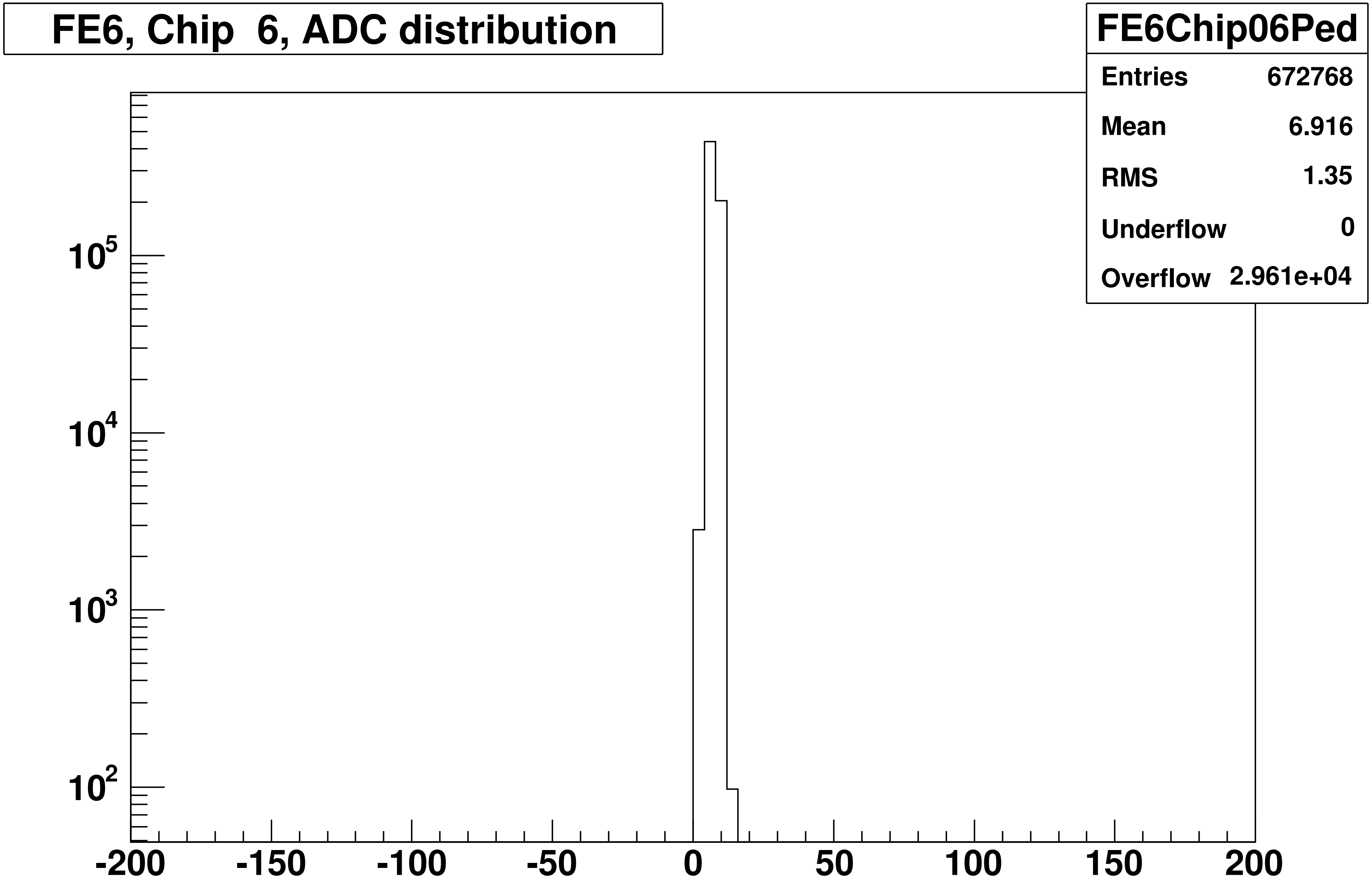
20000
25000


FE6, Chip 6, ADC distribution
FE6Chip06Ped
Entries 672768
Mean 6.916
RMS 1.35
Underflow 0
Overflow 2.961e+04
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10^4
10^3
10^2
-200
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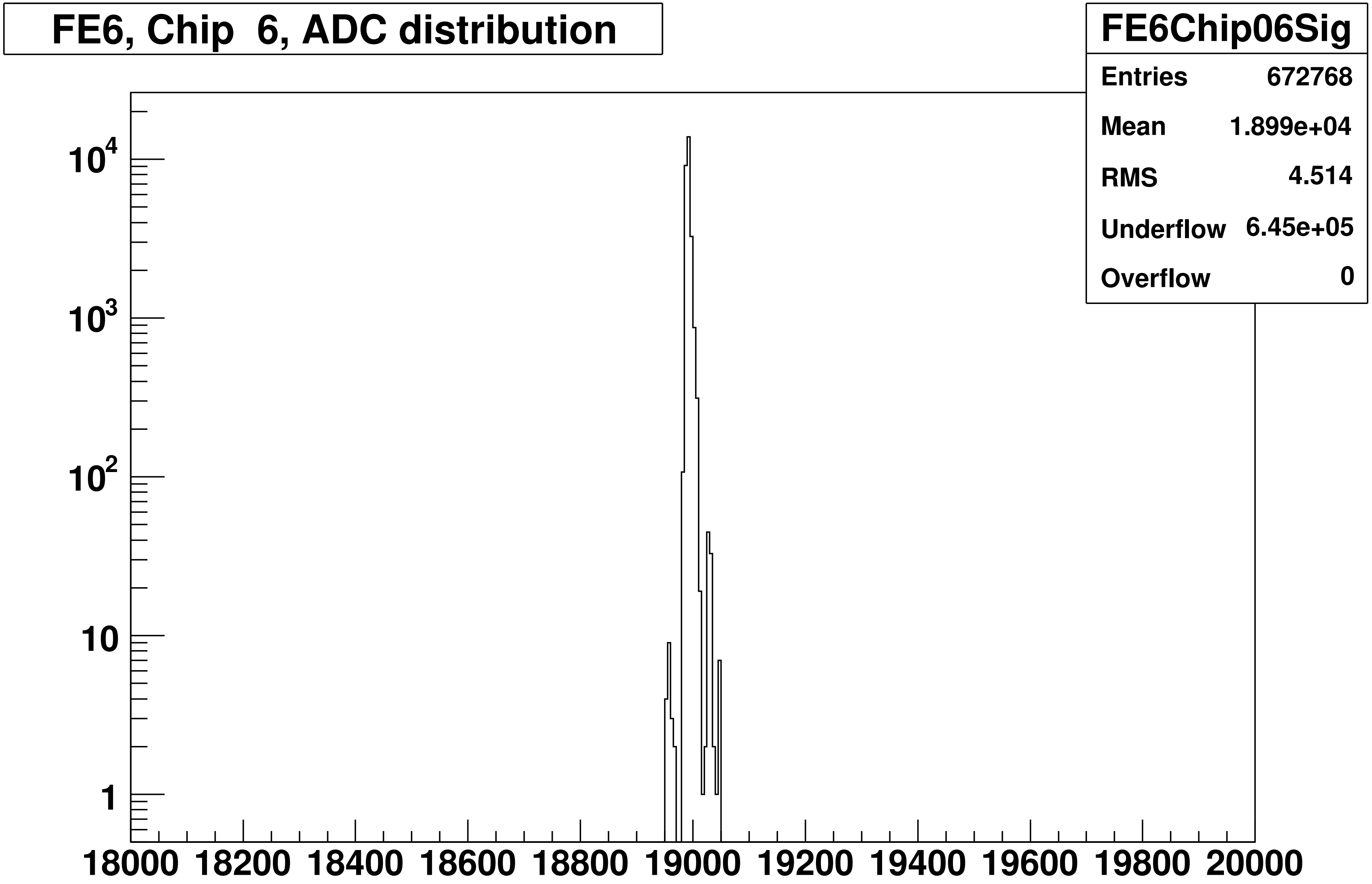
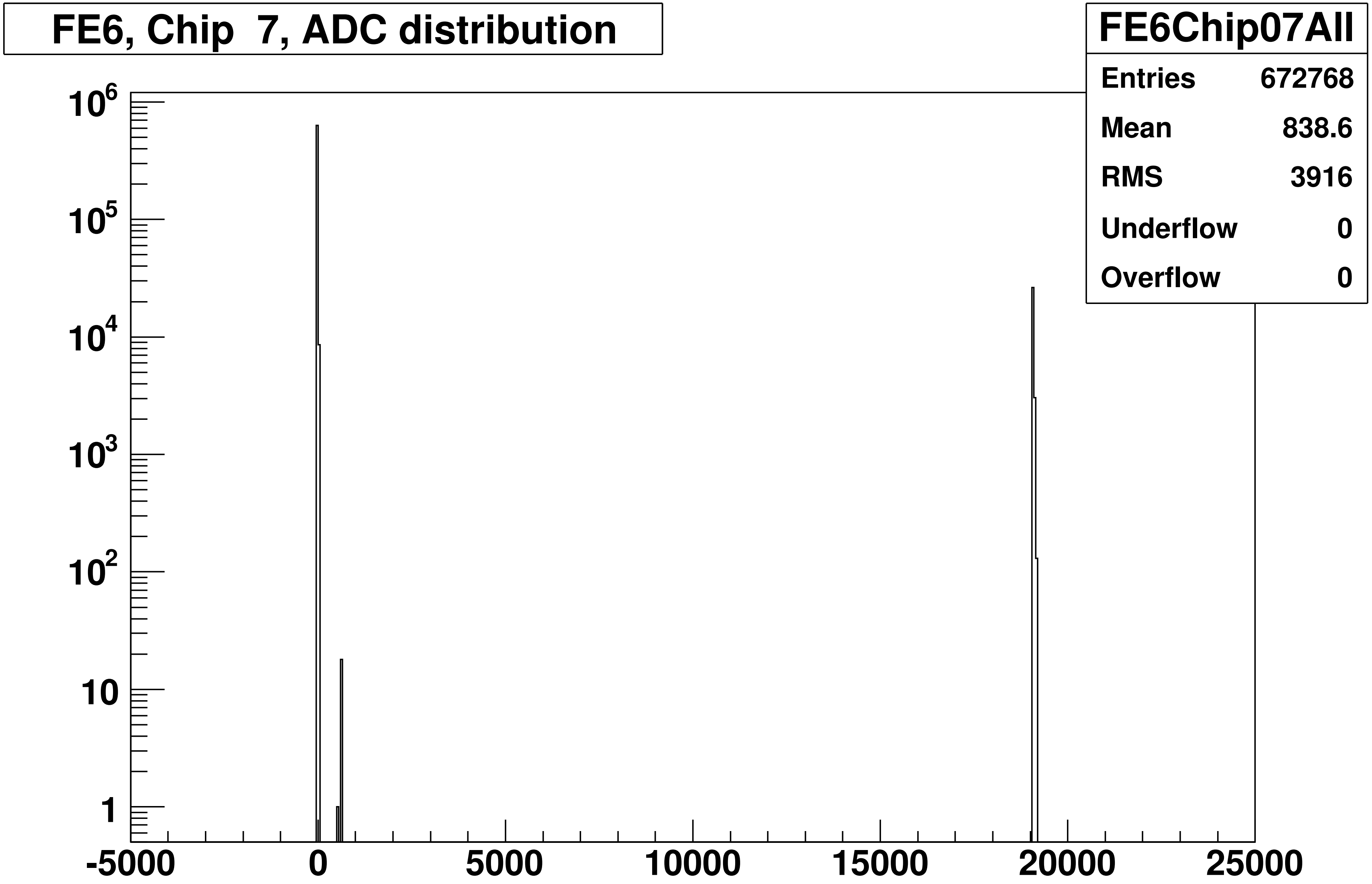
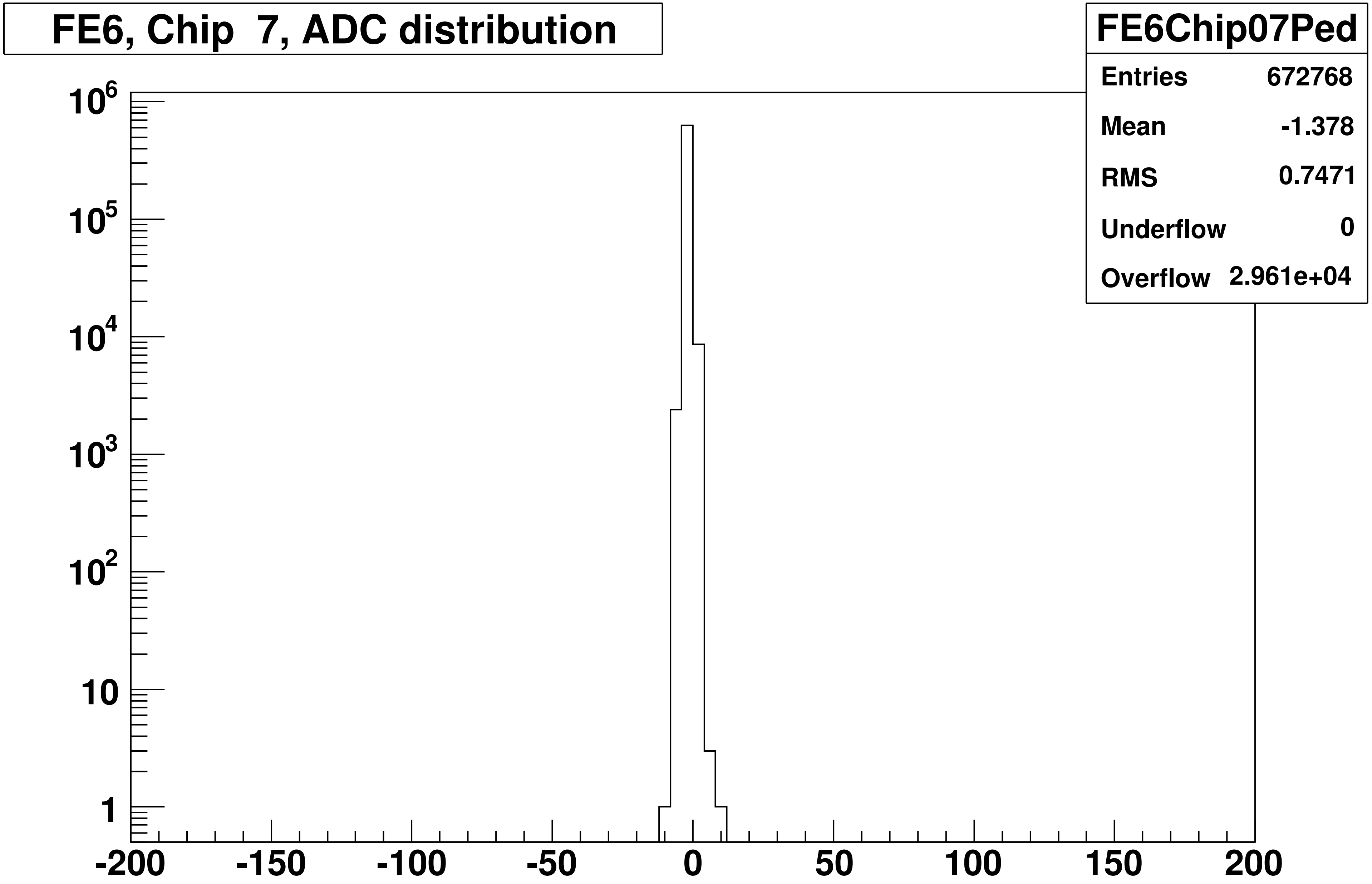
-100
-50
0
50
100
150
200



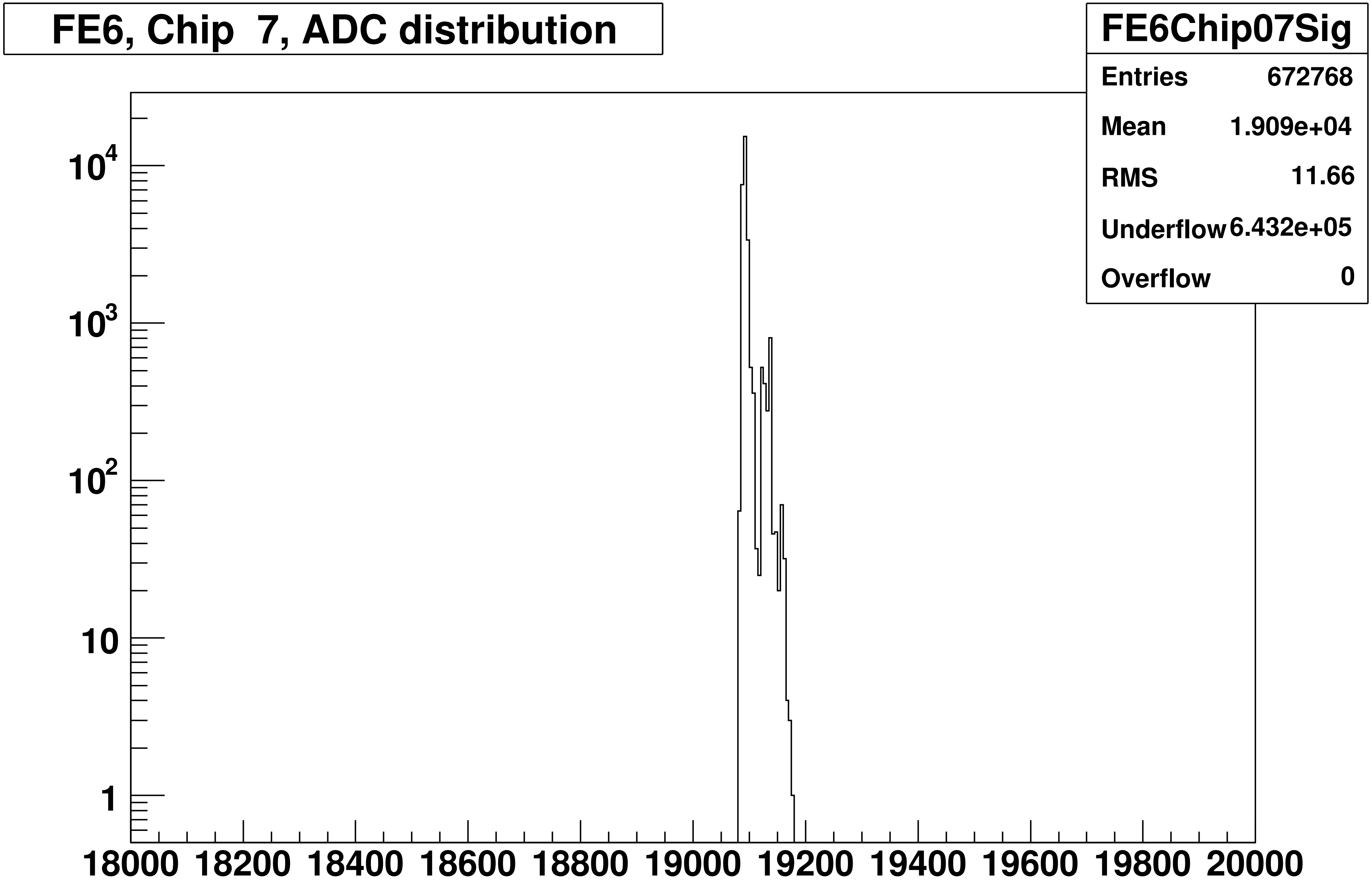
FE6, Chip 6, ADC distribution
FE6Chip06Sig
Entries 672768
Mean 1.899e+04
RMS 4.514
Underflow 6.45e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE6, Chip 7, ADC distribution
FE6Chip07All
Entries 672768
Mean 838.6
RMS 3916
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE6, Chip 7, ADC distribution
FE6Chip07Ped
Entries 672768
Mean -1.378
RMS 0.7471
Underflow 0
Overflow 2.961e+04
10^6
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
200



FE6, Chip 7, ADC distribution
FE6Chip07Sig
Entries 672768
Mean 1.909e+04
RMS 11.66
Underflow 6.432e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
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19800
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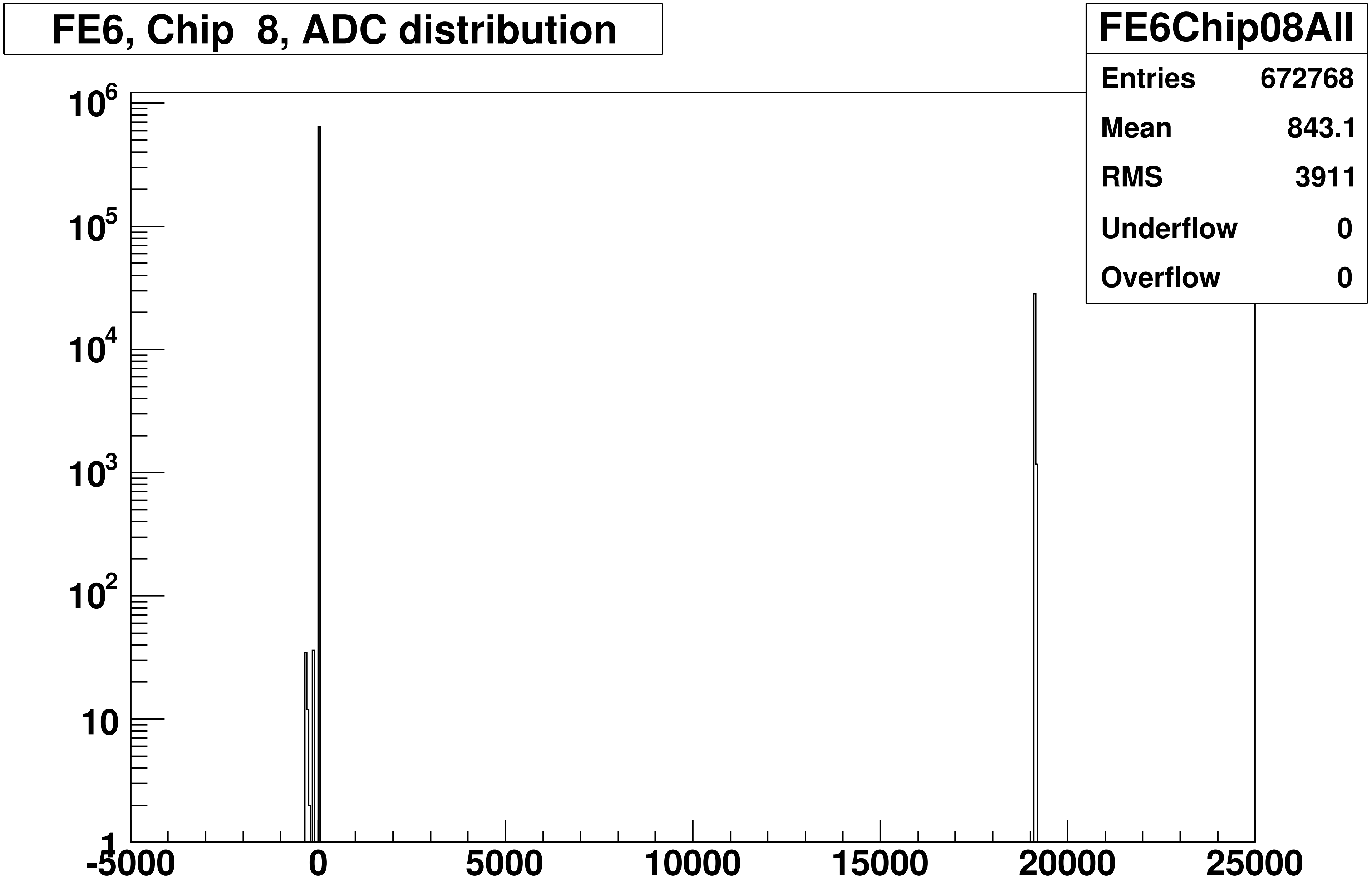
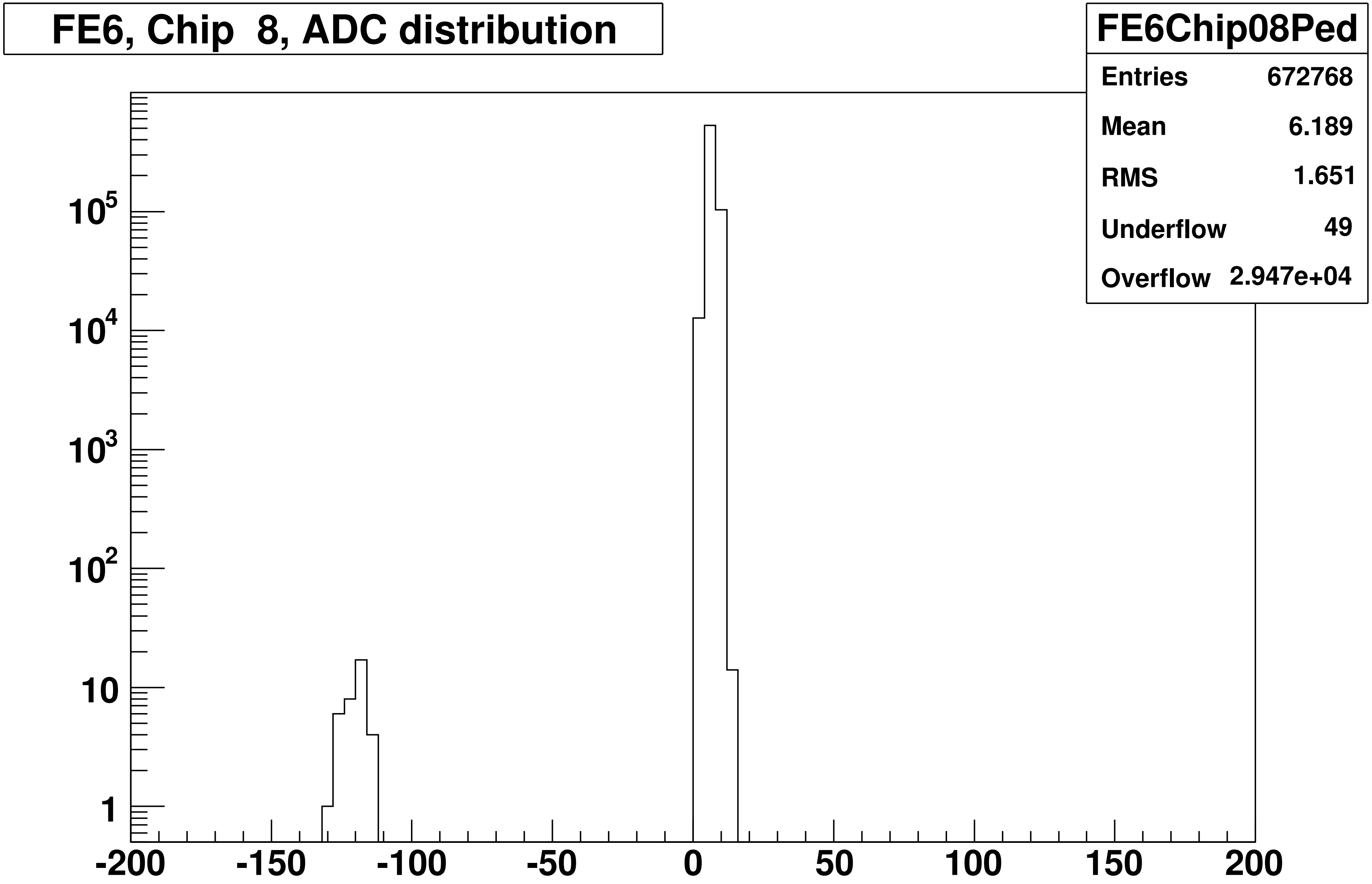

FE6, Chip 8, ADC distribution
FE6Chip08All
Entries 672768
Mean 843.1
RMS 3911
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE6, Chip 8, ADC distribution
FE6Chip08Ped
Entries 672768
Mean 6.189
RMS 1.651
Underflow 49
Overflow 2.947e+04
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10^4
10^3
10^2
10
1
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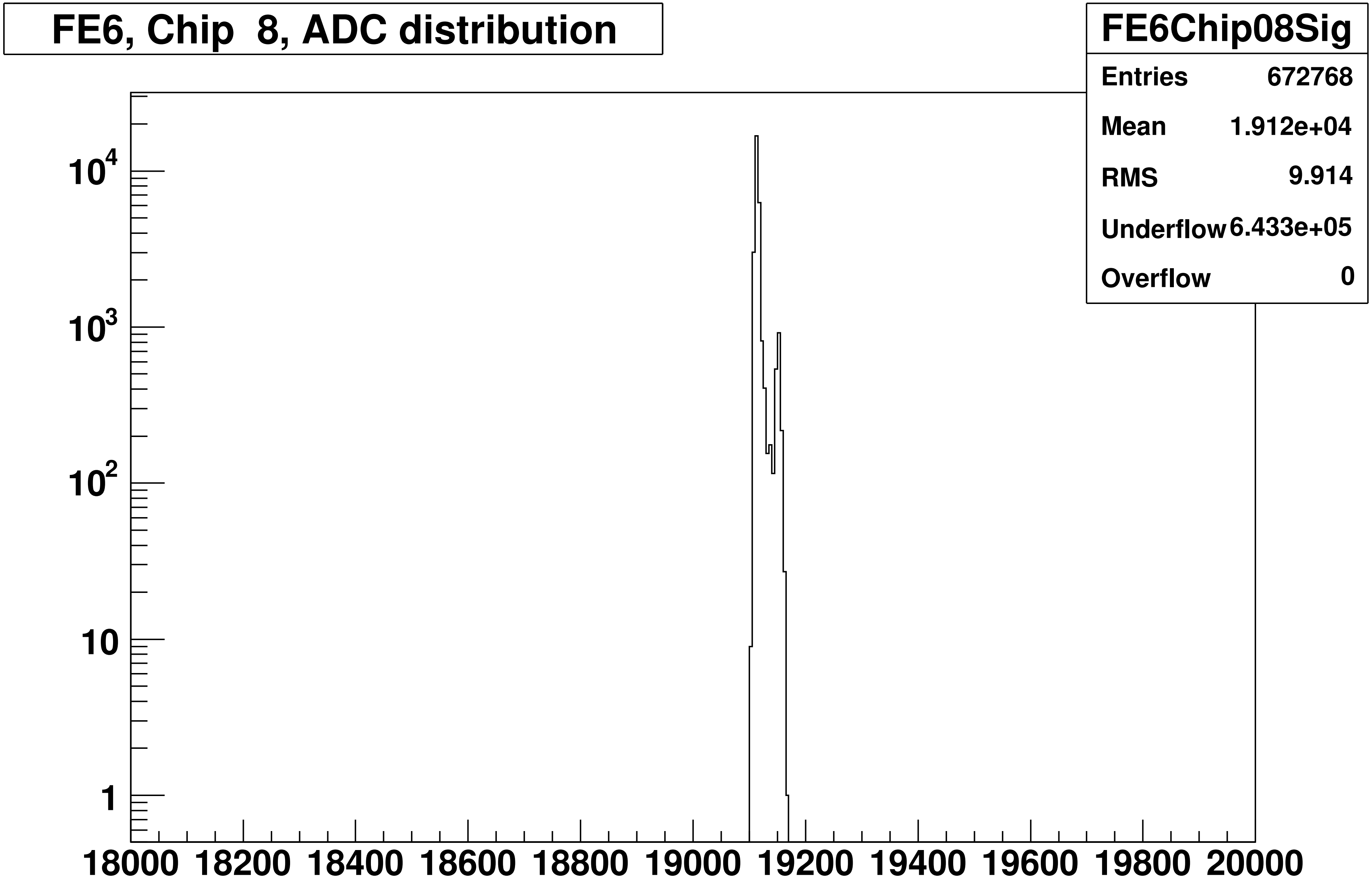
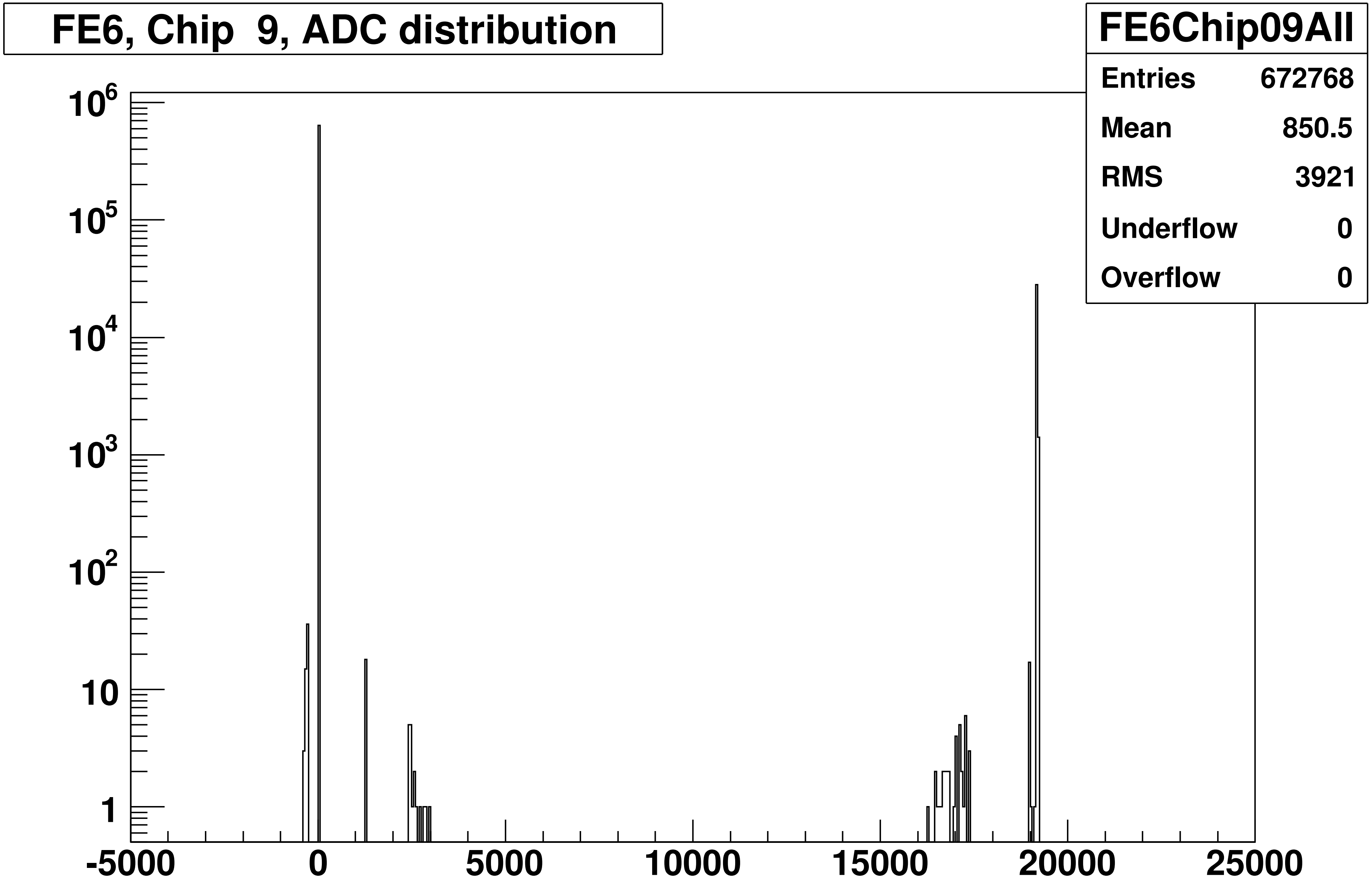
100
150
200



FE6, Chip 8, ADC distribution
FE6Chip08Sig
Entries 672768
Mean 1.912e+04
RMS 9.914
Underflow 6.433e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE6, Chip 9, ADC distribution
FE6Chip09All
Entries 672768
Mean 850.5
RMS 3921
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
1
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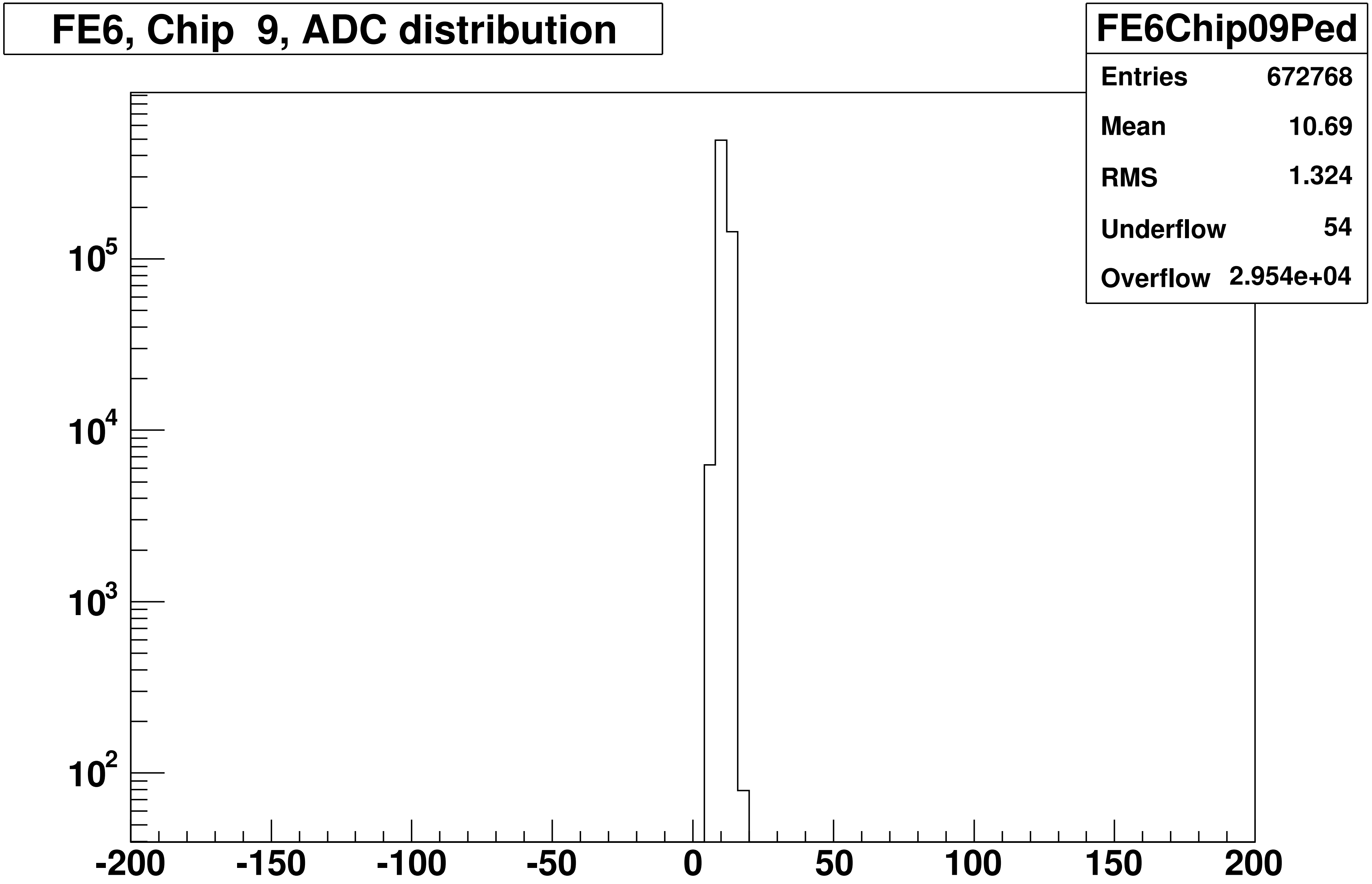
FE6, Chip 9, ADC distribution
FE6Chip09Ped
Entries 672768
Mean 10.69
RMS 1.324
Underflow 54
Overflow 2.954e+04
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10^4
10^3
10^2
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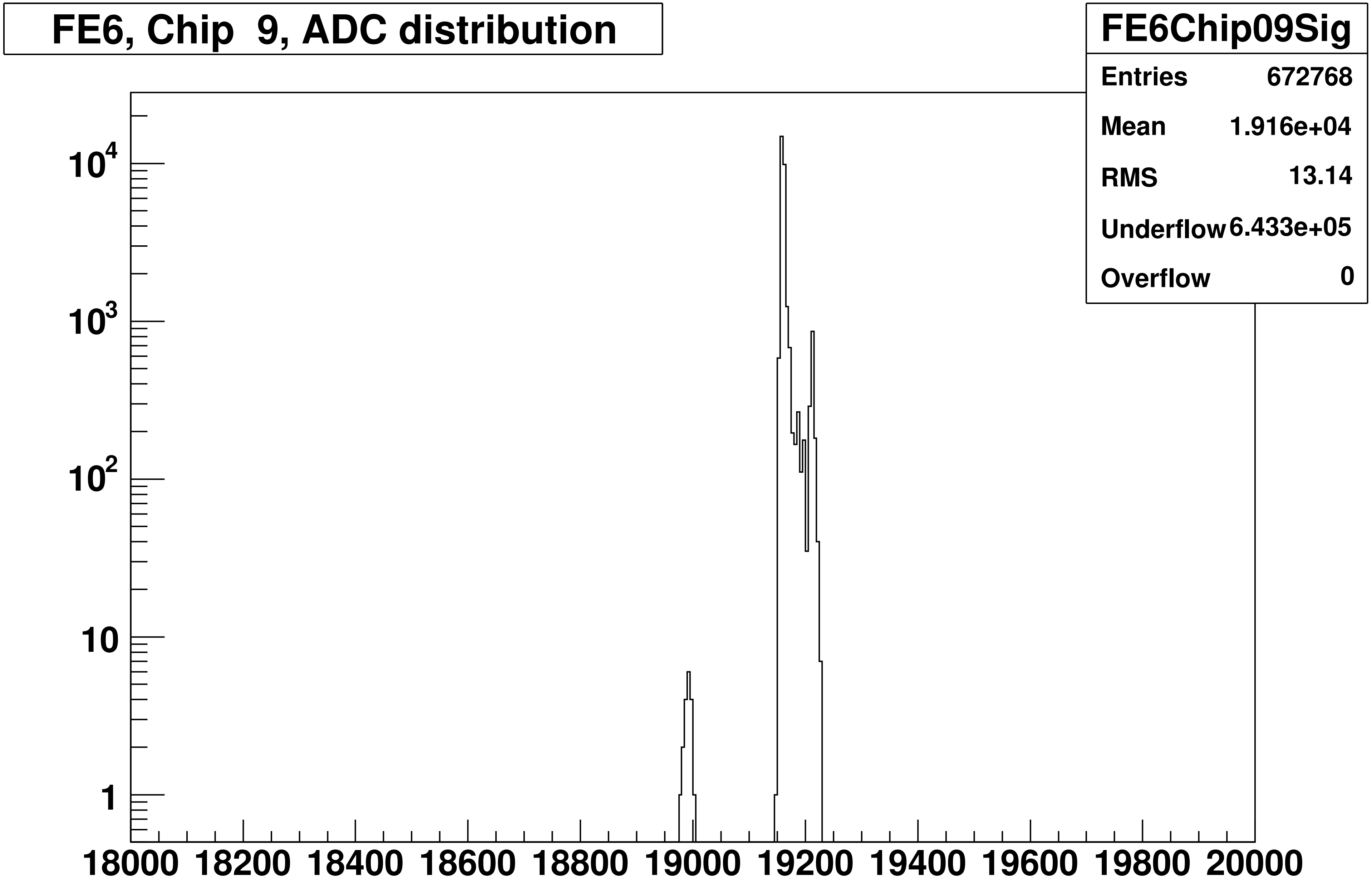
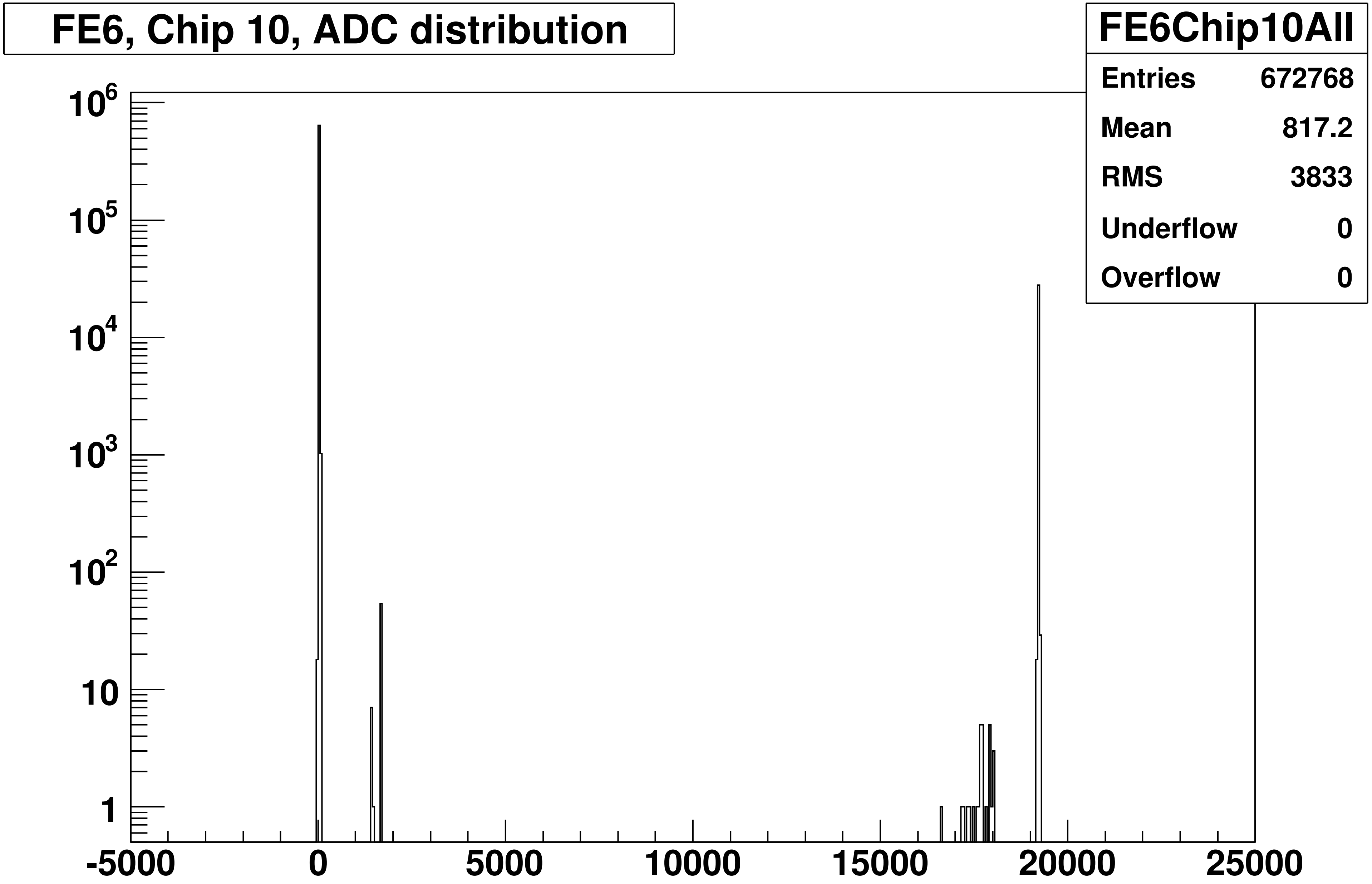
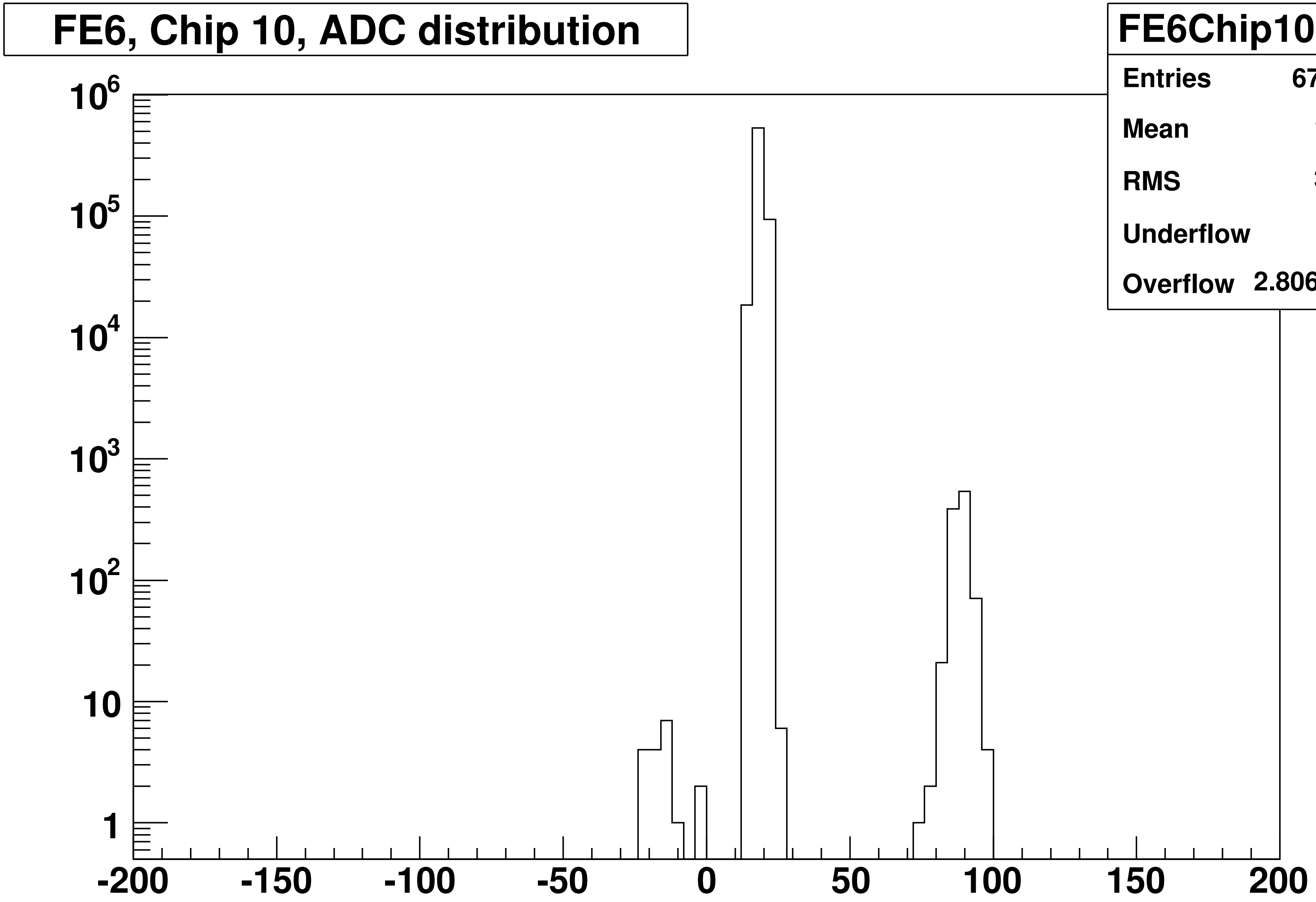
150
200


FE6, Chip 9, ADC distribution
FE6Chip09Sig
Entries 672768
Mean 1.916e+04
RMS 13.14
Underflow 6.433e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE6, Chip 10, ADC distribution
FE6Chip10All
Entries 672768
Mean 817.2
RMS 3833
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE6, Chip 10, ADC distribution
FE6Chip10Ped
Entries 672768
Mean 18.24
RMS 3.108
Underflow 0
Overflow 2.806e+04
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10^5
10^4
10^3
10^2
10
1
-200
-150
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0
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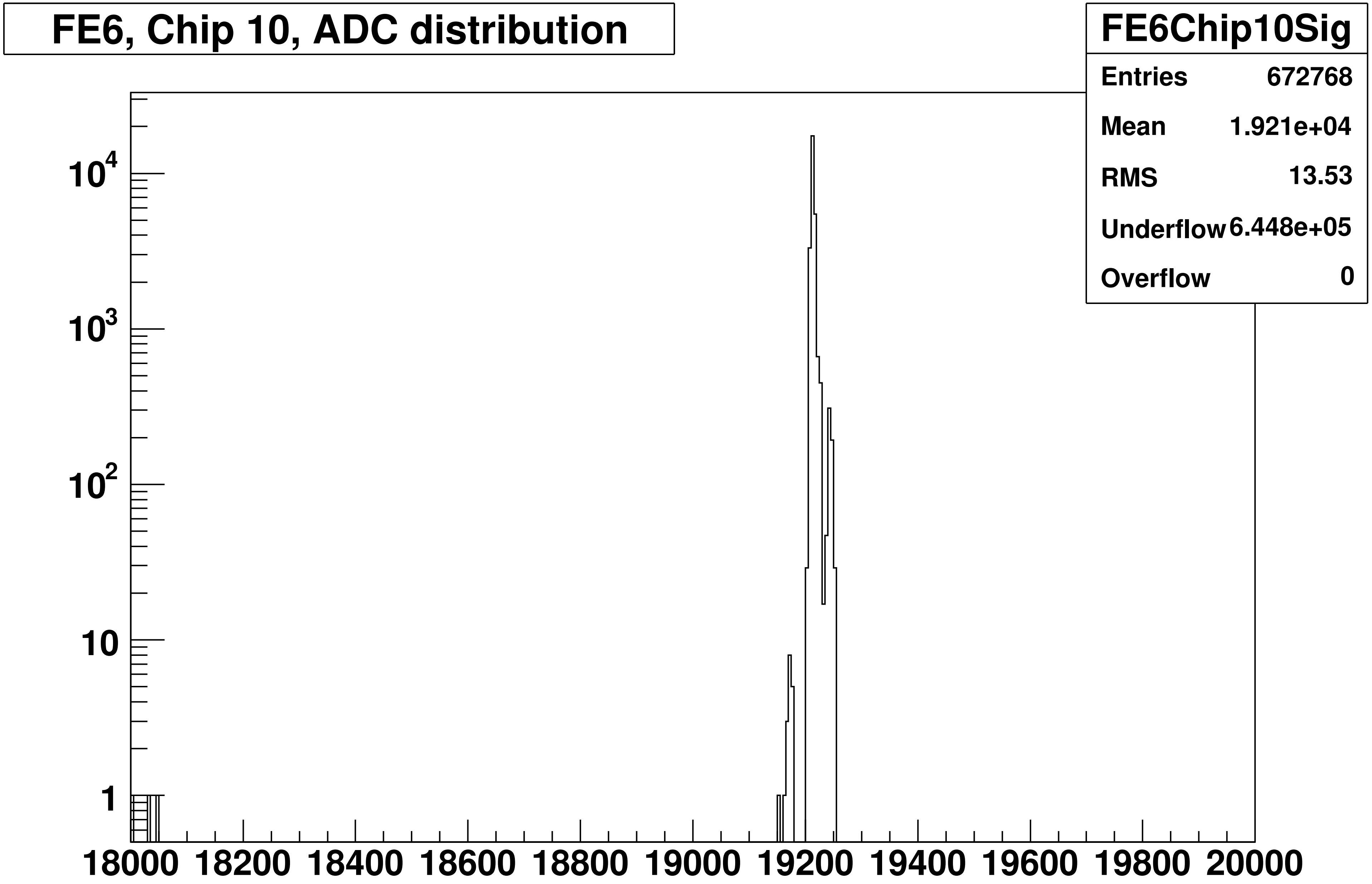
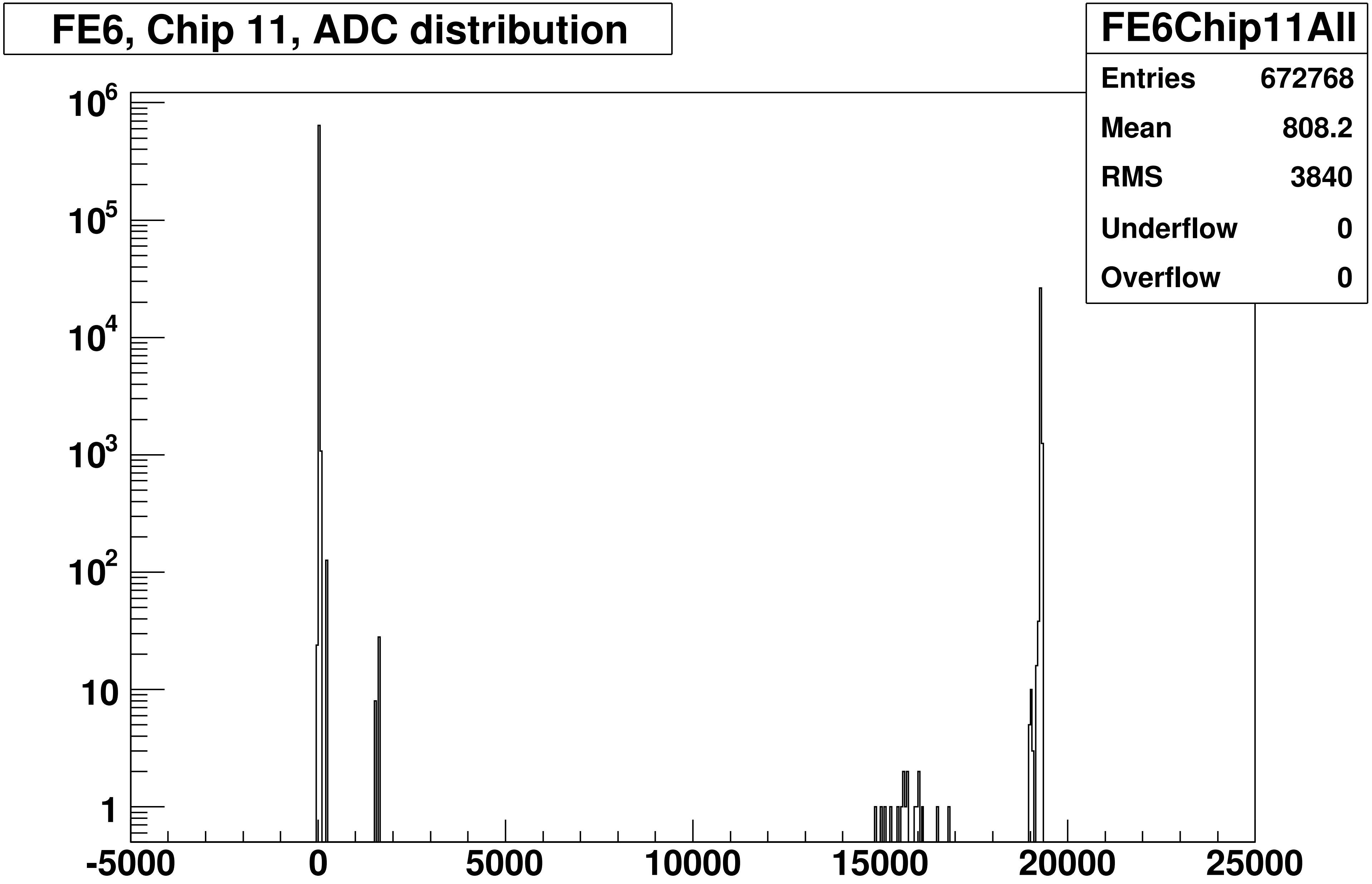
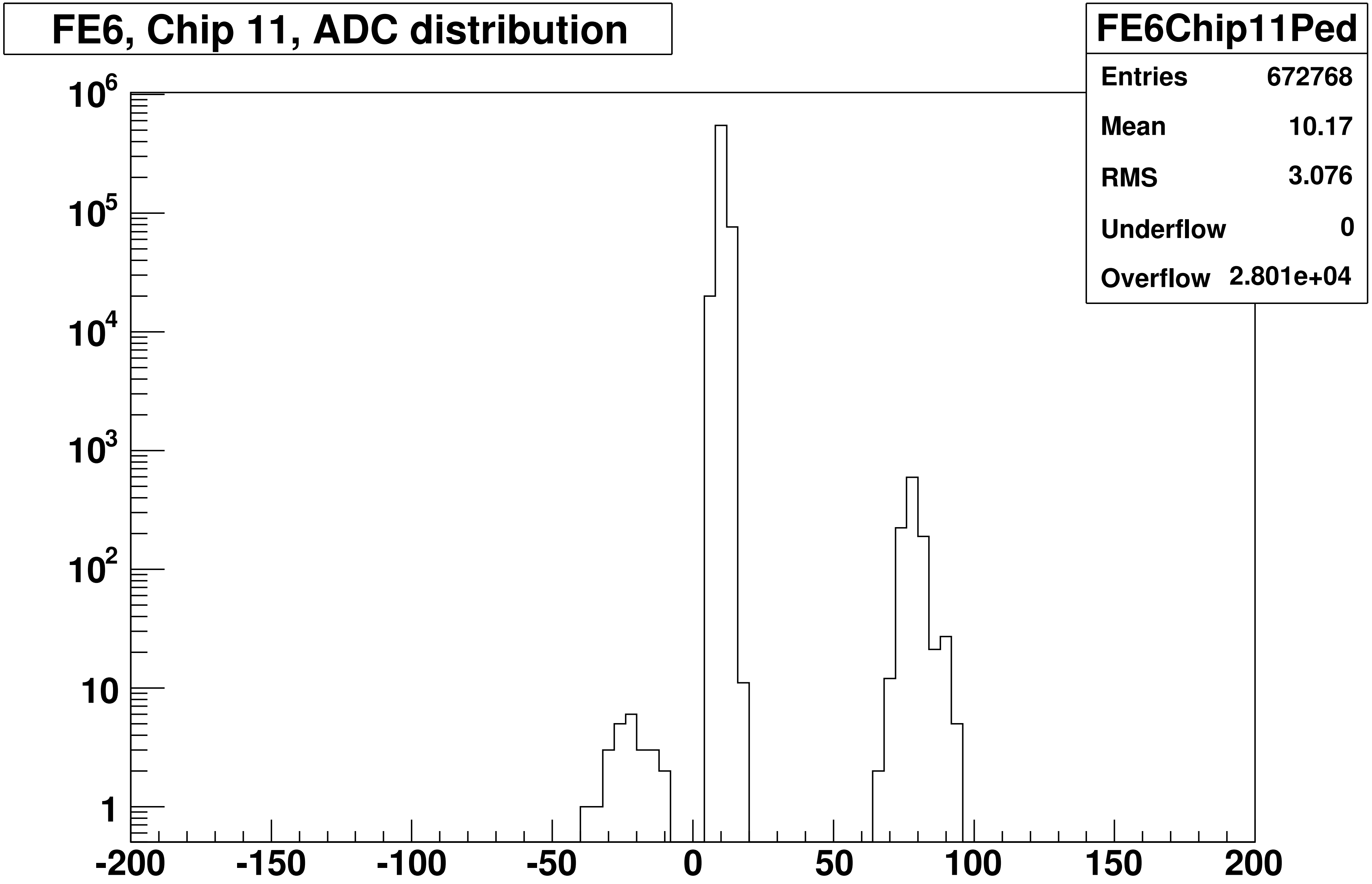
100
150
200



FE6, Chip 10, ADC distribution
FE6Chip10Sig
Entries 672768
Mean 1.921e+04
RMS 13.53
Underflow 6.448e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000



FE6, Chip 11, ADC distribution
FE6Chip11All
Entries 672768
Mean 808.2
RMS 3840
Underflow 0
Overflow 0


FE6, Chip 11, ADC distribution
FE6Chip11Ped
Entries 672768
Mean 10.17
RMS 3.076
Underflow 0
Overflow 2.801e+04
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10^5
10^4
10^3
10^2
10
1
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-100
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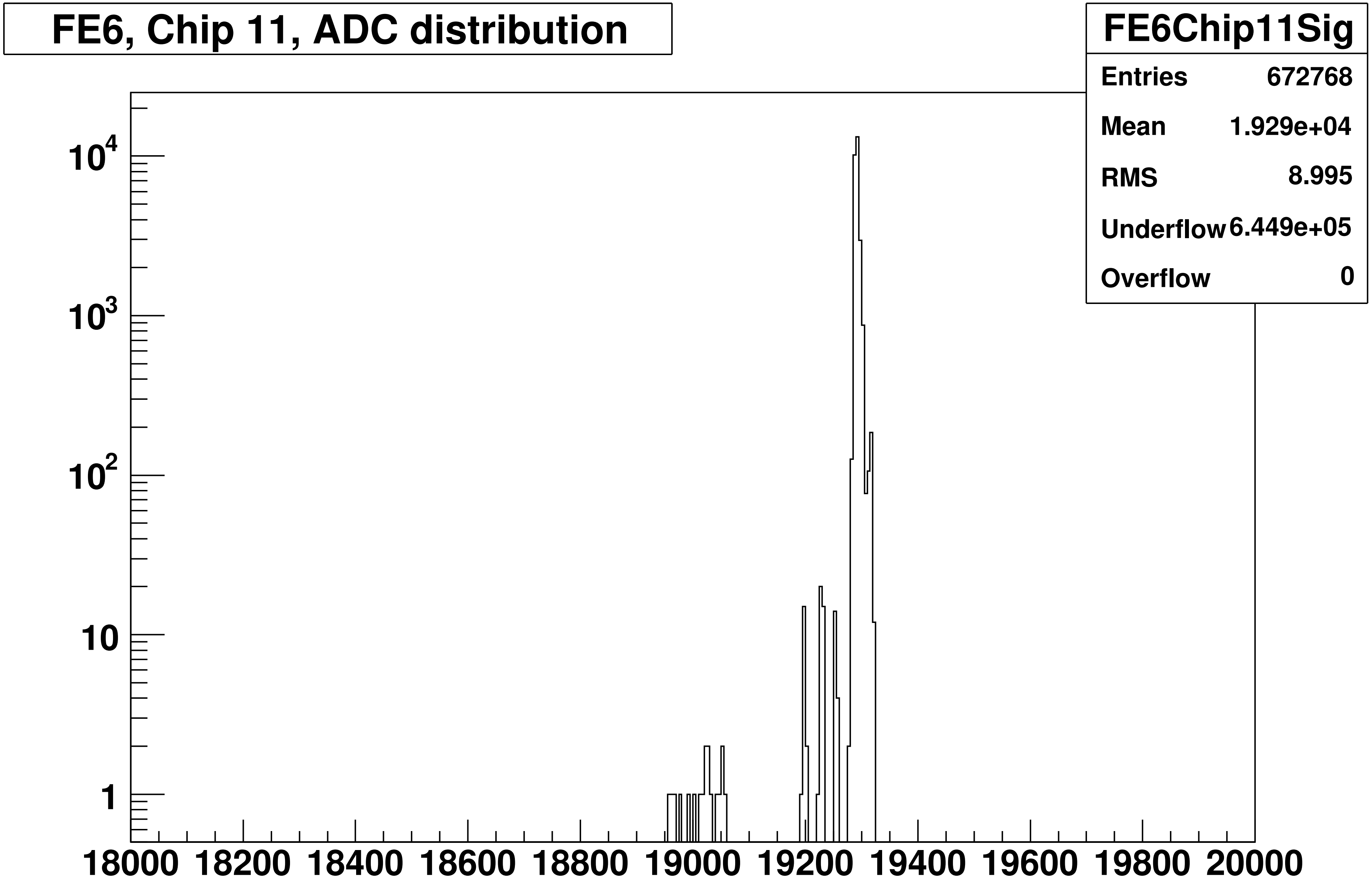
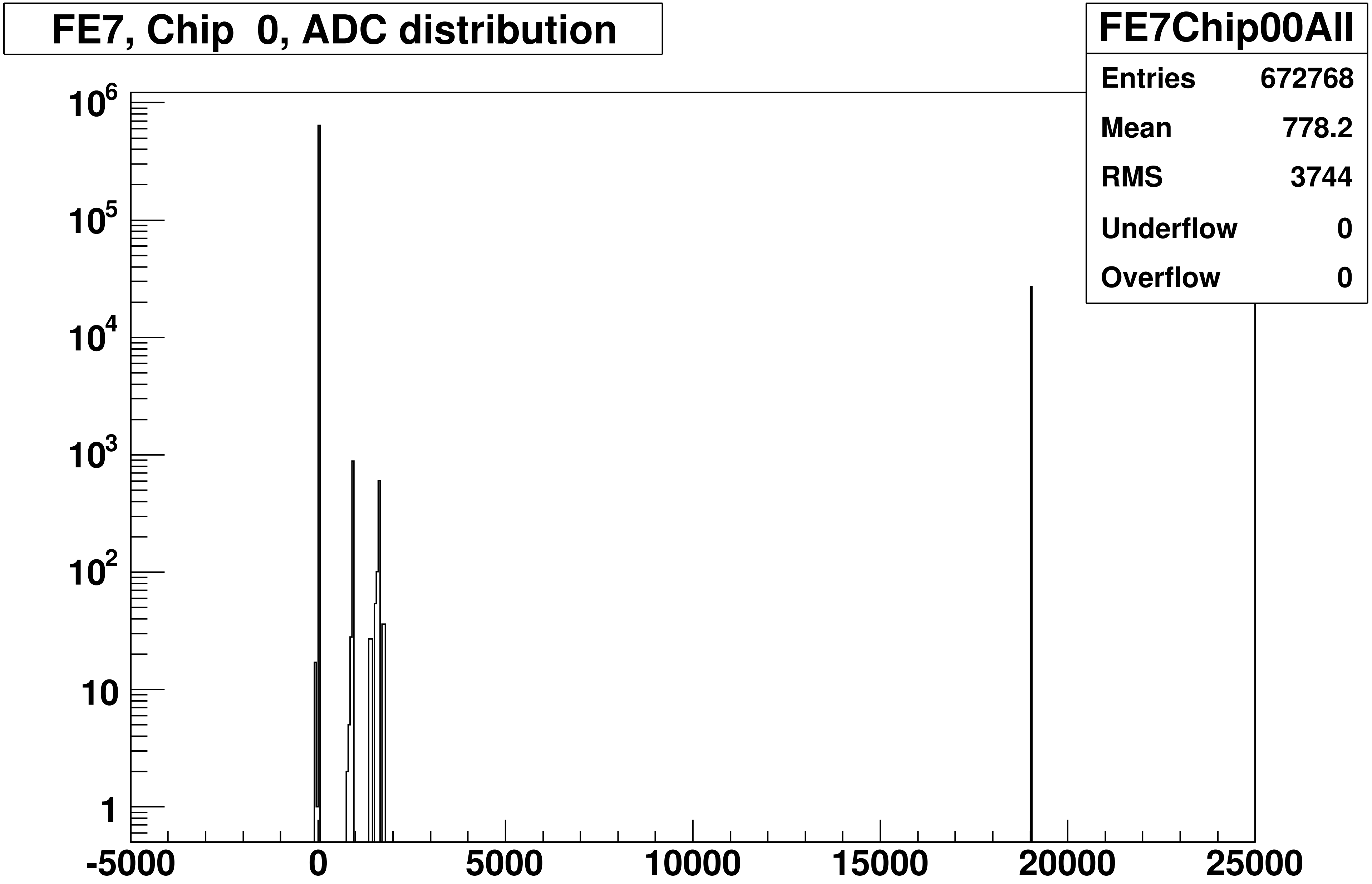
0
50
100
150
200



FE6, Chip 11, ADC distribution
FE6Chip11Sig
Entries 672768
Mean 1.929e+04
RMS 8.995
Underflow 6.449e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000



FE7, Chip 0, ADC distribution
FE7Chip00All
Entries 672768
Mean 778.2
RMS 3744
Underflow 0
Overflow 0
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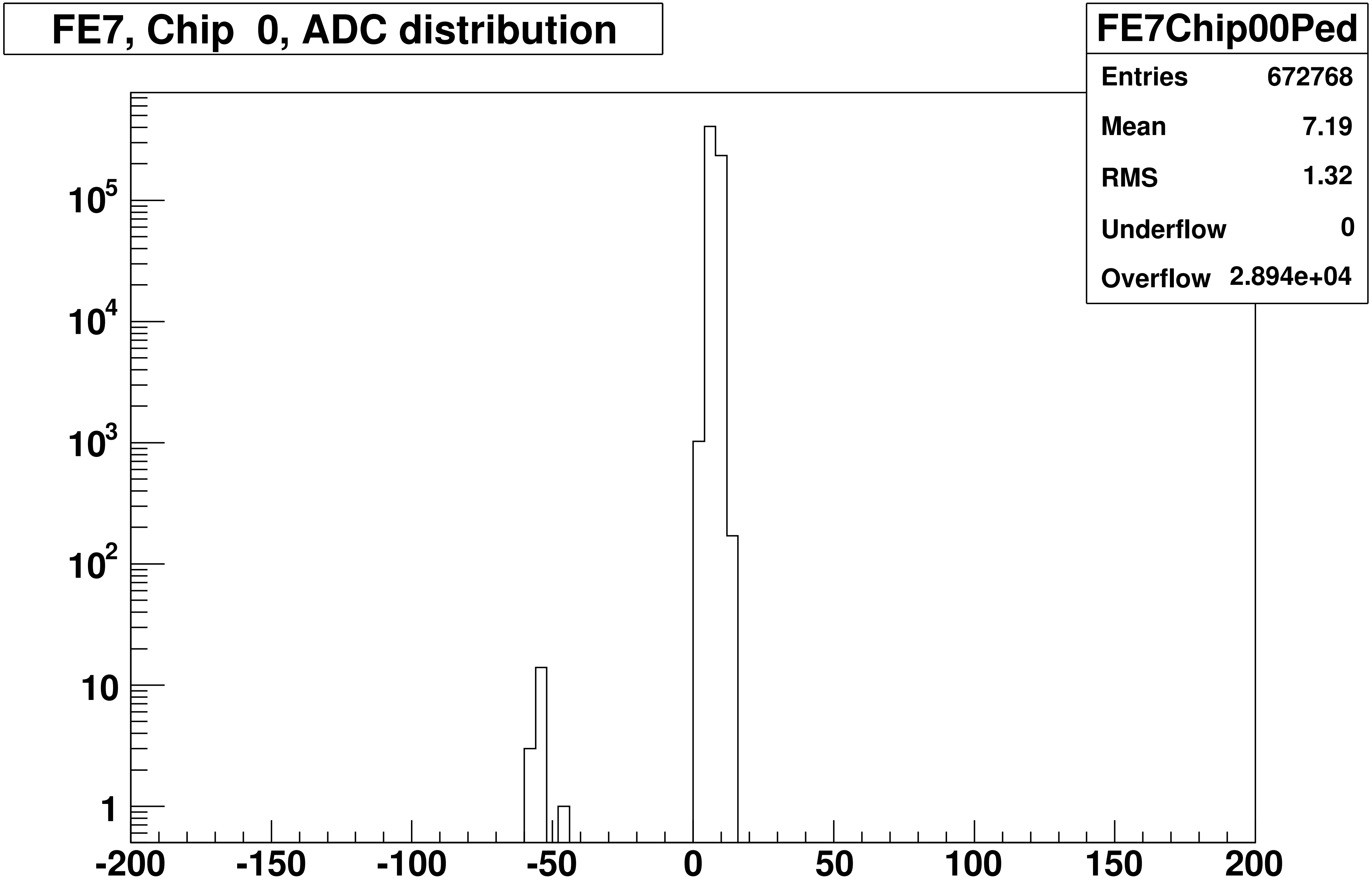
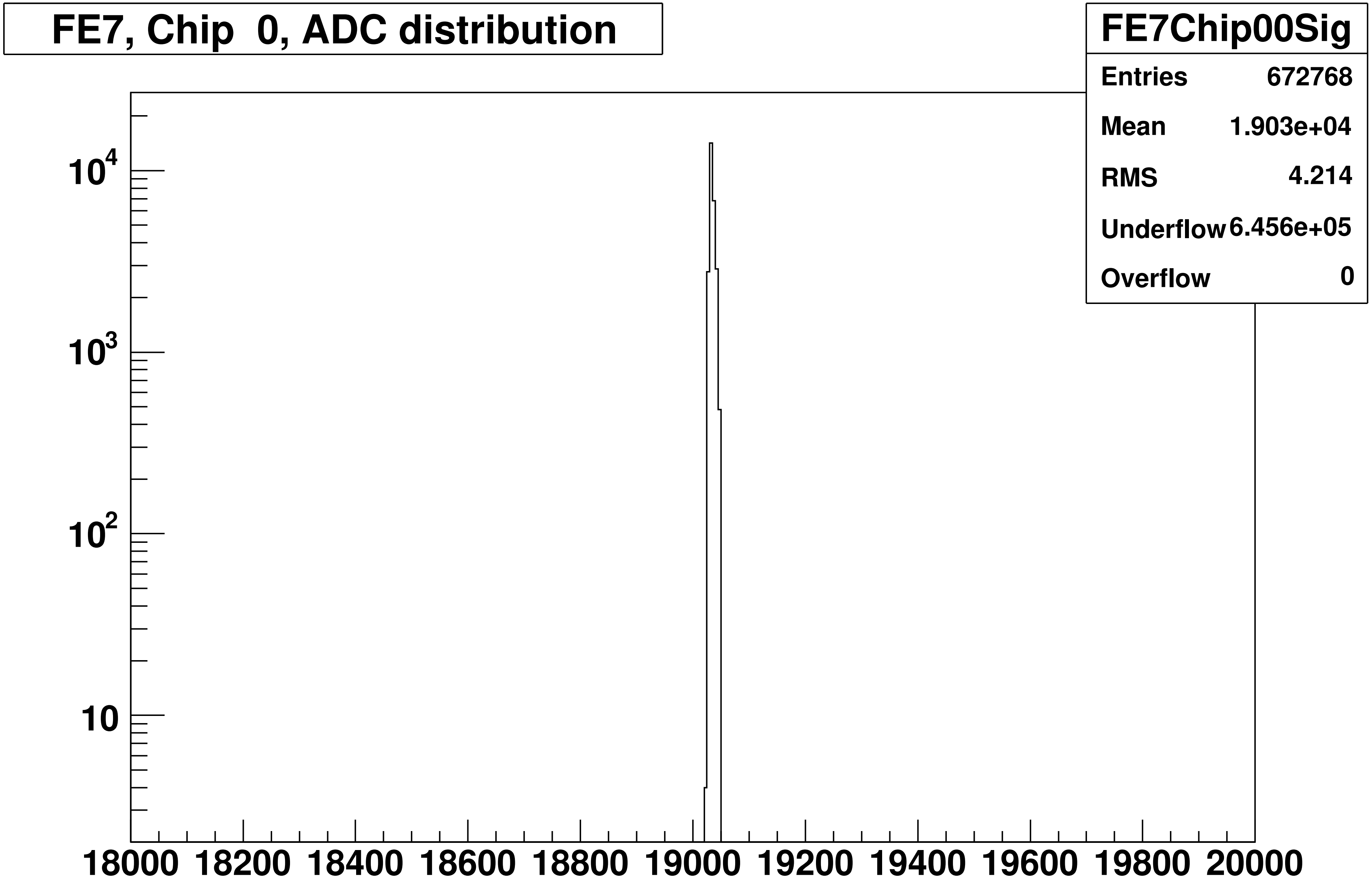
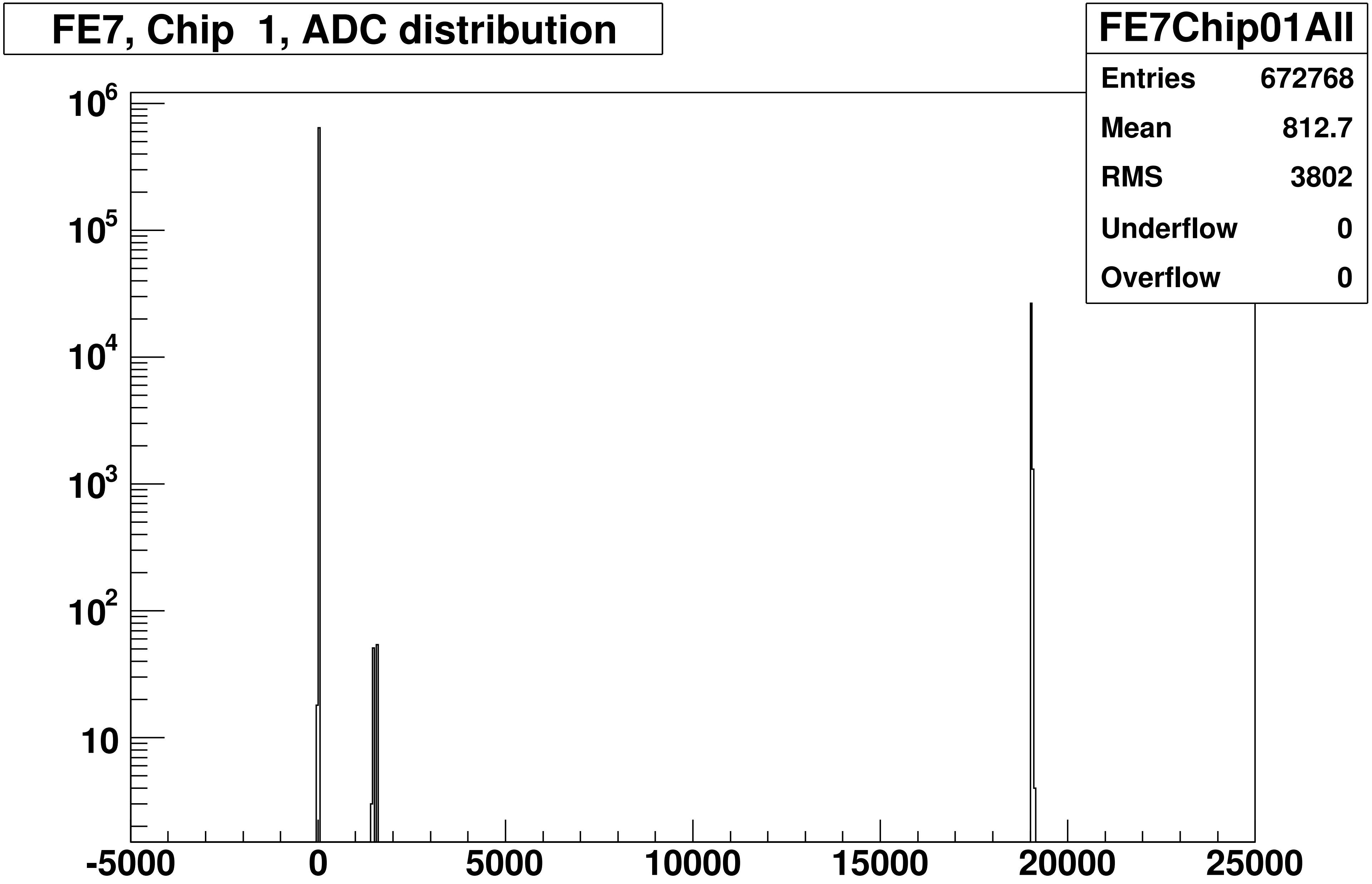
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000

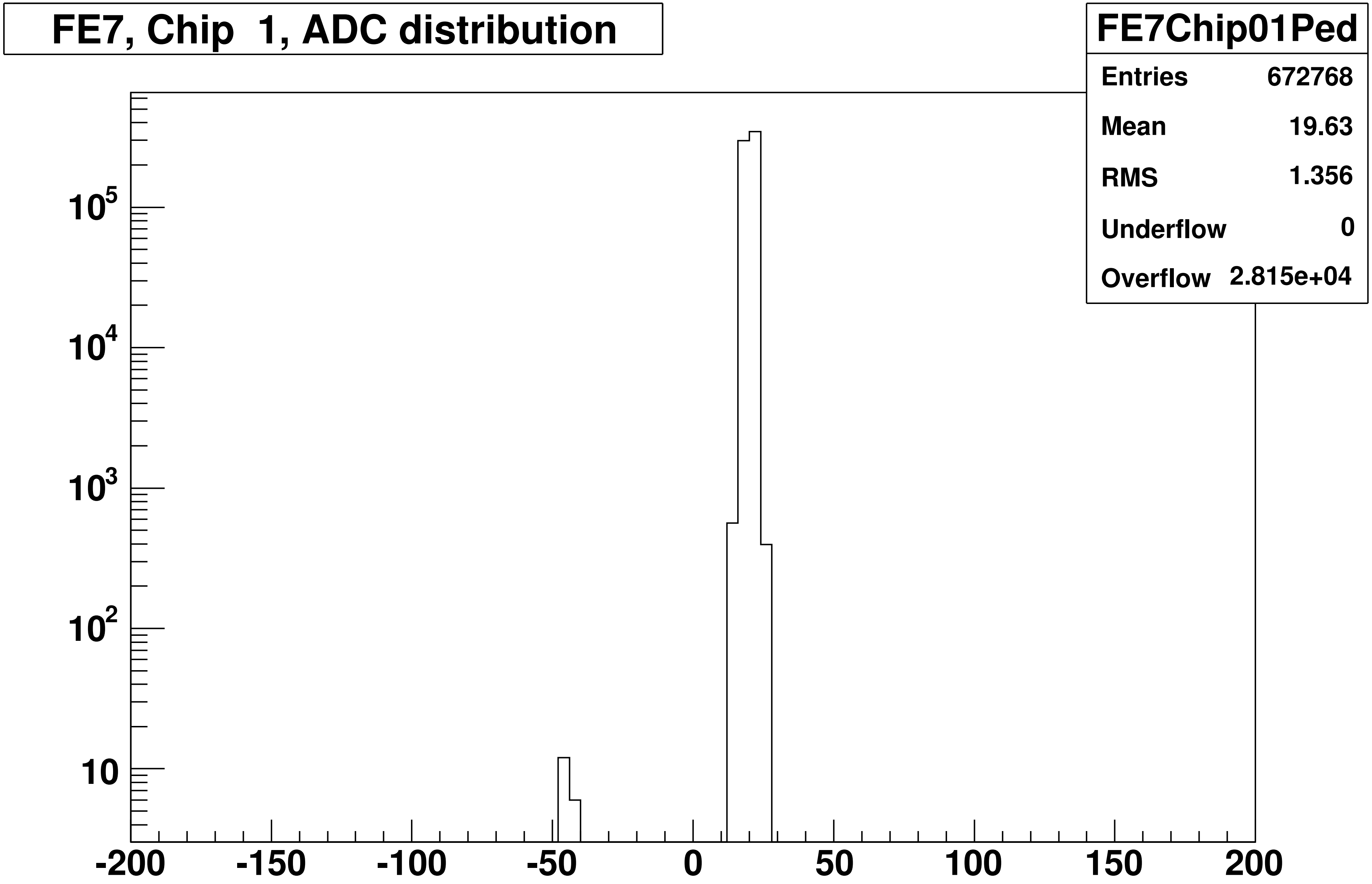


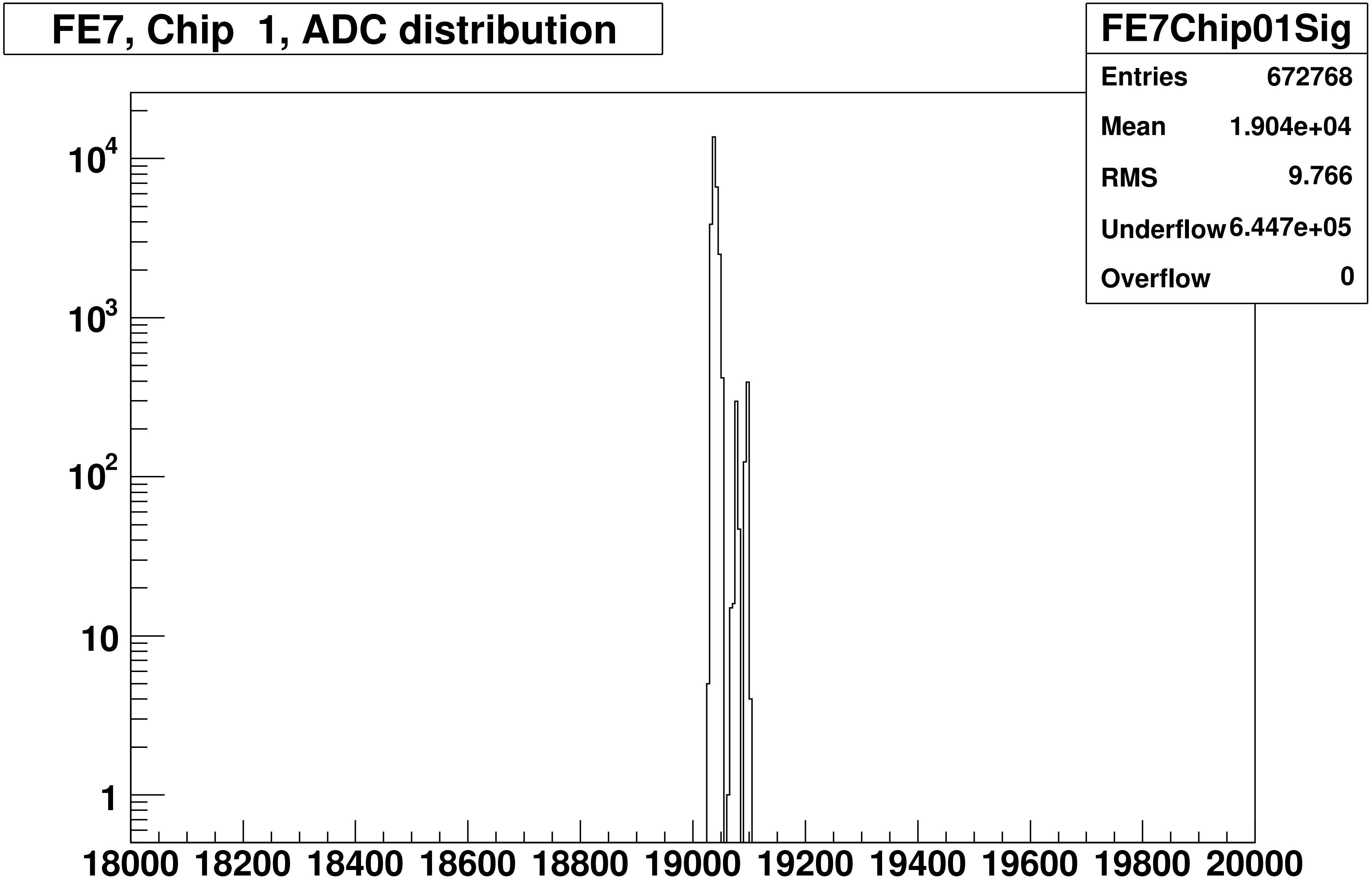
FE7, Chip 0, ADC distribution
FE7Chip00Ped
Entries 672768
Mean 7.19
RMS 1.32
Underflow 0
Overflow 2.894e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
200

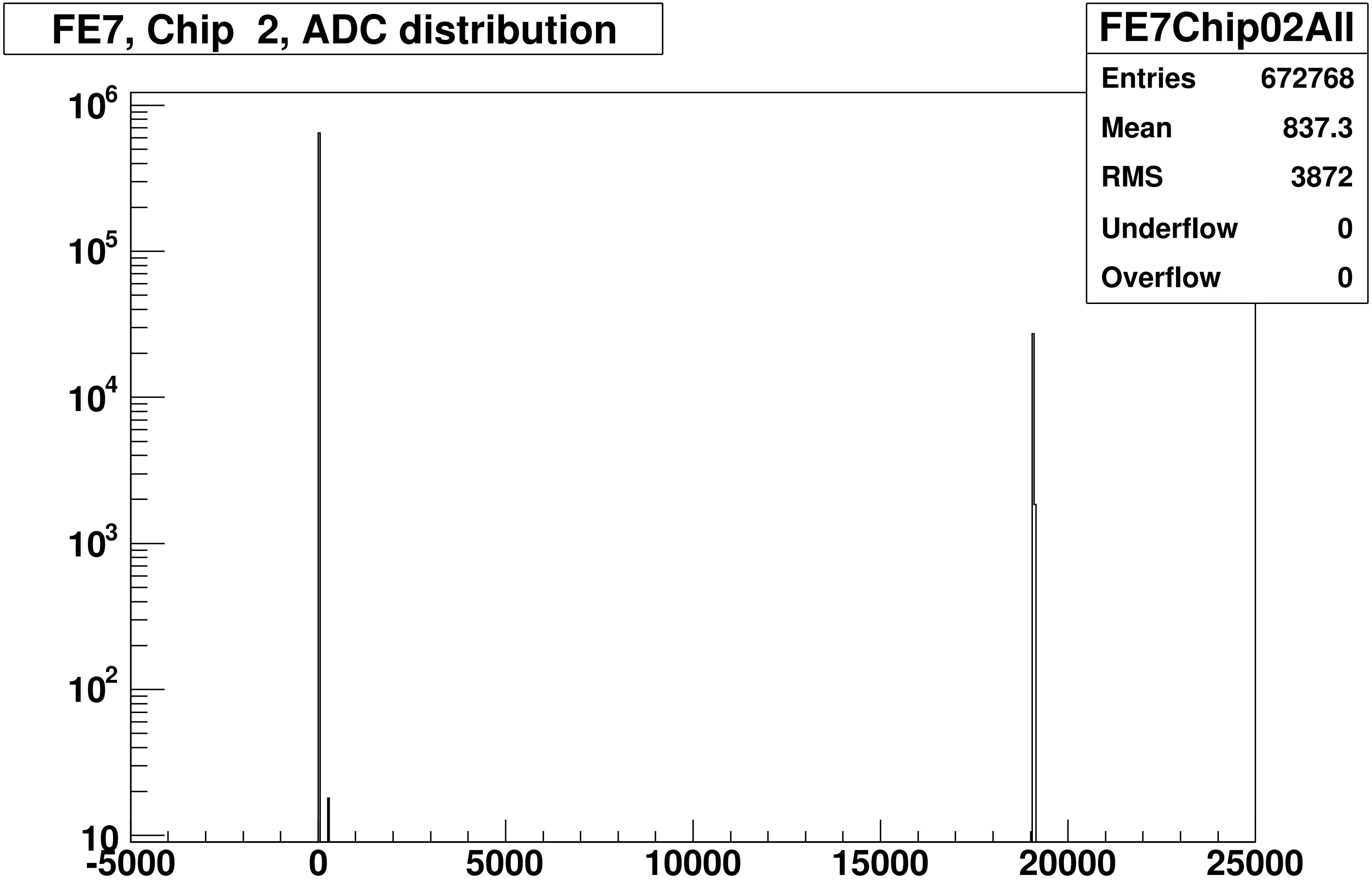


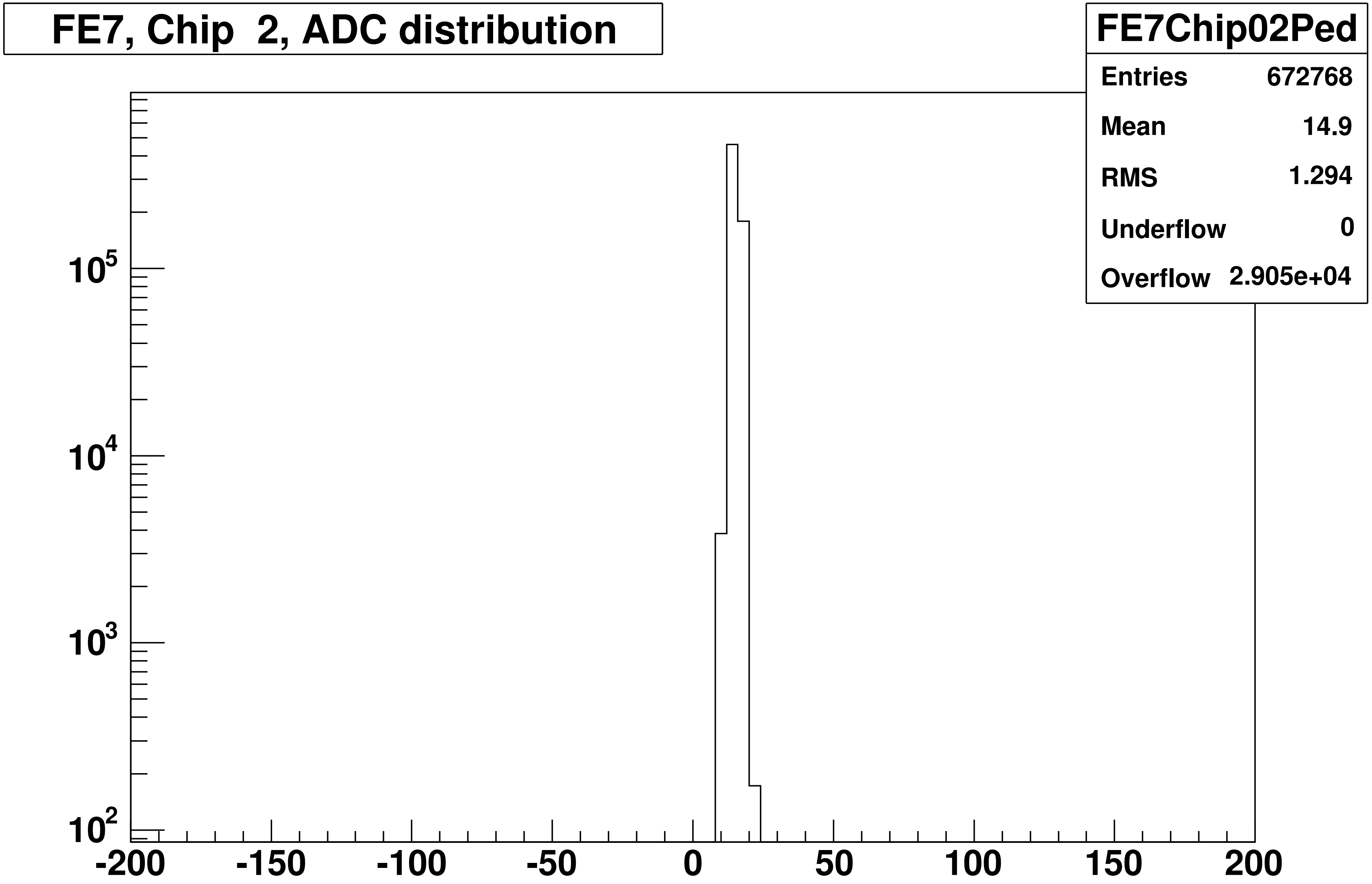
FE7, Chip 0, ADC distribution
FE7Chip00Sig
Entries 672768
Mean 1.903e+04
RMS 4.214
Underflow 6.456e+05
Overflow 0
10^4
10^3
10^2
10
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000


FE7, Chip 1, ADC distribution
FE7Chip01All
Entries 672768
Mean 812.7
RMS 3802
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE7, Chip 1, ADC distribution
FE7Chip01Ped
Entries 672768
Mean 19.63
RMS 1.356
Underflow 0
Overflow 2.815e+04
10^5
10^4
10^3
10^2
10
-200
-150
-100
-50
0
50
100
150
200


FE7, Chip 1, ADC distribution
FE7Chip01Sig
Entries 672768
Mean 1.904e+04
RMS 9.766
Underflow 6.447e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE7, Chip 2, ADC distribution
FE7Chip02All
Entries 672768
Mean 837.3
RMS 3872
Underflow 0
Overflow 0
10
10^2
10^3
10^4
10^5
10^6
-5000
0
5000
10000
15000
20000
25000



FE7, Chip 2, ADC distribution
FE7Chip02Ped
Entries 672768
Mean 14.9
RMS 1.294
Underflow 0
Overflow 2.905e+04
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10^4
10^3
10^2
-200
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-100
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0
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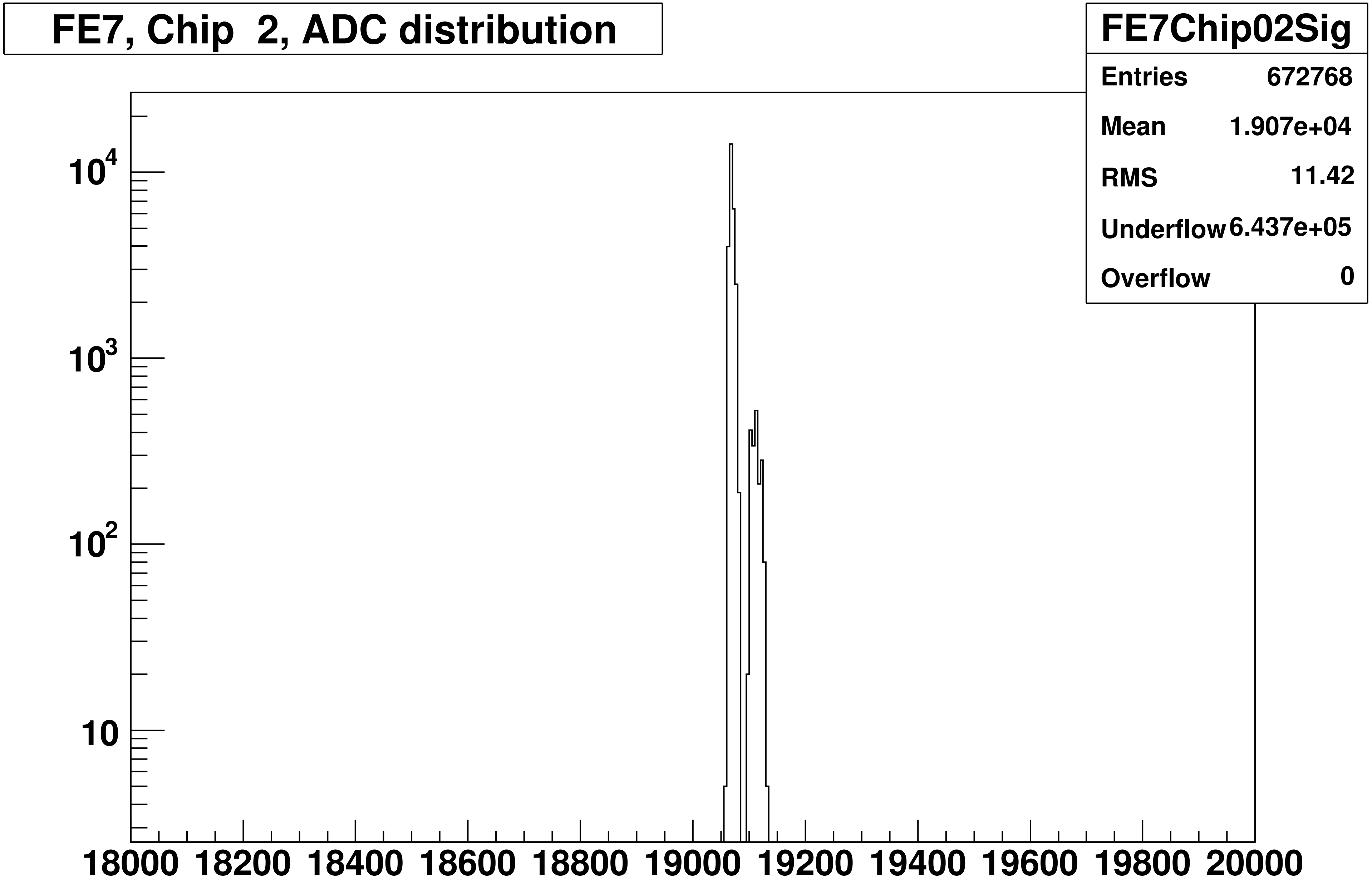
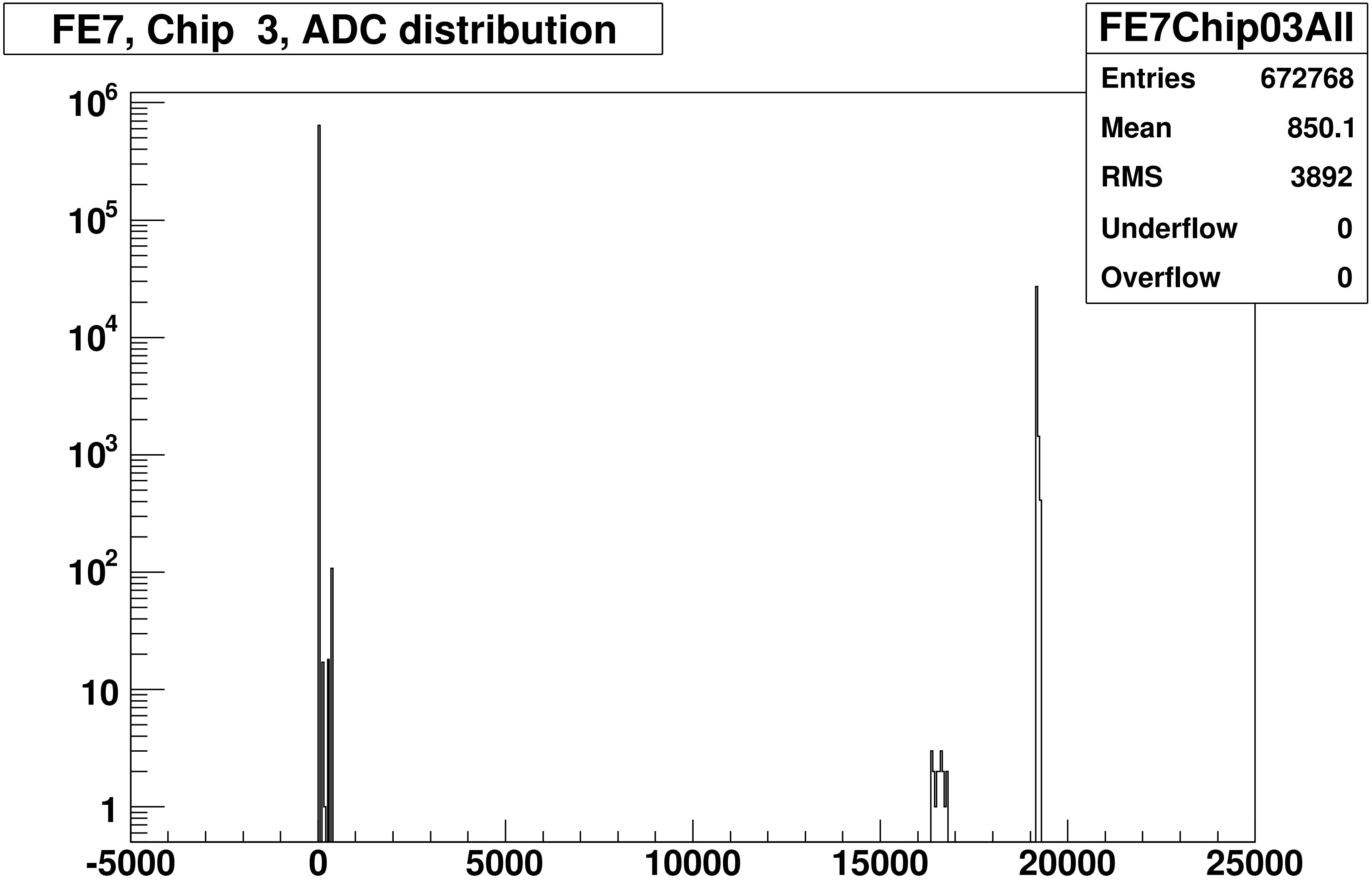
100
150
200


FE7, Chip 2, ADC distribution
FE7Chip02Sig
Entries 672768
Mean 1.907e+04
RMS 11.42
Underflow 6.437e+05
Overflow 0
10^4
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE7, Chip 3, ADC distribution
FE7Chip03All
Entries 672768
Mean 850.1
RMS 3892
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
1
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0
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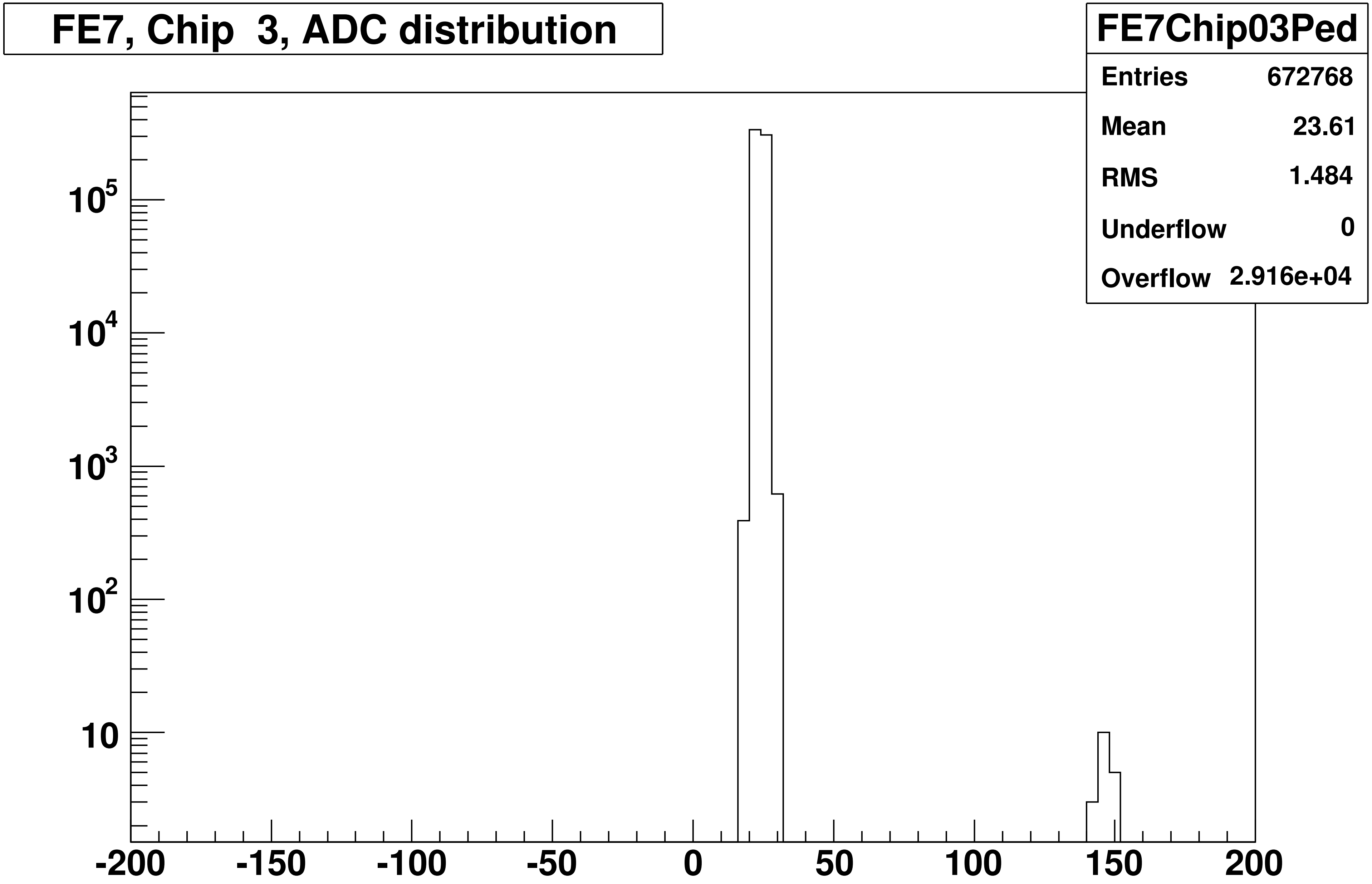
10000
15000
20000
25000


FE7, Chip 3, ADC distribution
FE7Chip03Ped
Entries 672768
Mean 23.61
RMS 1.484
Underflow 0
Overflow 2.916e+04
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10^4
10^3
10^2
10
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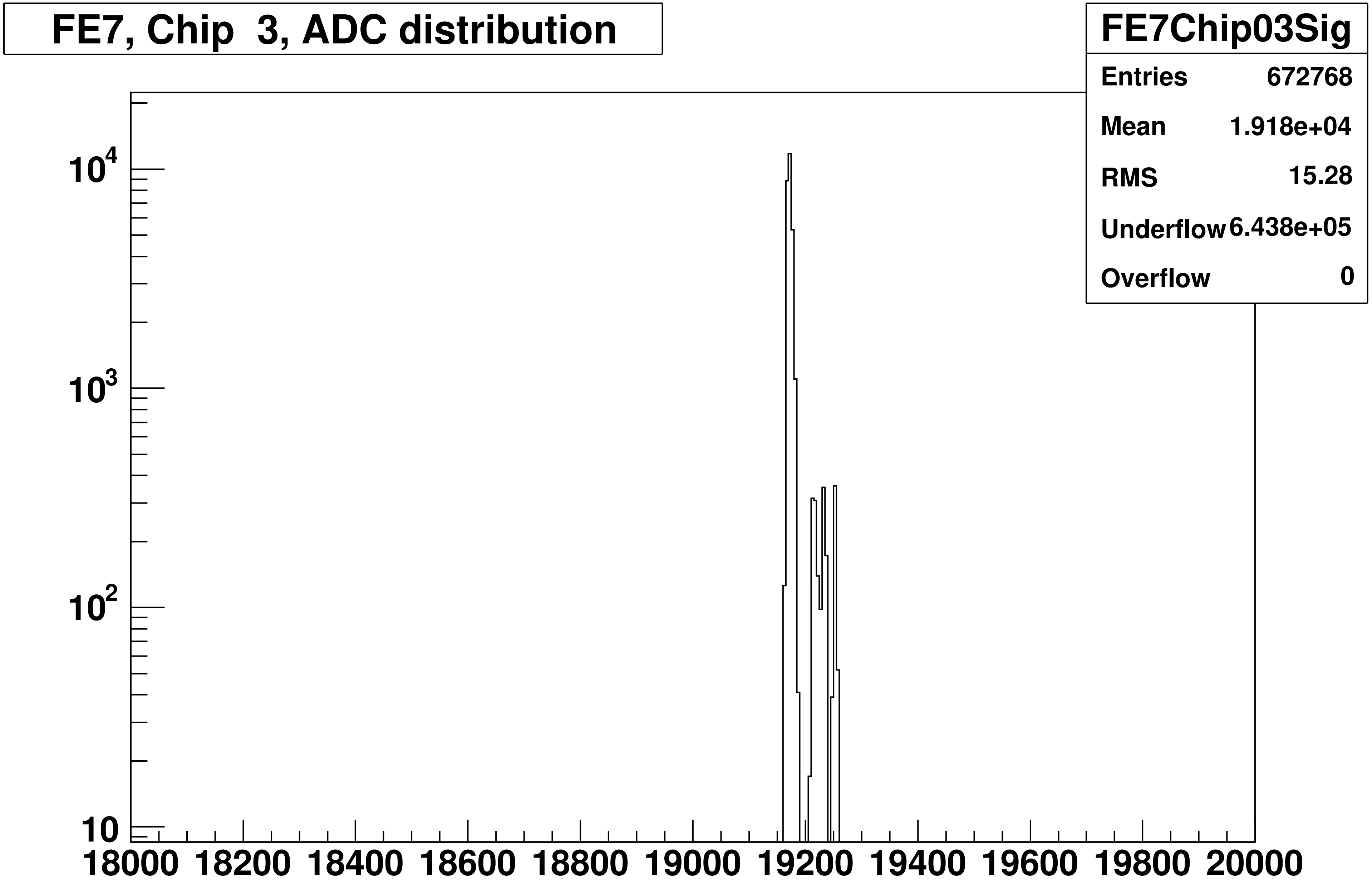
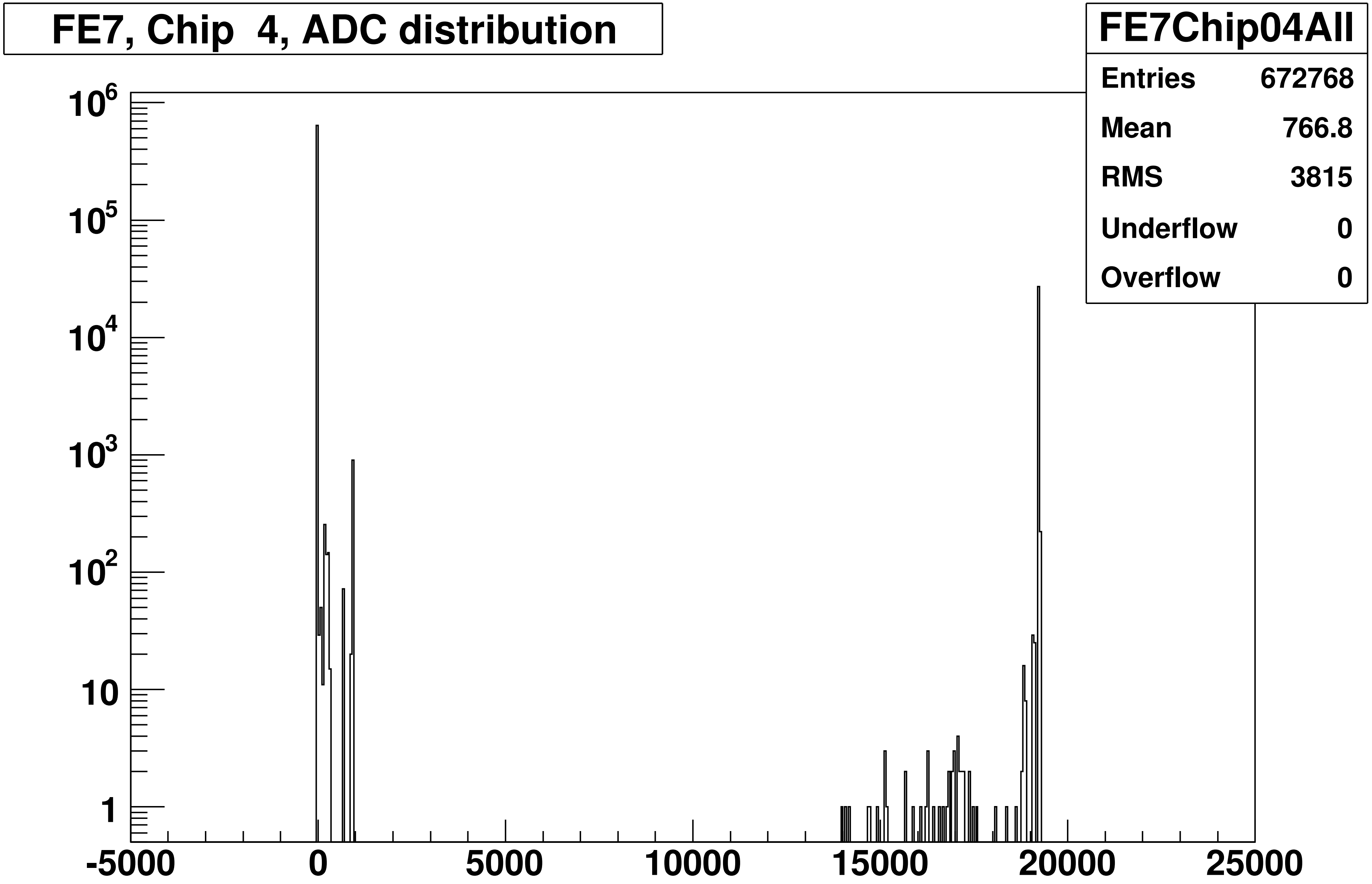
150
200


FE7, Chip 3, ADC distribution
FE7Chip03Sig
Entries 672768
Mean 1.918e+04
RMS 15.28
Underflow 6.438e+05
Overflow 0
10^4
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE7, Chip 4, ADC distribution
FE7Chip04All
Entries 672768
Mean 766.8
RMS 3815
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
1
-5000
0
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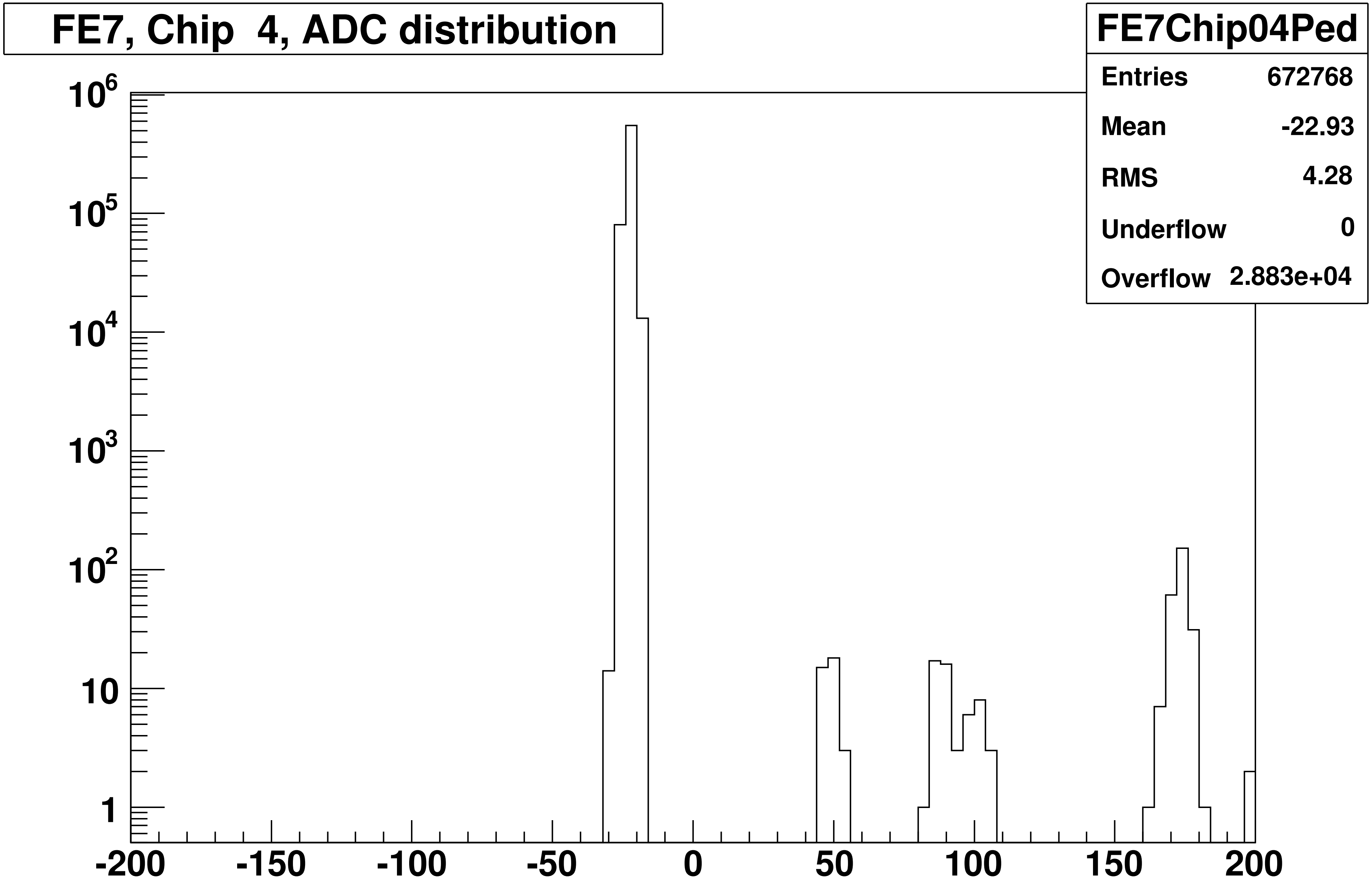
20000
25000


FE7, Chip 4, ADC distribution
FE7Chip04Ped
Entries 672768
Mean -22.93
RMS 4.28
Underflow 0
Overflow 2.883e+04
10^6
10^5
10^4
10^3
10^2
10
1
-200
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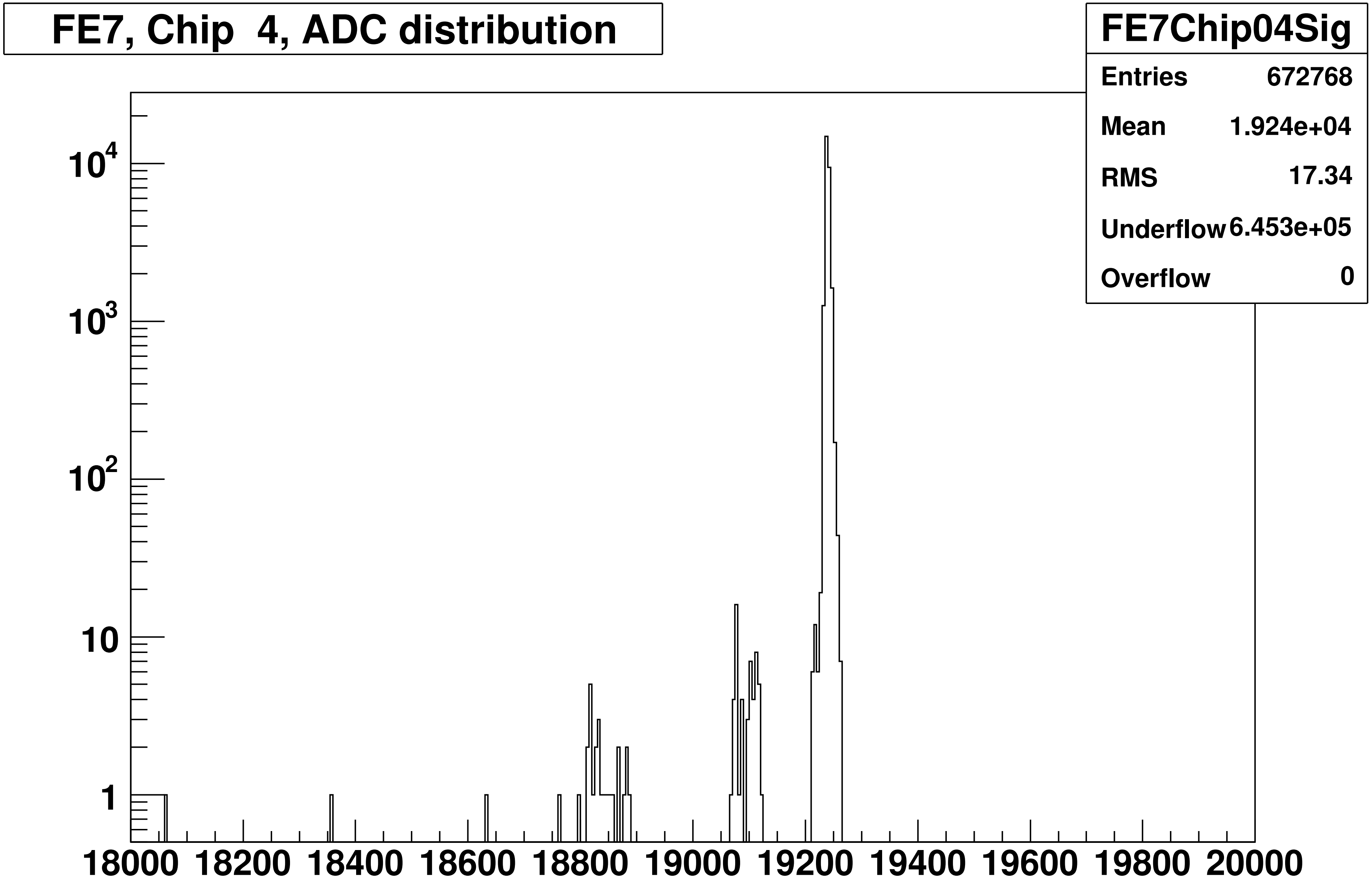
-100
-50
0
50
100
150
200



FE7, Chip 4, ADC distribution
FE7Chip04Sig
Entries 672768
Mean 1.924e+04
RMS 17.34
Underflow 6.453e+05
Overflow 0
10^4
10^3
10^2
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1
18000
18200
18400
18600
18800
19000
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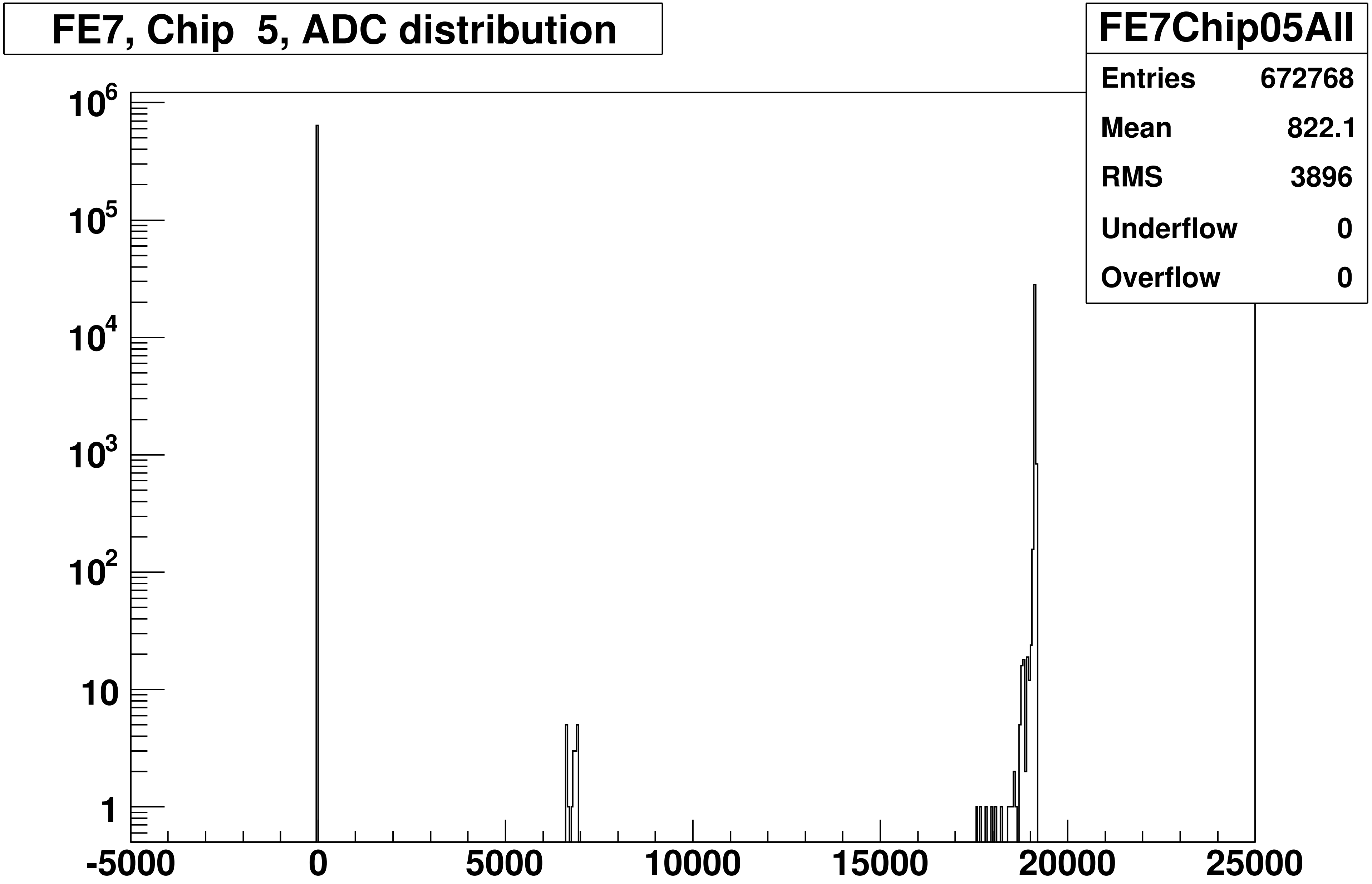
19800
20000


FE7, Chip 5, ADC distribution
FE7Chip05All
Entries 672768
Mean 822.1
RMS 3896
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
1
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0
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10000
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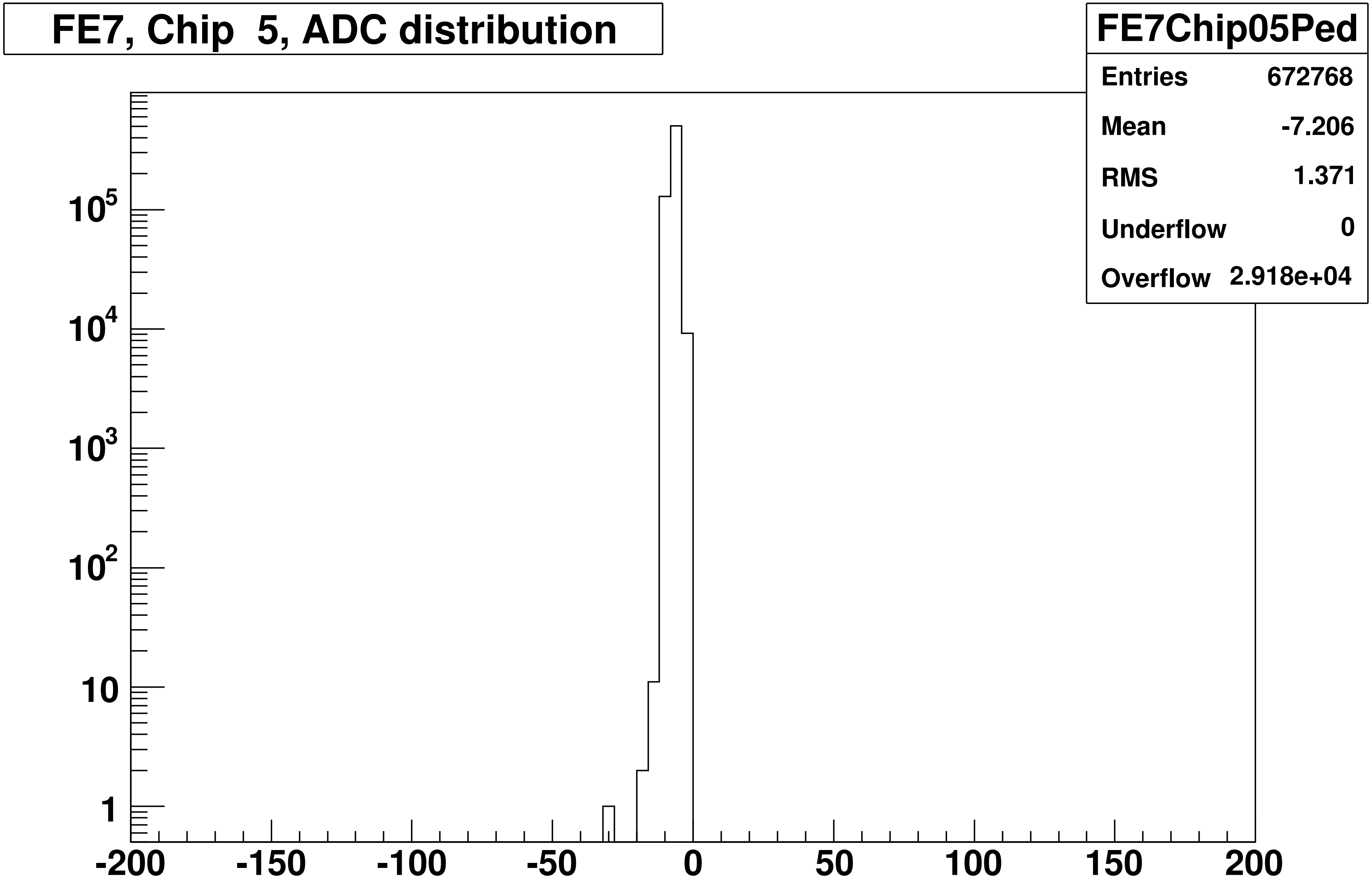
20000
25000



FE7, Chip 5, ADC distribution
FE7Chip05Ped
Entries 672768
Mean -7.206
RMS 1.371
Underflow 0
Overflow 2.918e+04
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10^4
10^3
10^2
10
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-100
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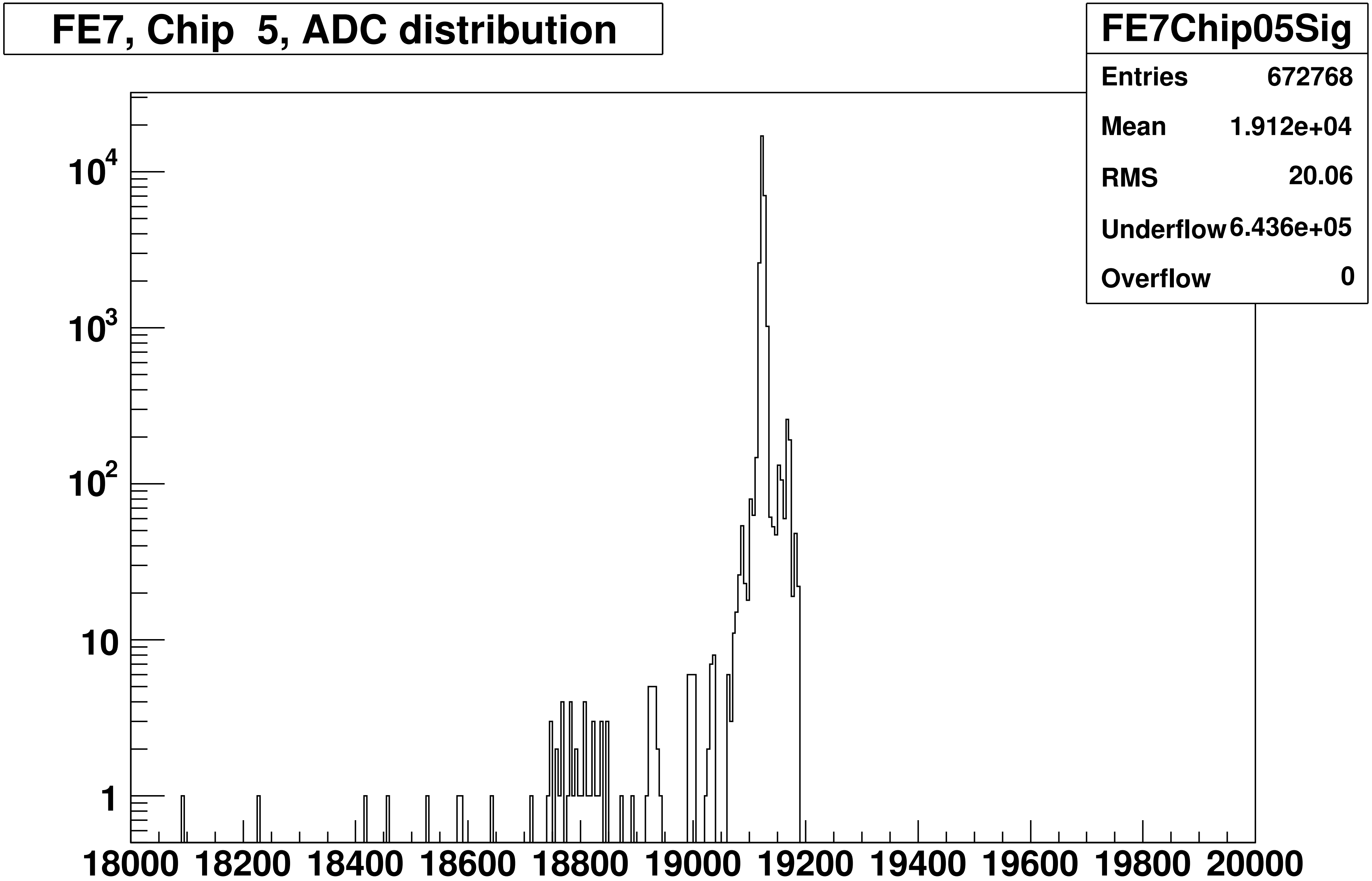
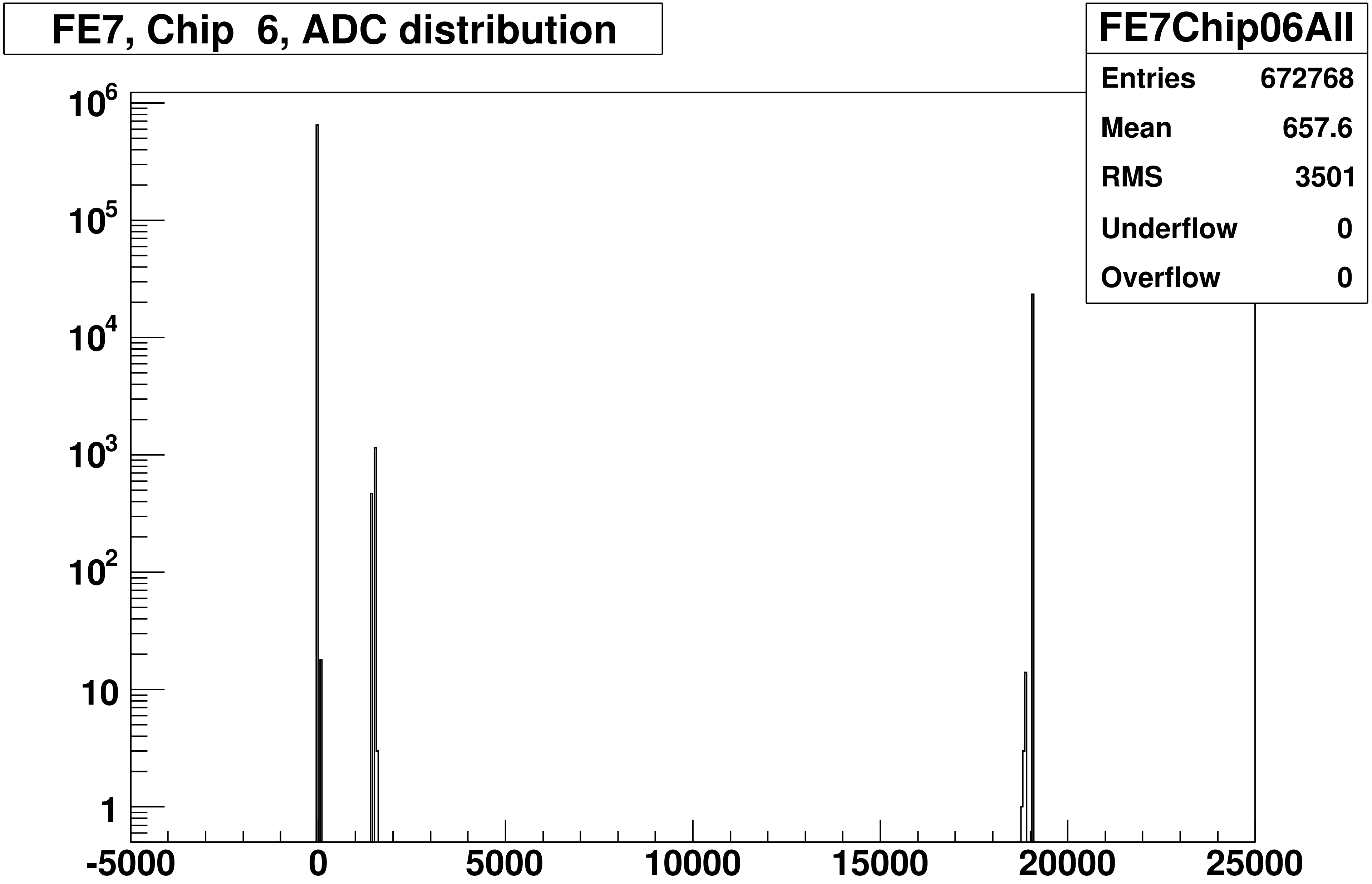
50
100
150
200


FE7, Chip 5, ADC distribution
FE7Chip05Sig
Entries 672768
Mean 1.912e+04
RMS 20.06
Underflow 6.436e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE7, Chip 6, ADC distribution
FE7Chip06All
Entries 672768
Mean 657.6
RMS 3501
Underflow 0
Overflow 0
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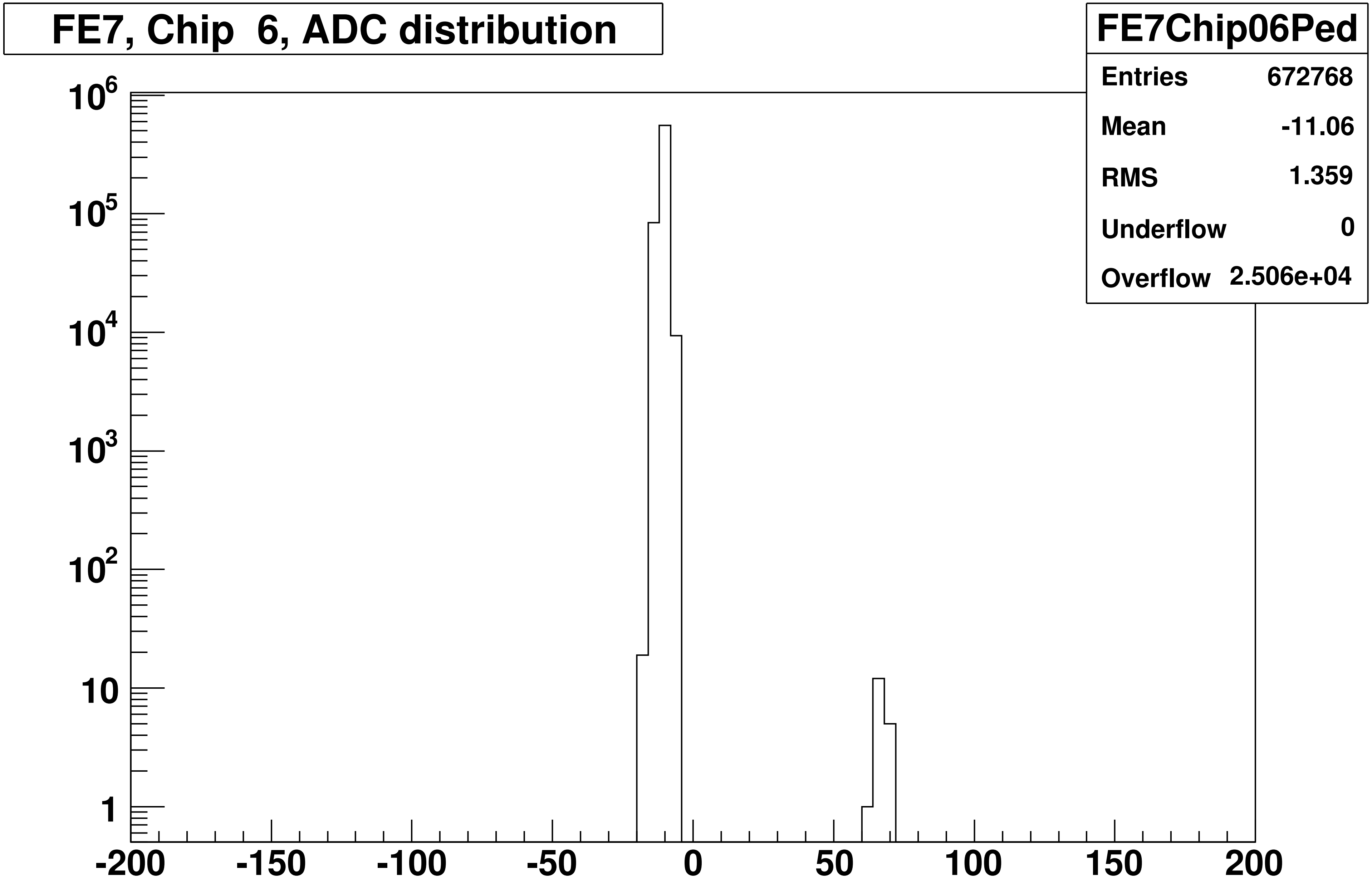
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE7, Chip 6, ADC distribution
FE7Chip06Ped
Entries 672768
Mean -11.06
RMS 1.359
Underflow 0
Overflow 2.506e+04
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10^5
10^4
10^3
10^2
10
1
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-100
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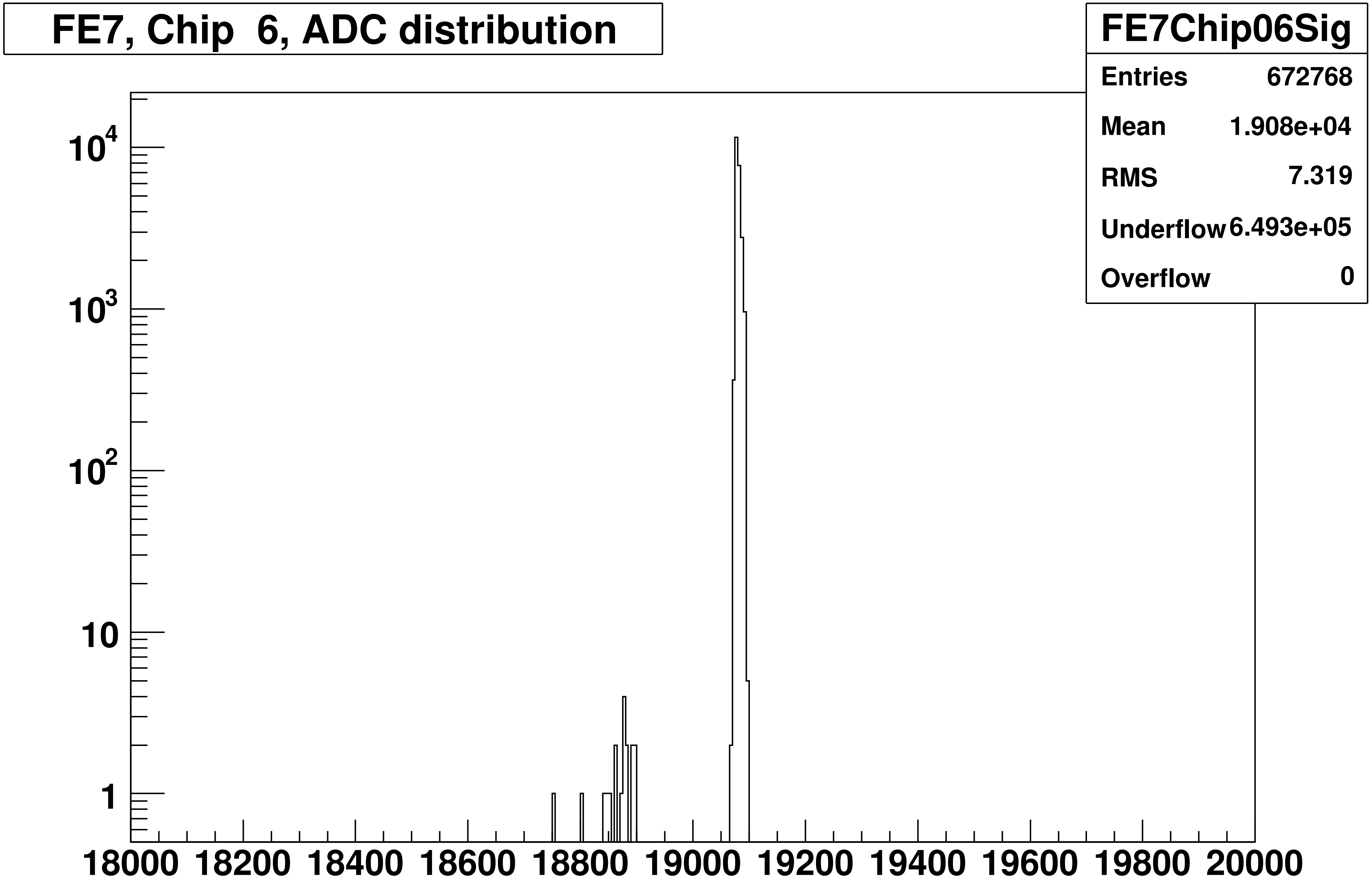
0
50
100
150
200



FE7, Chip 6, ADC distribution
FE7Chip06Sig
Entries 672768
Mean 1.908e+04
RMS 7.319
Underflow 6.493e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
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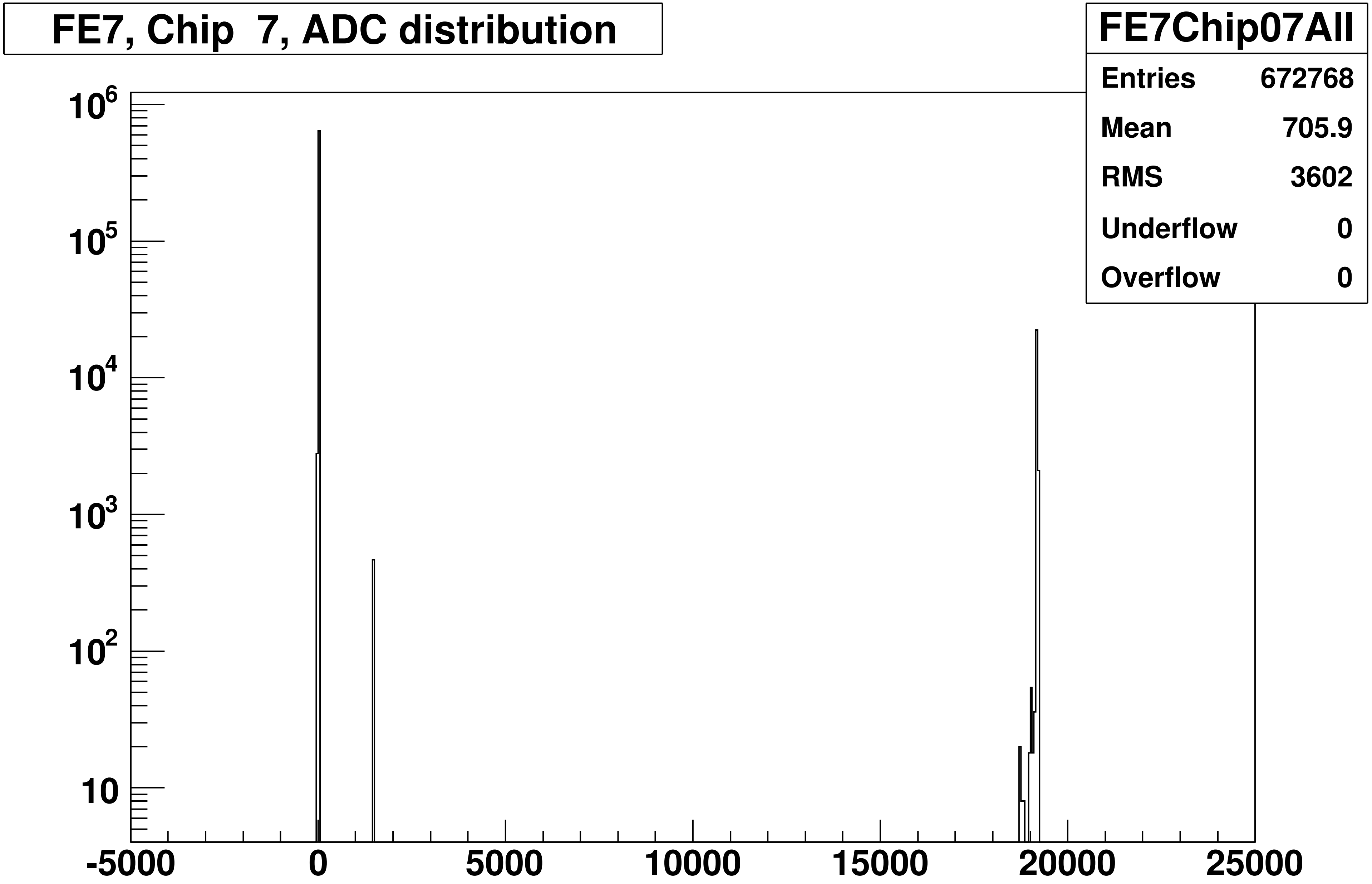
19400
19600
19800
20000


FE7, Chip 7, ADC distribution
FE7Chip07All
Entries 672768
Mean 705.9
RMS 3602
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
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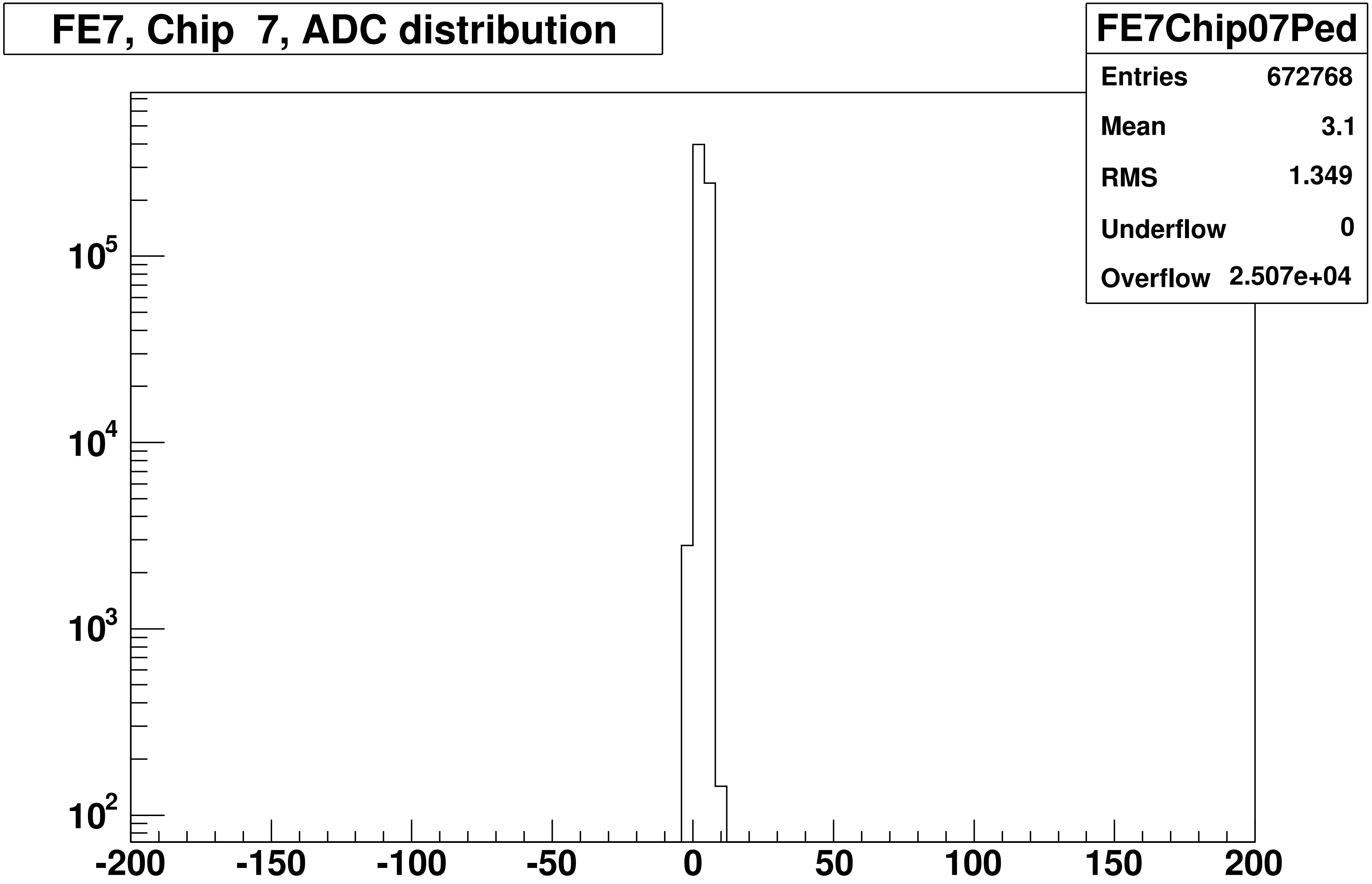
5000
10000
15000
20000
25000



FE7, Chip 7, ADC distribution
FE7Chip07Ped
Entries 672768
Mean 3.1
RMS 1.349
Underflow 0
Overflow 2.507e+04
10^5
10^4
10^3
10^2
-200
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-100
-50
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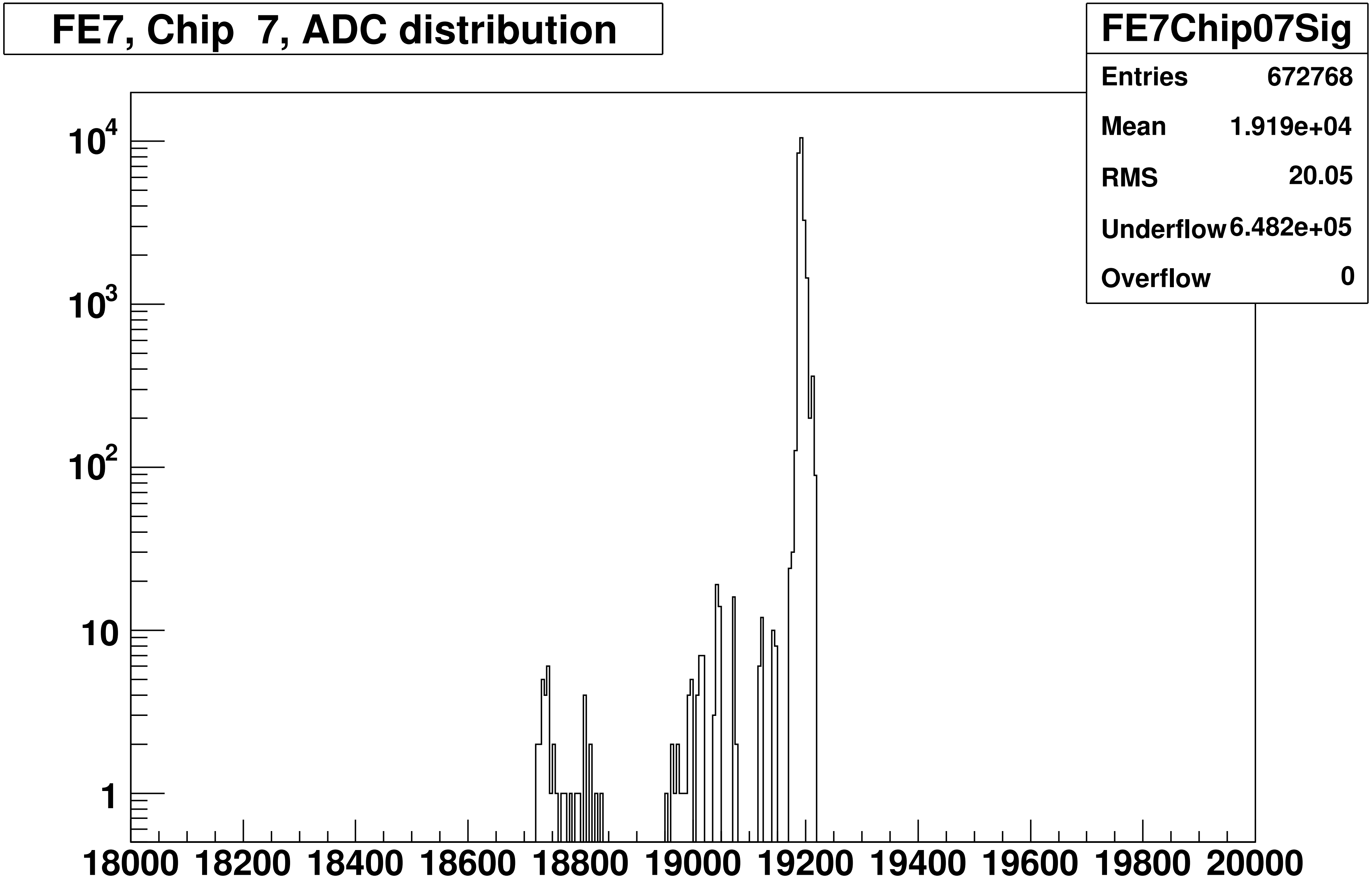
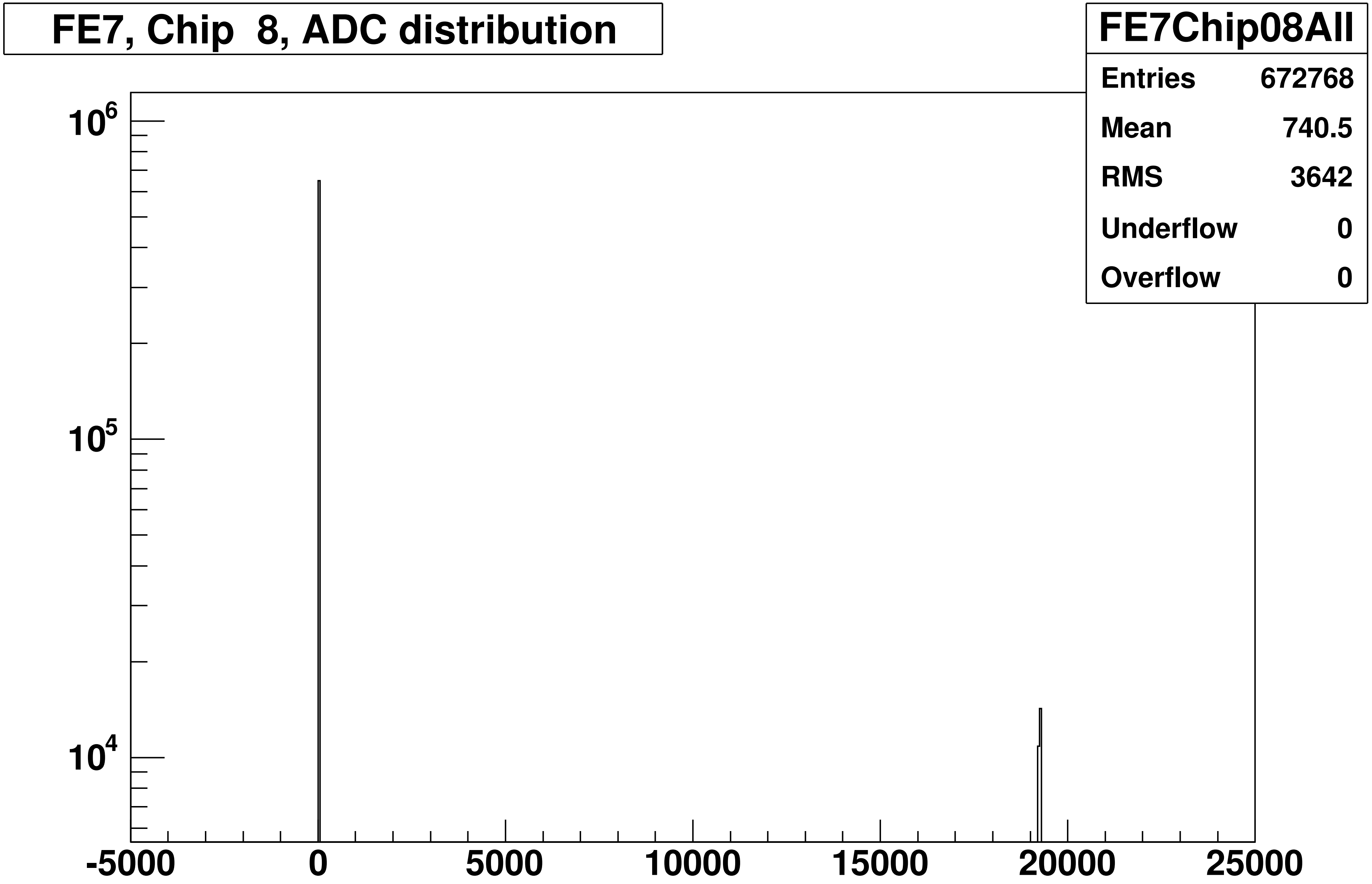
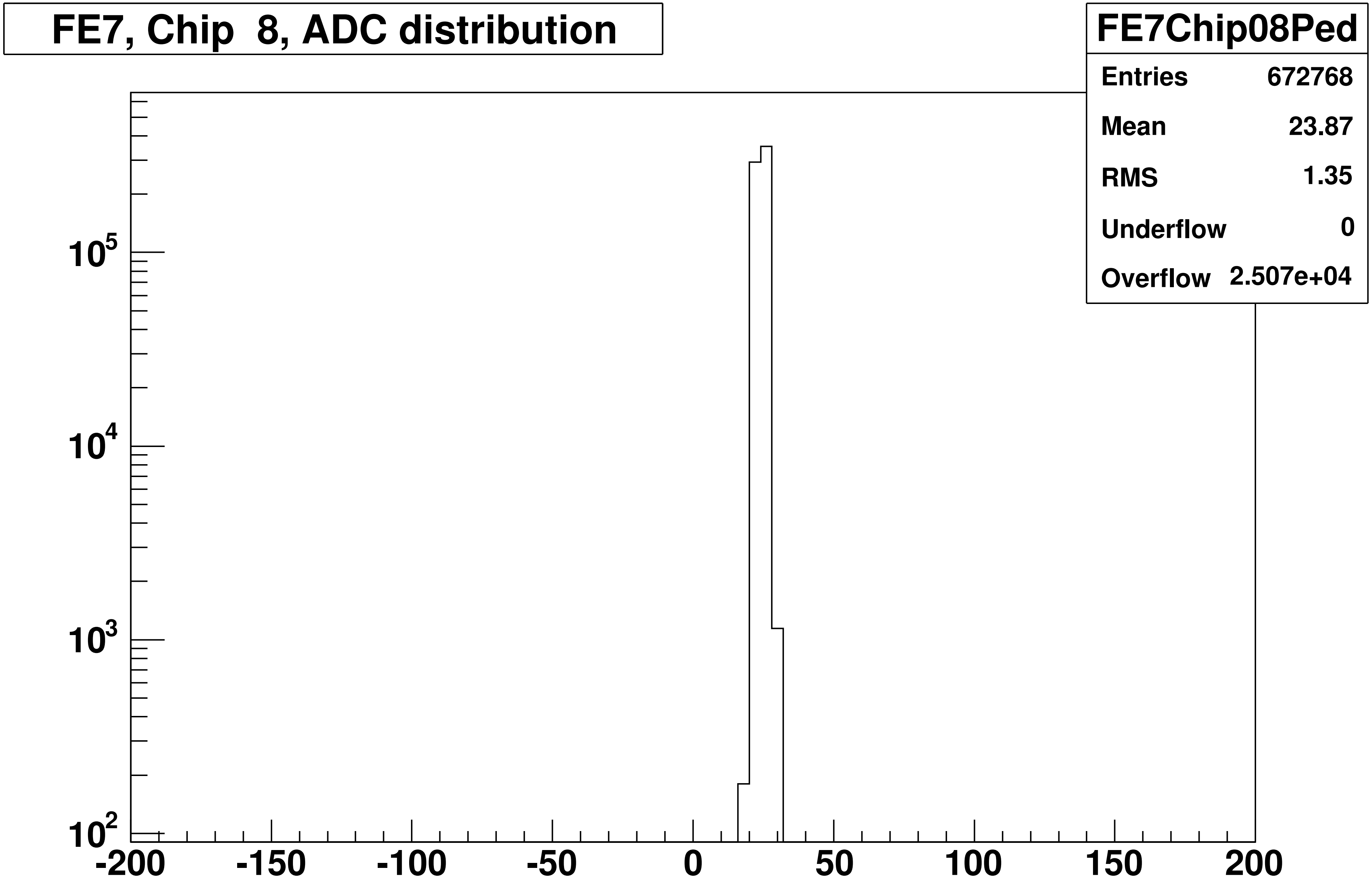
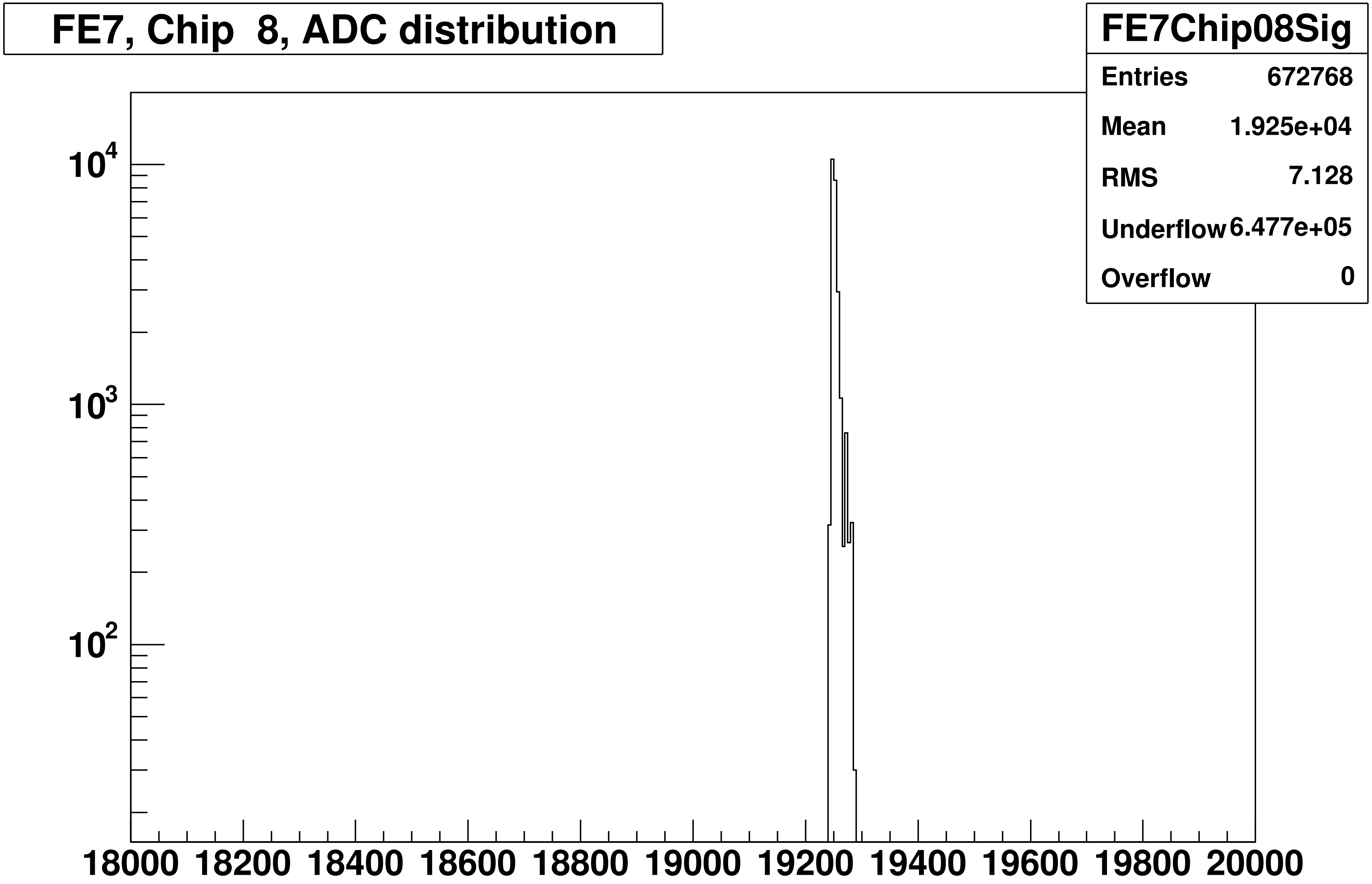
100
150
200

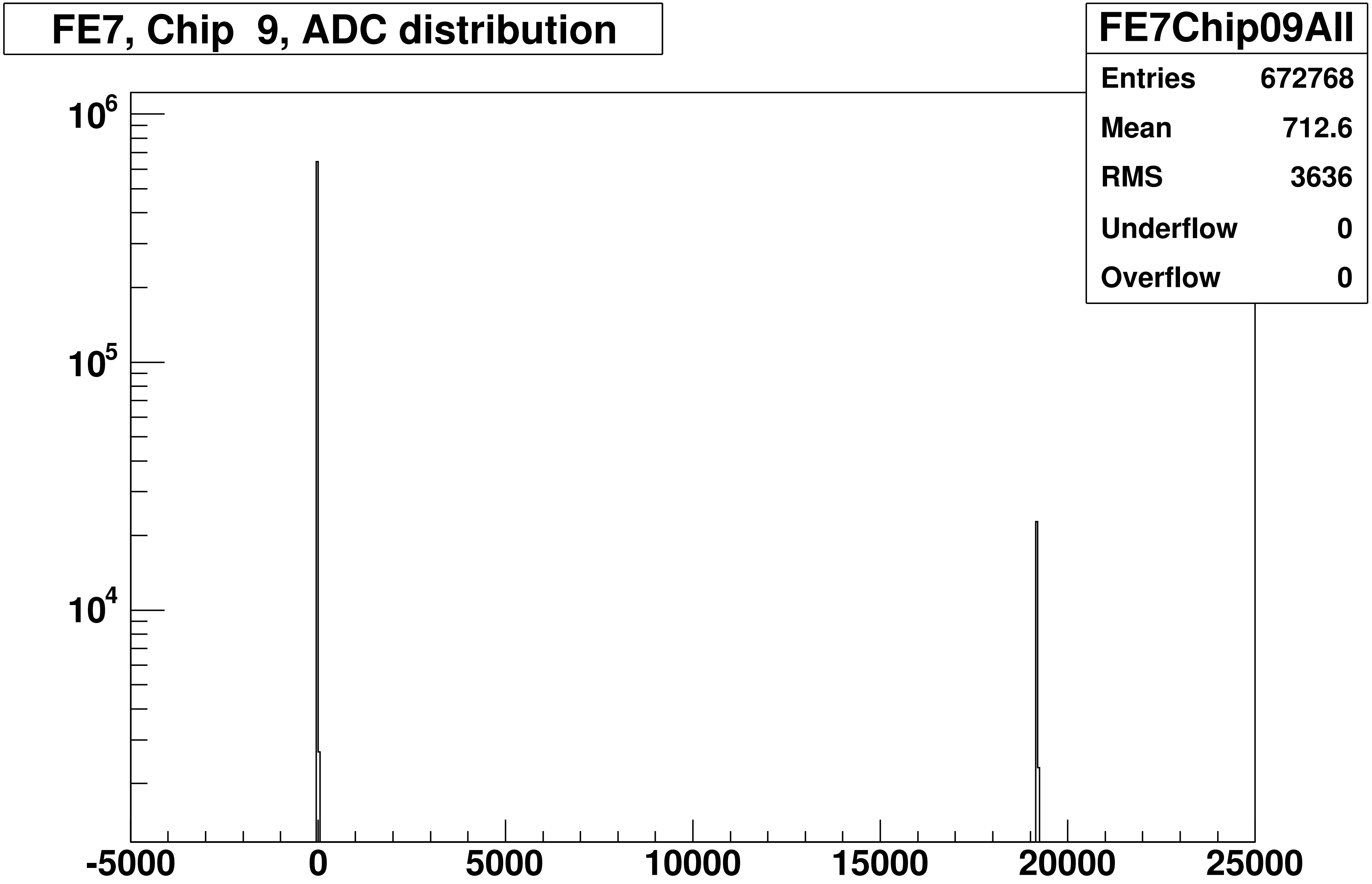

FE7, Chip 7, ADC distribution
FE7Chip07Sig
Entries 672768
Mean 1.919e+04
RMS 20.05
Underflow 6.482e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



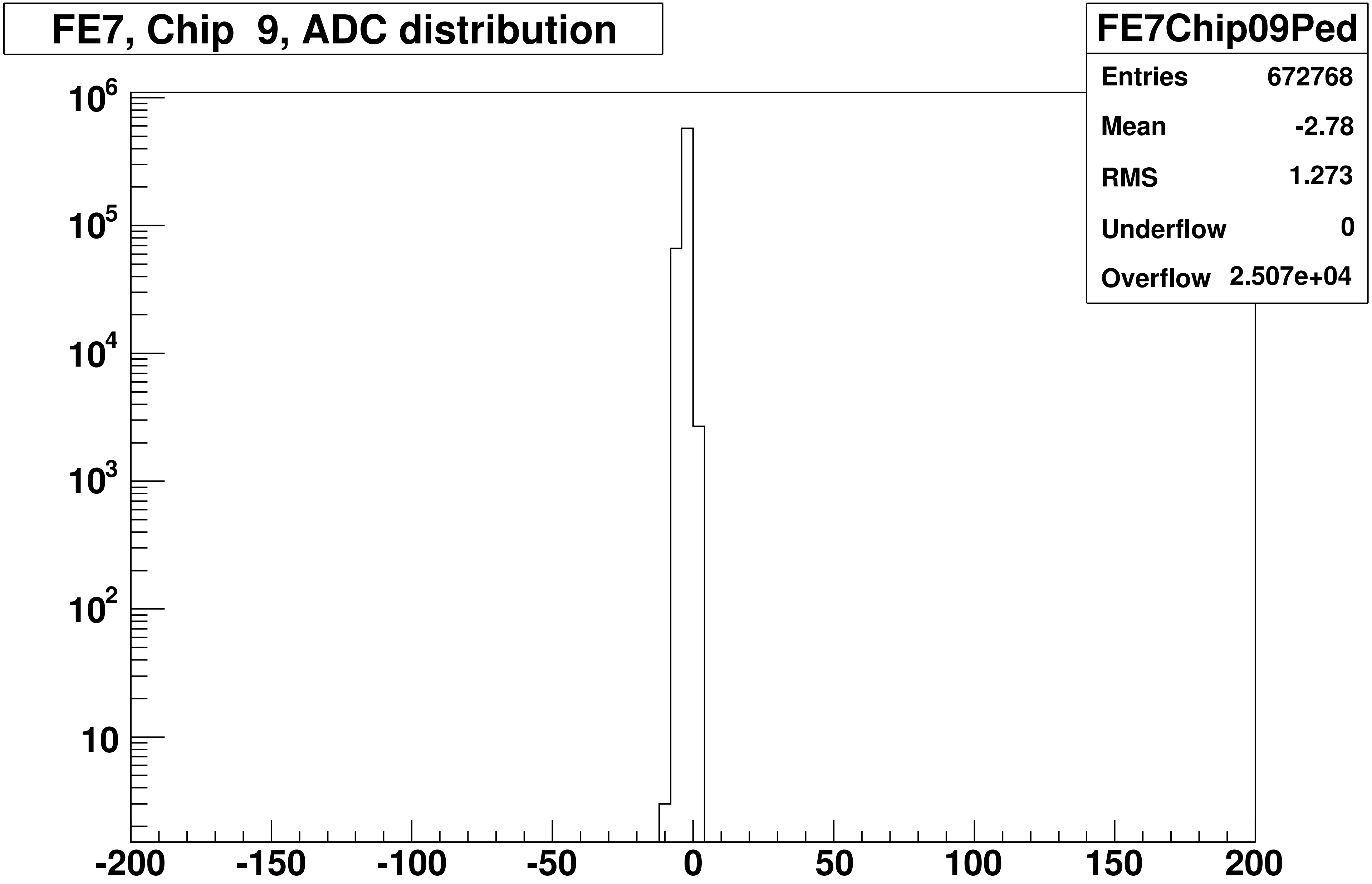
FE7, Chip 8, ADC distribution
FE7Chip08All
Entries 672768
Mean 740.5
RMS 3642
Underflow 0
Overflow 0
10^6
10^5
10^4
-5000
0
5000
10000
15000
20000
25000


FE7, Chip 8, ADC distribution
FE7Chip08Ped
Entries 672768
Mean 23.87
RMS 1.35
Underflow 0
Overflow 2.507e+04
10^5
10^4
10^3
10^2
-200
-150
-100
-50
0
50
100
150
200

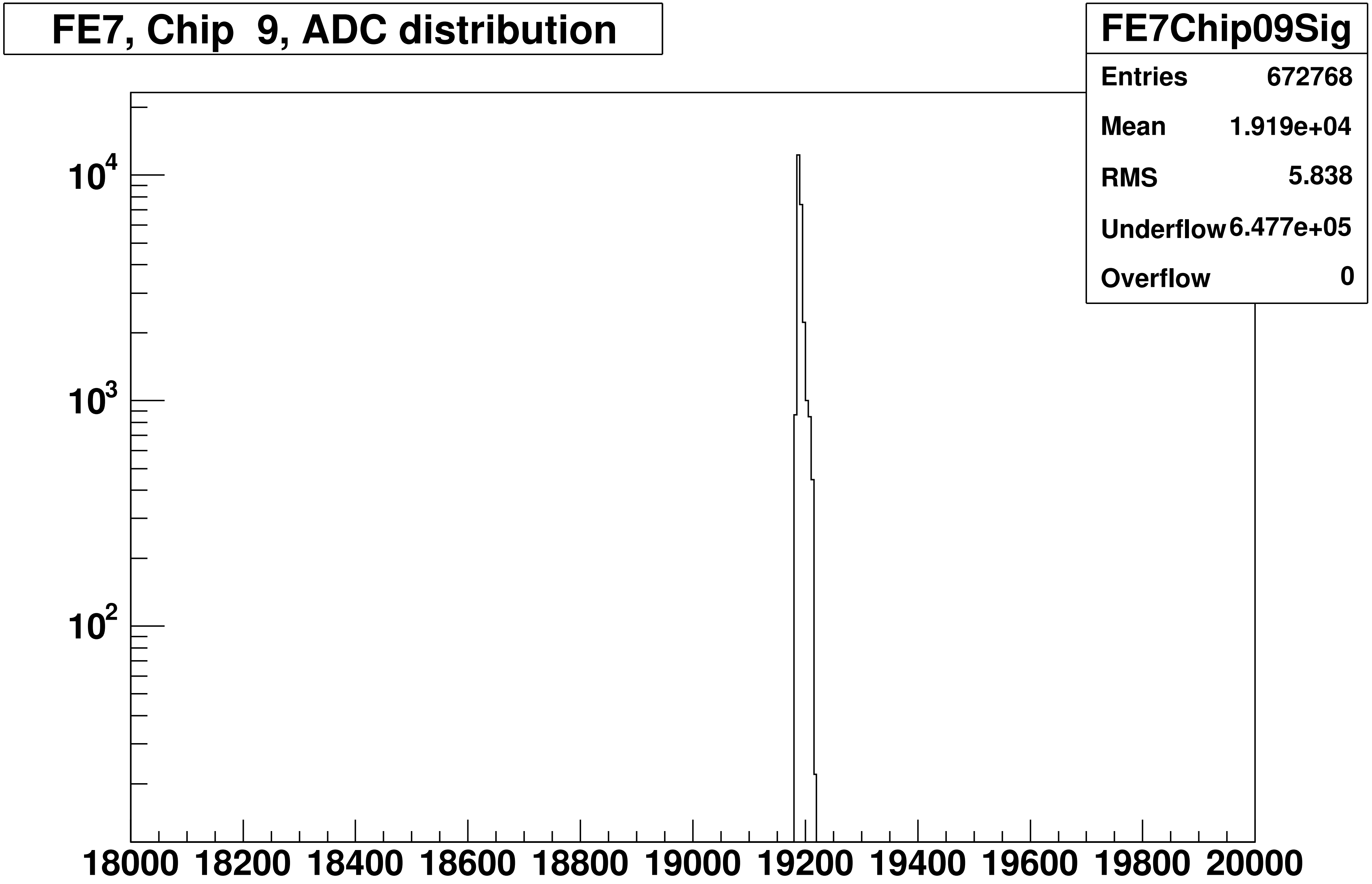

FE7, Chip 8, ADC distribution
FE7Chip08Sig
Entries 672768
Mean 1.925e+04
RMS 7.128
Underflow 6.477e+05
Overflow 0
10^4
10^3
10^2
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000

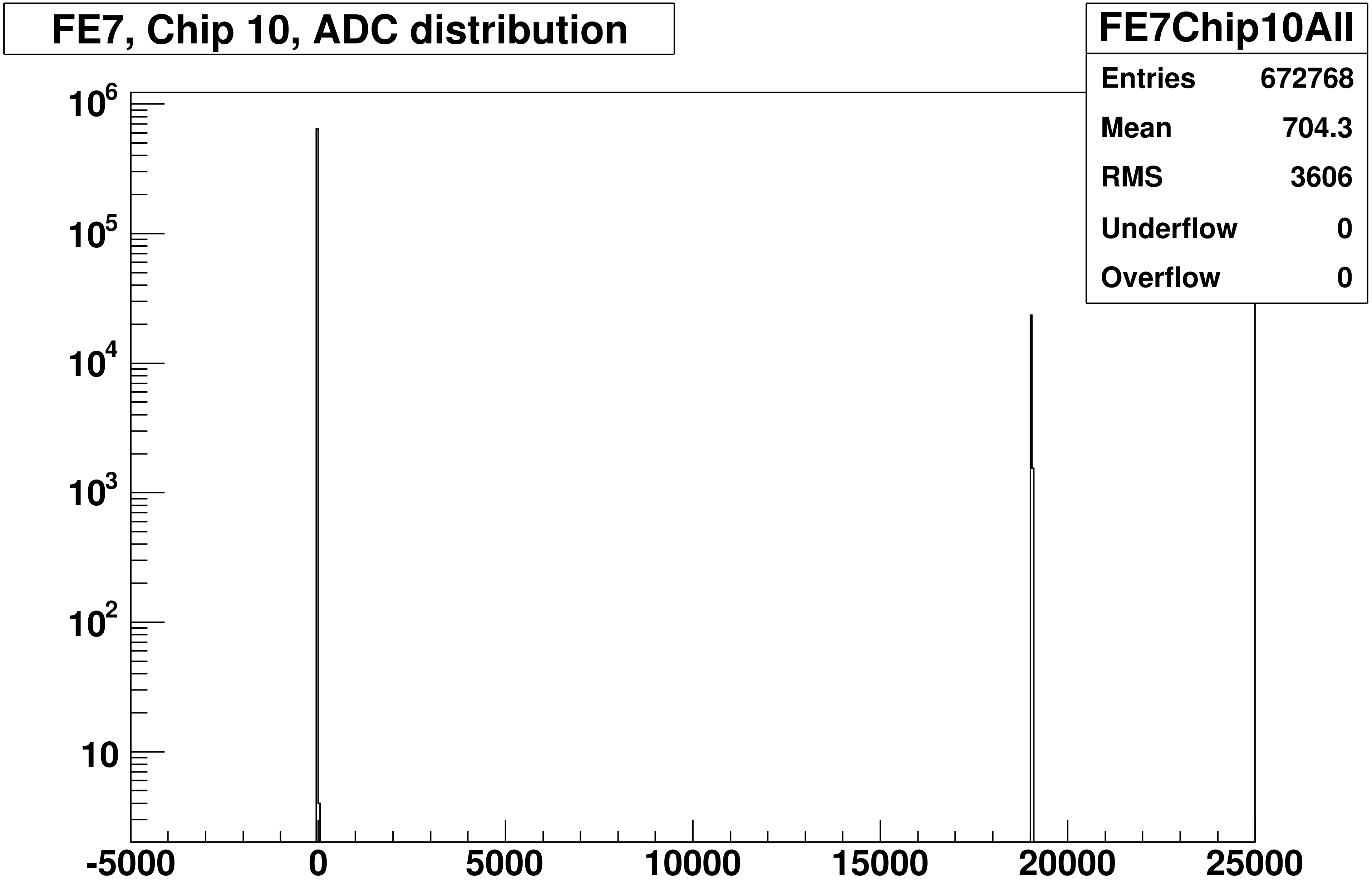


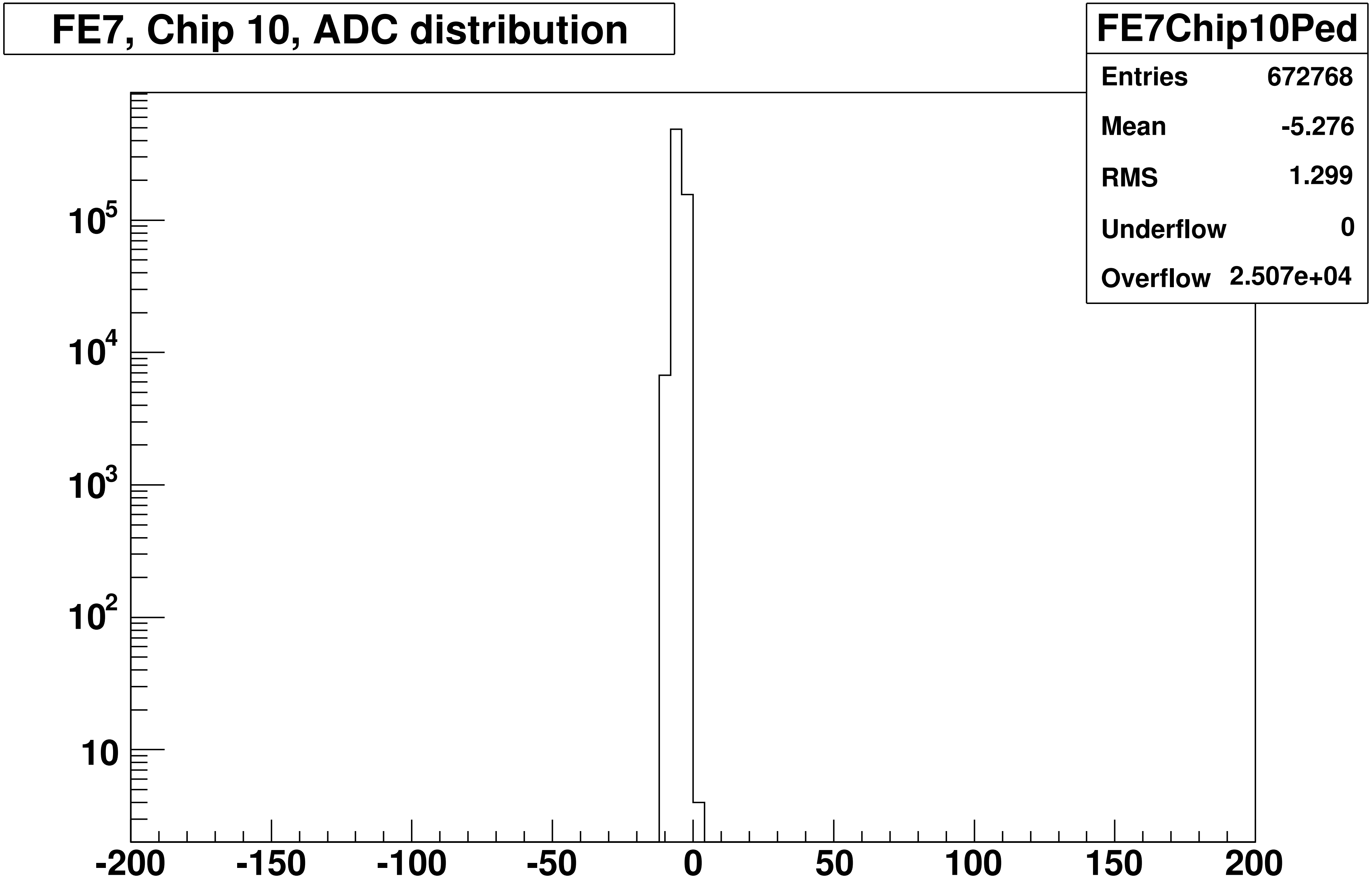
FE7, Chip 9, ADC distribution
FE7Chip09All
Entries 672768
Mean 712.6
RMS 3636
Underflow 0
Overflow 0
10^6
10^5
10^4
-5000
0
5000
10000
15000
20000
25000

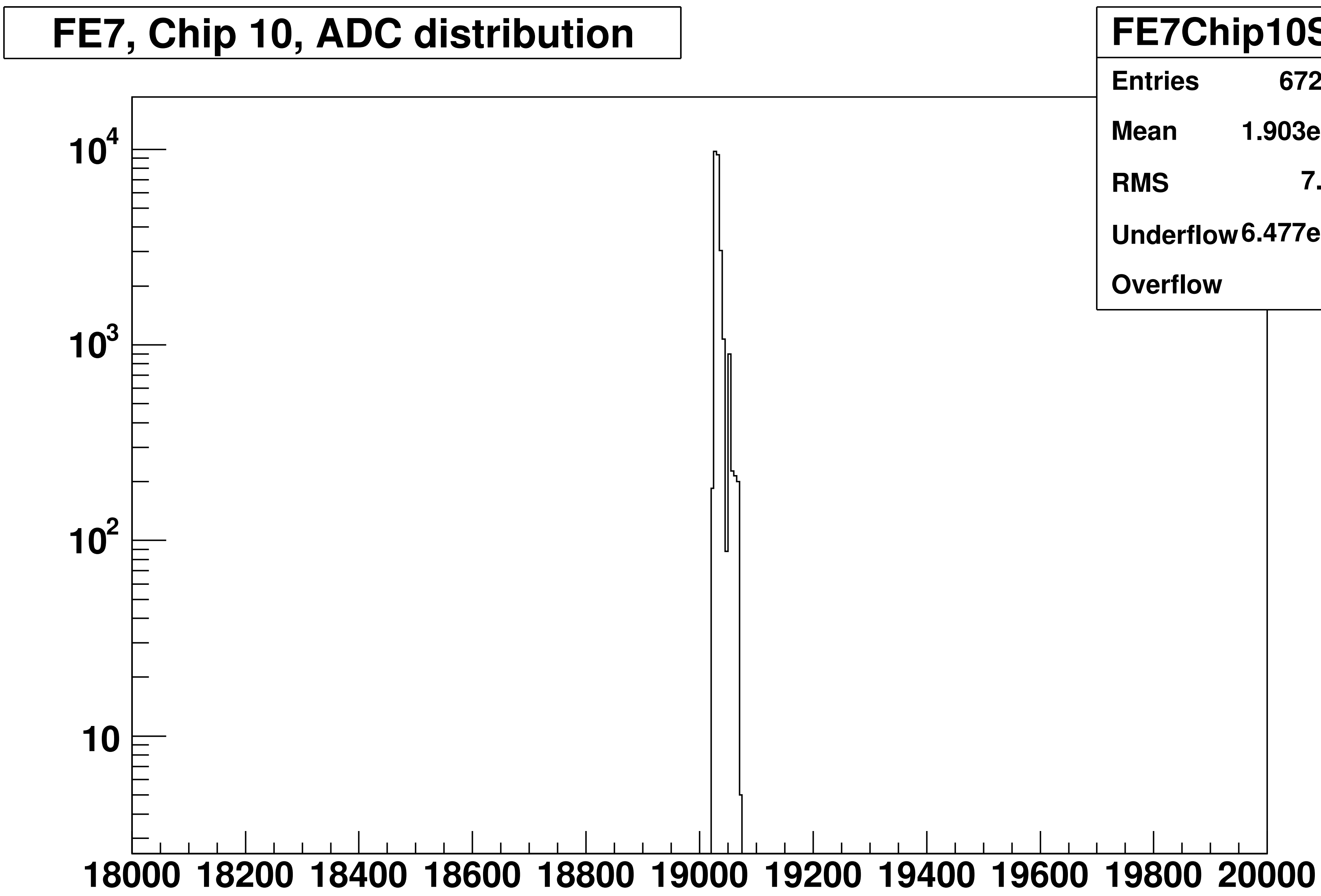


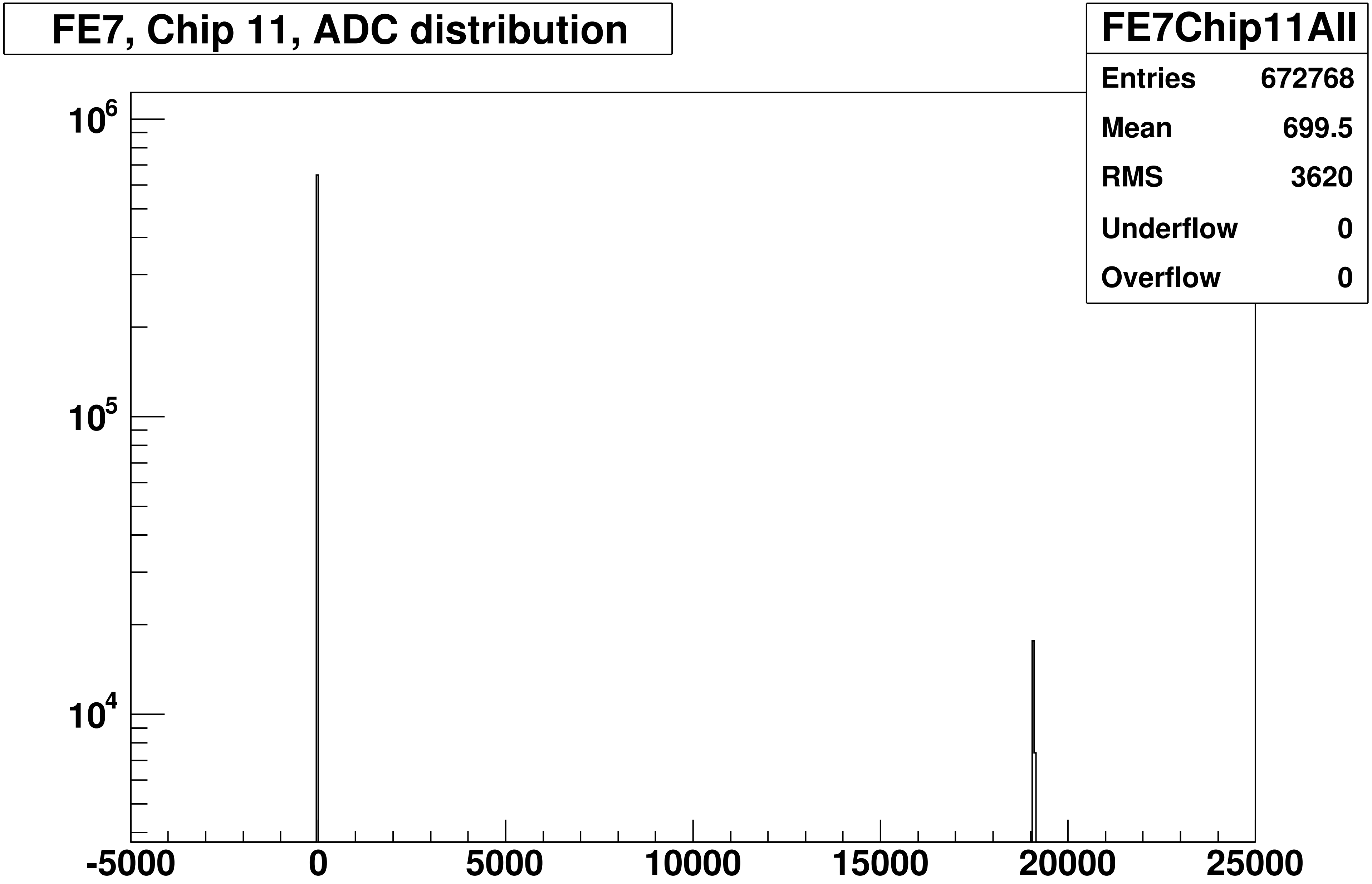
FE7, Chip 9, ADC distribution
FE7Chip09Ped
Entries 672768
Mean -2.78
RMS 1.273
Underflow 0
Overflow 2.507e+04
10^6
10^5
10^4
10^3
10^2
10
-200
-150
-100
-50
0
50
100
150
200


FE7, Chip 9, ADC distribution
FE7Chip09Sig
Entries 672768
Mean 1.919e+04
RMS 5.838
Underflow 6.477e+05
Overflow 0
10^4
10^3
10^2
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000

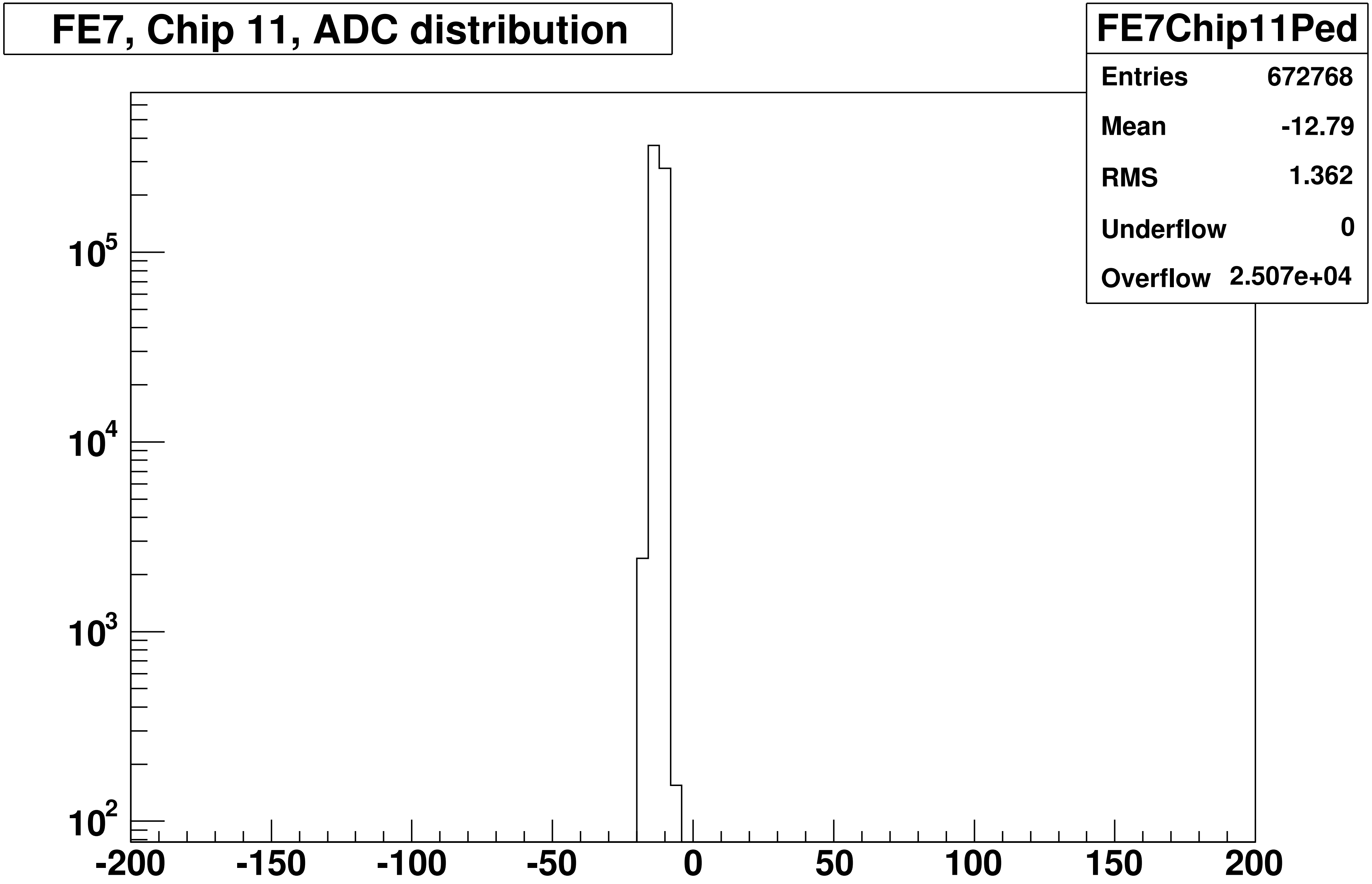

FE7, Chip 10, ADC distribution
FE7Chip10All
Entries 672768
Mean 704.3
RMS 3606
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000

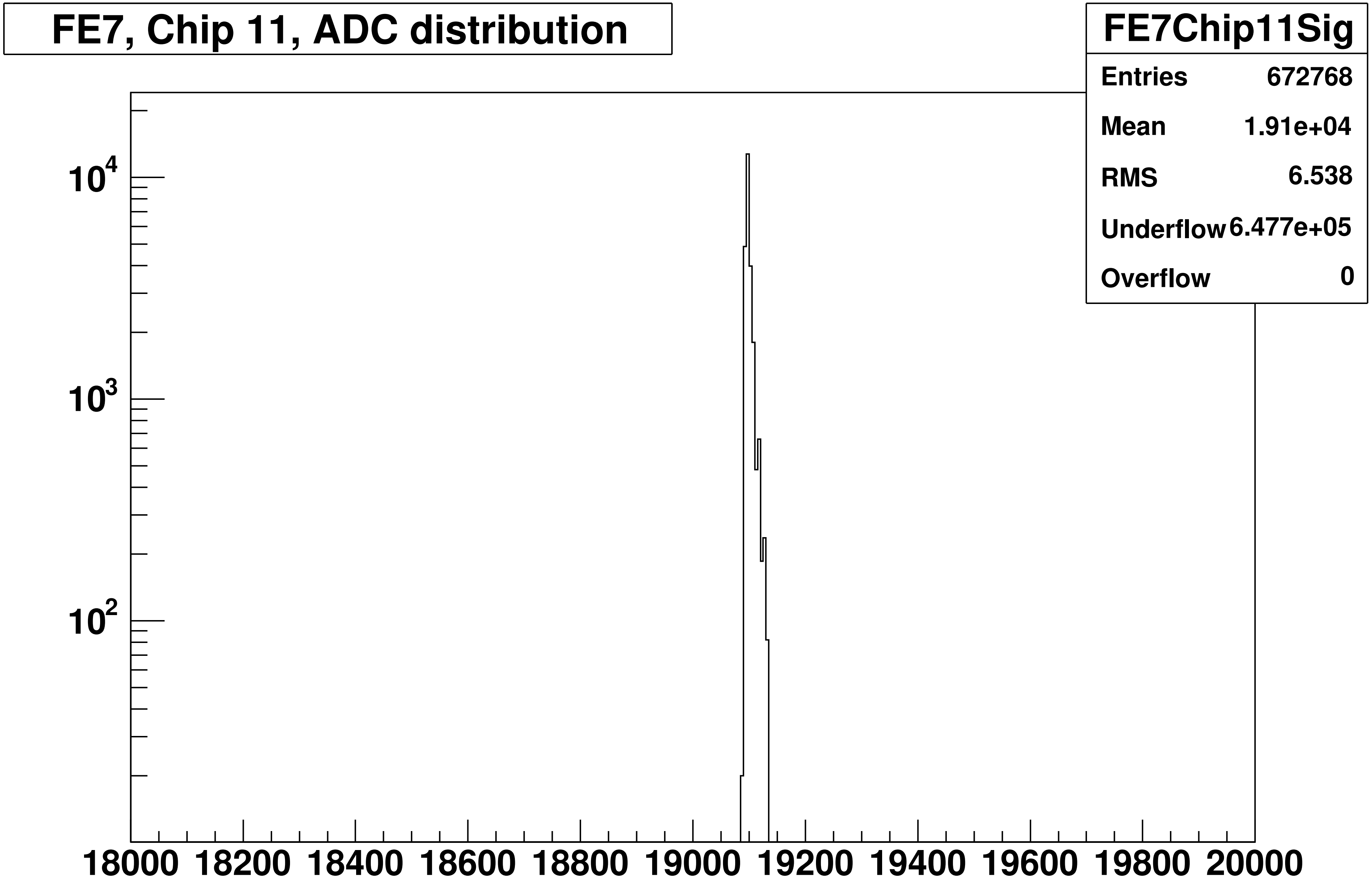

FE7, Chip 10, ADC distribution
FE7Chip10Ped
Entries 672768
Mean -5.276
RMS 1.299
Underflow 0
Overflow 2.507e+04
10
10^2
10^3
10^4
10^5
-200
-150
-100
-50
0
50
100
150
200


FE7, Chip 10, ADC distribution
FE7Chip10Sig
Entries 672768
Mean 1.903e+04
RMS 7.329
Underflow 6.477e+05
Overflow 0
10^4
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000

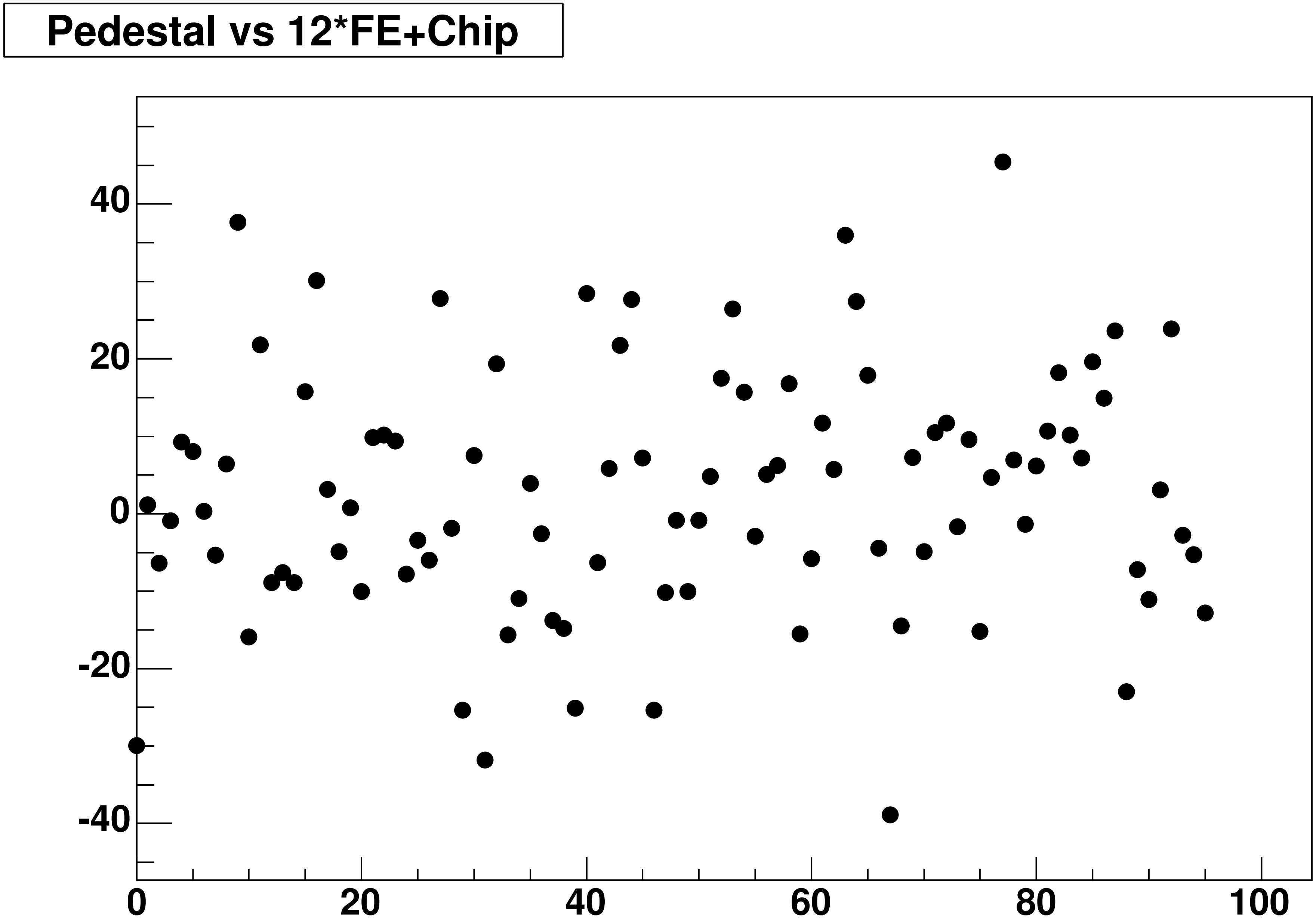


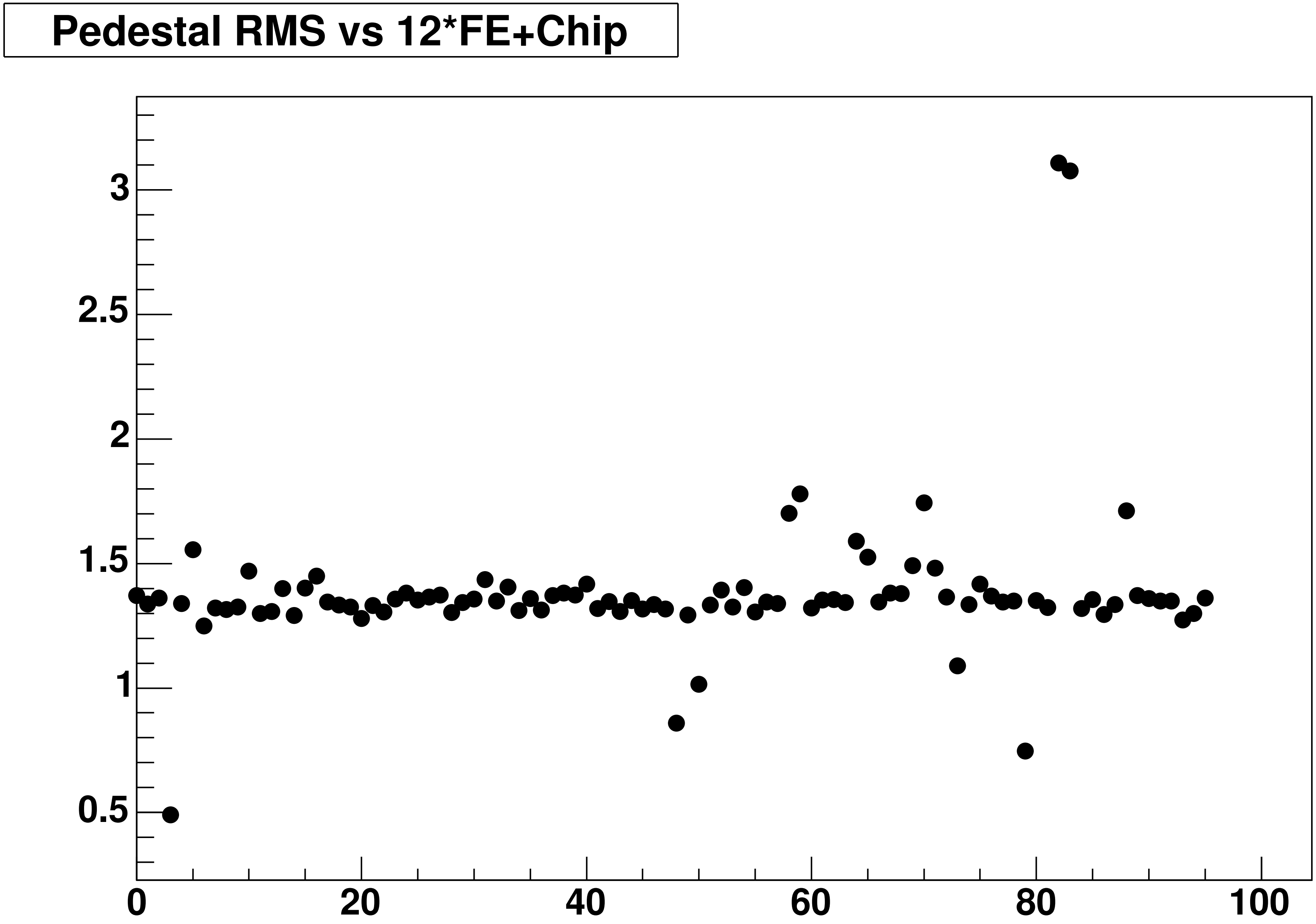
FE7, Chip 11, ADC distribution
FE7Chip11All
Entries 672768
Mean 699.5
RMS 3620
Underflow 0
Overflow 0
10^6
10^5
10^4
-5000
0
5000
10000
15000
20000
25000

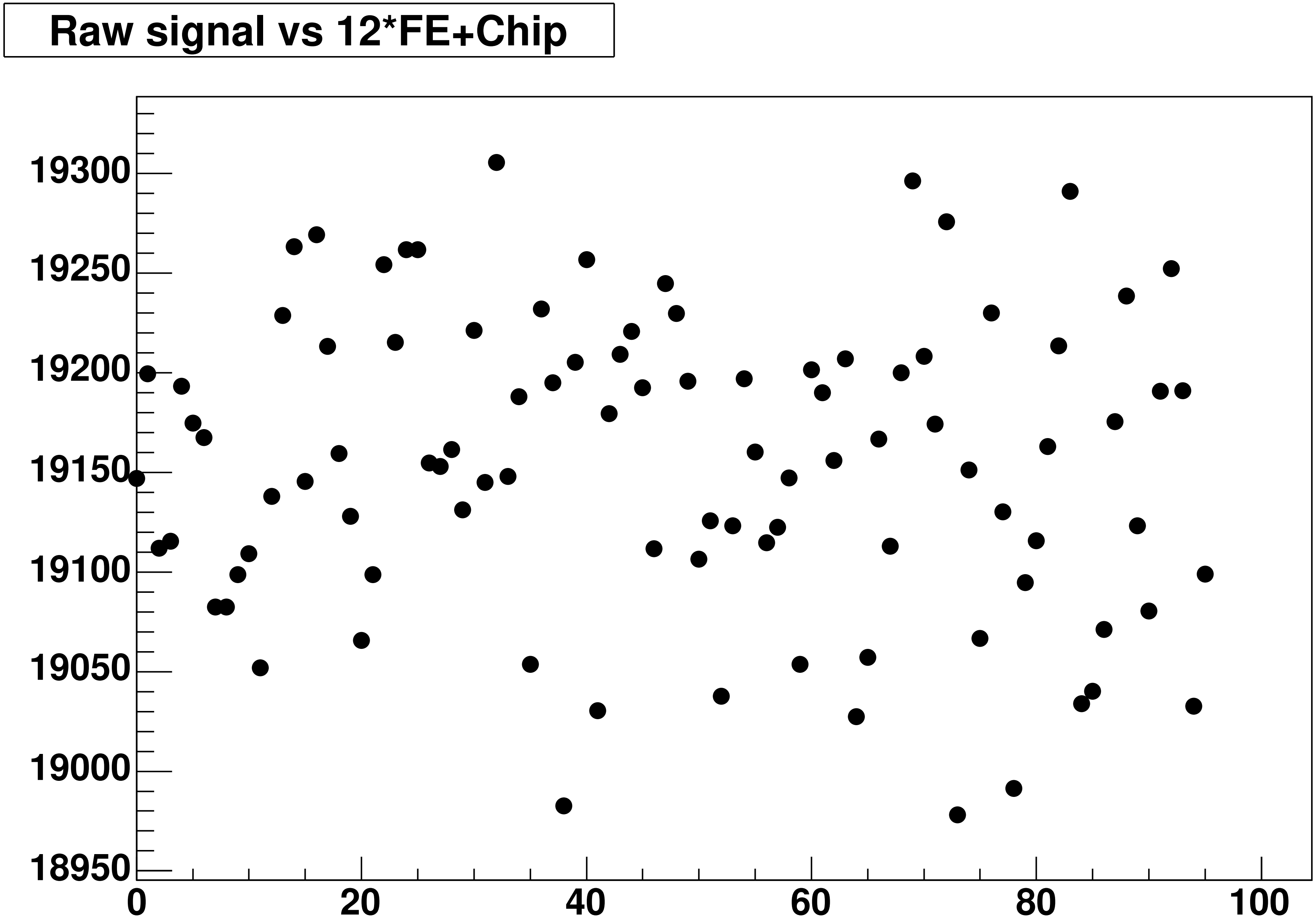

FE7, Chip 11, ADC distribution
FE7Chip11Ped
Entries 672768
Mean -12.79
RMS 1.362
Underflow 0
Overflow 2.507e+04
10^5
10^4
10^3
10^2
-200
-150
-100
-50
0
50
100
150
200

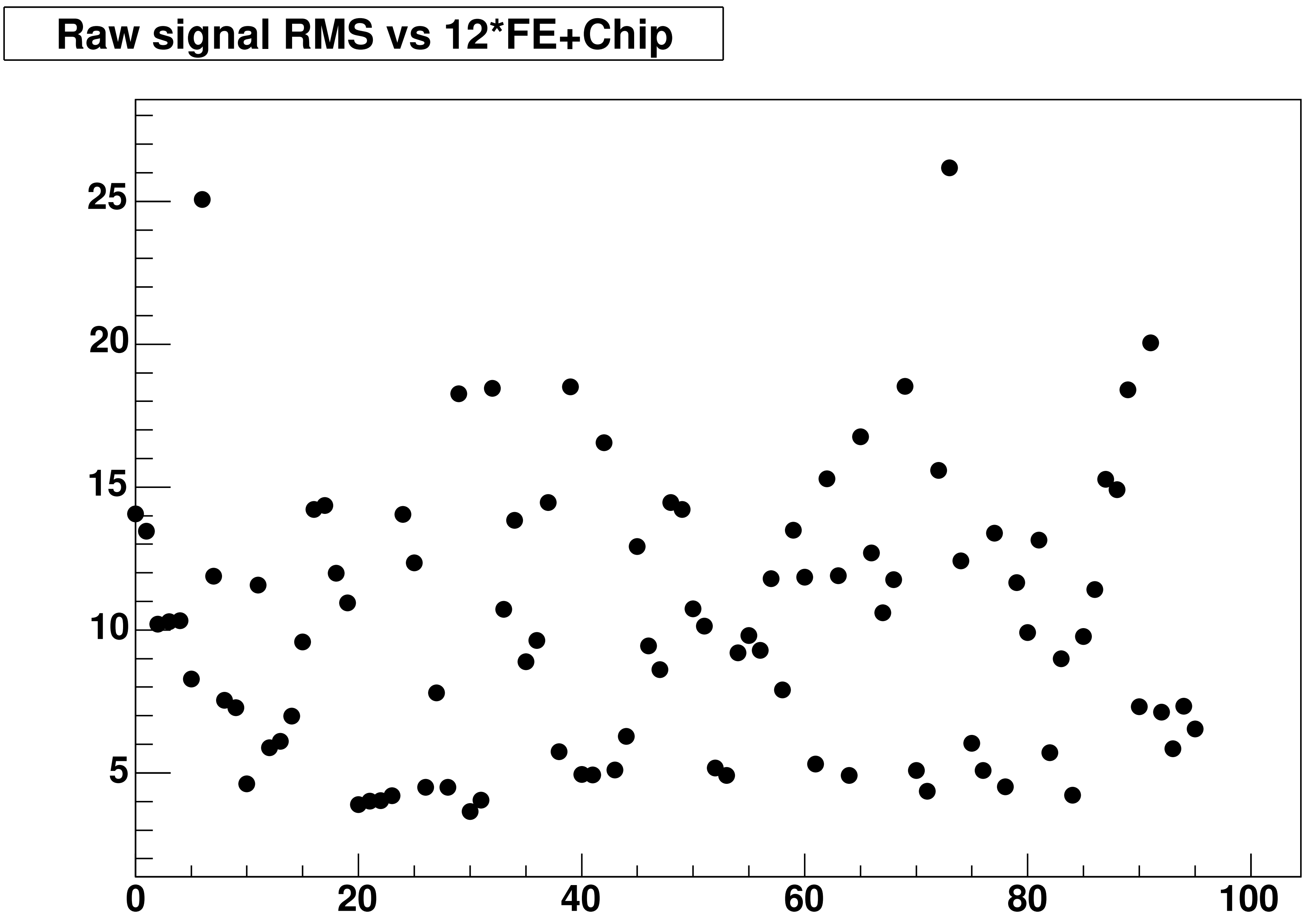


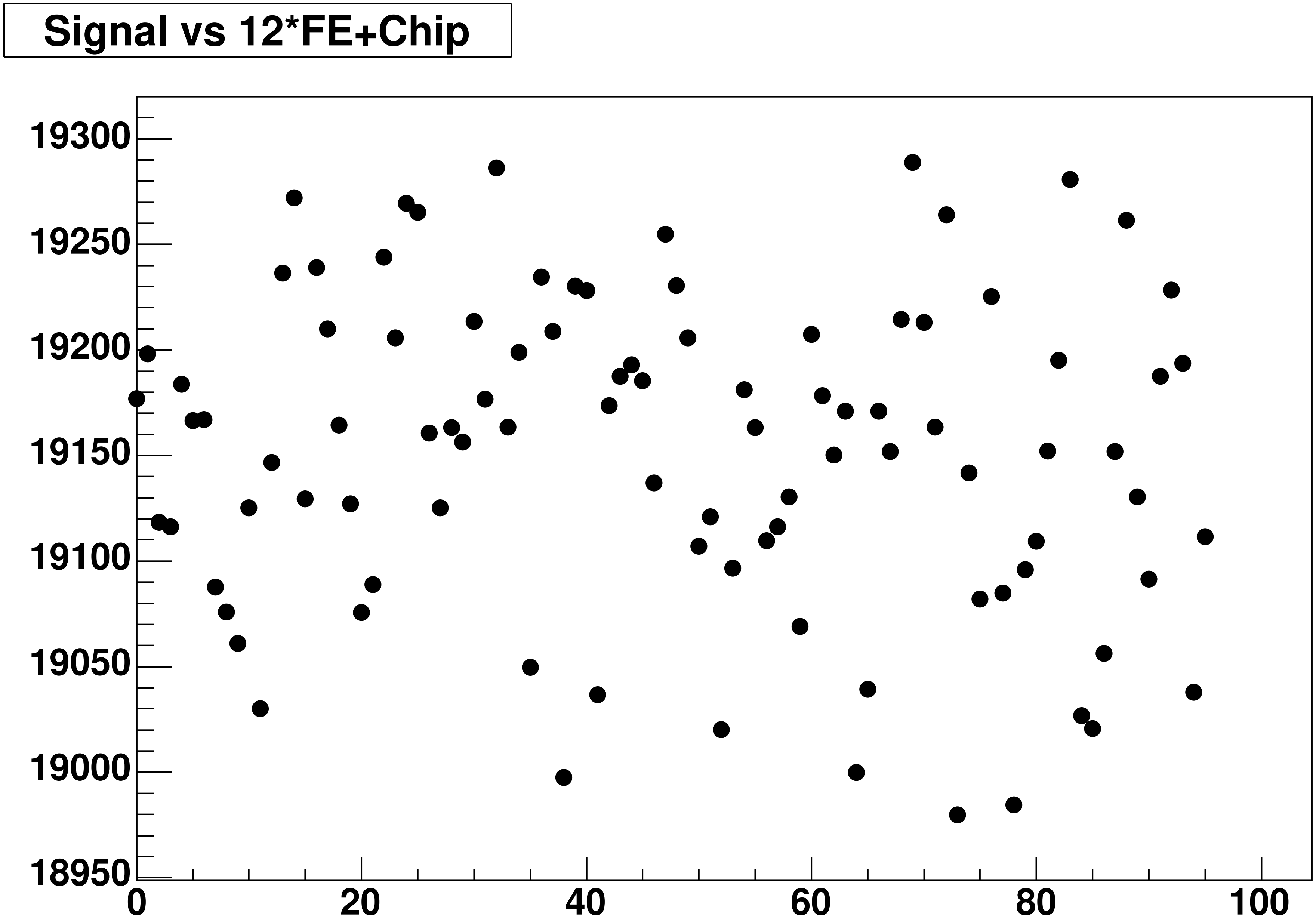
FE7, Chip 11, ADC distribution
FE7Chip11Sig
Entries 672768
Mean 1.91e+04
RMS 6.538
Underflow 6.477e+05
Overflow 0
10^4
10^3
10^2
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


Pedestal vs 12*FE+Chip
40
20
0
-20
-40
0
20
40
60
80
100

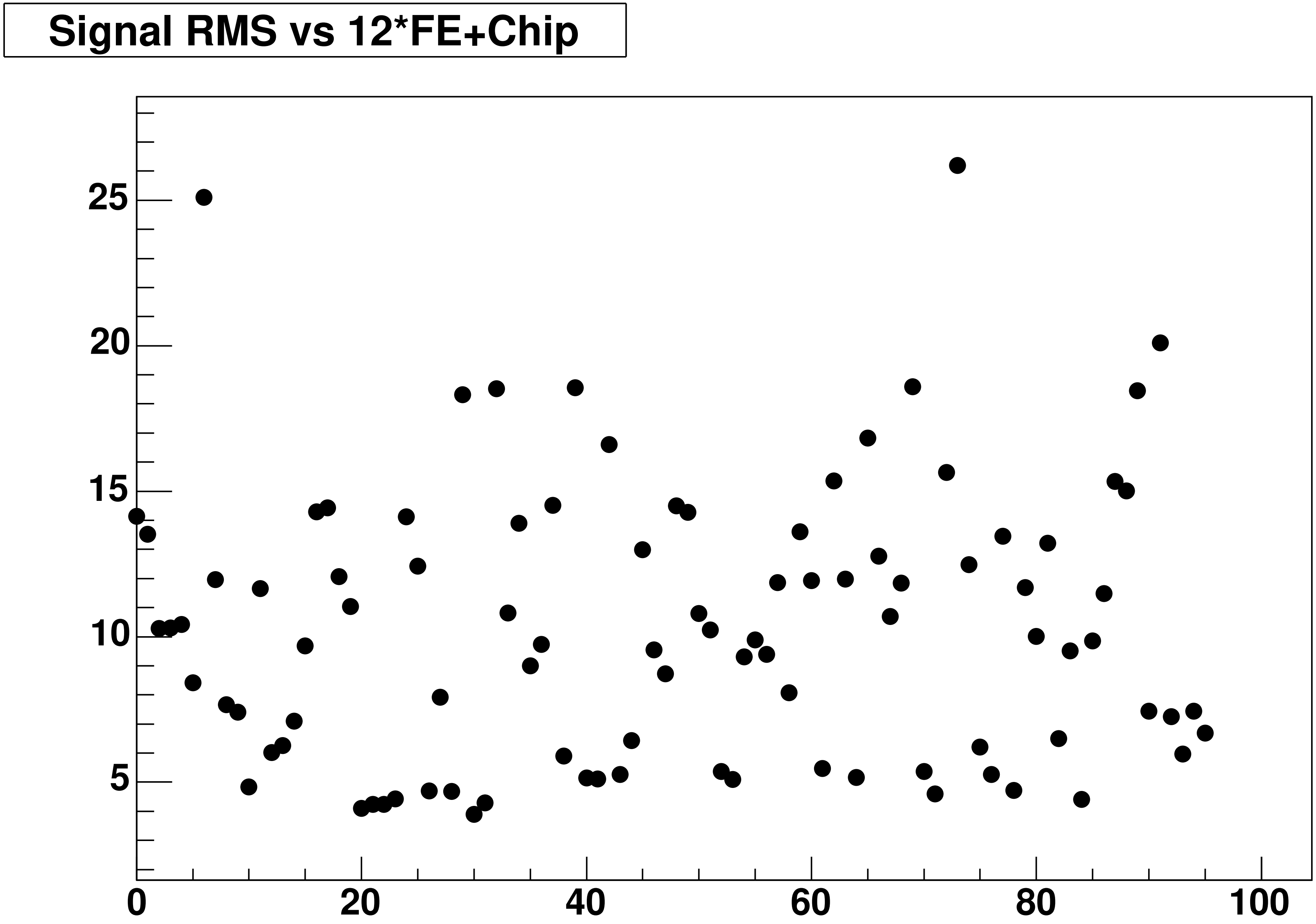

Pedestal RMS vs 12*FE+Chip
3
2.5
2
1.5
1
0.5
0
20
40
60
80
100


Raw signal vs 12*FE+Chip
19300
19250
19200
19150
19100
19050
19000
18950
0
20
40
60
80
100


Raw signal RMS vs 12*FE+Chip
25
20
15
10
5
0
20
40
60
80
100



Signal vs 12*FE+Chip
19300
19250
19200
19150
19100
19050
19000
18950
0
20
40
60
80
100


Signal RMS vs 12*FE+Chip
25
20
15
10
5
0
20
40
60
80
100