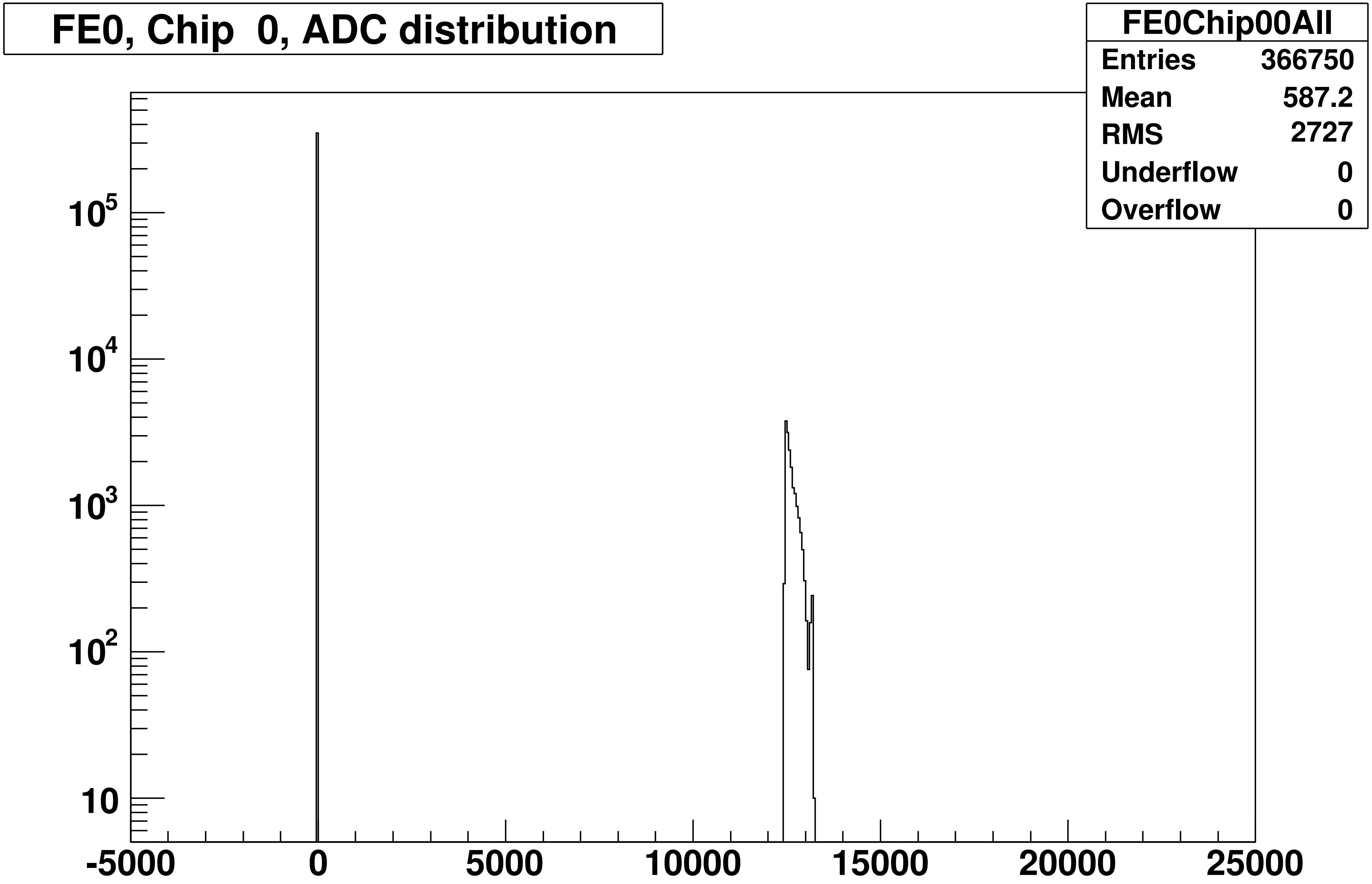
FE0, Chip 0, ADC distribution
FE0Chip00All
Entries 366750
Mean 587.2
RMS 2727
Underflow 0
Overflow 0
10
10^2
10^3
10^4
10^5
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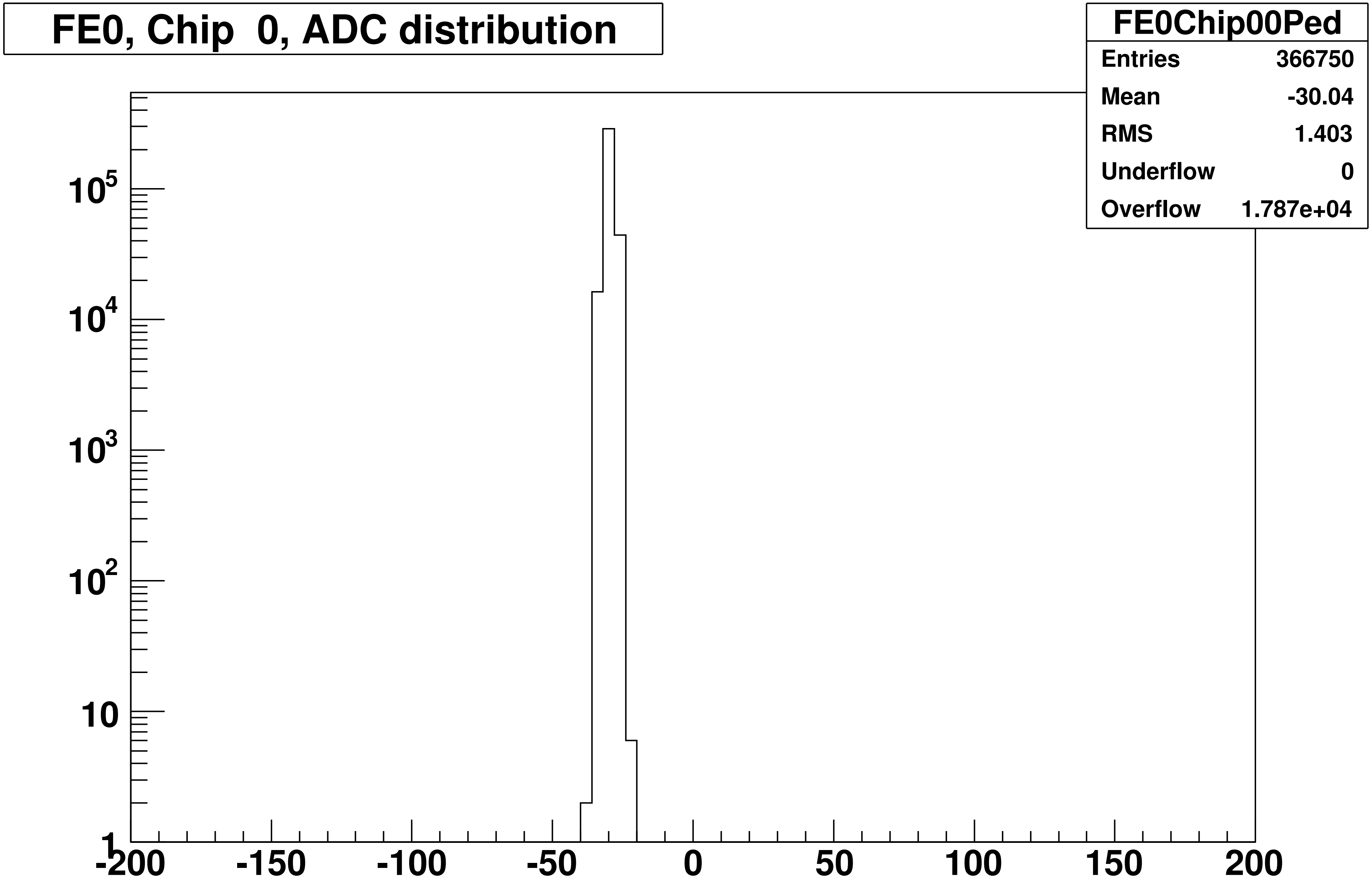
FE0, Chip 0, ADC distribution
FE0Chip00Ped
Entries 366750
Mean -30.04
RMS 1.403
Underflow 0
Overflow 1.787e+04
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10^3
10^2
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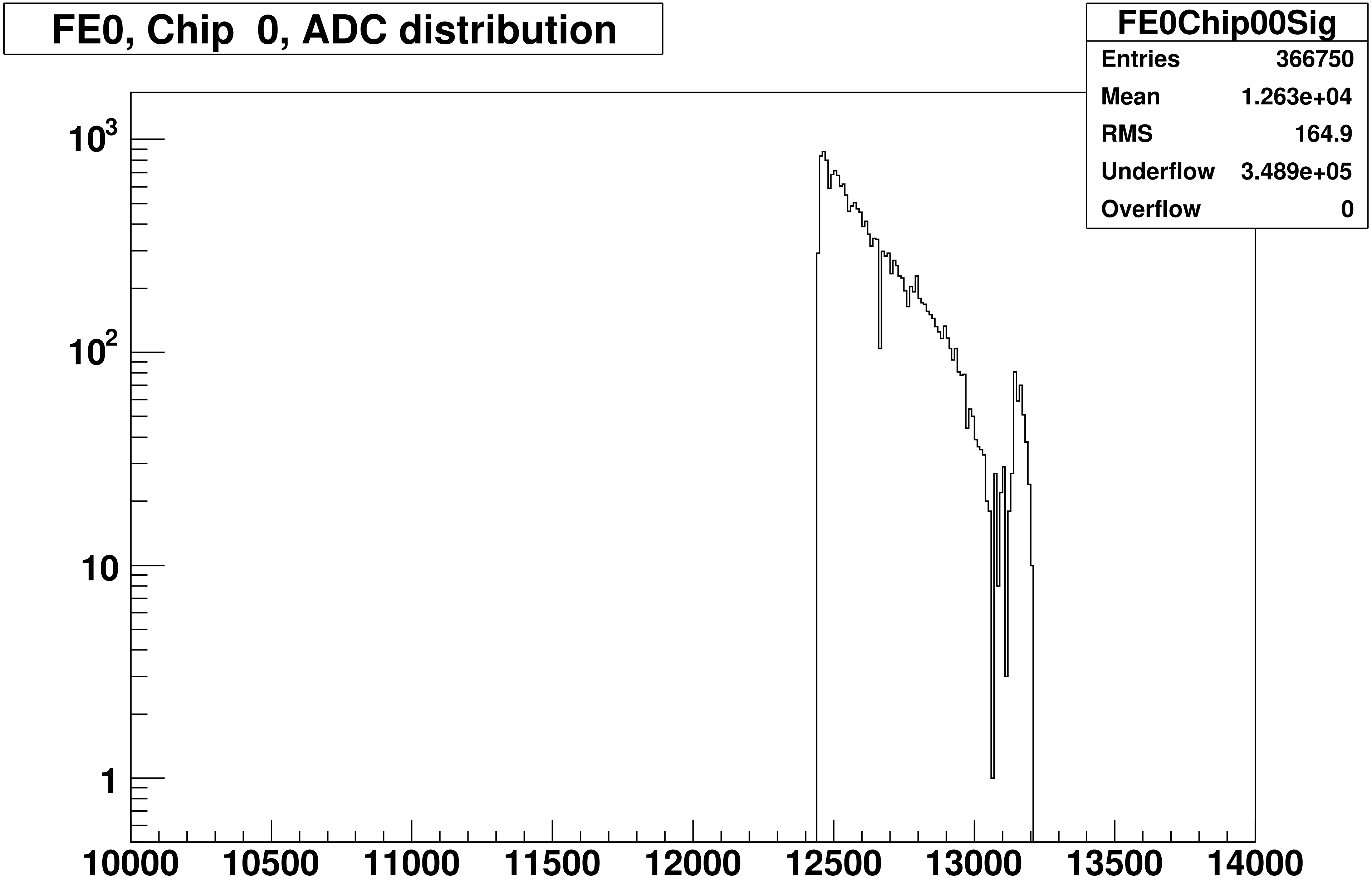
FE0, Chip 0, ADC distribution
FE0Chip00Sig
Entries 366750
Mean 1.263e+04
RMS 164.9
Underflow 3.489e+05
Overflow 0
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10^2
10
1
10000
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11500
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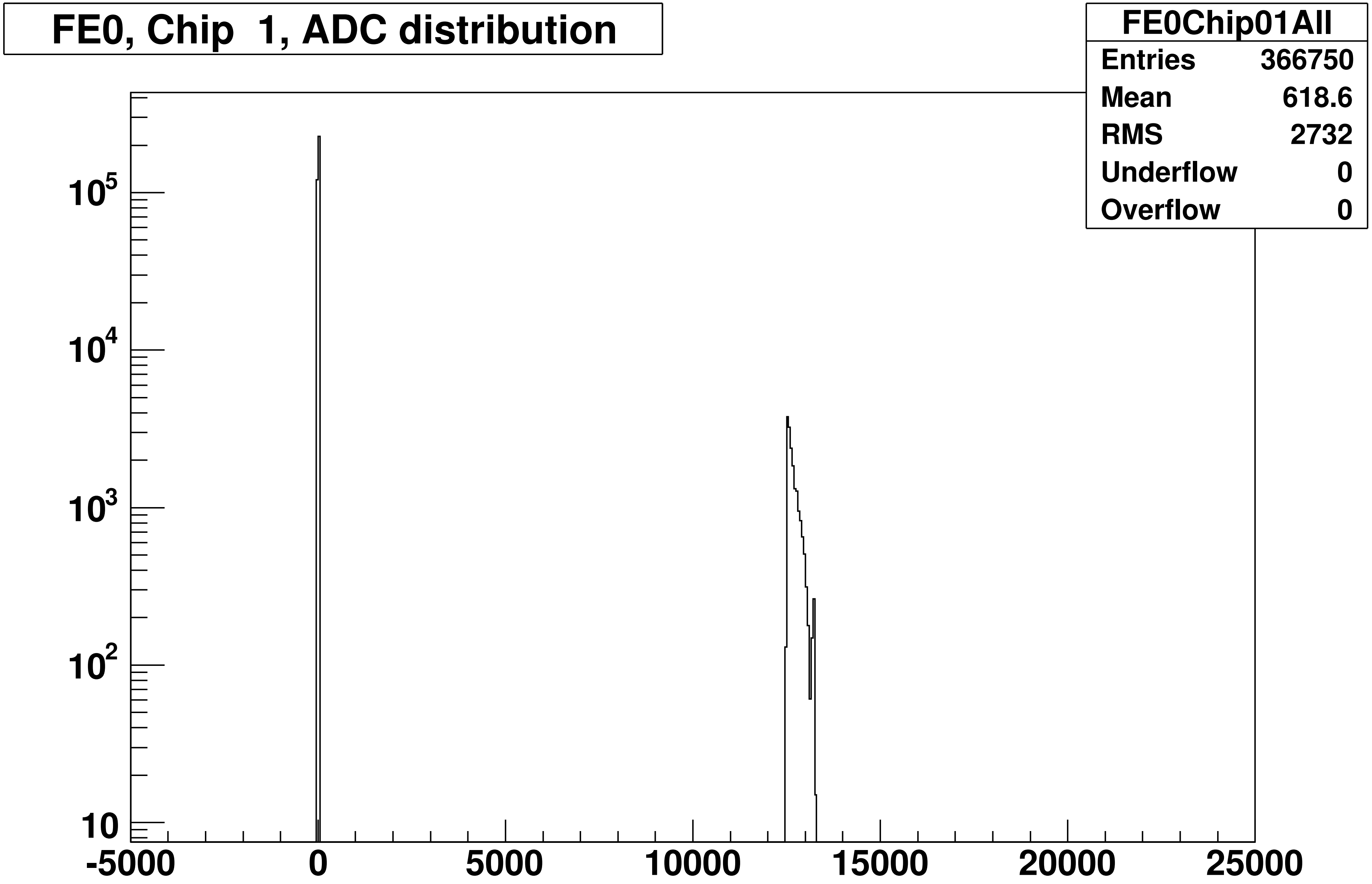
FE0, Chip 1, ADC distribution
FE0Chip01All
Entries 366750
Mean 618.6
RMS 2732
Underflow 0
Overflow 0
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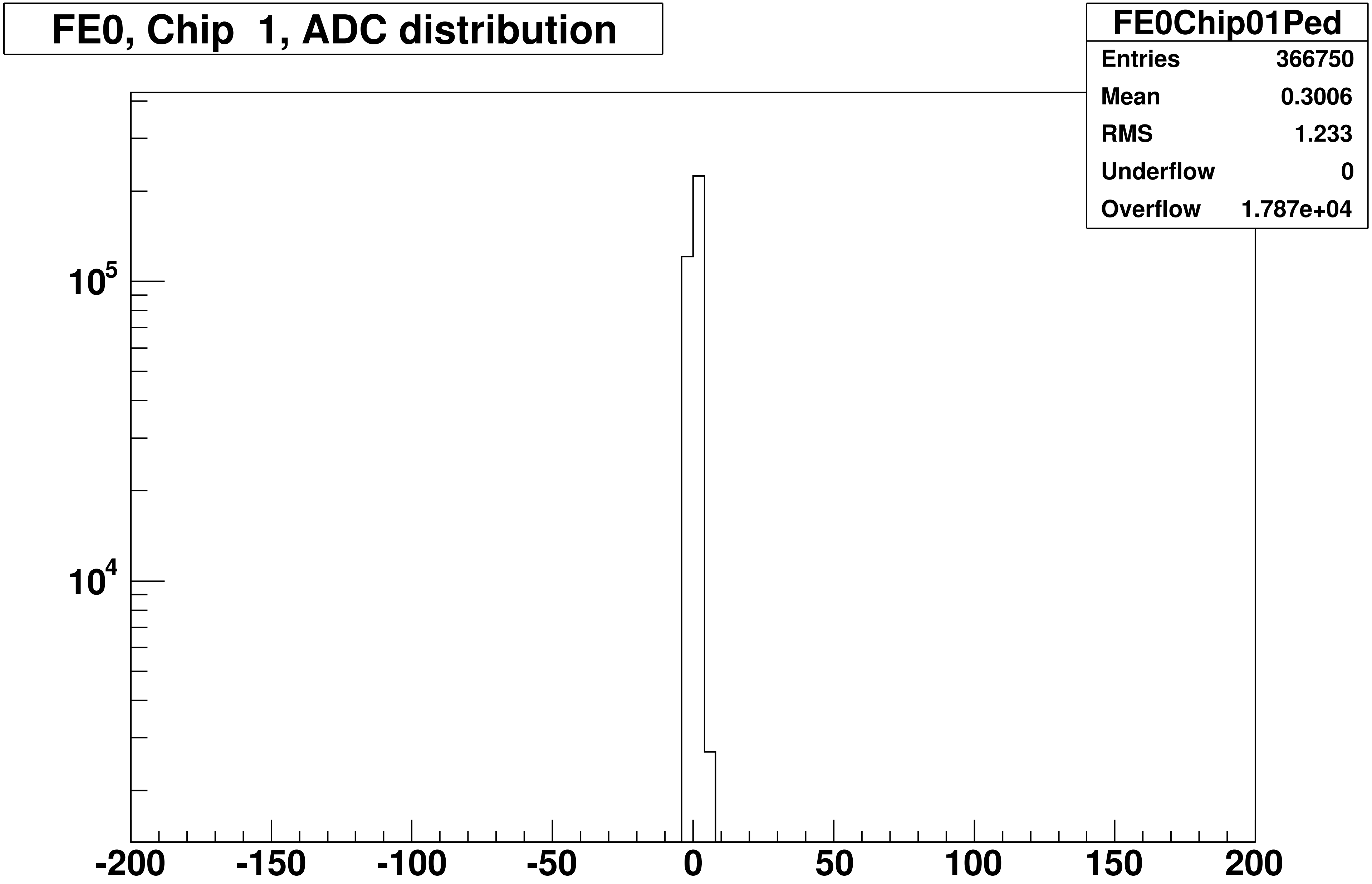
FE0, Chip 1, ADC distribution
FE0Chip01Ped
Entries 366750
Mean 0.3006
RMS 1.233
Underflow 0
Overflow 1.787e+04
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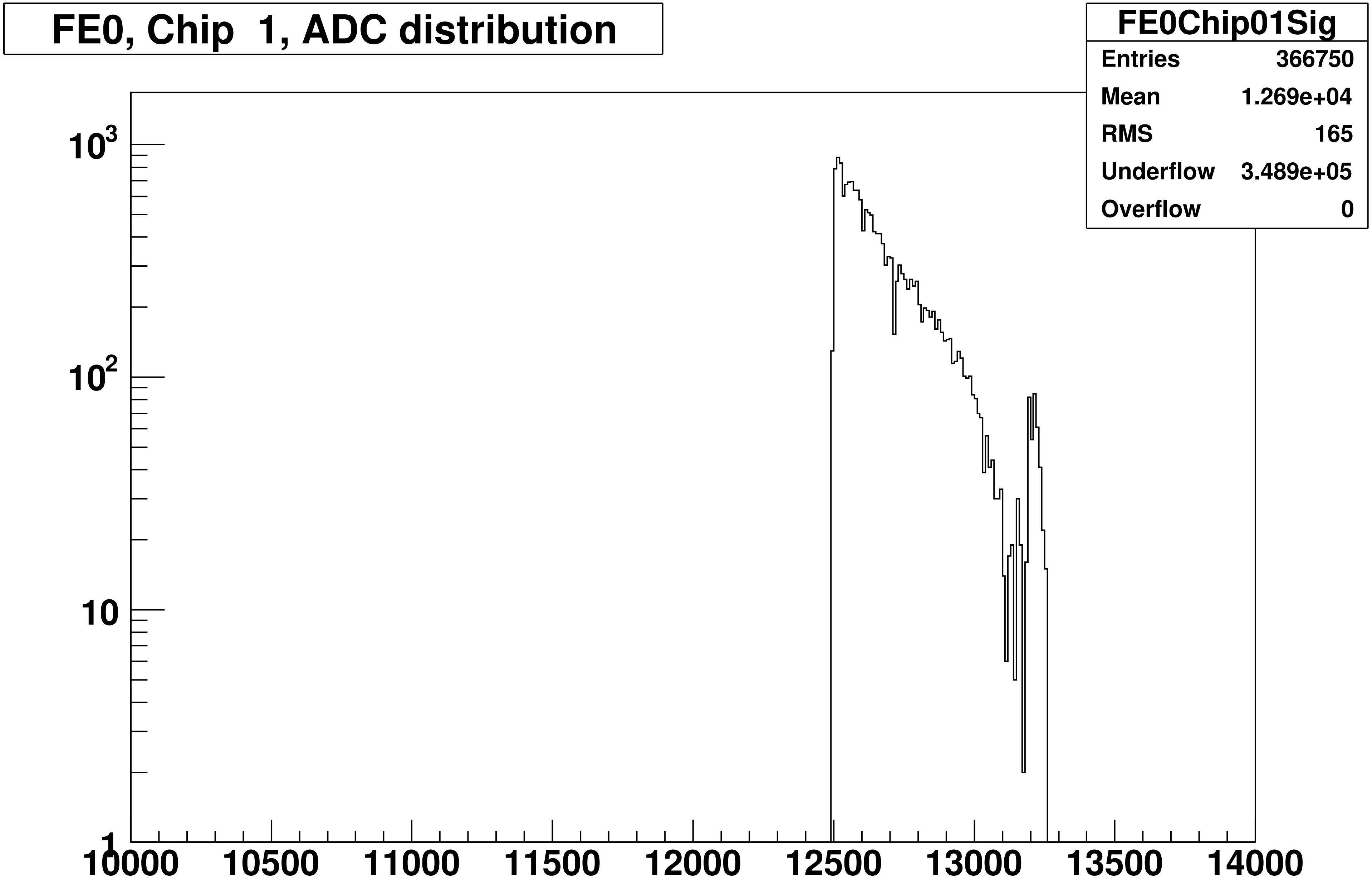
FE0, Chip 1, ADC distribution
FE0Chip01Sig
Entries 366750
Mean 1.269e+04
RMS 165
Underflow 3.489e+05
Overflow 0
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10
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11500
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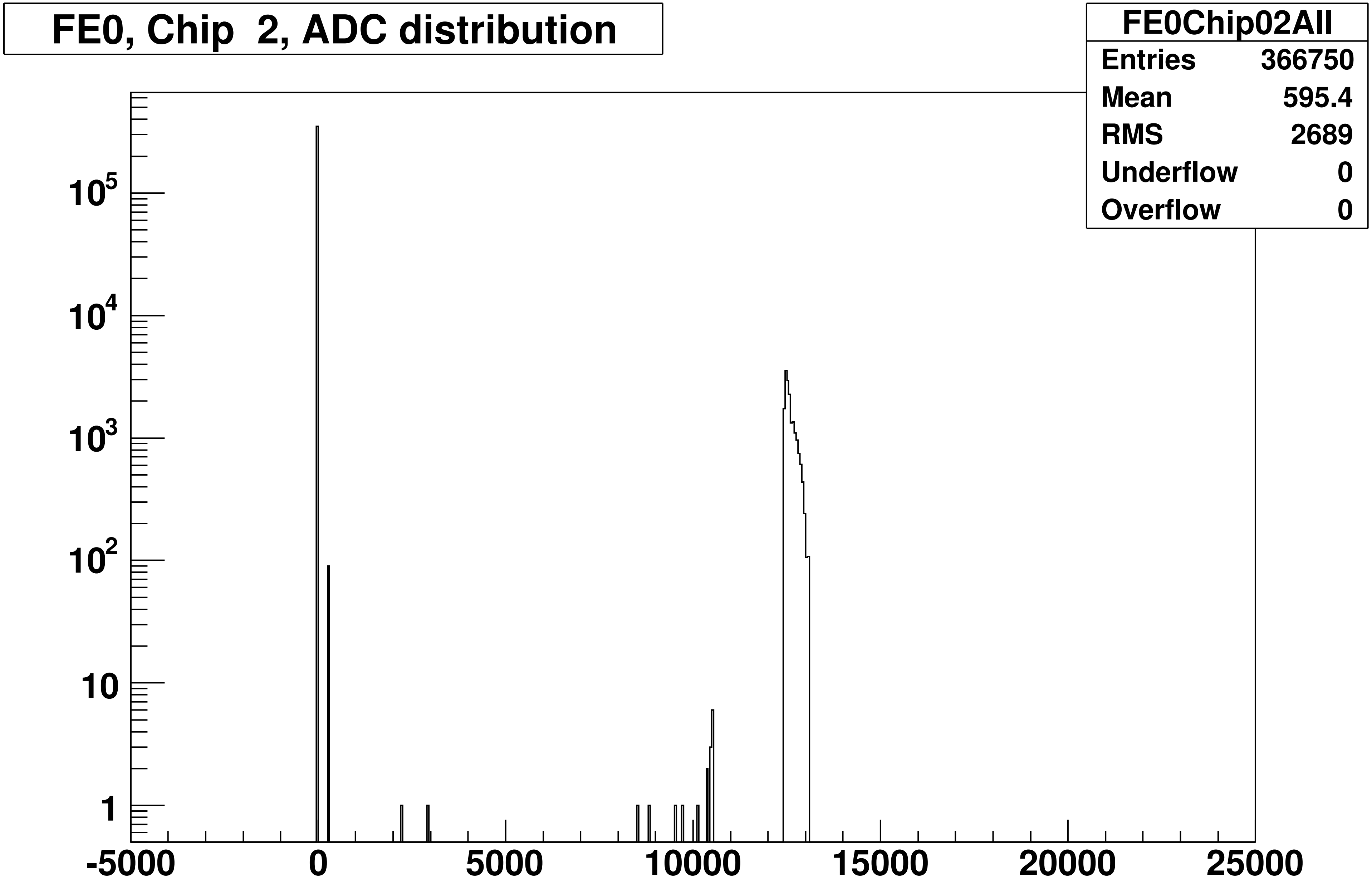
FE0, Chip 2, ADC distribution
FE0Chip02All
Entries 366750
Mean 595.4
RMS 2689
Underflow 0
Overflow 0
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10^4
10^3
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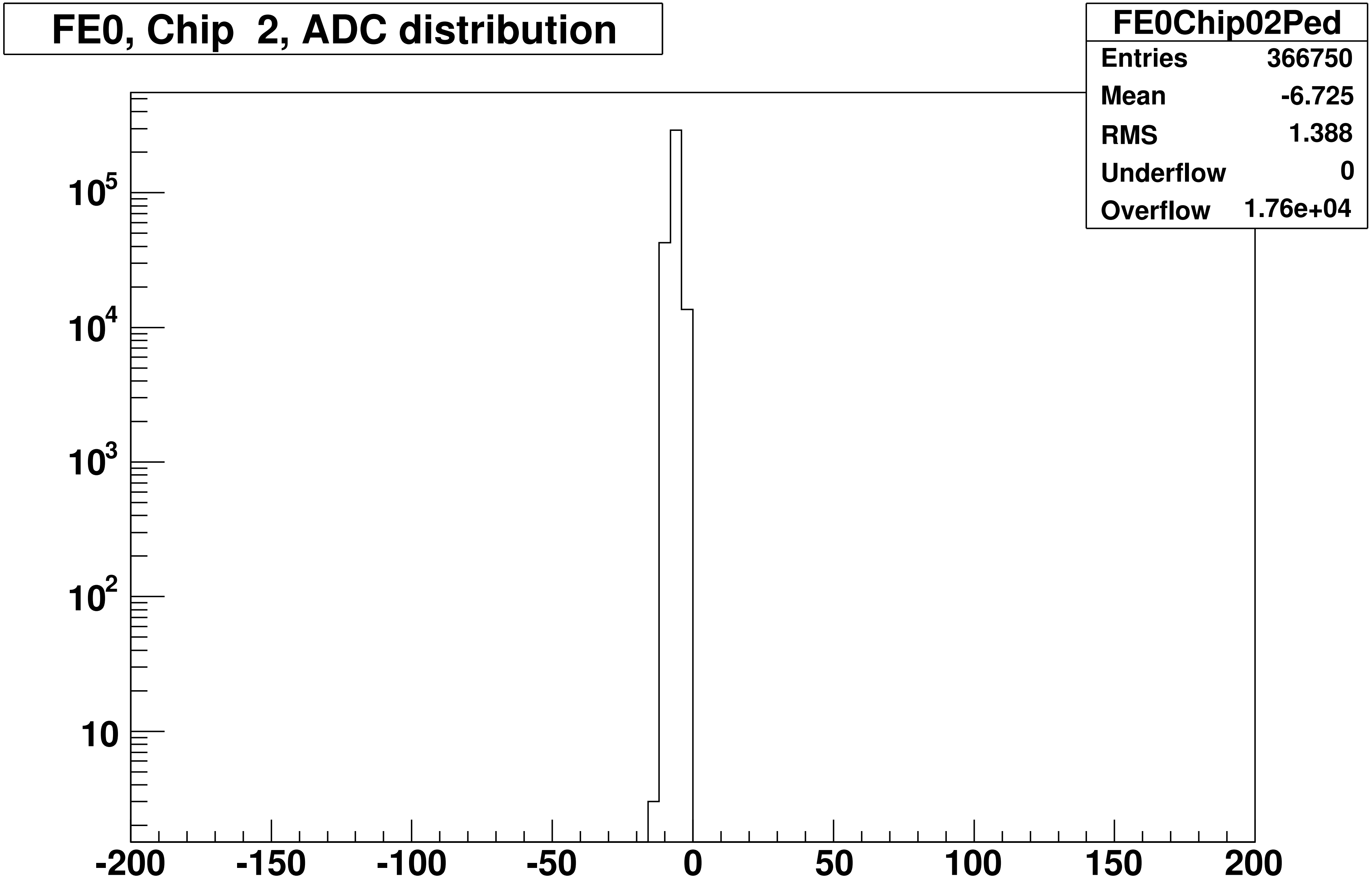
FE0, Chip 2, ADC distribution
FE0Chip02Ped
Entries 366750
Mean -6.725
RMS 1.388
Underflow 0
Overflow 1.76e+04
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150
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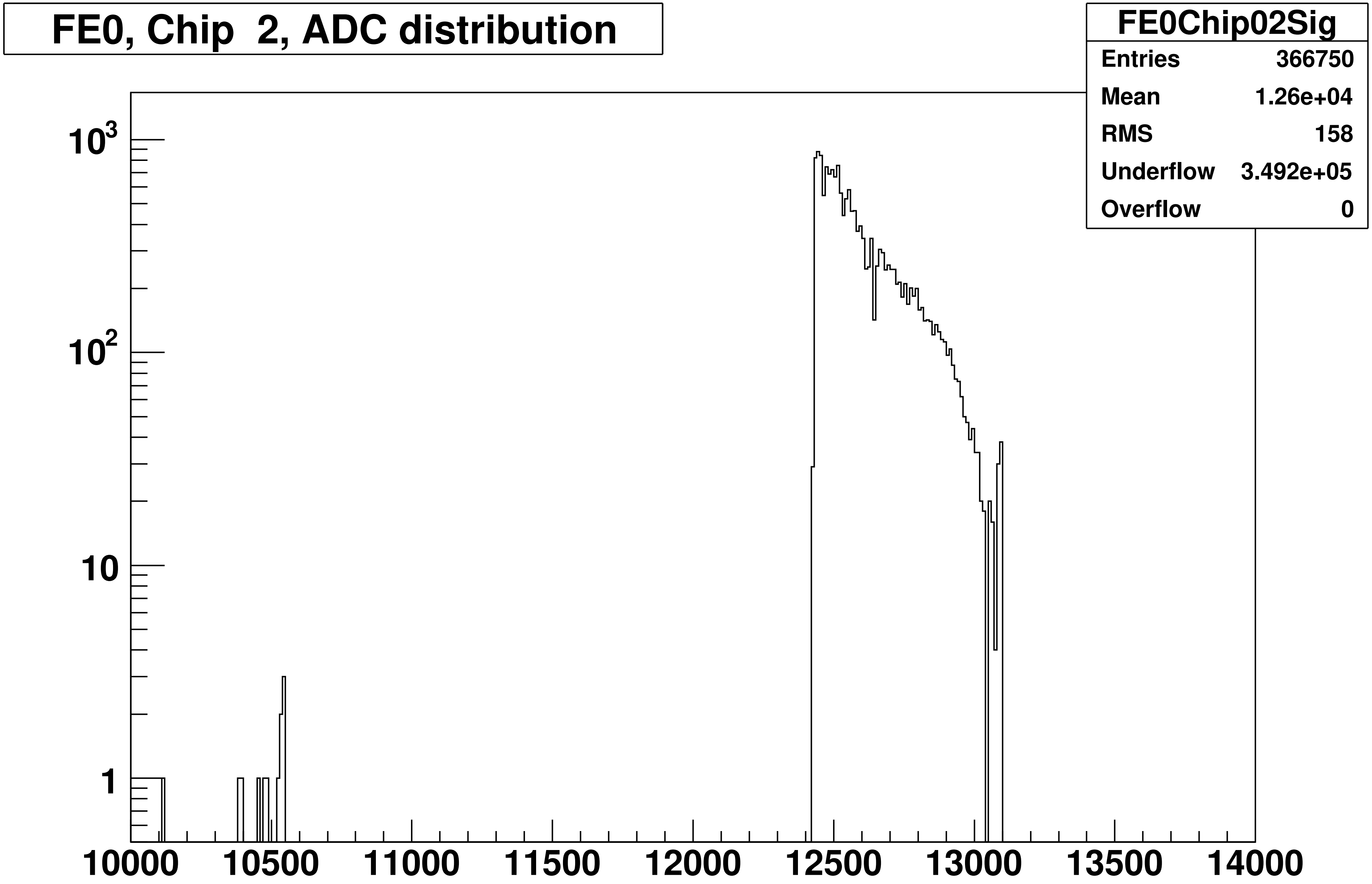
FE0, Chip 2, ADC distribution
FE0Chip02Sig
Entries 366750
Mean 1.26e+04
RMS 158
Underflow 3.492e+05
Overflow 0
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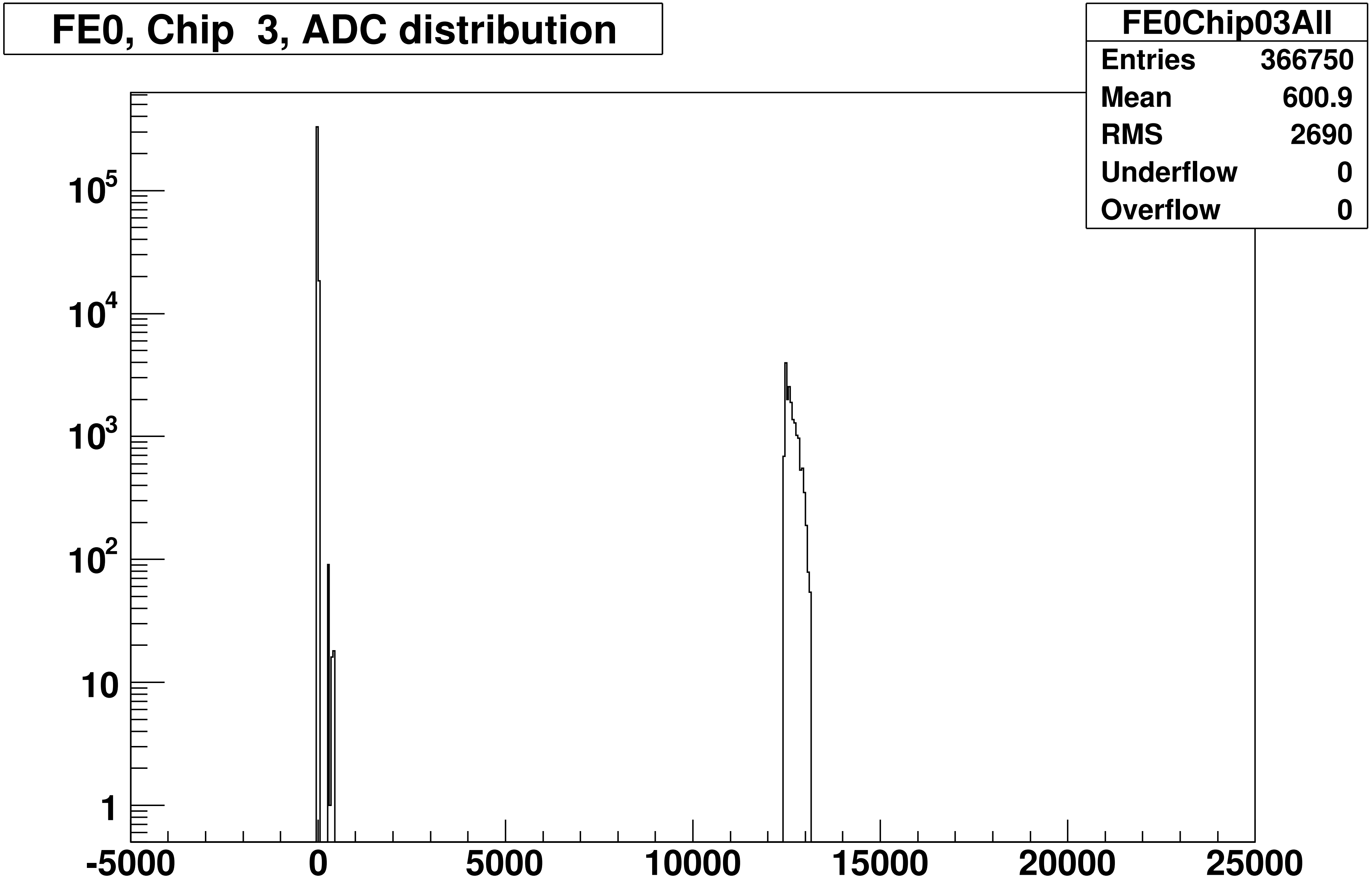
FE0, Chip 3, ADC distribution
FE0Chip03All
Entries 366750
Mean 600.9
RMS 2690
Underflow 0
Overflow 0
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10^4
10^3
10^2
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20000
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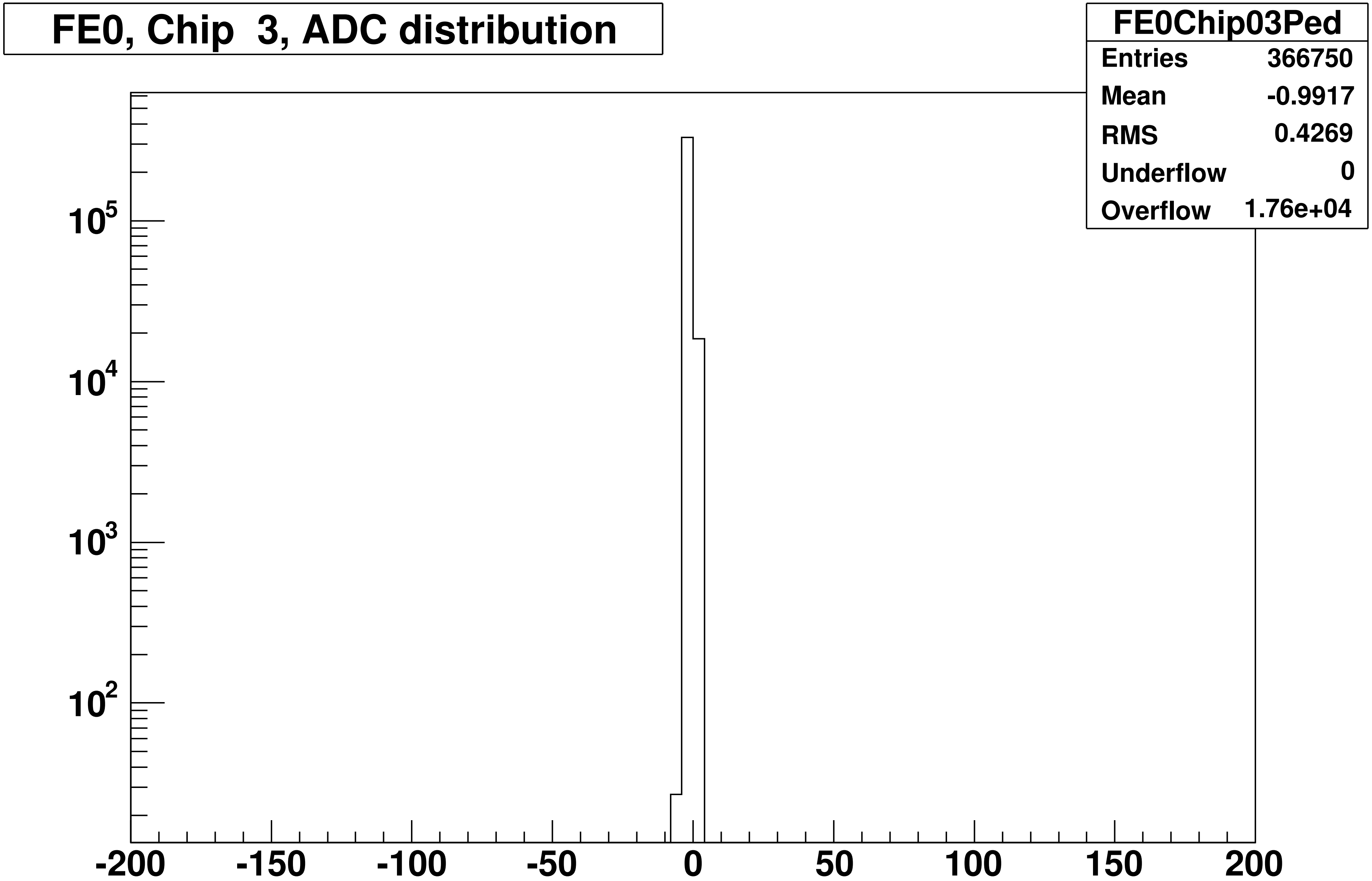
FE0, Chip 3, ADC distribution
FE0Chip03Ped
Entries 366750
Mean -0.9917
RMS 0.4269
Underflow 0
Overflow 1.76e+04
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10^3
10^2
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150
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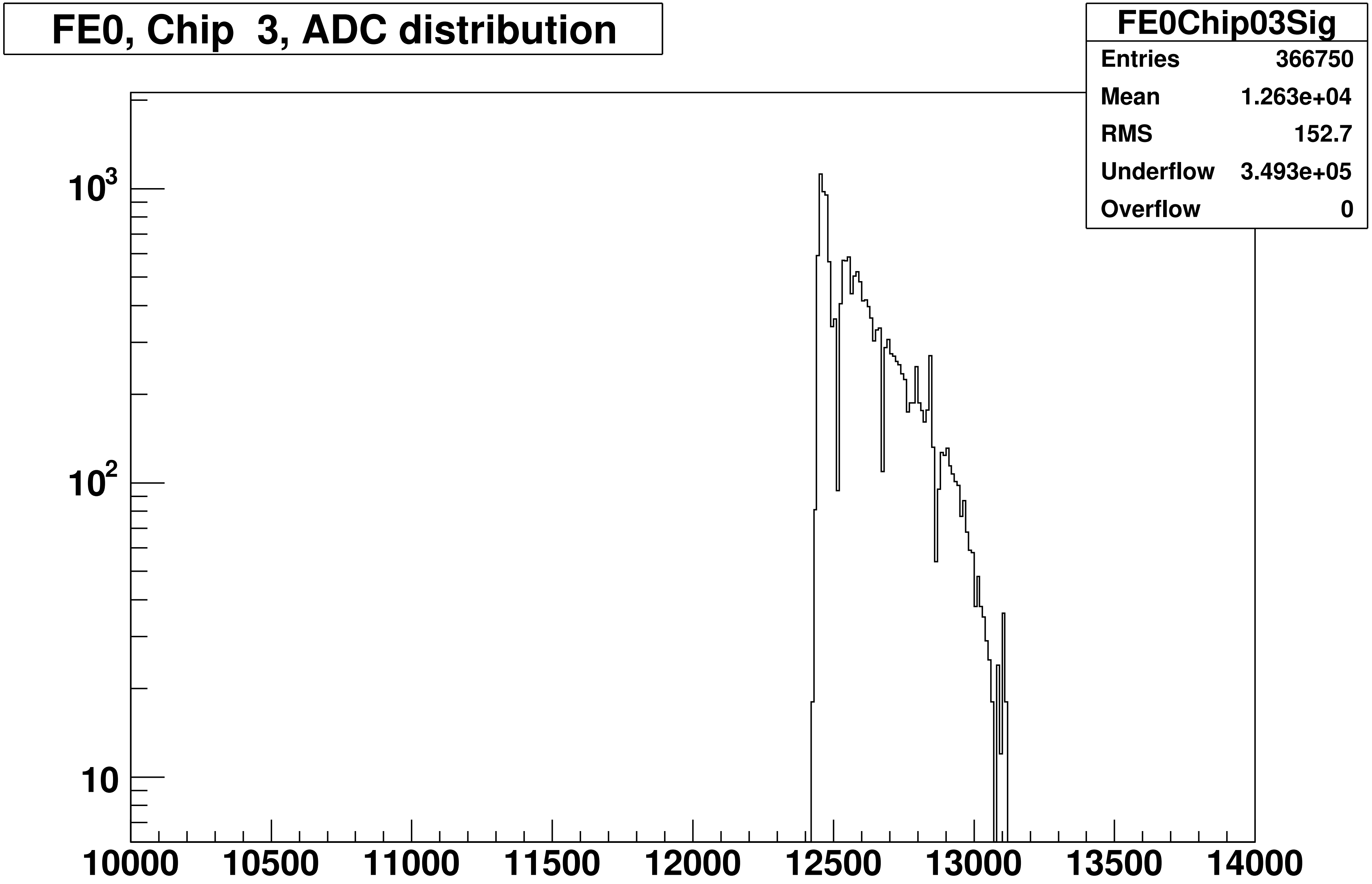
FE0, Chip 3, ADC distribution
FE0Chip03Sig
Entries 366750
Mean 1.263e+04
RMS 152.7
Underflow 3.493e+05
Overflow 0
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10^2
10
10000
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11500
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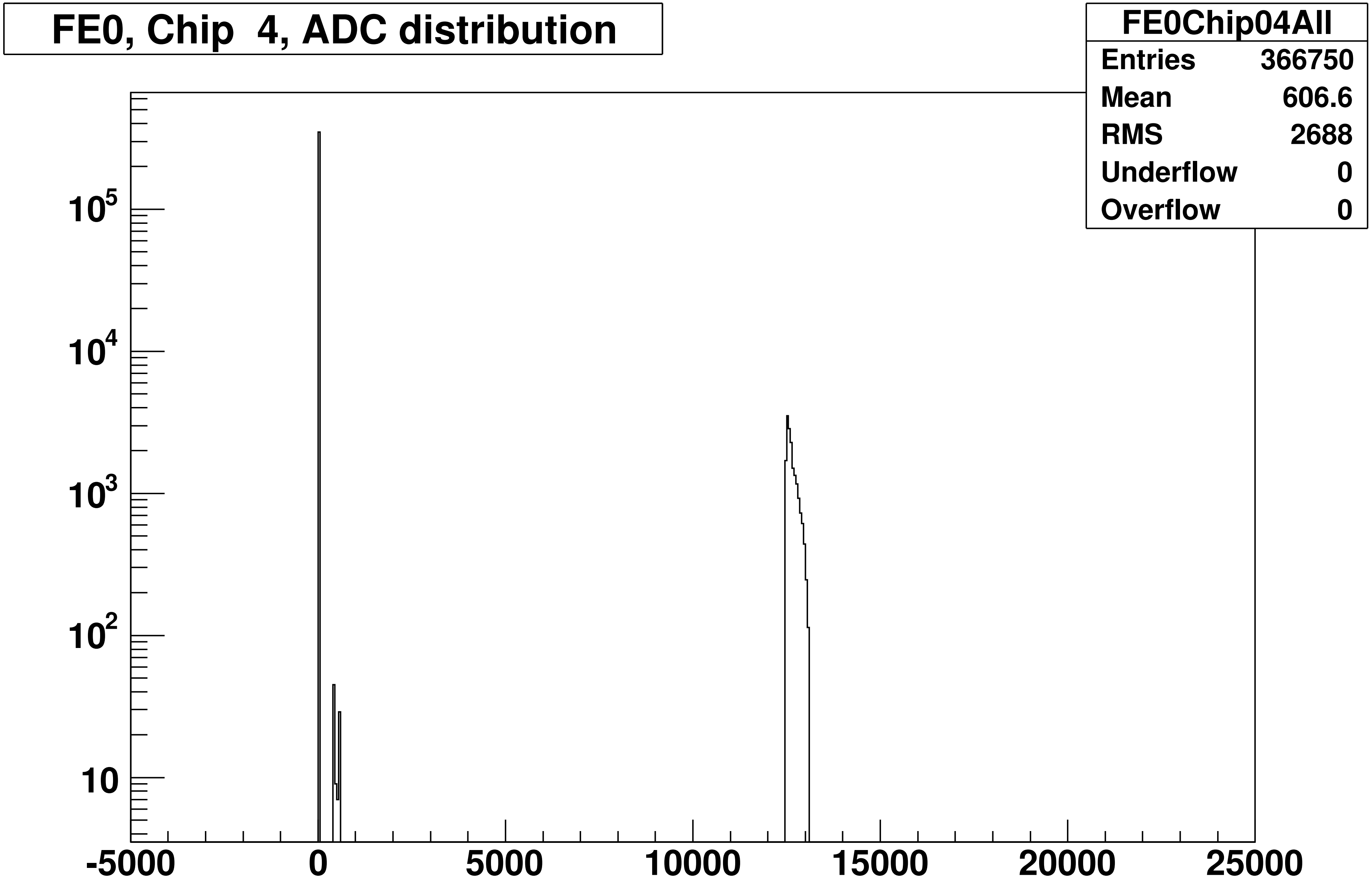
FE0, Chip 4, ADC distribution
FE0Chip04All
Entries 366750
Mean 606.6
RMS 2688
Underflow 0
Overflow 0
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10^4
10^3
10^2
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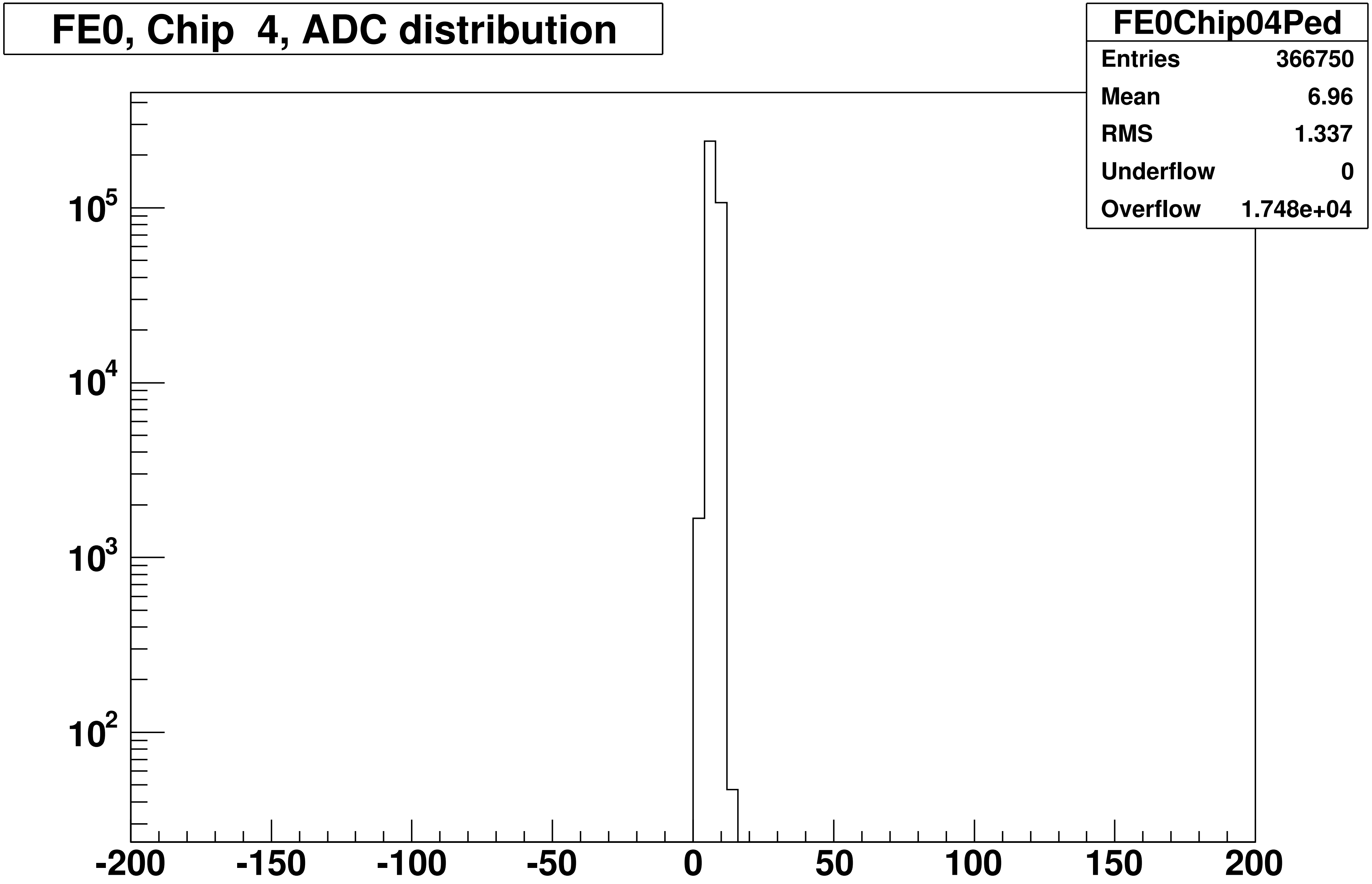
-5000
0
5000
10000
15000
20000
25000


FE0, Chip 4, ADC distribution
FE0Chip04Ped
Entries 366750
Mean 6.96
RMS 1.337
Underflow 0
Overflow 1.748e+04
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50
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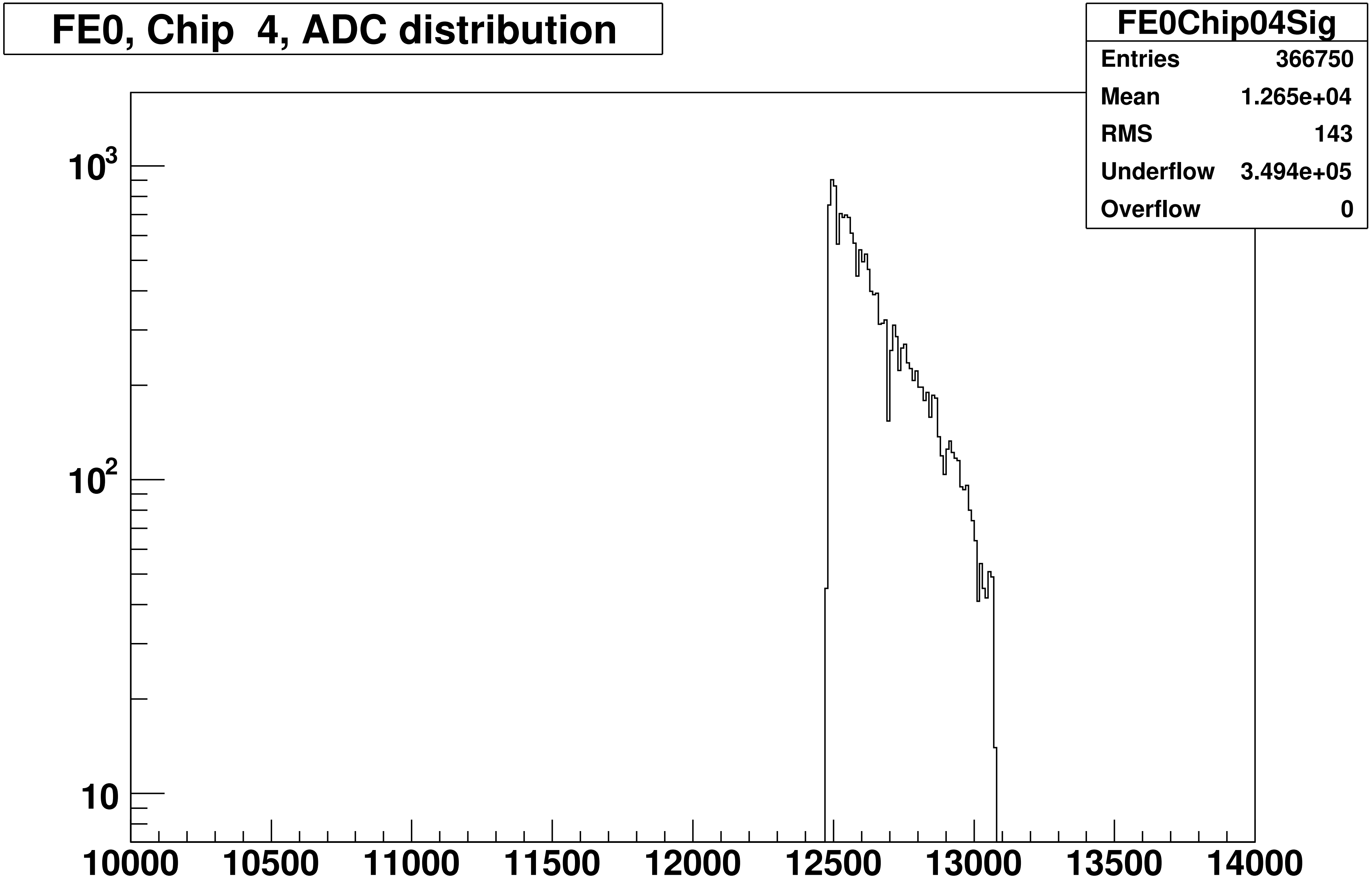
150
200


FE0, Chip 4, ADC distribution
FE0Chip04Sig
Entries 366750
Mean 1.265e+04
RMS 143
Underflow 3.494e+05
Overflow 0
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10^2
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10000
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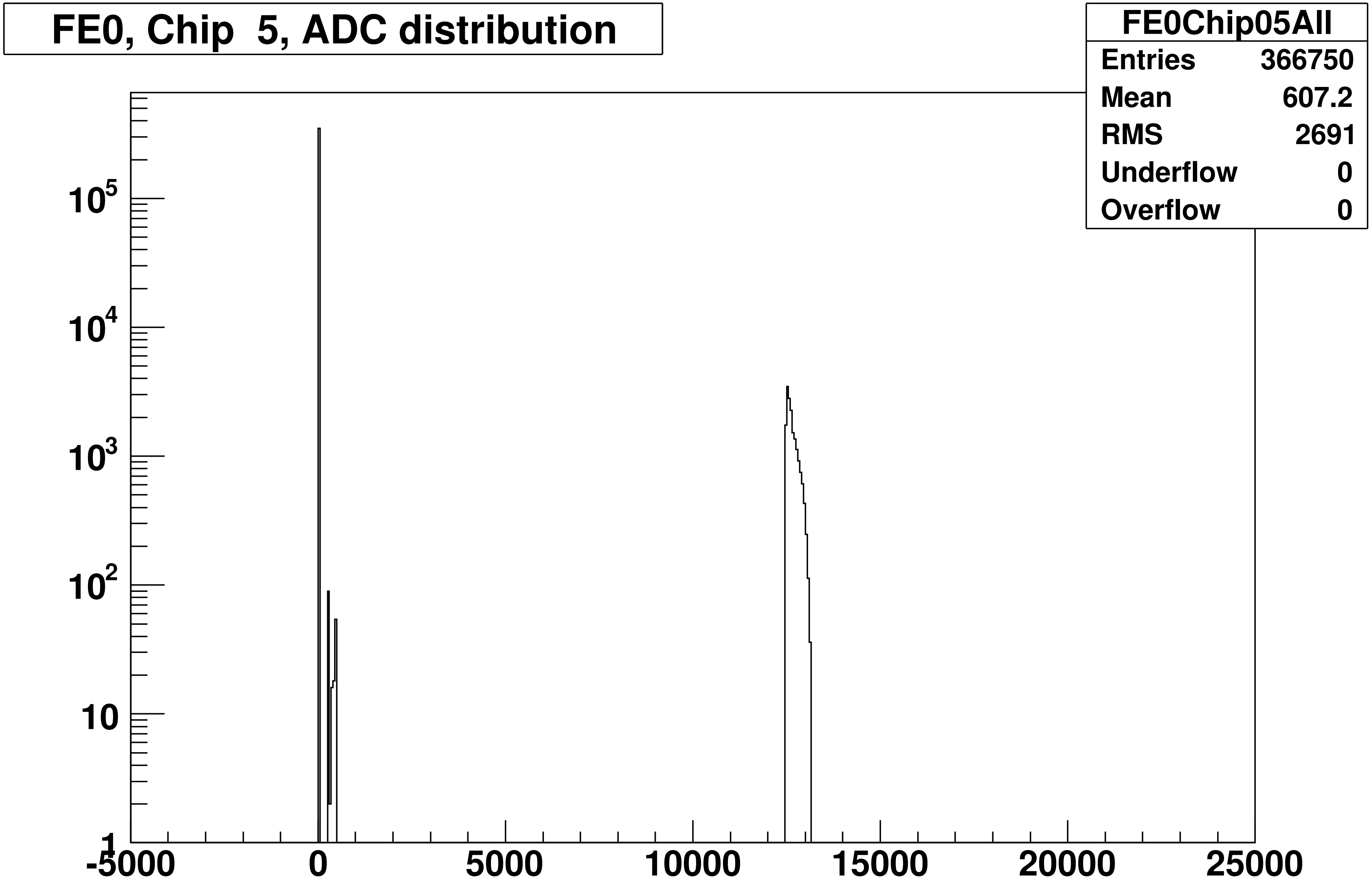
FE0, Chip 5, ADC distribution
FE0Chip05All
Entries 366750
Mean 607.2
RMS 2691
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
1
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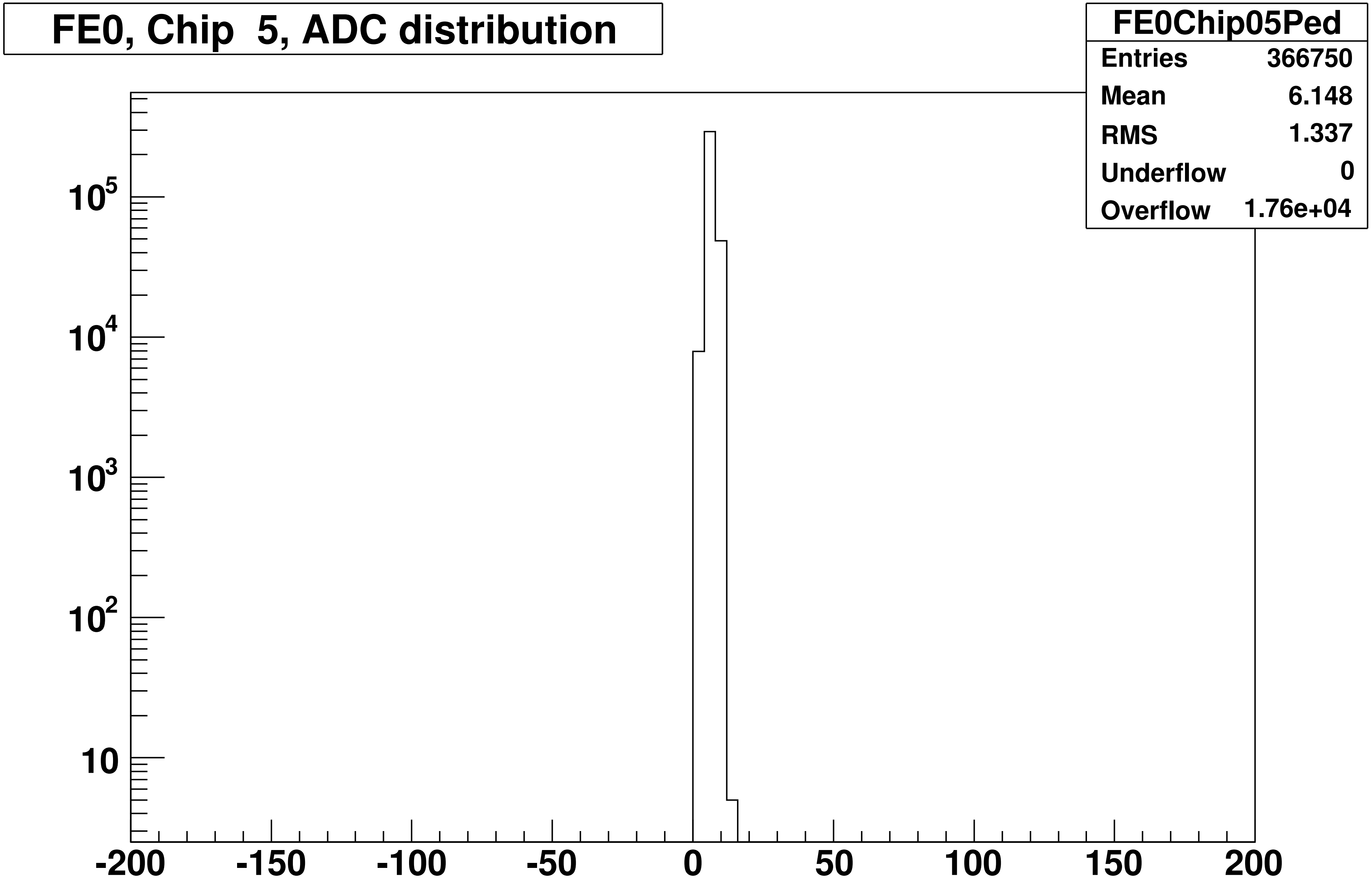
15000
20000
25000


FE0, Chip 5, ADC distribution
FE0Chip05Ped
Entries 366750
Mean 6.148
RMS 1.337
Underflow 0
Overflow 1.76e+04
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10^4
10^3
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100
150
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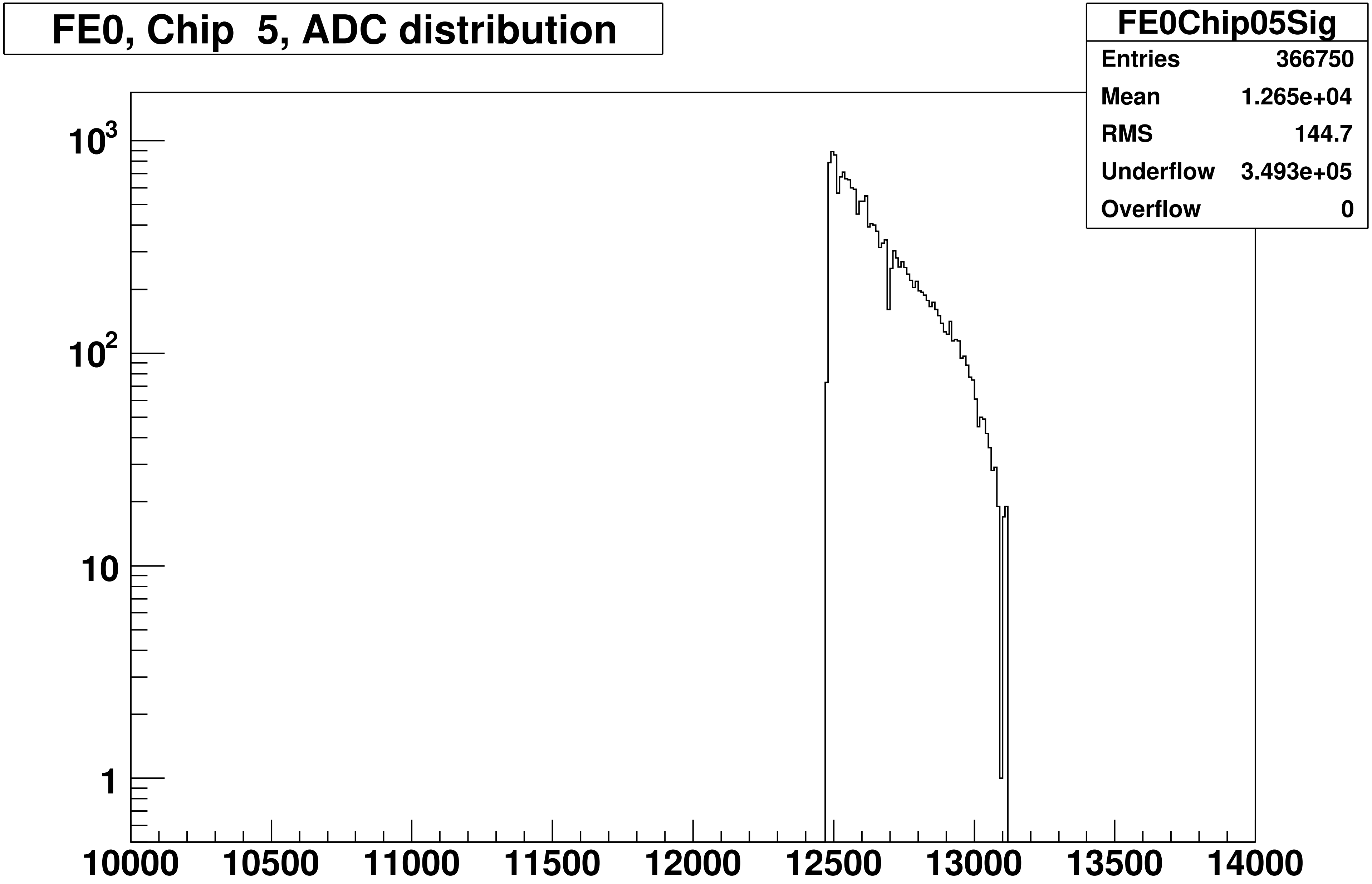
FE0, Chip 5, ADC distribution
FE0Chip05Sig
Entries 366750
Mean 1.265e+04
RMS 144.7
Underflow 3.493e+05
Overflow 0
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10
1
10000
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11500
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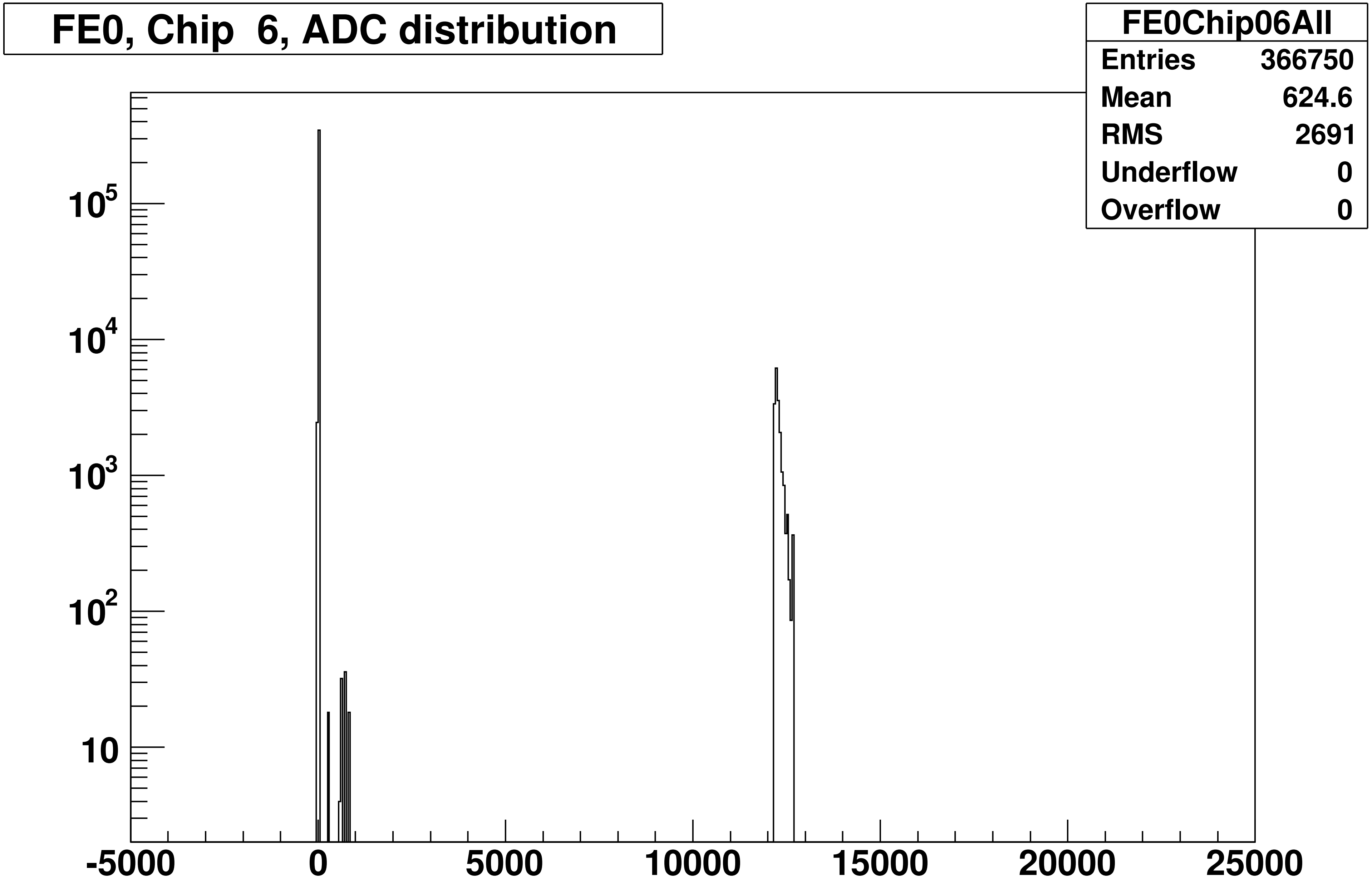
FE0, Chip 6, ADC distribution
FE0Chip06All
Entries 366750
Mean 624.6
RMS 2691
Underflow 0
Overflow 0
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10^4
10^3
10^2
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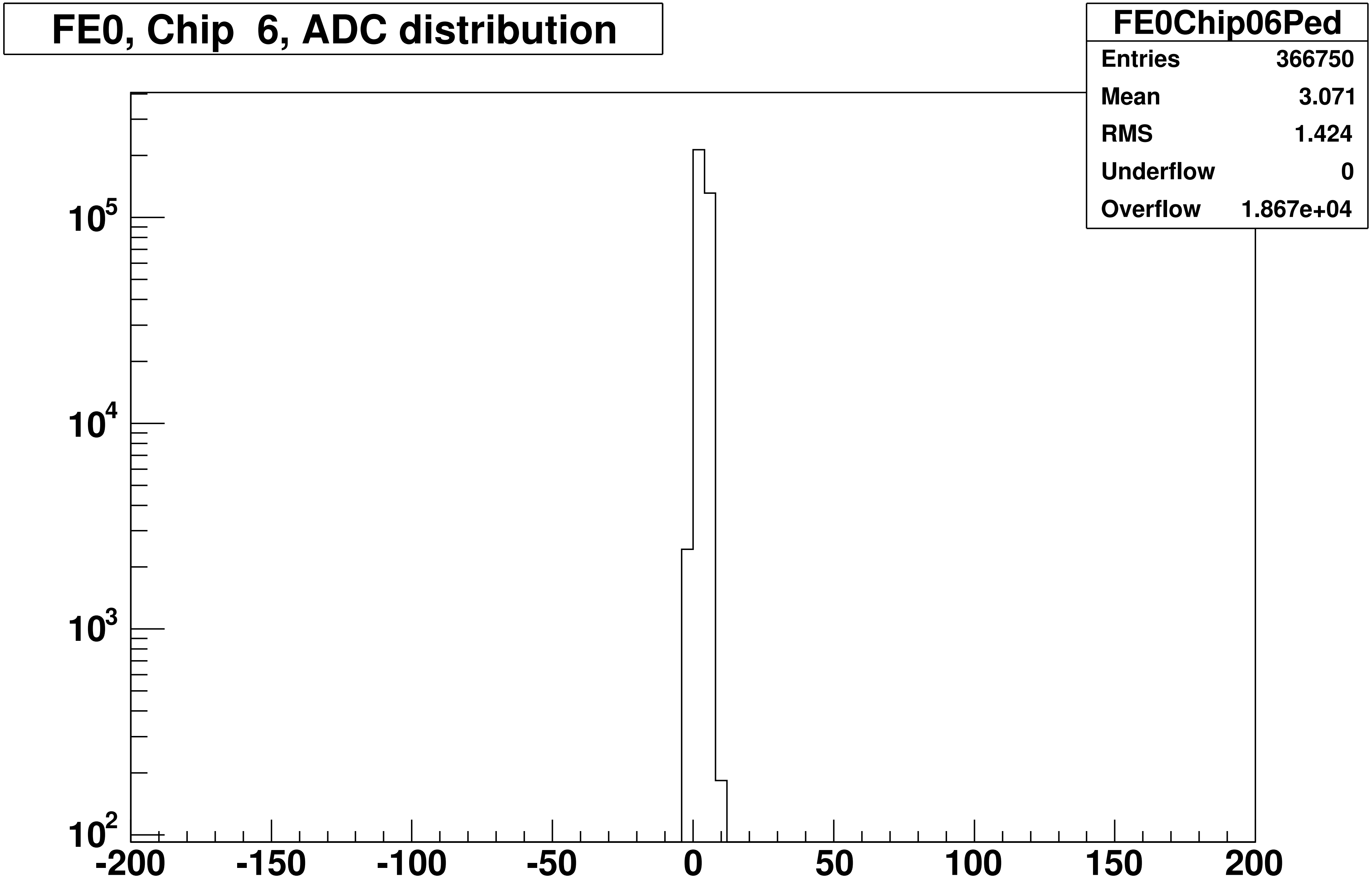
FE0, Chip 6, ADC distribution
FE0Chip06Ped
Entries 366750
Mean 3.071
RMS 1.424
Underflow 0
Overflow 1.867e+04
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10^3
10^2
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150
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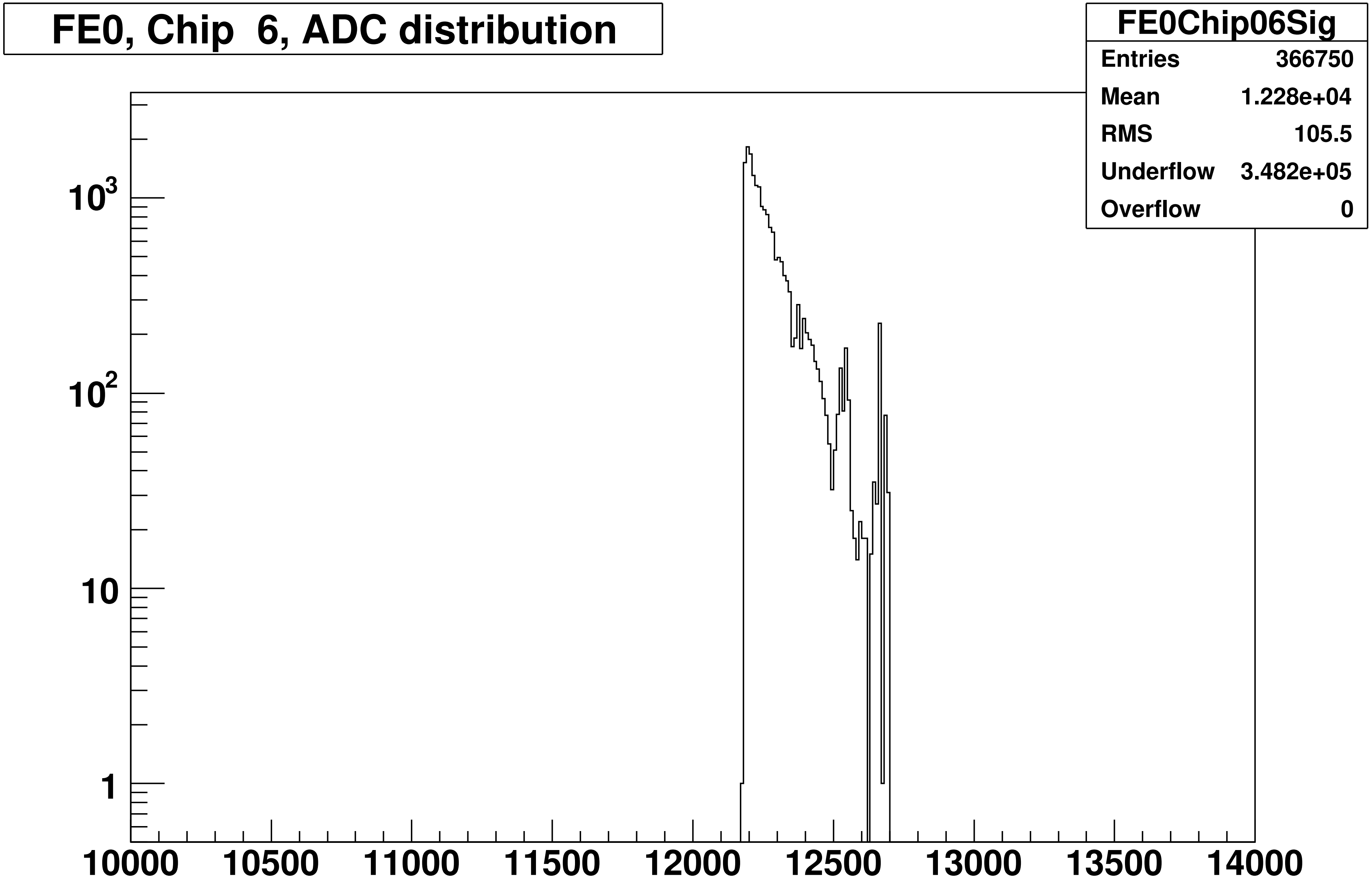

FE0, Chip 6, ADC distribution
FE0Chip06Sig
Entries 366750
Mean 1.228e+04
RMS 105.5
Underflow 3.482e+05
Overflow 0
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11500
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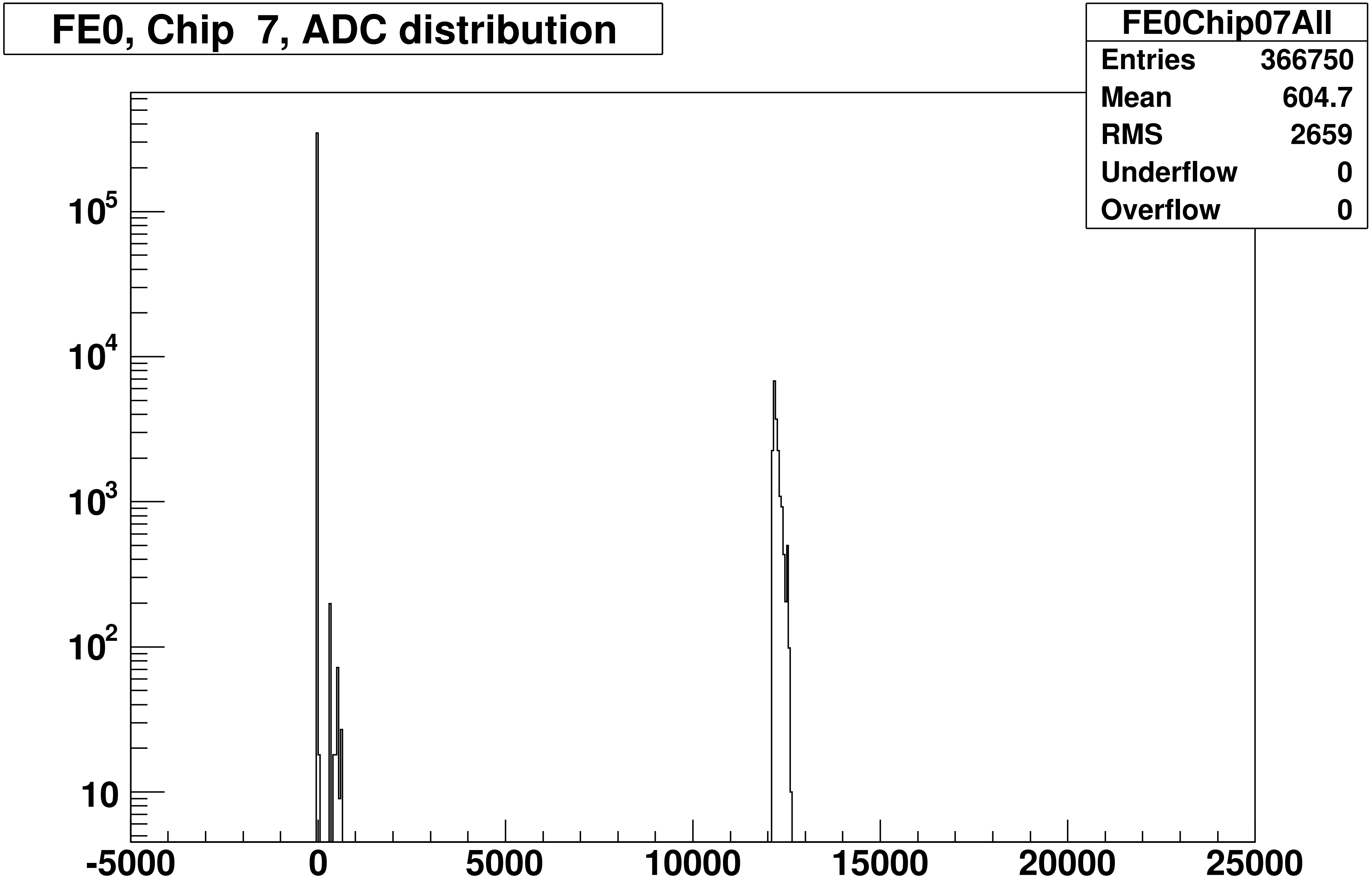
FE0, Chip 7, ADC distribution
FE0Chip07All
Entries 366750
Mean 604.7
RMS 2659
Underflow 0
Overflow 0
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10^2
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10^4
10^5
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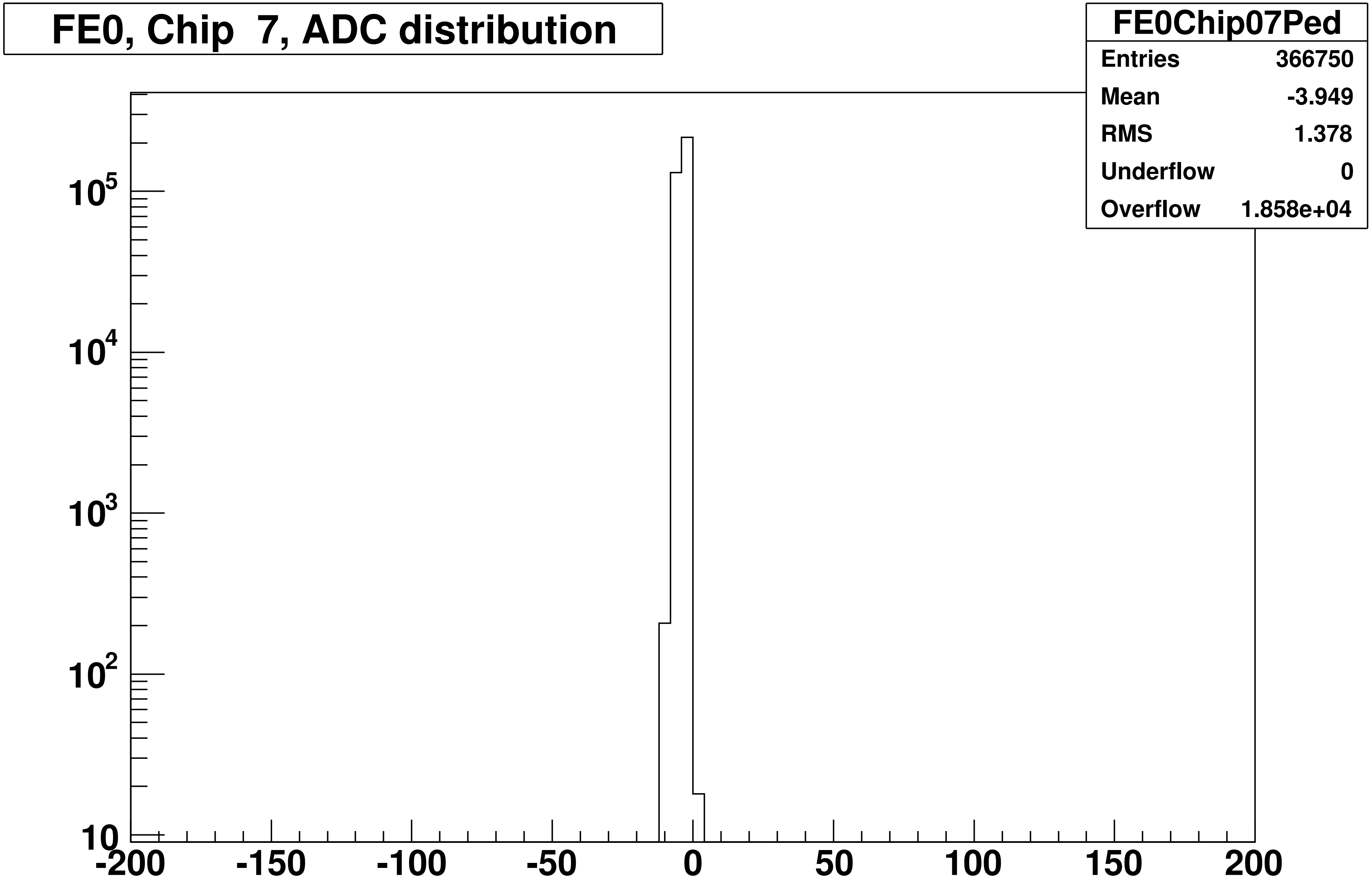
20000
25000


FE0, Chip 7, ADC distribution
FE0Chip07Ped
Entries 366750
Mean -3.949
RMS 1.378
Underflow 0
Overflow 1.858e+04
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10^3
10^4
10^5
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150
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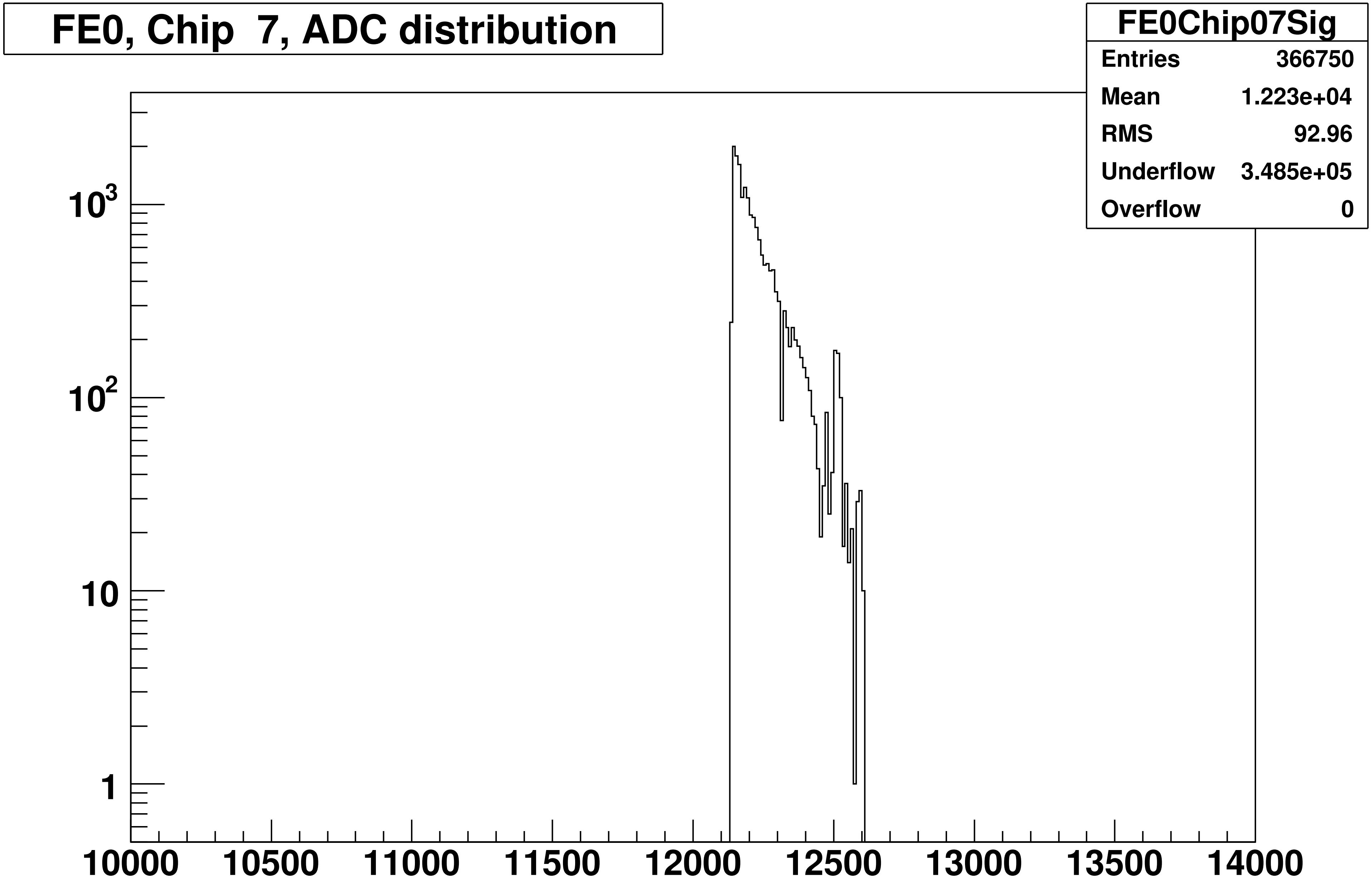
FE0, Chip 7, ADC distribution
FE0Chip07Sig
Entries 366750
Mean 1.223e+04
RMS 92.96
Underflow 3.485e+05
Overflow 0
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10^2
10
1
10000
10500
11000
11500
12000
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13500
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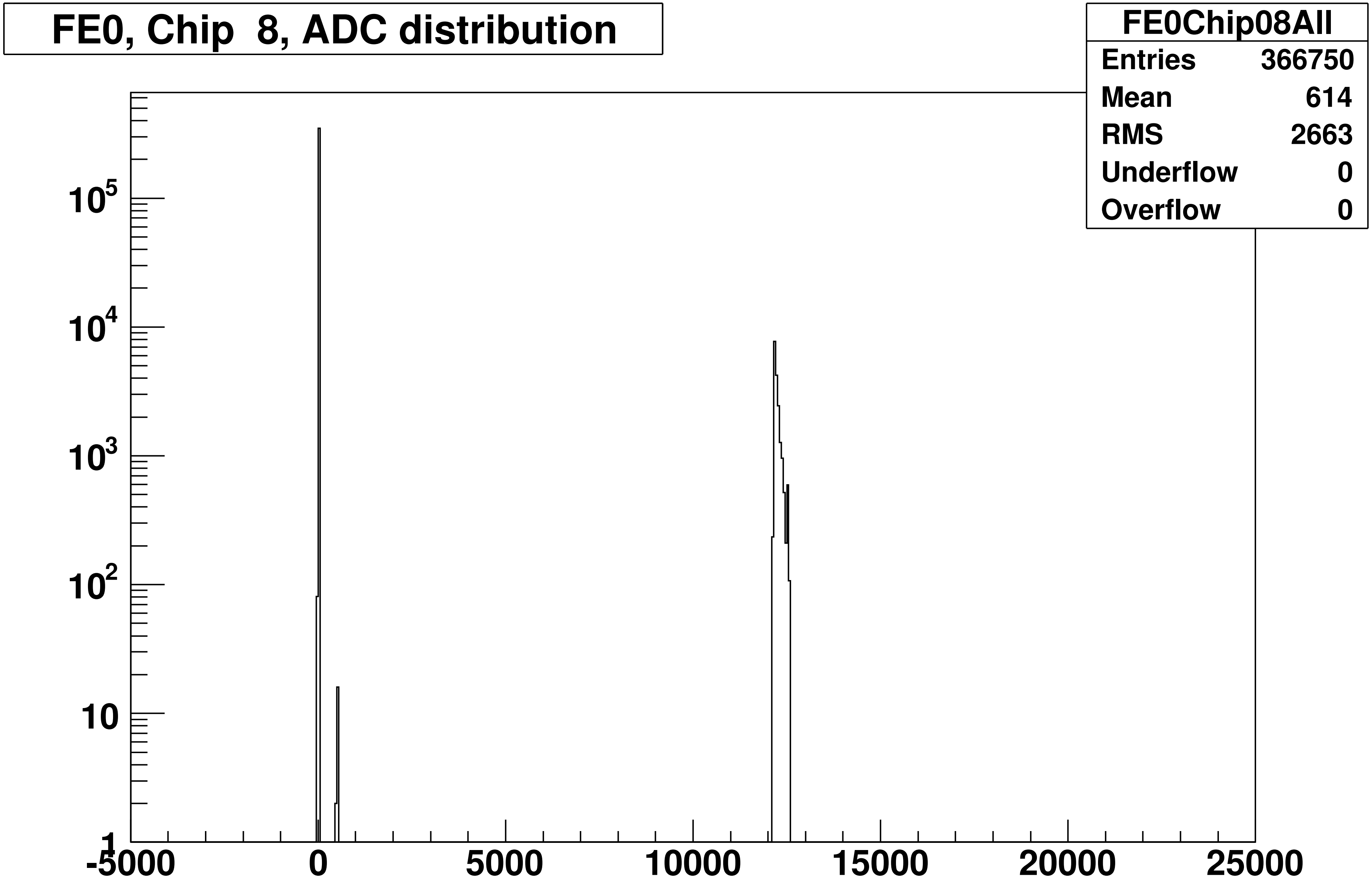
FE0, Chip 8, ADC distribution
FE0Chip08All
Entries 366750
Mean 614
RMS 2663
Underflow 0
Overflow 0
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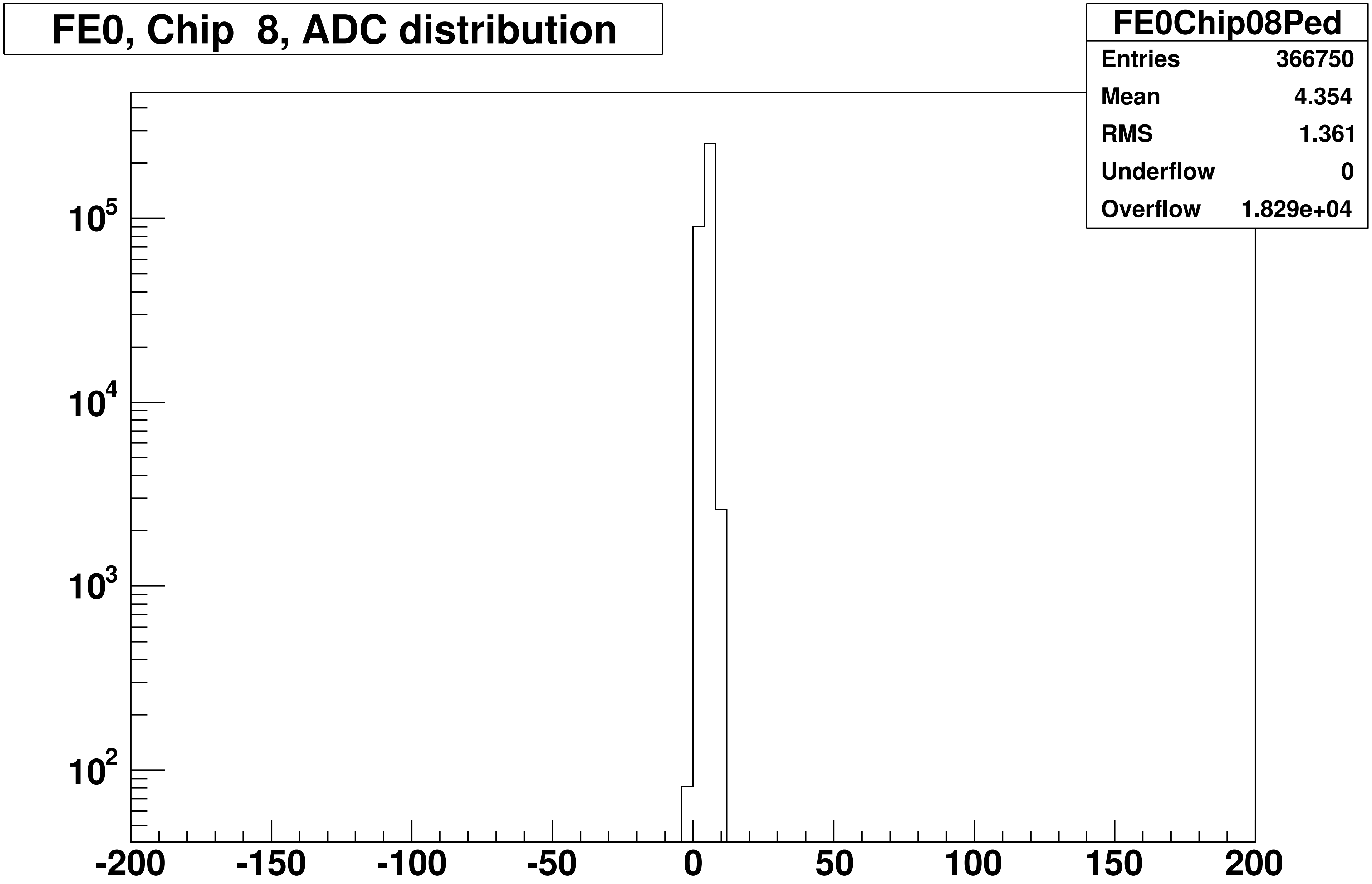
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE0, Chip 8, ADC distribution
FE0Chip08Ped
Entries 366750
Mean 4.354
RMS 1.361
Underflow 0
Overflow 1.829e+04
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10^4
10^3
10^2
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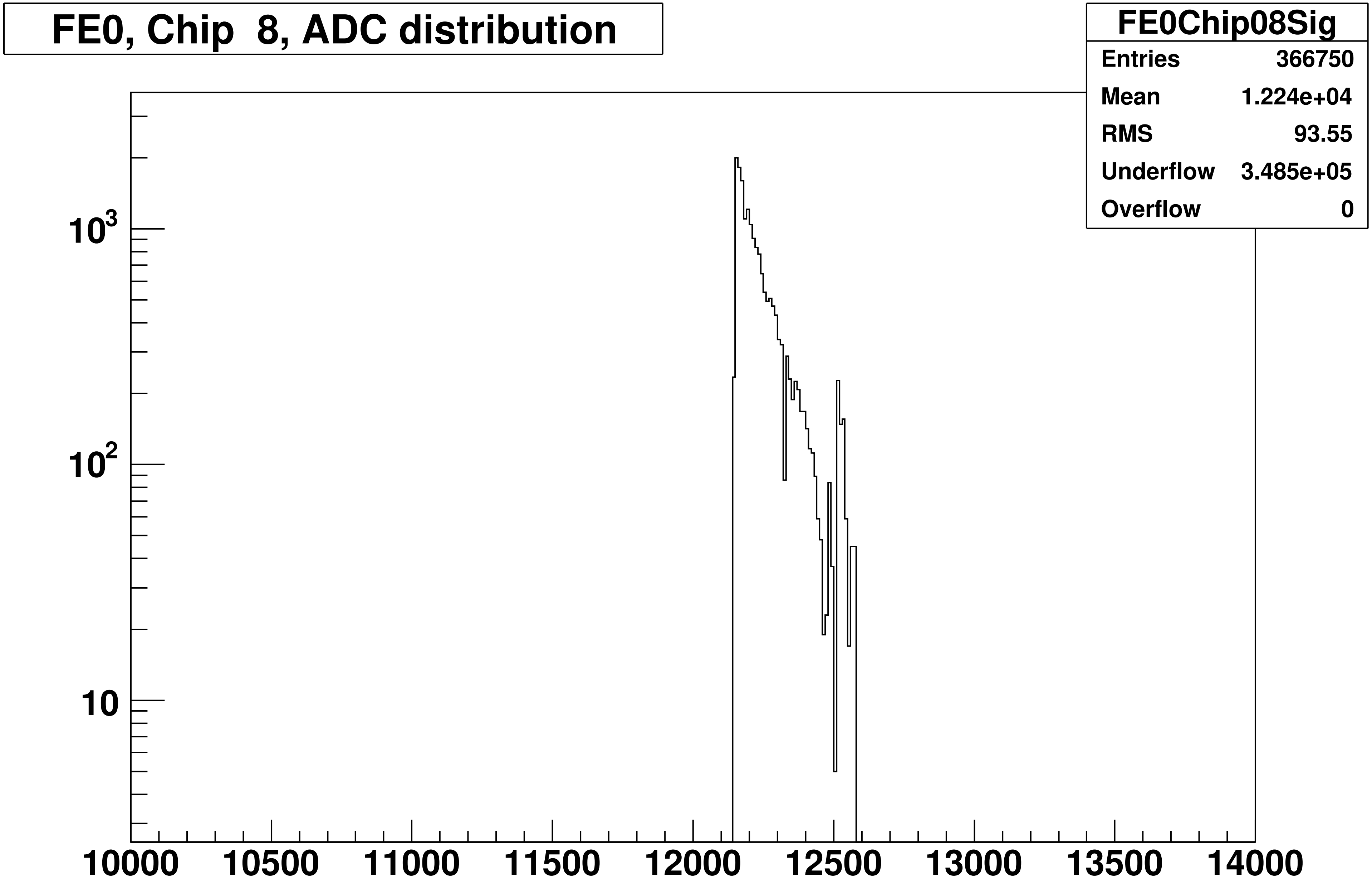
150
200


FE0, Chip 8, ADC distribution
FE0Chip08Sig
Entries 366750
Mean 1.224e+04
RMS 93.55
Underflow 3.485e+05
Overflow 0
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10^2
10
10000
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11500
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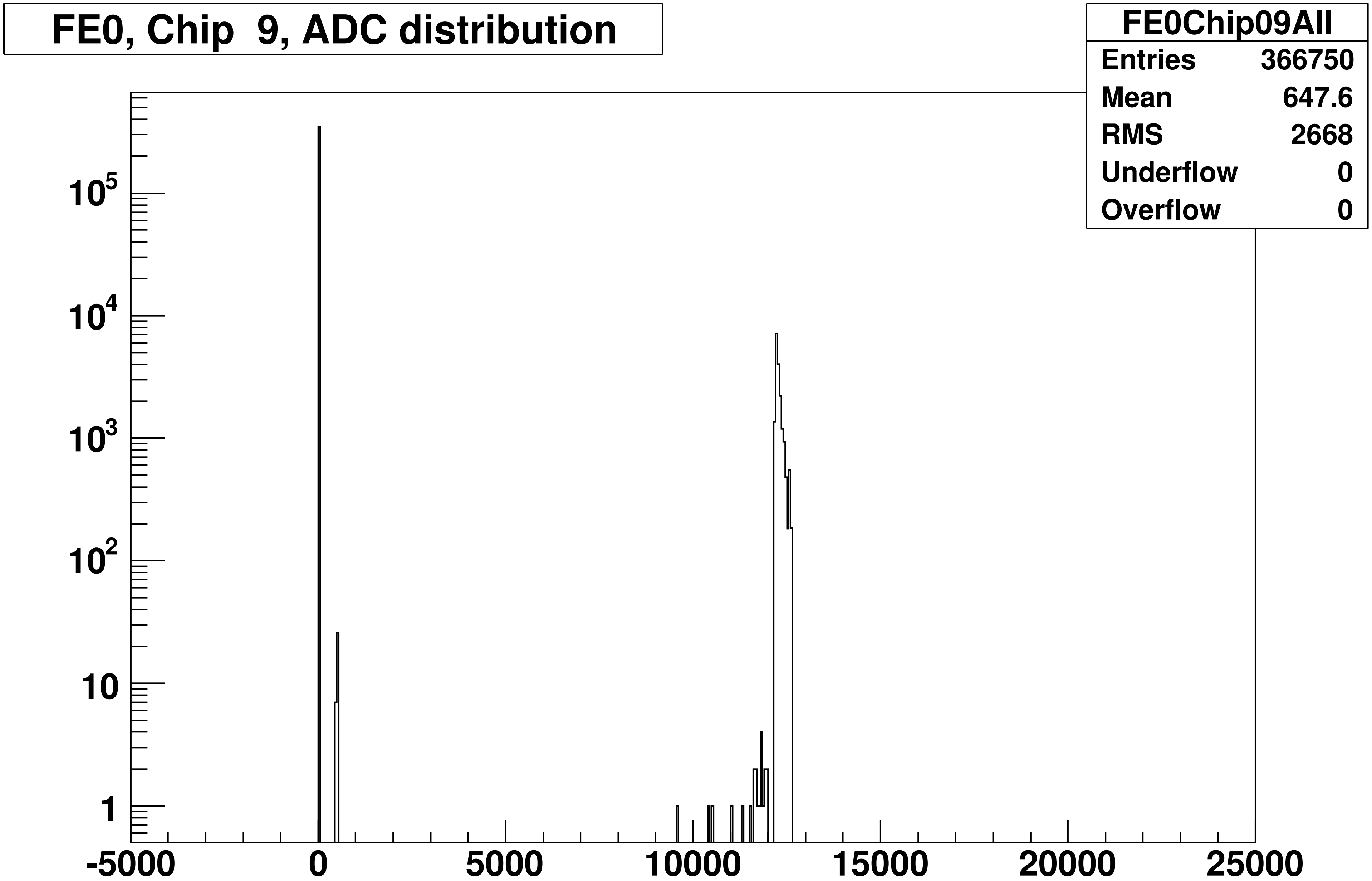
FE0, Chip 9, ADC distribution
FE0Chip09All
Entries 366750
Mean 647.6
RMS 2668
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
1
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10000
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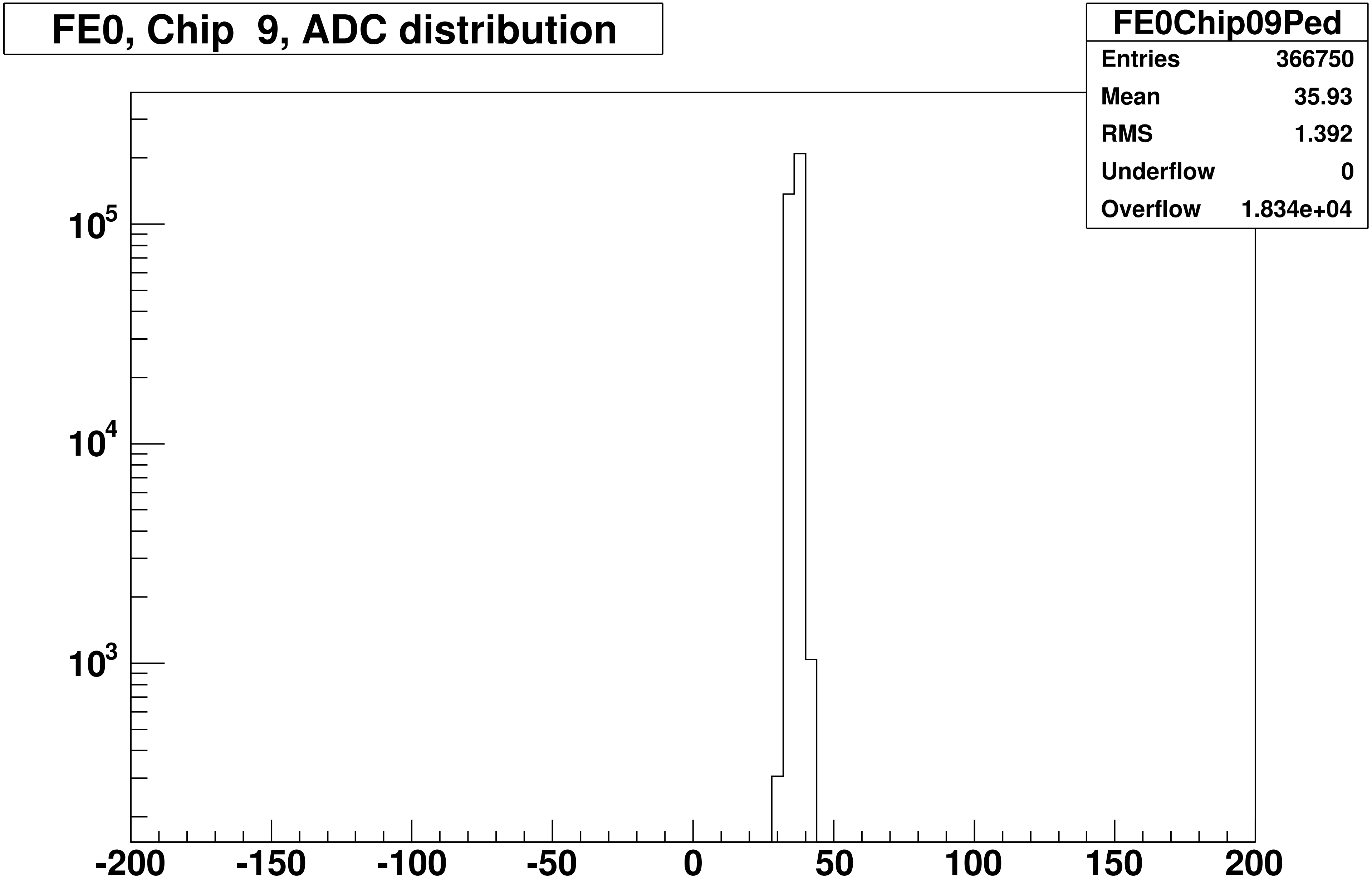
20000
25000



FE0, Chip 9, ADC distribution
FE0Chip09Ped
Entries 366750
Mean 35.93
RMS 1.392
Underflow 0
Overflow 1.834e+04
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10^4
10^3
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-100
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0
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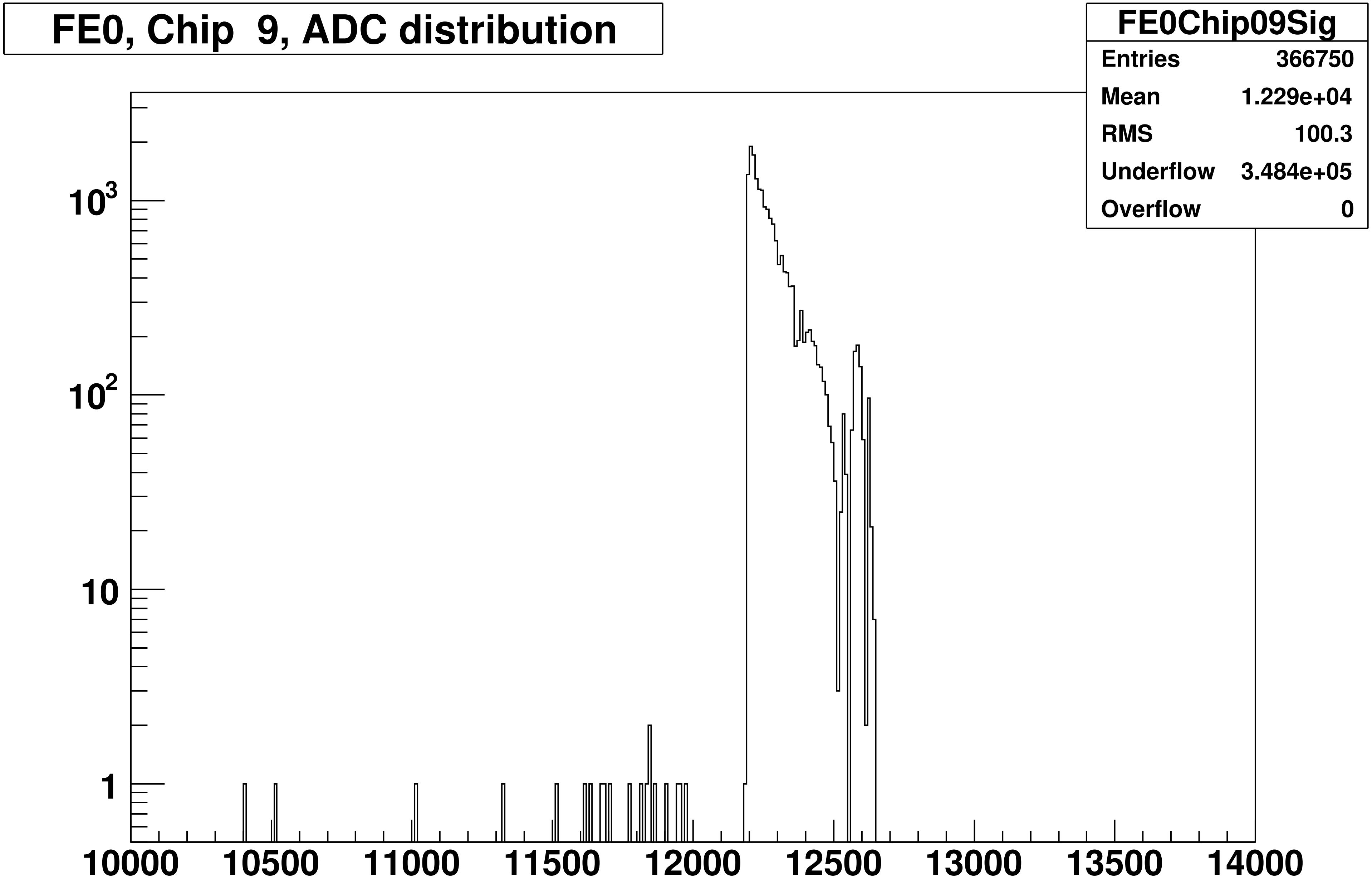
100
150
200


FE0, Chip 9, ADC distribution
FE0Chip09Sig
Entries 366750
Mean 1.229e+04
RMS 100.3
Underflow 3.484e+05
Overflow 0
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10^2
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1
10000
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11500
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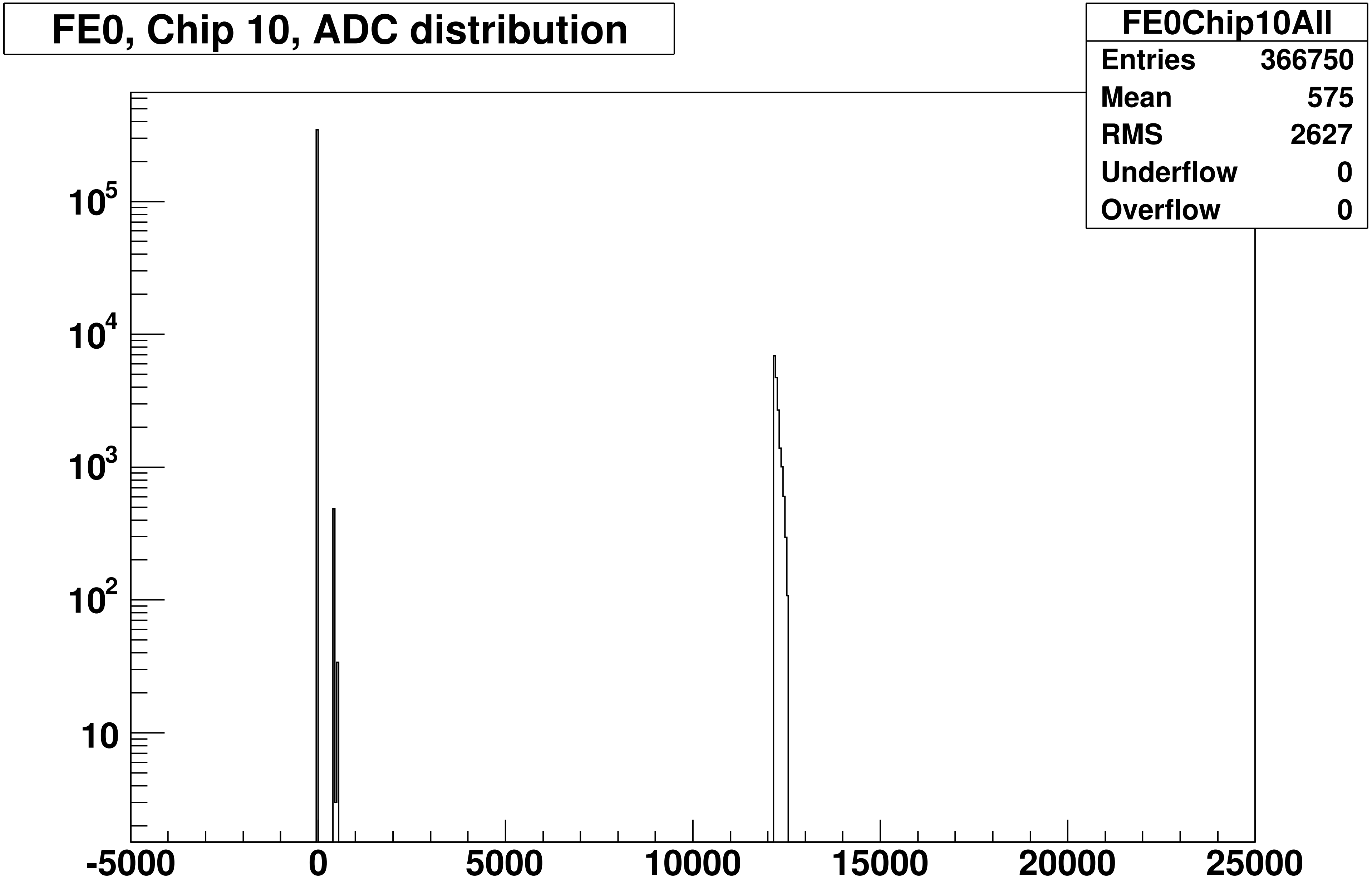
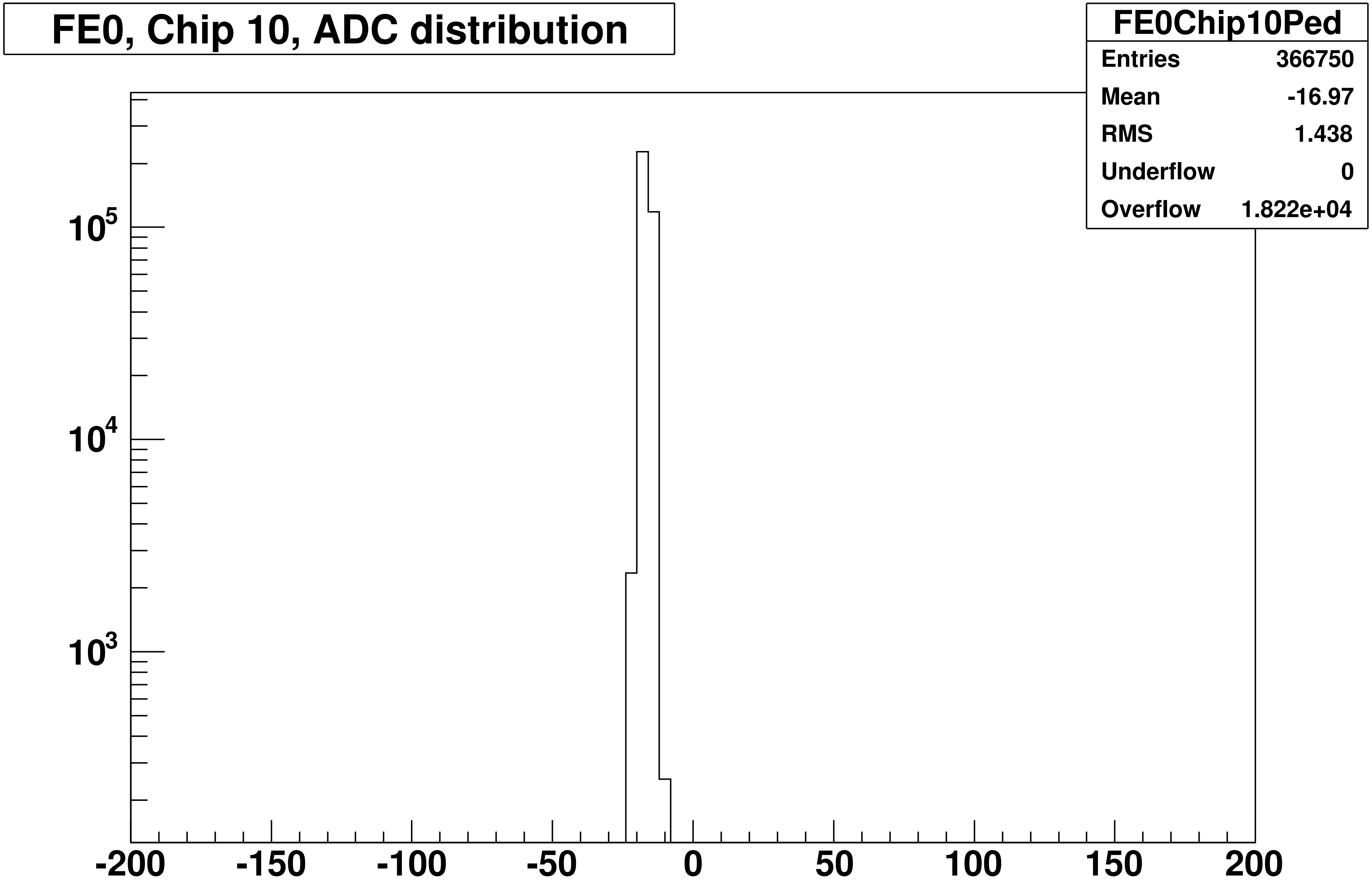


FE0, Chip 10, ADC distribution
FE0Chip10All
Entries 366750
Mean 575
RMS 2627
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE0, Chip 10, ADC distribution
FE0Chip10Ped
Entries 366750
Mean -16.97
RMS 1.438
Underflow 0
Overflow 1.822e+04
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10^4
10^3
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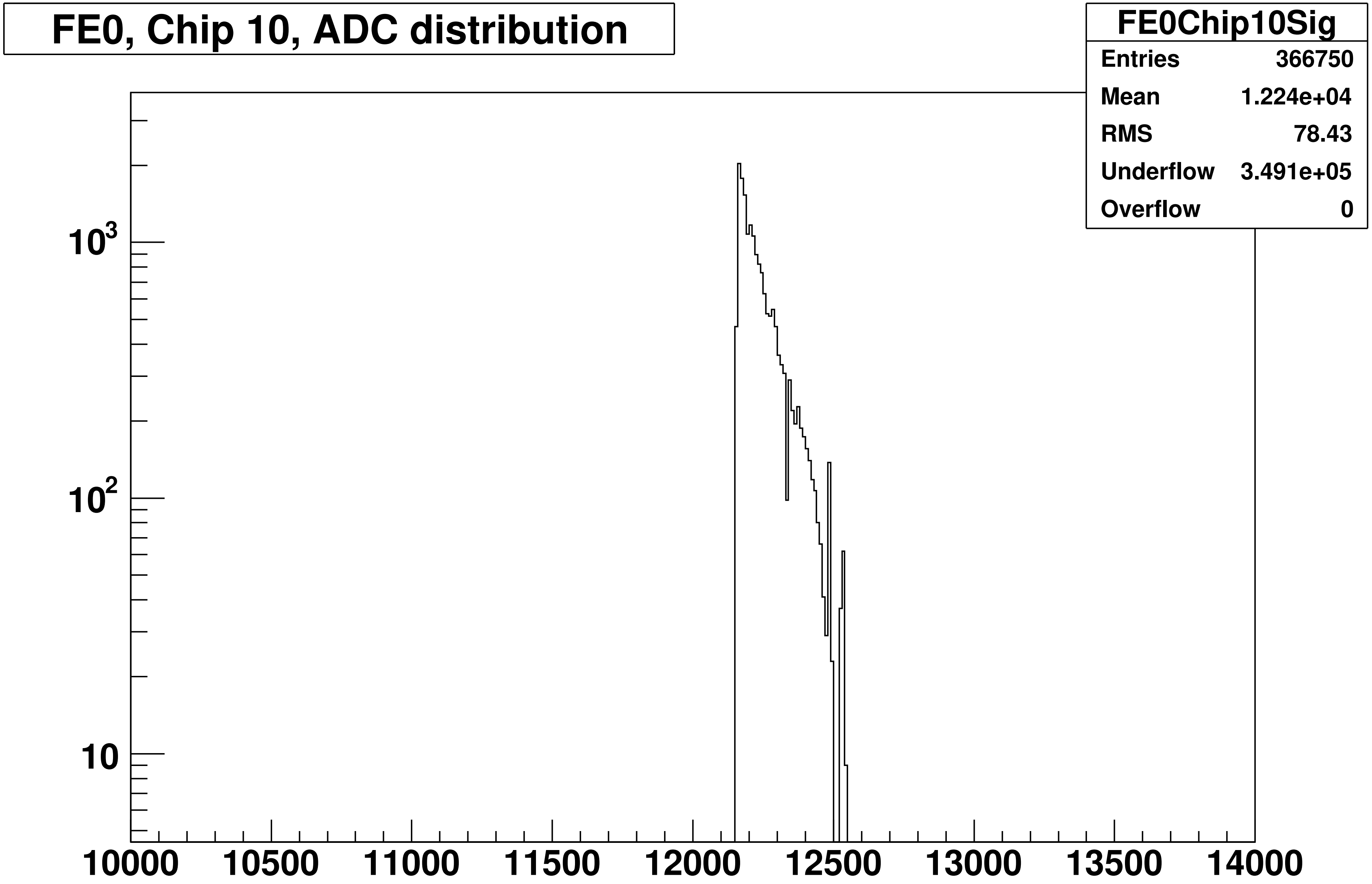
150
200


FE0, Chip 10, ADC distribution
FE0Chip10Sig
Entries 366750
Mean 1.224e+04
RMS 78.43
Underflow 3.491e+05
Overflow 0
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11500
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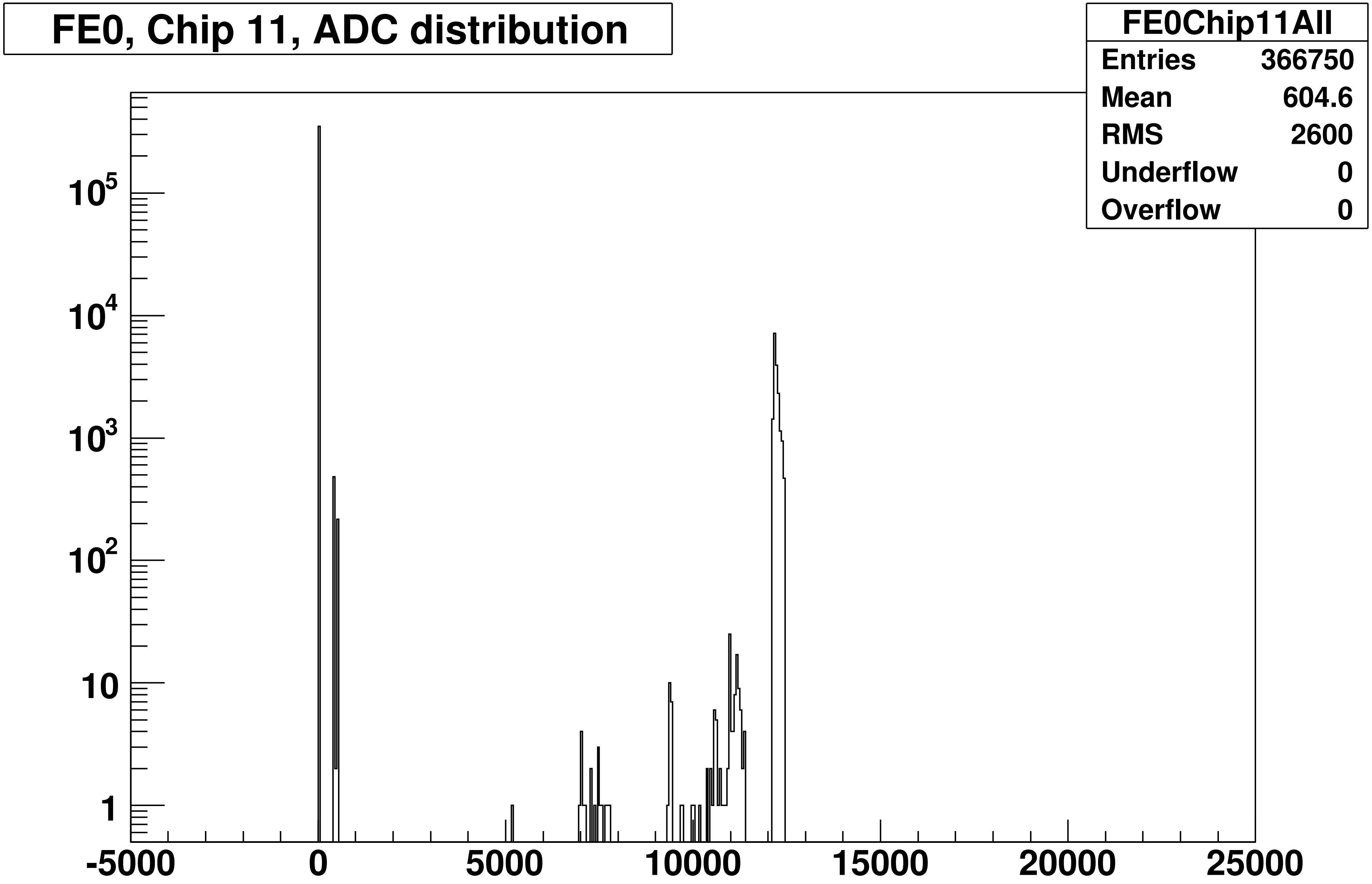

FE0, Chip 11, ADC distribution
FE0Chip11All
Entries 366750
Mean 604.6
RMS 2600
Underflow 0
Overflow 0
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10000
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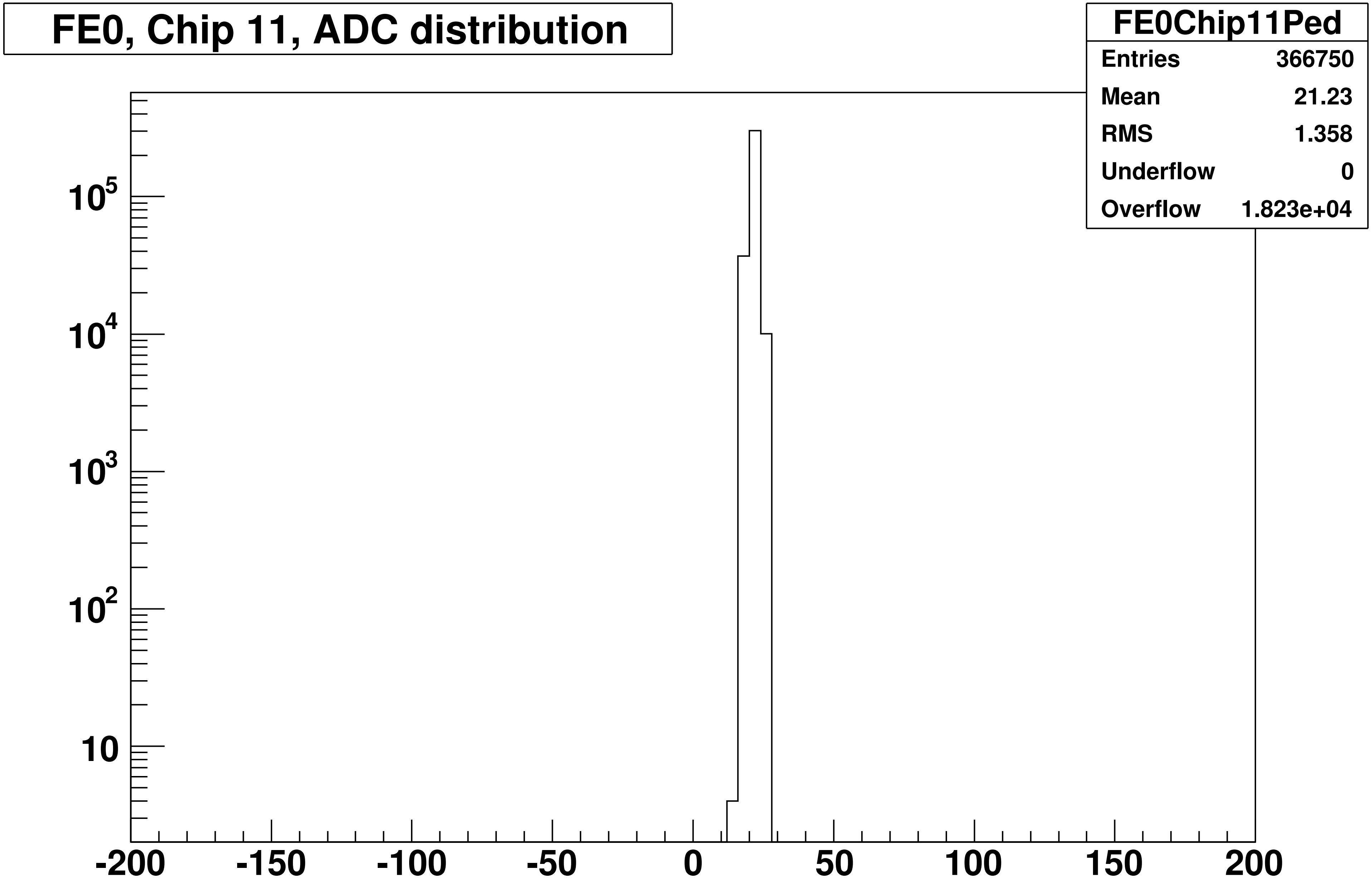
20000
25000


FE0, Chip 11, ADC distribution
FE0Chip11Ped
Entries 366750
Mean 21.23
RMS 1.358
Underflow 0
Overflow 1.823e+04
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10^3
10^4
10^5
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-100
-50
0
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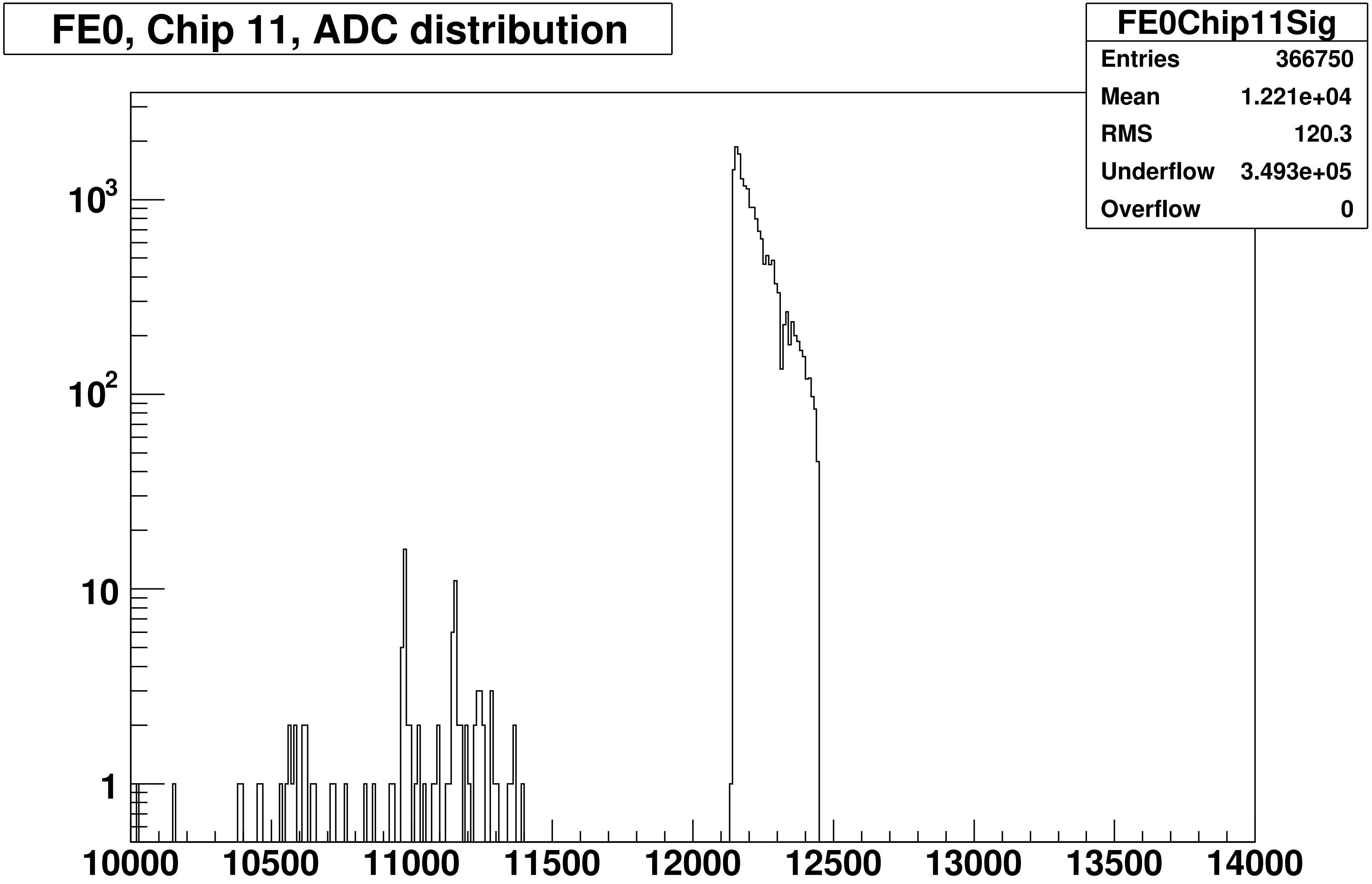
100
150
200


FE0, Chip 11, ADC distribution
FE0Chip11Sig
Entries 366750
Mean 1.221e+04
RMS 120.3
Underflow 3.493e+05
Overflow 0
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10^2
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1
10000
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11500
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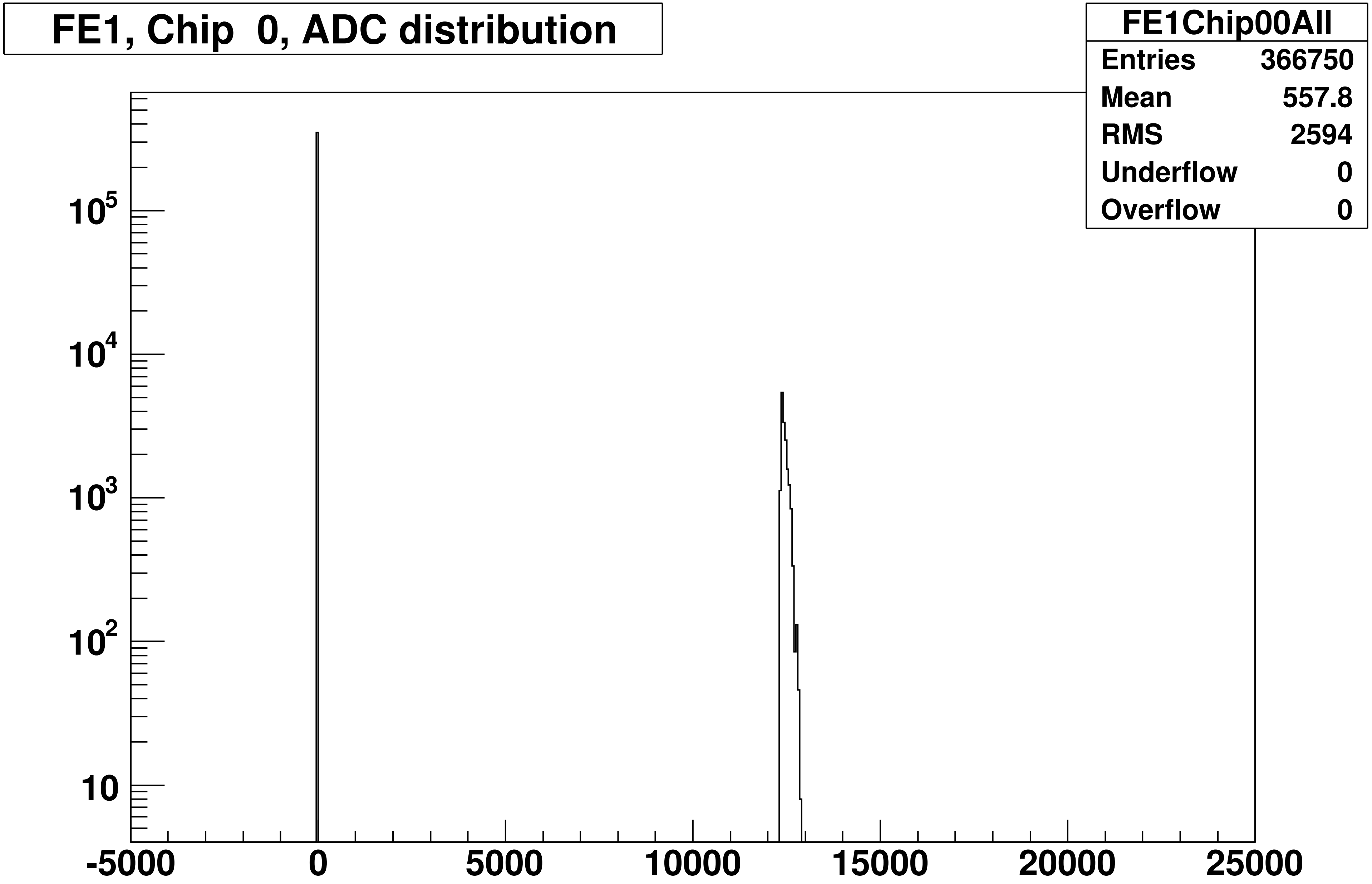
14000


FE1, Chip 0, ADC distribution
FE1Chip00All
Entries 366750
Mean 557.8
RMS 2594
Underflow 0
Overflow 0
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10^4
10^3
10^2
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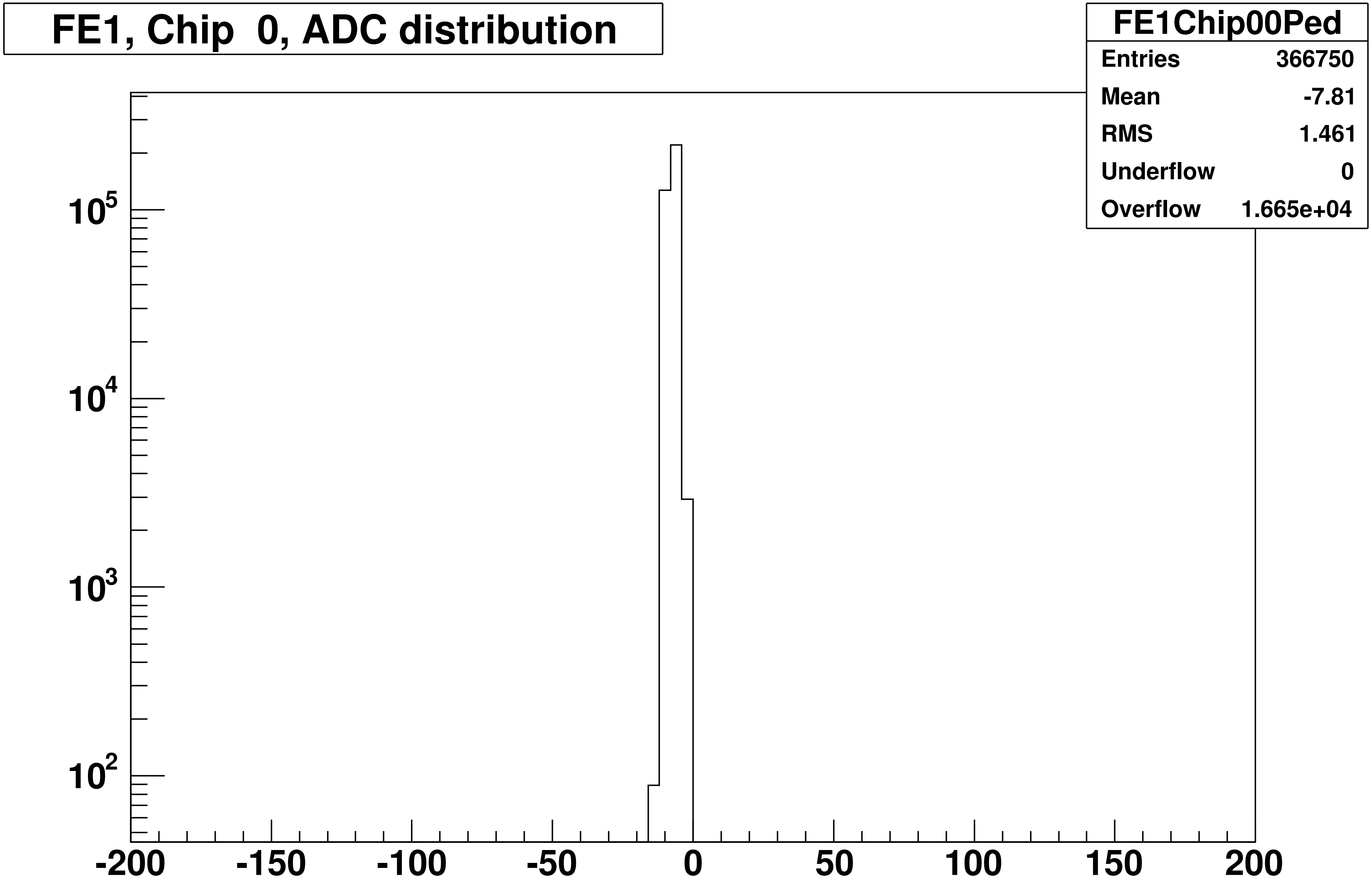
-5000
0
5000
10000
15000
20000
25000



FE1, Chip 0, ADC distribution
FE1Chip00Ped
Entries 366750
Mean -7.81
RMS 1.461
Underflow 0
Overflow 1.665e+04
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10^3
10^2
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-100
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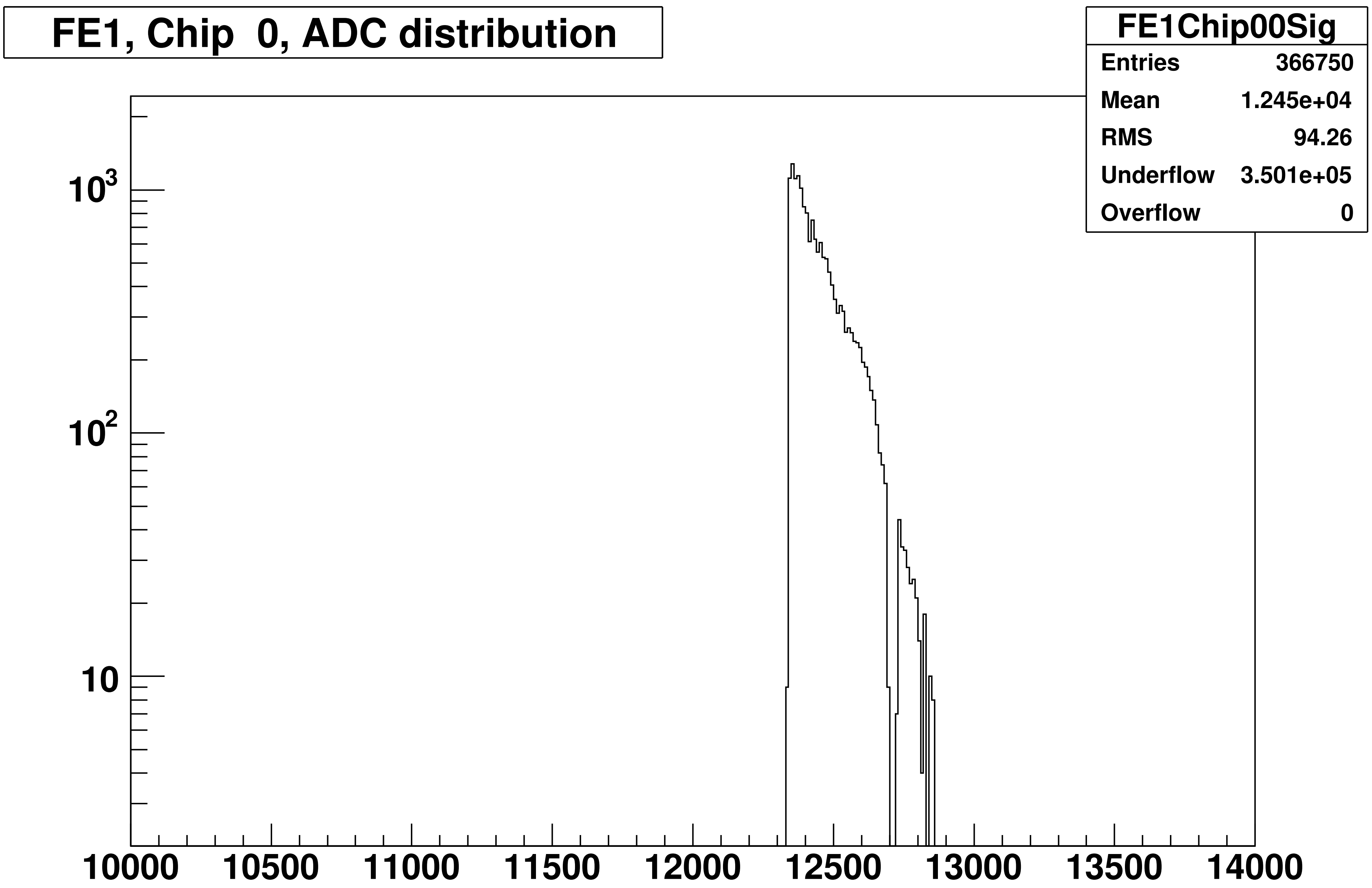
100
150
200


FE1, Chip 0, ADC distribution
FE1Chip00Sig
Entries 366750
Mean 1.245e+04
RMS 94.26
Underflow 3.501e+05
Overflow 0
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13500
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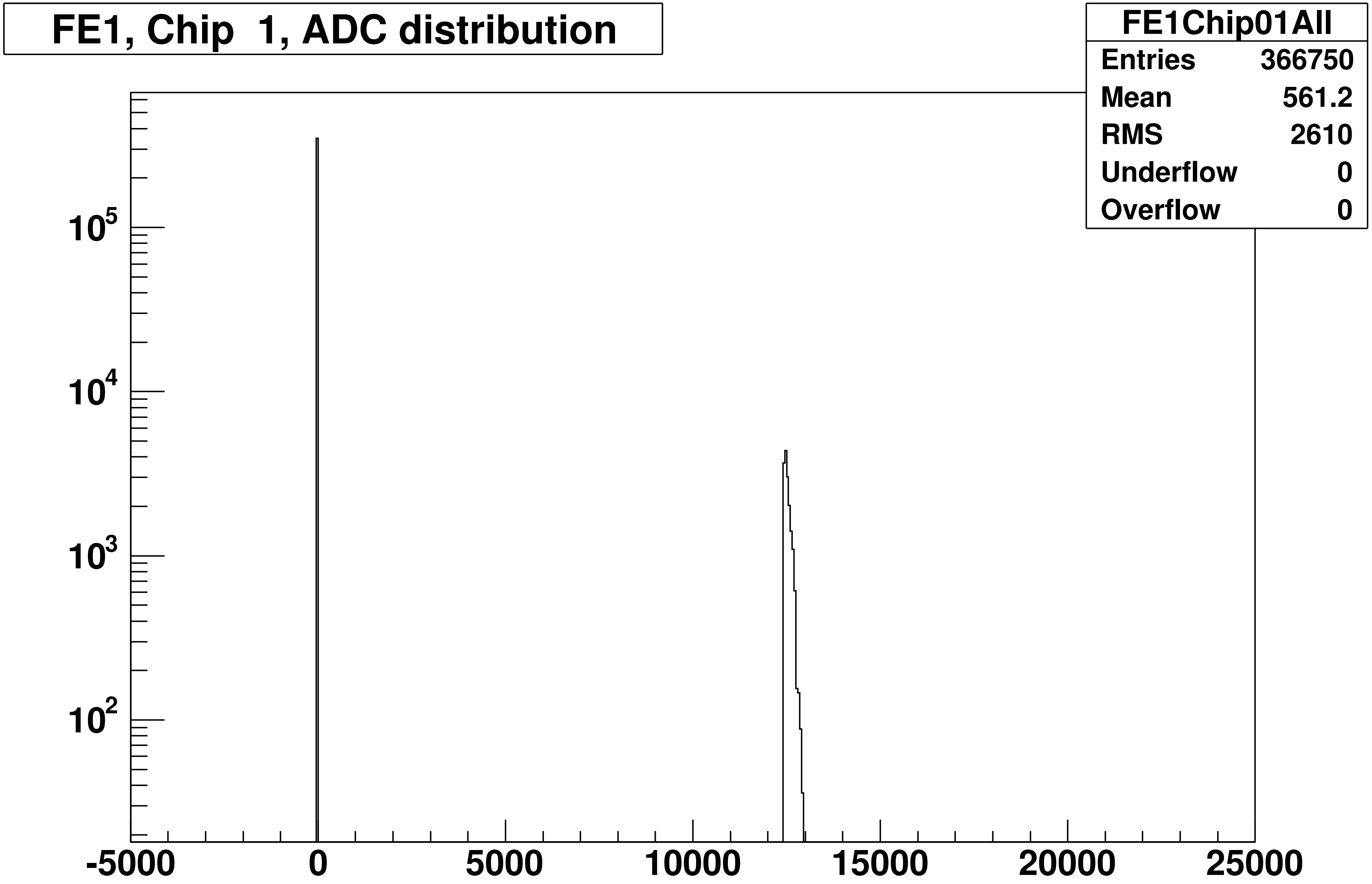
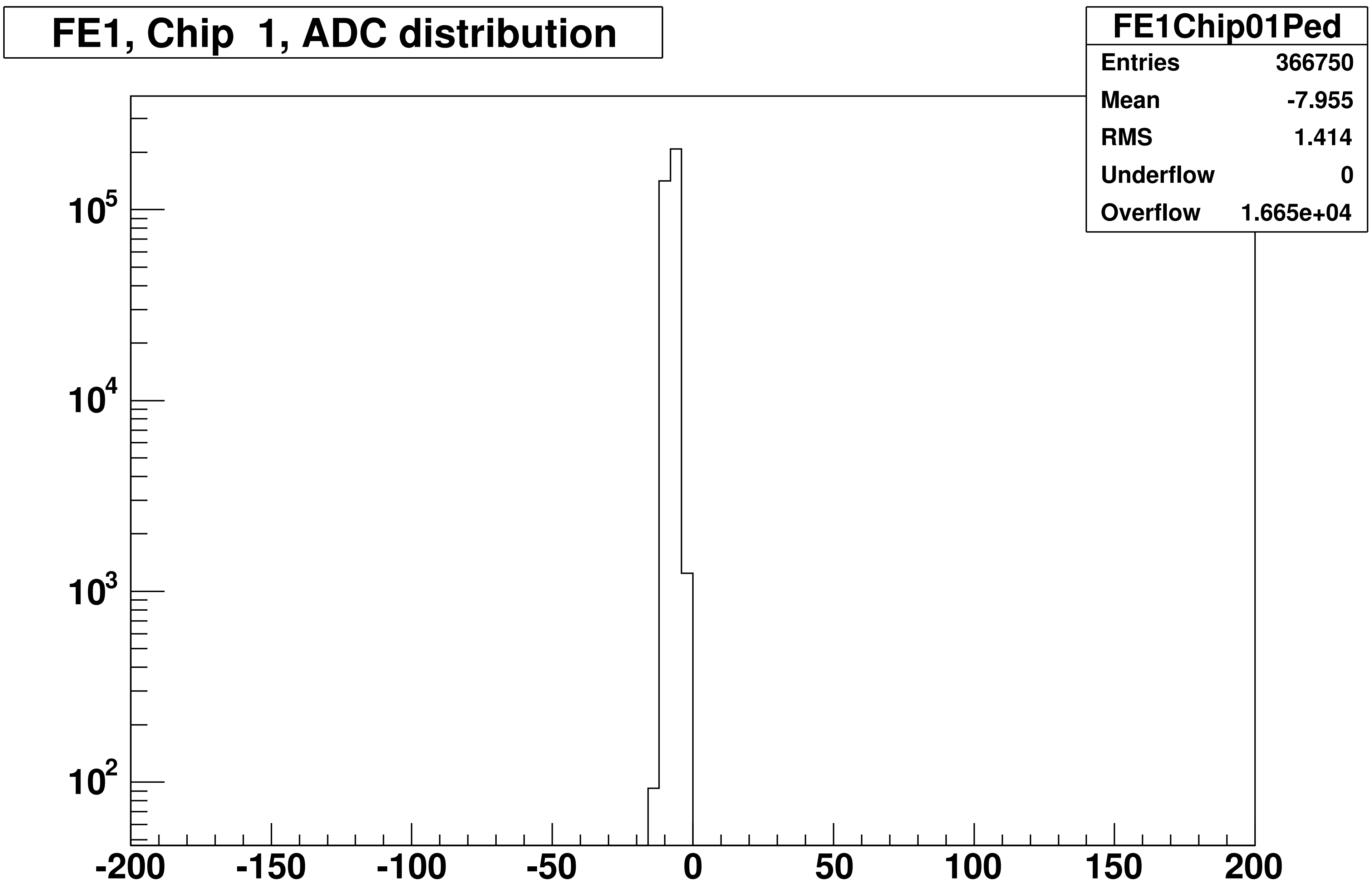


FE1, Chip 1, ADC distribution
FE1Chip01All
Entries 366750
Mean 561.2
RMS 2610
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000


FE1, Chip 1, ADC distribution
FE1Chip01Ped
Entries 366750
Mean -7.955
RMS 1.414
Underflow 0
Overflow 1.665e+04
10^5
10^4
10^3
10^2
-200
-150
-100
-50
0
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100
150
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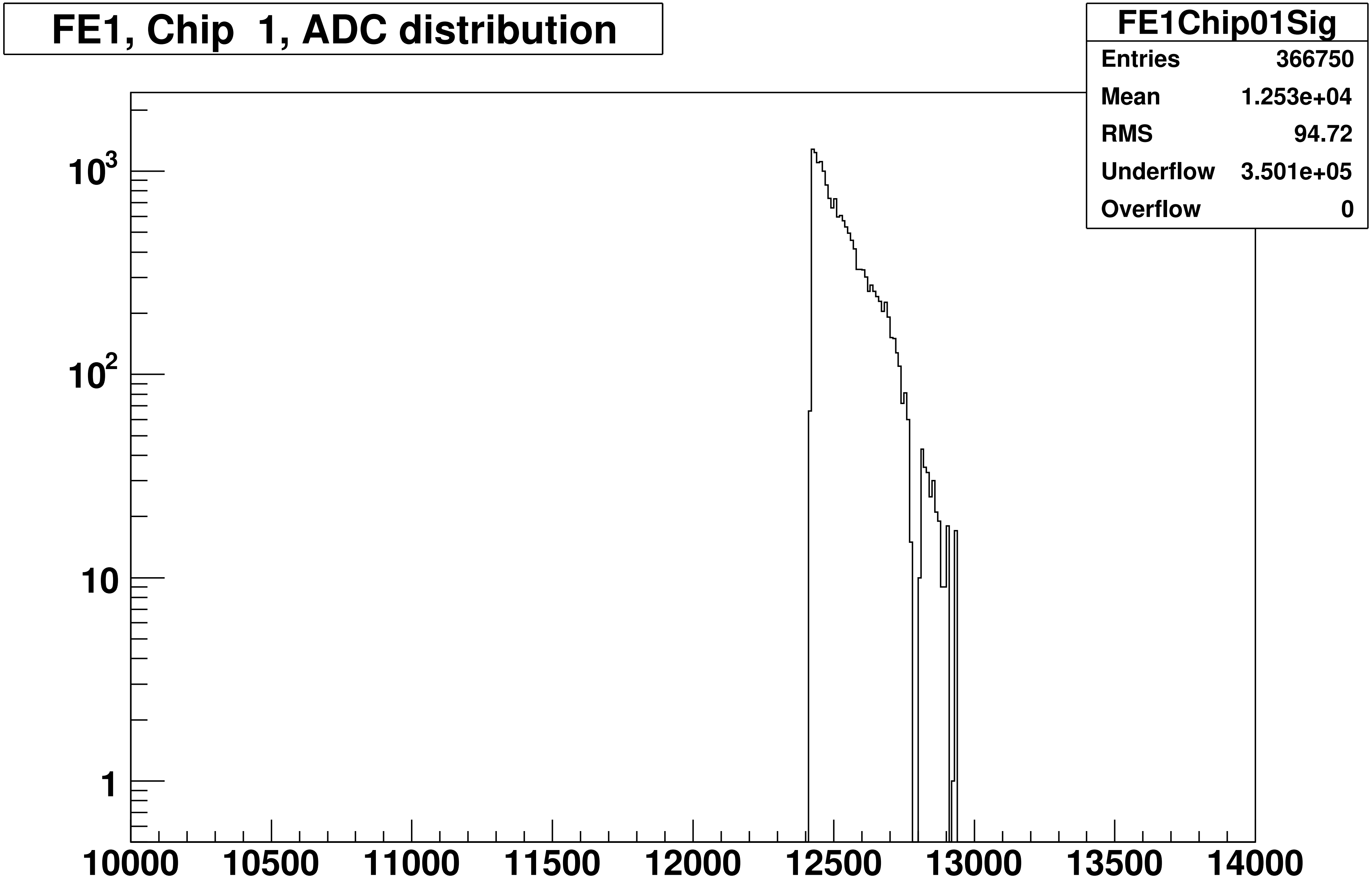
FE1, Chip 1, ADC distribution
FE1Chip01Sig
Entries 366750
Mean 1.253e+04
RMS 94.72
Underflow 3.501e+05
Overflow 0
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10^2
10
1
10000
10500
11000
11500
12000
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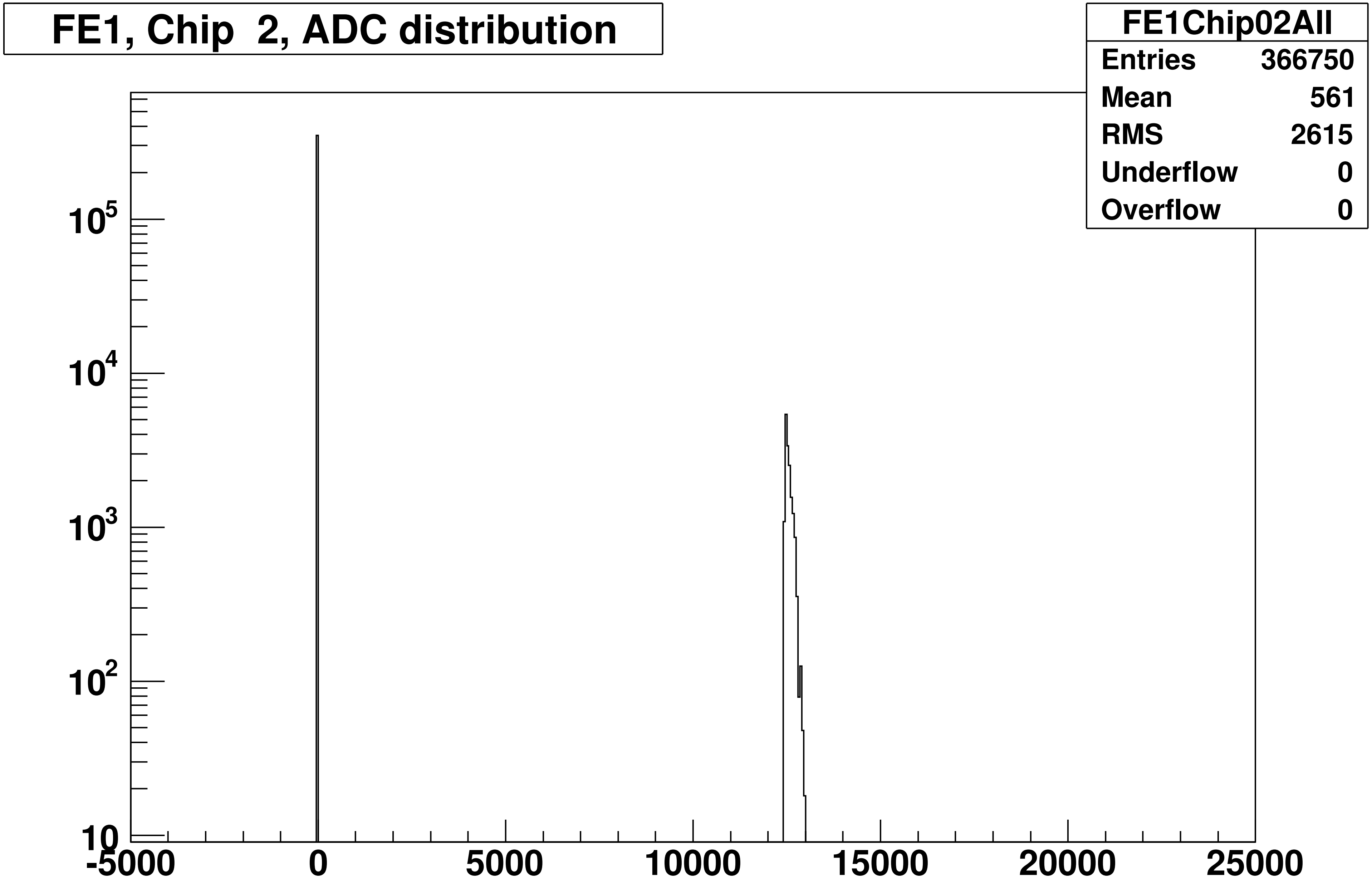
FE1, Chip 2, ADC distribution
FE1Chip02All
Entries 366750
Mean 561
RMS 2615
Underflow 0
Overflow 0
10
10^2
10^3
10^4
10^5
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0
5000
10000
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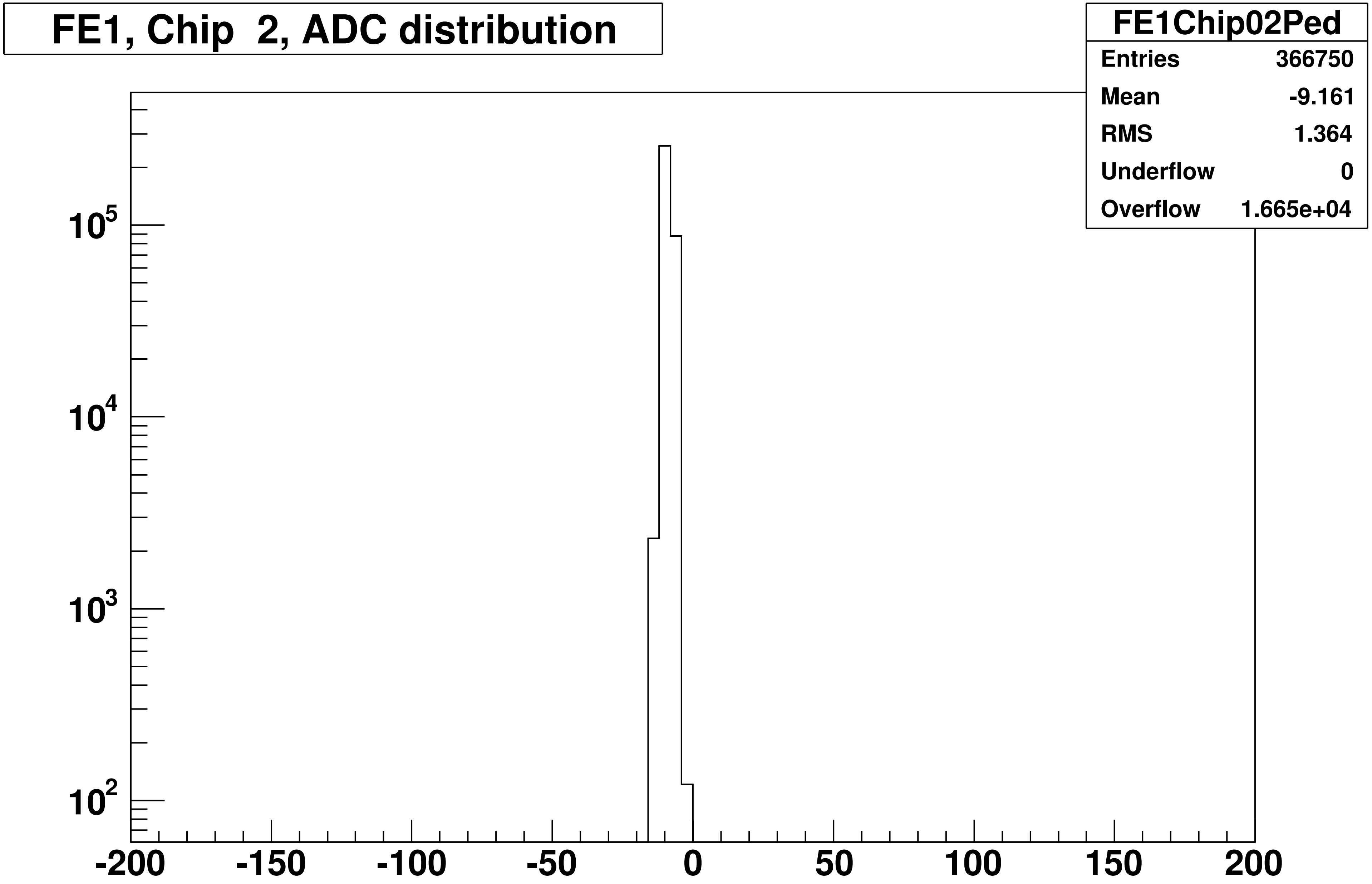
FE1, Chip 2, ADC distribution
FE1Chip02Ped
Entries 366750
Mean -9.161
RMS 1.364
Underflow 0
Overflow 1.665e+04
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10^4
10^3
10^2
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-100
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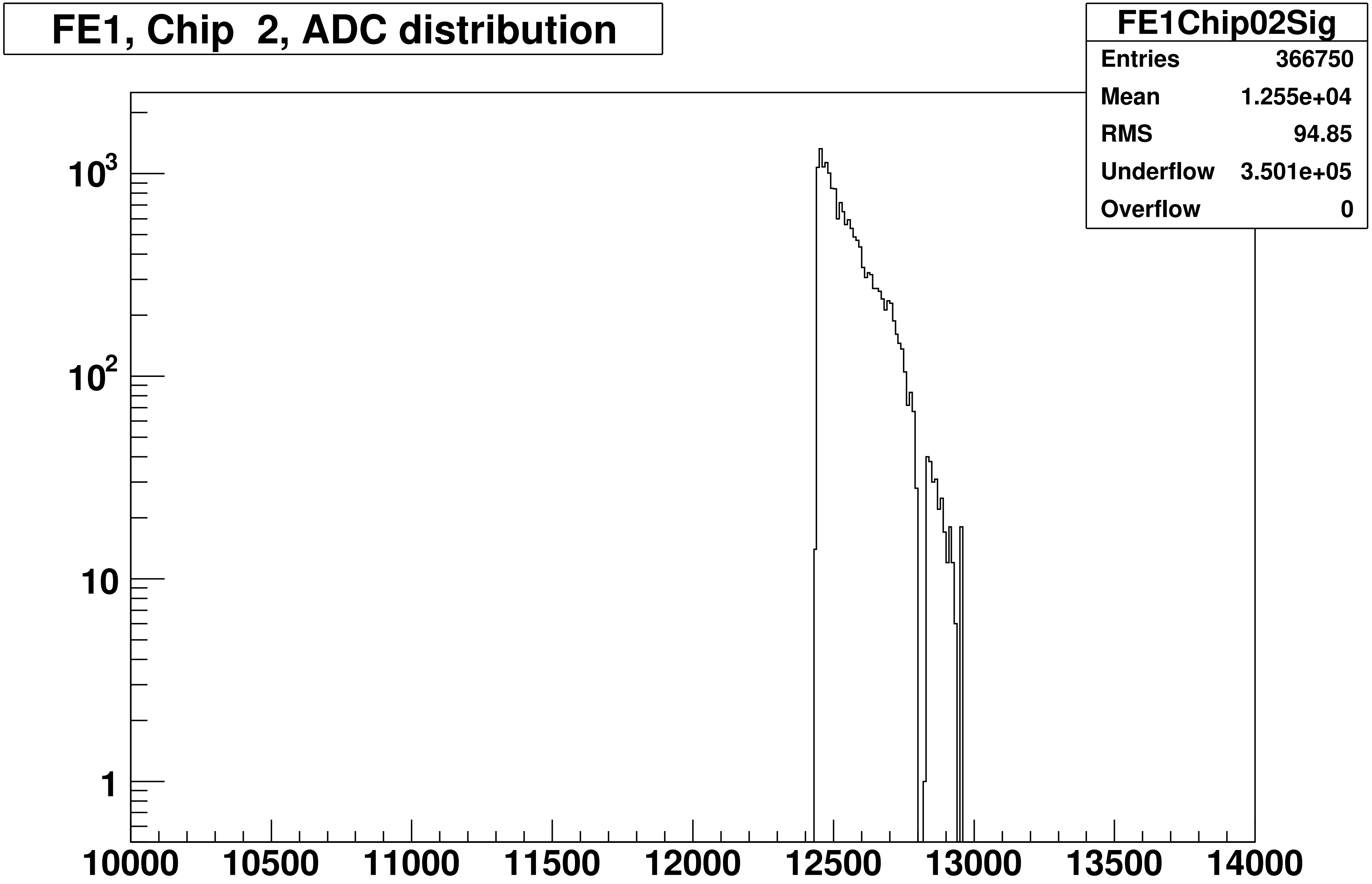

FE1, Chip 2, ADC distribution
FE1Chip02Sig
Entries 366750
Mean 1.255e+04
RMS 94.85
Underflow 3.501e+05
Overflow 0
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10^2
10
1
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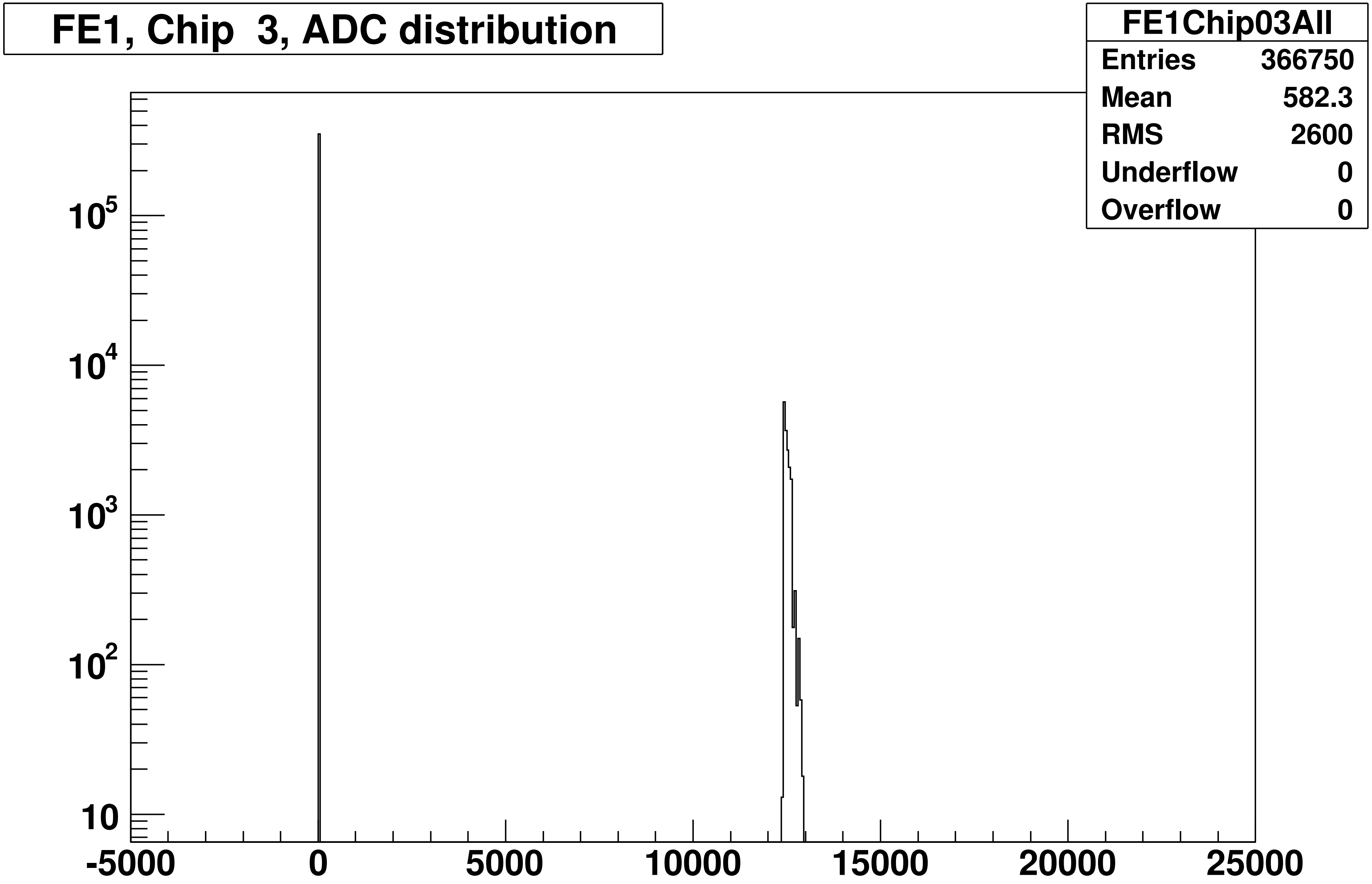
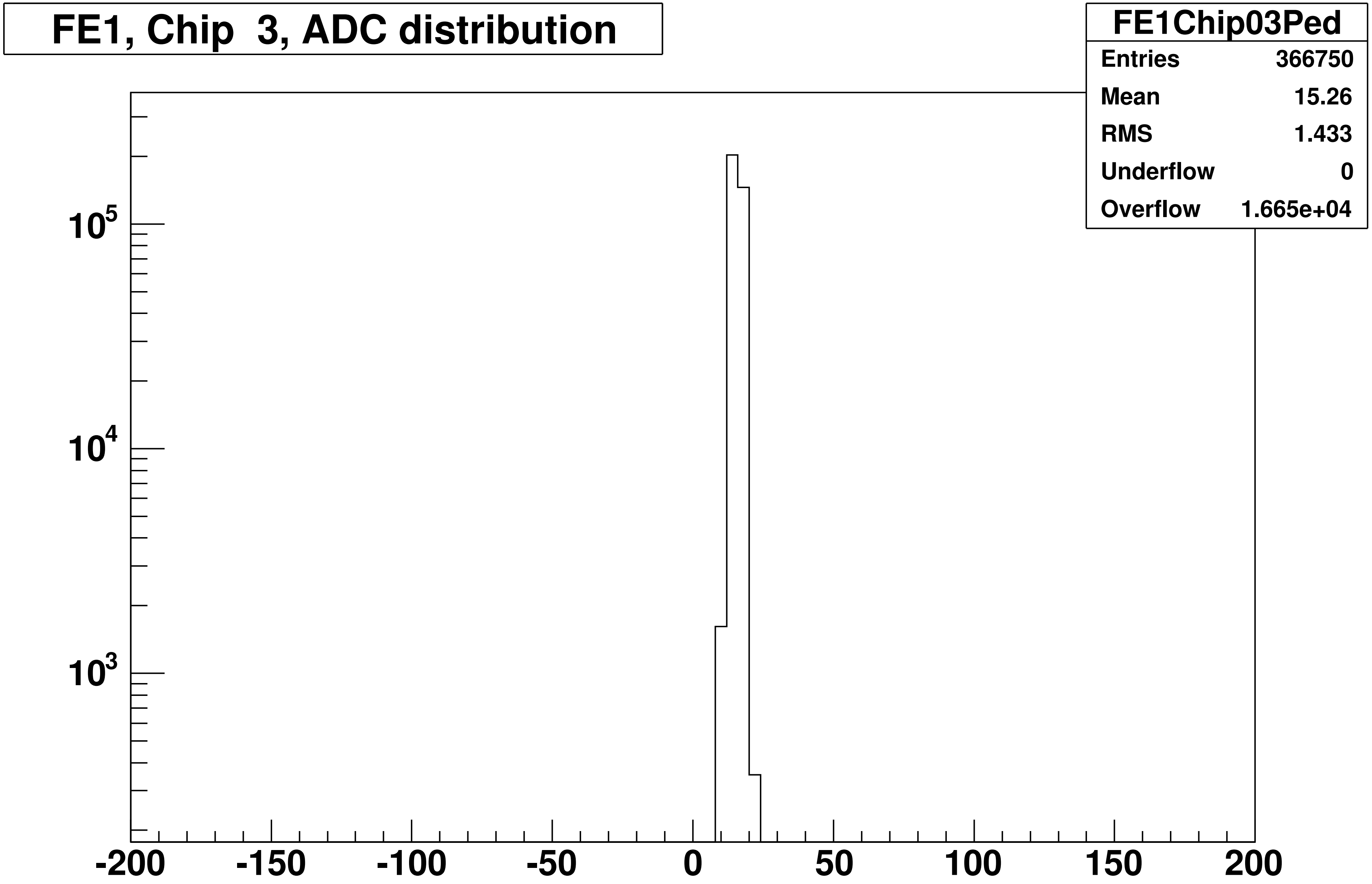


FE1, Chip 3, ADC distribution
FE1Chip03All
Entries 366750
Mean 582.3
RMS 2600
Underflow 0
Overflow 0
10
10^2
10^3
10^4
10^5
-5000
0
5000
10000
15000
20000
25000


FE1, Chip 3, ADC distribution
FE1Chip03Ped
Entries 366750
Mean 15.26
RMS 1.433
Underflow 0
Overflow 1.665e+04
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10^4
10^3
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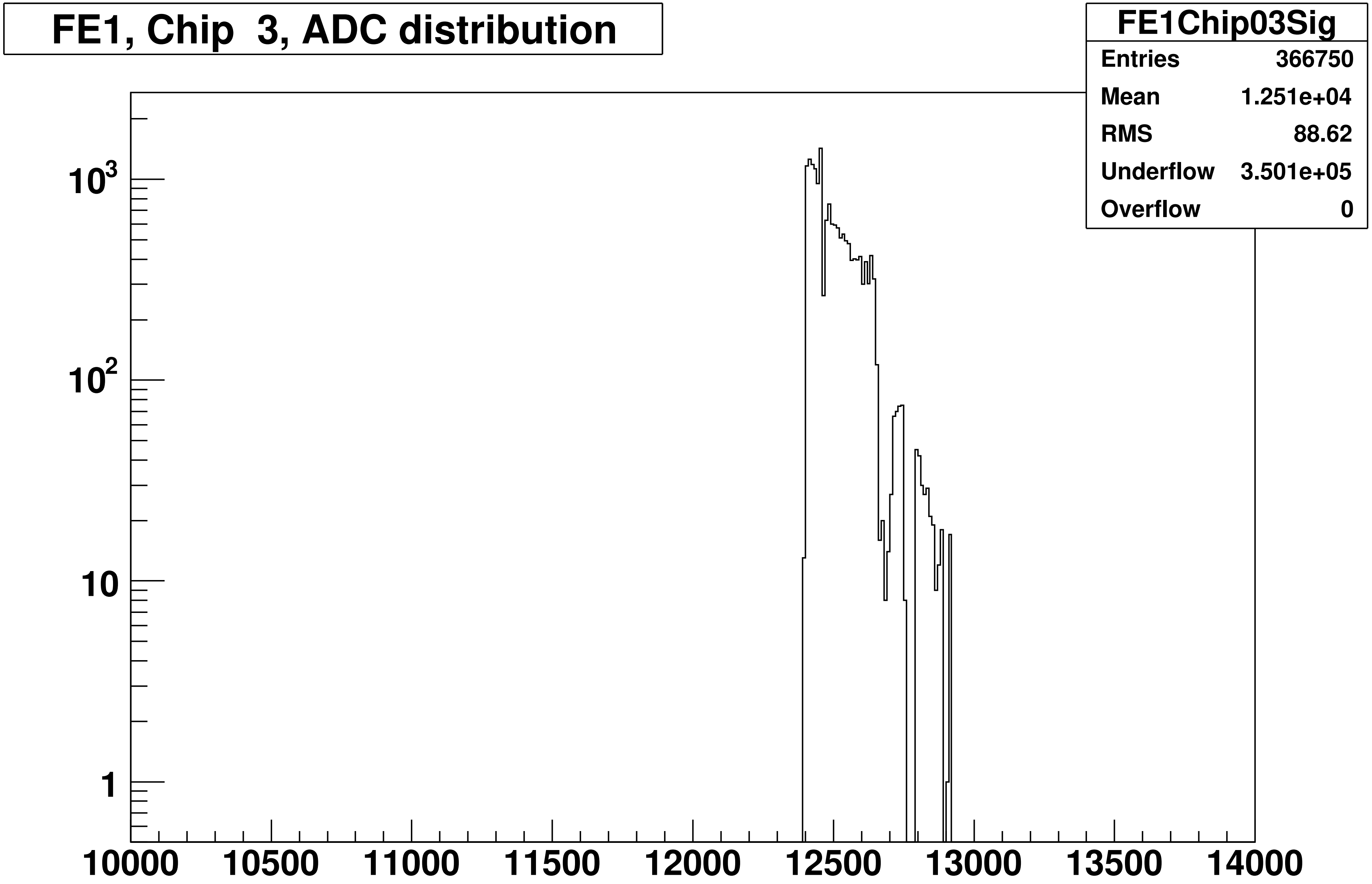
-100
-50
0
50
100
150
200



FE1, Chip 3, ADC distribution
FE1Chip03Sig
Entries 366750
Mean 1.251e+04
RMS 88.62
Underflow 3.501e+05
Overflow 0
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10^2
10
1
10000
10500
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11500
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12500
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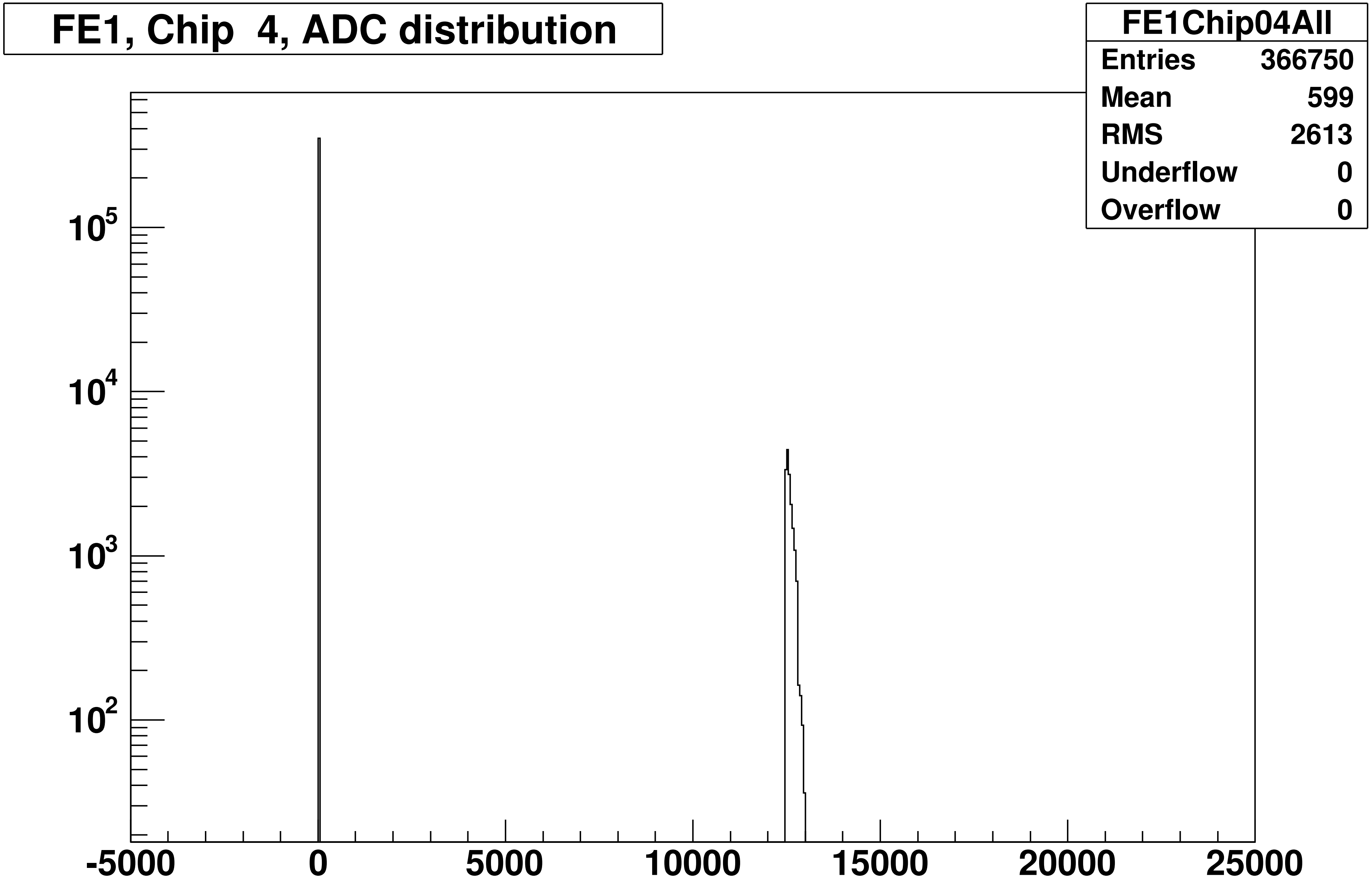
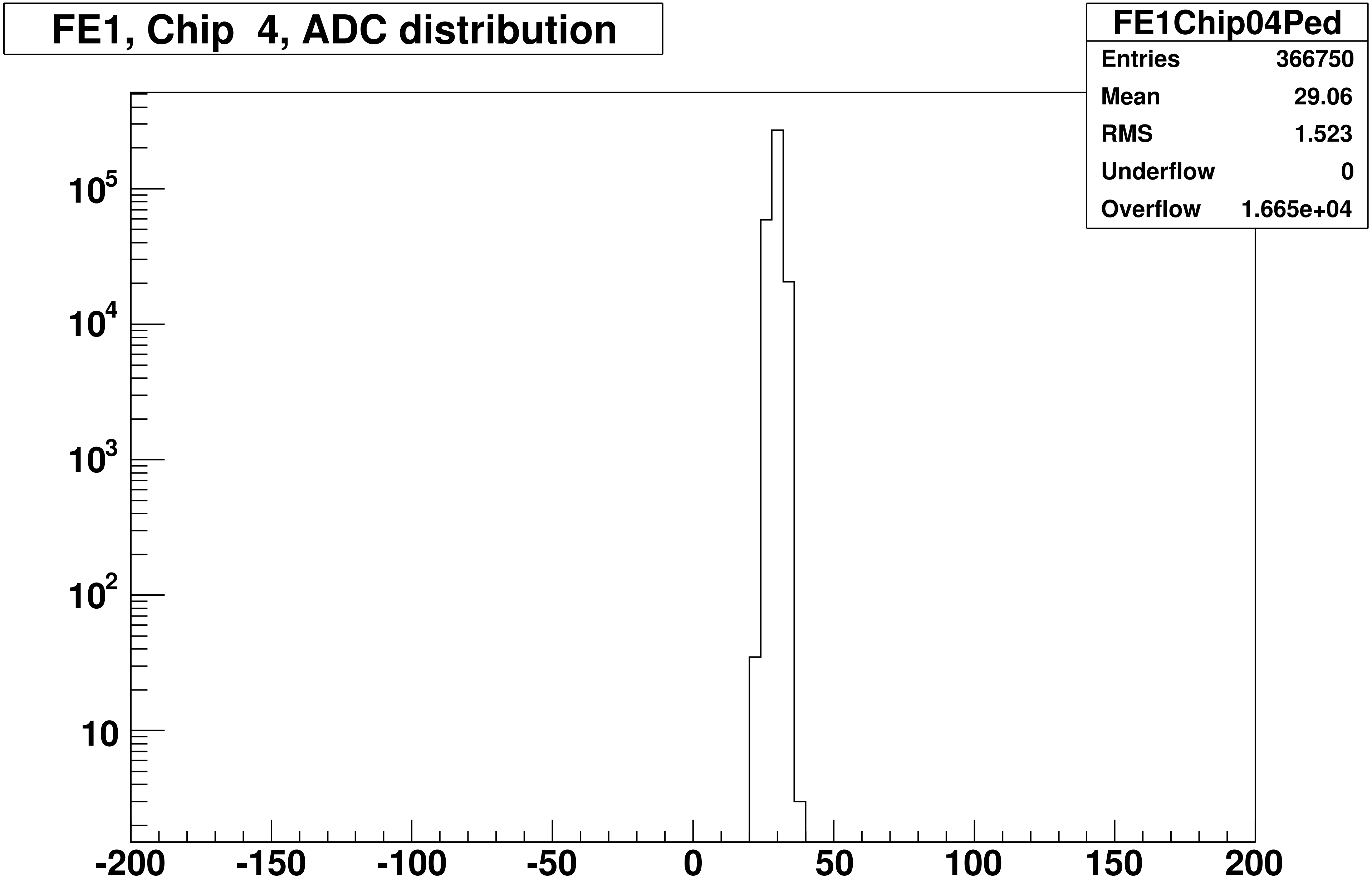
13500
14000


FE1, Chip 4, ADC distribution
FE1Chip04All
Entries 366750
Mean 599
RMS 2613
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000


FE1, Chip 4, ADC distribution
FE1Chip04Ped
Entries 366750
Mean 29.06
RMS 1.523
Underflow 0
Overflow 1.665e+04
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10^4
10^3
10^2
10
-200
-150
-100
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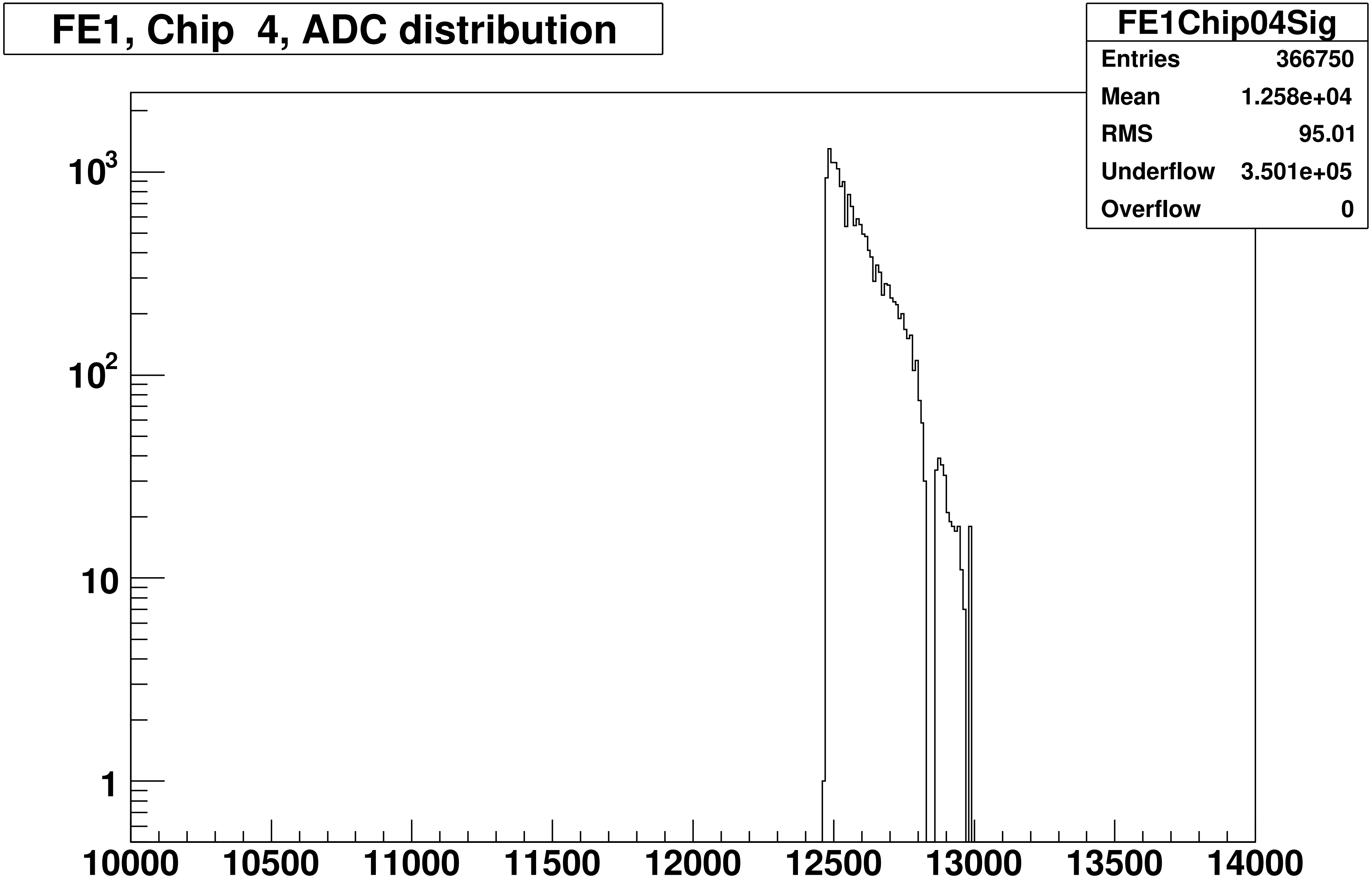
0
50
100
150
200



FE1, Chip 4, ADC distribution
FE1Chip04Sig
Entries 366750
Mean 1.258e+04
RMS 95.01
Underflow 3.501e+05
Overflow 0
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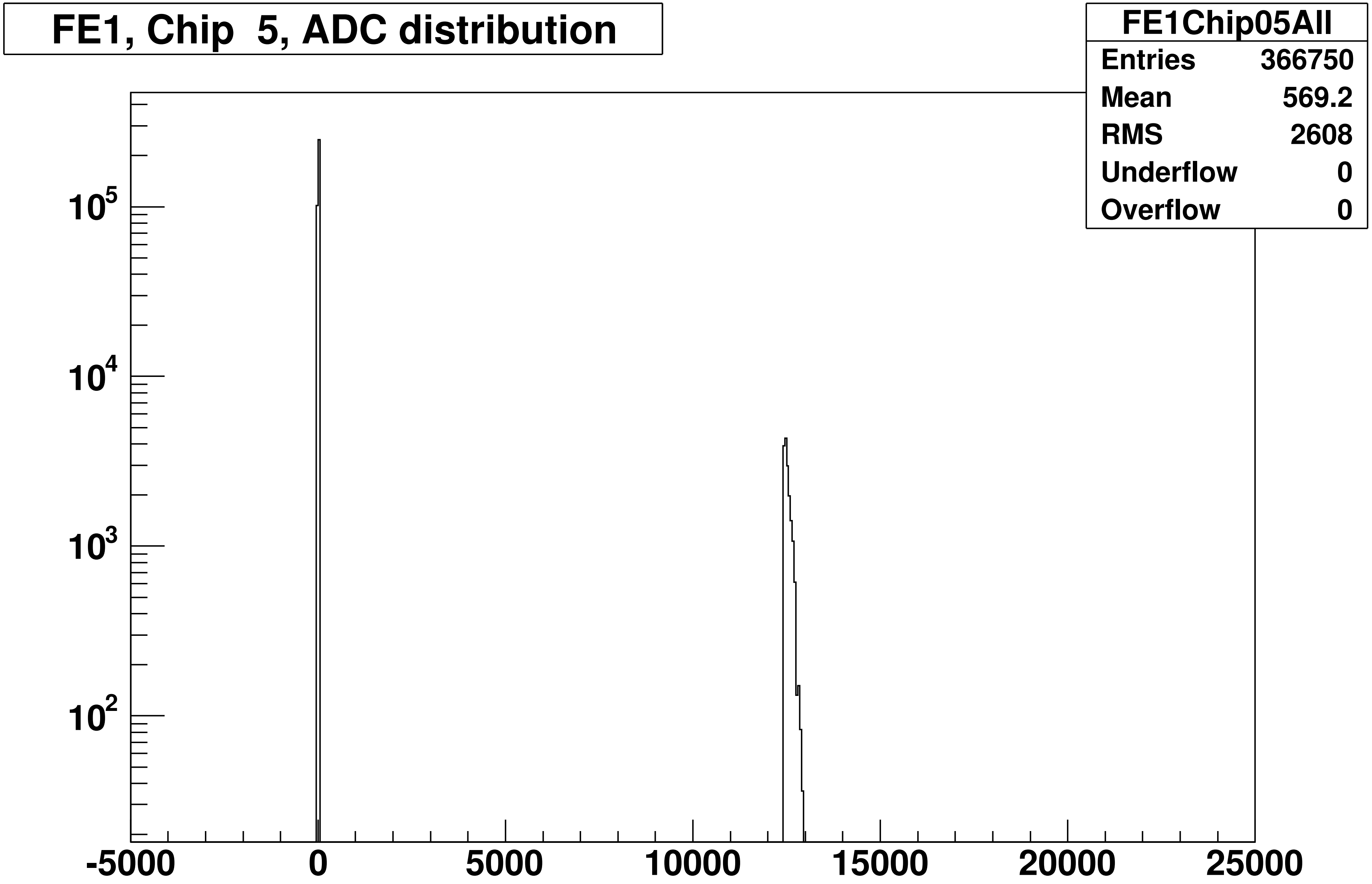
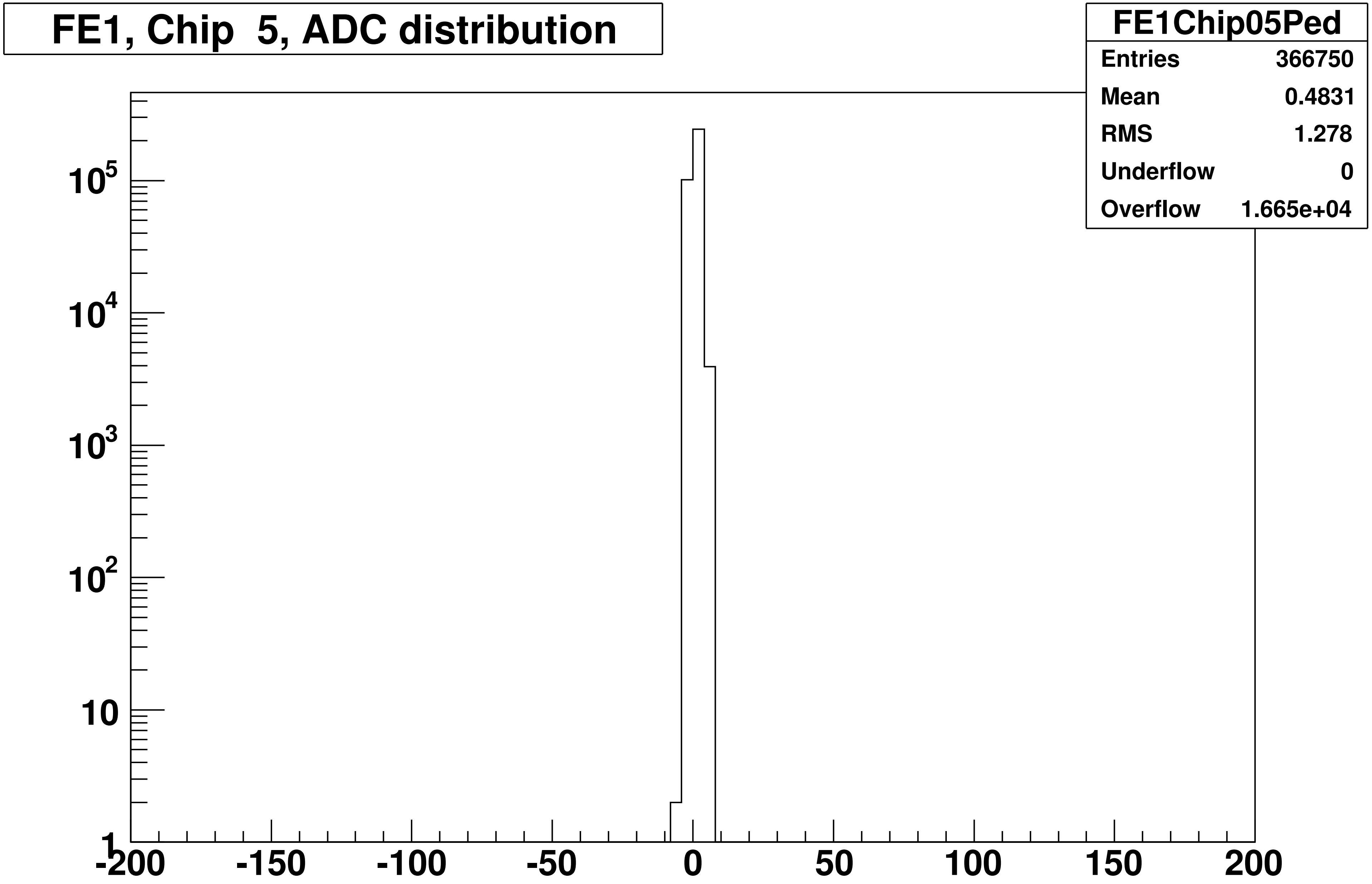
10^2
10
1
10000
10500
11000
11500
12000
12500
13000
13500
14000



FE1, Chip 5, ADC distribution
FE1Chip05All
Entries 366750
Mean 569.2
RMS 2608
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000


FE1, Chip 5, ADC distribution
FE1Chip05Ped
Entries 366750
Mean 0.4831
RMS 1.278
Underflow 0
Overflow 1.665e+04
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10^4
10^3
10^2
10
1
-200
-150
-100
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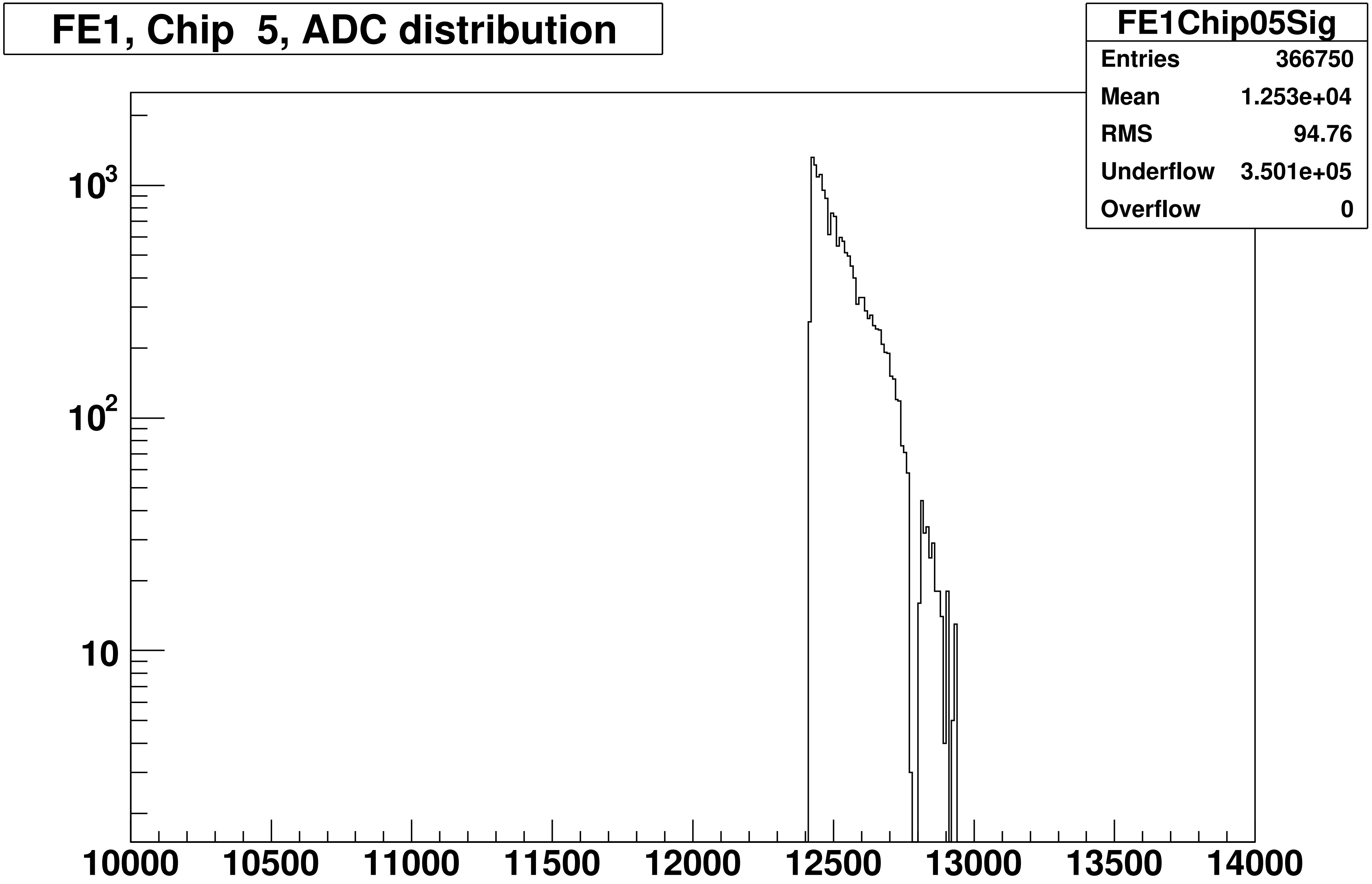
0
50
100
150
200


FE1, Chip 5, ADC distribution
FE1Chip05Sig
Entries 366750
Mean 1.253e+04
RMS 94.76
Underflow 3.501e+05
Overflow 0
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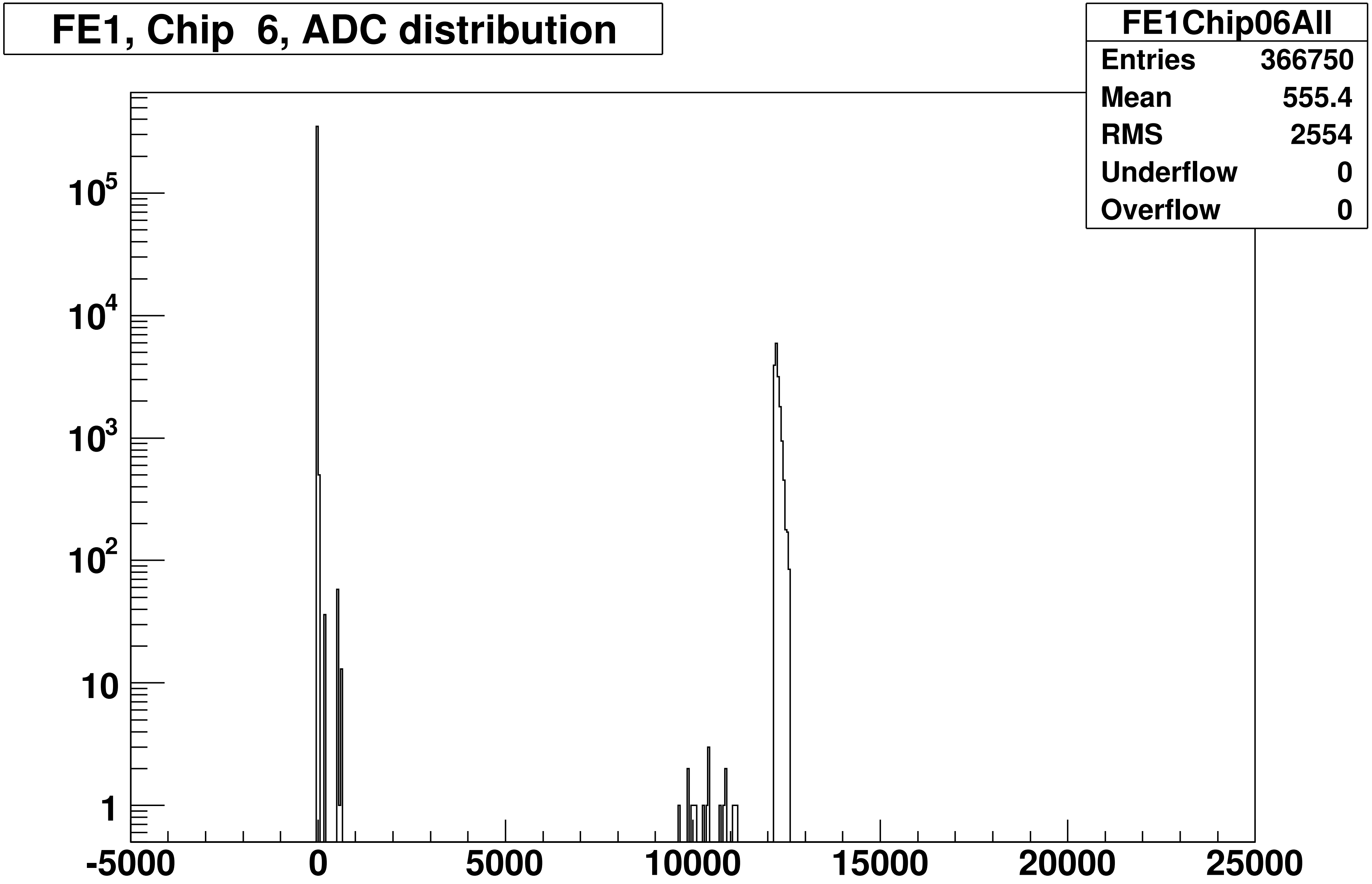
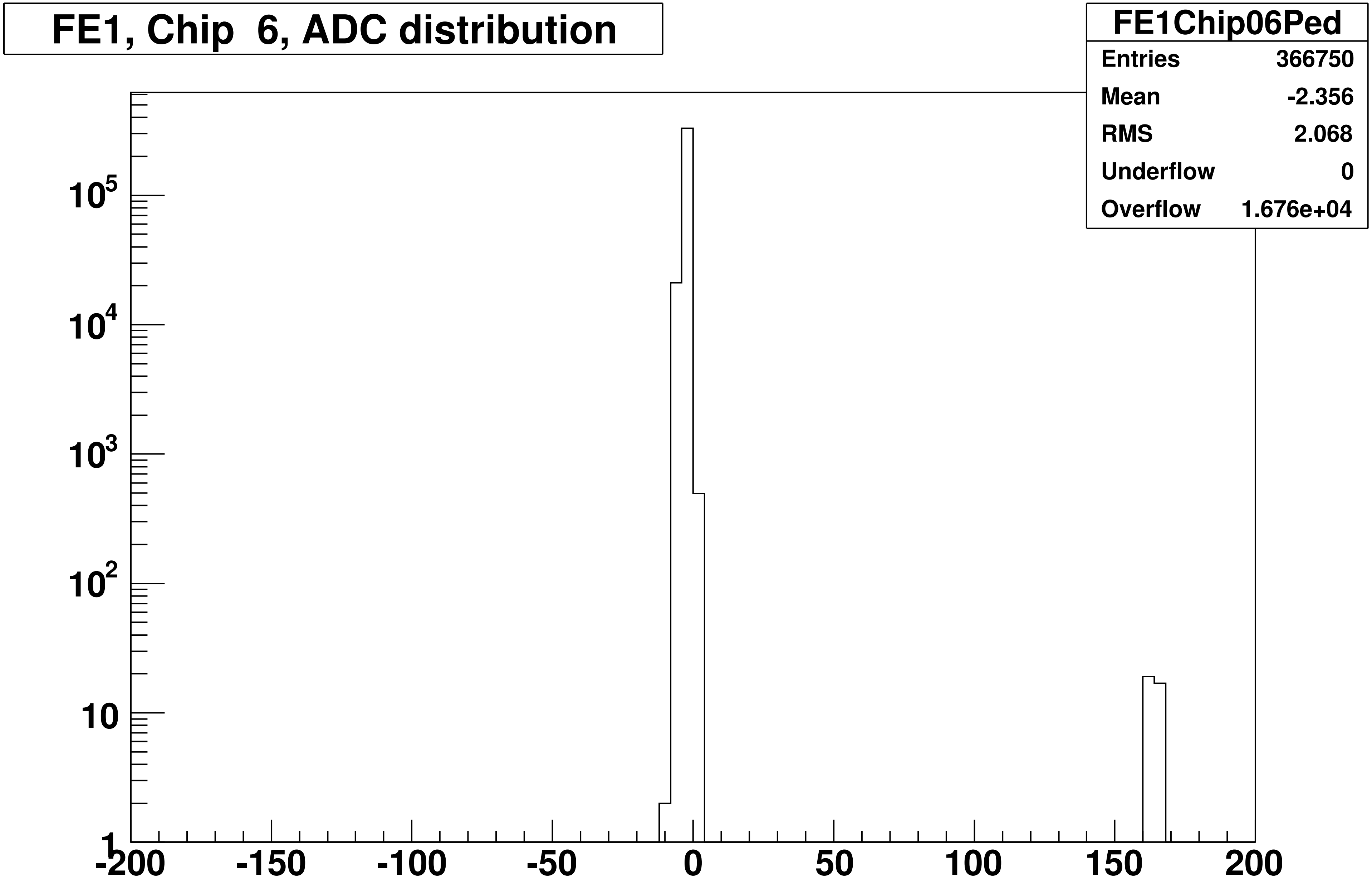
10^2
10
10000
10500
11000
11500
12000
12500
13000
13500
14000


FE1, Chip 6, ADC distribution
FE1Chip06All
Entries 366750
Mean 555.4
RMS 2554
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE1, Chip 6, ADC distribution
FE1Chip06Ped
Entries 366750
Mean -2.356
RMS 2.068
Underflow 0
Overflow 1.676e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
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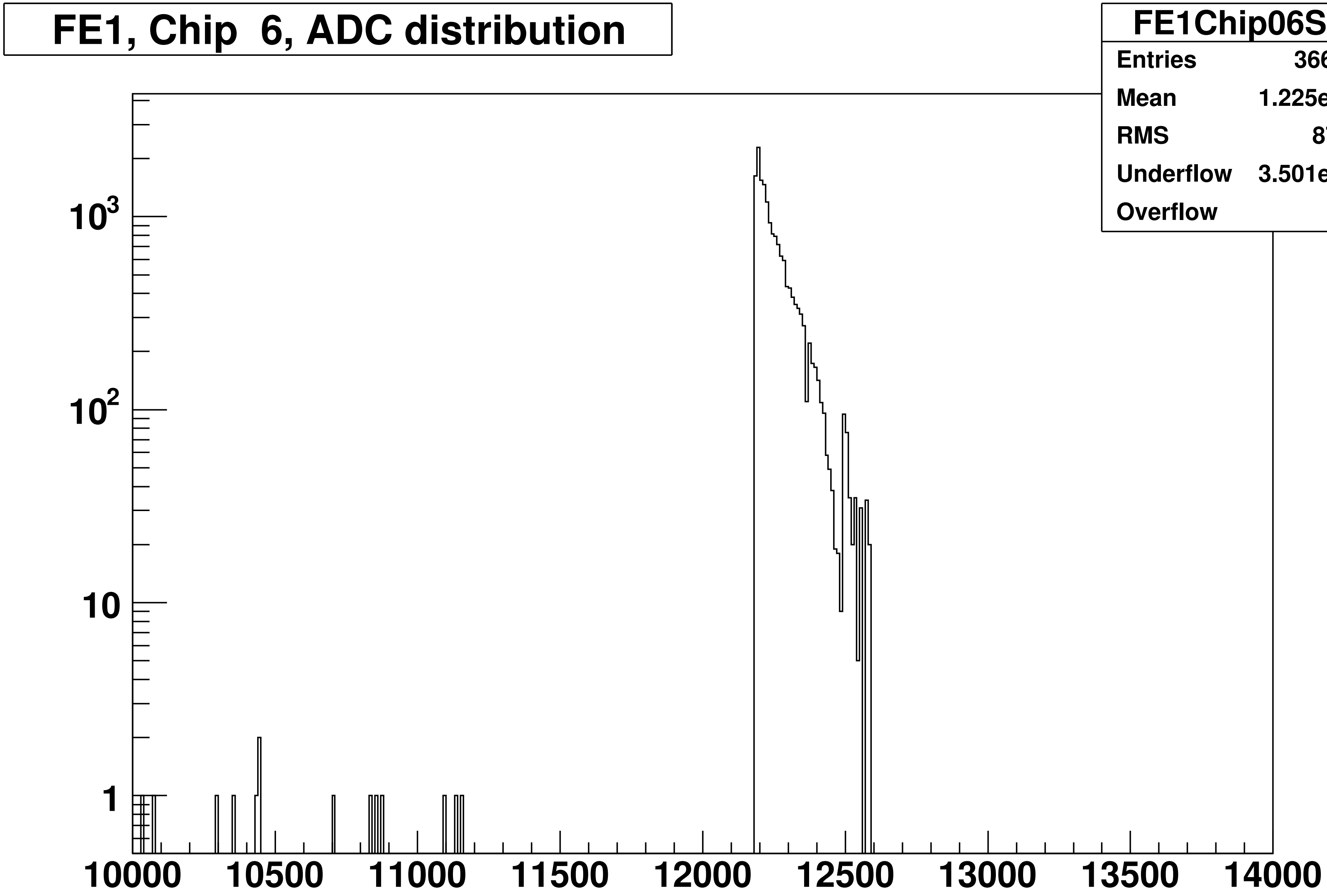
0
50
100
150
200


FE1, Chip 6, ADC distribution
FE1Chip06Sig
Entries 366750
Mean 1.225e+04
RMS 87.66
Underflow 3.501e+05
Overflow 0
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10^2
10
1
10000
10500
11000
11500
12000
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13000
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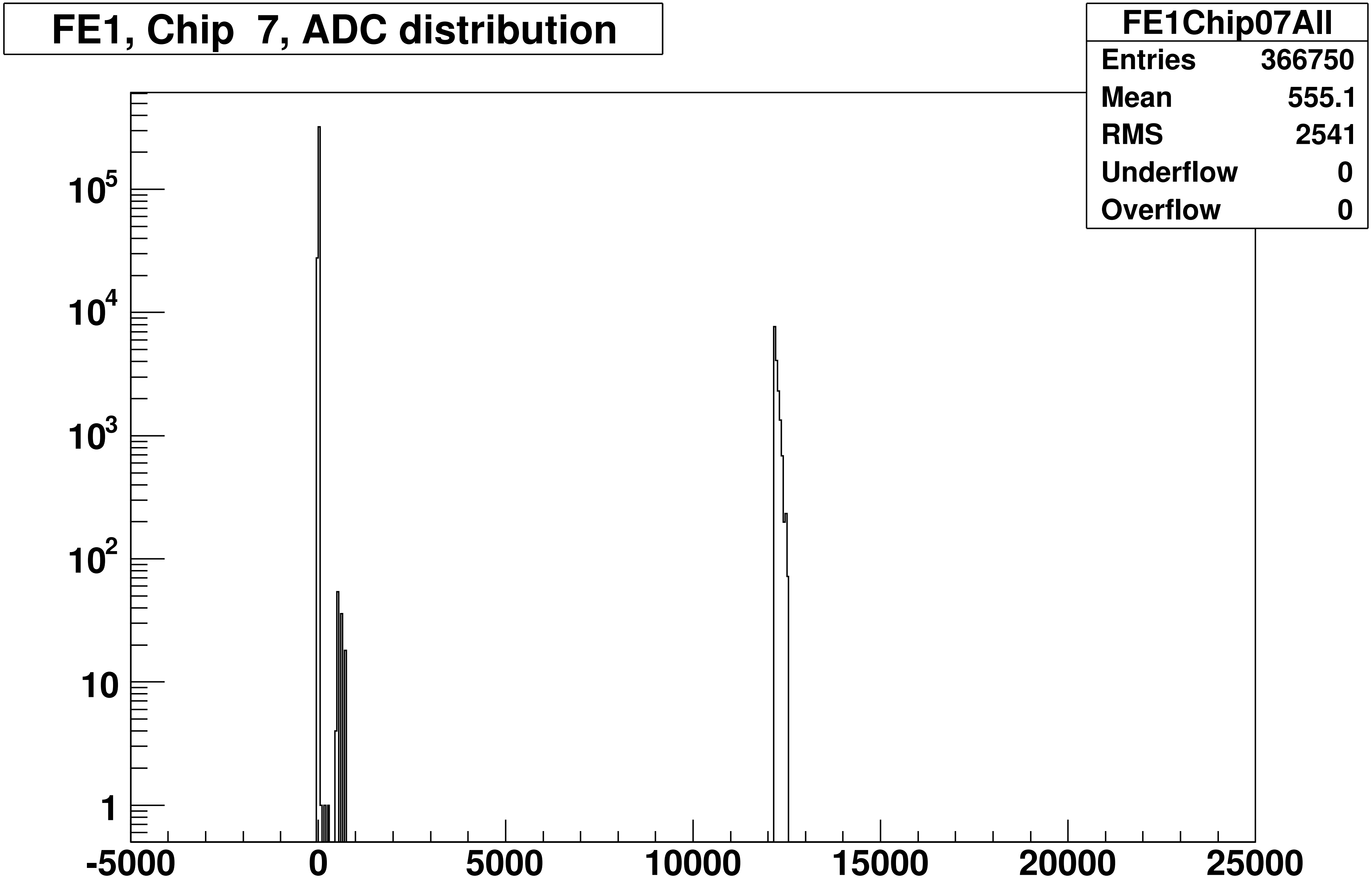

FE1, Chip 7, ADC distribution
FE1Chip07All
Entries 366750
Mean 555.1
RMS 2541
Underflow 0
Overflow 0
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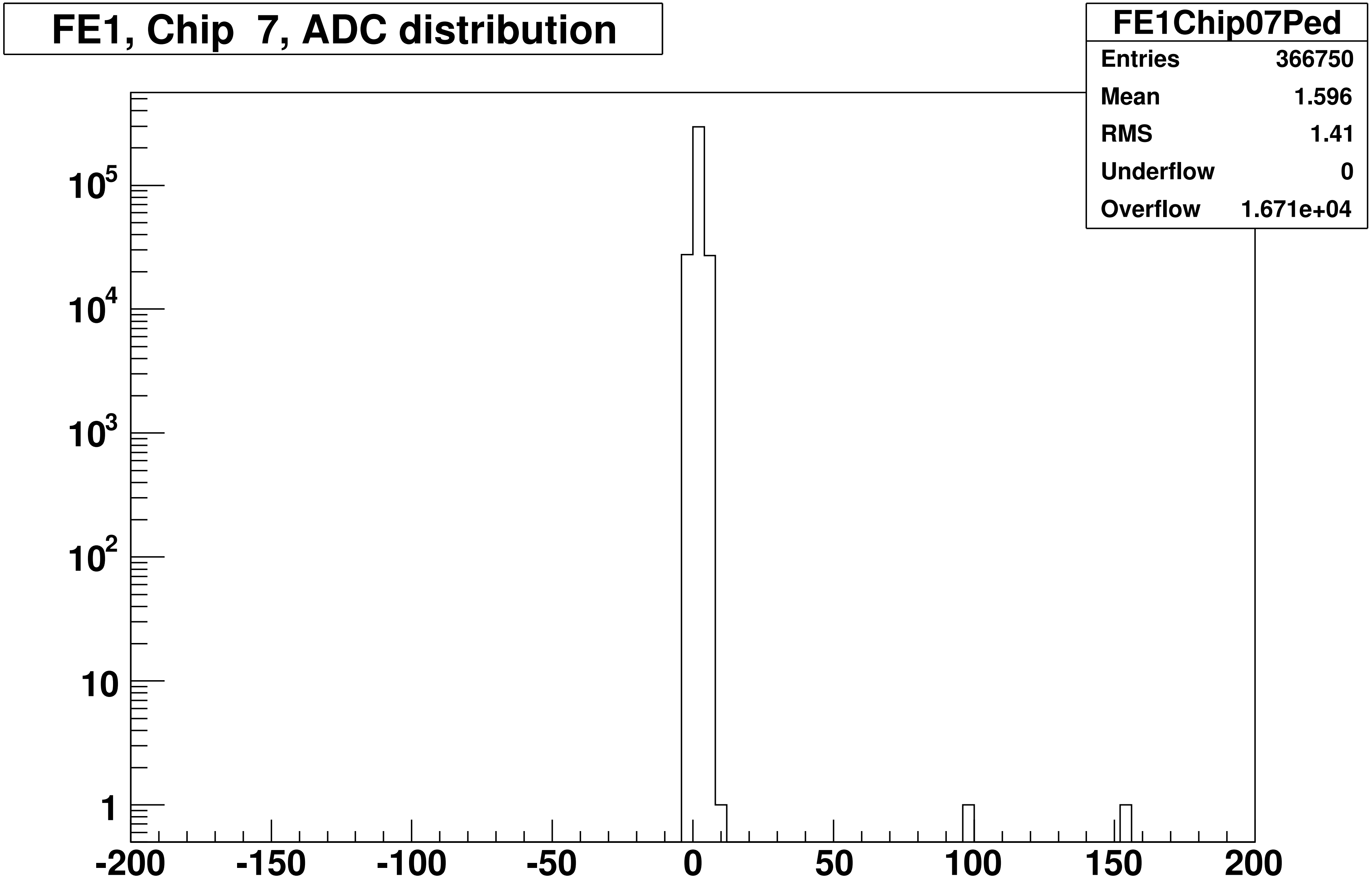
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE1, Chip 7, ADC distribution
FE1Chip07Ped
Entries 366750
Mean 1.596
RMS 1.41
Underflow 0
Overflow 1.671e+04
10^5
10^4
10^3
10^2
10
1
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-150
-100
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50
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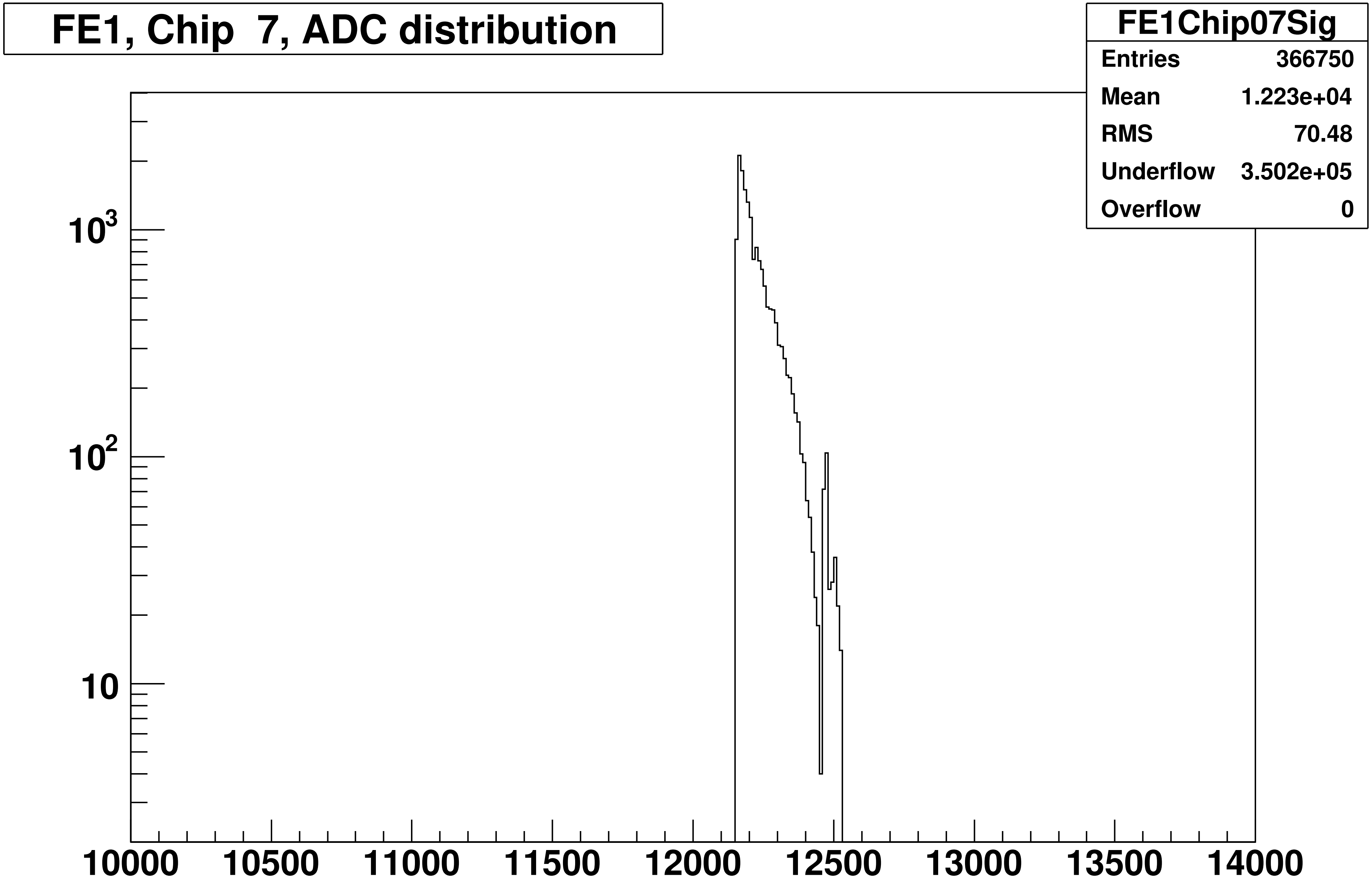
150
200


FE1, Chip 7, ADC distribution
FE1Chip07Sig
Entries 366750
Mean 1.223e+04
RMS 70.48
Underflow 3.502e+05
Overflow 0
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10^2
10
10000
10500
11000
11500
12000
12500
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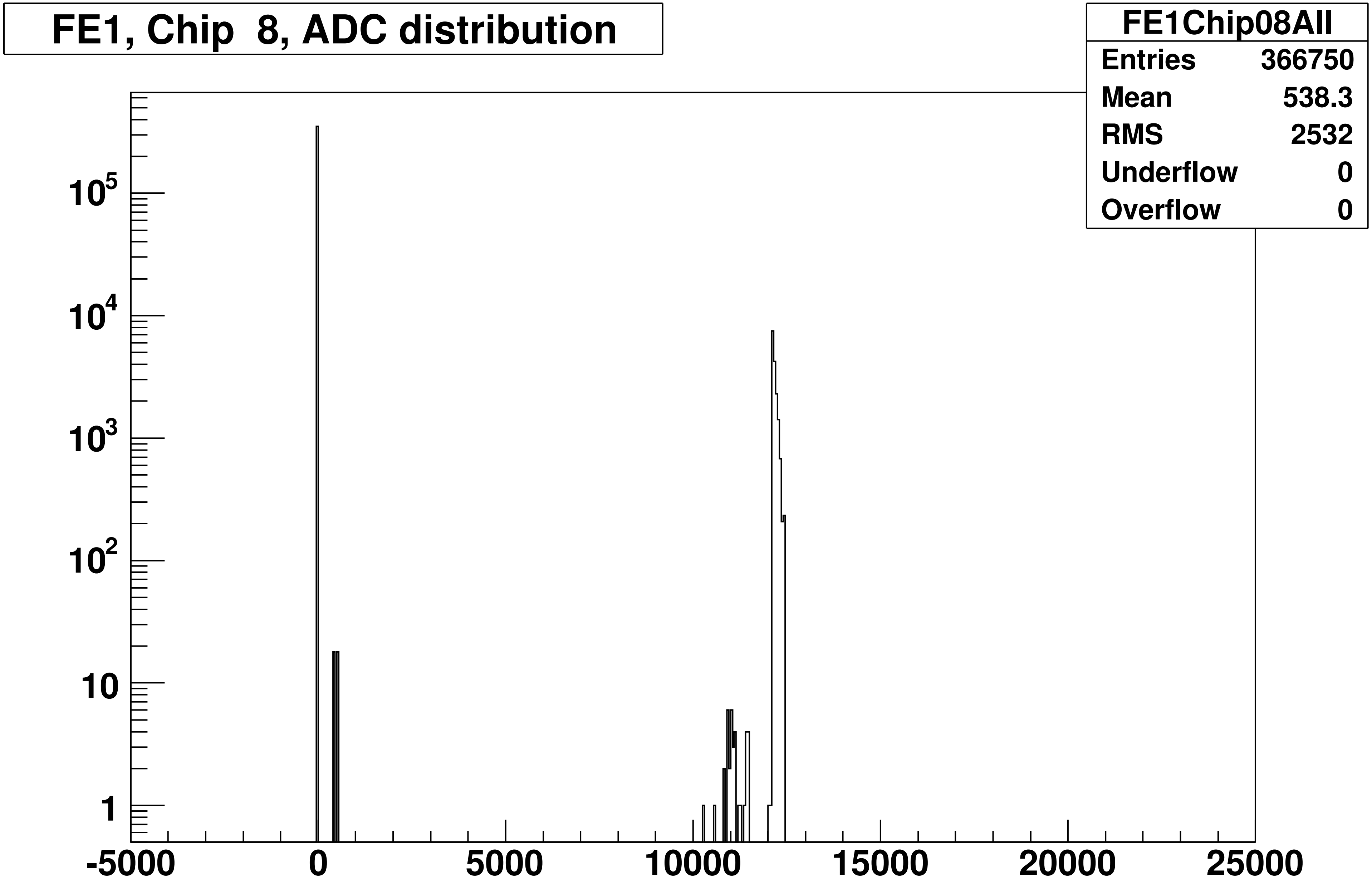
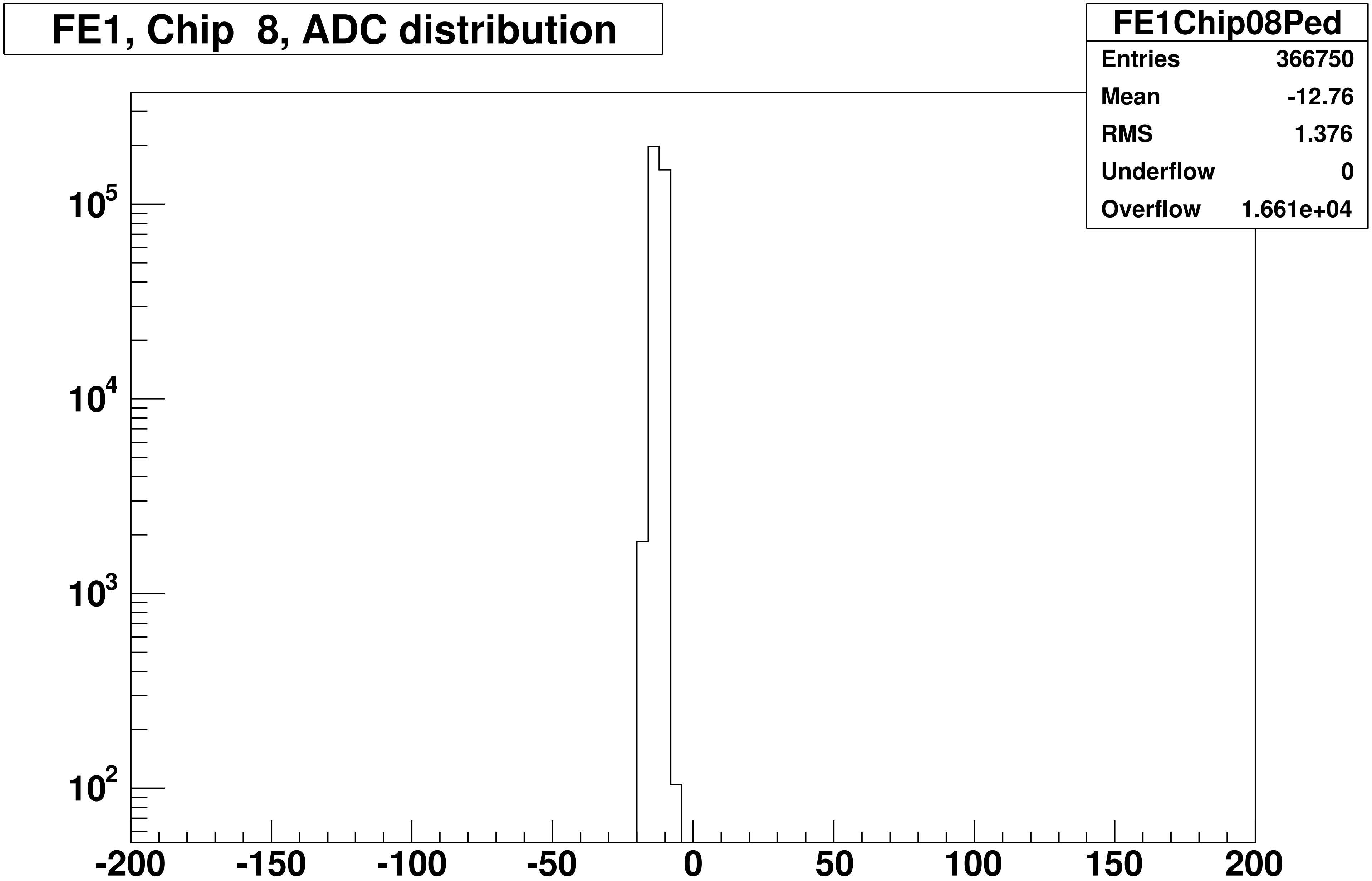

FE1, Chip 8, ADC distribution
FE1Chip08All
Entries 366750
Mean 538.3
RMS 2532
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE1, Chip 8, ADC distribution
FE1Chip08Ped
Entries 366750
Mean -12.76
RMS 1.376
Underflow 0
Overflow 1.661e+04
10^5
10^4
10^3
10^2
-200
-150
-100
-50
0
50
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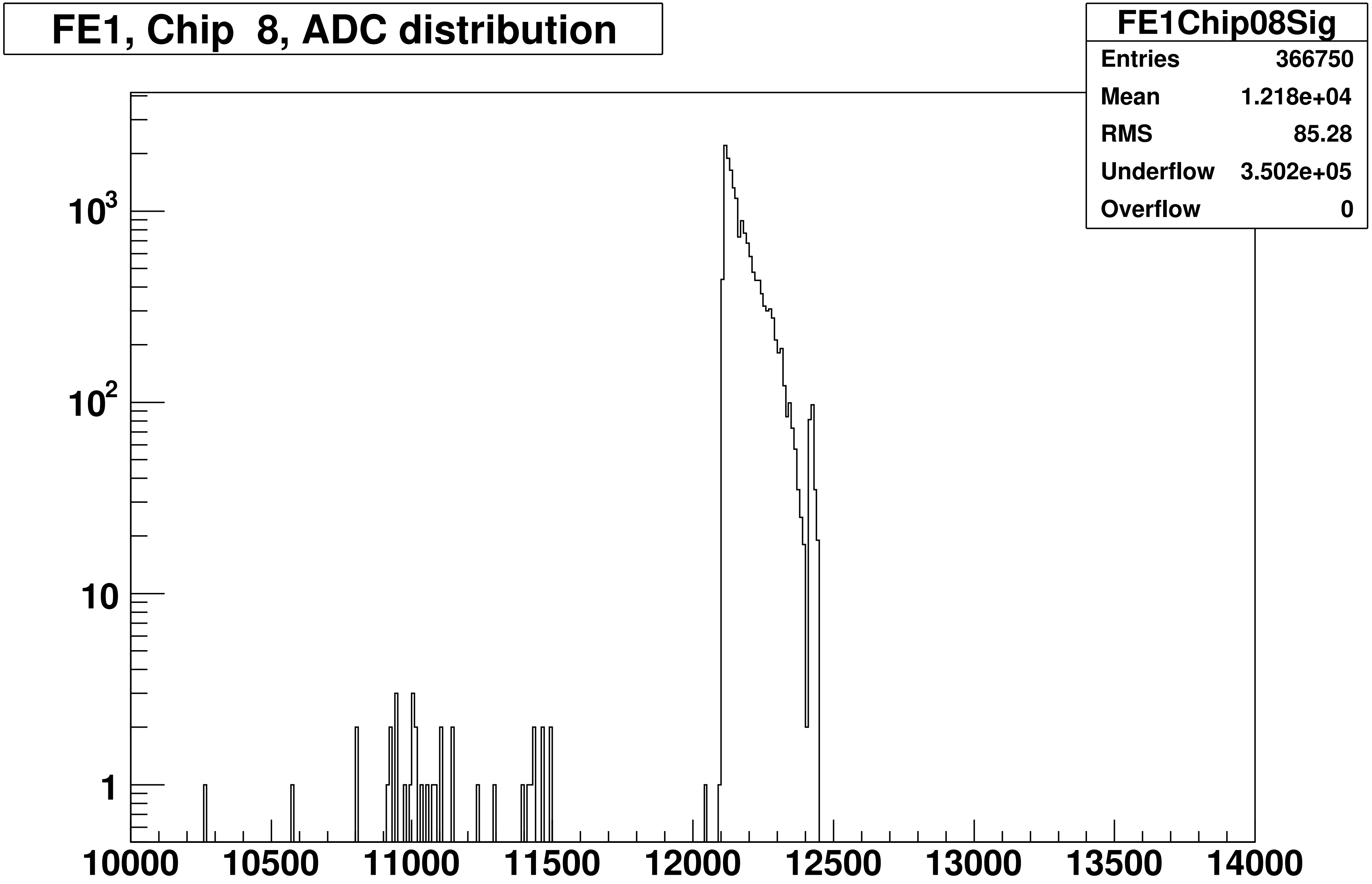

FE1, Chip 8, ADC distribution
FE1Chip08Sig
Entries 366750
Mean 1.218e+04
RMS 85.28
Underflow 3.502e+05
Overflow 0
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10^2
10
1
10000
10500
11000
11500
12000
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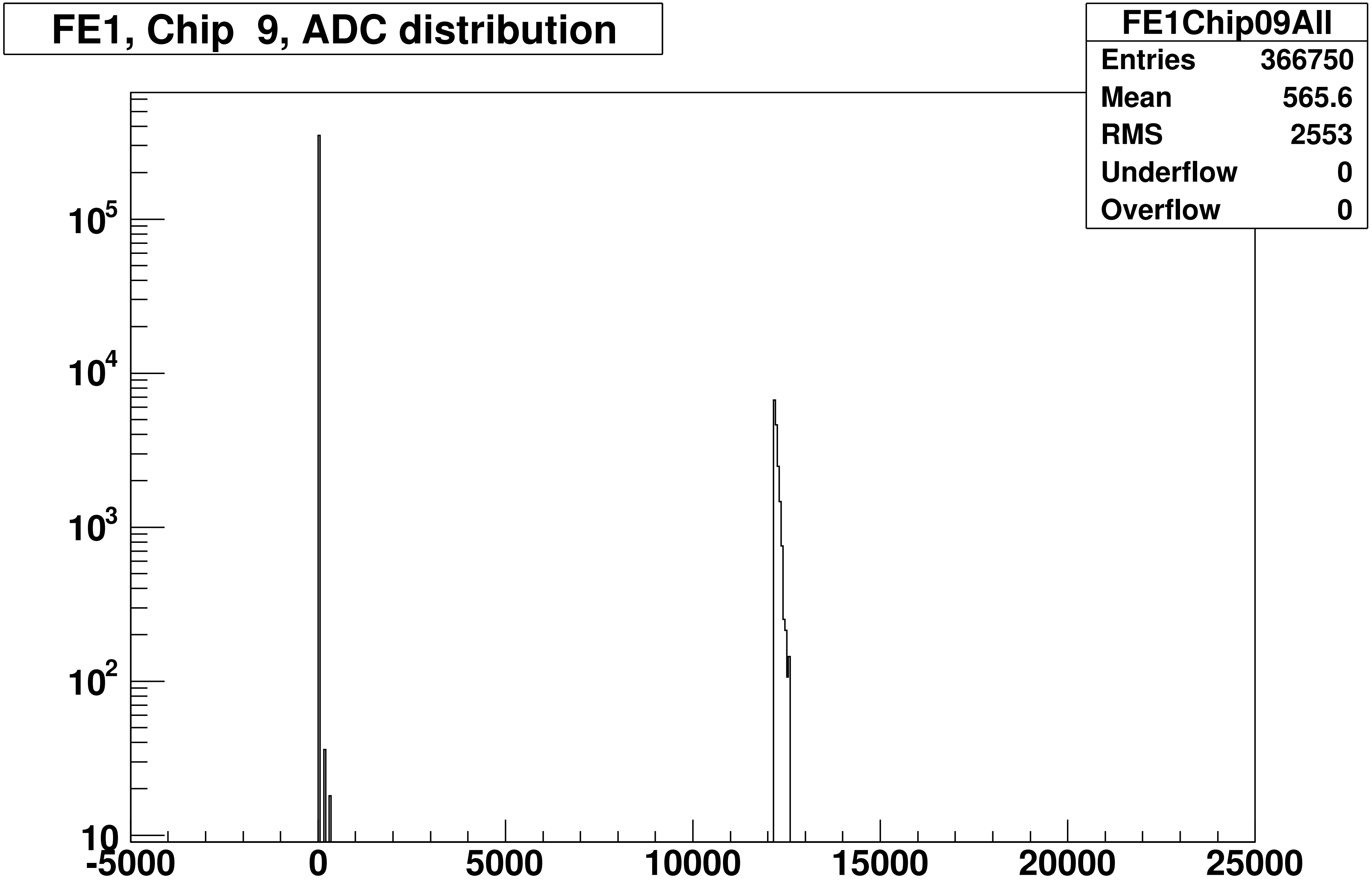
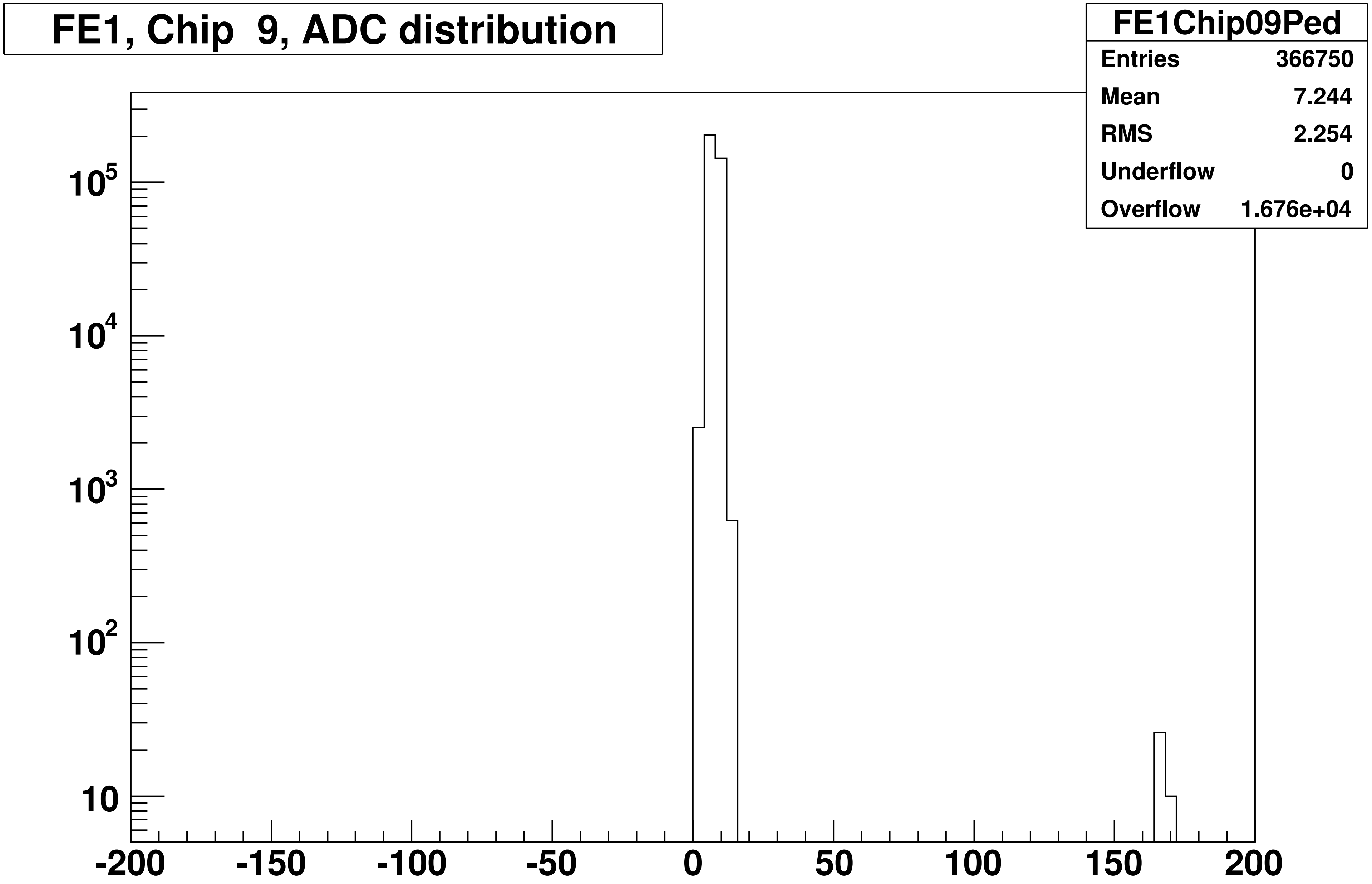
14000


FE1, Chip 9, ADC distribution
FE1Chip09All
Entries 366750
Mean 565.6
RMS 2553
Underflow 0
Overflow 0
10
10^2
10^3
10^4
10^5
-5000
0
5000
10000
15000
20000
25000



FE1, Chip 9, ADC distribution
FE1Chip09Ped
Entries 366750
Mean 7.244
RMS 2.254
Underflow 0
Overflow 1.676e+04
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10^4
10^3
10^2
10
-200
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-100
-50
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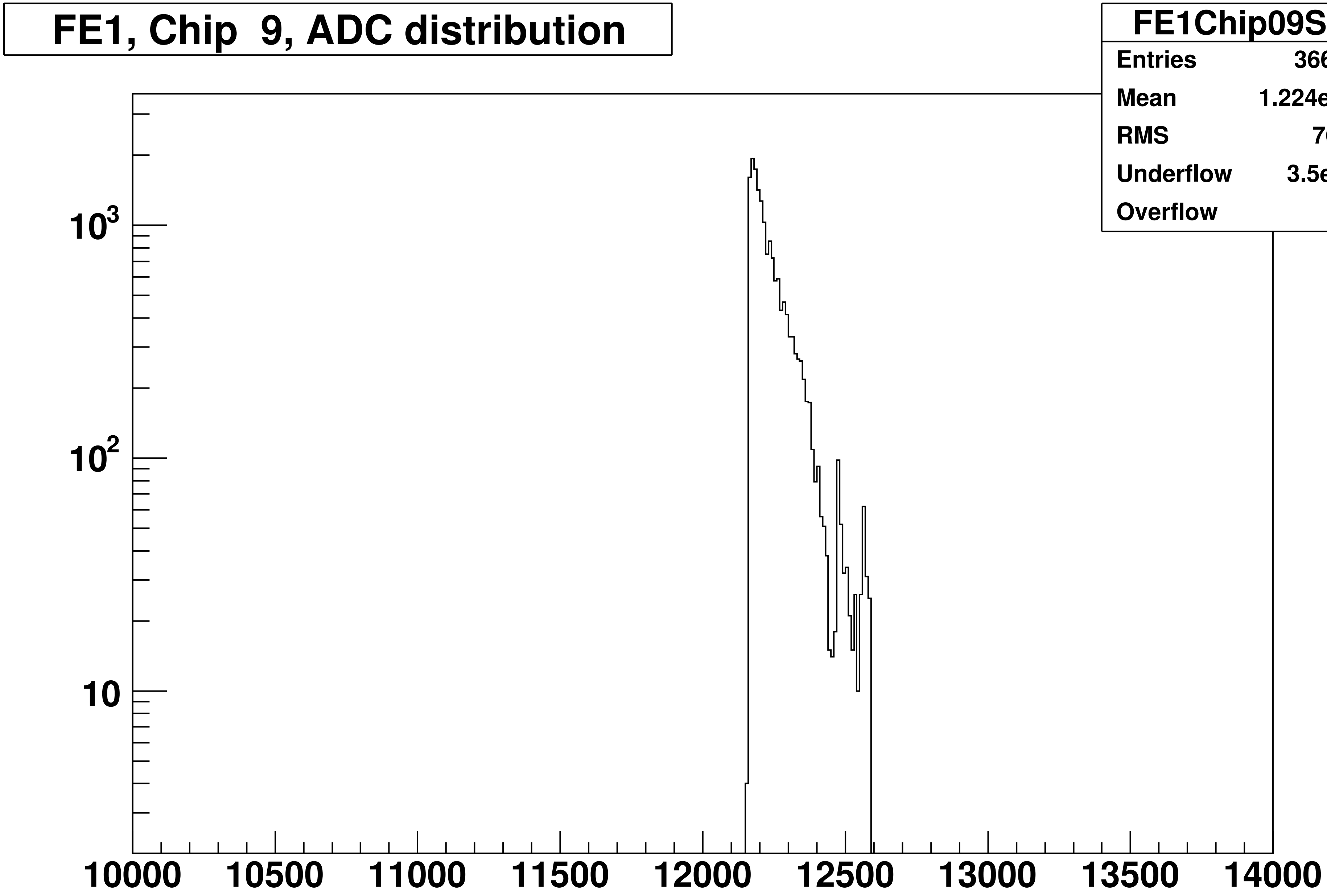
150
200


FE1, Chip 9, ADC distribution
FE1Chip09Sig
Entries 366750
Mean 1.224e+04
RMS 76.75
Underflow 3.5e+05
Overflow 0
10^3
10^2
10
10000
10500
11000
11500
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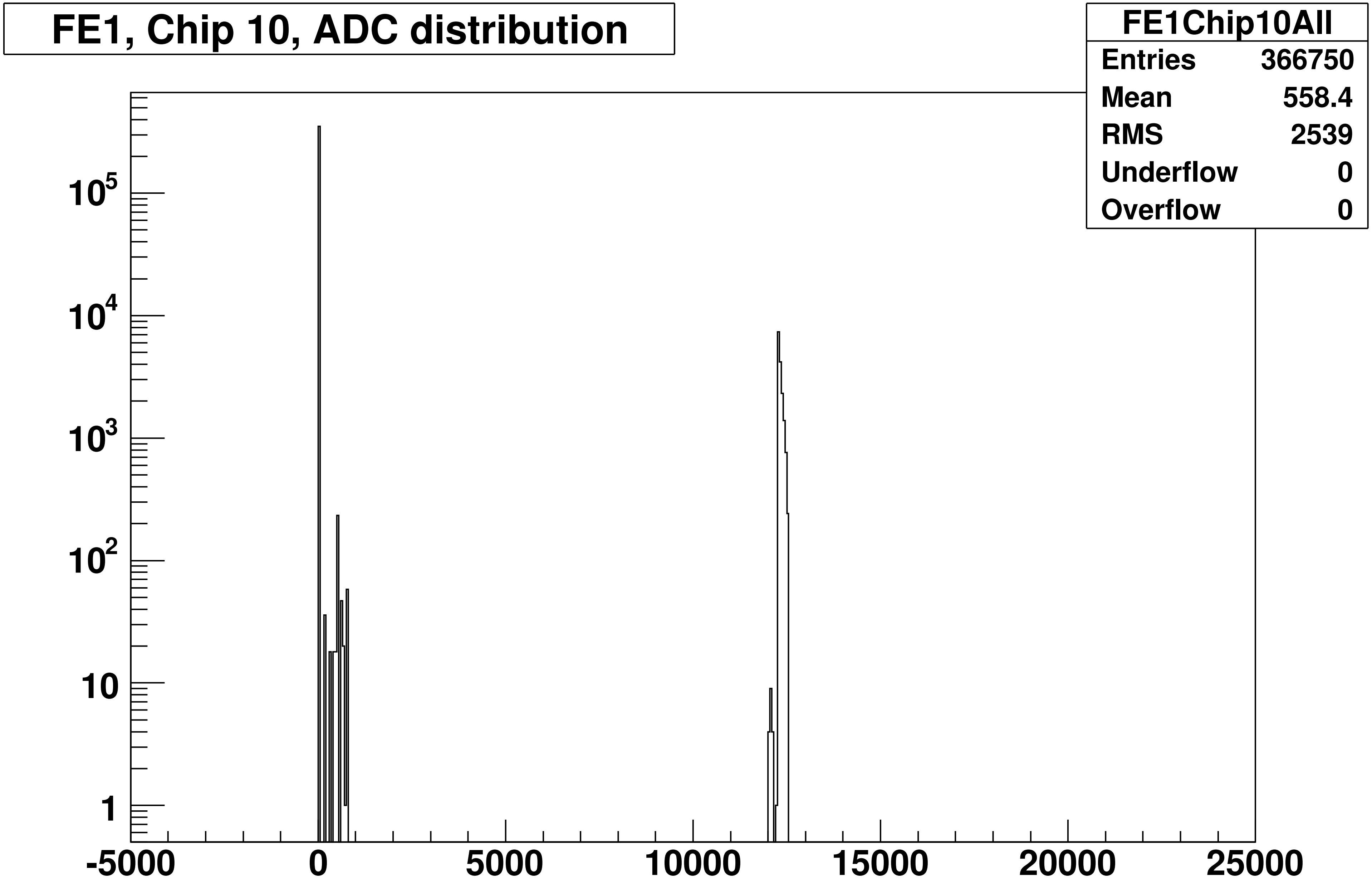
FE1, Chip 10, ADC distribution
FE1Chip10All
Entries 366750
Mean 558.4
RMS 2539
Underflow 0
Overflow 0
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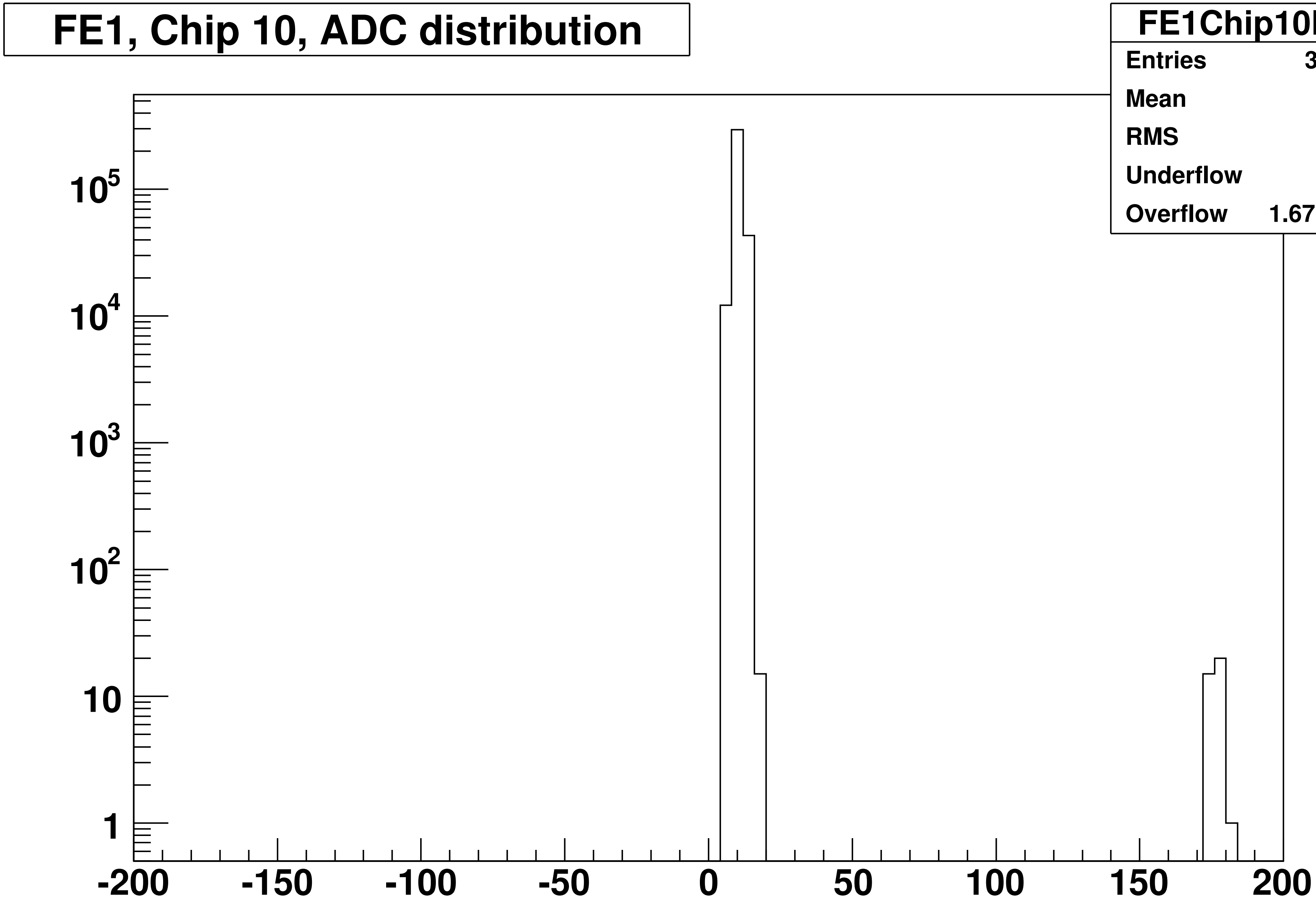
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE1, Chip 10, ADC distribution
FE1Chip10Ped
Entries 366750
Mean 10.1
RMS 2.18
Underflow 0
Overflow 1.672e+04
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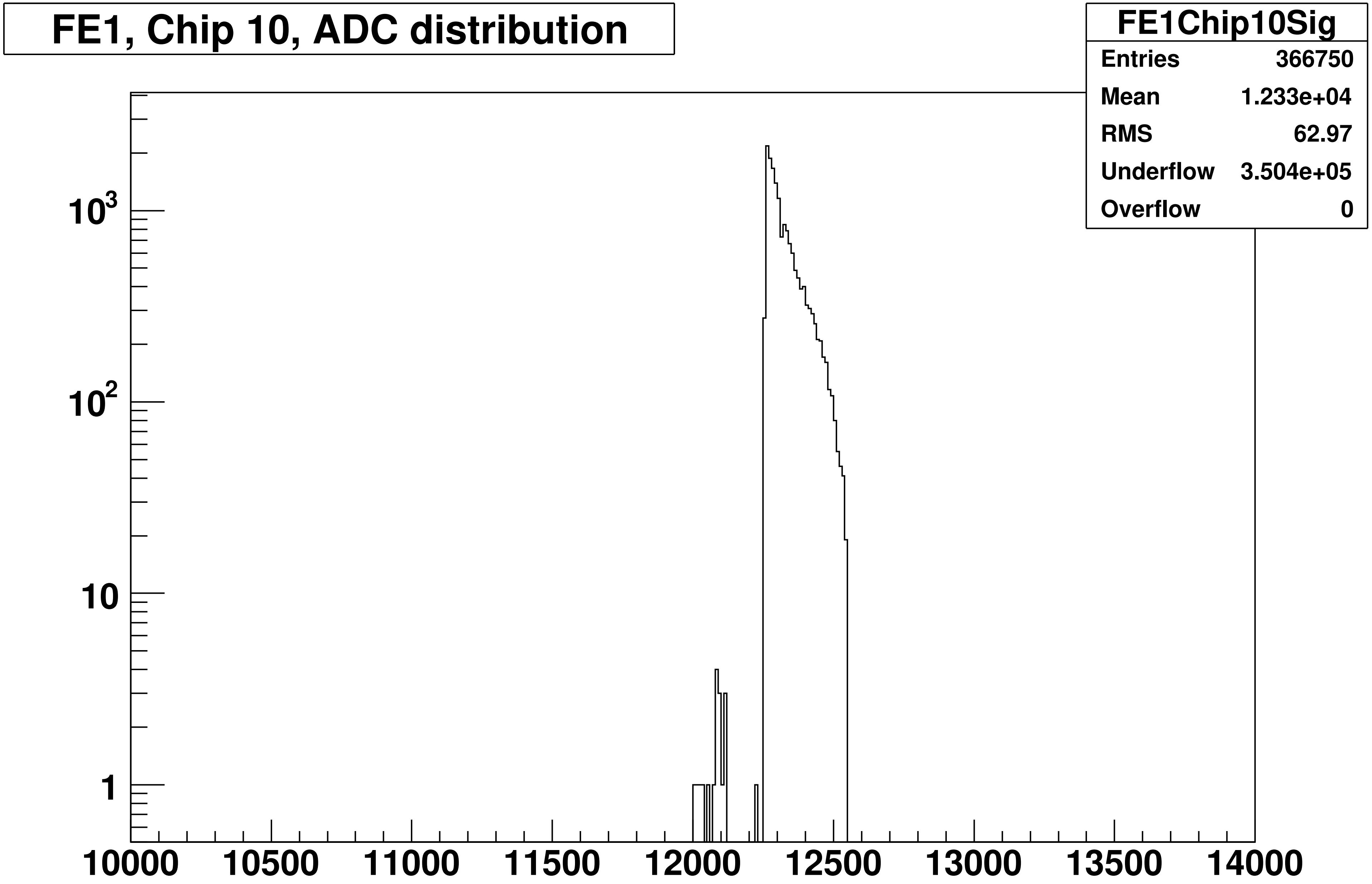
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
200


FE1, Chip 10, ADC distribution
FE1Chip10Sig
Entries 366750
Mean 1.233e+04
RMS 62.97
Underflow 3.504e+05
Overflow 0
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10^2
10
1
10000
10500
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11500
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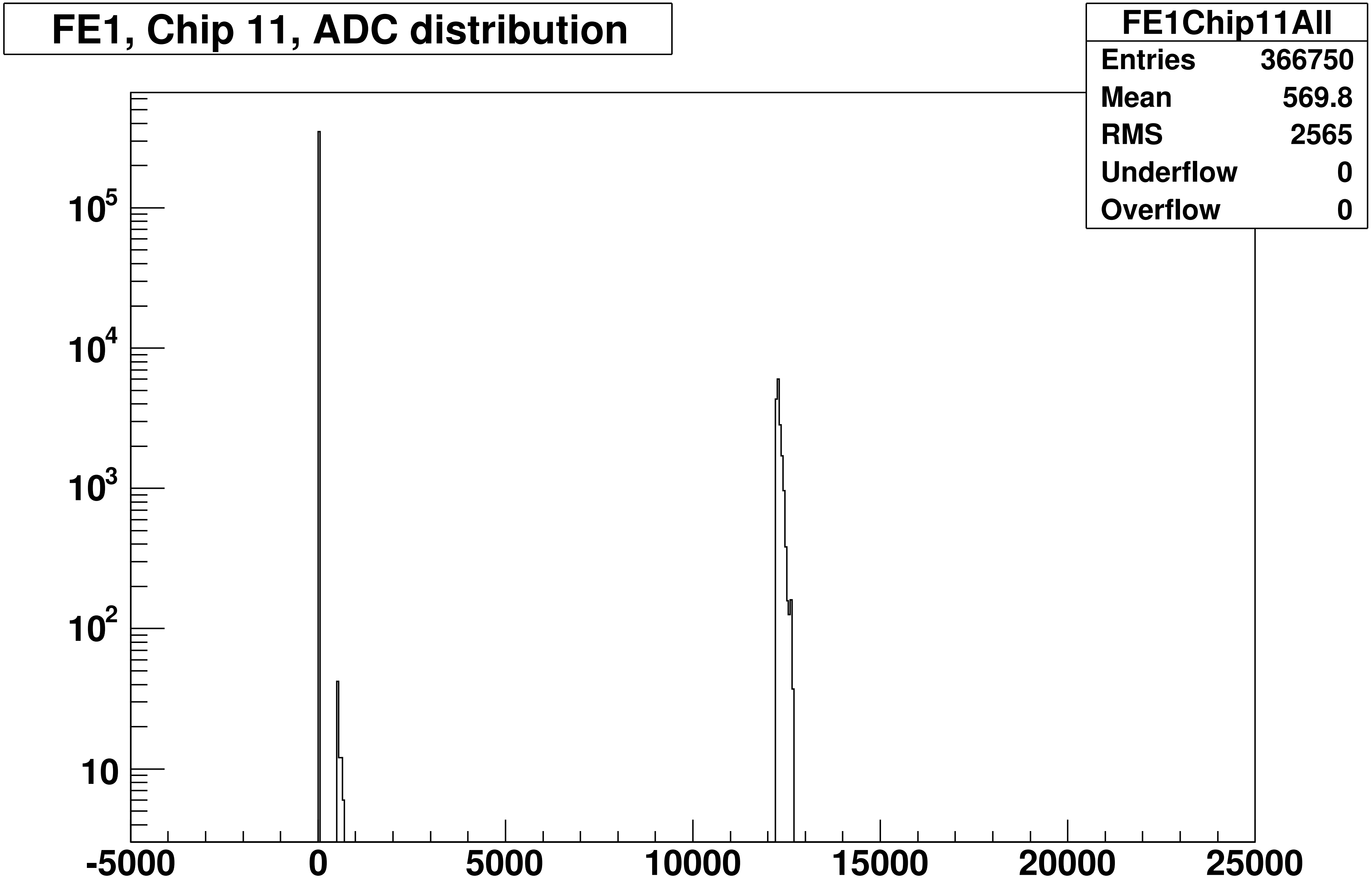
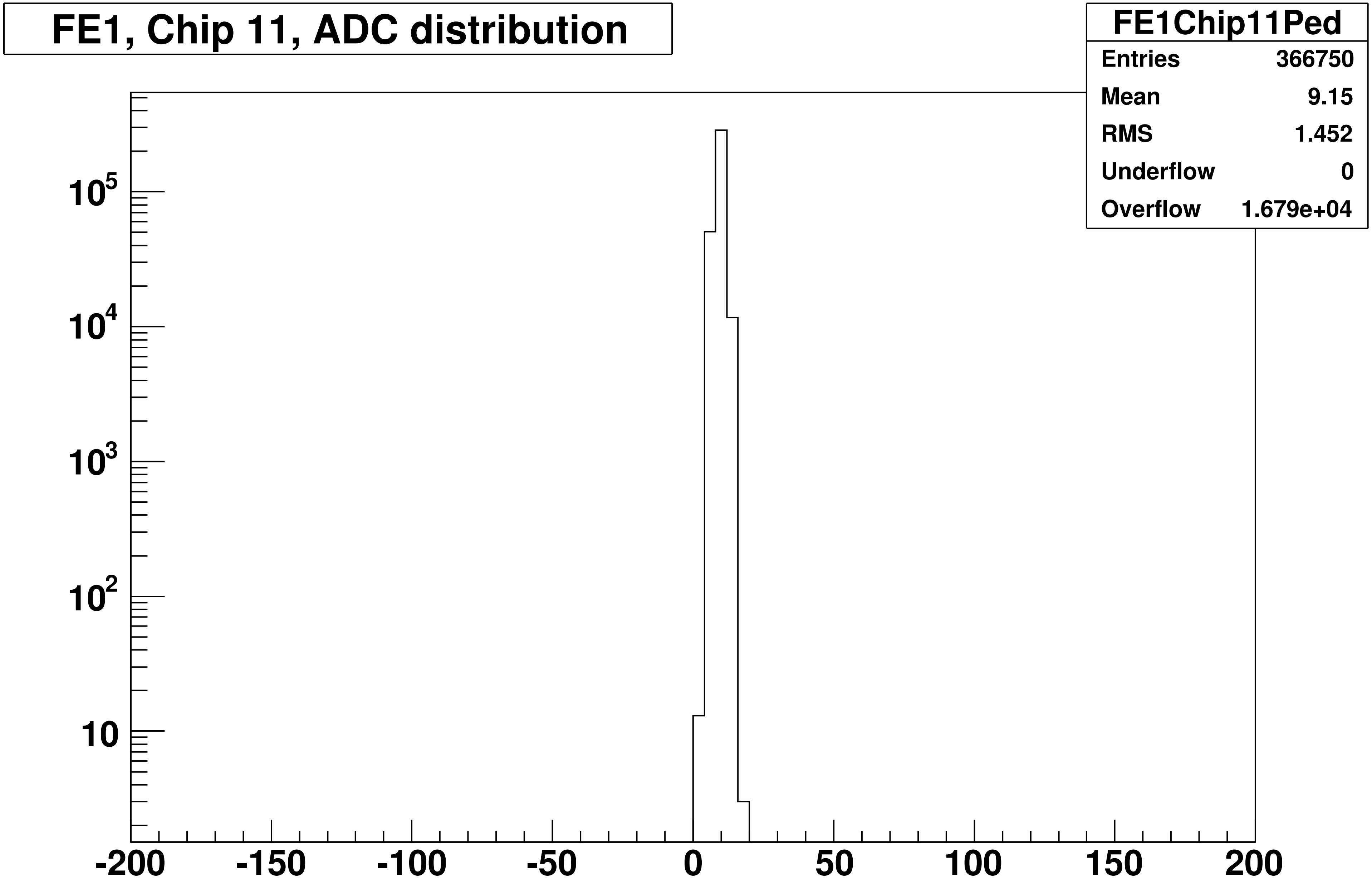

FE1, Chip 11, ADC distribution
FE1Chip11All
Entries 366750
Mean 569.8
RMS 2565
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE1, Chip 11, ADC distribution
FE1Chip11Ped
Entries 366750
Mean 9.15
RMS 1.452
Underflow 0
Overflow 1.679e+04
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10^4
10^3
10^2
10
-200
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-100
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150
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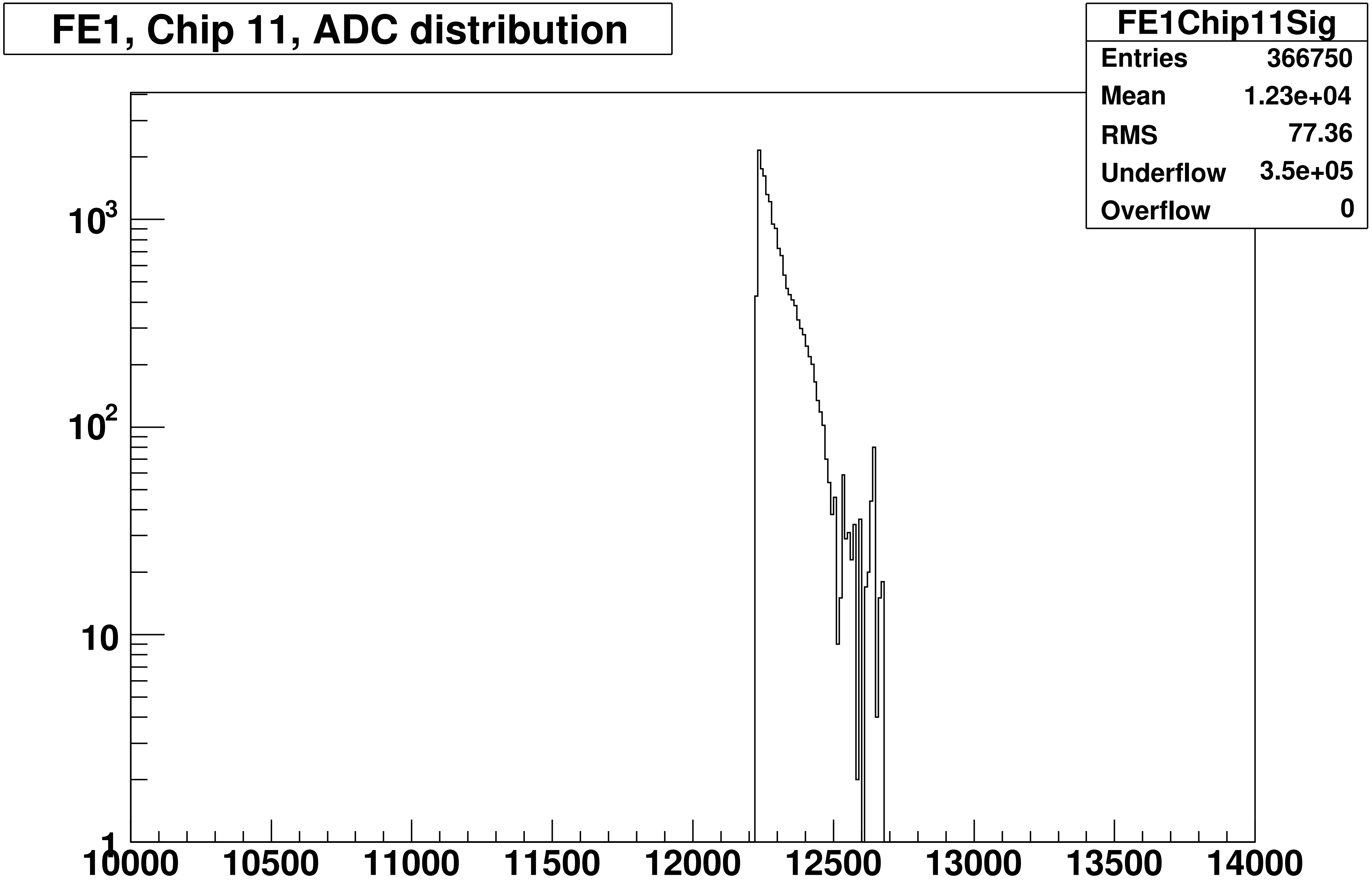
FE1, Chip 11, ADC distribution
FE1Chip11Sig
Entries 366750
Mean 1.23e+04
RMS 77.36
Underflow 3.5e+05
Overflow 0
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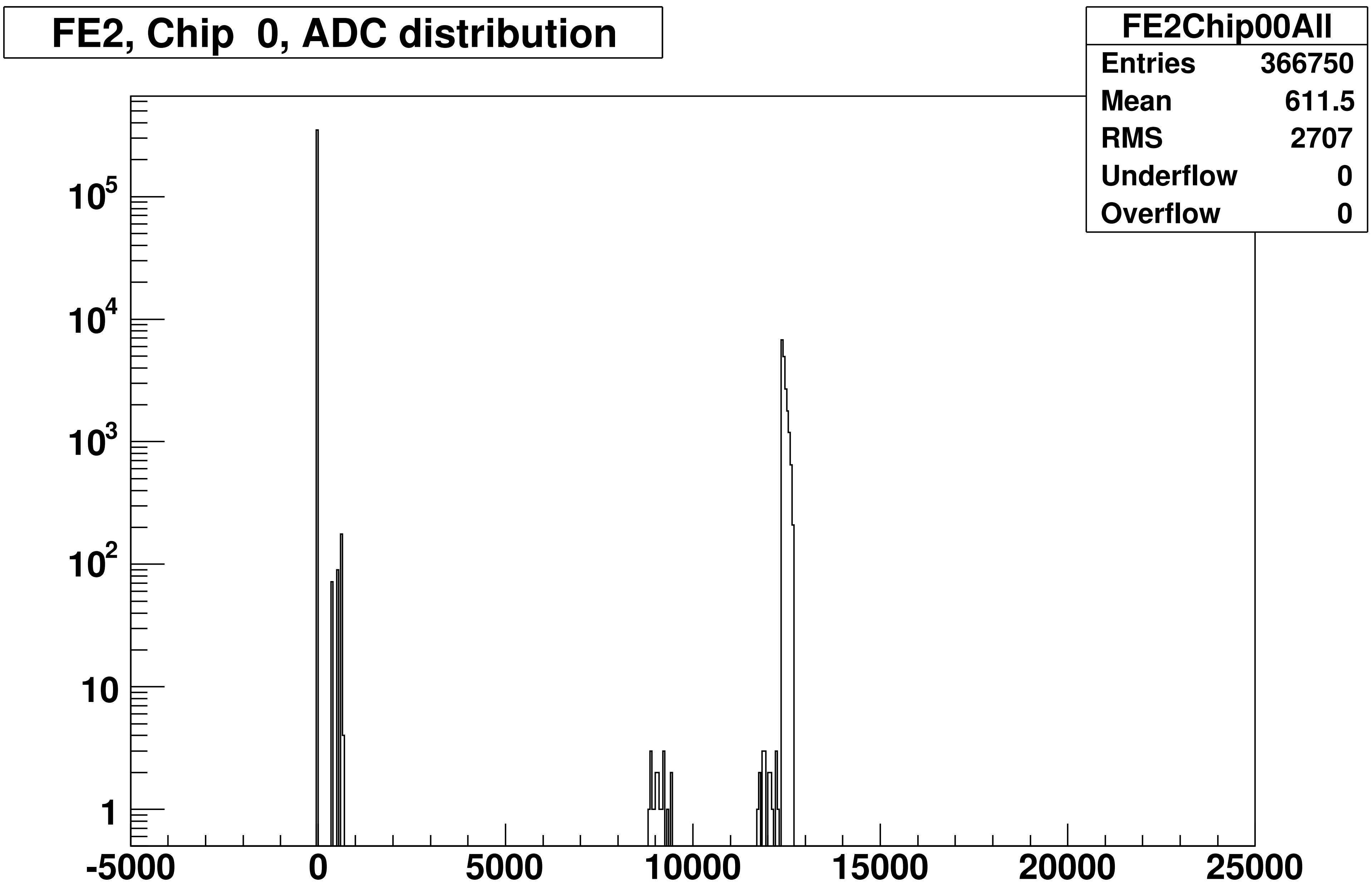
FE2, Chip 0, ADC distribution
FE2Chip00All
Entries 366750
Mean 611.5
RMS 2707
Underflow 0
Overflow 0
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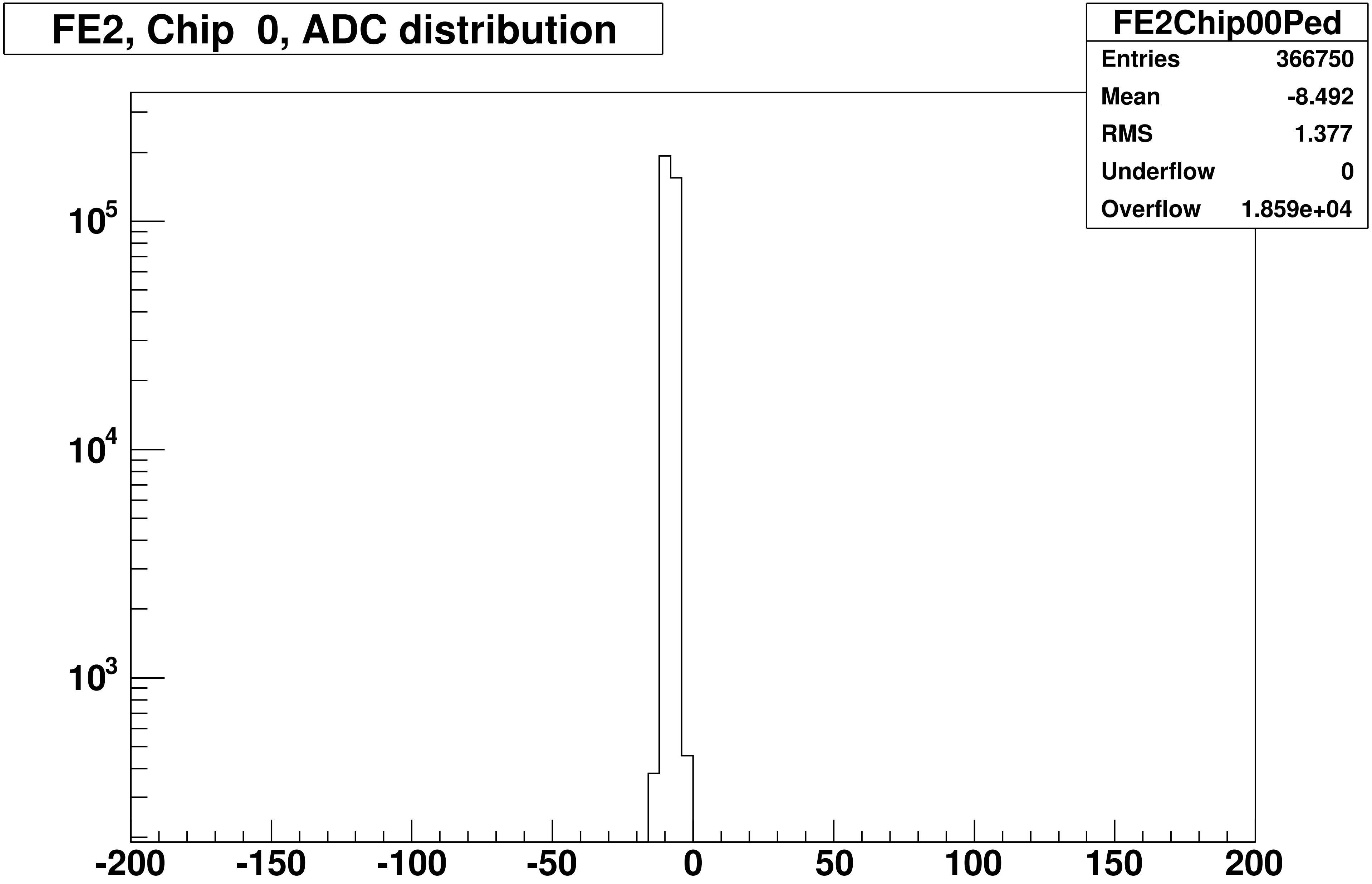
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE2, Chip 0, ADC distribution
FE2Chip00Ped
Entries 366750
Mean -8.492
RMS 1.377
Underflow 0
Overflow 1.859e+04
10^5
10^4
10^3
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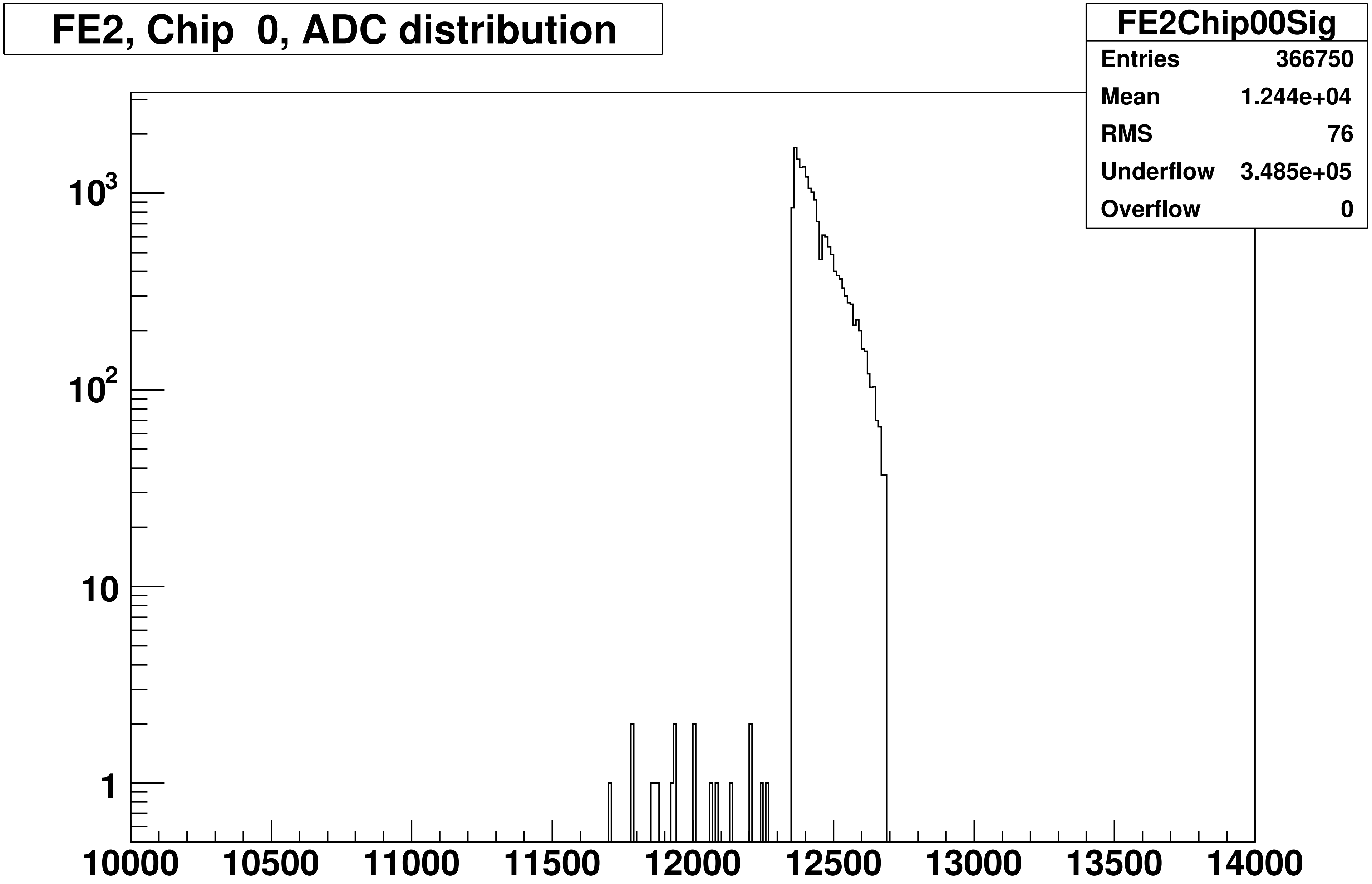
-100
-50
0
50
100
150
200


FE2, Chip 0, ADC distribution
FE2Chip00Sig
Entries 366750
Mean 1.244e+04
RMS 76
Underflow 3.485e+05
Overflow 0
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10^2
10
1
10000
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11500
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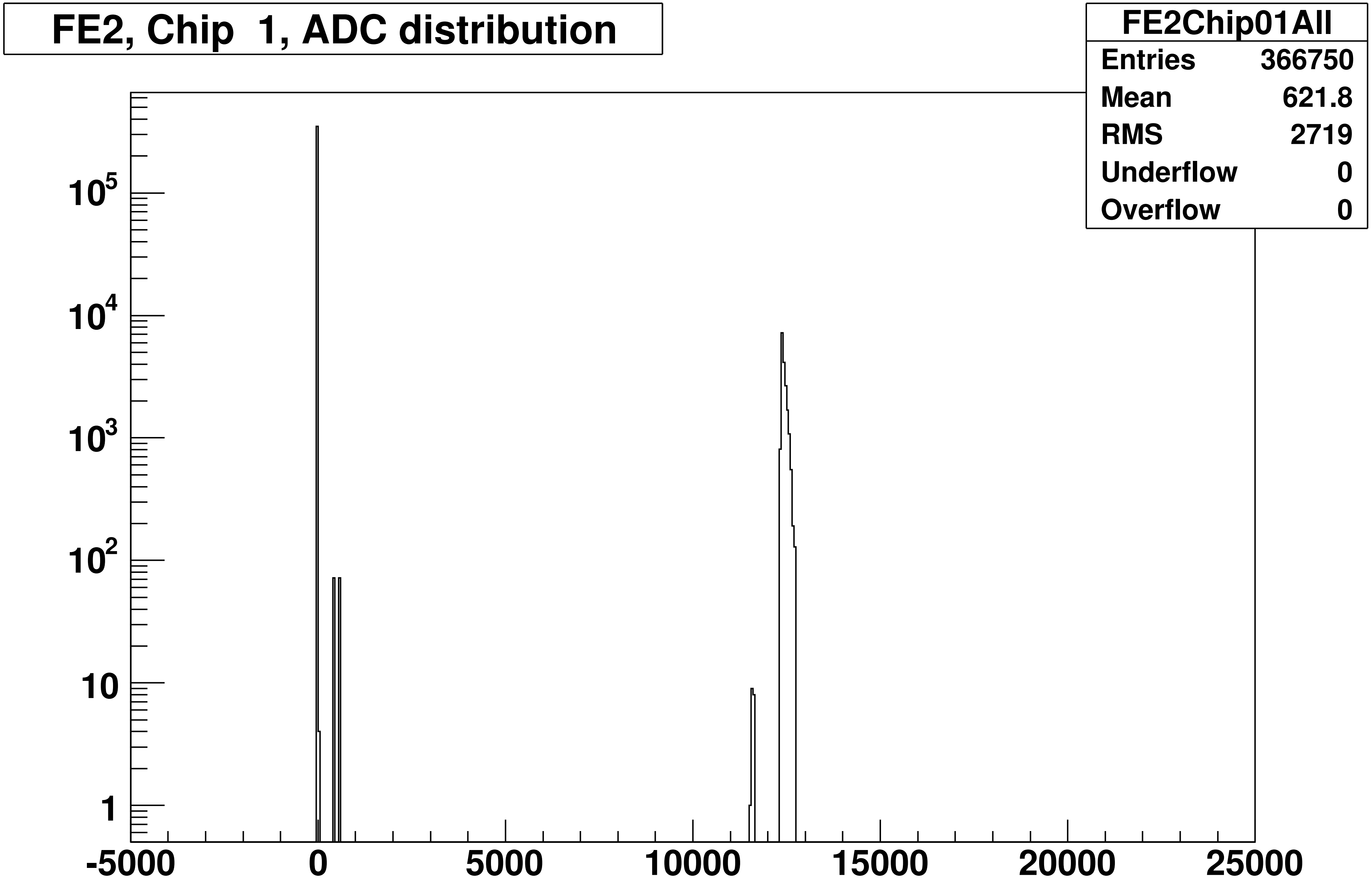
FE2, Chip 1, ADC distribution
FE2Chip01All
Entries 366750
Mean 621.8
RMS 2719
Underflow 0
Overflow 0
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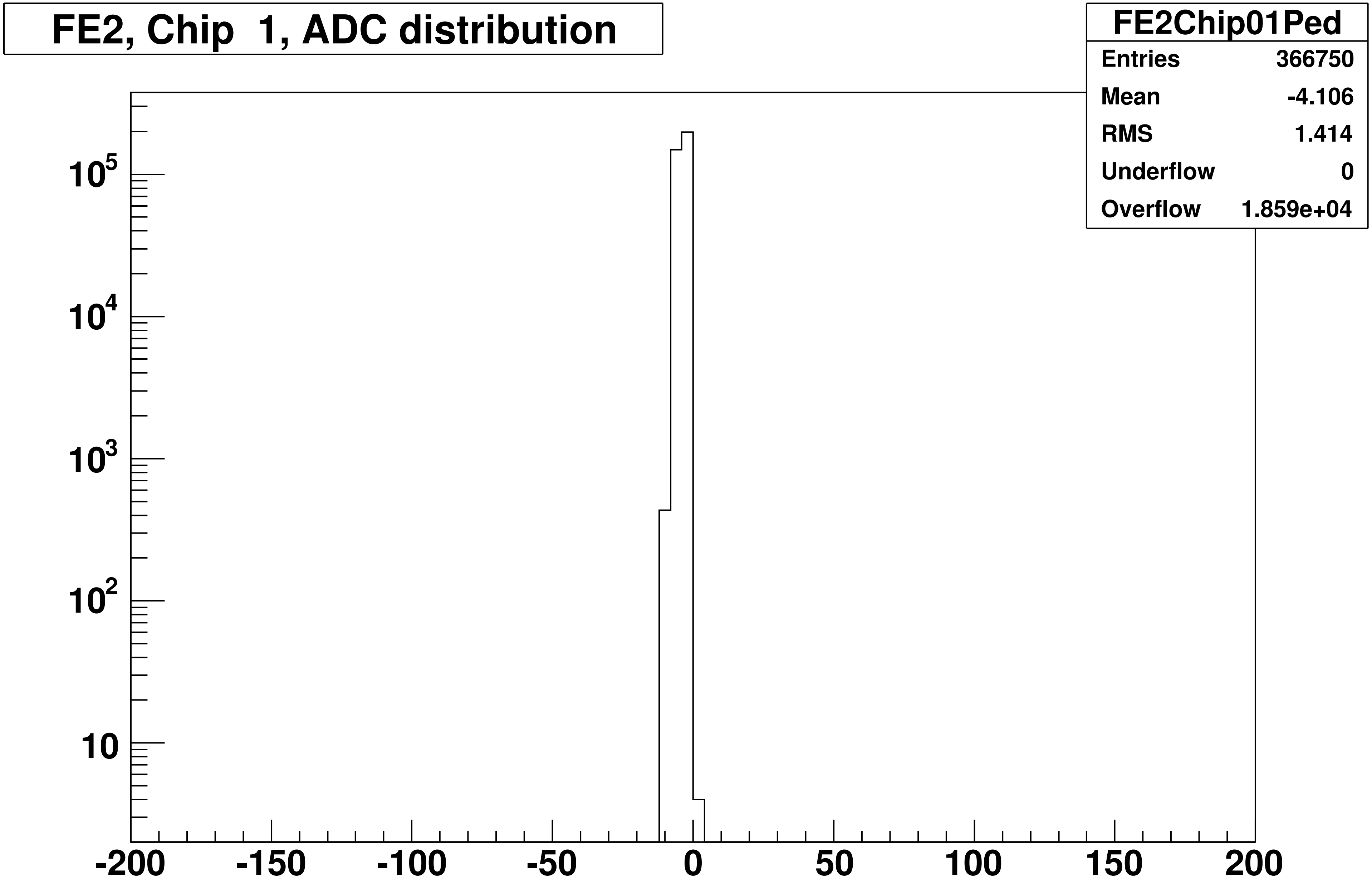
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE2, Chip 1, ADC distribution
FE2Chip01Ped
Entries 366750
Mean -4.106
RMS 1.414
Underflow 0
Overflow 1.859e+04
10^5
10^4
10^3
10^2
10
-200
-150
-100
-50
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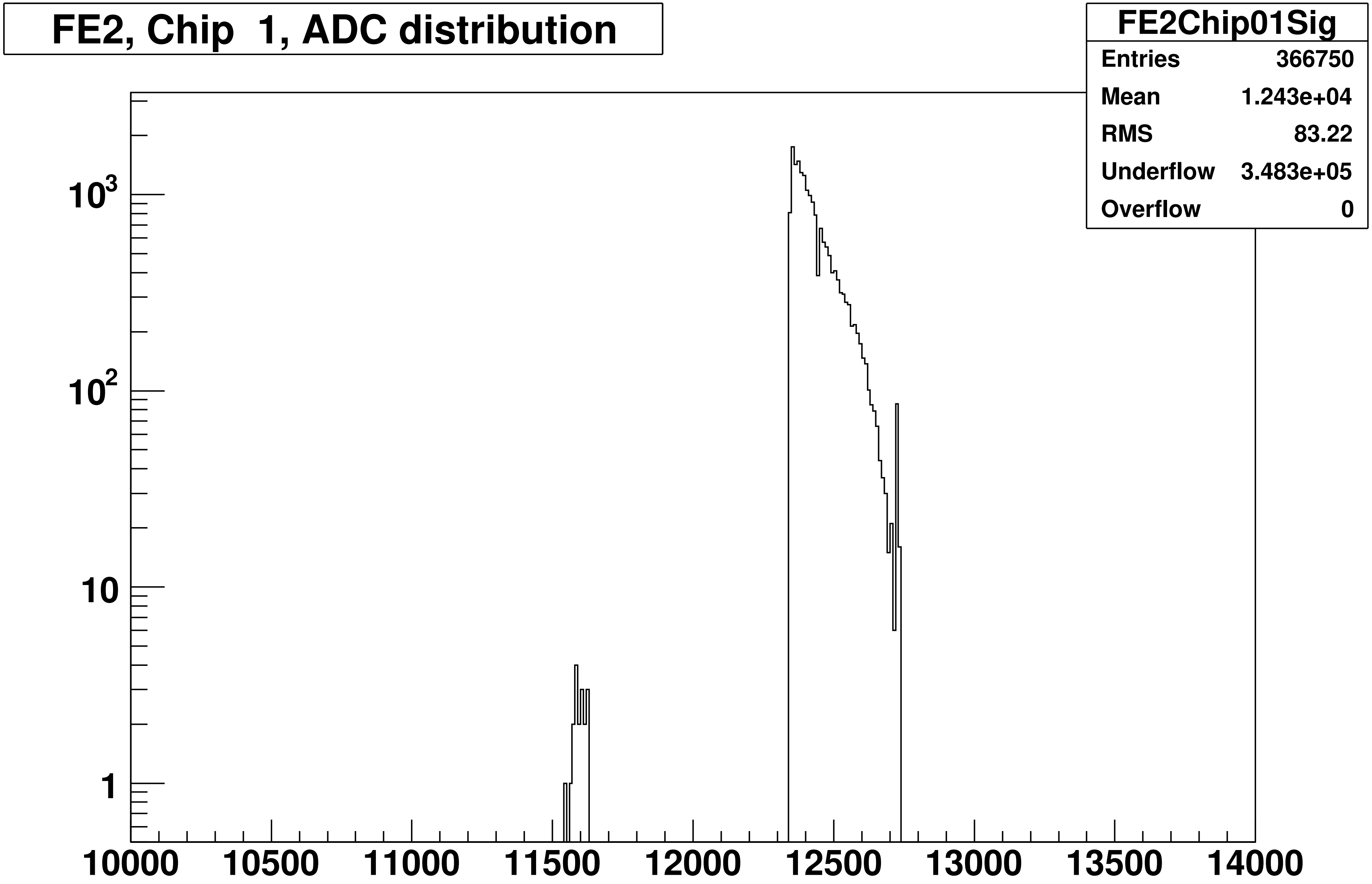
50
100
150
200


FE2, Chip 1, ADC distribution
FE2Chip01Sig
Entries 366750
Mean 1.243e+04
RMS 83.22
Underflow 3.483e+05
Overflow 0
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10^2
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1
10000
10500
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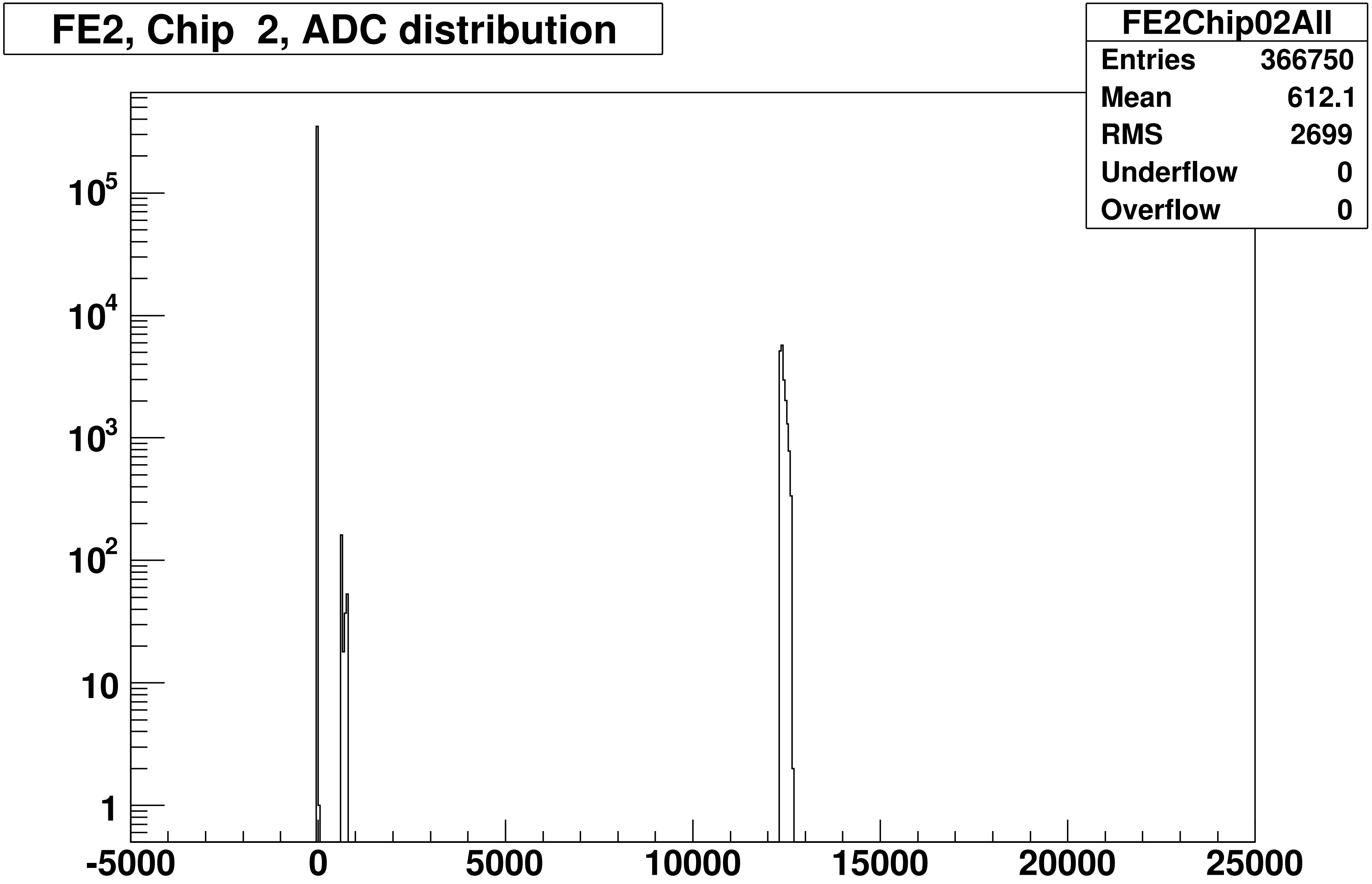
FE2, Chip 2, ADC distribution
FE2Chip02All
Entries 366750
Mean 612.1
RMS 2699
Underflow 0
Overflow 0
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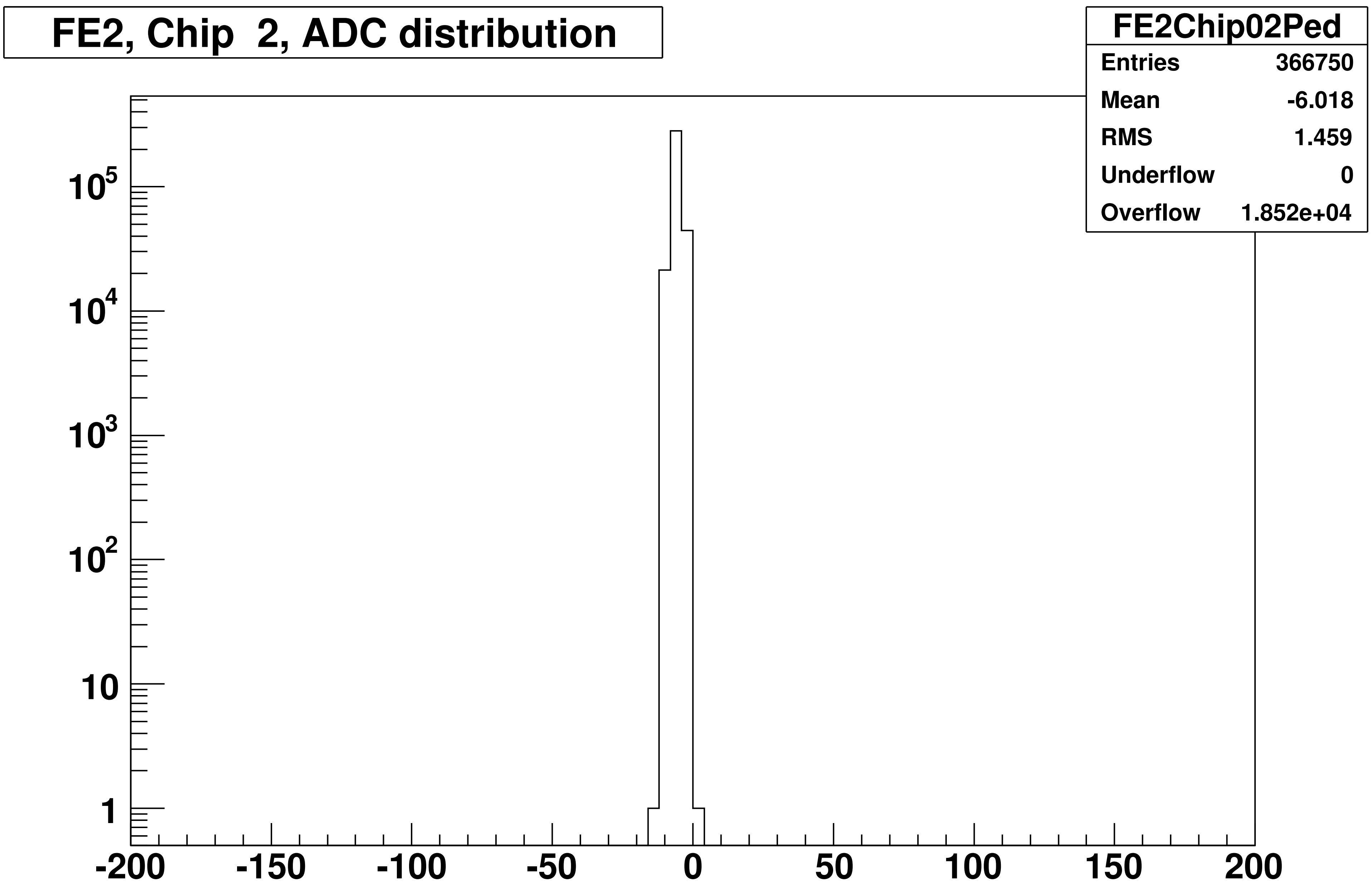
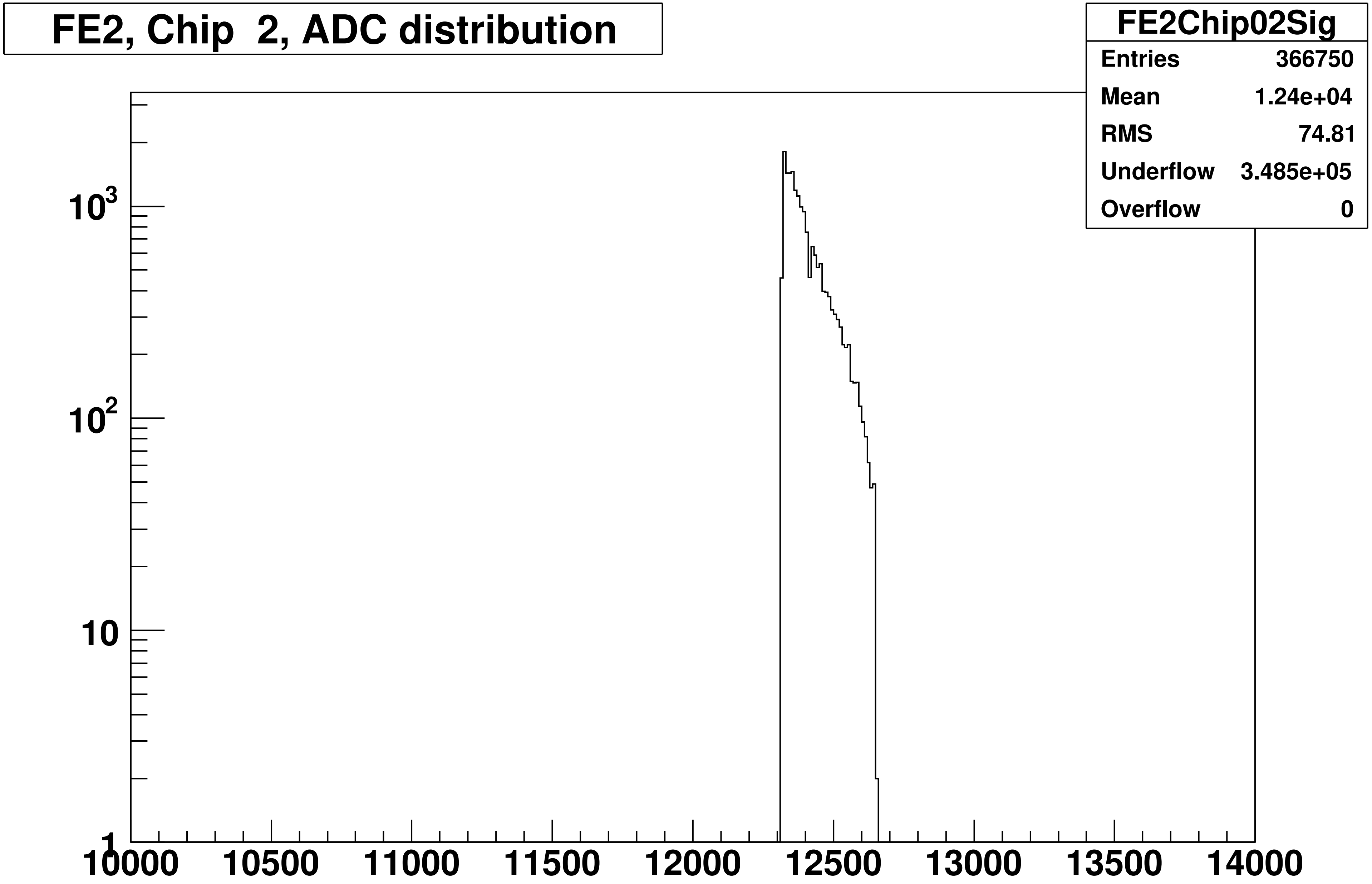
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE2, Chip 2, ADC distribution
FE2Chip02Ped
Entries 366750
Mean -6.018
RMS 1.459
Underflow 0
Overflow 1.852e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
200


FE2, Chip 2, ADC distribution
FE2Chip02Sig
Entries 366750
Mean 1.24e+04
RMS 74.81
Underflow 3.485e+05
Overflow 0
10^3
10^2
10
1
10000
10500
11000
11500
12000
12500
13000
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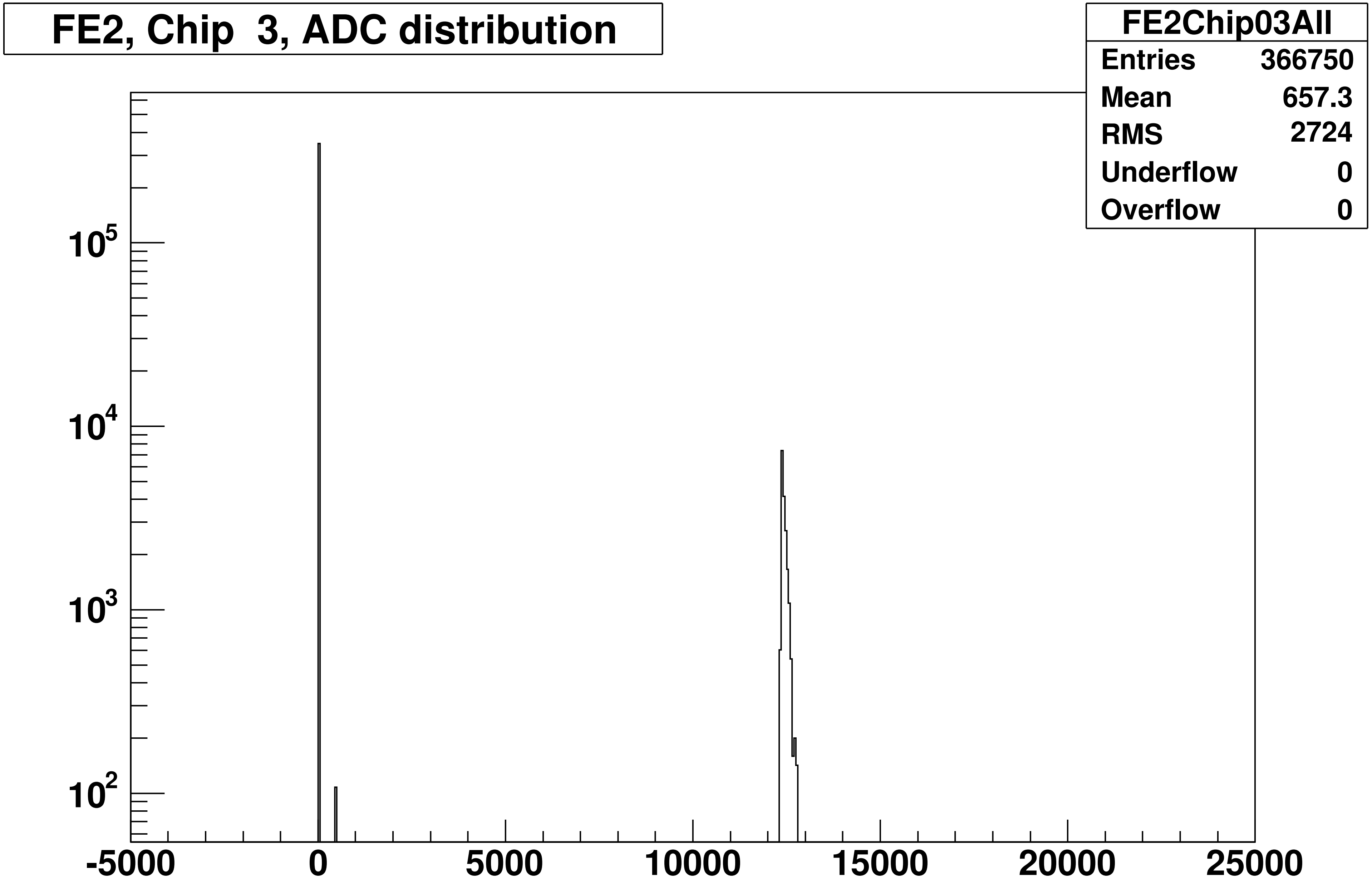
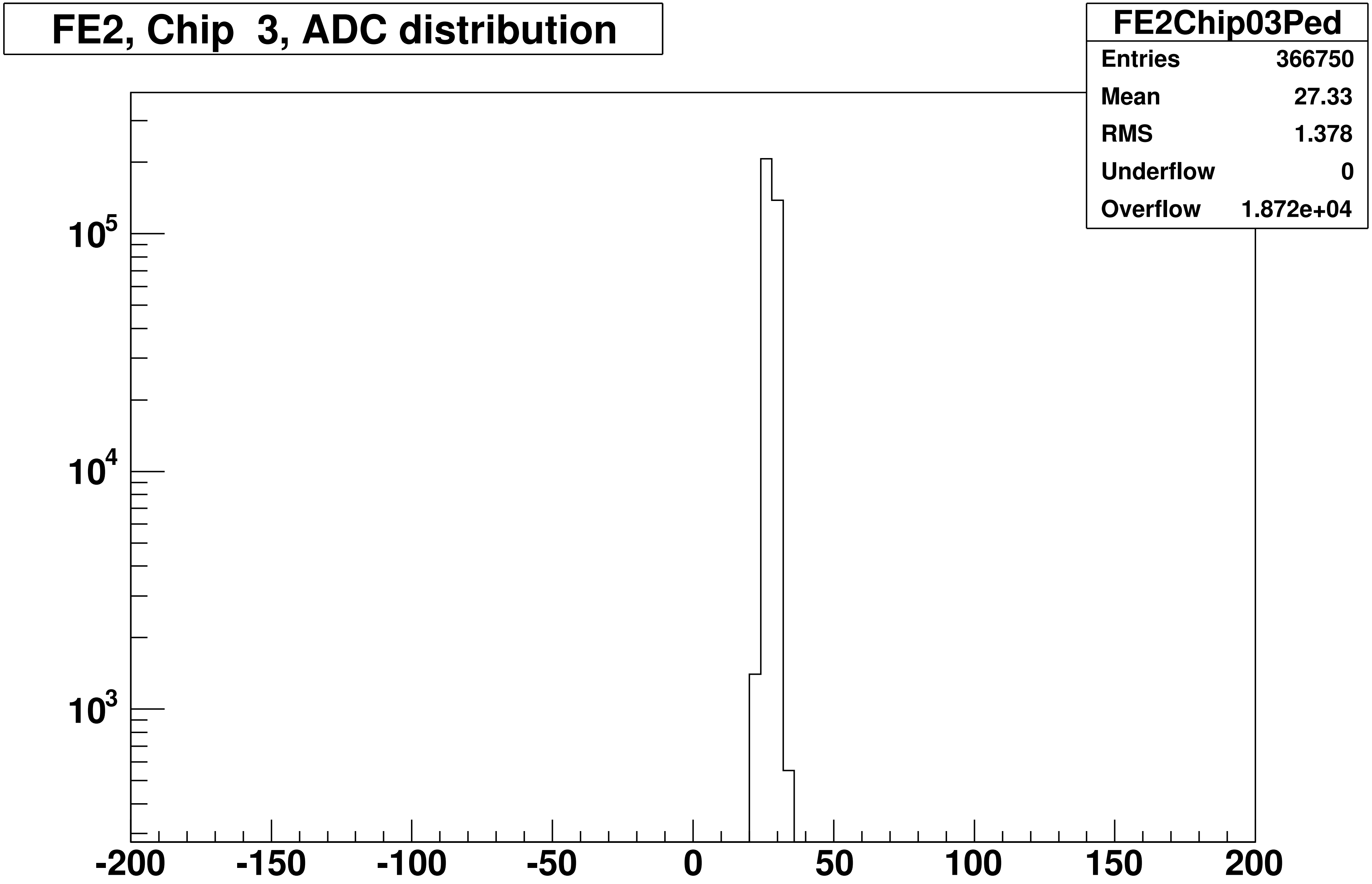
14000



FE2, Chip 3, ADC distribution
FE2Chip03All
Entries 366750
Mean 657.3
RMS 2724
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000



FE2, Chip 3, ADC distribution
FE2Chip03Ped
Entries 366750
Mean 27.33
RMS 1.378
Underflow 0
Overflow 1.872e+04
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10^4
10^3
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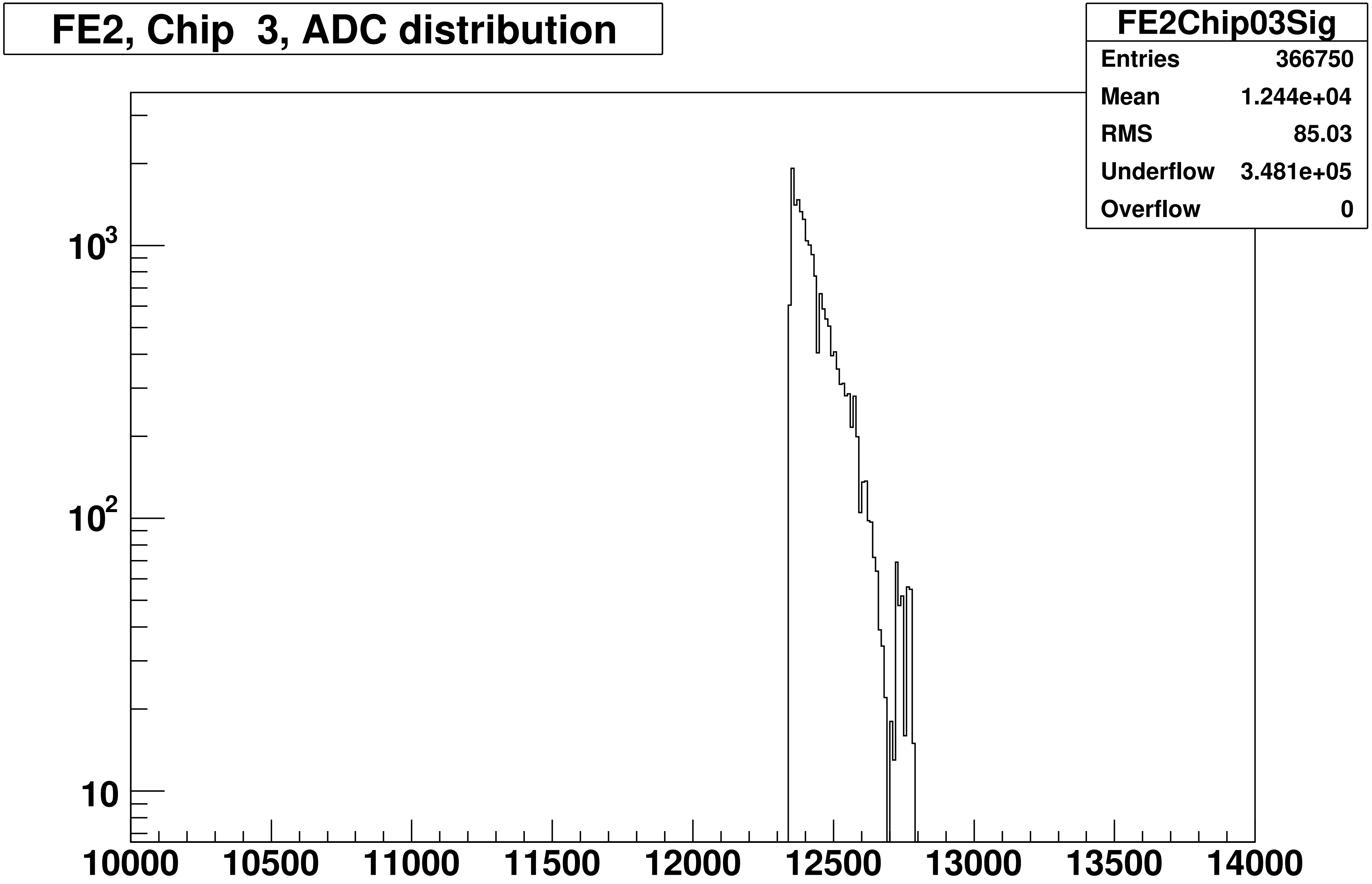
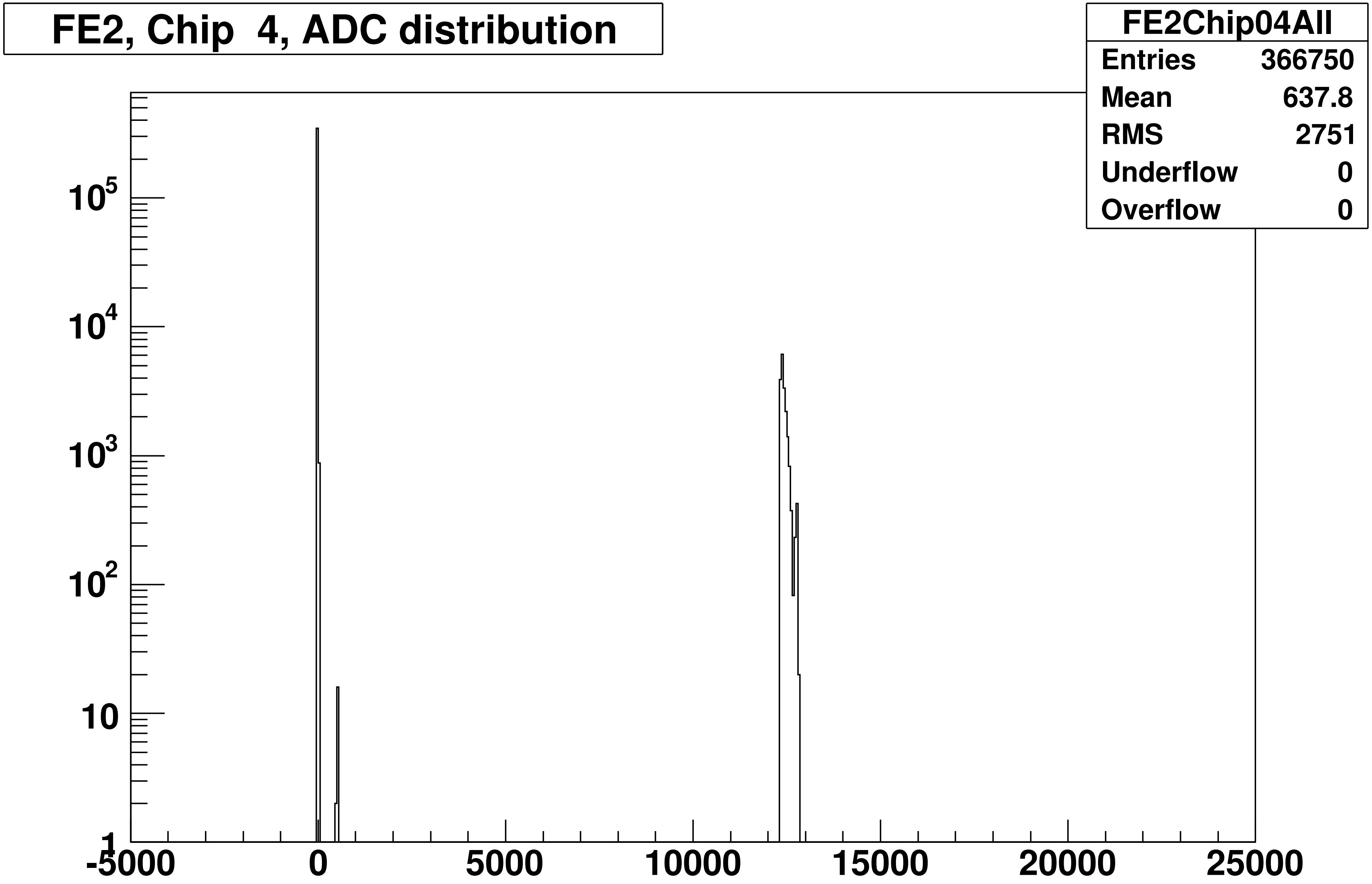
-100
-50
0
50
100
150
200


FE2, Chip 3, ADC distribution
FE2Chip03Sig
Entries 366750
Mean 1.244e+04
RMS 85.03
Underflow 3.481e+05
Overflow 0
10
10^2
10^3
10000
10500
11000
11500
12000
12500
13000
13500
14000



FE2, Chip 4, ADC distribution
FE2Chip04All
Entries 366750
Mean 637.8
RMS 2751
Underflow 0
Overflow 0
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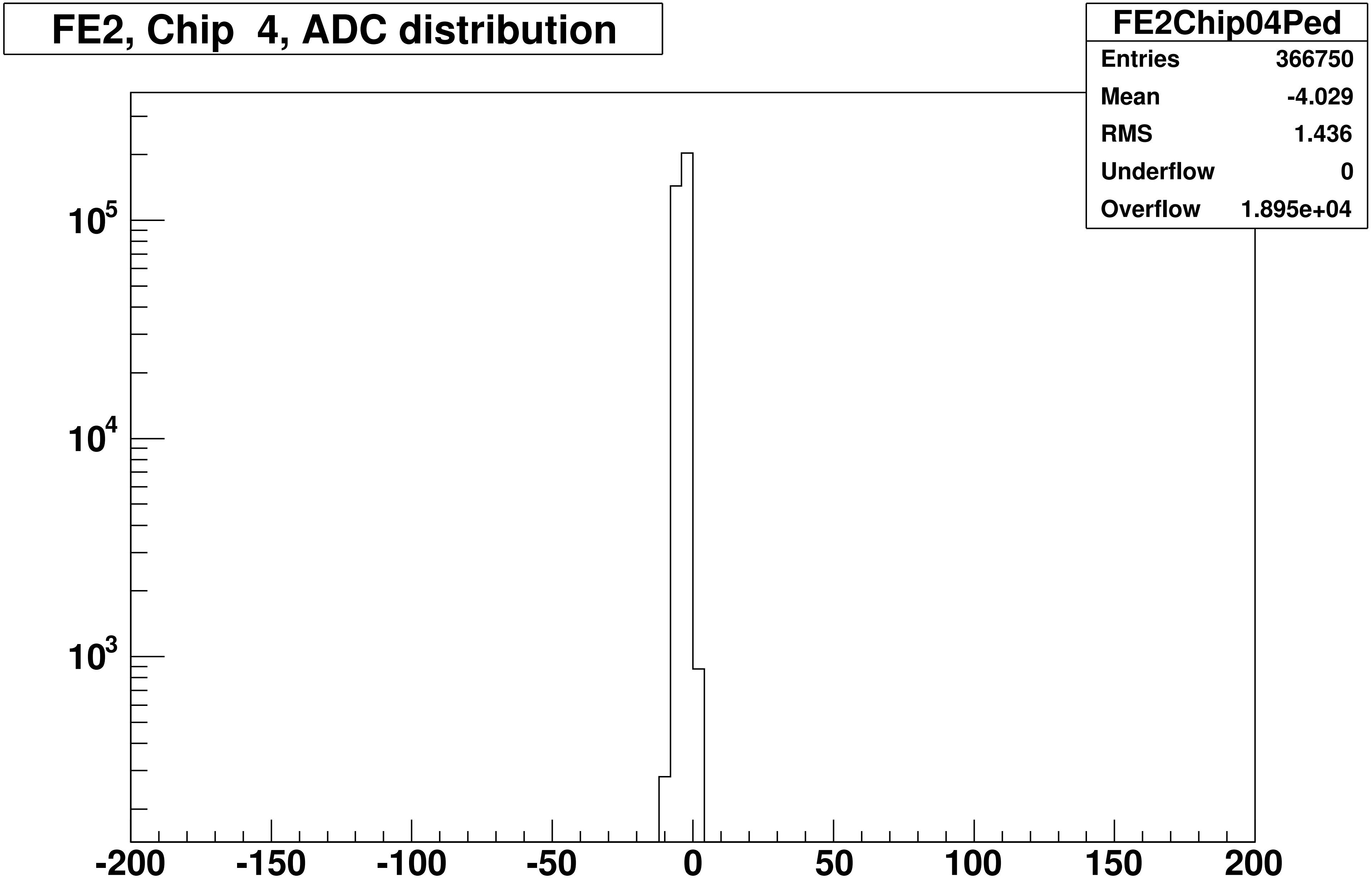
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE2, Chip 4, ADC distribution
FE2Chip04Ped
Entries 366750
Mean -4.029
RMS 1.436
Underflow 0
Overflow 1.895e+04
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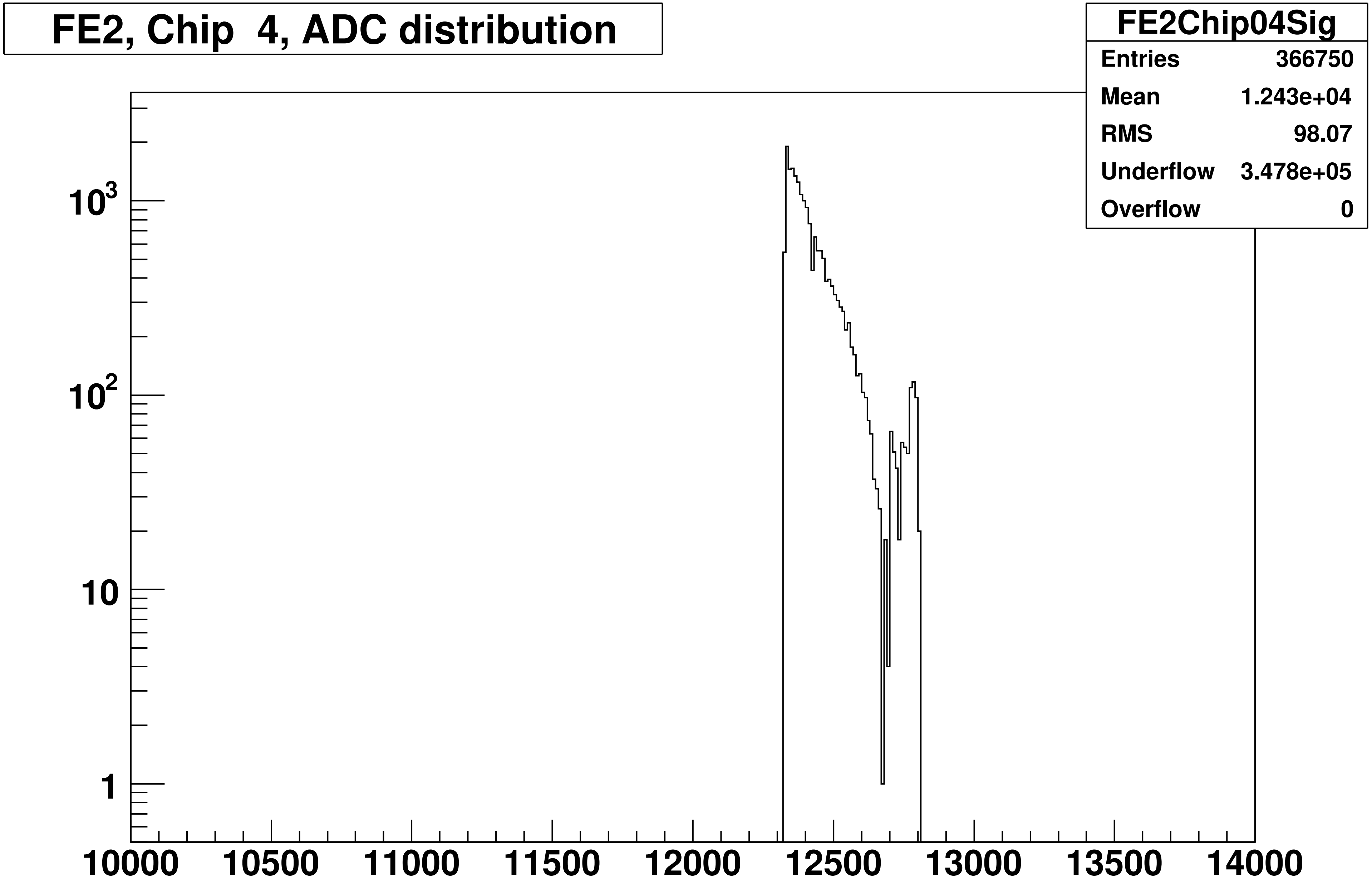
10^4
10^3
-200
-150
-100
-50
0
50
100
150
200


FE2, Chip 4, ADC distribution
FE2Chip04Sig
Entries 366750
Mean 1.243e+04
RMS 98.07
Underflow 3.478e+05
Overflow 0
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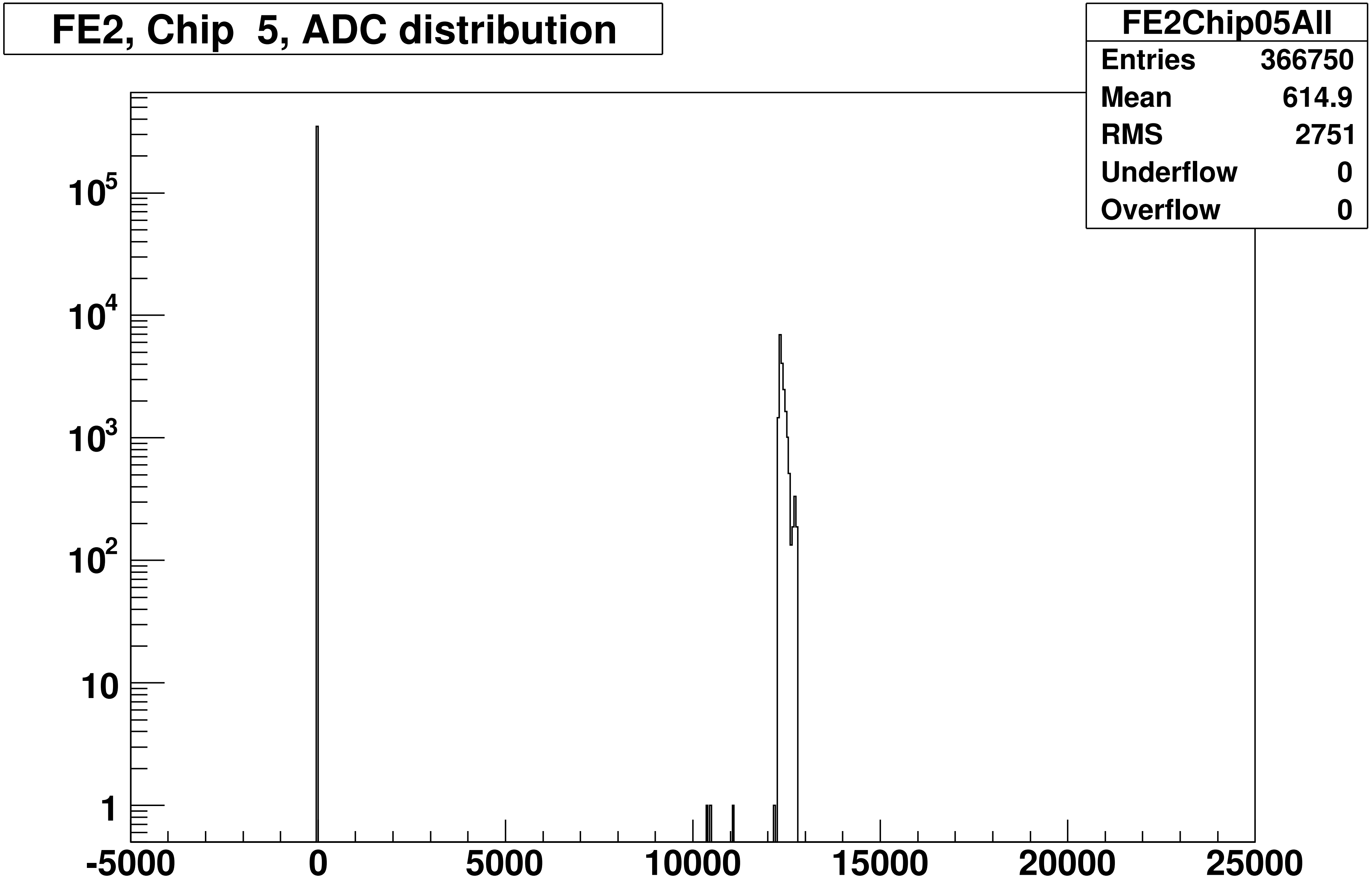
10^2
10
1
10000
10500
11000
11500
12000
12500
13000
13500
14000


FE2, Chip 5, ADC distribution
FE2Chip05All
Entries 366750
Mean 614.9
RMS 2751
Underflow 0
Overflow 0
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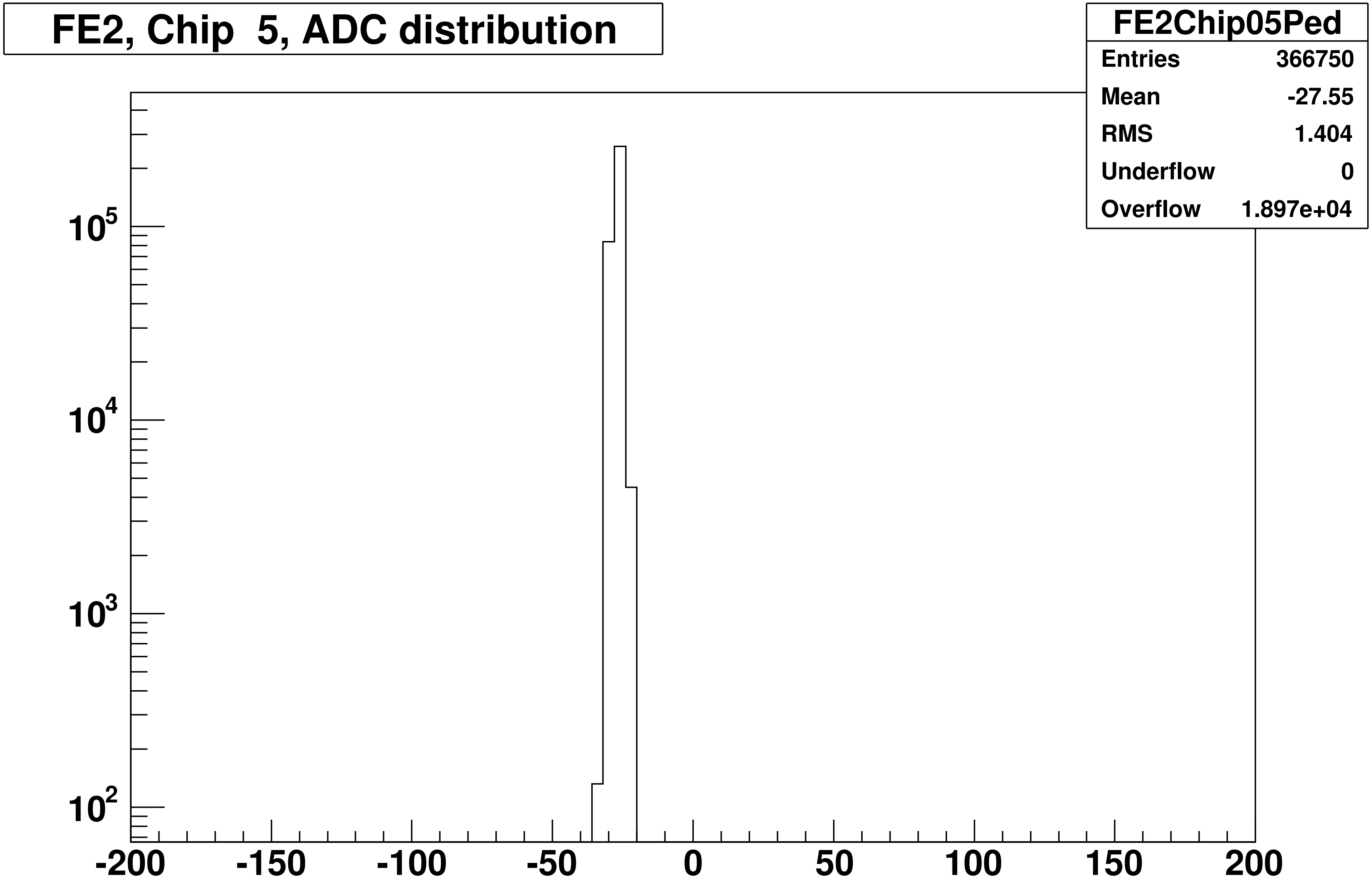
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE2, Chip 5, ADC distribution
FE2Chip05Ped
Entries 366750
Mean -27.55
RMS 1.404
Underflow 0
Overflow 1.897e+04
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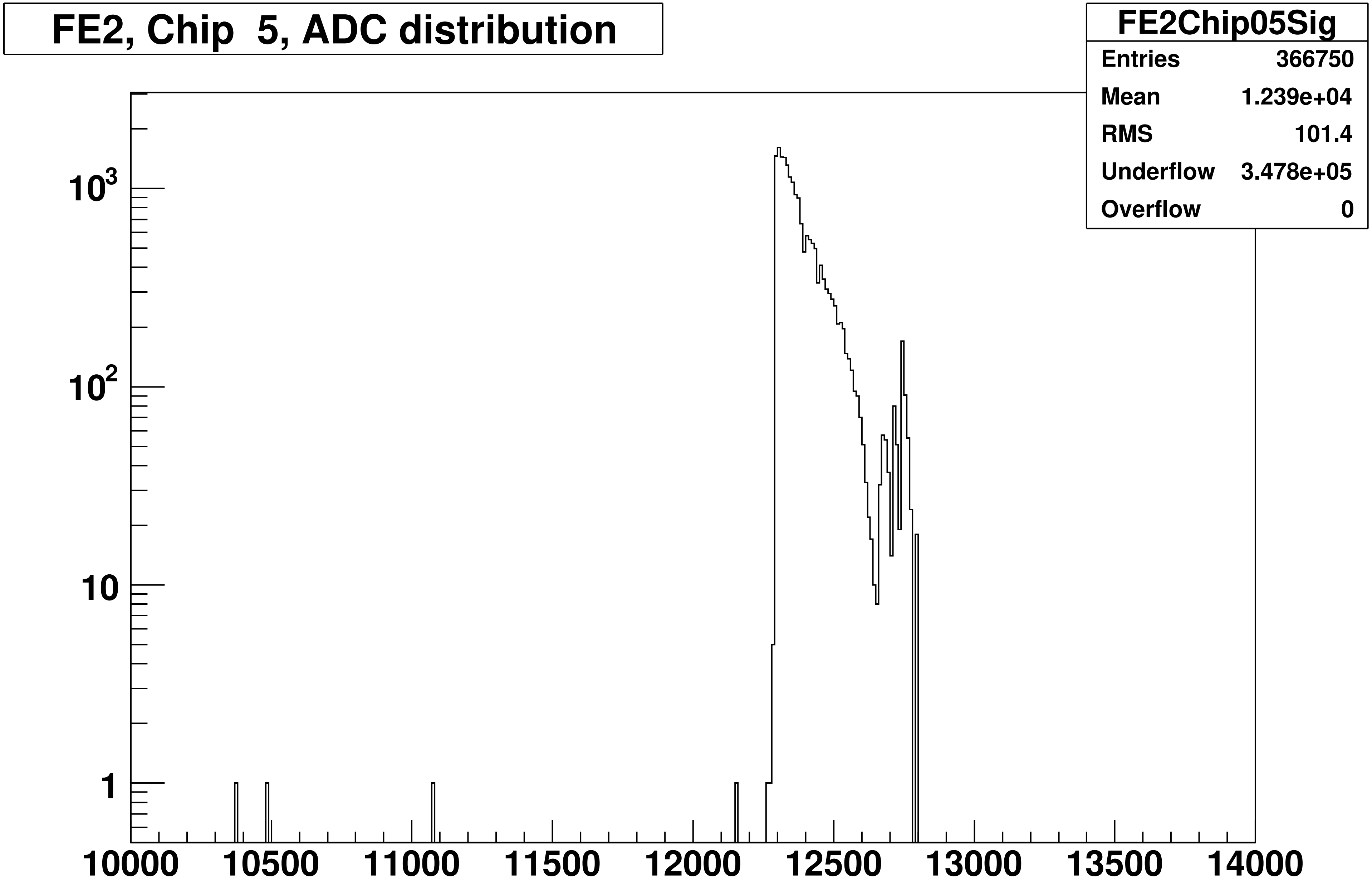
10^4
10^3
10^2
-200
-150
-100
-50
0
50
100
150
200


FE2, Chip 5, ADC distribution
FE2Chip05Sig
Entries 366750
Mean 1.239e+04
RMS 101.4
Underflow 3.478e+05
Overflow 0
10³
10²
10
1
10000
10500
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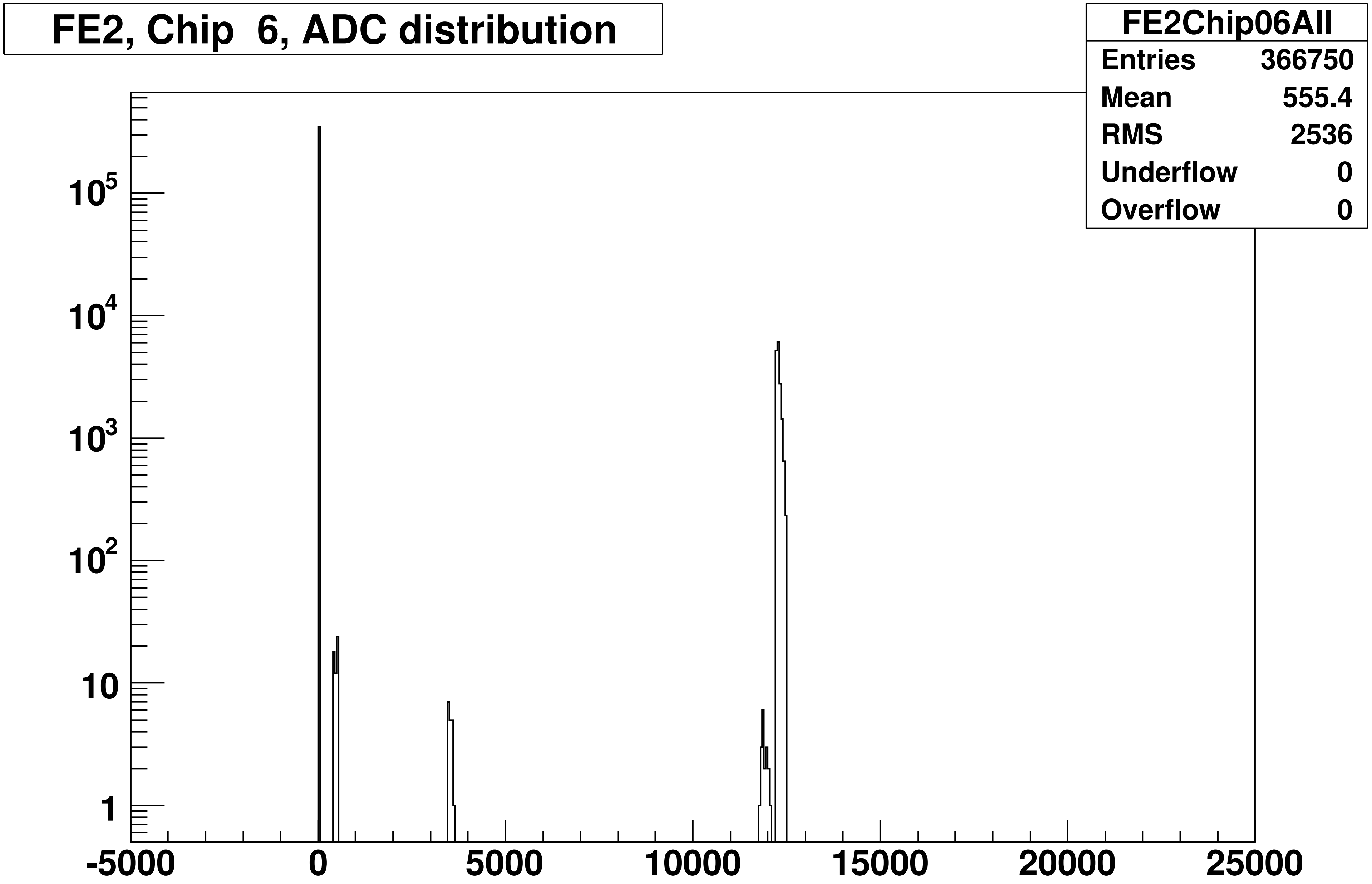
11500
12000
12500
13000
13500
14000


FE2, Chip 6, ADC distribution
FE2Chip06All
Entries 366750
Mean 555.4
RMS 2536
Underflow 0
Overflow 0
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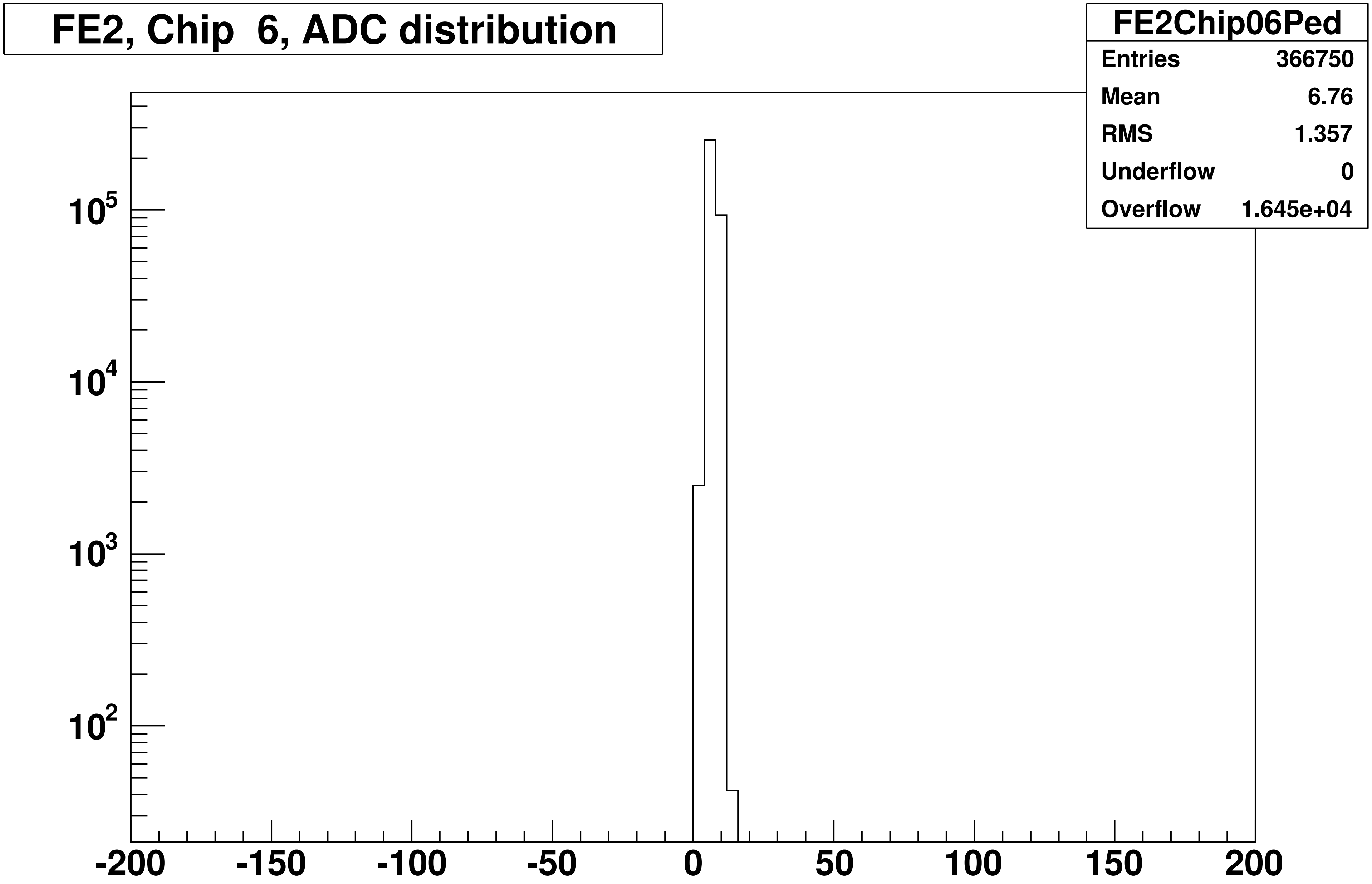
10
10^2
10^3
10^4
10^5
-5000
0
5000
10000
15000
20000
25000



FE2, Chip 6, ADC distribution
FE2Chip06Ped
Entries 366750
Mean 6.76
RMS 1.357
Underflow 0
Overflow 1.645e+04
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10^4
10^3
10^2
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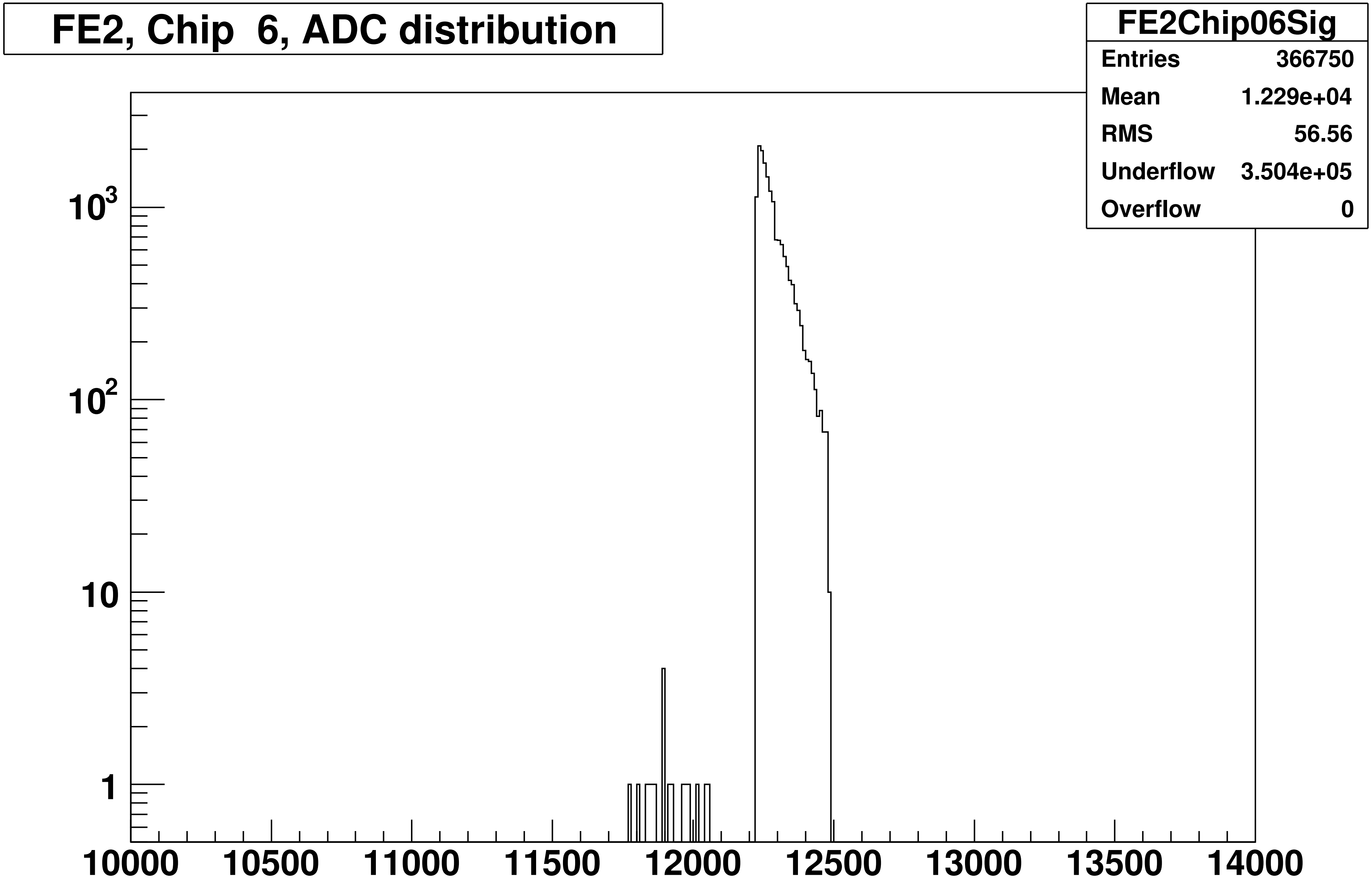
-100
-50
0
50
100
150
200


FE2, Chip 6, ADC distribution
FE2Chip06Sig
Entries 366750
Mean 1.229e+04
RMS 56.56
Underflow 3.504e+05
Overflow 0
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10^2
10
1
10000
10500
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11500
12000
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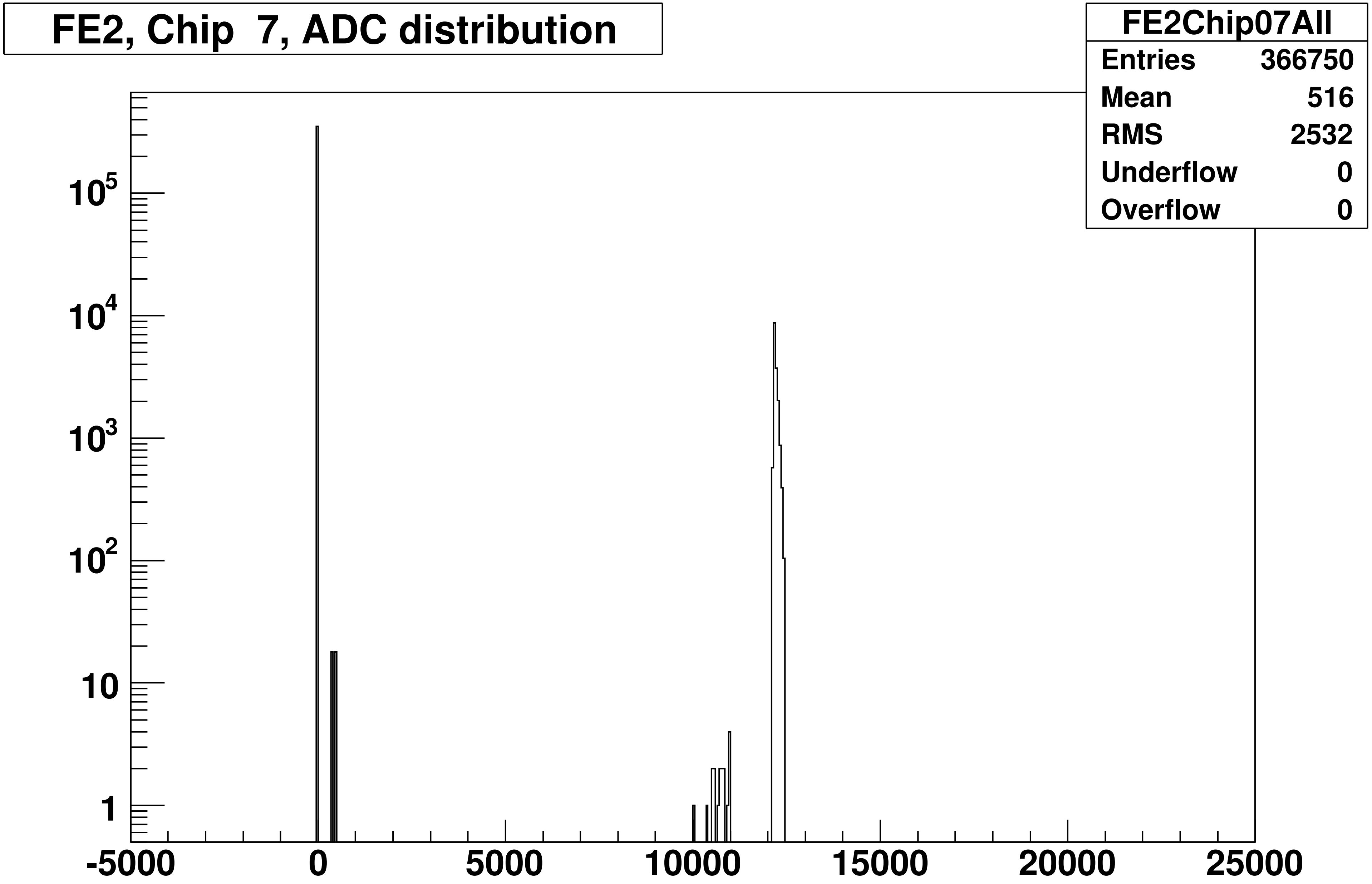

FE2, Chip 7, ADC distribution
FE2Chip07All
Entries 366750
Mean 516
RMS 2532
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
1
-5000
0
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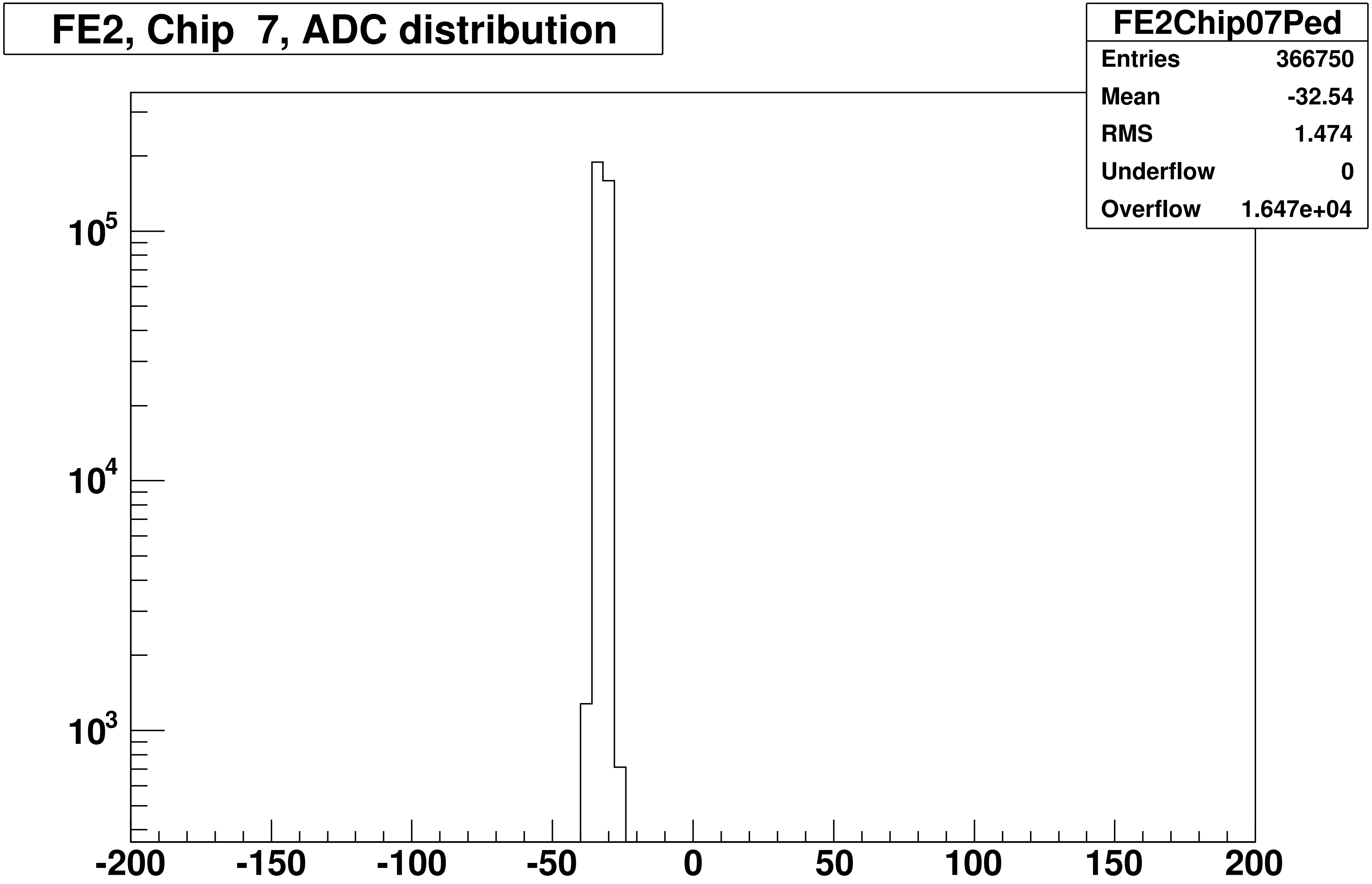
10000
15000
20000
25000


FE2, Chip 7, ADC distribution
FE2Chip07Ped
Entries 366750
Mean -32.54
RMS 1.474
Underflow 0
Overflow 1.647e+04
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10^4
10^3
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-100
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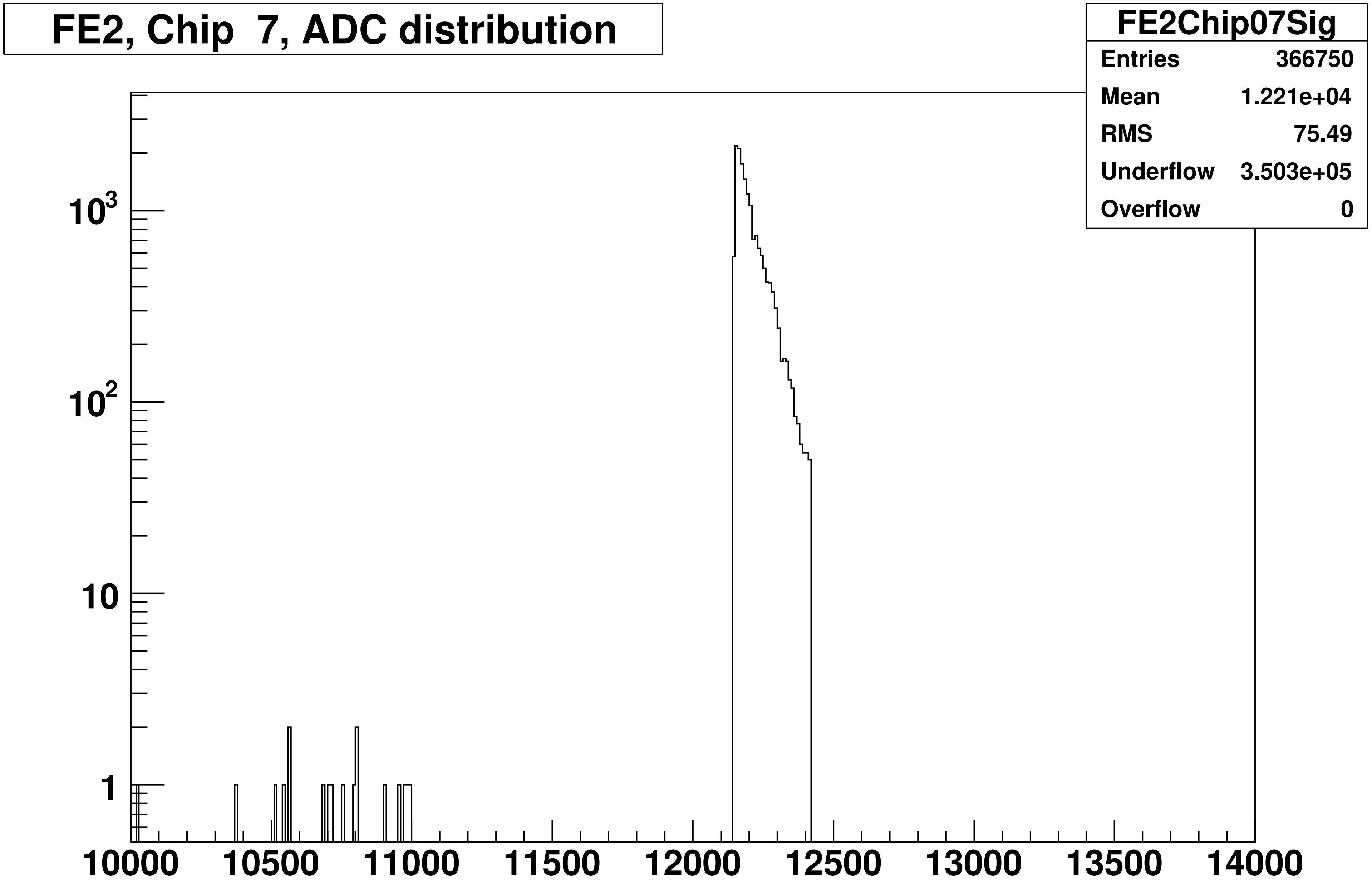
0
50
100
150
200


FE2, Chip 7, ADC distribution
FE2Chip07Sig
Entries 366750
Mean 1.221e+04
RMS 75.49
Underflow 3.503e+05
Overflow 0
10^3
10^2
10
1
10000
10500
11000
11500
12000
12500
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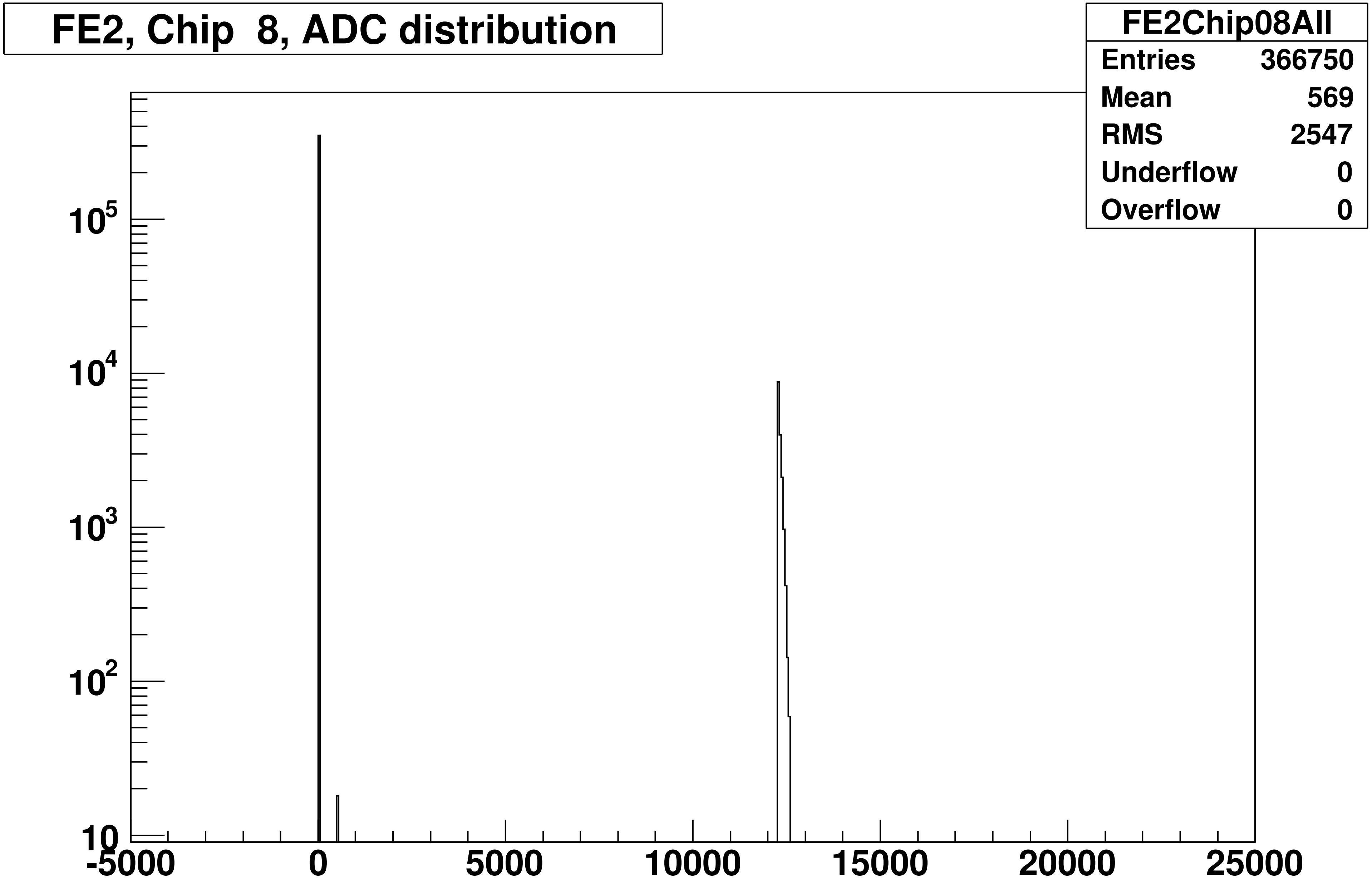
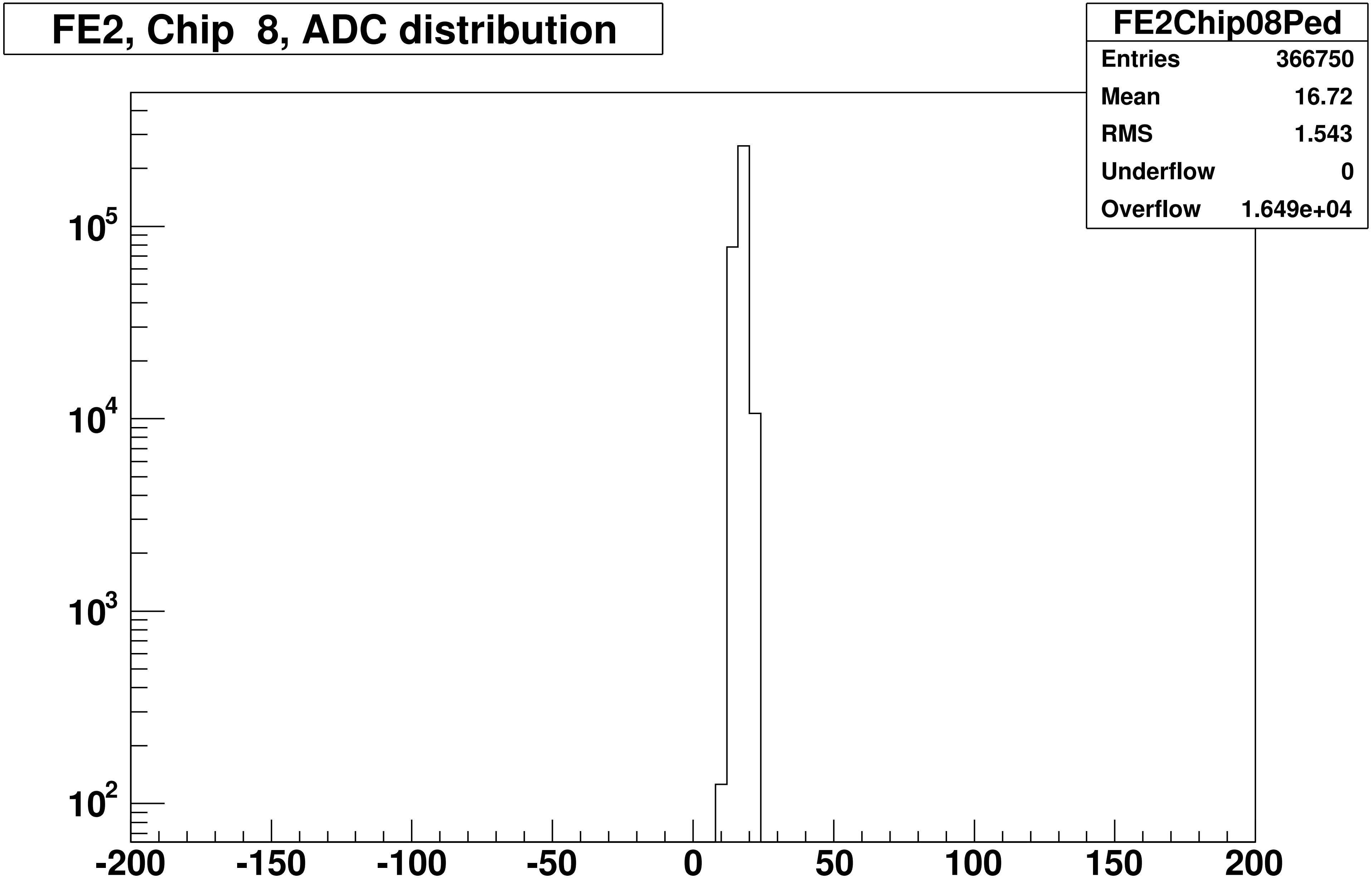


FE2, Chip 8, ADC distribution
FE2Chip08All
Entries 366750
Mean 569
RMS 2547
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000



FE2, Chip 8, ADC distribution
FE2Chip08Ped
Entries 366750
Mean 16.72
RMS 1.543
Underflow 0
Overflow 1.649e+04
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10^4
10^3
10^2
-200
-150
-100
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0
50
100
150
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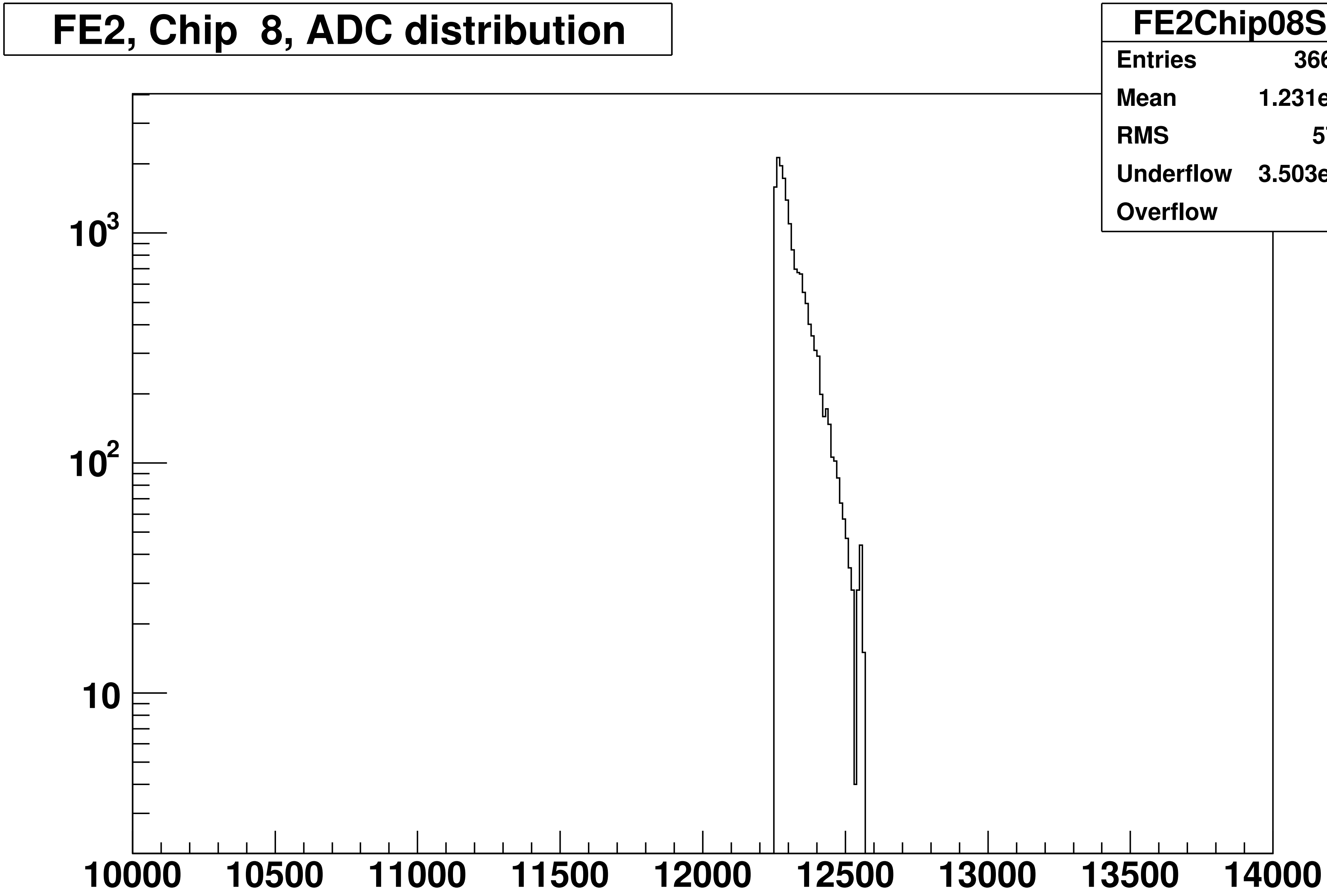
FE2, Chip 8, ADC distribution
FE2Chip08Sig
Entries 366750
Mean 1.231e+04
RMS 57.99
Underflow 3.503e+05
Overflow 0
10³
10²
10
10000
10500
11000
11500
12000
12500
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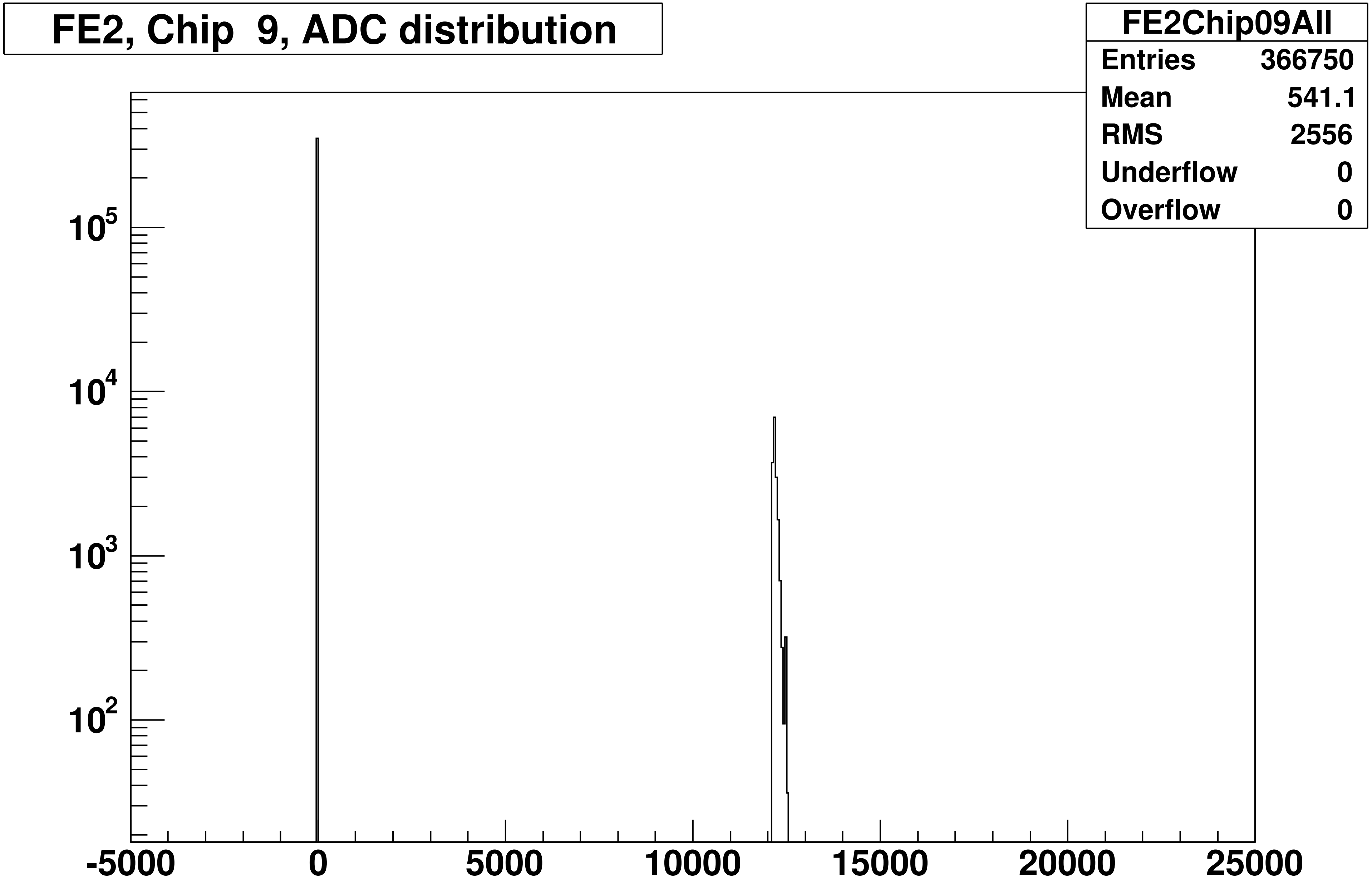
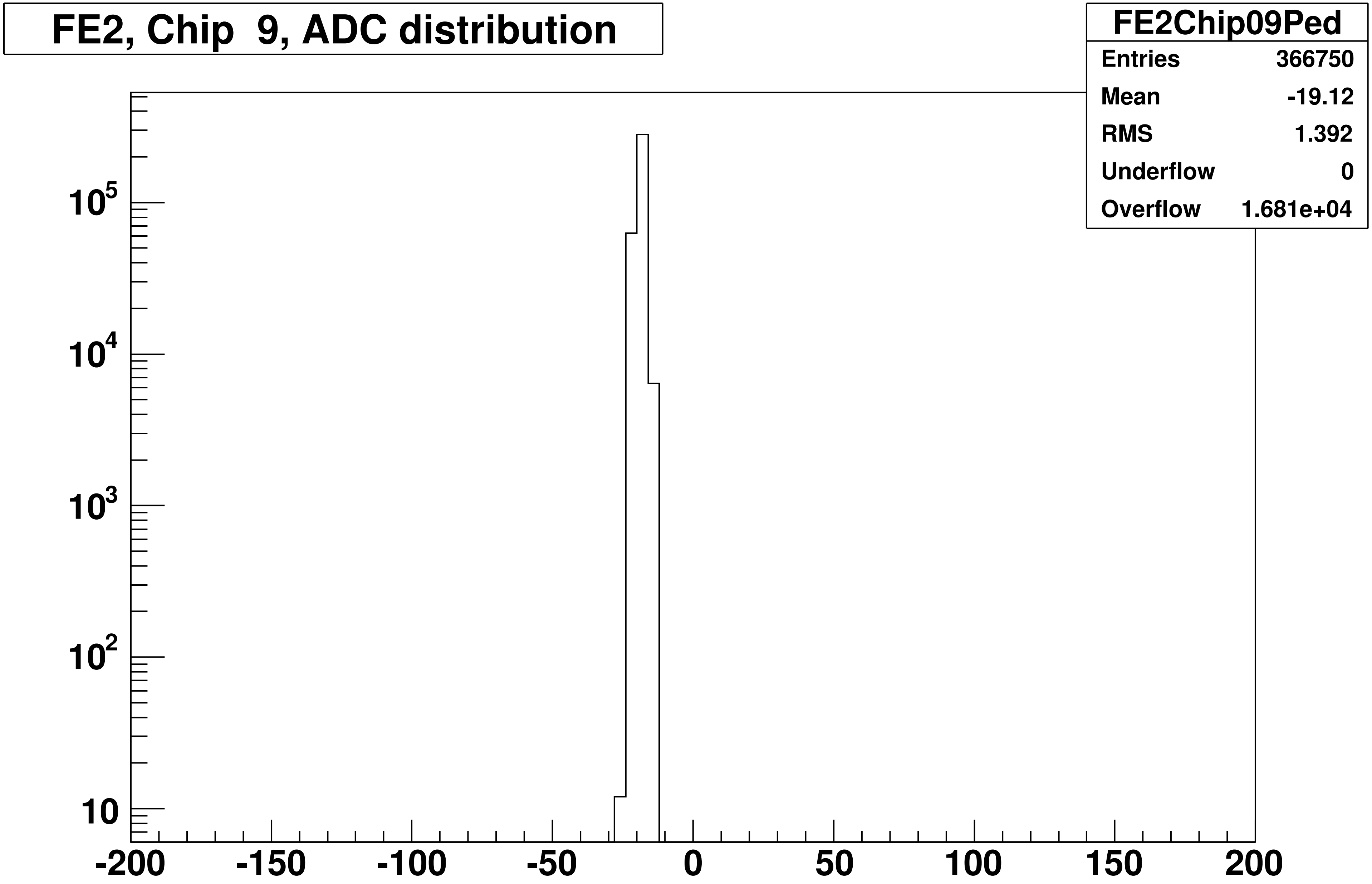


FE2, Chip 9, ADC distribution
FE2Chip09All
Entries 366750
Mean 541.1
RMS 2556
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000


FE2, Chip 9, ADC distribution
FE2Chip09Ped
Entries 366750
Mean -19.12
RMS 1.392
Underflow 0
Overflow 1.681e+04
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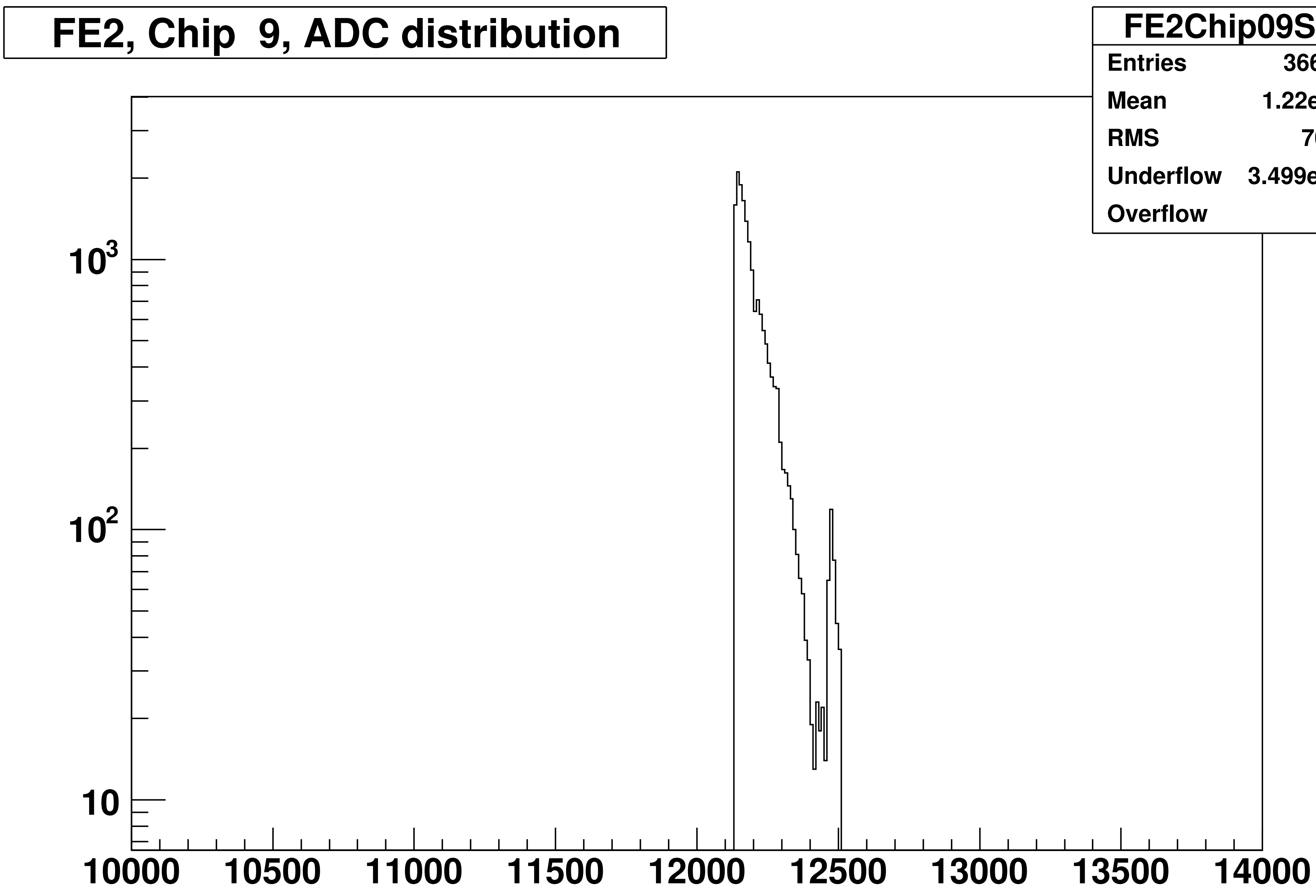
10^4
10^3
10^2
10
-200
-150
-100
-50
0
50
100
150
200


FE2, Chip 9, ADC distribution
FE2Chip09Sig
Entries 366750
Mean 1.22e+04
RMS 70.19
Underflow 3.499e+05
Overflow 0
10^3
10^2
10
10000
10500
11000
11500
12000
12500
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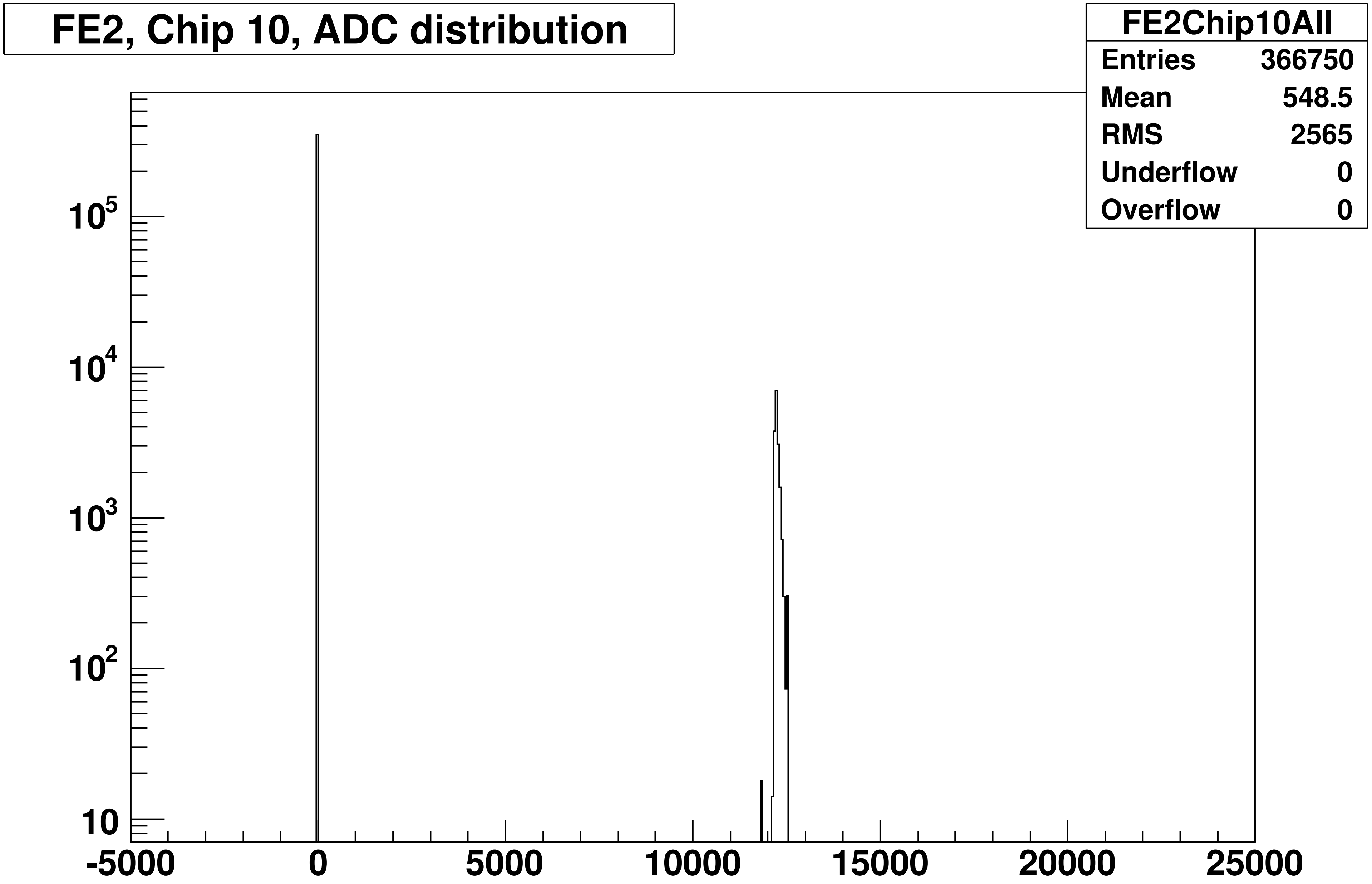
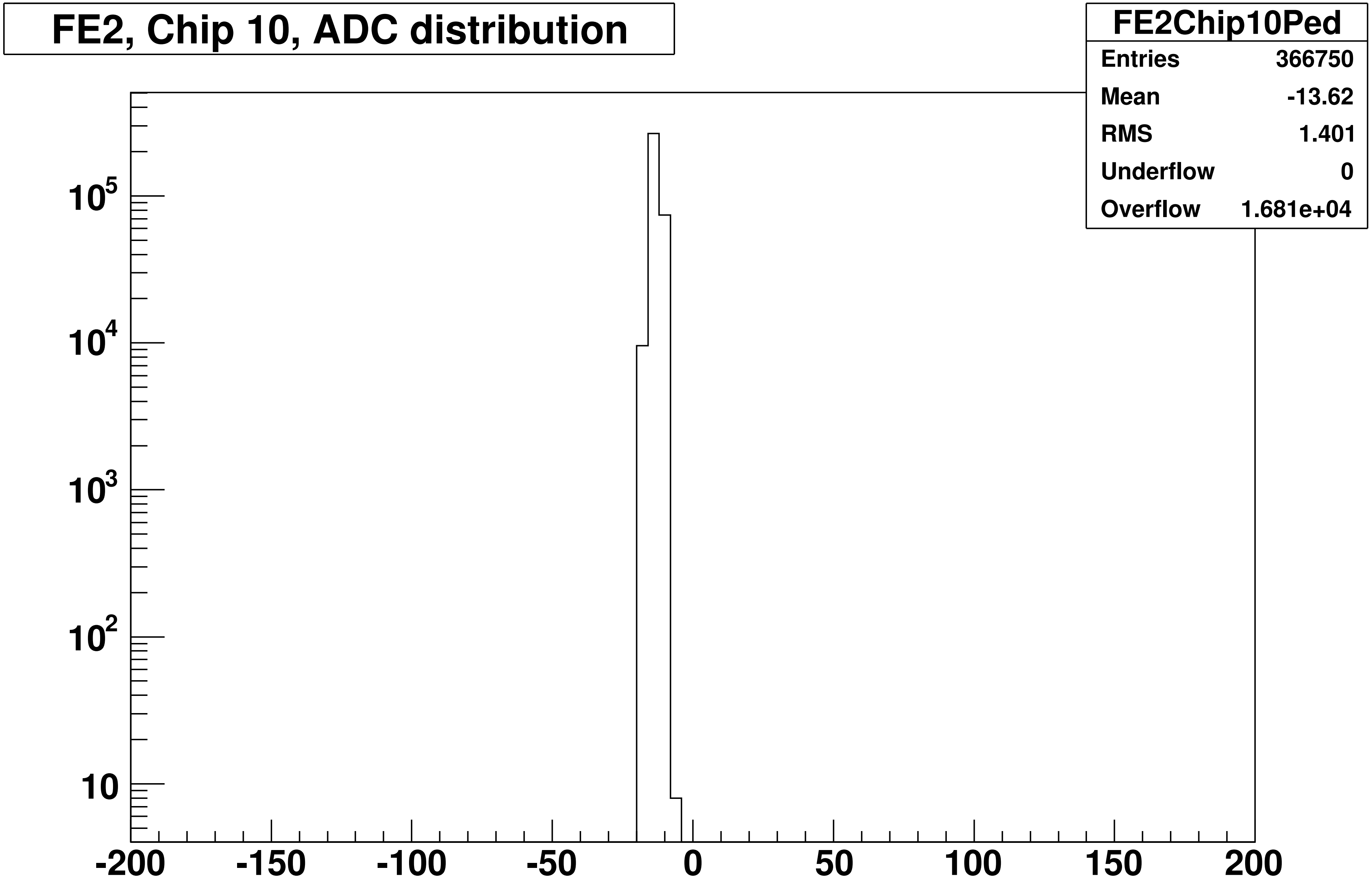
13500
14000


FE2, Chip 10, ADC distribution
FE2Chip10All
Entries 366750
Mean 548.5
RMS 2565
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE2, Chip 10, ADC distribution
FE2Chip10Ped
Entries 366750
Mean -13.62
RMS 1.401
Underflow 0
Overflow 1.681e+04
10^5
10^4
10^3
10^2
10
-200
-150
-100
-50
0
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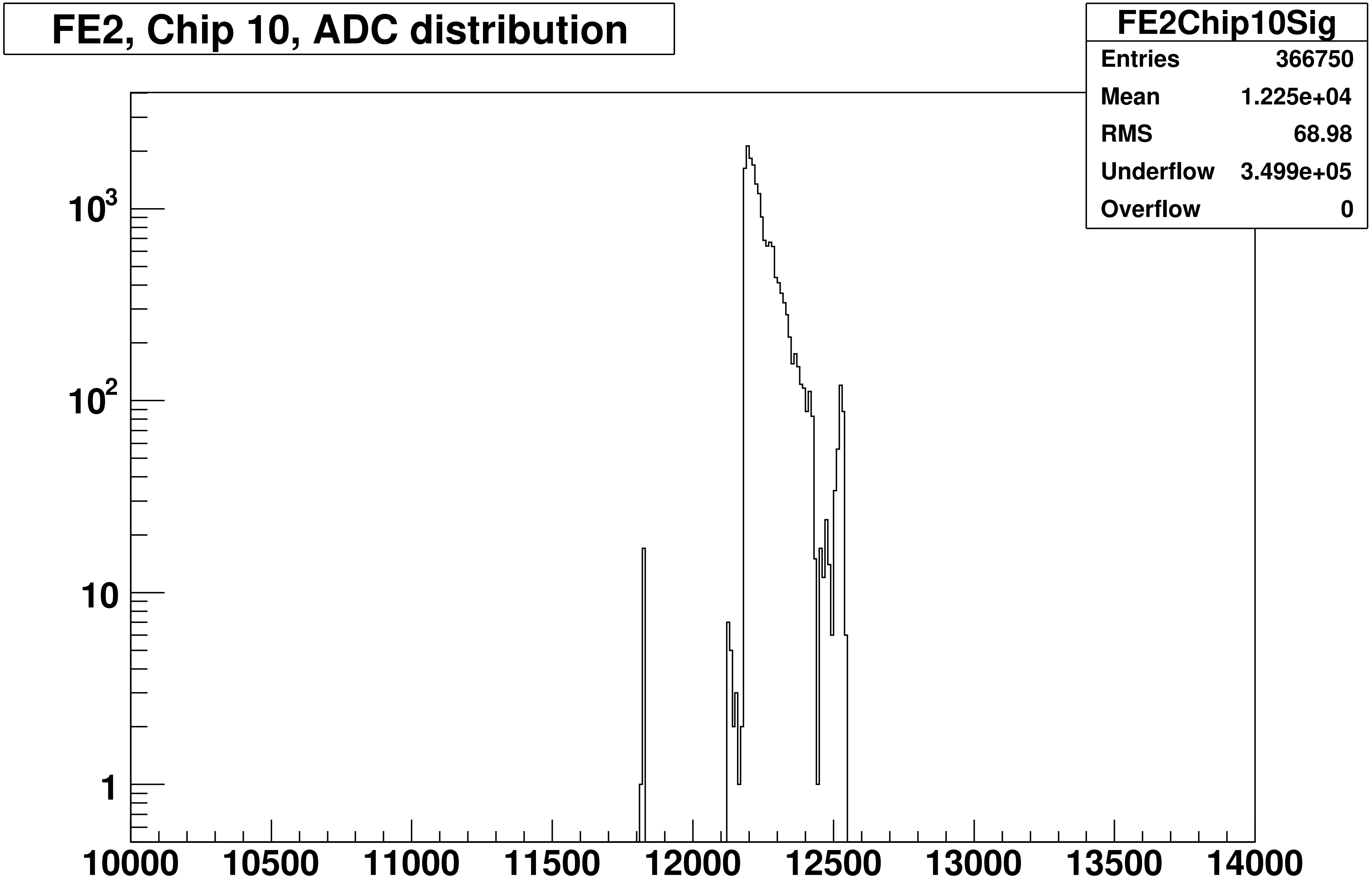
100
150
200


FE2, Chip 10, ADC distribution
FE2Chip10Sig
Entries 366750
Mean 1.225e+04
RMS 68.98
Underflow 3.499e+05
Overflow 0
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10^2
10
1
10000
10500
11000
11500
12000
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13000
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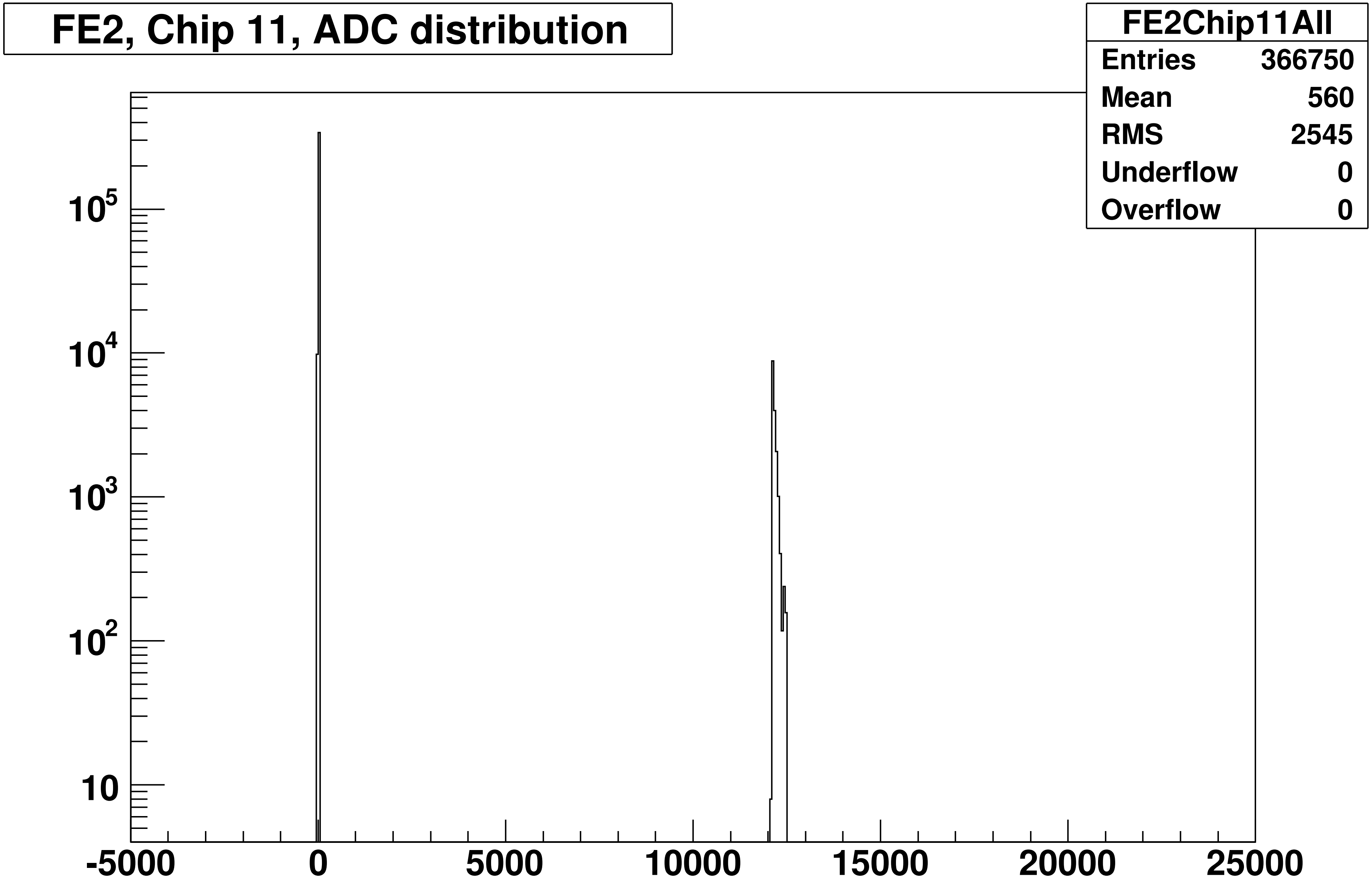
FE2, Chip 11, ADC distribution
FE2Chip11All
Entries 366750
Mean 560
RMS 2545
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
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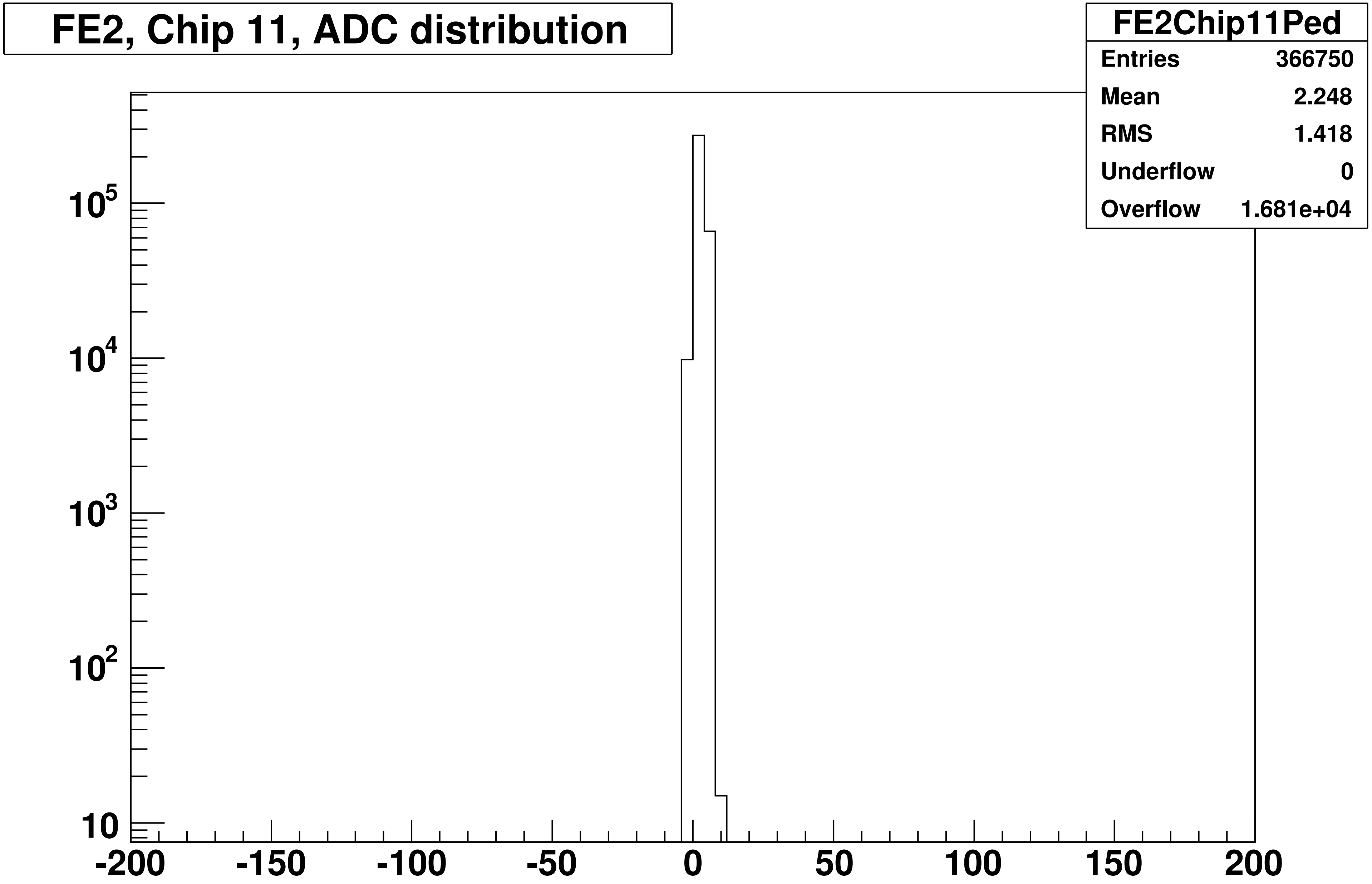
25000



FE2, Chip 11, ADC distribution
FE2Chip11Ped
Entries 366750
Mean 2.248
RMS 1.418
Underflow 0
Overflow 1.681e+04
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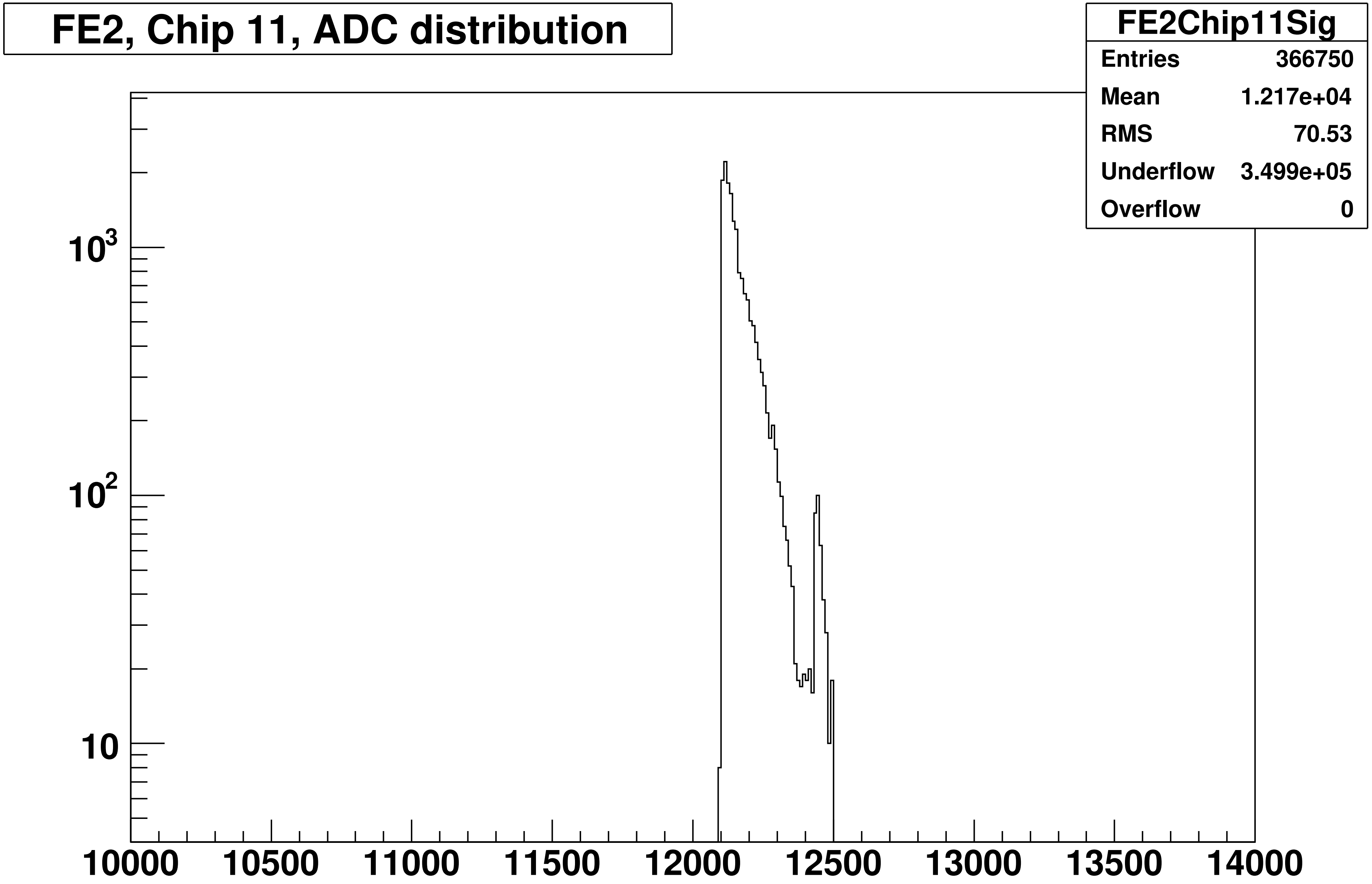
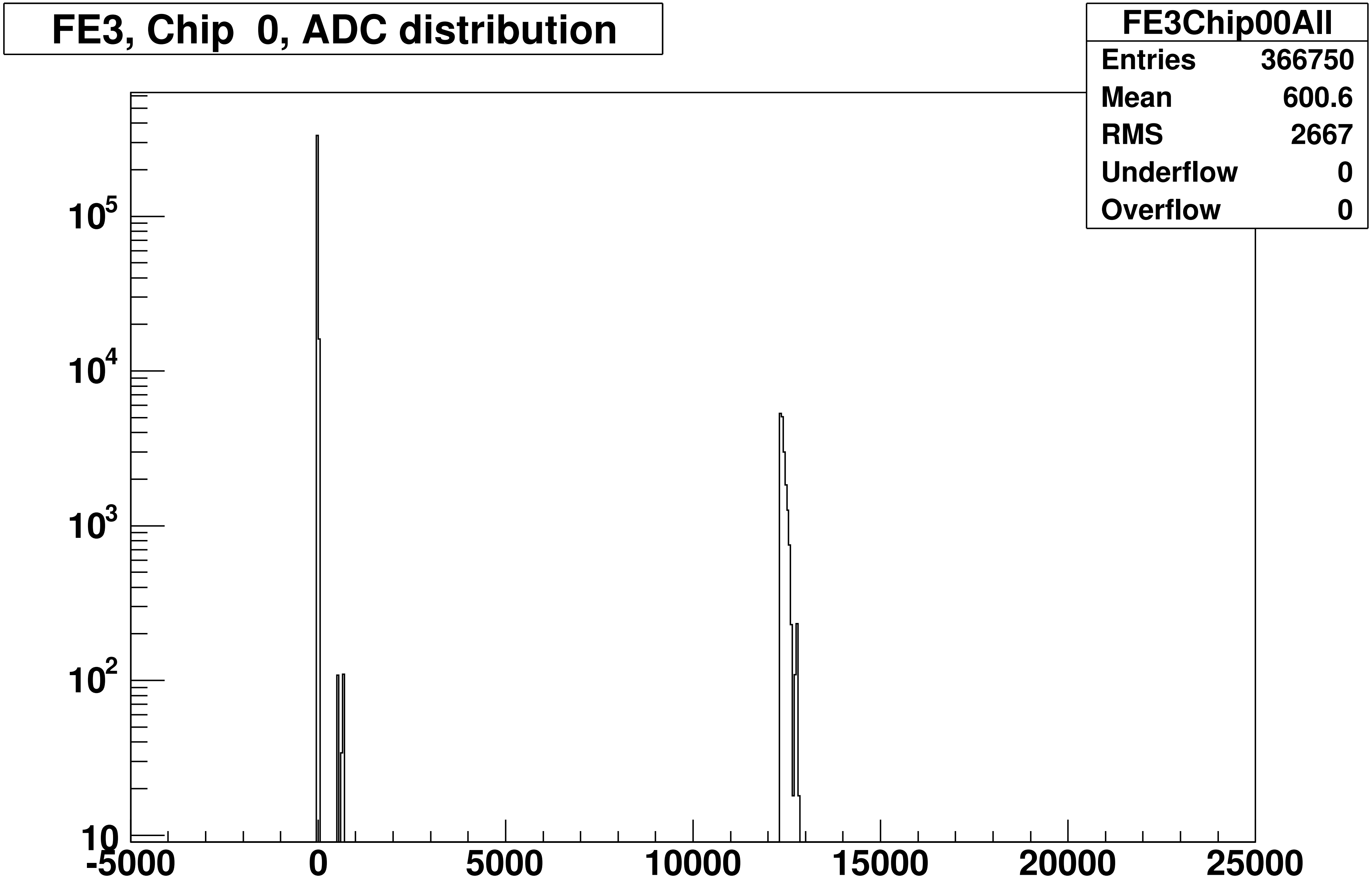
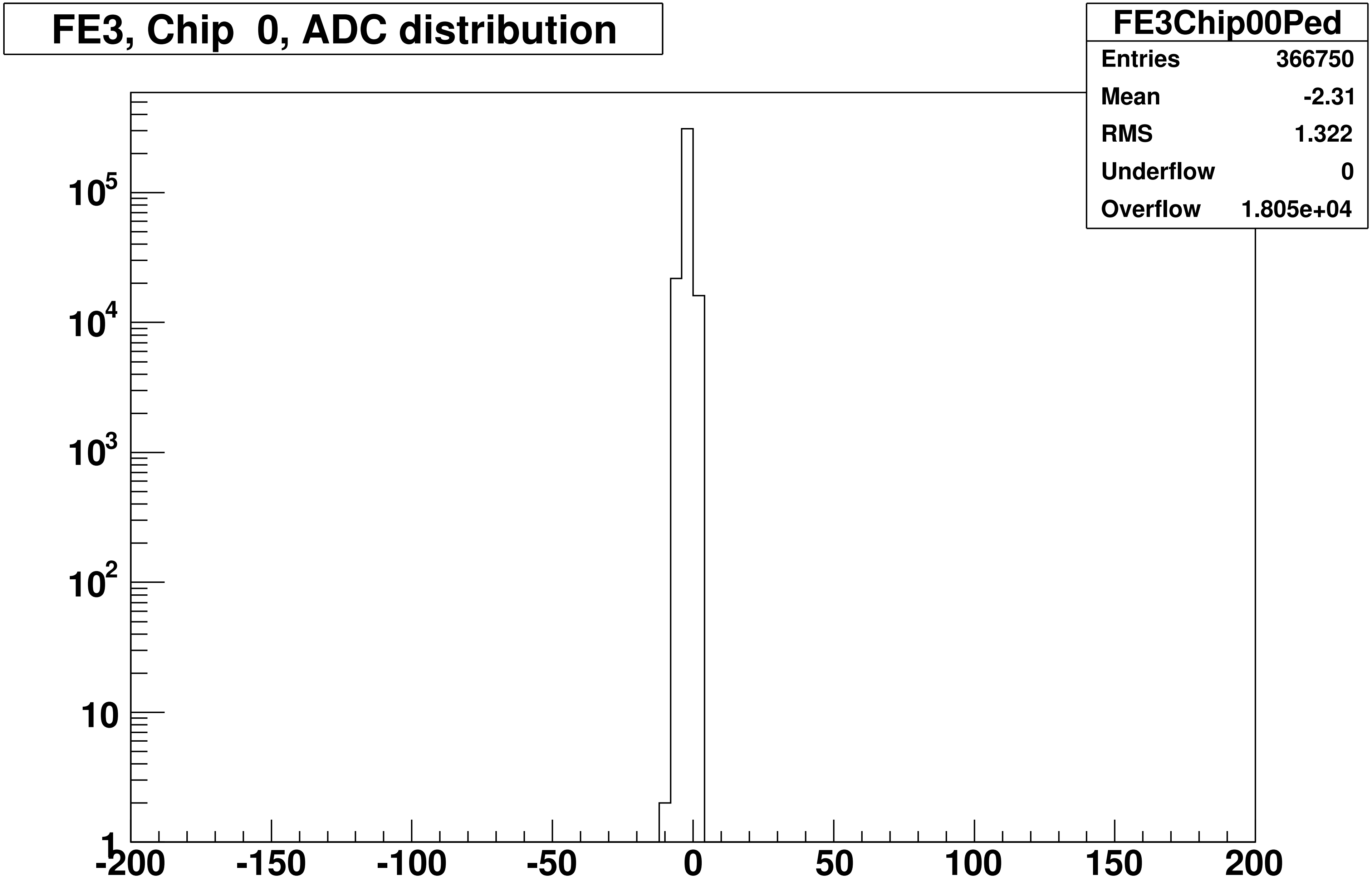
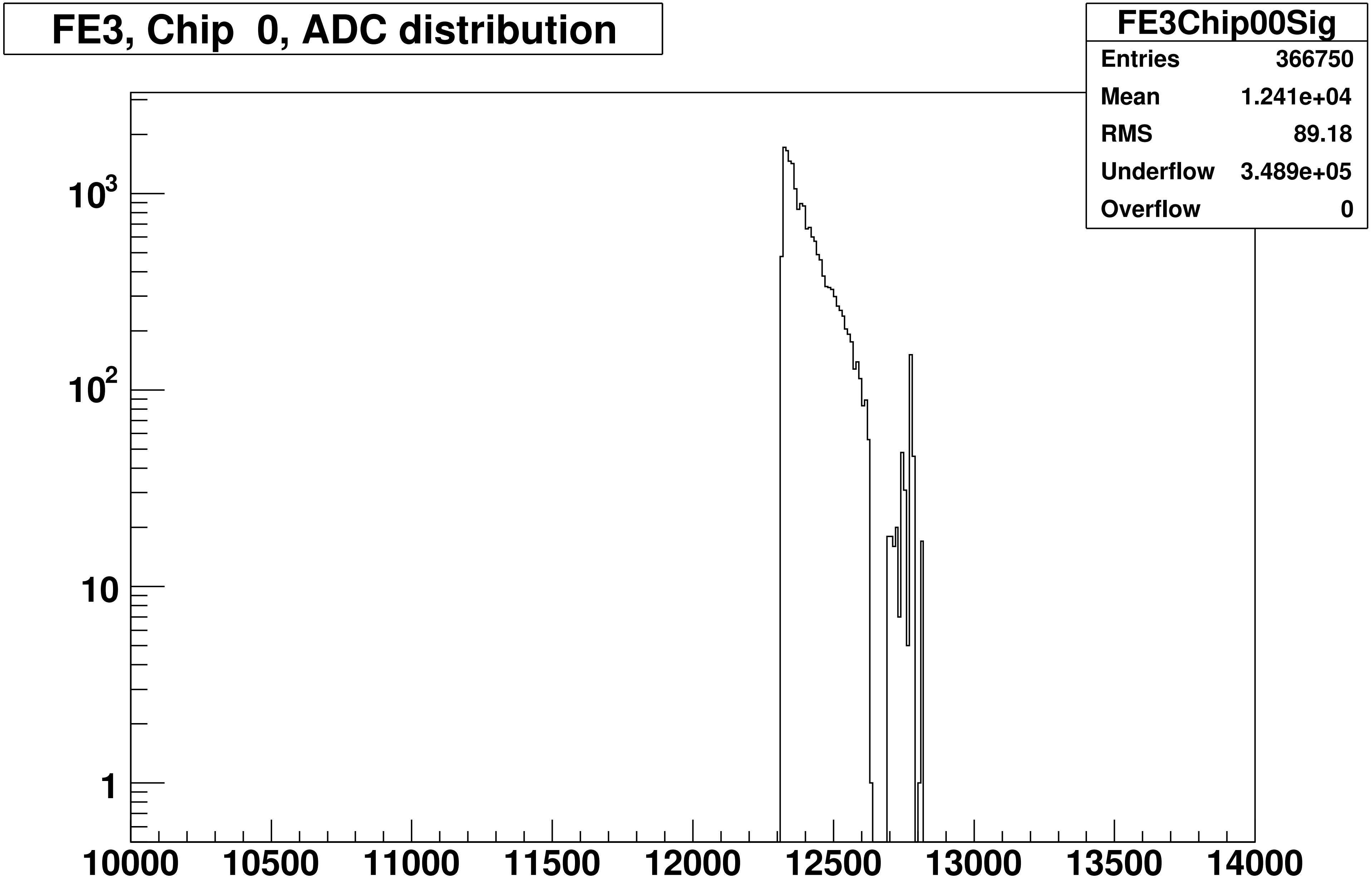
10^2
10^3
10^4
10^5
-200
-150
-100
-50
0
50
100
150
200



FE2, Chip 11, ADC distribution
FE2Chip11Sig
Entries 366750
Mean 1.217e+04
RMS 70.53
Underflow 3.499e+05
Overflow 0
10^3
10^2
10
10000
10500
11000
11500
12000
12500
13000
13500
14000


FE3, Chip 0, ADC distribution
FE3Chip00All
Entries 366750
Mean 600.6
RMS 2667
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE3, Chip 0, ADC distribution
FE3Chip00Ped
Entries 366750
Mean -2.31
RMS 1.322
Underflow 0
Overflow 1.805e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
200


FE3, Chip 0, ADC distribution
FE3Chip00Sig
Entries 366750
Mean 1.241e+04
RMS 89.18
Underflow 3.489e+05
Overflow 0
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10²
10
1
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10500
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11500
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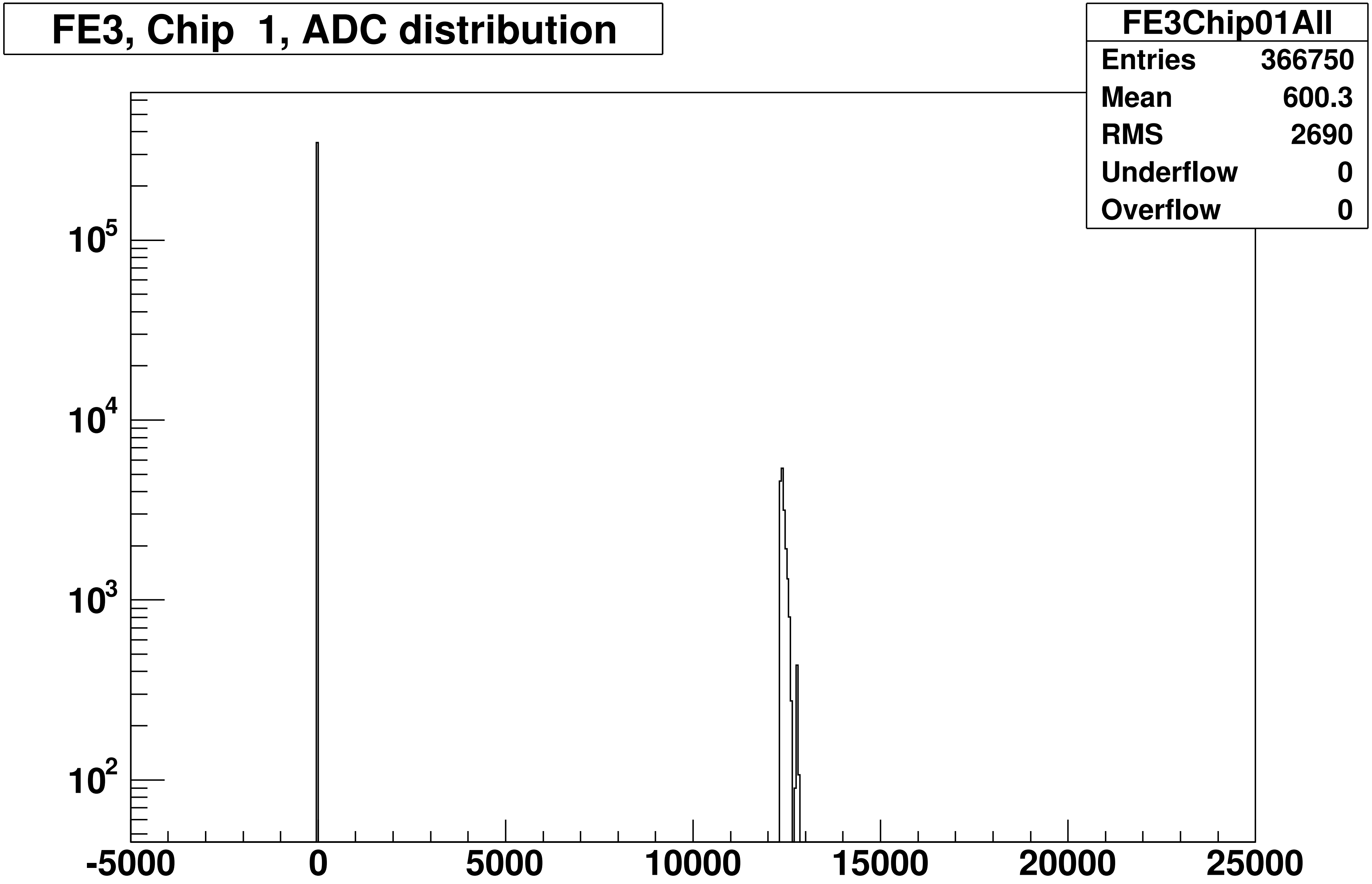
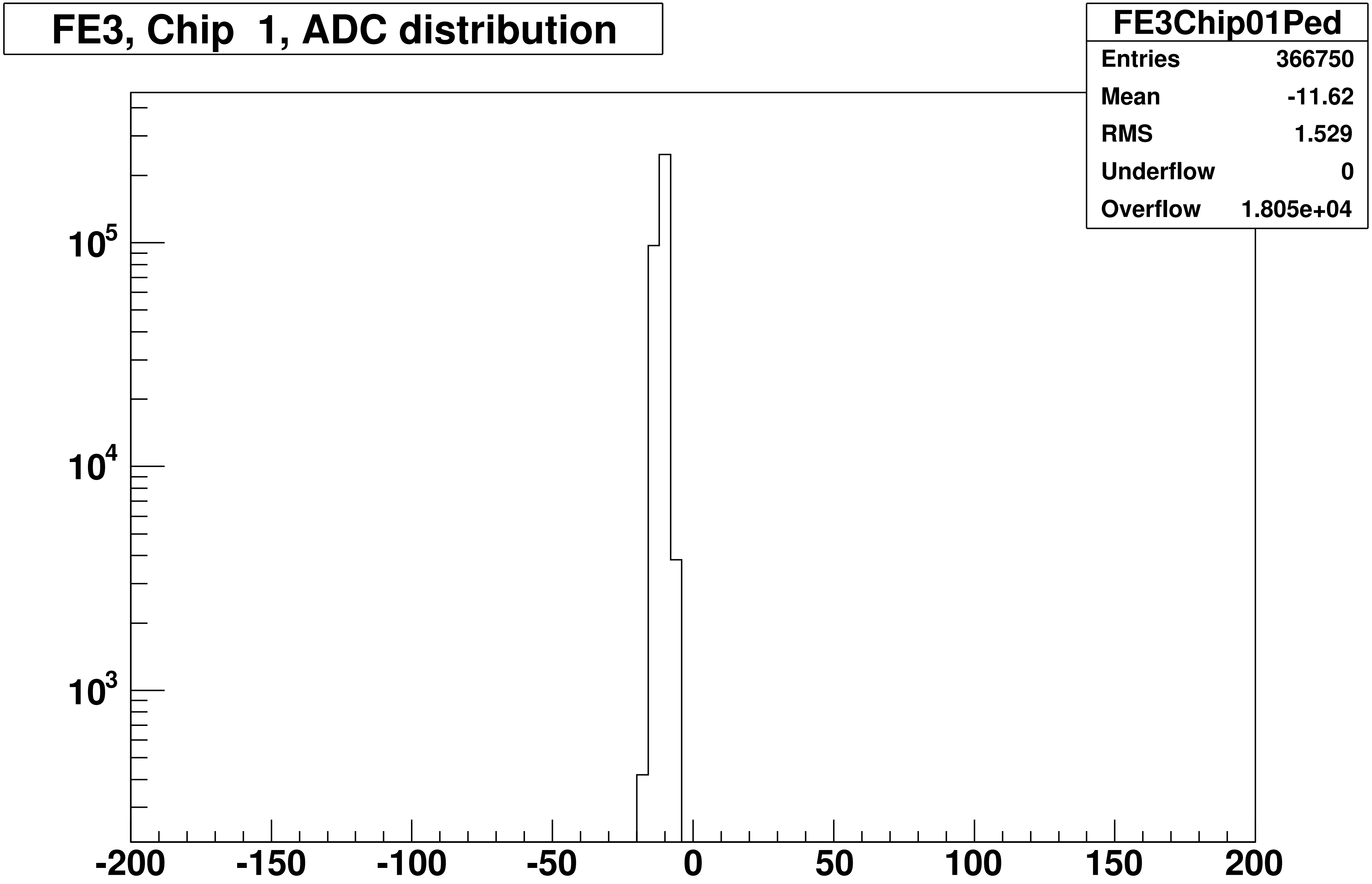
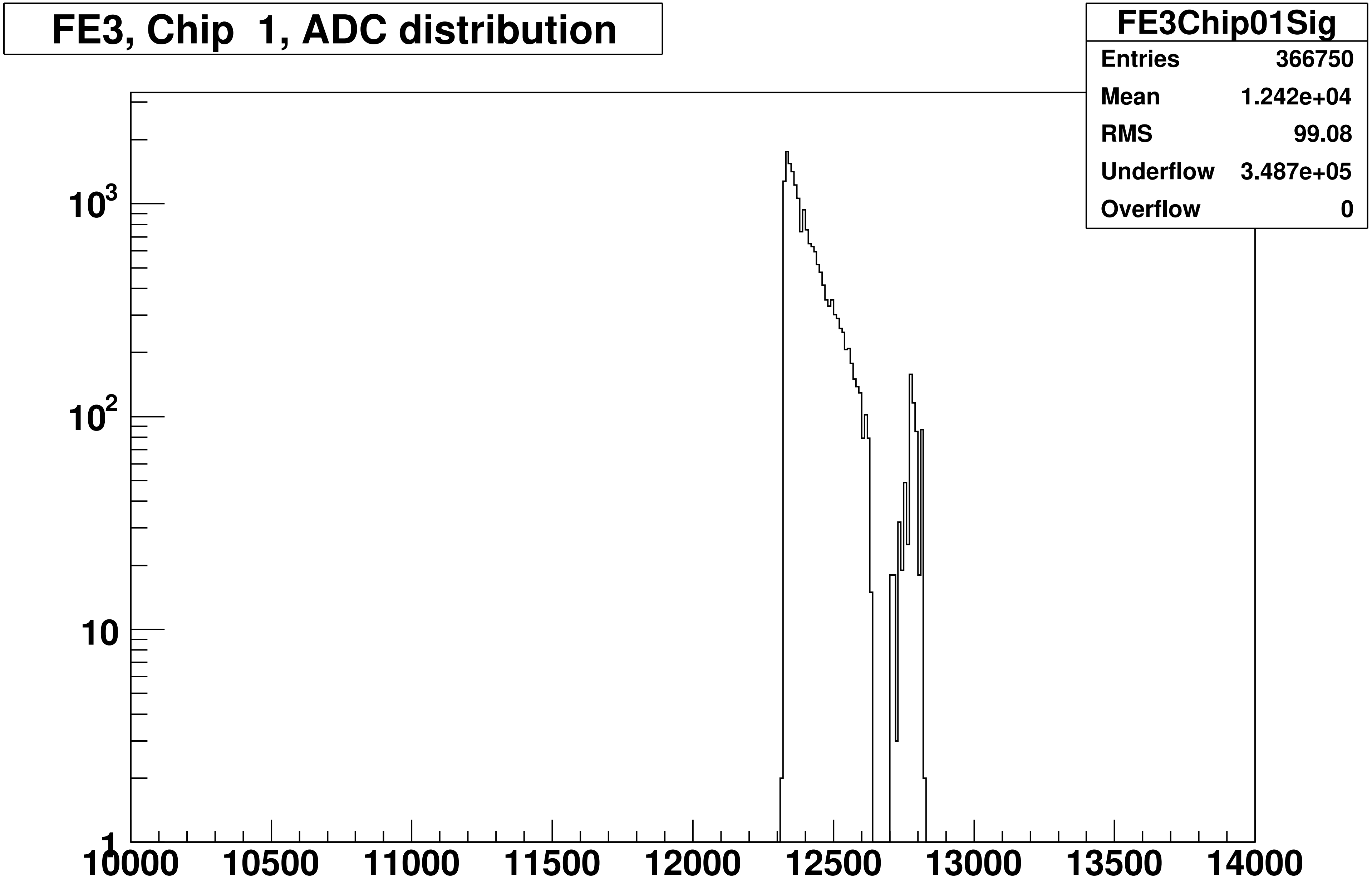
14000


FE3, Chip 1, ADC distribution
FE3Chip01All
Entries 366750
Mean 600.3
RMS 2690
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000



FE3, Chip 1, ADC distribution
FE3Chip01Ped
Entries 366750
Mean -11.62
RMS 1.529
Underflow 0
Overflow 1.805e+04
10^5
10^4
10^3
-200
-150
-100
-50
0
50
100
150
200


FE3, Chip 1, ADC distribution
FE3Chip01Sig
Entries 366750
Mean 1.242e+04
RMS 99.08
Underflow 3.487e+05
Overflow 0
10^3
10^2
10
1
10000
10500
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11500
12000
12500
13000
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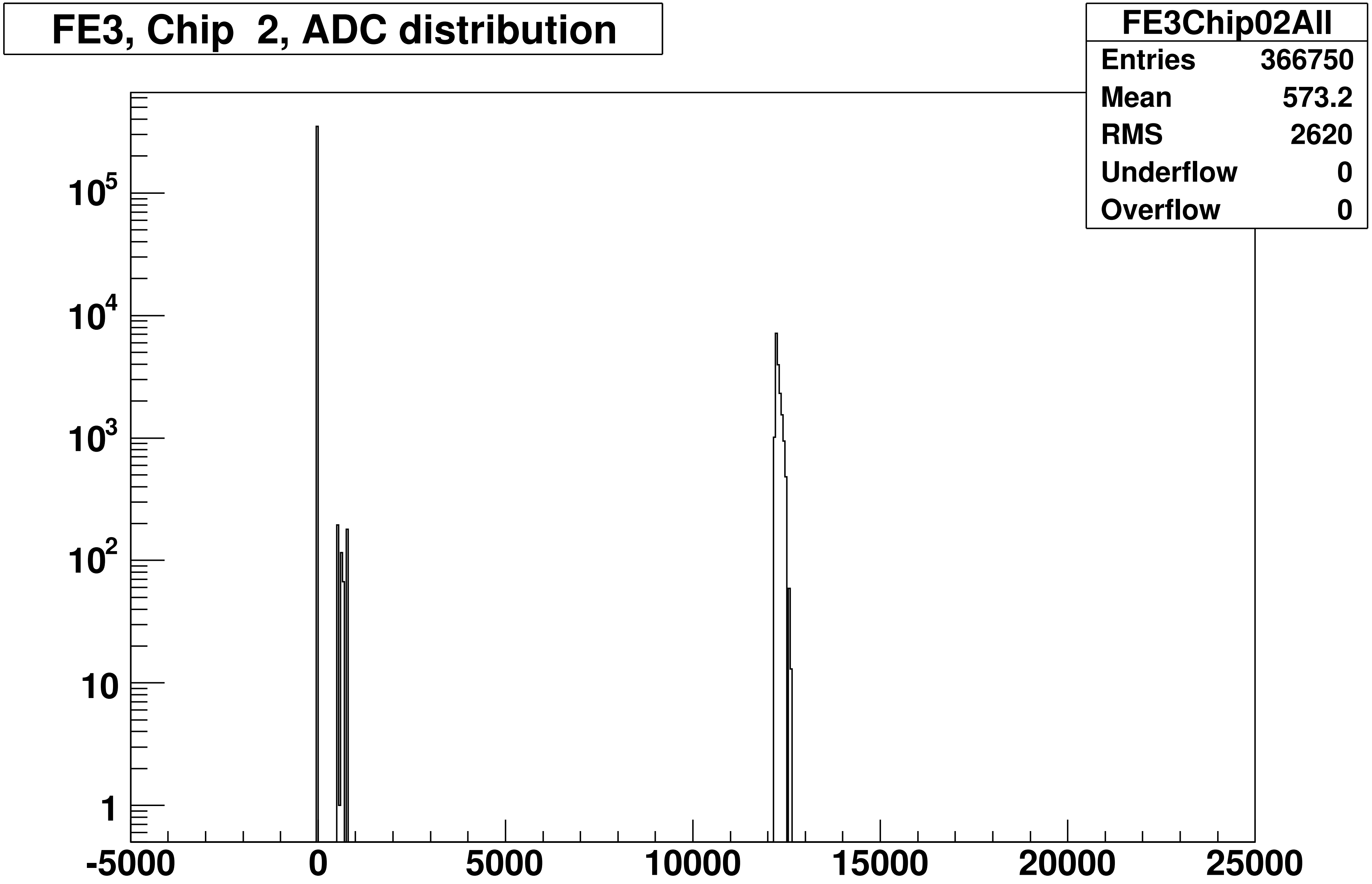

FE3, Chip 2, ADC distribution
FE3Chip02All
Entries 366750
Mean 573.2
RMS 2620
Underflow 0
Overflow 0
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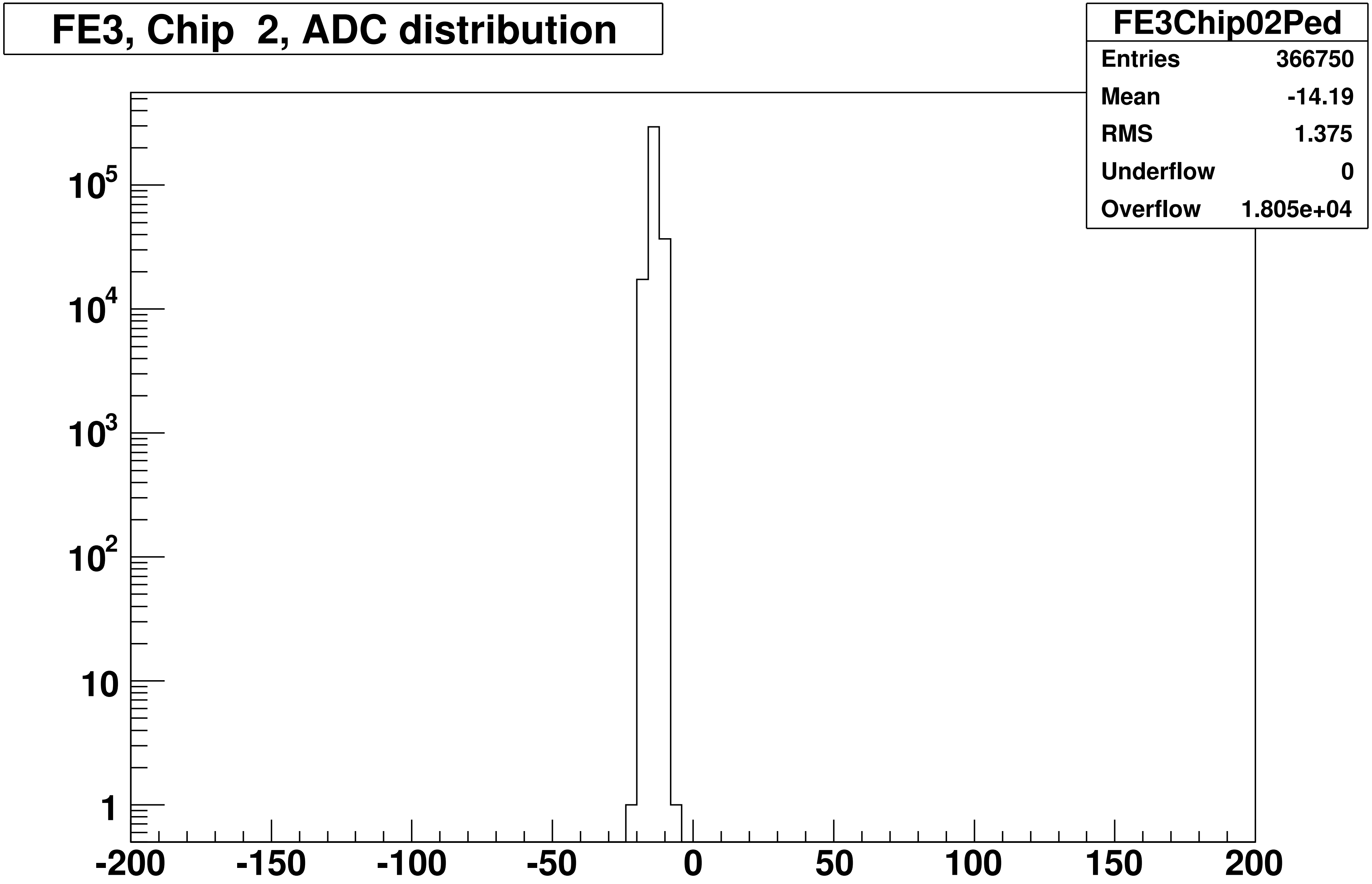
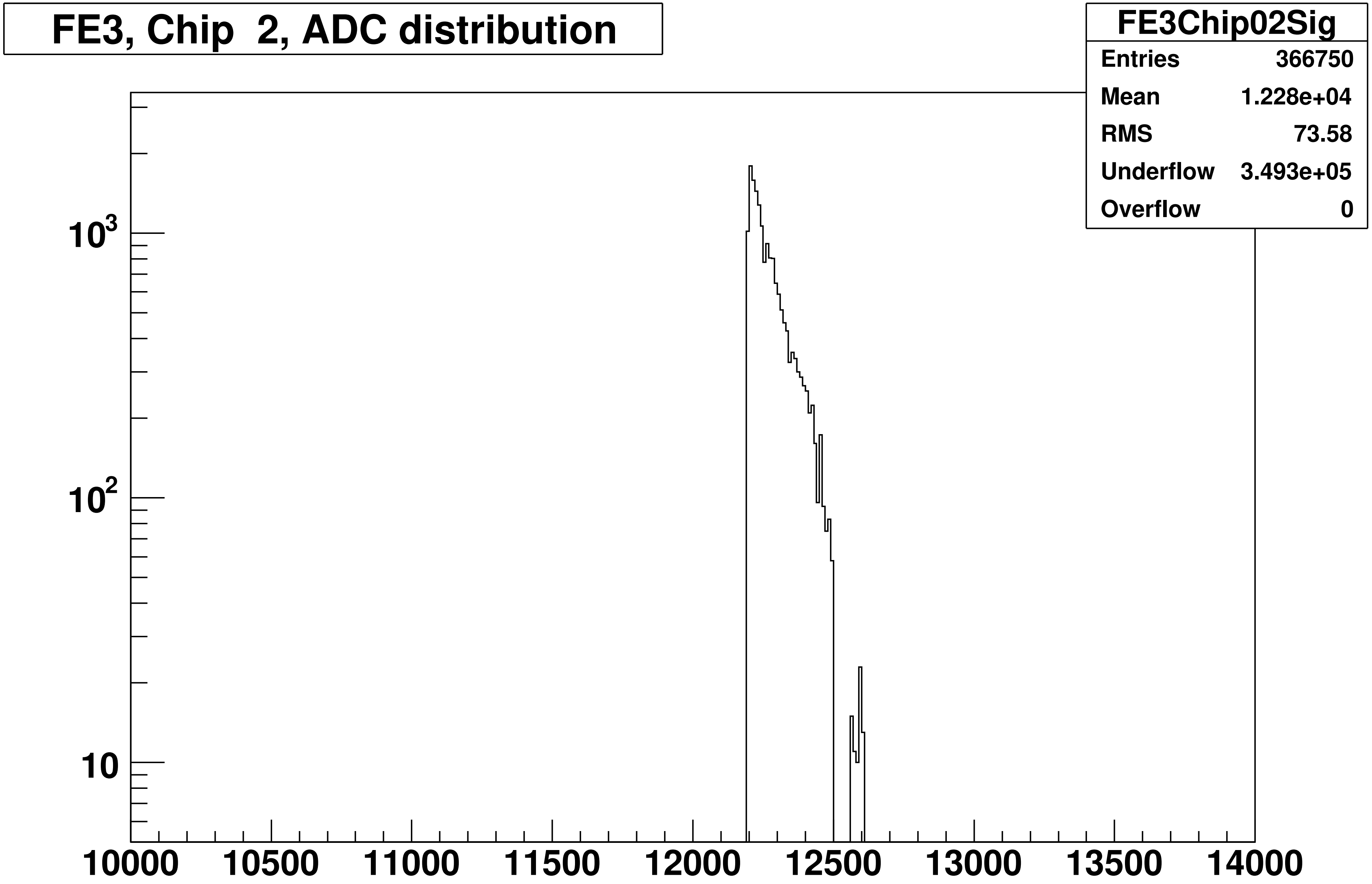
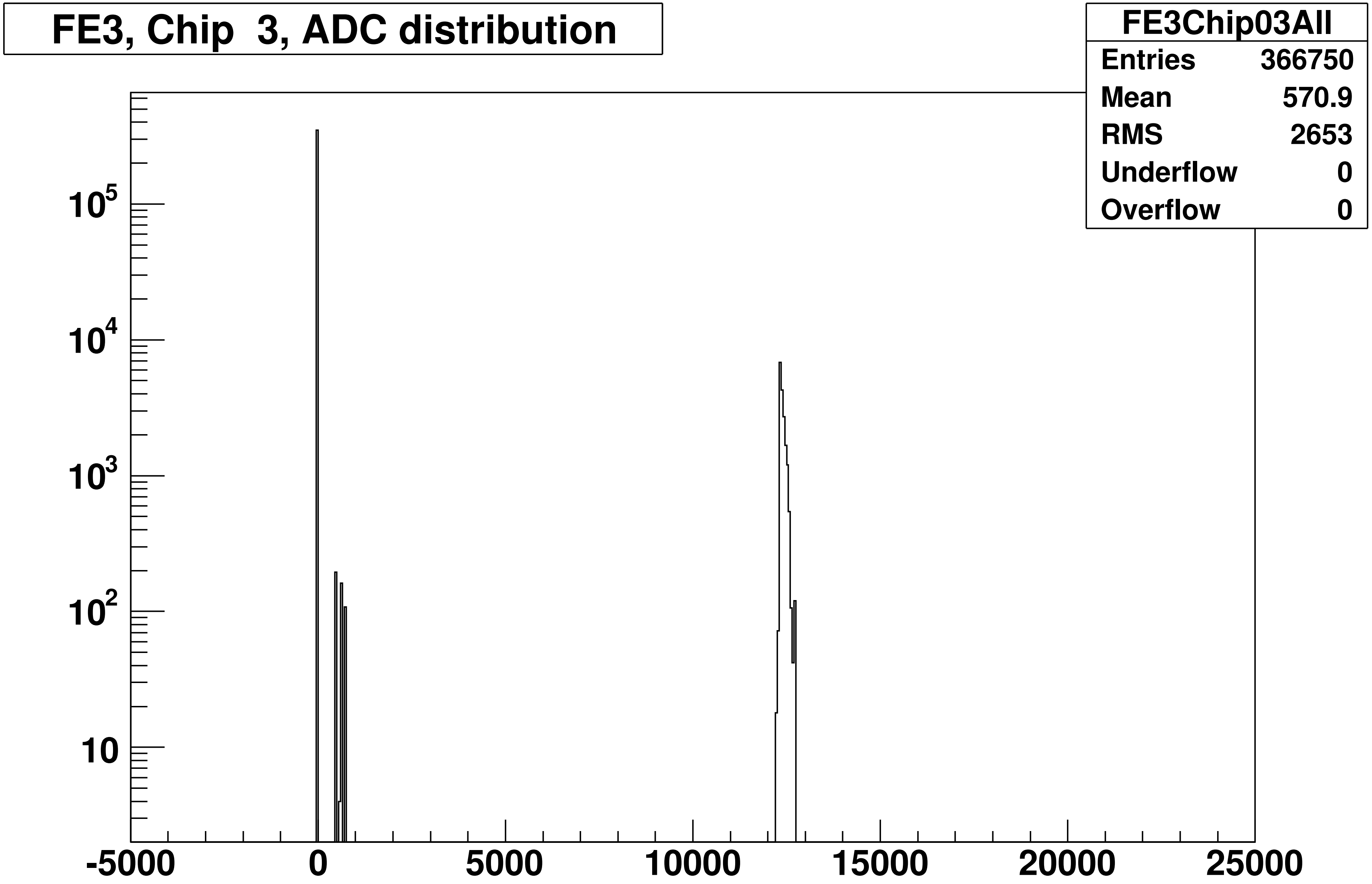
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE3, Chip 2, ADC distribution
FE3Chip02Ped
Entries 366750
Mean -14.19
RMS 1.375
Underflow 0
Overflow 1.805e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
200



FE3, Chip 2, ADC distribution
FE3Chip02Sig
Entries 366750
Mean 1.228e+04
RMS 73.58
Underflow 3.493e+05
Overflow 0
10
10^2
10^3
10000
10500
11000
11500
12000
12500
13000
13500
14000



FE3, Chip 3, ADC distribution
FE3Chip03All
Entries 366750
Mean 570.9
RMS 2653
Underflow 0
Overflow 0
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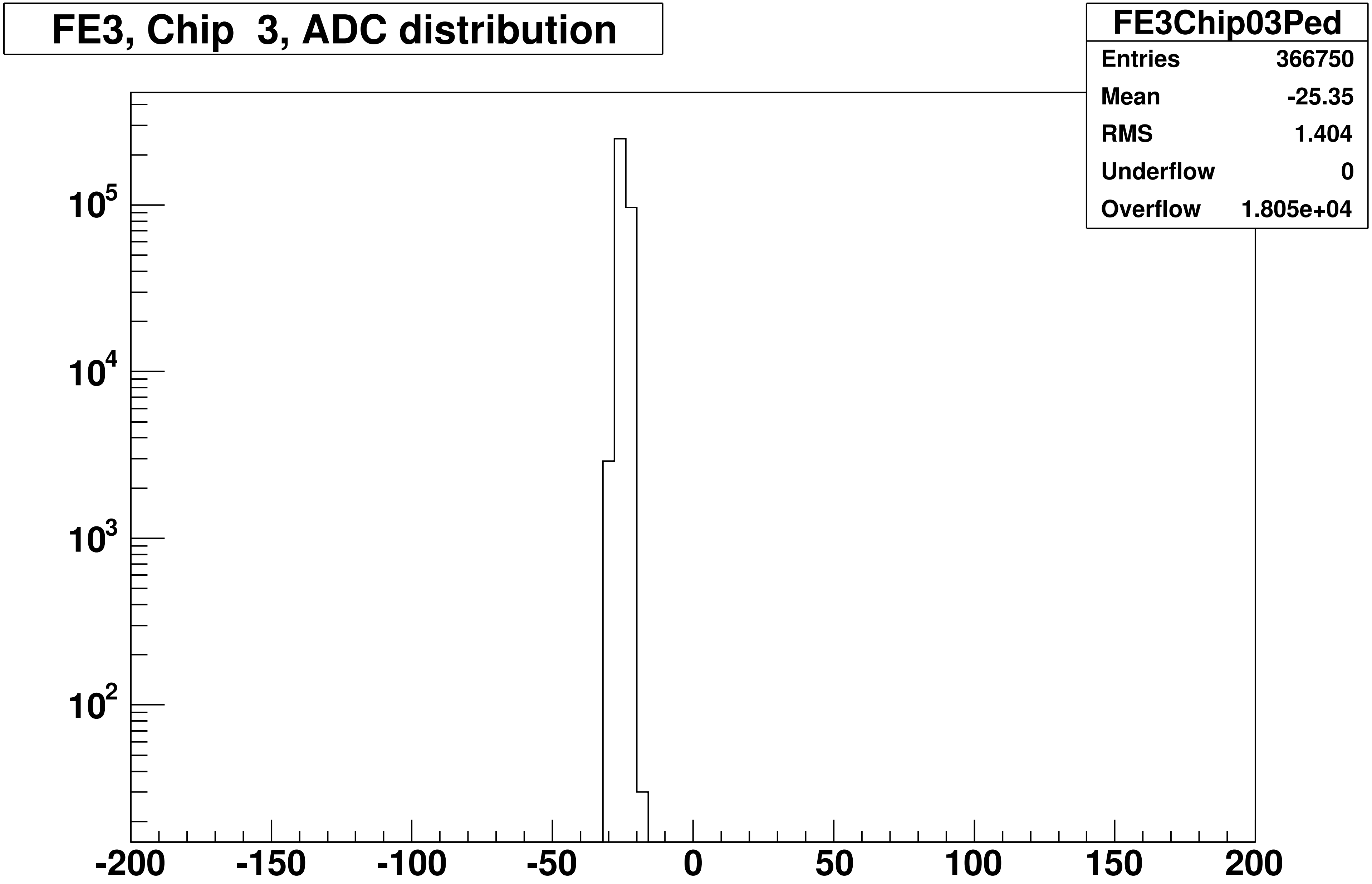
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000



FE3, Chip 3, ADC distribution
FE3Chip03Ped
Entries 366750
Mean -25.35
RMS 1.404
Underflow 0
Overflow 1.805e+04
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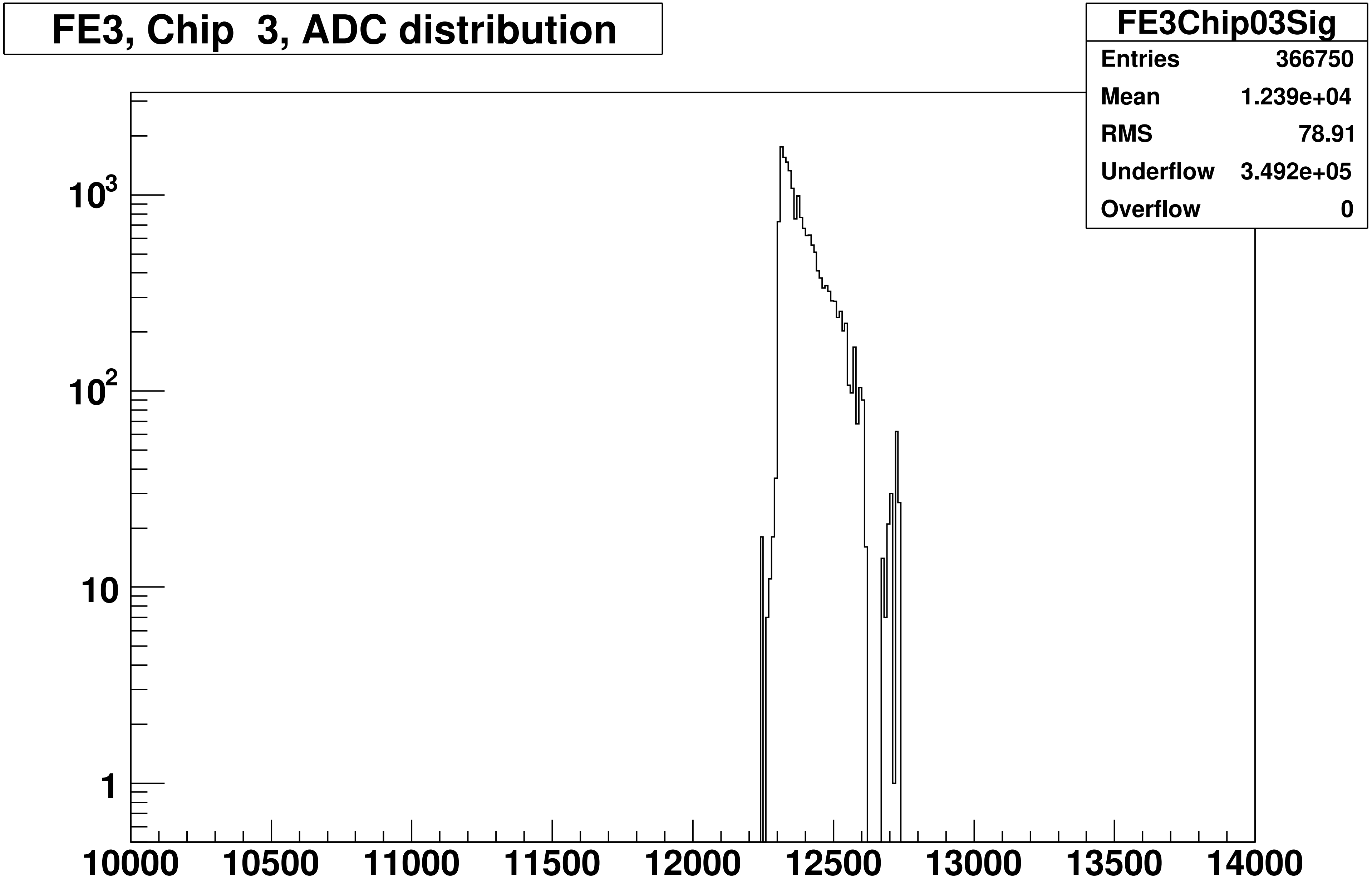
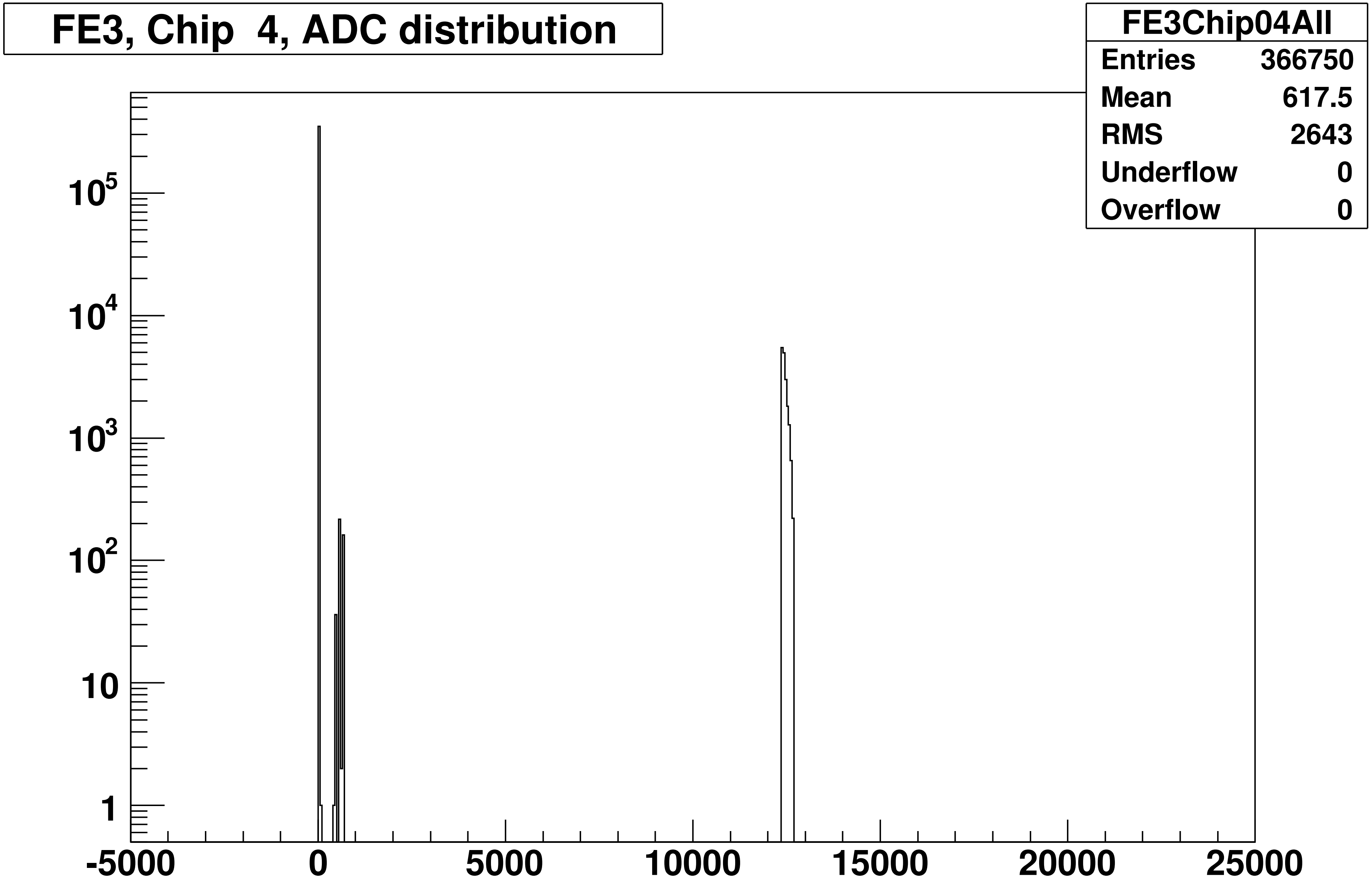
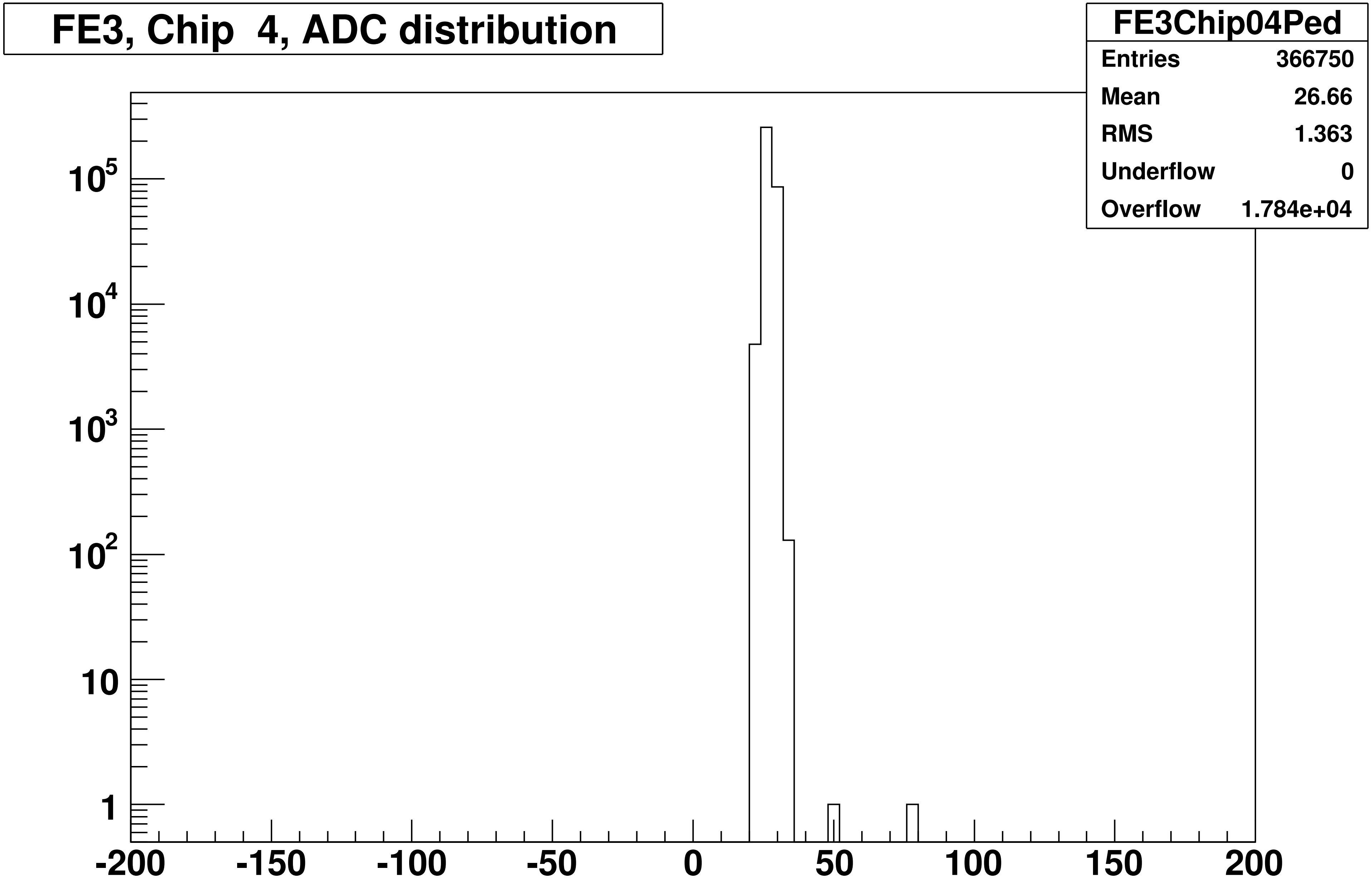
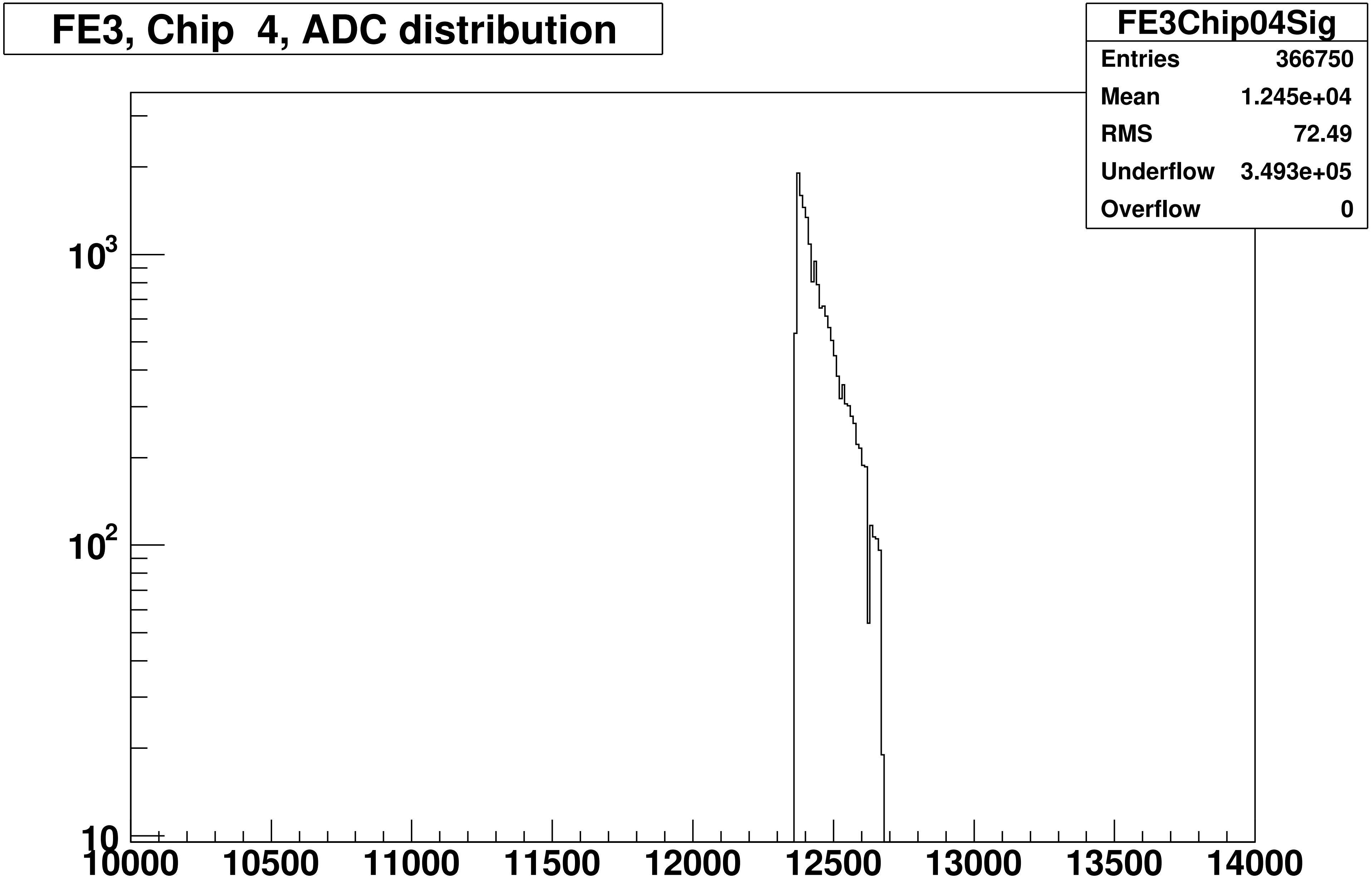
10^4
10^3
10^2
-200
-150
-100
-50
0
50
100
150
200

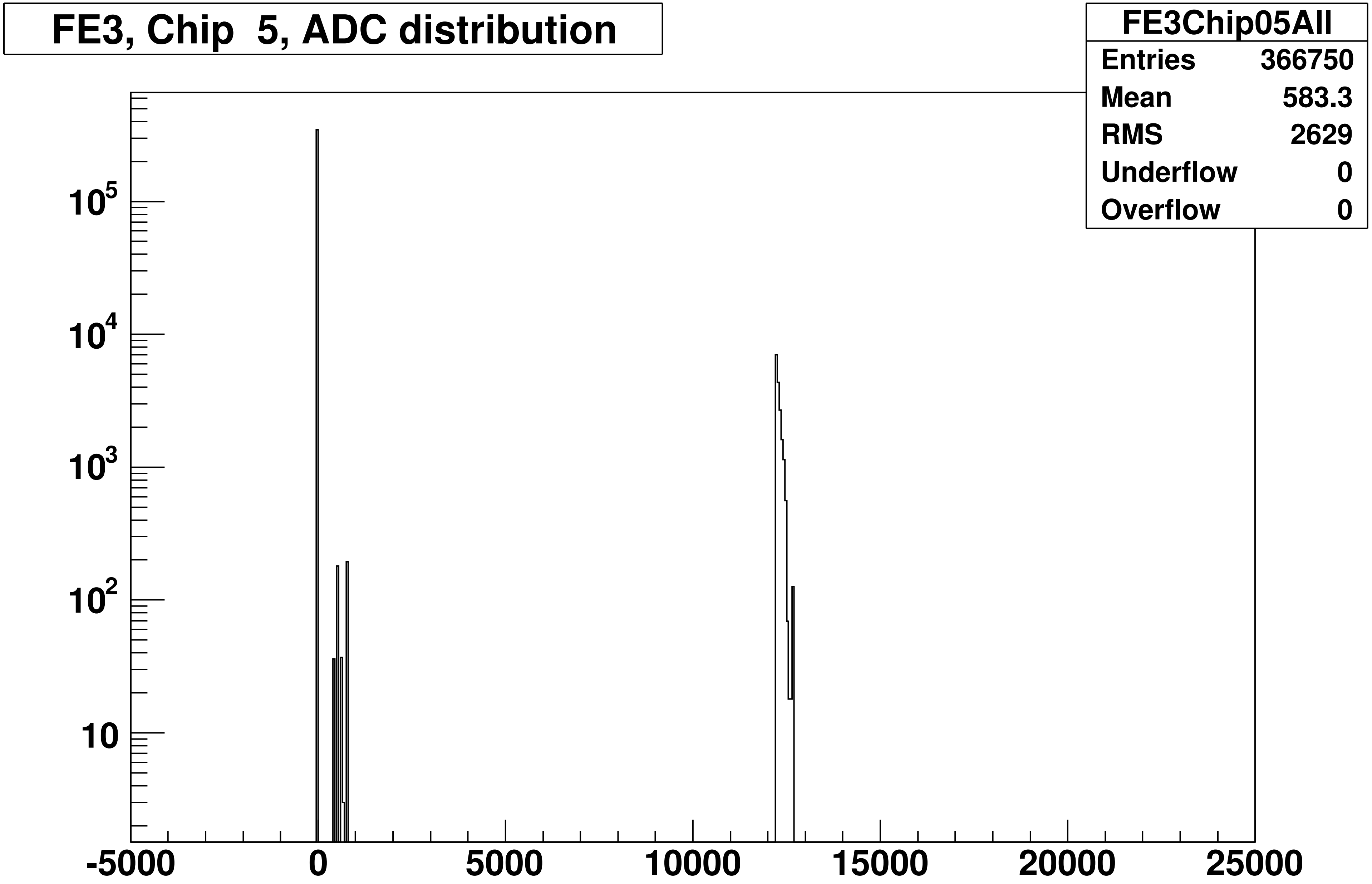

FE3, Chip 3, ADC distribution
FE3Chip03Sig
Entries 366750
Mean 1.239e+04
RMS 78.91
Underflow 3.492e+05
Overflow 0
10^3
10^2
10
1
10000
10500
11000
11500
12000
12500
13000
13500
14000


FE3, Chip 4, ADC distribution
FE3Chip04All
Entries 366750
Mean 617.5
RMS 2643
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE3, Chip 4, ADC distribution
FE3Chip04Ped
Entries 366750
Mean 26.66
RMS 1.363
Underflow 0
Overflow 1.784e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
200


FE3, Chip 4, ADC distribution
FE3Chip04Sig
Entries 366750
Mean 1.245e+04
RMS 72.49
Underflow 3.493e+05
Overflow 0
10^3
10^2
10
10000
10500
11000
11500
12000
12500
13000
13500
14000


FE3, Chip 5, ADC distribution
FE3Chip05All
Entries 366750
Mean 583.3
RMS 2629
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
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20000
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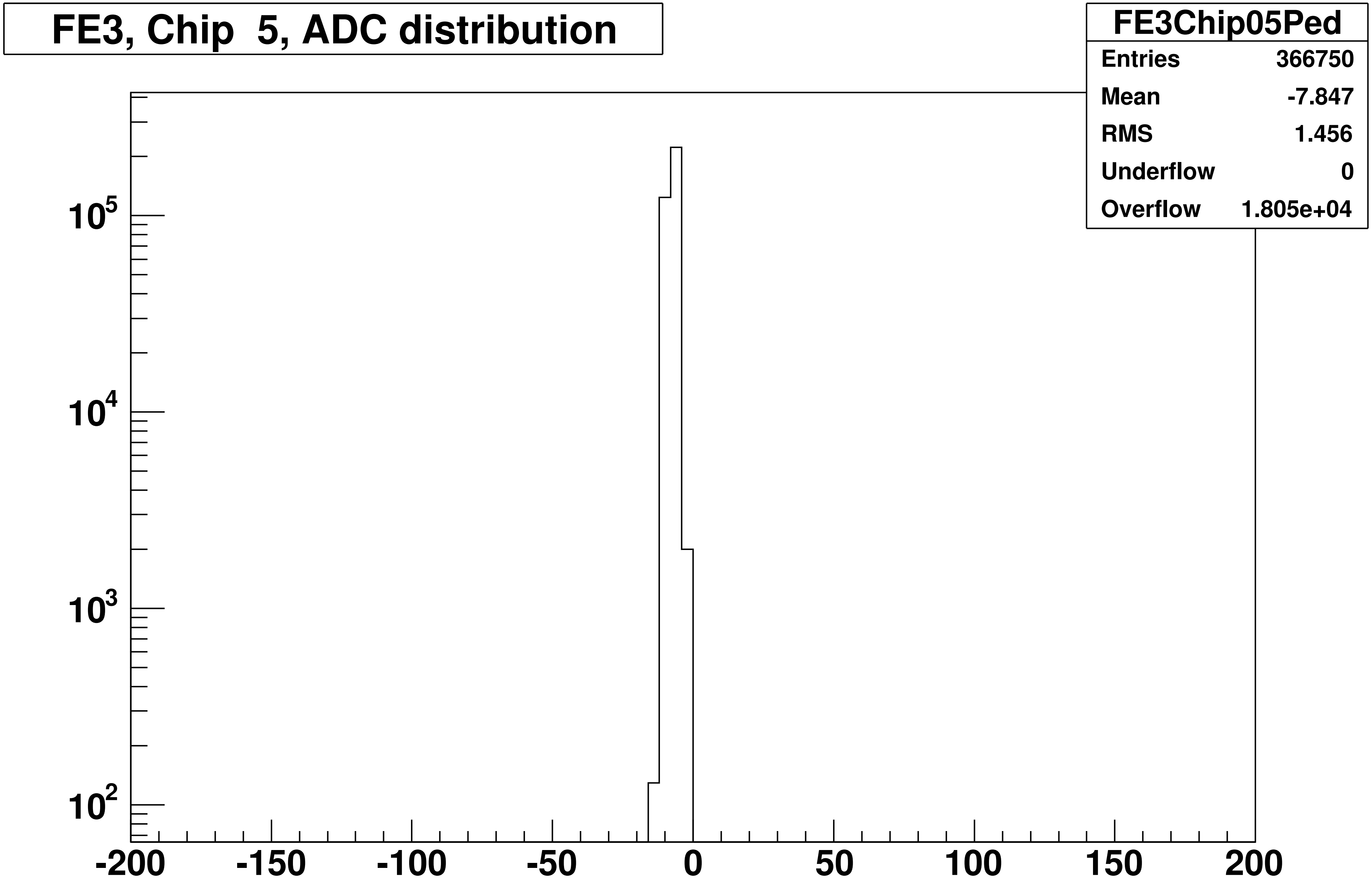

FE3, Chip 5, ADC distribution
FE3Chip05Ped
Entries 366750
Mean -7.847
RMS 1.456
Underflow 0
Overflow 1.805e+04
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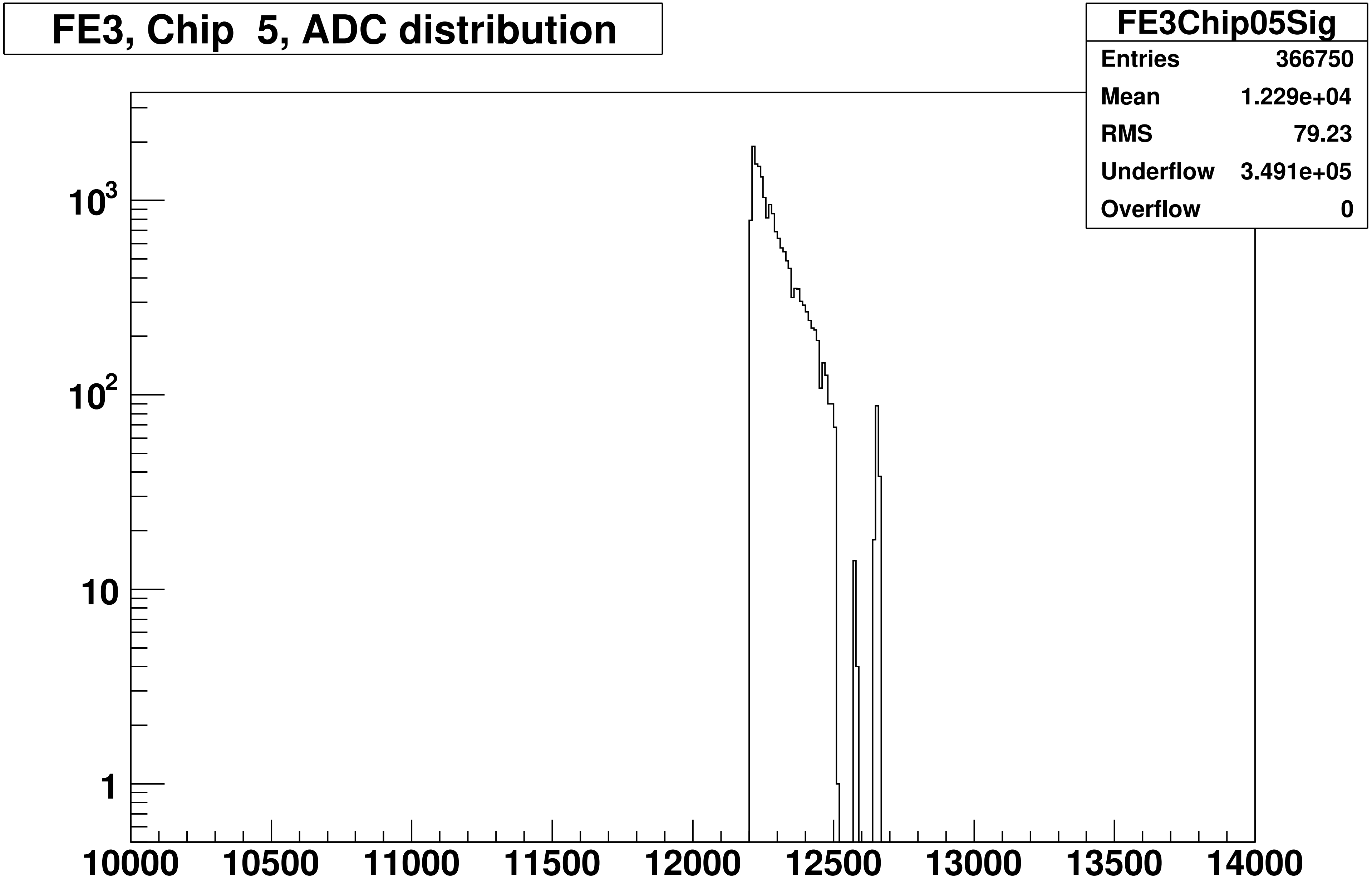
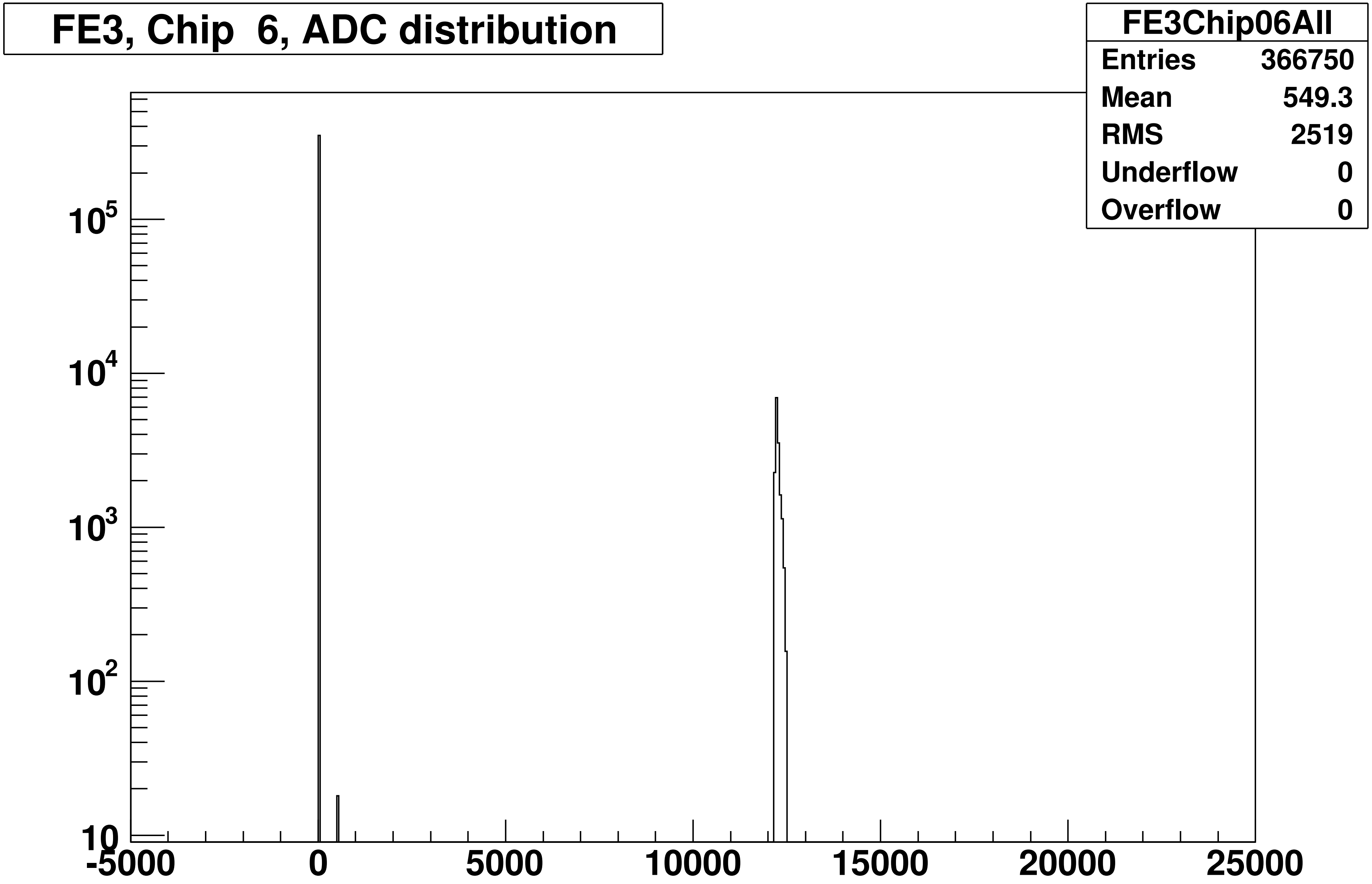
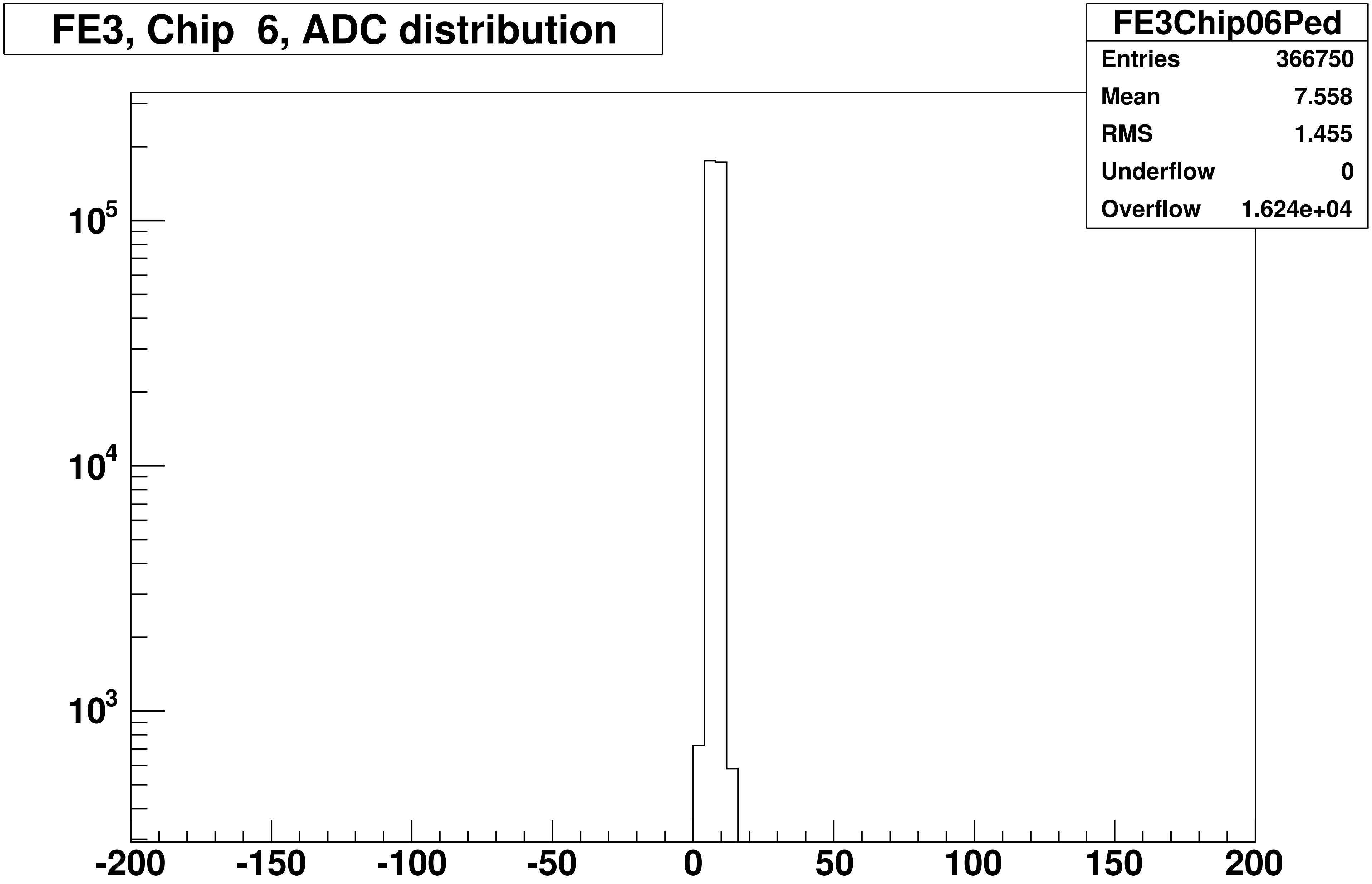
10^4
10^3
10^2
-200
-150
-100
-50
0
50
100
150
200


FE3, Chip 5, ADC distribution
FE3Chip05Sig
Entries 366750
Mean 1.229e+04
RMS 79.23
Underflow 3.491e+05
Overflow 0
10³
10²
10
1
10000
10500
11000
11500
12000
12500
13000
13500
14000


FE3, Chip 6, ADC distribution
FE3Chip06All
Entries 366750
Mean 549.3
RMS 2519
Underflow 0
Overflow 0
10
10^2
10^3
10^4
10^5
-5000
0
5000
10000
15000
20000
25000


FE3, Chip 6, ADC distribution
FE3Chip06Ped
Entries 366750
Mean 7.558
RMS 1.455
Underflow 0
Overflow 1.624e+04
10^5
10^4
10^3
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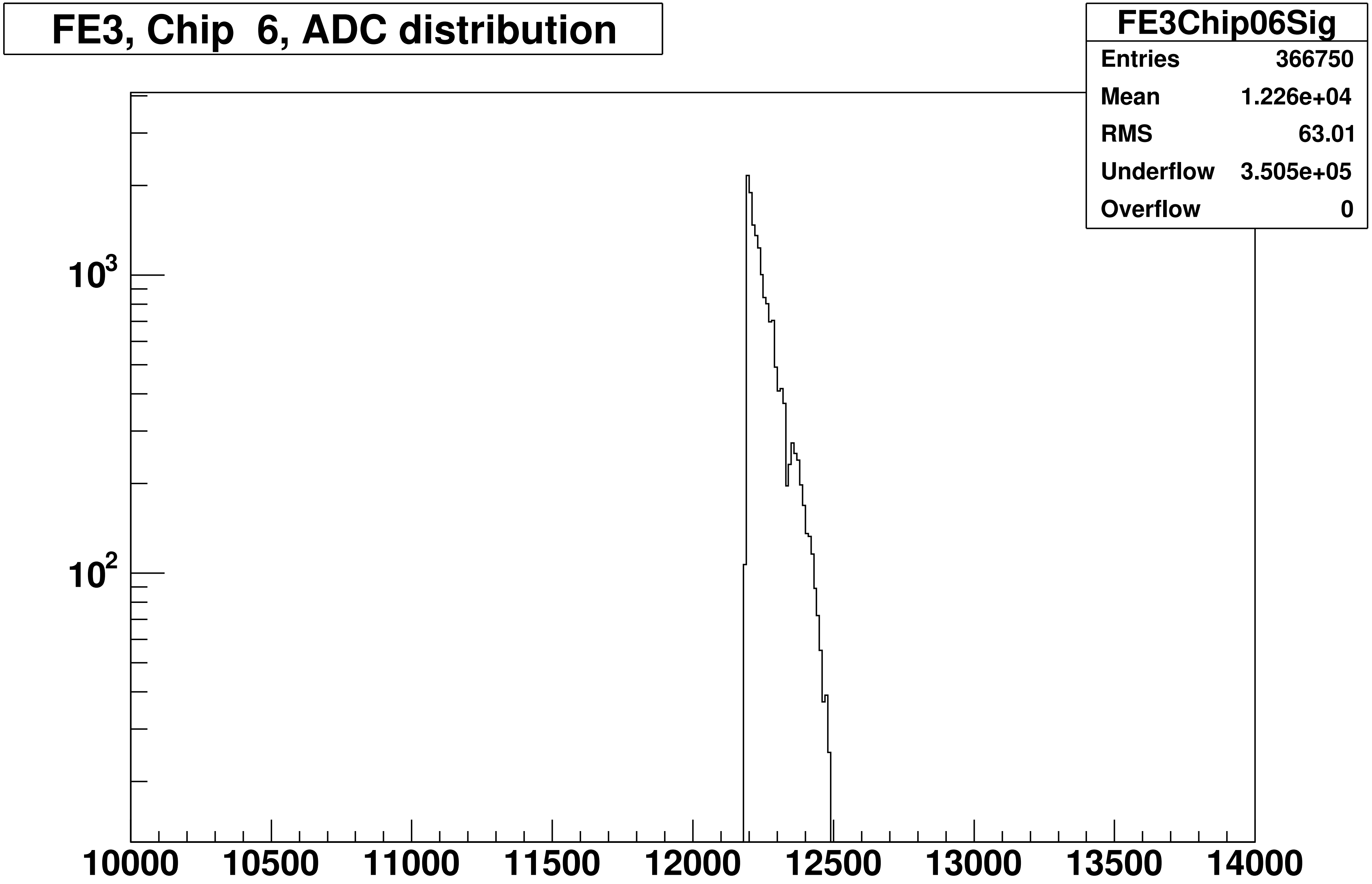
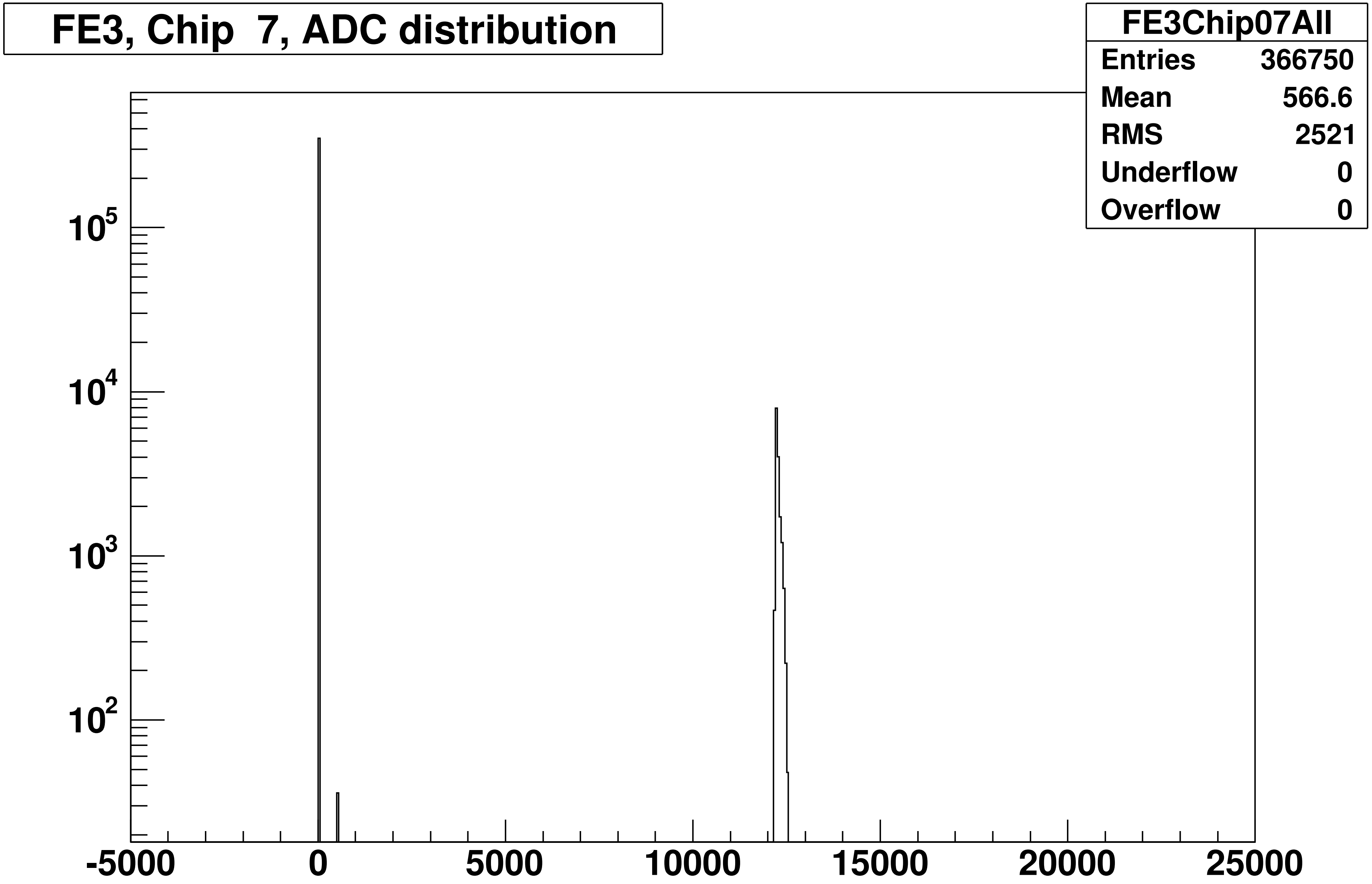
-150
-100
-50
0
50
100
150
200



FE3, Chip 6, ADC distribution
FE3Chip06Sig
Entries 366750
Mean 1.226e+04
RMS 63.01
Underflow 3.505e+05
Overflow 0
10^3
10^2
10000
10500
11000
11500
12000
12500
13000
13500
14000



FE3, Chip 7, ADC distribution
FE3Chip07All
Entries 366750
Mean 566.6
RMS 2521
Underflow 0
Overflow 0
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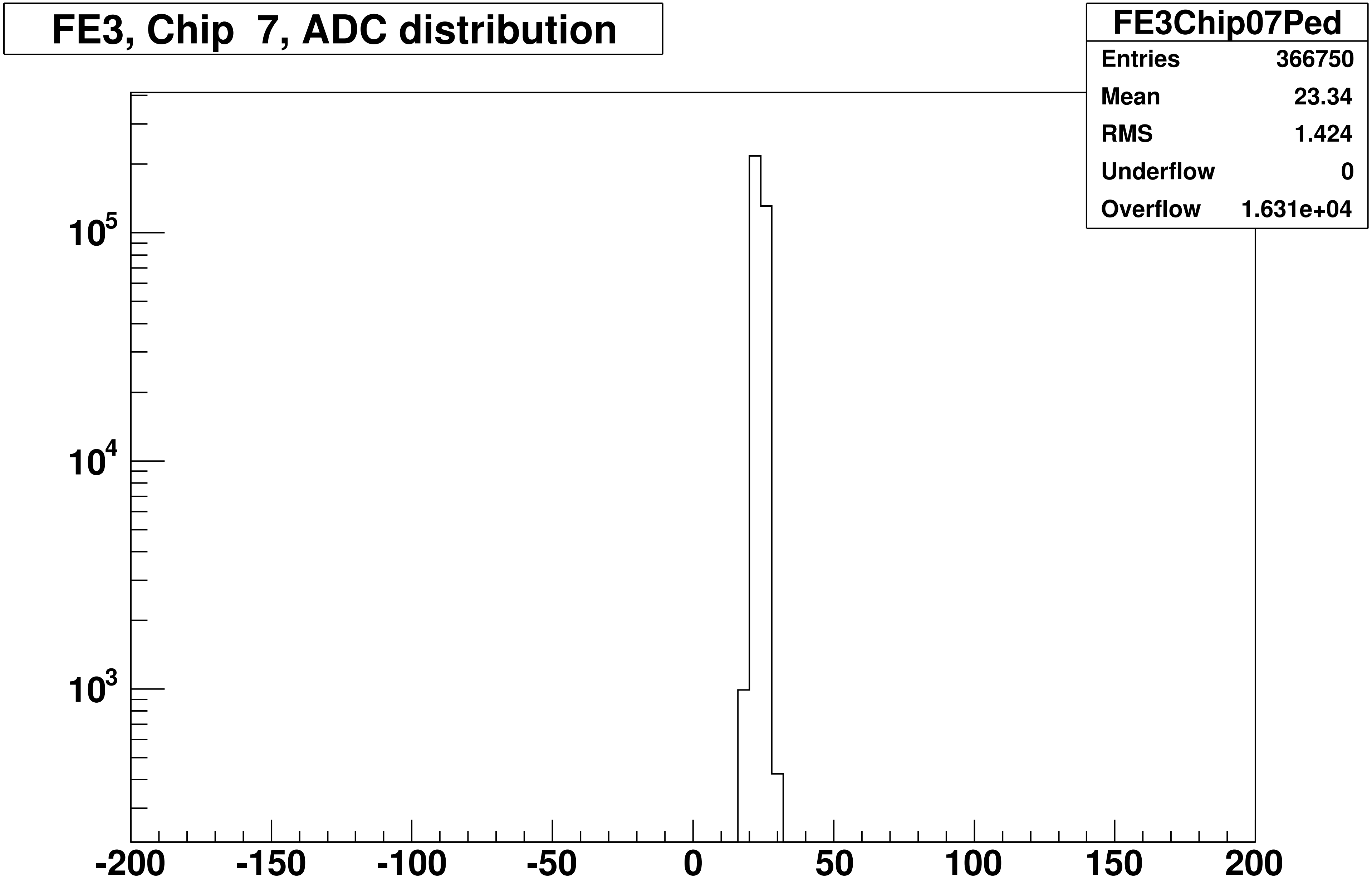
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000


FE3, Chip 7, ADC distribution
FE3Chip07Ped
Entries 366750
Mean 23.34
RMS 1.424
Underflow 0
Overflow 1.631e+04
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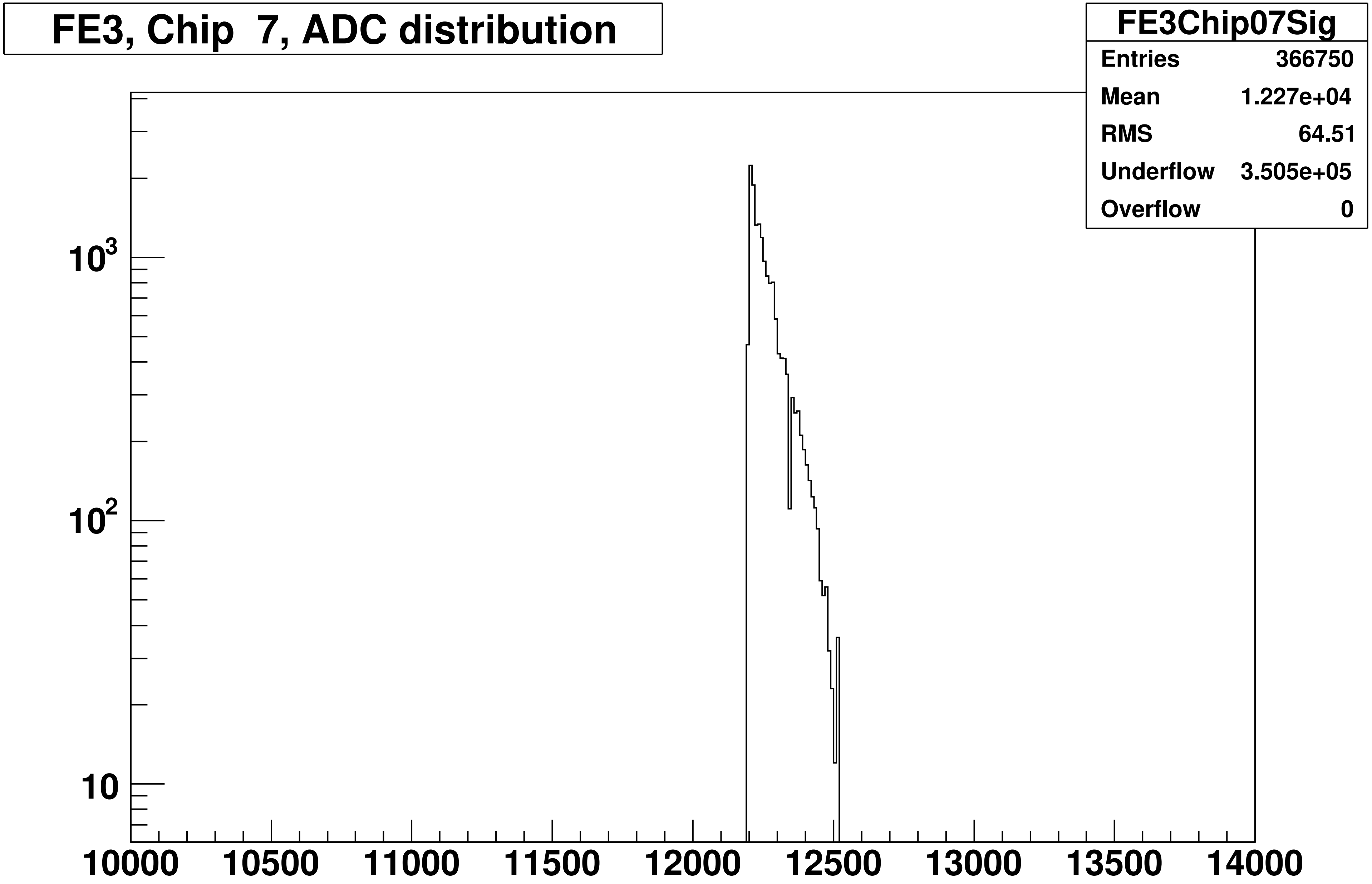
10^4
10^3
-200 -150 -100 -50 0 50 100 150 200


FE3, Chip 7, ADC distribution
FE3Chip07Sig
Entries 366750
Mean 1.227e+04
RMS 64.51
Underflow 3.505e+05
Overflow 0
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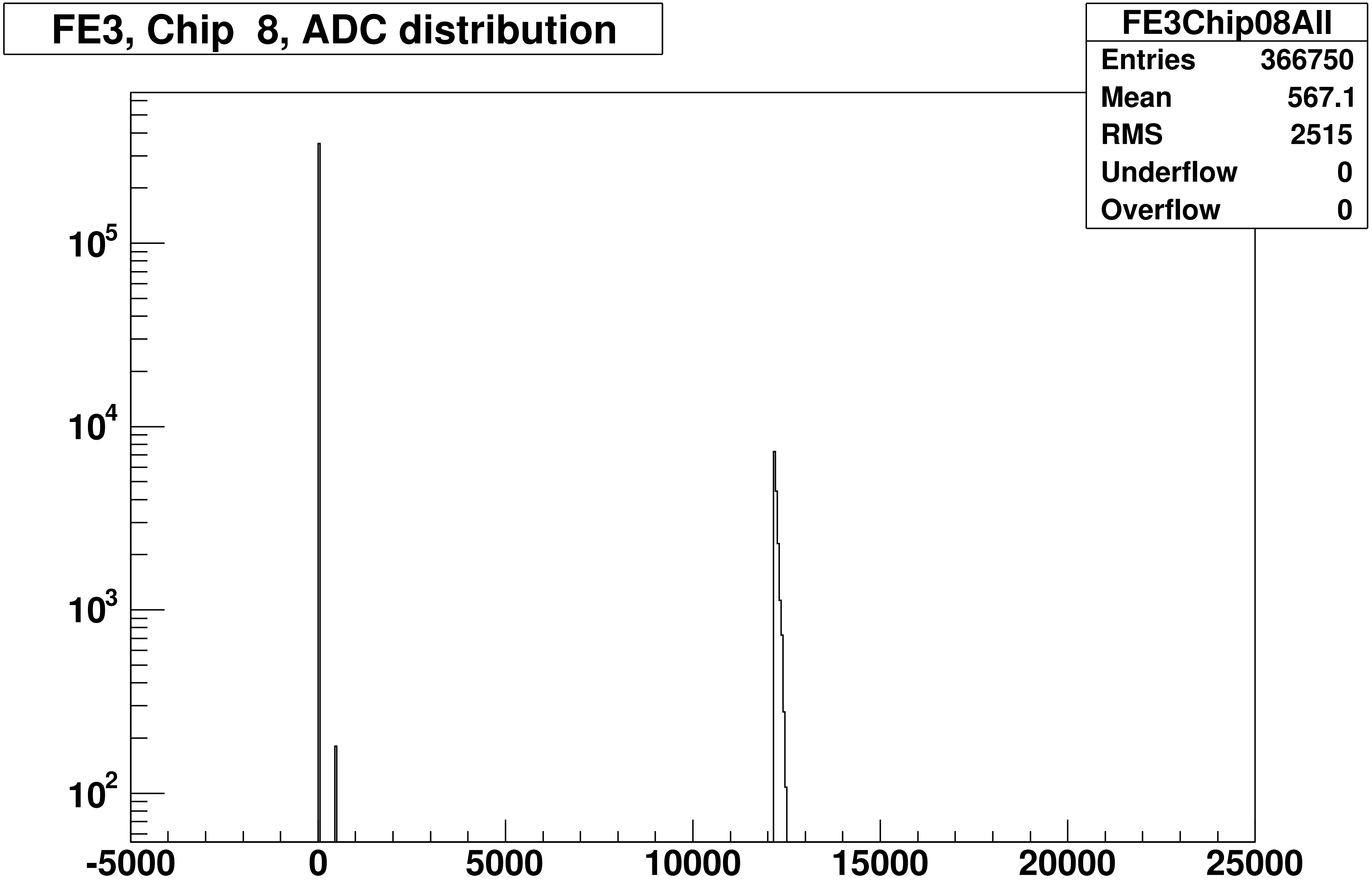
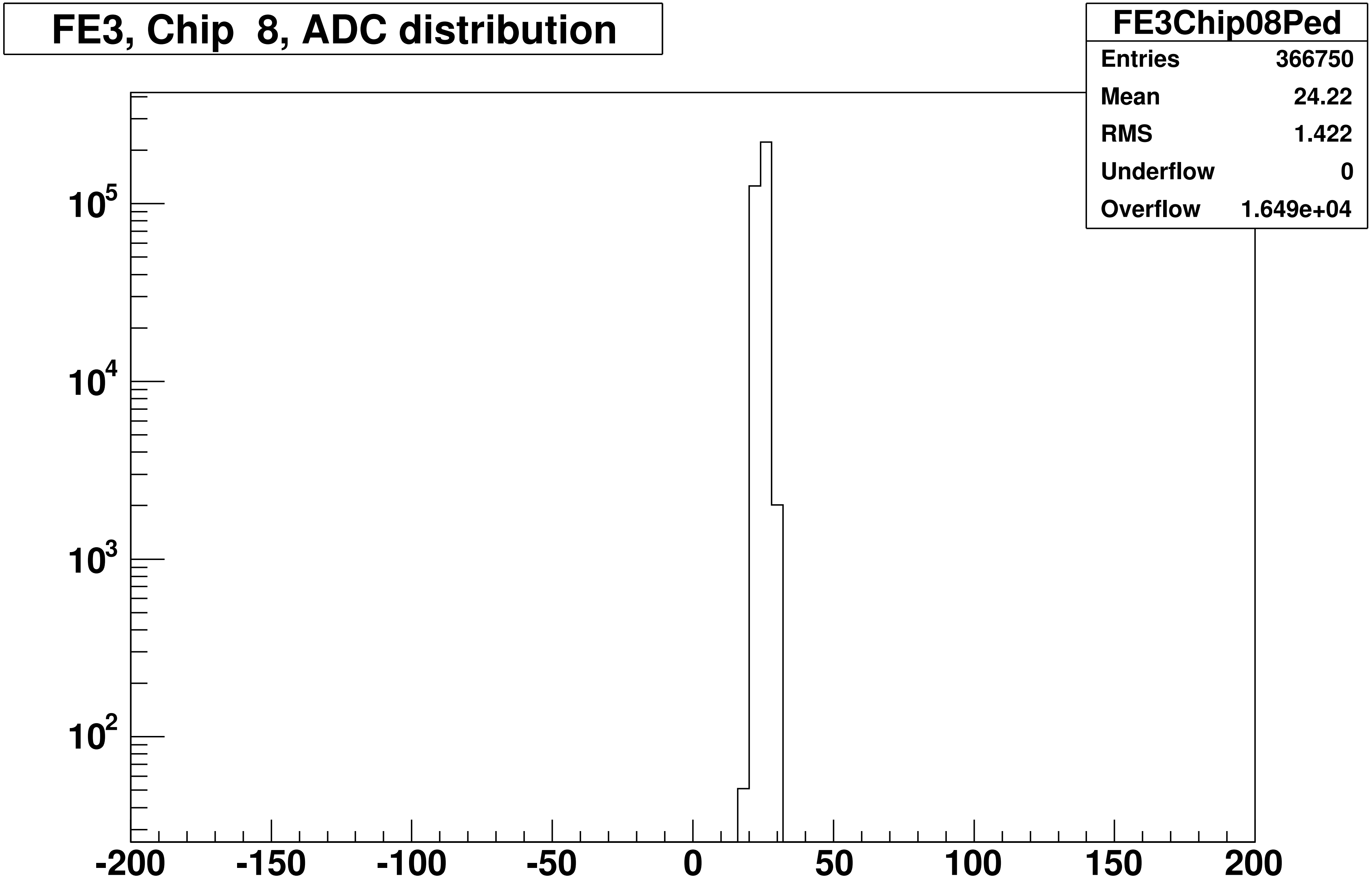
10^2
10^3
10000
10500
11000
11500
12000
12500
13000
13500
14000



FE3, Chip 8, ADC distribution
FE3Chip08All
Entries 366750
Mean 567.1
RMS 2515
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000


FE3, Chip 8, ADC distribution
FE3Chip08Ped
Entries 366750
Mean 24.22
RMS 1.422
Underflow 0
Overflow 1.649e+04
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10^4
10^3
10^2
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-150
-100
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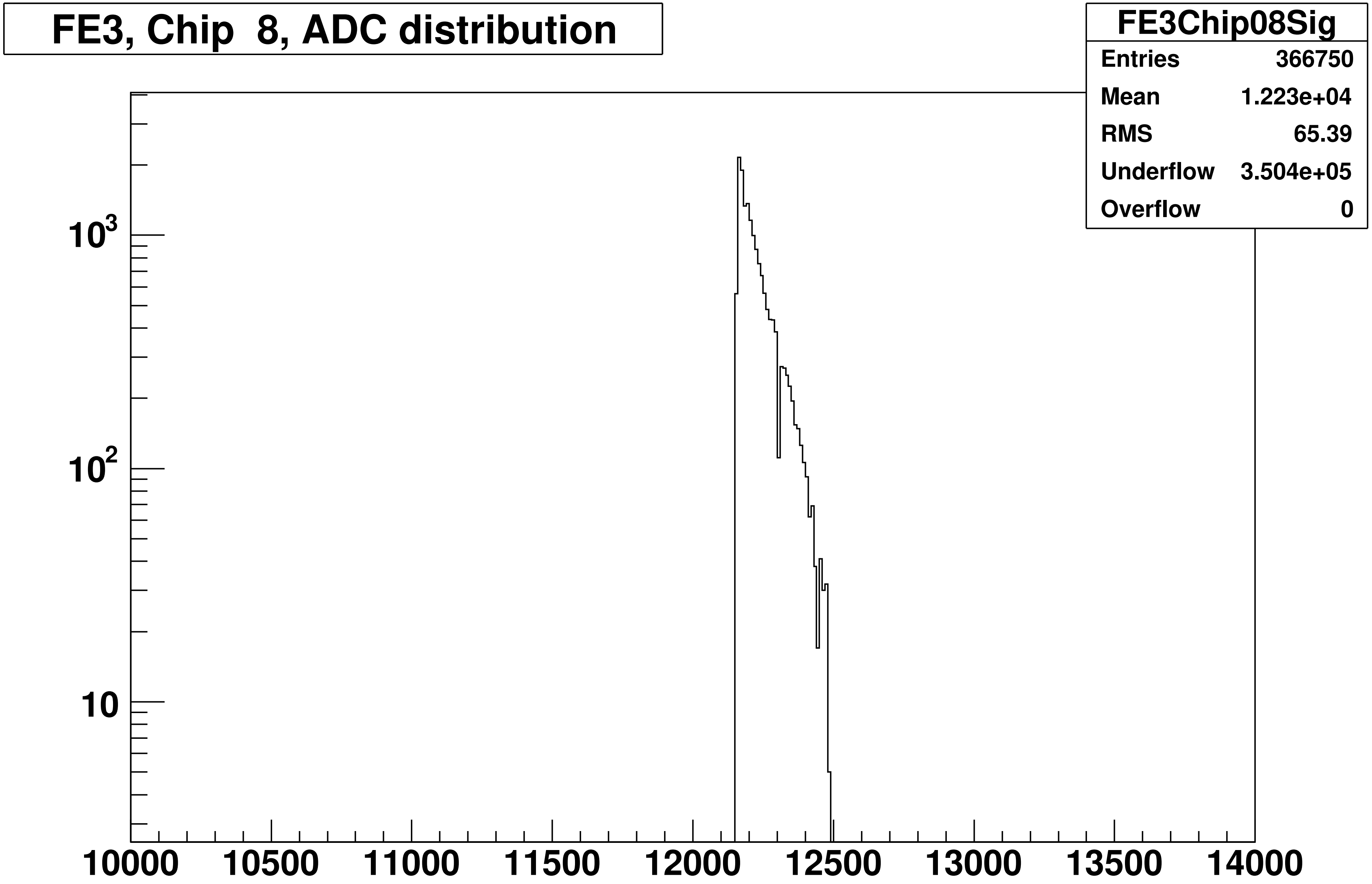
100
150
200


FE3, Chip 8, ADC distribution
FE3Chip08Sig
Entries 366750
Mean 1.223e+04
RMS 65.39
Underflow 3.504e+05
Overflow 0
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10^2
10
10000
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11500
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13500
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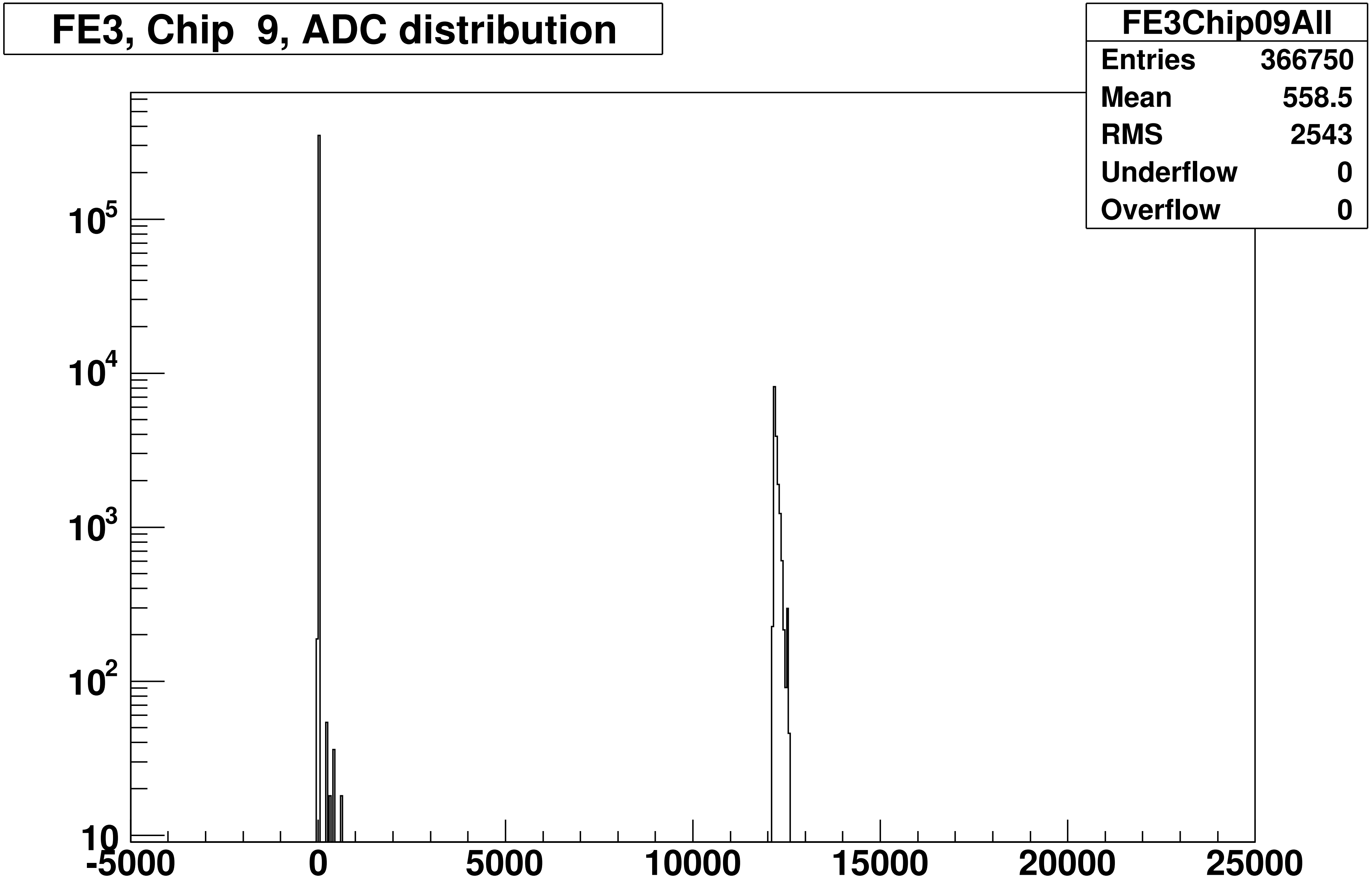
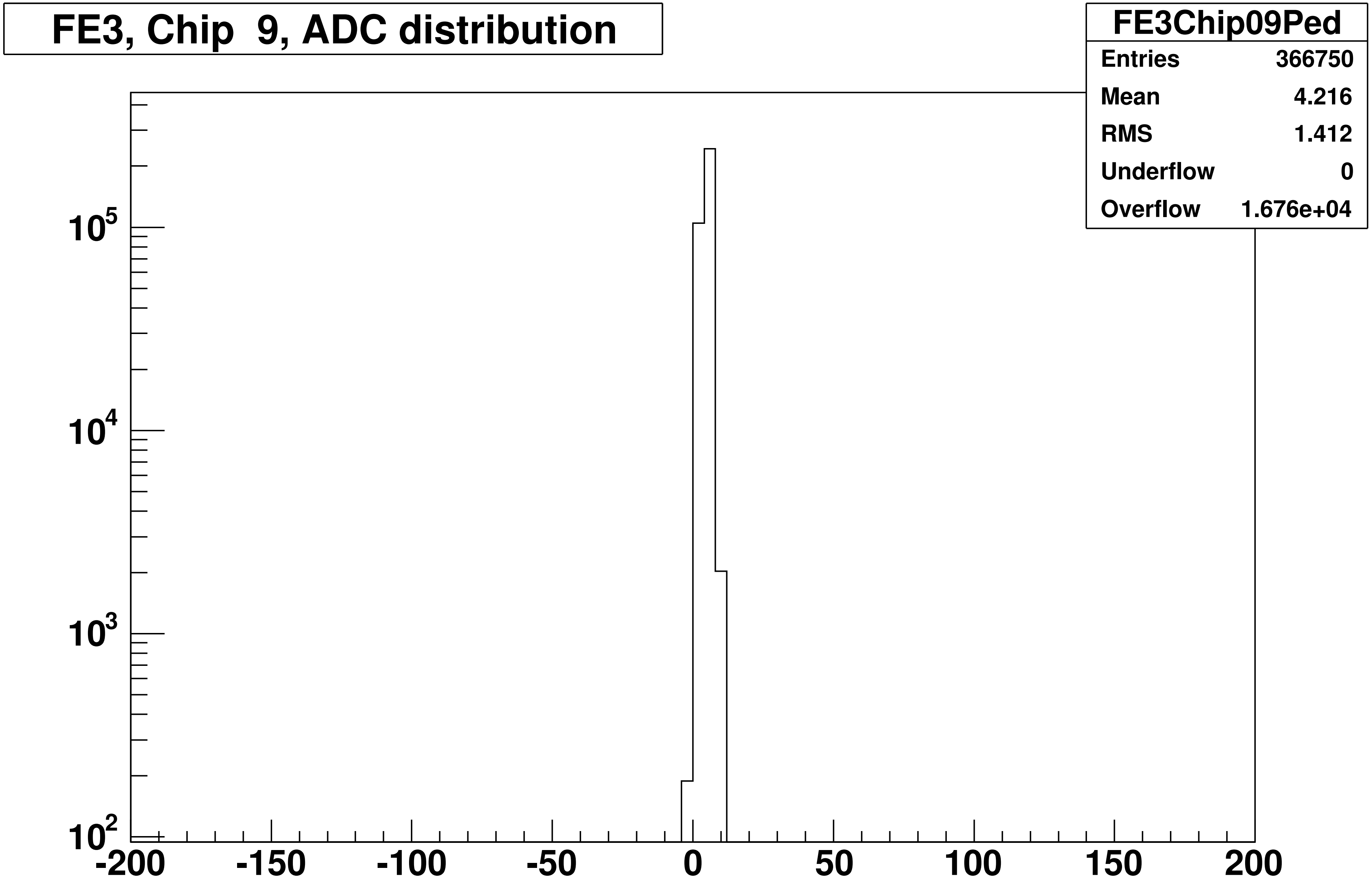
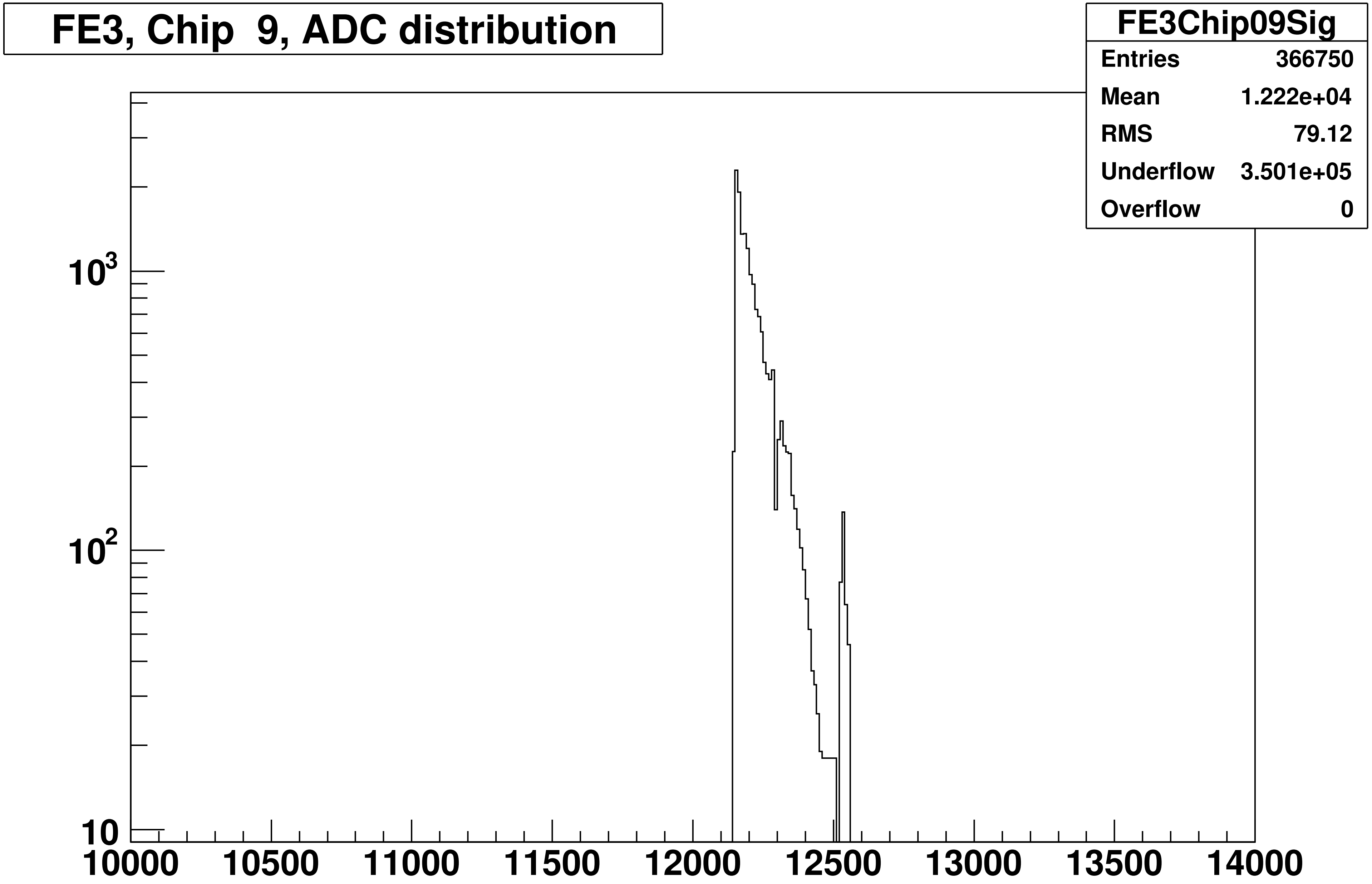
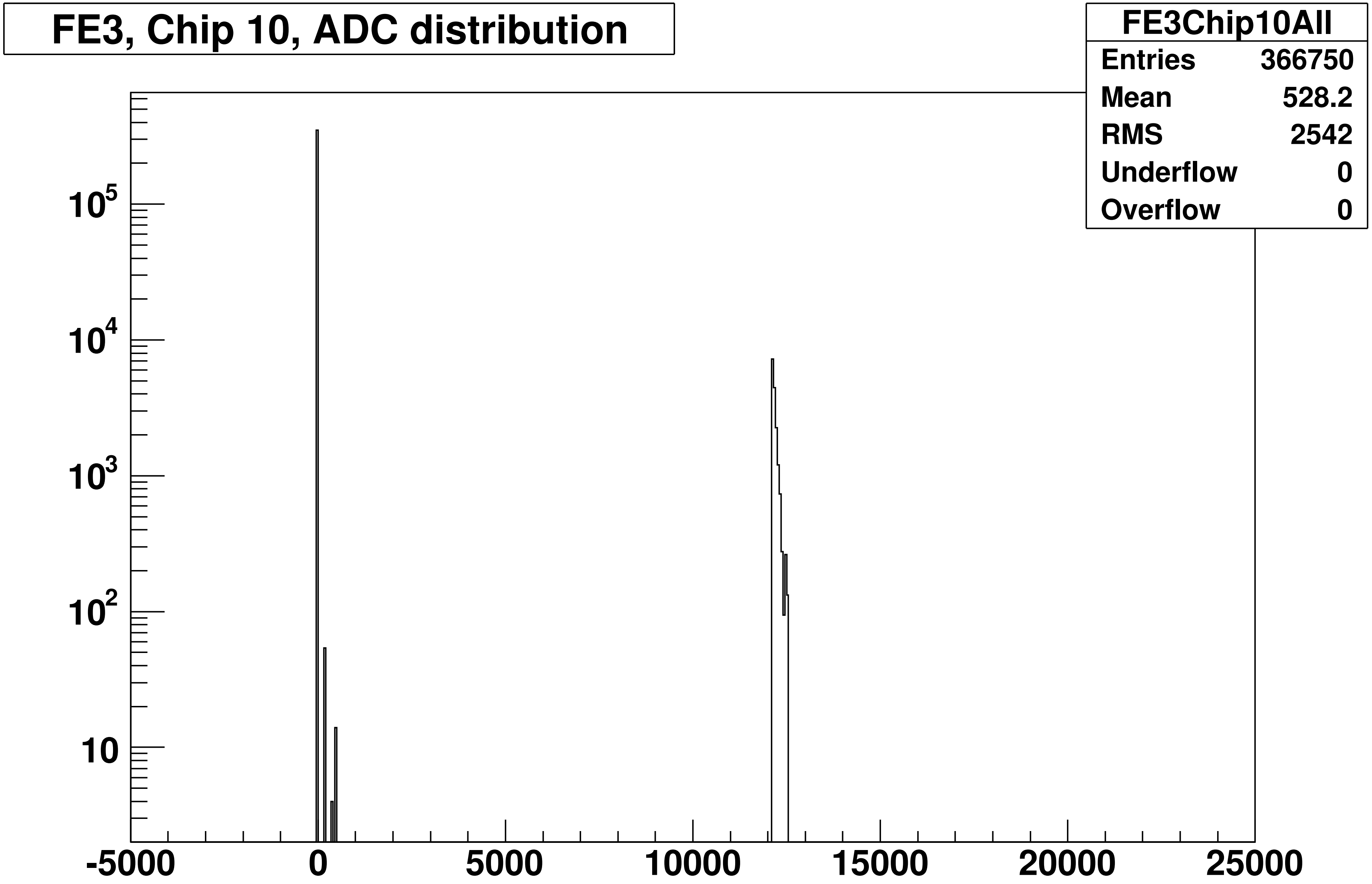
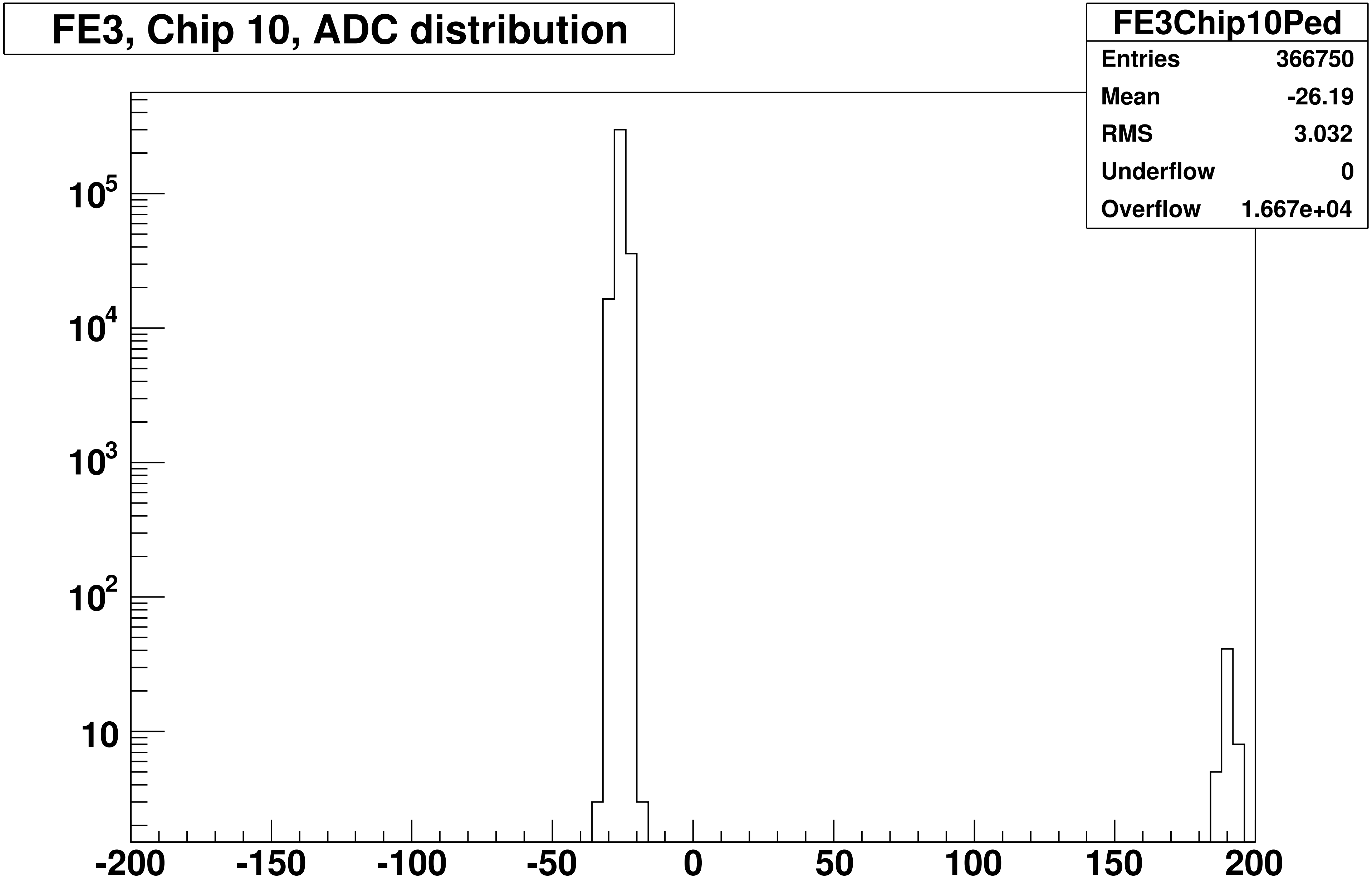

FE3, Chip 9, ADC distribution
FE3Chip09All
Entries 366750
Mean 558.5
RMS 2543
Underflow 0
Overflow 0
10
10^2
10^3
10^4
10^5
-5000
0
5000
10000
15000
20000
25000


FE3, Chip 9, ADC distribution
FE3Chip09Ped
Entries 366750
Mean 4.216
RMS 1.412
Underflow 0
Overflow 1.676e+04
10^5
10^4
10^3
10^2
-200
-150
-100
-50
0
50
100
150
200


FE3, Chip 9, ADC distribution
FE3Chip09Sig
Entries 366750
Mean 1.222e+04
RMS 79.12
Underflow 3.501e+05
Overflow 0
10
10^2
10^3
10000
10500
11000
11500
12000
12500
13000
13500
14000


FE3, Chip 10, ADC distribution
FE3Chip10All
Entries 366750
Mean 528.2
RMS 2542
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000



FE3, Chip 10, ADC distribution
FE3Chip10Ped
Entries 366750
Mean -26.19
RMS 3.032
Underflow 0
Overflow 1.667e+04
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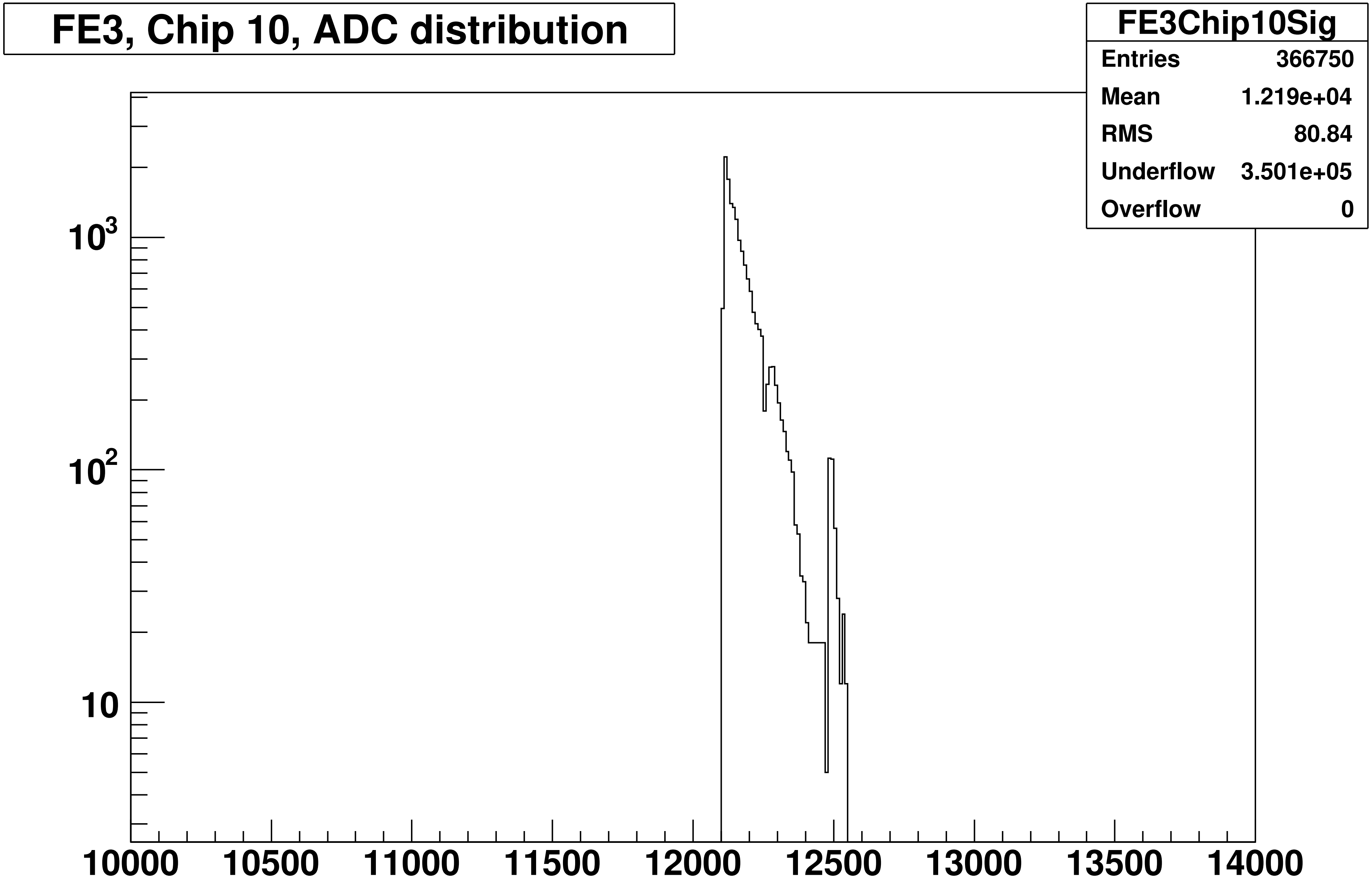
10^4
10^3
10^2
10
-200
-150
-100
-50
0
50
100
150
200



FE3, Chip 10, ADC distribution
FE3Chip10Sig
Entries 366750
Mean 1.219e+04
RMS 80.84
Underflow 3.501e+05
Overflow 0
10^3
10^2
10
10000
10500
11000
11500
12000
12500
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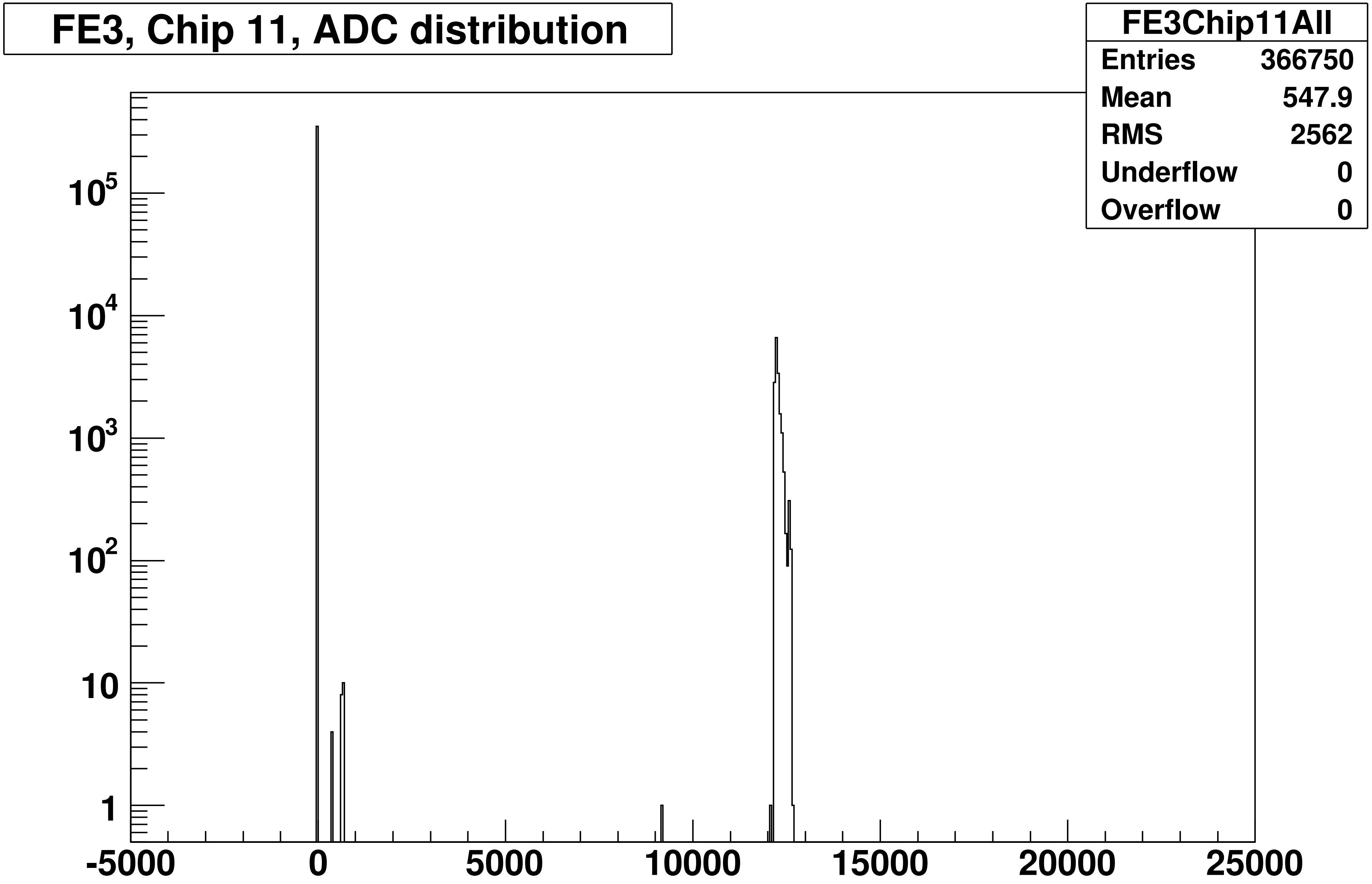
14000


FE3, Chip 11, ADC distribution
FE3Chip11All
Entries 366750
Mean 547.9
RMS 2562
Underflow 0
Overflow 0
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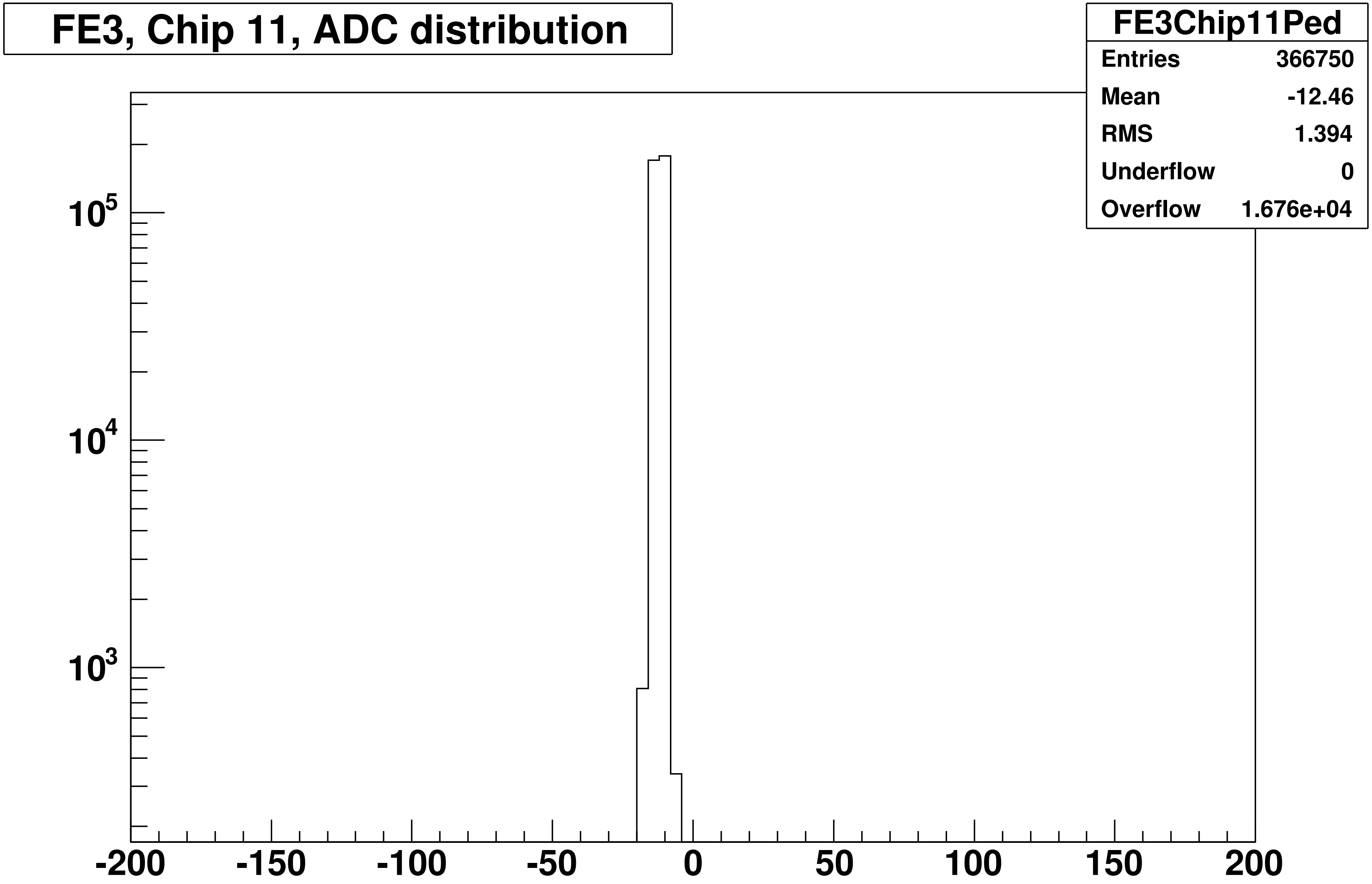
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE3, Chip 11, ADC distribution
FE3Chip11Ped
Entries 366750
Mean -12.46
RMS 1.394
Underflow 0
Overflow 1.676e+04
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10^4
10^3
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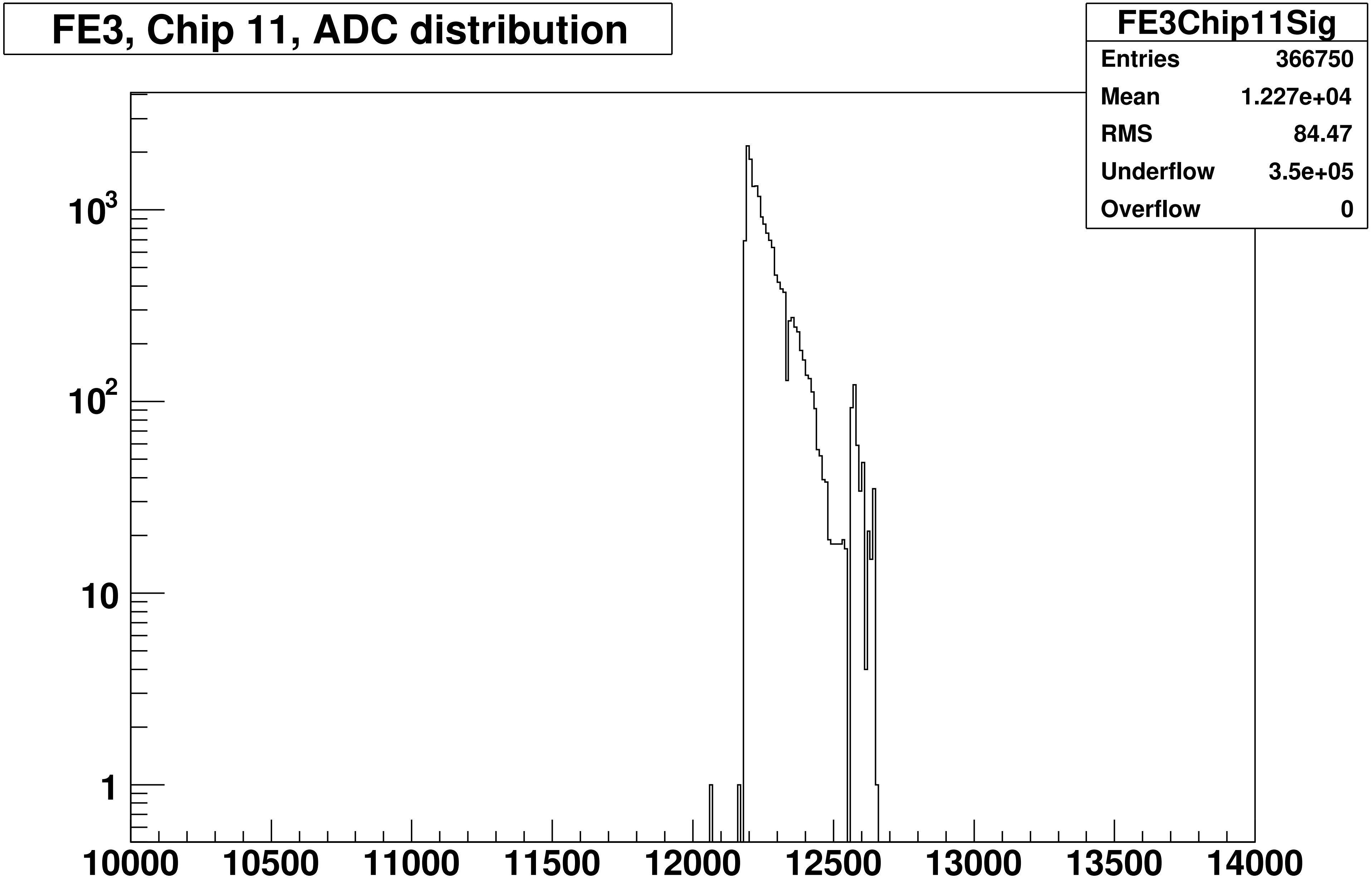
-150
-100
-50
0
50
100
150
200


FE3, Chip 11, ADC distribution
FE3Chip11Sig
Entries 366750
Mean 1.227e+04
RMS 84.47
Underflow 3.5e+05
Overflow 0
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10^2
10
1
10000
10500
11000
11500
12000
12500
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13500
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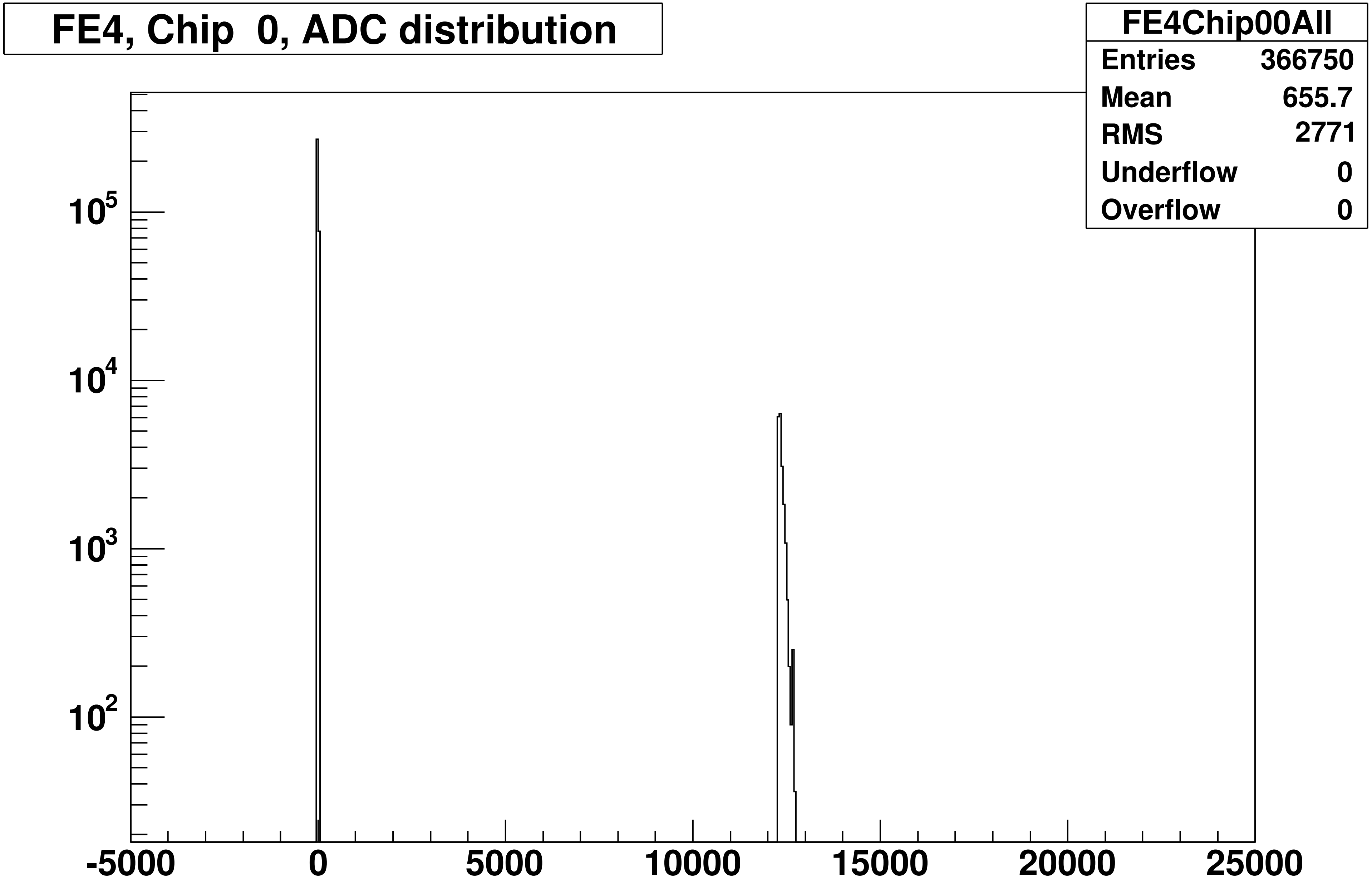
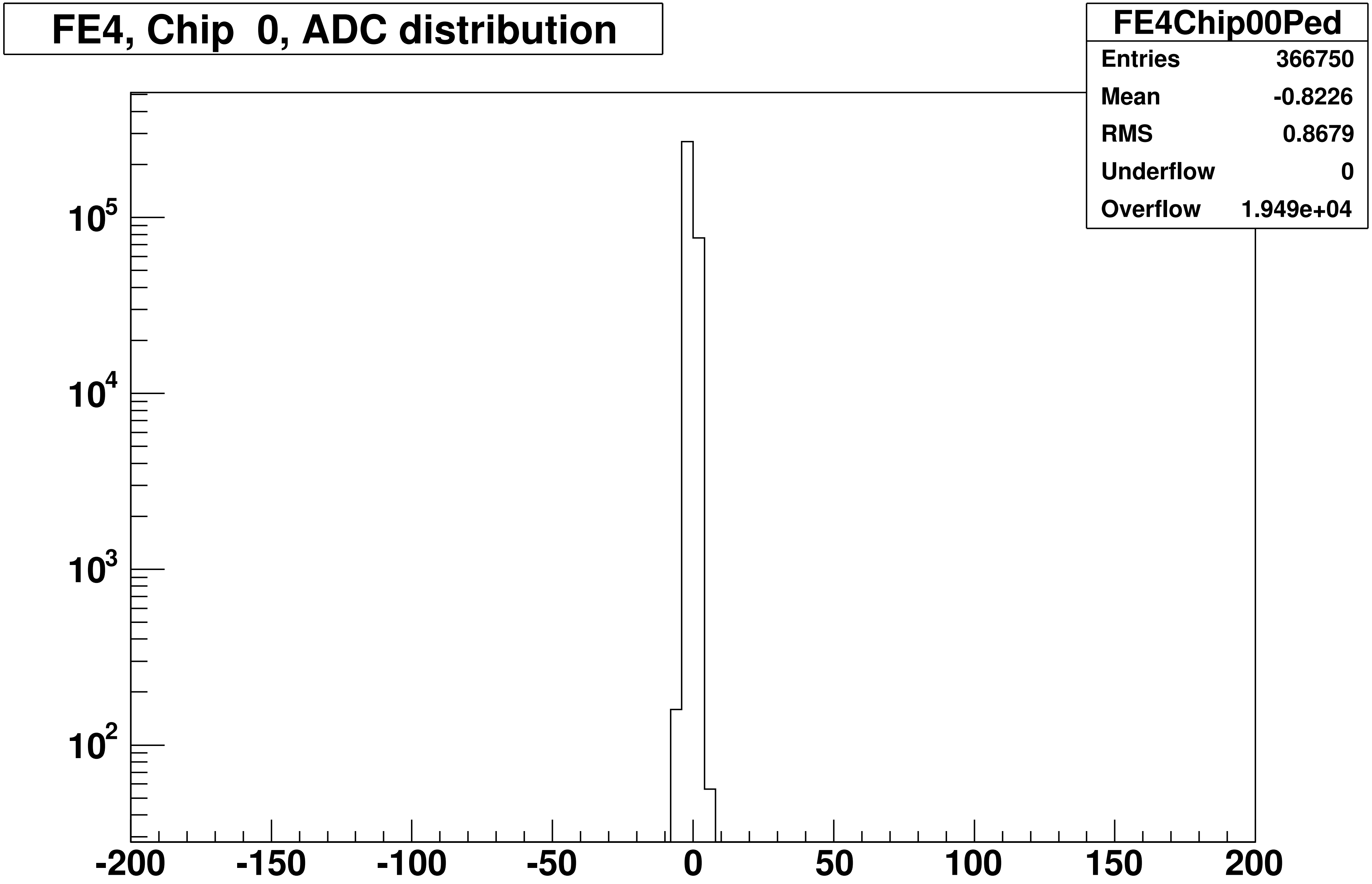

FE4, Chip 0, ADC distribution
FE4Chip00All
Entries 366750
Mean 655.7
RMS 2771
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000



FE4, Chip 0, ADC distribution
FE4Chip00Ped
Entries 366750
Mean -0.8226
RMS 0.8679
Underflow 0
Overflow 1.949e+04
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10^4
10^3
10^2
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-100
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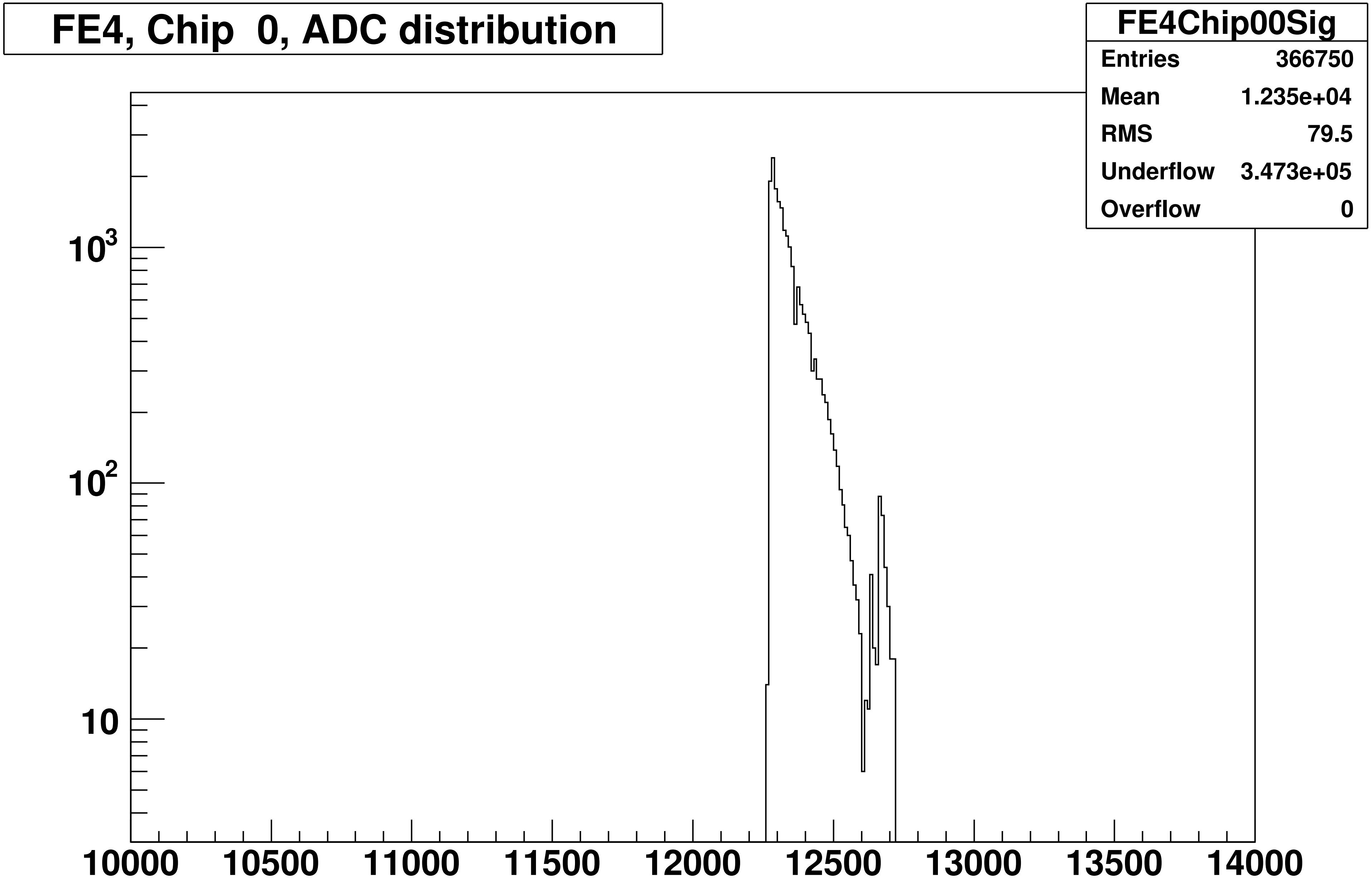
150
200


FE4, Chip 0, ADC distribution
FE4Chip00Sig
Entries 366750
Mean 1.235e+04
RMS 79.5
Underflow 3.473e+05
Overflow 0
10
10^2
10^3
10000
10500
11000
11500
12000
12500
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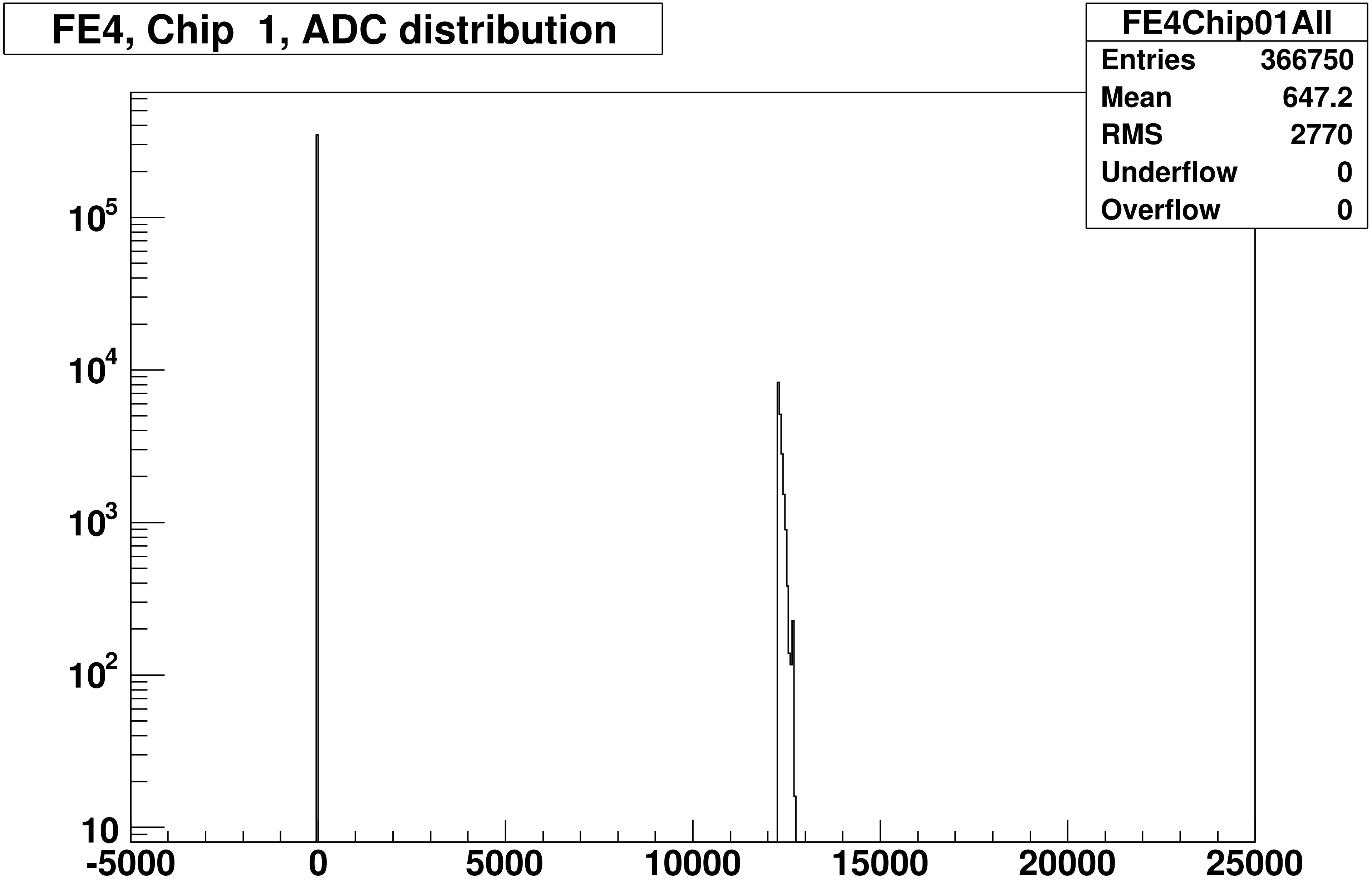
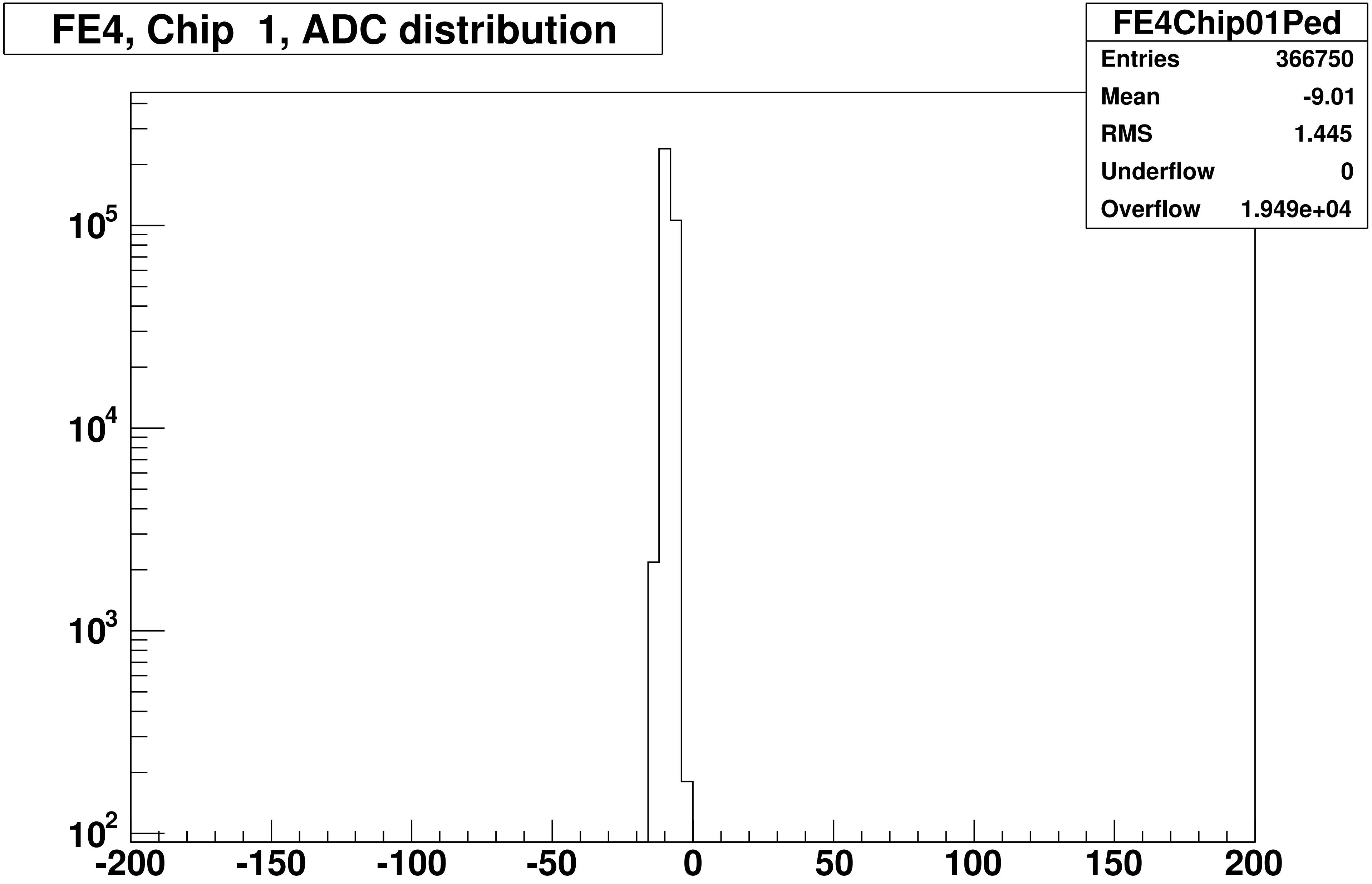
13500
14000


FE4, Chip 1, ADC distribution
FE4Chip01All
Entries 366750
Mean 647.2
RMS 2770
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE4, Chip 1, ADC distribution
FE4Chip01Ped
Entries 366750
Mean -9.01
RMS 1.445
Underflow 0
Overflow 1.949e+04
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10^4
10^3
10^2
-200
-150
-100
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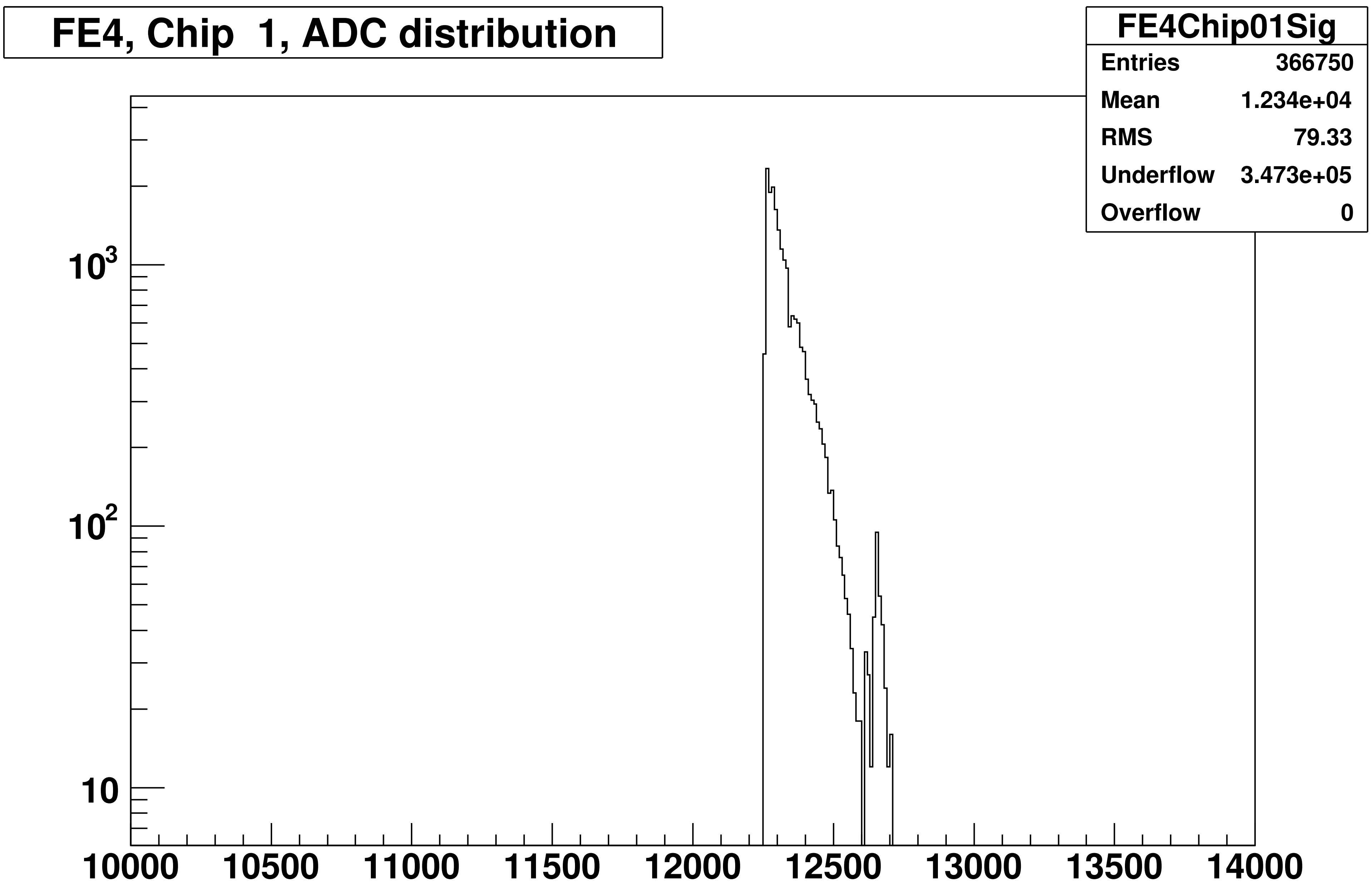
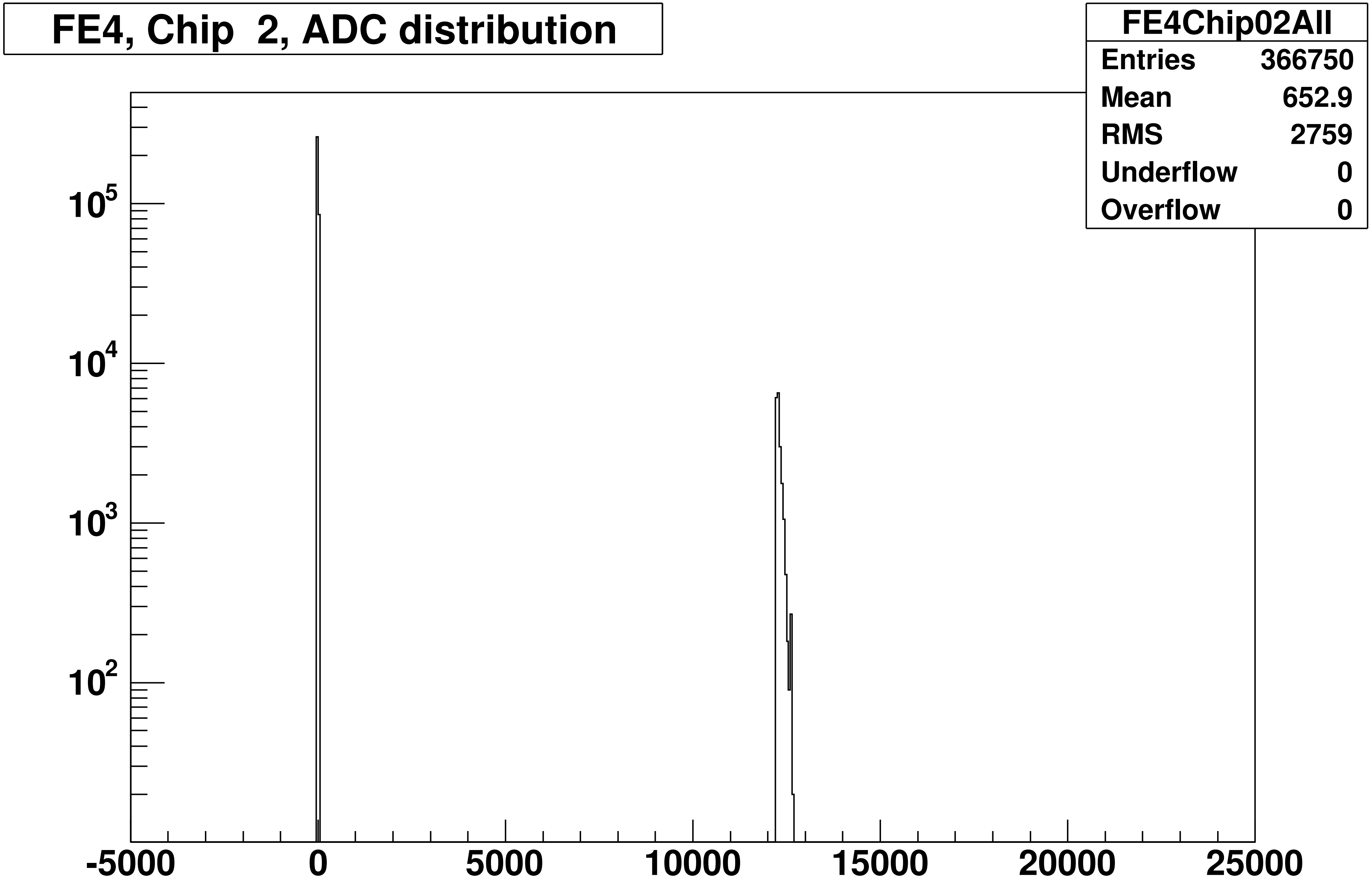
100
150
200



FE4, Chip 1, ADC distribution
FE4Chip01Sig
Entries 366750
Mean 1.234e+04
RMS 79.33
Underflow 3.473e+05
Overflow 0
10³
10²
10
10000
10500
11000
11500
12000
12500
13000
13500
14000



FE4, Chip 2, ADC distribution
FE4Chip02All
Entries 366750
Mean 652.9
RMS 2759
Underflow 0
Overflow 0
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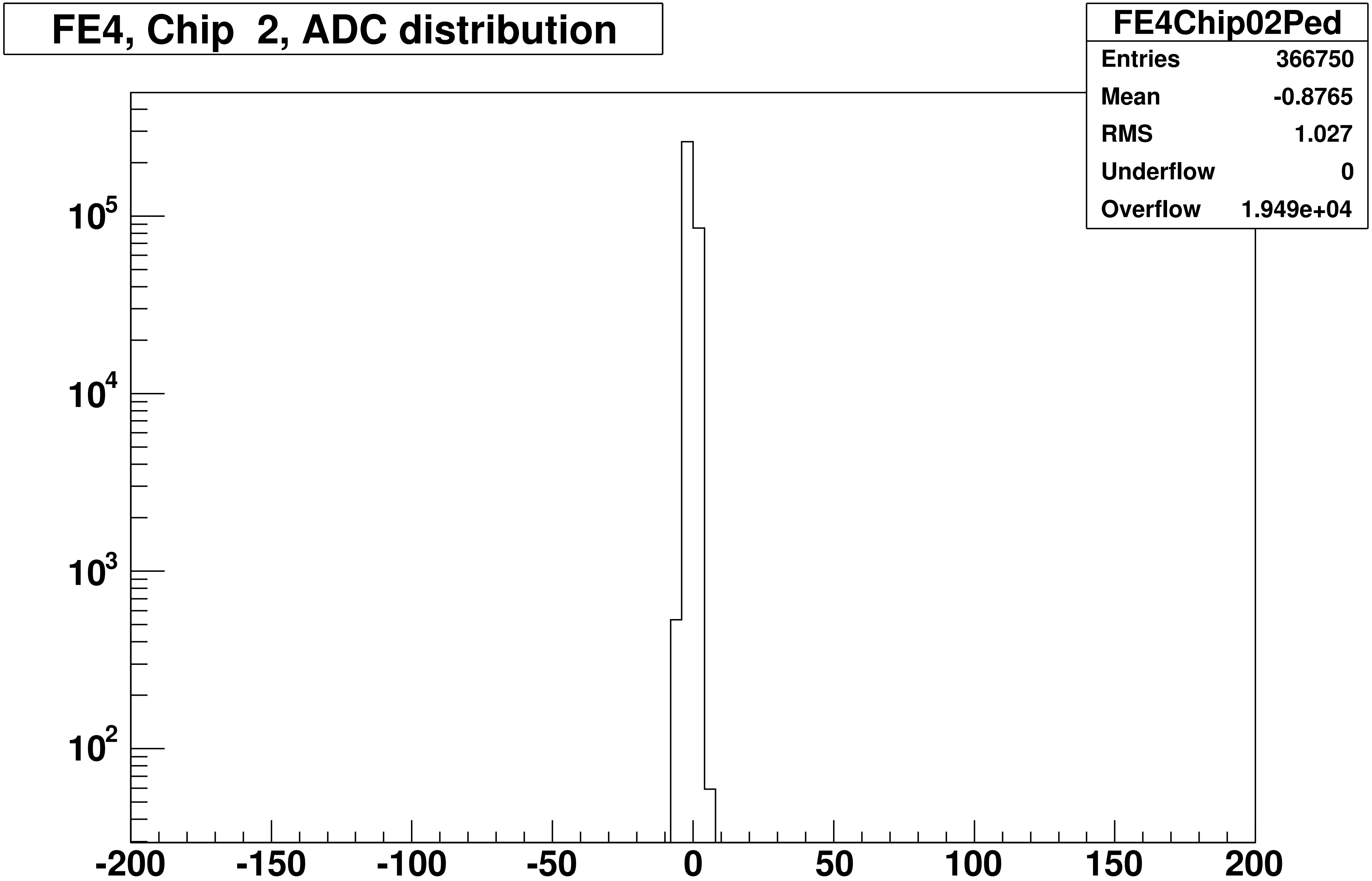
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000



FE4, Chip 2, ADC distribution
FE4Chip02Ped
Entries 366750
Mean -0.8765
RMS 1.027
Underflow 0
Overflow 1.949e+04
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10^4
10^3
10^2
-200
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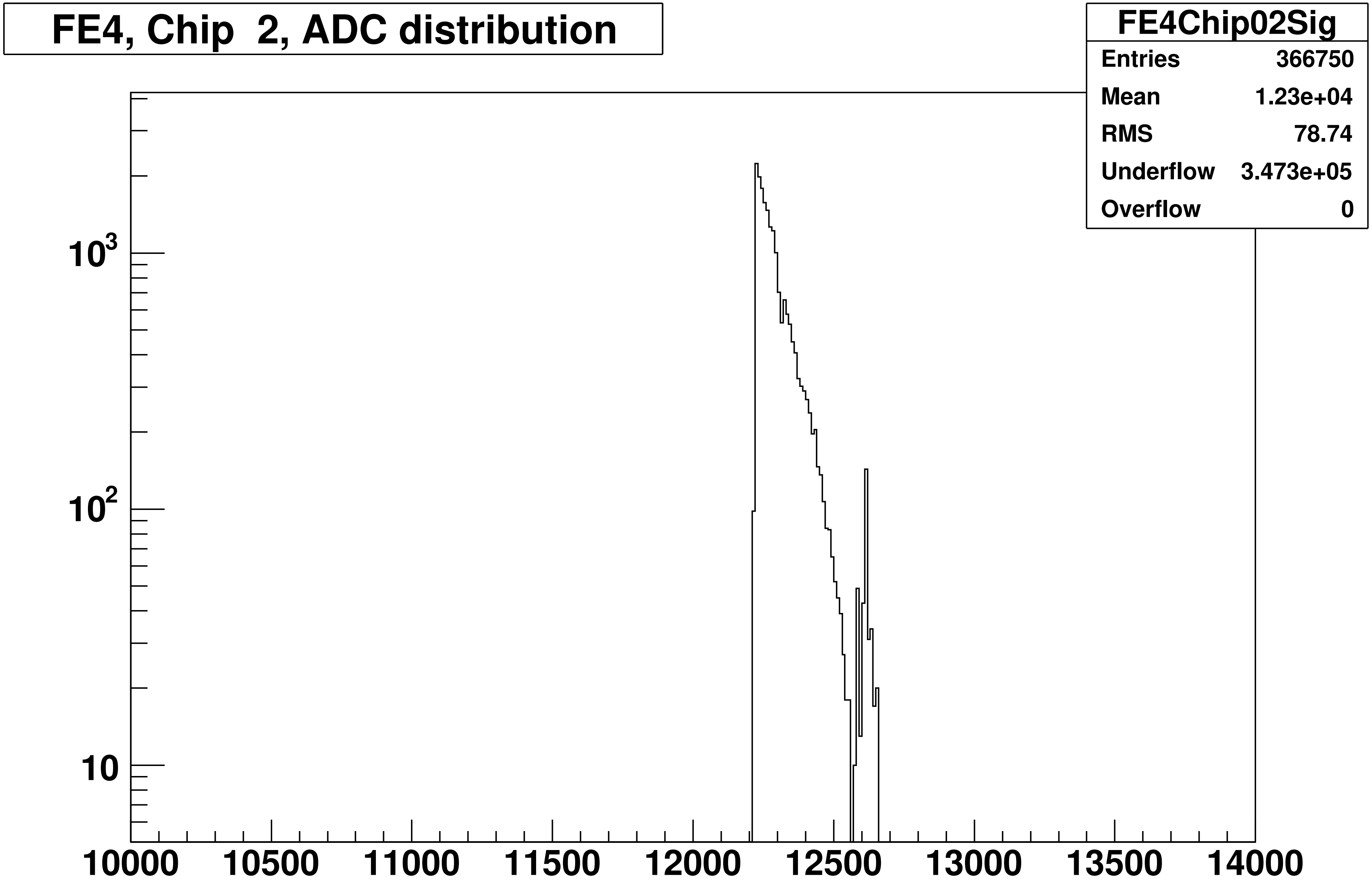
-100
-50
0
50
100
150
200


FE4, Chip 2, ADC distribution
FE4Chip02Sig
Entries 366750
Mean 1.23e+04
RMS 78.74
Underflow 3.473e+05
Overflow 0
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10^2
10
10000
10500
11000
11500
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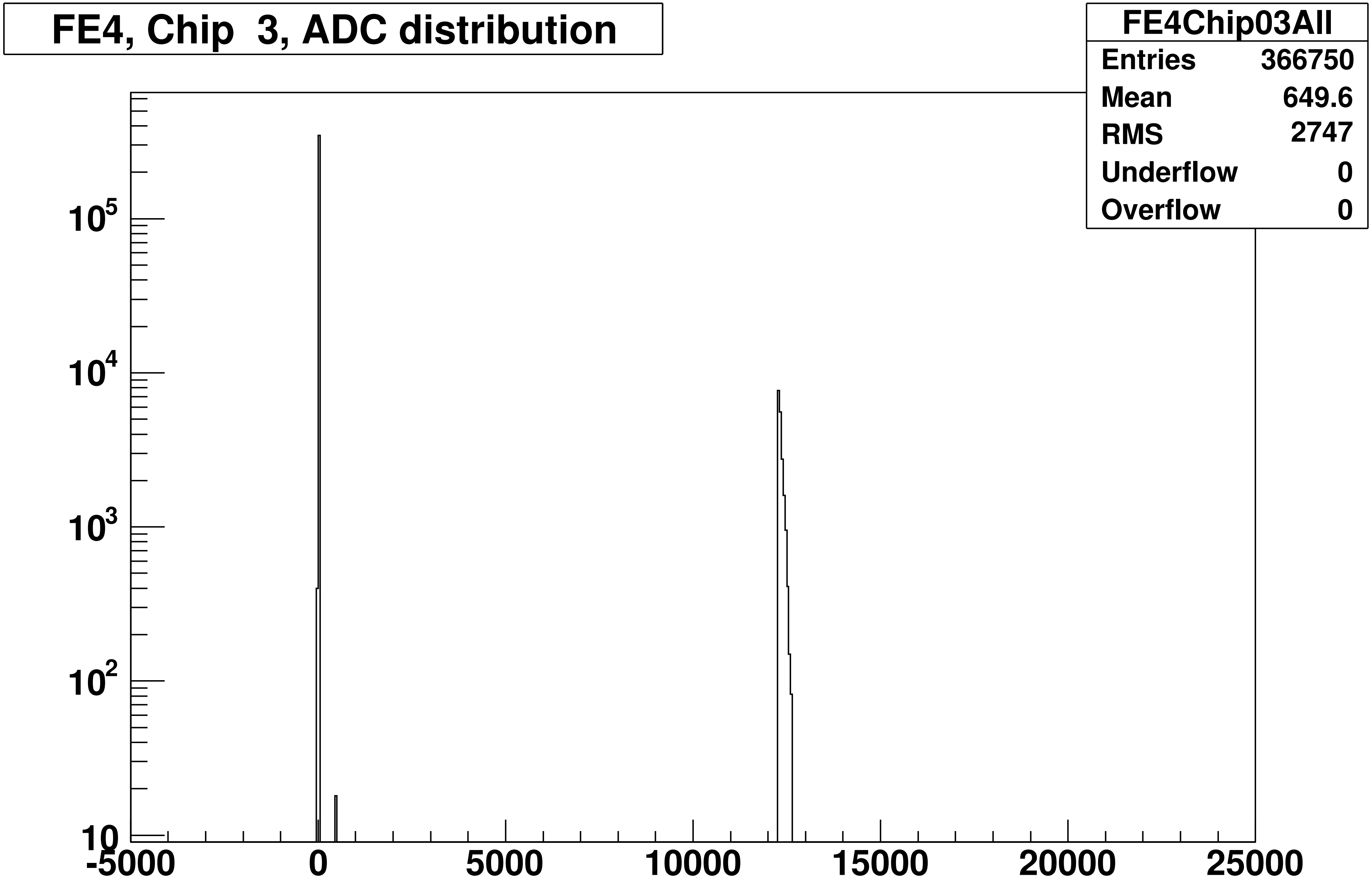
14000


FE4, Chip 3, ADC distribution
FE4Chip03All
Entries 366750
Mean 649.6
RMS 2747
Underflow 0
Overflow 0
10
10^2
10^3
10^4
10^5
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0
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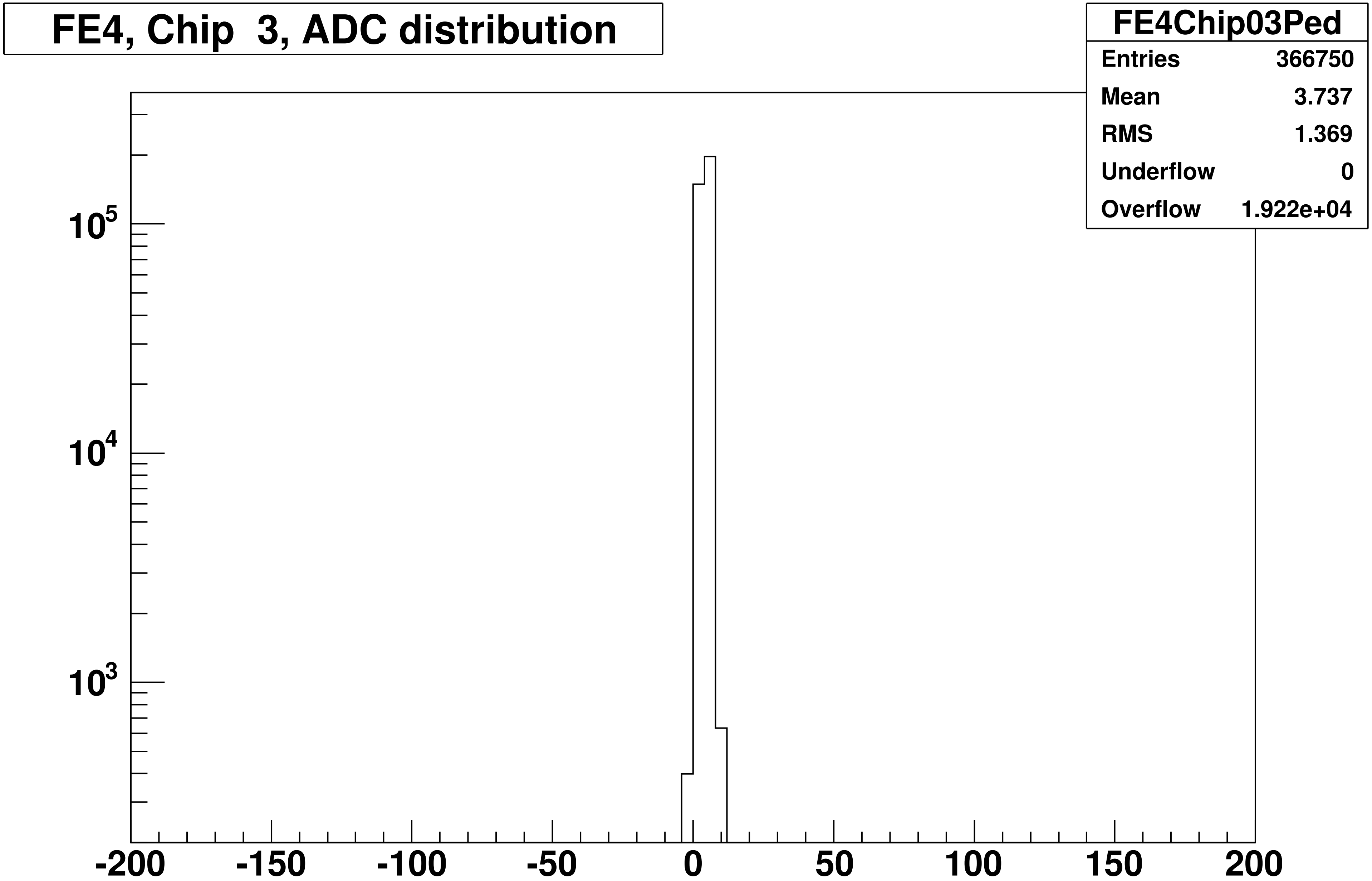
25000


FE4, Chip 3, ADC distribution
FE4Chip03Ped
Entries 366750
Mean 3.737
RMS 1.369
Underflow 0
Overflow 1.922e+04
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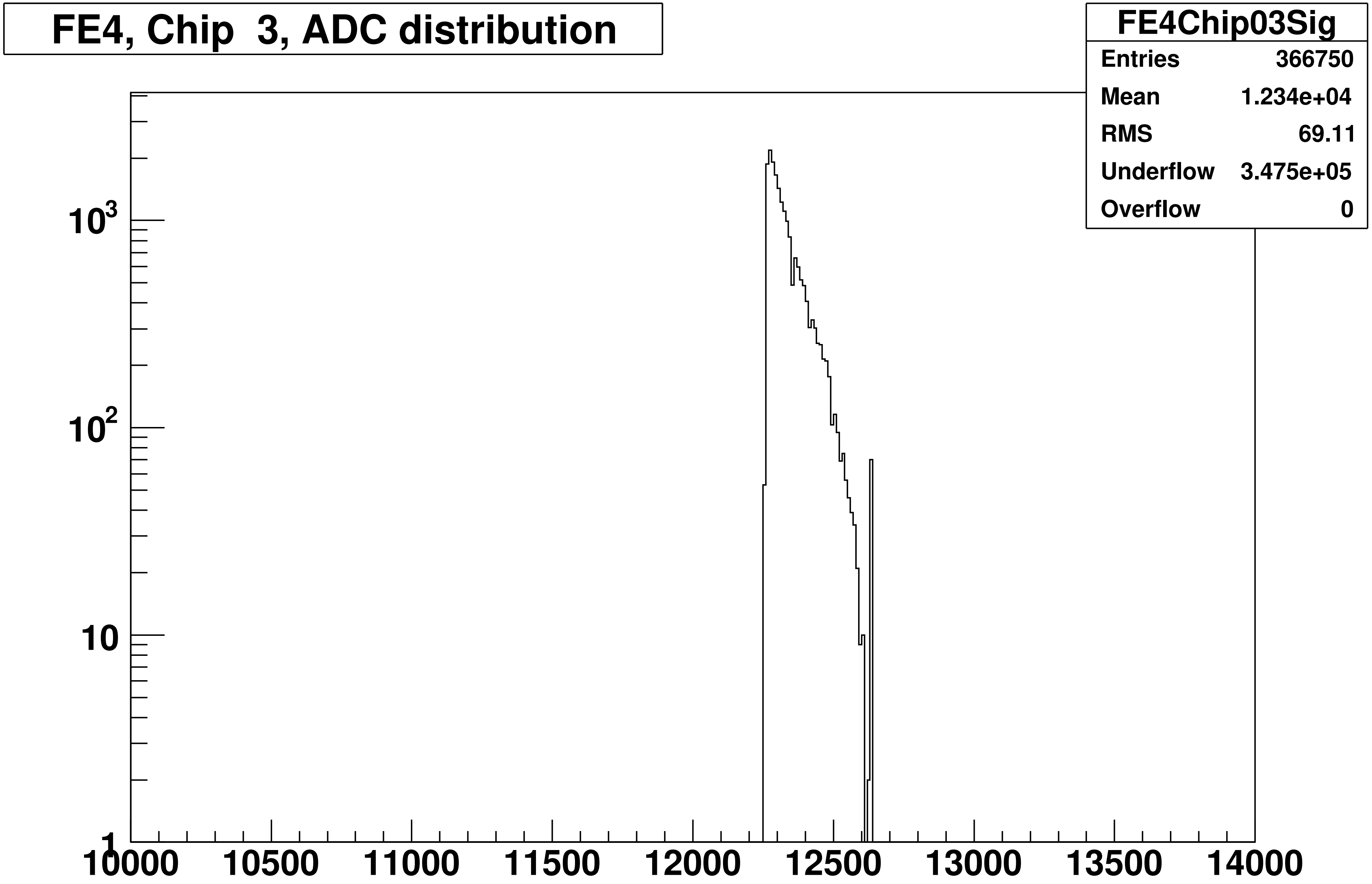
10^4
10^3
-200
-150
-100
-50
0
50
100
150
200



FE4, Chip 3, ADC distribution
FE4Chip03Sig
Entries 366750
Mean 1.234e+04
RMS 69.11
Underflow 3.475e+05
Overflow 0
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10^2
10
1
10000
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11000
11500
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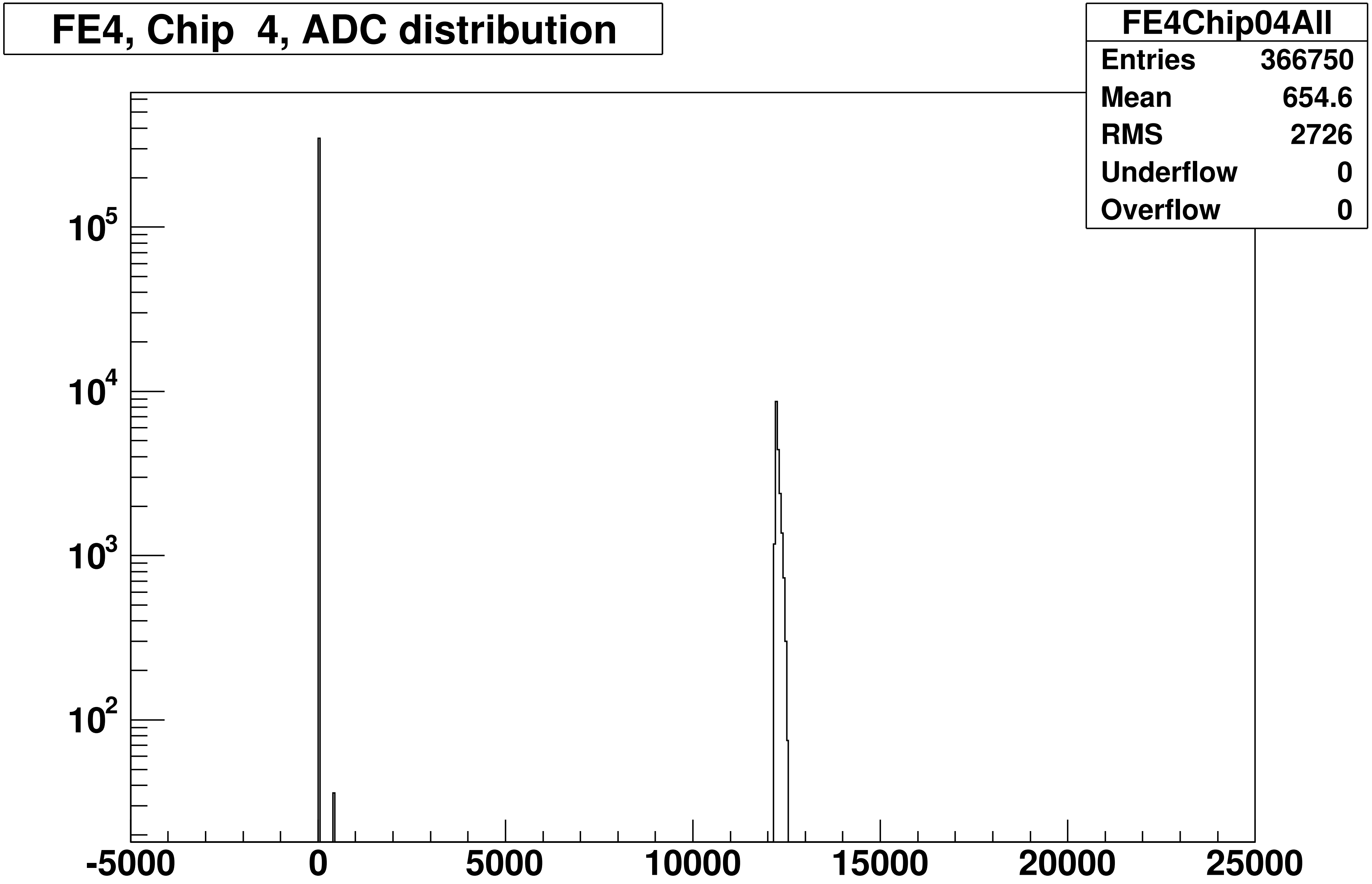
14000


FE4, Chip 4, ADC distribution
FE4Chip04All
Entries 366750
Mean 654.6
RMS 2726
Underflow 0
Overflow 0
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10^4
10^3
10^2
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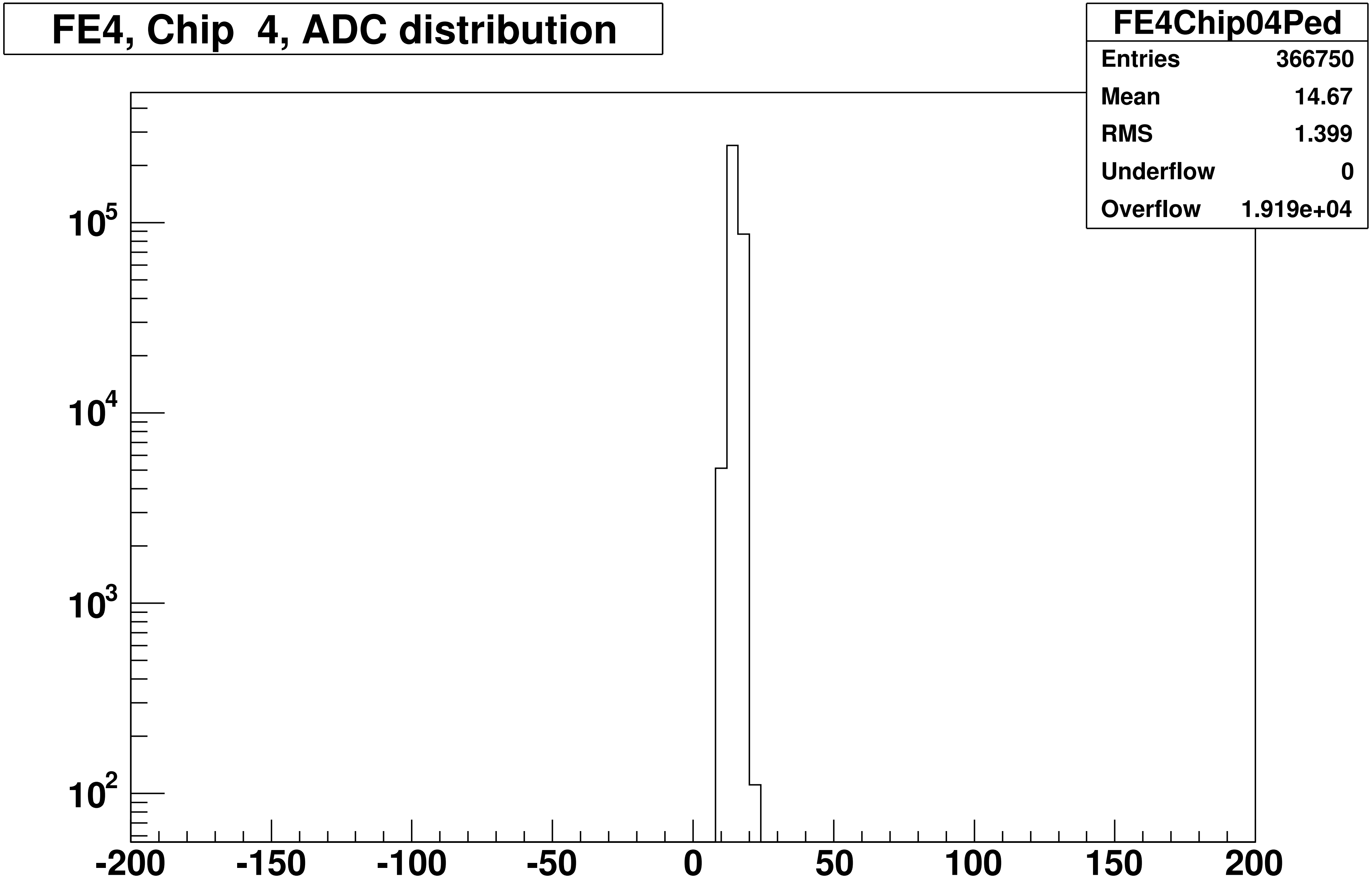
25000


FE4, Chip 4, ADC distribution
FE4Chip04Ped
Entries 366750
Mean 14.67
RMS 1.399
Underflow 0
Overflow 1.919e+04
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10^4
10^3
10^2
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-100
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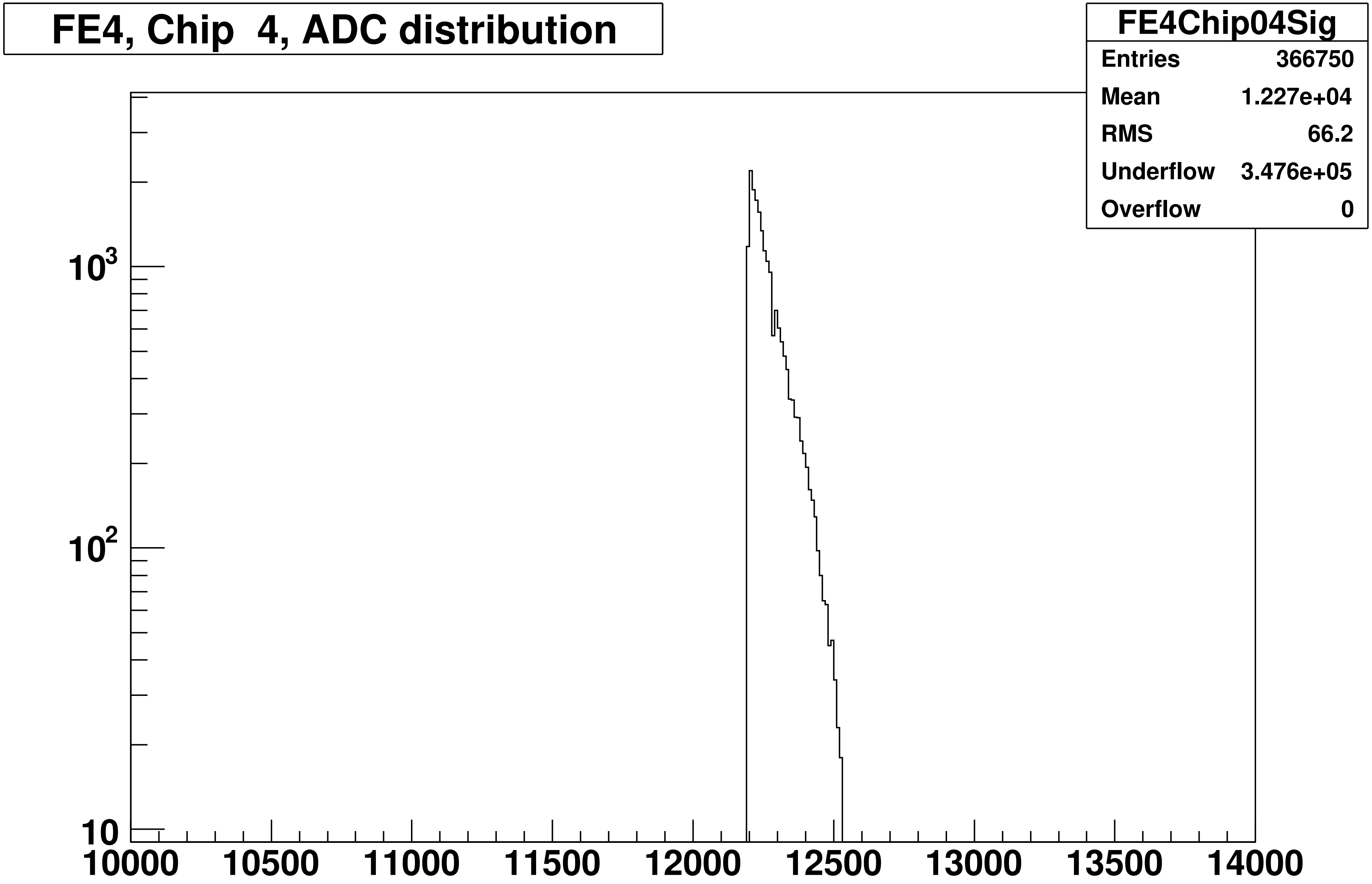
0
50
100
150
200



FE4, Chip 4, ADC distribution
FE4Chip04Sig
Entries 366750
Mean 1.227e+04
RMS 66.2
Underflow 3.476e+05
Overflow 0
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10^2
10
10000
10500
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11500
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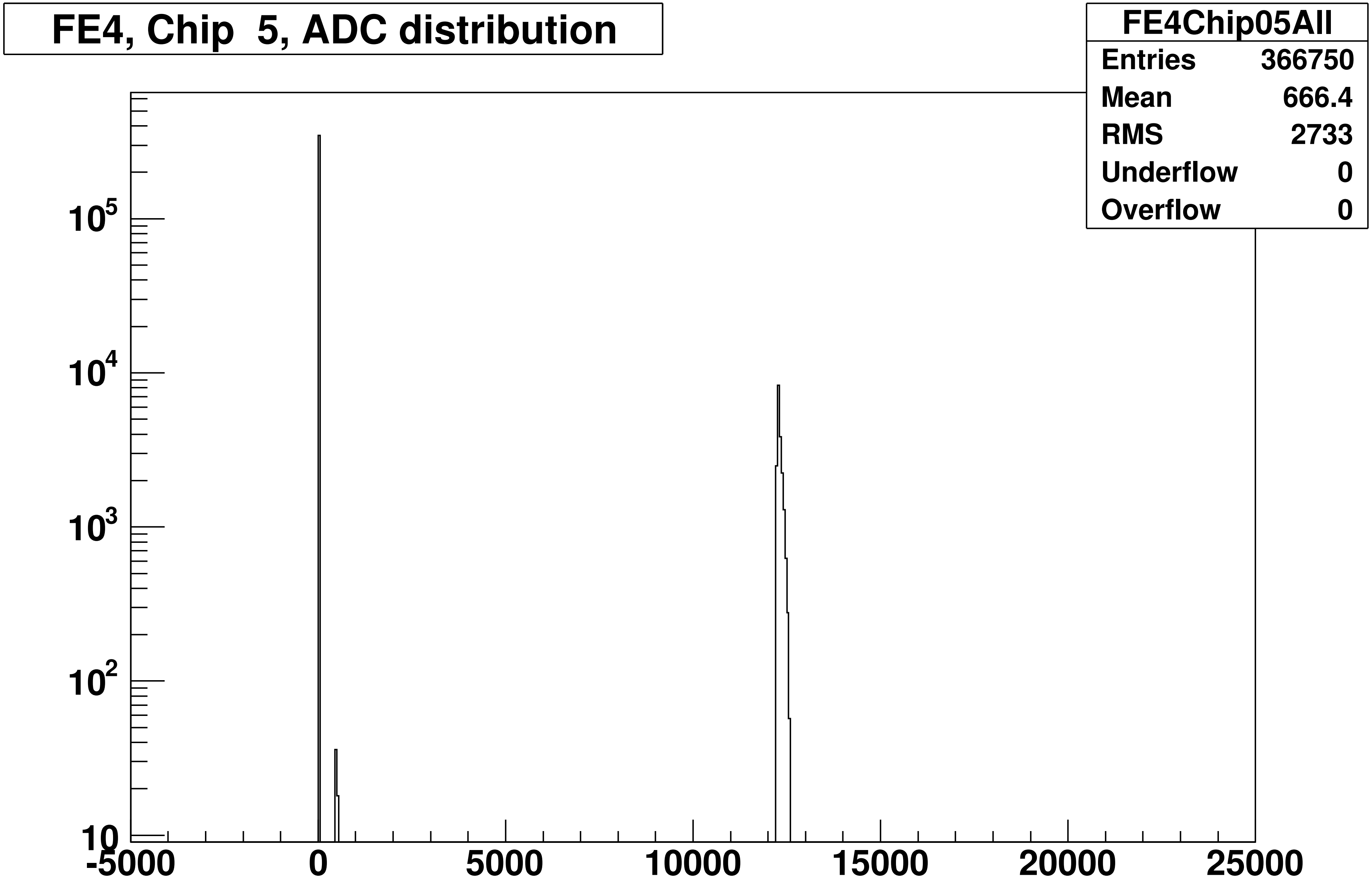

FE4, Chip 5, ADC distribution
FE4Chip05All
Entries 366750
Mean 666.4
RMS 2733
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
-5000
0
5000
10000
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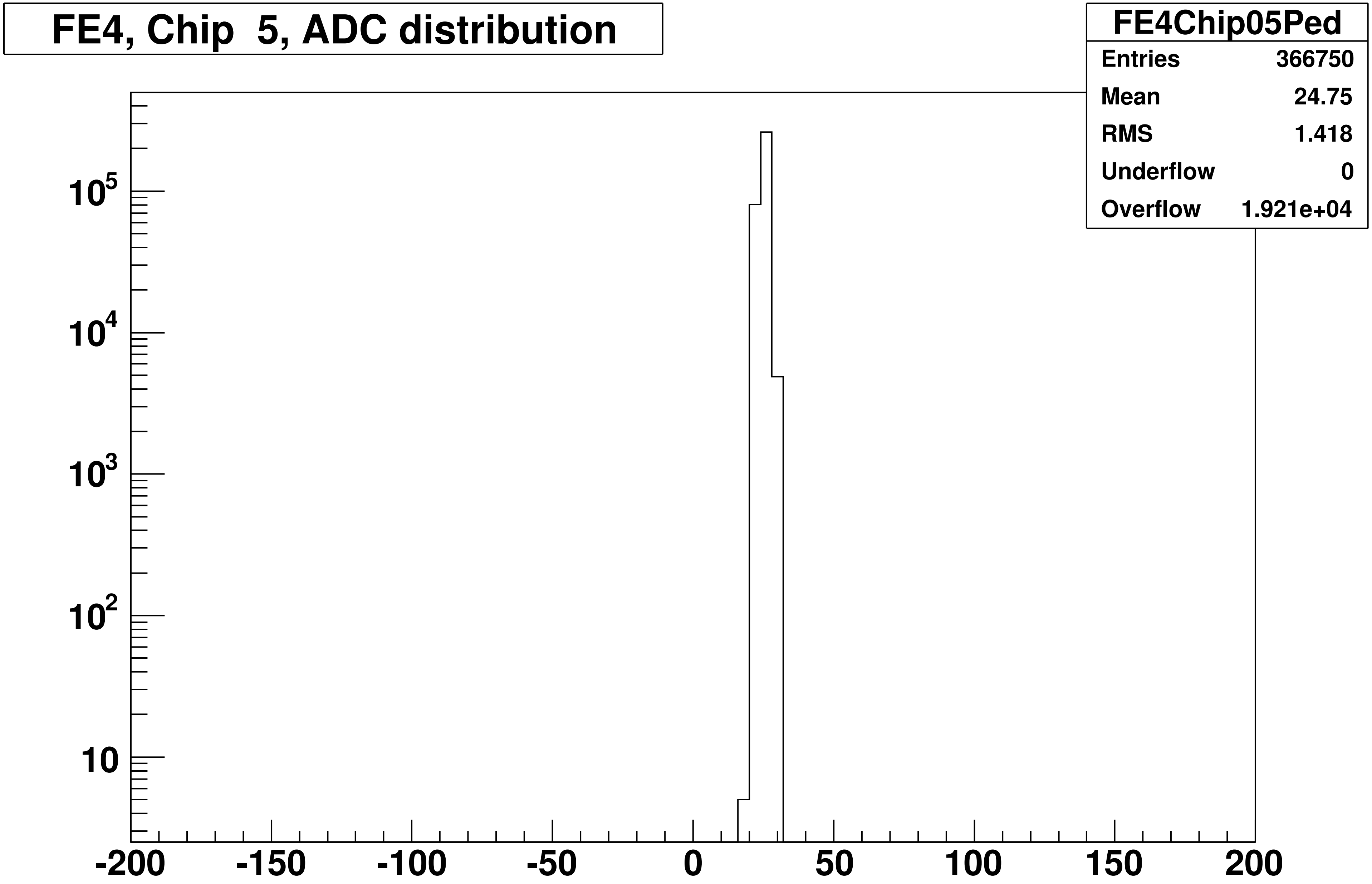
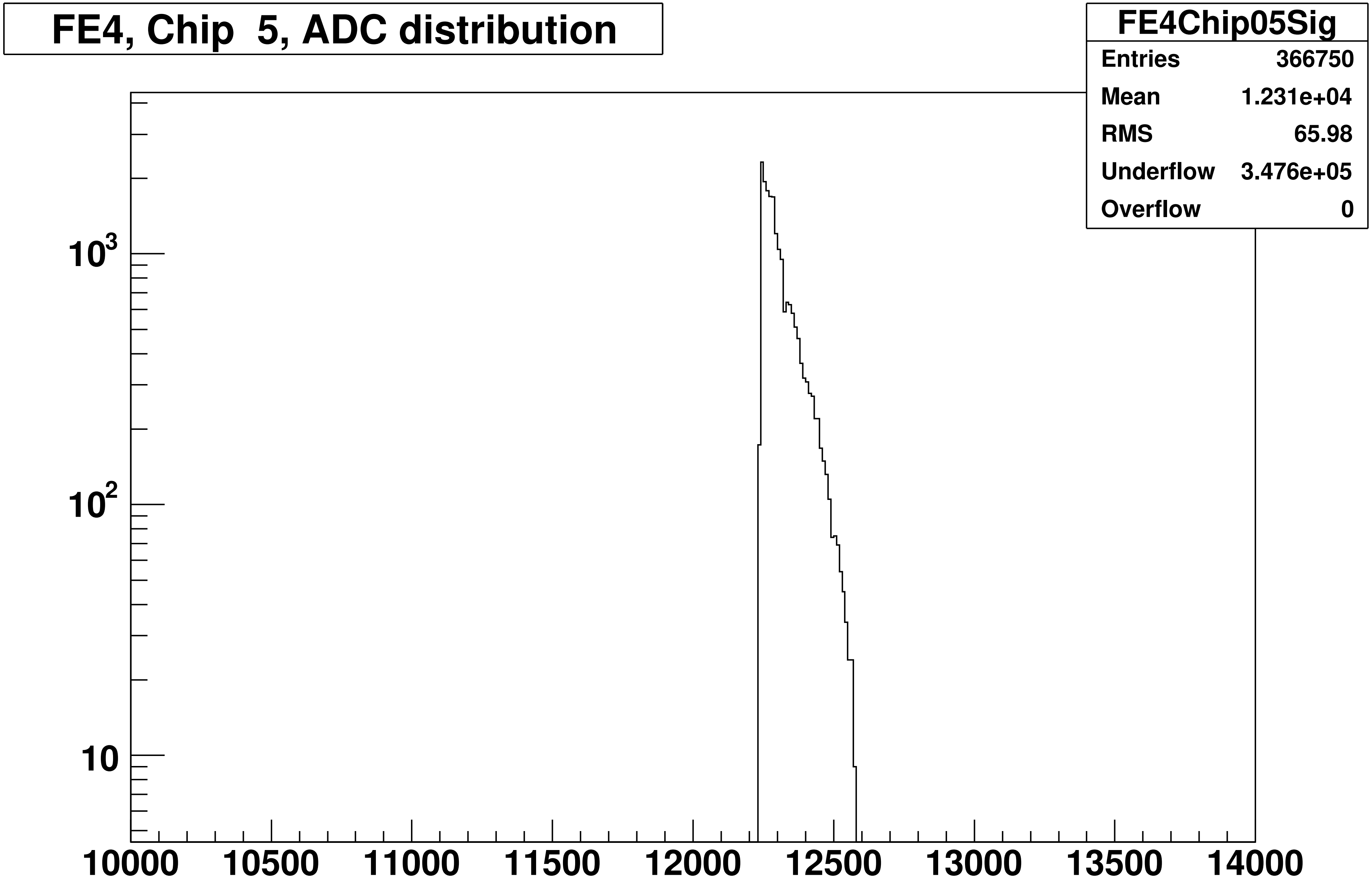
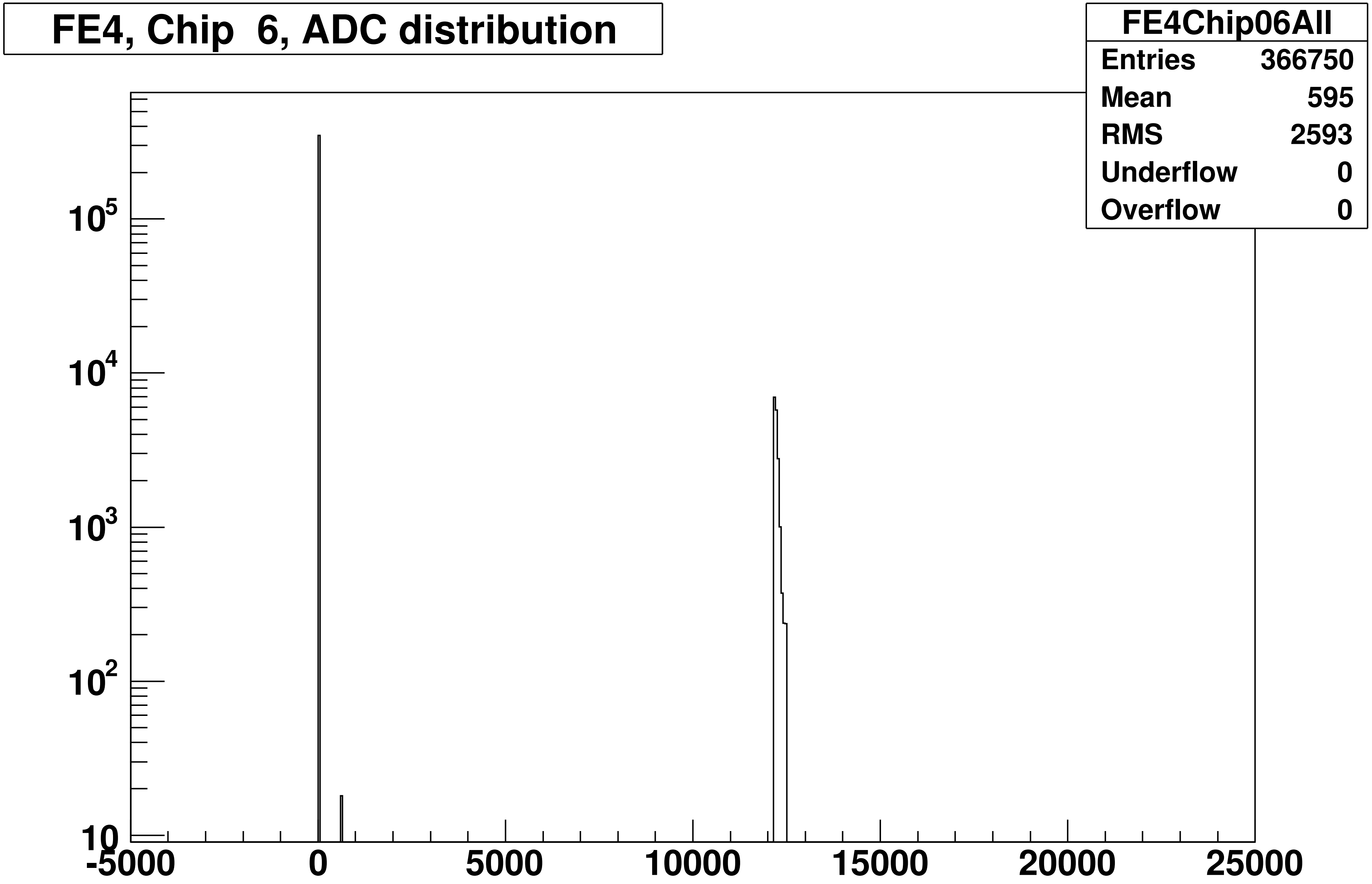
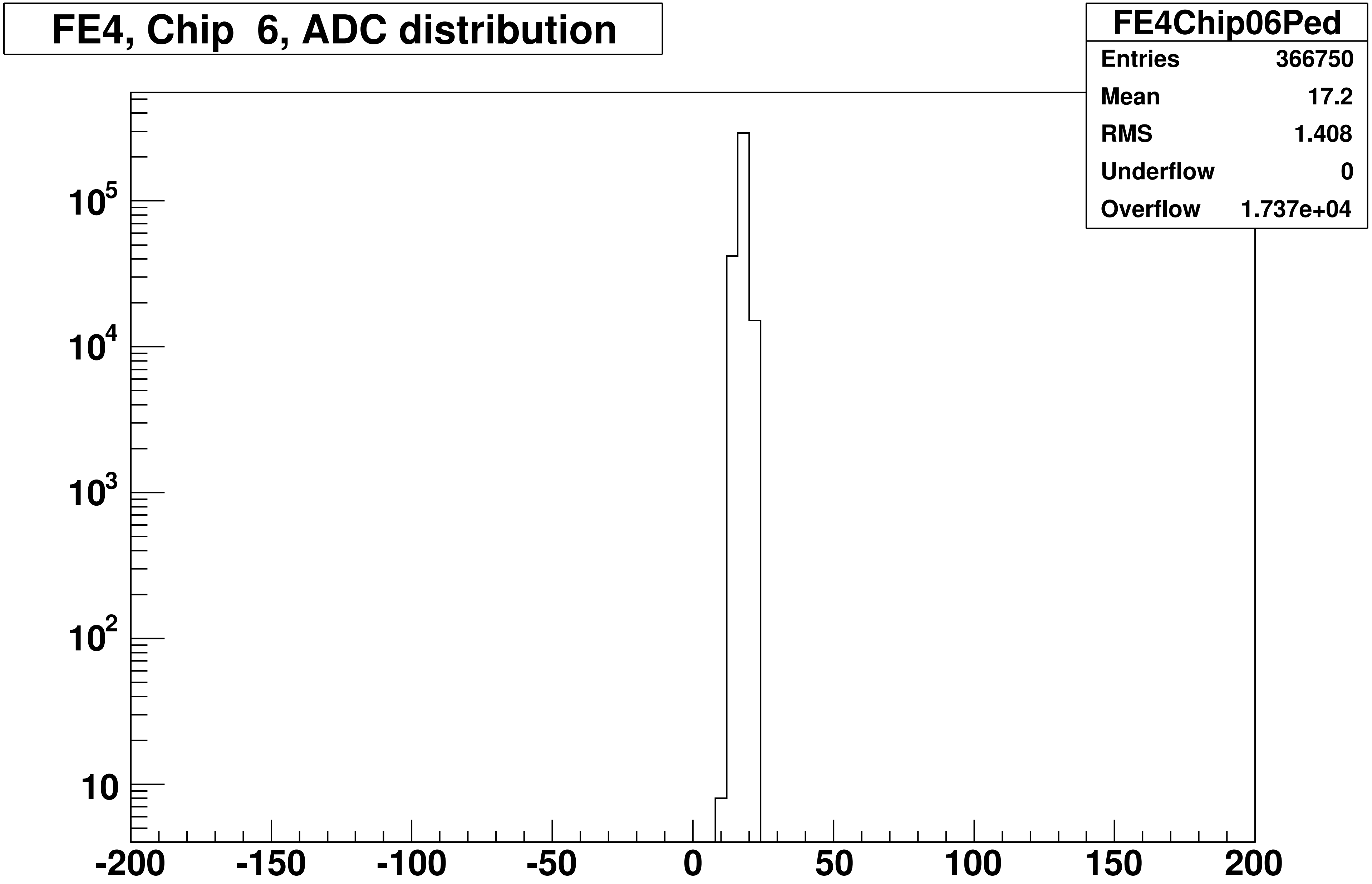
20000
25000


FE4, Chip 5, ADC distribution
FE4Chip05Ped
Entries 366750
Mean 24.75
RMS 1.418
Underflow 0
Overflow 1.921e+04
10^5
10^4
10^3
10^2
10
-200
-150
-100
-50
0
50
100
150
200



FE4, Chip 5, ADC distribution
FE4Chip05Sig
Entries 366750
Mean 1.231e+04
RMS 65.98
Underflow 3.476e+05
Overflow 0
10^3
10^2
10
10000
10500
11000
11500
12000
12500
13000
13500
14000


FE4, Chip 6, ADC distribution
FE4Chip06All
Entries 366750
Mean 595
RMS 2593
Underflow 0
Overflow 0
10
10^2
10^3
10^4
10^5
-5000
0
5000
10000
15000
20000
25000


FE4, Chip 6, ADC distribution
FE4Chip06Ped
Entries 366750
Mean 17.2
RMS 1.408
Underflow 0
Overflow 1.737e+04
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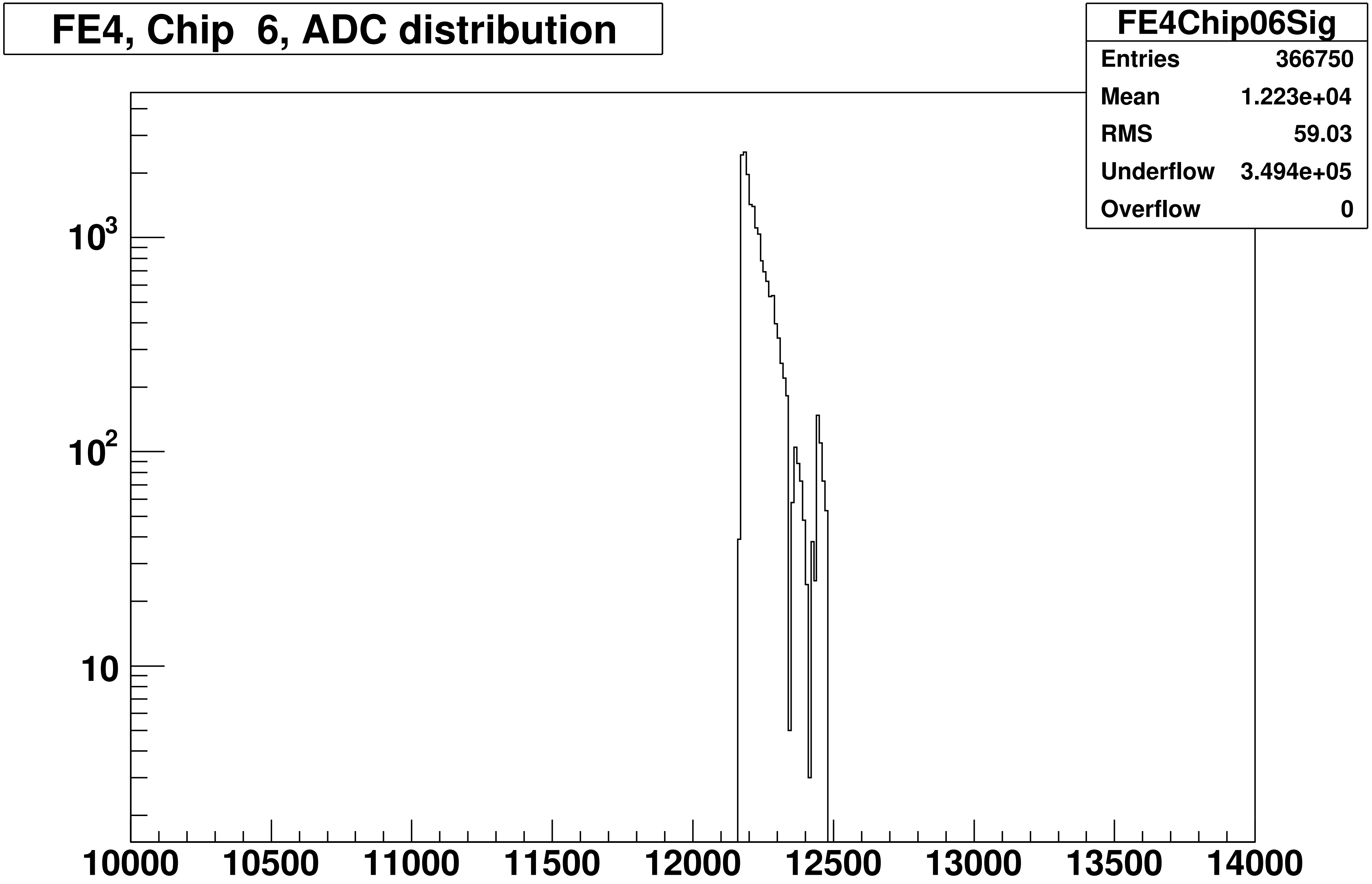
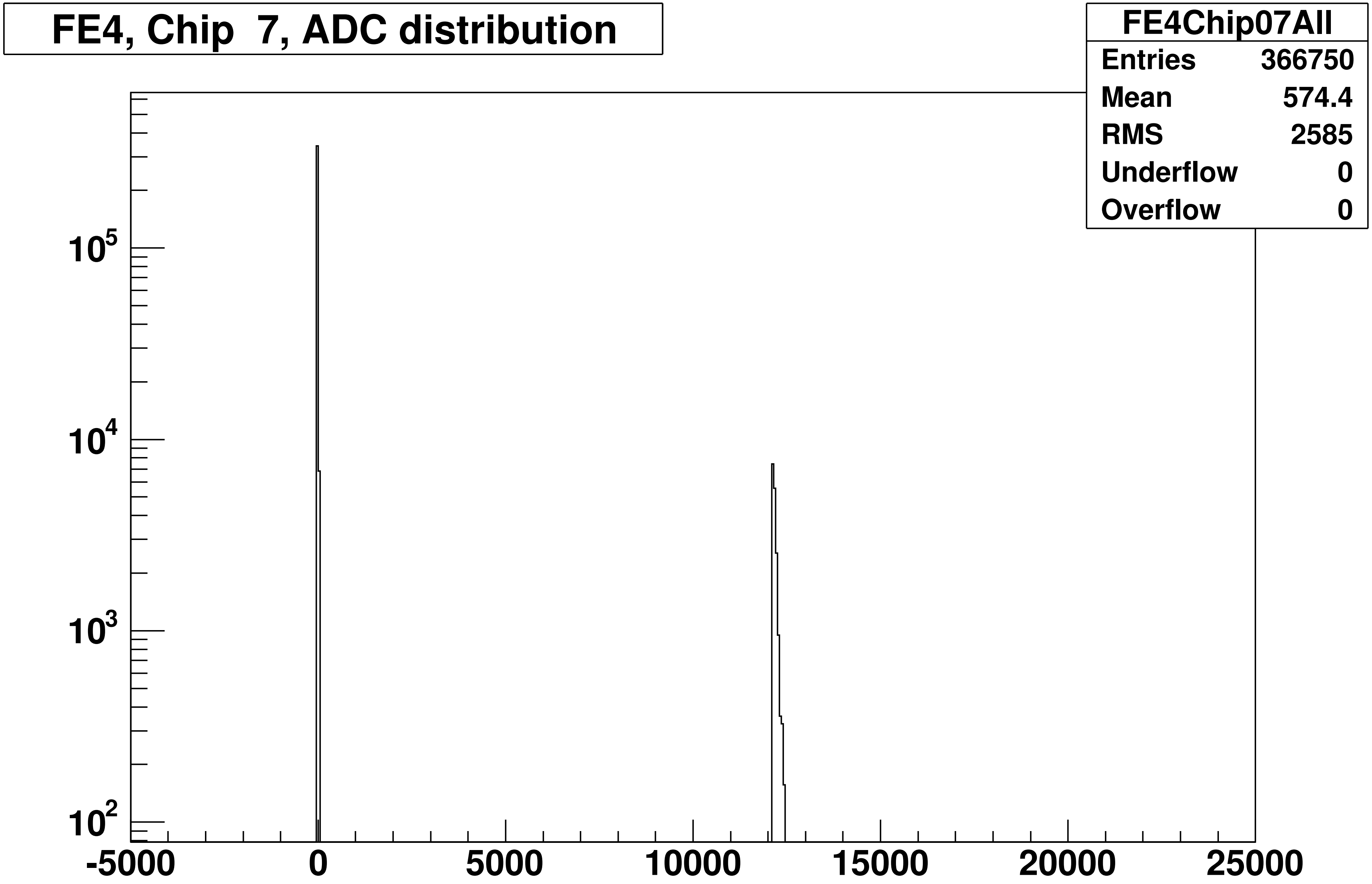
10^2
10^3
10^4
10^5
-200
-150
-100
-50
0
50
100
150
200



FE4, Chip 6, ADC distribution
FE4Chip06Sig
Entries 366750
Mean 1.223e+04
RMS 59.03
Underflow 3.494e+05
Overflow 0
10
10^2
10^3
10000
10500
11000
11500
12000
12500
13000
13500
14000


FE4, Chip 7, ADC distribution
FE4Chip07All
Entries 366750
Mean 574.4
RMS 2585
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
-5000
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5000
10000
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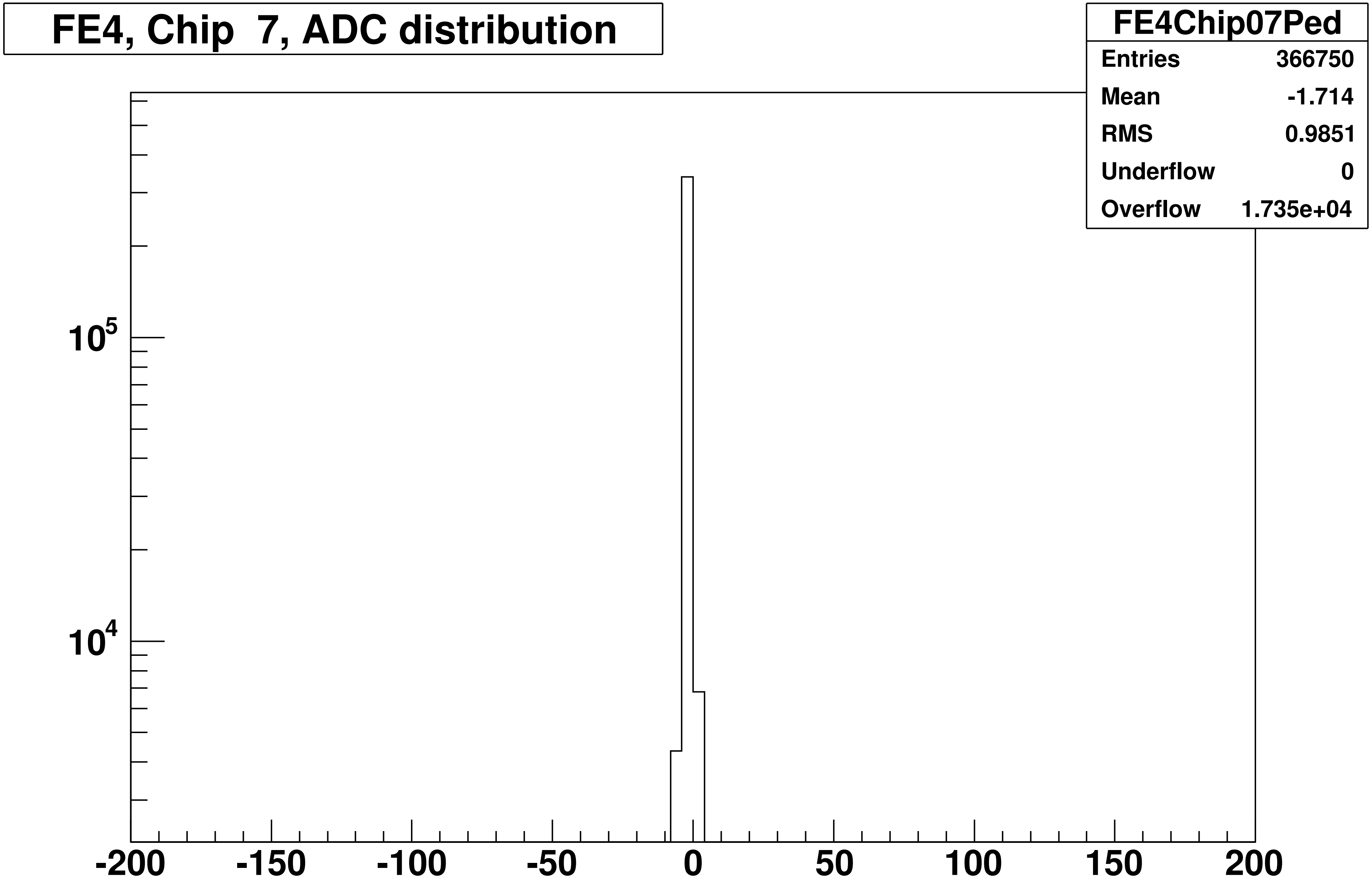
20000
25000



FE4, Chip 7, ADC distribution
FE4Chip07Ped
Entries 366750
Mean -1.714
RMS 0.9851
Underflow 0
Overflow 1.735e+04
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10^4
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-150
-100
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0
50
100
150
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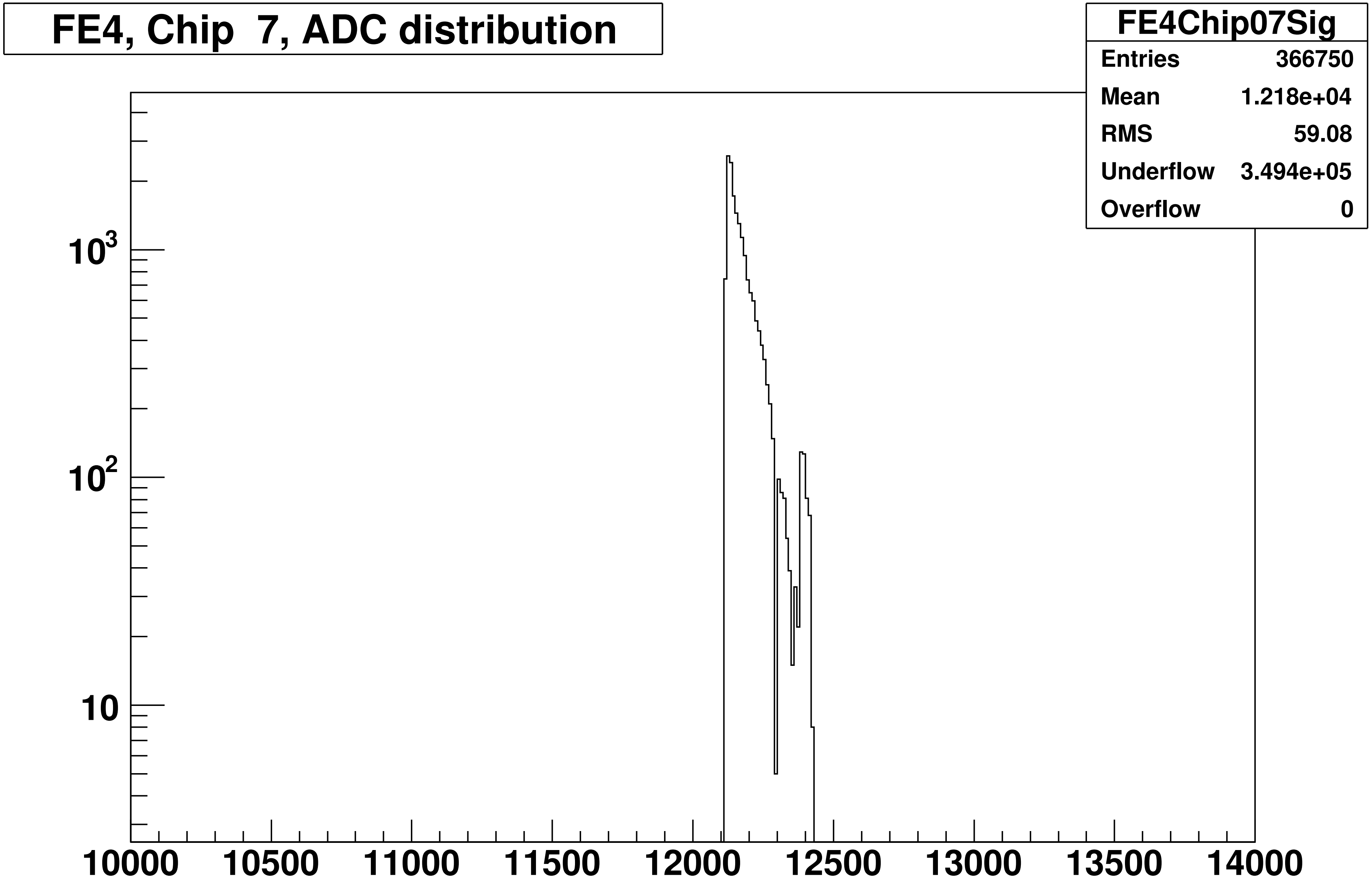

FE4, Chip 7, ADC distribution
FE4Chip07Sig
Entries 366750
Mean 1.218e+04
RMS 59.08
Underflow 3.494e+05
Overflow 0
10^3
10^2
10
10000
10500
11000
11500
12000
12500
13000
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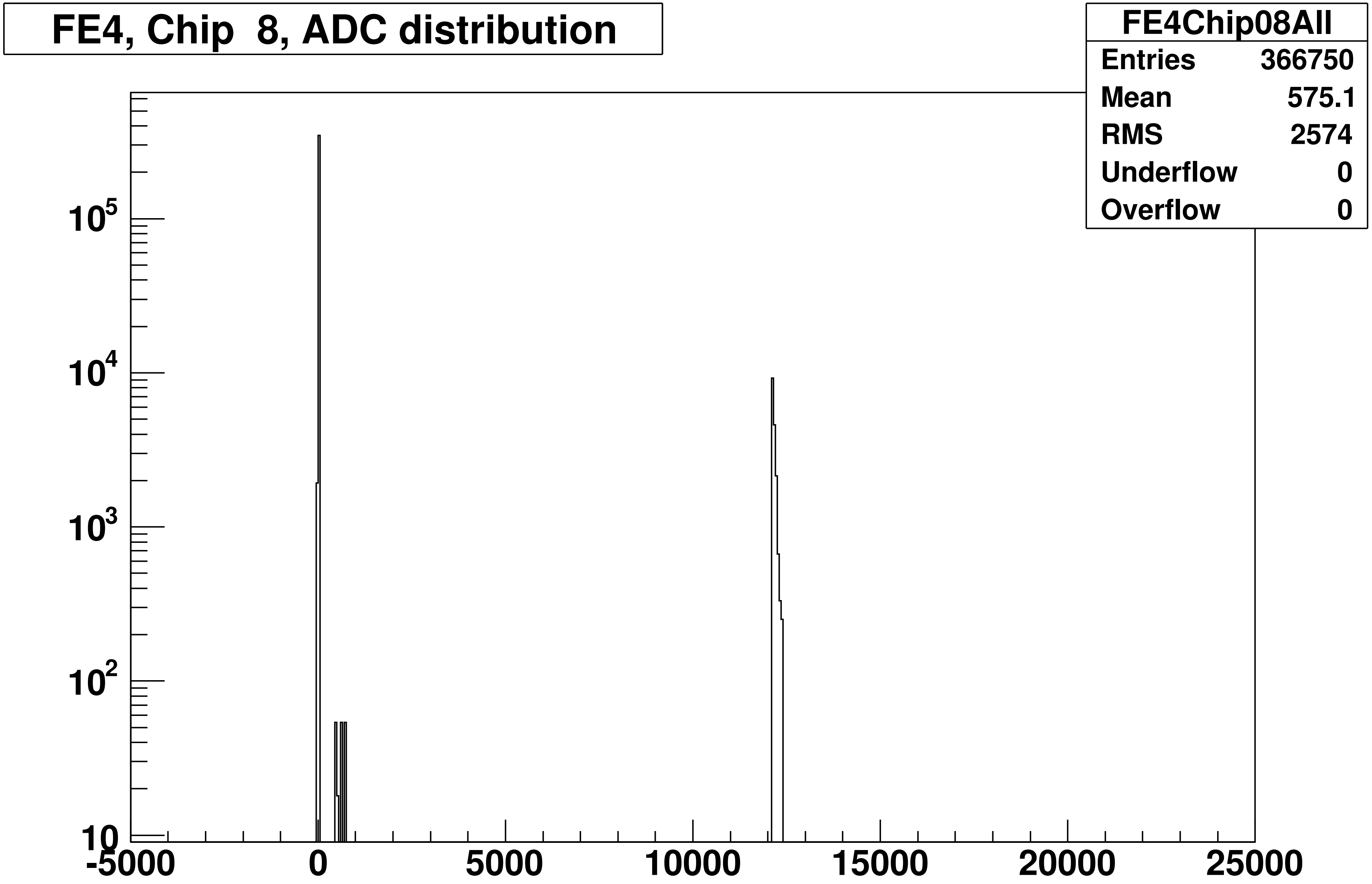
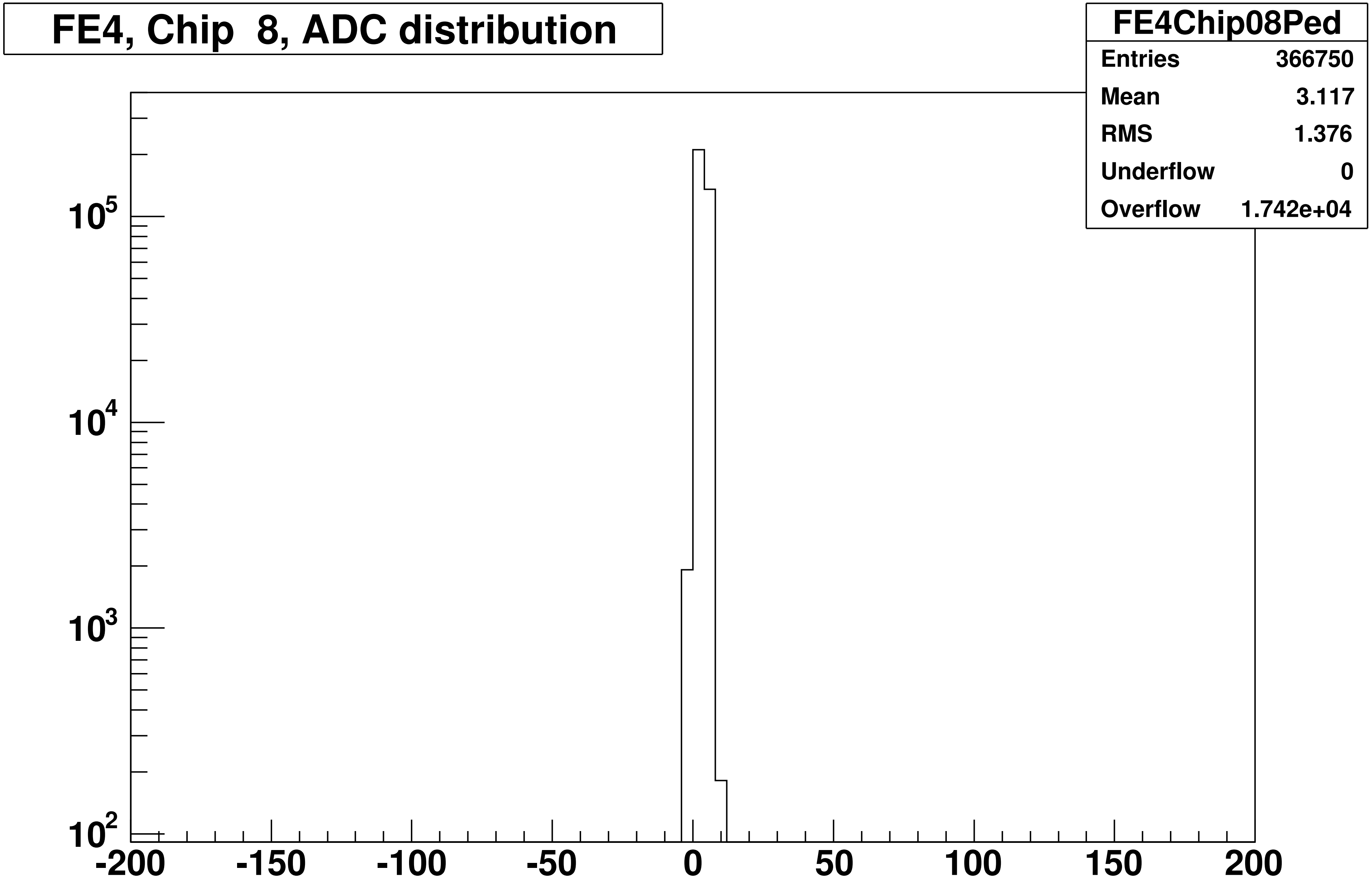
14000


FE4, Chip 8, ADC distribution
FE4Chip08All
Entries 366750
Mean 575.1
RMS 2574
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000



FE4, Chip 8, ADC distribution
FE4Chip08Ped
Entries 366750
Mean 3.117
RMS 1.376
Underflow 0
Overflow 1.742e+04
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10^4
10^3
10^2
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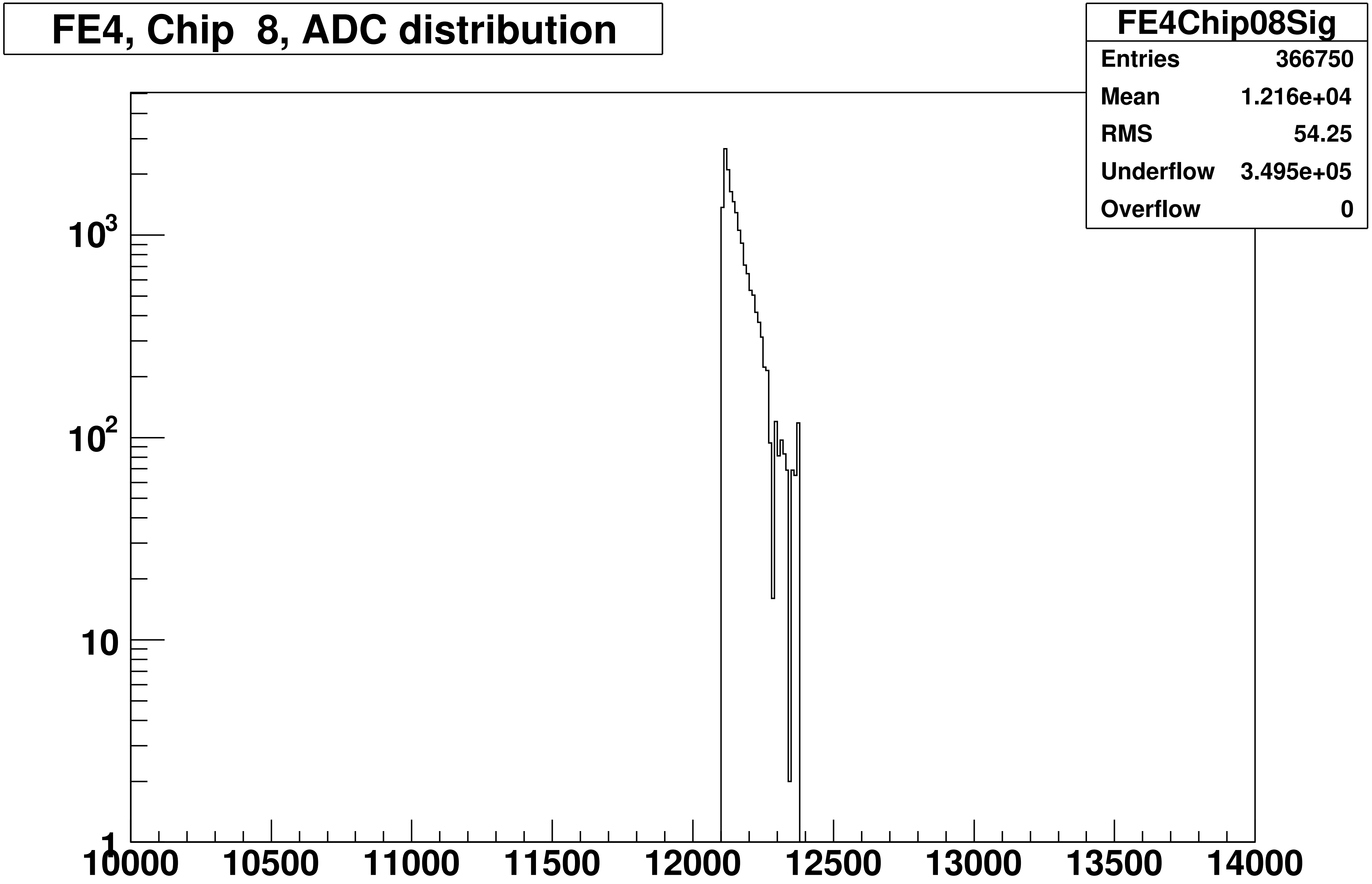
-150
-100
-50
0
50
100
150
200


FE4, Chip 8, ADC distribution
FE4Chip08Sig
Entries 366750
Mean 1.216e+04
RMS 54.25
Underflow 3.495e+05
Overflow 0
10³
10²
10
1
10000
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11500
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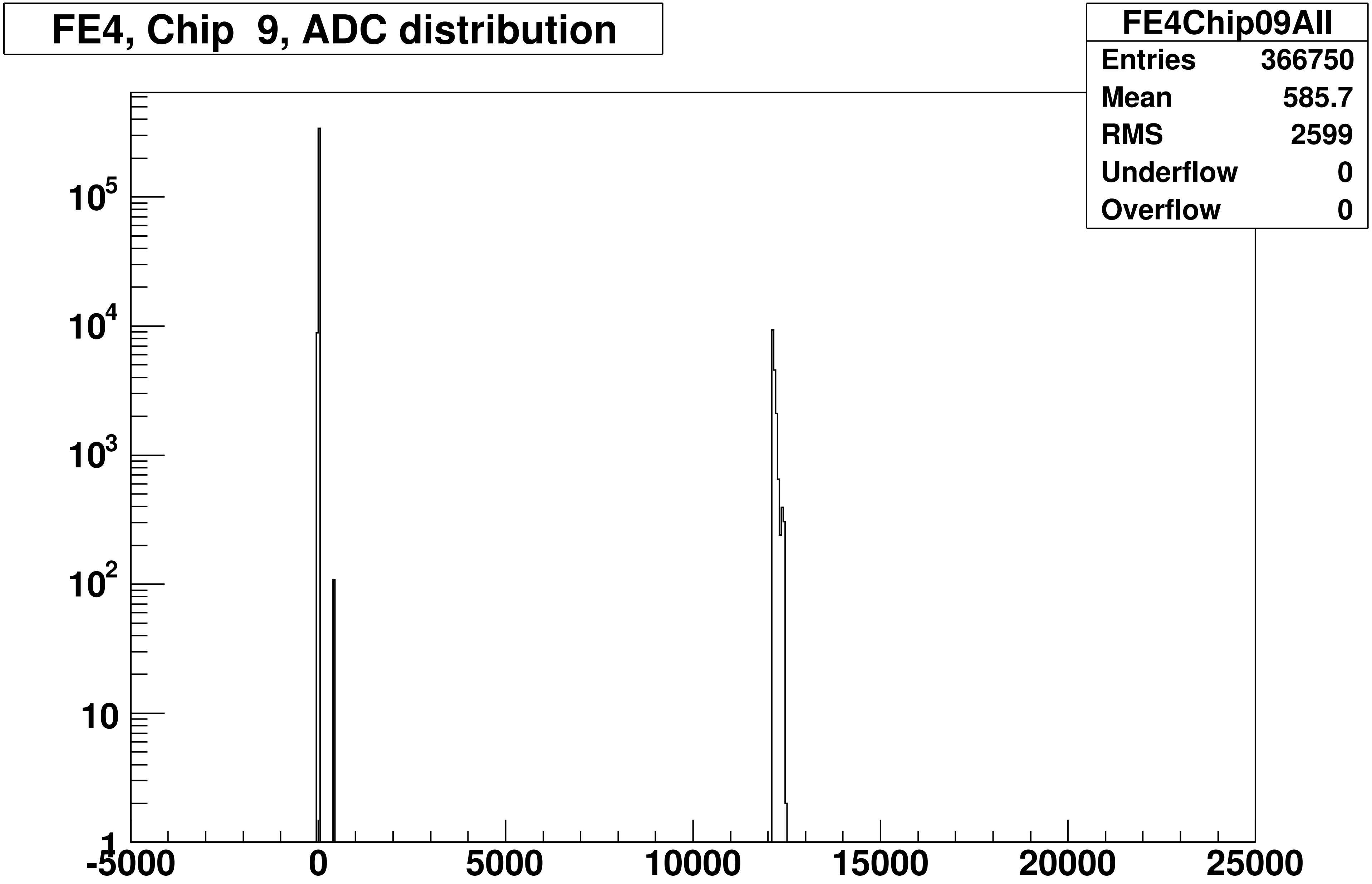
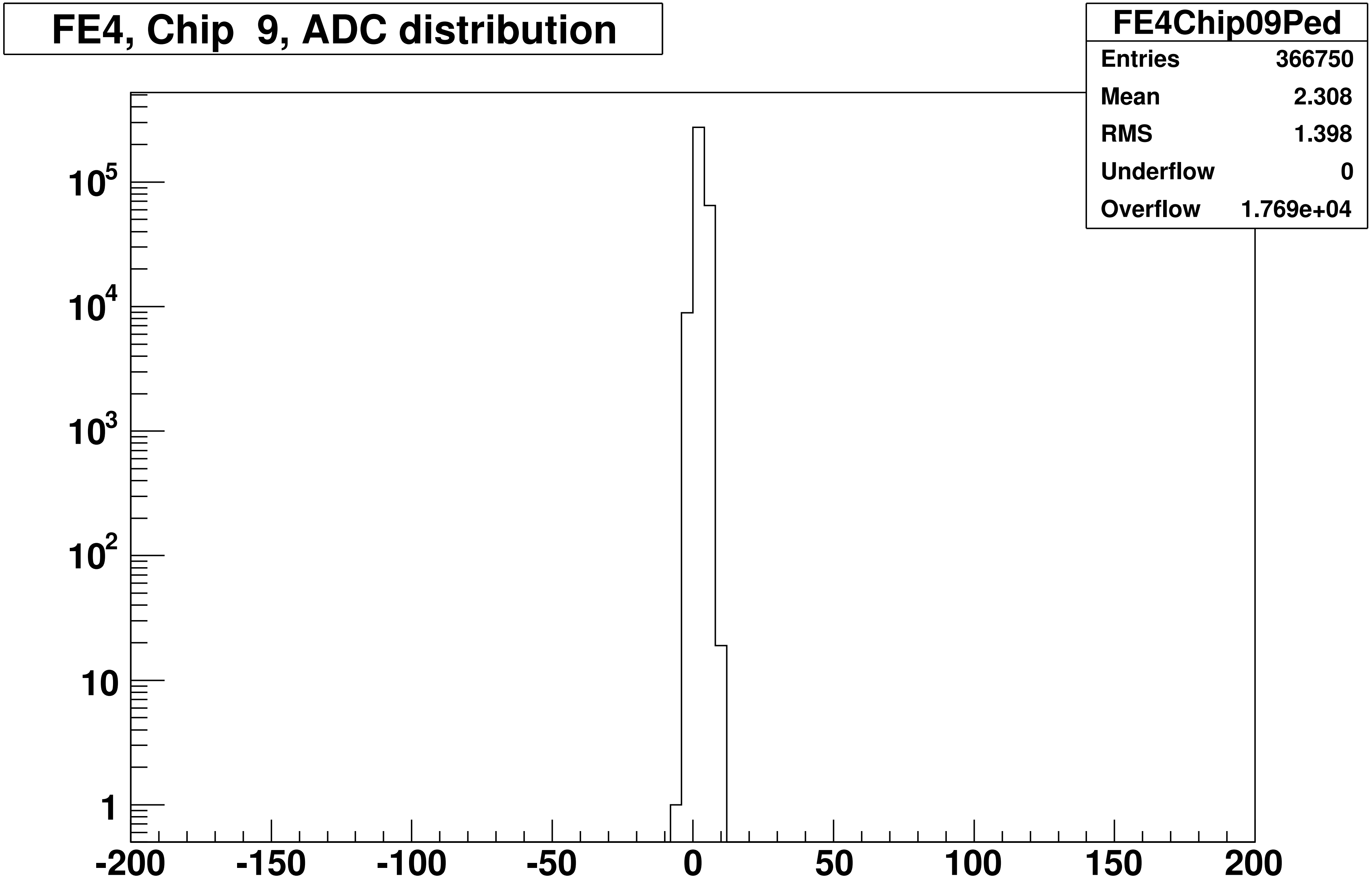
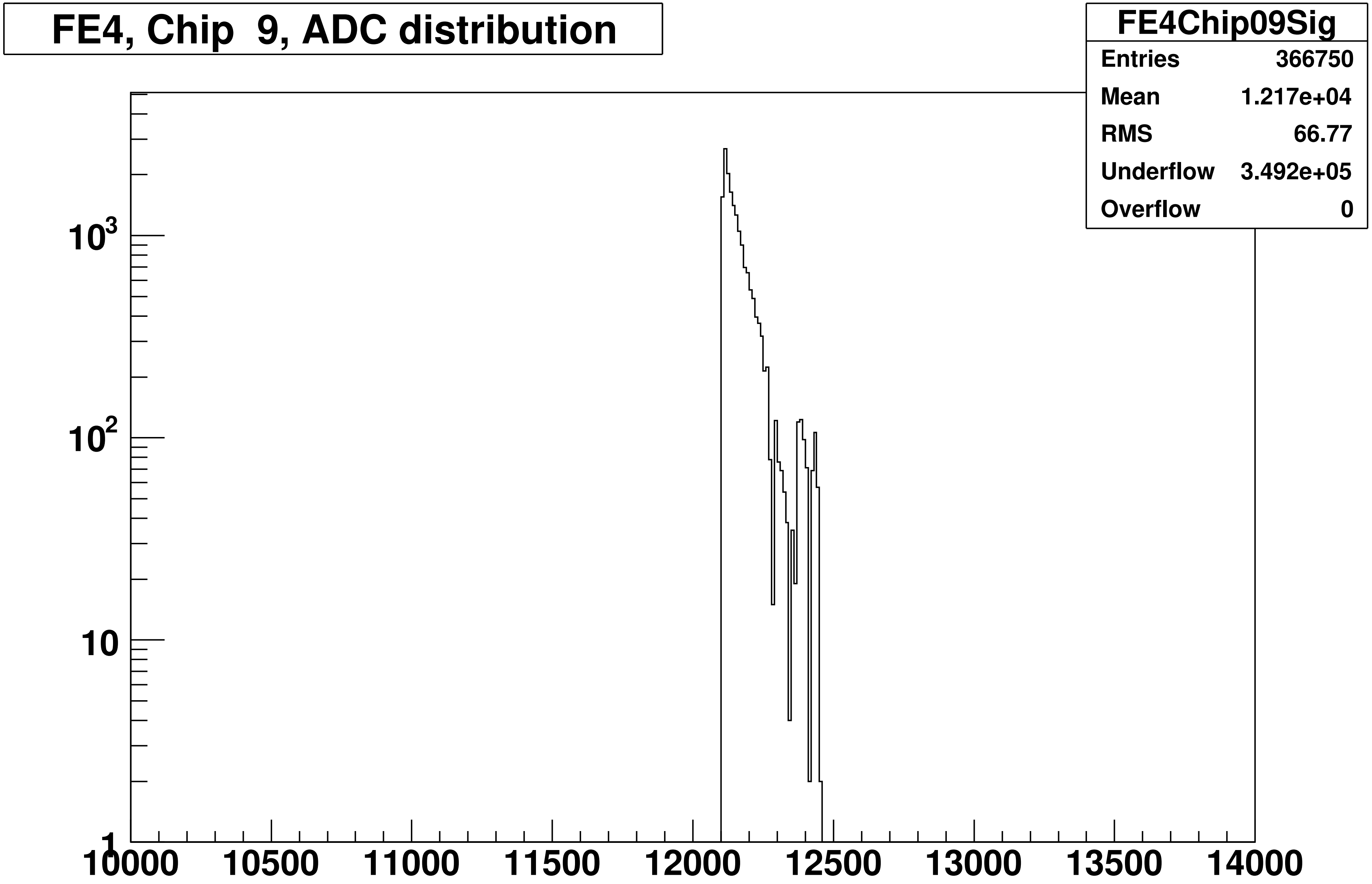
13500
14000


FE4, Chip 9, ADC distribution
FE4Chip09All
Entries 366750
Mean 585.7
RMS 2599
Underflow 0
Overflow 0
1
10
10^2
10^3
10^4
10^5
-5000
0
5000
10000
15000
20000
25000



FE4, Chip 9, ADC distribution
FE4Chip09Ped
Entries 366750
Mean 2.308
RMS 1.398
Underflow 0
Overflow 1.769e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
200


FE4, Chip 9, ADC distribution
FE4Chip09Sig
Entries 366750
Mean 1.217e+04
RMS 66.77
Underflow 3.492e+05
Overflow 0
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10^2
10
1
10000
10500
11000
11500
12000
12500
13000
13500
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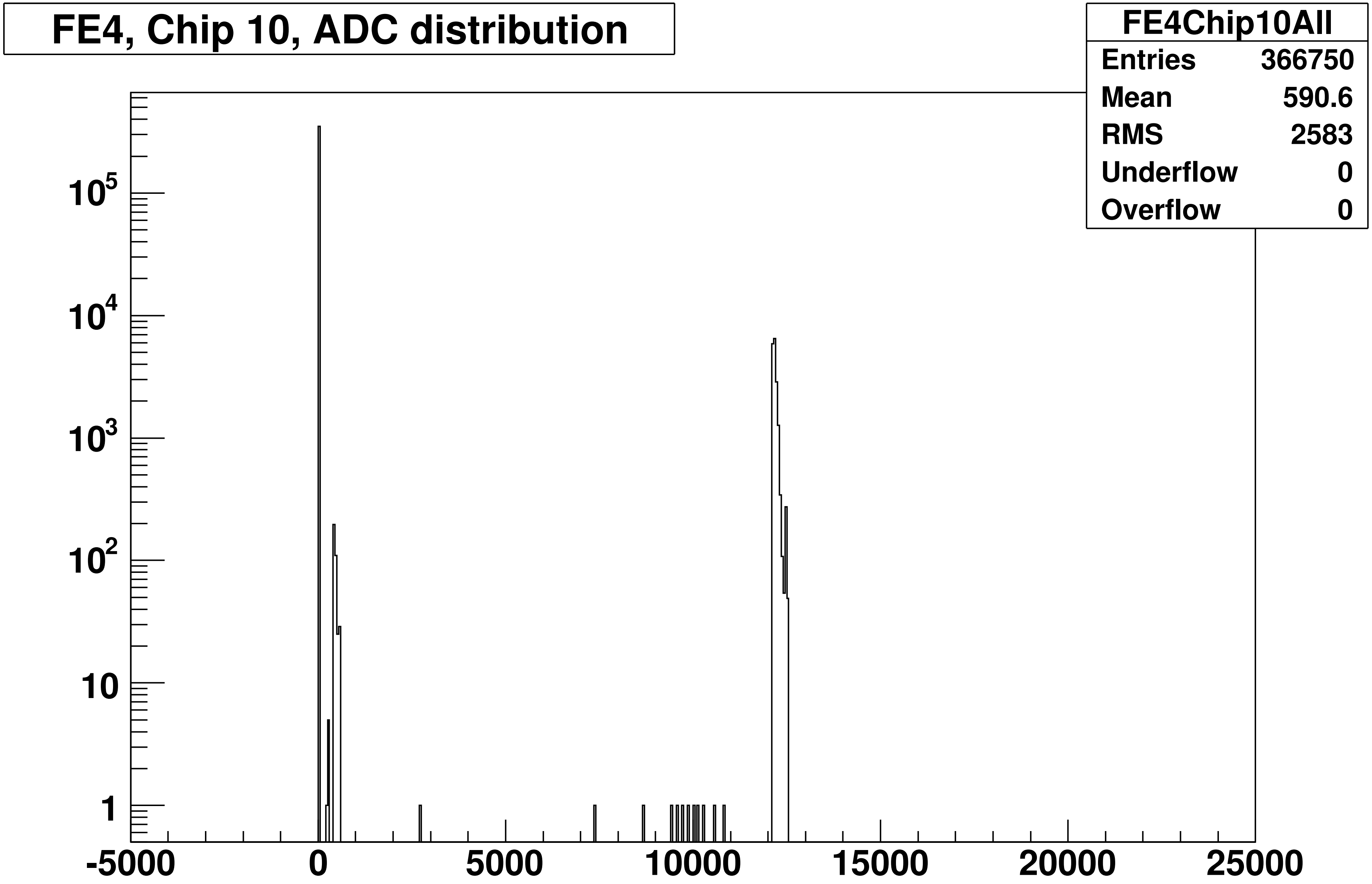
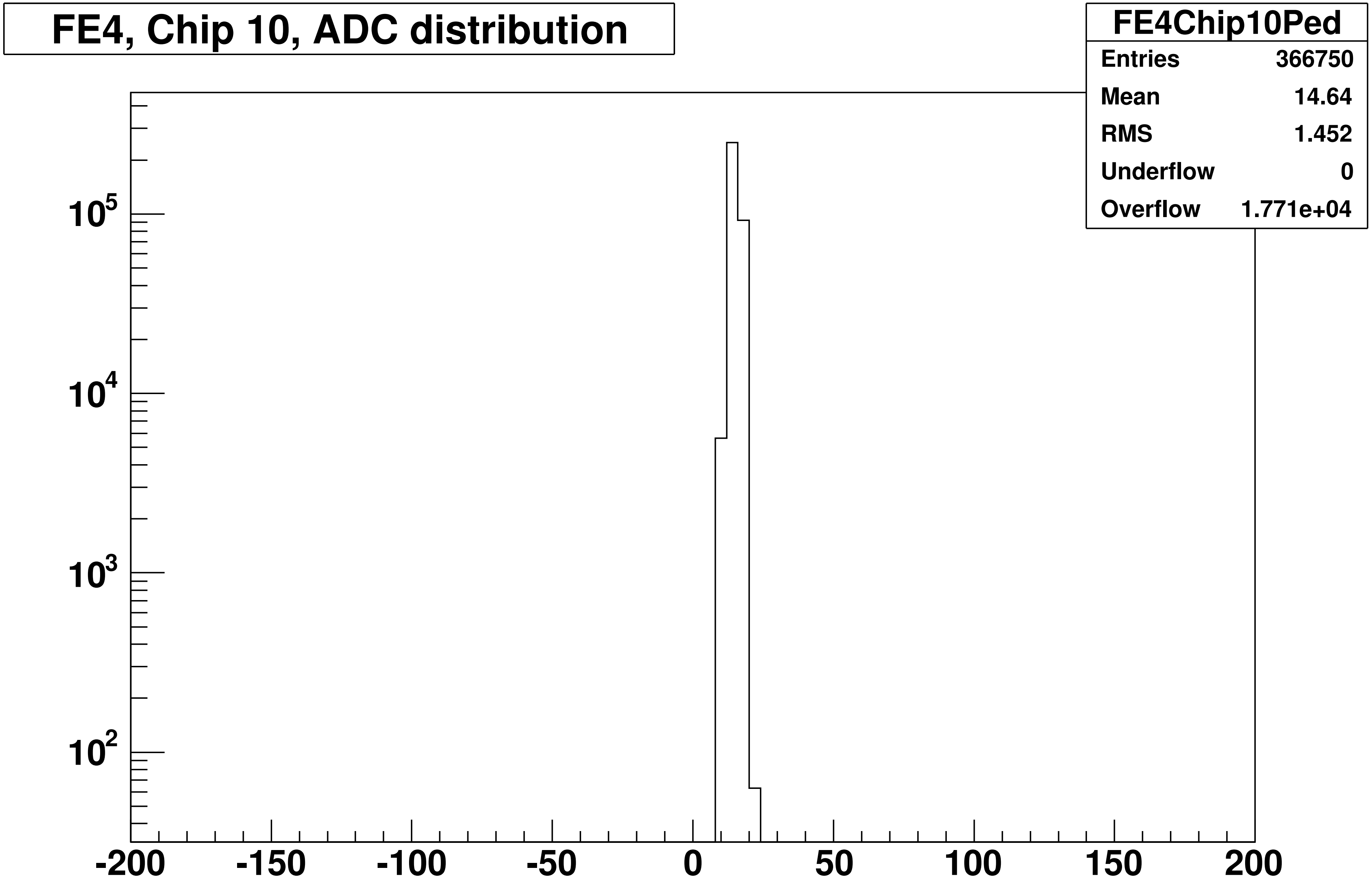
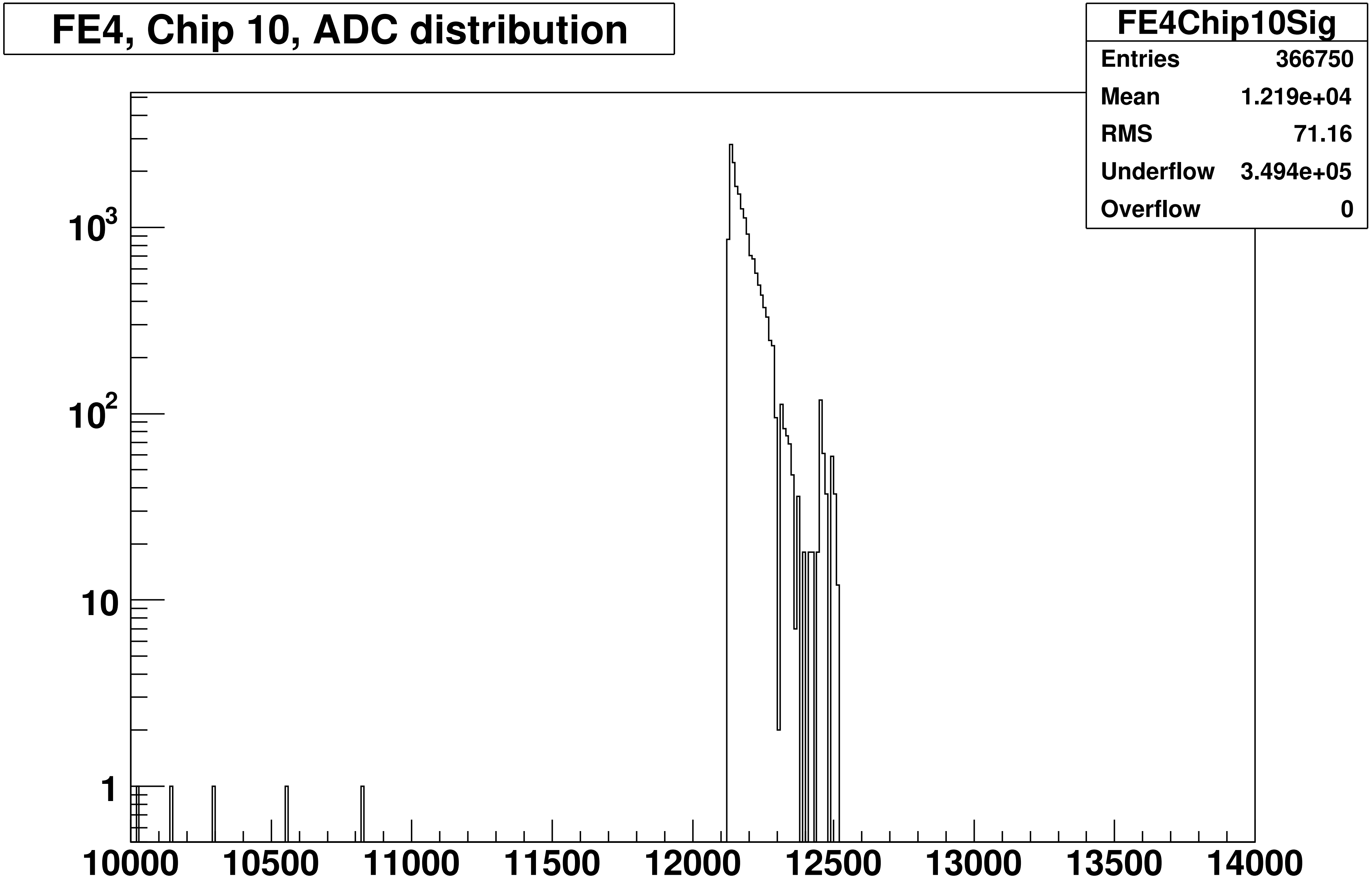


FE4, Chip 10, ADC distribution
FE4Chip10All
Entries 366750
Mean 590.6
RMS 2583
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE4, Chip 10, ADC distribution
FE4Chip10Ped
Entries 366750
Mean 14.64
RMS 1.452
Underflow 0
Overflow 1.771e+04
10^5
10^4
10^3
10^2
-200
-150
-100
-50
0
50
100
150
200


FE4, Chip 10, ADC distribution
FE4Chip10Sig
Entries 366750
Mean 1.219e+04
RMS 71.16
Underflow 3.494e+05
Overflow 0
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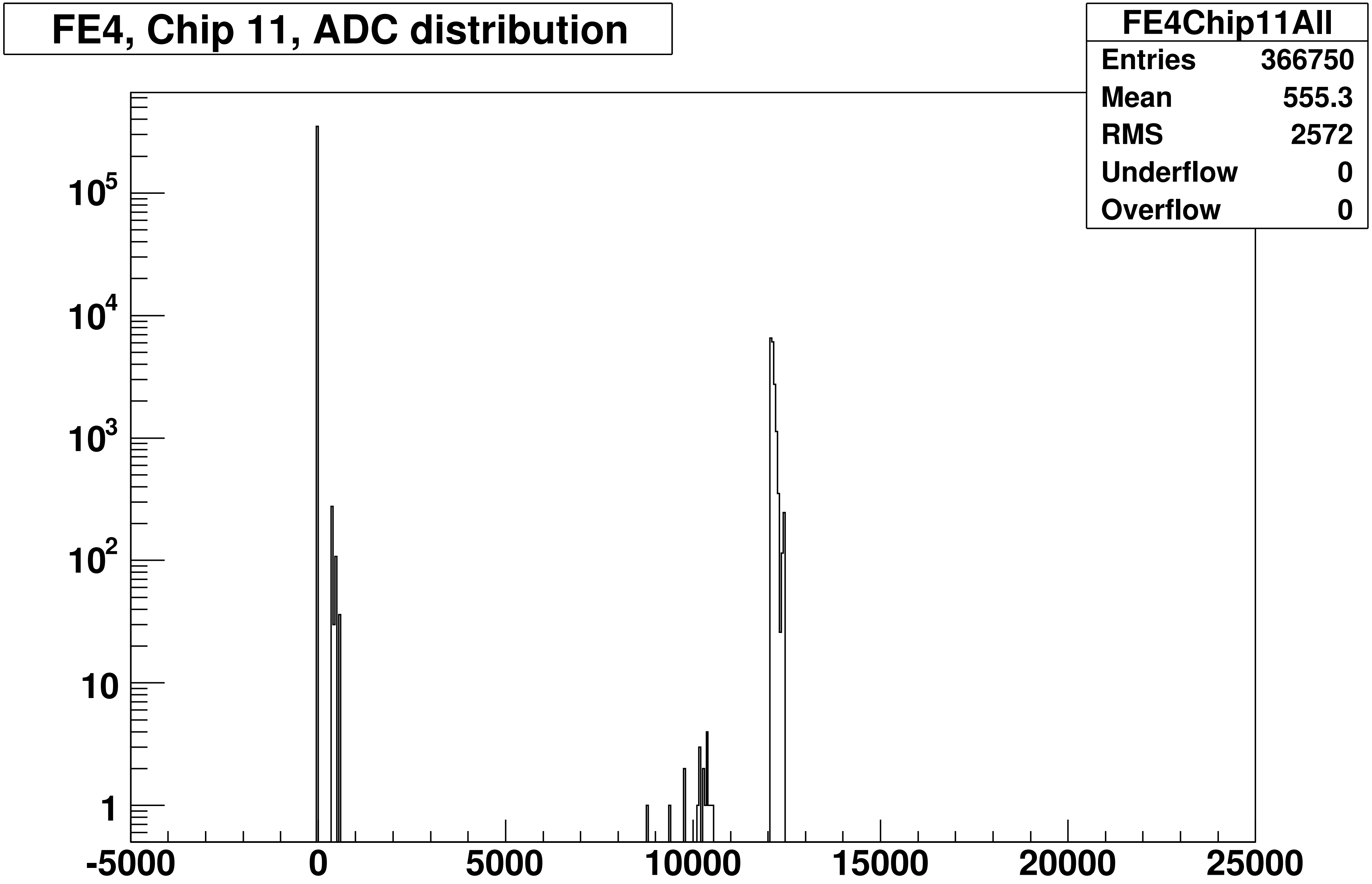
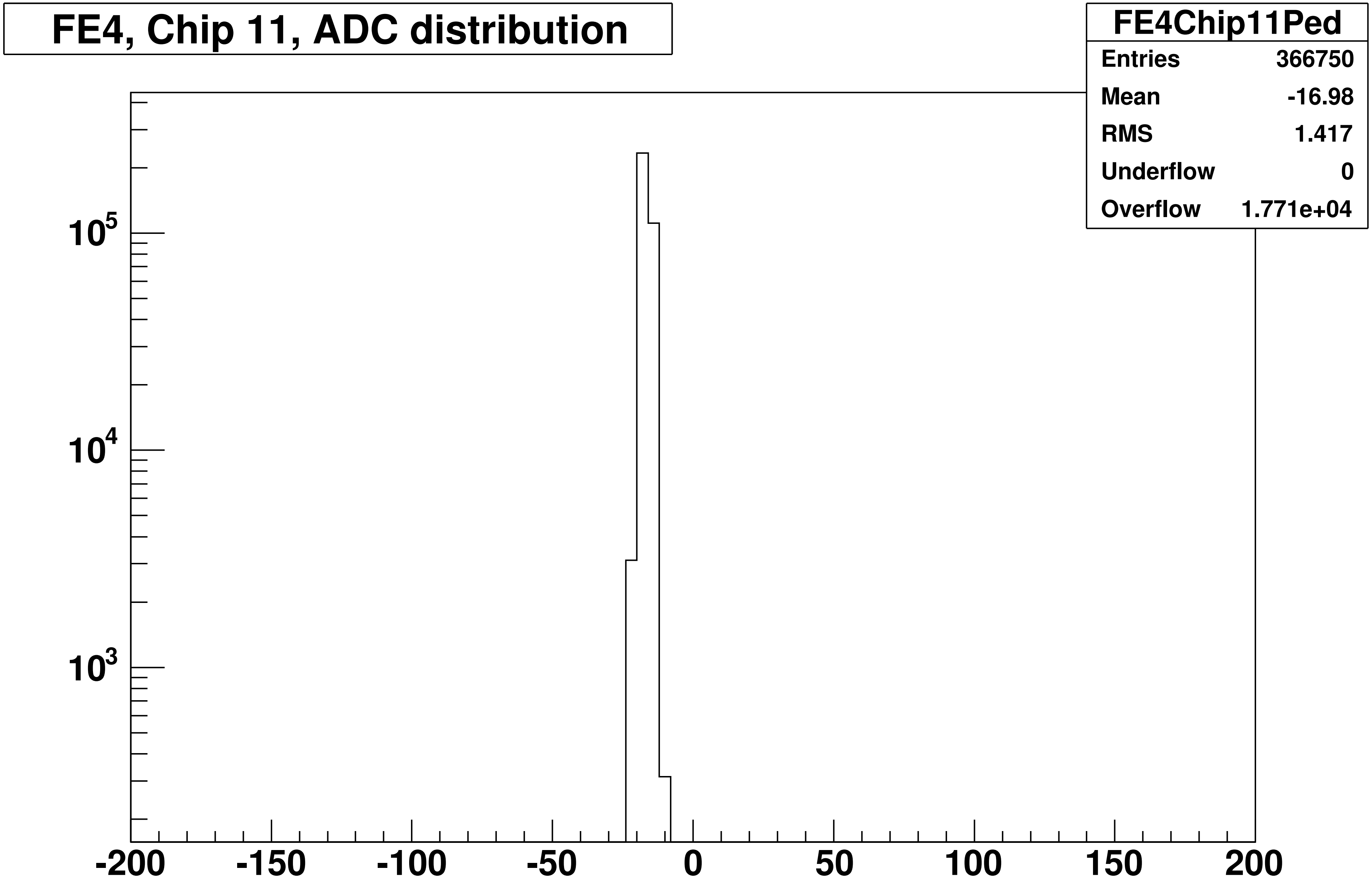
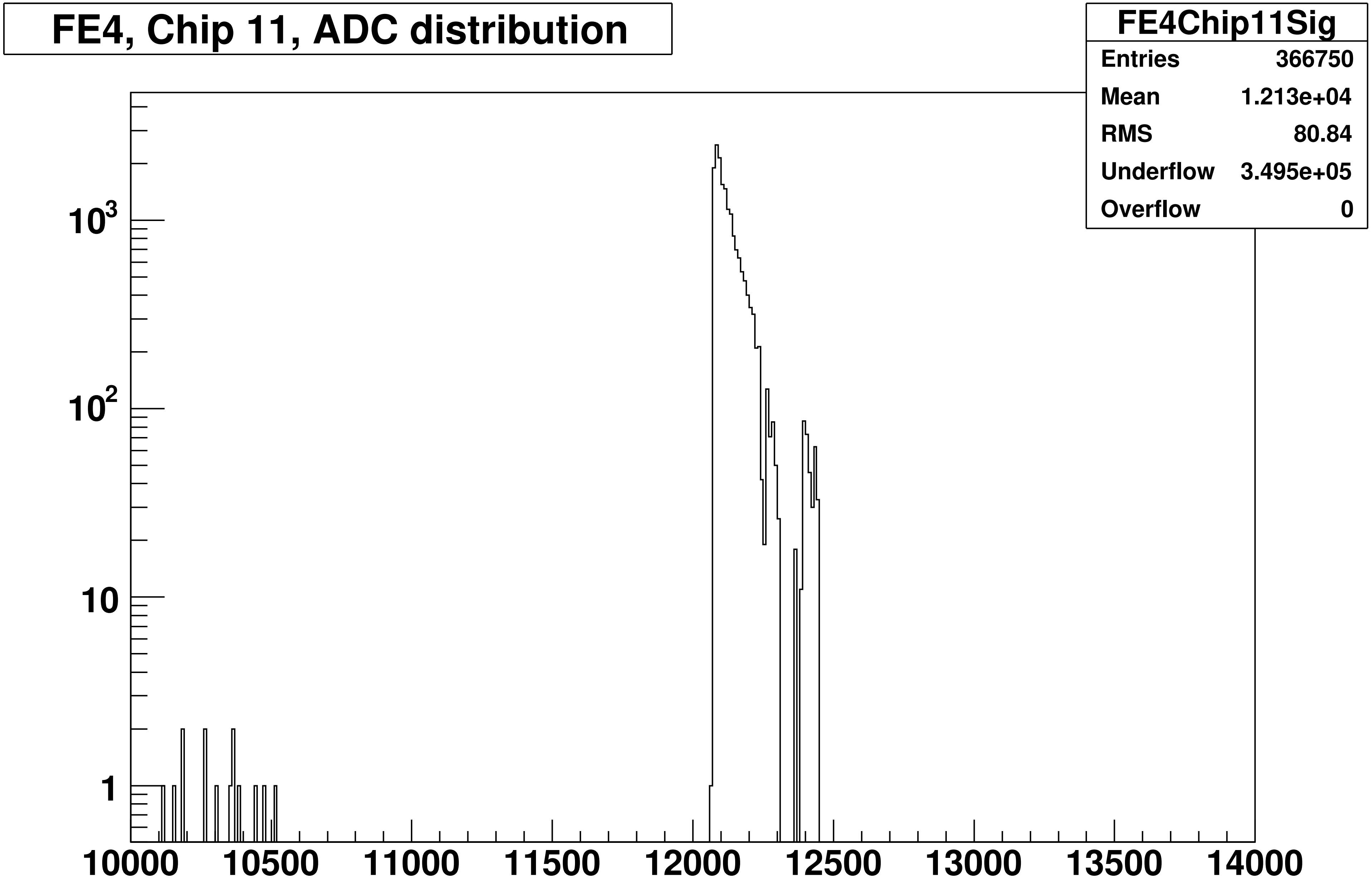
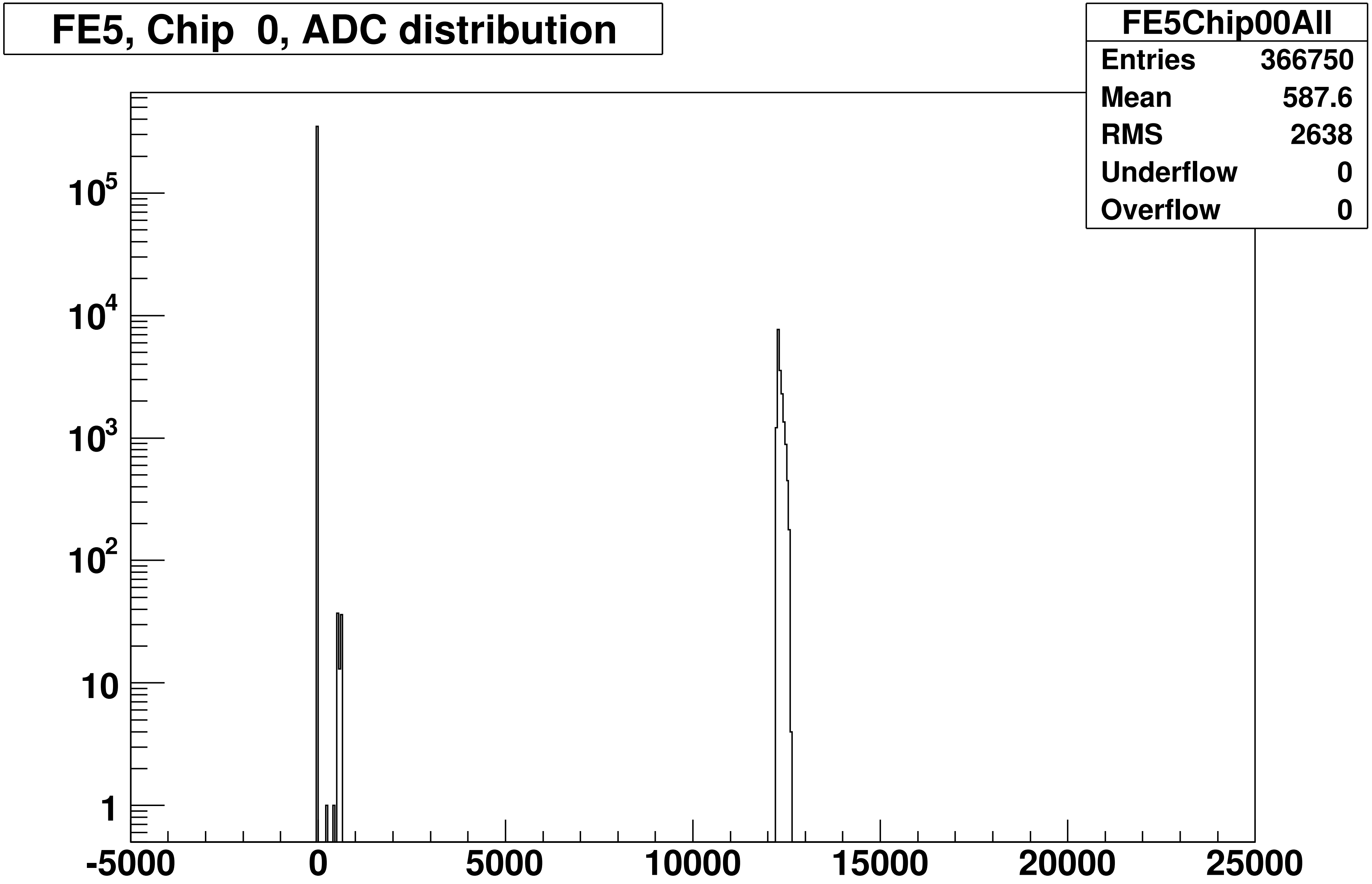
10^2
10
1
10000
10500
11000
11500
12000
12500
13000
13500
14000

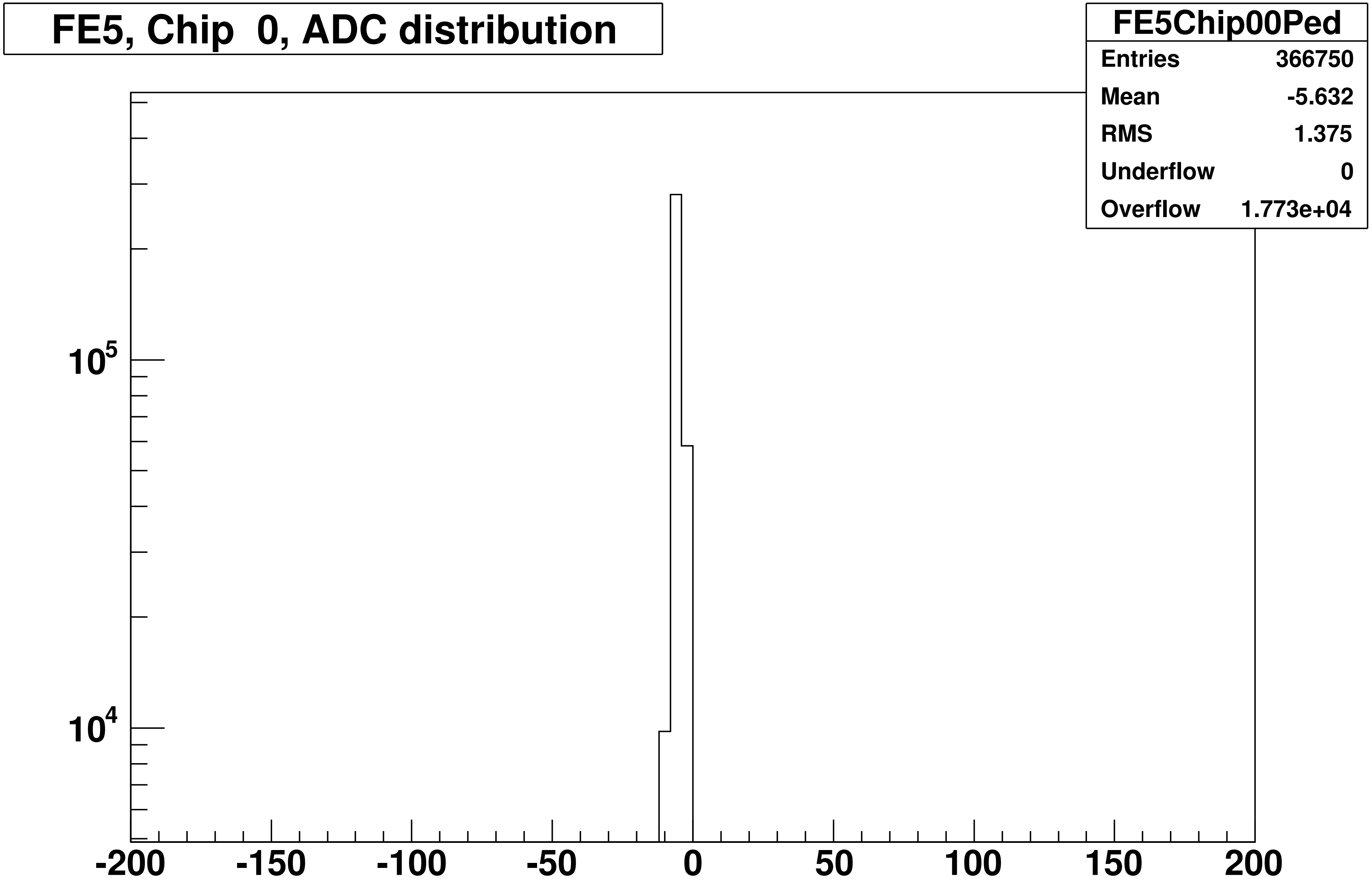

FE4, Chip 11, ADC distribution
FE4Chip11All
Entries 366750
Mean 555.3
RMS 2572
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000

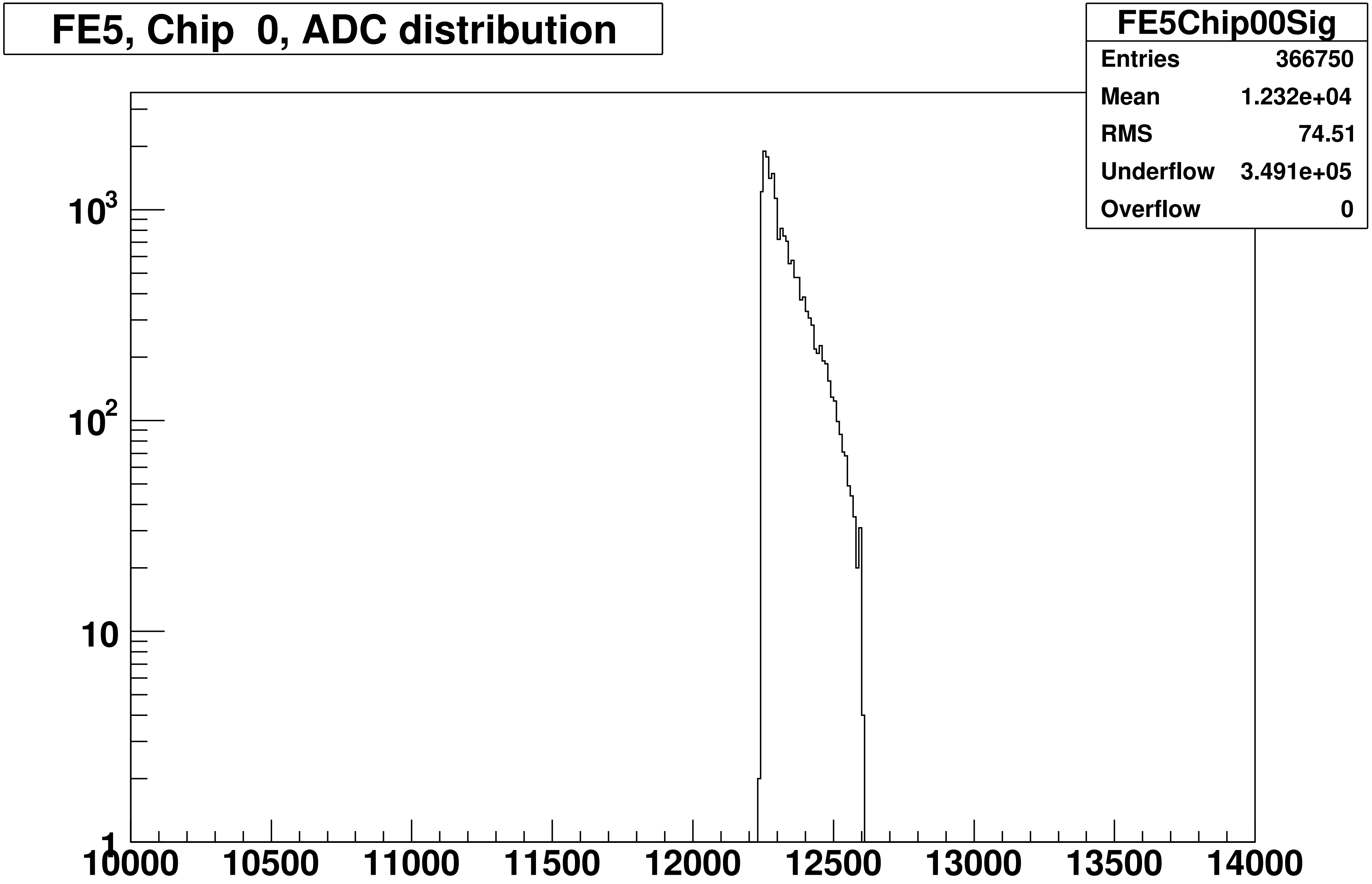

FE4, Chip 11, ADC distribution
FE4Chip11Ped
Entries 366750
Mean -16.98
RMS 1.417
Underflow 0
Overflow 1.771e+04
10^5
10^4
10^3
-200
-150
-100
-50
0
50
100
150
200



FE4, Chip 11, ADC distribution
FE4Chip11Sig
Entries 366750
Mean 1.213e+04
RMS 80.84
Underflow 3.495e+05
Overflow 0
10^3
10^2
10
1
10000
10500
11000
11500
12000
12500
13000
13500
14000


FE5, Chip 0, ADC distribution
FE5Chip00All
Entries 366750
Mean 587.6
RMS 2638
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE5, Chip 0, ADC distribution
FE5Chip00Ped
Entries 366750
Mean -5.632
RMS 1.375
Underflow 0
Overflow 1.773e+04
10^5
10^4
-200
-150
-100
-50
0
50
100
150
200



FE5, Chip 0, ADC distribution
FE5Chip00Sig
Entries 366750
Mean 1.232e+04
RMS 74.51
Underflow 3.491e+05
Overflow 0
10^3
10^2
10
1
10000
10500
11000
11500
12000
12500
13000
13500
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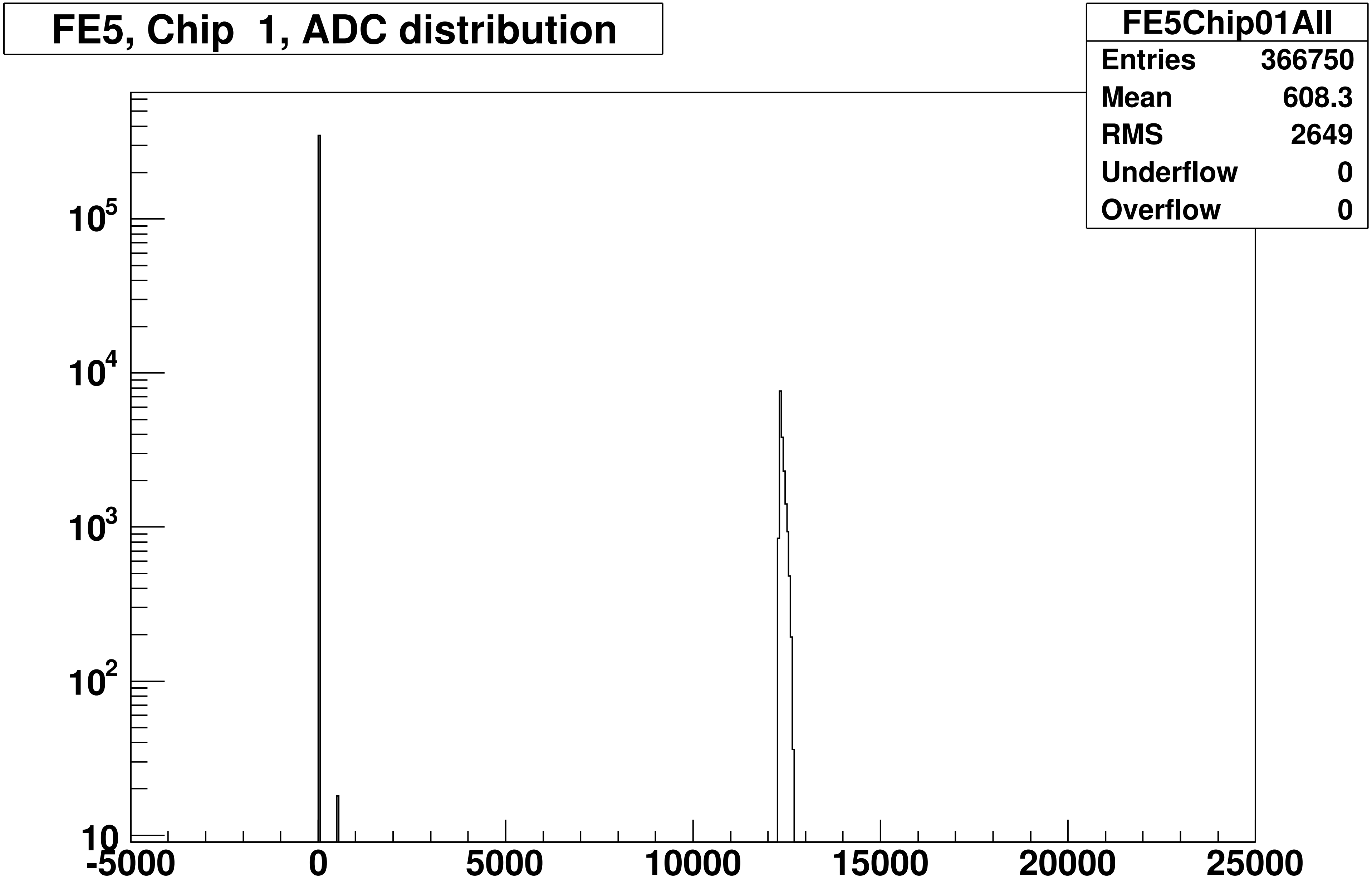
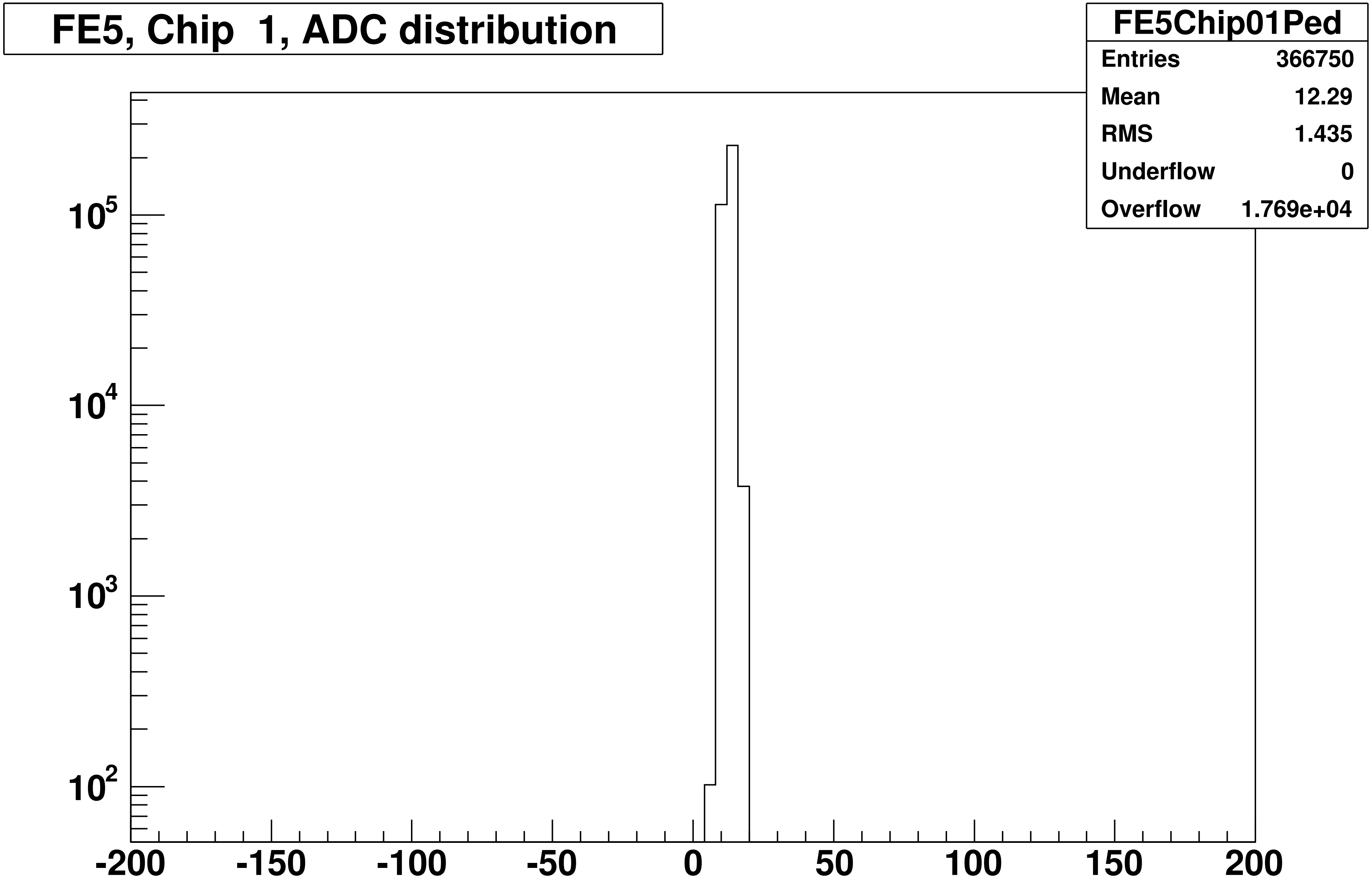

FE5, Chip 1, ADC distribution
FE5Chip01All
Entries 366750
Mean 608.3
RMS 2649
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE5, Chip 1, ADC distribution
FE5Chip01Ped
Entries 366750
Mean 12.29
RMS 1.435
Underflow 0
Overflow 1.769e+04
10^5
10^4
10^3
10^2
-200
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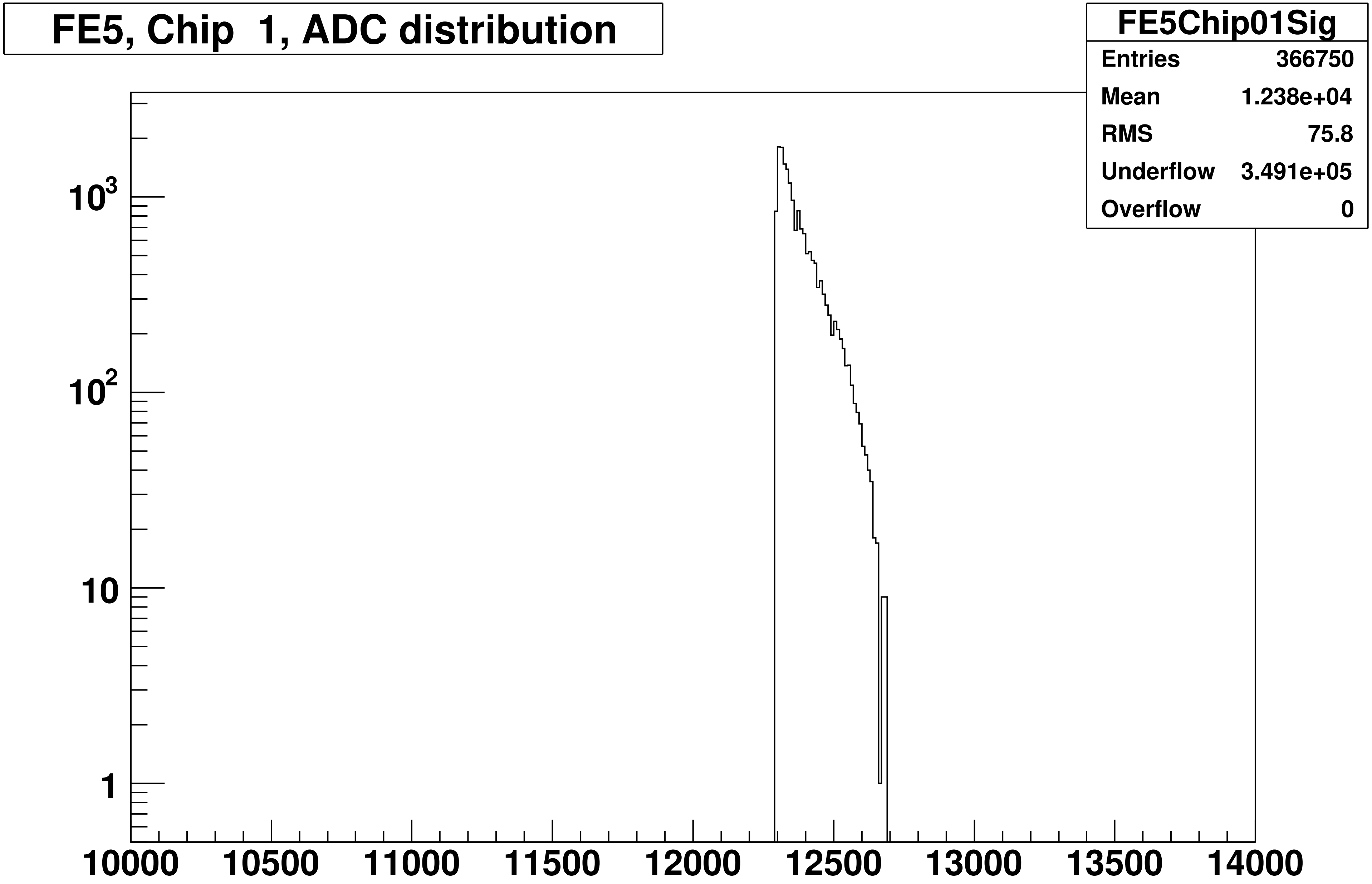
-100
-50
0
50
100
150
200



FE5, Chip 1, ADC distribution
FE5Chip01Sig
Entries 366750
Mean 1.238e+04
RMS 75.8
Underflow 3.491e+05
Overflow 0
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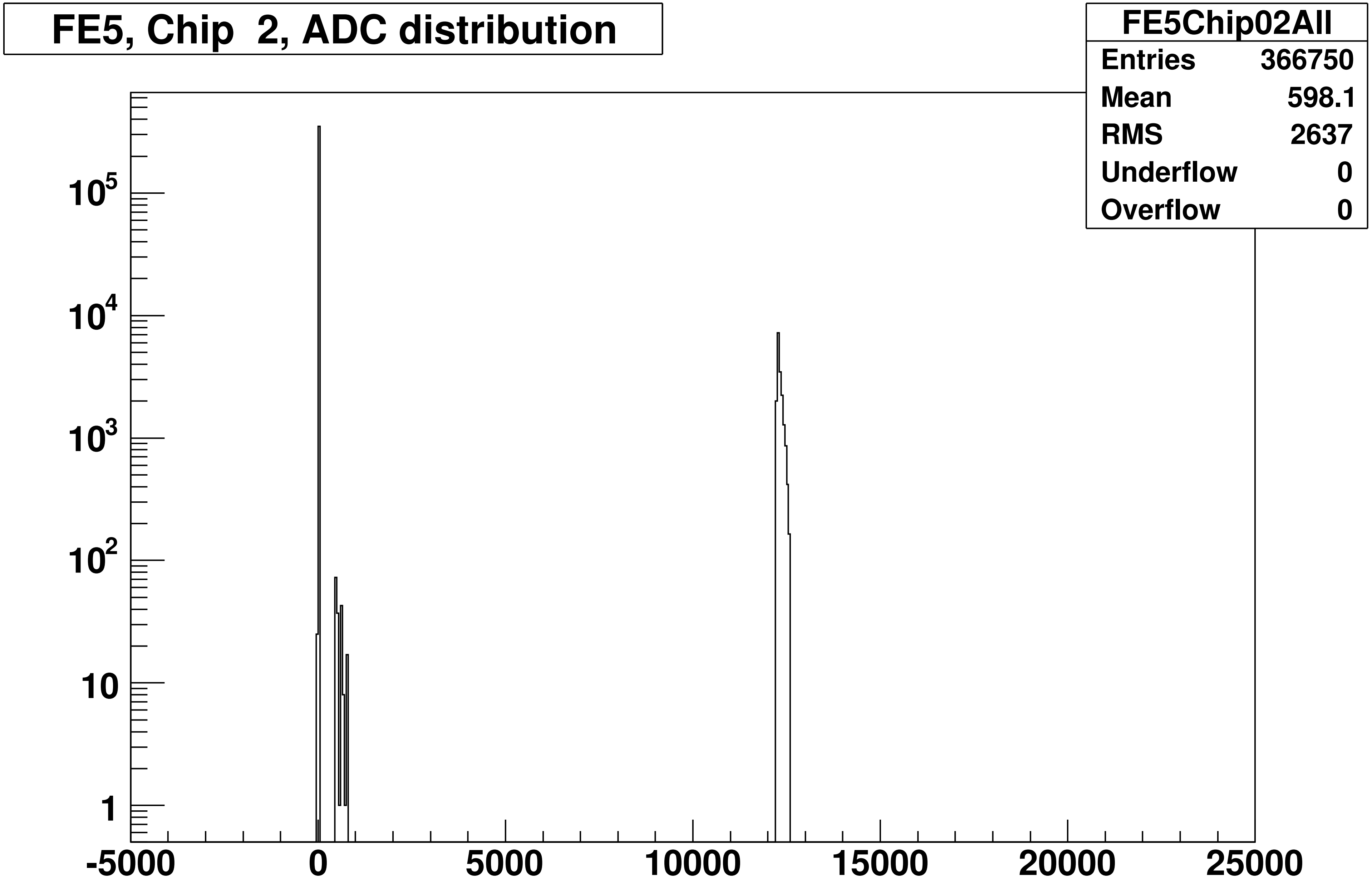
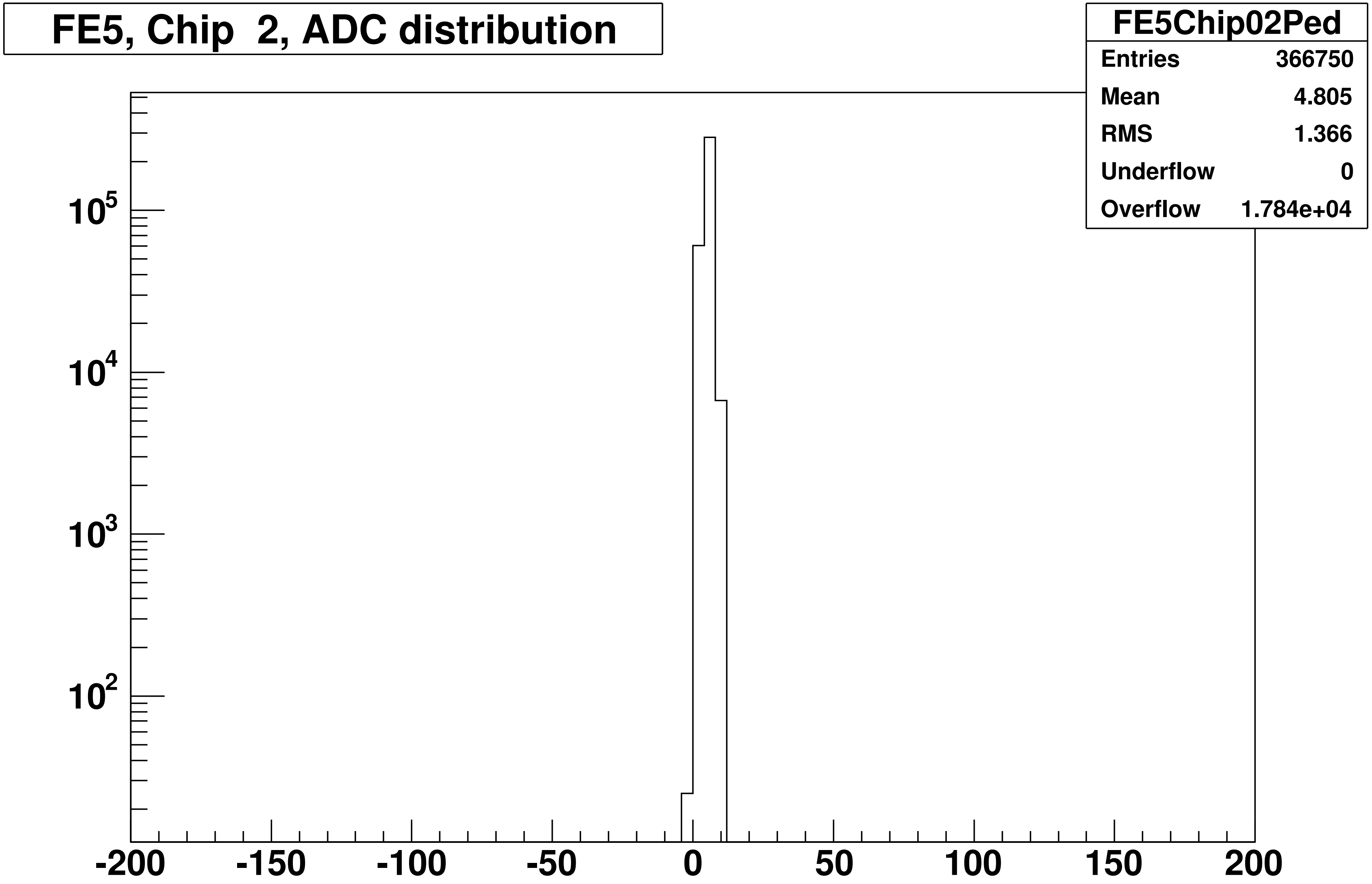
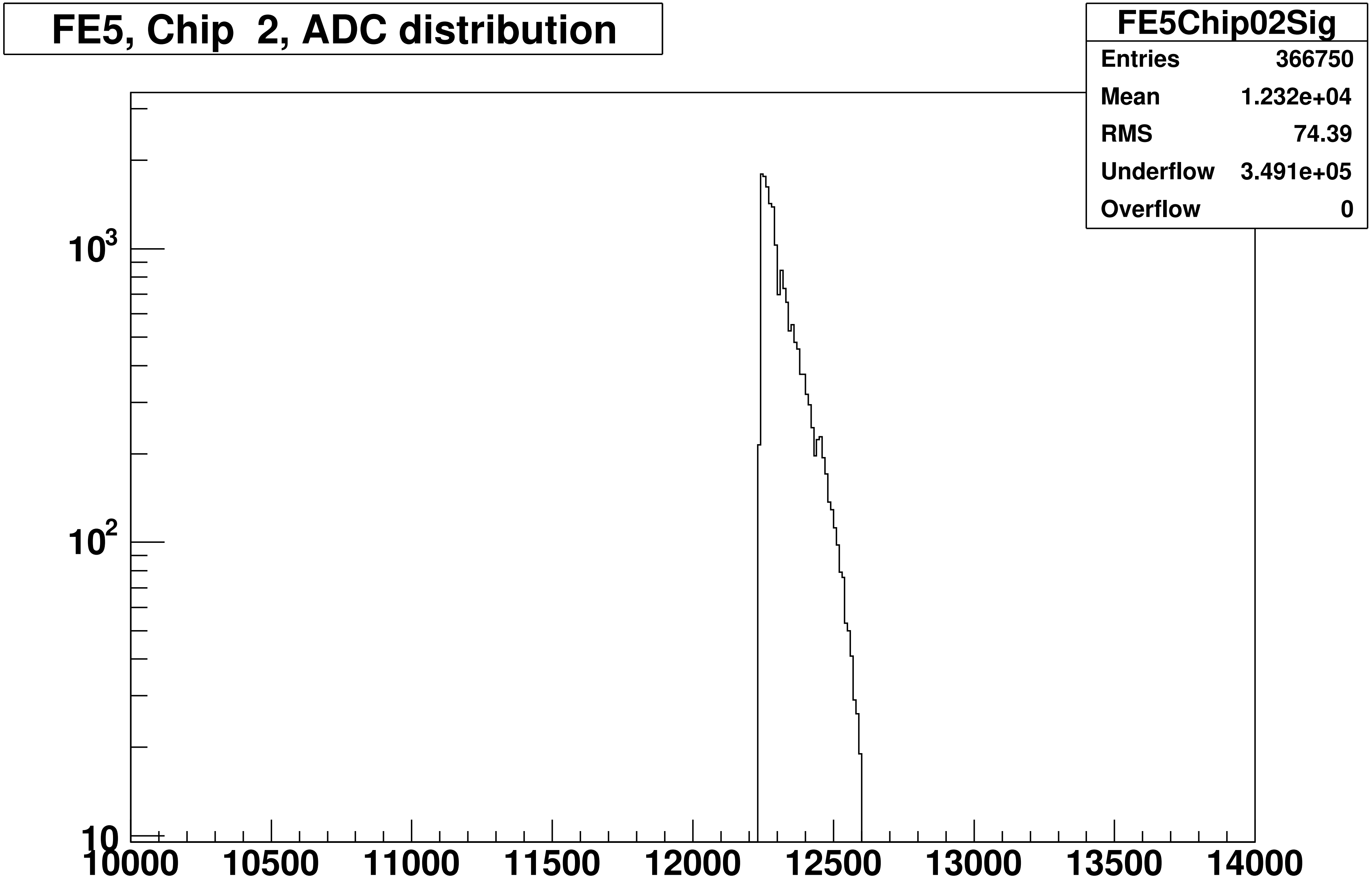
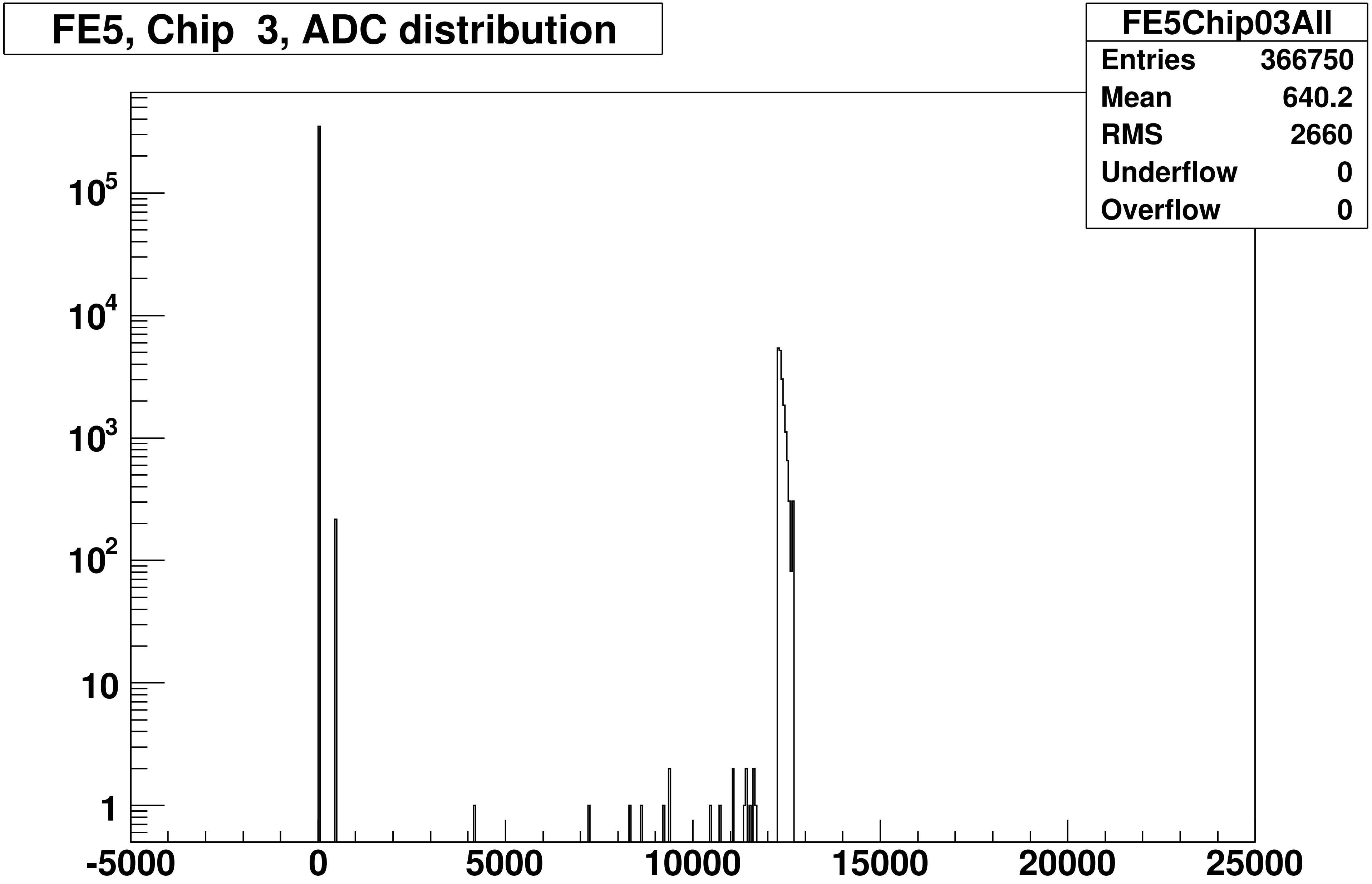
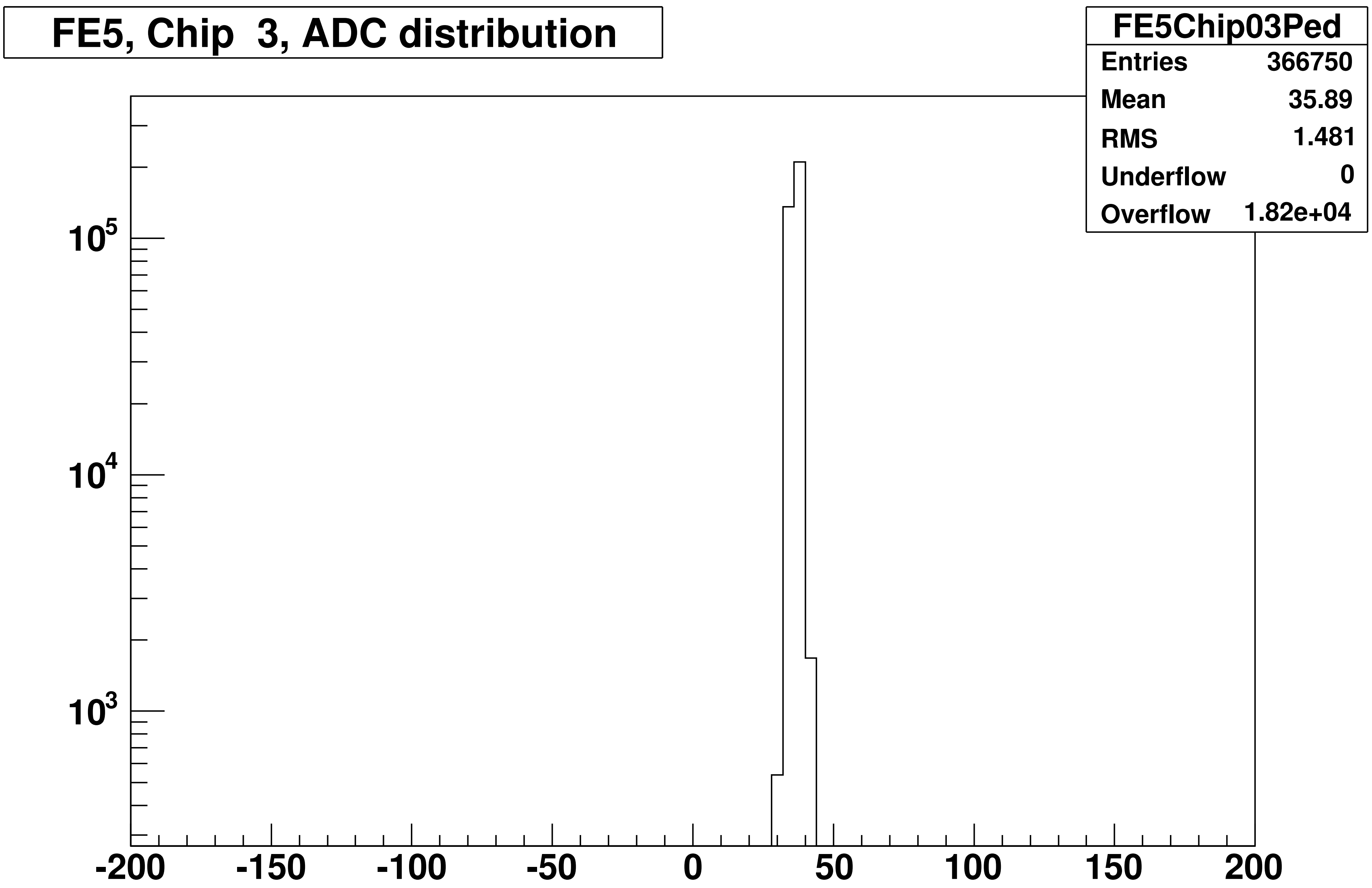
10^2
10
1
10000
10500
11000
11500
12000
12500
13000
13500
14000

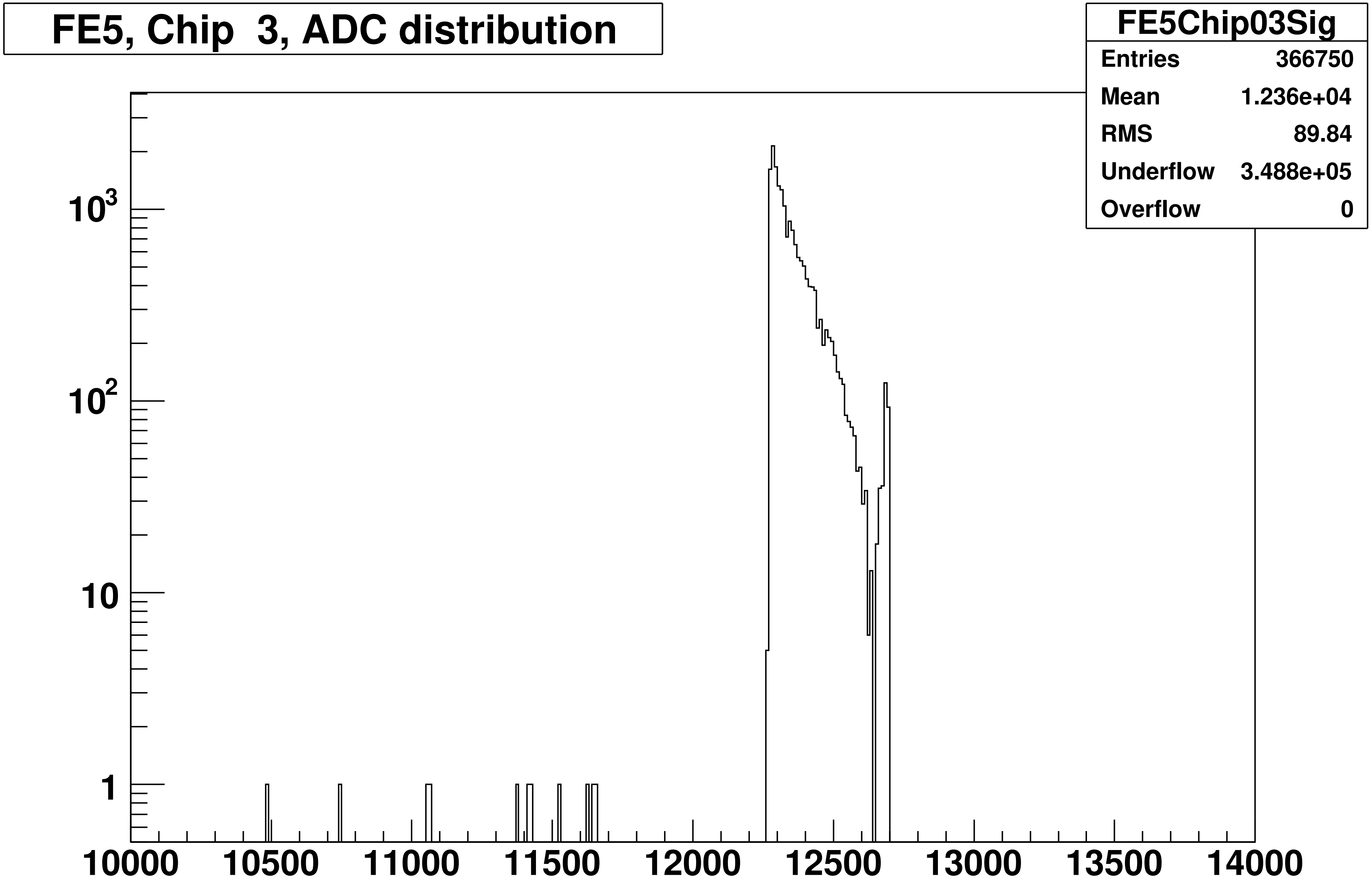

FE5, Chip 2, ADC distribution
FE5Chip02All
Entries 366750
Mean 598.1
RMS 2637
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000

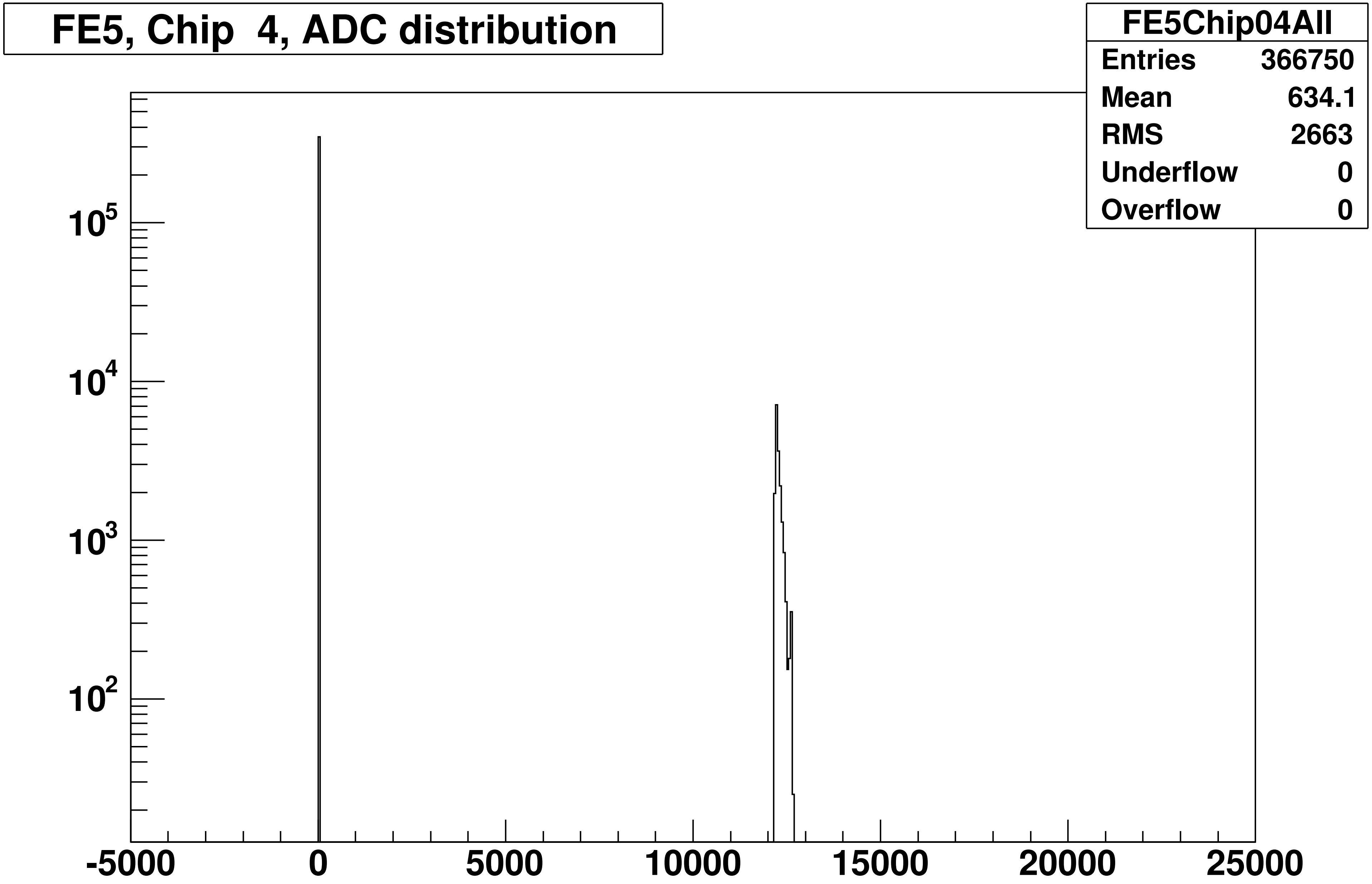

FE5, Chip 2, ADC distribution
FE5Chip02Ped
Entries 366750
Mean 4.805
RMS 1.366
Underflow 0
Overflow 1.784e+04
10^5
10^4
10^3
10^2
-200
-150
-100
-50
0
50
100
150
200

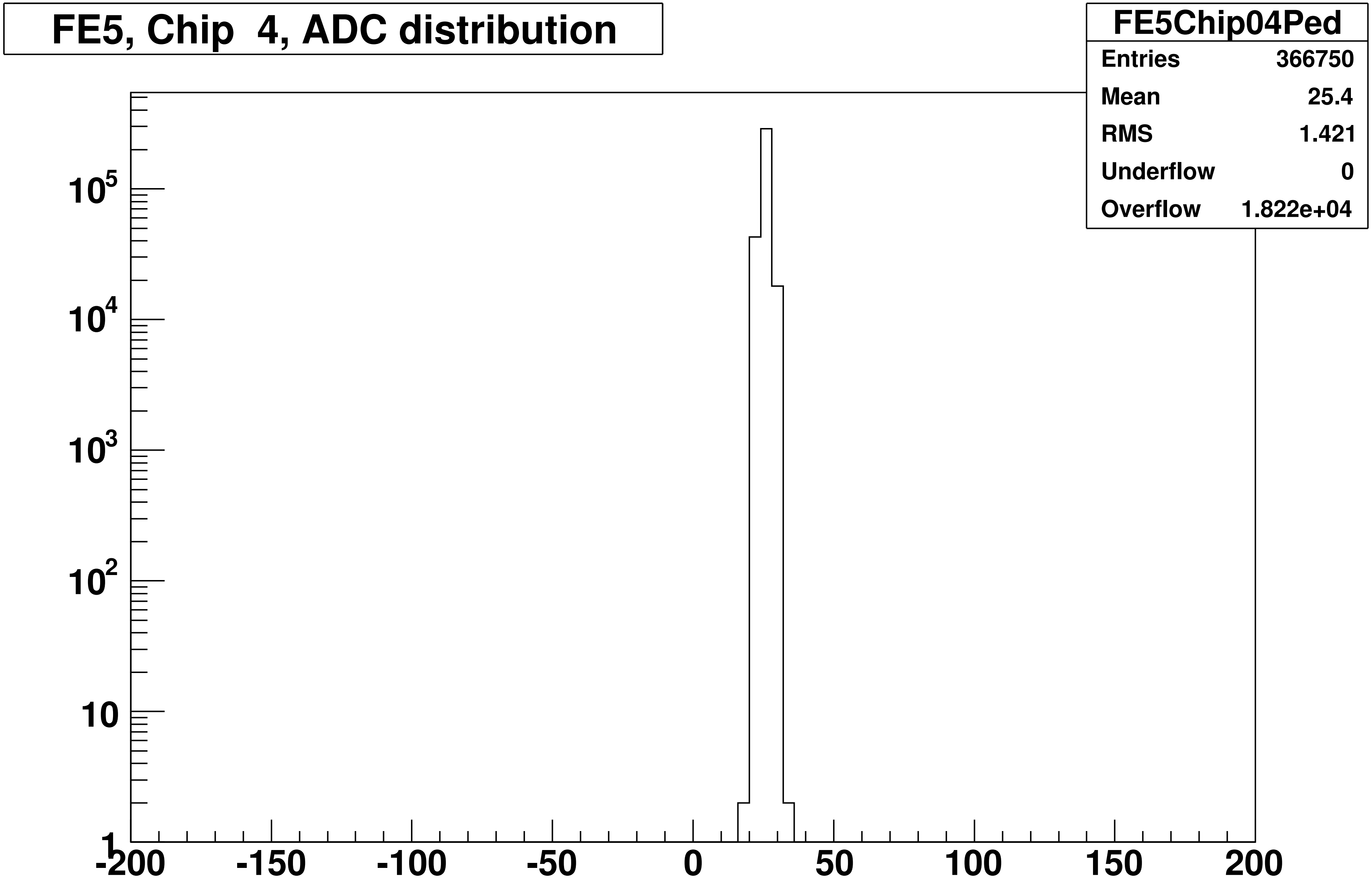

FE5, Chip 2, ADC distribution
FE5Chip02Sig
Entries 366750
Mean 1.232e+04
RMS 74.39
Underflow 3.491e+05
Overflow 0
10^3
10^2
10
10000
10500
11000
11500
12000
12500
13000
13500
14000

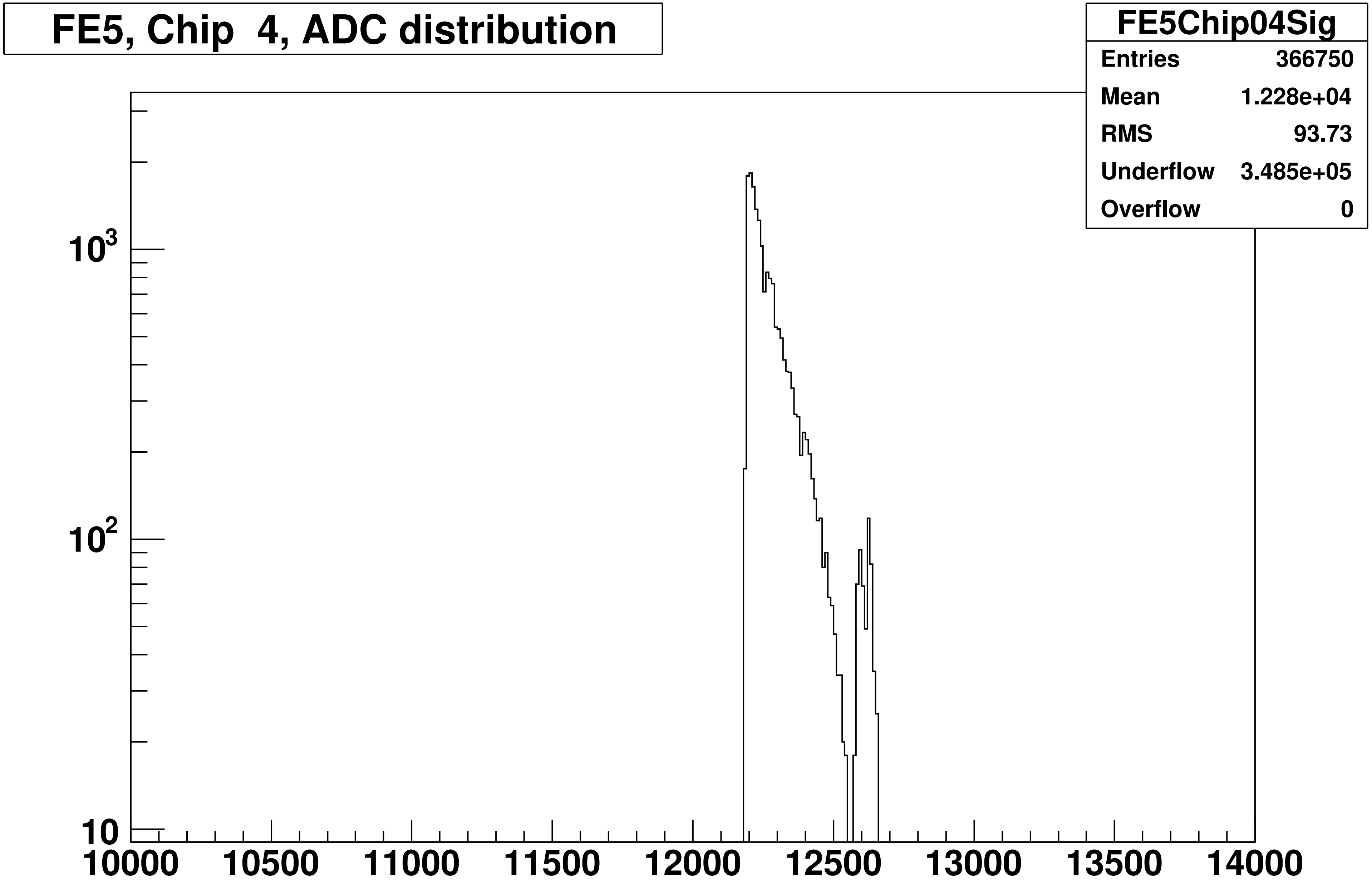

FE5, Chip 3, ADC distribution
FE5Chip03All
Entries 366750
Mean 640.2
RMS 2660
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000

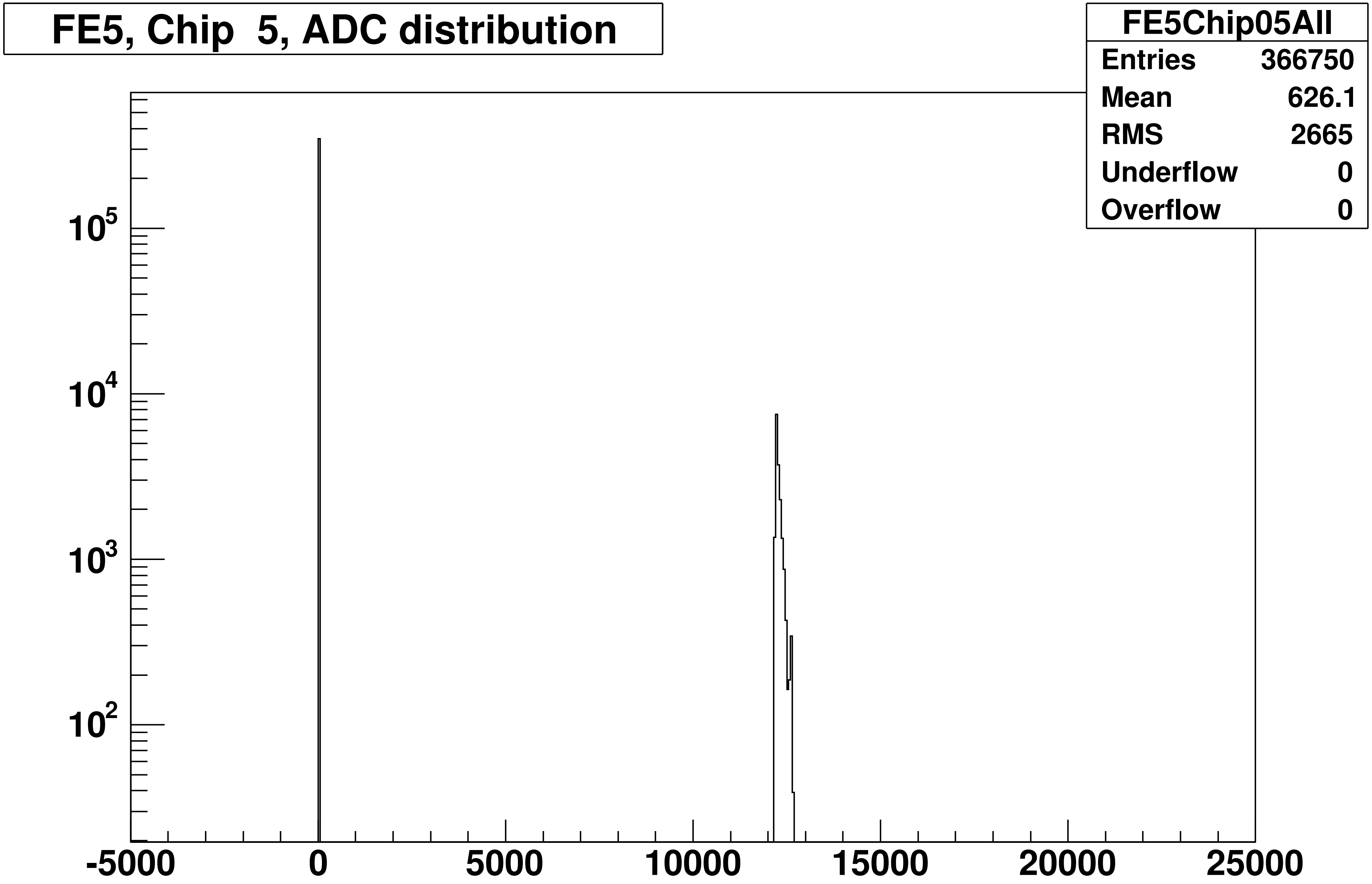

FE5, Chip 3, ADC distribution
FE5Chip03Ped
Entries 366750
Mean 35.89
RMS 1.481
Underflow 0
Overflow 1.82e+04
10^5
10^4
10^3
-200
-150
-100
-50
0
50
100
150
200


FE5, Chip 3, ADC distribution
FE5Chip03Sig
Entries 366750
Mean 1.236e+04
RMS 89.84
Underflow 3.488e+05
Overflow 0
10^3
10^2
10
1
10000
10500
11000
11500
12000
12500
13000
13500
14000

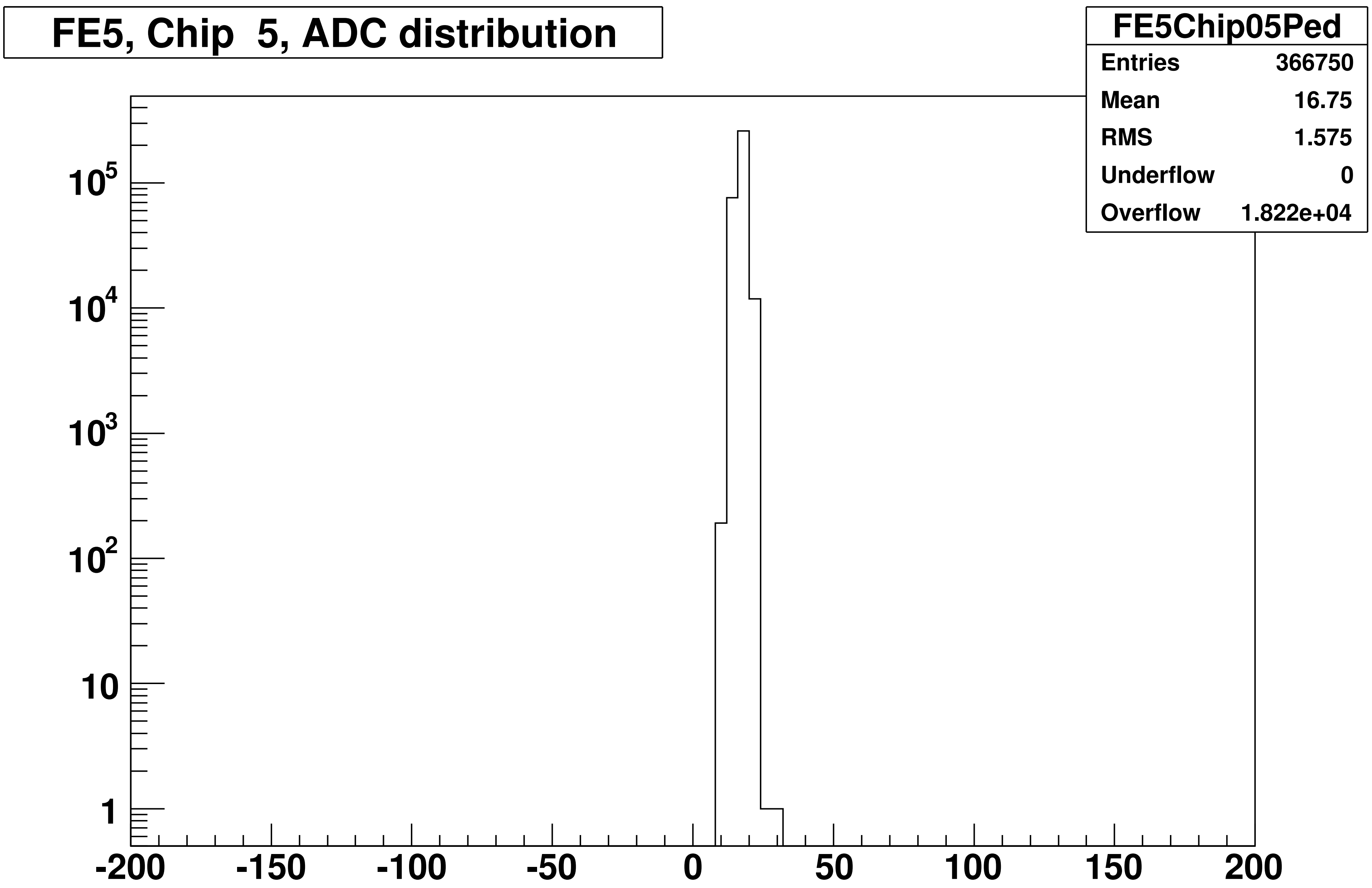

FE5, Chip 4, ADC distribution
FE5Chip04All
Entries 366750
Mean 634.1
RMS 2663
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000

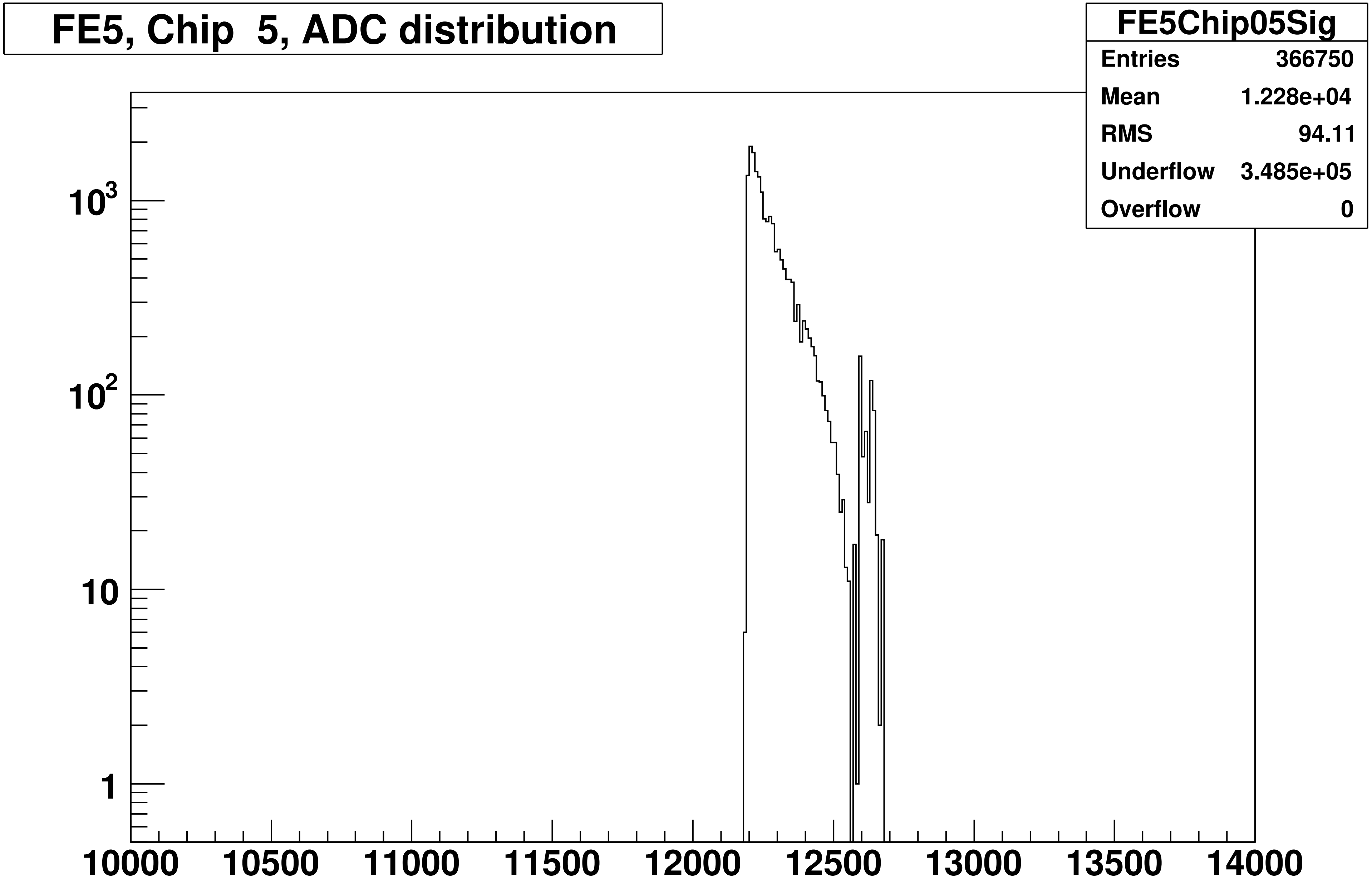

FE5, Chip 4, ADC distribution
FE5Chip04Ped
Entries 366750
Mean 25.4
RMS 1.421
Underflow 0
Overflow 1.822e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
200


FE5, Chip 4, ADC distribution
FE5Chip04Sig
Entries 366750
Mean 1.228e+04
RMS 93.73
Underflow 3.485e+05
Overflow 0
10
10^2
10^3
10000
10500
11000
11500
12000
12500
13000
13500
14000



FE5, Chip 5, ADC distribution
FE5Chip05All
Entries 366750
Mean 626.1
RMS 2665
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000


FE5, Chip 5, ADC distribution
FE5Chip05Ped
Entries 366750
Mean 16.75
RMS 1.575
Underflow 0
Overflow 1.822e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
200


FE5, Chip 5, ADC distribution
FE5Chip05Sig
Entries 366750
Mean 1.228e+04
RMS 94.11
Underflow 3.485e+05
Overflow 0
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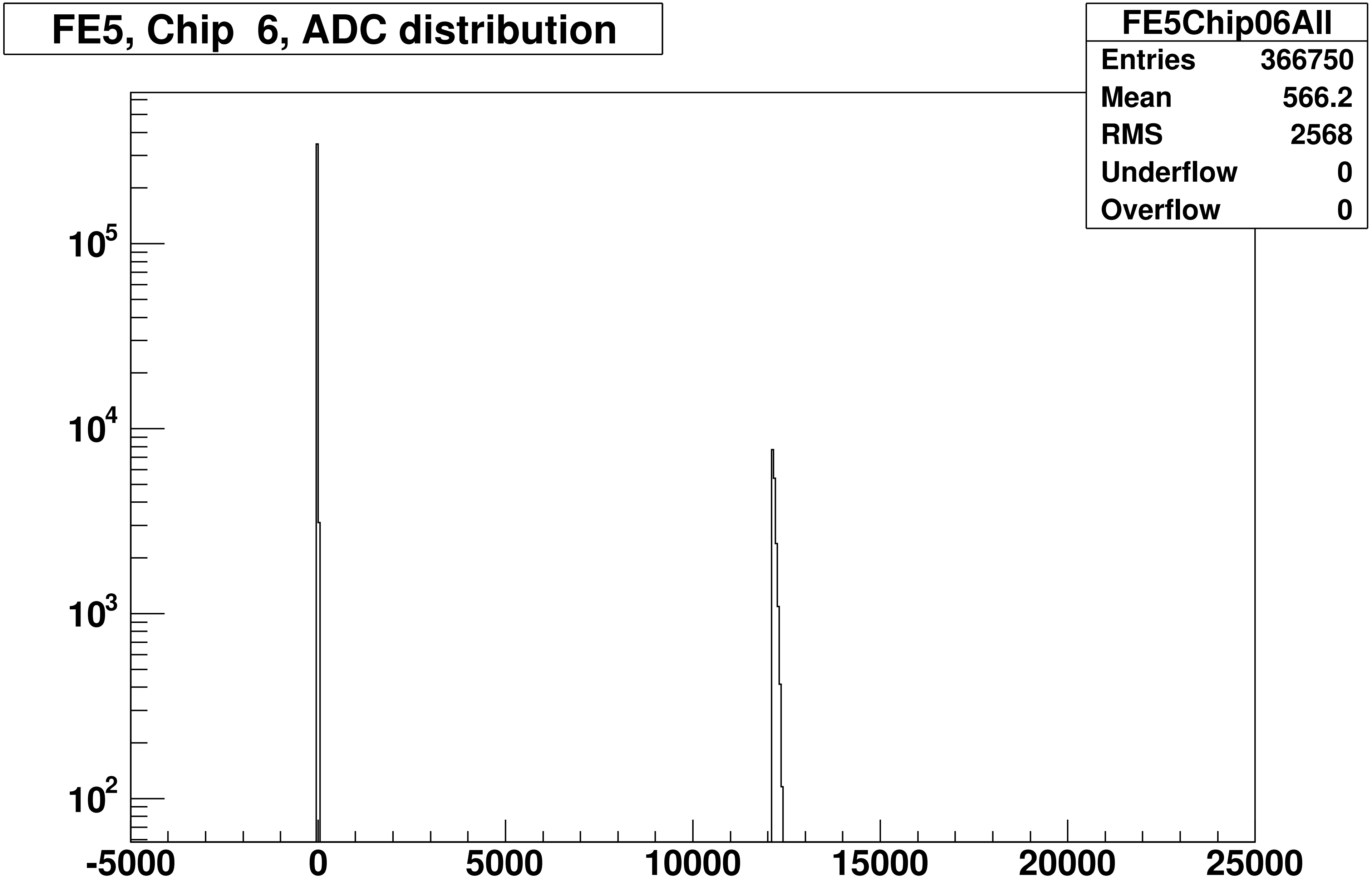
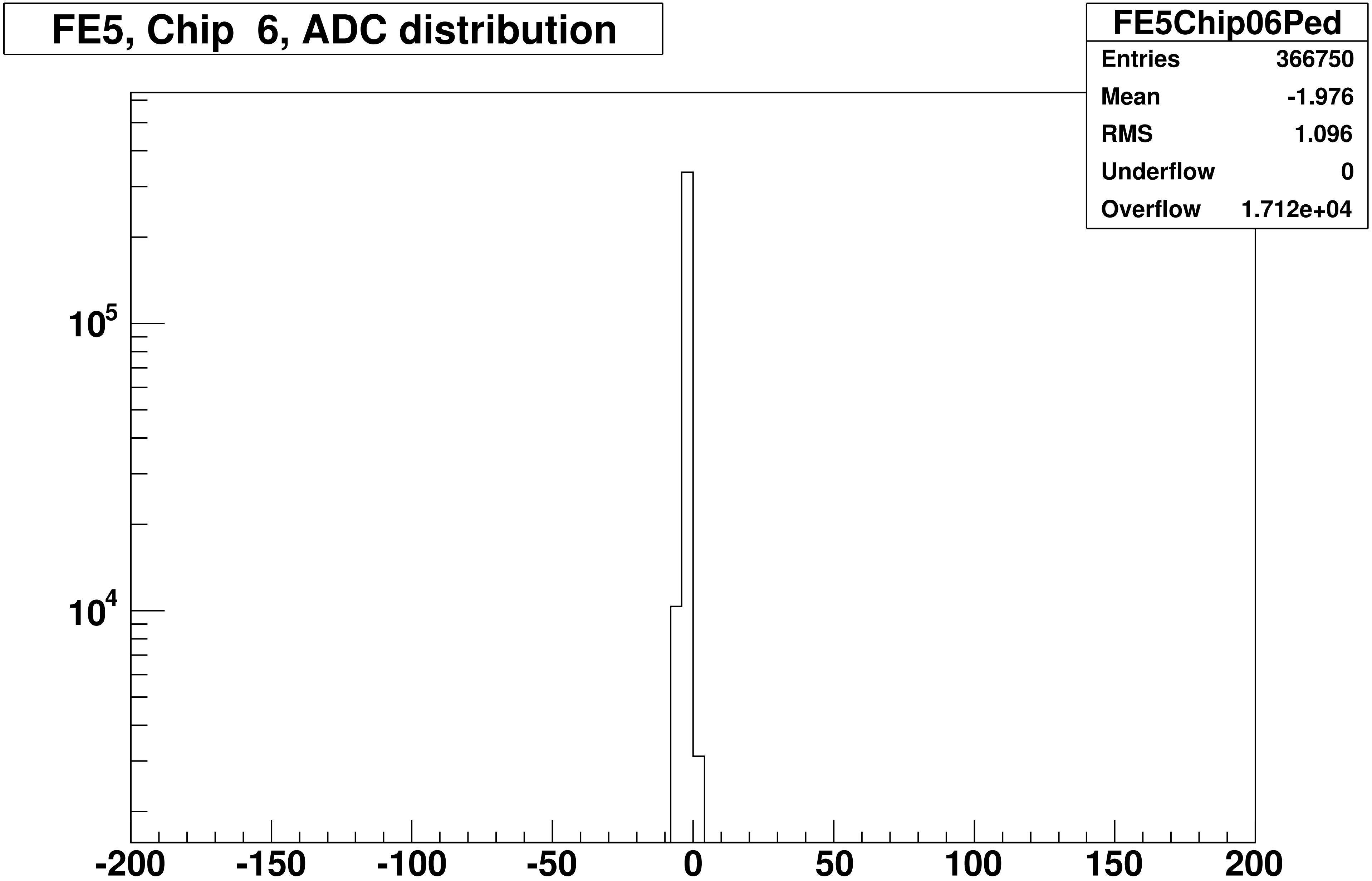
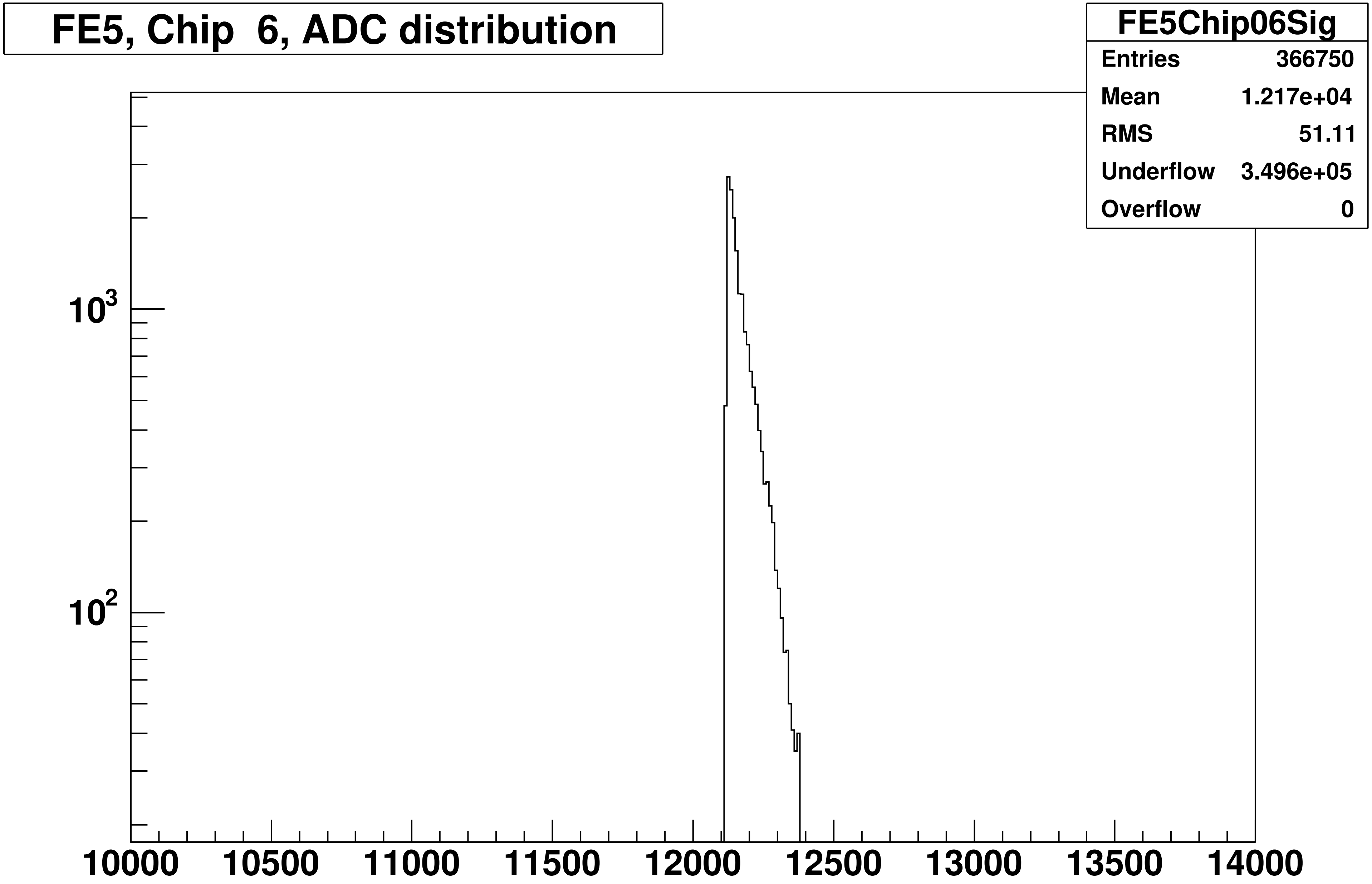
10500
11000
11500
12000
12500
13000
13500
14000
1
10
10^2
10^3

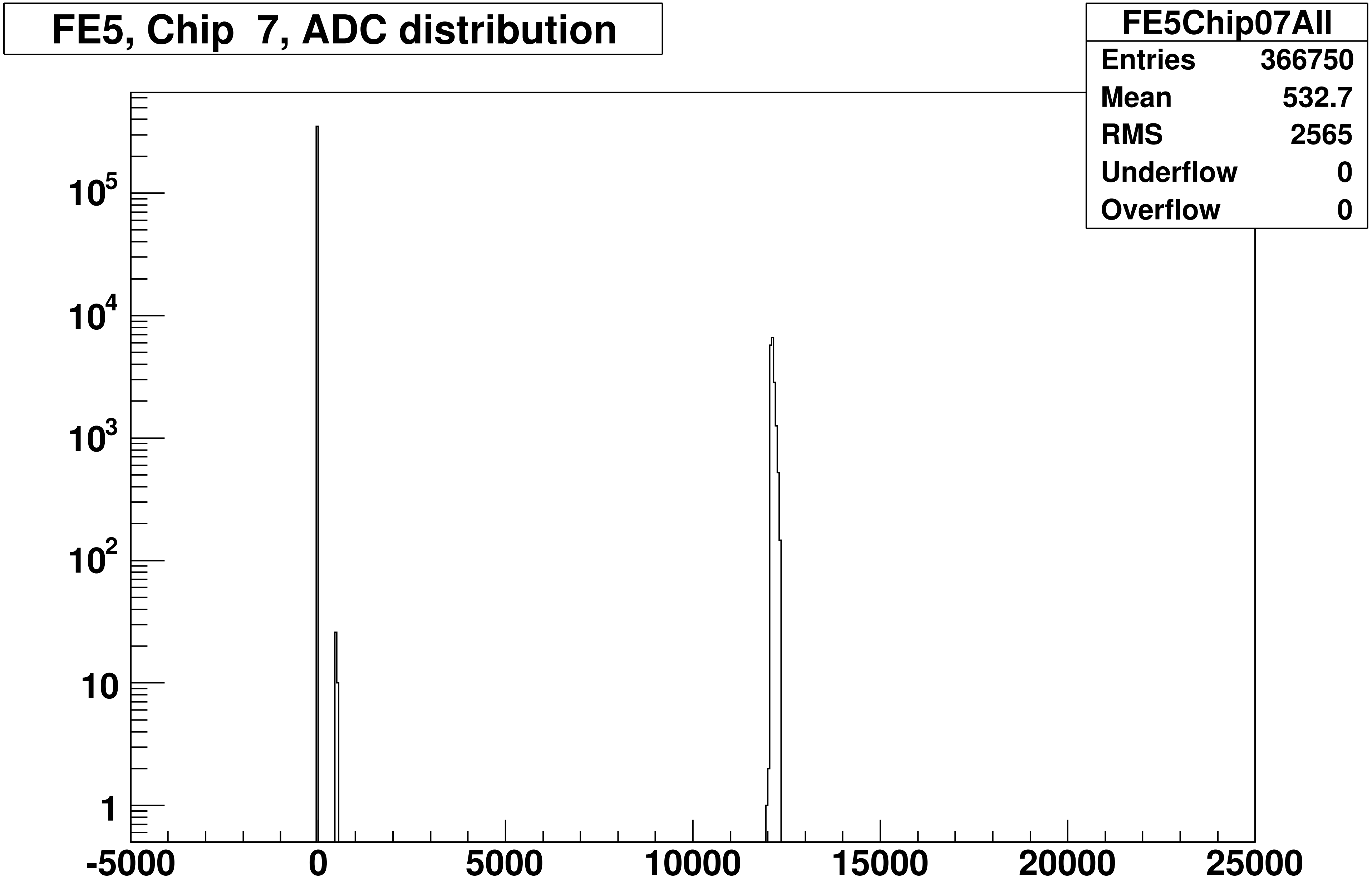


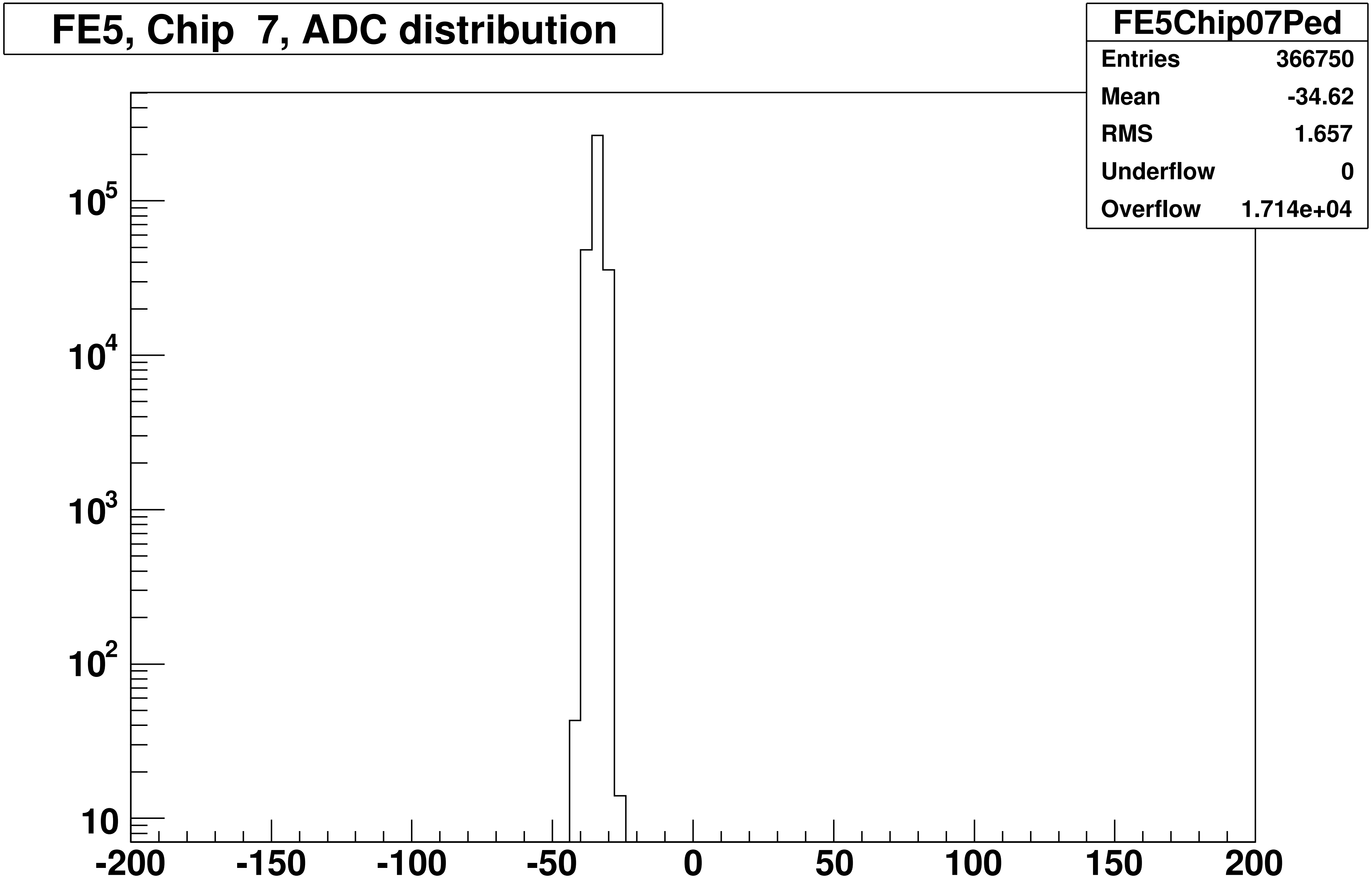
FE5, Chip 6, ADC distribution
FE5Chip06All
Entries 366750
Mean 566.2
RMS 2568
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000



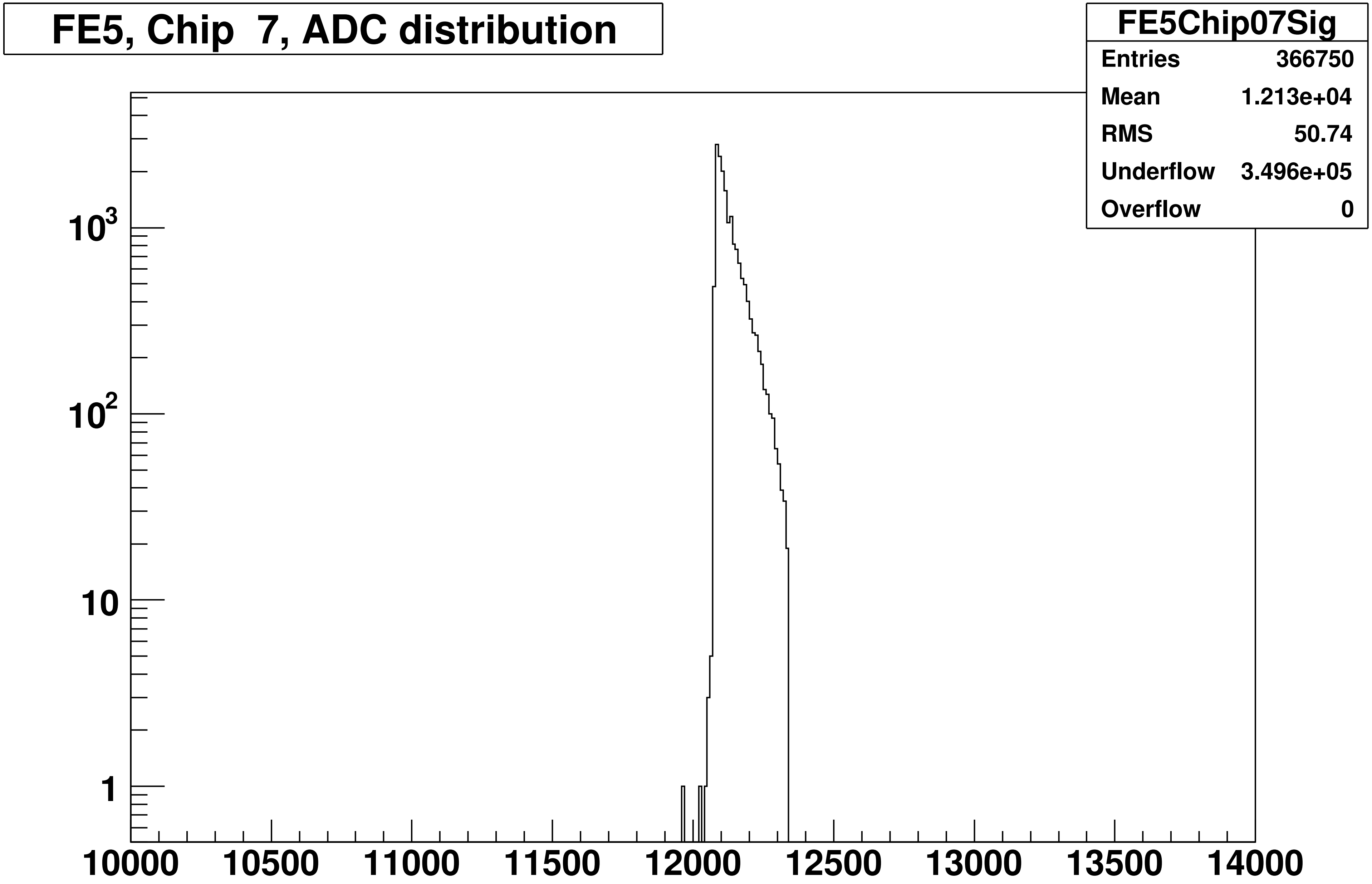
FE5, Chip 6, ADC distribution
FE5Chip06Ped
Entries 366750
Mean -1.976
RMS 1.096
Underflow 0
Overflow 1.712e+04
10^5
10^4
-200
-150
-100
-50
0
50
100
150
200


FE5, Chip 6, ADC distribution
FE5Chip06Sig
Entries 366750
Mean 1.217e+04
RMS 51.11
Underflow 3.496e+05
Overflow 0
10^3
10^2
10000
10500
11000
11500
12000
12500
13000
13500
14000


FE5, Chip 7, ADC distribution
FE5Chip07All
Entries 366750
Mean 532.7
RMS 2565
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE5, Chip 7, ADC distribution
FE5Chip07Ped
Entries 366750
Mean -34.62
RMS 1.657
Underflow 0
Overflow 1.714e+04
10
10^2
10^3
10^4
10^5
-200
-150
-100
-50
0
50
100
150
200


FE5, Chip 7, ADC distribution
FE5Chip07Sig
Entries 366750
Mean 1.213e+04
RMS 50.74
Underflow 3.496e+05
Overflow 0
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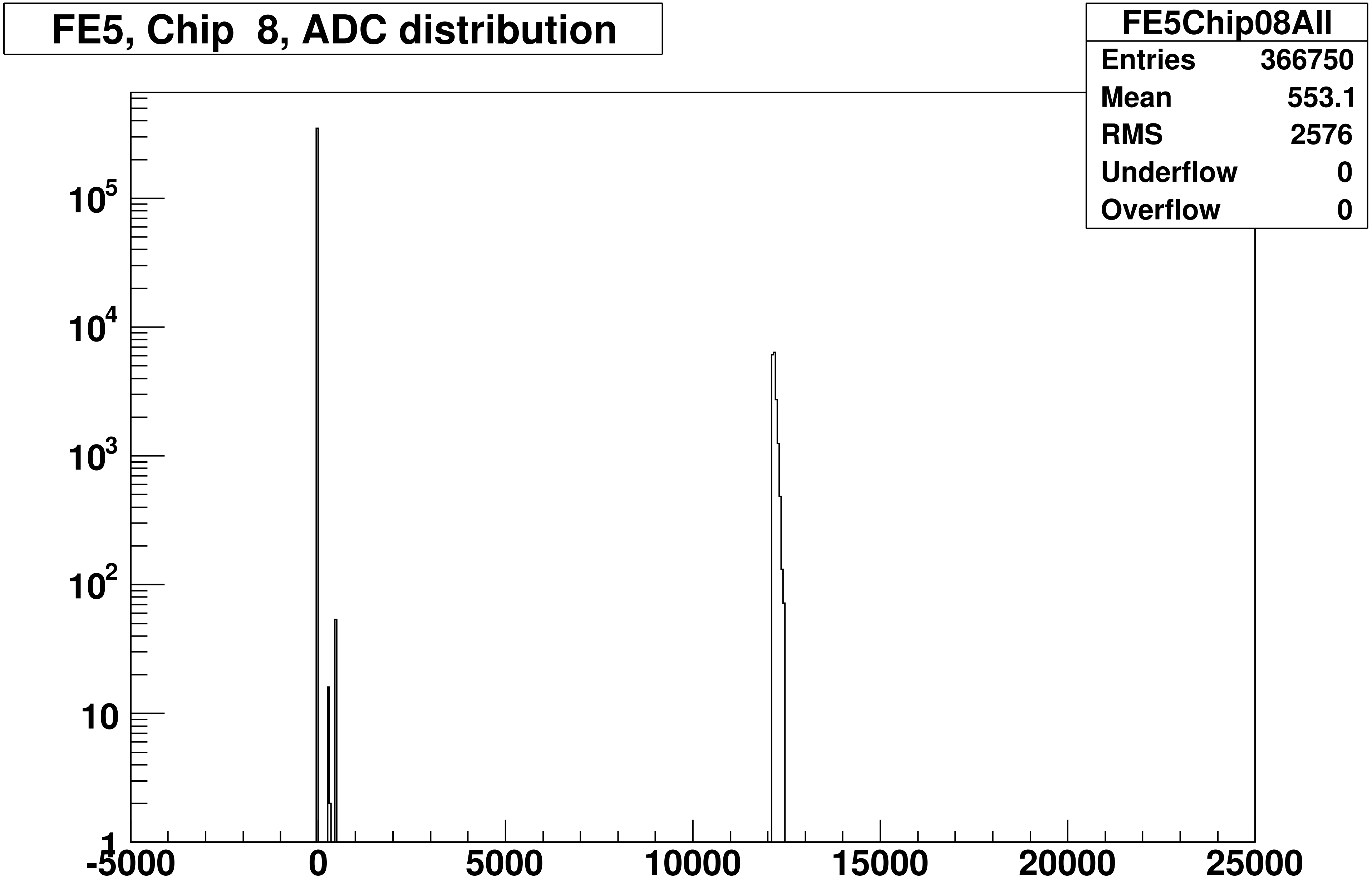
10^2
10
1
10000
10500
11000
11500
12000
12500
13000
13500
14000


FE5, Chip 8, ADC distribution
FE5Chip08All
Entries 366750
Mean 553.1
RMS 2576
Underflow 0
Overflow 0
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10
10^2
10^3
10^4
10^5
-5000
0
5000
10000
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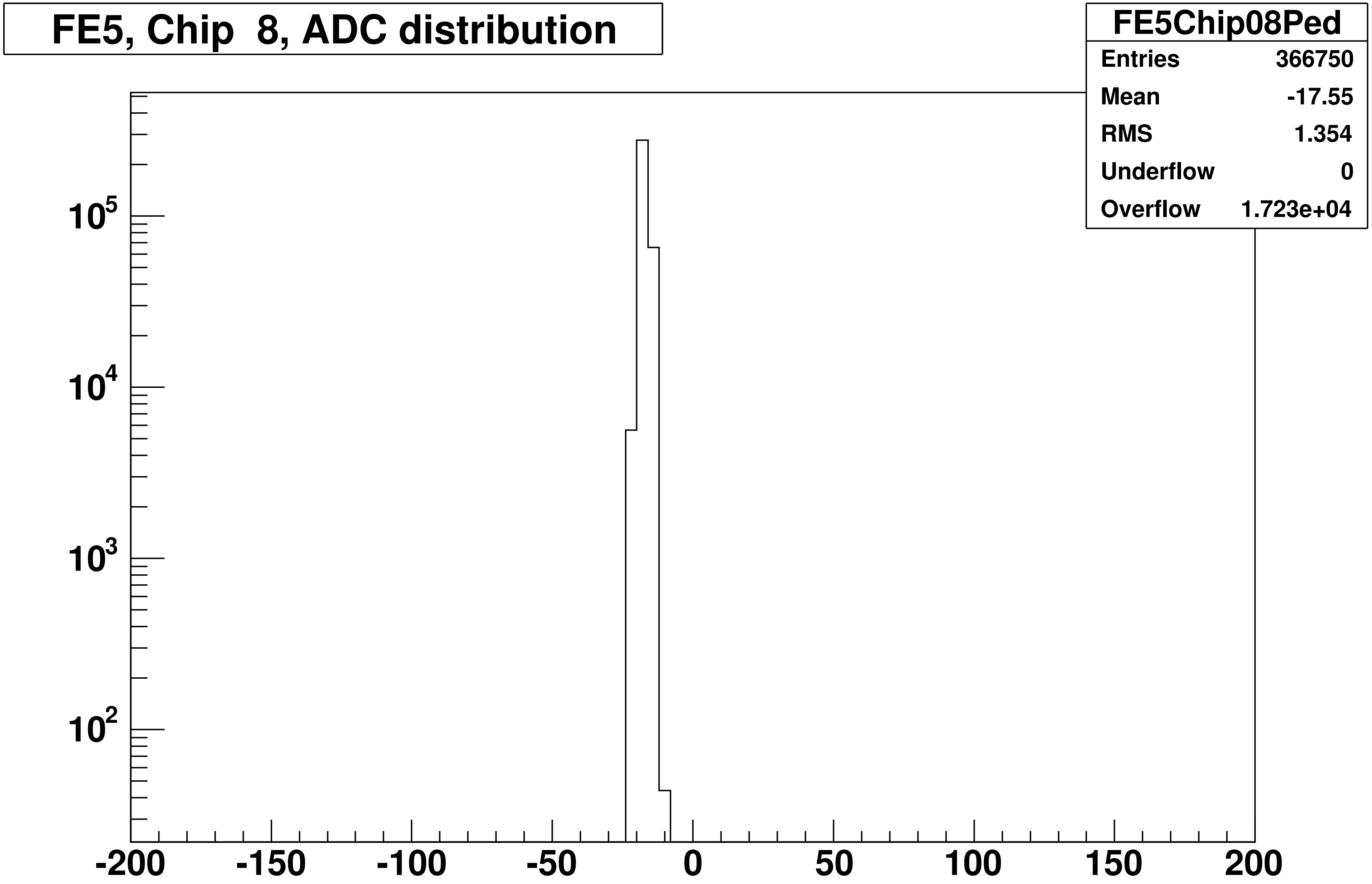
20000
25000



FE5, Chip 8, ADC distribution
FE5Chip08Ped
Entries 366750
Mean -17.55
RMS 1.354
Underflow 0
Overflow 1.723e+04
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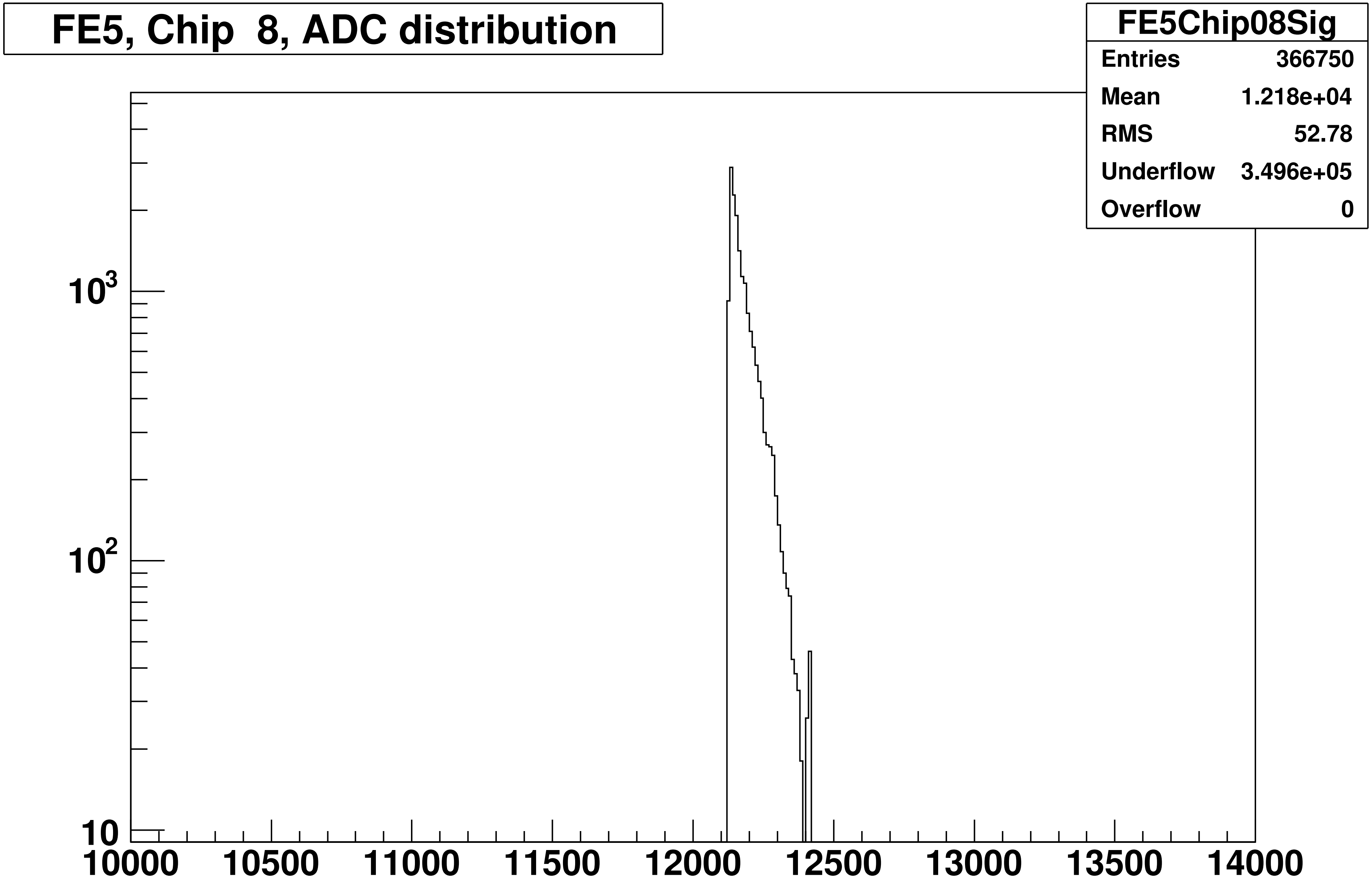
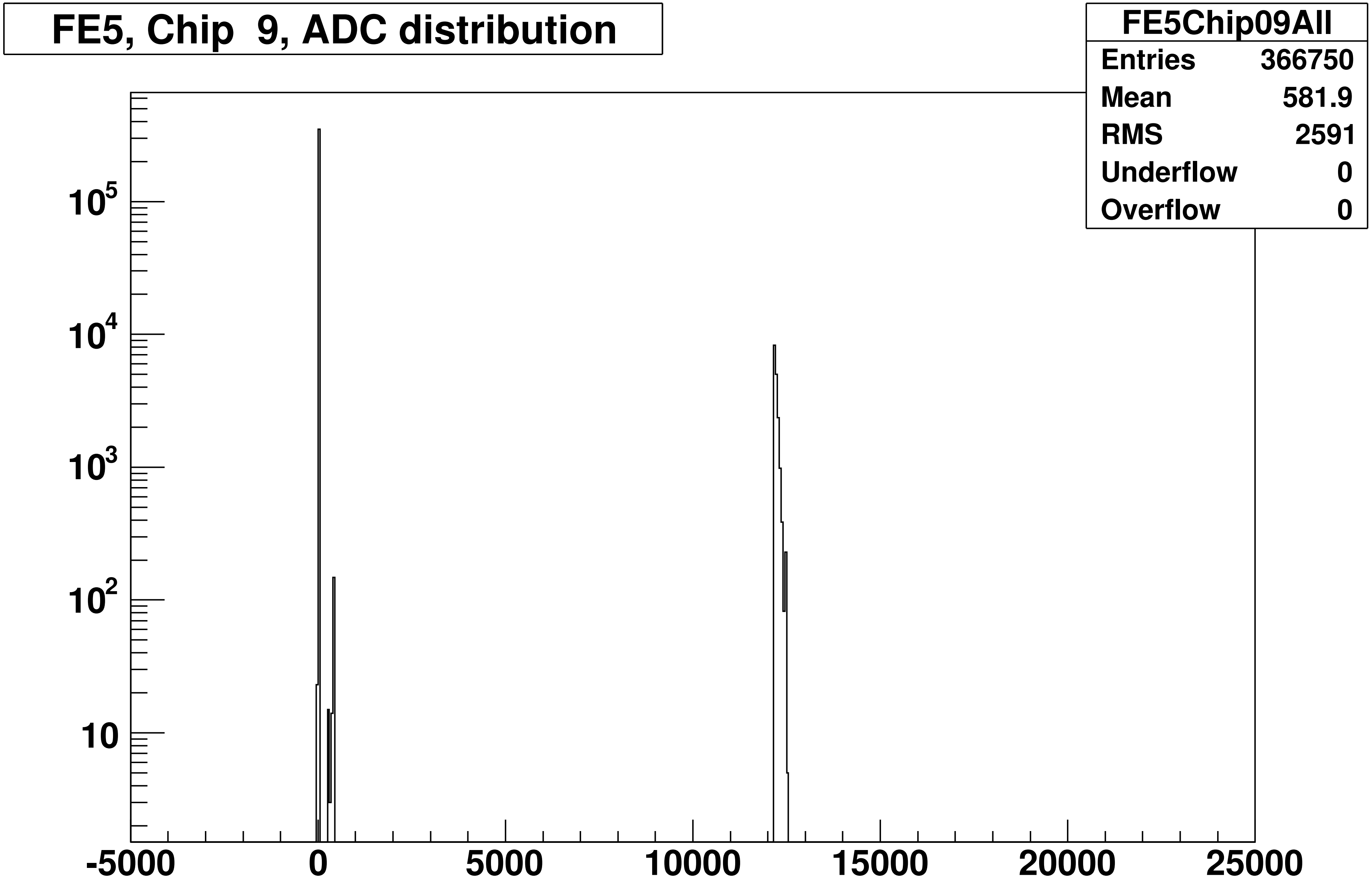
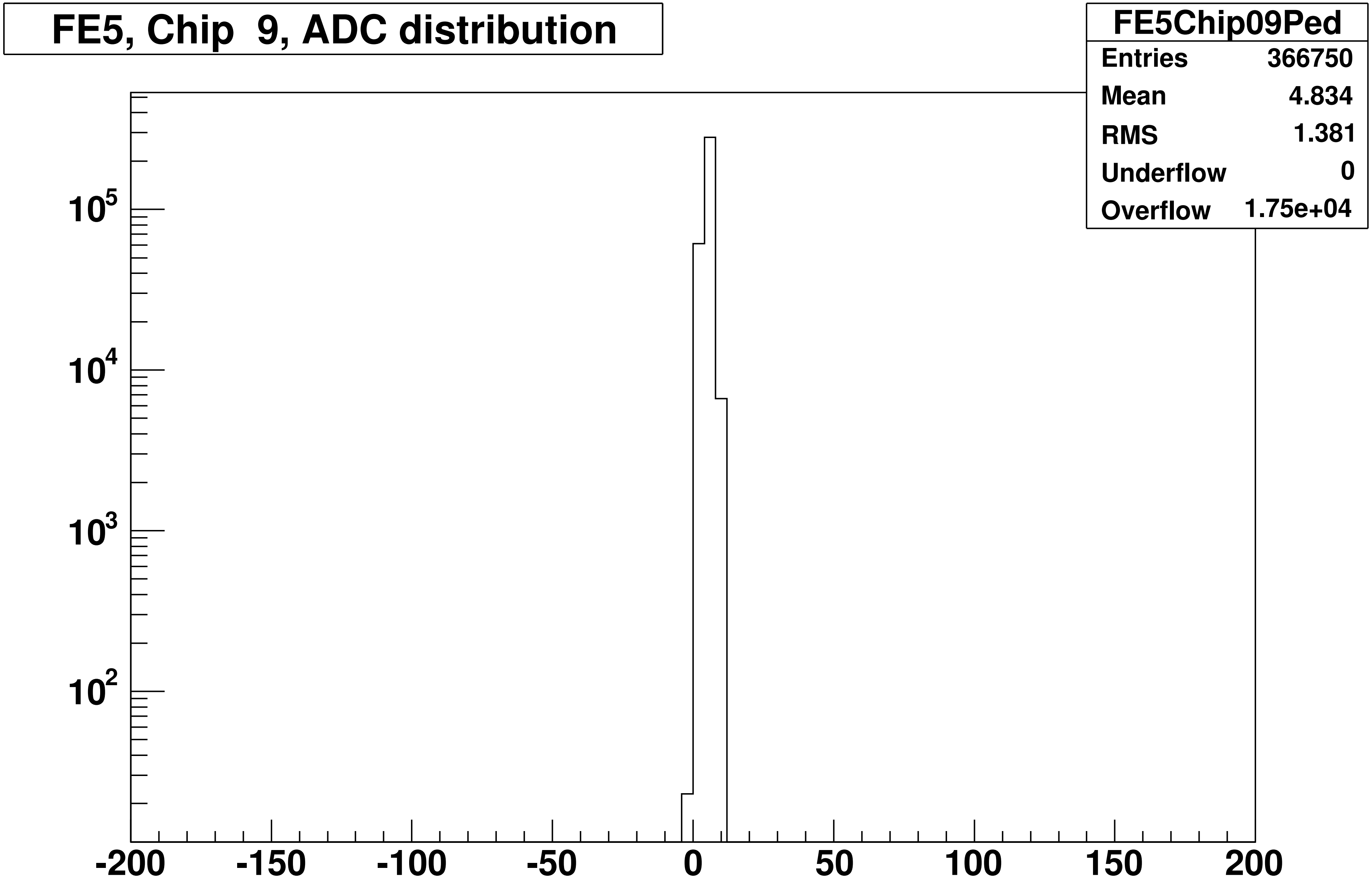
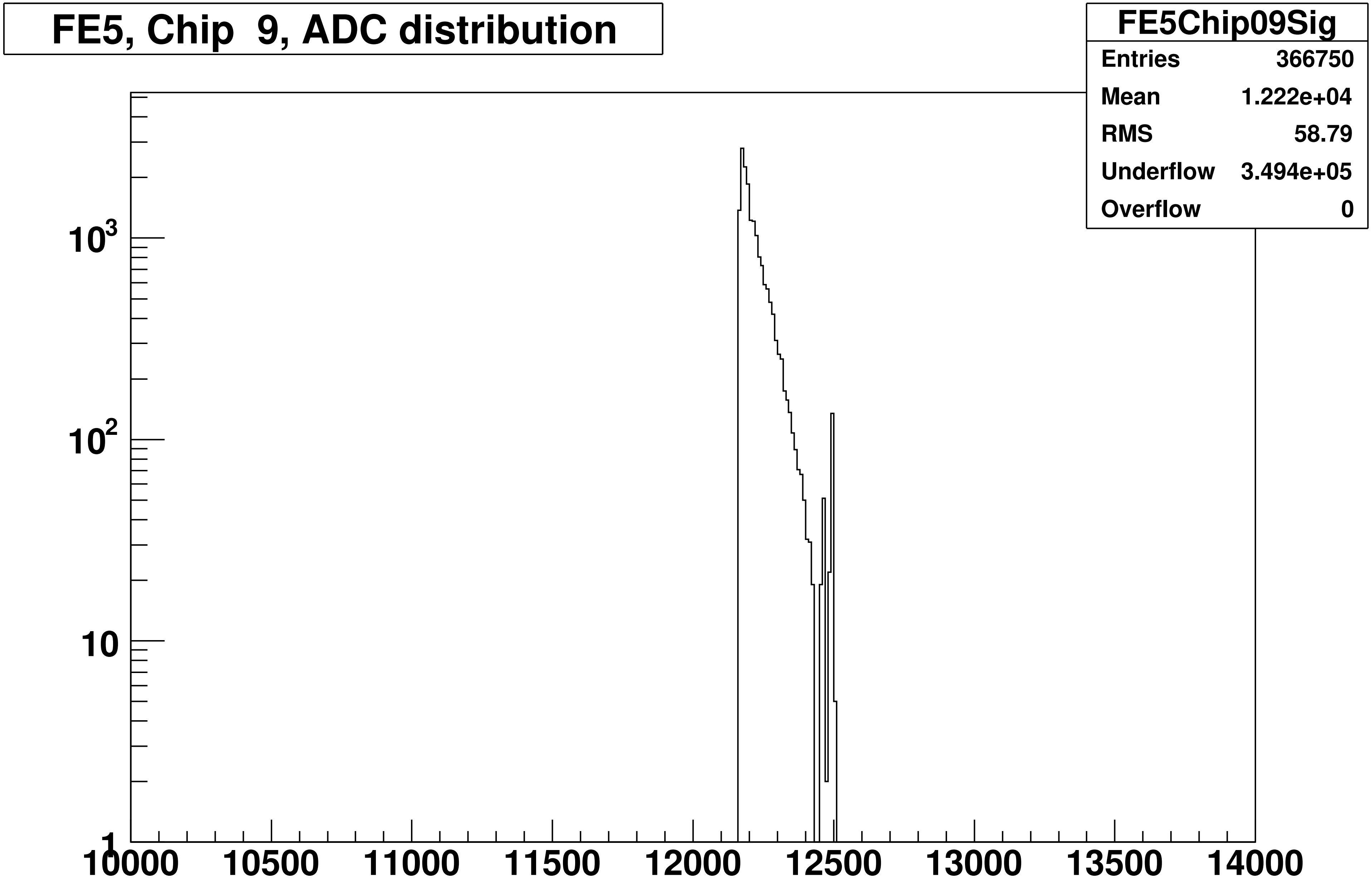
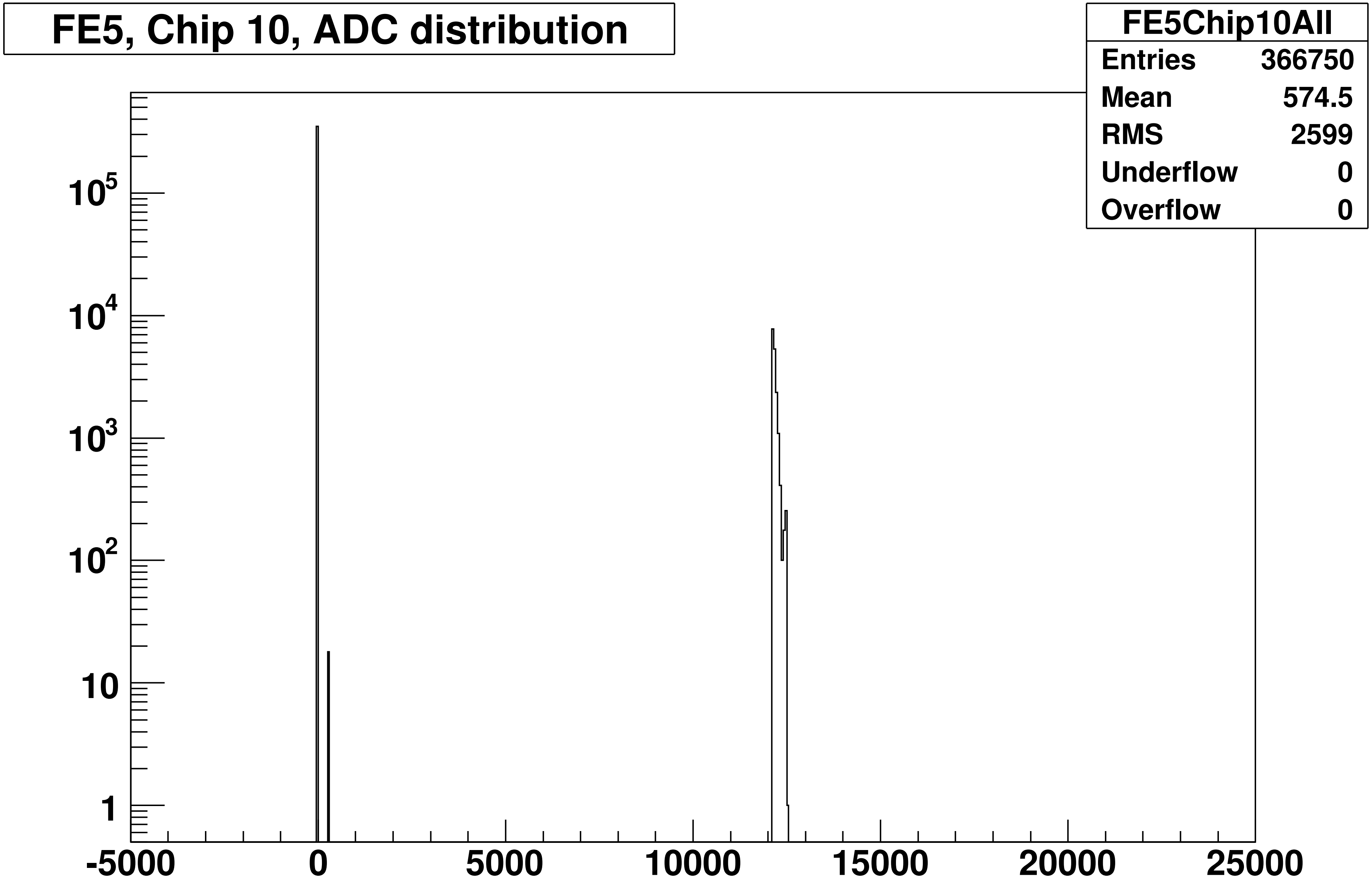
10^4
10^3
10^2
-200
-150
-100
-50
0
50
100
150
200

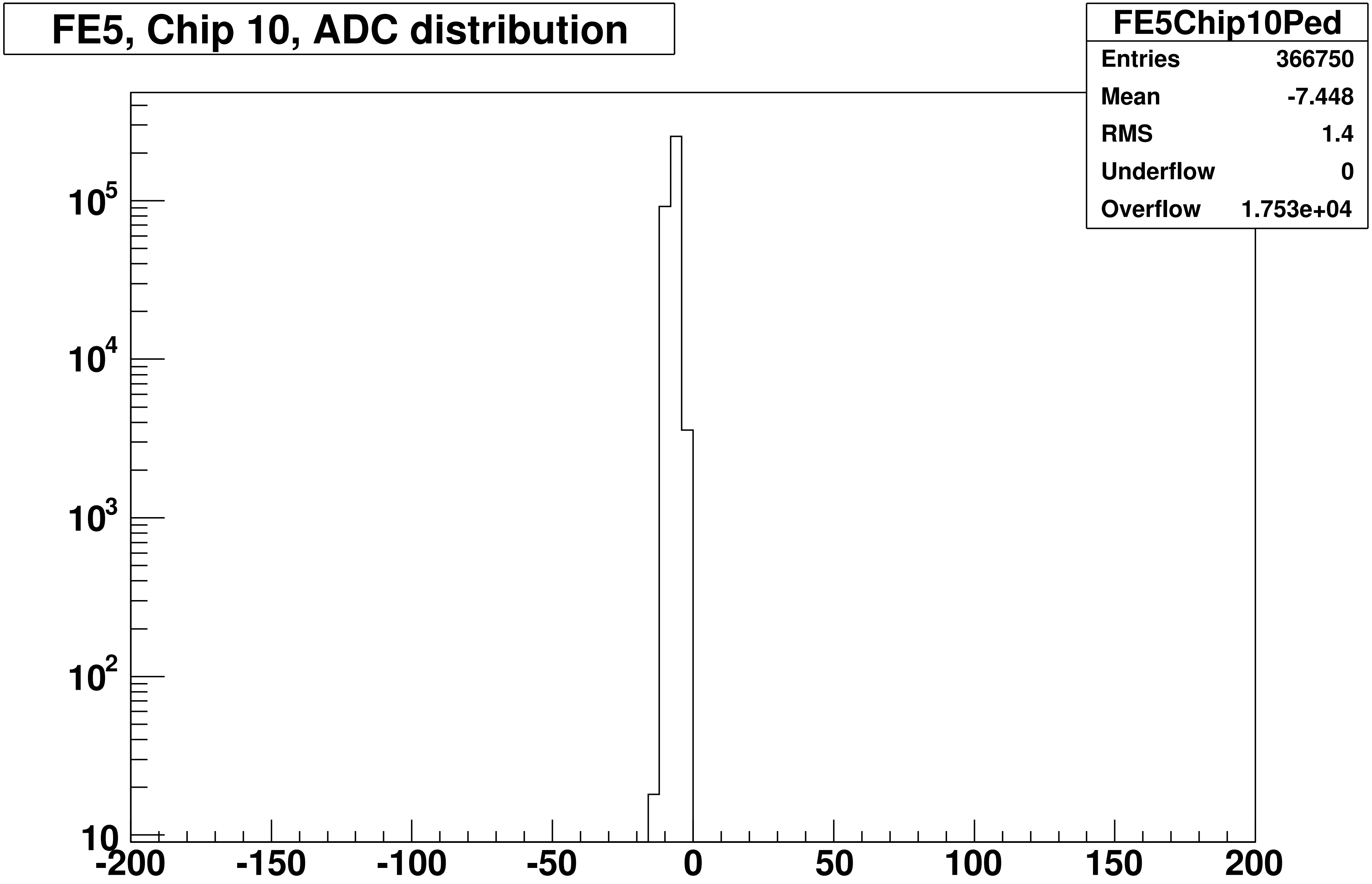

FE5, Chip 8, ADC distribution
FE5Chip08Sig
Entries 366750
Mean 1.218e+04
RMS 52.78
Underflow 3.496e+05
Overflow 0
10
10^2
10^3
10000
10500
11000
11500
12000
12500
13000
13500
14000

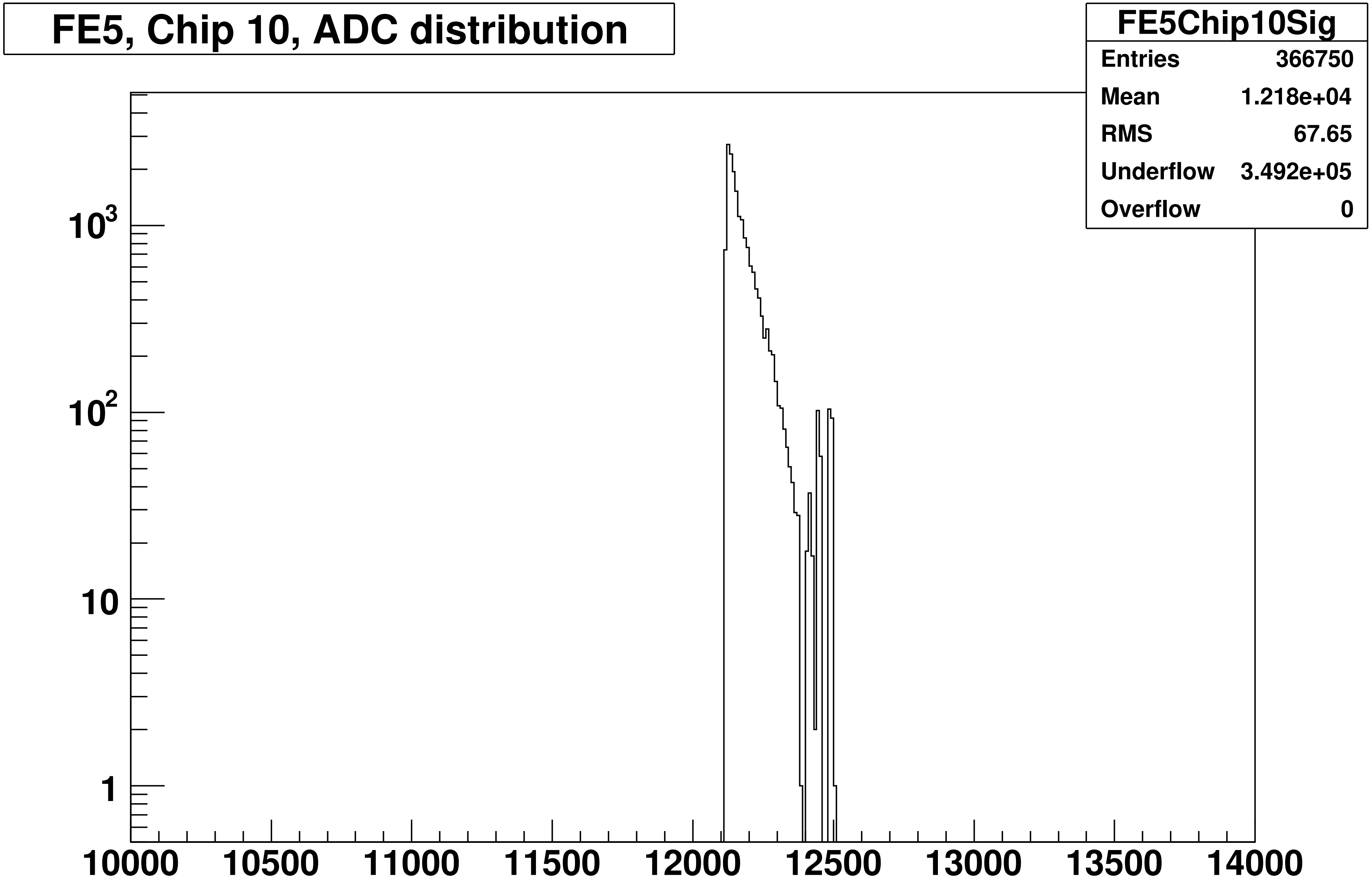

FE5, Chip 9, ADC distribution
FE5Chip09All
Entries 366750
Mean 581.9
RMS 2591
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000

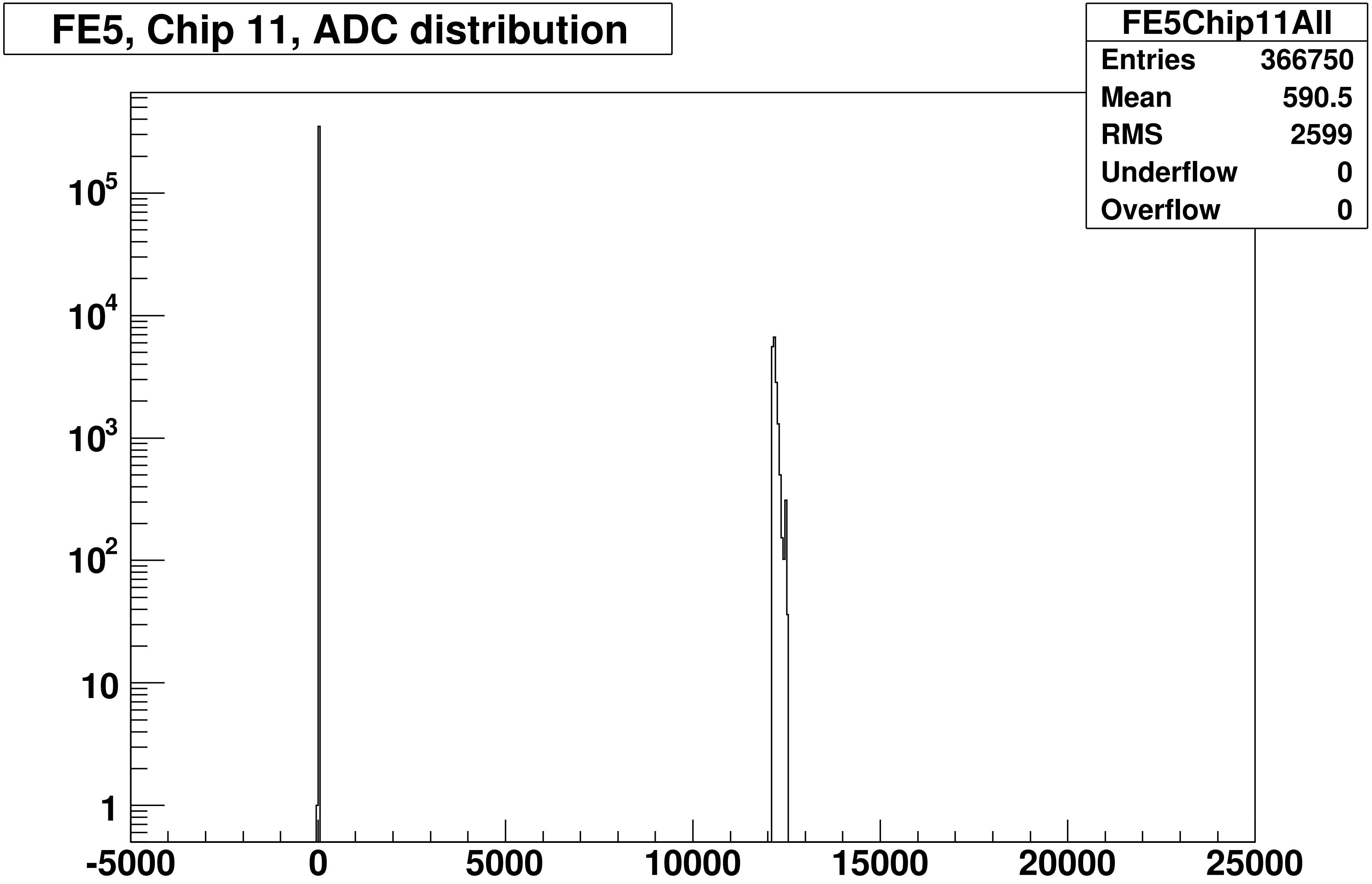

FE5, Chip 9, ADC distribution
FE5Chip09Ped
Entries 366750
Mean 4.834
RMS 1.381
Underflow 0
Overflow 1.75e+04
10^5
10^4
10^3
10^2
-200
-150
-100
-50
0
50
100
150
200


FE5, Chip 9, ADC distribution
FE5Chip09Sig
Entries 366750
Mean 1.222e+04
RMS 58.79
Underflow 3.494e+05
Overflow 0
10^3
10^2
10
1
10000
10500
11000
11500
12000
12500
13000
13500
14000

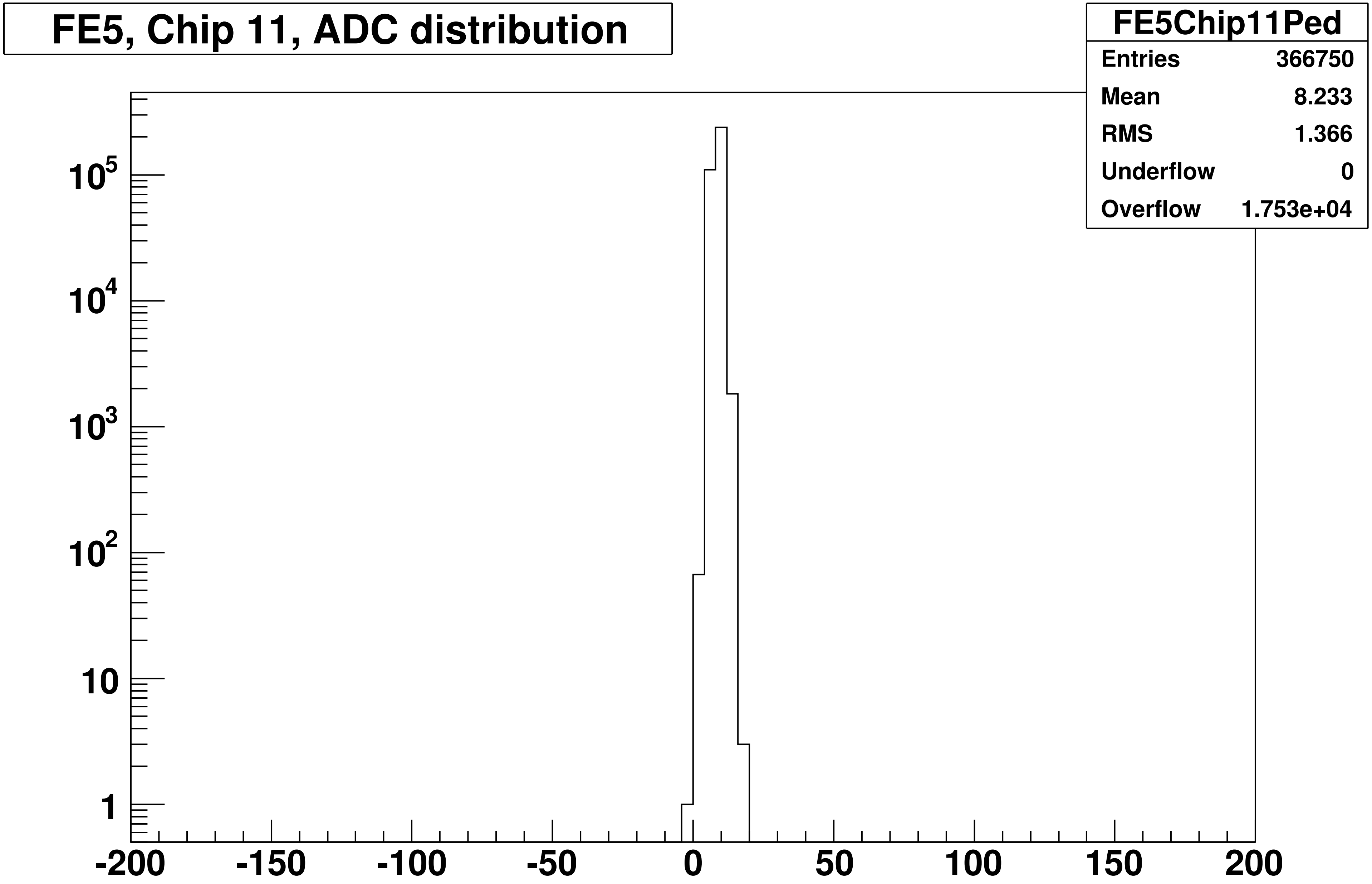

FE5, Chip 10, ADC distribution
FE5Chip10All
Entries 366750
Mean 574.5
RMS 2599
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE5, Chip 10, ADC distribution
FE5Chip10Ped
Entries 366750
Mean -7.448
RMS 1.4
Underflow 0
Overflow 1.753e+04
10
10^2
10^3
10^4
10^5
-200
-150
-100
-50
0
50
100
150
200

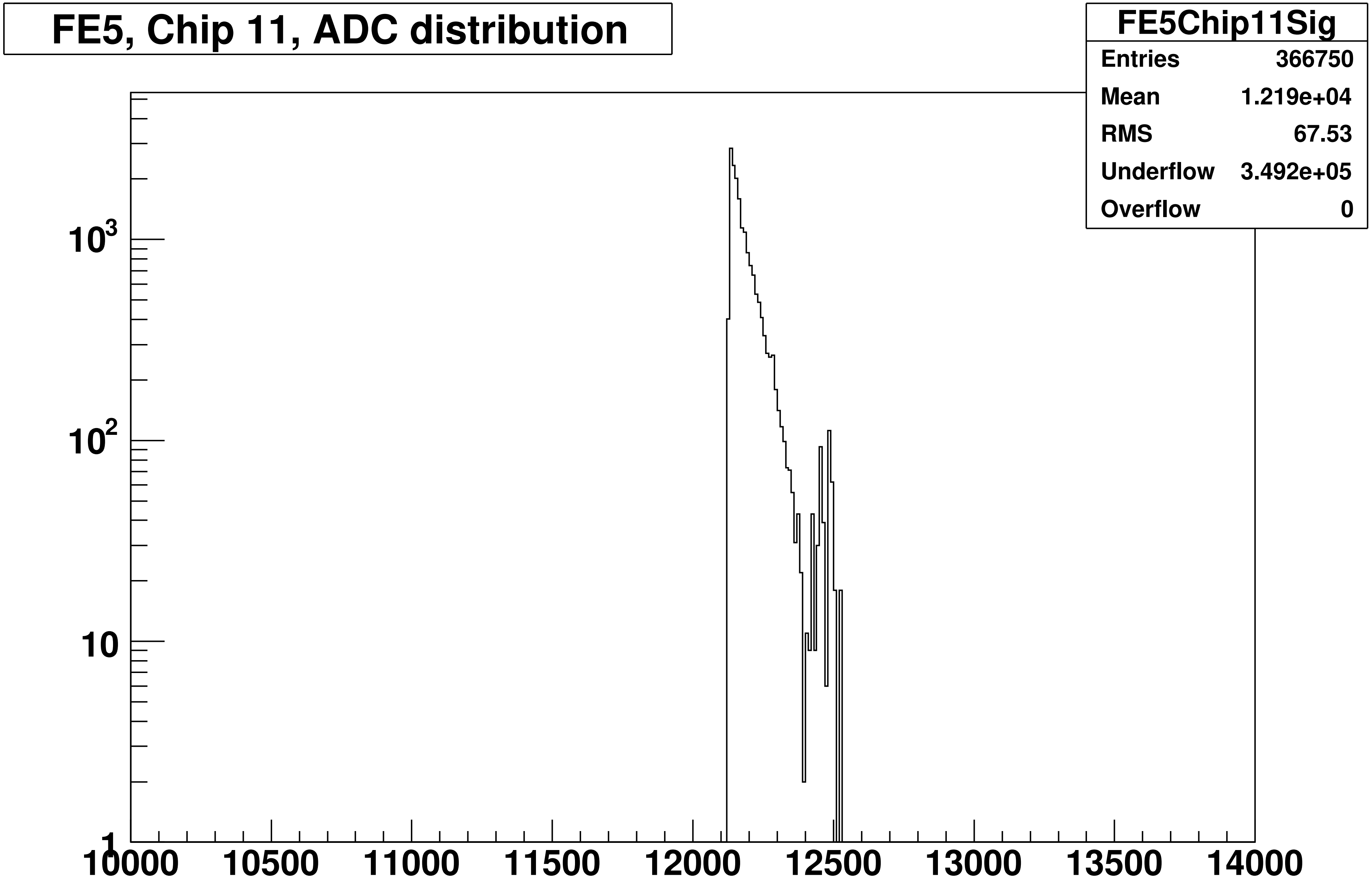

FE5, Chip 10, ADC distribution
FE5Chip10Sig
Entries 366750
Mean 1.218e+04
RMS 67.65
Underflow 3.492e+05
Overflow 0
10^3
10^2
10
1
10000
10500
11000
11500
12000
12500
13000
13500
14000

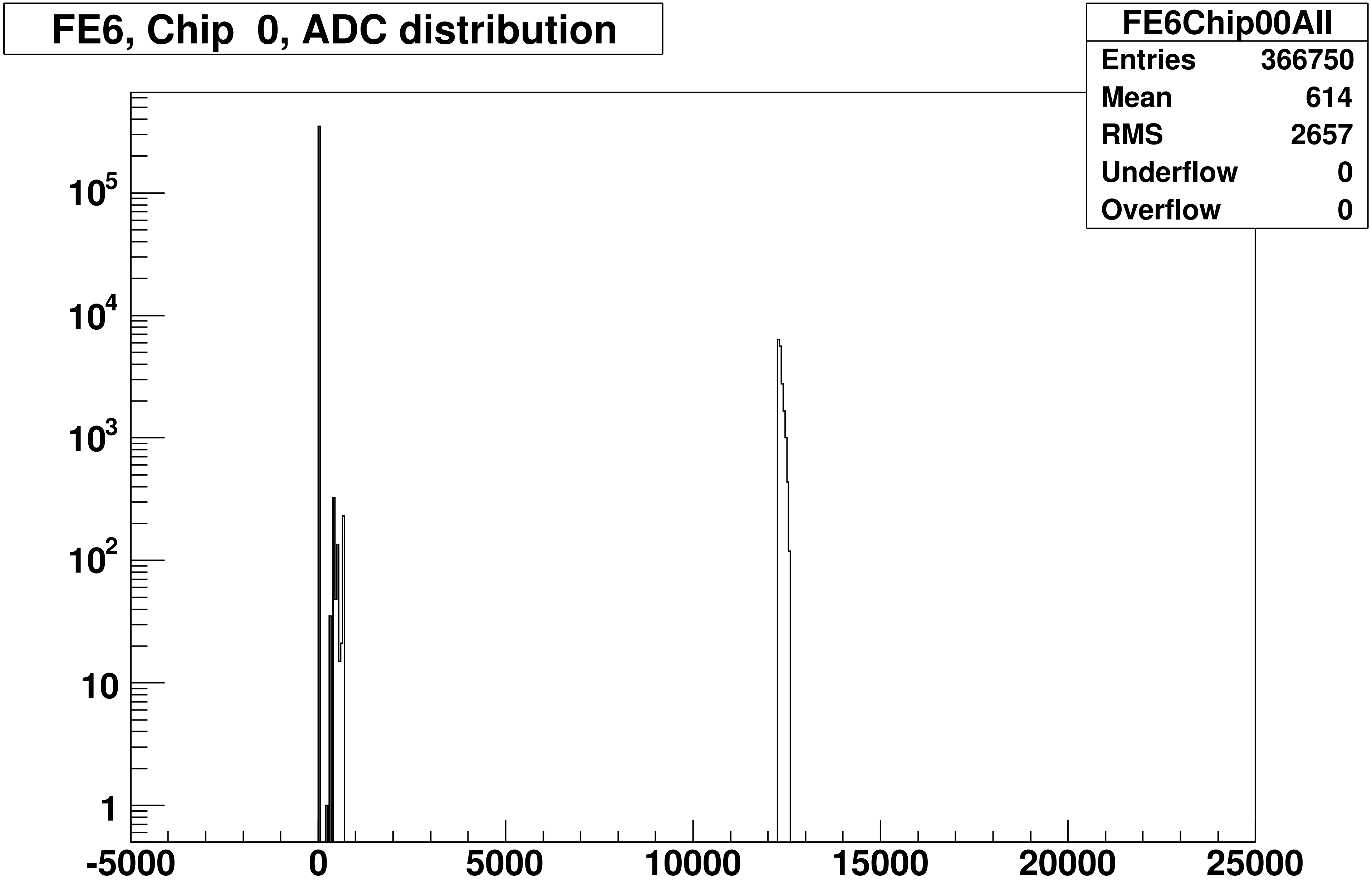


FE5, Chip 11, ADC distribution
FE5Chip11All
Entries 366750
Mean 590.5
RMS 2599
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000

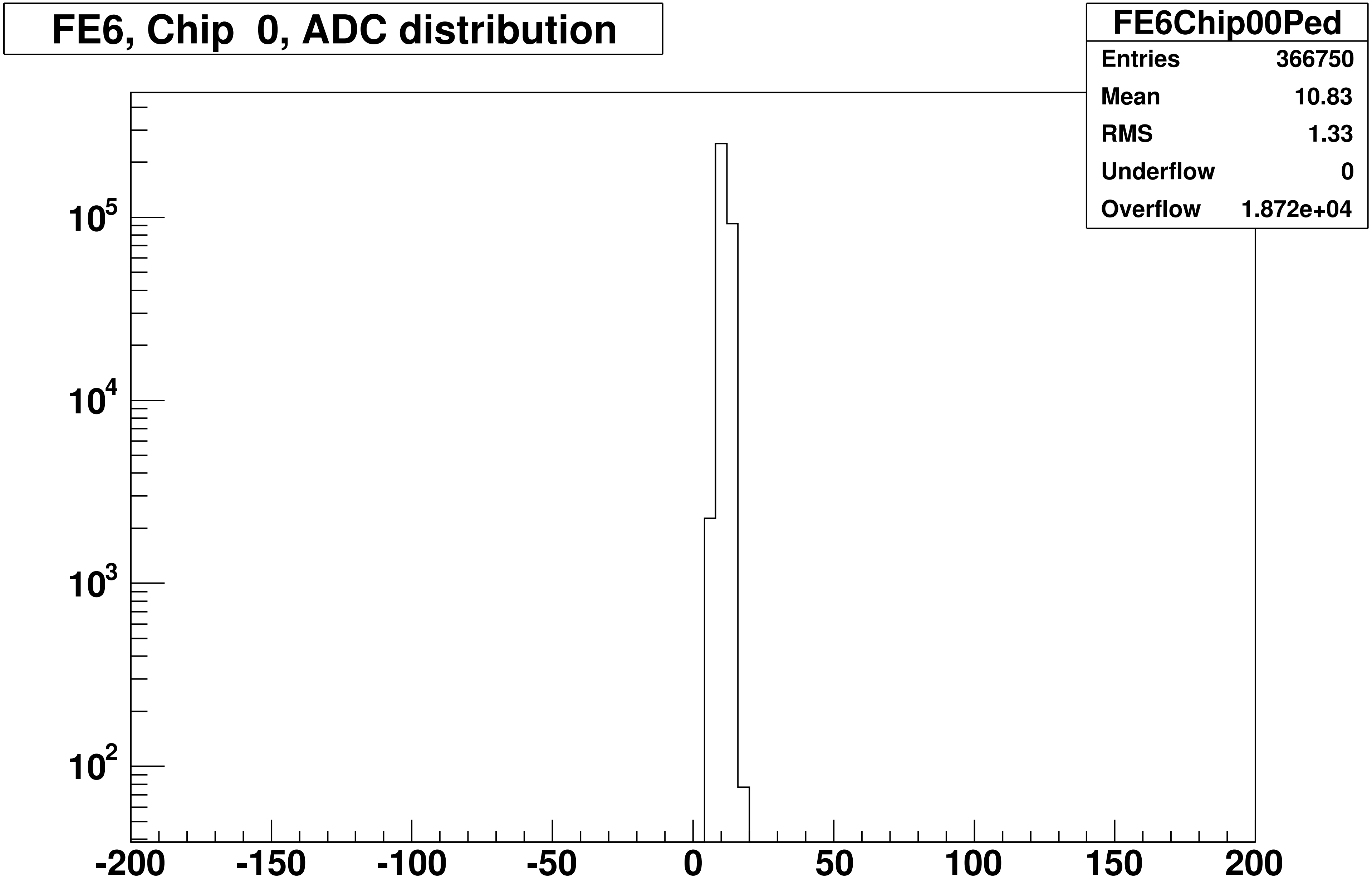


FE5, Chip 11, ADC distribution
FE5Chip11Ped
Entries 366750
Mean 8.233
RMS 1.366
Underflow 0
Overflow 1.753e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
200

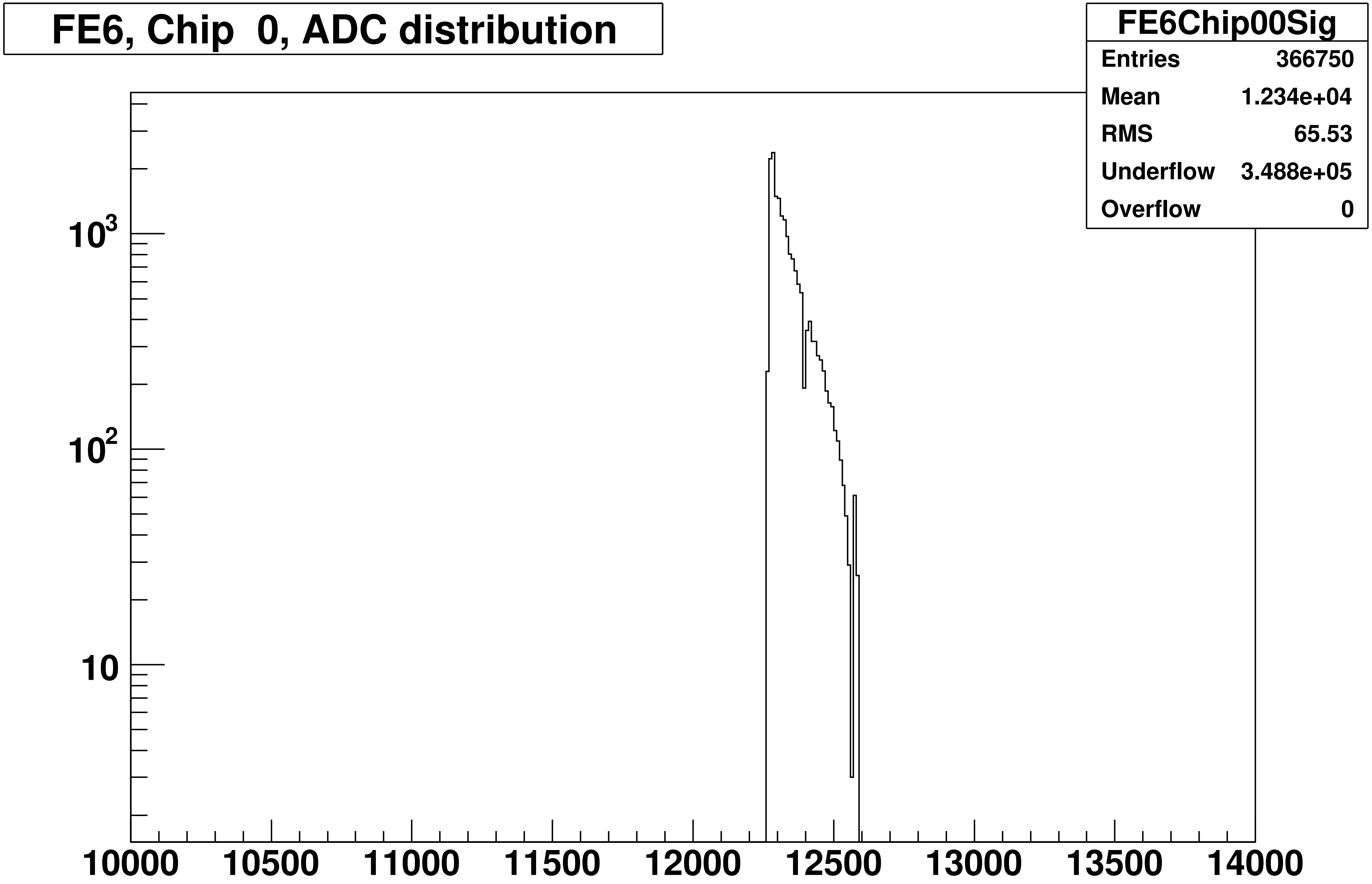

FE5, Chip 11, ADC distribution
FE5Chip11Sig
Entries 366750
Mean 1.219e+04
RMS 67.53
Underflow 3.492e+05
Overflow 0
10^3
10^2
10
1
10000
10500
11000
11500
12000
12500
13000
13500
14000

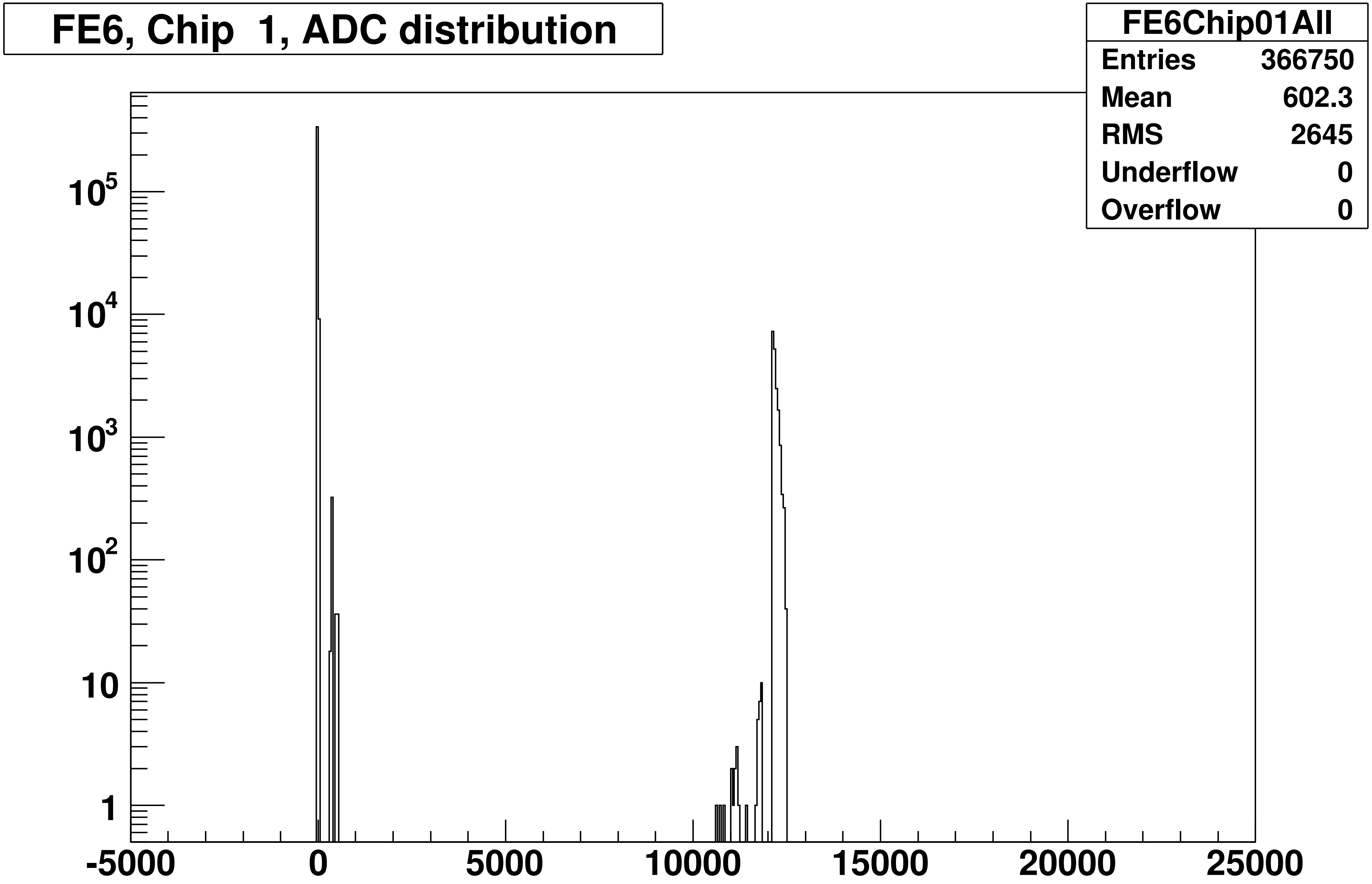


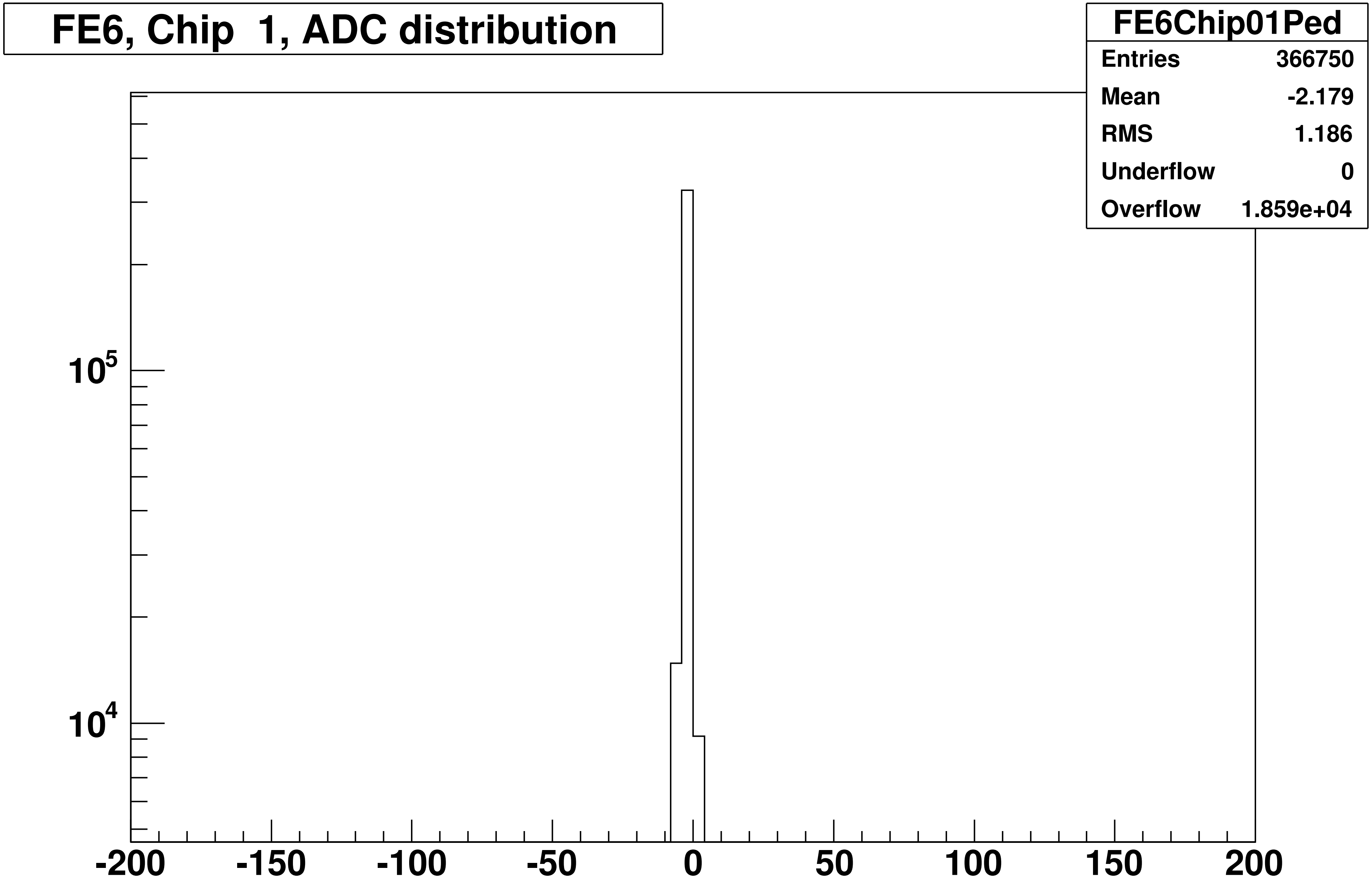
FE6, Chip 0, ADC distribution
FE6Chip00All
Entries 366750
Mean 614
RMS 2657
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



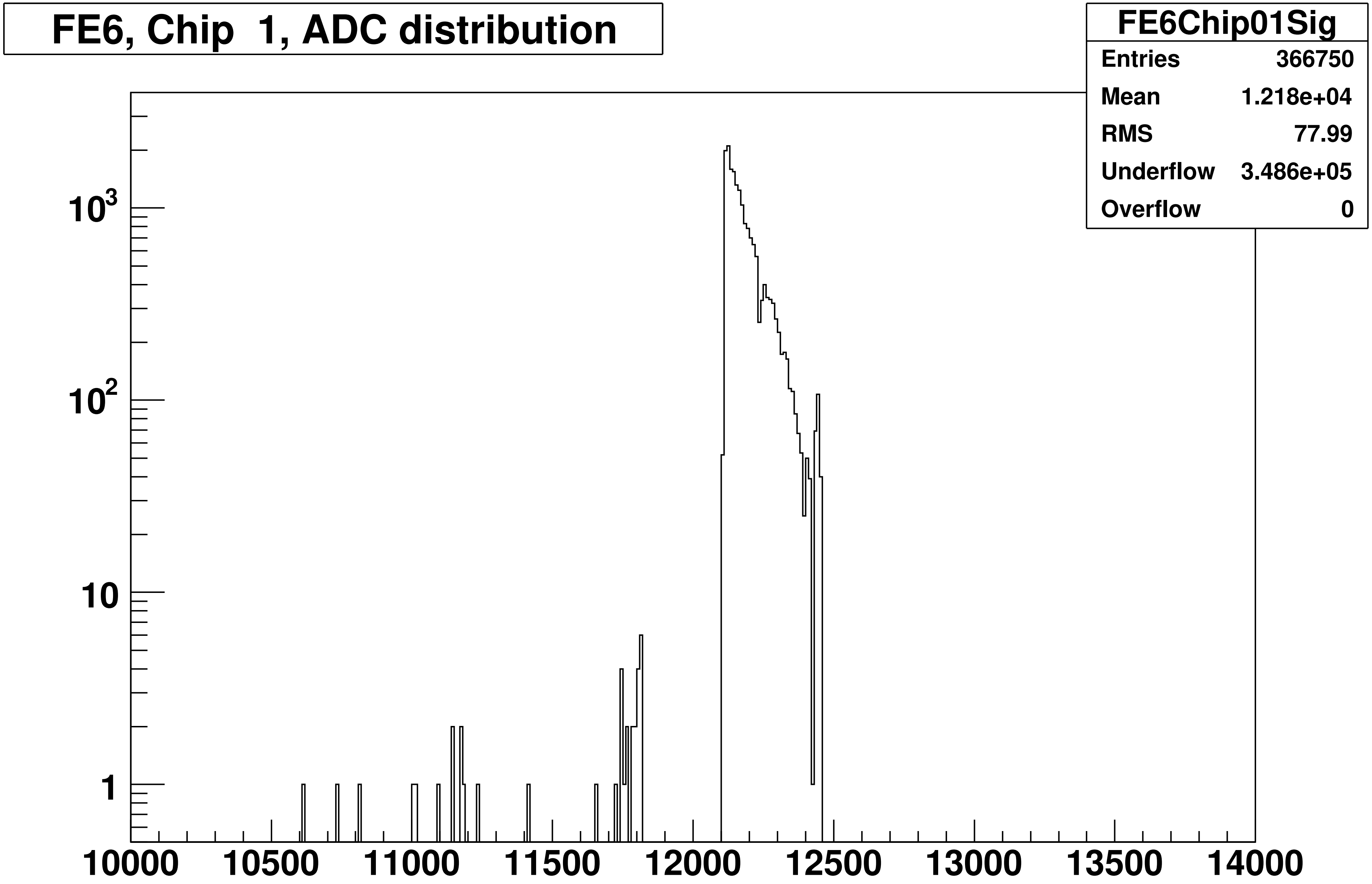
FE6, Chip 0, ADC distribution
FE6Chip00Ped
Entries 366750
Mean 10.83
RMS 1.33
Underflow 0
Overflow 1.872e+04
10^5
10^4
10^3
10^2
-200 -150 -100 -50 0 50 100 150 200

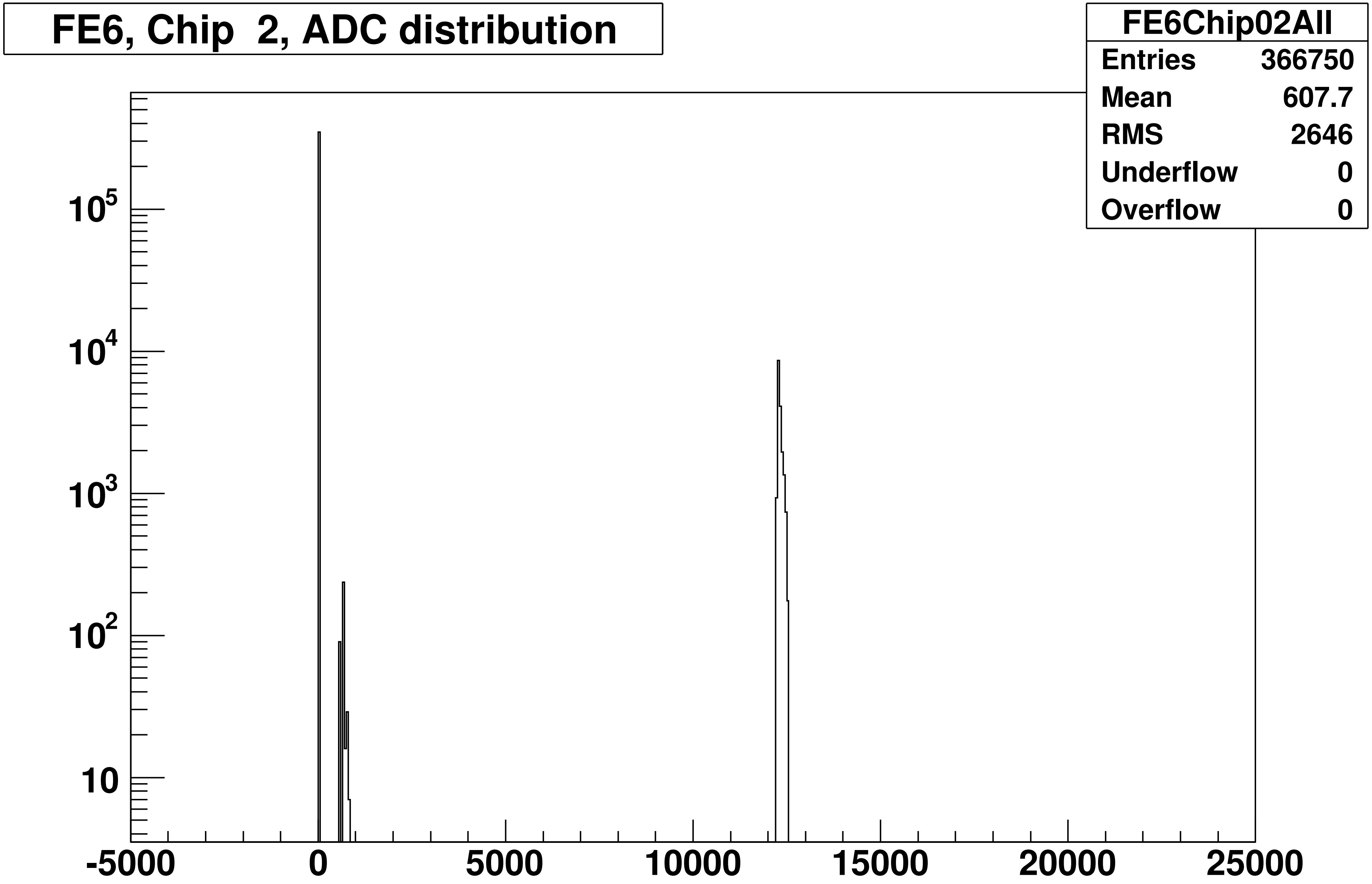

FE6, Chip 0, ADC distribution
FE6Chip00Sig
Entries 366750
Mean 1.234e+04
RMS 65.53
Underflow 3.488e+05
Overflow 0
10^3
10^2
10
10000
10500
11000
11500
12000
12500
13000
13500
14000


FE6, Chip 1, ADC distribution
FE6Chip01All
Entries 366750
Mean 602.3
RMS 2645
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000

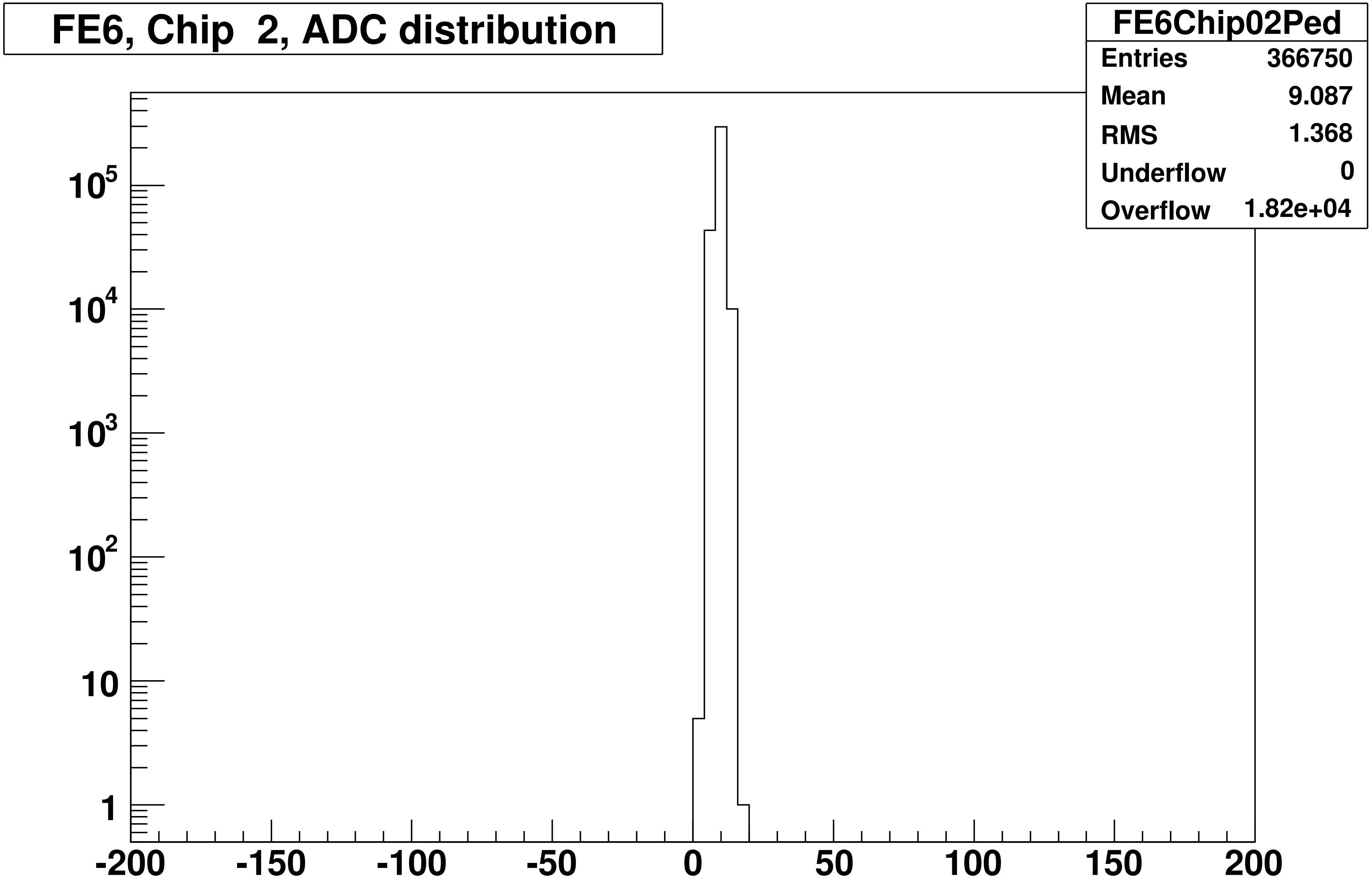


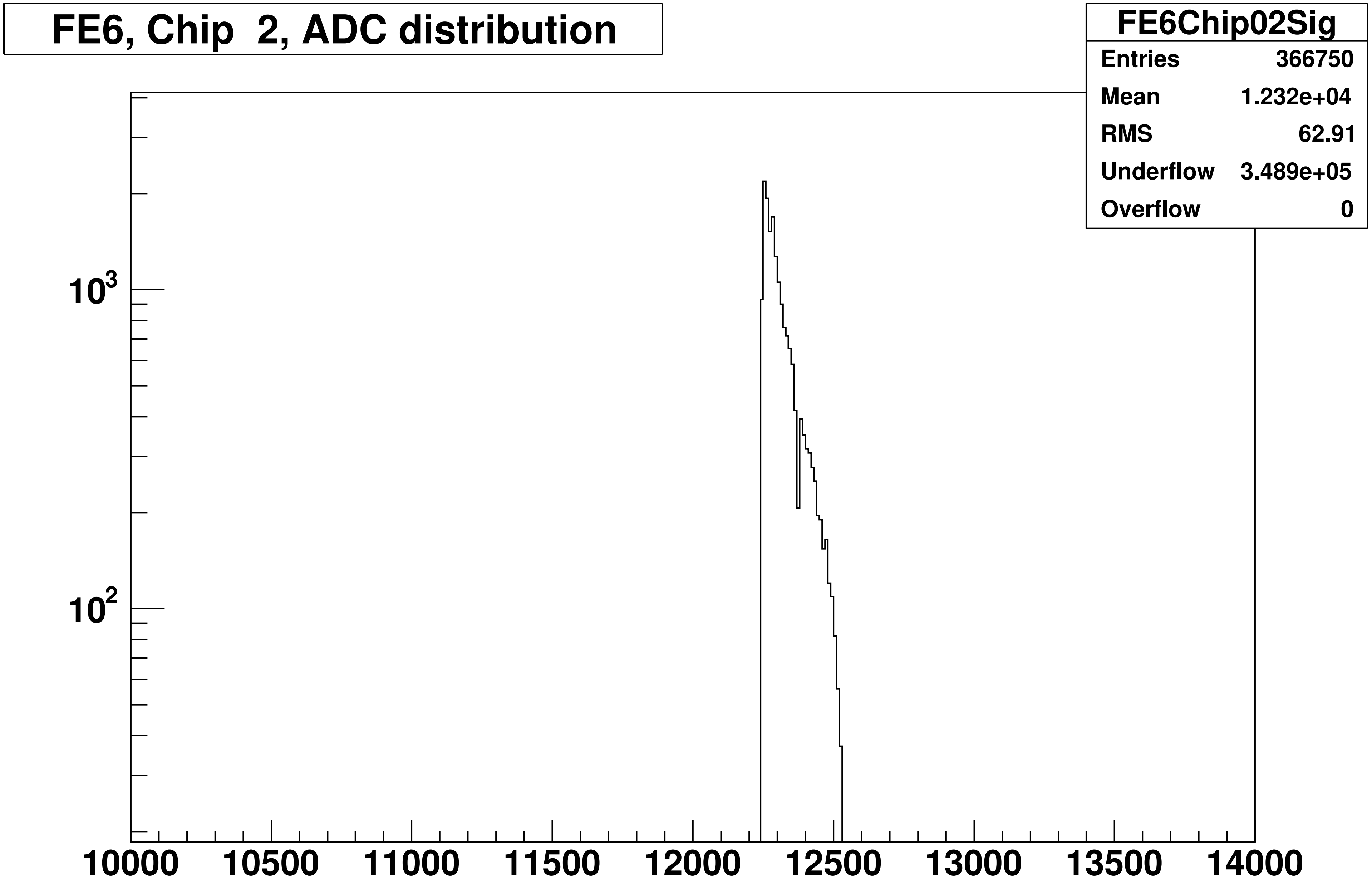
FE6, Chip 1, ADC distribution
FE6Chip01Ped
Entries 366750
Mean -2.179
RMS 1.186
Underflow 0
Overflow 1.859e+04
10^5
10^4
-200
-150
-100
-50
0
50
100
150
200


FE6, Chip 1, ADC distribution
FE6Chip01Sig
Entries 366750
Mean 1.218e+04
RMS 77.99
Underflow 3.486e+05
Overflow 0
10^3
10^2
10
1
10000
10500
11000
11500
12000
12500
13000
13500
14000



FE6, Chip 2, ADC distribution
FE6Chip02All
Entries 366750
Mean 607.7
RMS 2646
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE6, Chip 2, ADC distribution
FE6Chip02Ped
Entries 366750
Mean 9.087
RMS 1.368
Underflow 0
Overflow 1.82e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
200


FE6, Chip 2, ADC distribution
FE6Chip02Sig
Entries 366750
Mean 1.232e+04
RMS 62.91
Underflow 3.489e+05
Overflow 0
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10^2
10000
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11500
12000
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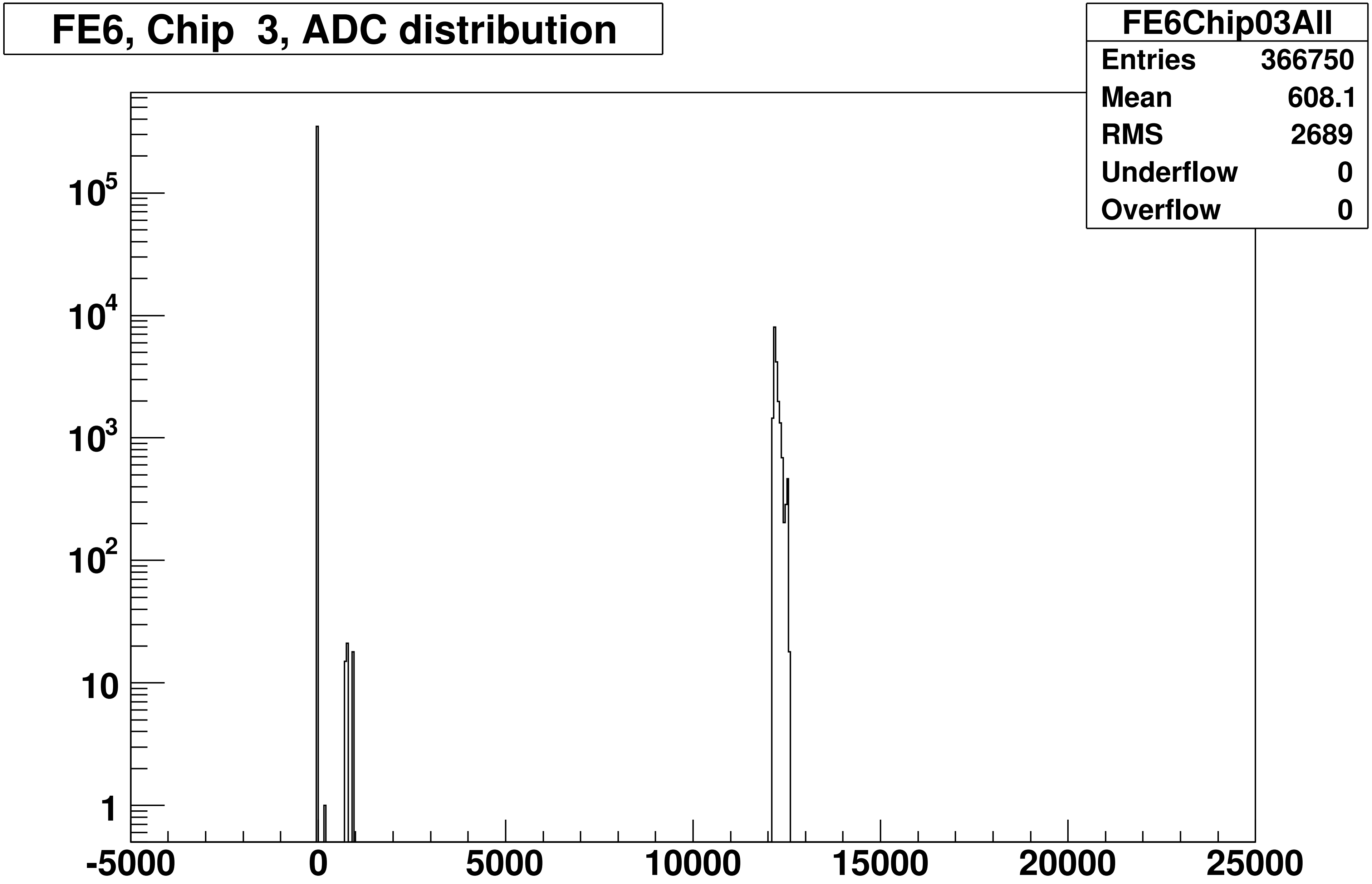
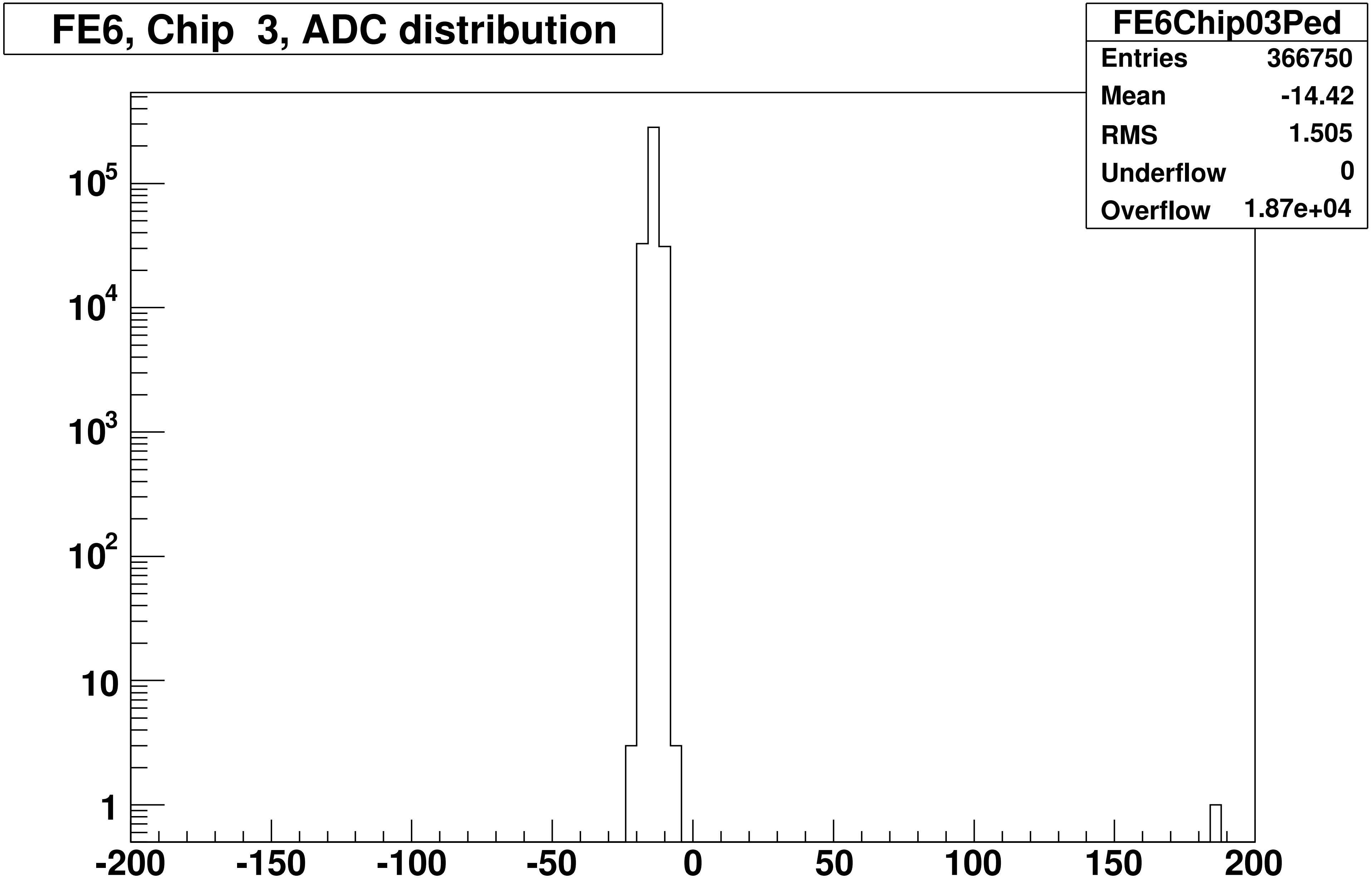
13500
14000


FE6, Chip 3, ADC distribution
FE6Chip03All
Entries 366750
Mean 608.1
RMS 2689
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE6, Chip 3, ADC distribution
FE6Chip03Ped
Entries 366750
Mean -14.42
RMS 1.505
Underflow 0
Overflow 1.87e+04
10^5
10^4
10^3
10^2
10
1
-200
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-100
-50
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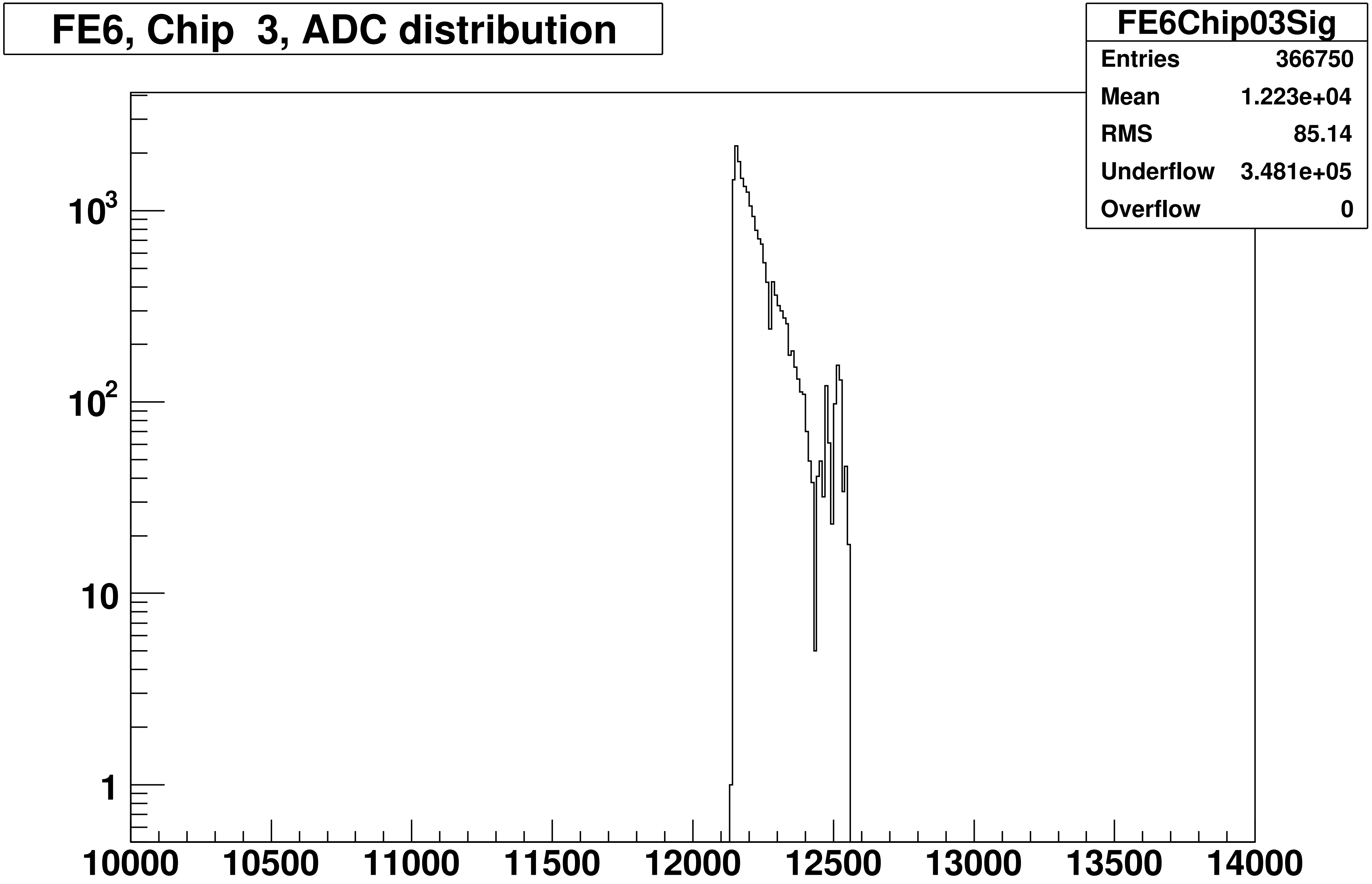
100
150
200


FE6, Chip 3, ADC distribution
FE6Chip03Sig
Entries 366750
Mean 1.223e+04
RMS 85.14
Underflow 3.481e+05
Overflow 0
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10^2
10
1
10000
10500
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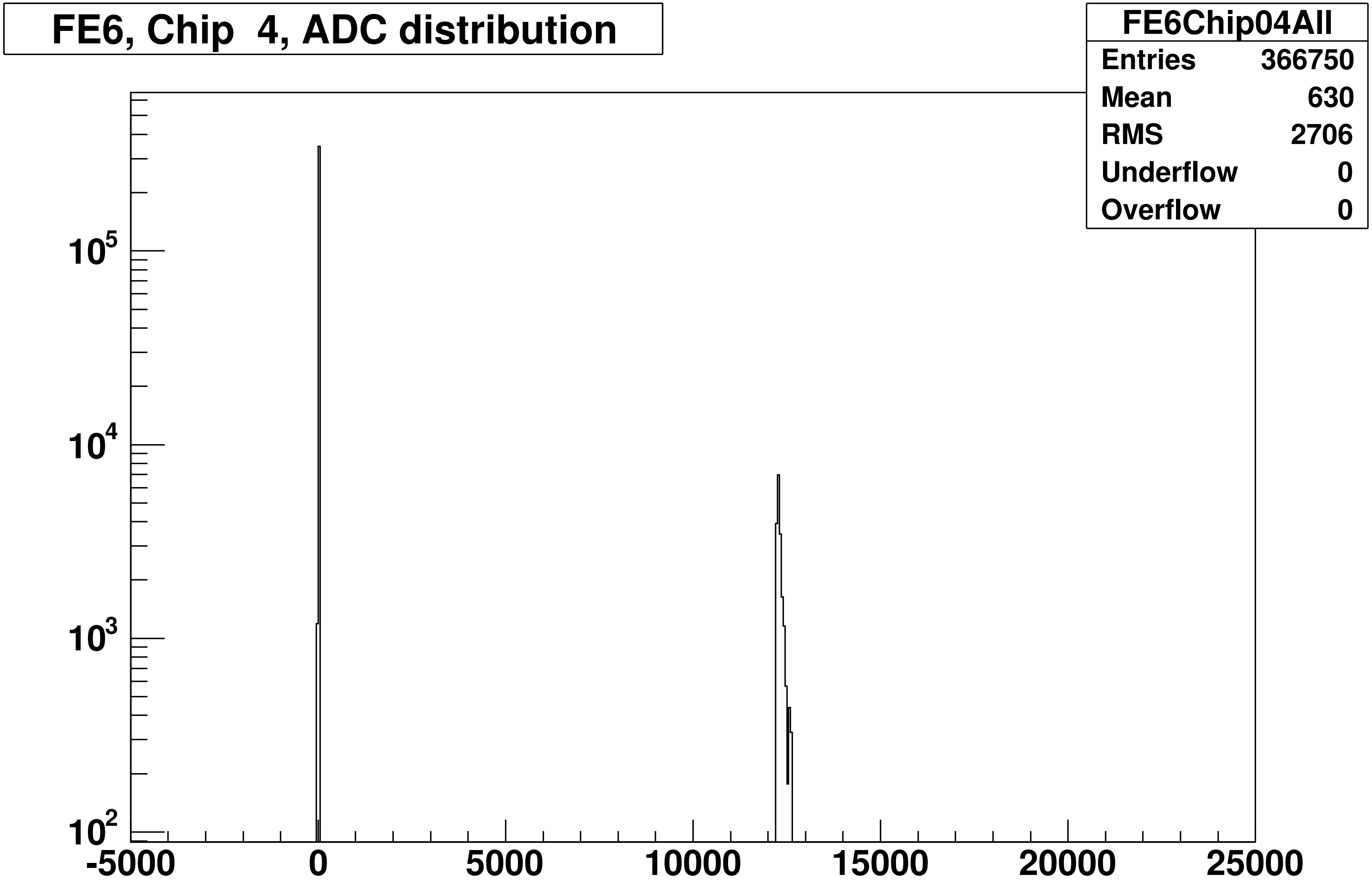
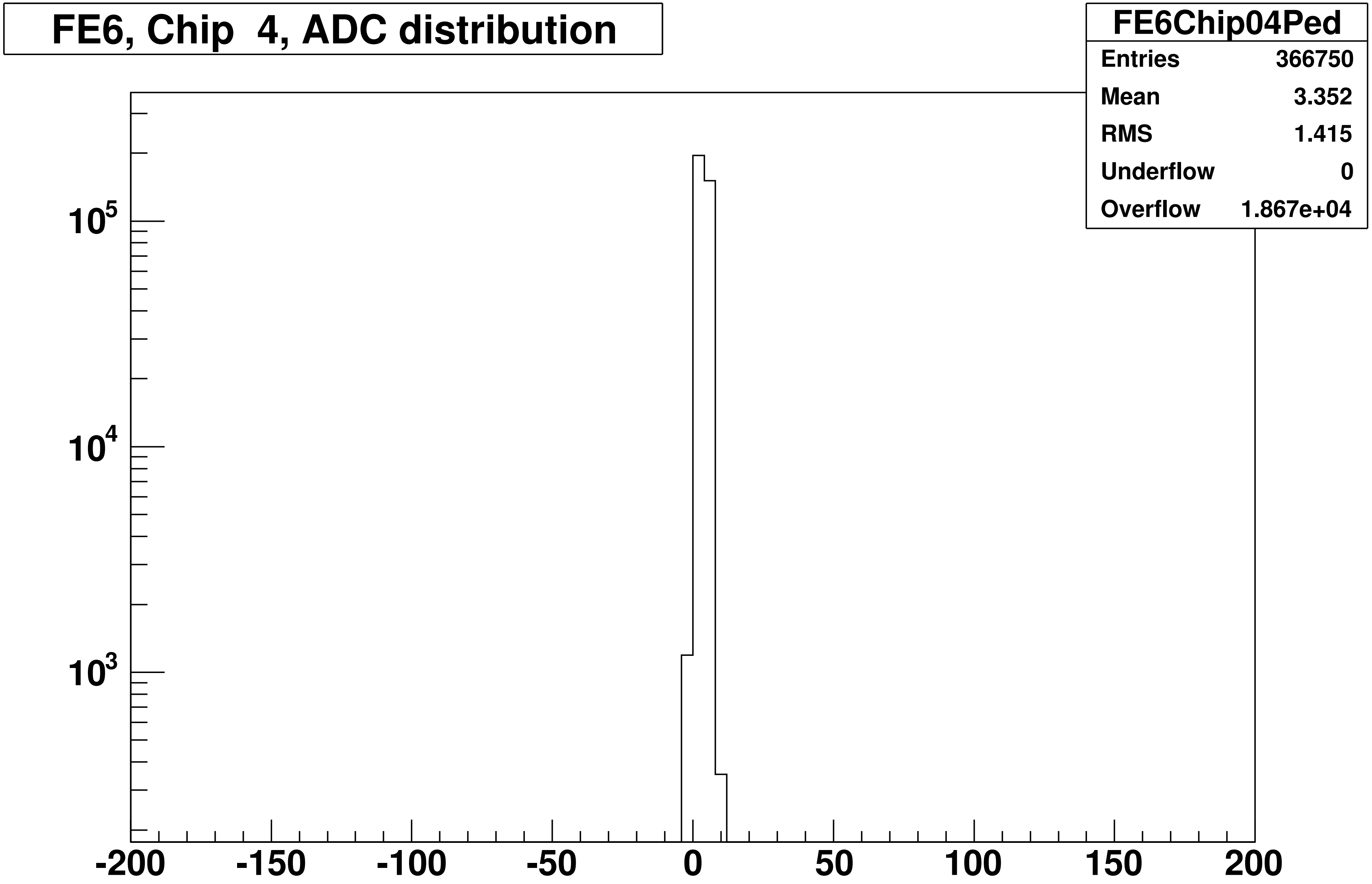
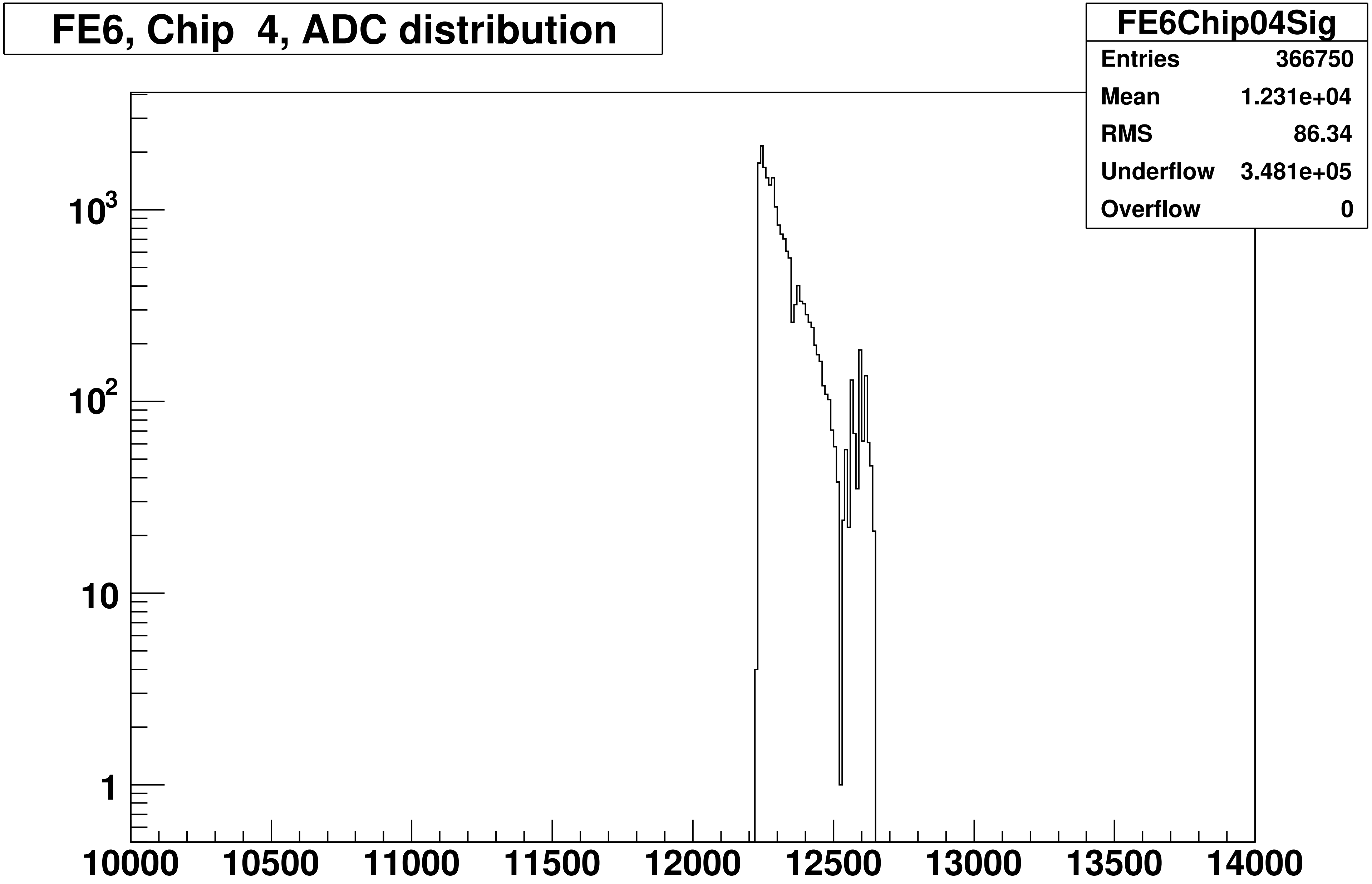

FE6, Chip 4, ADC distribution
FE6Chip04All
Entries 366750
Mean 630
RMS 2706
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000


FE6, Chip 4, ADC distribution
FE6Chip04Ped
Entries 366750
Mean 3.352
RMS 1.415
Underflow 0
Overflow 1.867e+04
10^5
10^4
10^3
-200
-150
-100
-50
0
50
100
150
200



FE6, Chip 4, ADC distribution
FE6Chip04Sig
Entries 366750
Mean 1.231e+04
RMS 86.34
Underflow 3.481e+05
Overflow 0
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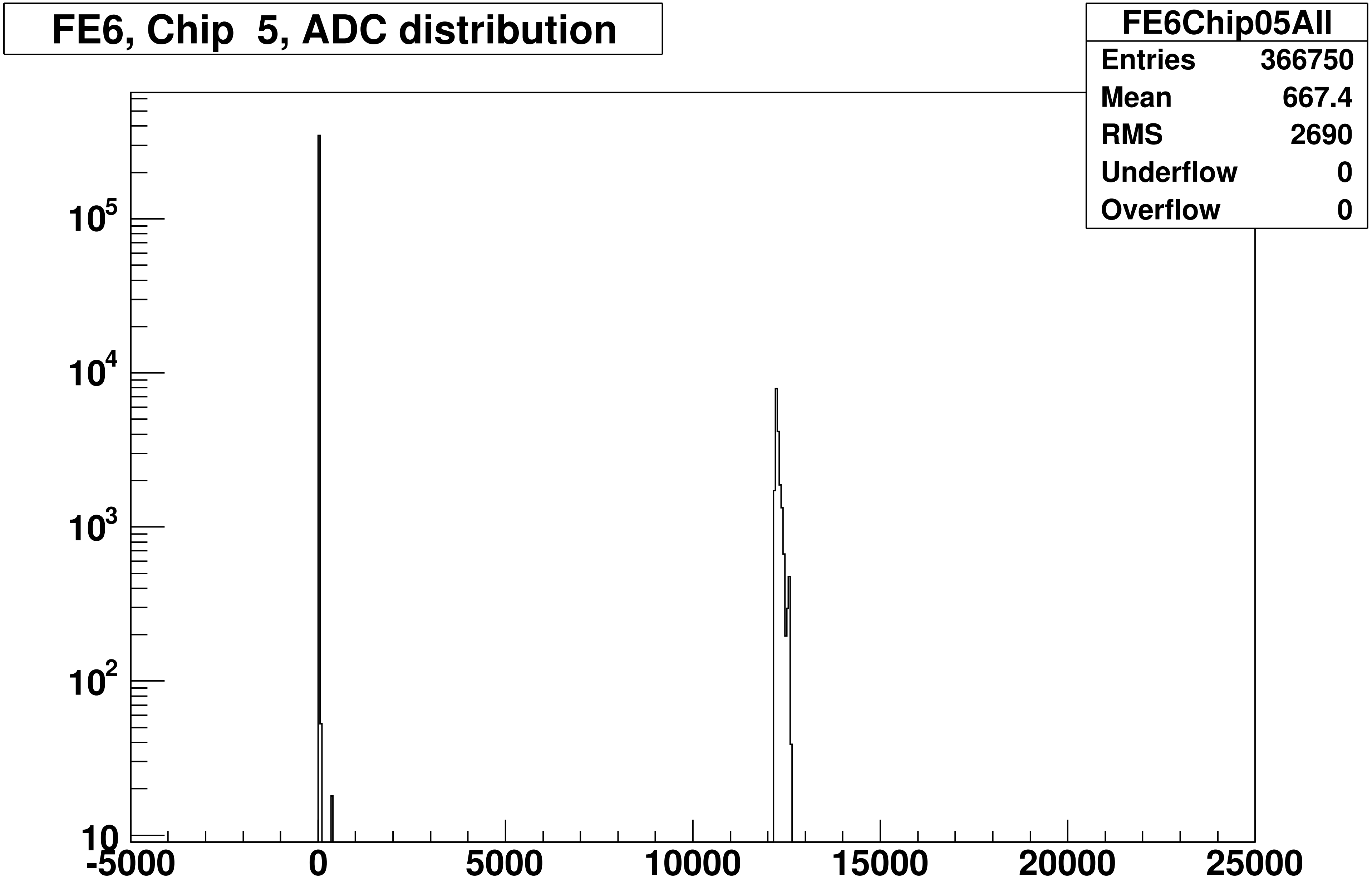
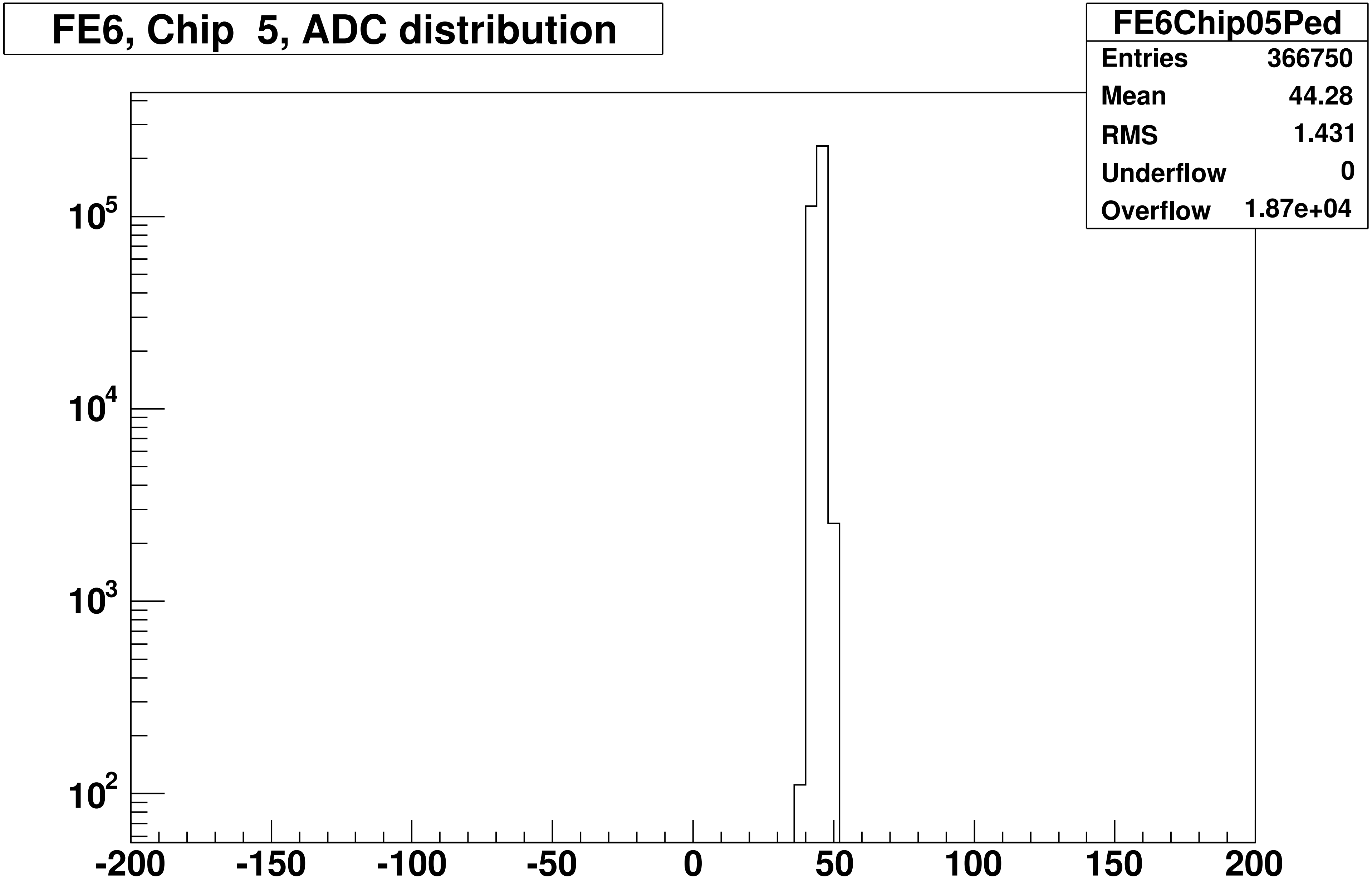
10^2
10
1
10000
10500
11000
11500
12000
12500
13000
13500
14000


FE6, Chip 5, ADC distribution
FE6Chip05All
Entries 366750
Mean 667.4
RMS 2690
Underflow 0
Overflow 0
10
10^2
10^3
10^4
10^5
-5000
0
5000
10000
15000
20000
25000



FE6, Chip 5, ADC distribution
FE6Chip05Ped
Entries 366750
Mean 44.28
RMS 1.431
Underflow 0
Overflow 1.87e+04
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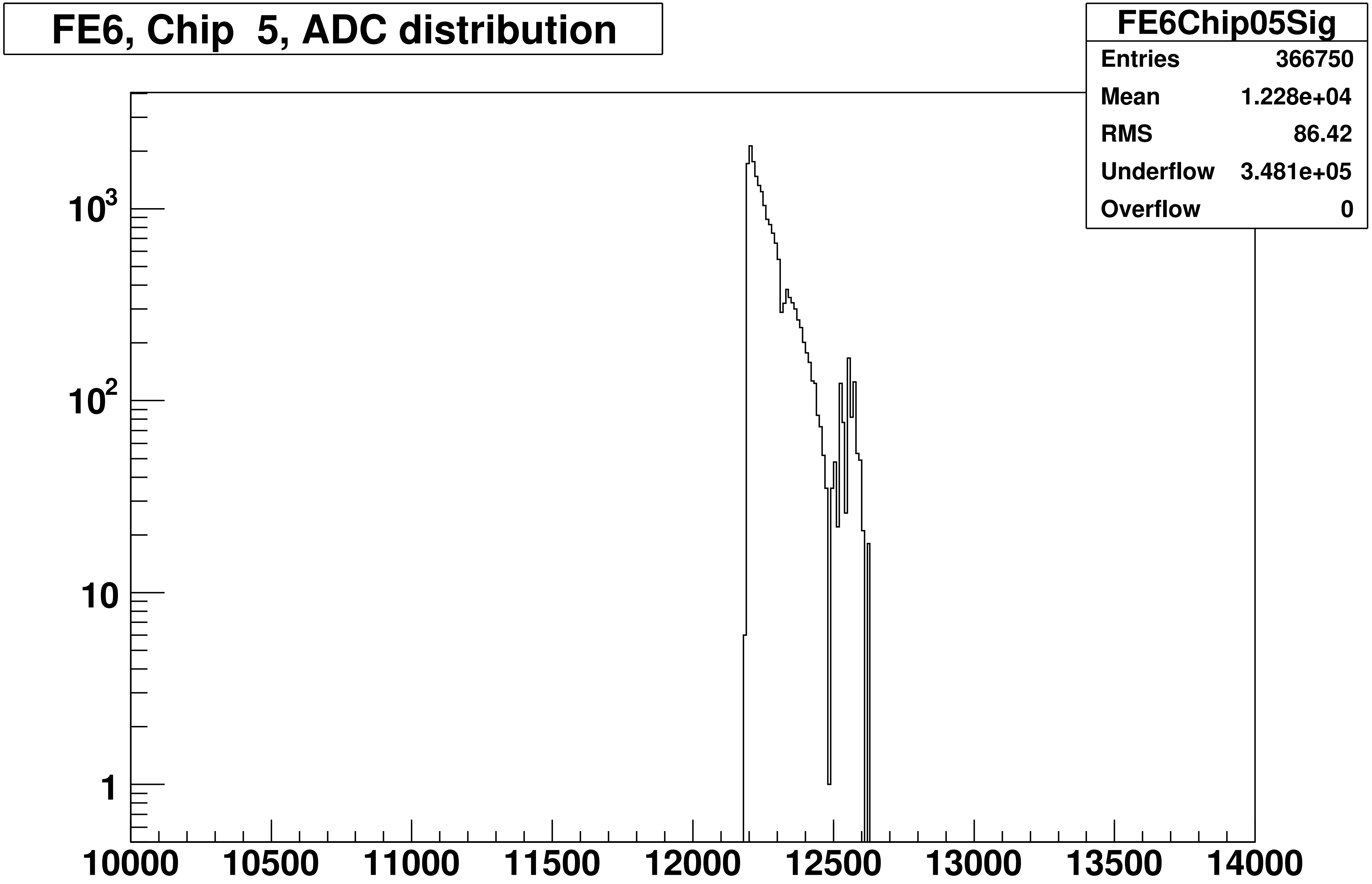
10^4
10^3
10^2
-200
-150
-100
-50
0
50
100
150
200


FE6, Chip 5, ADC distribution
FE6Chip05Sig
Entries 366750
Mean 1.228e+04
RMS 86.42
Underflow 3.481e+05
Overflow 0
10^3
10^2
10
1
10000
10500
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11500
12000
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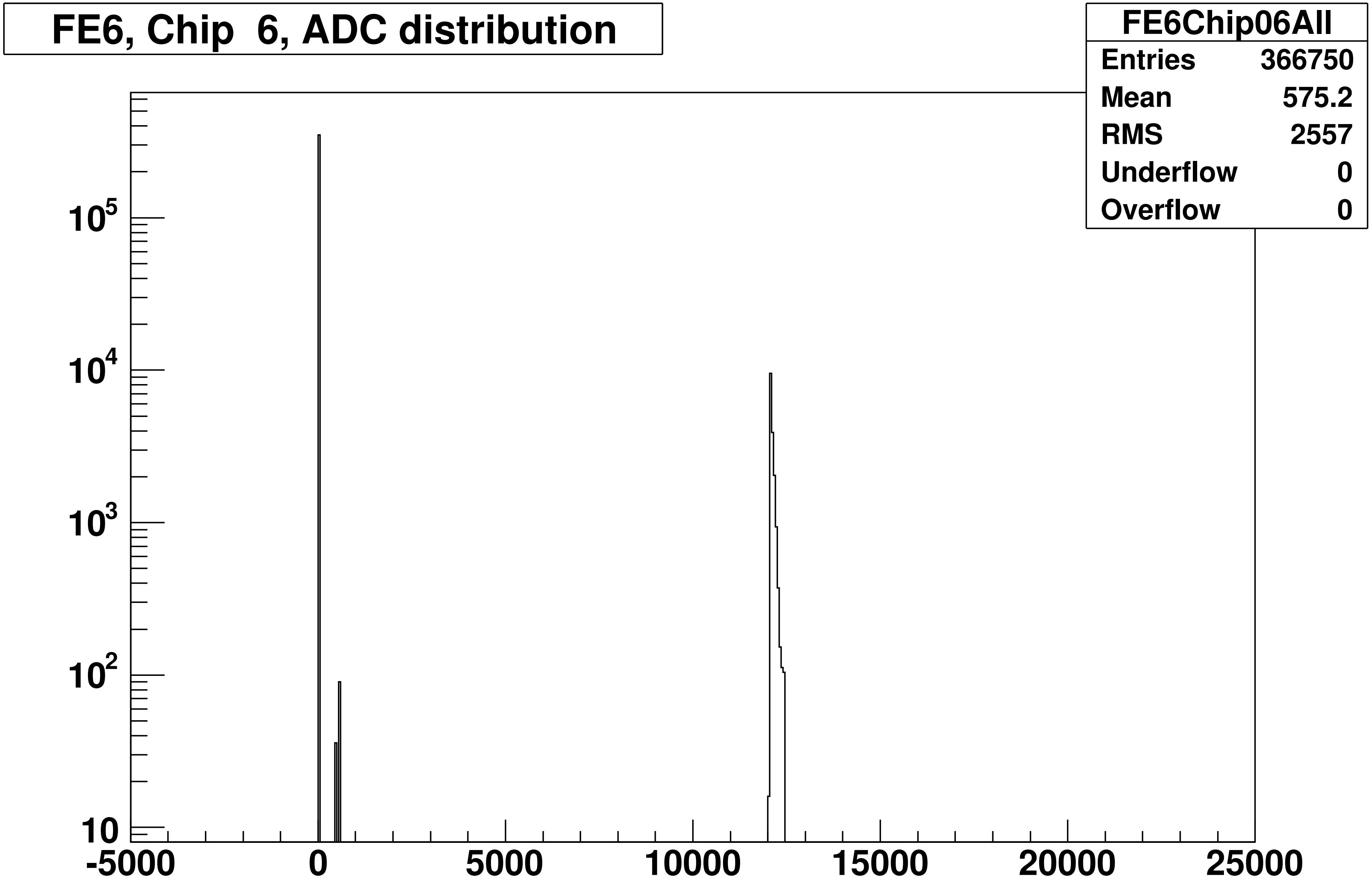
FE6, Chip 6, ADC distribution
FE6Chip06All
Entries 366750
Mean 575.2
RMS 2557
Underflow 0
Overflow 0
10
10^2
10^3
10^4
10^5
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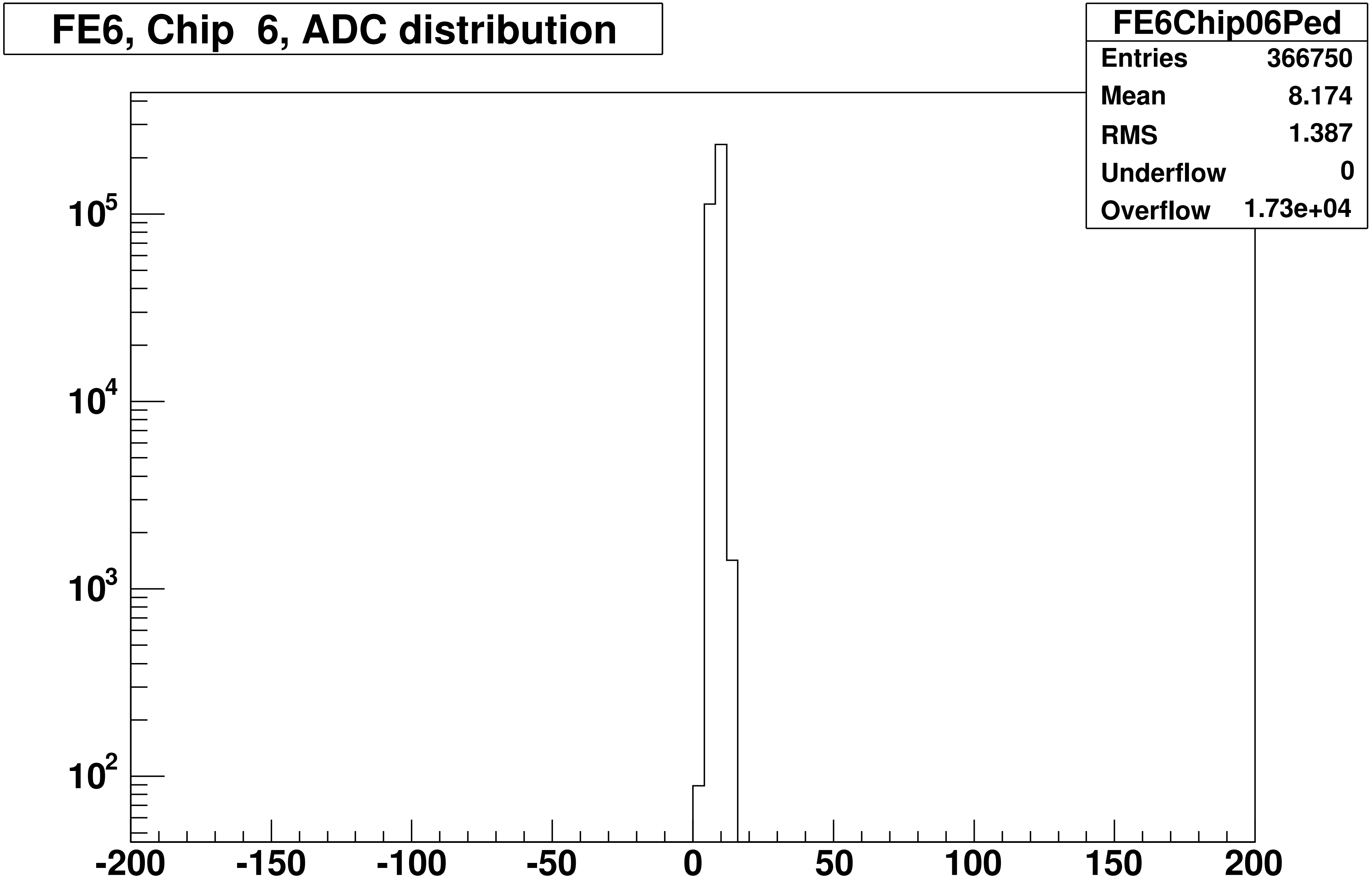
10000
15000
20000
25000


FE6, Chip 6, ADC distribution
FE6Chip06Ped
Entries 366750
Mean 8.174
RMS 1.387
Underflow 0
Overflow 1.73e+04
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10^4
10^3
10^2
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-100
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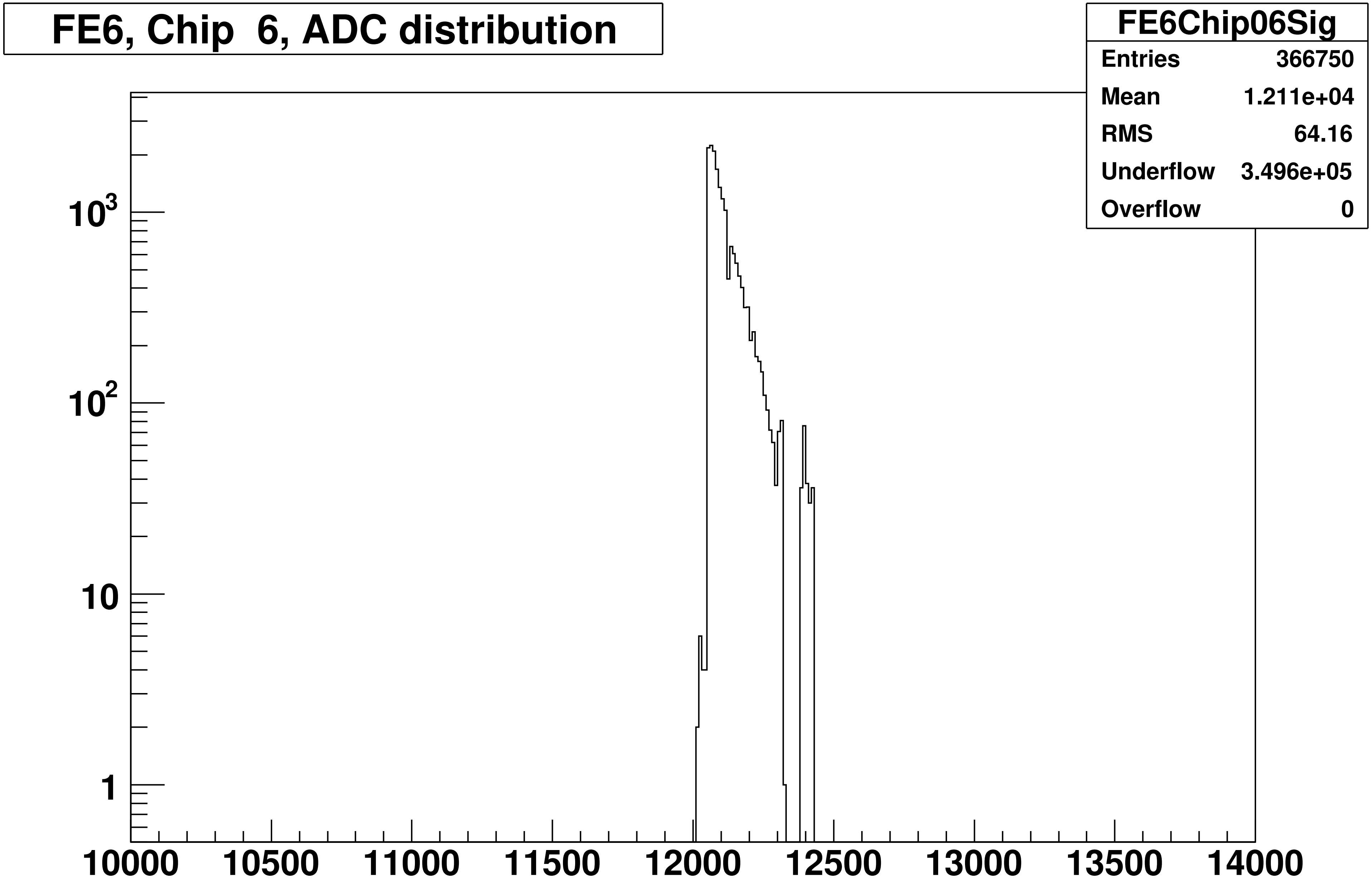
100
150
200


FE6, Chip 6, ADC distribution
FE6Chip06Sig
Entries 366750
Mean 1.211e+04
RMS 64.16
Underflow 3.496e+05
Overflow 0
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10^2
10
1
10000
10500
11000
11500
12000
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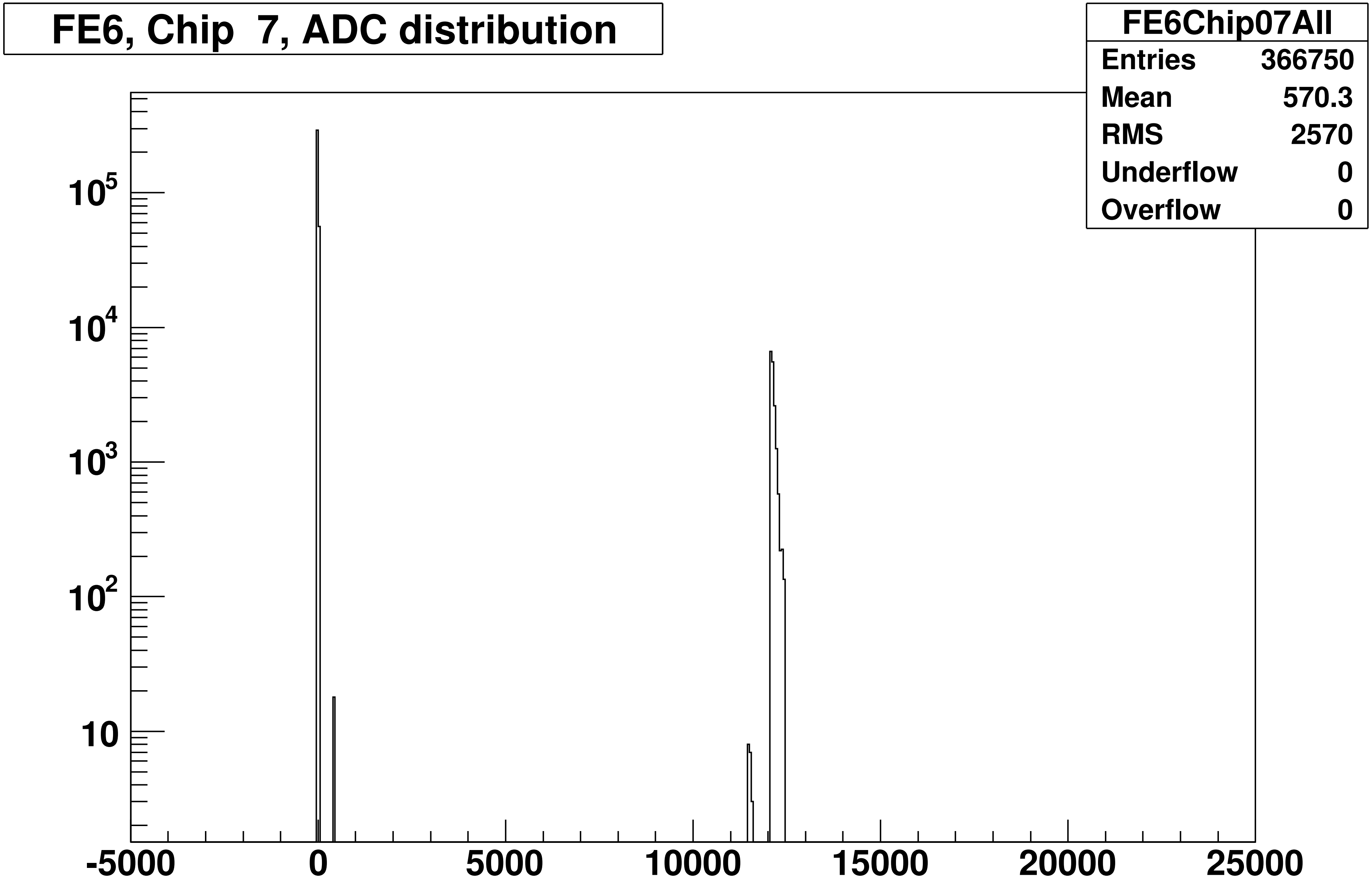
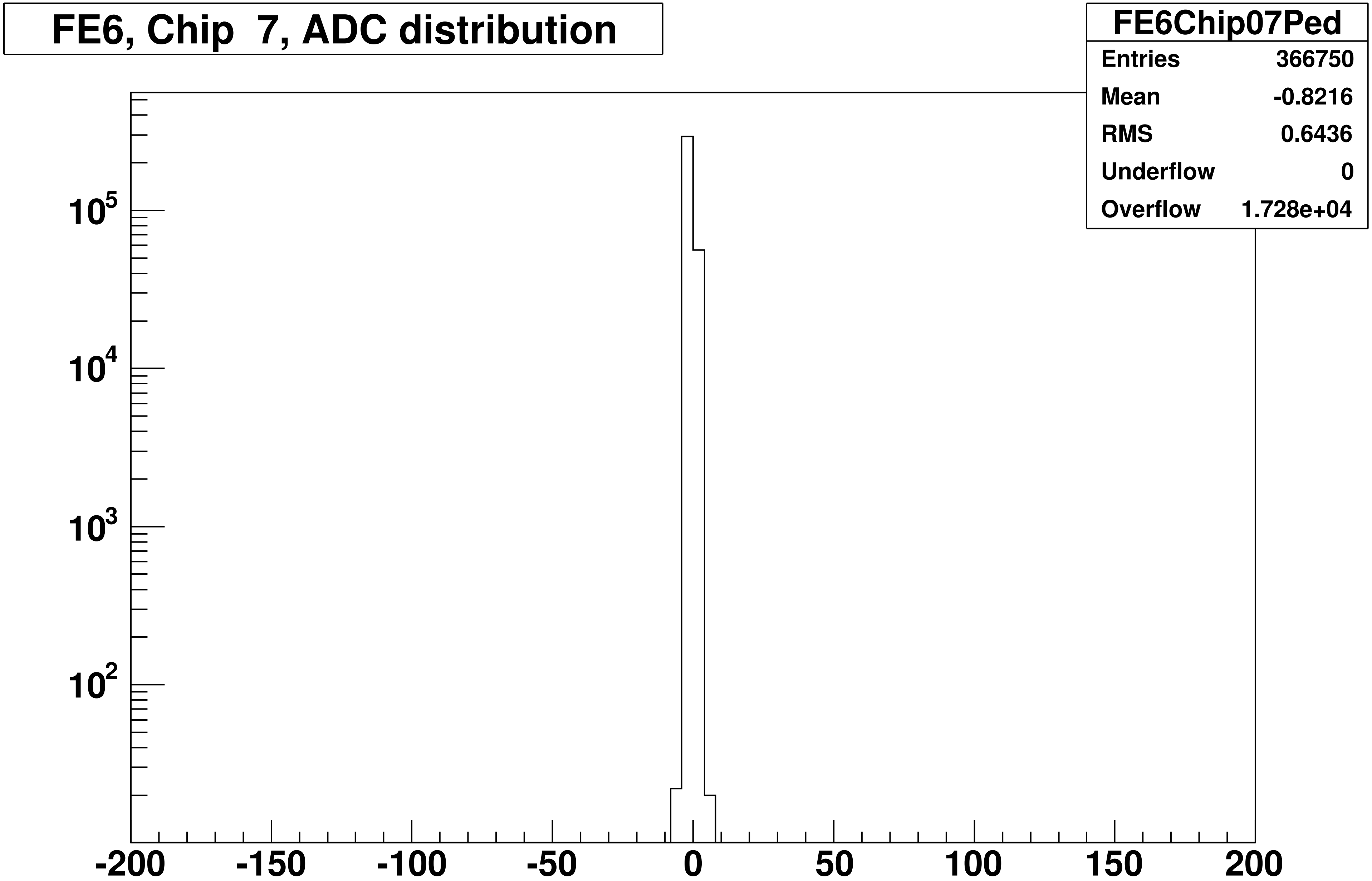
14000


FE6, Chip 7, ADC distribution
FE6Chip07All
Entries 366750
Mean 570.3
RMS 2570
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE6, Chip 7, ADC distribution
FE6Chip07Ped
Entries 366750
Mean -0.8216
RMS 0.6436
Underflow 0
Overflow 1.728e+04
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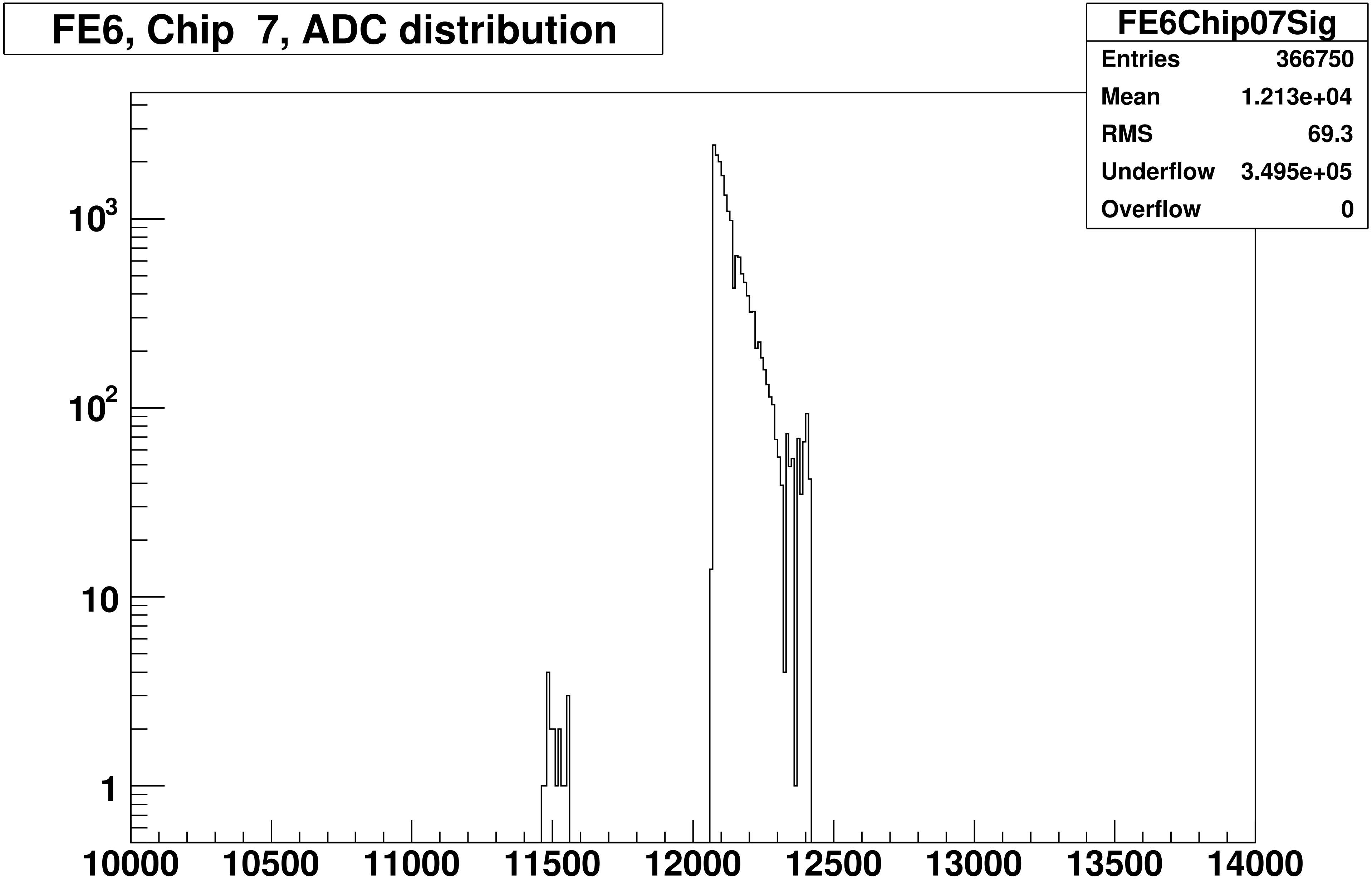
10^4
10^3
10^2
-200
-150
-100
-50
0
50
100
150
200


FE6, Chip 7, ADC distribution
FE6Chip07Sig
Entries 366750
Mean 1.213e+04
RMS 69.3
Underflow 3.495e+05
Overflow 0
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10^2
10
1
10000
10500
11000
11500
12000
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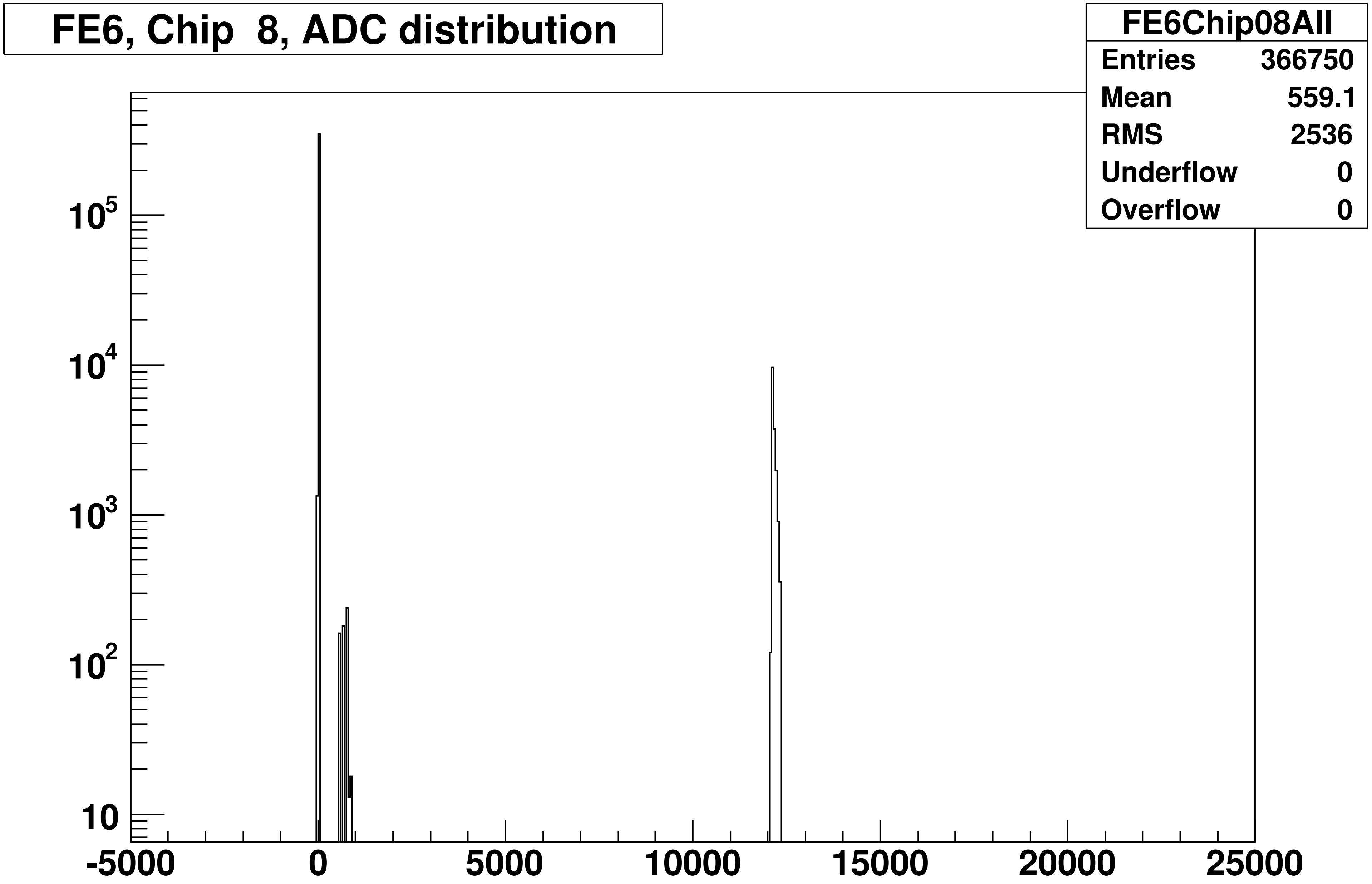
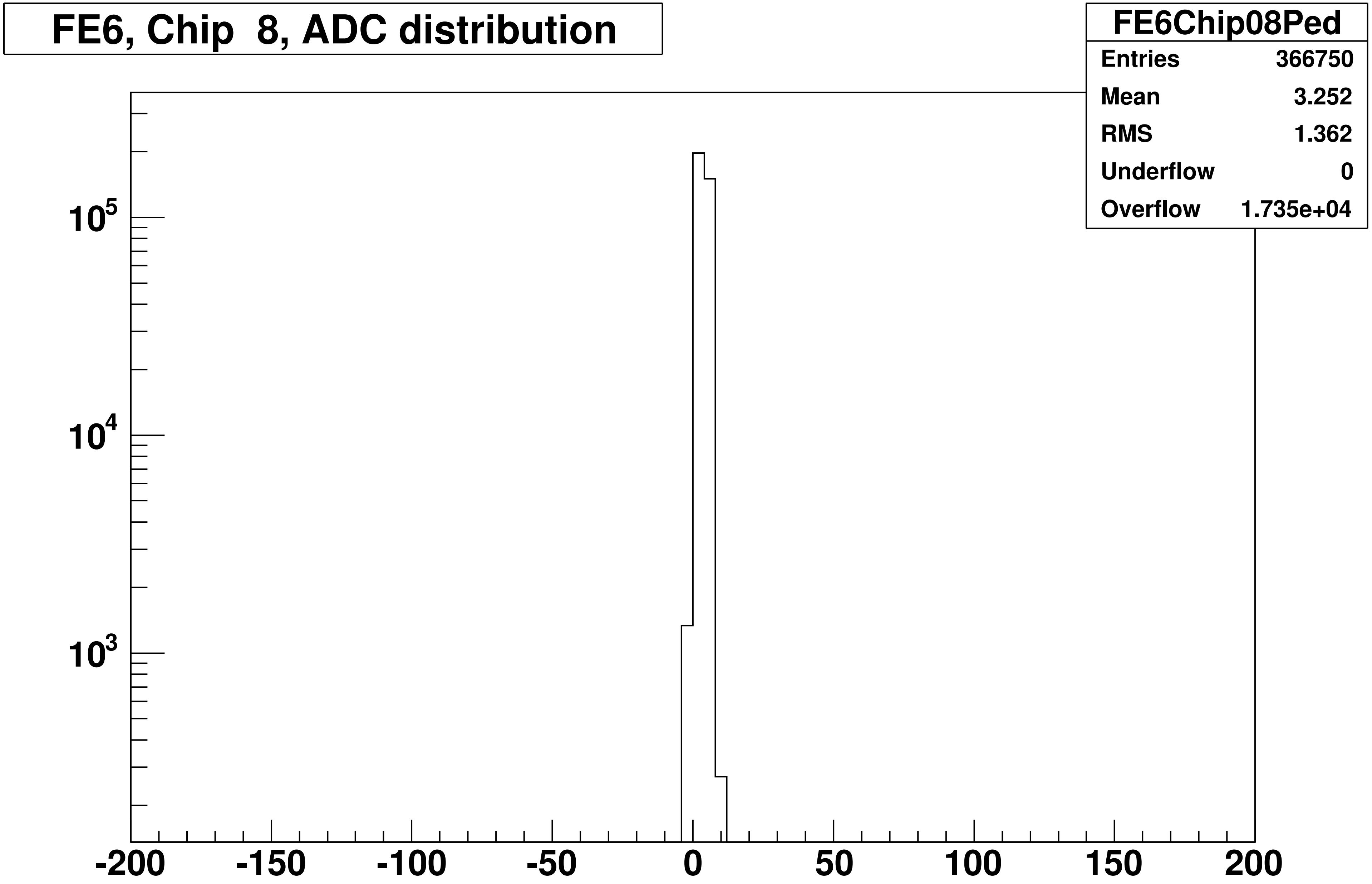
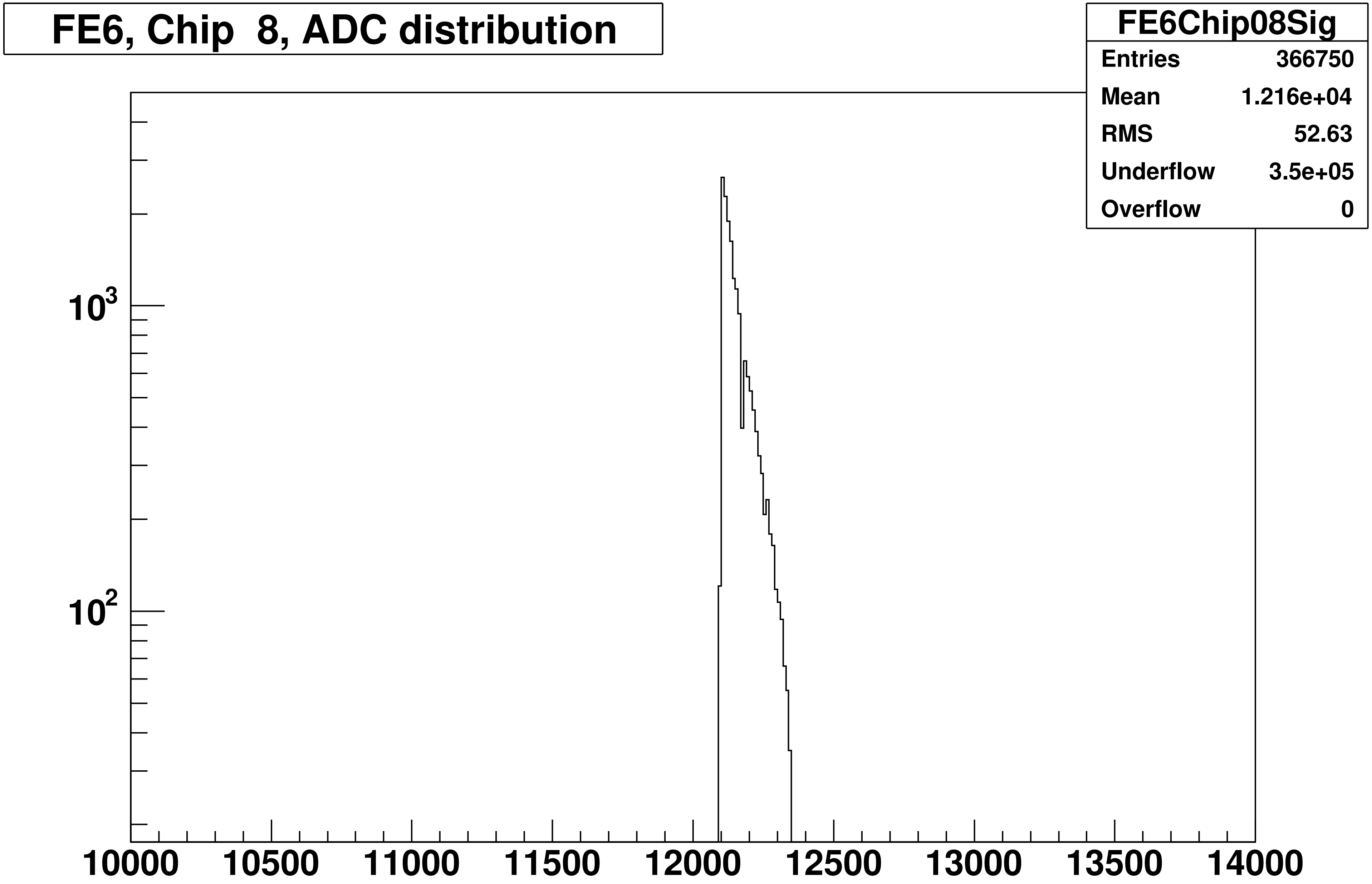
14000

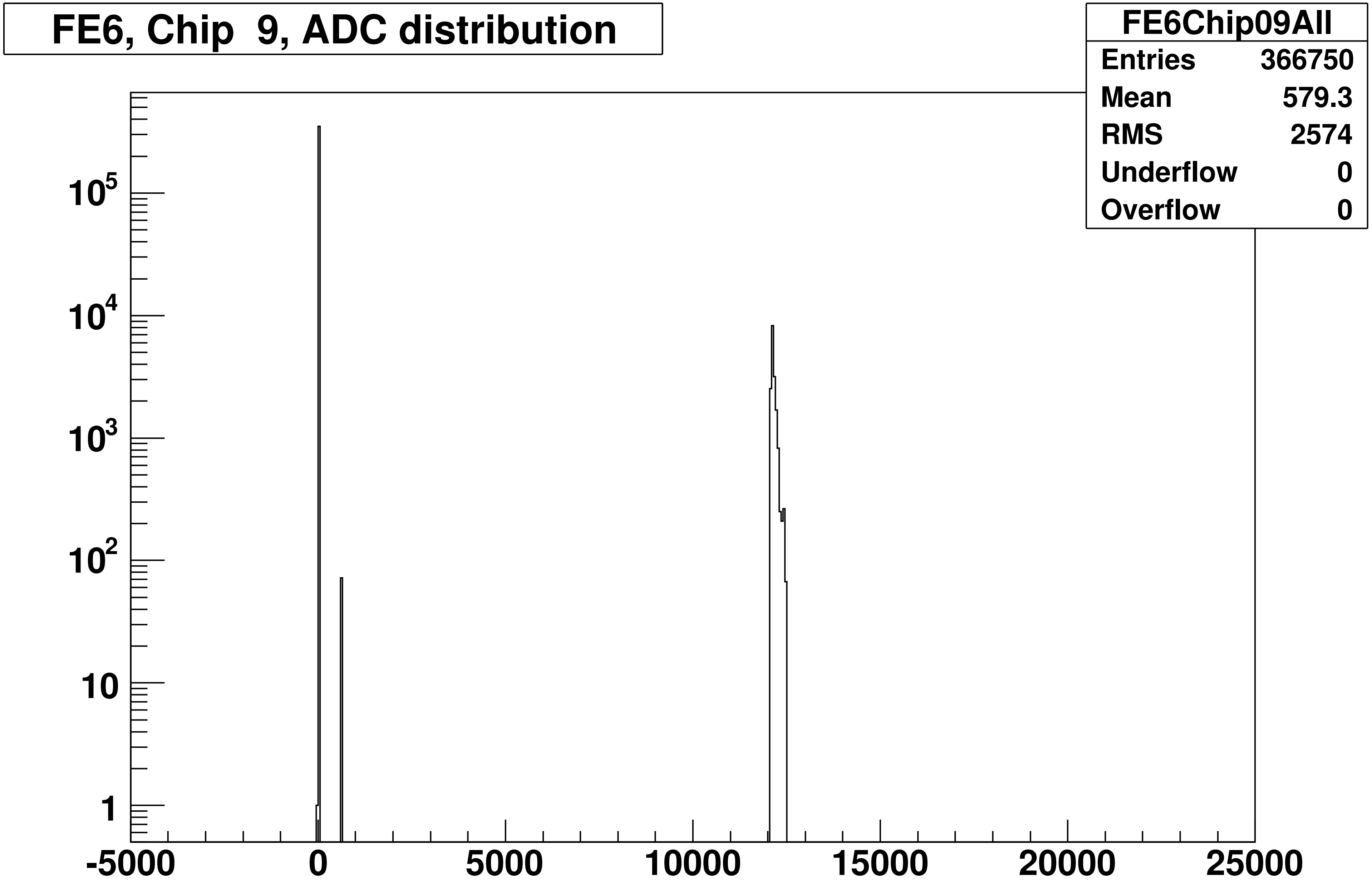


FE6, Chip 8, ADC distribution
FE6Chip08All
Entries 366750
Mean 559.1
RMS 2536
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000



FE6, Chip 8, ADC distribution
FE6Chip08Ped
Entries 366750
Mean 3.252
RMS 1.362
Underflow 0
Overflow 1.735e+04
10^5
10^4
10^3
-200
-150
-100
-50
0
50
100
150
200


FE6, Chip 8, ADC distribution
FE6Chip08Sig
Entries 366750
Mean 1.216e+04
RMS 52.63
Underflow 3.5e+05
Overflow 0
10^3
10^2
10000
10500
11000
11500
12000
12500
13000
13500
14000


FE6, Chip 9, ADC distribution
FE6Chip09All
Entries 366750
Mean 579.3
RMS 2574
Underflow 0
Overflow 0
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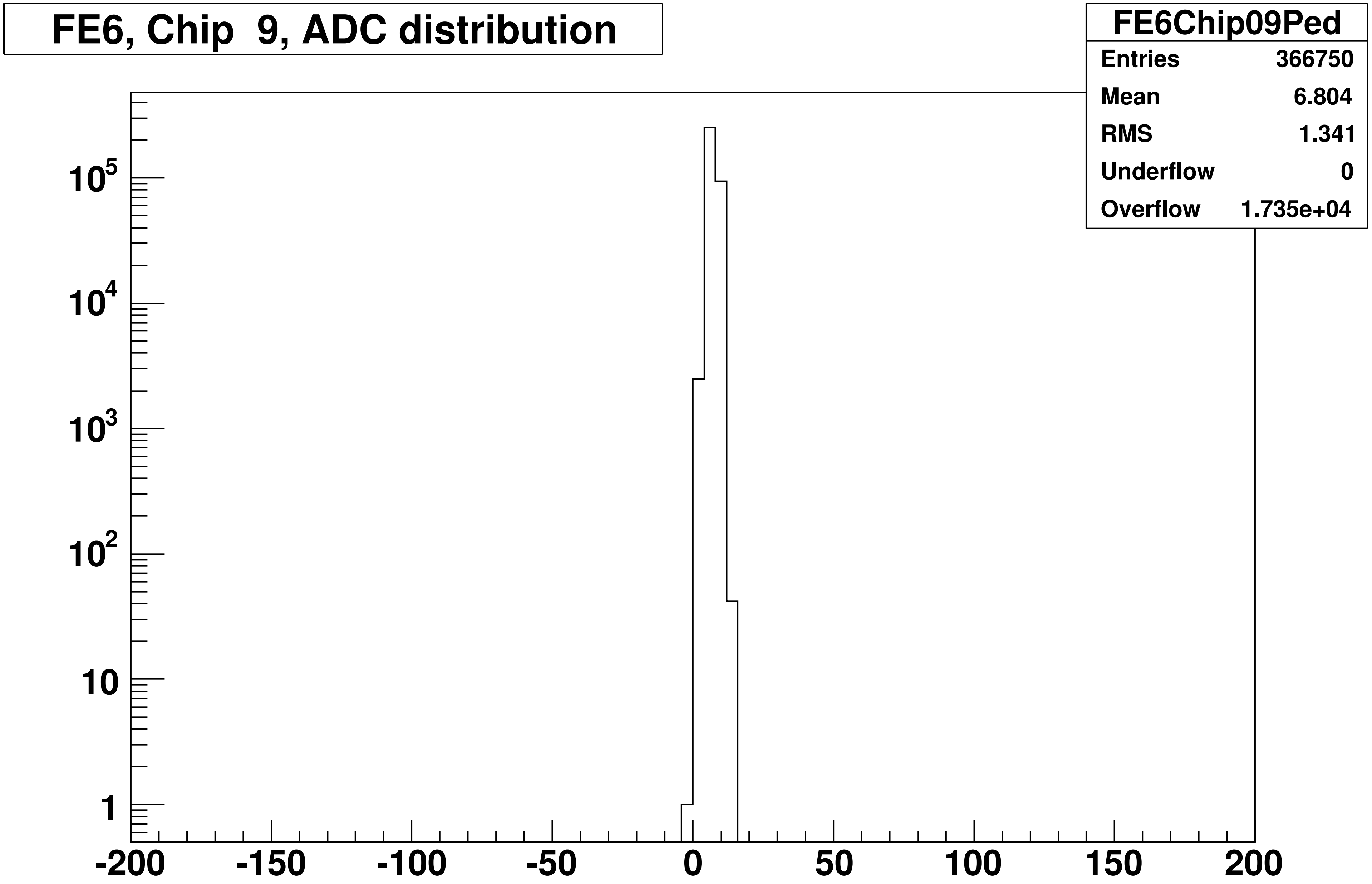
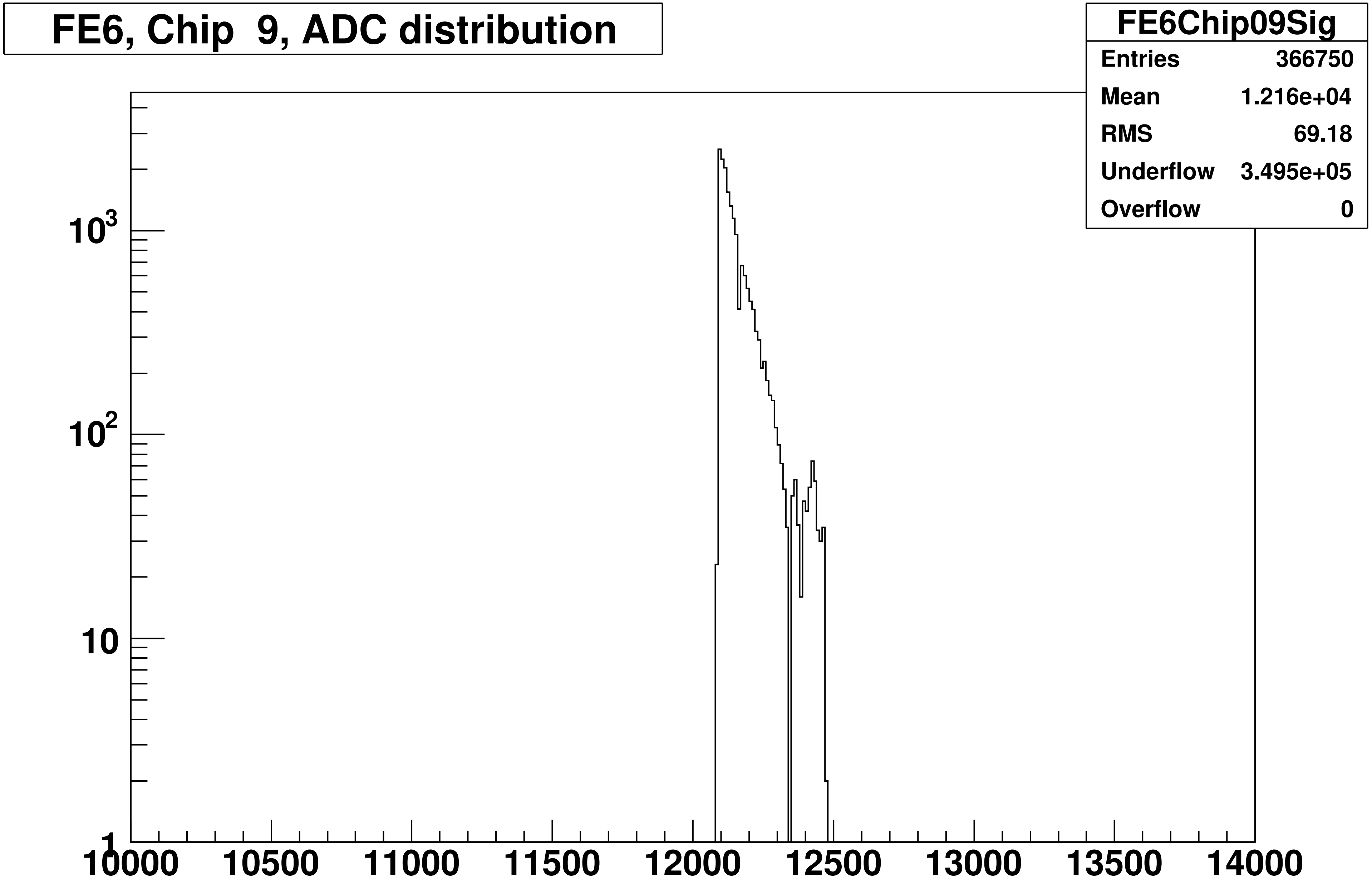
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE6, Chip 9, ADC distribution
FE6Chip09Ped
Entries 366750
Mean 6.804
RMS 1.341
Underflow 0
Overflow 1.735e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
200


FE6, Chip 9, ADC distribution
FE6Chip09Sig
Entries 366750
Mean 1.216e+04
RMS 69.18
Underflow 3.495e+05
Overflow 0
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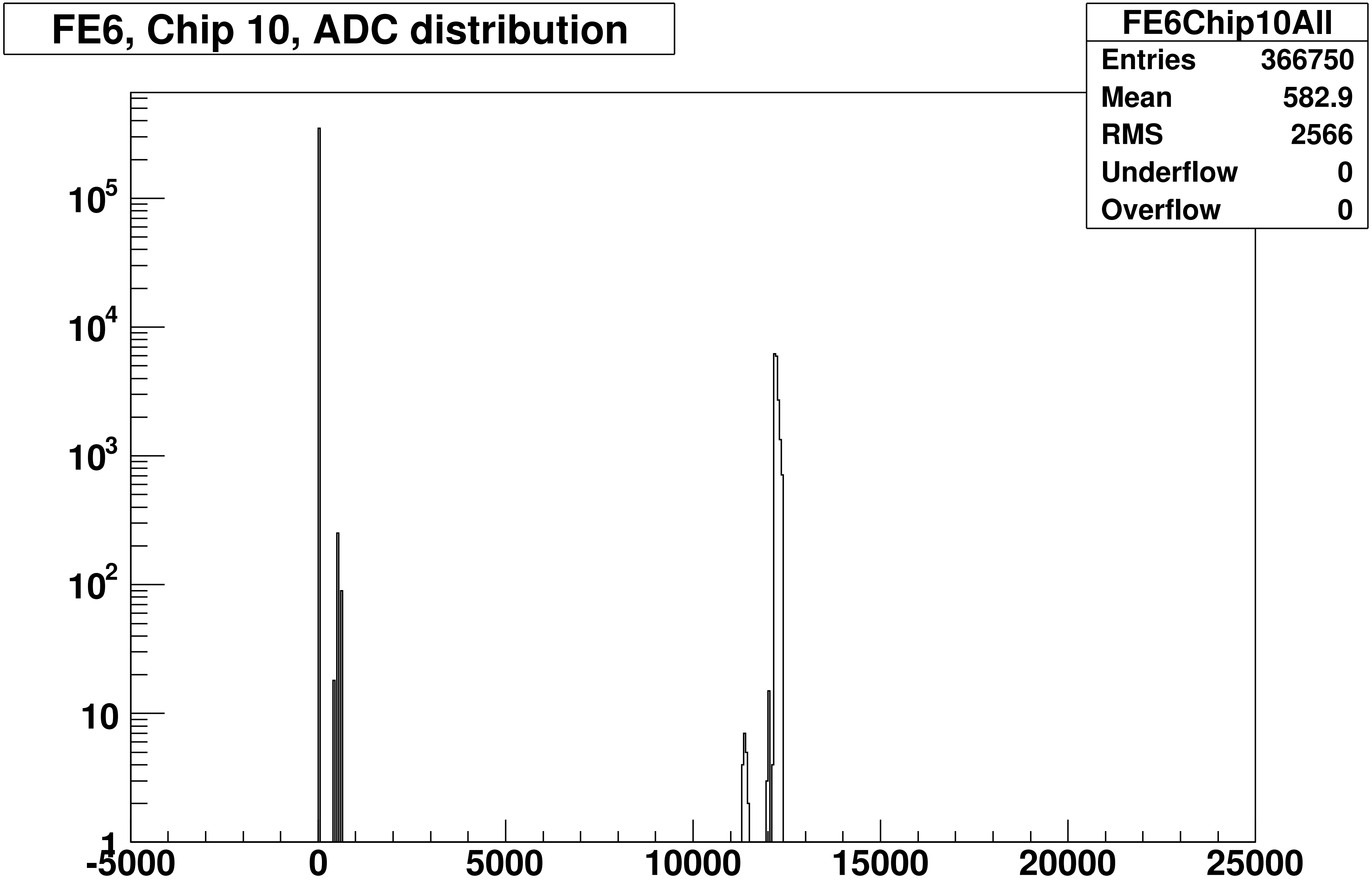
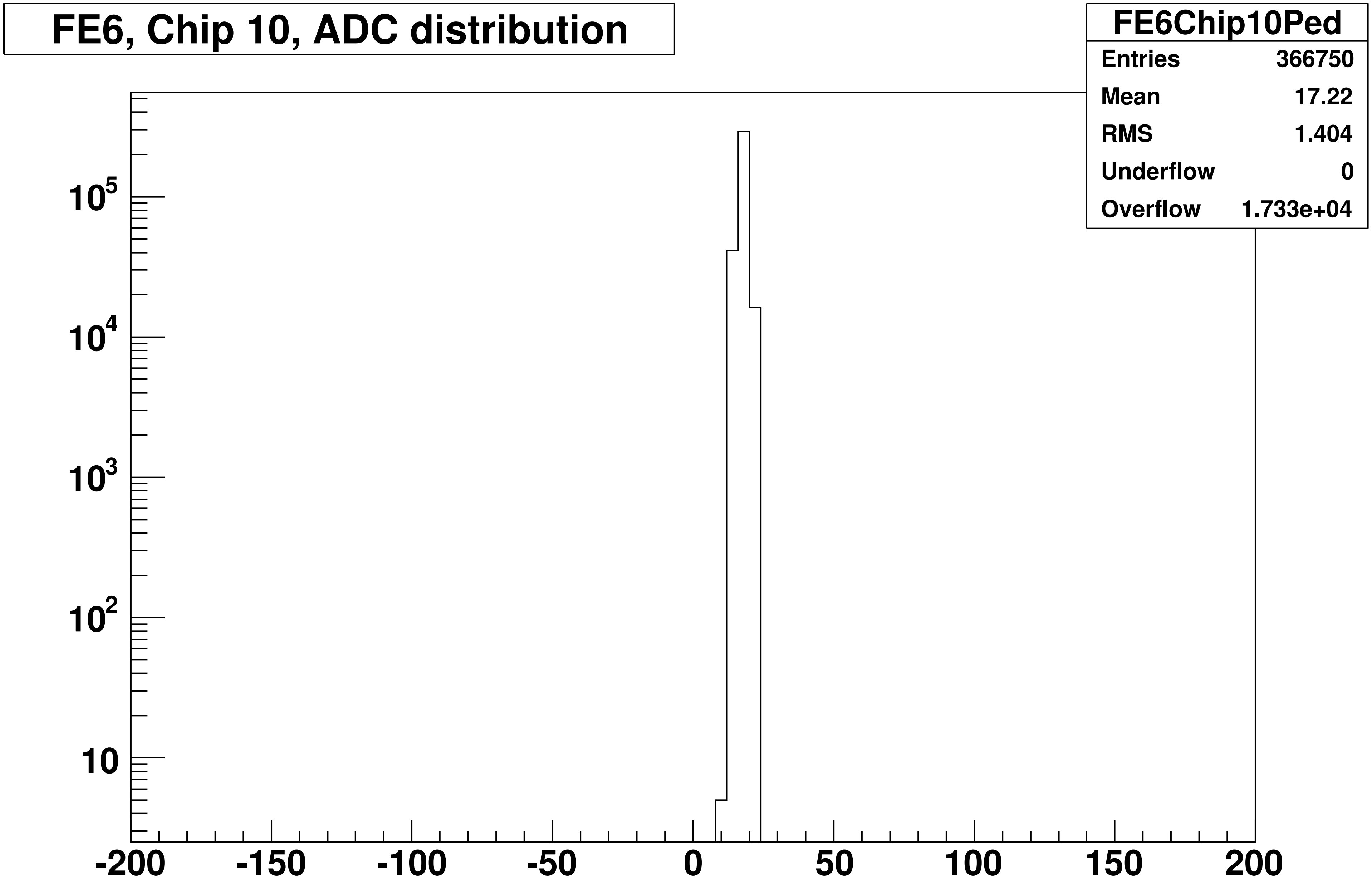
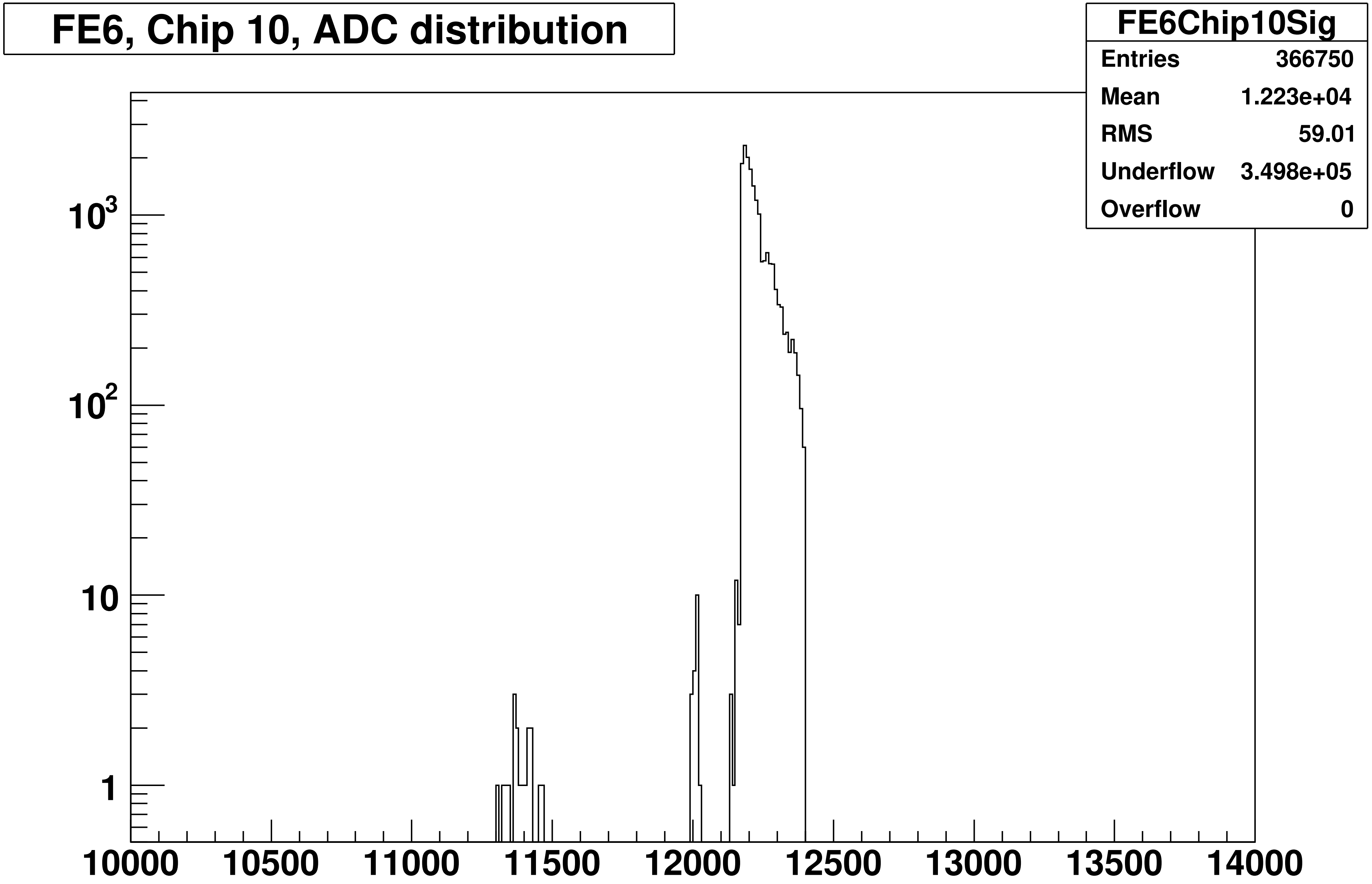
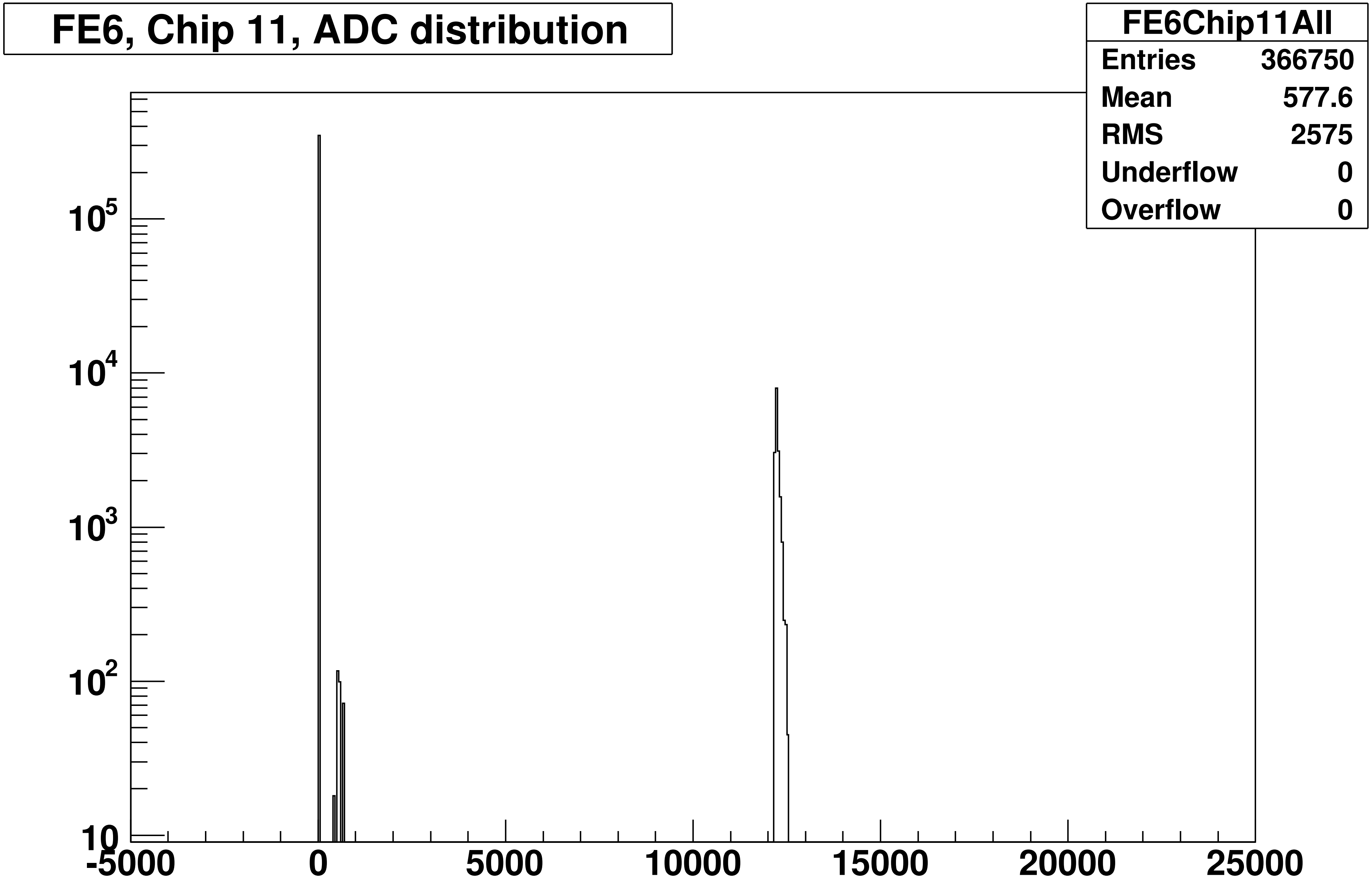
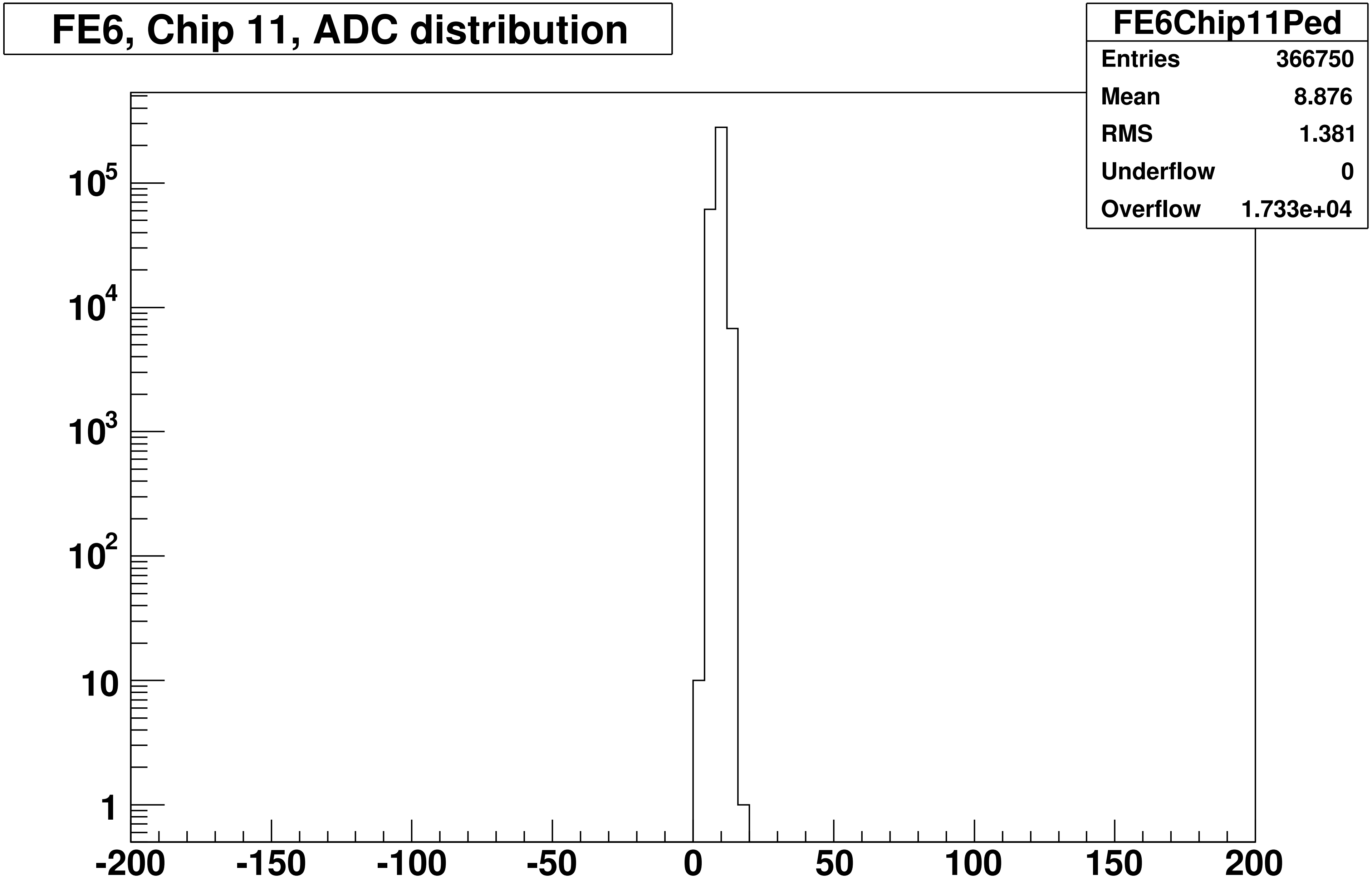
10^2
10
1
10000
10500
11000
11500
12000
12500
13000
13500
14000


FE6, Chip 10, ADC distribution
FE6Chip10All
Entries 366750
Mean 582.9
RMS 2566
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000

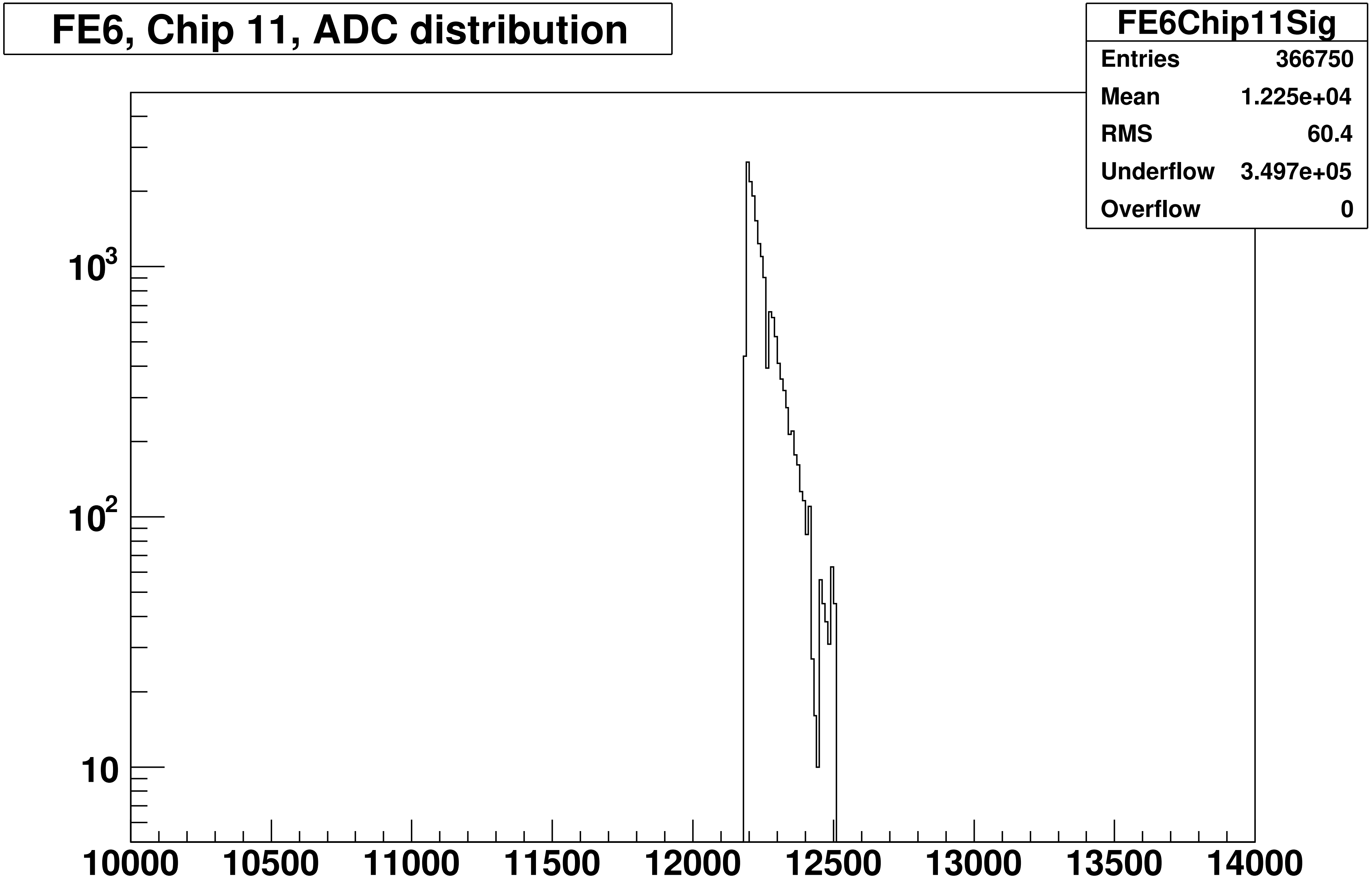

FE6, Chip 10, ADC distribution
FE6Chip10Ped
Entries 366750
Mean 17.22
RMS 1.404
Underflow 0
Overflow 1.733e+04
10
10^2
10^3
10^4
10^5
-200
-150
-100
-50
0
50
100
150
200

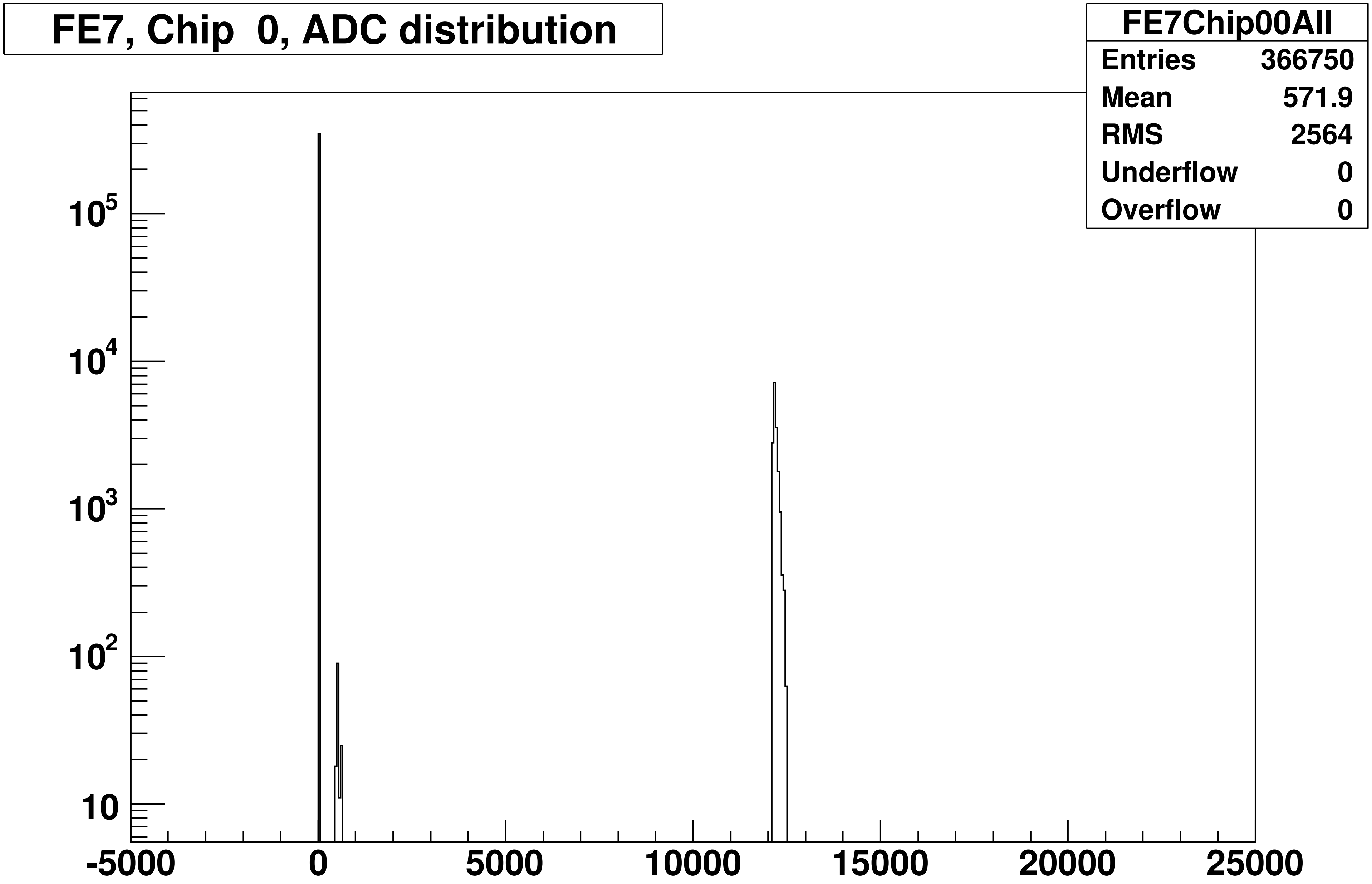

FE6, Chip 10, ADC distribution
FE6Chip10Sig
Entries 366750
Mean 1.223e+04
RMS 59.01
Underflow 3.498e+05
Overflow 0
10^3
10^2
10
1
10000
10500
11000
11500
12000
12500
13000
13500
14000


FE6, Chip 11, ADC distribution
FE6Chip11All
Entries 366750
Mean 577.6
RMS 2575
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000

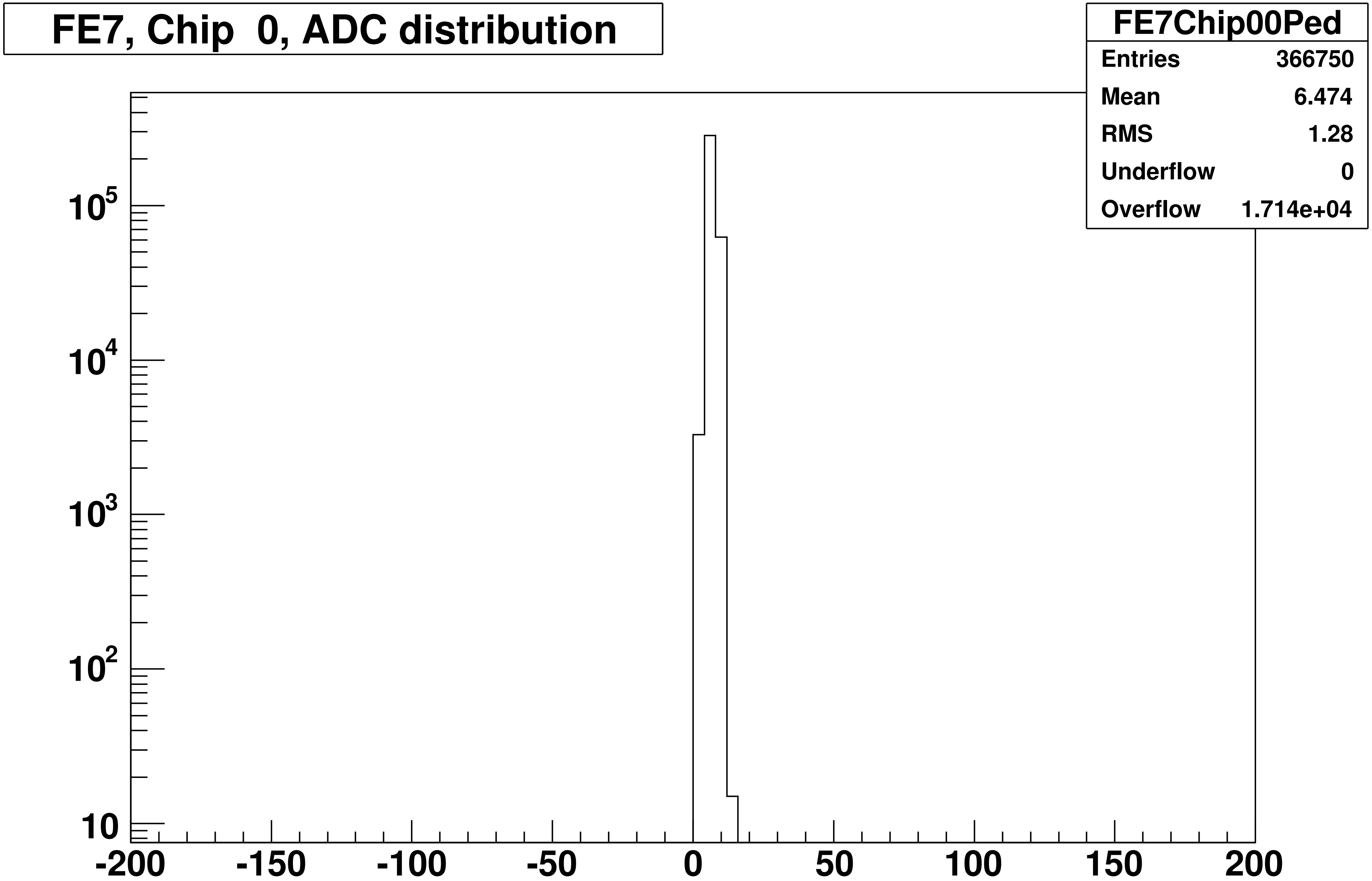


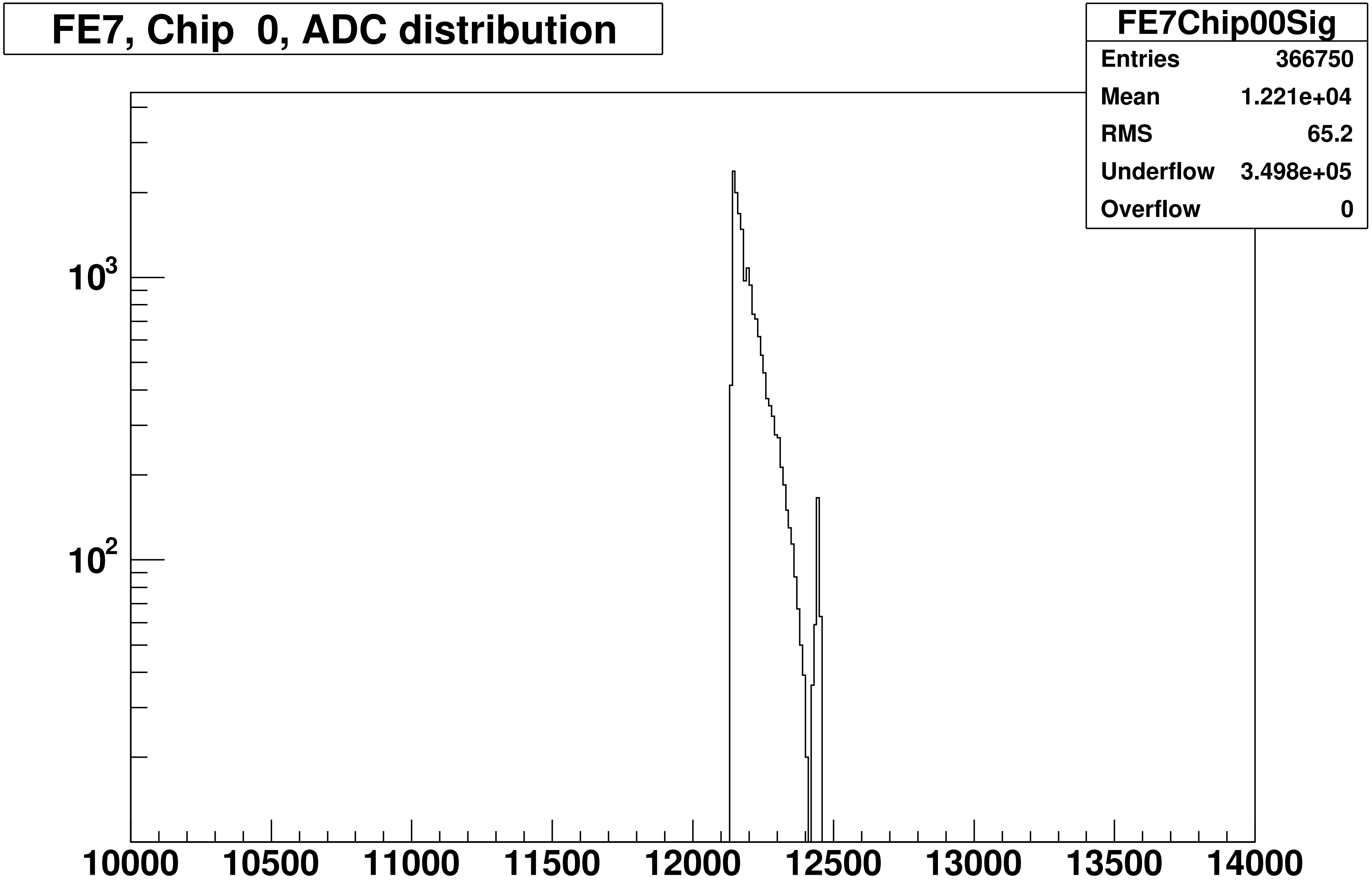
FE6, Chip 11, ADC distribution
FE6Chip11Ped
Entries 366750
Mean 8.876
RMS 1.381
Underflow 0
Overflow 1.733e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
200

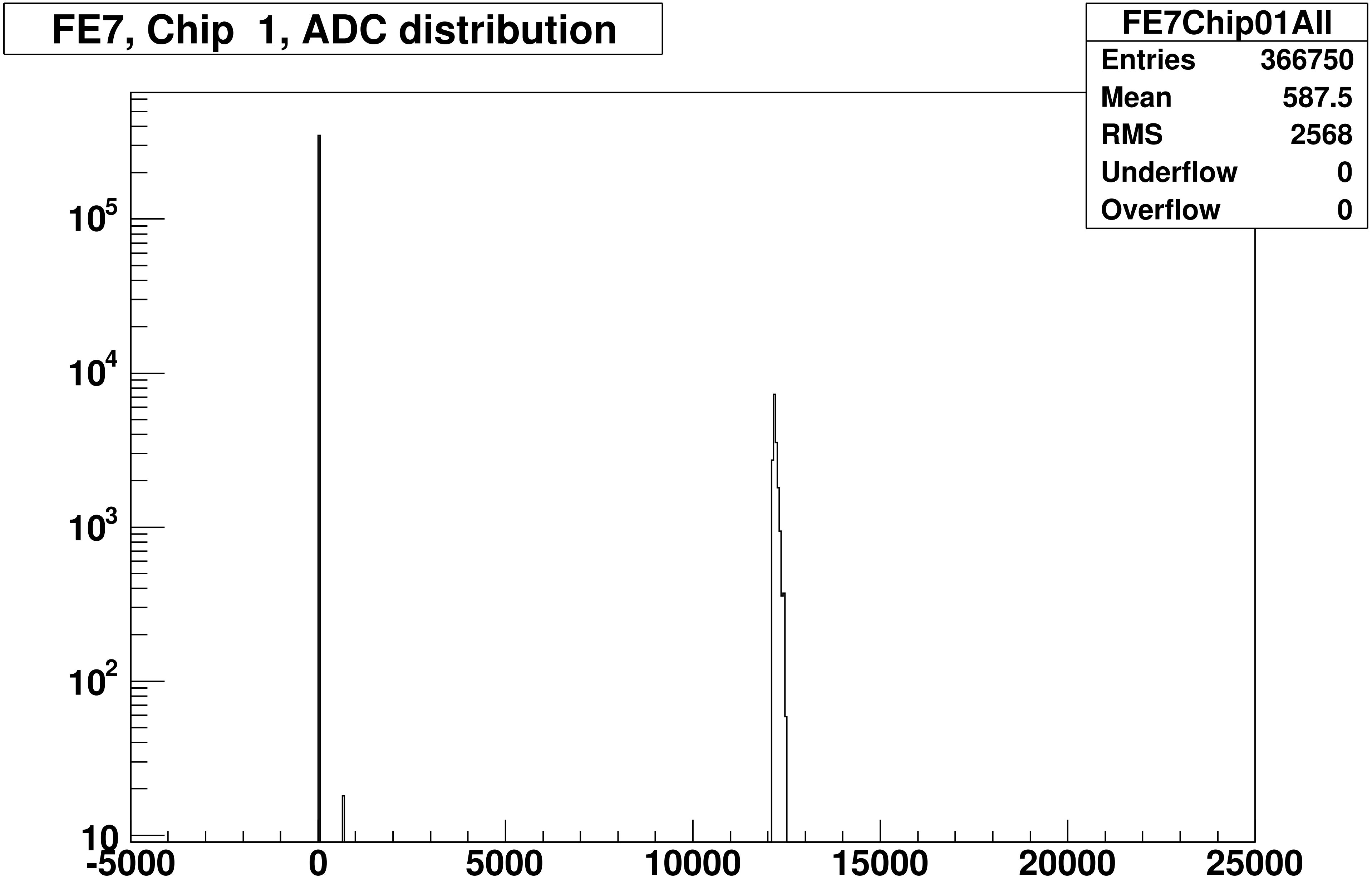

FE6, Chip 11, ADC distribution
FE6Chip11Sig
Entries 366750
Mean 1.225e+04
RMS 60.4
Underflow 3.497e+05
Overflow 0
10
10^2
10^3
10000
10500
11000
11500
12000
12500
13000
13500
14000

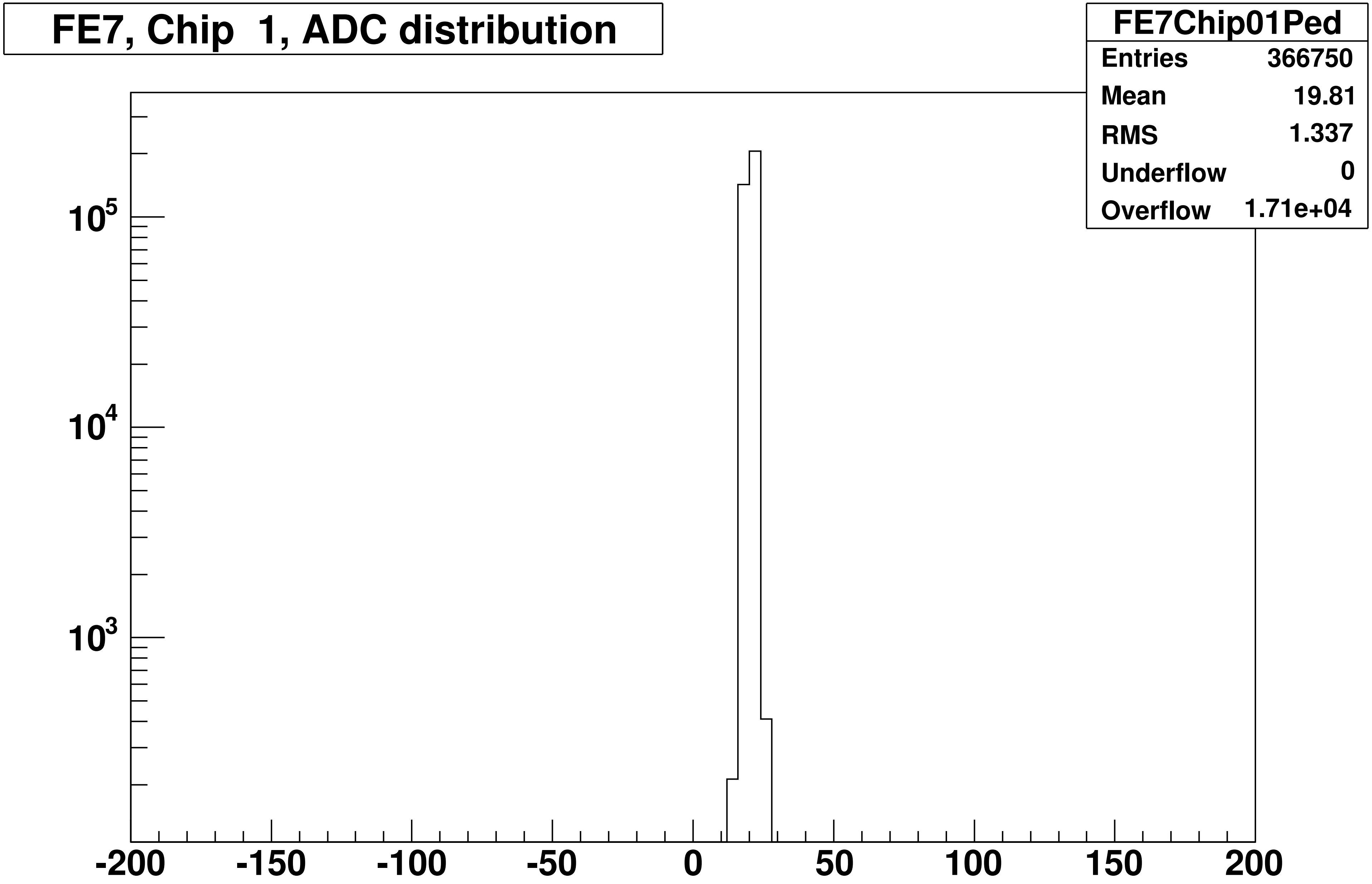


FE7, Chip 0, ADC distribution
FE7Chip00All
Entries 366750
Mean 571.9
RMS 2564
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000

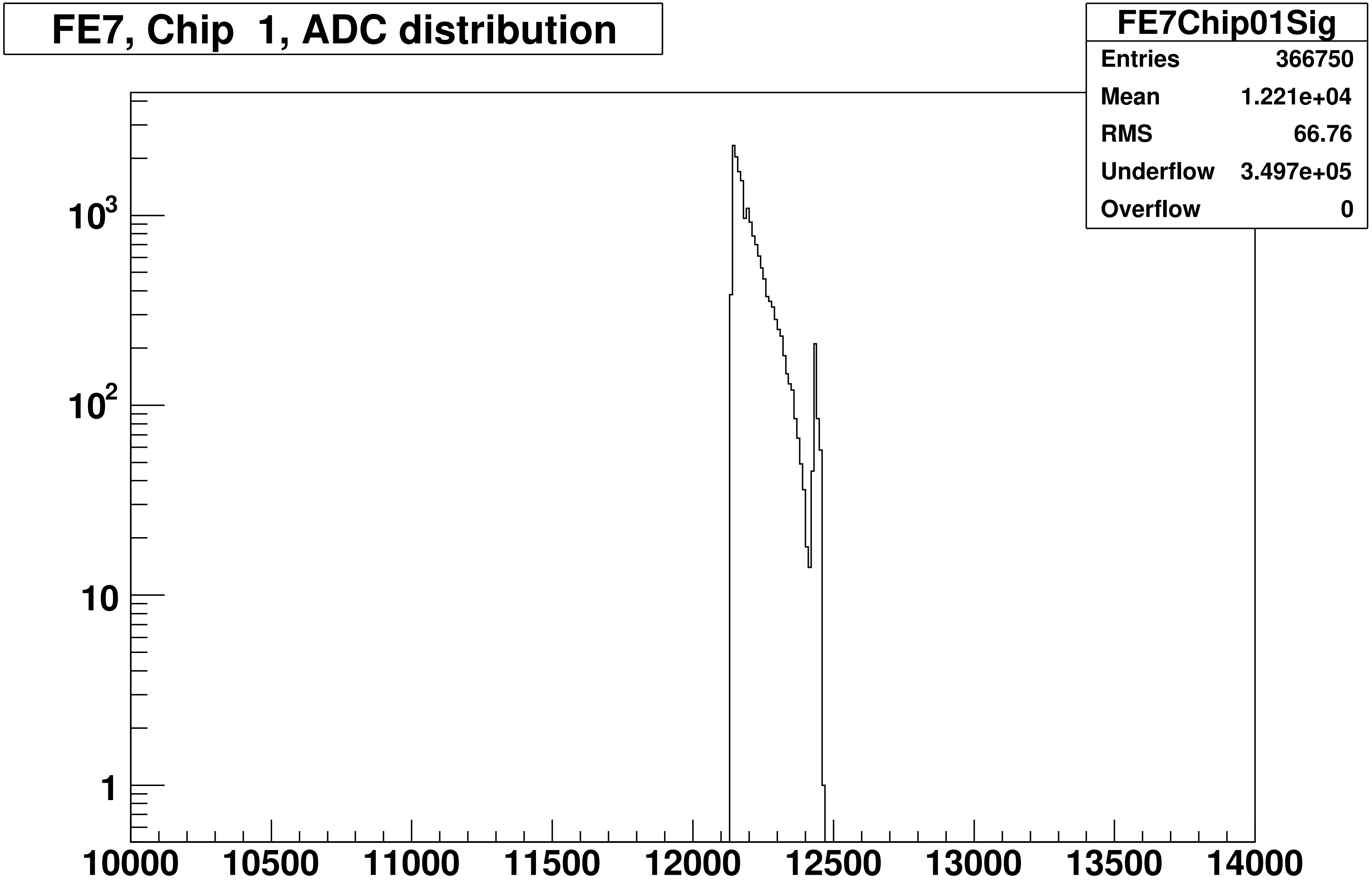

FE7, Chip 0, ADC distribution
FE7Chip00Ped
Entries 366750
Mean 6.474
RMS 1.28
Underflow 0
Overflow 1.714e+04
10
10^2
10^3
10^4
10^5
-200
-150
-100
-50
0
50
100
150
200


FE7, Chip 0, ADC distribution
FE7Chip00Sig
Entries 366750
Mean 1.221e+04
RMS 65.2
Underflow 3.498e+05
Overflow 0
10^3
10^2
10000
10500
11000
11500
12000
12500
13000
13500
14000

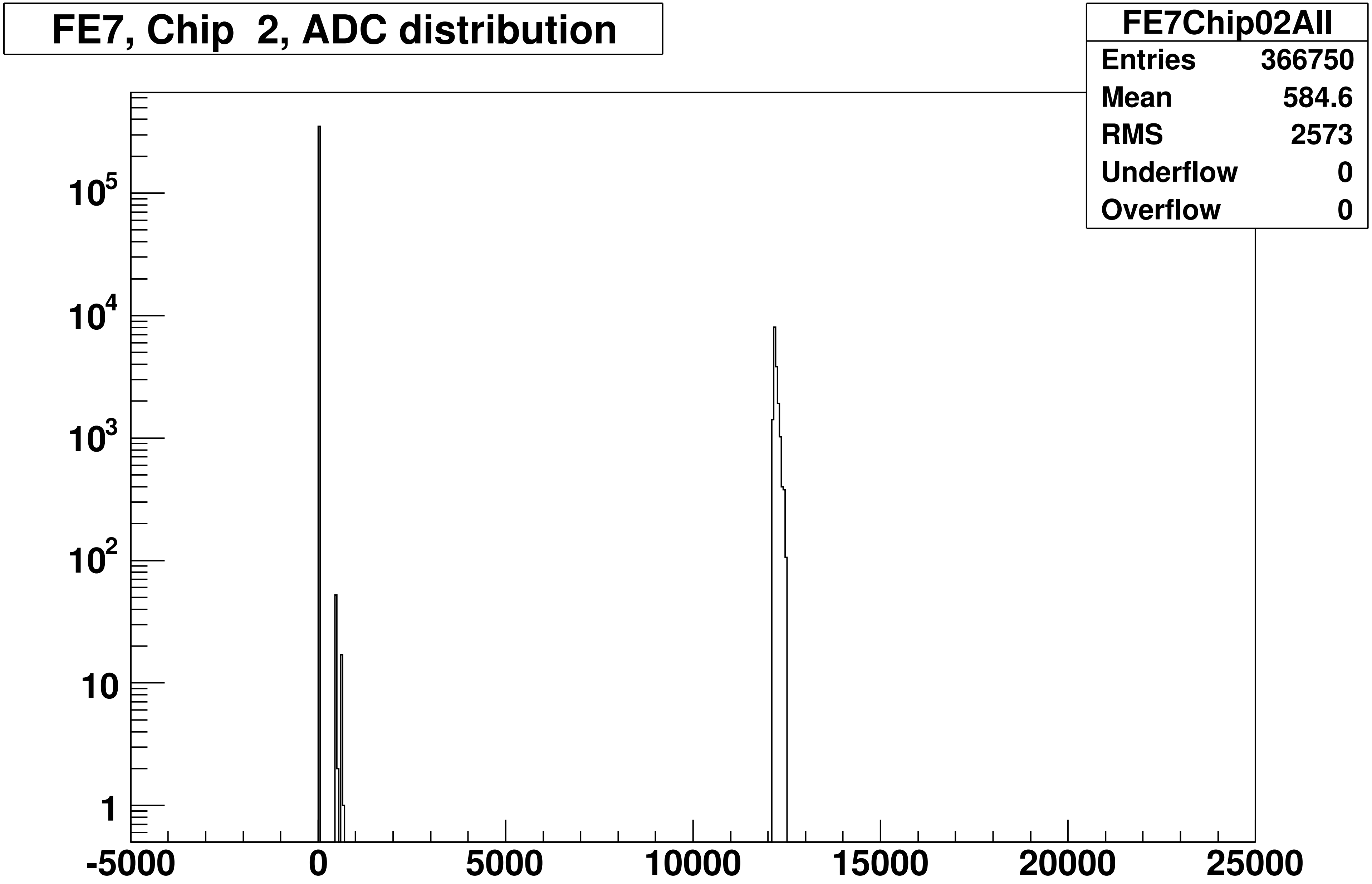

FE7, Chip 1, ADC distribution
FE7Chip01All
Entries 366750
Mean 587.5
RMS 2568
Underflow 0
Overflow 0
10
10^2
10^3
10^4
10^5
-5000
0
5000
10000
15000
20000
25000

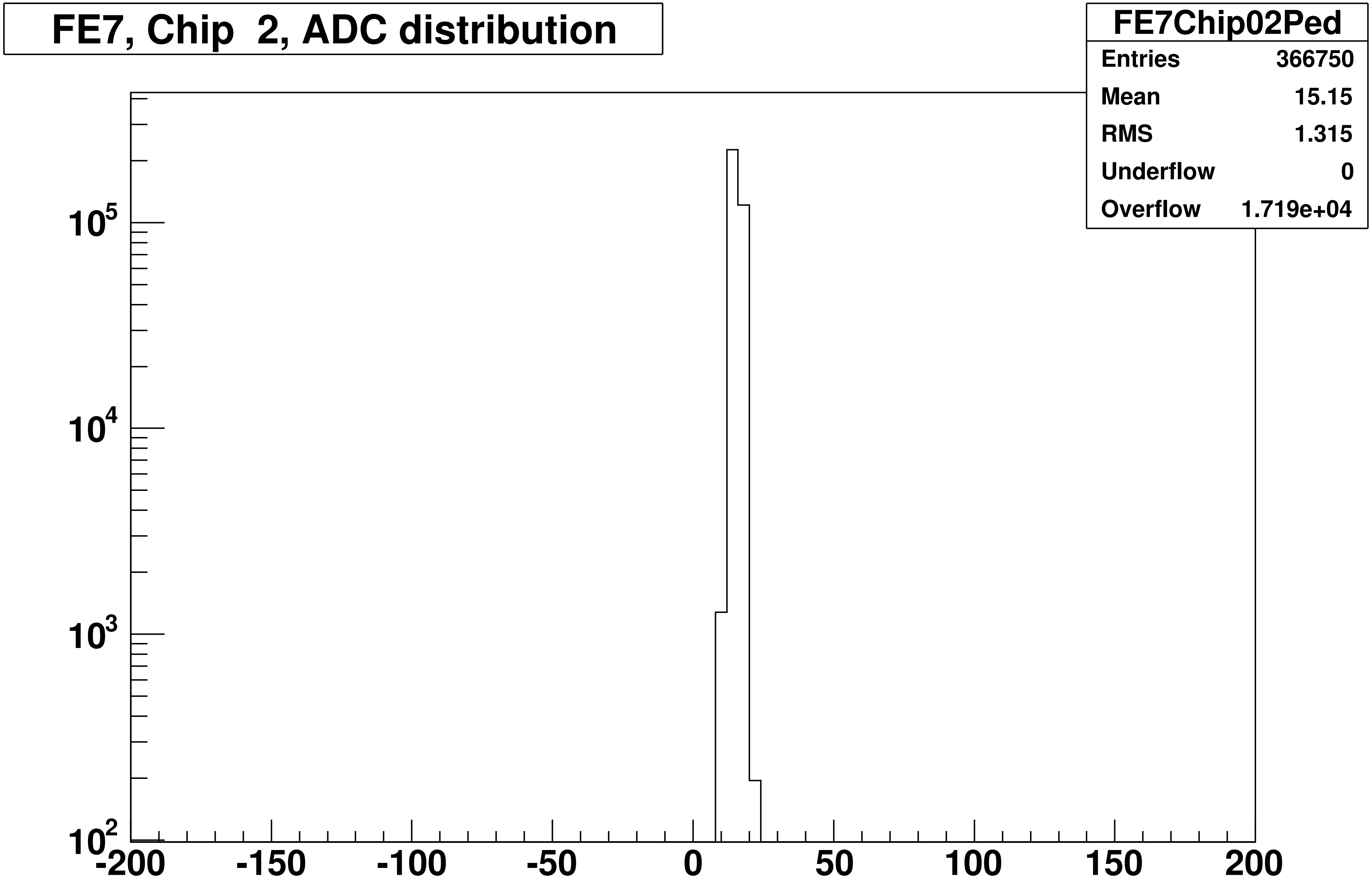


FE7, Chip 1, ADC distribution
FE7Chip01Ped
Entries 366750
Mean 19.81
RMS 1.337
Underflow 0
Overflow 1.71e+04
10^5
10^4
10^3
-200
-150
-100
-50
0
50
100
150
200

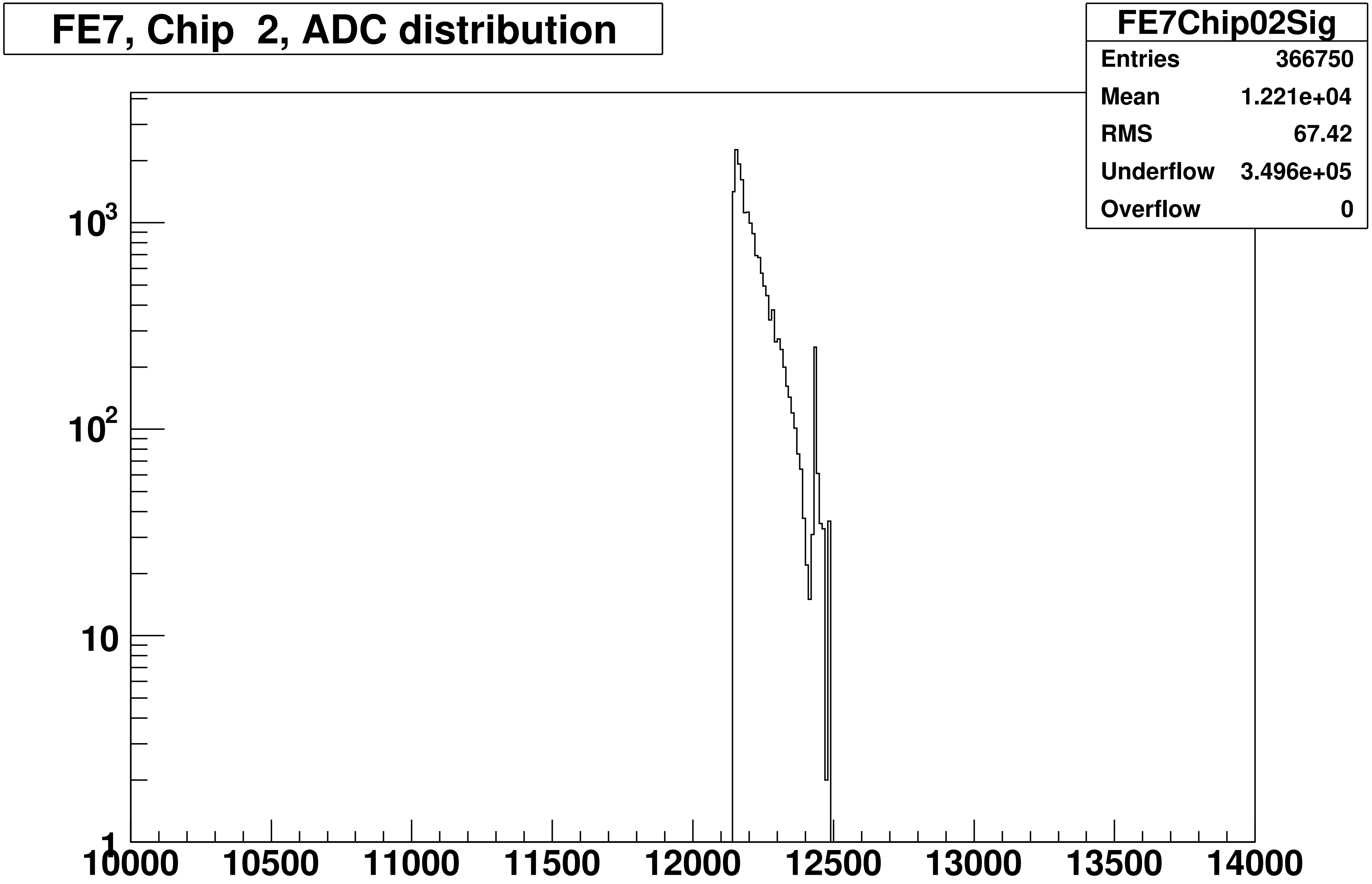


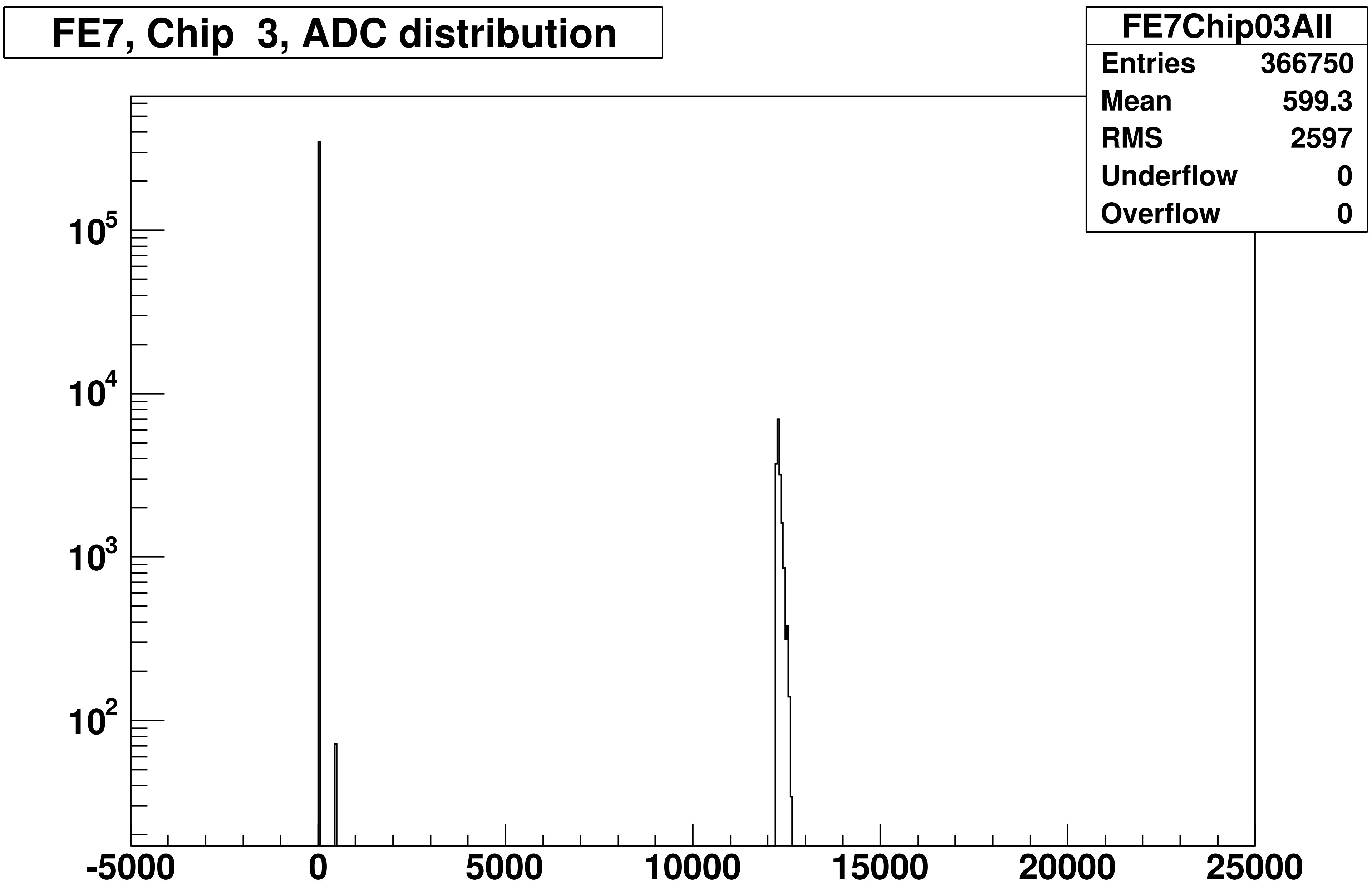
FE7, Chip 1, ADC distribution
FE7Chip01Sig
Entries 366750
Mean 1.221e+04
RMS 66.76
Underflow 3.497e+05
Overflow 0
10^3
10^2
10
1
10000
10500
11000
11500
12000
12500
13000
13500
14000

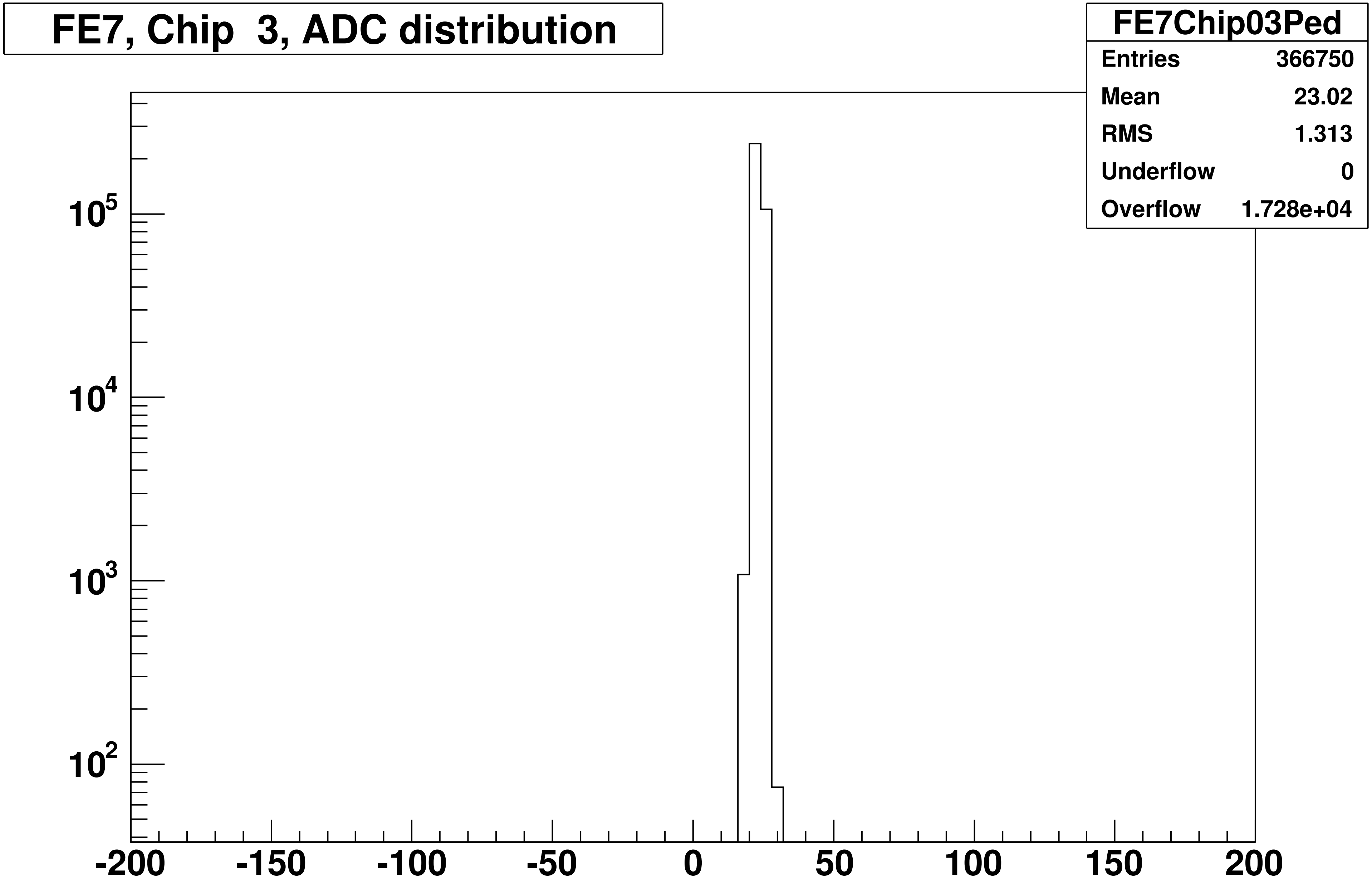

FE7, Chip 2, ADC distribution
FE7Chip02All
Entries 366750
Mean 584.6
RMS 2573
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000

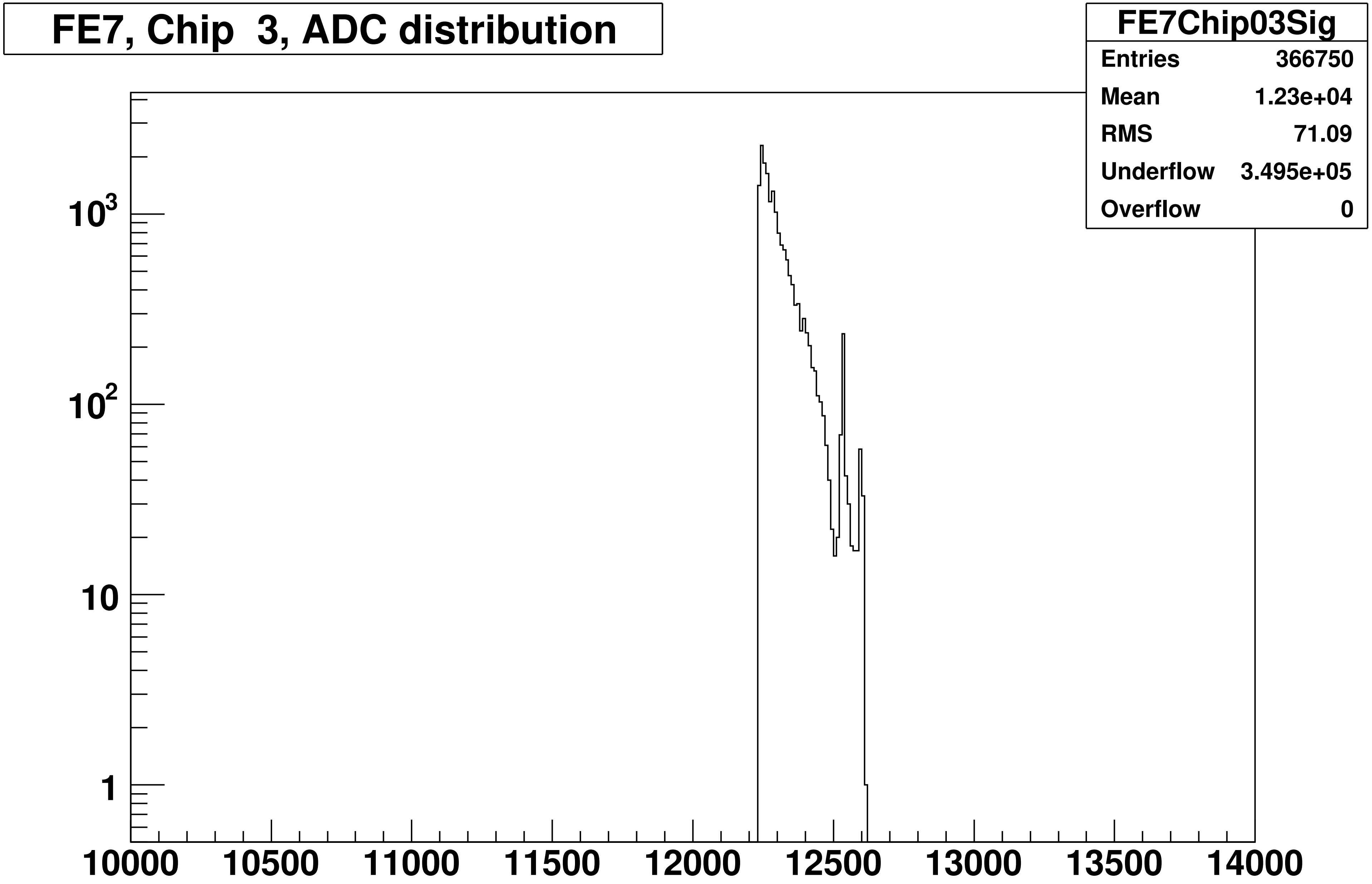


FE7, Chip 2, ADC distribution
FE7Chip02Ped
Entries 366750
Mean 15.15
RMS 1.315
Underflow 0
Overflow 1.719e+04
10^5
10^4
10^3
10^2
-200
-150
-100
-50
0
50
100
150
200

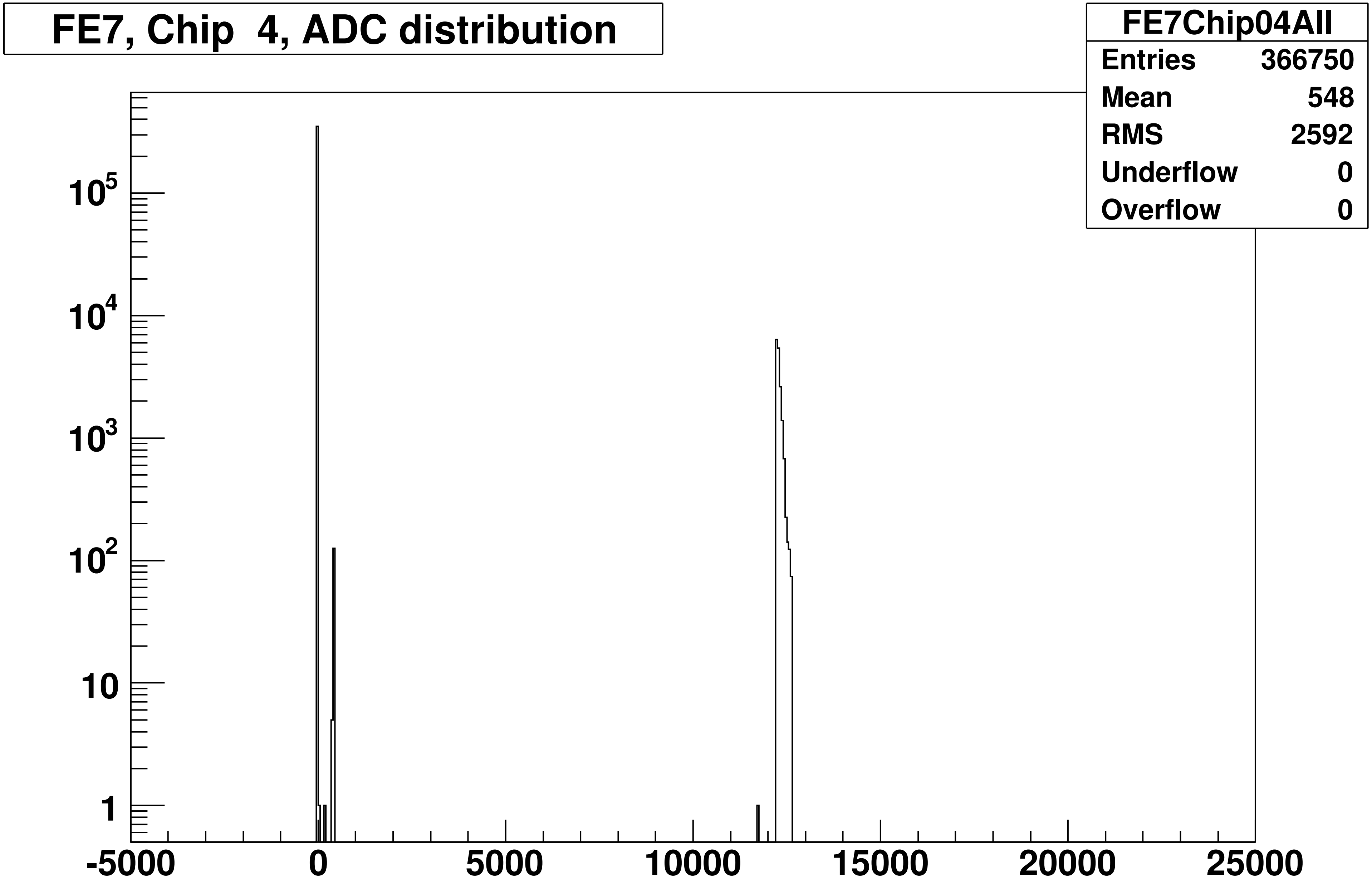

FE7, Chip 2, ADC distribution
FE7Chip02Sig
Entries 366750
Mean 1.221e+04
RMS 67.42
Underflow 3.496e+05
Overflow 0
10^3
10^2
10
1
10000
10500
11000
11500
12000
12500
13000
13500
14000


FE7, Chip 3, ADC distribution
FE7Chip03All
Entries 366750
Mean 599.3
RMS 2597
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000

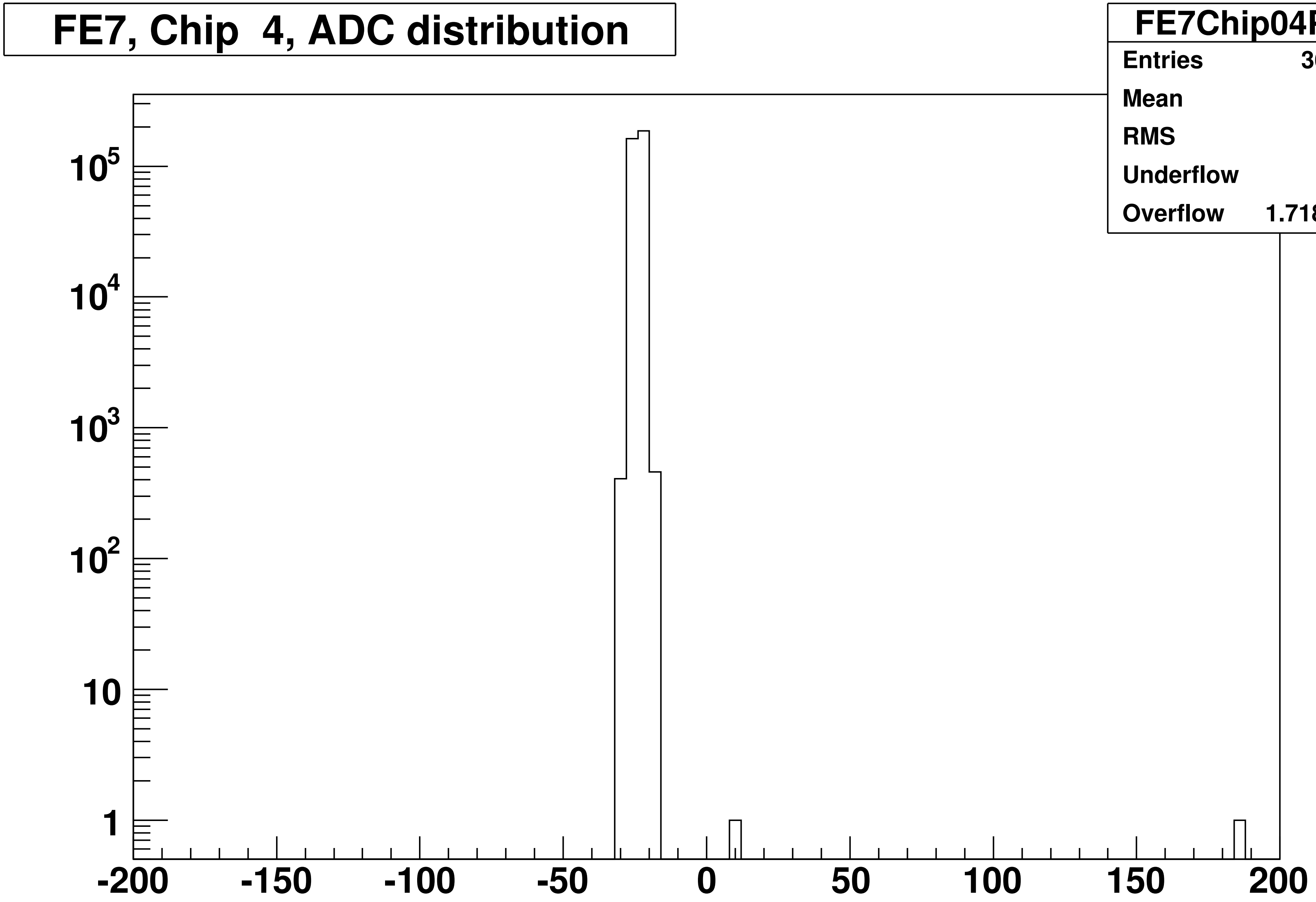

FE7, Chip 3, ADC distribution
FE7Chip03Ped
Entries 366750
Mean 23.02
RMS 1.313
Underflow 0
Overflow 1.728e+04
10^5
10^4
10^3
10^2
-200
-150
-100
-50
0
50
100
150
200



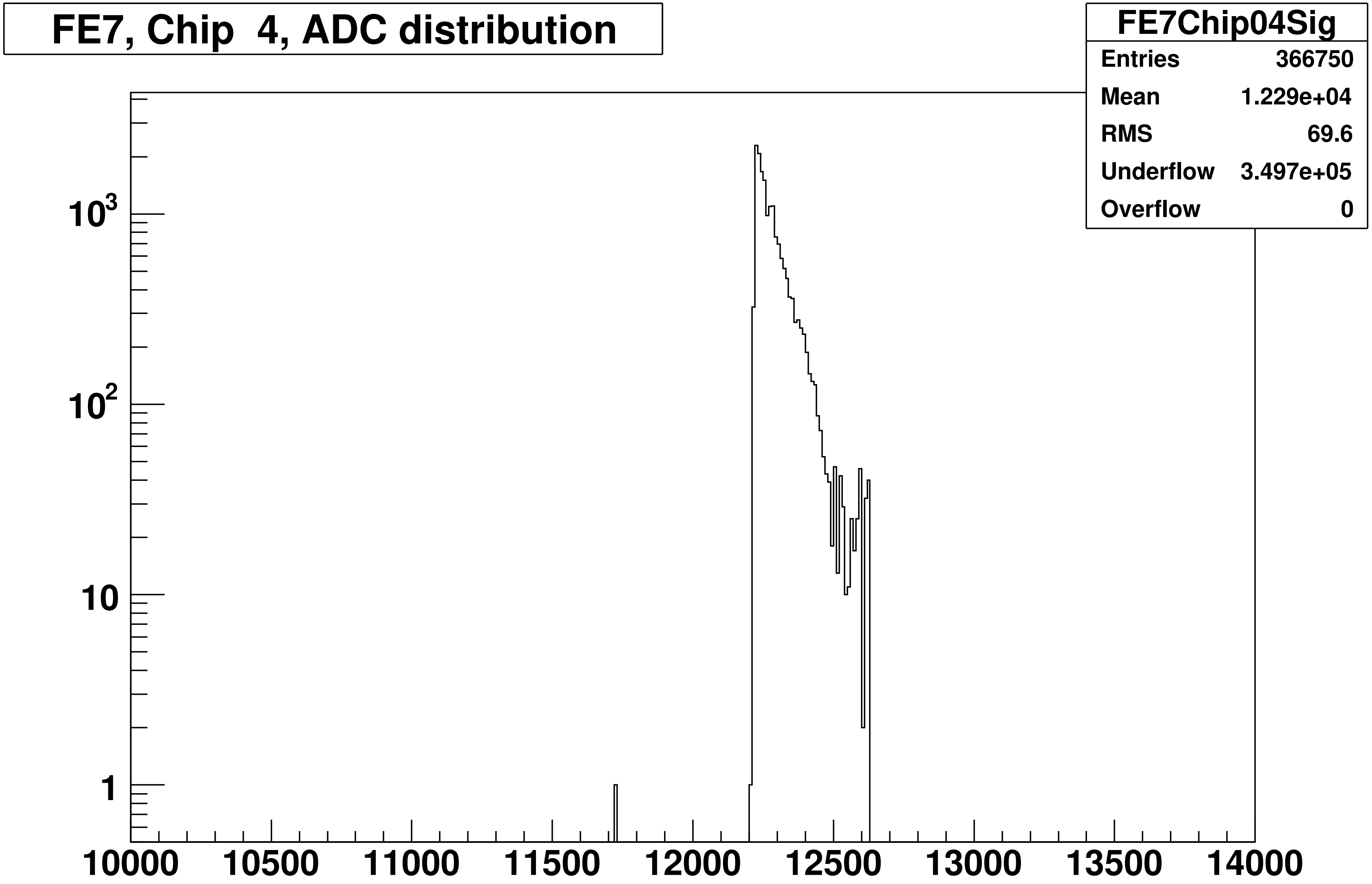
FE7, Chip 3, ADC distribution
FE7Chip03Sig
Entries 366750
Mean 1.23e+04
RMS 71.09
Underflow 3.495e+05
Overflow 0
10^3
10^2
10
1
10000
10500
11000
11500
12000
12500
13000
13500
14000



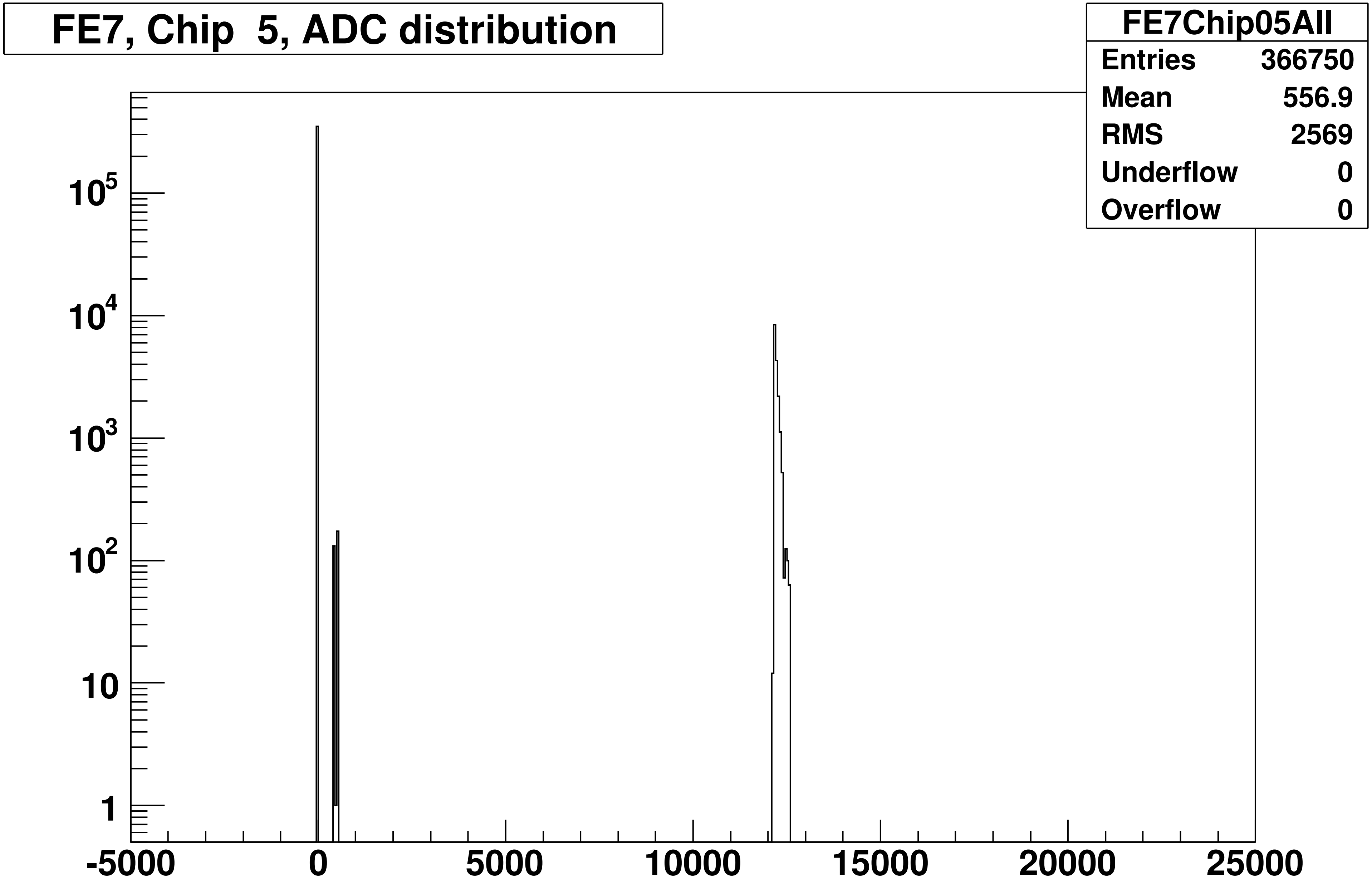
FE7, Chip 4, ADC distribution
FE7Chip04All
Entries 366750
Mean 548
RMS 2592
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000

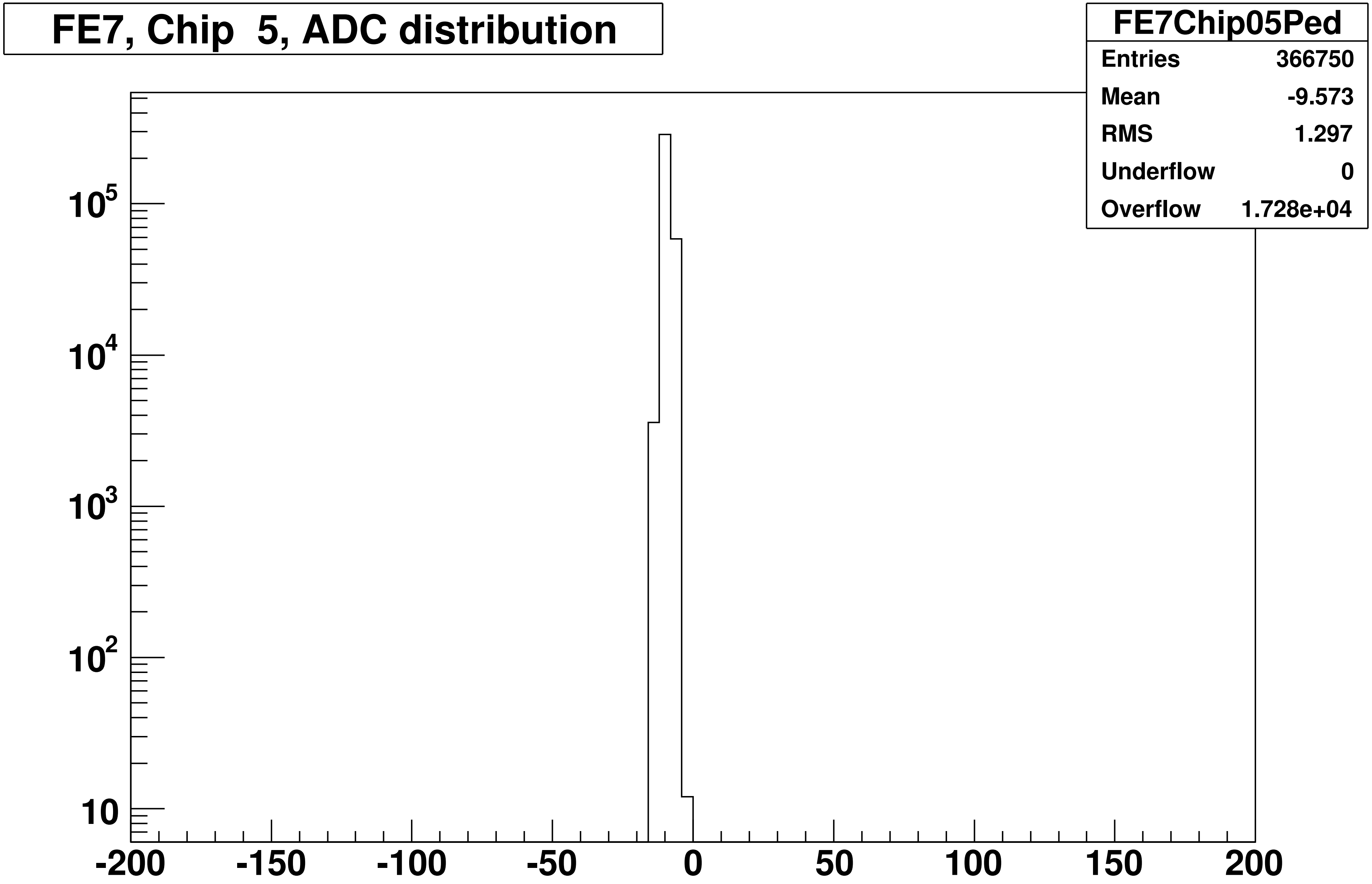


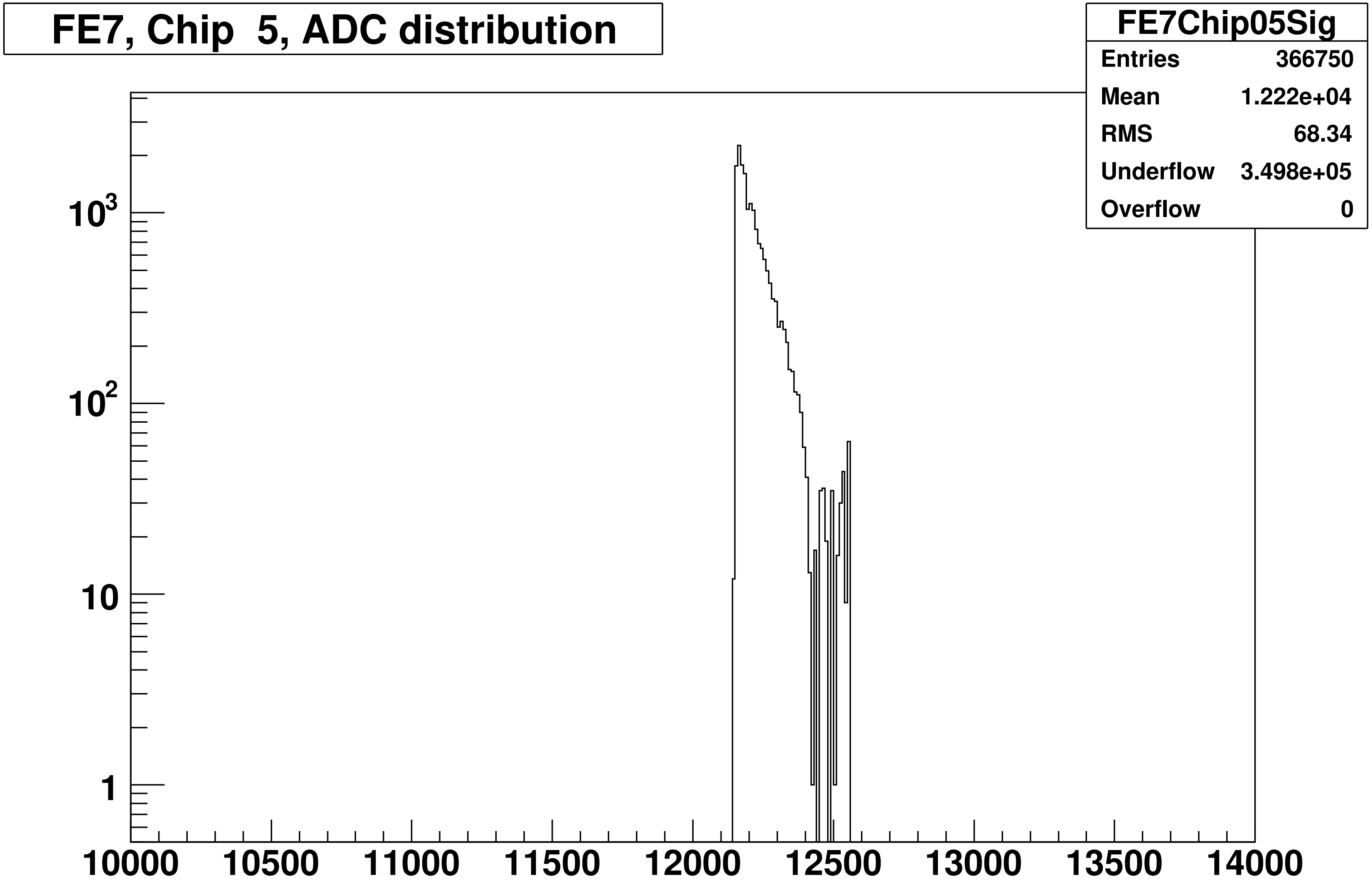
FE7, Chip 4, ADC distribution
FE7Chip04Ped
Entries 366750
Mean -24.4
RMS 1.432
Underflow 0
Overflow 1.718e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
200

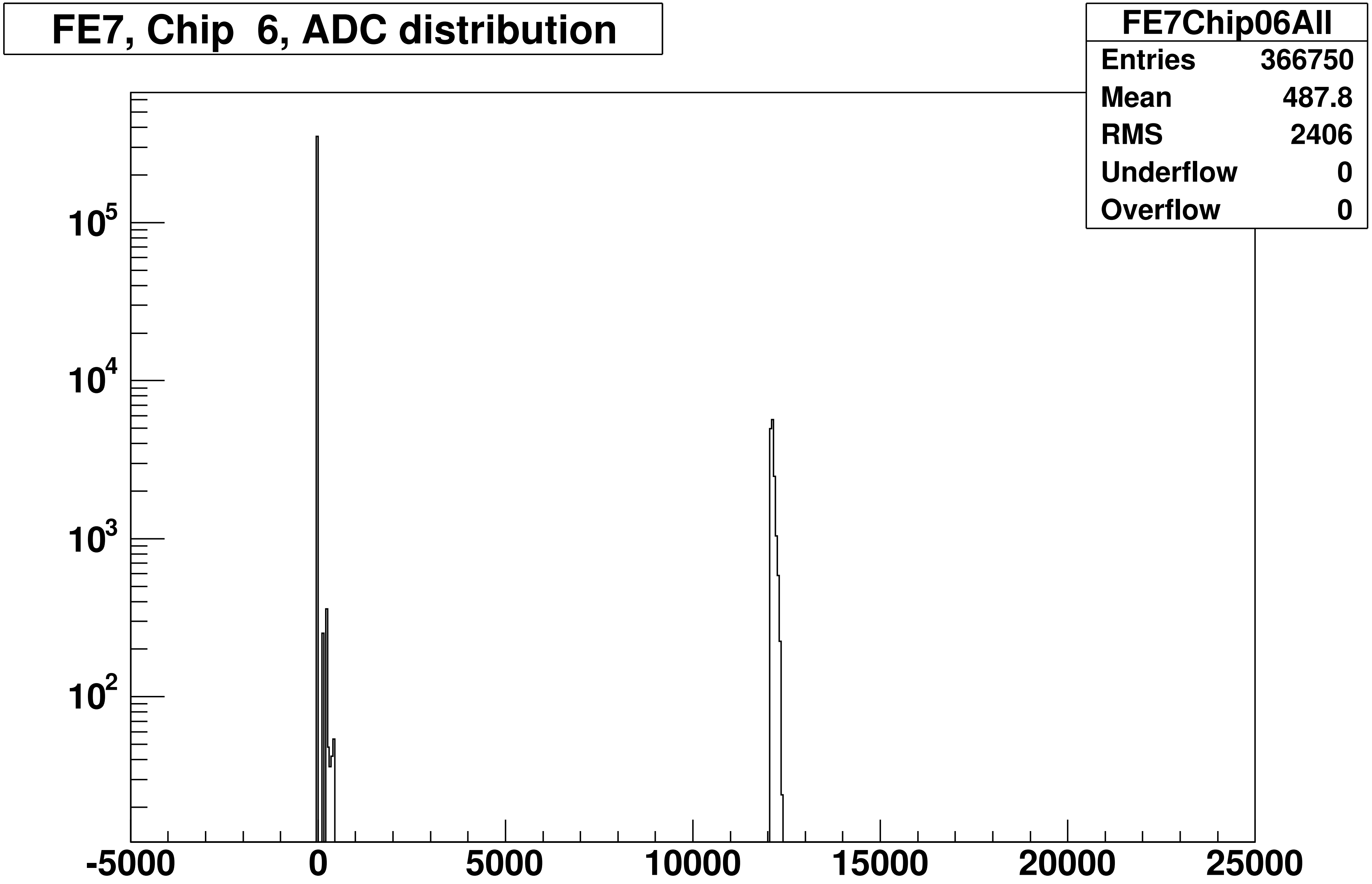


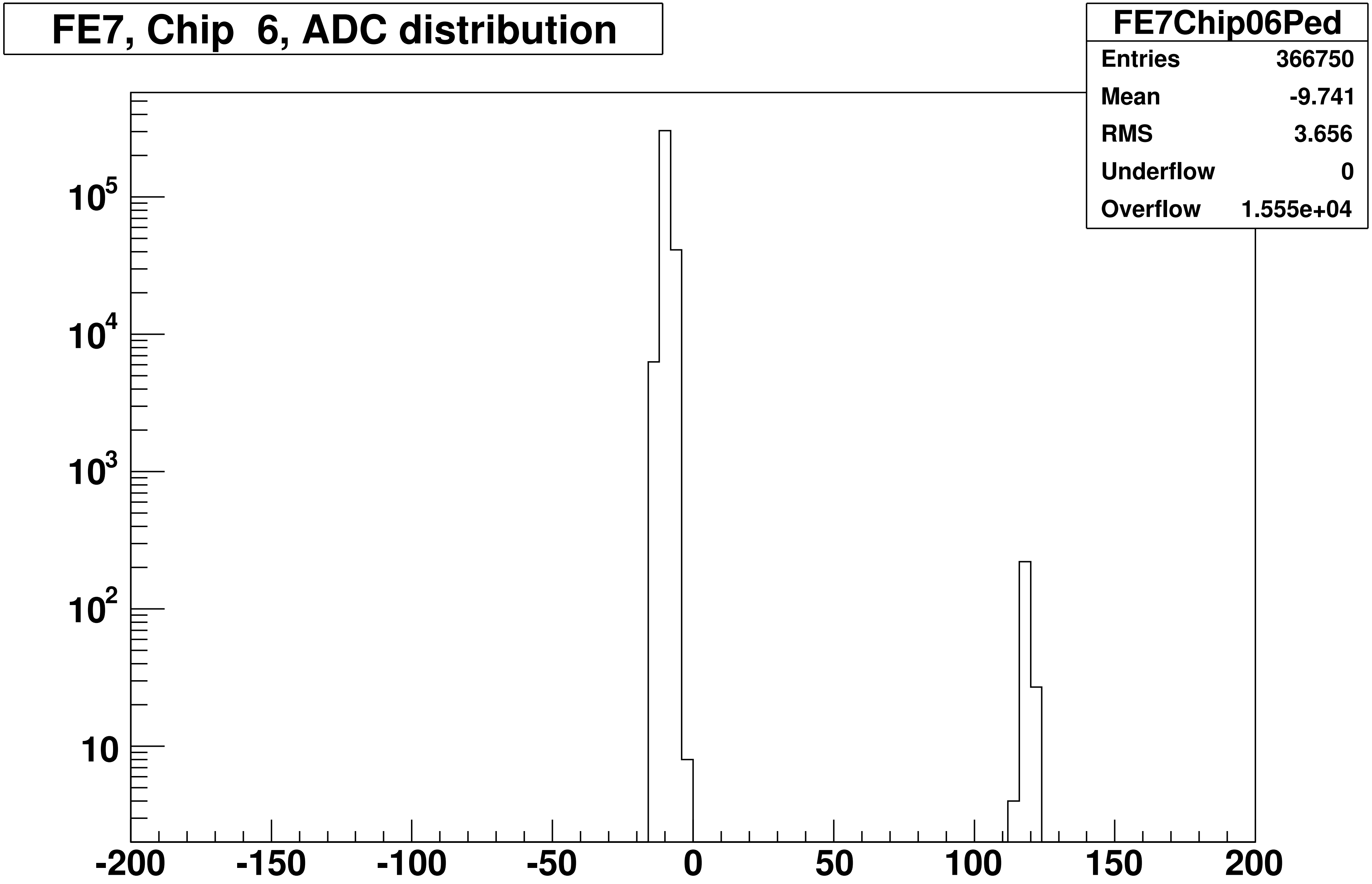
FE7, Chip 4, ADC distribution
FE7Chip04Sig
Entries 366750
Mean 1.229e+04
RMS 69.6
Underflow 3.497e+05
Overflow 0
10³
10²
10
1
10000 10500 11000 11500 12000 12500 13000 13500 14000


FE7, Chip 5, ADC distribution
FE7Chip05All
Entries 366750
Mean 556.9
RMS 2569
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE7, Chip 5, ADC distribution
FE7Chip05Ped
Entries 366750
Mean -9.573
RMS 1.297
Underflow 0
Overflow 1.728e+04
10^5
10^4
10^3
10^2
10
-200 -150 -100 -50 0 50 100 150 200


FE7, Chip 5, ADC distribution
FE7Chip05Sig
Entries 366750
Mean 1.222e+04
RMS 68.34
Underflow 3.498e+05
Overflow 0
10^3
10^2
10
1
10000
10500
11000
11500
12000
12500
13000
13500
14000


FE7, Chip 6, ADC distribution
FE7Chip06All
Entries 366750
Mean 487.8
RMS 2406
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000


FE7, Chip 6, ADC distribution
FE7Chip06Ped
Entries 366750
Mean -9.741
RMS 3.656
Underflow 0
Overflow 1.555e+04
10^5
10^4
10^3
10^2
10
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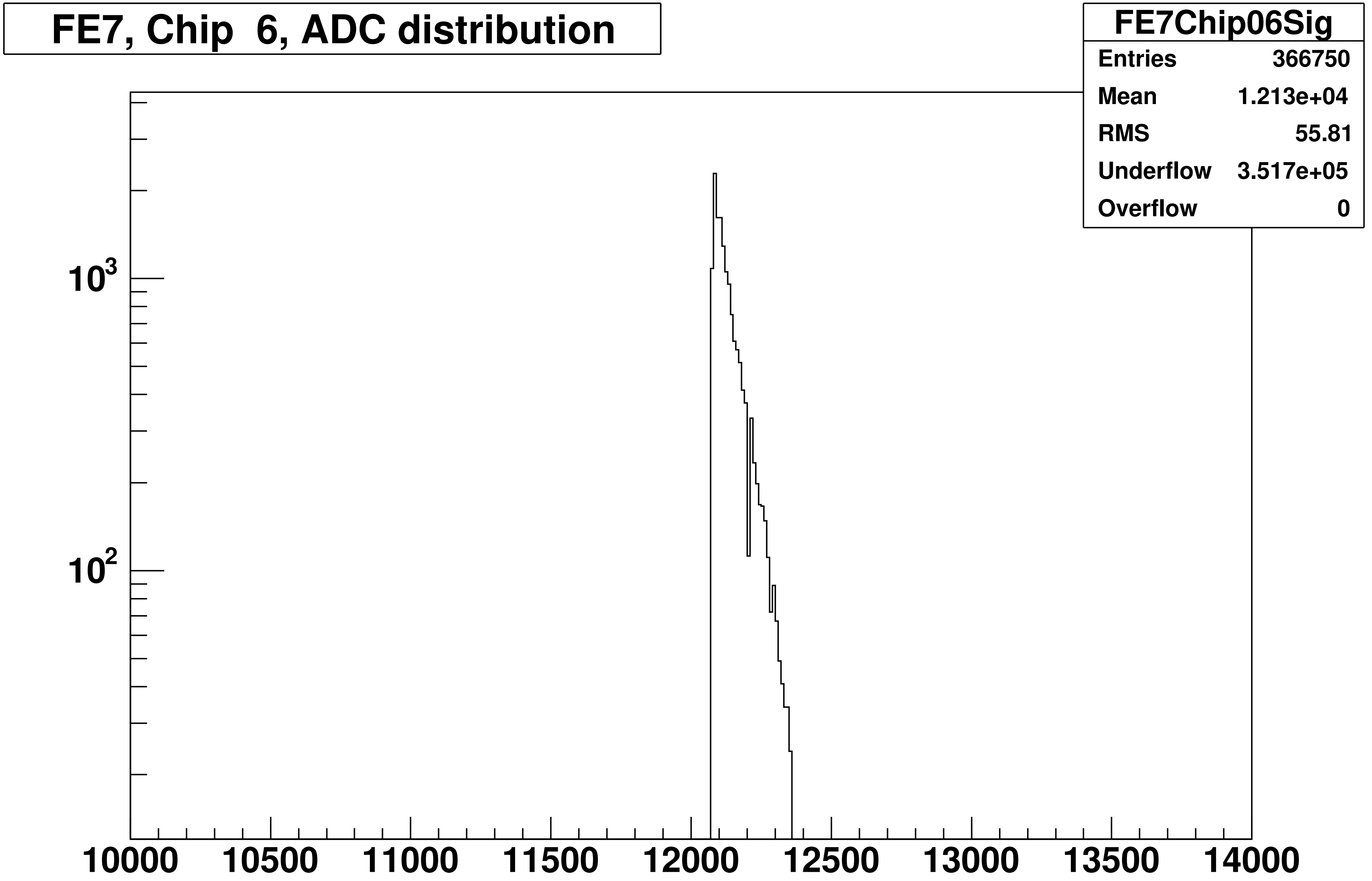
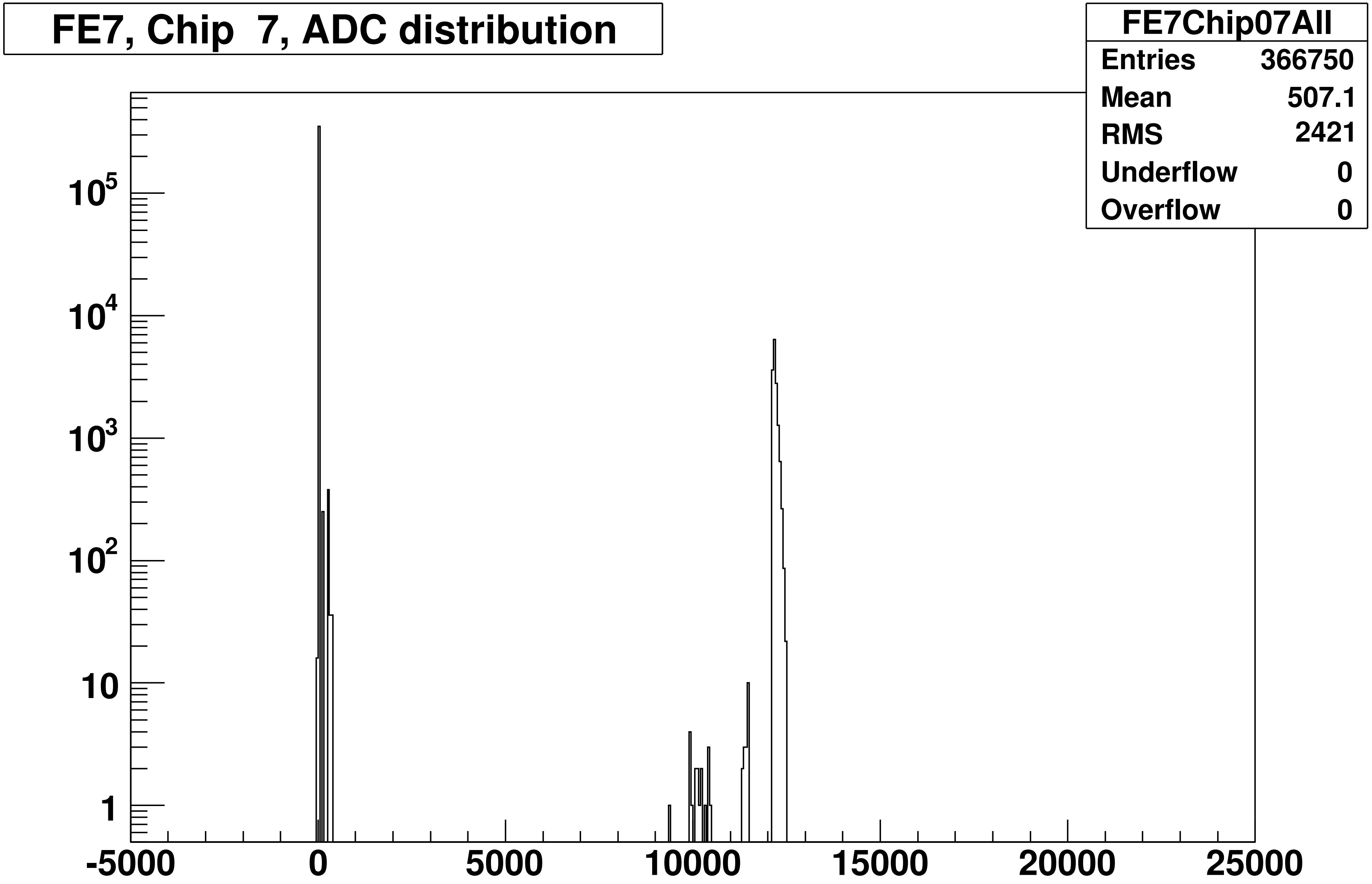
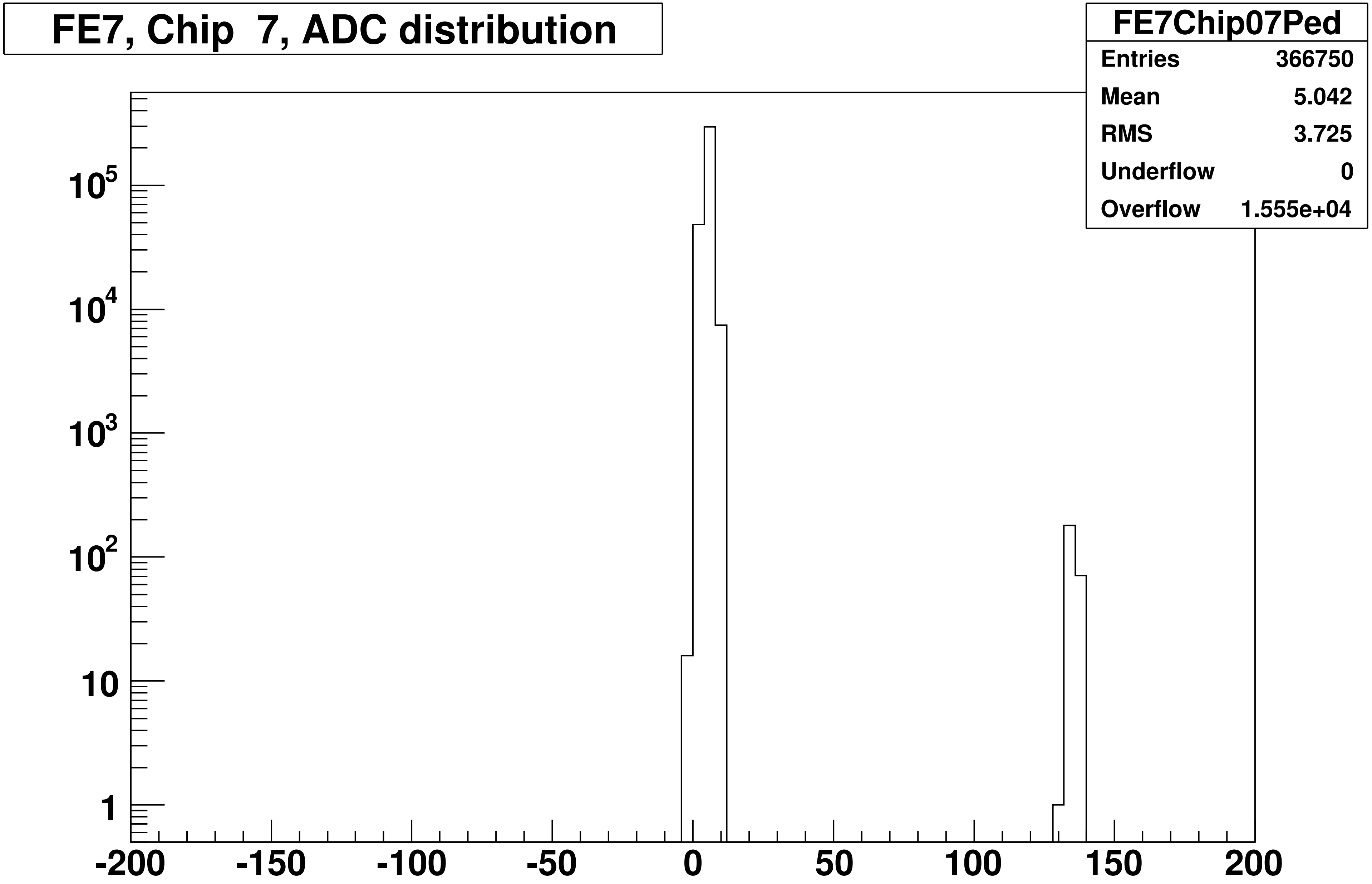
-150
-100
-50
0
50
100
150
200

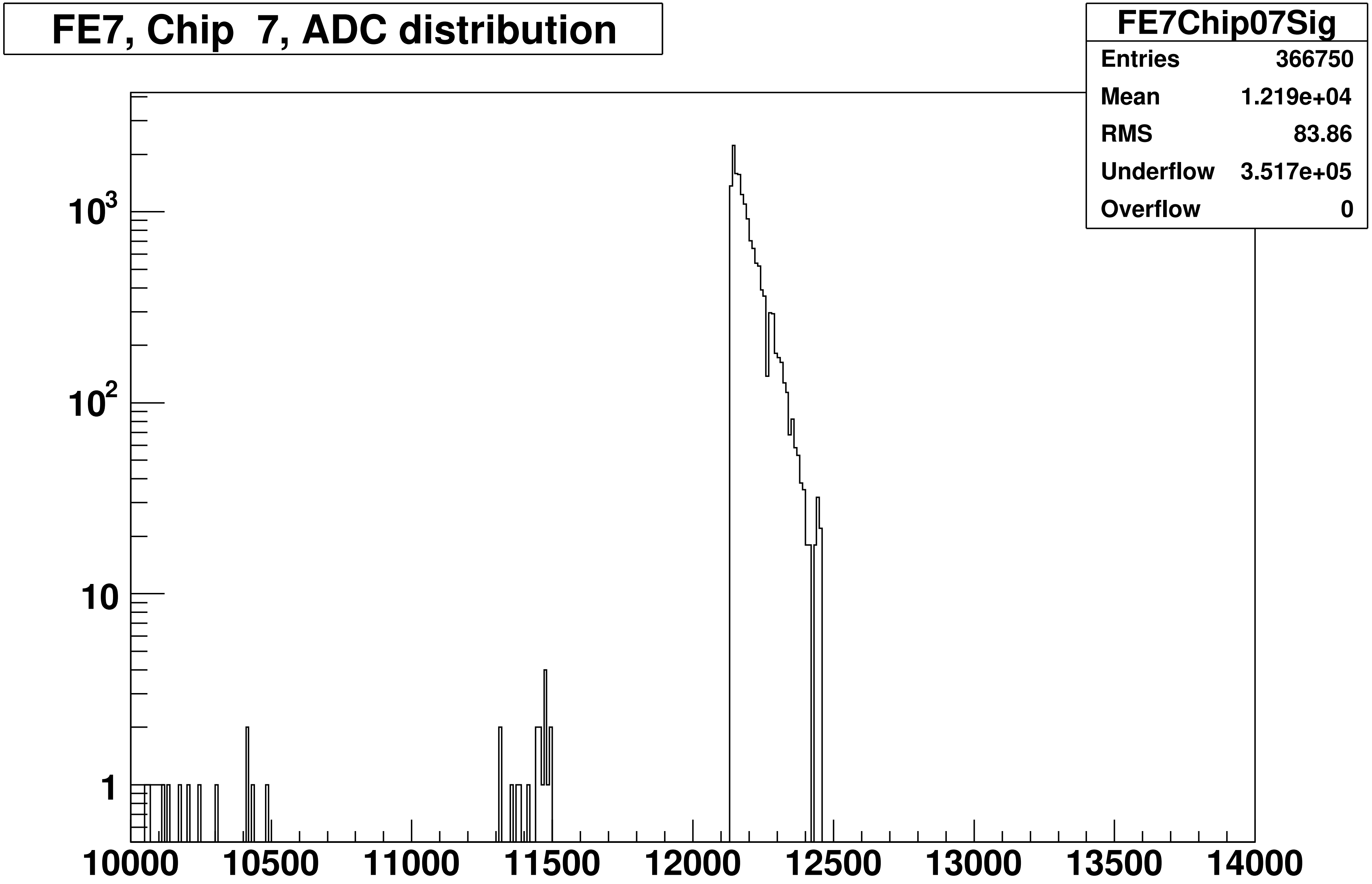

FE7, Chip 6, ADC distribution
FE7Chip06Sig
Entries 366750
Mean 1.213e+04
RMS 55.81
Underflow 3.517e+05
Overflow 0
10^3
10^2
10000
10500
11000
11500
12000
12500
13000
13500
14000



FE7, Chip 7, ADC distribution
FE7Chip07All
Entries 366750
Mean 507.1
RMS 2421
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE7, Chip 7, ADC distribution
FE7Chip07Ped
Entries 366750
Mean 5.042
RMS 3.725
Underflow 0
Overflow 1.555e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
200


FE7, Chip 7, ADC distribution
FE7Chip07Sig
Entries 366750
Mean 1.219e+04
RMS 83.86
Underflow 3.517e+05
Overflow 0
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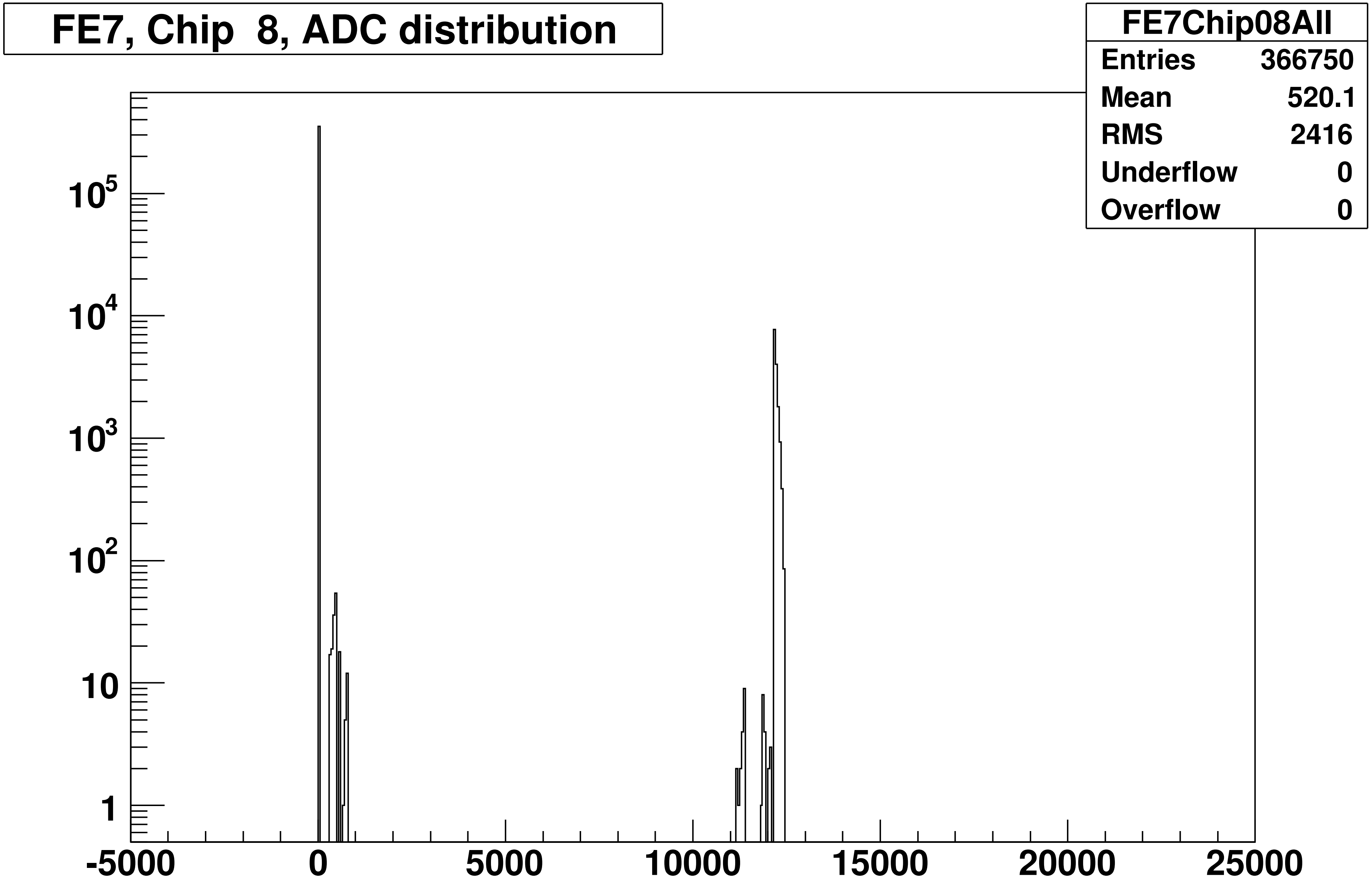
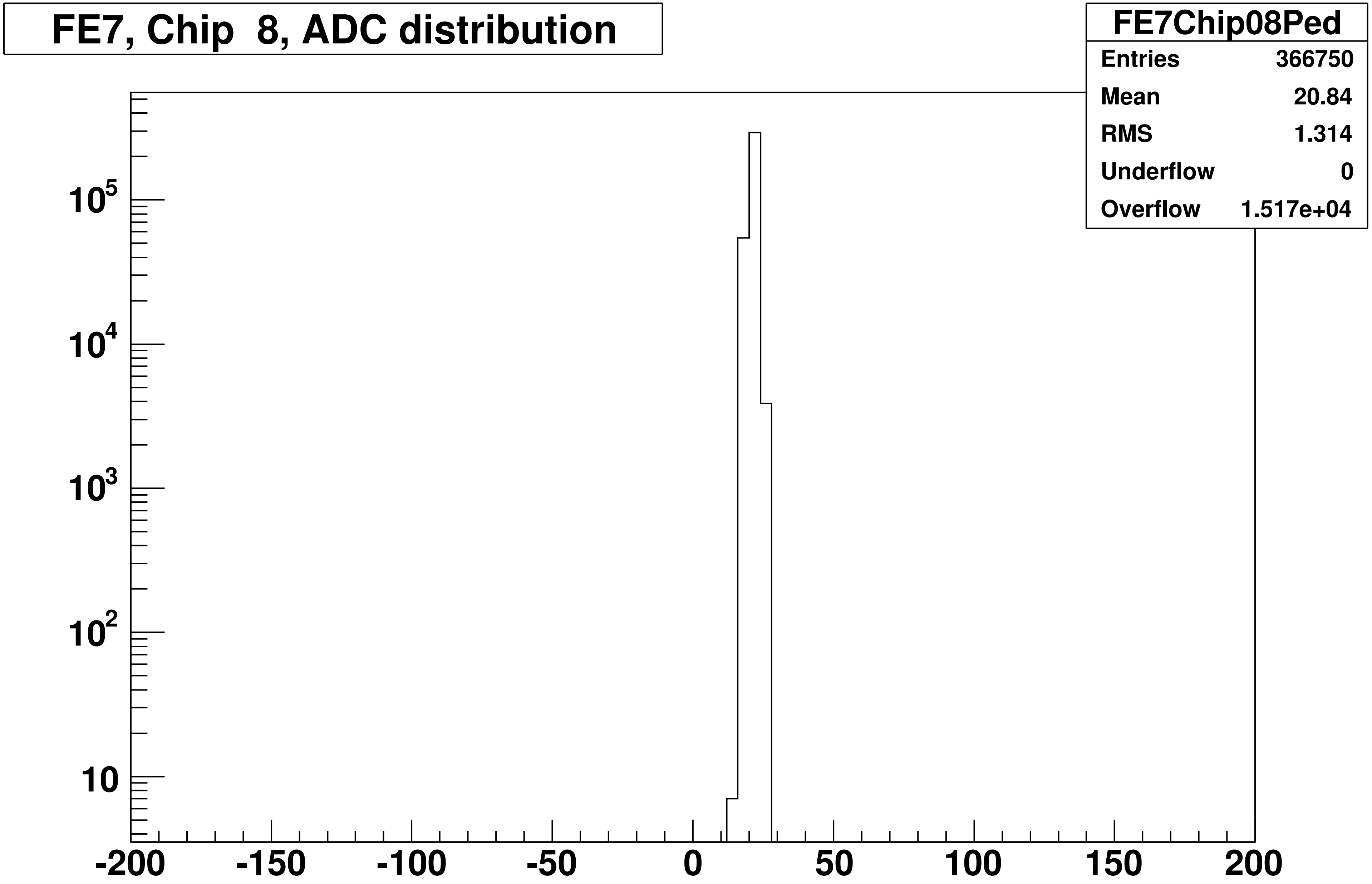
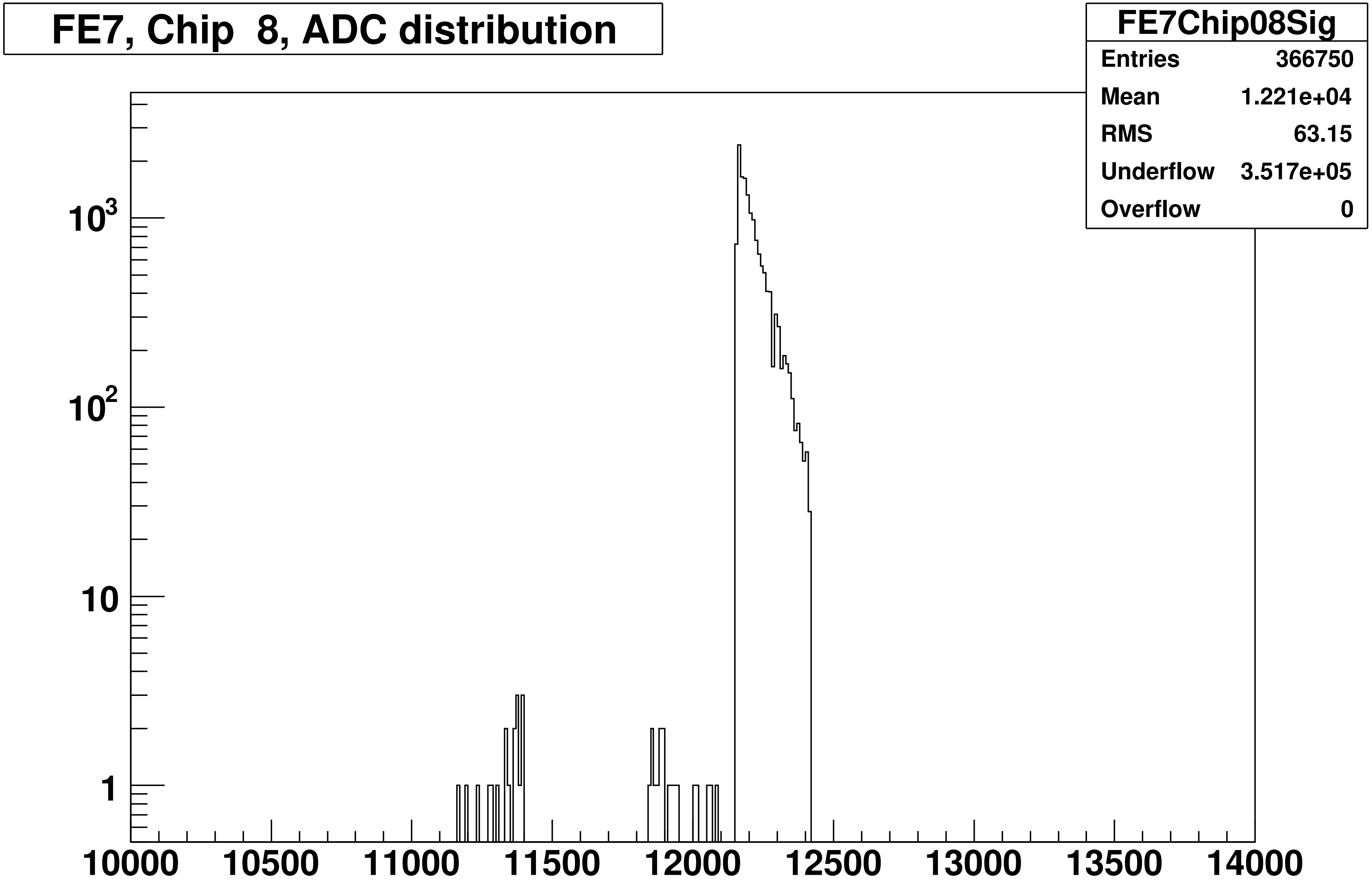
10^2
10
1
10000
10500
11000
11500
12000
12500
13000
13500
14000

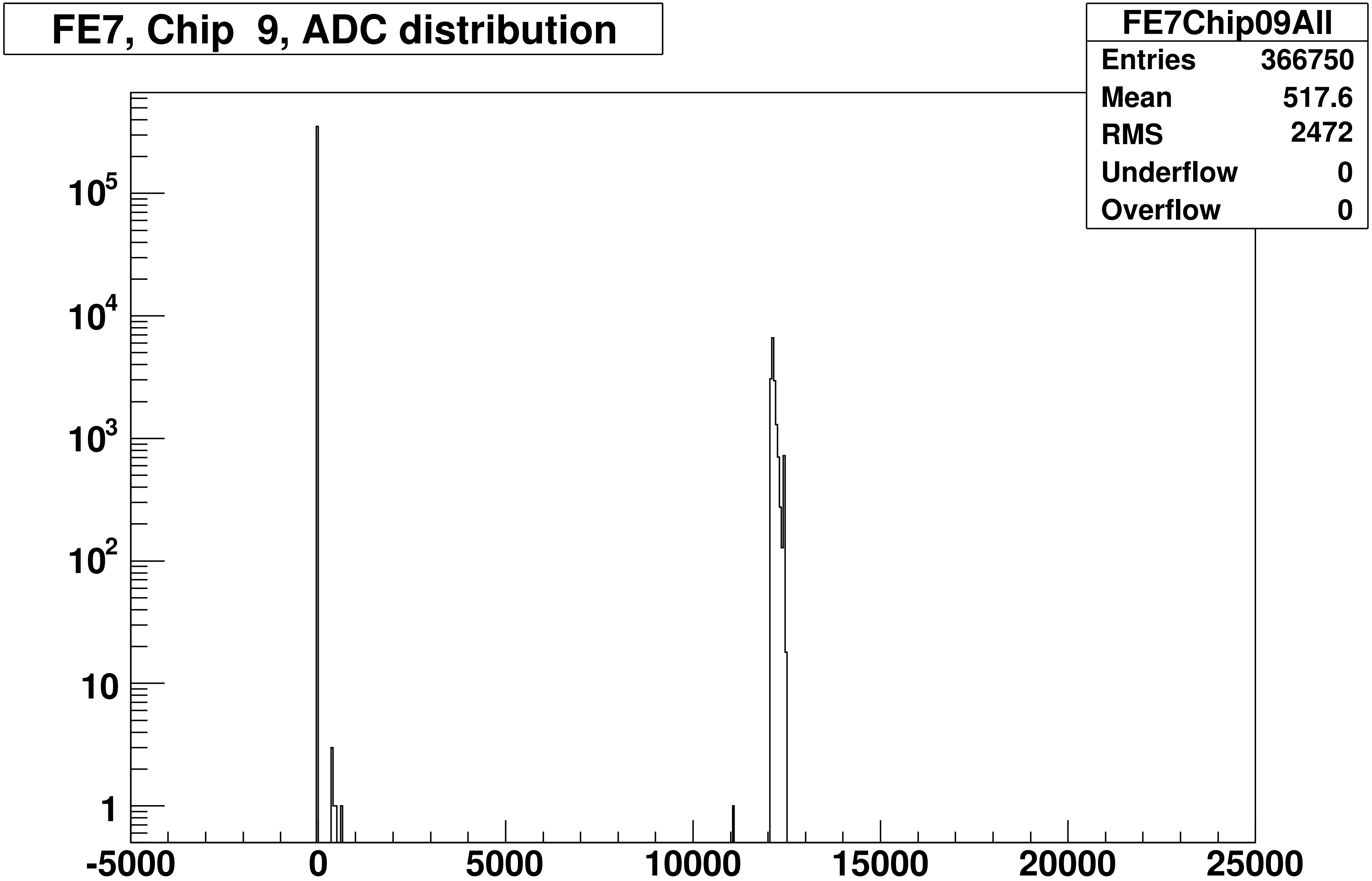


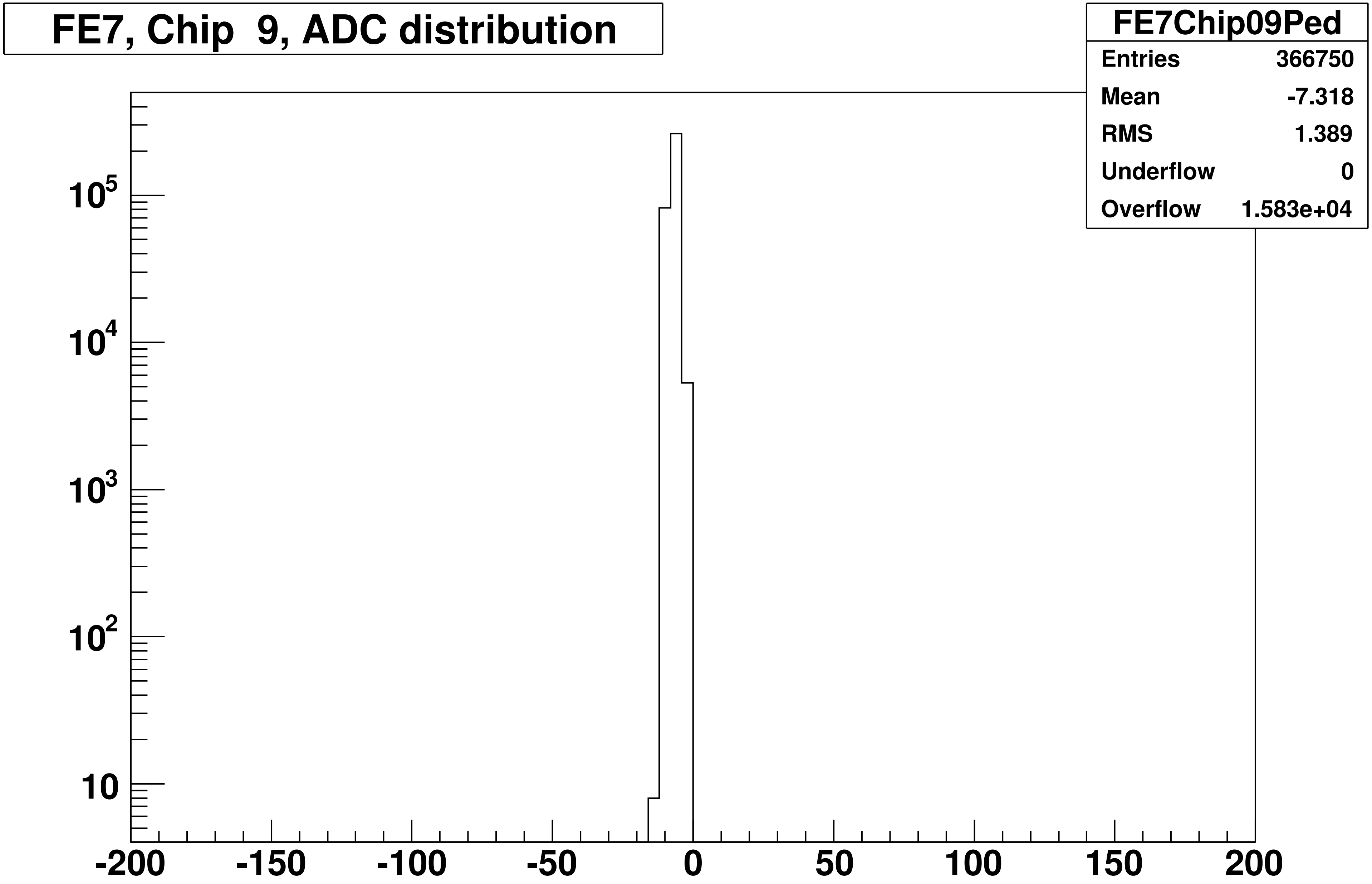
FE7, Chip 8, ADC distribution
FE7Chip08All
Entries 366750
Mean 520.1
RMS 2416
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000

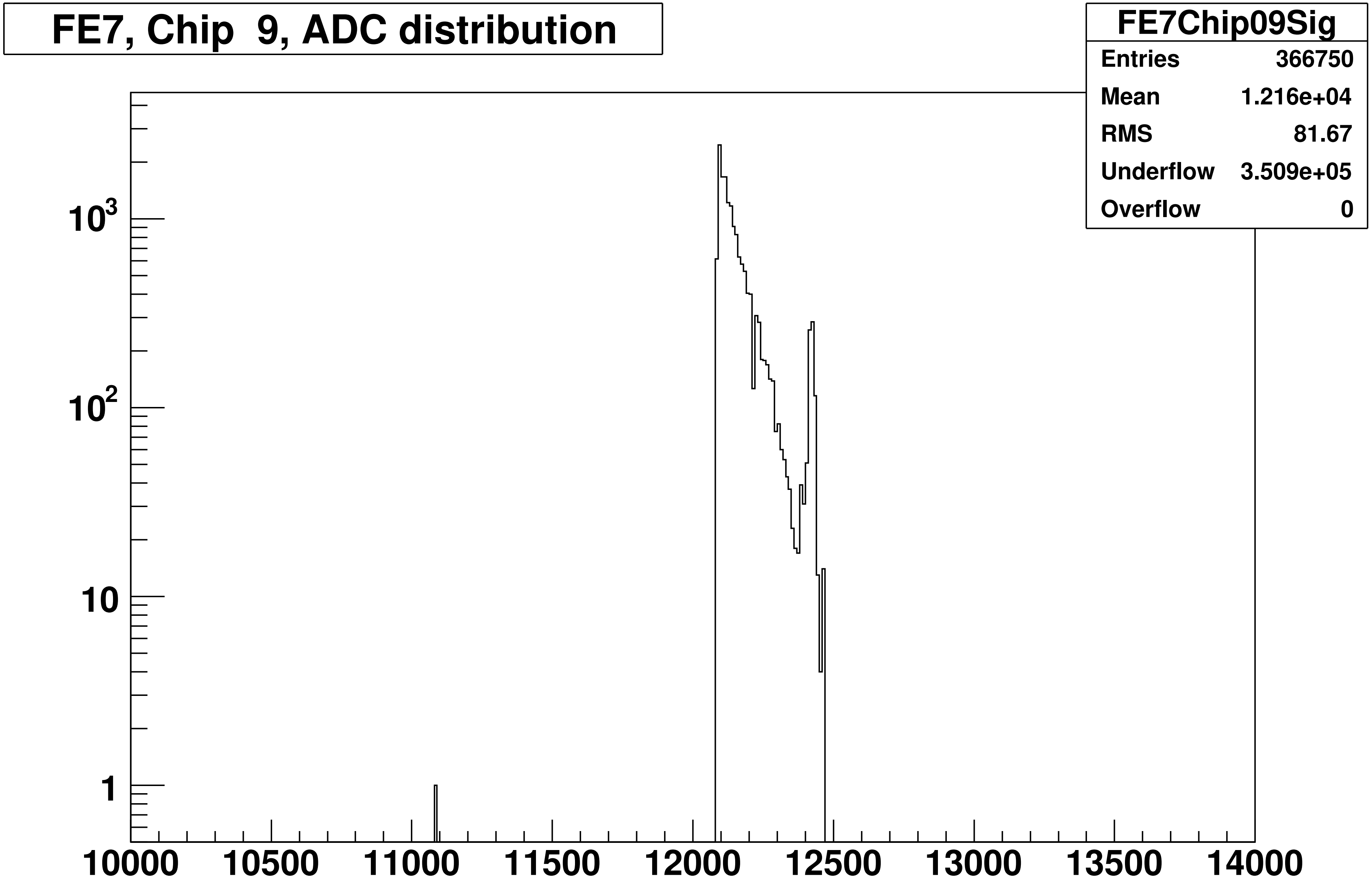

FE7, Chip 8, ADC distribution
FE7Chip08Ped
Entries 366750
Mean 20.84
RMS 1.314
Underflow 0
Overflow 1.517e+04
10
10^2
10^3
10^4
10^5
-200
-150
-100
-50
0
50
100
150
200



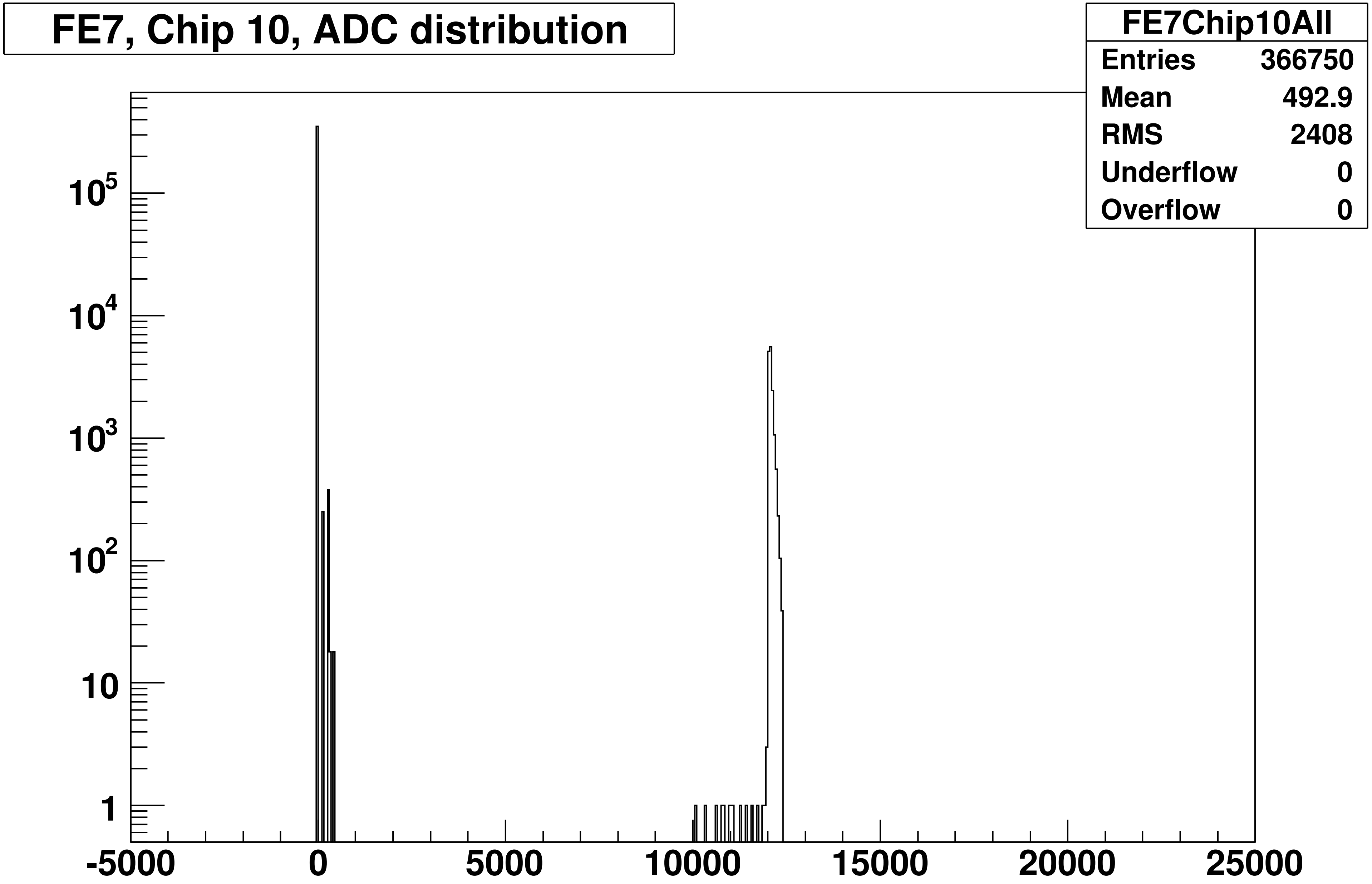
FE7, Chip 8, ADC distribution
FE7Chip08Sig
Entries 366750
Mean 1.221e+04
RMS 63.15
Underflow 3.517e+05
Overflow 0
10^3
10^2
10
1
10000
10500
11000
11500
12000
12500
13000
13500
14000

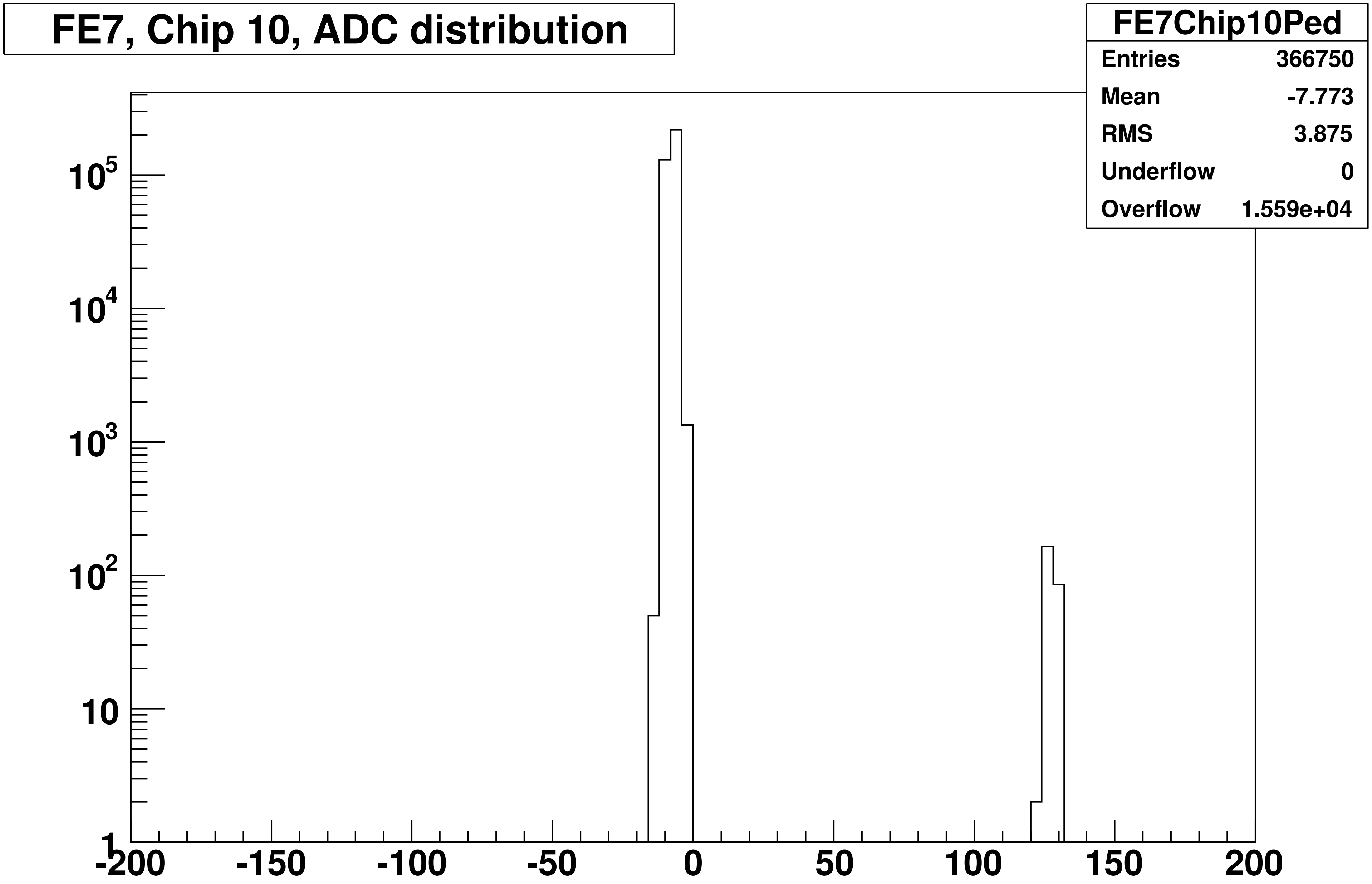

FE7, Chip 9, ADC distribution
FE7Chip09All
Entries 366750
Mean 517.6
RMS 2472
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000

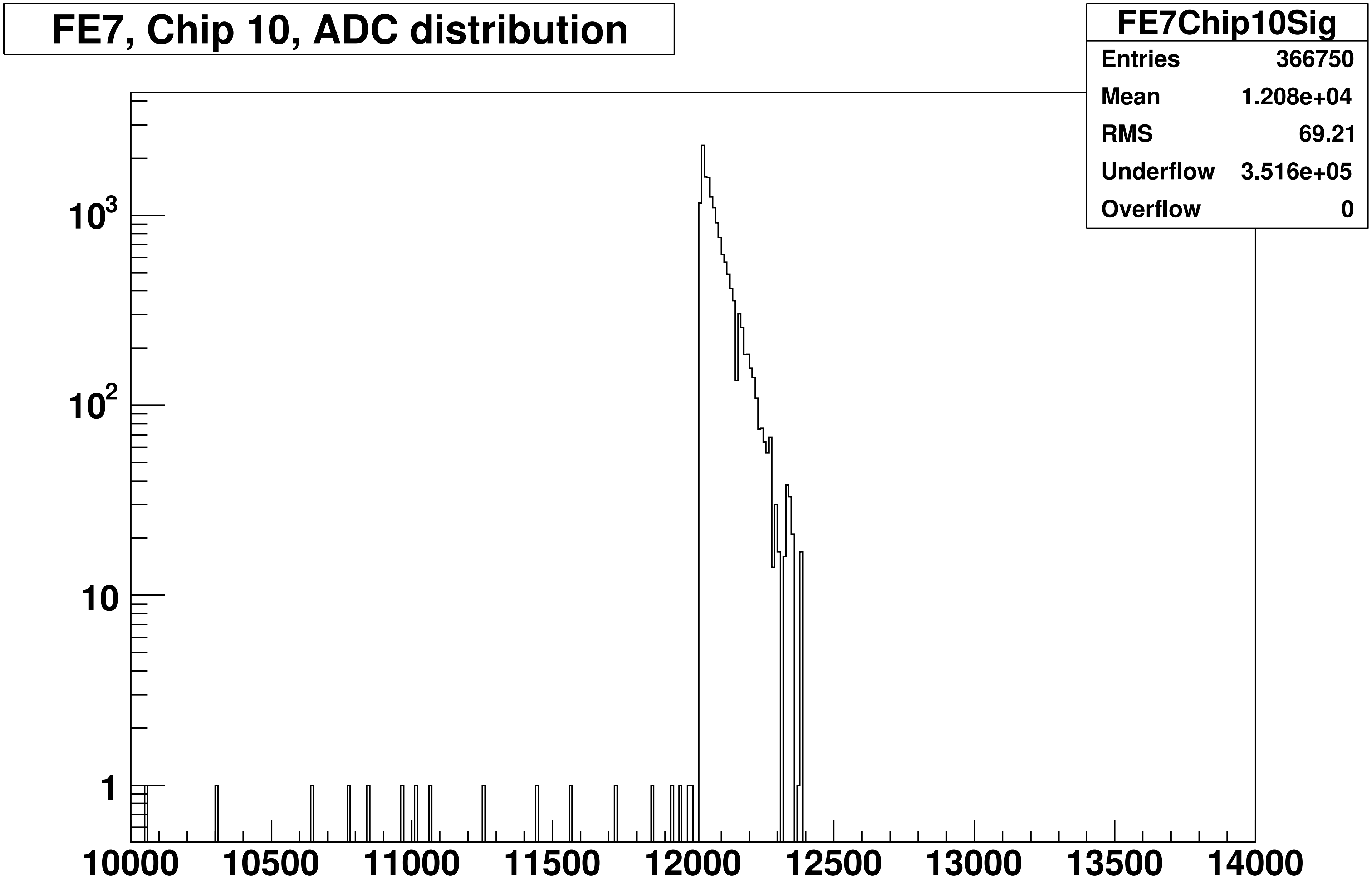

FE7, Chip 9, ADC distribution
FE7Chip09Ped
Entries 366750
Mean -7.318
RMS 1.389
Underflow 0
Overflow 1.583e+04
10^5
10^4
10^3
10^2
10
-200
-150
-100
-50
0
50
100
150
200

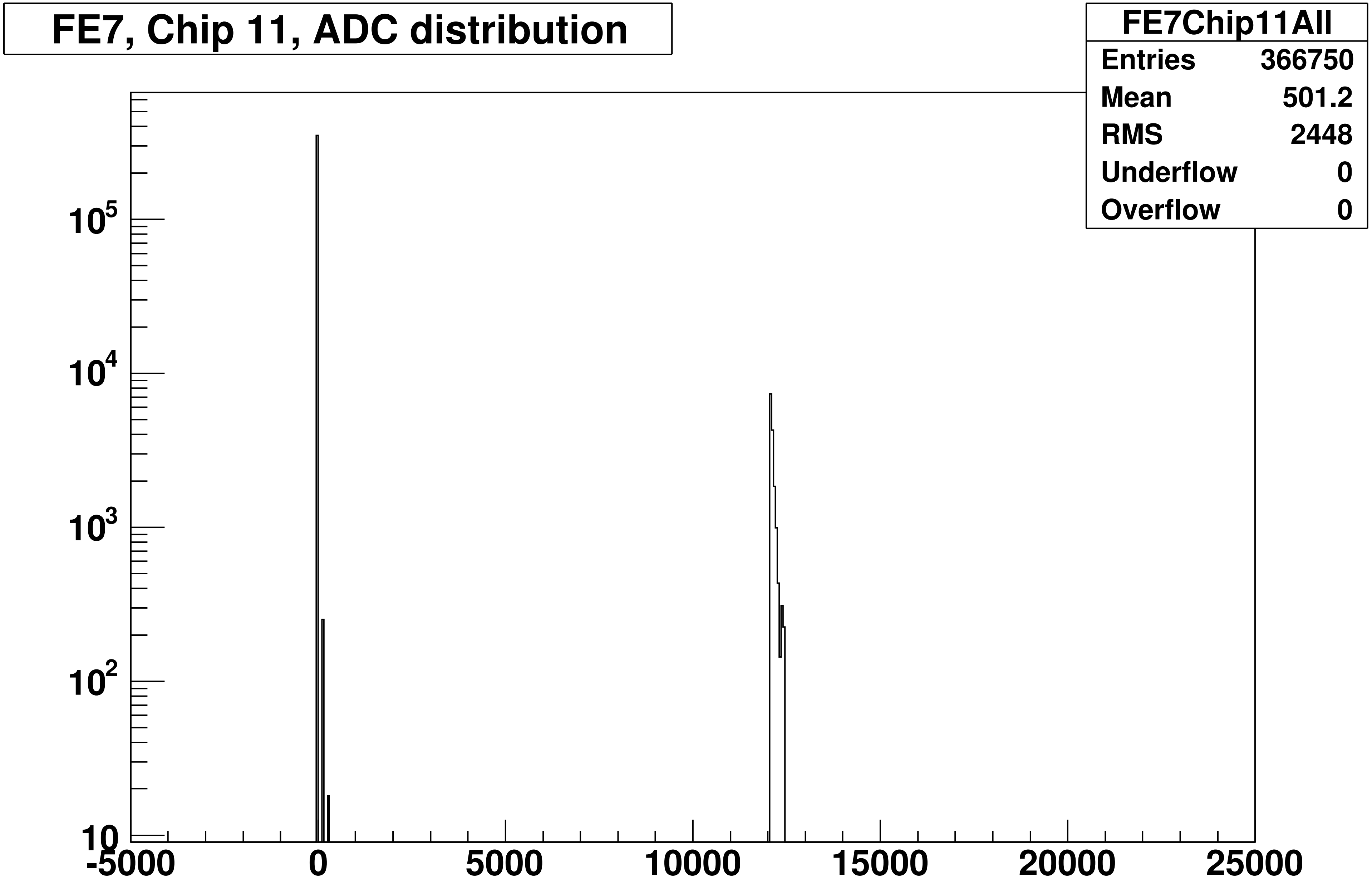


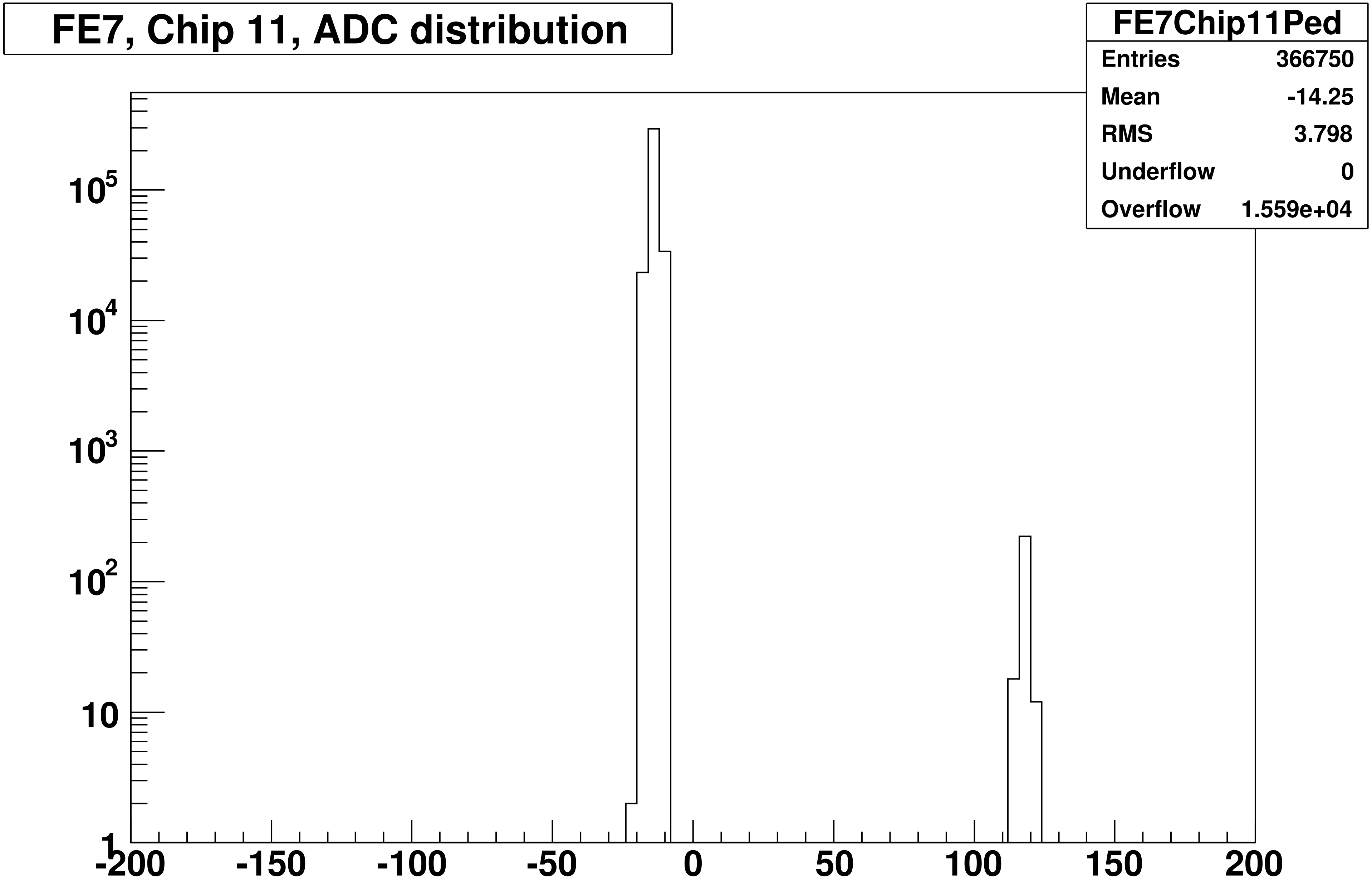
FE7, Chip 9, ADC distribution
FE7Chip09Sig
Entries 366750
Mean 1.216e+04
RMS 81.67
Underflow 3.509e+05
Overflow 0
10^3
10^2
10
1
10000
10500
11000
11500
12000
12500
13000
13500
14000

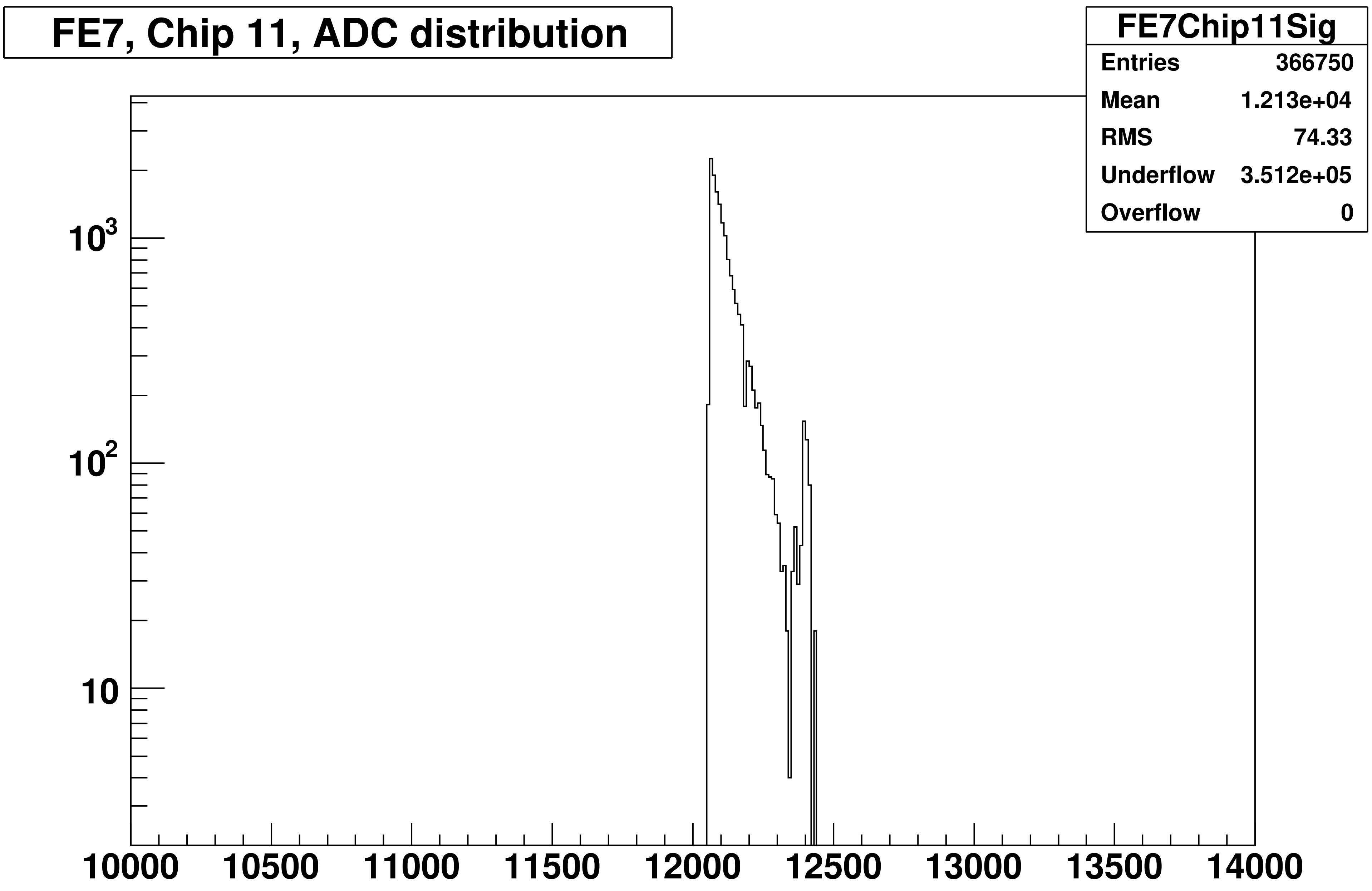

FE7, Chip 10, ADC distribution
FE7Chip10All
Entries 366750
Mean 492.9
RMS 2408
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE7, Chip 10, ADC distribution
FE7Chip10Ped
Entries 366750
Mean -7.773
RMS 3.875
Underflow 0
Overflow 1.559e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
200

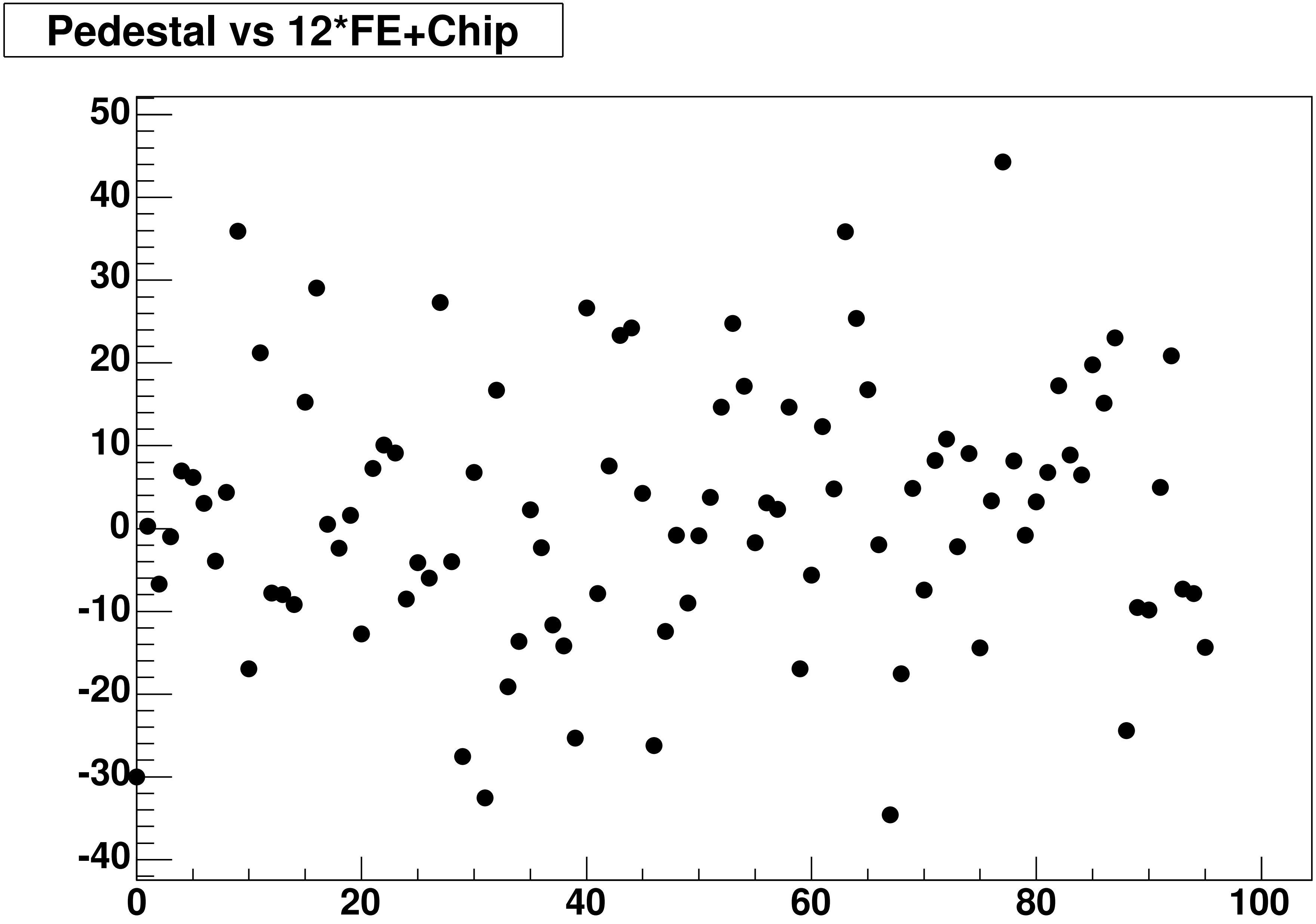

FE7, Chip 10, ADC distribution
FE7Chip10Sig
Entries 366750
Mean 1.208e+04
RMS 69.21
Underflow 3.516e+05
Overflow 0
10^3
10^2
10
1
10000
10500
11000
11500
12000
12500
13000
13500
14000

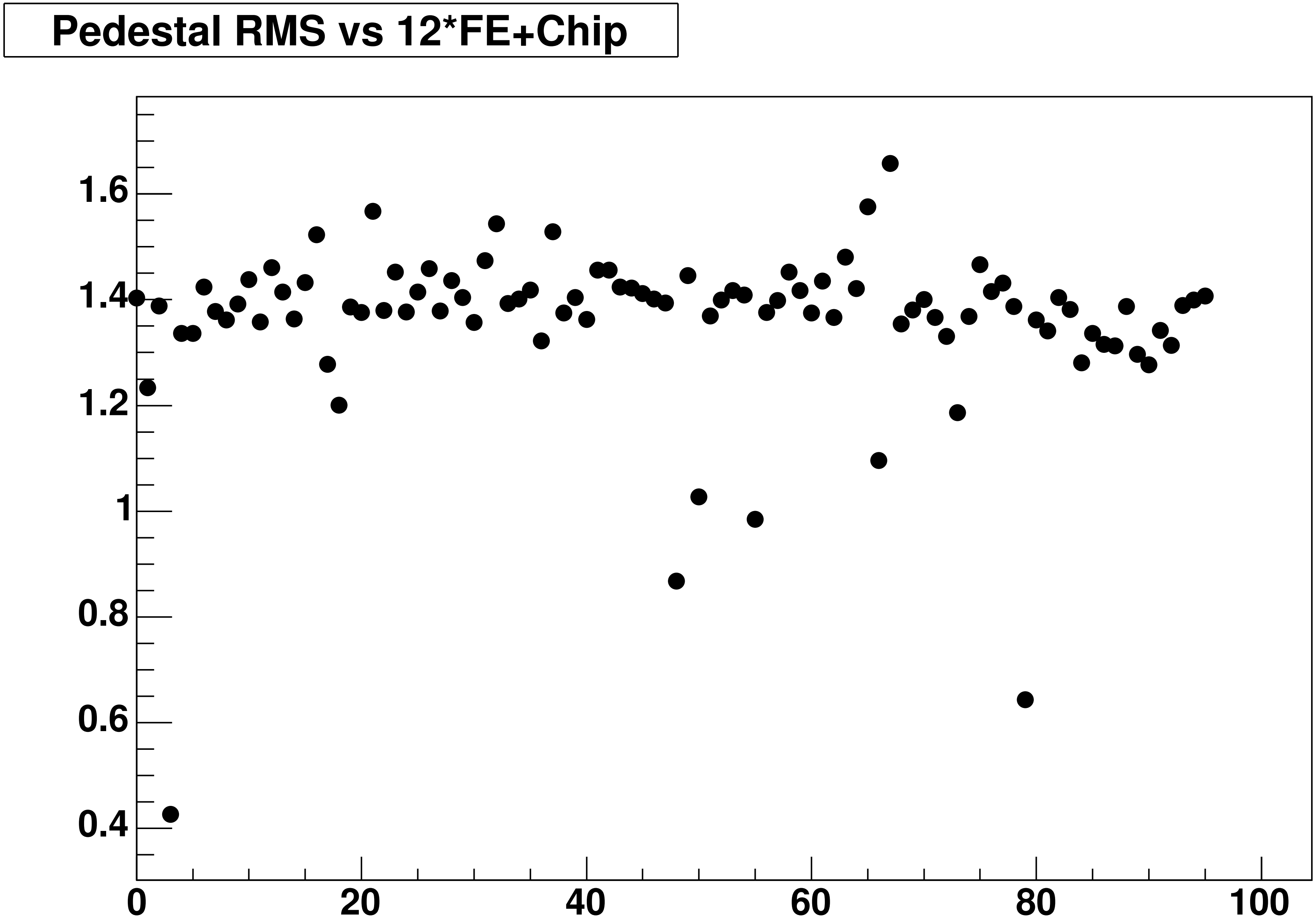

FE7, Chip 11, ADC distribution
FE7Chip11All
Entries 366750
Mean 501.2
RMS 2448
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000

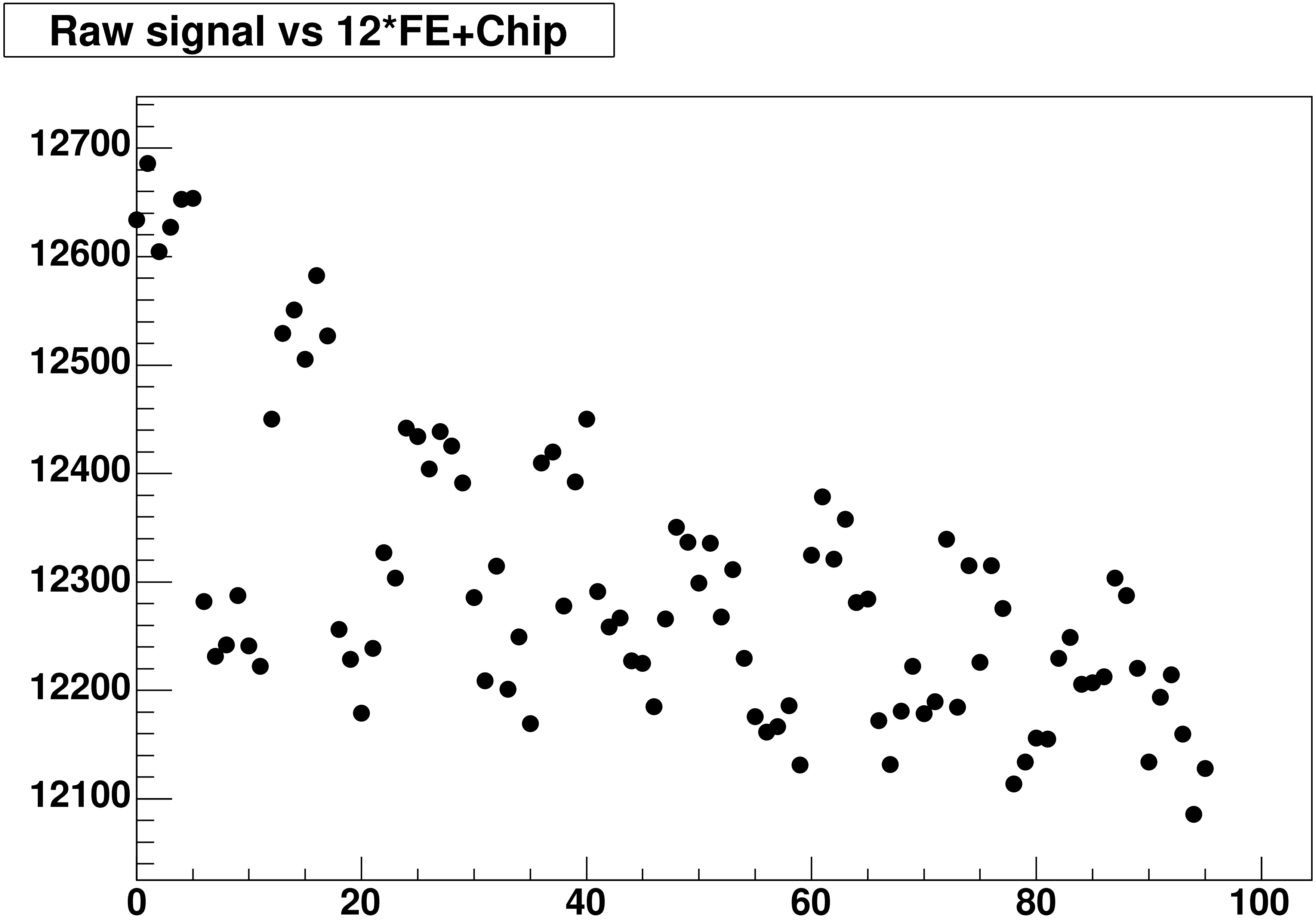

FE7, Chip 11, ADC distribution
FE7Chip11Ped
Entries 366750
Mean -14.25
RMS 3.798
Underflow 0
Overflow 1.559e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
200

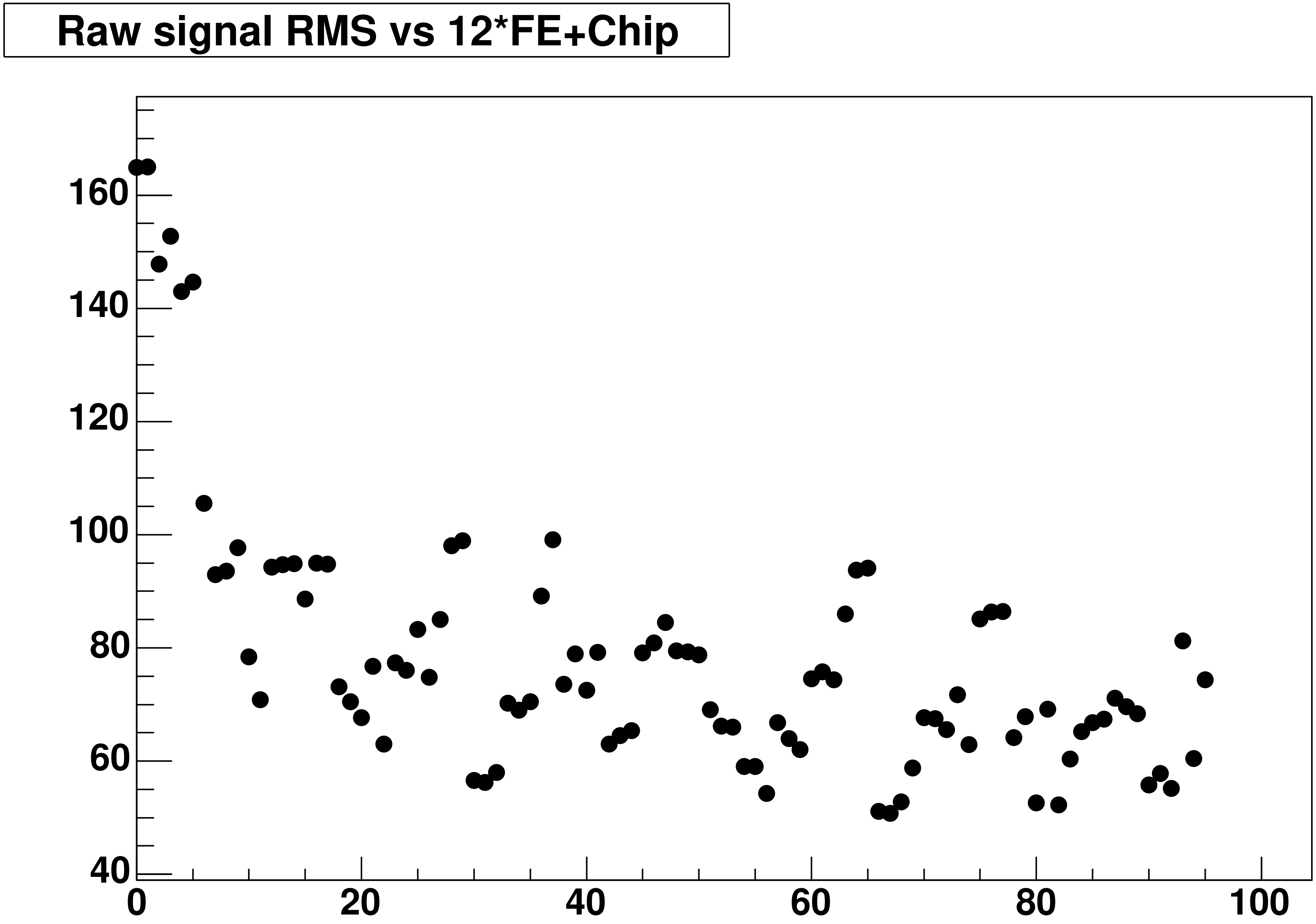


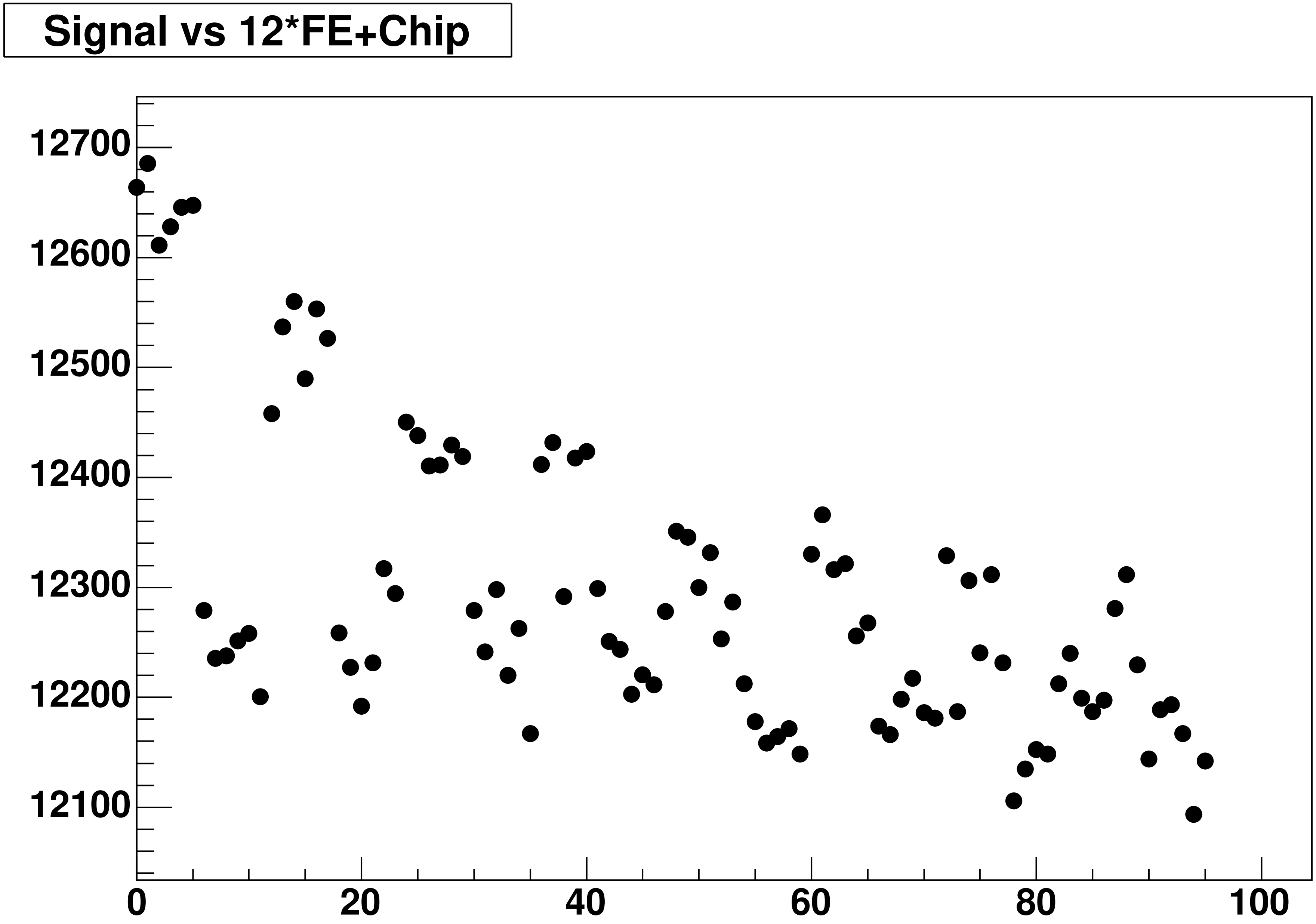
FE7, Chip 11, ADC distribution
FE7Chip11Sig
Entries 366750
Mean 1.213e+04
RMS 74.33
Underflow 3.512e+05
Overflow 0
10^3
10^2
10
10000
10500
11000
11500
12000
12500
13000
13500
14000

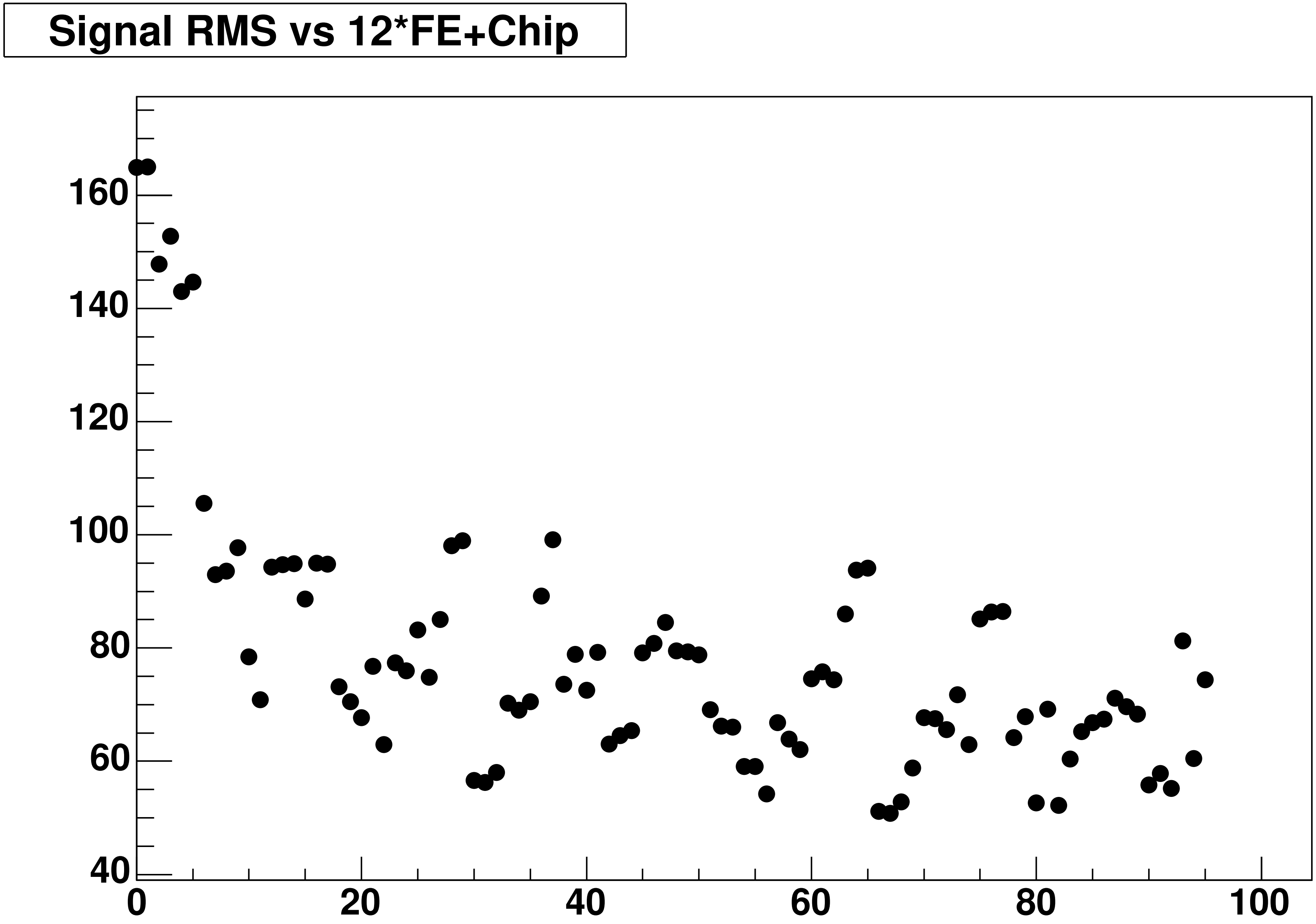

Pedestal vs 12*FE+Chip
50
40
30
20
10
0
-10
-20
-30
-40
0
20
40
60
80
100


Pedestal RMS vs 12*FE+Chip
1.6
1.4
1.2
1
0.8
0.6
0.4
0
20
40
60
80
100


Raw signal vs 12*FE+Chip
12700
12600
12500
12400
12300
12200
12100
0
20
40
60
80
100


Raw signal RMS vs 12*FE+Chip
160
140
120
100
80
60
40
0
20
40
60
80
100


Signal vs 12*FE+Chip
12700
12600
12500
12400
12300
12200
12100
0
20
40
60
80
100


Signal RMS vs 12*FE+Chip
160
140
120
100
80
60
40
0
20
40
60
80
100