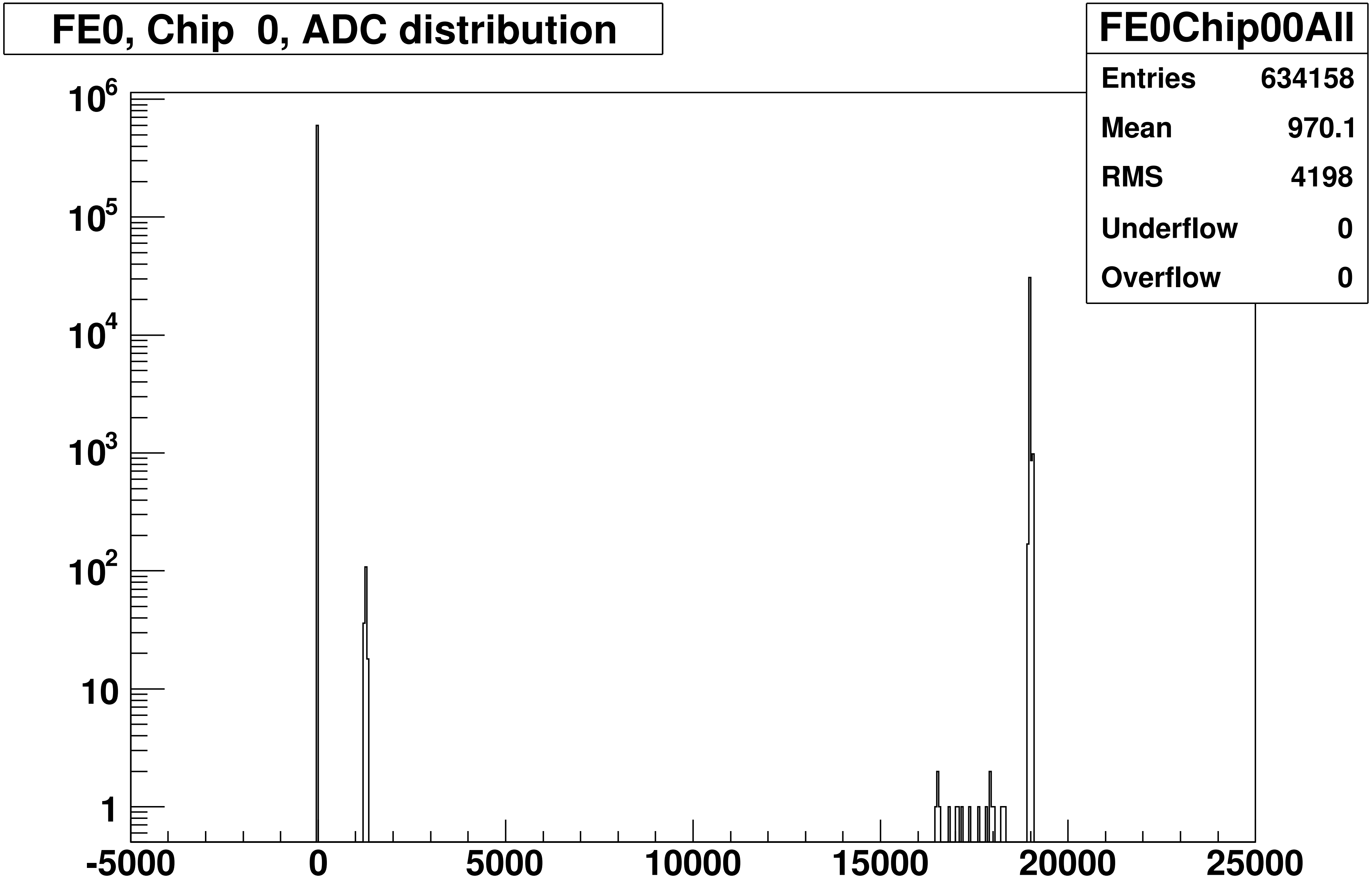
FE0, Chip 0, ADC distribution
FE0Chip00All
Entries 634158
Mean 970.1
RMS 4198
Underflow 0
Overflow 0
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10^4
10^3
10^2
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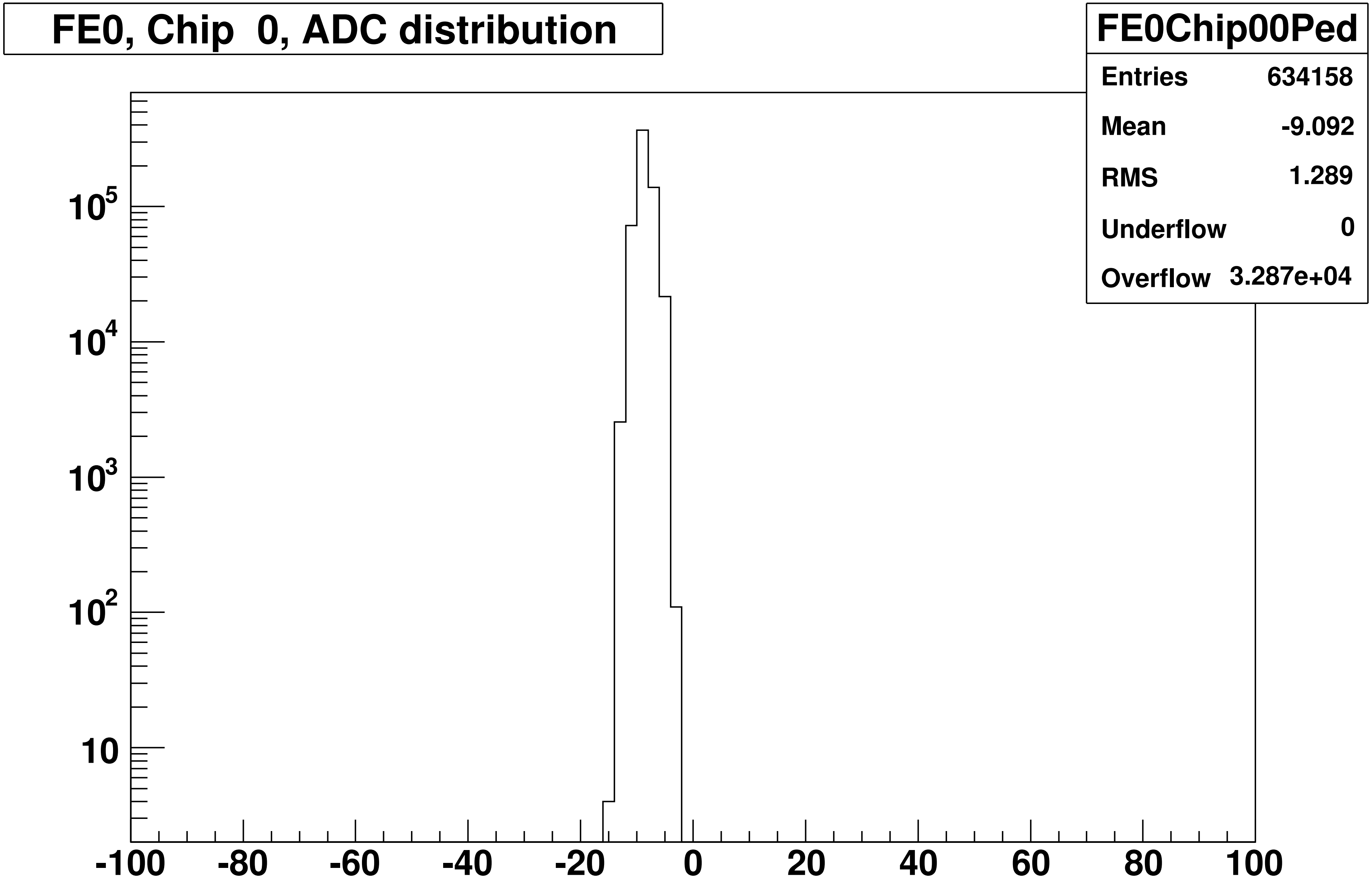
10000
15000
20000
25000


FE0, Chip 0, ADC distribution
FE0Chip00Ped
Entries 634158
Mean -9.092
RMS 1.289
Underflow 0
Overflow 3.287e+04
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10^3
10^4
10^5
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80
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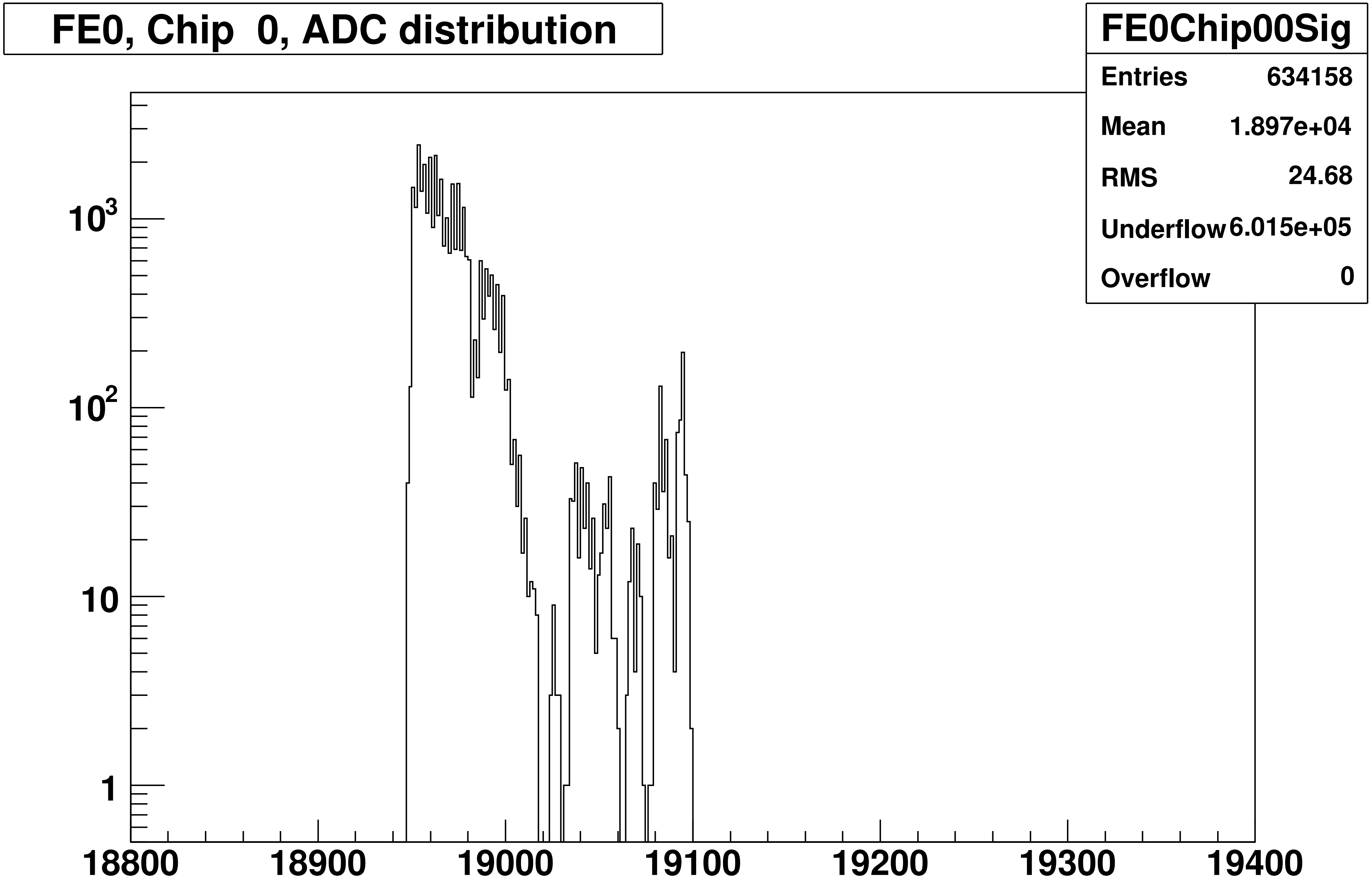
FE0, Chip 0, ADC distribution
FE0Chip00Sig
Entries 634158
Mean 1.897e+04
RMS 24.68
Underflow 6.015e+05
Overflow 0
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10^2
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18900
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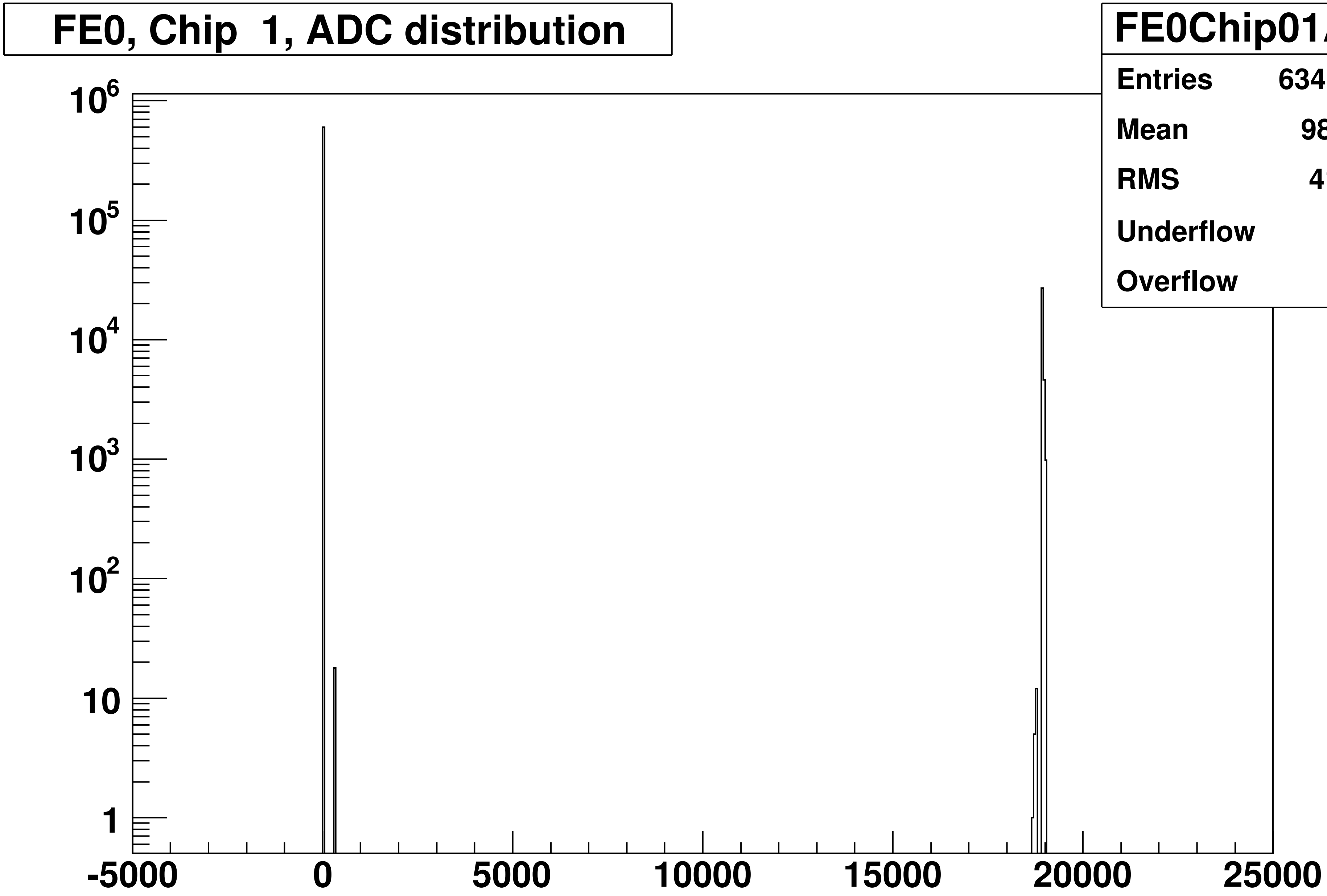
FE0, Chip 1, ADC distribution
FE0Chip01All
Entries 634158
Mean 981.3
RMS 4178
Underflow 0
Overflow 0
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10^4
10^3
10^2
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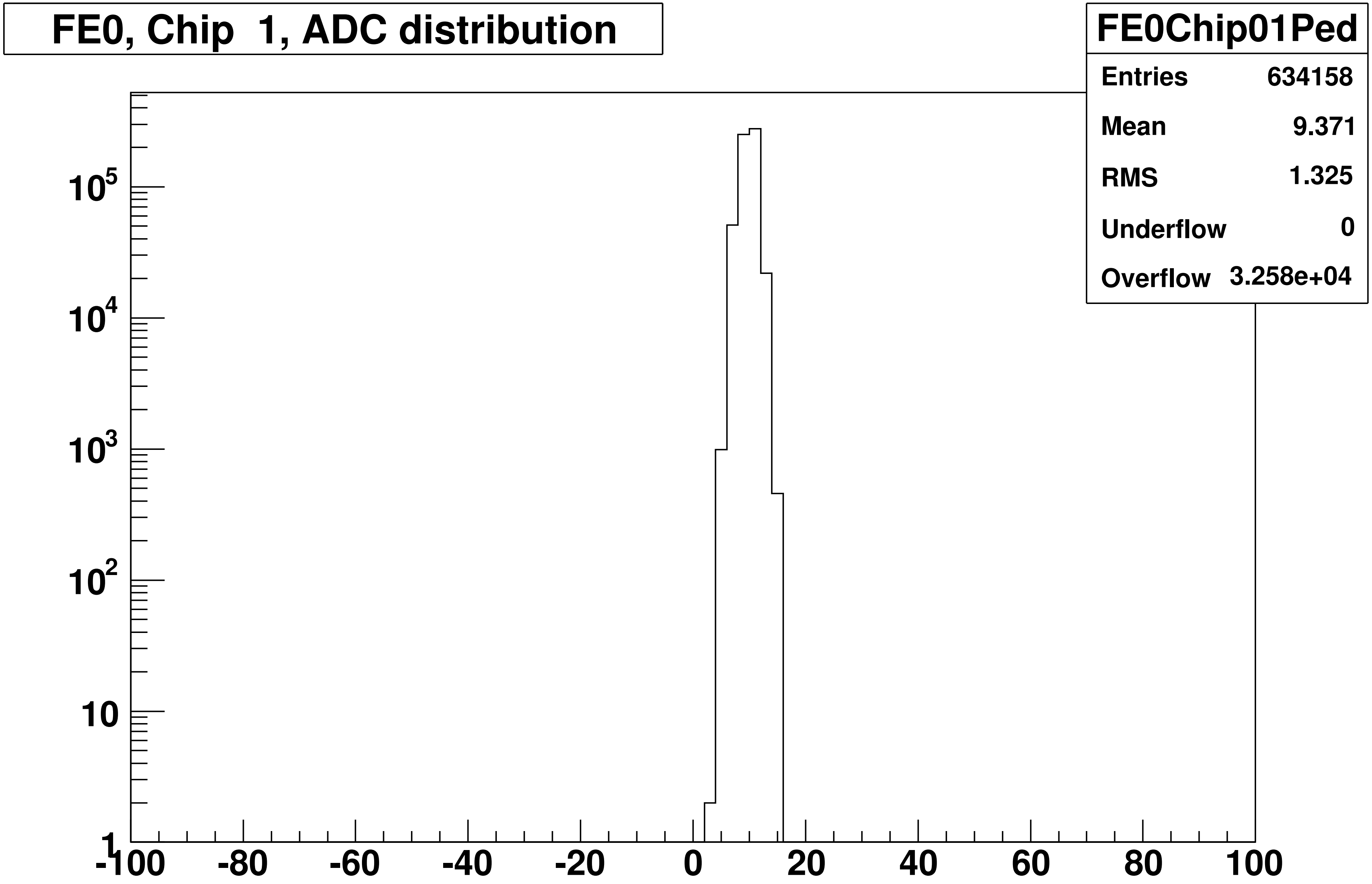
FE0, Chip 1, ADC distribution
FE0Chip01Ped
Entries 634158
Mean 9.371
RMS 1.325
Underflow 0
Overflow 3.258e+04
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10^2
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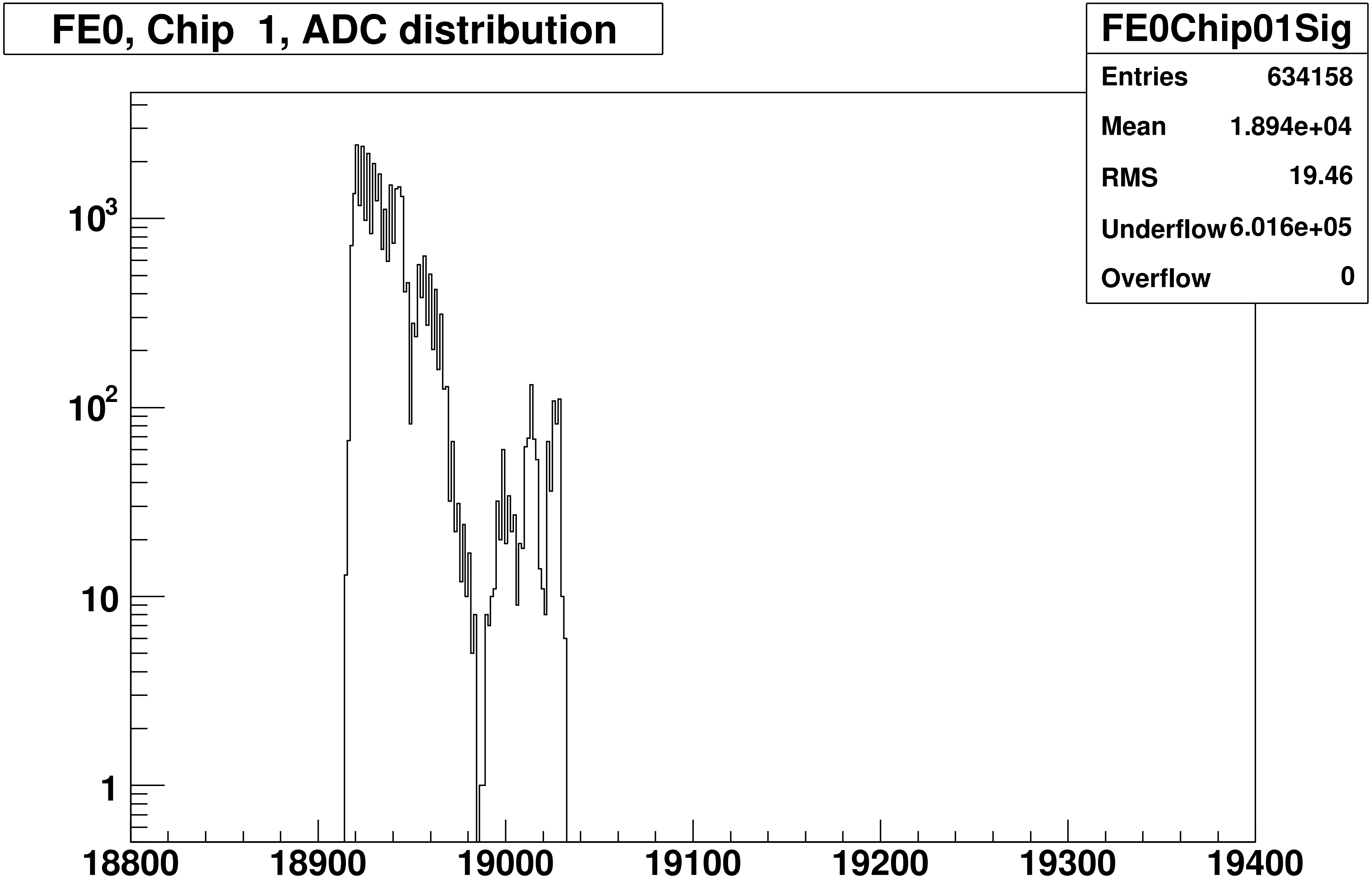

FE0, Chip 1, ADC distribution
FE0Chip01Sig
Entries 634158
Mean 1.894e+04
RMS 19.46
Underflow 6.016e+05
Overflow 0
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10^2
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1
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18900
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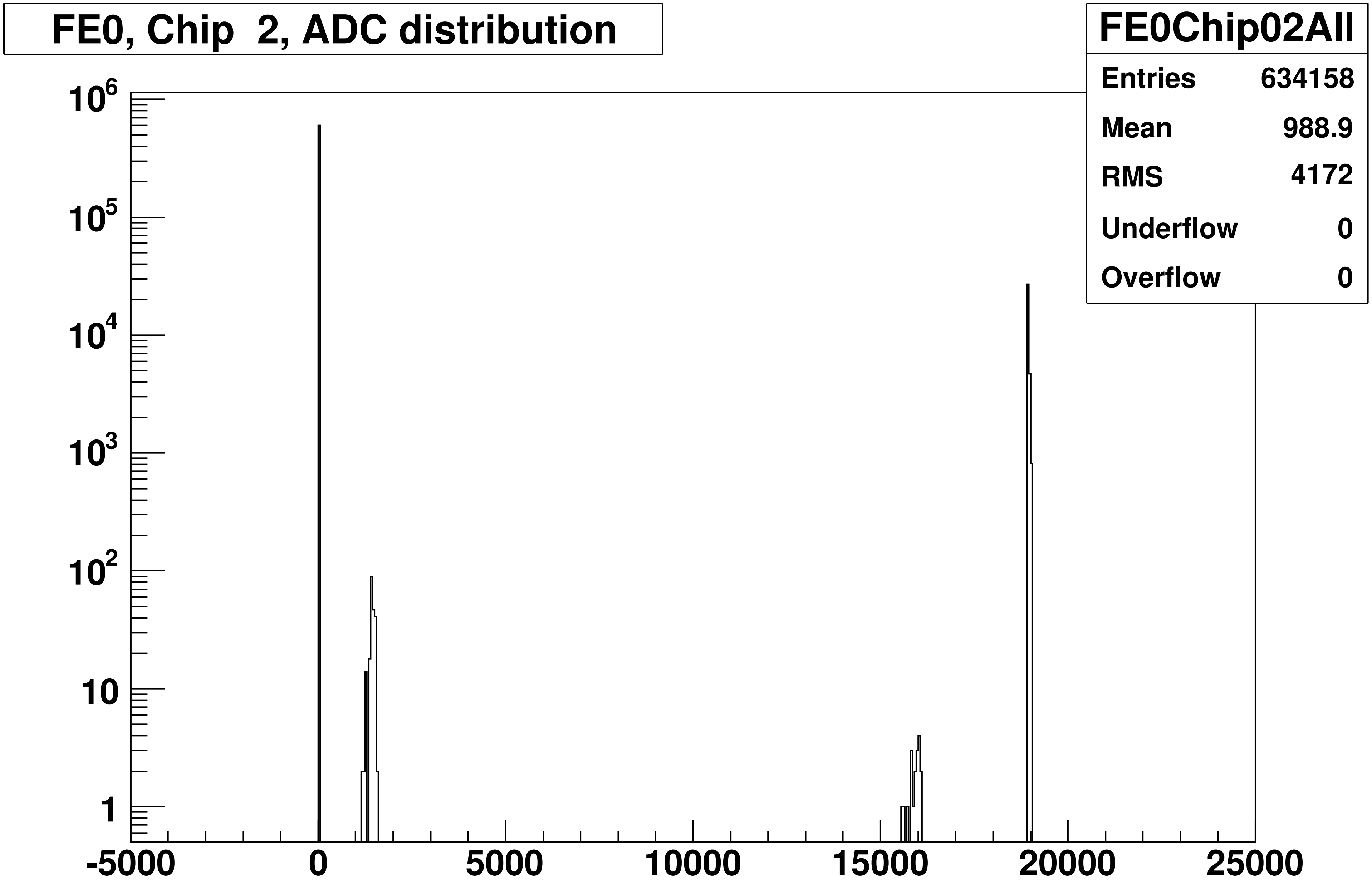
FE0, Chip 2, ADC distribution
FE0Chip02All
Entries 634158
Mean 988.9
RMS 4172
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
1
-5000
0
5000
10000
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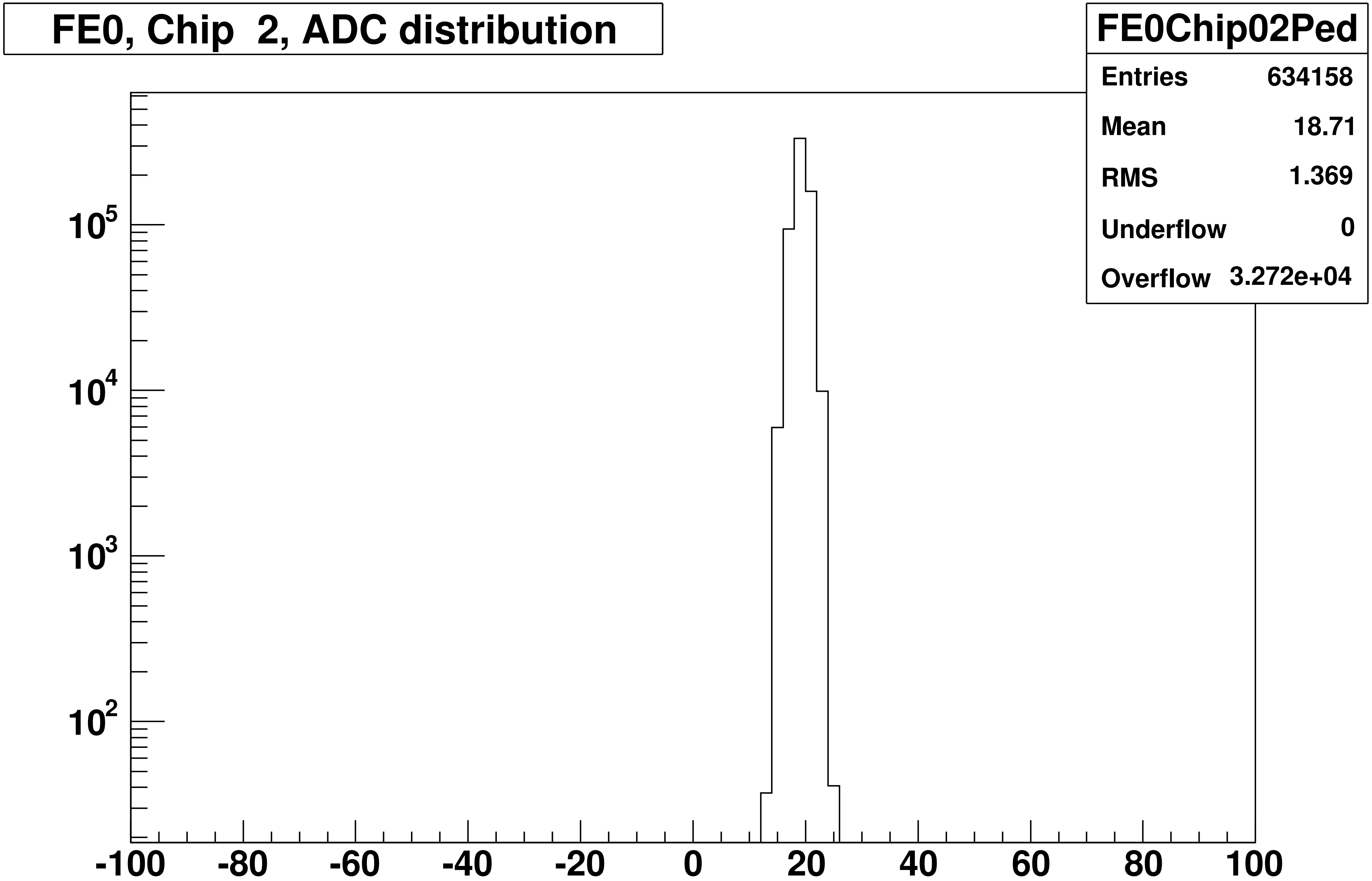
20000
25000



FE0, Chip 2, ADC distribution
FE0Chip02Ped
Entries 634158
Mean 18.71
RMS 1.369
Underflow 0
Overflow 3.272e+04
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10^4
10^3
10^2
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-80
-60
-40
-20
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80
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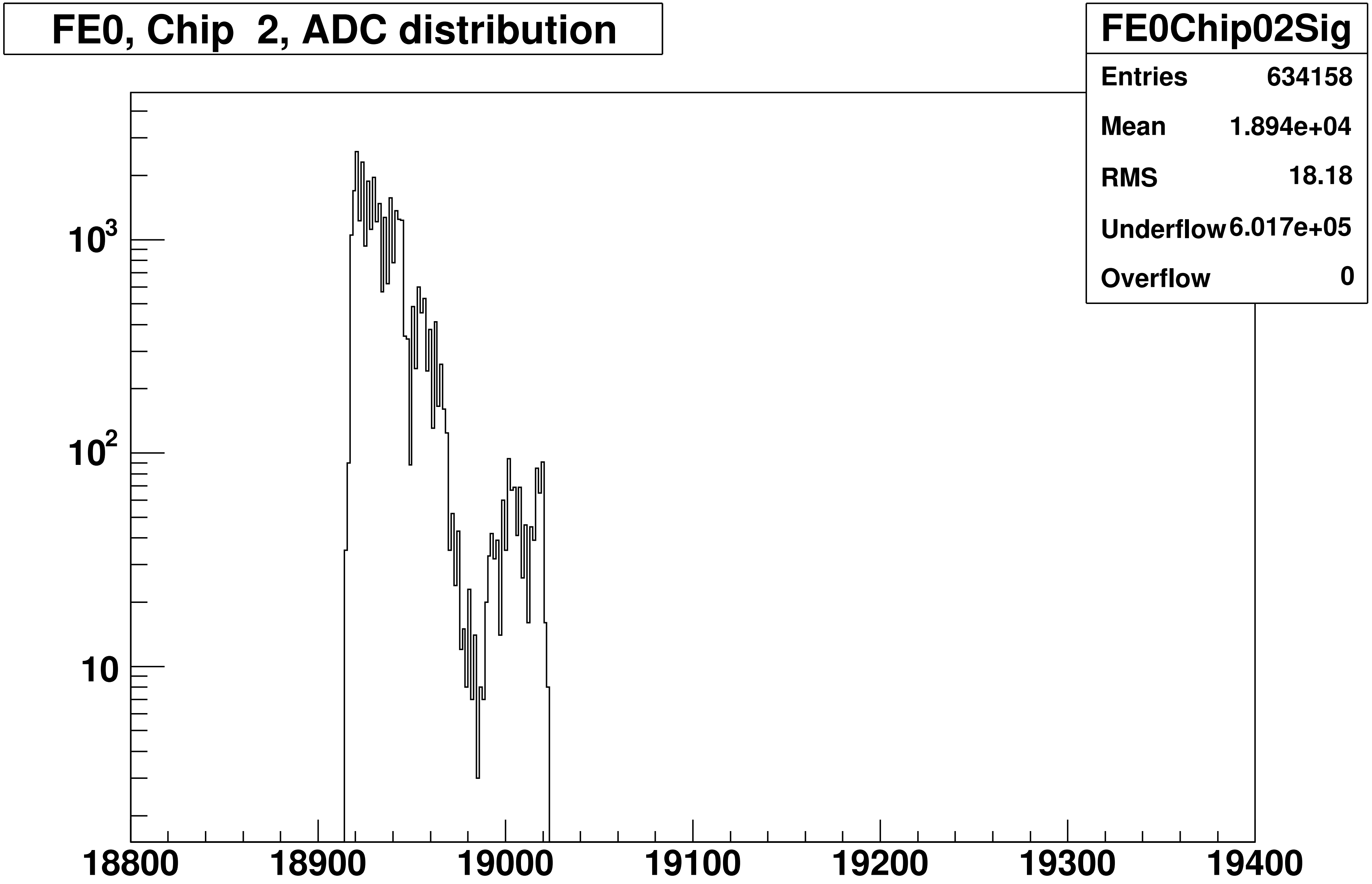
FE0, Chip 2, ADC distribution
FE0Chip02Sig
Entries 634158
Mean 1.894e+04
RMS 18.18
Underflow 6.017e+05
Overflow 0
10
10^2
10^3
18800
18900
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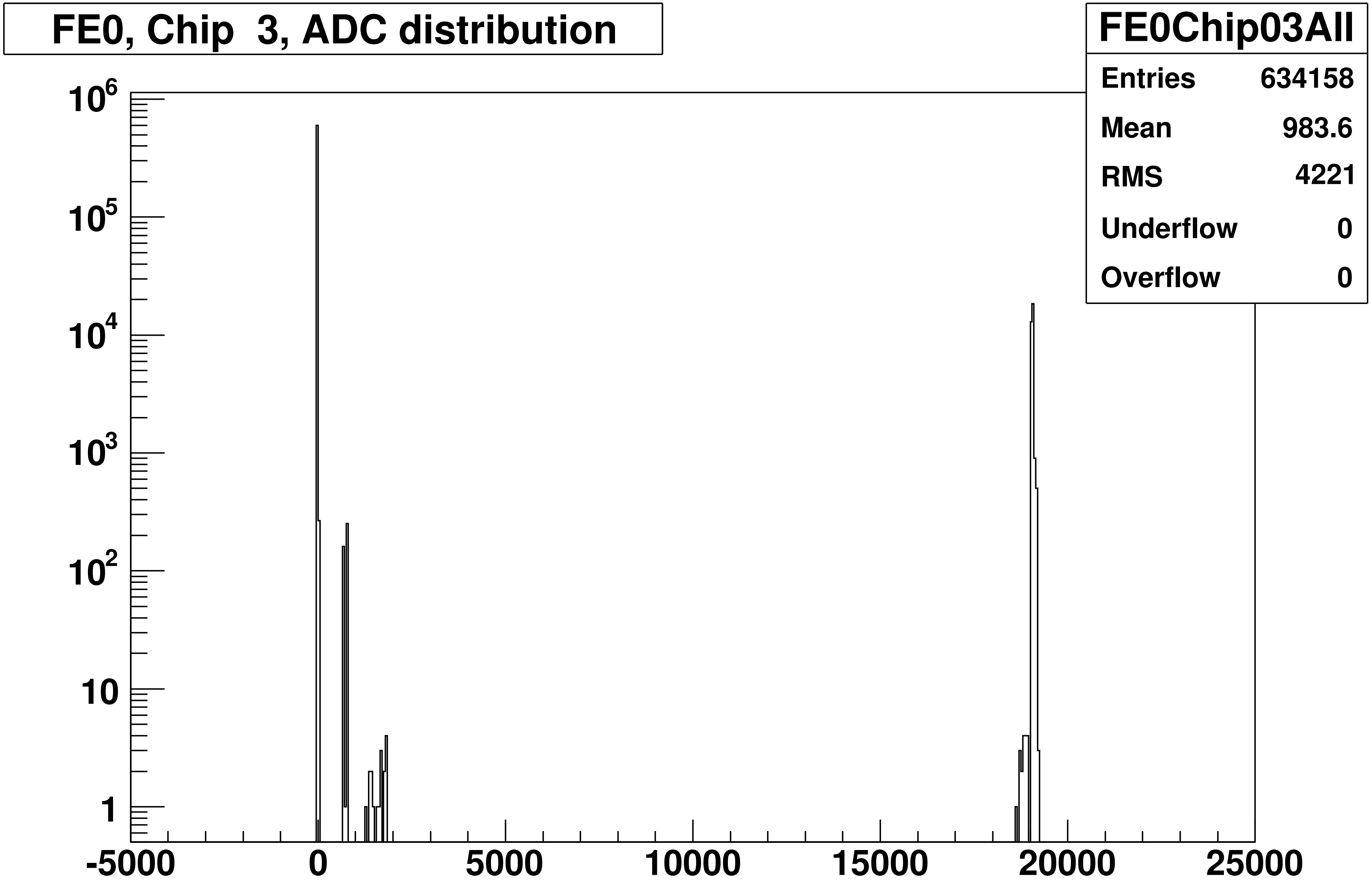
19400



FE0, Chip 3, ADC distribution
FE0Chip03All
Entries 634158
Mean 983.6
RMS 4221
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
1
-5000
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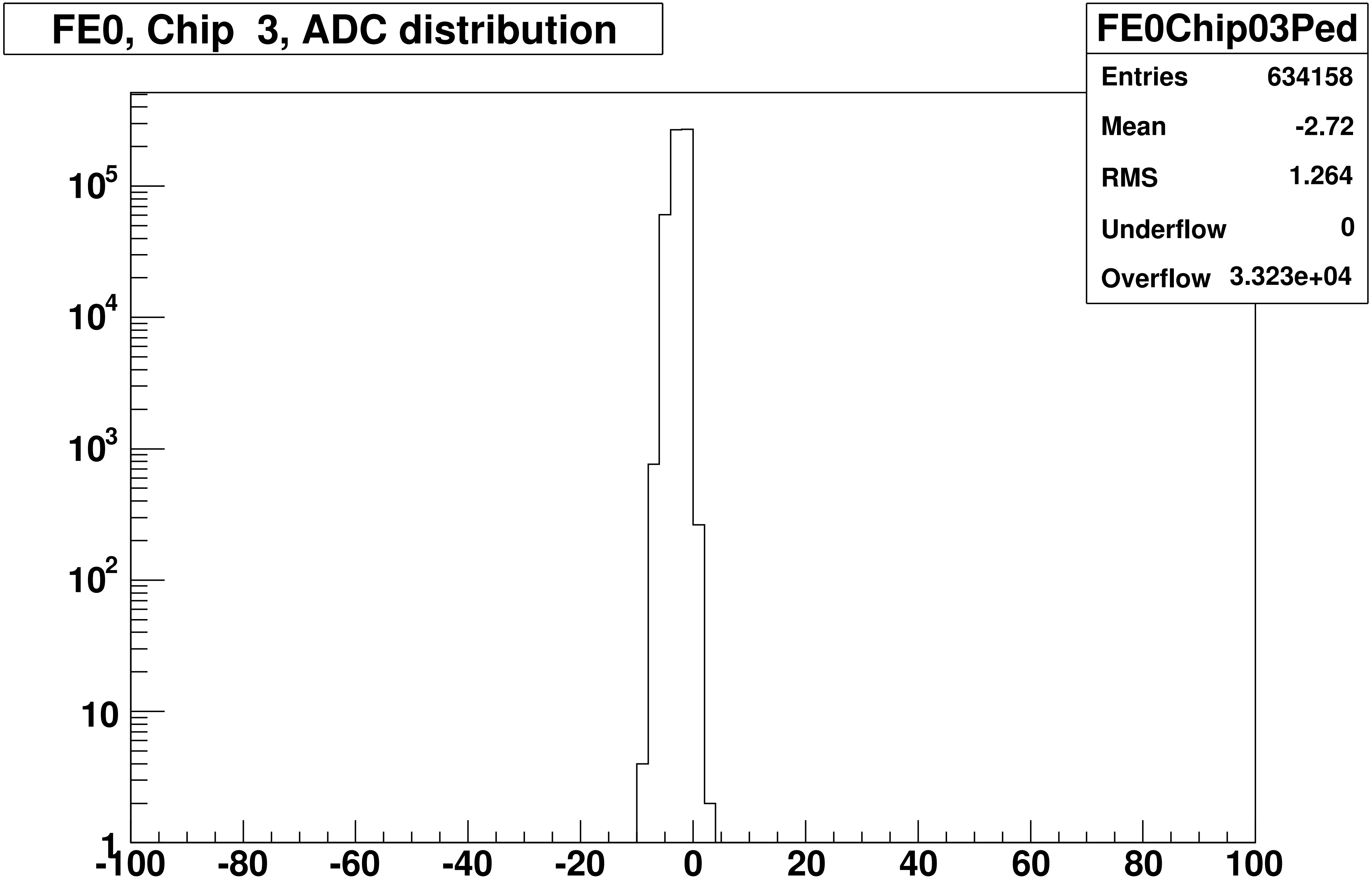

FE0, Chip 3, ADC distribution
FE0Chip03Ped
Entries 634158
Mean -2.72
RMS 1.264
Underflow 0
Overflow 3.323e+04
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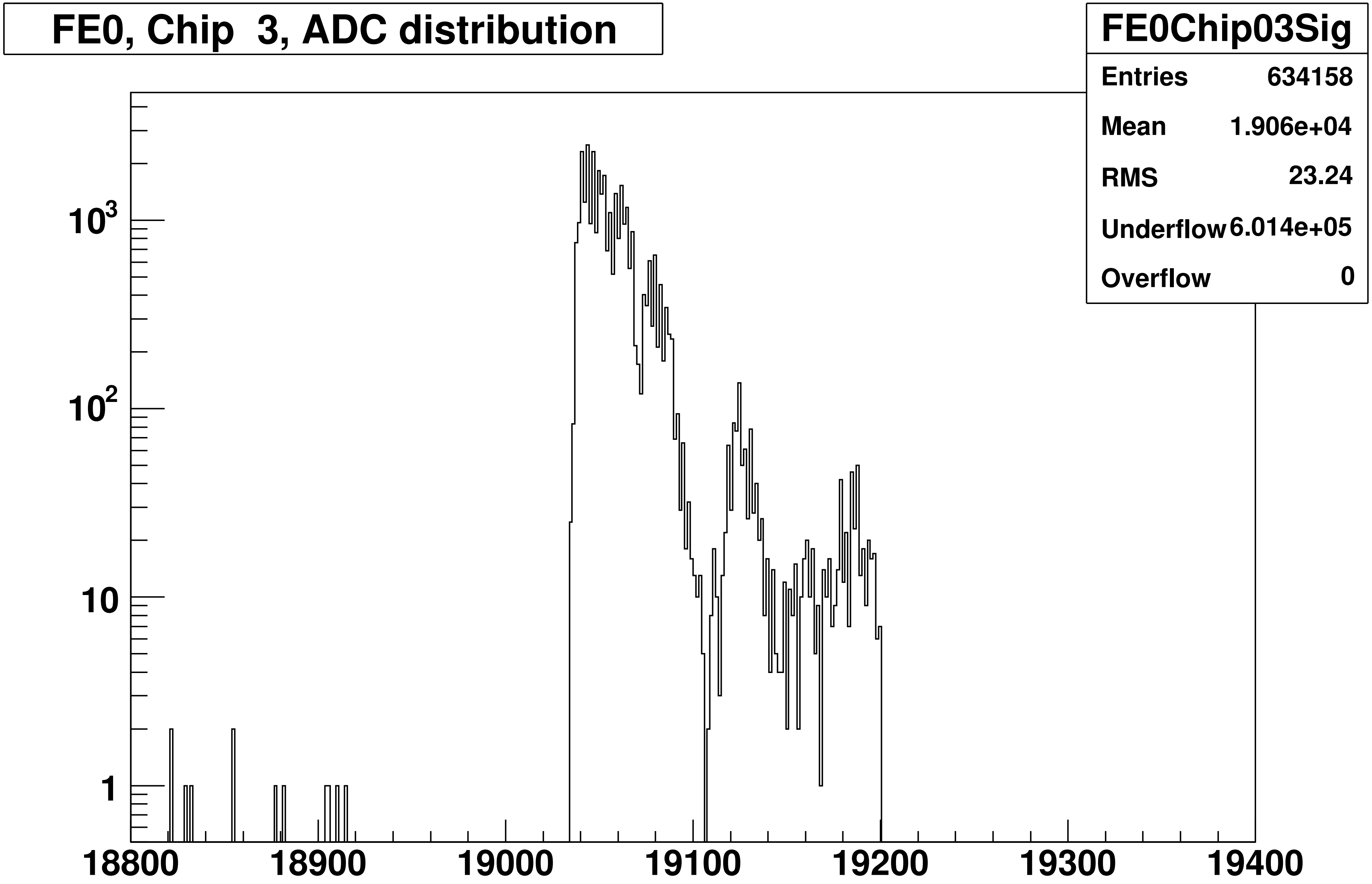
10^4
10^3
10^2
10
1
-100 -80 -60 -40 -20 0 20 40 60 80 100


FE0, Chip 3, ADC distribution
FE0Chip03Sig
Entries 634158
Mean 1.906e+04
RMS 23.24
Underflow 6.014e+05
Overflow 0
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19300
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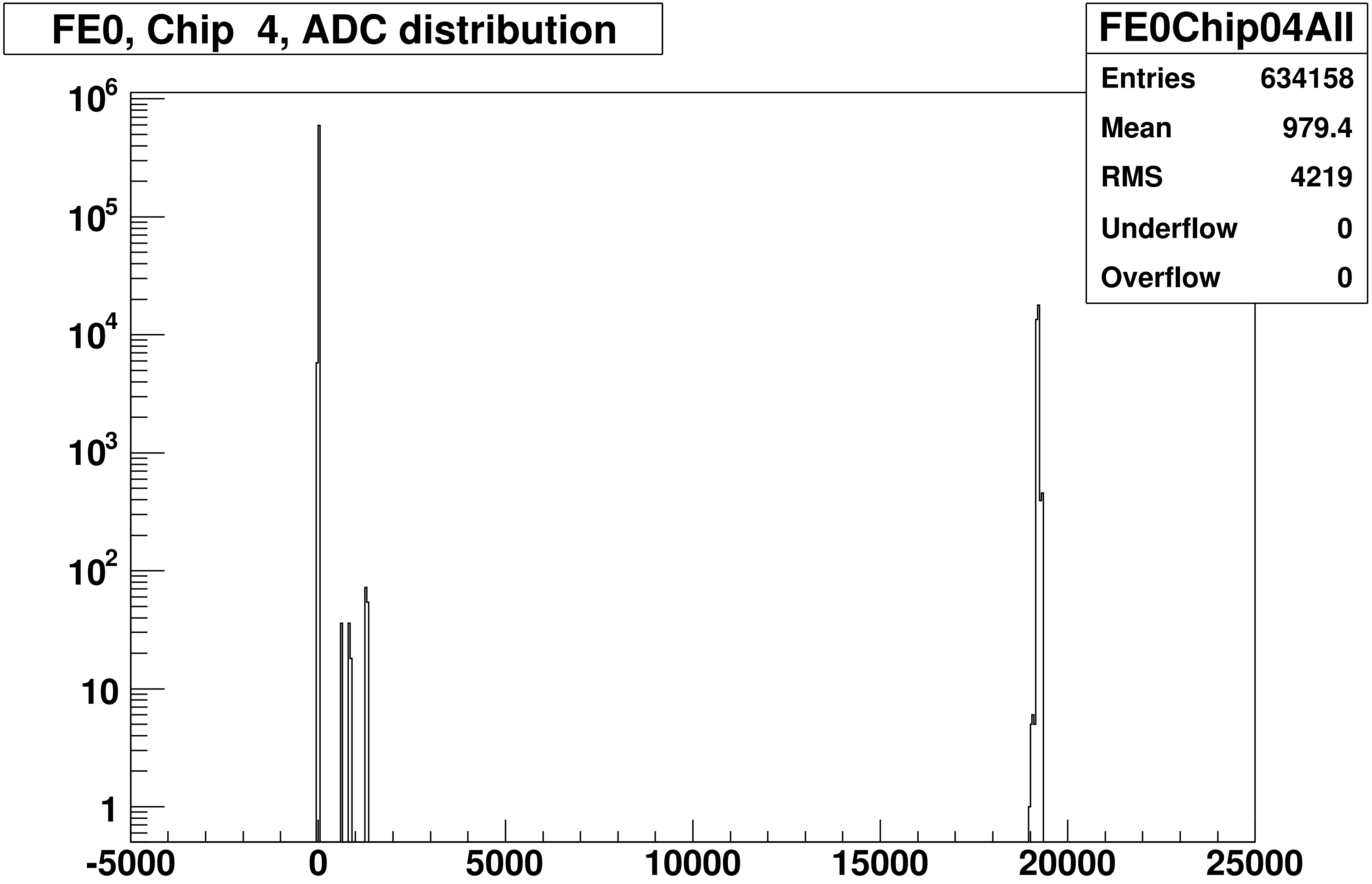
FE0, Chip 4, ADC distribution
FE0Chip04All
Entries 634158
Mean 979.4
RMS 4219
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
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-5000
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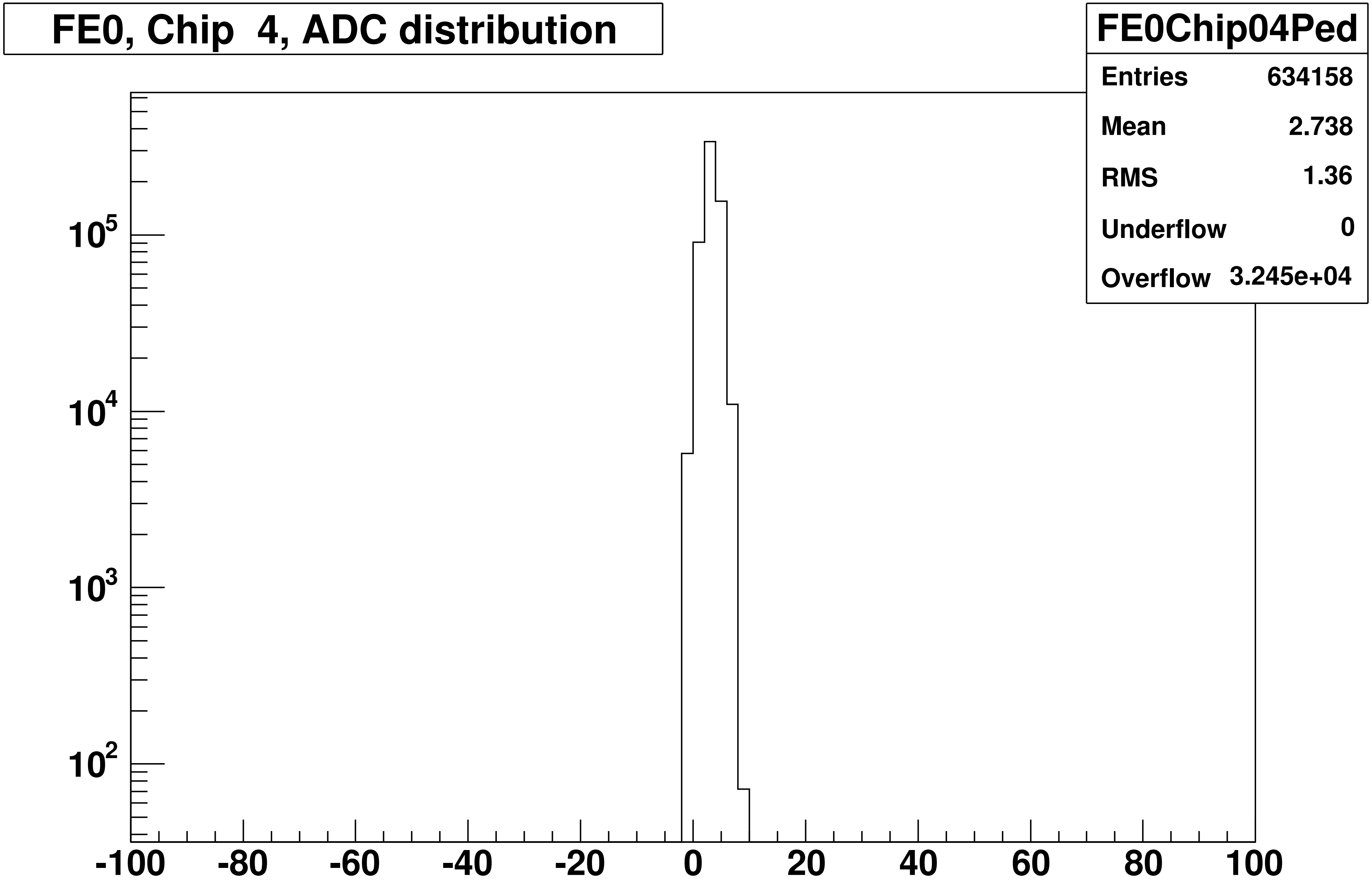
15000
20000
25000


FE0, Chip 4, ADC distribution
FE0Chip04Ped
Entries 634158
Mean 2.738
RMS 1.36
Underflow 0
Overflow 3.245e+04
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10^3
10^2
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-40
-20
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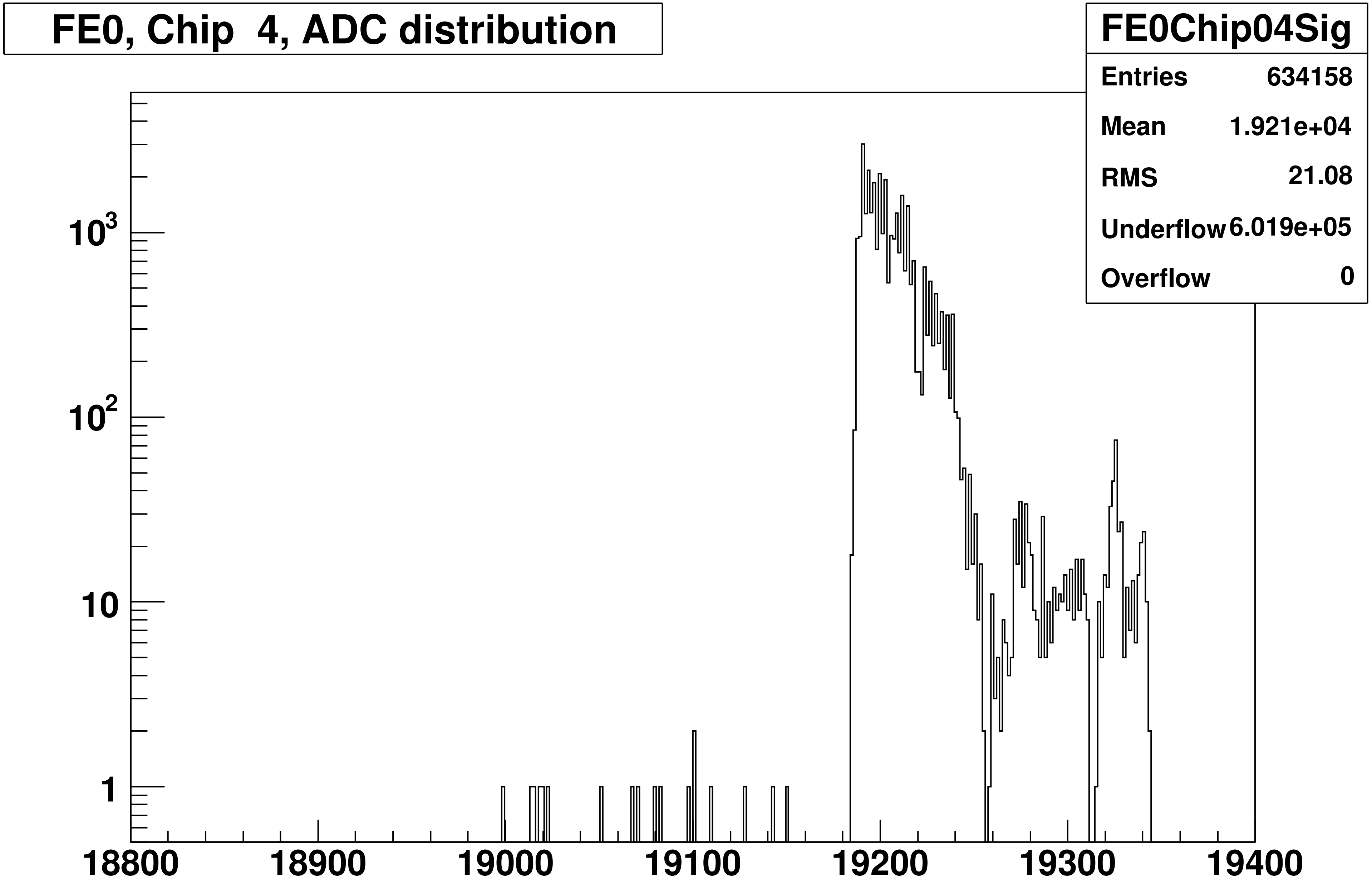
40
60
80
100


FE0, Chip 4, ADC distribution
FE0Chip04Sig
Entries 634158
Mean 1.921e+04
RMS 21.08
Underflow 6.019e+05
Overflow 0
10^3
10^2
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18900
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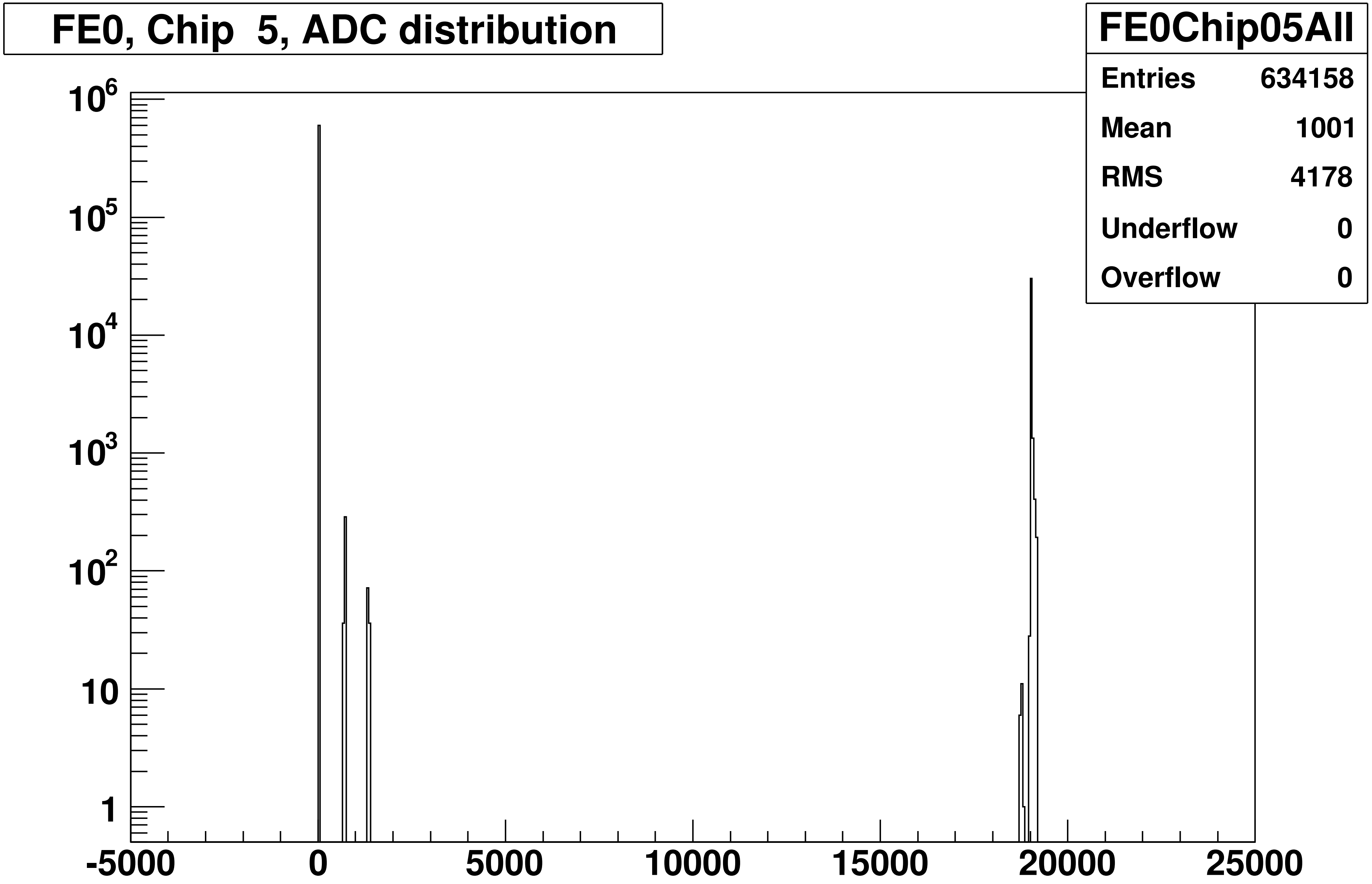
FE0, Chip 5, ADC distribution
FE0Chip05All
Entries 634158
Mean 1001
RMS 4178
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
1
-5000
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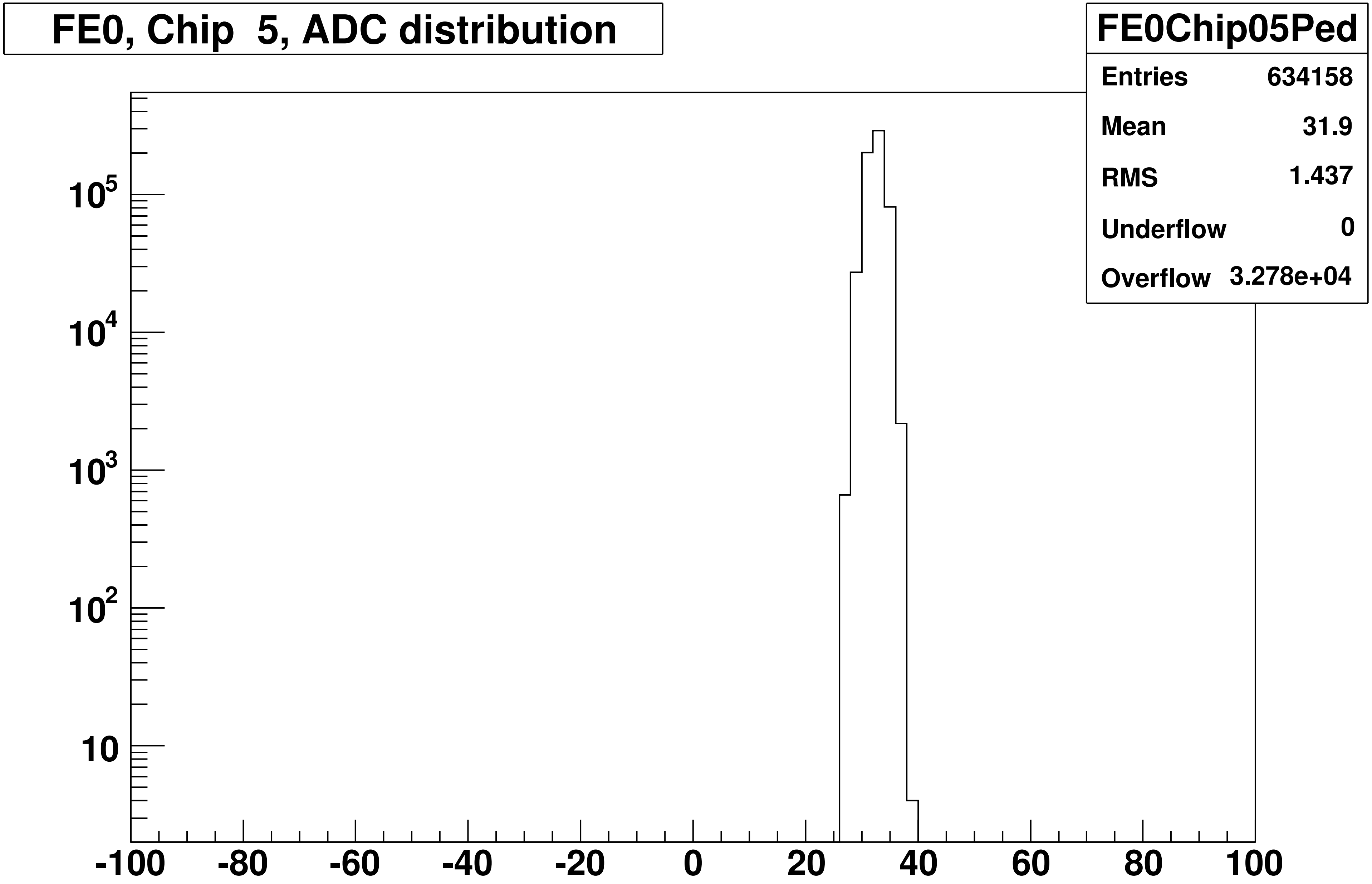
10000
15000
20000
25000


FE0, Chip 5, ADC distribution
FE0Chip05Ped
Entries 634158
Mean 31.9
RMS 1.437
Underflow 0
Overflow 3.278e+04
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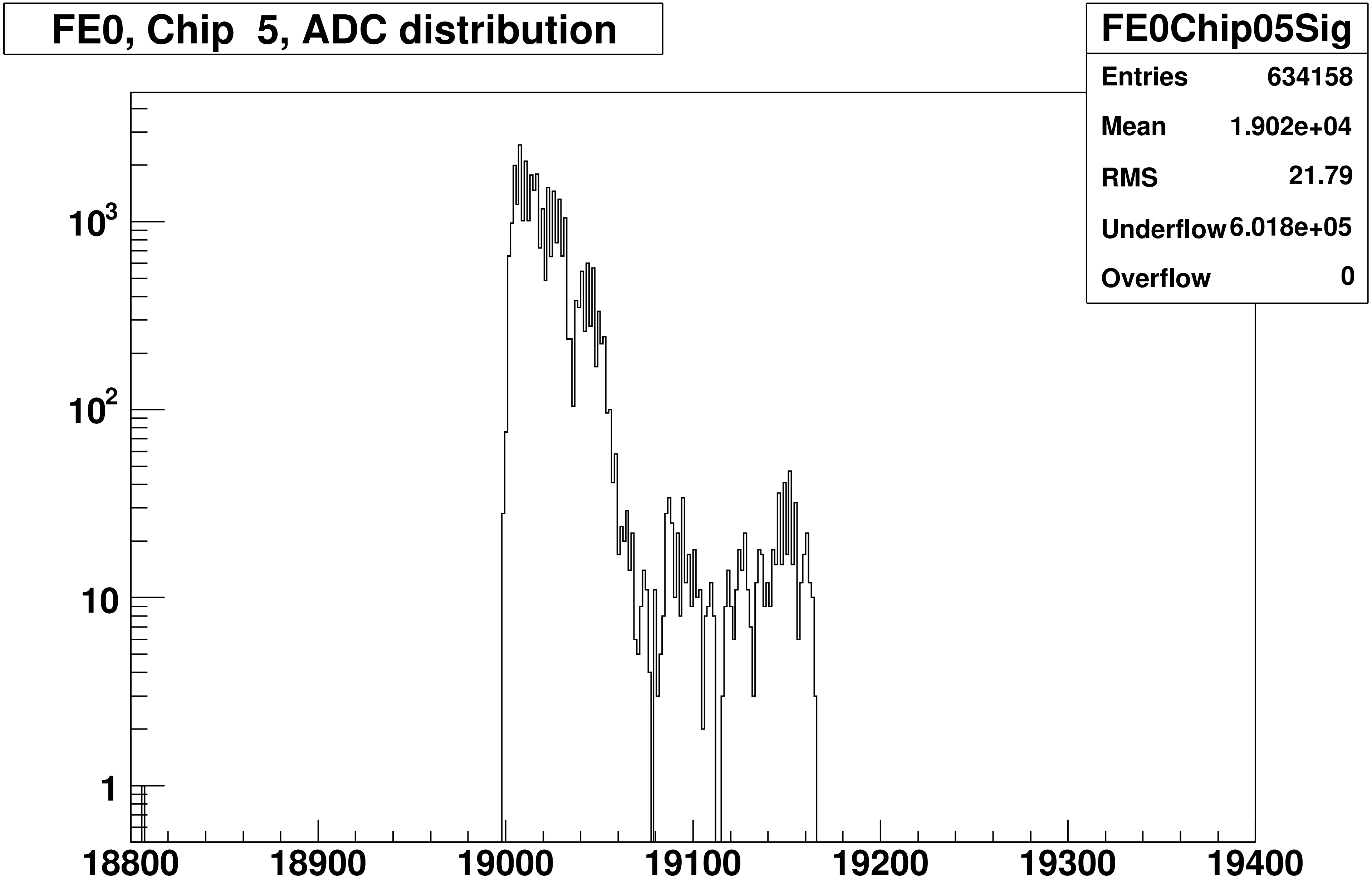
10^4
10^3
10^2
10
-100 -80 -60 -40 -20 0 20 40 60 80 100


FE0, Chip 5, ADC distribution
FE0Chip05Sig
Entries 634158
Mean 1.902e+04
RMS 21.79
Underflow 6.018e+05
Overflow 0
10^3
10^2
10
1
18800
18900
19000
19100
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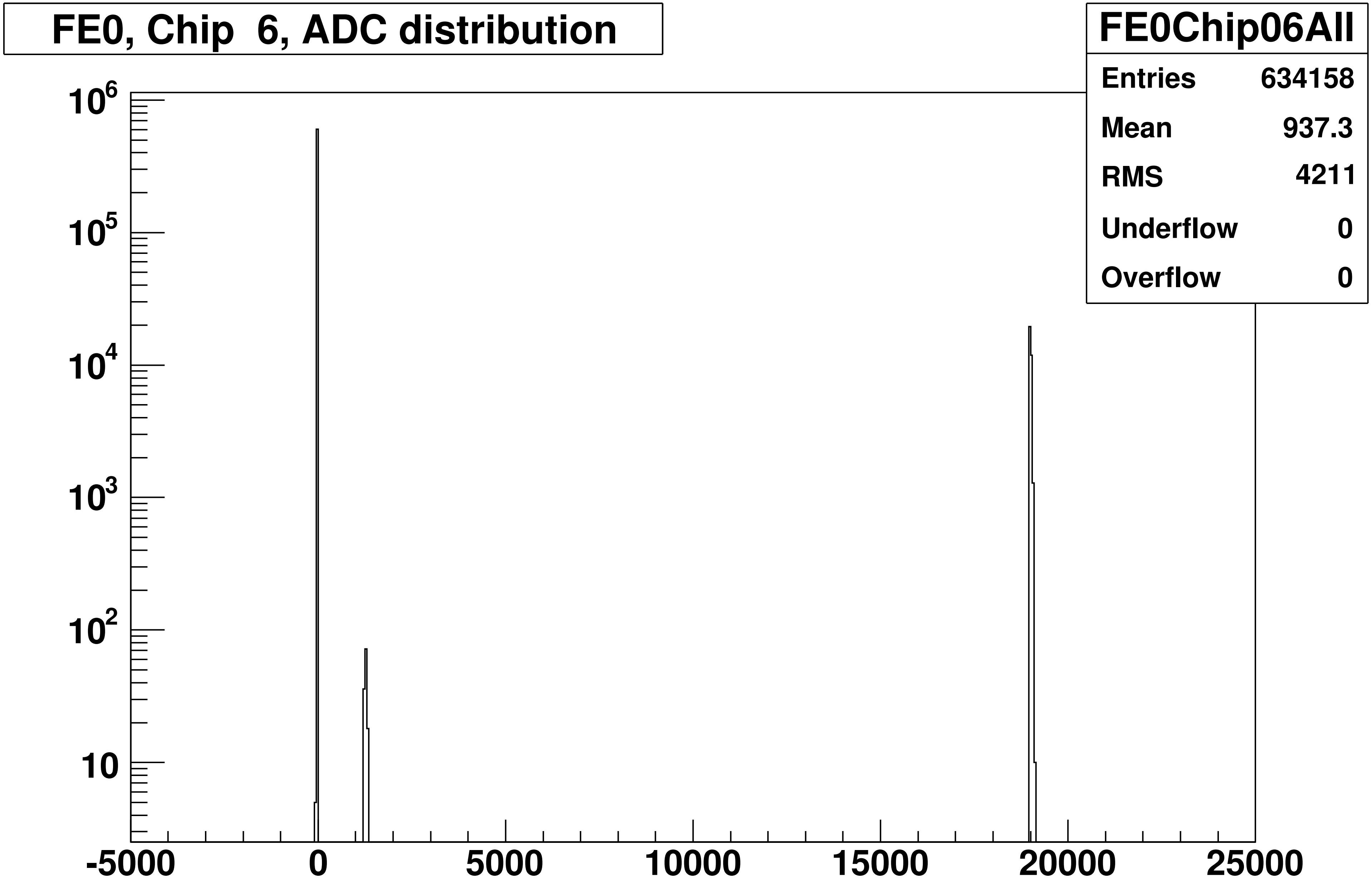
19300
19400


FE0, Chip 6, ADC distribution
FE0Chip06All
Entries 634158
Mean 937.3
RMS 4211
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
-5000
0
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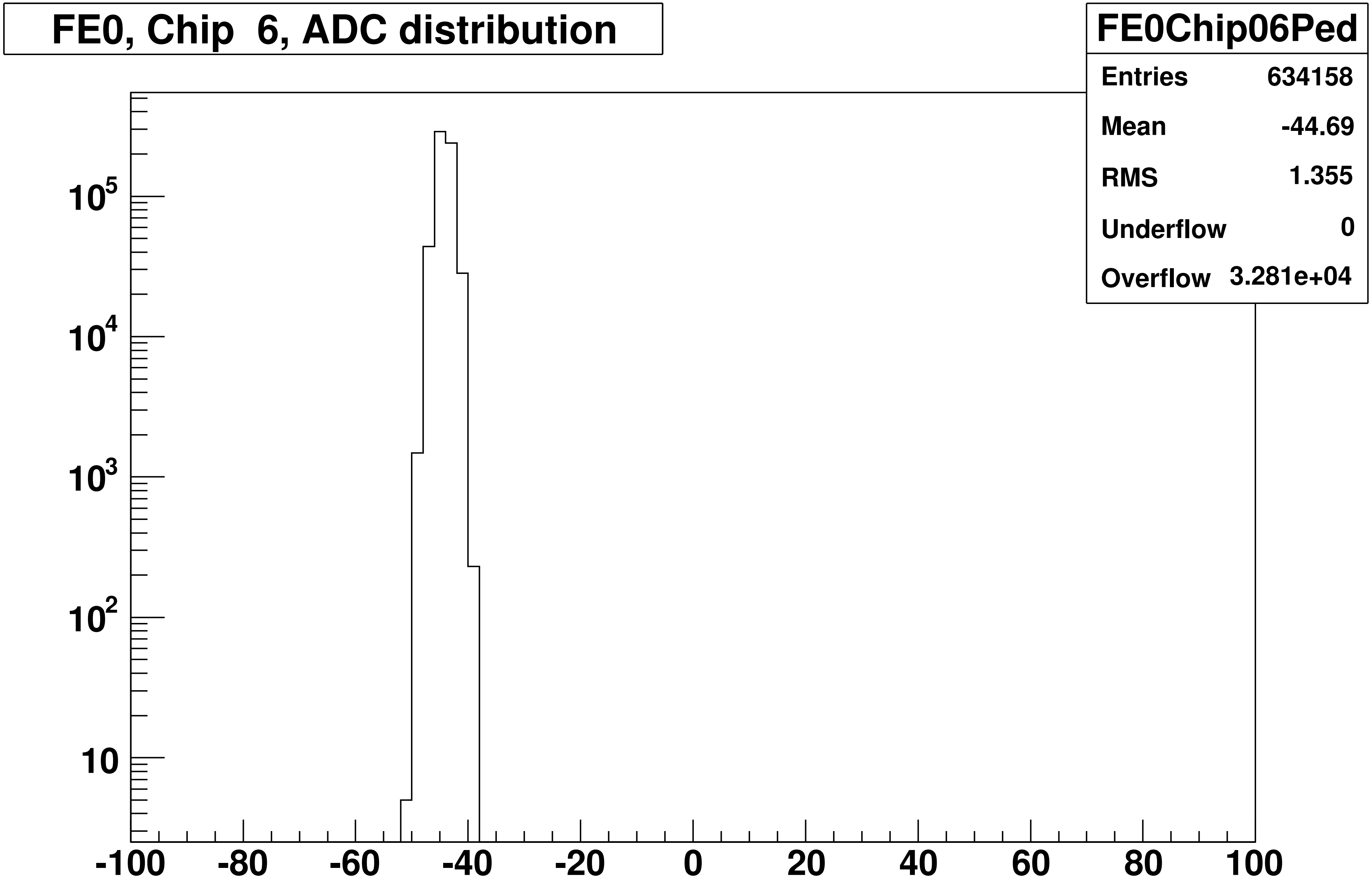
10000
15000
20000
25000


FE0, Chip 6, ADC distribution
FE0Chip06Ped
Entries 634158
Mean -44.69
RMS 1.355
Underflow 0
Overflow 3.281e+04
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10^2
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10^4
10^5
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80
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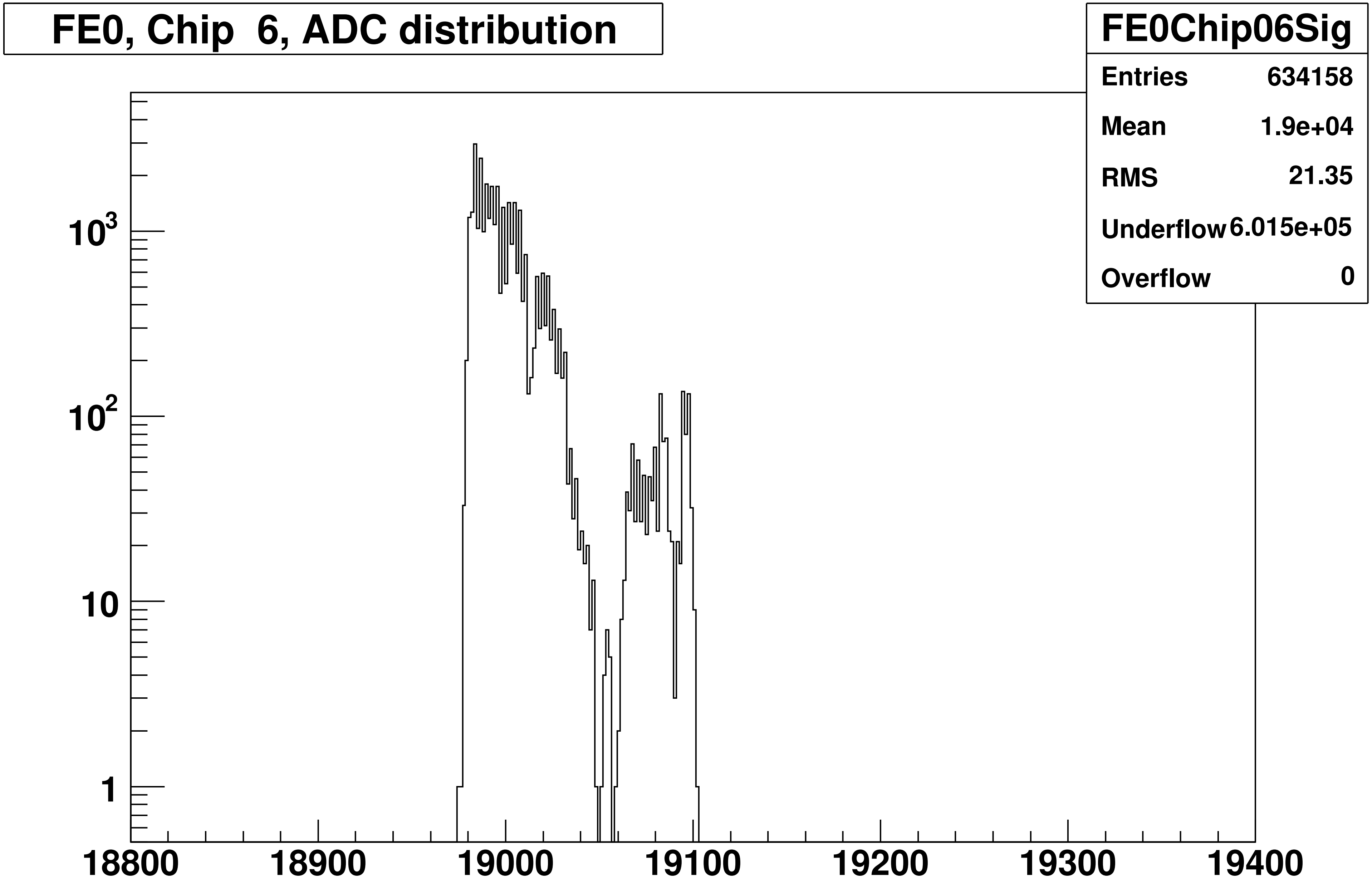
FE0, Chip 6, ADC distribution
FE0Chip06Sig
Entries 634158
Mean 1.9e+04
RMS 21.35
Underflow 6.015e+05
Overflow 0
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10^2
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18900
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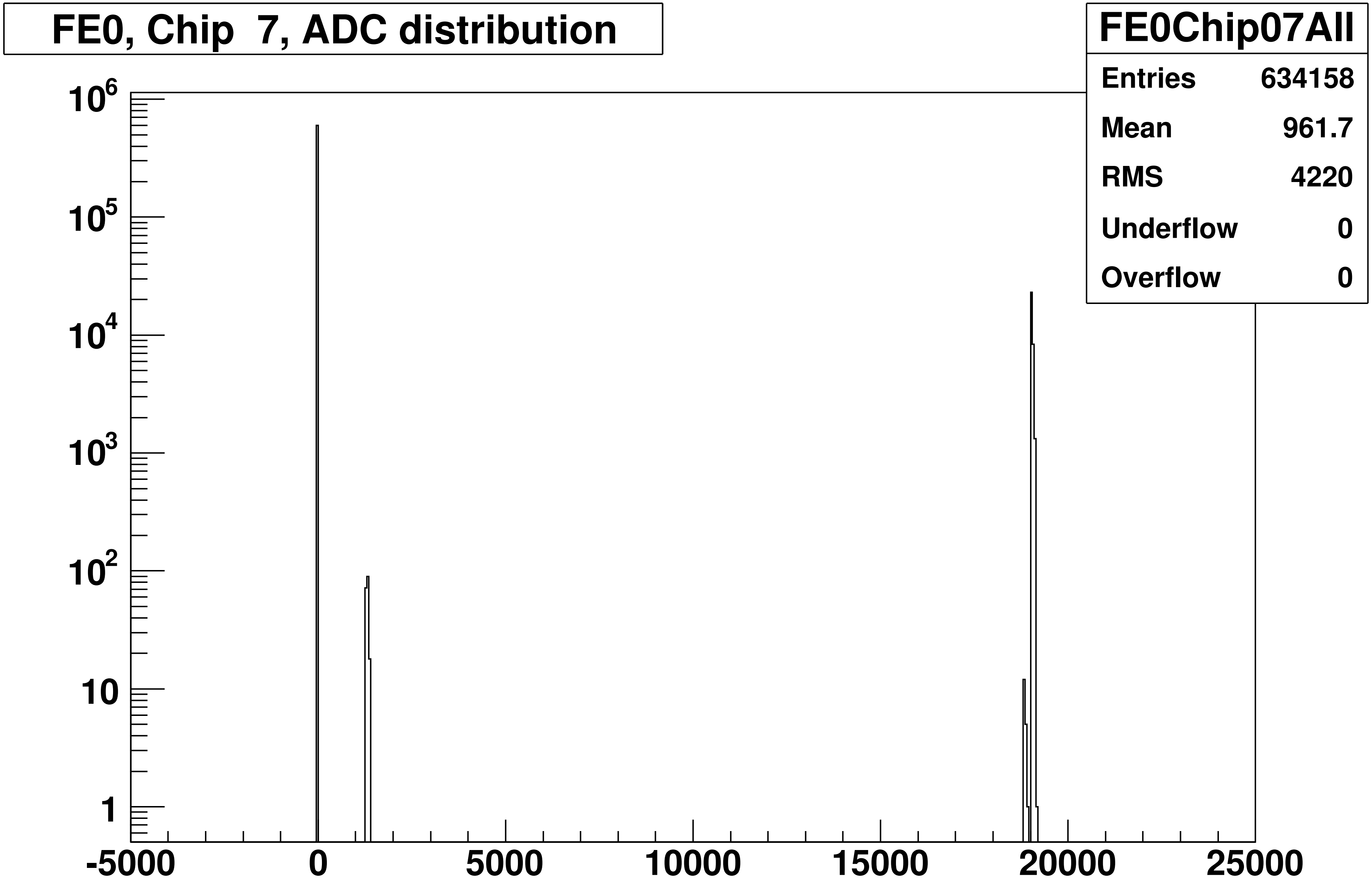

FE0, Chip 7, ADC distribution
FE0Chip07All
Entries 634158
Mean 961.7
RMS 4220
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
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-5000
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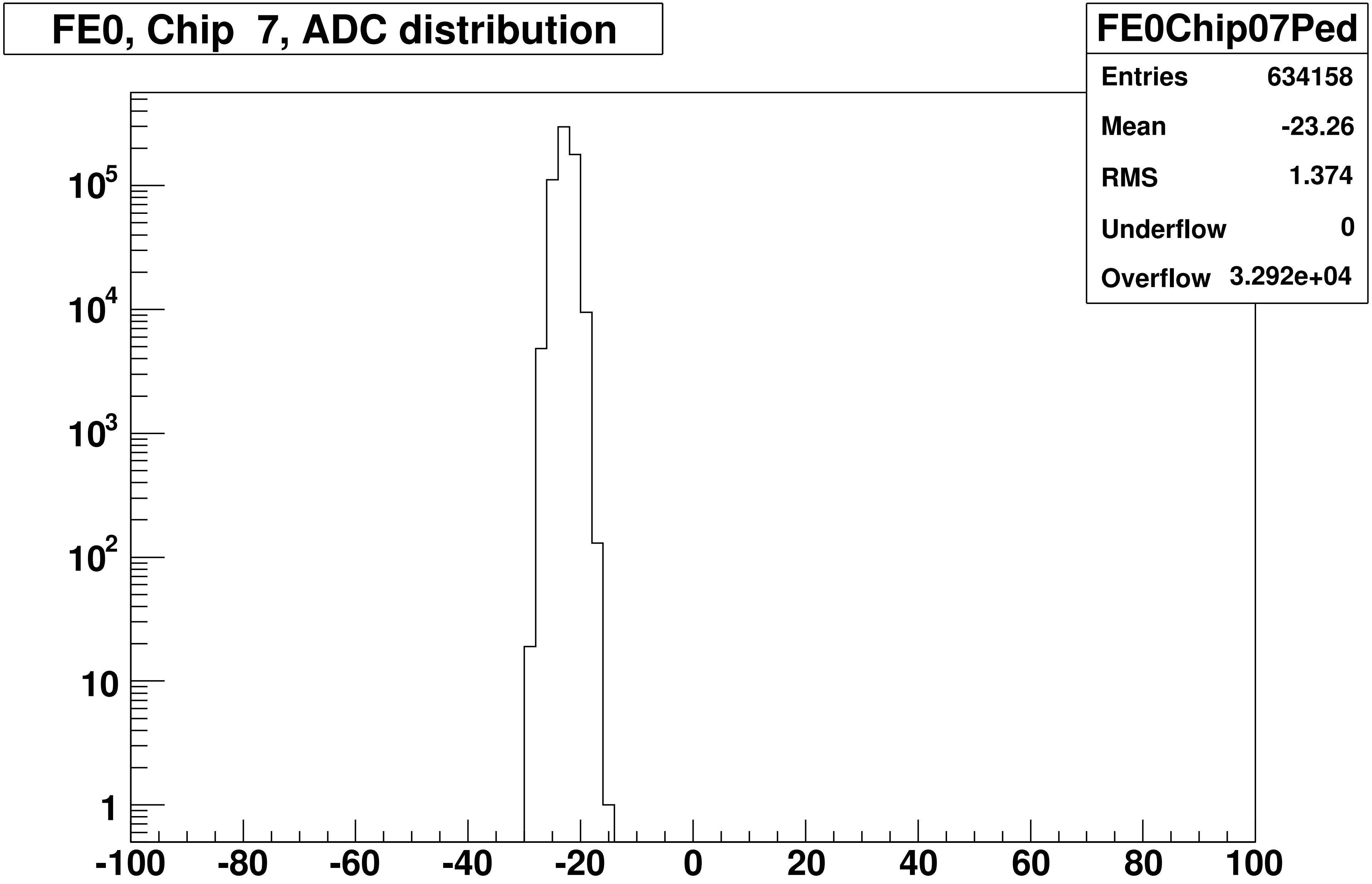
10000
15000
20000
25000


FE0, Chip 7, ADC distribution
FE0Chip07Ped
Entries 634158
Mean -23.26
RMS 1.374
Underflow 0
Overflow 3.292e+04
10^5
10^4
10^3
10^2
10
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-20
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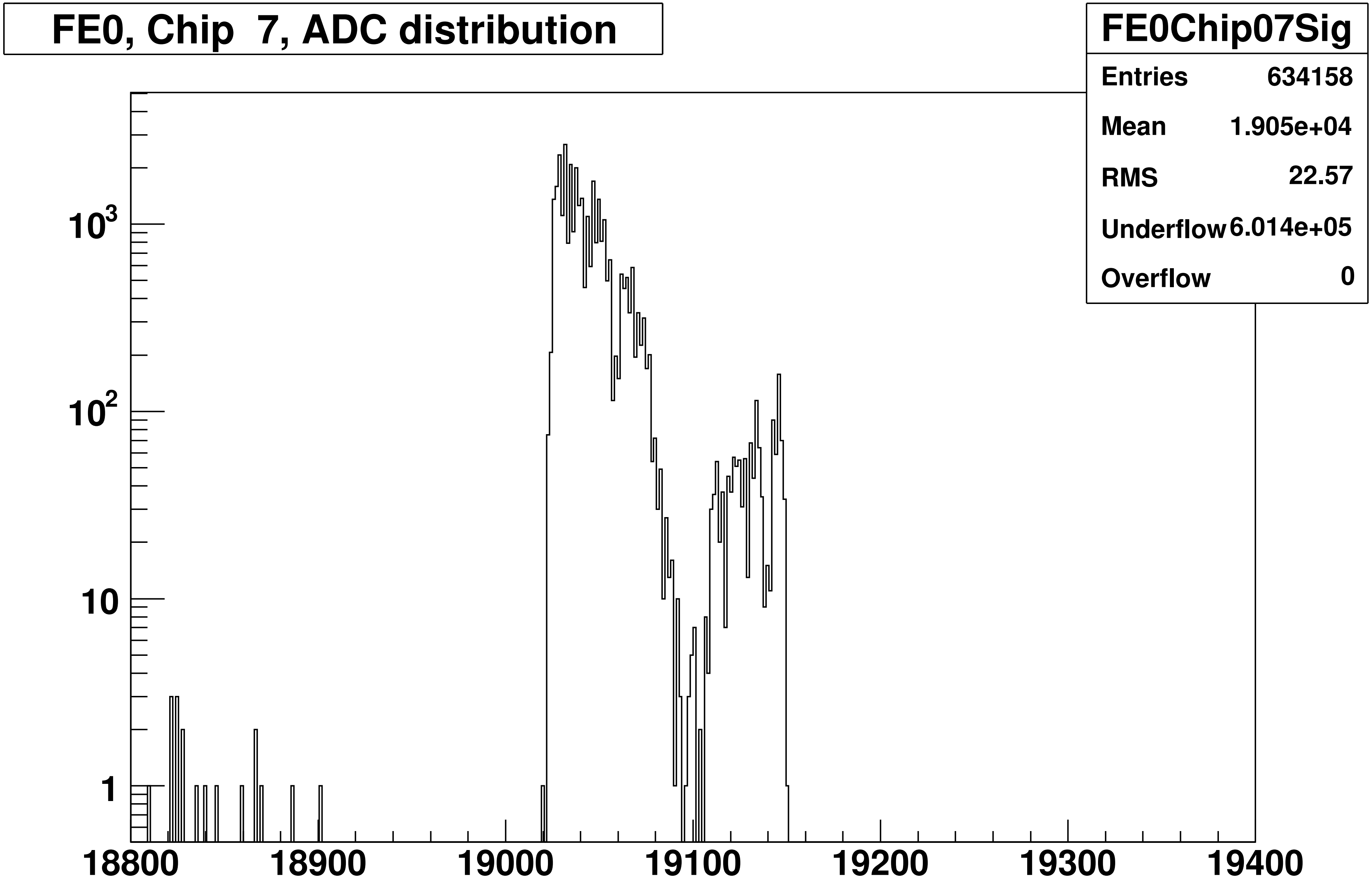

FE0, Chip 7, ADC distribution
FE0Chip07Sig
Entries 634158
Mean 1.905e+04
RMS 22.57
Underflow 6.014e+05
Overflow 0
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10^2
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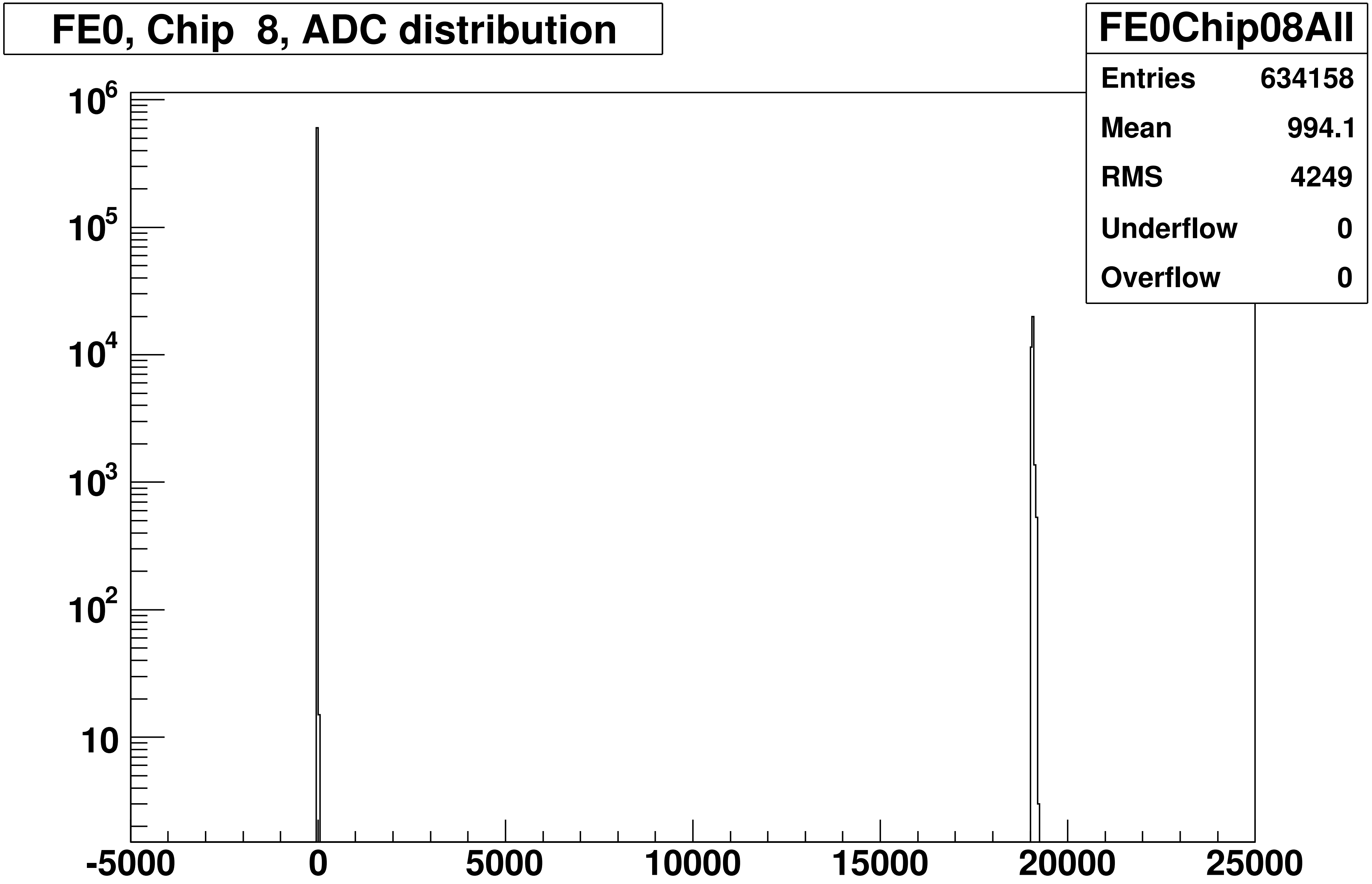
FE0, Chip 8, ADC distribution
FE0Chip08All
Entries 634158
Mean 994.1
RMS 4249
Underflow 0
Overflow 0
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10^2
10^3
10^4
10^5
10^6
-5000
0
5000
10000
15000
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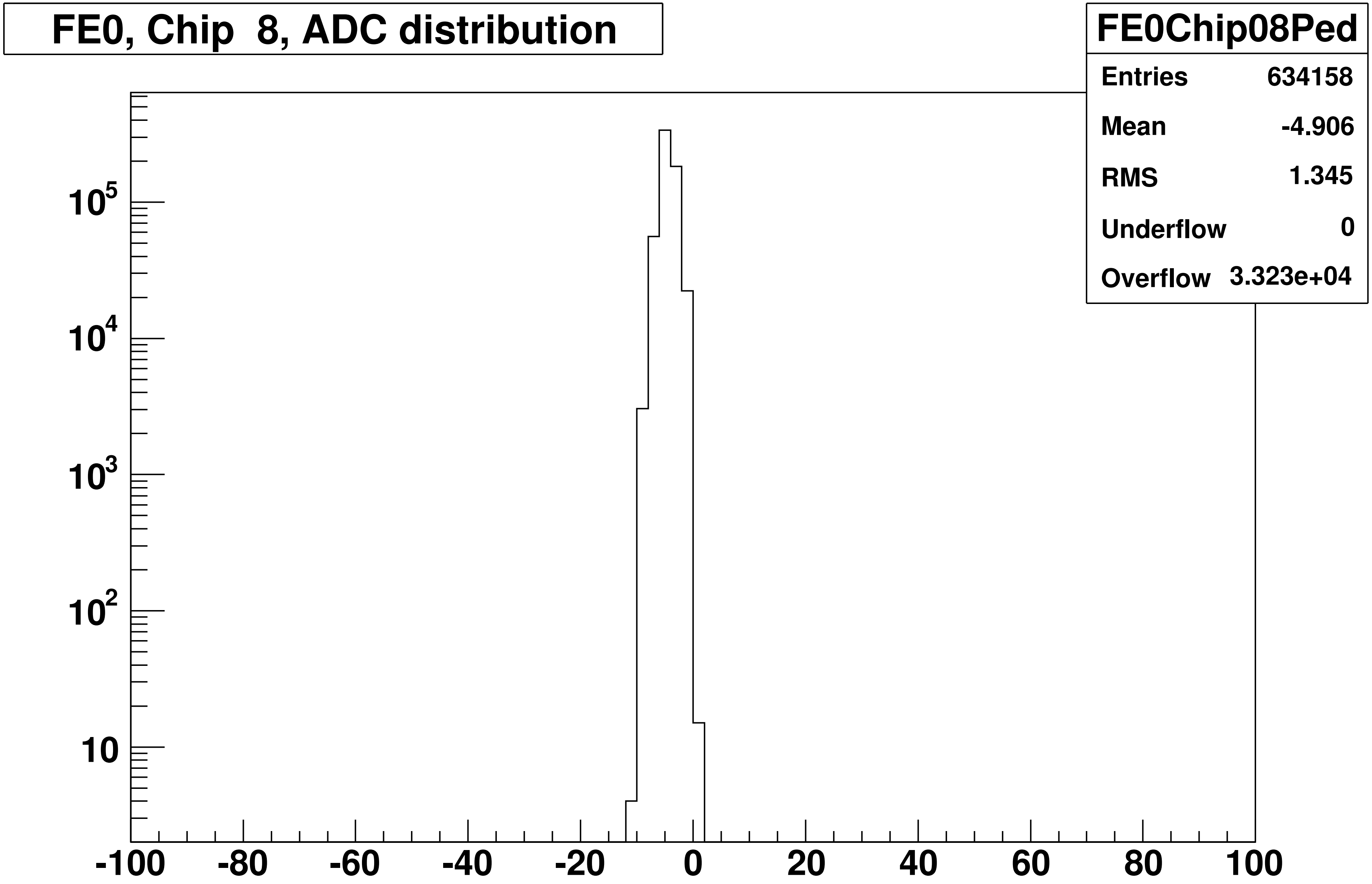
FE0, Chip 8, ADC distribution
FE0Chip08Ped
Entries 634158
Mean -4.906
RMS 1.345
Underflow 0
Overflow 3.323e+04
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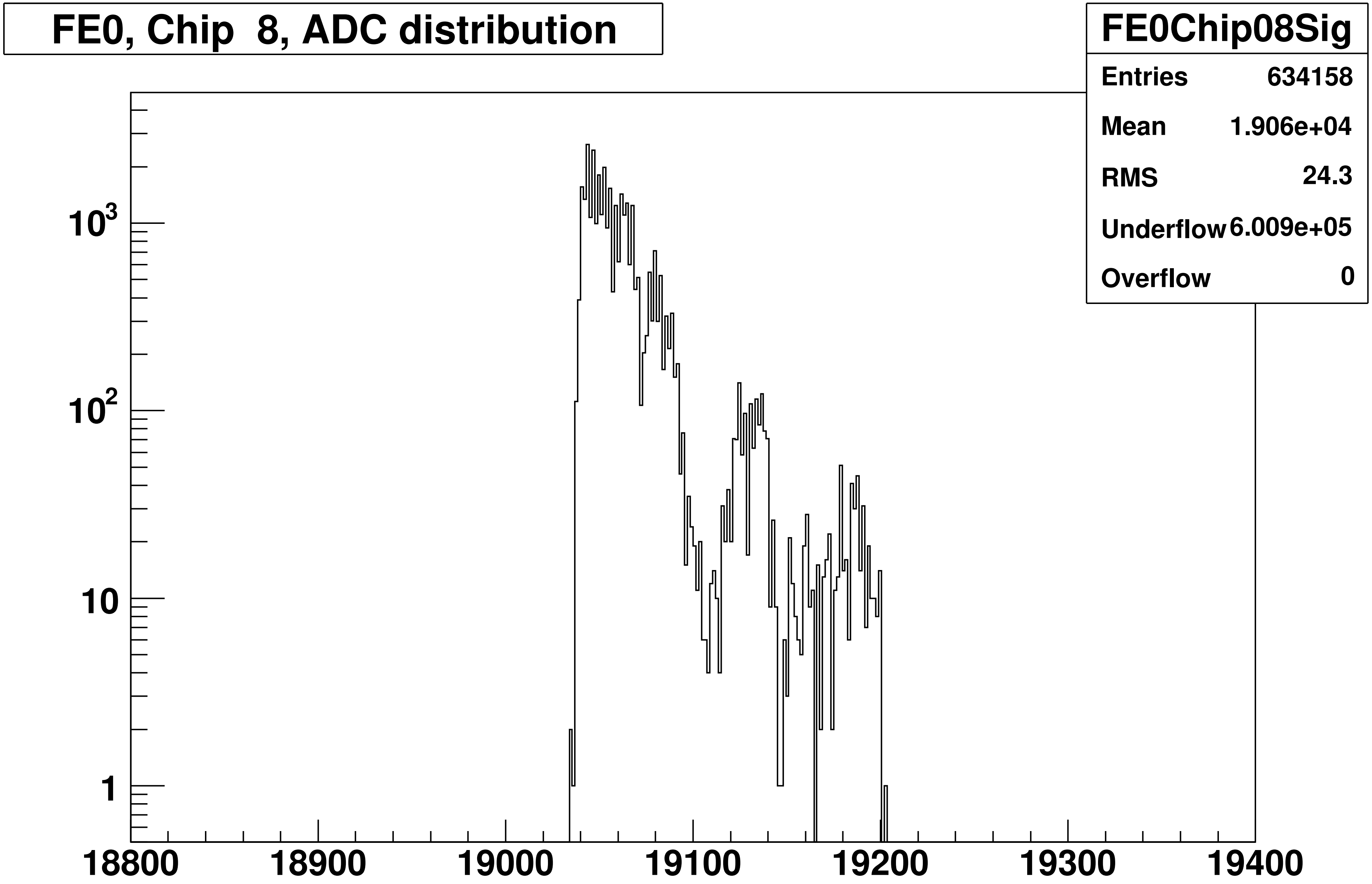
FE0, Chip 8, ADC distribution
FE0Chip08Sig
Entries 634158
Mean 1.906e+04
RMS 24.3
Underflow 6.009e+05
Overflow 0
10^3
10^2
10
1
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18900
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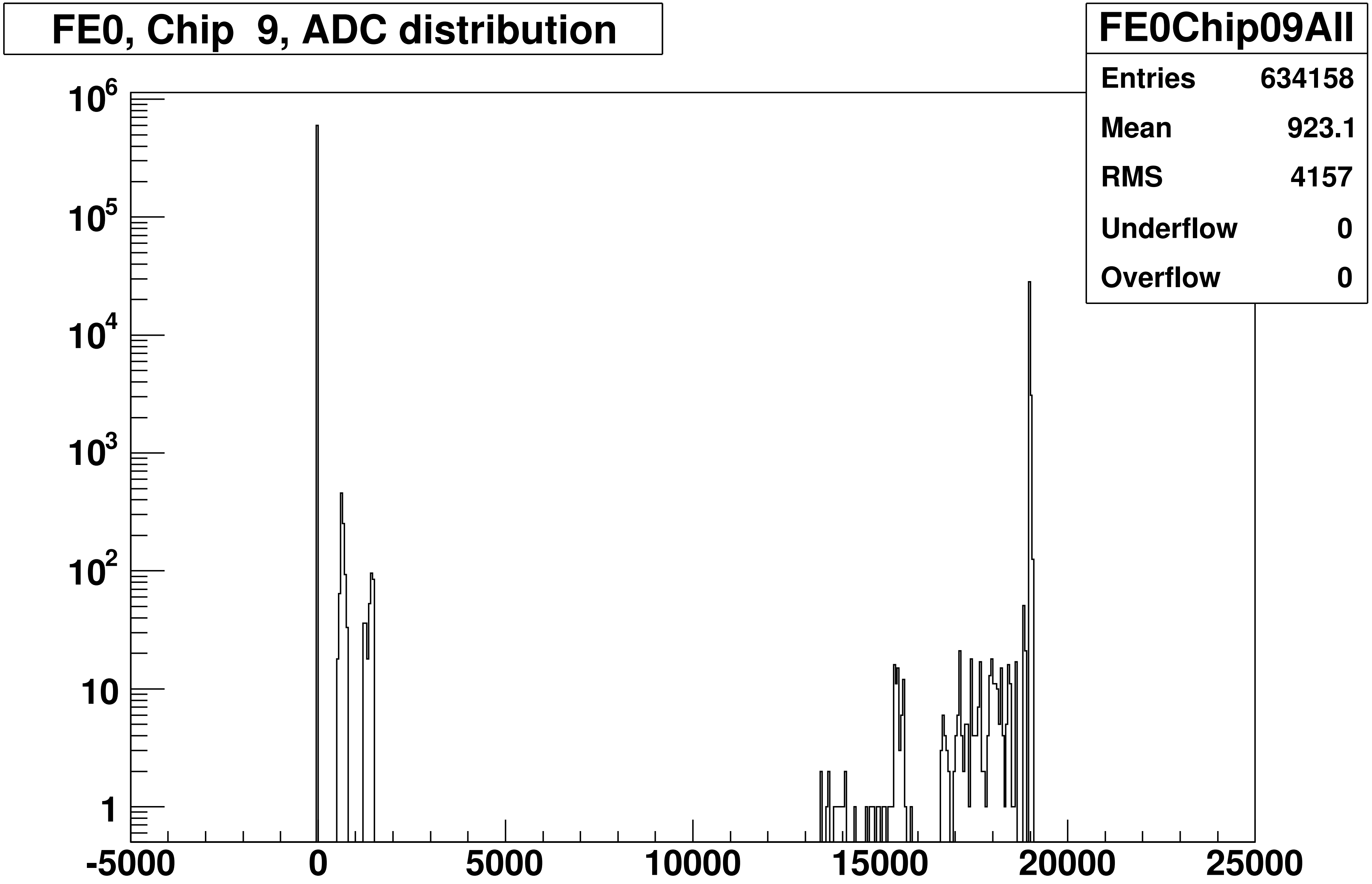
19400


FE0, Chip 9, ADC distribution
FE0Chip09All
Entries 634158
Mean 923.1
RMS 4157
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
1
-5000
0
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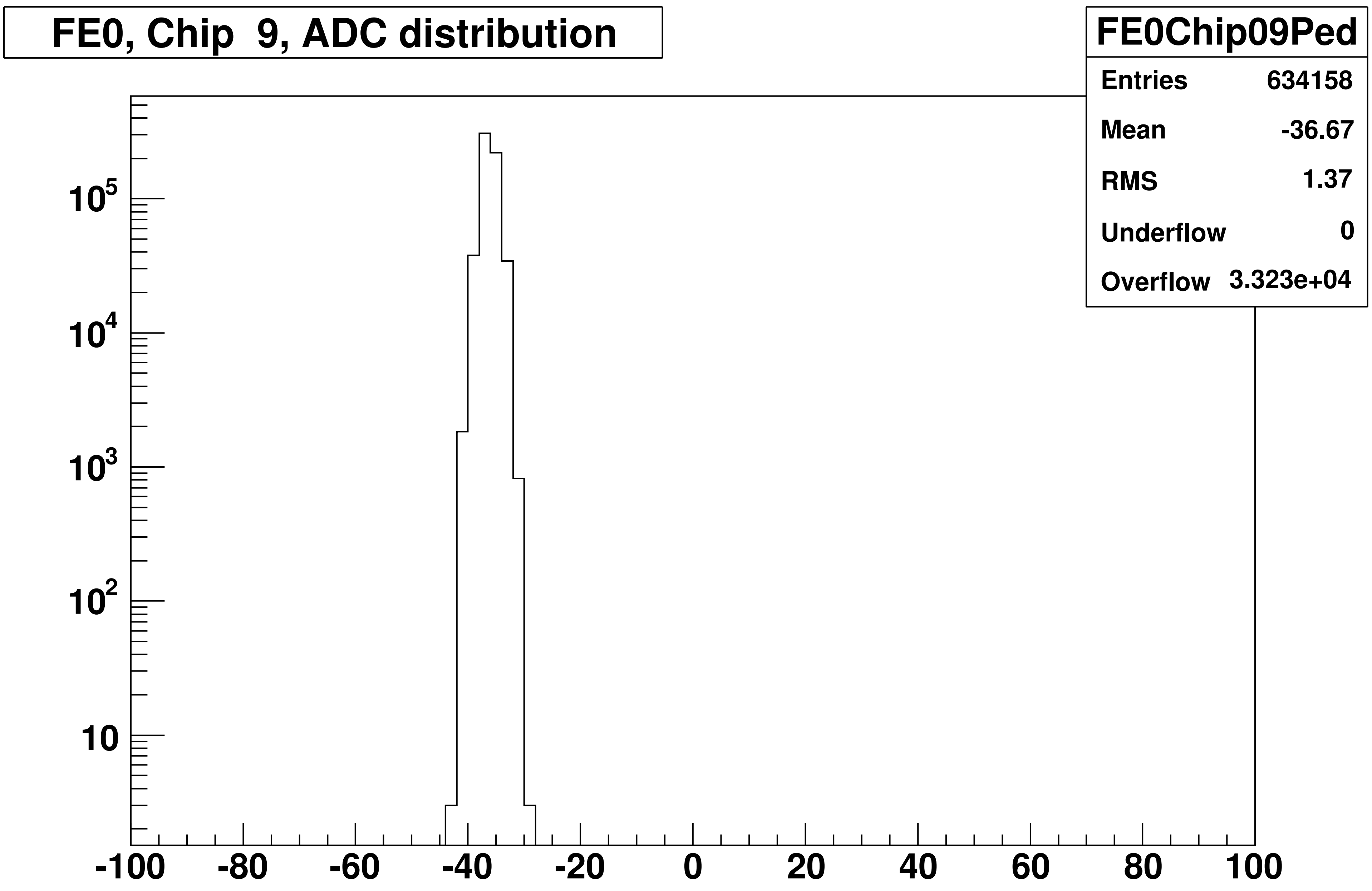
10000
15000
20000
25000



FE0, Chip 9, ADC distribution
FE0Chip09Ped
Entries 634158
Mean -36.67
RMS 1.37
Underflow 0
Overflow 3.323e+04
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10^4
10^5
-100
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-20
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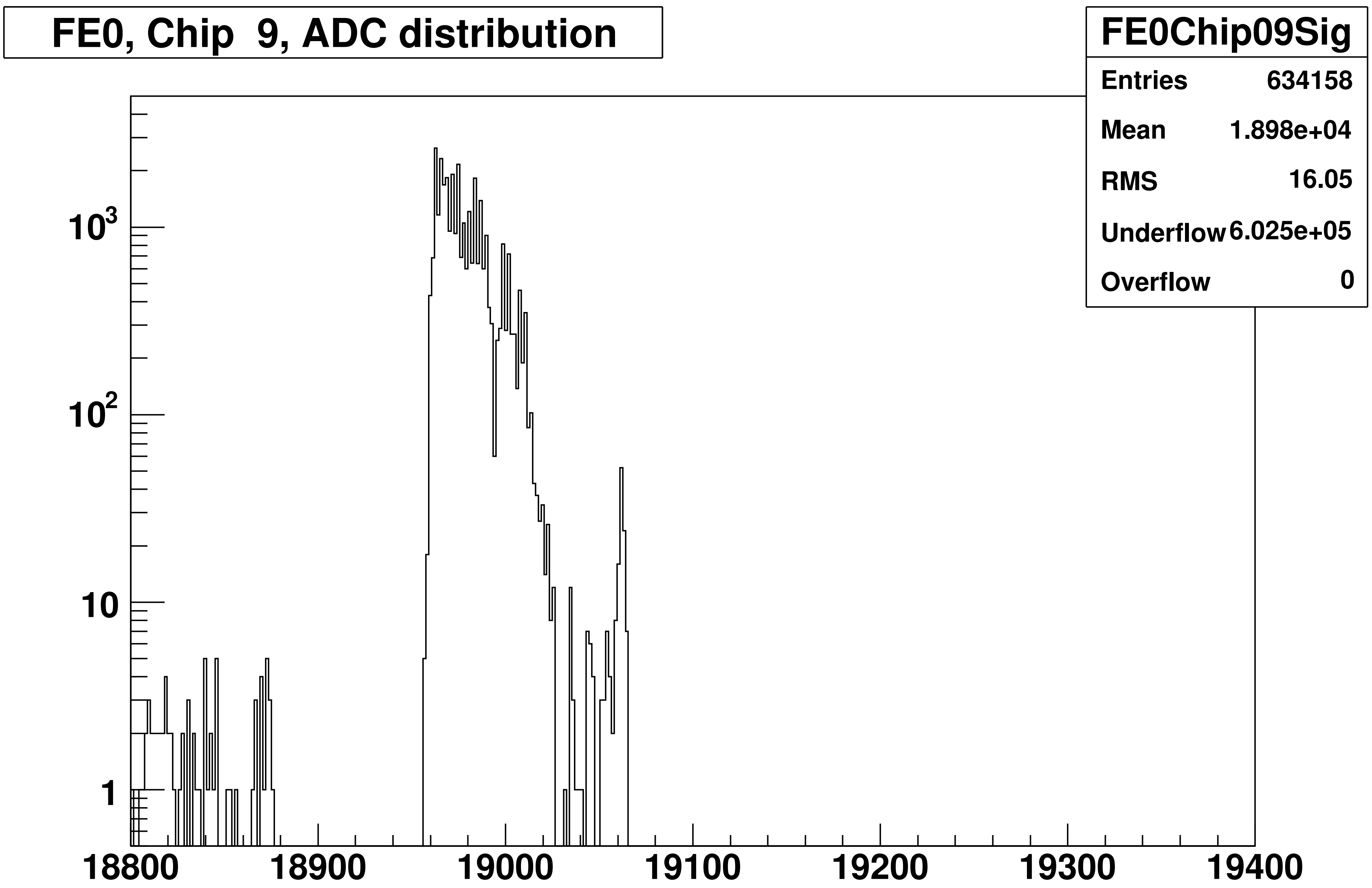
40
60
80
100


FE0, Chip 9, ADC distribution
FE0Chip09Sig
Entries 634158
Mean 1.898e+04
RMS 16.05
Underflow 6.025e+05
Overflow 0
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10^2
10
1
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18900
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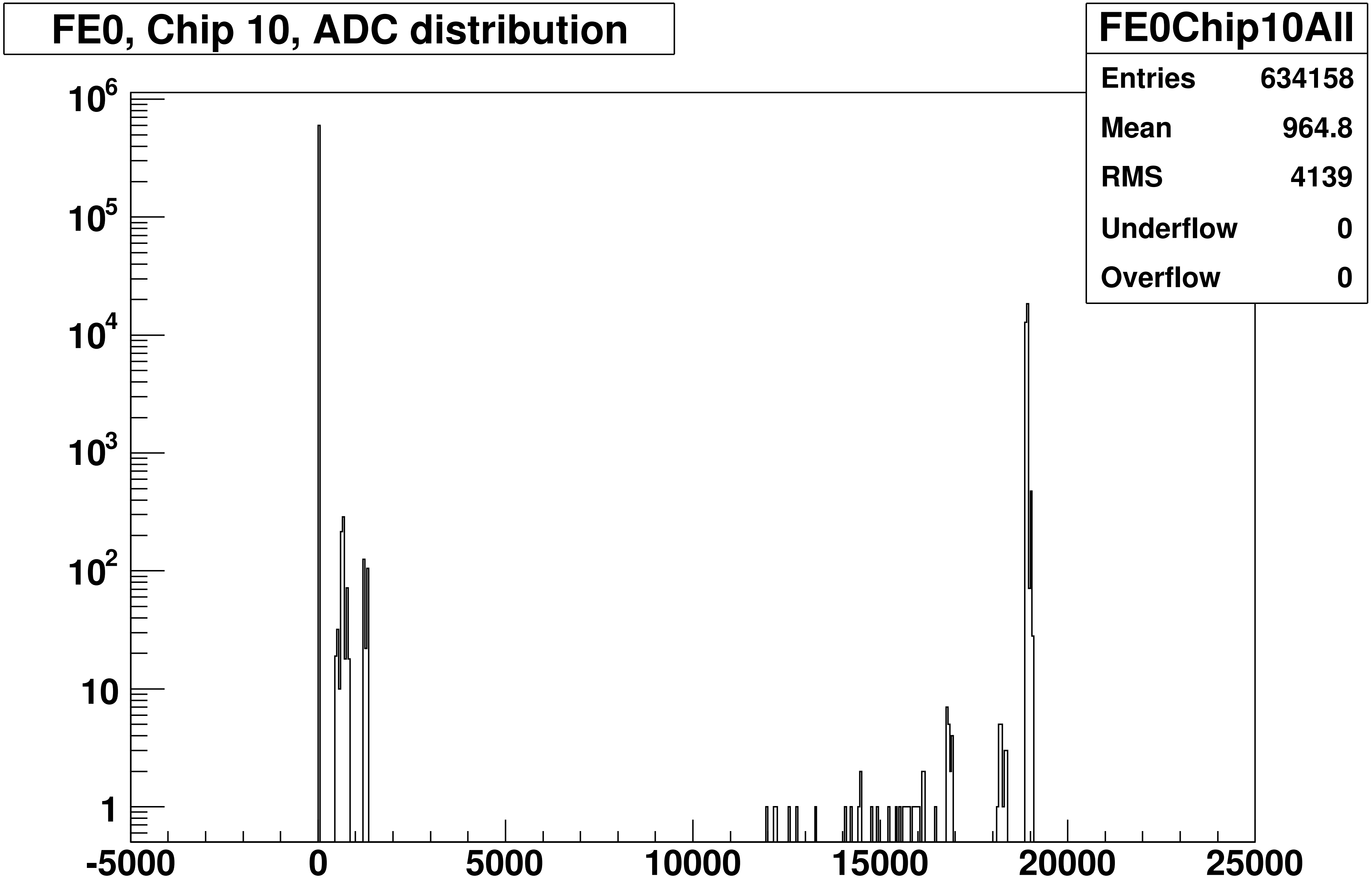
19400



FE0, Chip 10, ADC distribution
FE0Chip10All
Entries 634158
Mean 964.8
RMS 4139
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
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-5000
0
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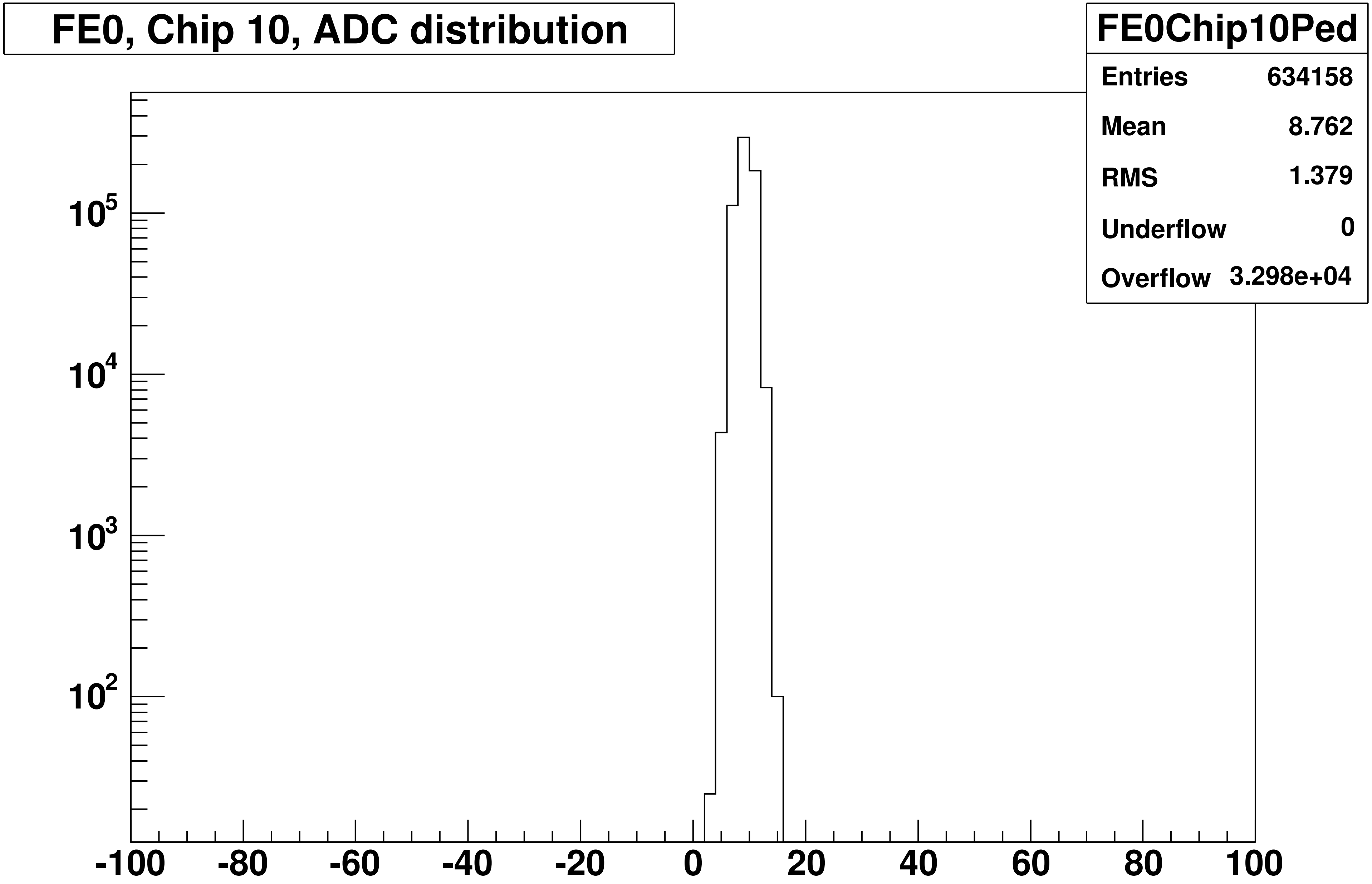
20000
25000


FE0, Chip 10, ADC distribution
FE0Chip10Ped
Entries 634158
Mean 8.762
RMS 1.379
Underflow 0
Overflow 3.298e+04
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10^3
10^2
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-20
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80
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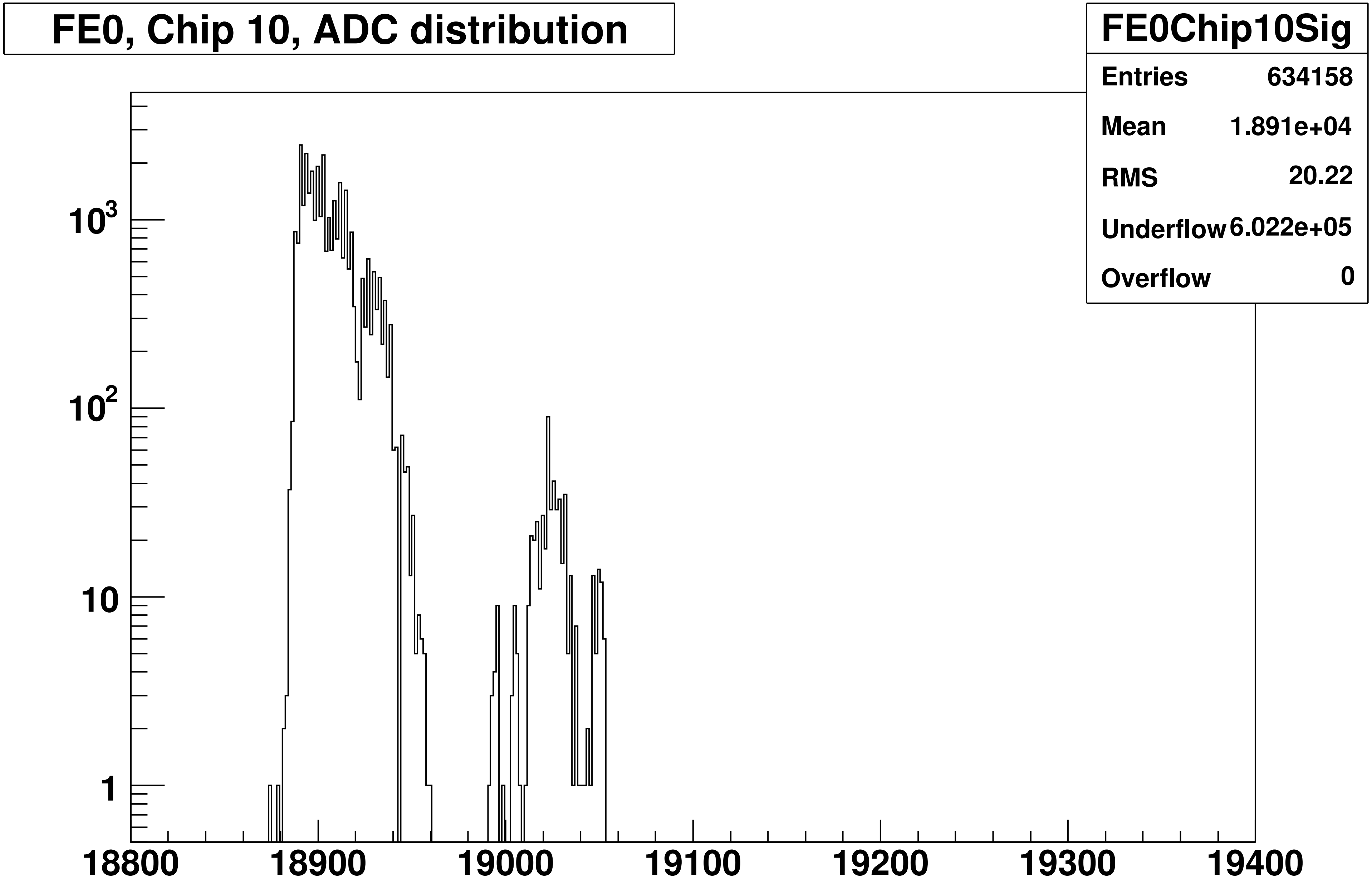
FE0, Chip 10, ADC distribution
FE0Chip10Sig
Entries 634158
Mean 1.891e+04
RMS 20.22
Underflow 6.022e+05
Overflow 0
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10^2
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18900
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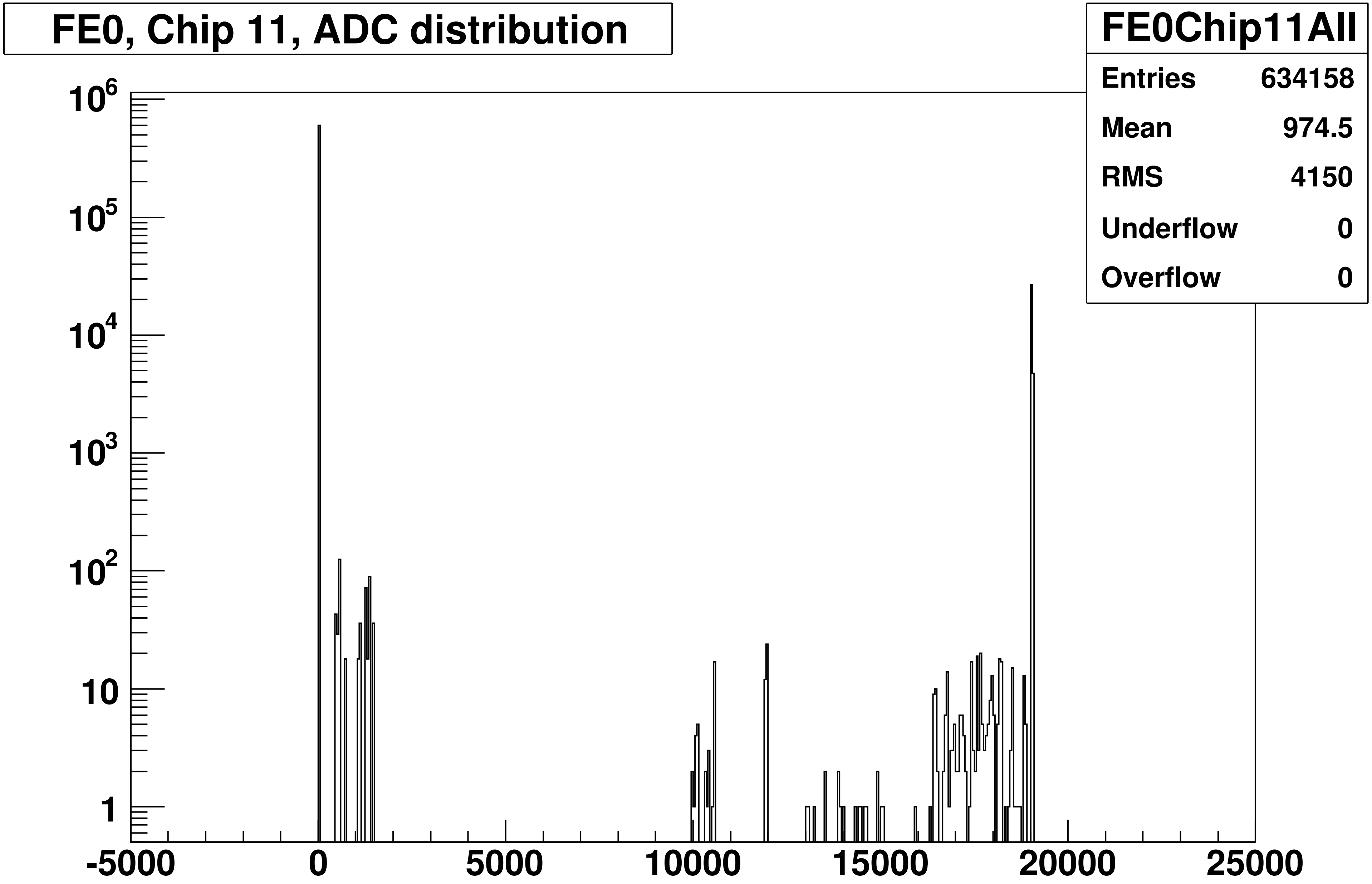
FE0, Chip 11, ADC distribution
FE0Chip11All
Entries 634158
Mean 974.5
RMS 4150
Underflow 0
Overflow 0
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10^3
10^2
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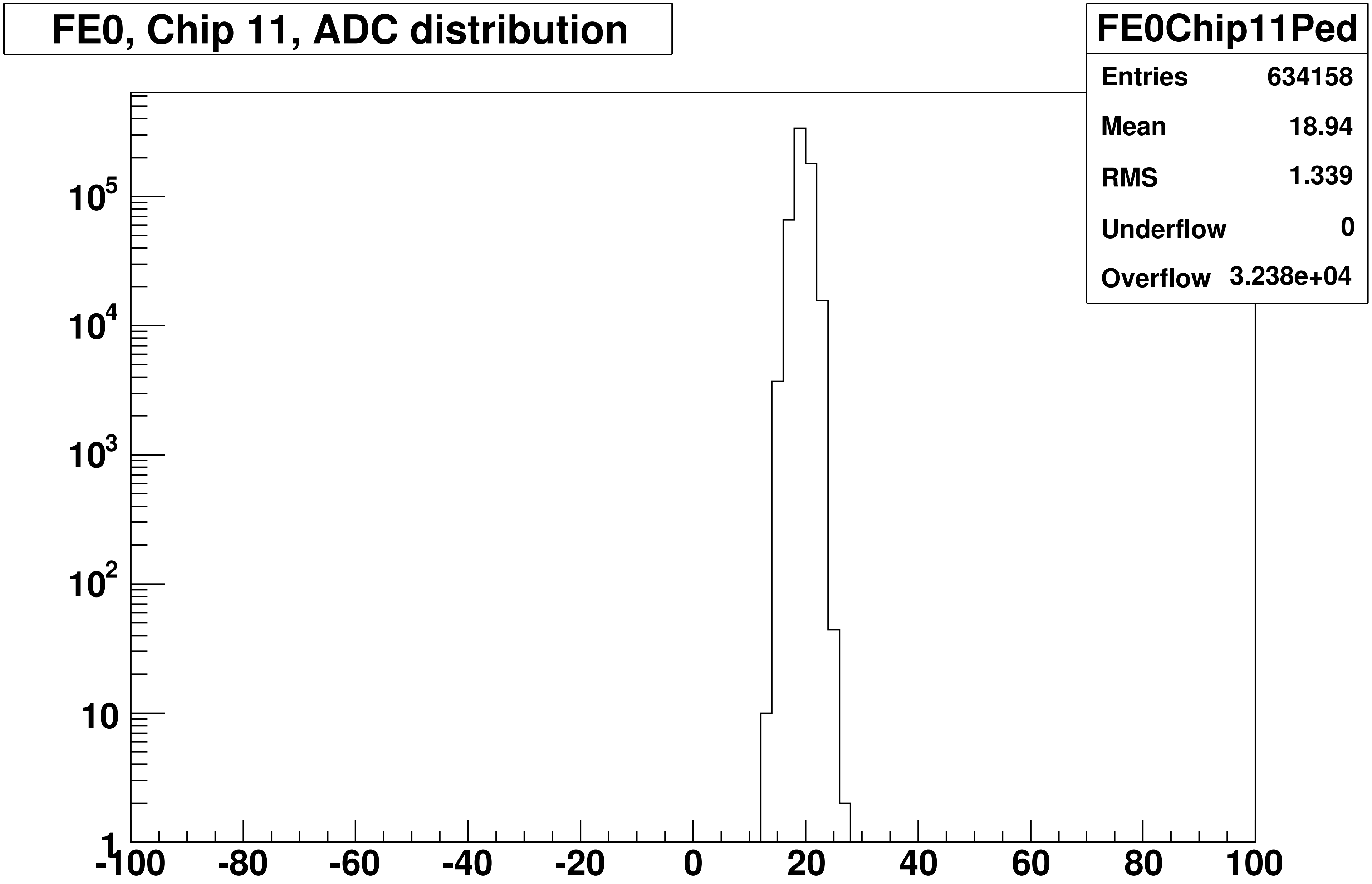
FE0, Chip 11, ADC distribution
FE0Chip11Ped
Entries 634158
Mean 18.94
RMS 1.339
Underflow 0
Overflow 3.238e+04
10^5
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10^3
10^2
10
1
-100
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-20
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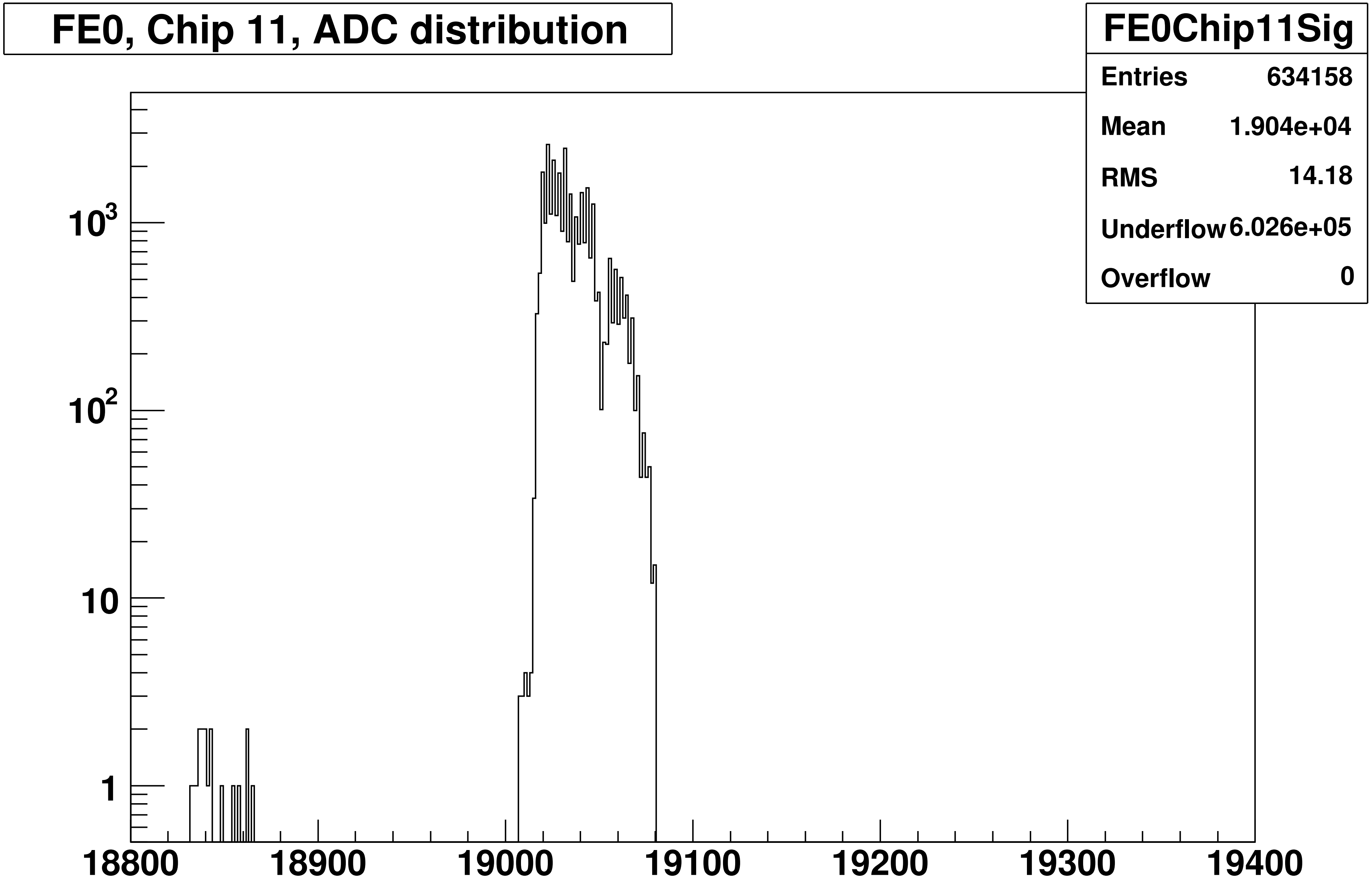
FE0, Chip 11, ADC distribution
FE0Chip11Sig
Entries 634158
Mean 1.904e+04
RMS 14.18
Underflow 6.026e+05
Overflow 0
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10^2
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18900
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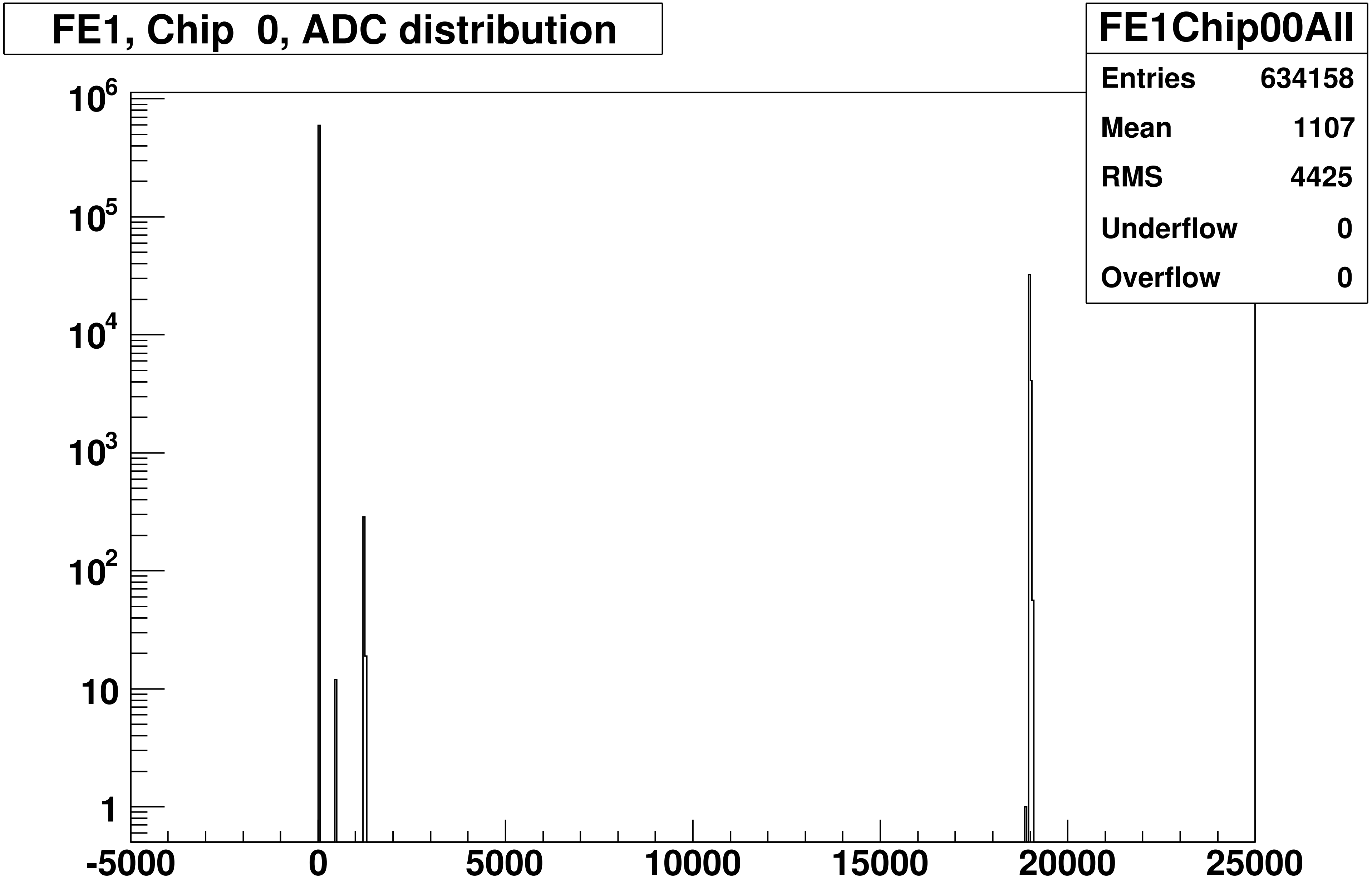

FE1, Chip 0, ADC distribution
FE1Chip00All
Entries 634158
Mean 1107
RMS 4425
Underflow 0
Overflow 0
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10^3
10^2
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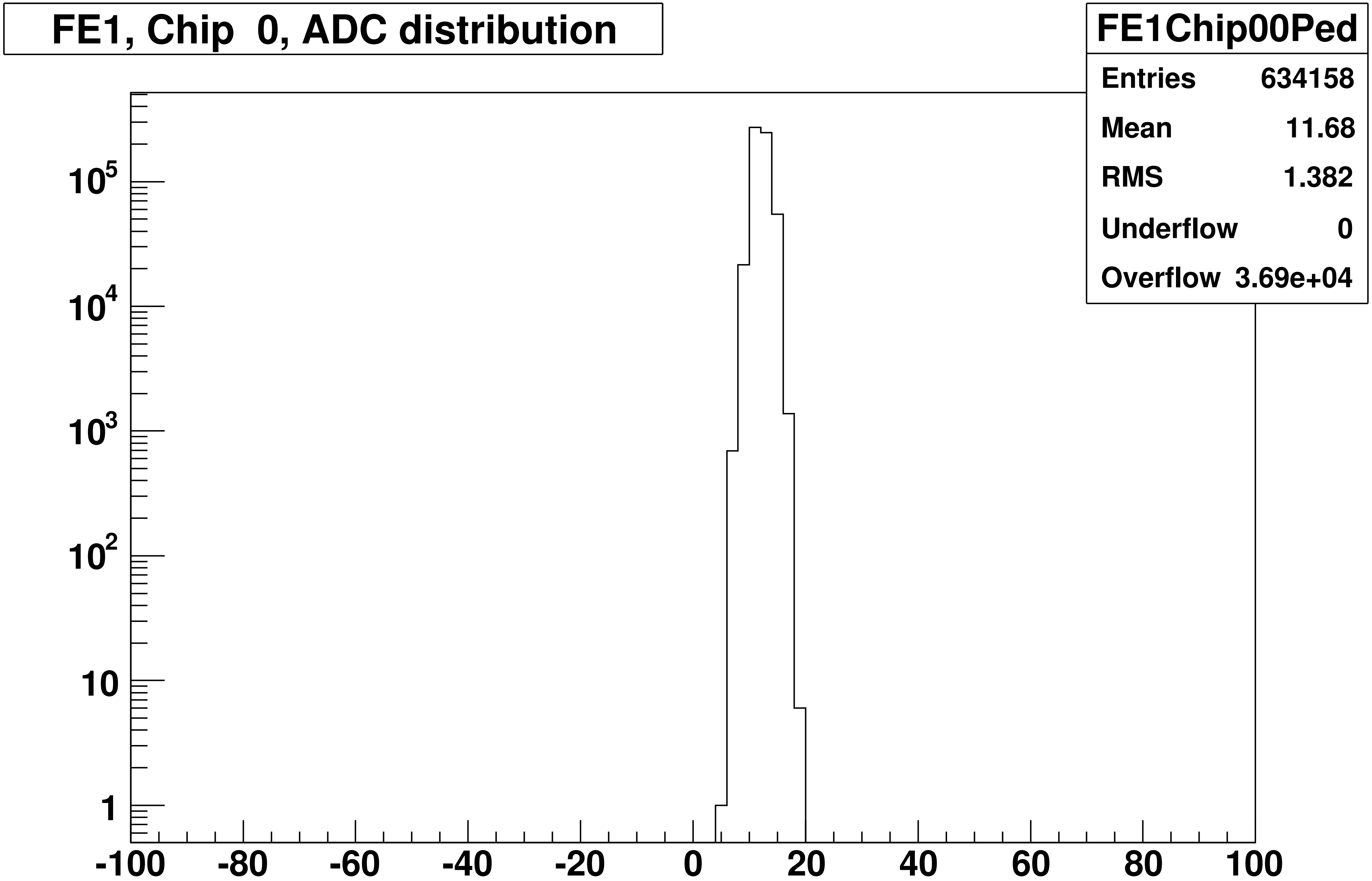

FE1, Chip 0, ADC distribution
FE1Chip00Ped
Entries 634158
Mean 11.68
RMS 1.382
Underflow 0
Overflow 3.69e+04
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10^4
10^3
10^2
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1
-100
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-20
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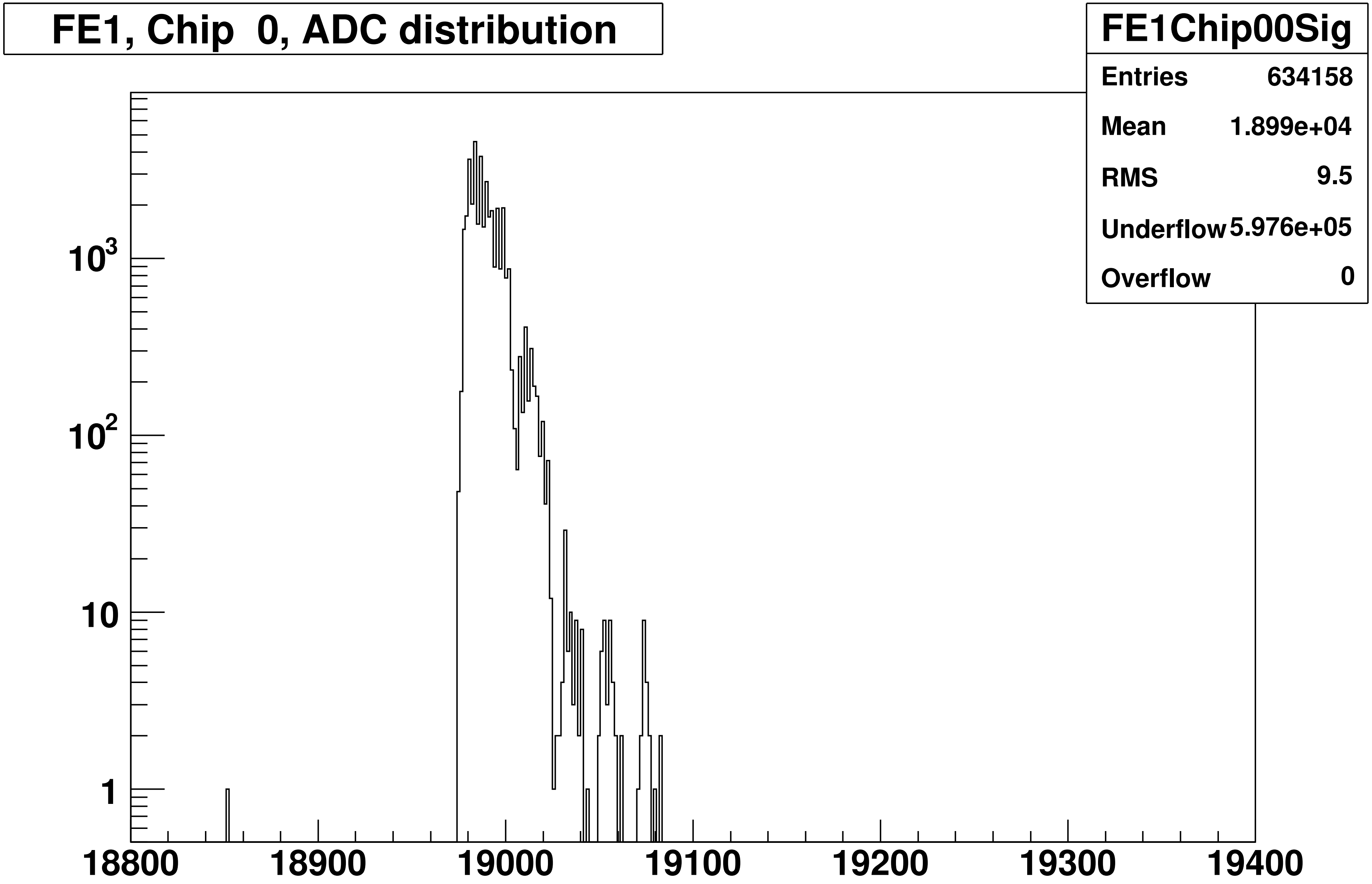
80
100



FE1, Chip 0, ADC distribution
FE1Chip00Sig
Entries 634158
Mean 1.899e+04
RMS 9.5
Underflow 5.976e+05
Overflow 0
10^3
10^2
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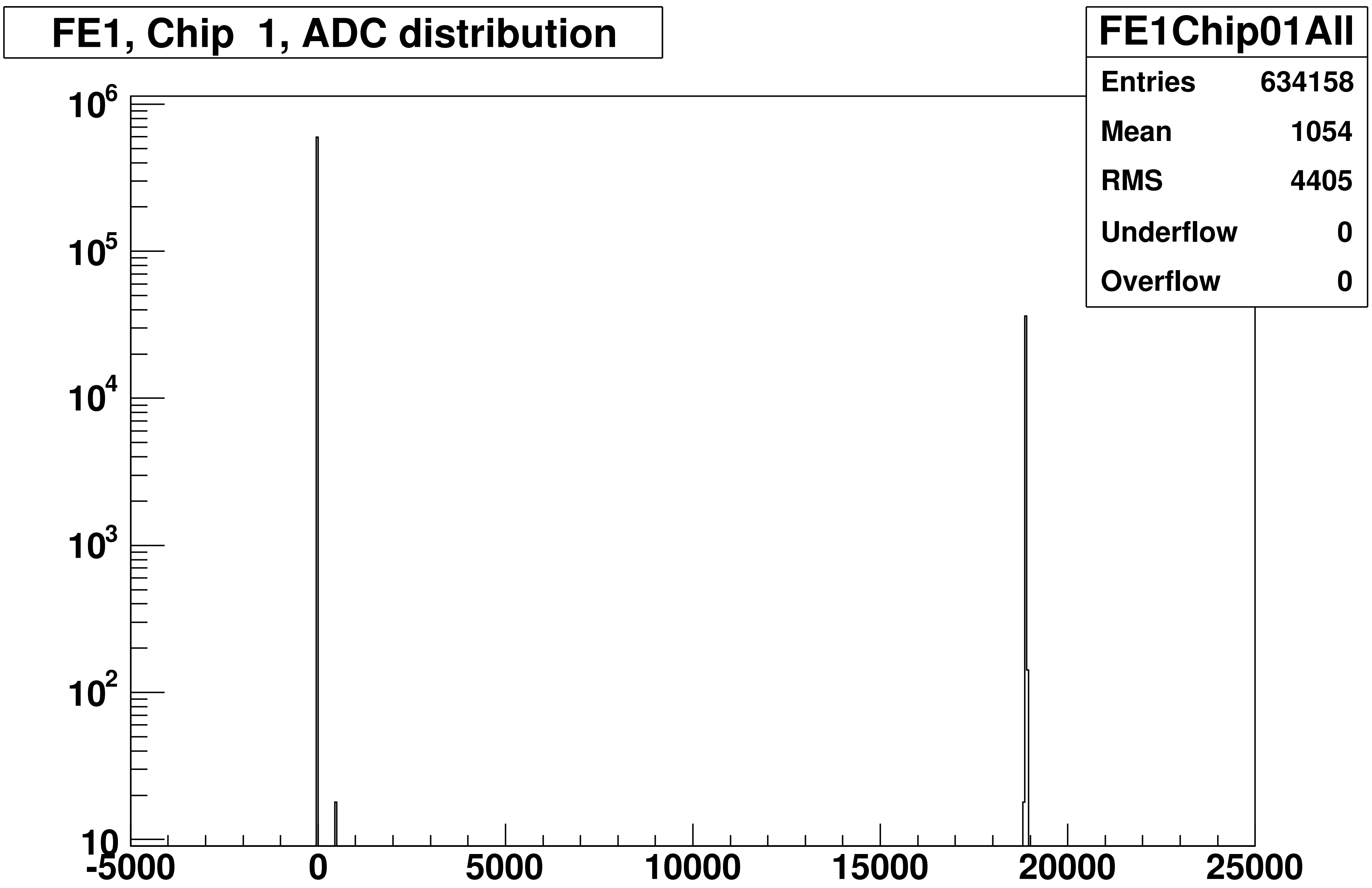
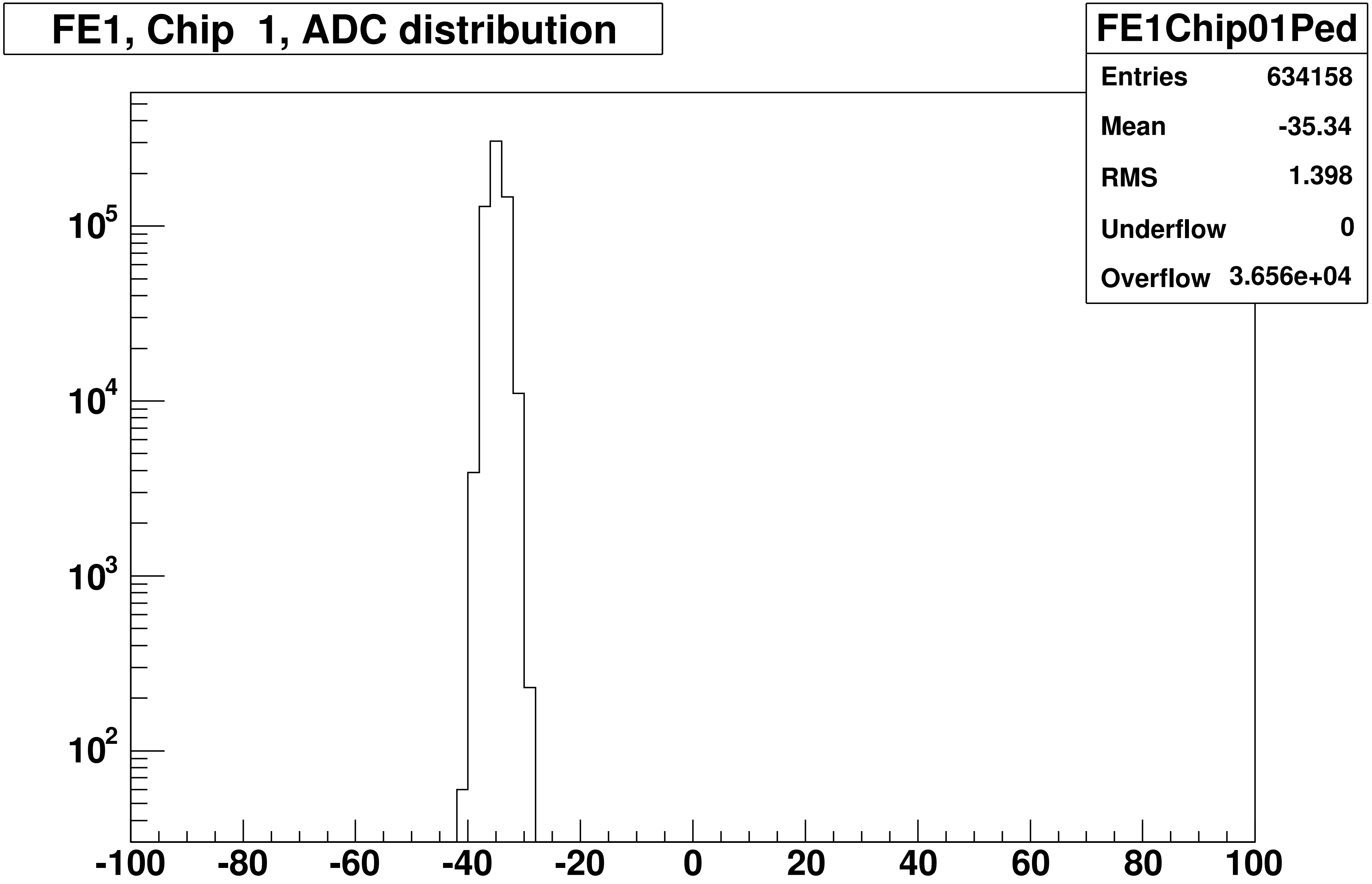

FE1, Chip 1, ADC distribution
FE1Chip01All
Entries 634158
Mean 1054
RMS 4405
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE1, Chip 1, ADC distribution
FE1Chip01Ped
Entries 634158
Mean -35.34
RMS 1.398
Underflow 0
Overflow 3.656e+04
10^5
10^4
10^3
10^2
-100
-80
-60
-40
-20
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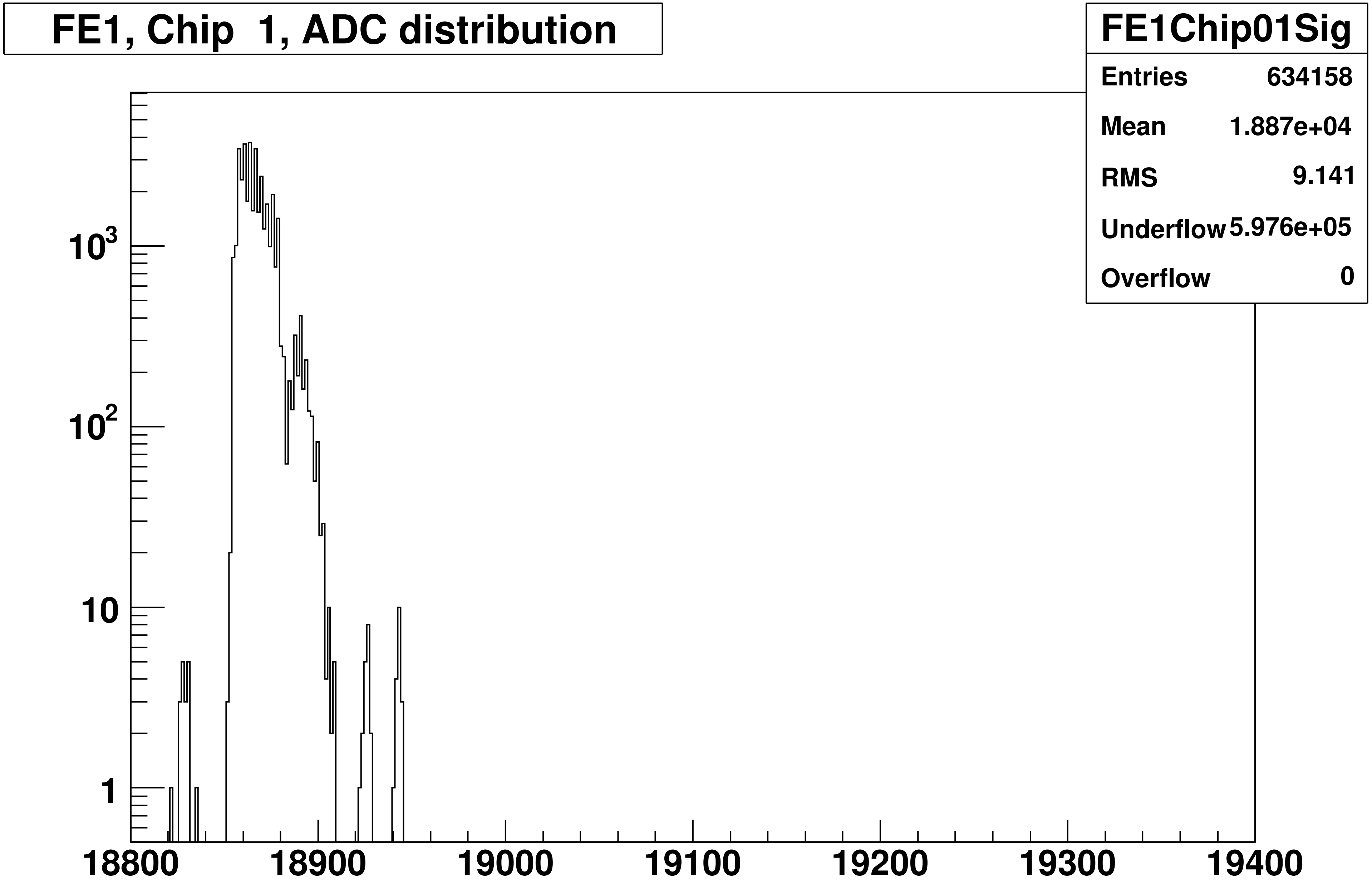
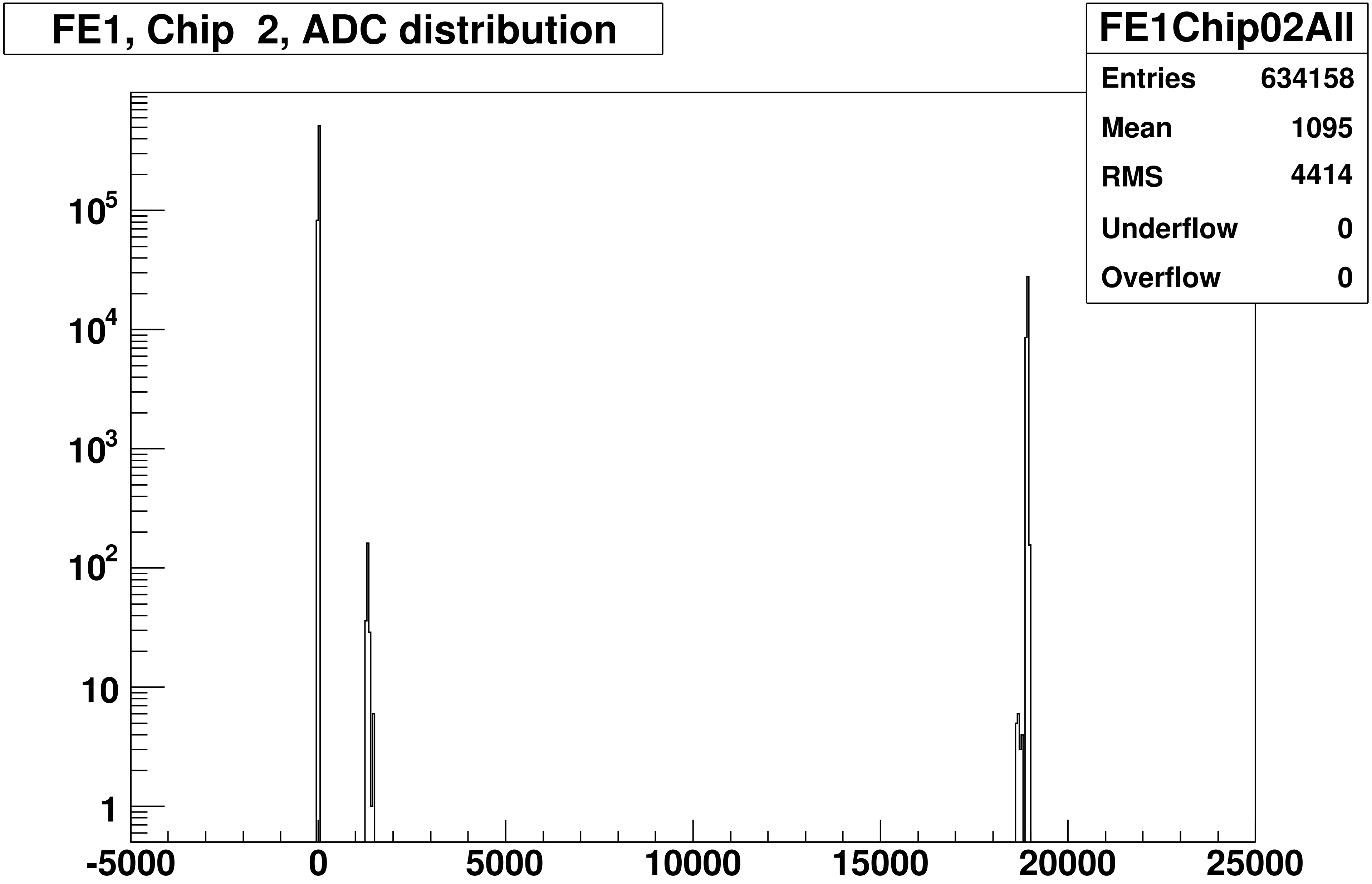
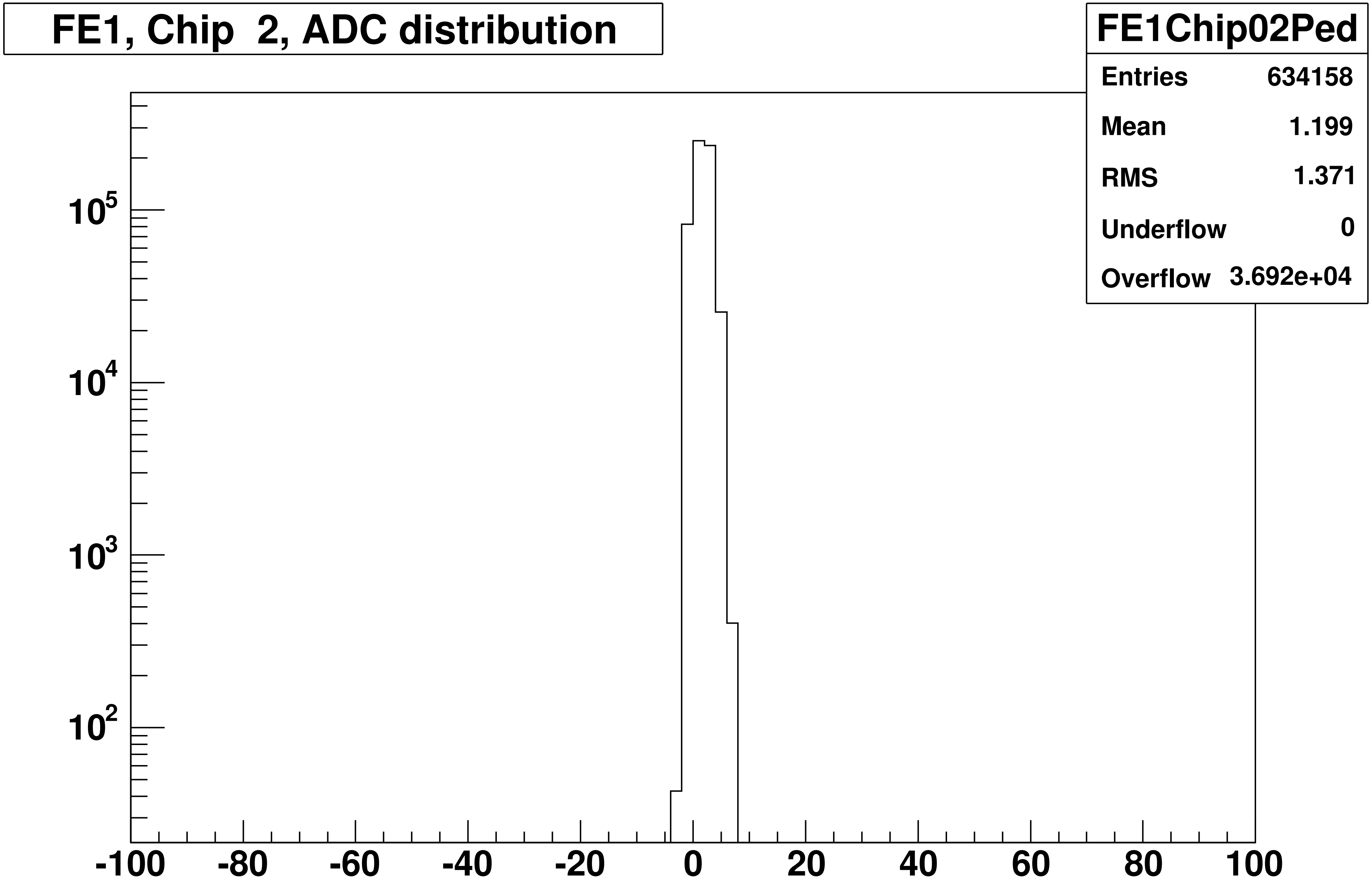
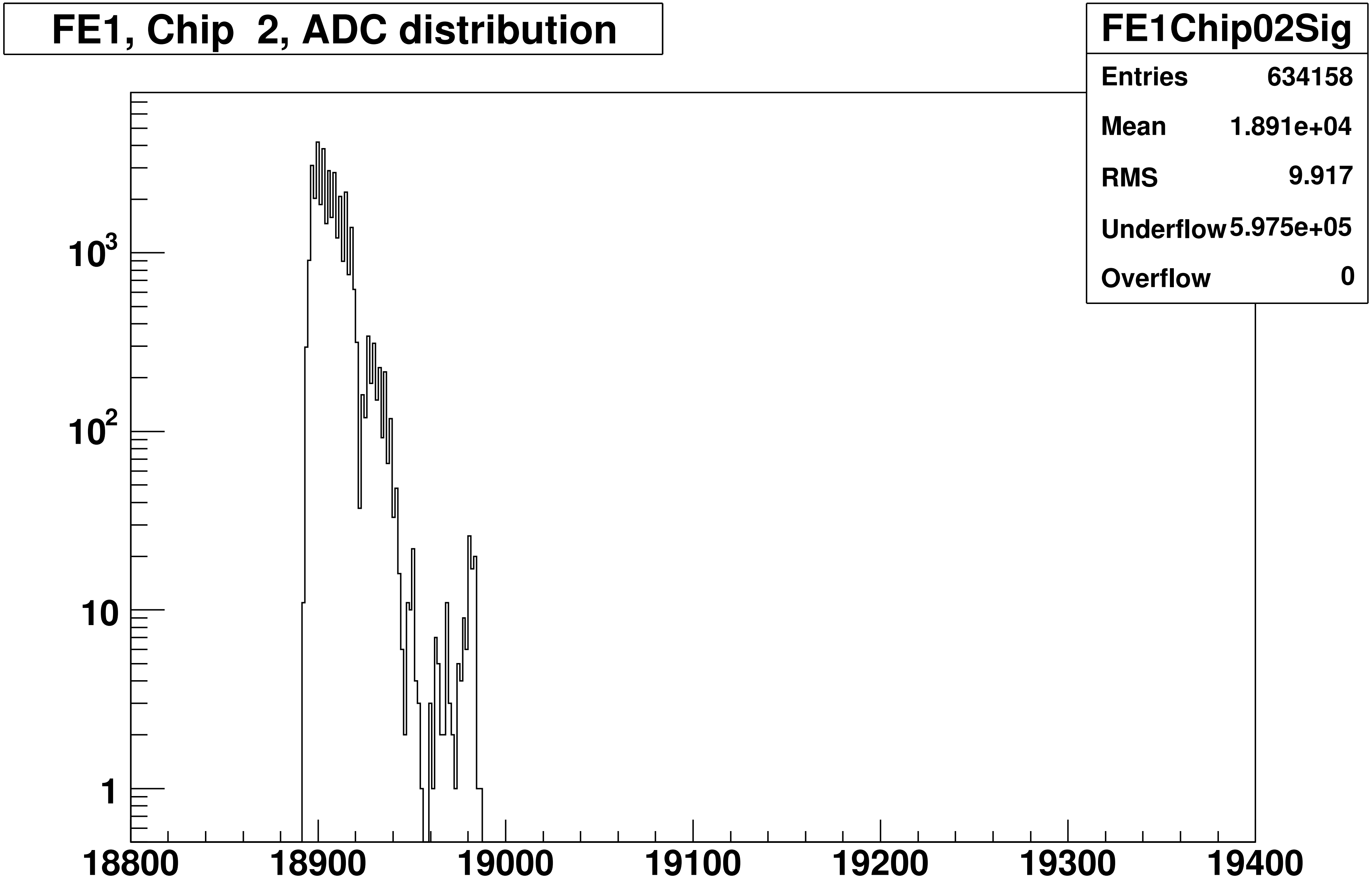
40
60
80
100


FE1, Chip 1, ADC distribution
FE1Chip01Sig
Entries 634158
Mean 1.887e+04
RMS 9.141
Underflow 5.976e+05
Overflow 0
10^3
10^2
10
1
18800
18900
19000
19100
19200
19300
19400


FE1, Chip 2, ADC distribution
FE1Chip02All
Entries 634158
Mean 1095
RMS 4414
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE1, Chip 2, ADC distribution
FE1Chip02Ped
Entries 634158
Mean 1.199
RMS 1.371
Underflow 0
Overflow 3.692e+04
10^5
10^4
10^3
10^2
-100 -80 -60 -40 -20 0 20 40 60 80 100


FE1, Chip 2, ADC distribution
FE1Chip02Sig
Entries 634158
Mean 1.891e+04
RMS 9.917
Underflow 5.975e+05
Overflow 0
10^3
10^2
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18900
19000
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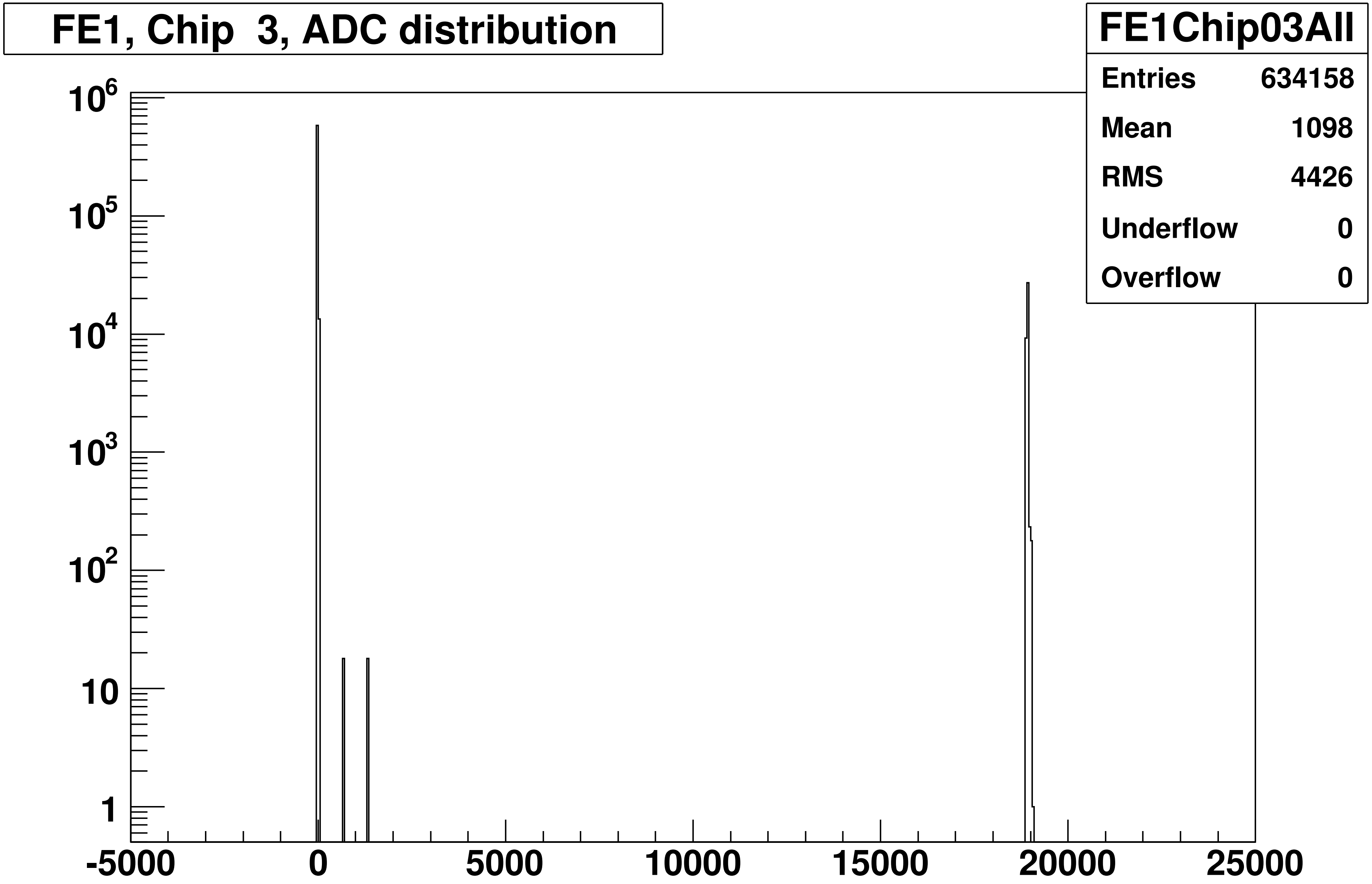
19300
19400



FE1, Chip 3, ADC distribution
FE1Chip03All
Entries 634158
Mean 1098
RMS 4426
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
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10000
15000
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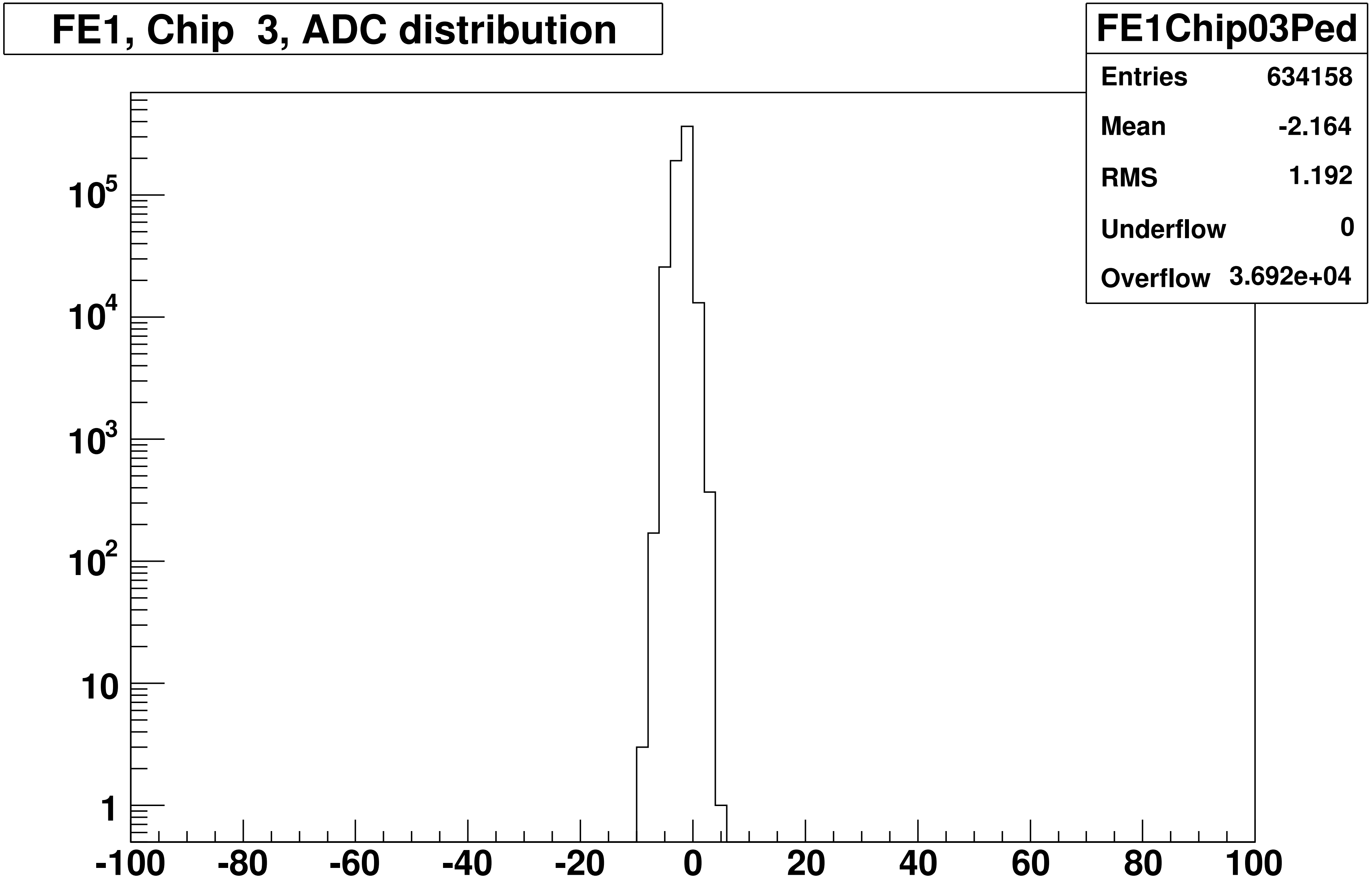
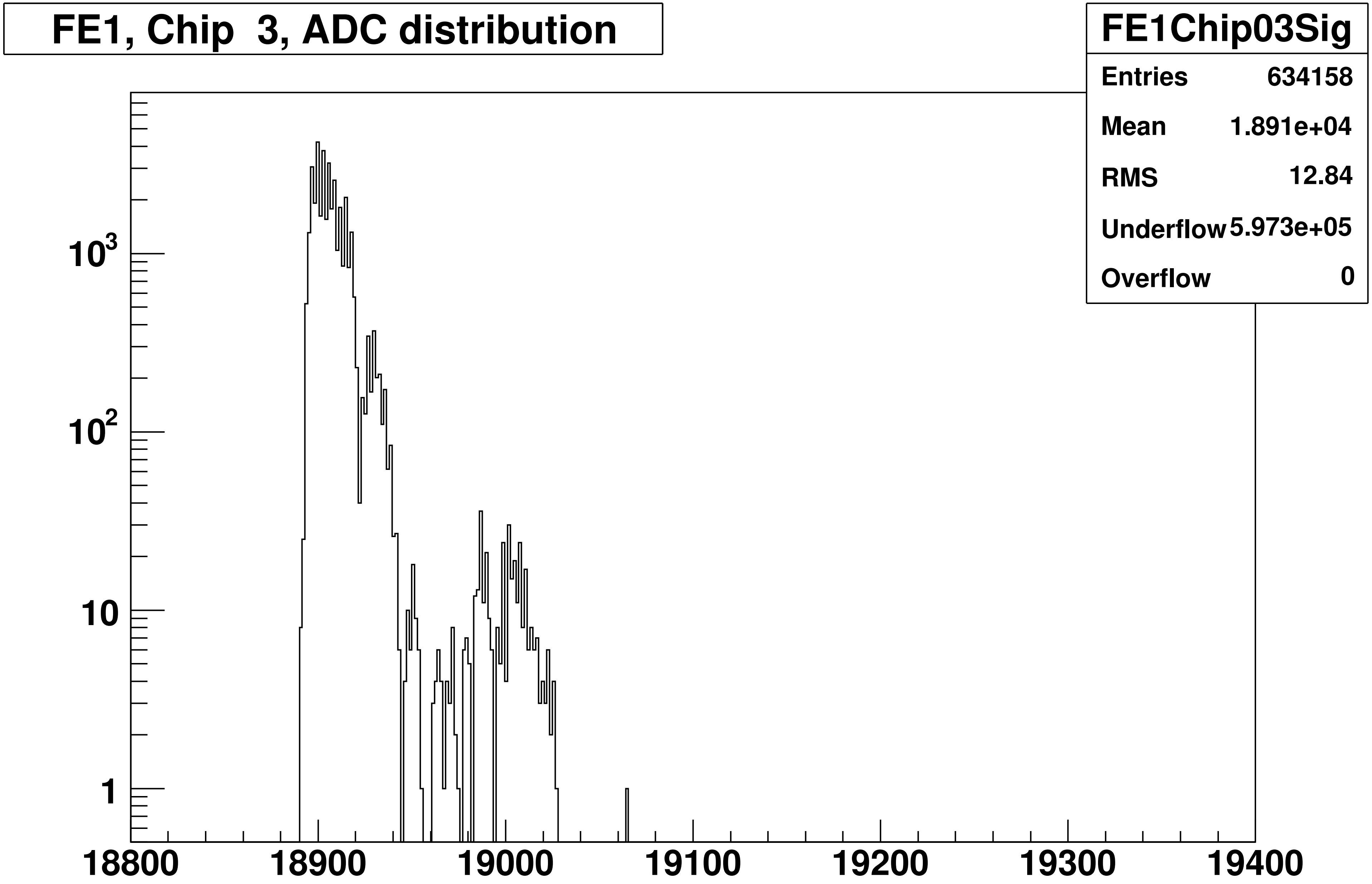
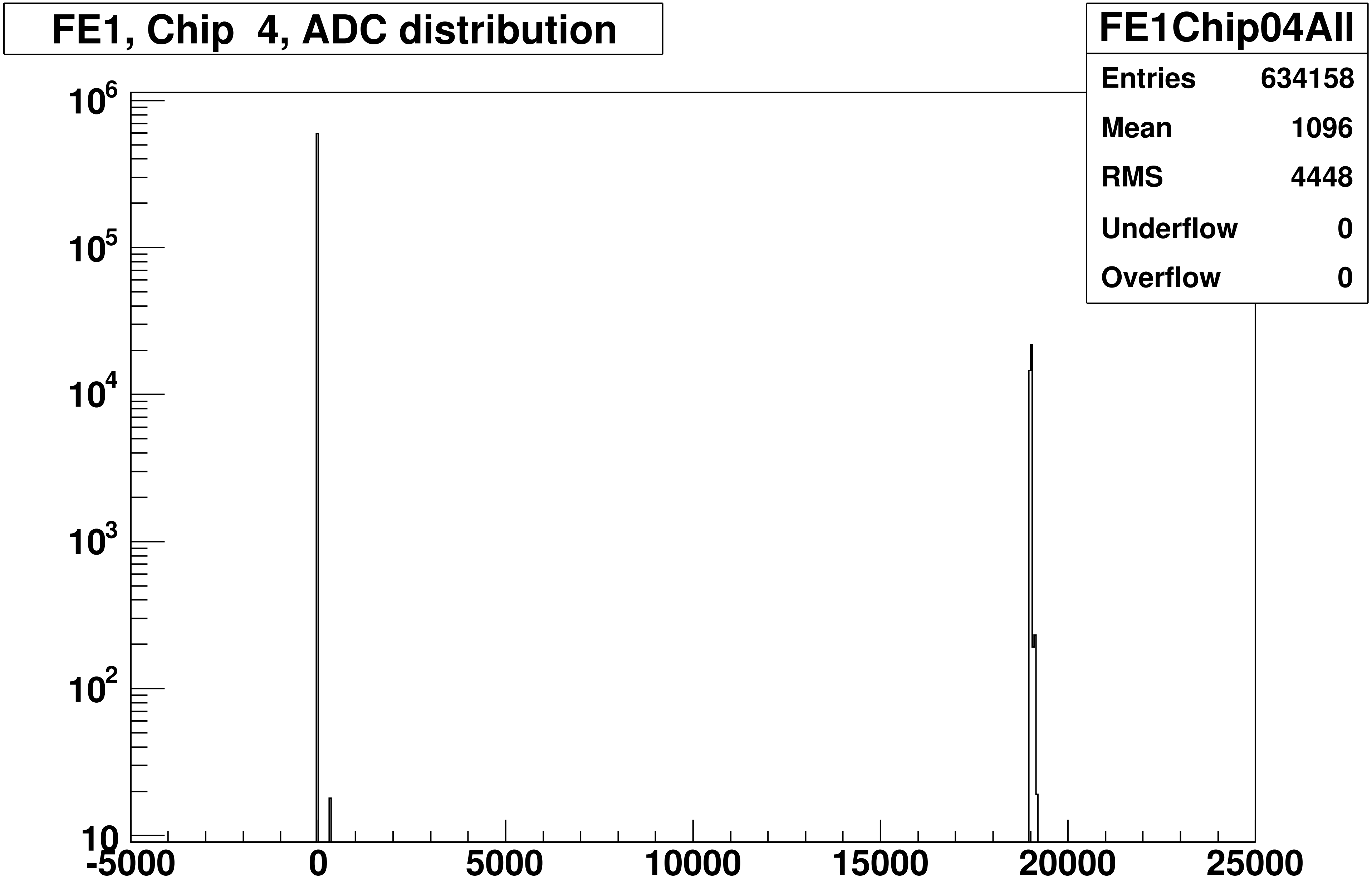
25000

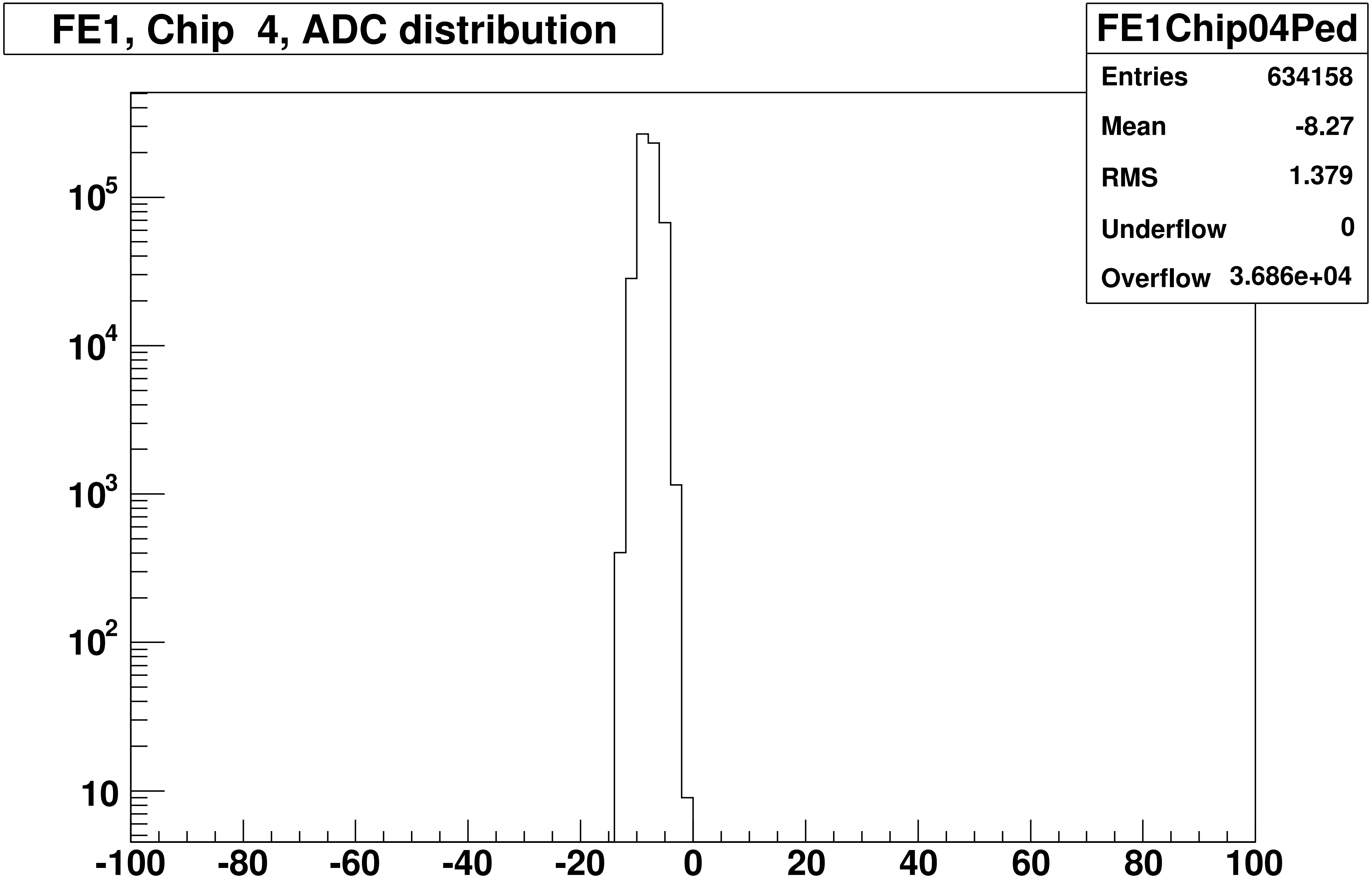

FE1, Chip 3, ADC distribution
FE1Chip03Ped
Entries 634158
Mean -2.164
RMS 1.192
Underflow 0
Overflow 3.692e+04
1
10
10^2
10^3
10^4
10^5
-100
-80
-60
-40
-20
0
20
40
60
80
100

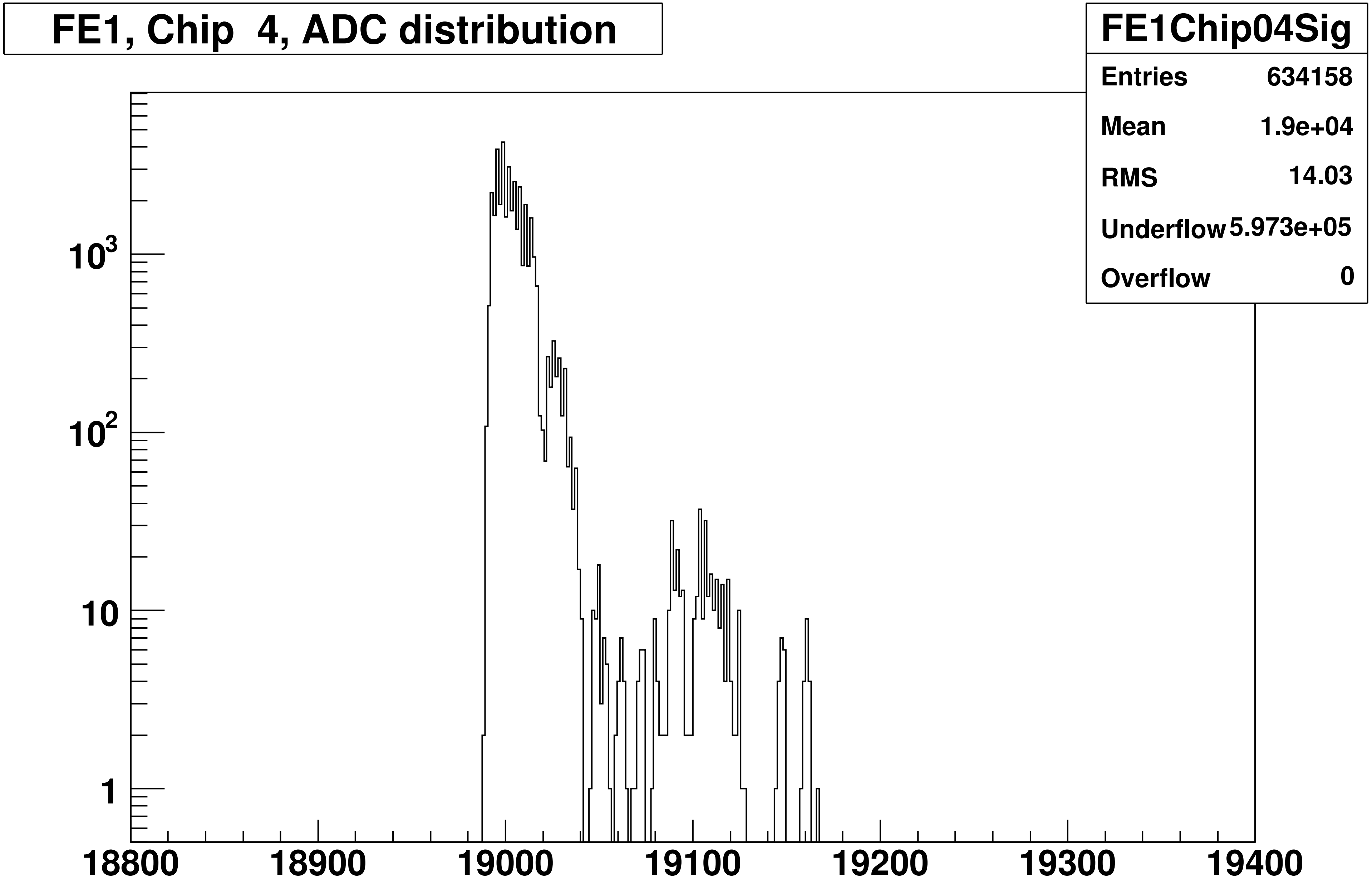


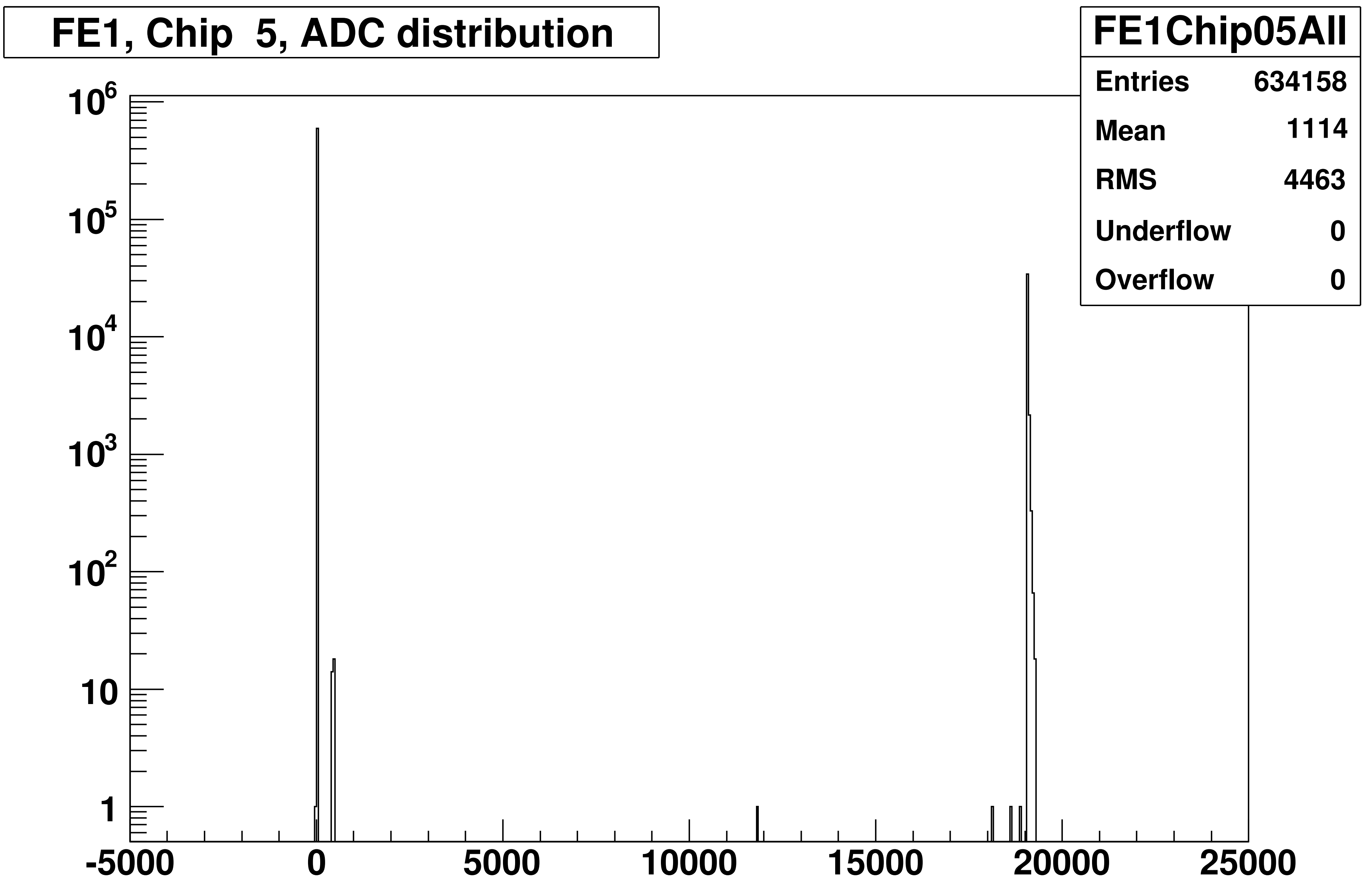
FE1, Chip 3, ADC distribution
FE1Chip03Sig
Entries 634158
Mean 1.891e+04
RMS 12.84
Underflow 5.973e+05
Overflow 0
10^3
10^2
10
1
18800
18900
19000
19100
19200
19300
19400



FE1, Chip 4, ADC distribution
FE1Chip04All
Entries 634158
Mean 1096
RMS 4448
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE1, Chip 4, ADC distribution
FE1Chip04Ped
Entries 634158
Mean -8.27
RMS 1.379
Underflow 0
Overflow 3.686e+04
10
10^2
10^3
10^4
10^5
-100
-80
-60
-40
-20
0
20
40
60
80
100


FE1, Chip 4, ADC distribution
FE1Chip04Sig
Entries 634158
Mean 1.9e+04
RMS 14.03
Underflow 5.973e+05
Overflow 0
10^3
10^2
10
1
18800
18900
19000
19100
19200
19300
19400


FE1, Chip 5, ADC distribution
FE1Chip05All
Entries 634158
Mean 1114
RMS 4463
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
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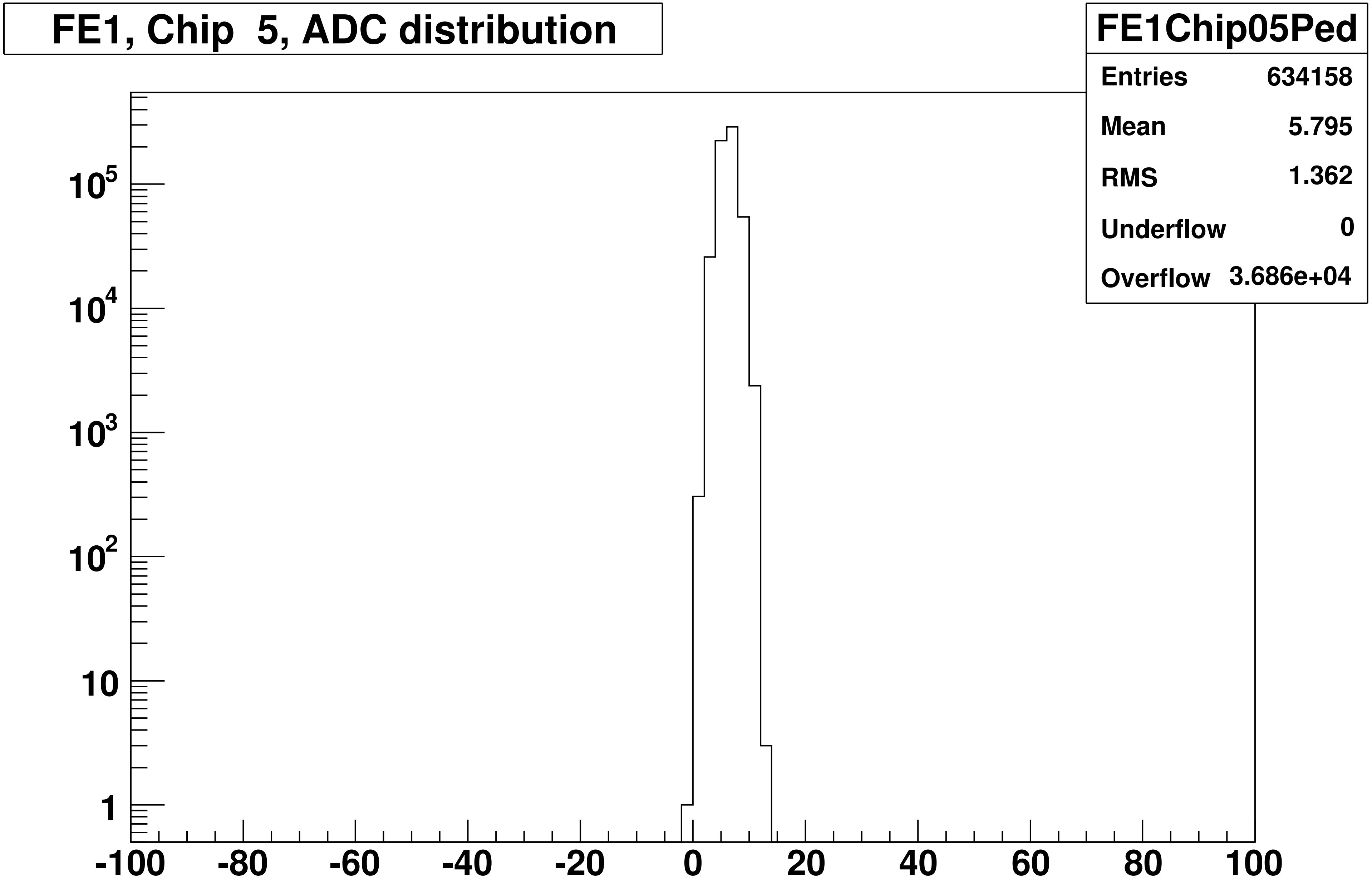
10000
15000
20000
25000


FE1, Chip 5, ADC distribution
FE1Chip05Ped
Entries 634158
Mean 5.795
RMS 1.362
Underflow 0
Overflow 3.686e+04
10^5
10^4
10^3
10^2
10
1
-100
-80
-60
-40
-20
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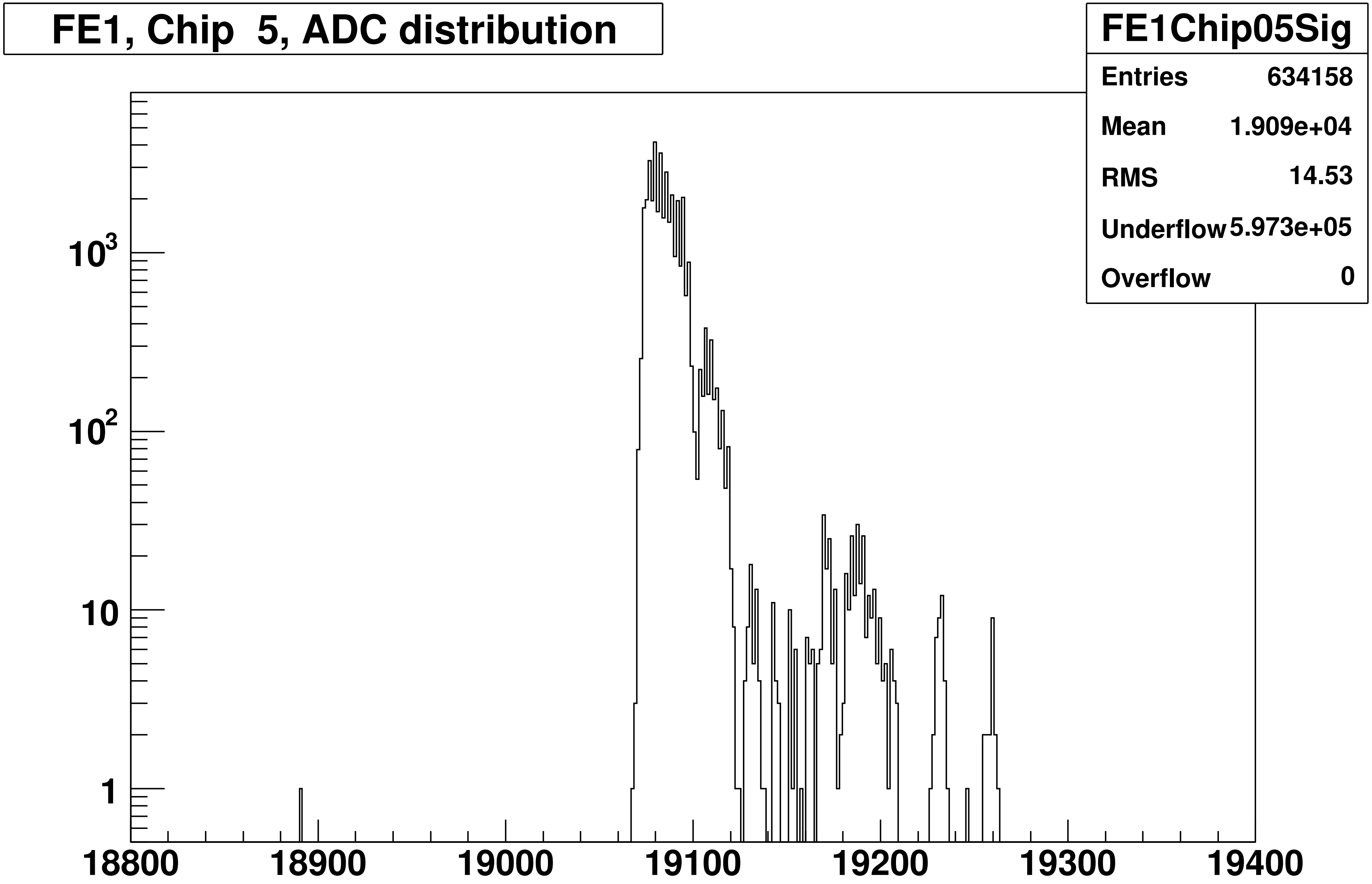
40
60
80
100



FE1, Chip 5, ADC distribution
FE1Chip05Sig
Entries 634158
Mean 1.909e+04
RMS 14.53
Underflow 5.973e+05
Overflow 0
10^3
10^2
10
1
18800
18900
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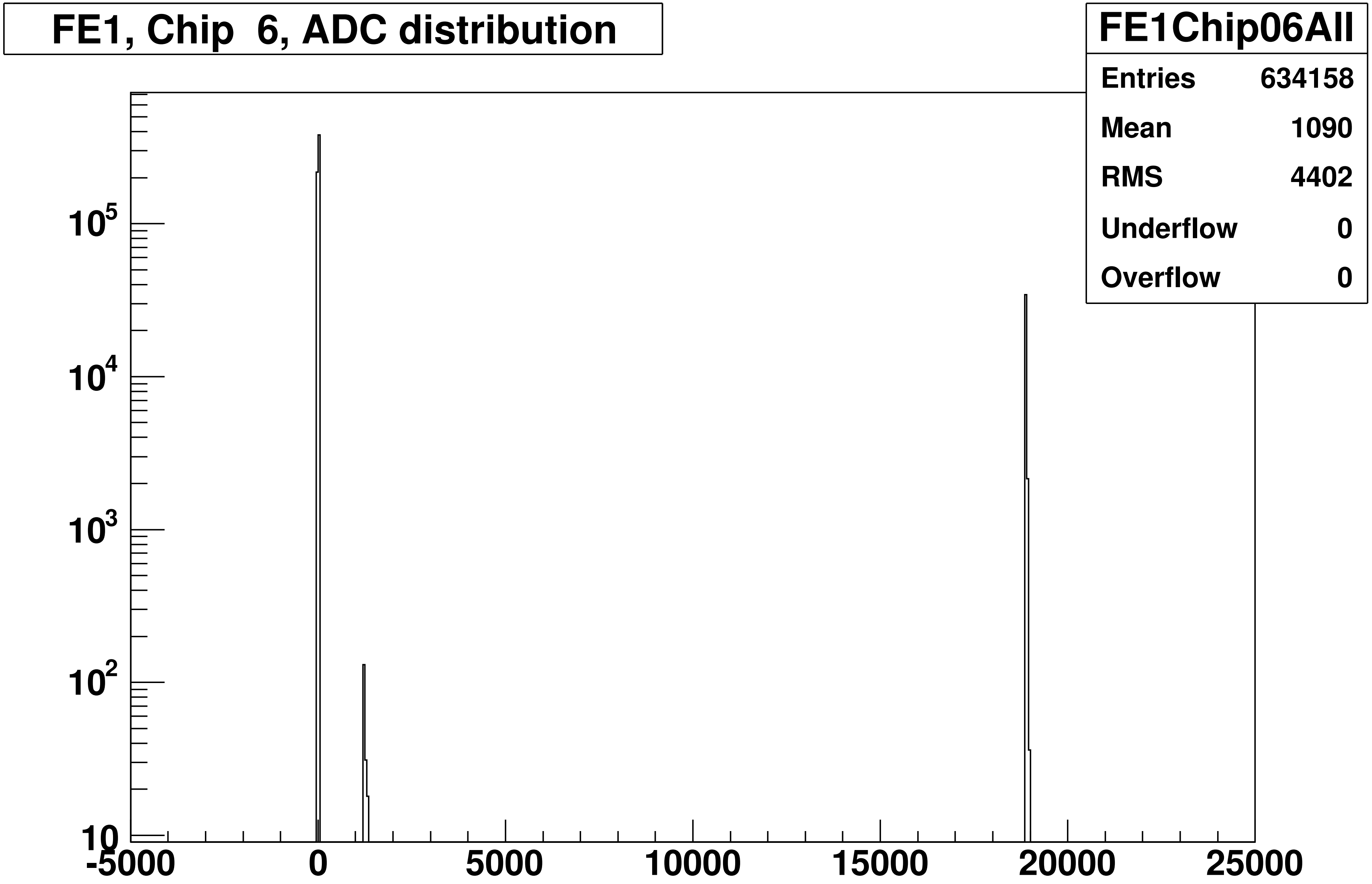
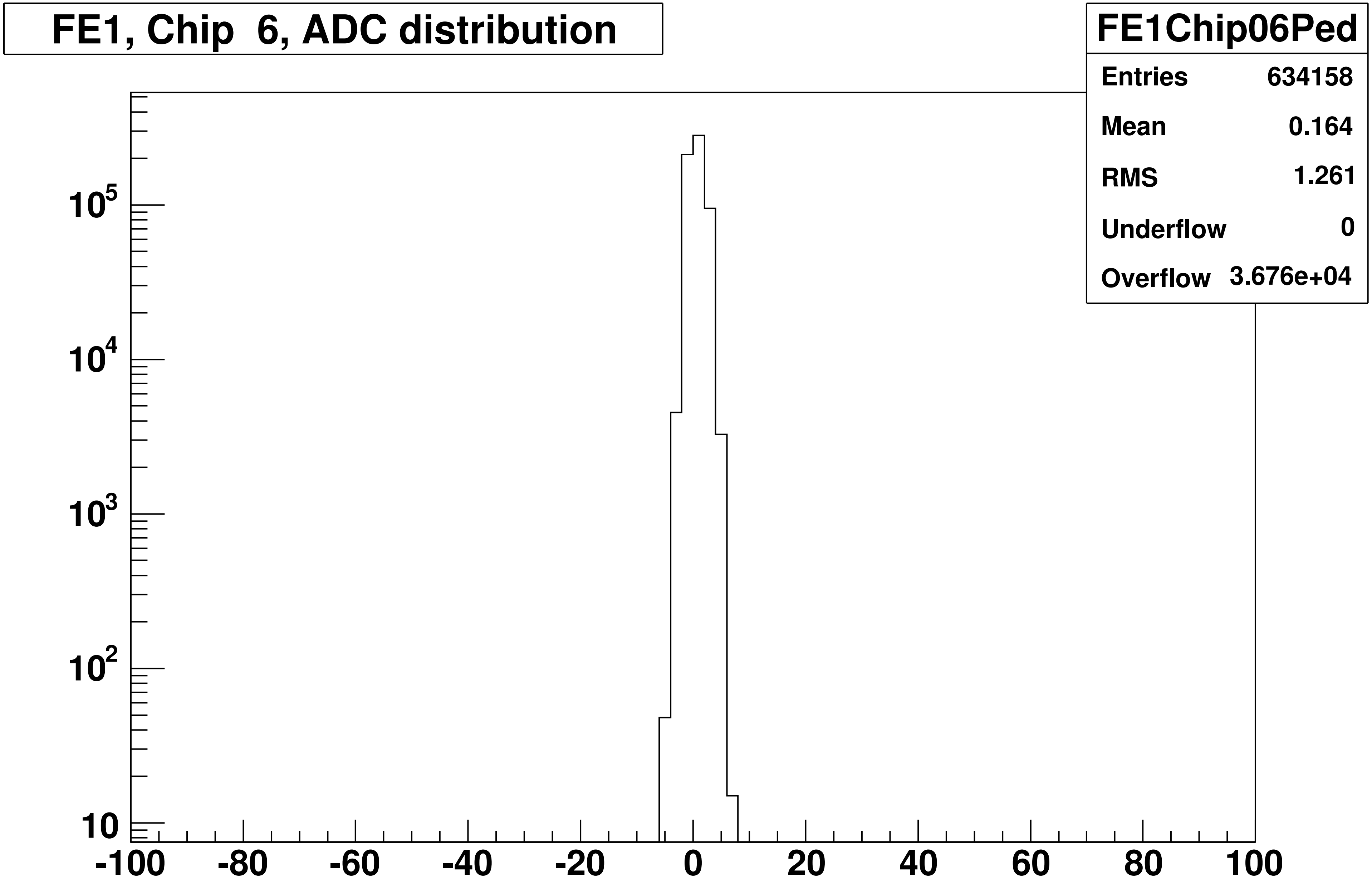
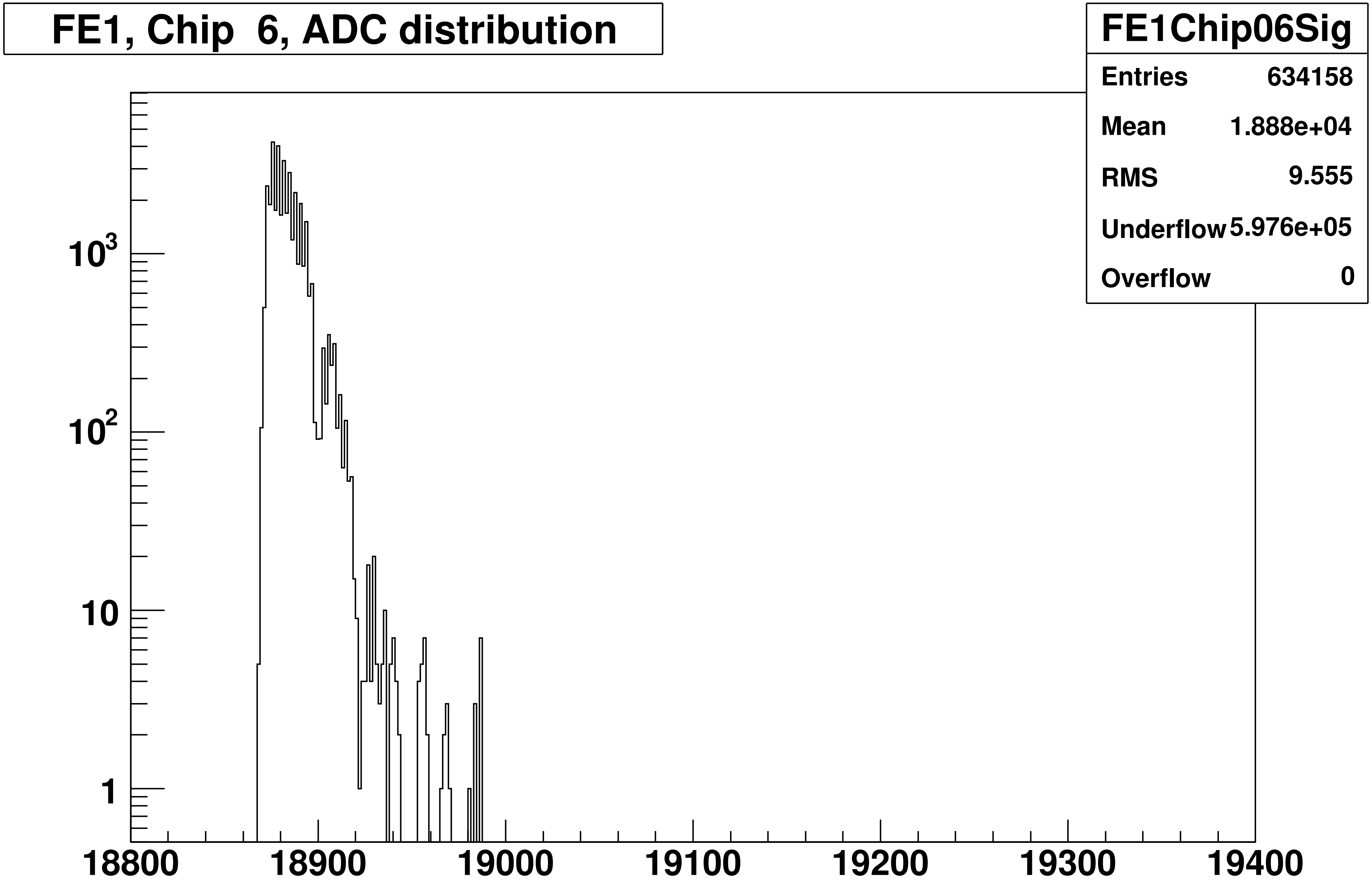
19100
19200
19300
19400

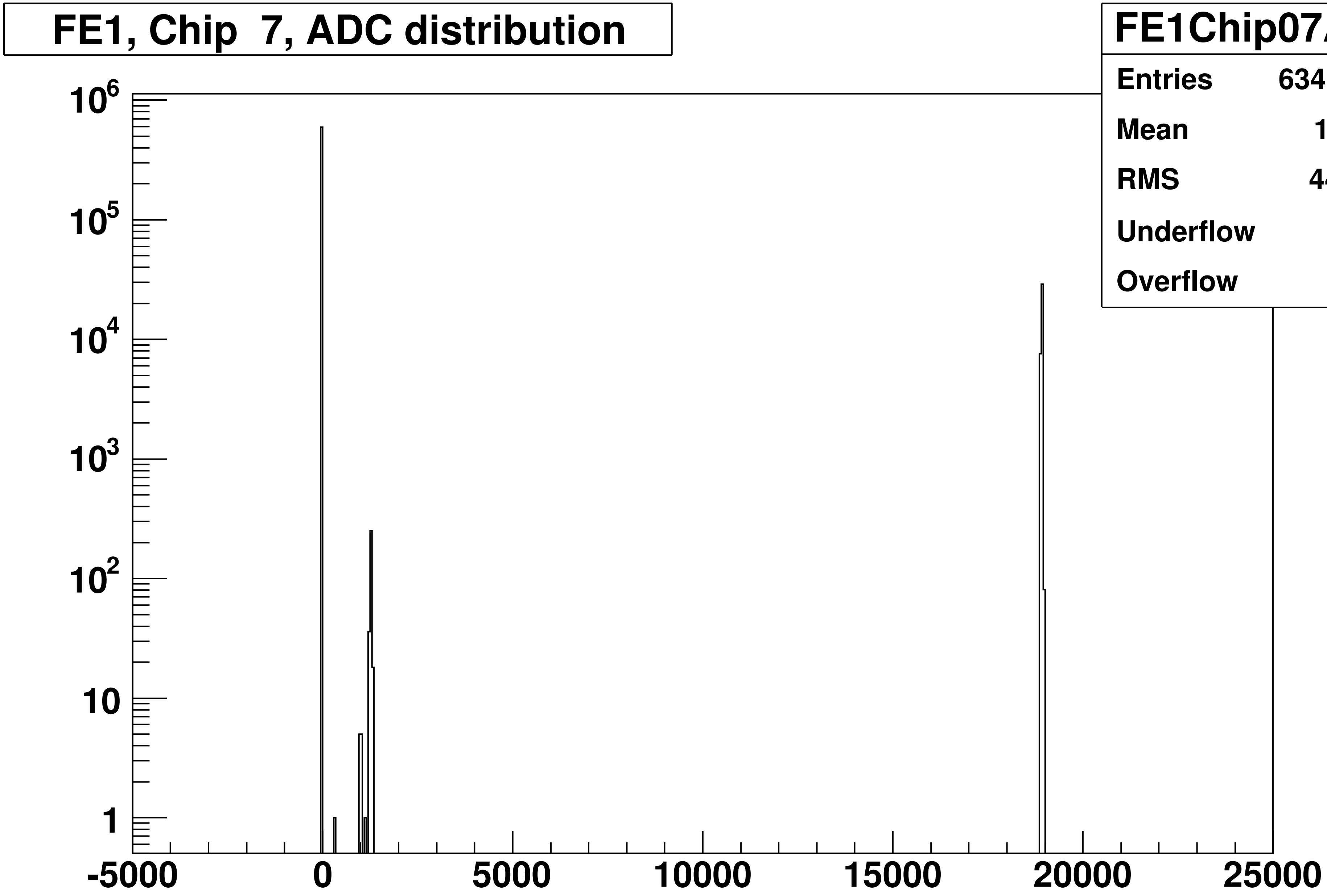

FE1, Chip 6, ADC distribution
FE1Chip06All
Entries 634158
Mean 1090
RMS 4402
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000

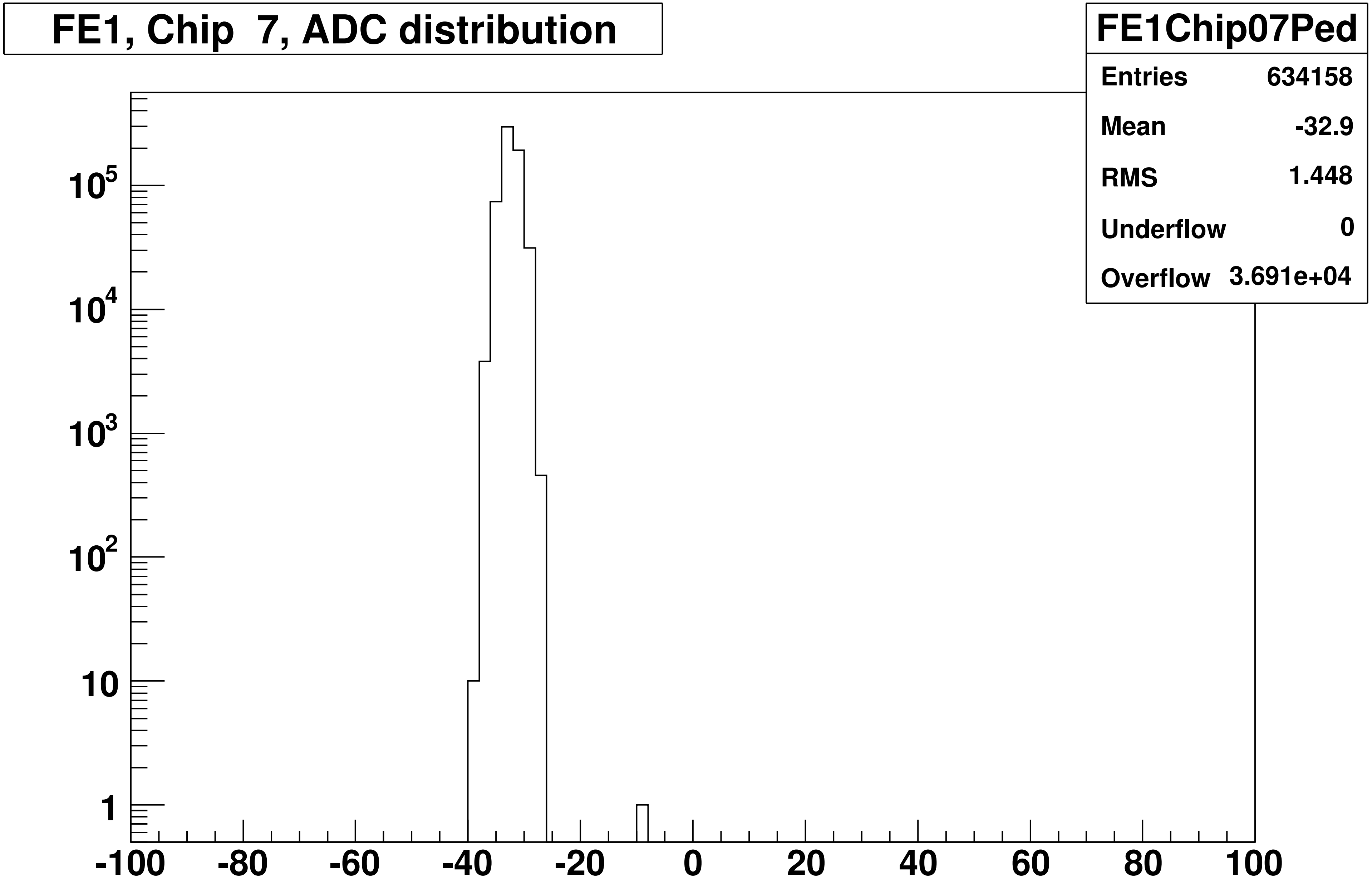


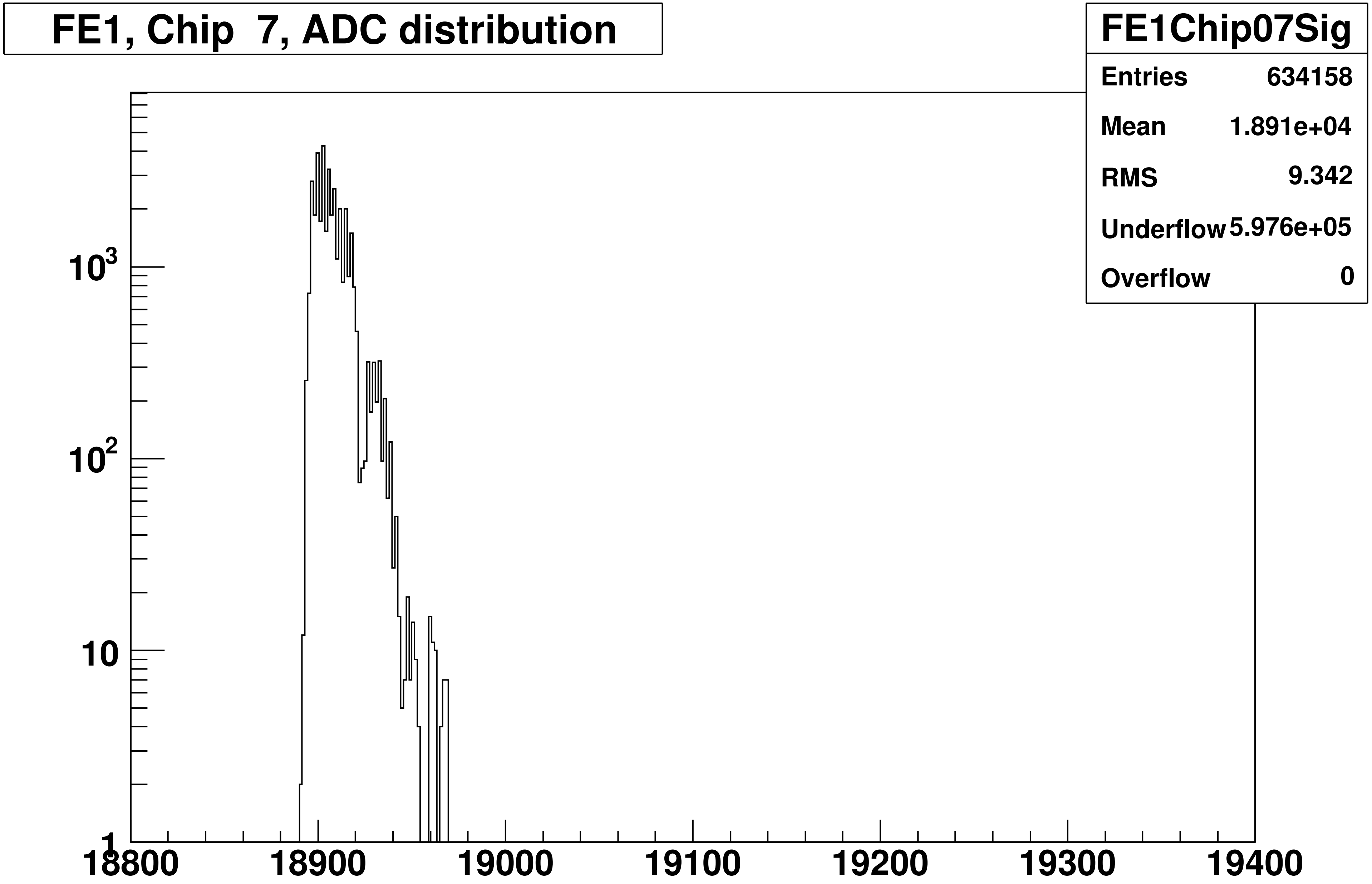
FE1, Chip 6, ADC distribution
FE1Chip06Ped
Entries 634158
Mean 0.164
RMS 1.261
Underflow 0
Overflow 3.676e+04
10^5
10^4
10^3
10^2
10
-100
-80
-60
-40
-20
0
20
40
60
80
100



FE1, Chip 6, ADC distribution
FE1Chip06Sig
Entries 634158
Mean 1.888e+04
RMS 9.555
Underflow 5.976e+05
Overflow 0
10^3
10^2
10
1
18800
18900
19000
19100
19200
19300
19400


FE1, Chip 7, ADC distribution
FE1Chip07All
Entries 634158
Mean 1061
RMS 4416
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE1, Chip 7, ADC distribution
FE1Chip07Ped
Entries 634158
Mean -32.9
RMS 1.448
Underflow 0
Overflow 3.691e+04
10^5
10^4
10^3
10^2
10
1
-100
-80
-60
-40
-20
0
20
40
60
80
100


FE1, Chip 7, ADC distribution
FE1Chip07Sig
Entries 634158
Mean 1.891e+04
RMS 9.342
Underflow 5.976e+05
Overflow 0
1
10
10^2
10^3
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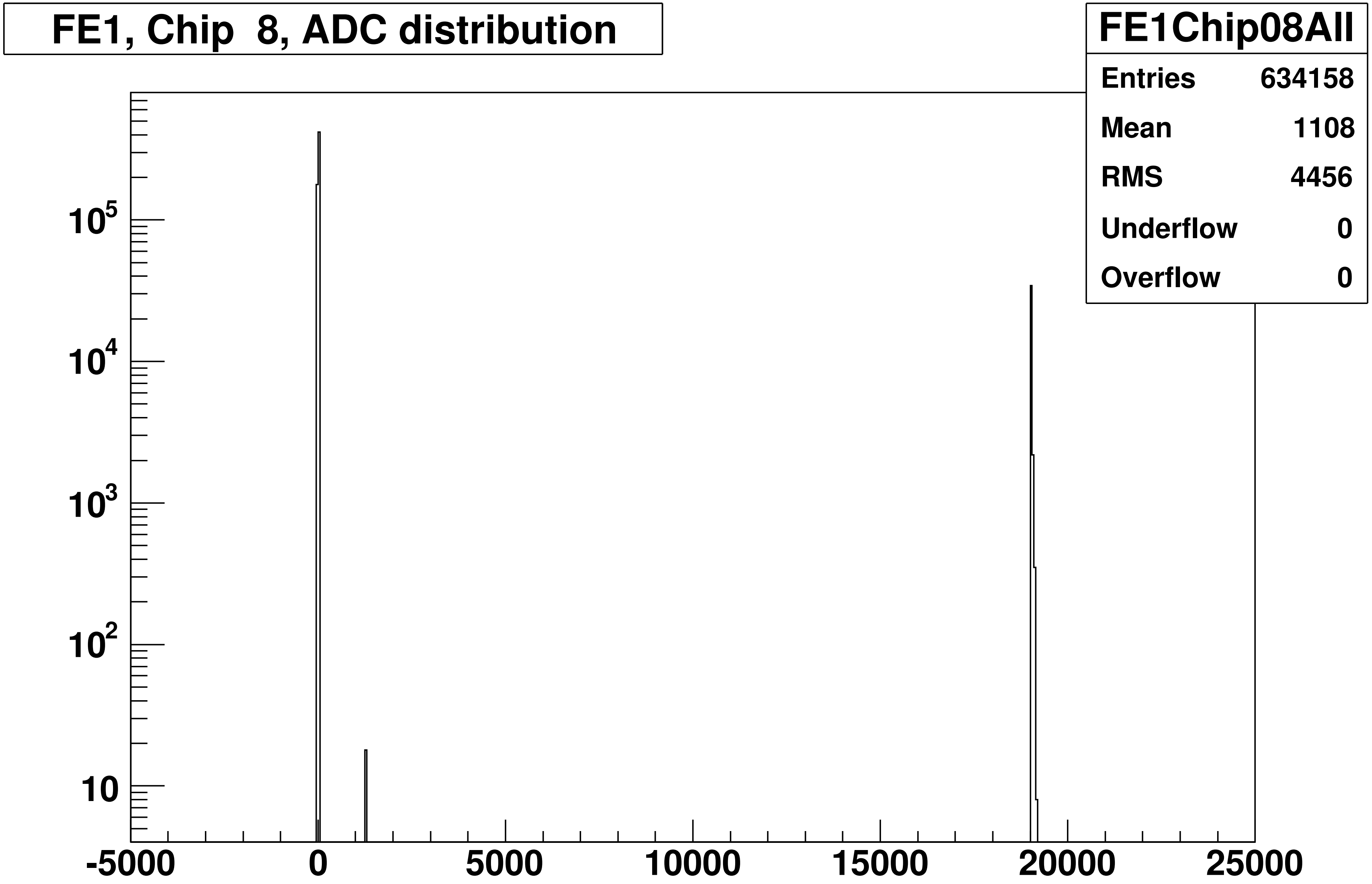
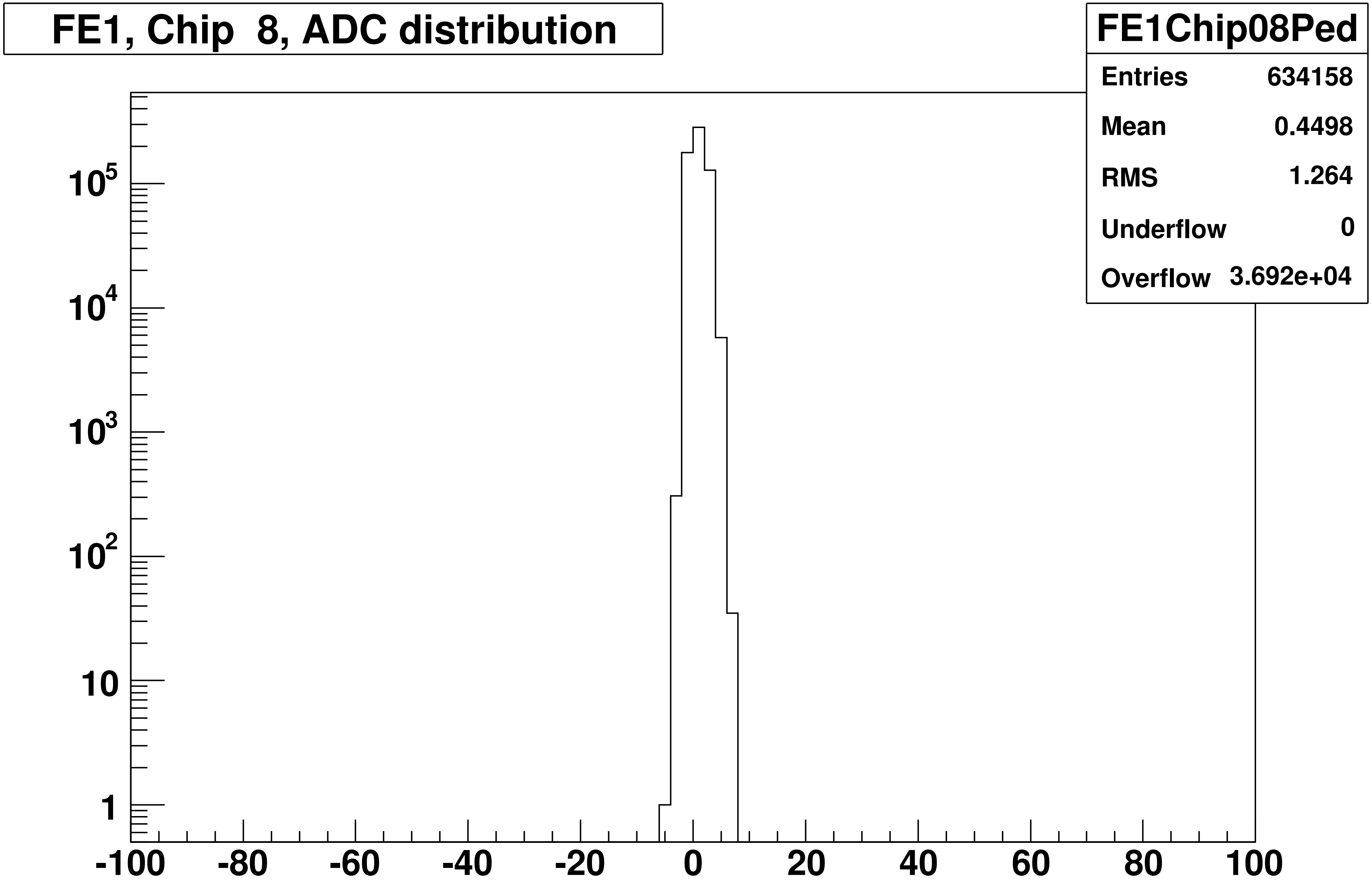
19100
19200
19300
19400



FE1, Chip 8, ADC distribution
FE1Chip08All
Entries 634158
Mean 1108
RMS 4456
Underflow 0
Overflow 0
10
10^2
10^3
10^4
10^5
-5000
0
5000
10000
15000
20000
25000


FE1, Chip 8, ADC distribution
FE1Chip08Ped
Entries 634158
Mean 0.4498
RMS 1.264
Underflow 0
Overflow 3.692e+04
10^5
10^4
10^3
10^2
10
1
-100
-80
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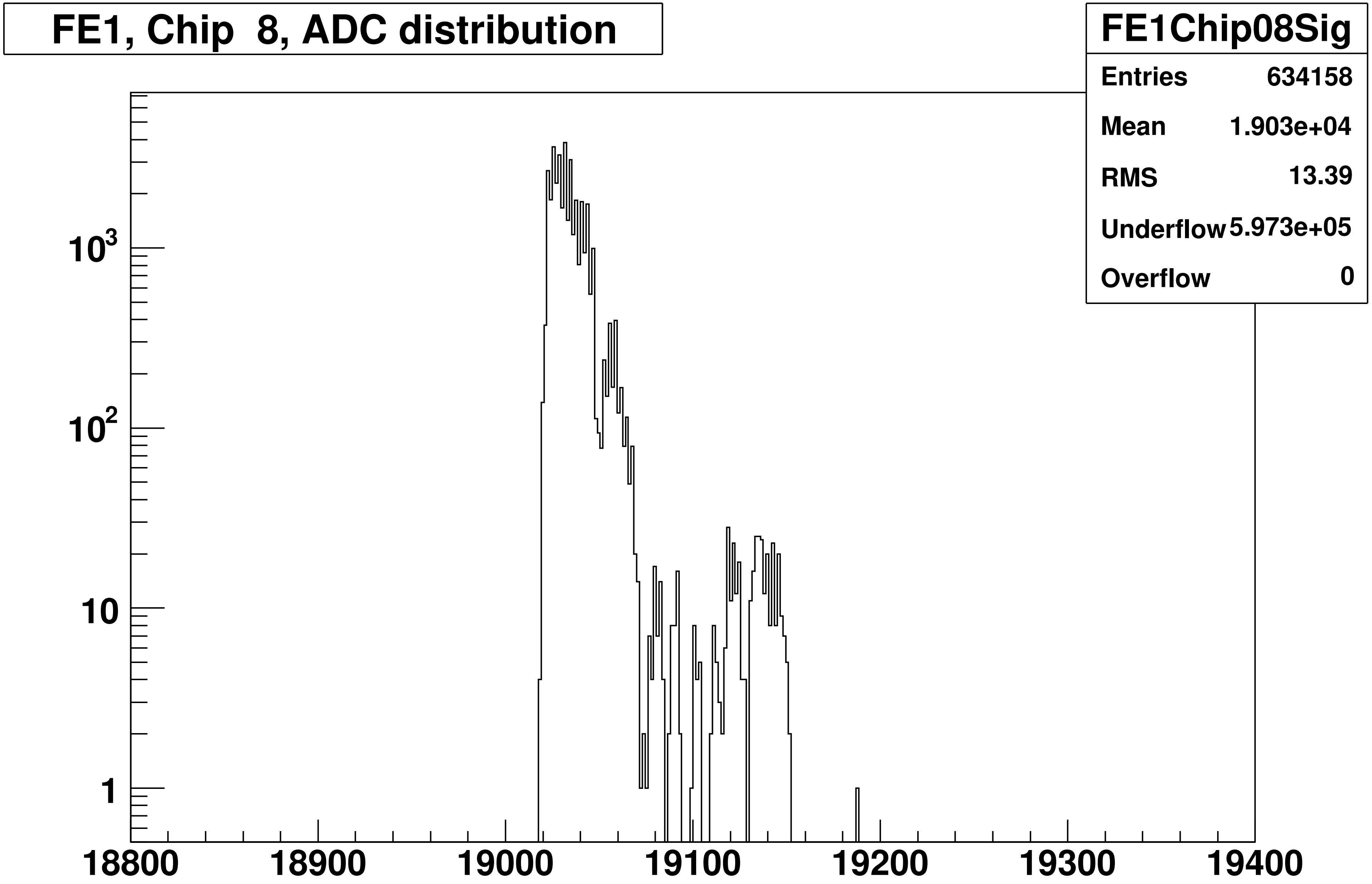
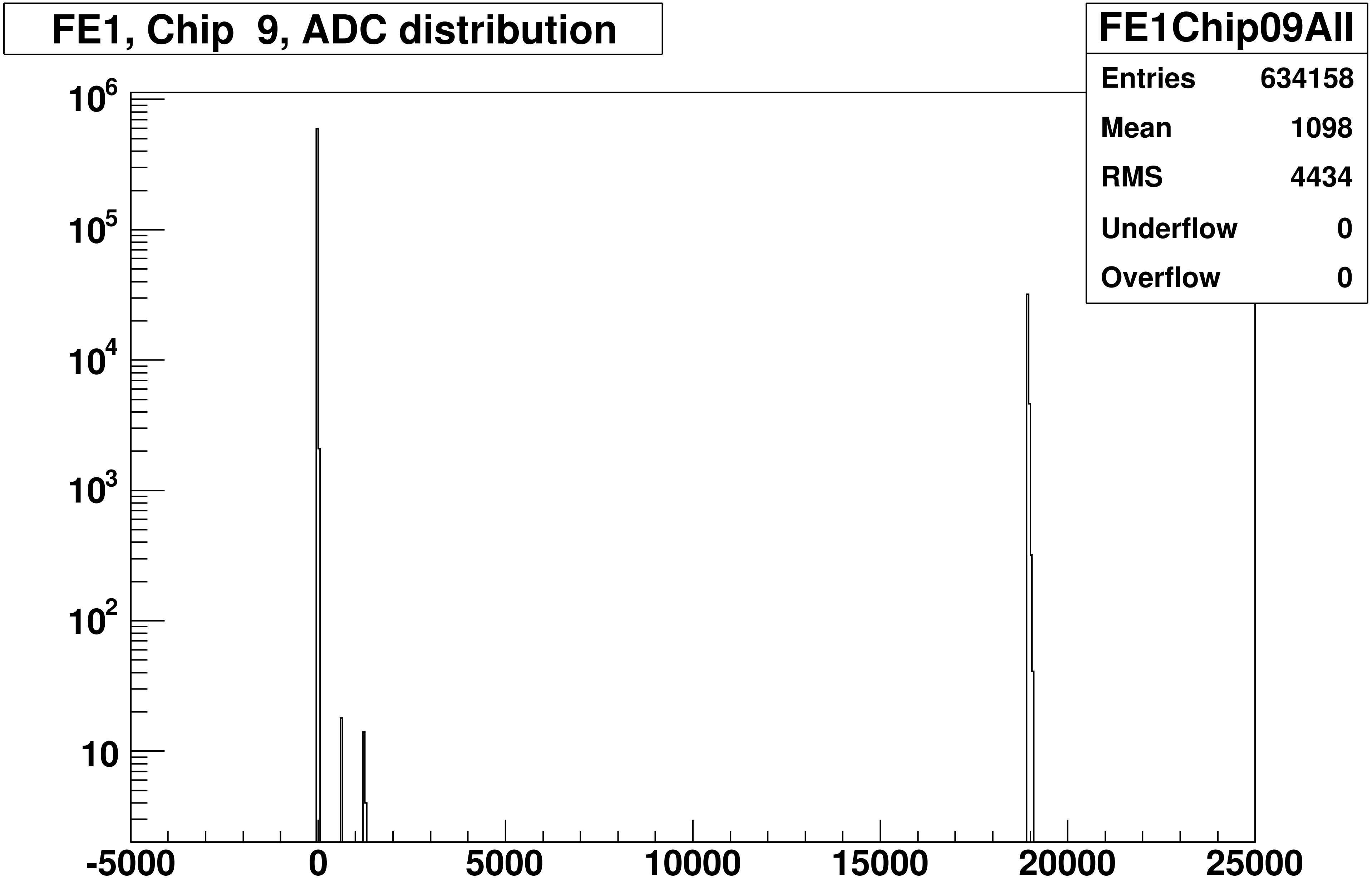
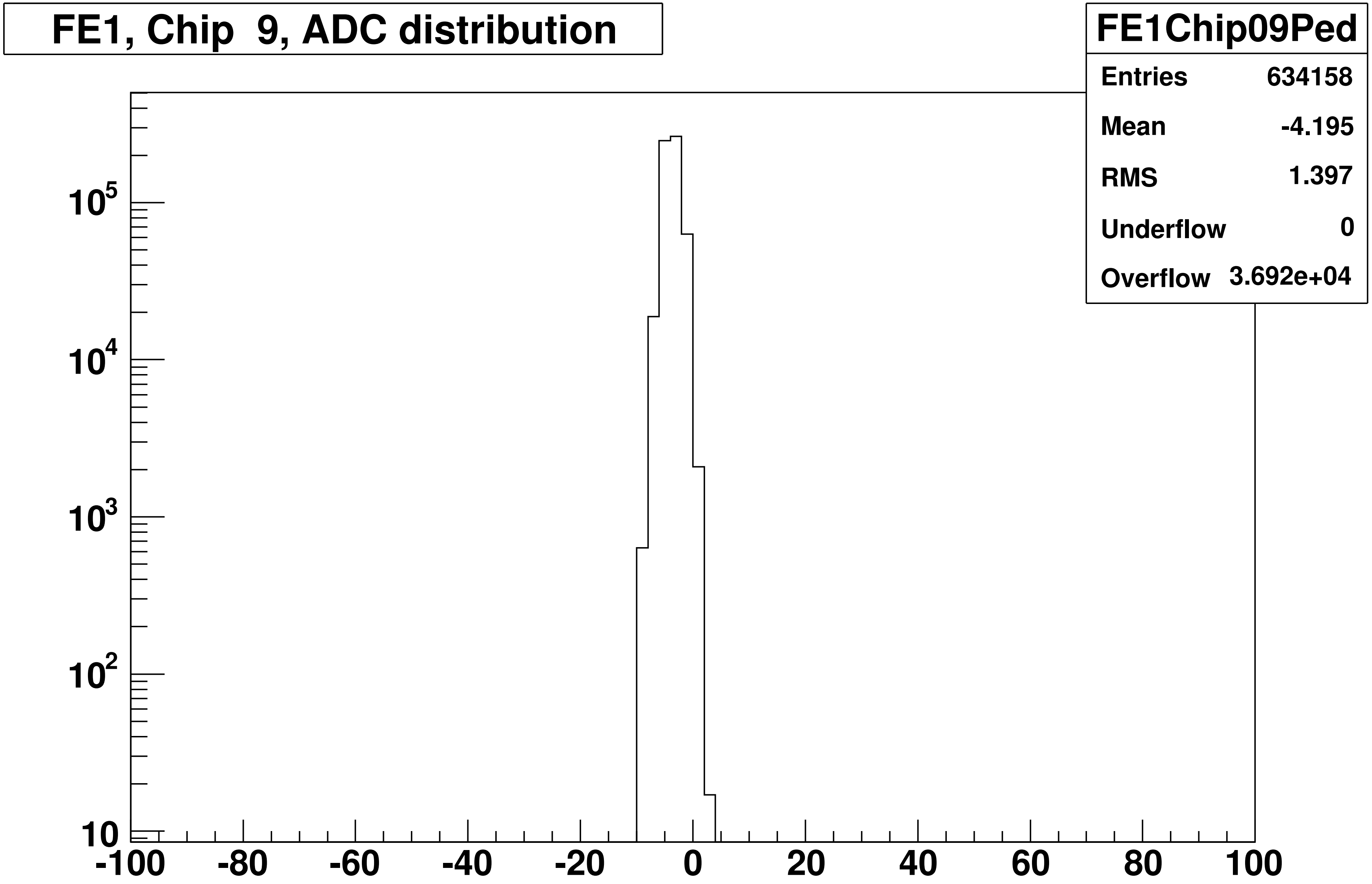
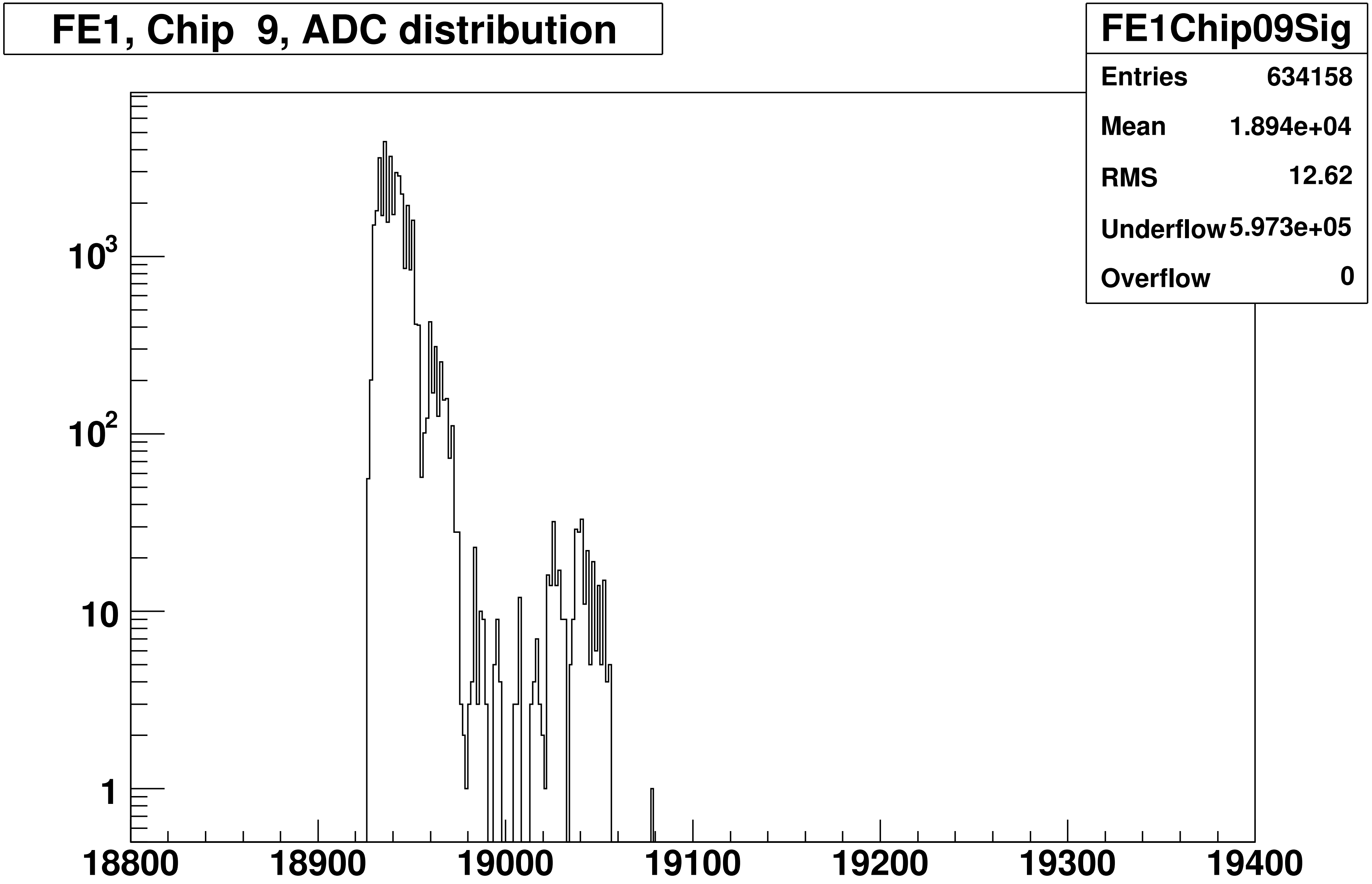
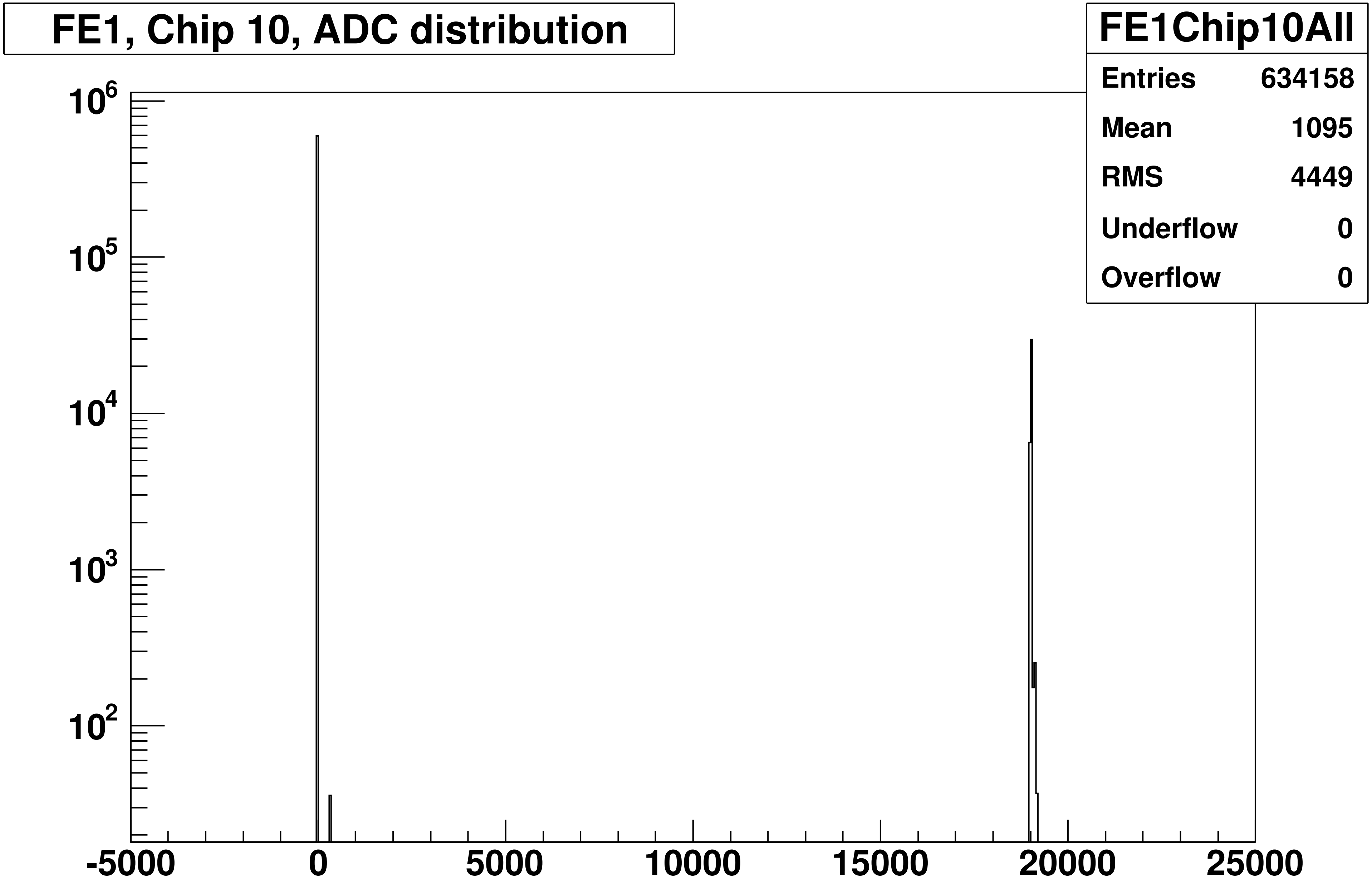
-40
-20
0
20
40
60
80
100


FE1, Chip 8, ADC distribution
FE1Chip08Sig
Entries 634158
Mean 1.903e+04
RMS 13.39
Underflow 5.973e+05
Overflow 0
10^3
10^2
10
1
18800
18900
19000
19100
19200
19300
19400


FE1, Chip 9, ADC distribution
FE1Chip09All
Entries 634158
Mean 1098
RMS 4434
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE1, Chip 9, ADC distribution
FE1Chip09Ped
Entries 634158
Mean -4.195
RMS 1.397
Underflow 0
Overflow 3.692e+04
10
10^2
10^3
10^4
10^5
-100
-80
-60
-40
-20
0
20
40
60
80
100


FE1, Chip 9, ADC distribution
FE1Chip09Sig
Entries 634158
Mean 1.894e+04
RMS 12.62
Underflow 5.973e+05
Overflow 0
10^3
10^2
10
1
18800
18900
19000
19100
19200
19300
19400


FE1, Chip 10, ADC distribution
FE1Chip10All
Entries 634158
Mean 1095
RMS 4449
Underflow 0
Overflow 0
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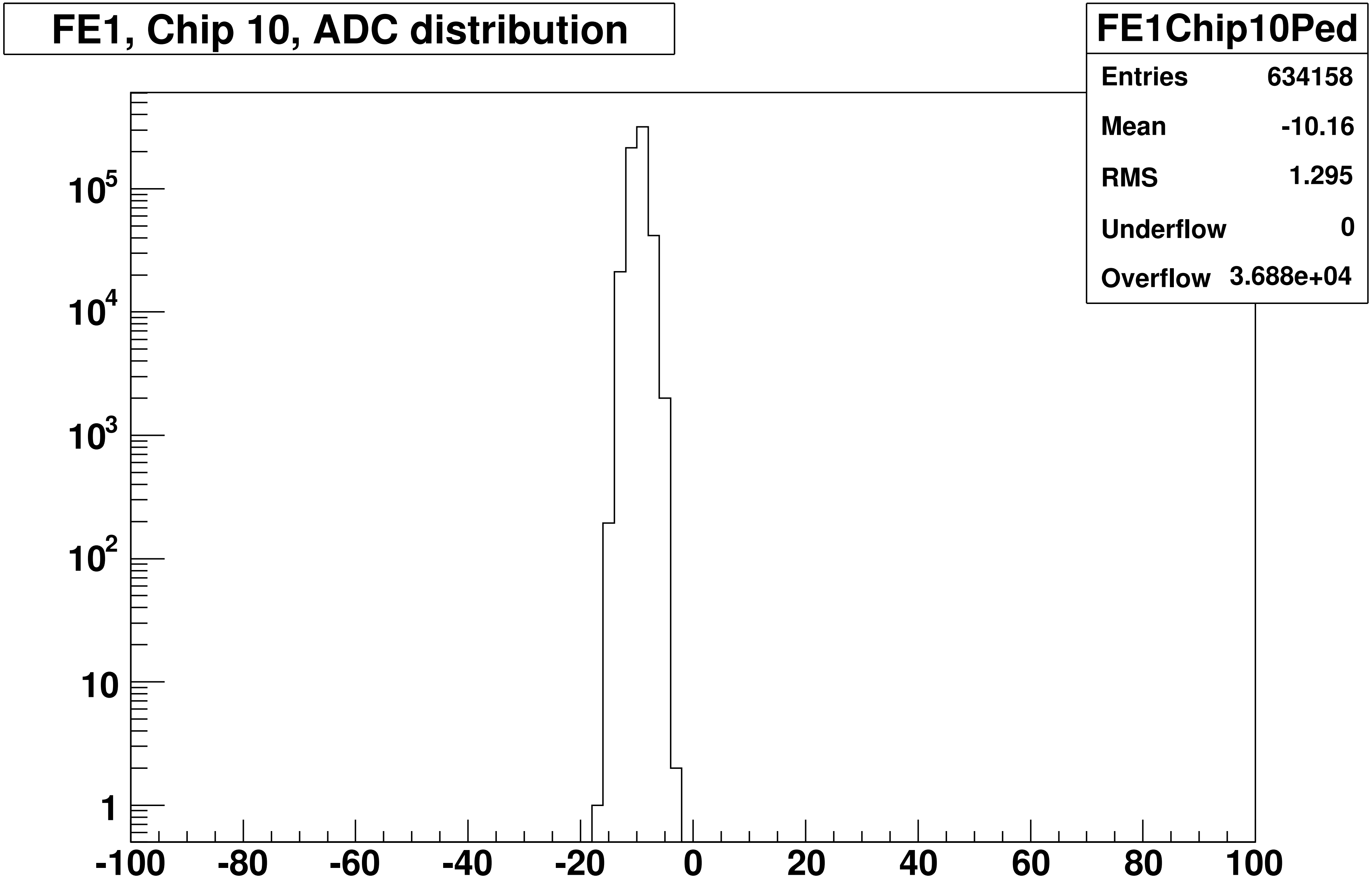
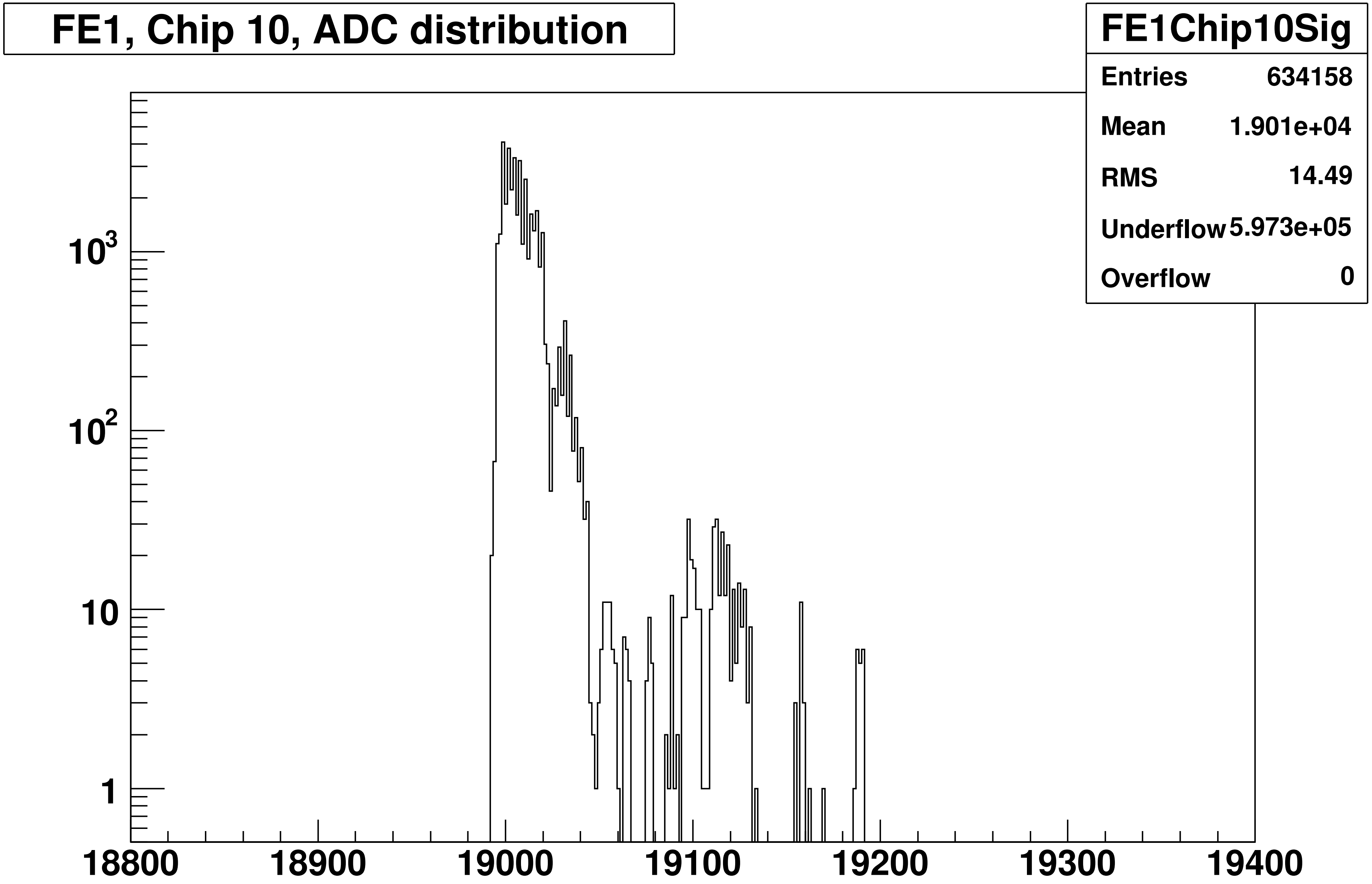
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000


FE1, Chip 10, ADC distribution
FE1Chip10Ped
Entries 634158
Mean -10.16
RMS 1.295
Underflow 0
Overflow 3.688e+04
10^5
10^4
10^3
10^2
10
1
-100
-80
-60
-40
-20
0
20
40
60
80
100



FE1, Chip 10, ADC distribution
FE1Chip10Sig
Entries 634158
Mean 1.901e+04
RMS 14.49
Underflow 5.973e+05
Overflow 0
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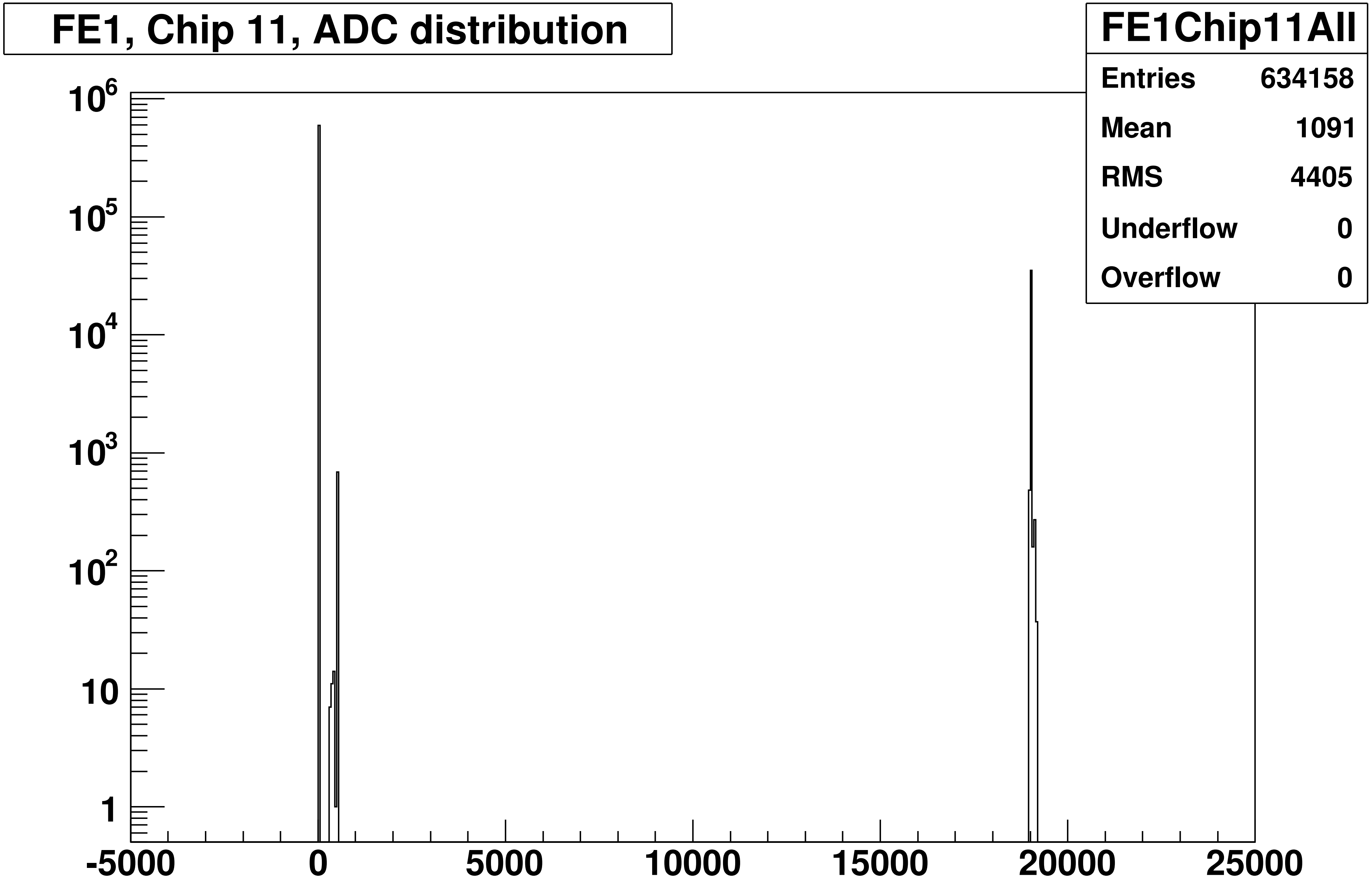
10^2
10
1
18800
18900
19000
19100
19200
19300
19400


FE1, Chip 11, ADC distribution
FE1Chip11All
Entries 634158
Mean 1091
RMS 4405
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
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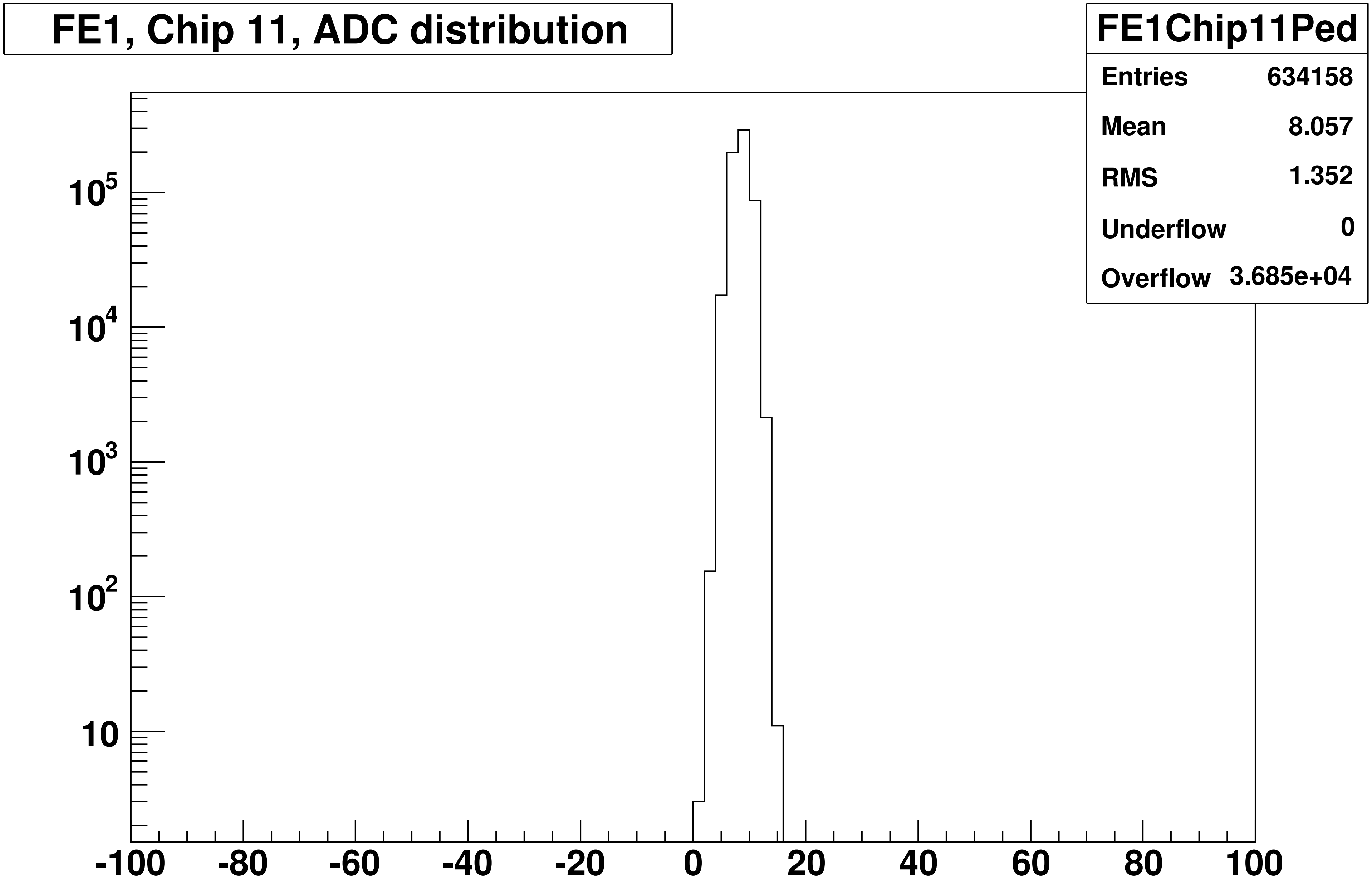
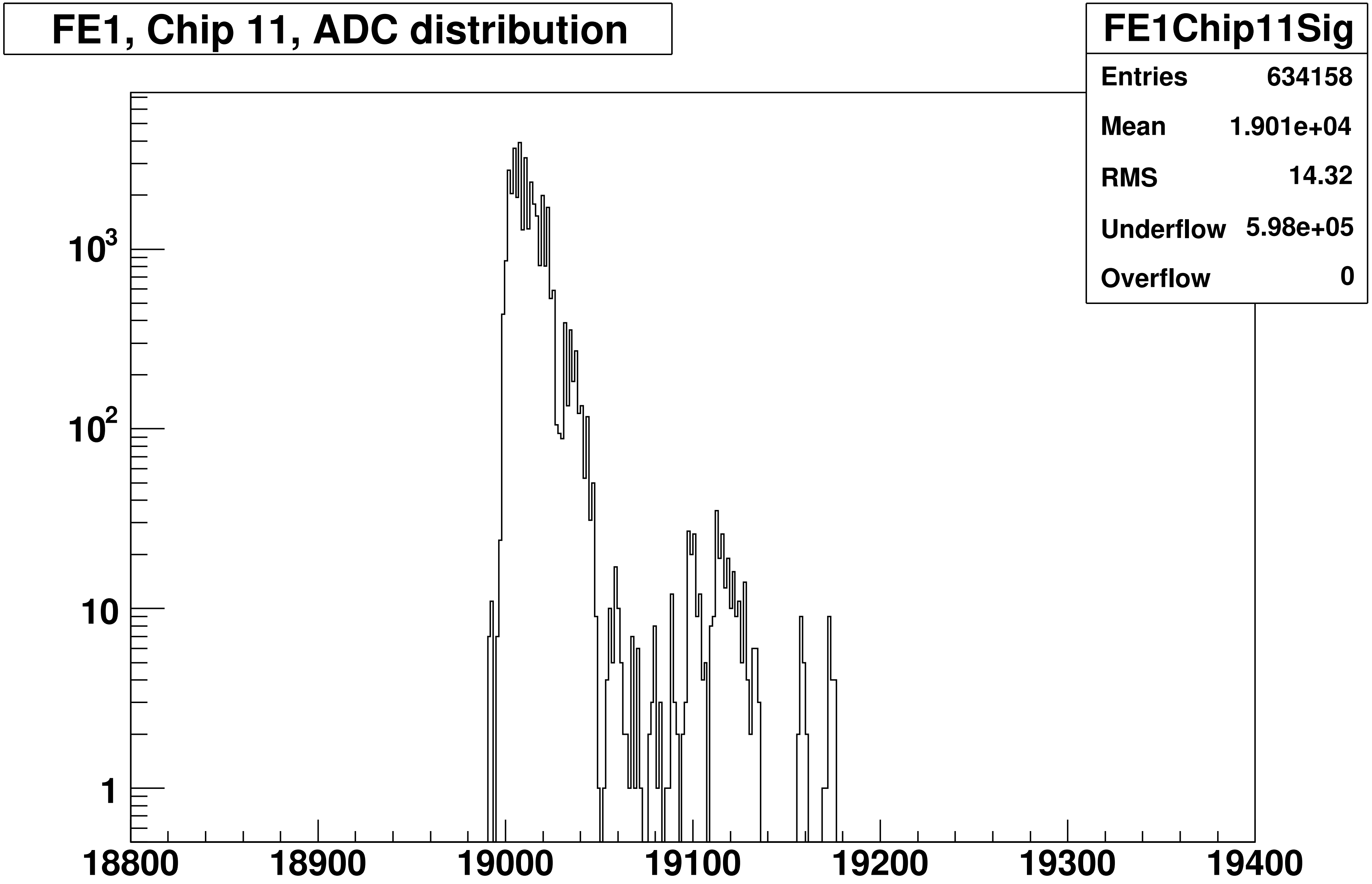
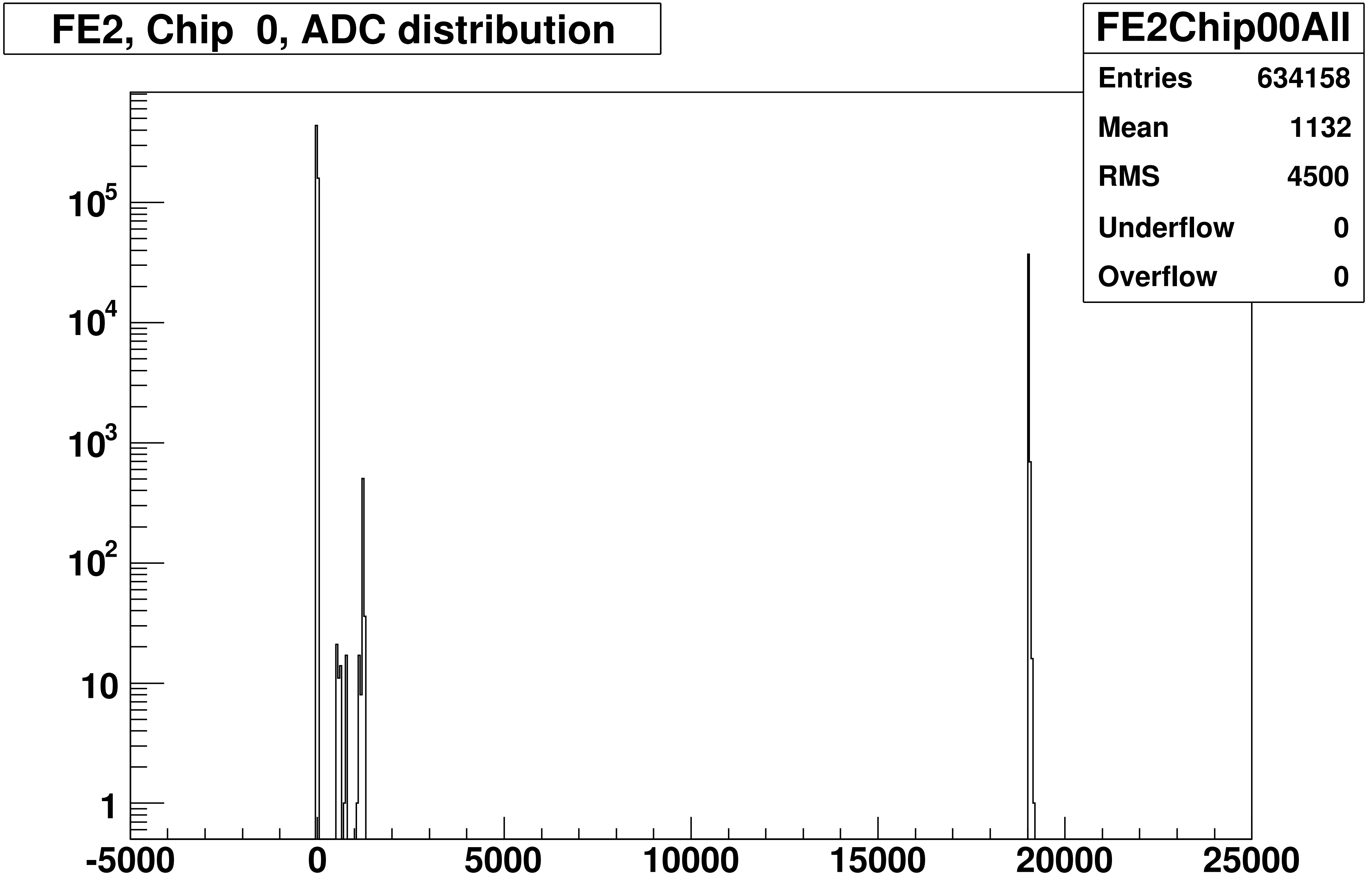
10000
15000
20000
25000



FE1, Chip 11, ADC distribution
FE1Chip11Ped
Entries 634158
Mean 8.057
RMS 1.352
Underflow 0
Overflow 3.685e+04
10^5
10^4
10^3
10^2
10
-100 -80 -60 -40 -20 0 20 40 60 80 100


FE1, Chip 11, ADC distribution
FE1Chip11Sig
Entries 634158
Mean 1.901e+04
RMS 14.32
Underflow 5.98e+05
Overflow 0
10^3
10^2
10
1
18800
18900
19000
19100
19200
19300
19400


FE2, Chip 0, ADC distribution
FE2Chip00All
Entries 634158
Mean 1132
RMS 4500
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
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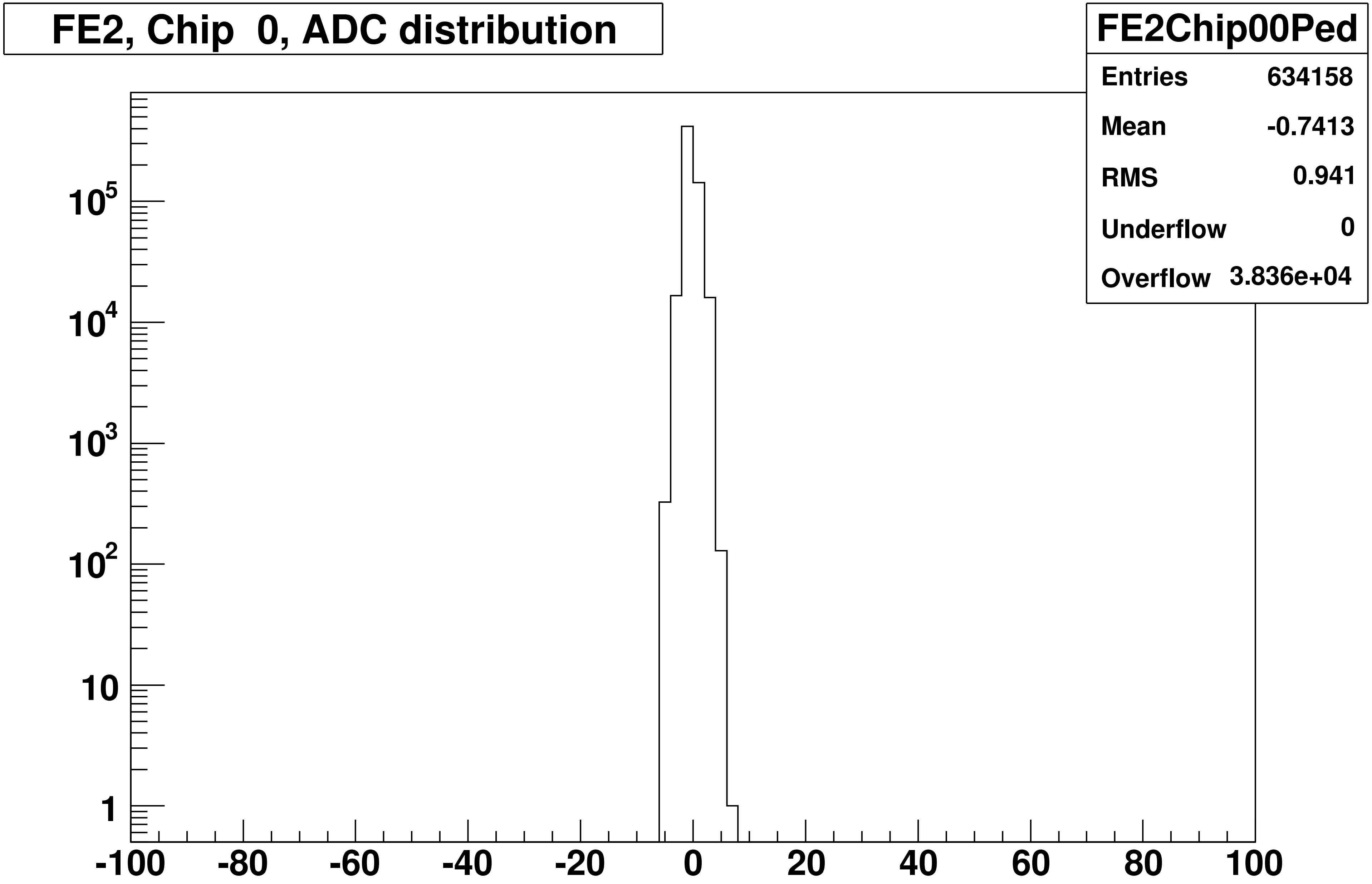
10000
15000
20000
25000


FE2, Chip 0, ADC distribution
FE2Chip00Ped
Entries 634158
Mean -0.7413
RMS 0.941
Underflow 0
Overflow 3.836e+04
10^5
10^4
10^3
10^2
10
1
-100
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-60
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-20
0
20
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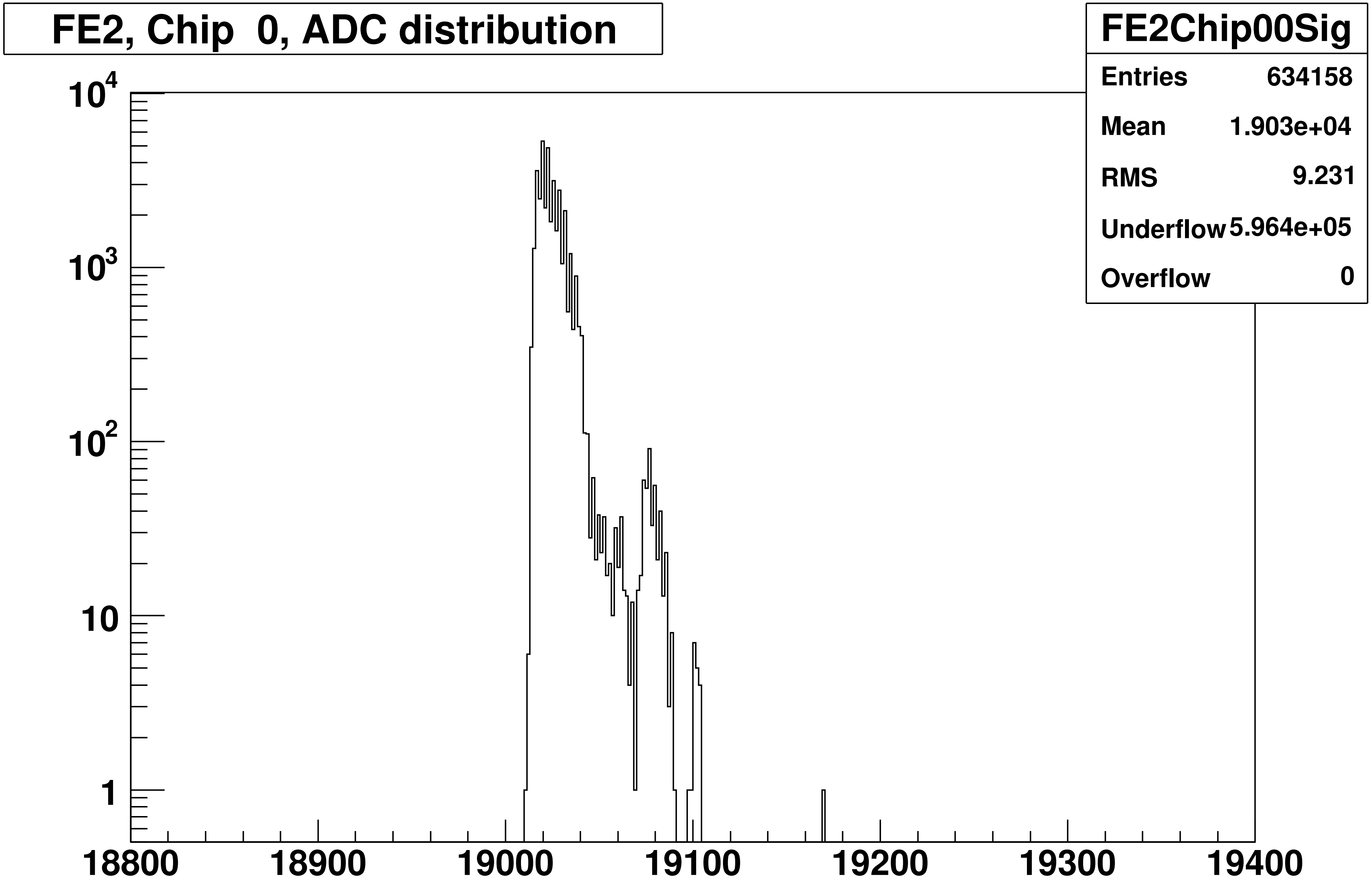
60
80
100


FE2, Chip 0, ADC distribution
FE2Chip00Sig
Entries 634158
Mean 1.903e+04
RMS 9.231
Underflow 5.964e+05
Overflow 0
10^4
10^3
10^2
10
1
18800
18900
19000
19100
19200
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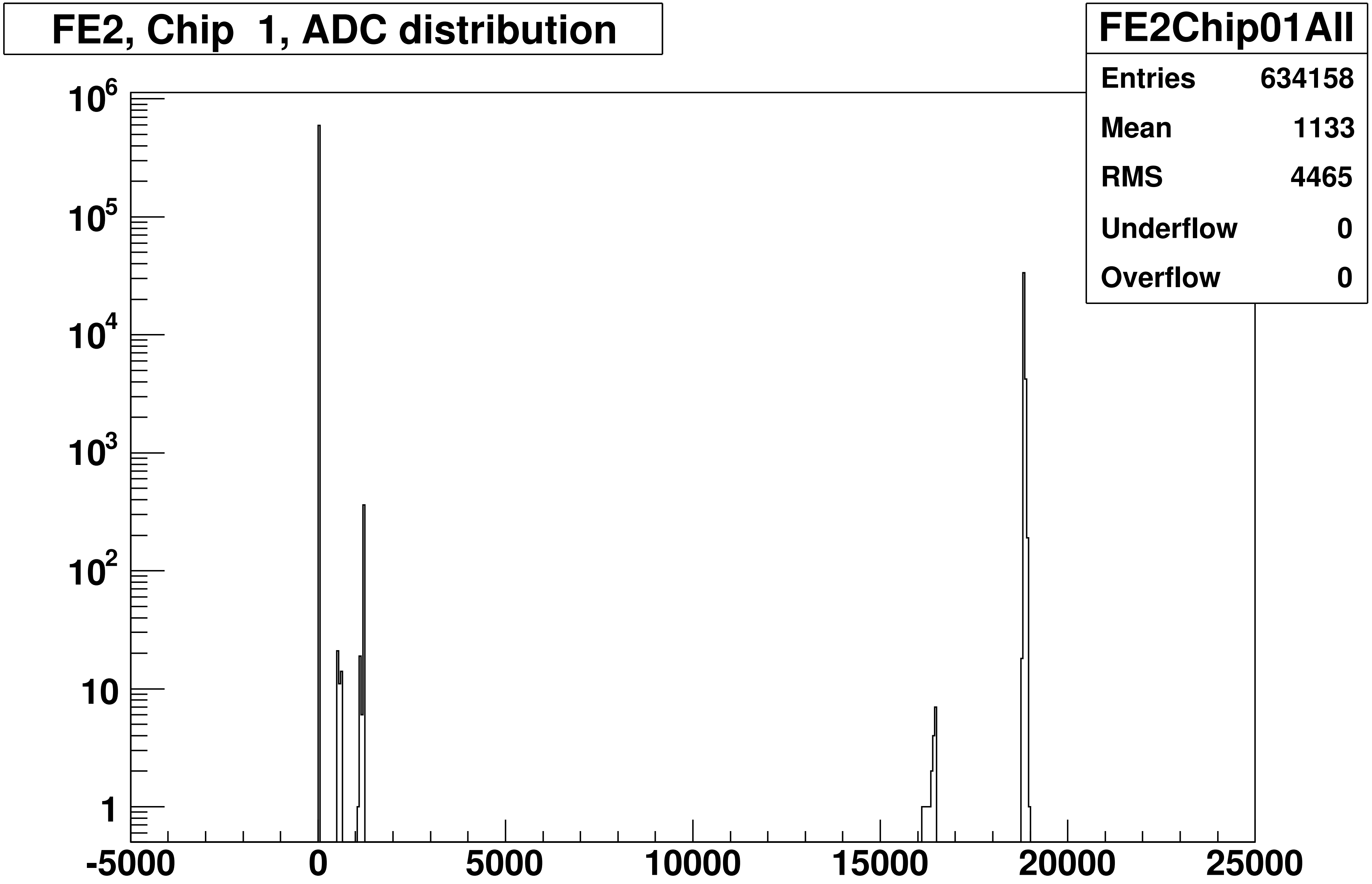
19400


FE2, Chip 1, ADC distribution
FE2Chip01All
Entries 634158
Mean 1133
RMS 4465
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
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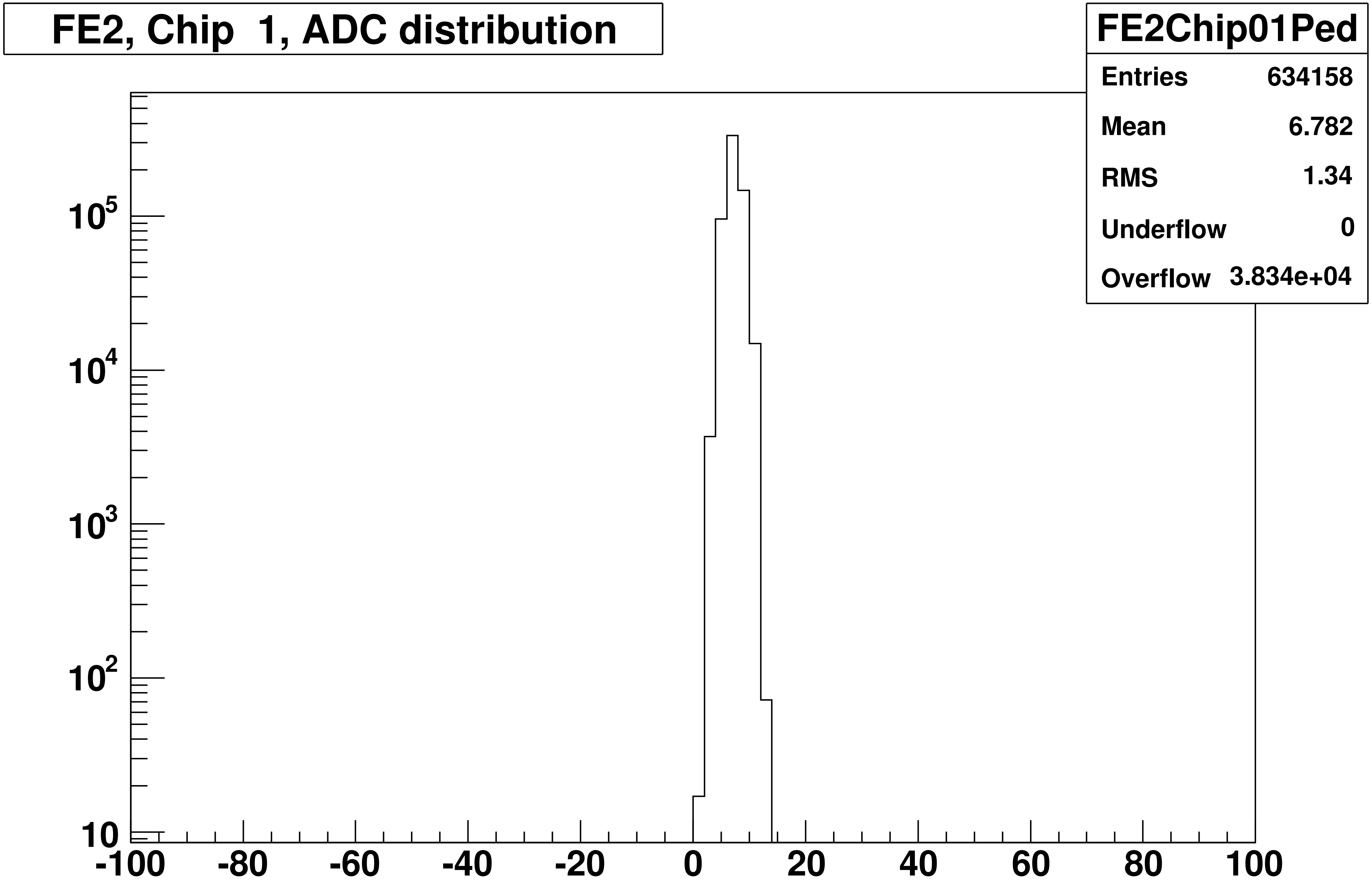
FE2, Chip 1, ADC distribution
FE2Chip01Ped
Entries 634158
Mean 6.782
RMS 1.34
Underflow 0
Overflow 3.834e+04
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10^4
10^3
10^2
10
-100
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-20
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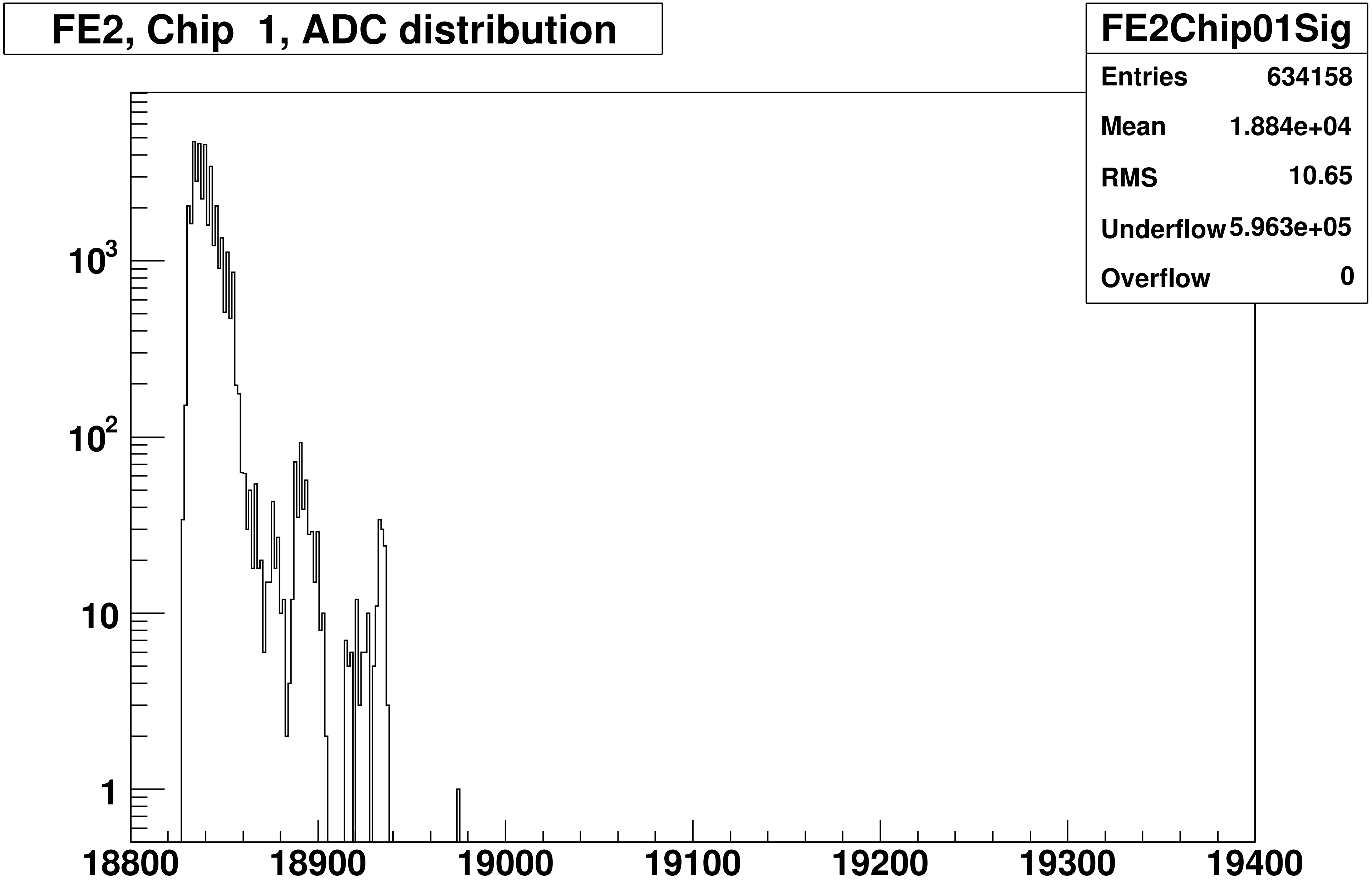
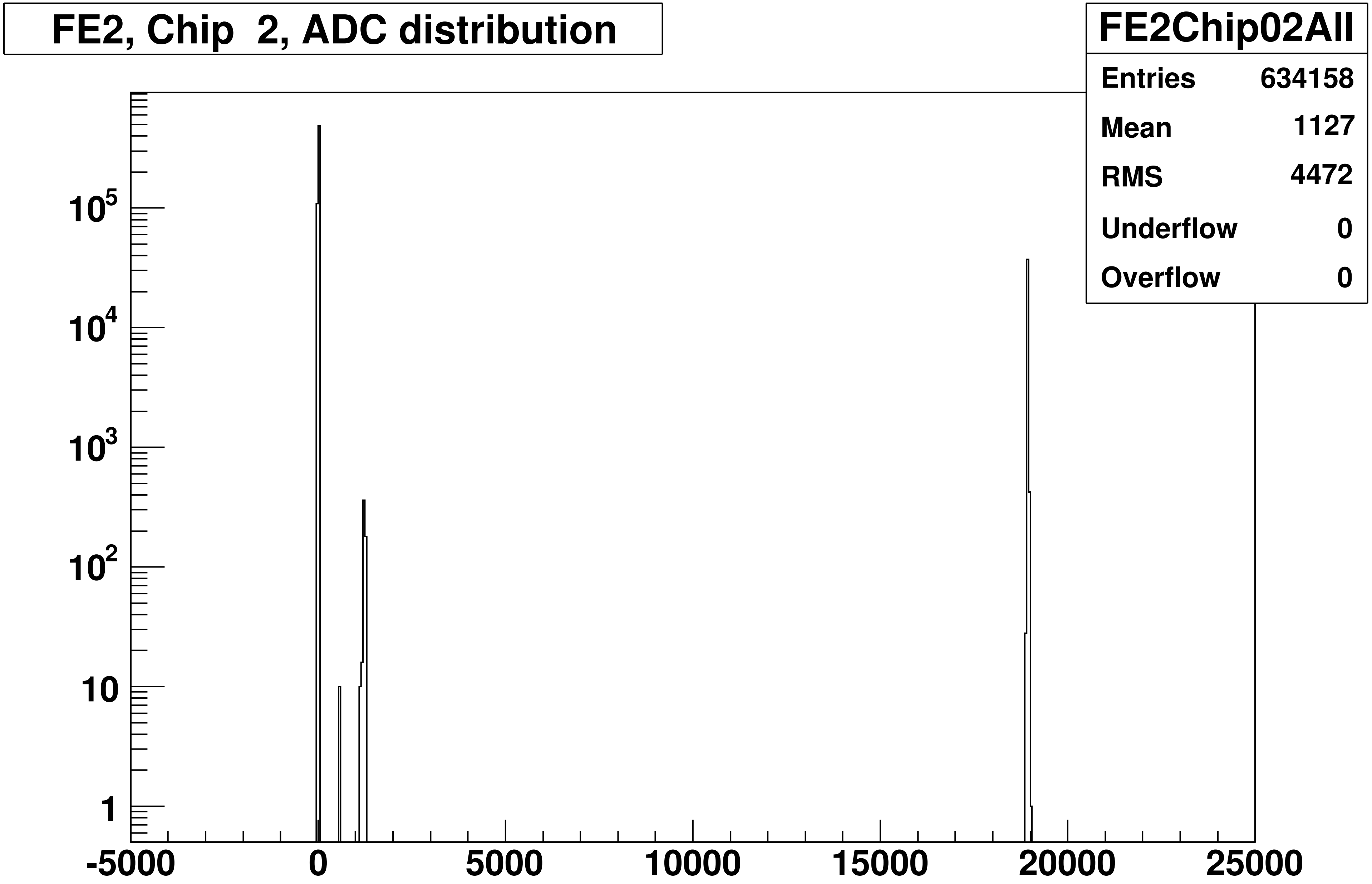
80
100


FE2, Chip 1, ADC distribution
FE2Chip01Sig
Entries 634158
Mean 1.884e+04
RMS 10.65
Underflow 5.963e+05
Overflow 0
10^3
10^2
10
1
18800
18900
19000
19100
19200
19300
19400


FE2, Chip 2, ADC distribution
FE2Chip02All
Entries 634158
Mean 1127
RMS 4472
Underflow 0
Overflow 0
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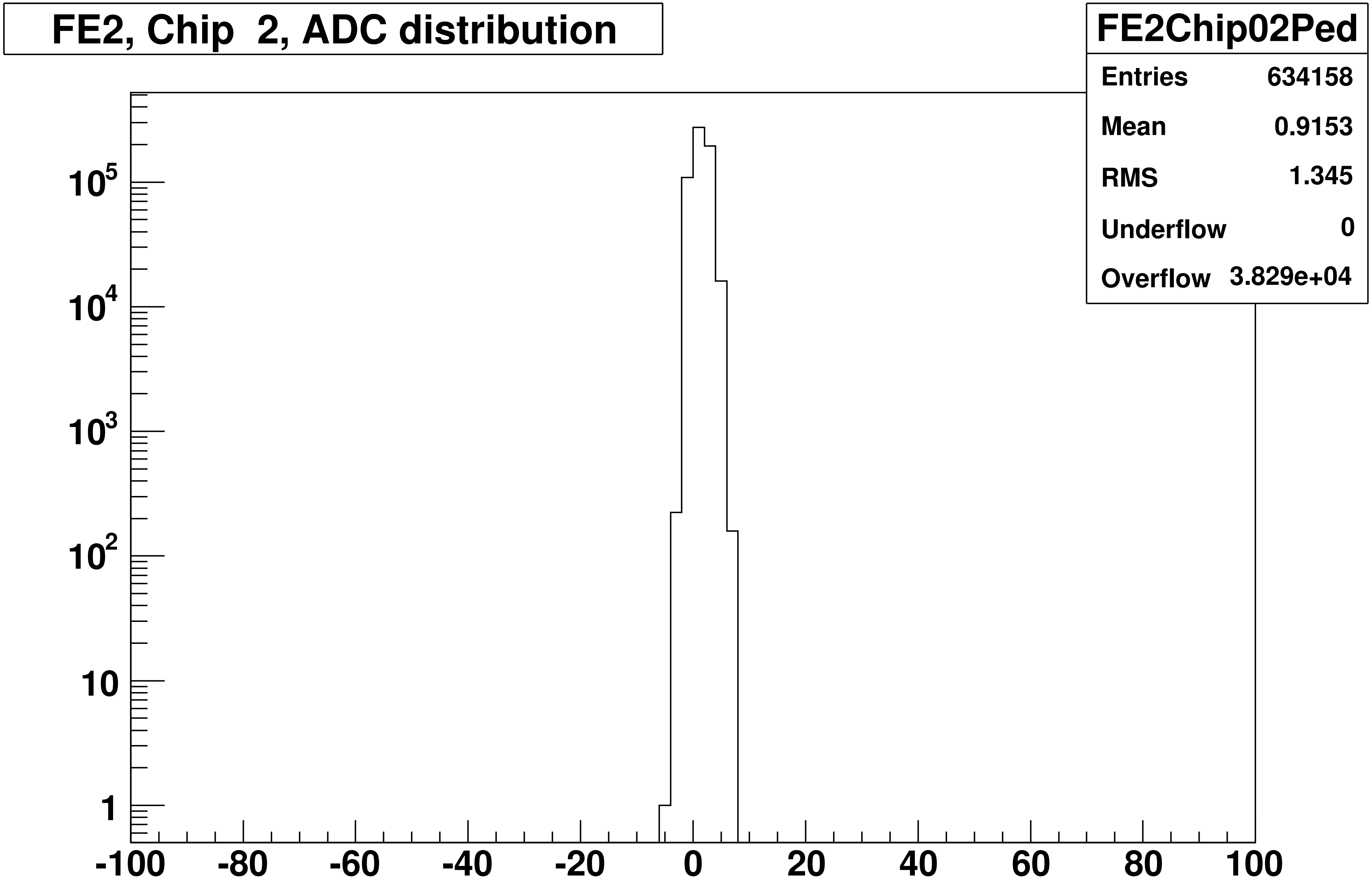
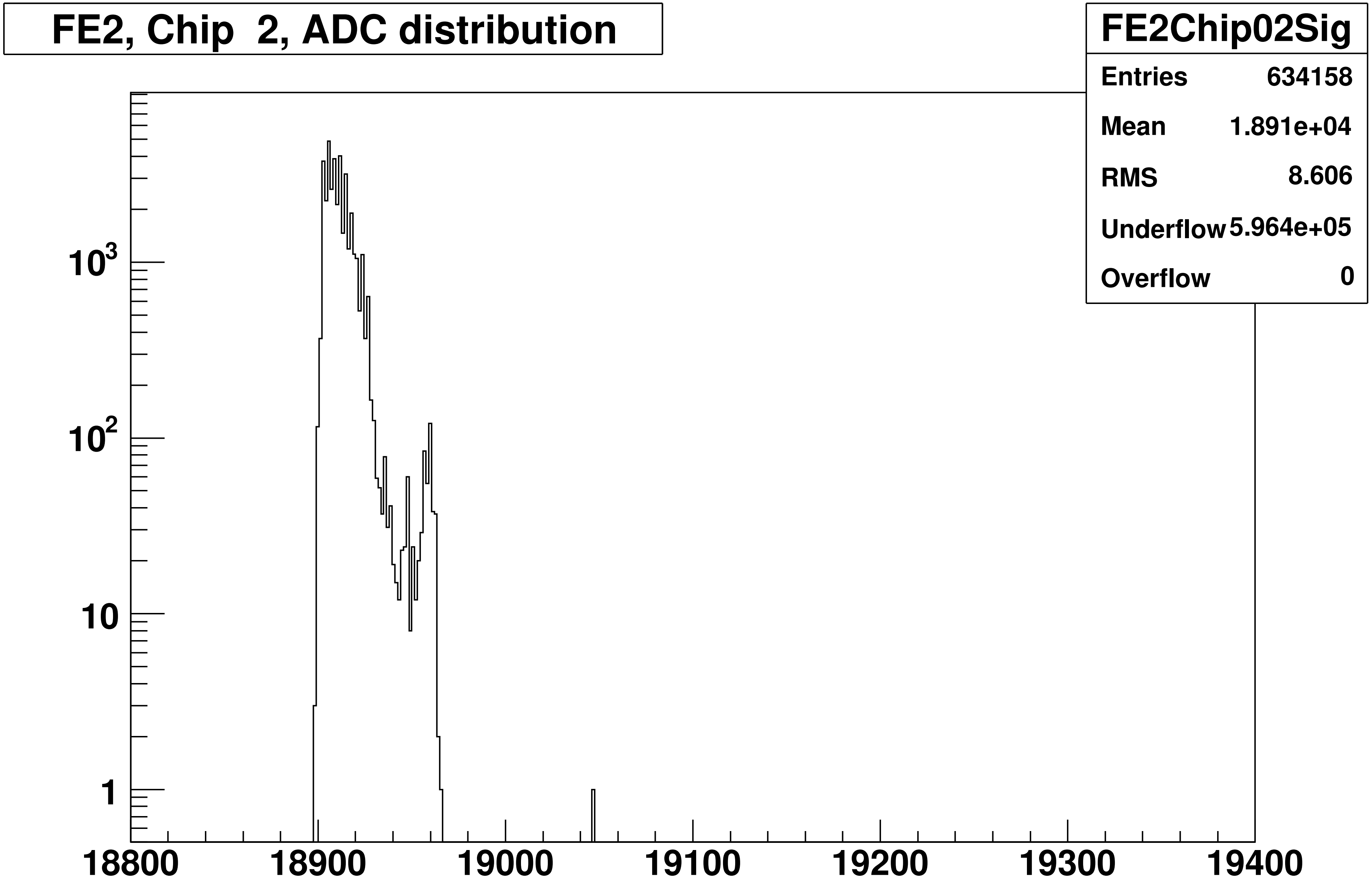
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE2, Chip 2, ADC distribution
FE2Chip02Ped
Entries 634158
Mean 0.9153
RMS 1.345
Underflow 0
Overflow 3.829e+04
10^5
10^4
10^3
10^2
10
1
-100 -80 -60 -40 -20 0 20 40 60 80 100


FE2, Chip 2, ADC distribution
FE2Chip02Sig
Entries 634158
Mean 1.891e+04
RMS 8.606
Underflow 5.964e+05
Overflow 0
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10
10^2
10^3
18800
18900
19000
19100
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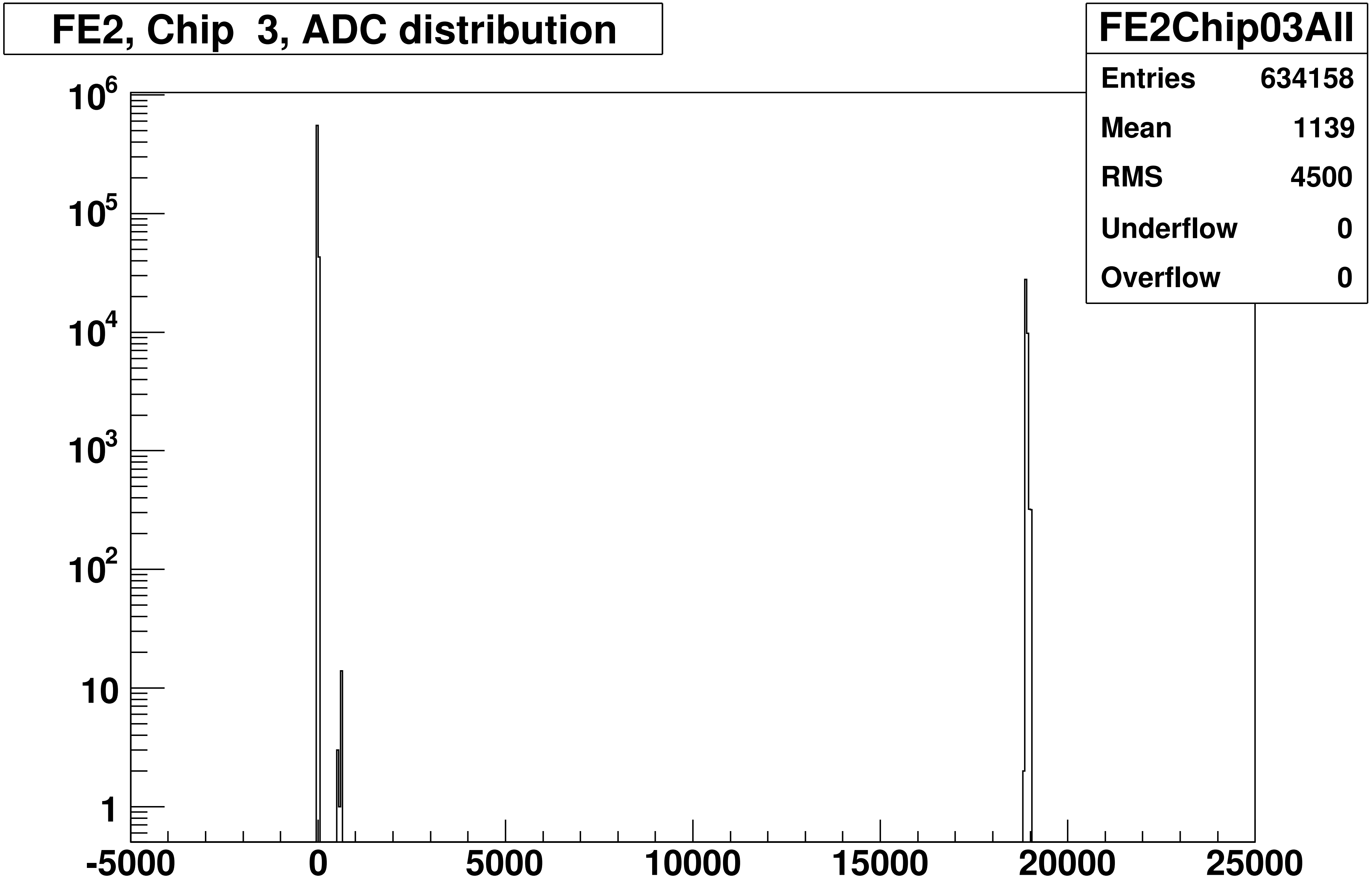
FE2, Chip 3, ADC distribution
FE2Chip03All
Entries 634158
Mean 1139
RMS 4500
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
1
-5000
0
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10000
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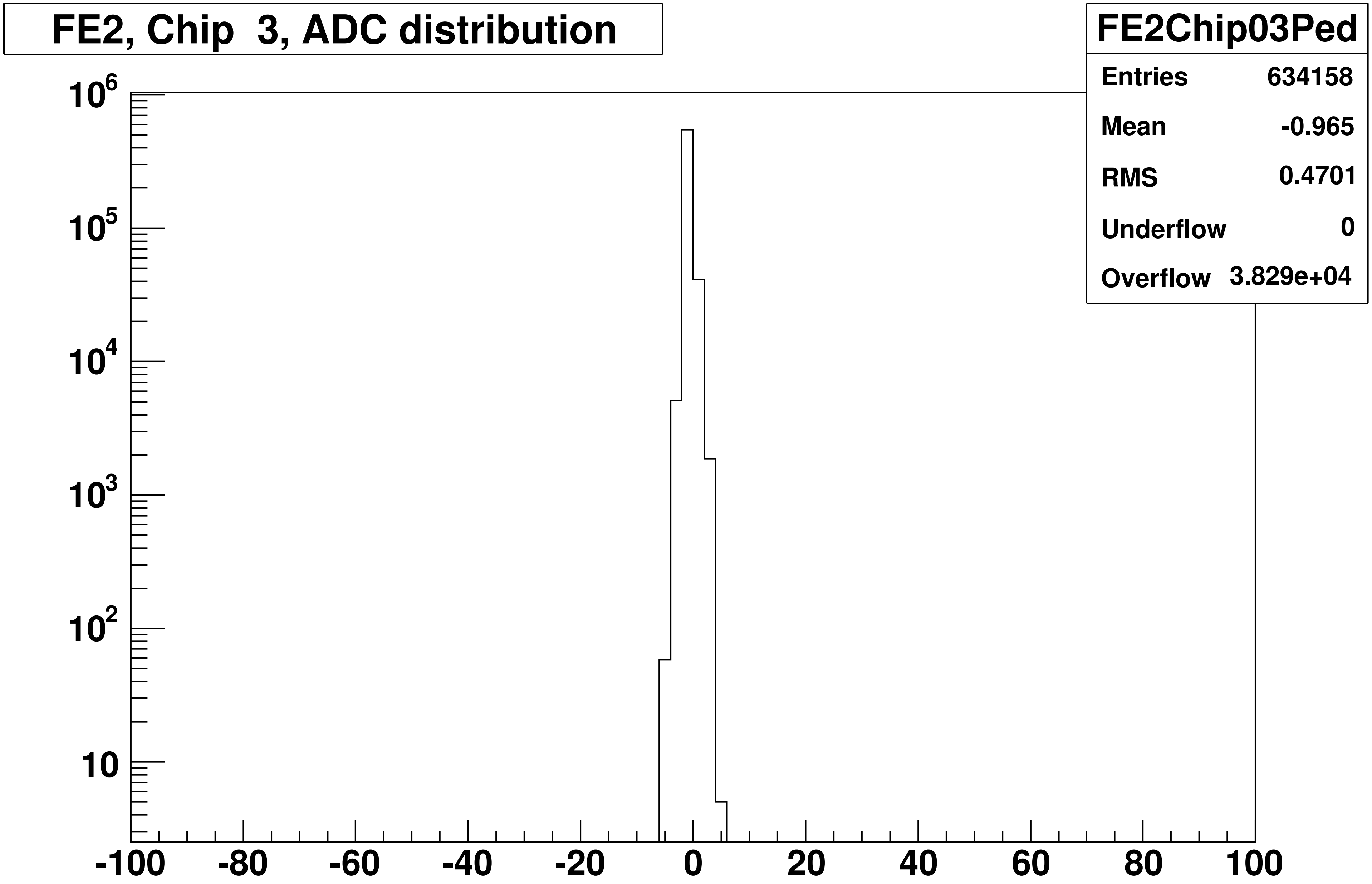
20000
25000


FE2, Chip 3, ADC distribution
FE2Chip03Ped
Entries 634158
Mean -0.965
RMS 0.4701
Underflow 0
Overflow 3.829e+04
10^6
10^5
10^4
10^3
10^2
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-100
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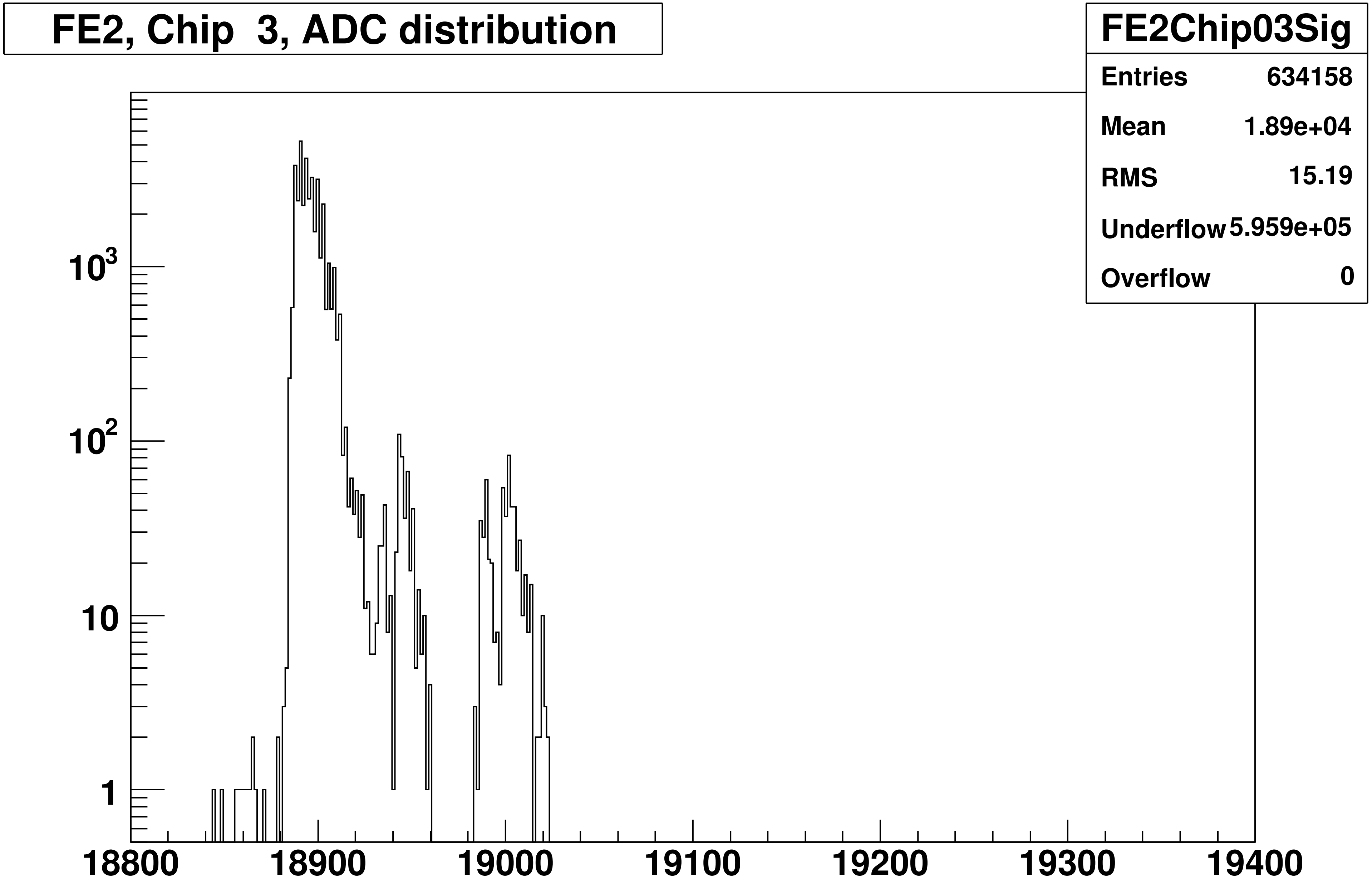
-40
-20
0
20
40
60
80
100


FE2, Chip 3, ADC distribution
FE2Chip03Sig
Entries 634158
Mean 1.89e+04
RMS 15.19
Underflow 5.959e+05
Overflow 0
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10^2
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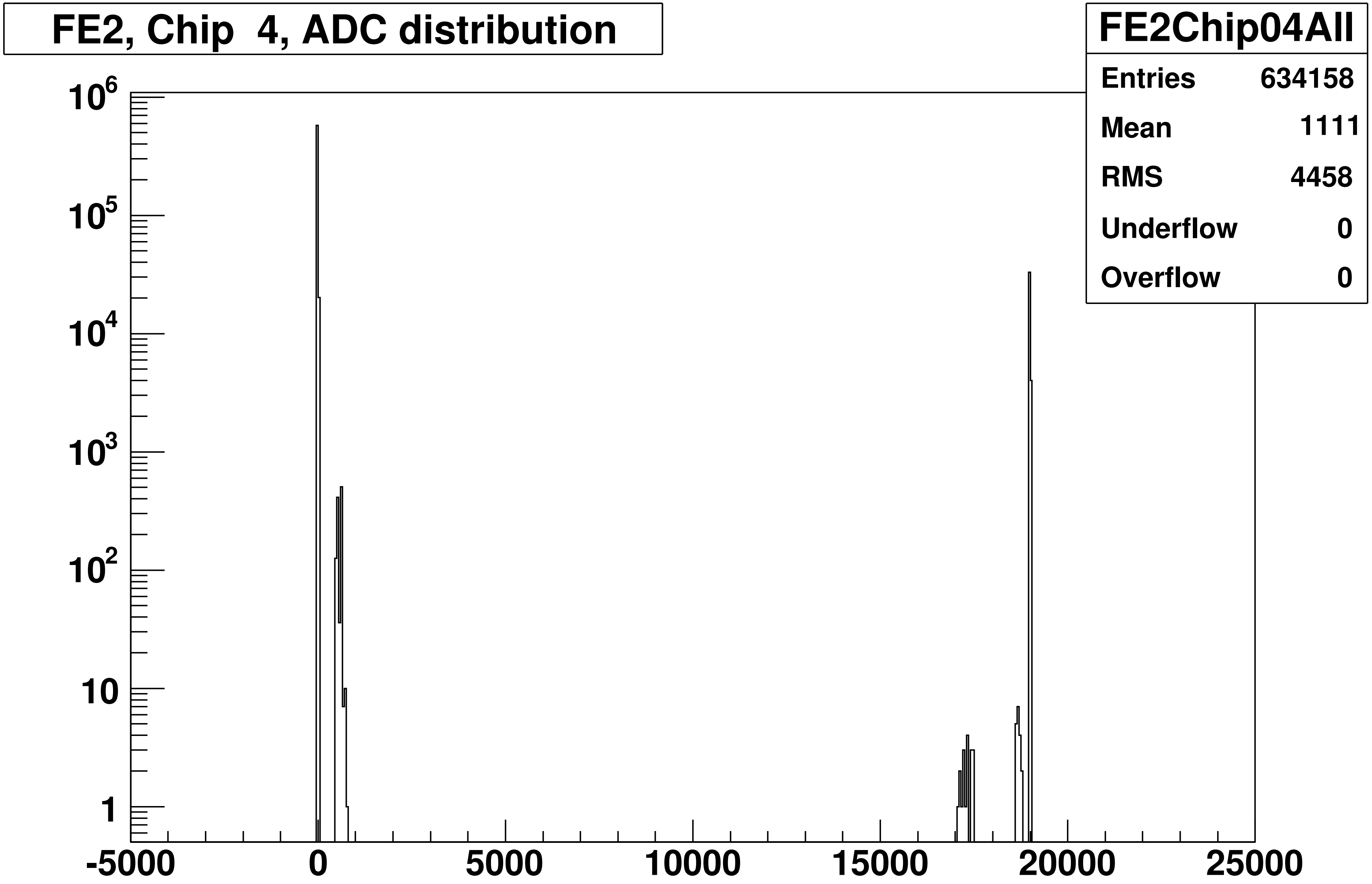
19400


FE2, Chip 4, ADC distribution
FE2Chip04All
Entries 634158
Mean 1111
RMS 4458
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
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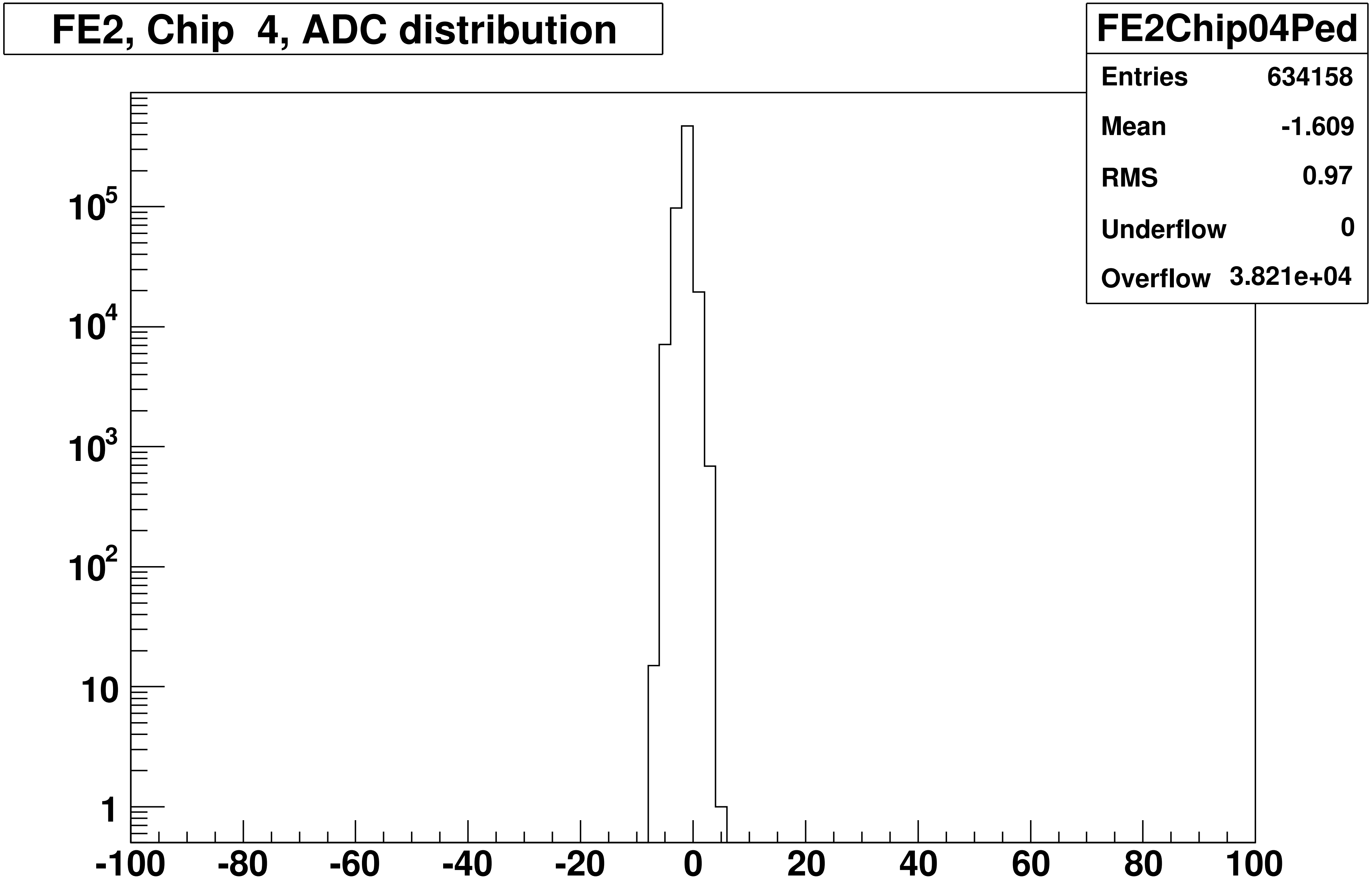
15000
20000
25000



FE2, Chip 4, ADC distribution
FE2Chip04Ped
Entries 634158
Mean -1.609
RMS 0.97
Underflow 0
Overflow 3.821e+04
10^5
10^4
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10^2
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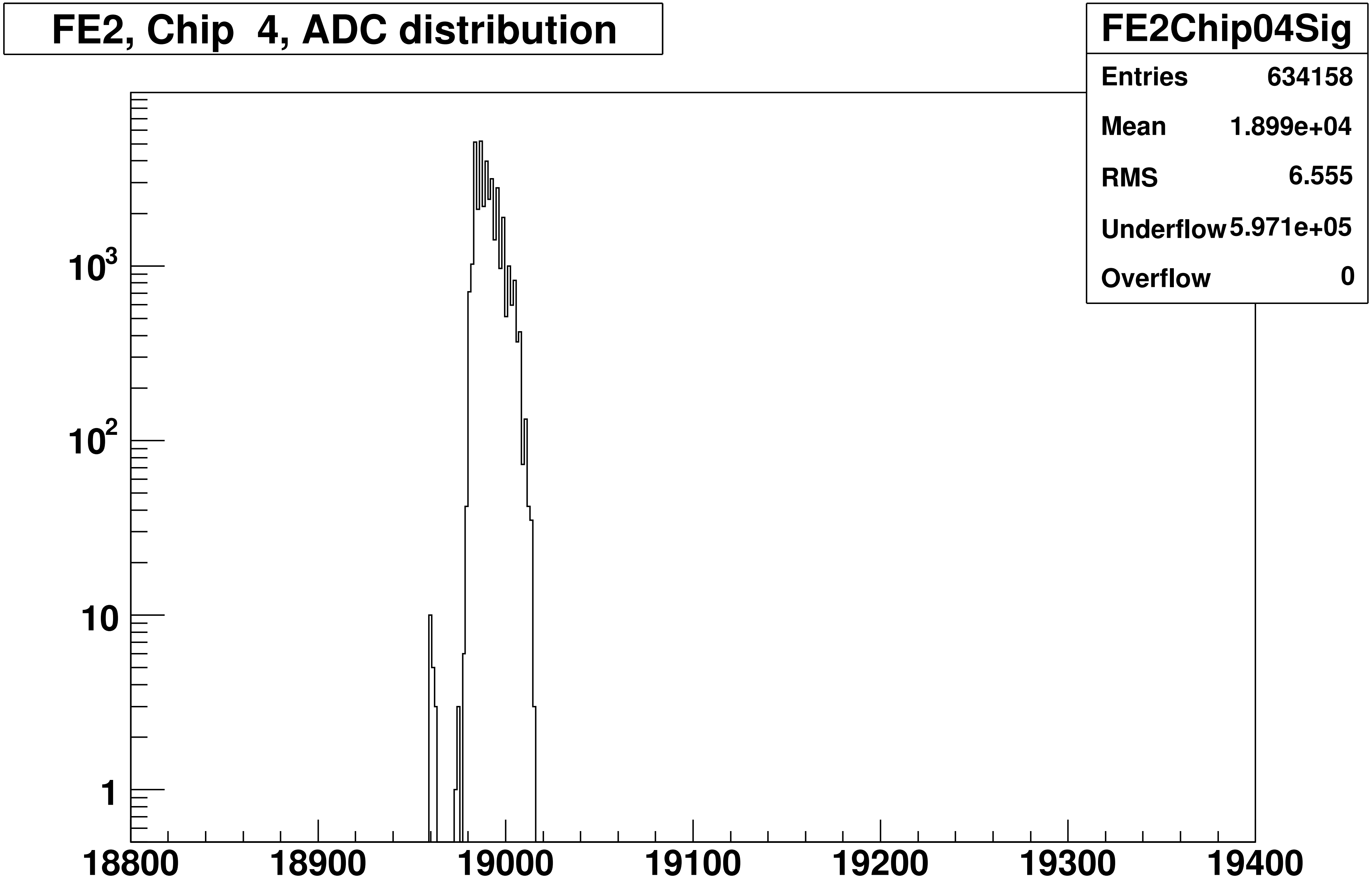
FE2, Chip 4, ADC distribution
FE2Chip04Sig
Entries 634158
Mean 1.899e+04
RMS 6.555
Underflow 5.971e+05
Overflow 0
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10^2
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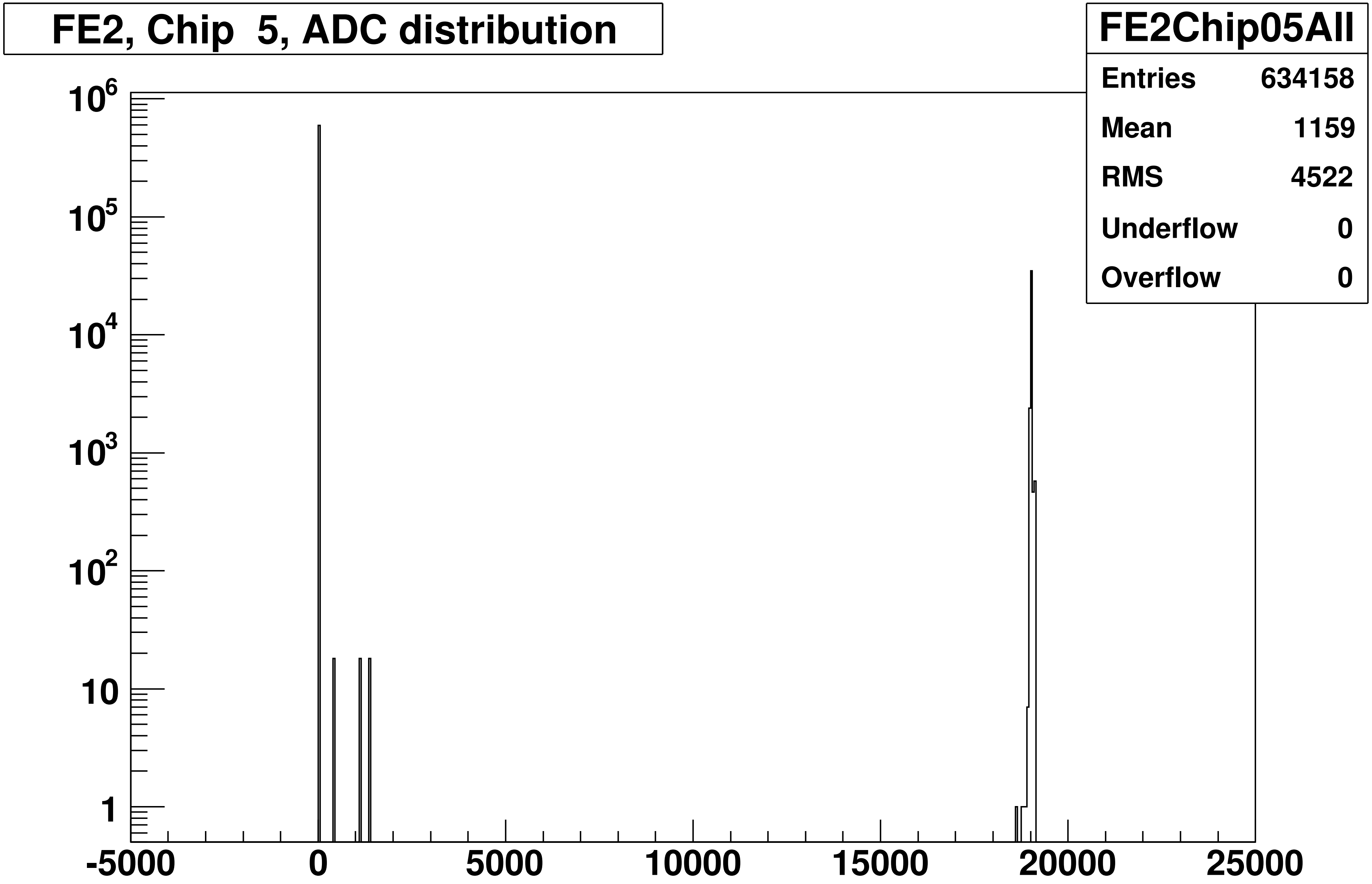

FE2, Chip 5, ADC distribution
FE2Chip05All
Entries 634158
Mean 1159
RMS 4522
Underflow 0
Overflow 0
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10^3
10^2
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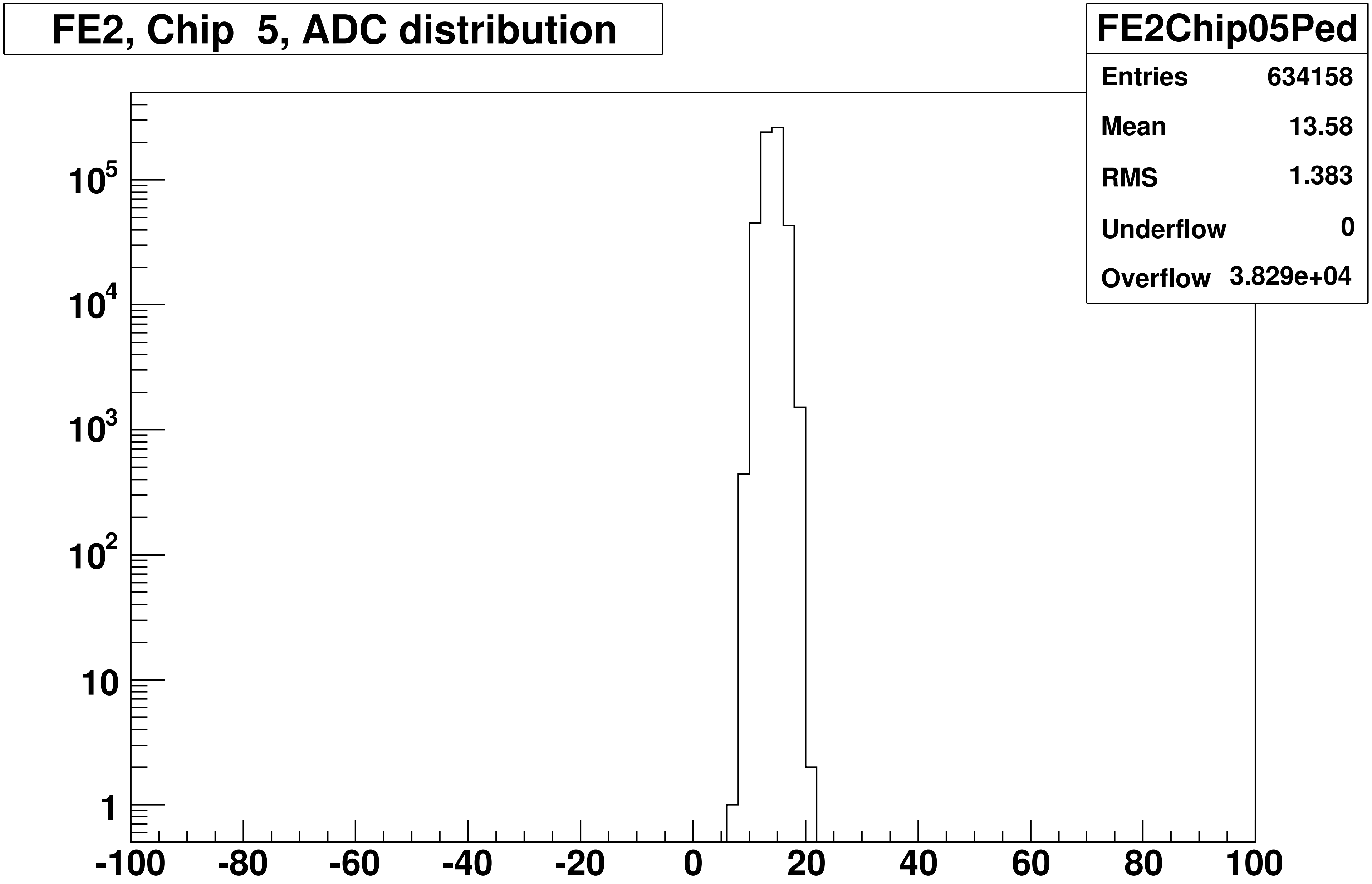
FE2, Chip 5, ADC distribution
FE2Chip05Ped
Entries 634158
Mean 13.58
RMS 1.383
Underflow 0
Overflow 3.829e+04
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10^4
10^3
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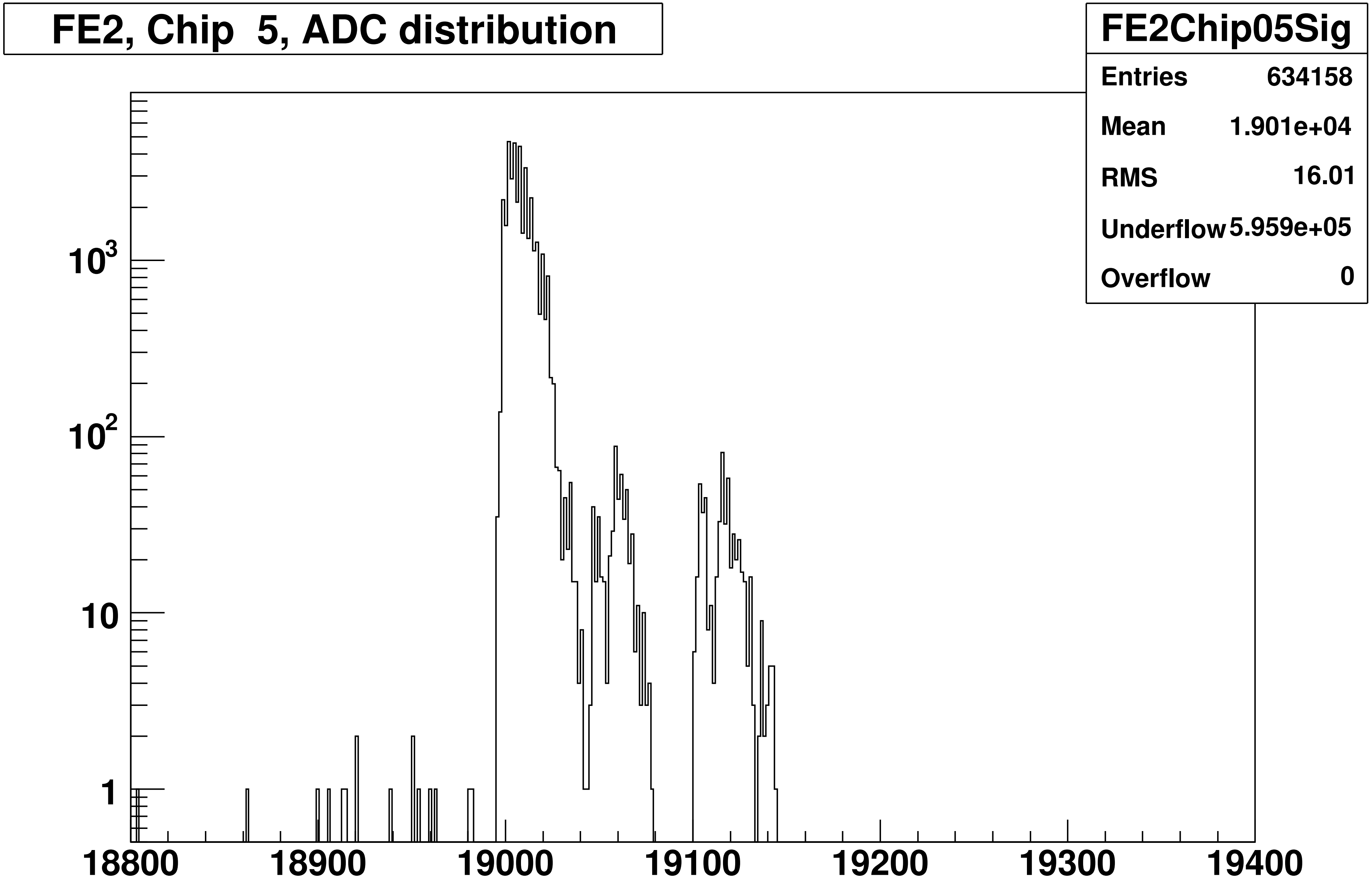
FE2, Chip 5, ADC distribution
FE2Chip05Sig
Entries 634158
Mean 1.901e+04
RMS 16.01
Underflow 5.959e+05
Overflow 0
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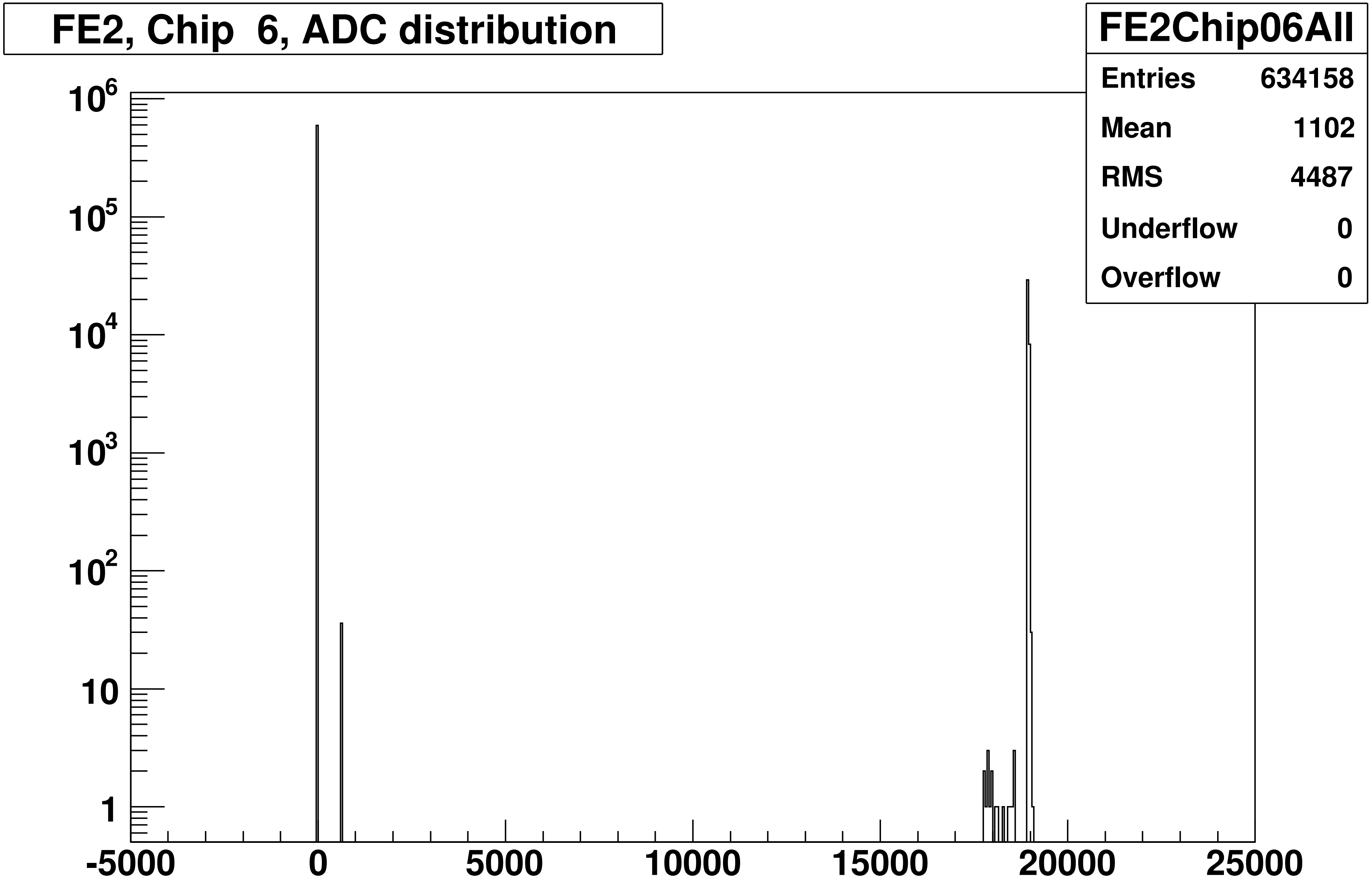
FE2, Chip 6, ADC distribution
FE2Chip06All
Entries 634158
Mean 1102
RMS 4487
Underflow 0
Overflow 0
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10^3
10^2
10
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-5000
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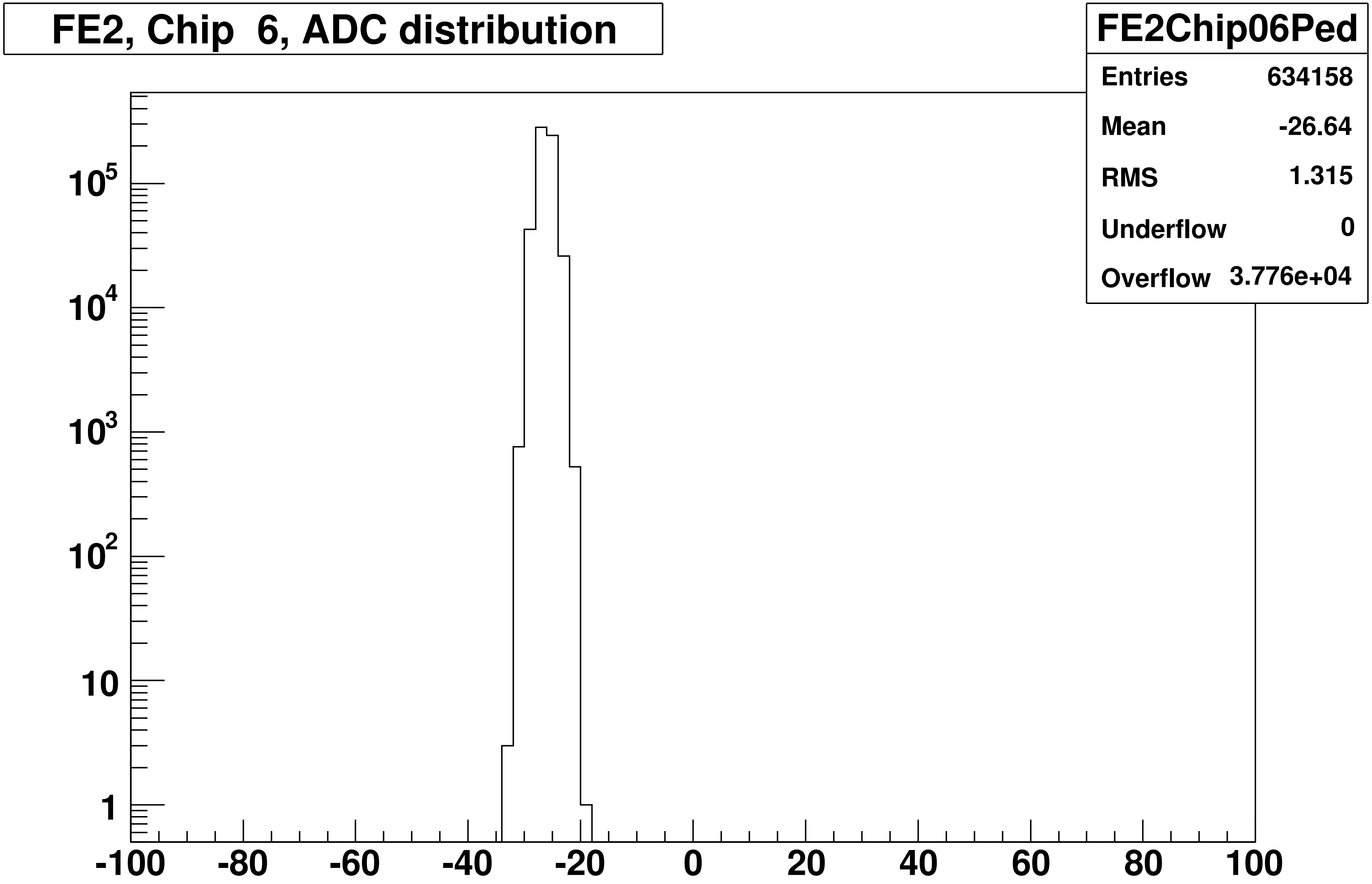
15000
20000
25000



FE2, Chip 6, ADC distribution
FE2Chip06Ped
Entries 634158
Mean -26.64
RMS 1.315
Underflow 0
Overflow 3.776e+04
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10^4
10^3
10^2
10
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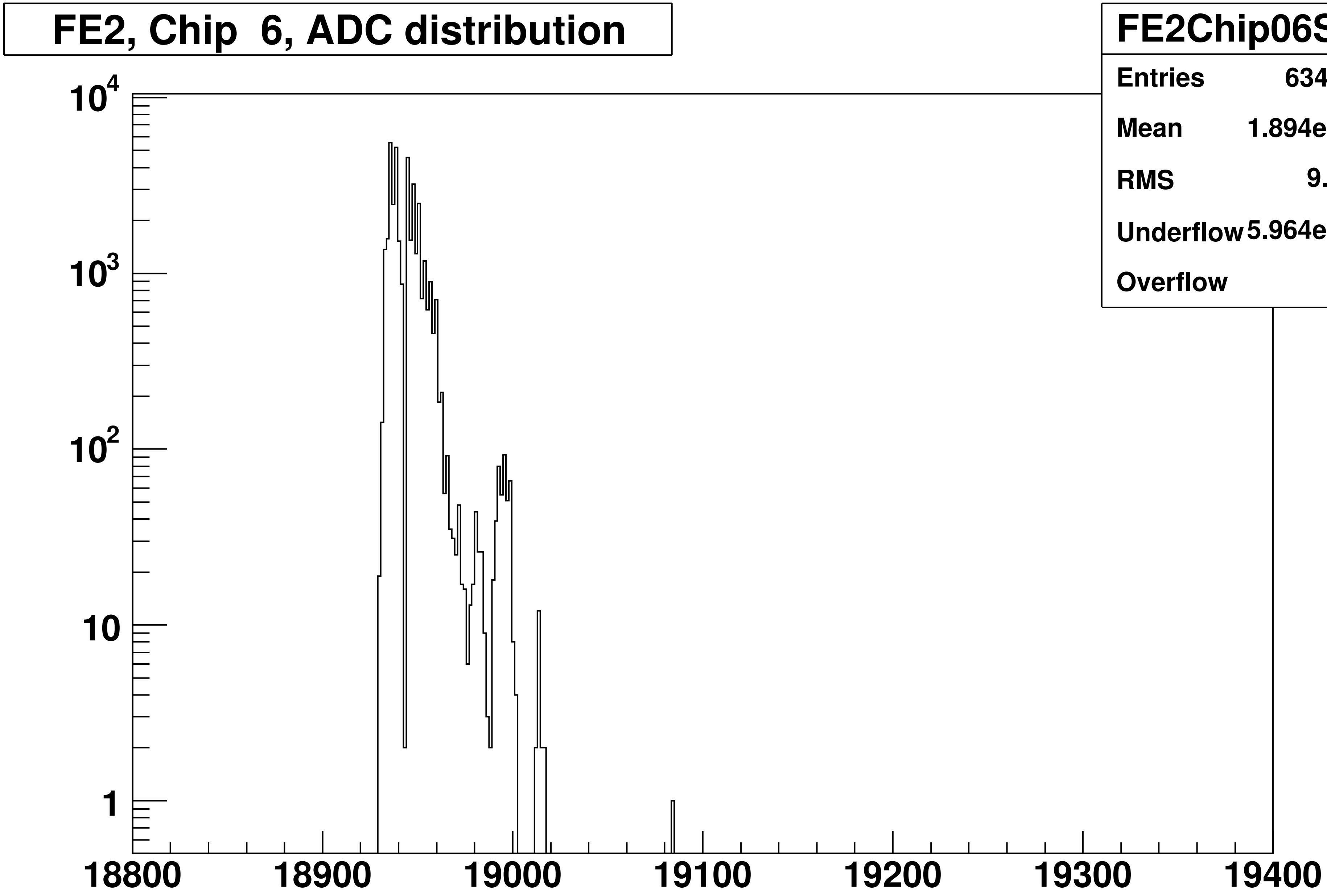

FE2, Chip 6, ADC distribution
FE2Chip06Sig
Entries 634158
Mean 1.894e+04
RMS 9.756
Underflow 5.964e+05
Overflow 0
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10^3
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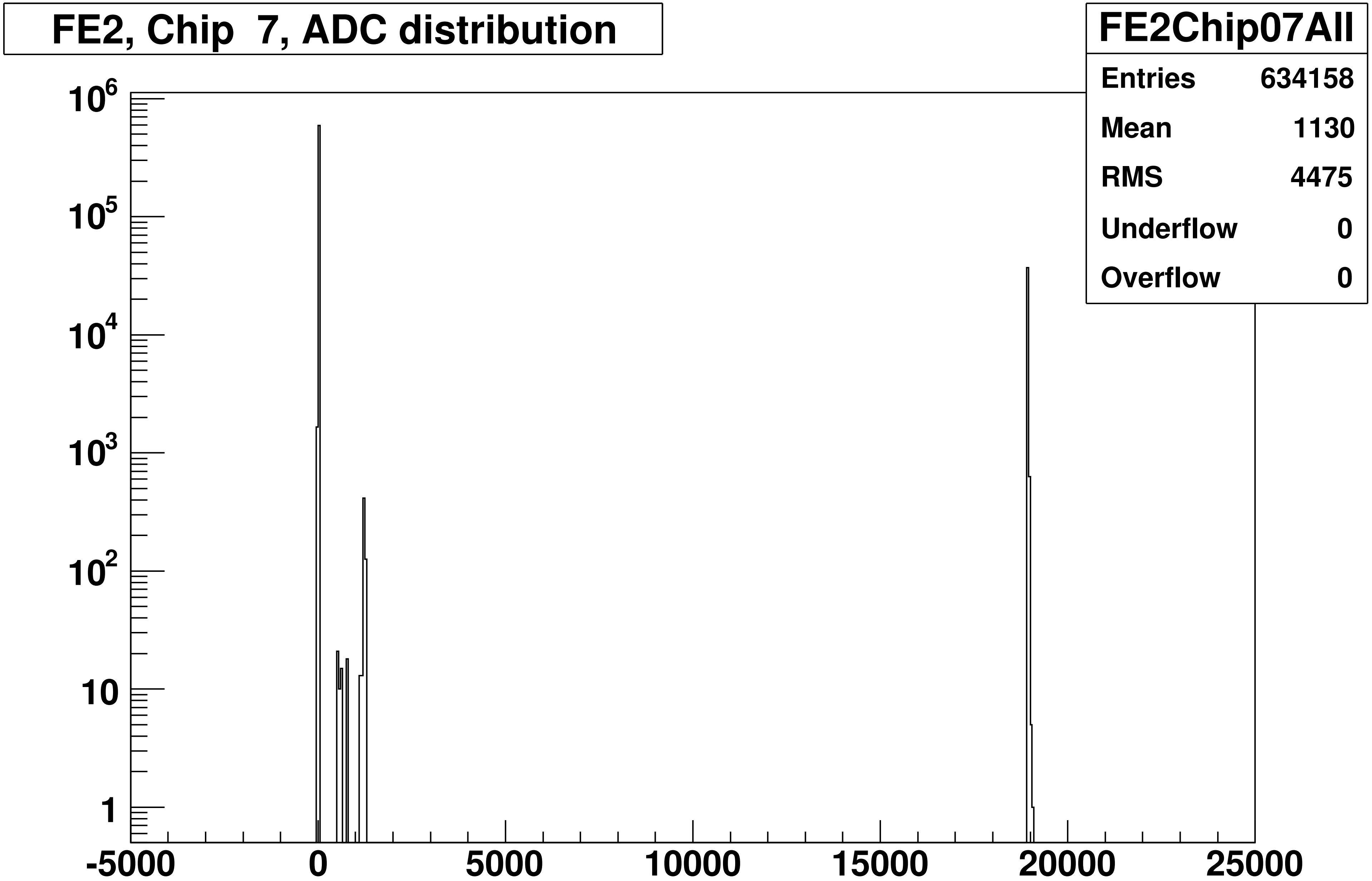
FE2, Chip 7, ADC distribution
FE2Chip07All
Entries 634158
Mean 1130
RMS 4475
Underflow 0
Overflow 0
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10^3
10^2
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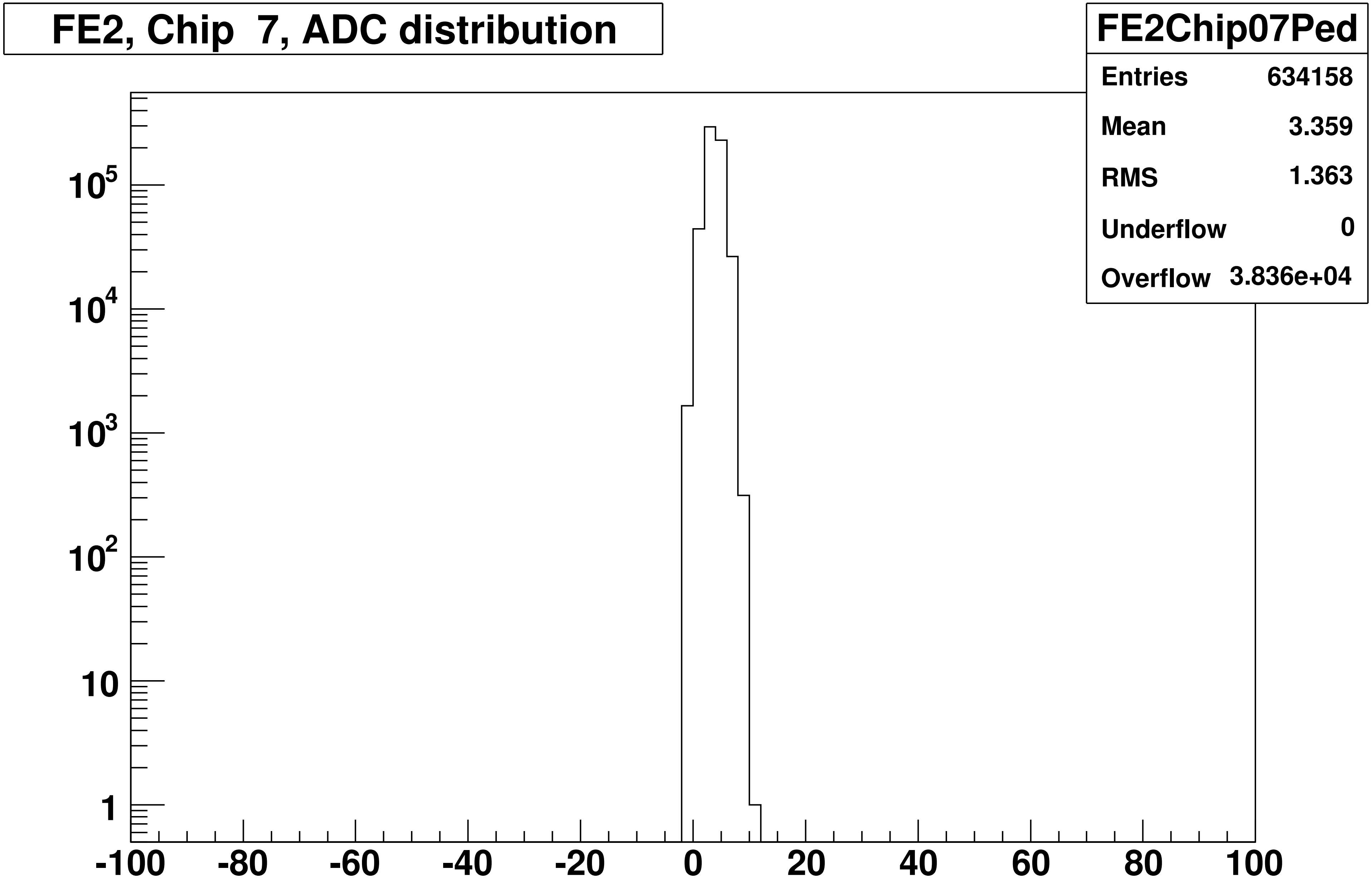
FE2, Chip 7, ADC distribution
FE2Chip07Ped
Entries 634158
Mean 3.359
RMS 1.363
Underflow 0
Overflow 3.836e+04
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10^2
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80
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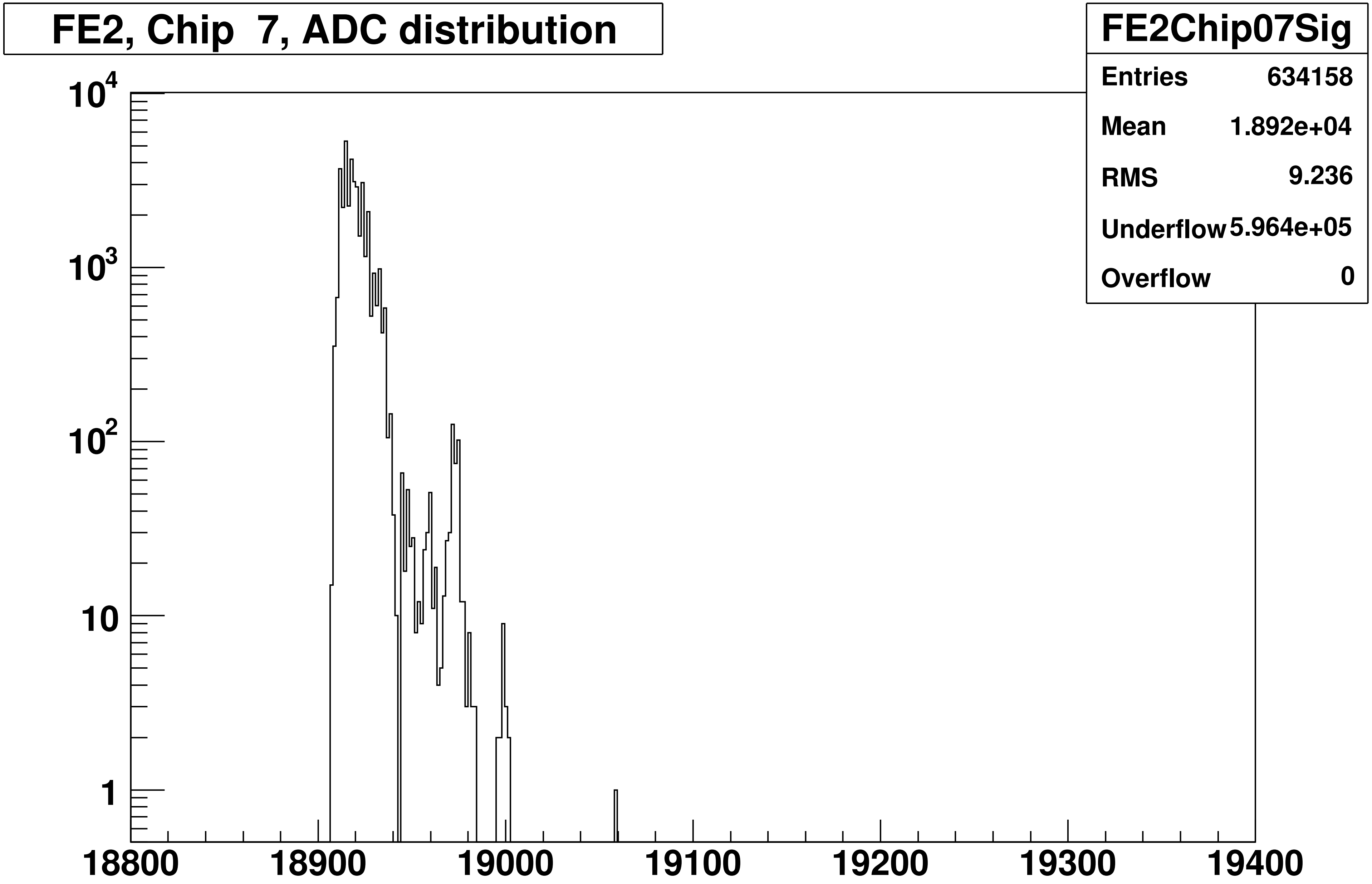
FE2, Chip 7, ADC distribution
FE2Chip07Sig
Entries 634158
Mean 1.892e+04
RMS 9.236
Underflow 5.964e+05
Overflow 0
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10^3
10^2
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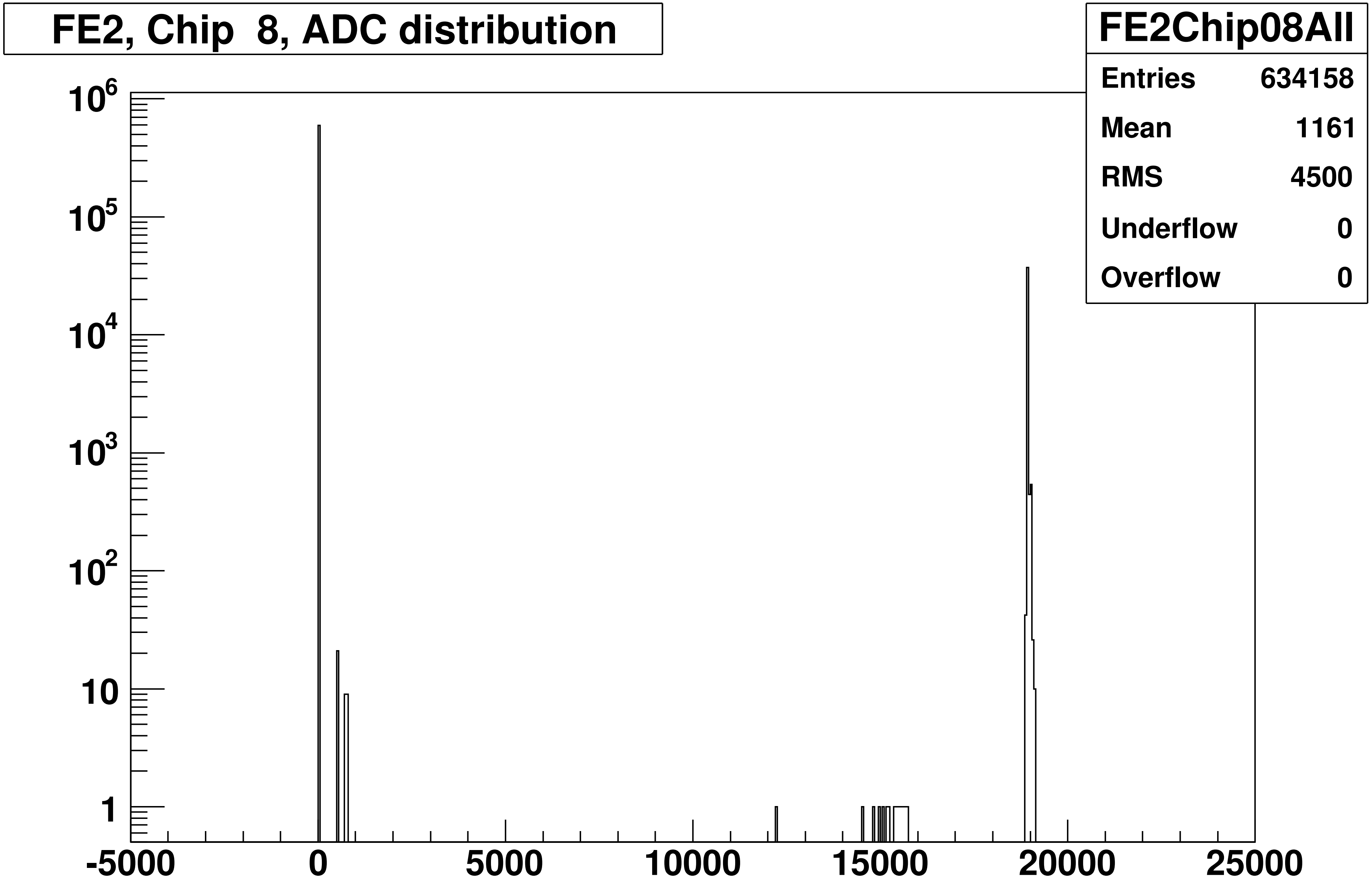
FE2, Chip 8, ADC distribution
FE2Chip08All
Entries 634158
Mean 1161
RMS 4500
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
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20000
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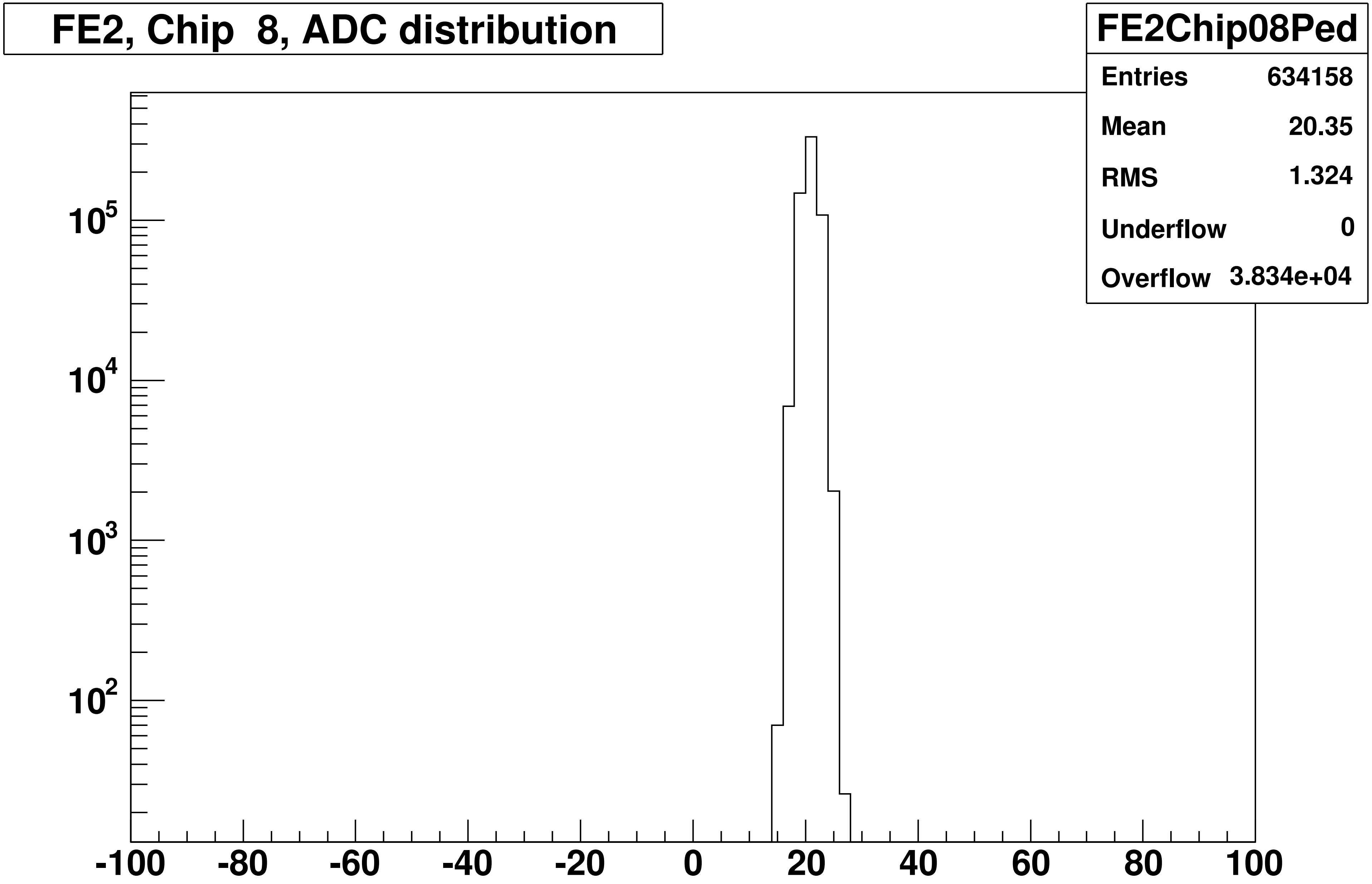
FE2, Chip 8, ADC distribution
FE2Chip08Ped
Entries 634158
Mean 20.35
RMS 1.324
Underflow 0
Overflow 3.834e+04
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10^3
10^2
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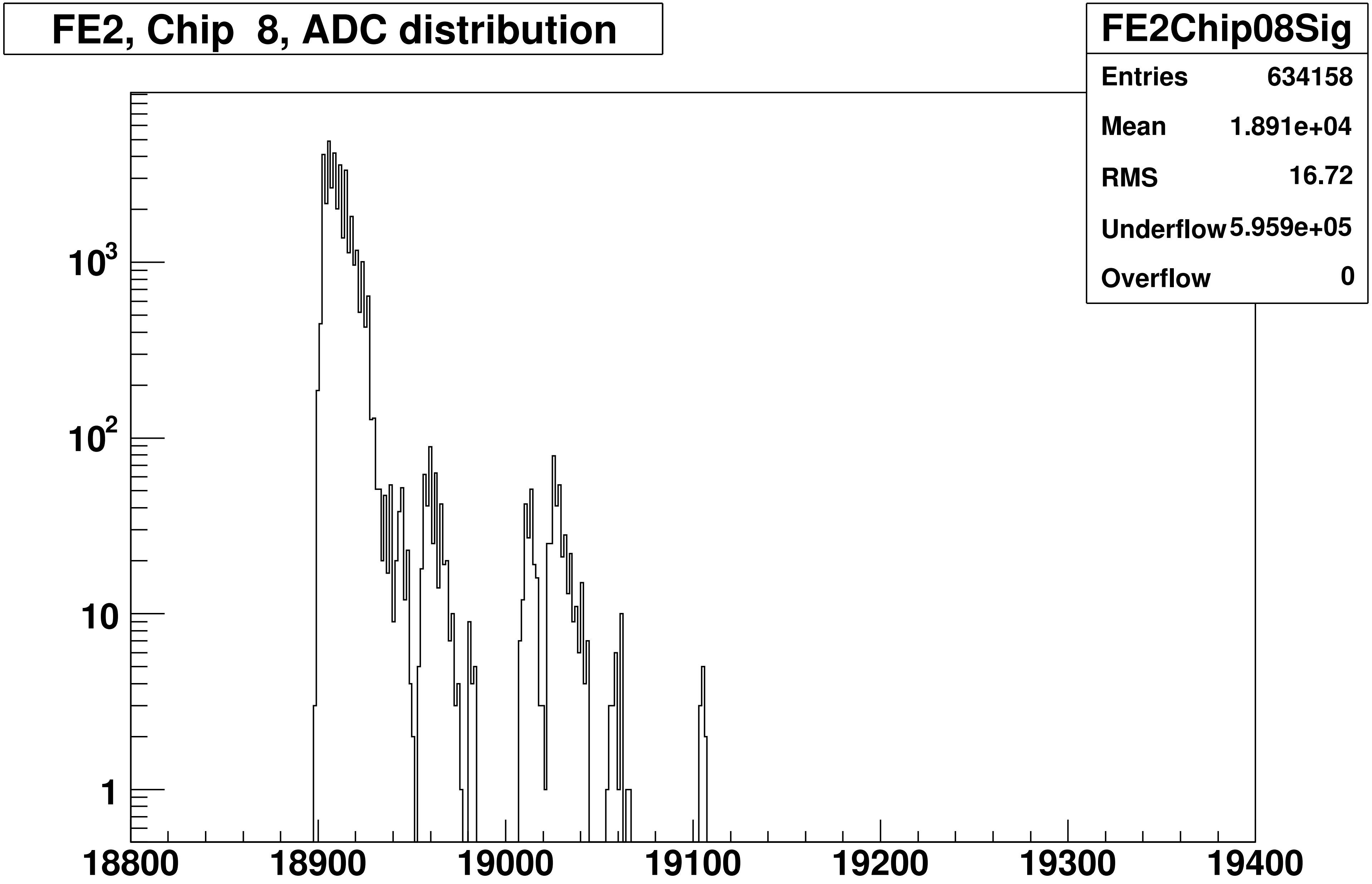
FE2, Chip 8, ADC distribution
FE2Chip08Sig
Entries 634158
Mean 1.891e+04
RMS 16.72
Underflow 5.959e+05
Overflow 0
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10^2
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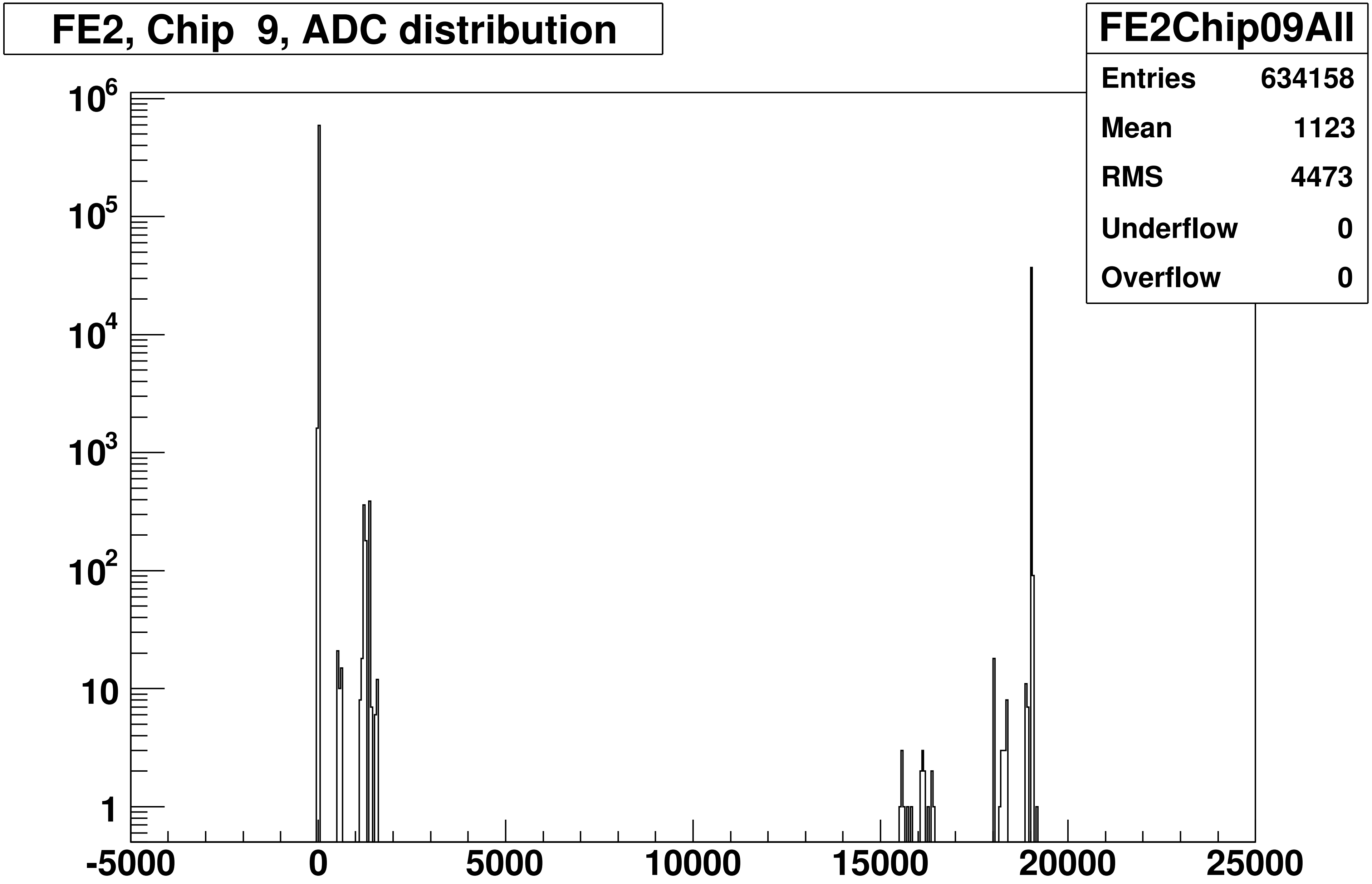

FE2, Chip 9, ADC distribution
FE2Chip09All
Entries 634158
Mean 1123
RMS 4473
Underflow 0
Overflow 0
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10^4
10^3
10^2
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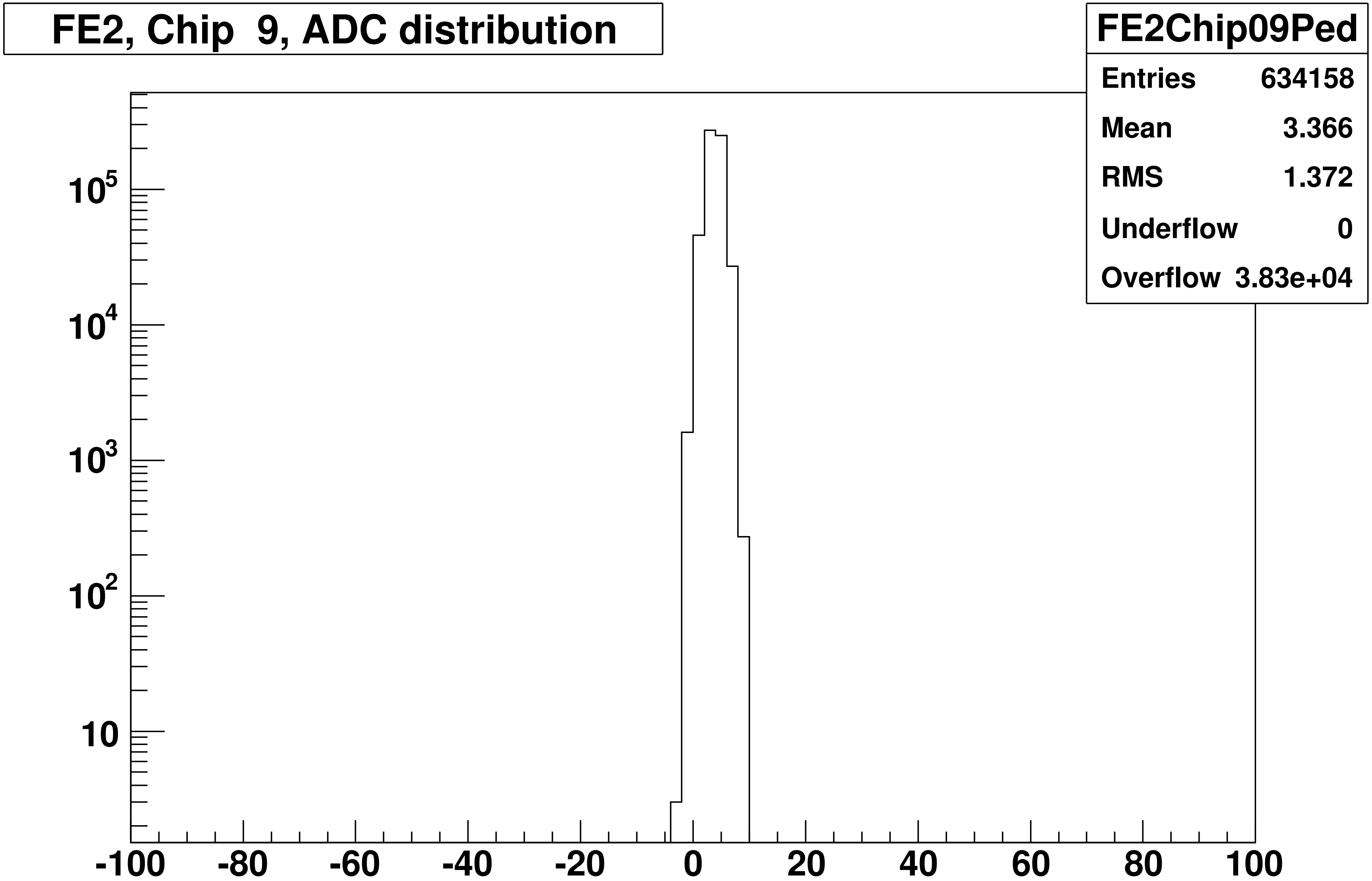
20000
25000


FE2, Chip 9, ADC distribution
FE2Chip09Ped
Entries 634158
Mean 3.366
RMS 1.372
Underflow 0
Overflow 3.83e+04
10^5
10^4
10^3
10^2
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-40
-20
0
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60
80
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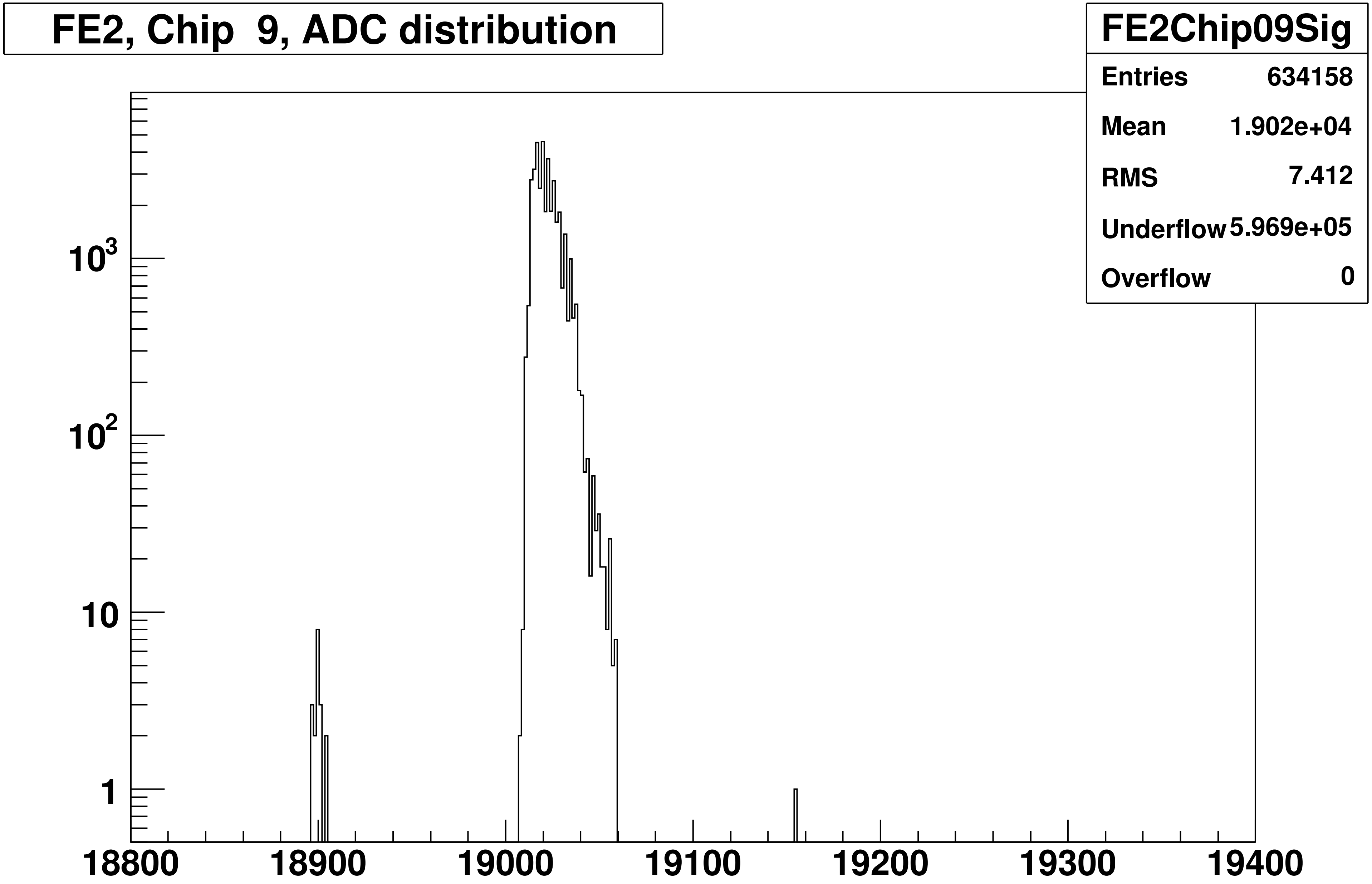
FE2, Chip 9, ADC distribution
FE2Chip09Sig
Entries 634158
Mean 1.902e+04
RMS 7.412
Underflow 5.969e+05
Overflow 0
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10^2
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18900
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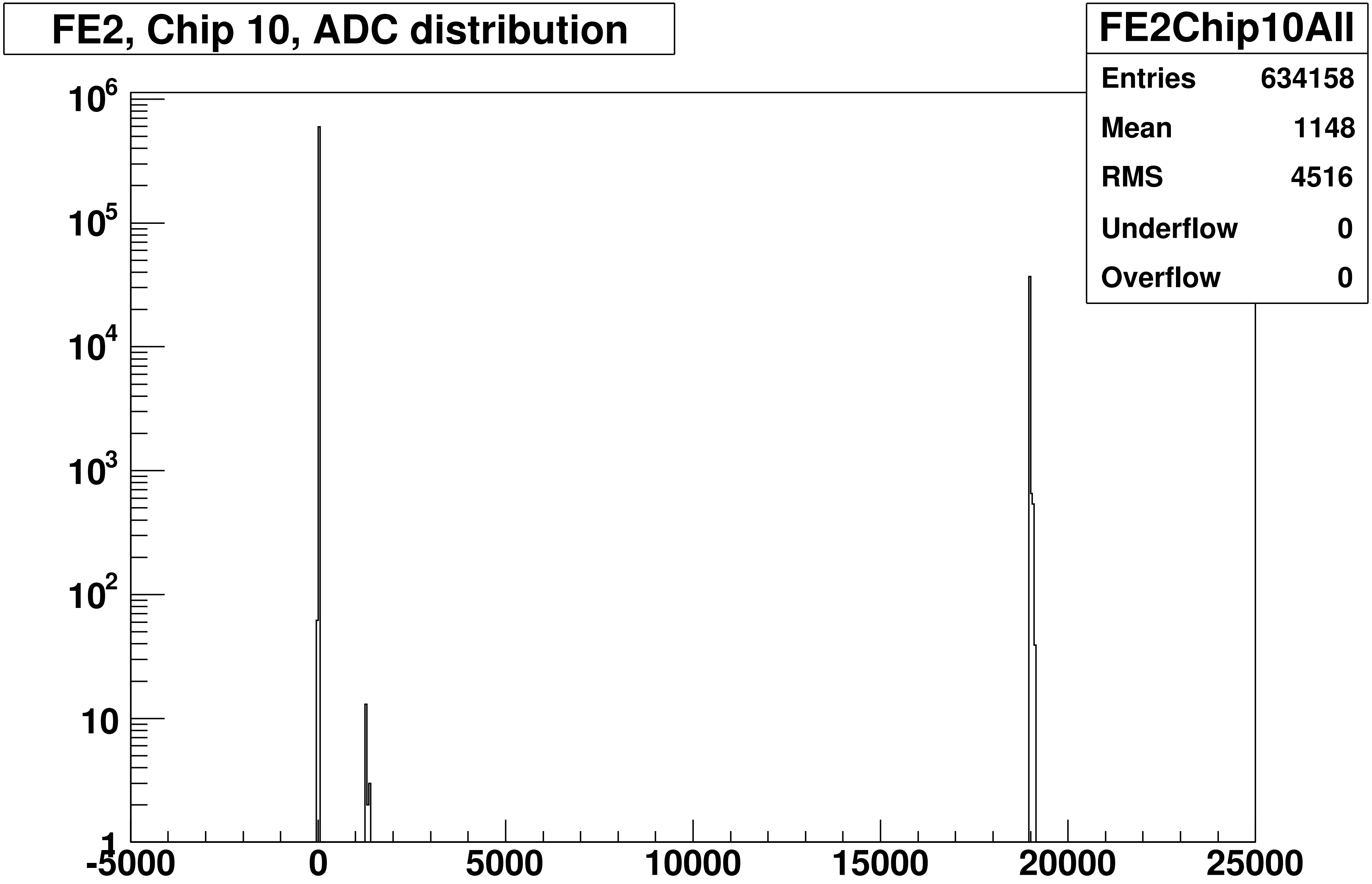

FE2, Chip 10, ADC distribution
FE2Chip10All
Entries 634158
Mean 1148
RMS 4516
Underflow 0
Overflow 0
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10^4
10^3
10^2
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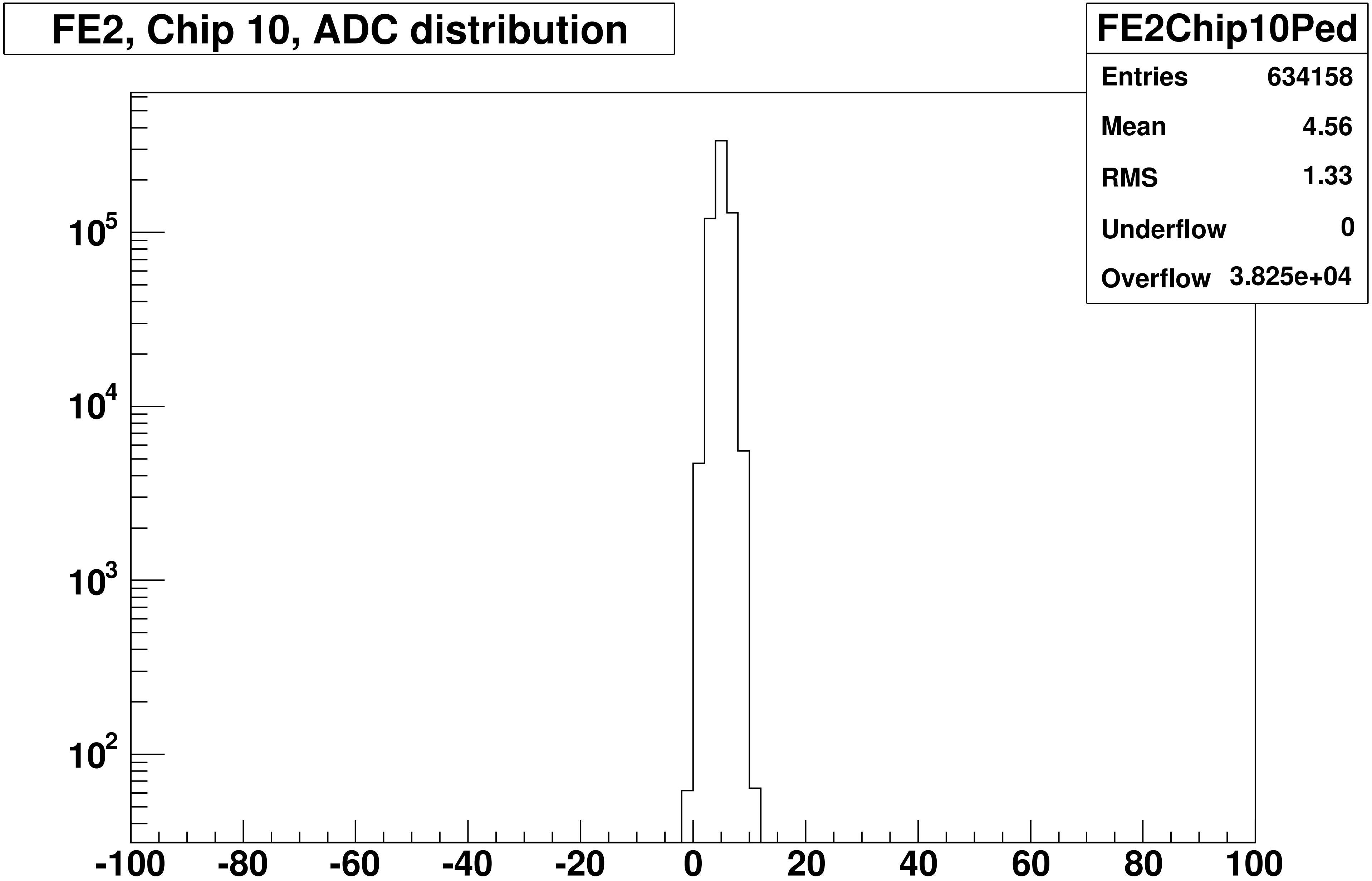
FE2, Chip 10, ADC distribution
FE2Chip10Ped
Entries 634158
Mean 4.56
RMS 1.33
Underflow 0
Overflow 3.825e+04
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10^3
10^2
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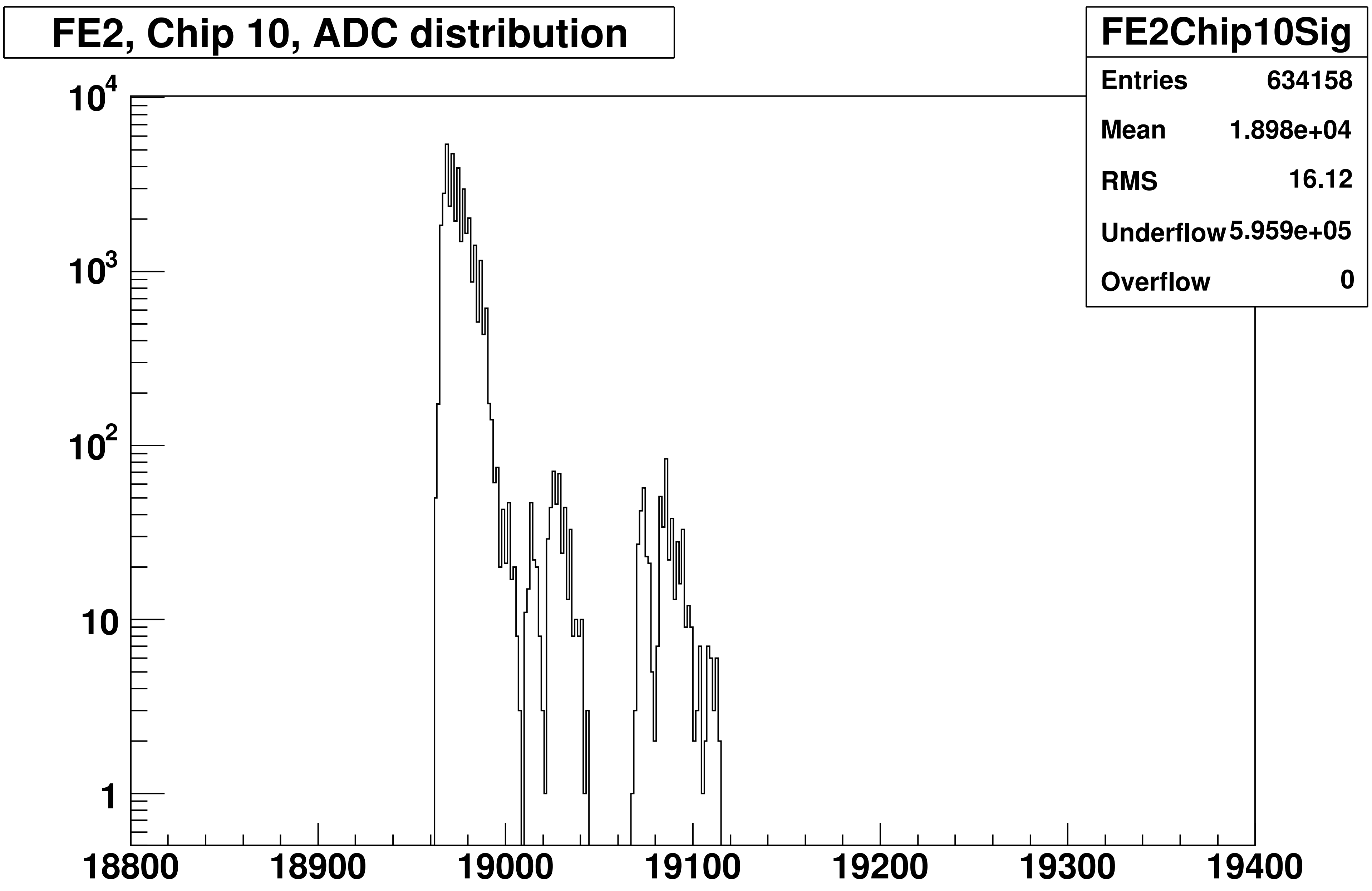
FE2, Chip 10, ADC distribution
FE2Chip10Sig
Entries 634158
Mean 1.898e+04
RMS 16.12
Underflow 5.959e+05
Overflow 0
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10^3
10^2
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18900
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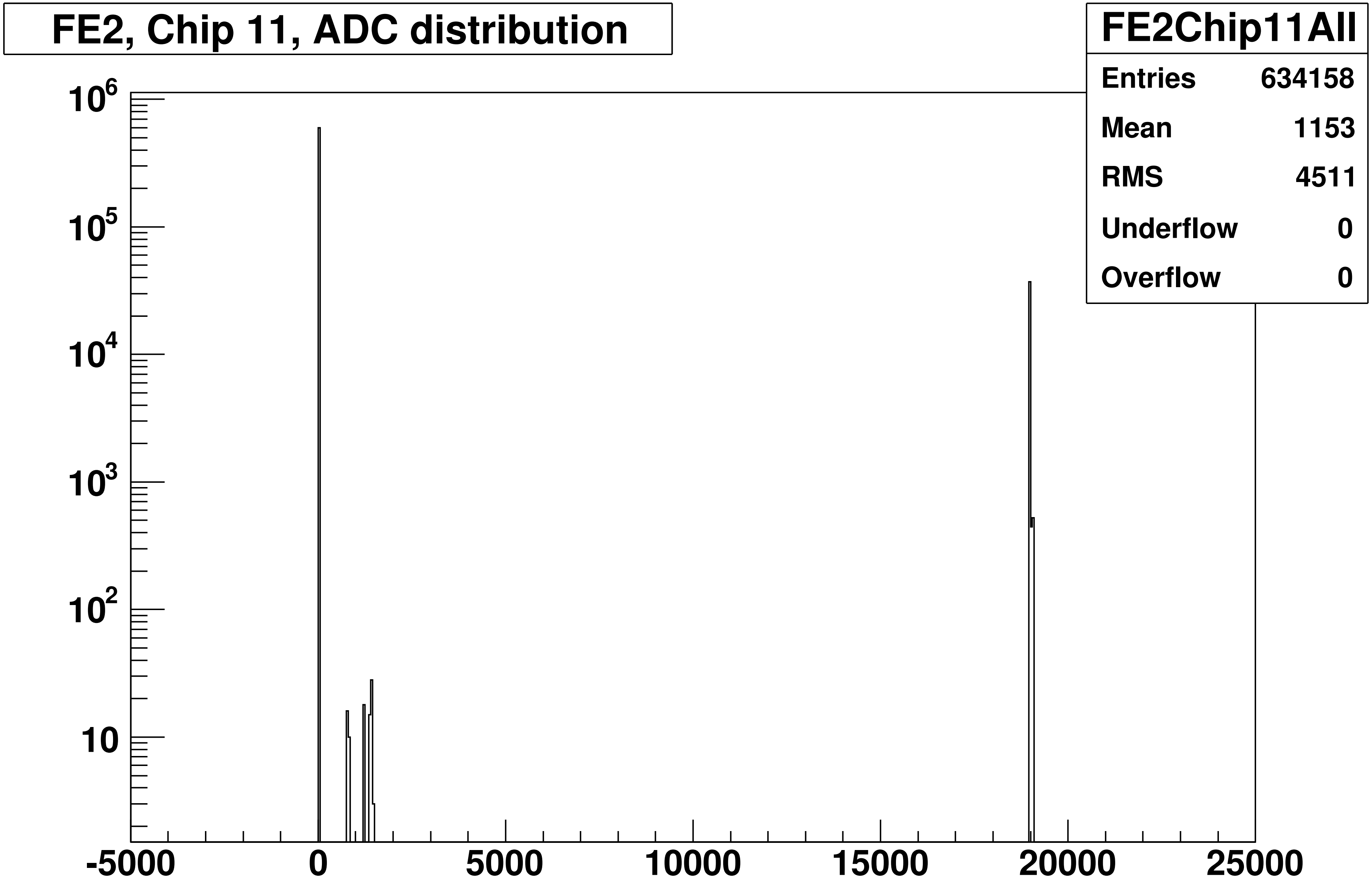
FE2, Chip 11, ADC distribution
FE2Chip11All
Entries 634158
Mean 1153
RMS 4511
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
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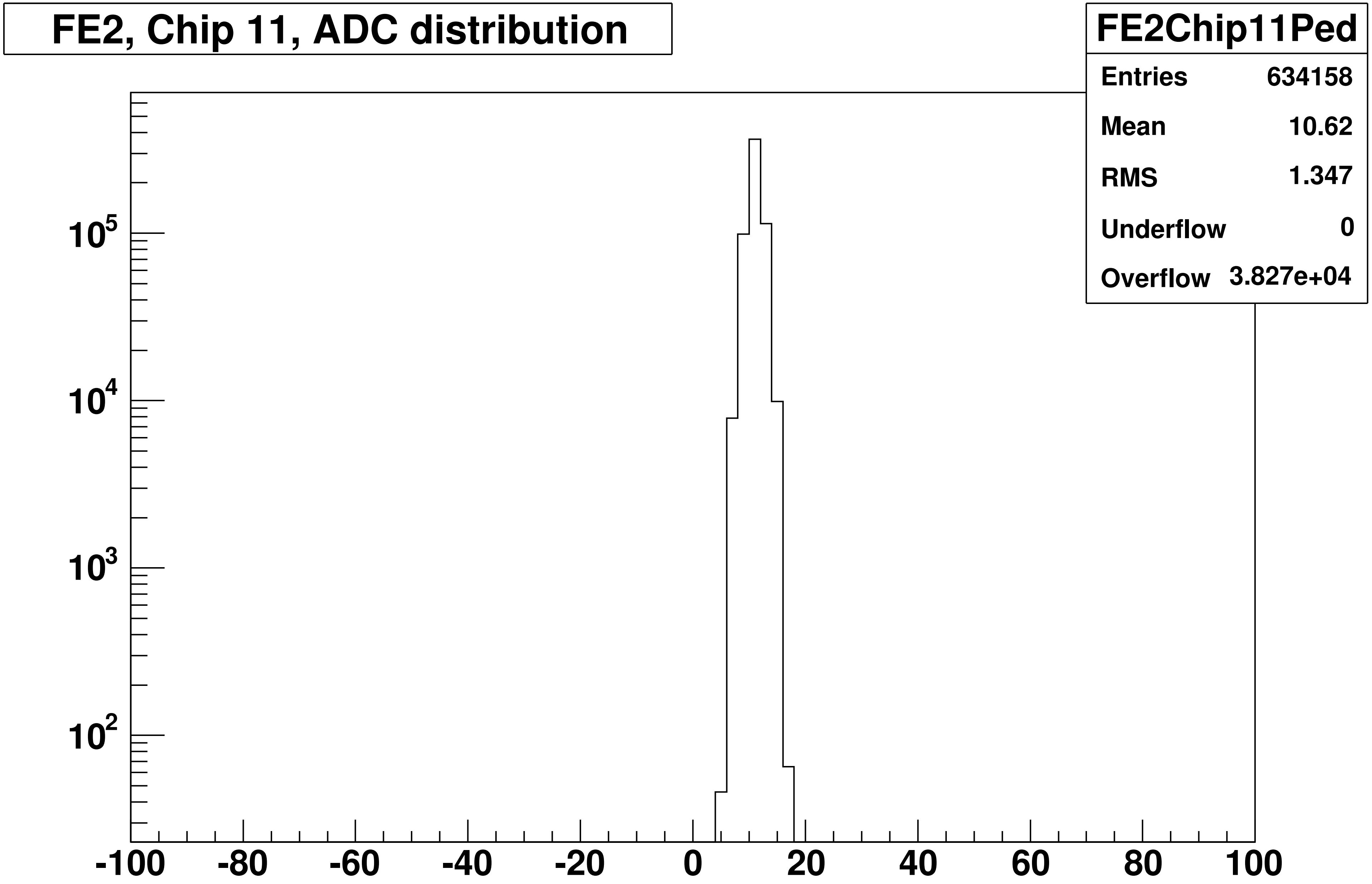
FE2, Chip 11, ADC distribution
FE2Chip11Ped
Entries 634158
Mean 10.62
RMS 1.347
Underflow 0
Overflow 3.827e+04
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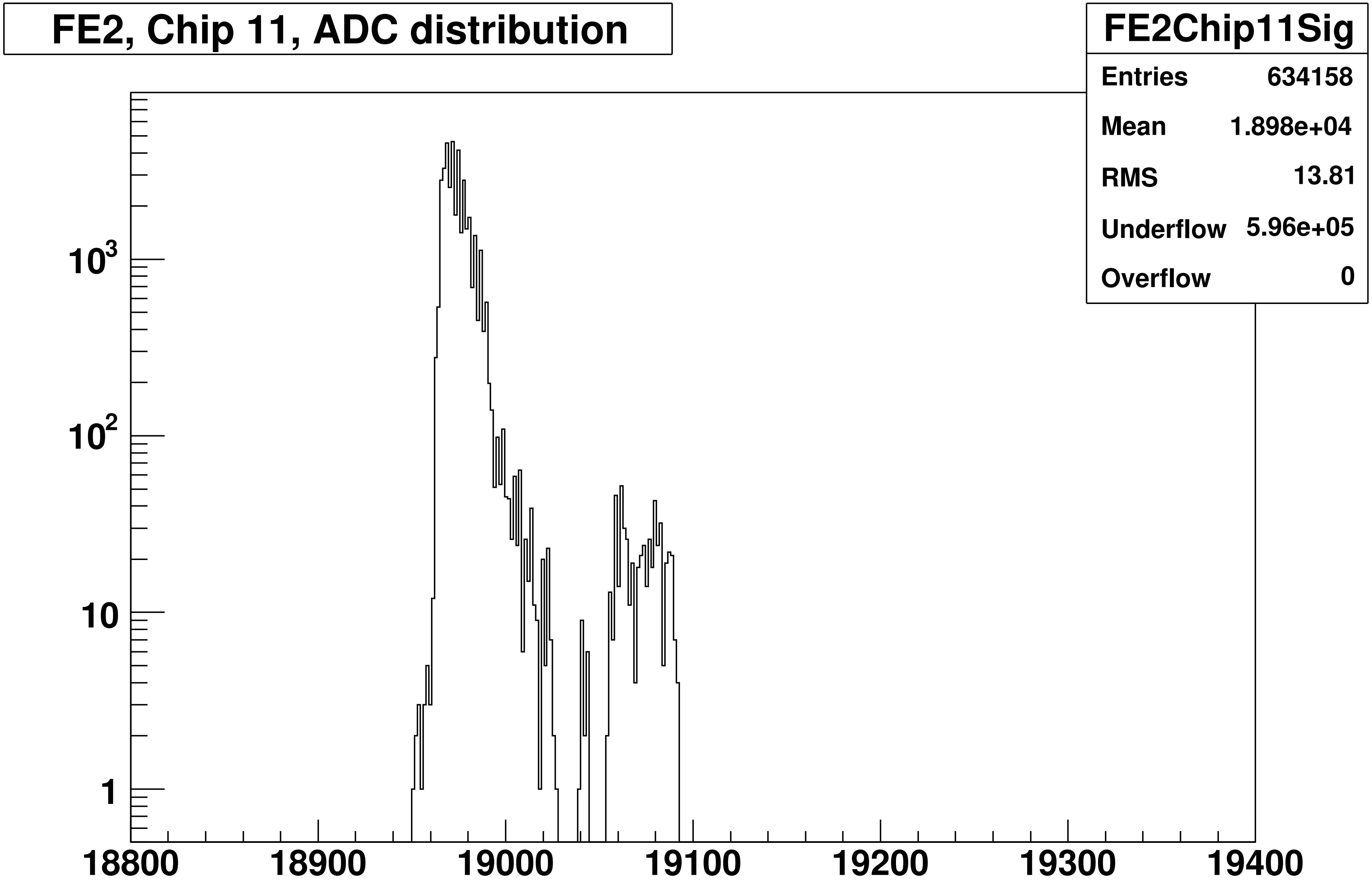
10^4
10^3
10^2
-100 -80 -60 -40 -20 0 20 40 60 80 100


FE2, Chip 11, ADC distribution
FE2Chip11Sig
Entries 634158
Mean 1.898e+04
RMS 13.81
Underflow 5.96e+05
Overflow 0
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10^2
10
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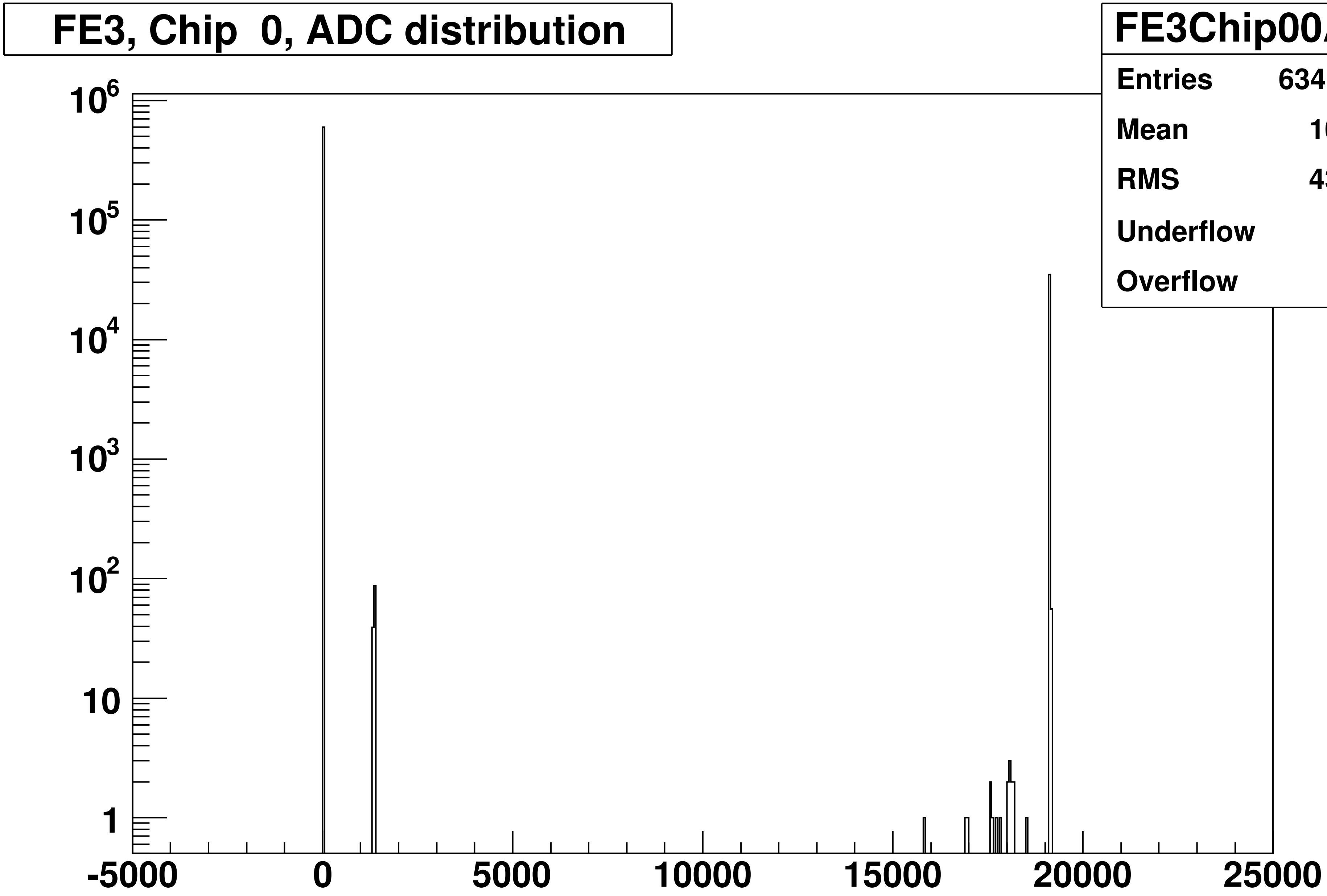
19400


FE3, Chip 0, ADC distribution
FE3Chip00All
Entries 634158
Mean 1073
RMS 4372
Underflow 0
Overflow 0
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10^3
10^2
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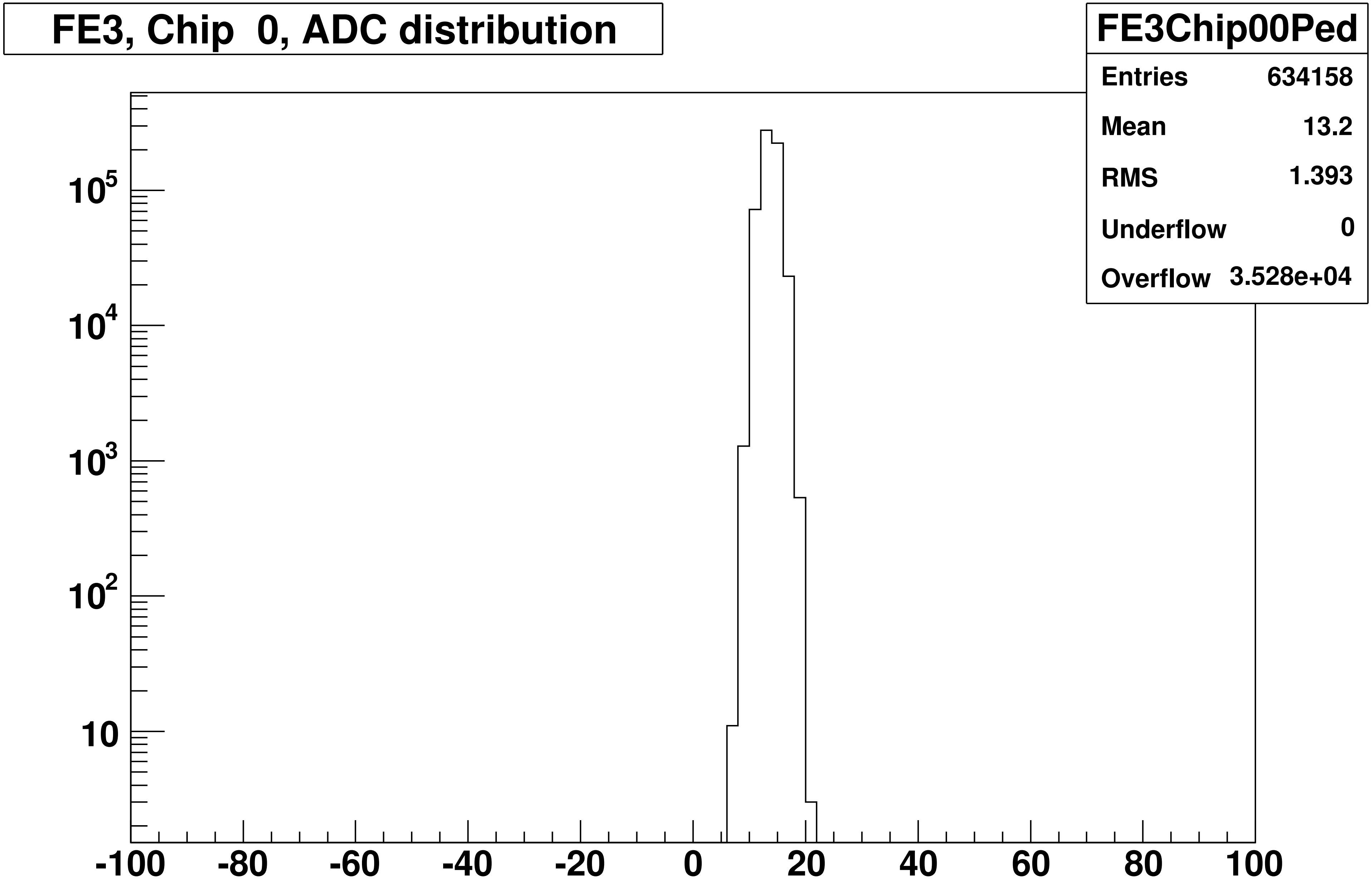
10000
15000
20000
25000


FE3, Chip 0, ADC distribution
FE3Chip00Ped
Entries 634158
Mean 13.2
RMS 1.393
Underflow 0
Overflow 3.528e+04
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10^3
10^2
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-40
-20
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80
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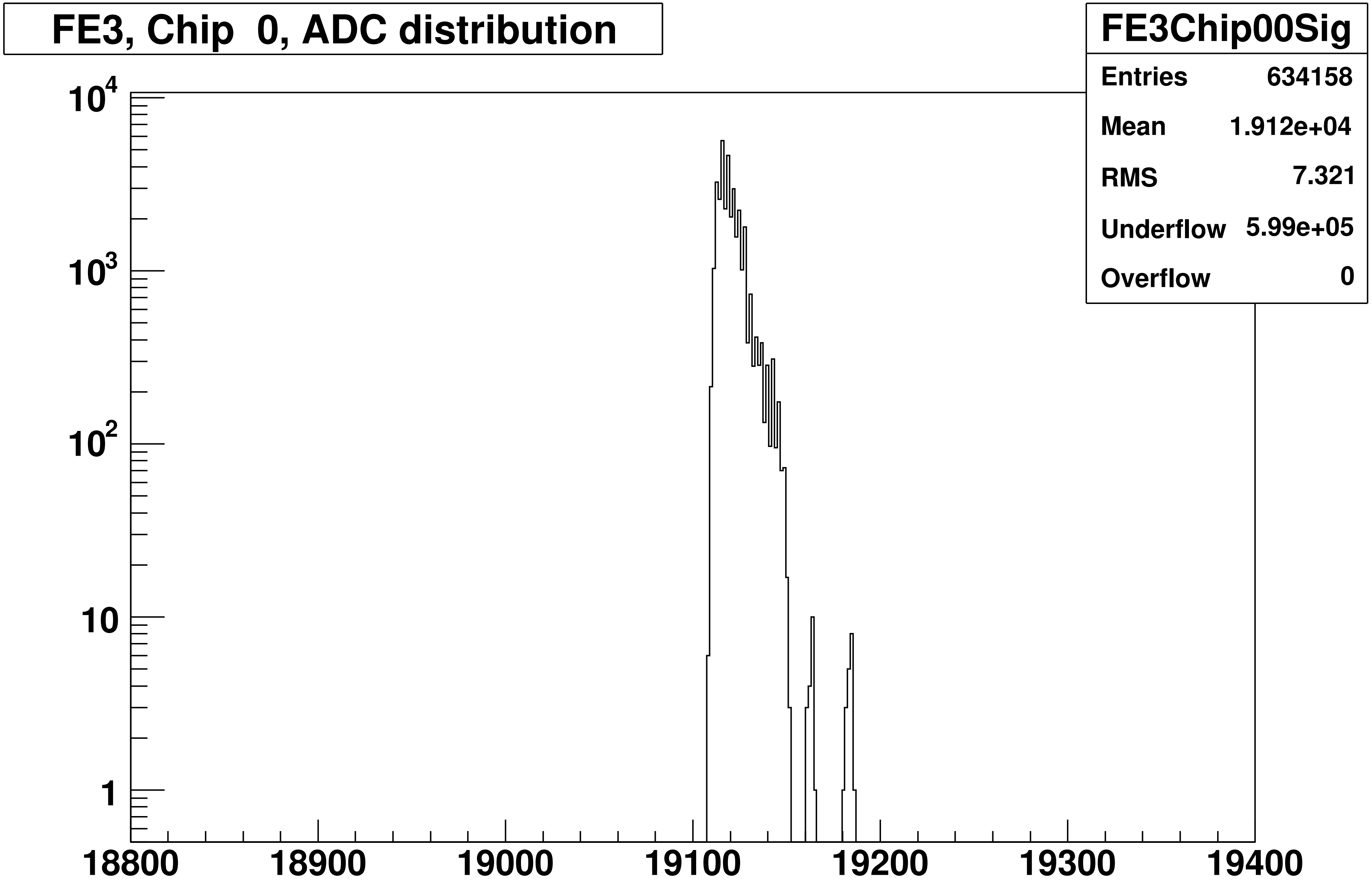
FE3, Chip 0, ADC distribution
FE3Chip00Sig
Entries 634158
Mean 1.912e+04
RMS 7.321
Underflow 5.99e+05
Overflow 0
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10^3
10^2
10
1
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18900
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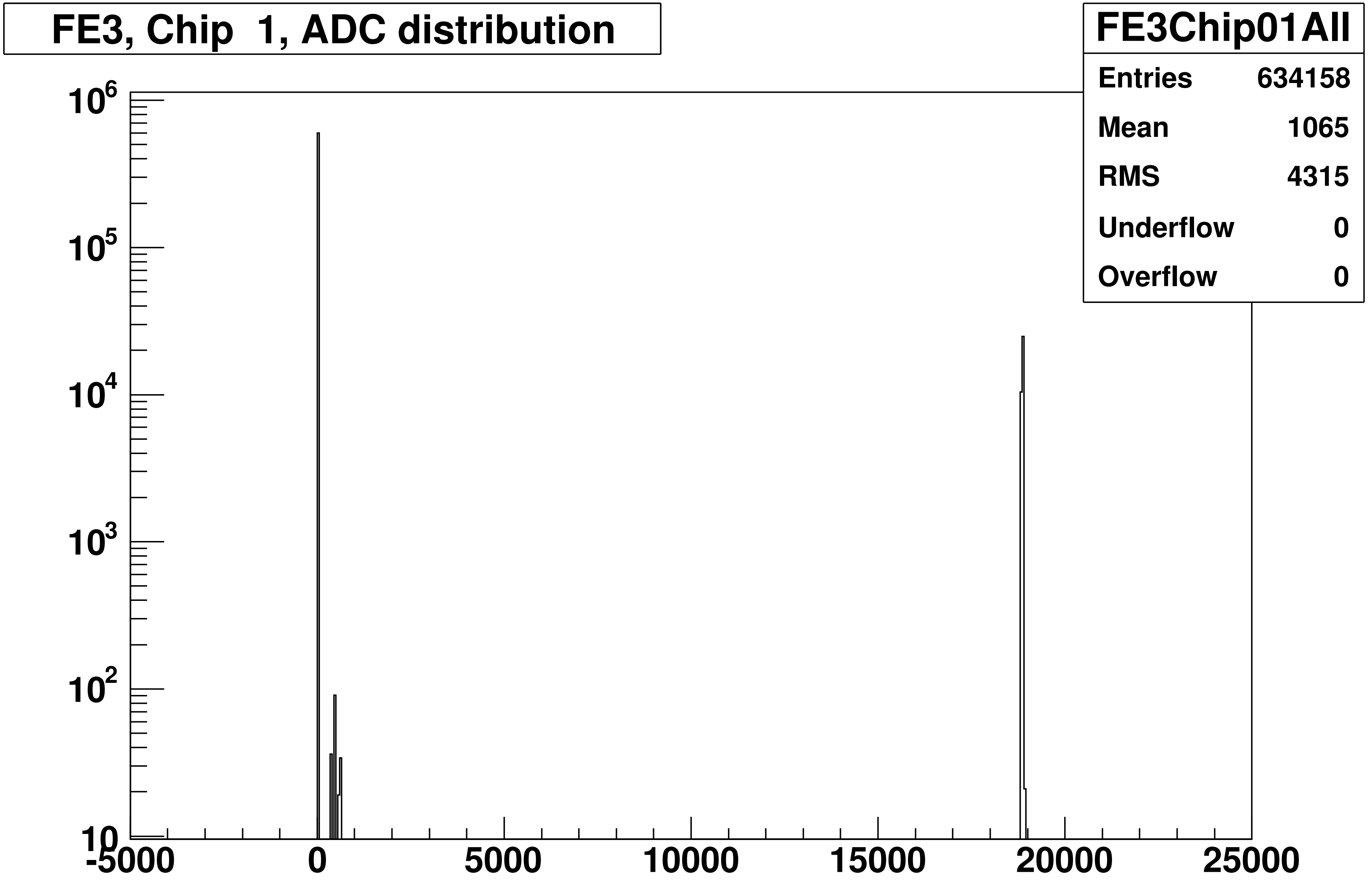
FE3, Chip 1, ADC distribution
FE3Chip01All
Entries 634158
Mean 1065
RMS 4315
Underflow 0
Overflow 0
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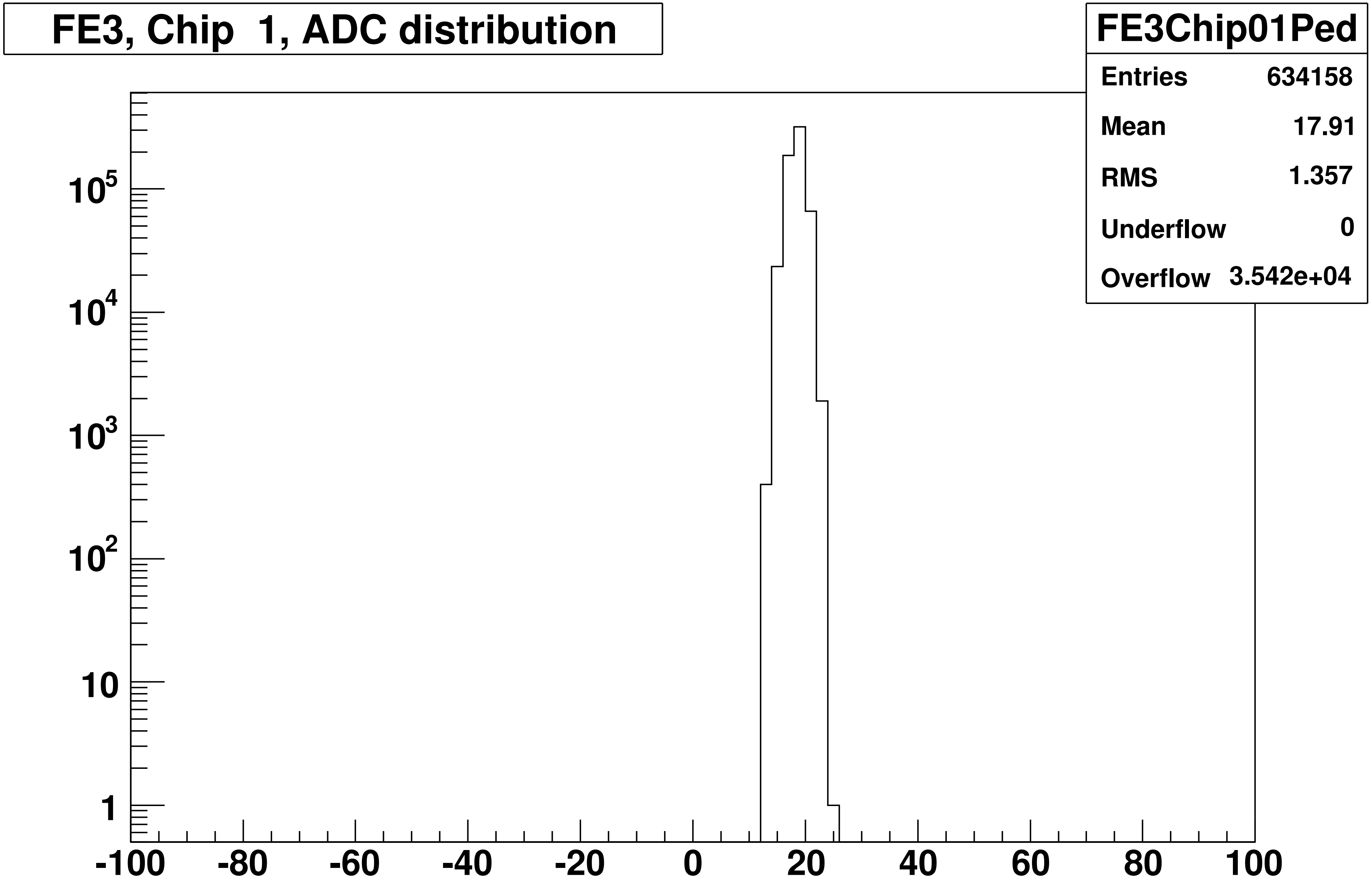
25000


FE3, Chip 1, ADC distribution
FE3Chip01Ped
Entries 634158
Mean 17.91
RMS 1.357
Underflow 0
Overflow 3.542e+04
10^5
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10^3
10^2
10
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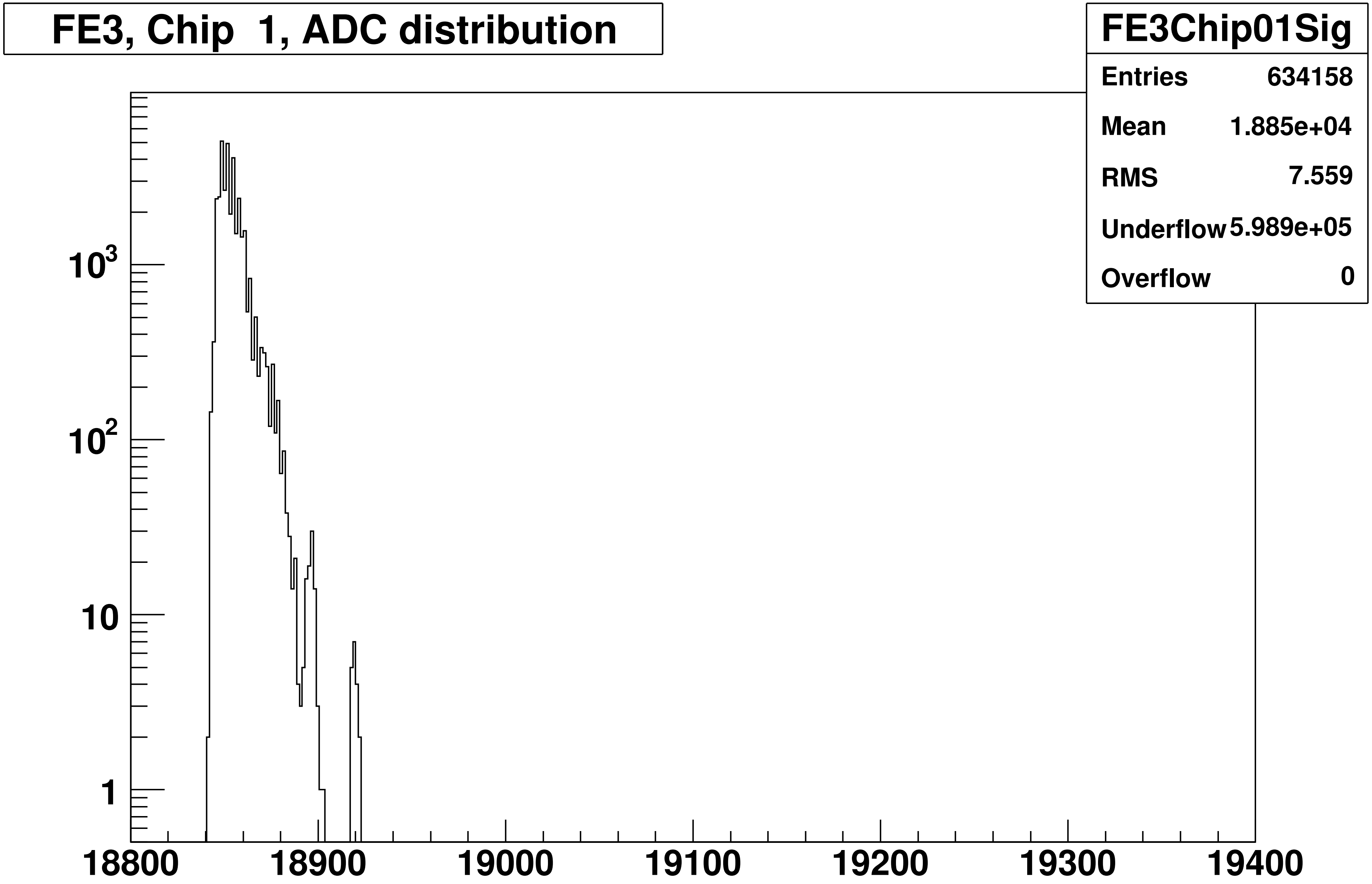
-100 -80 -60 -40 -20 0 20 40 60 80 100


FE3, Chip 1, ADC distribution
FE3Chip01Sig
Entries 634158
Mean 1.885e+04
RMS 7.559
Underflow 5.989e+05
Overflow 0
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10^2
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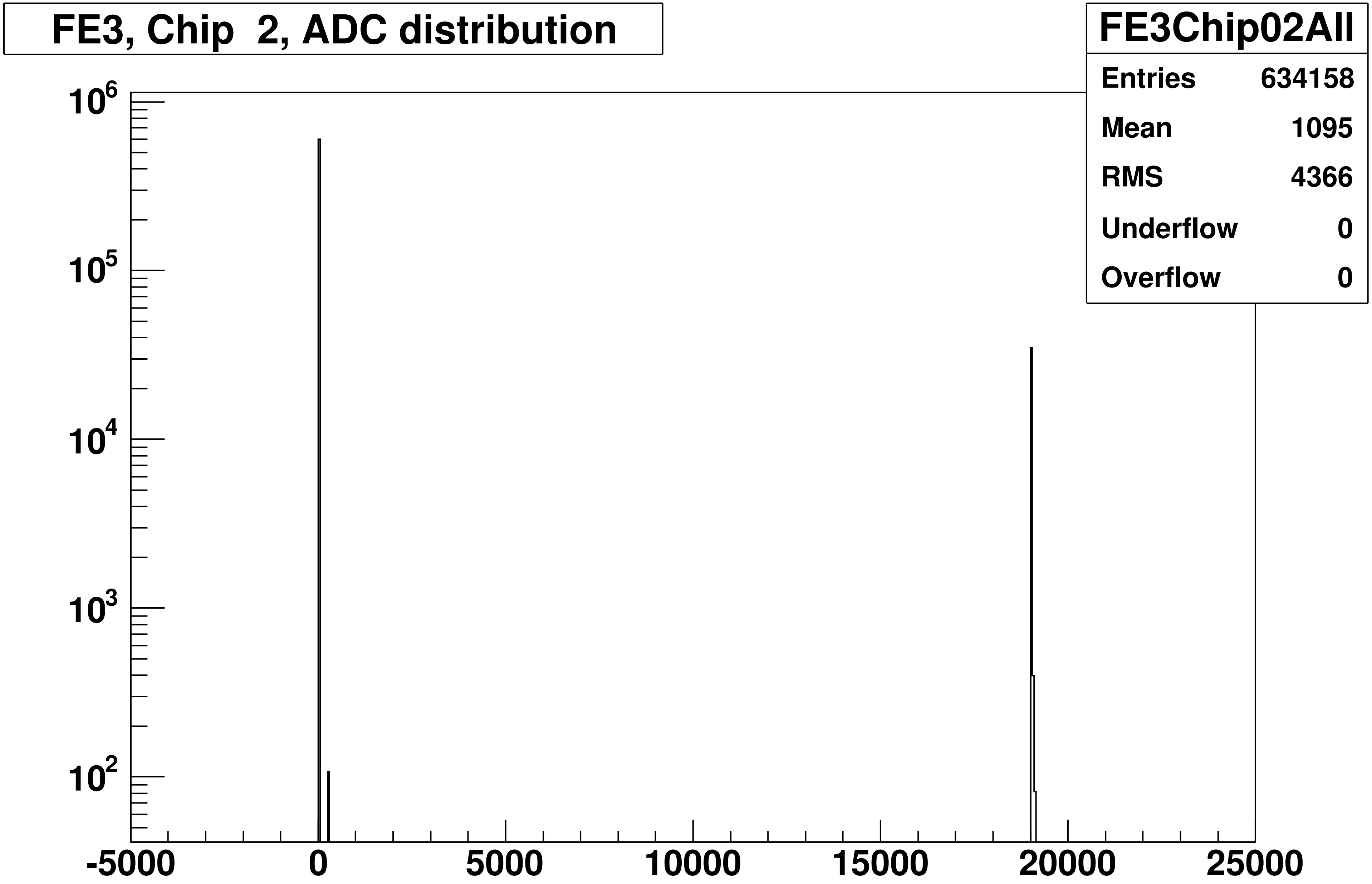
FE3, Chip 2, ADC distribution
FE3Chip02All
Entries 634158
Mean 1095
RMS 4366
Underflow 0
Overflow 0
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10^5
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10^2
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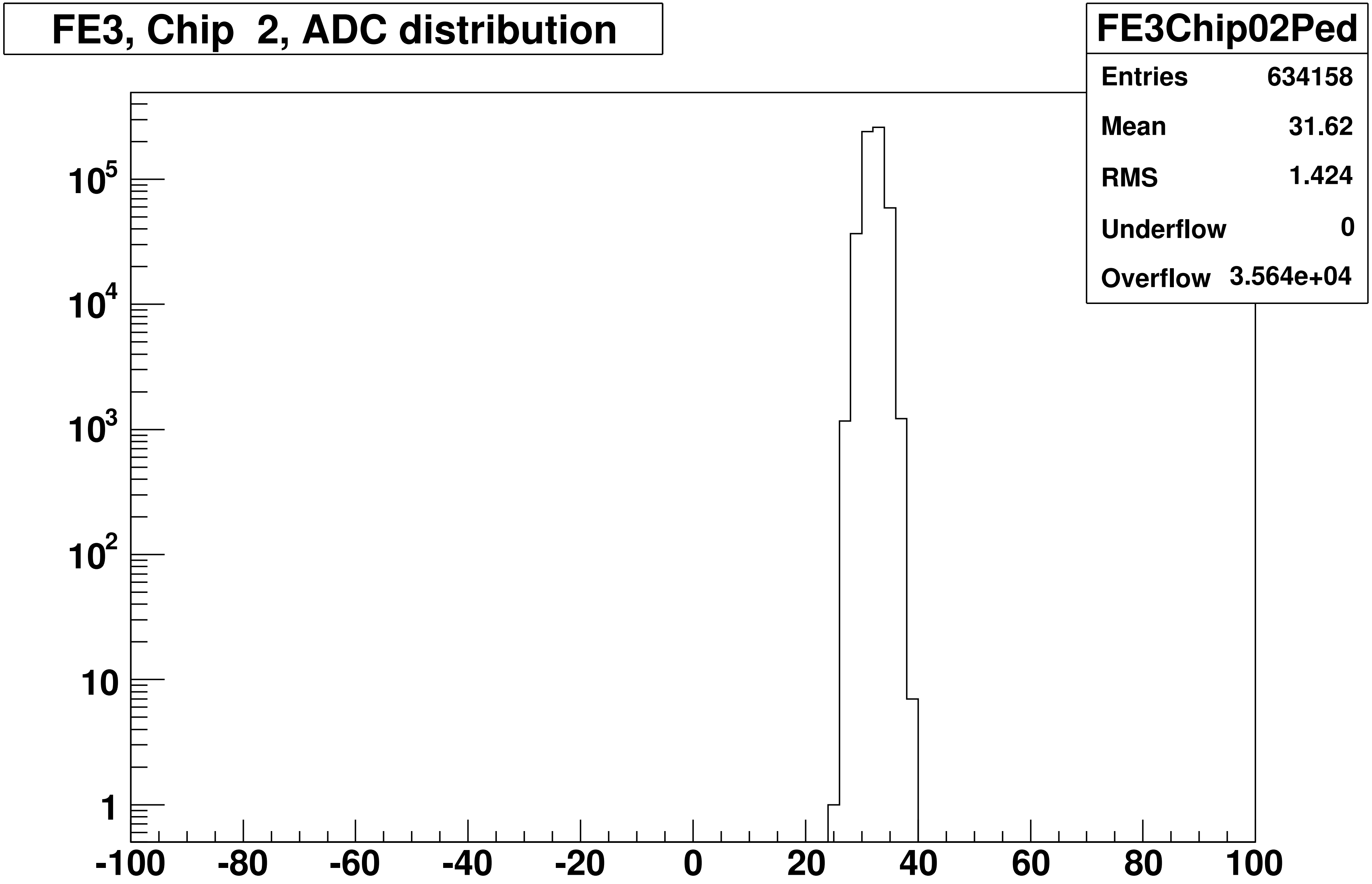
25000



FE3, Chip 2, ADC distribution
FE3Chip02Ped
Entries 634158
Mean 31.62
RMS 1.424
Underflow 0
Overflow 3.564e+04
10^5
10^4
10^3
10^2
10
1
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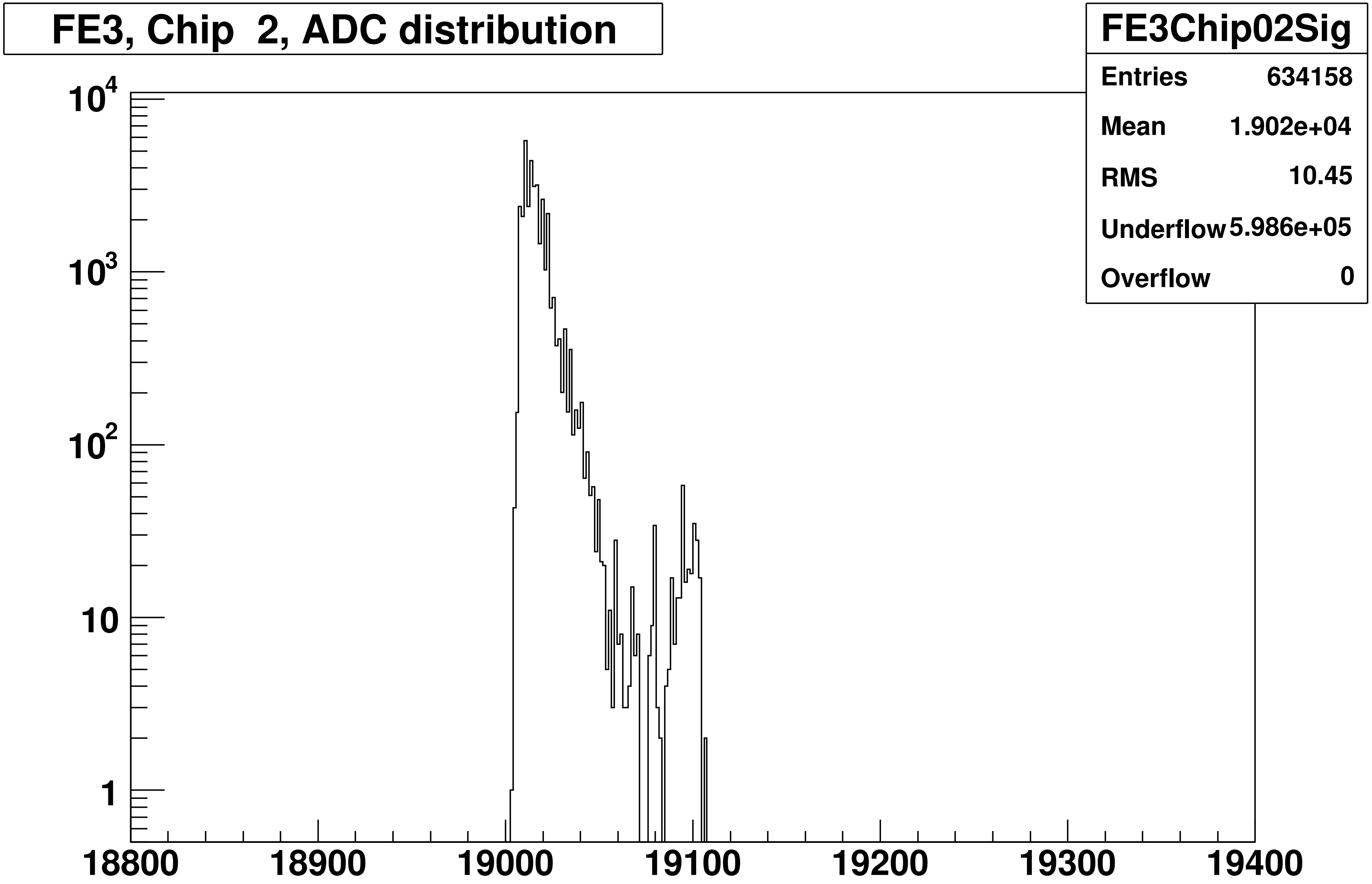
FE3, Chip 2, ADC distribution
FE3Chip02Sig
Entries 634158
Mean 1.902e+04
RMS 10.45
Underflow 5.986e+05
Overflow 0
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10^3
10^2
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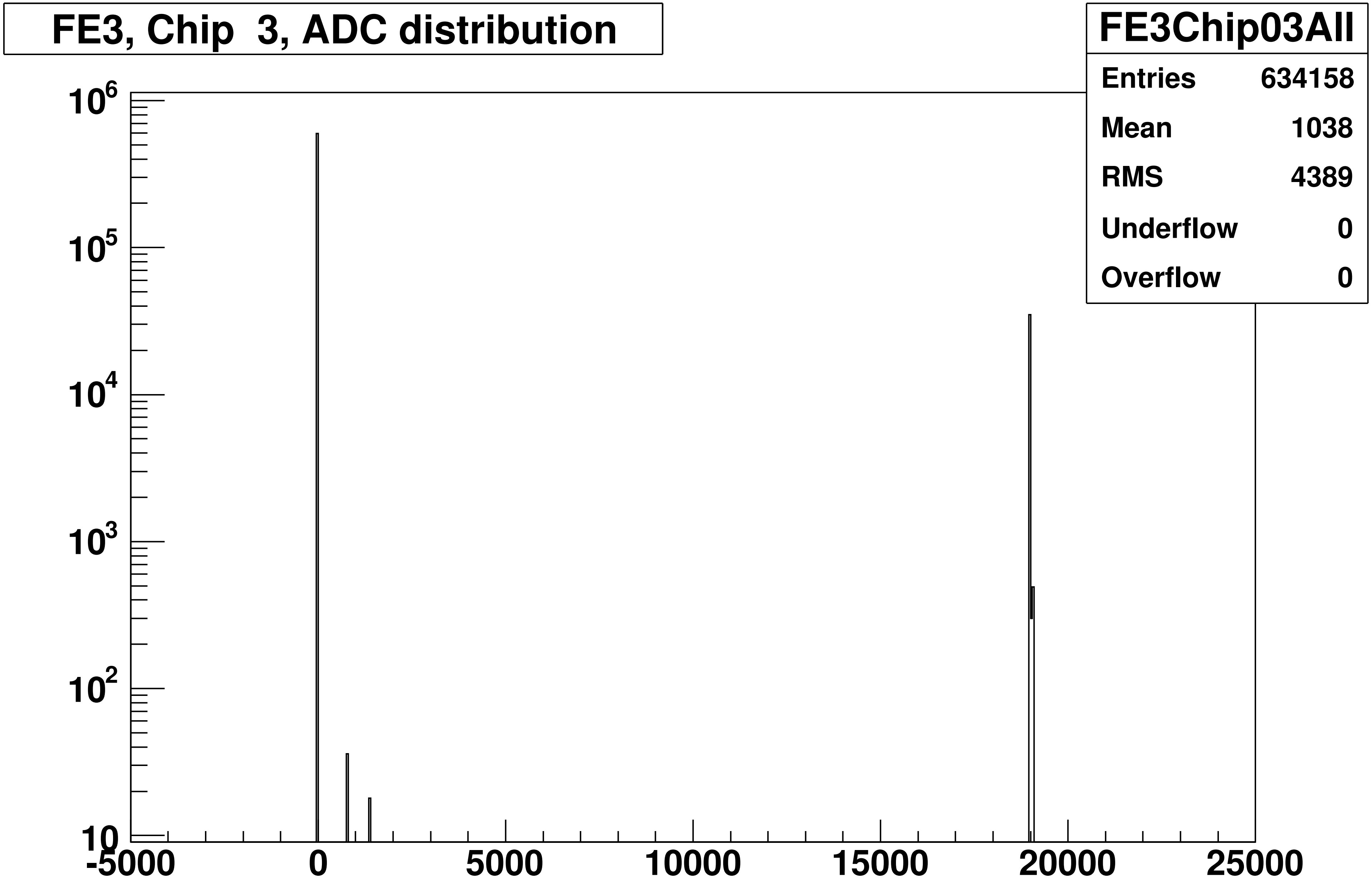
FE3, Chip 3, ADC distribution
FE3Chip03All
Entries 634158
Mean 1038
RMS 4389
Underflow 0
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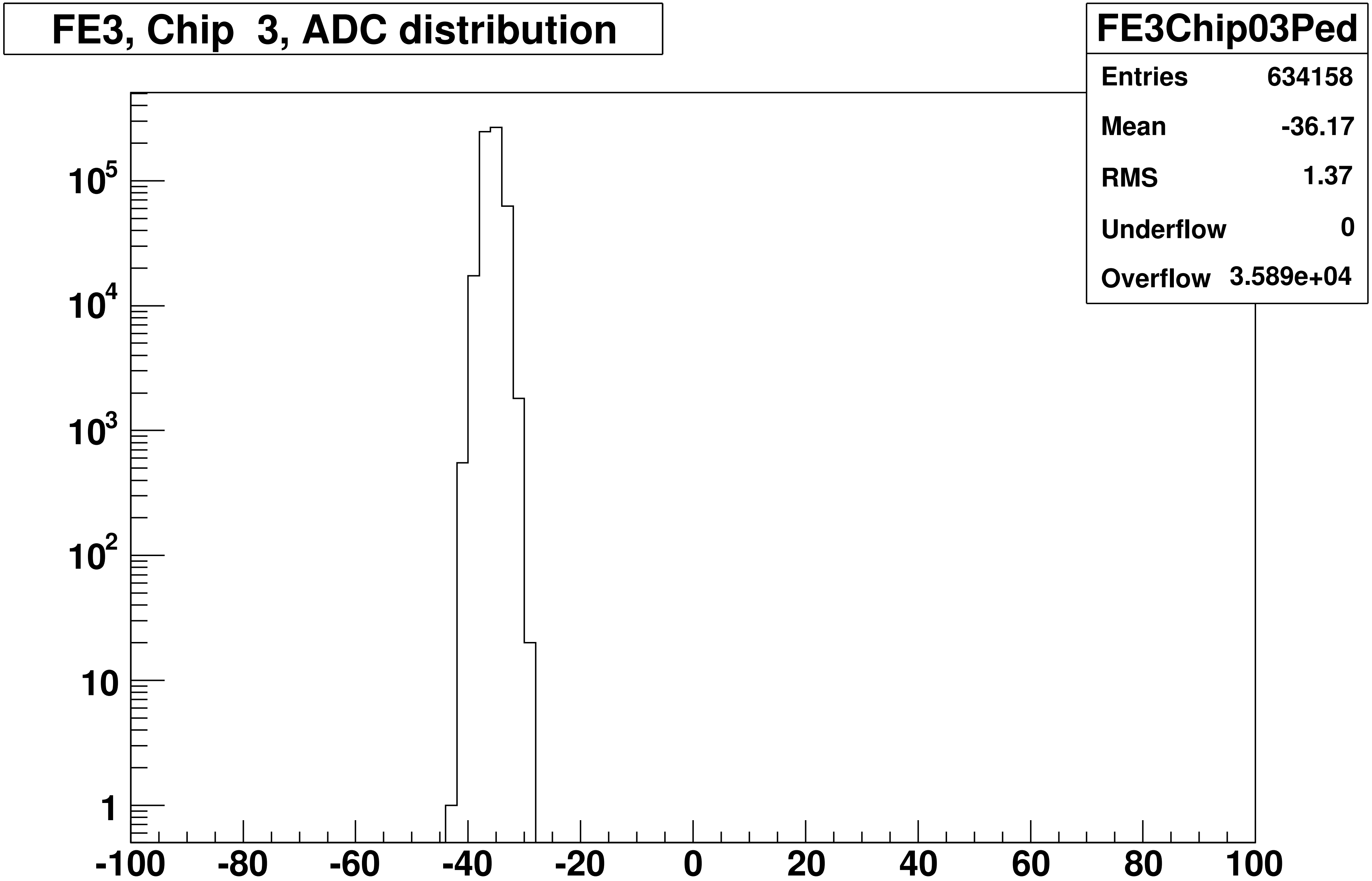

FE3, Chip 3, ADC distribution
FE3Chip03Ped
Entries 634158
Mean -36.17
RMS 1.37
Underflow 0
Overflow 3.589e+04
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10^3
10^2
10
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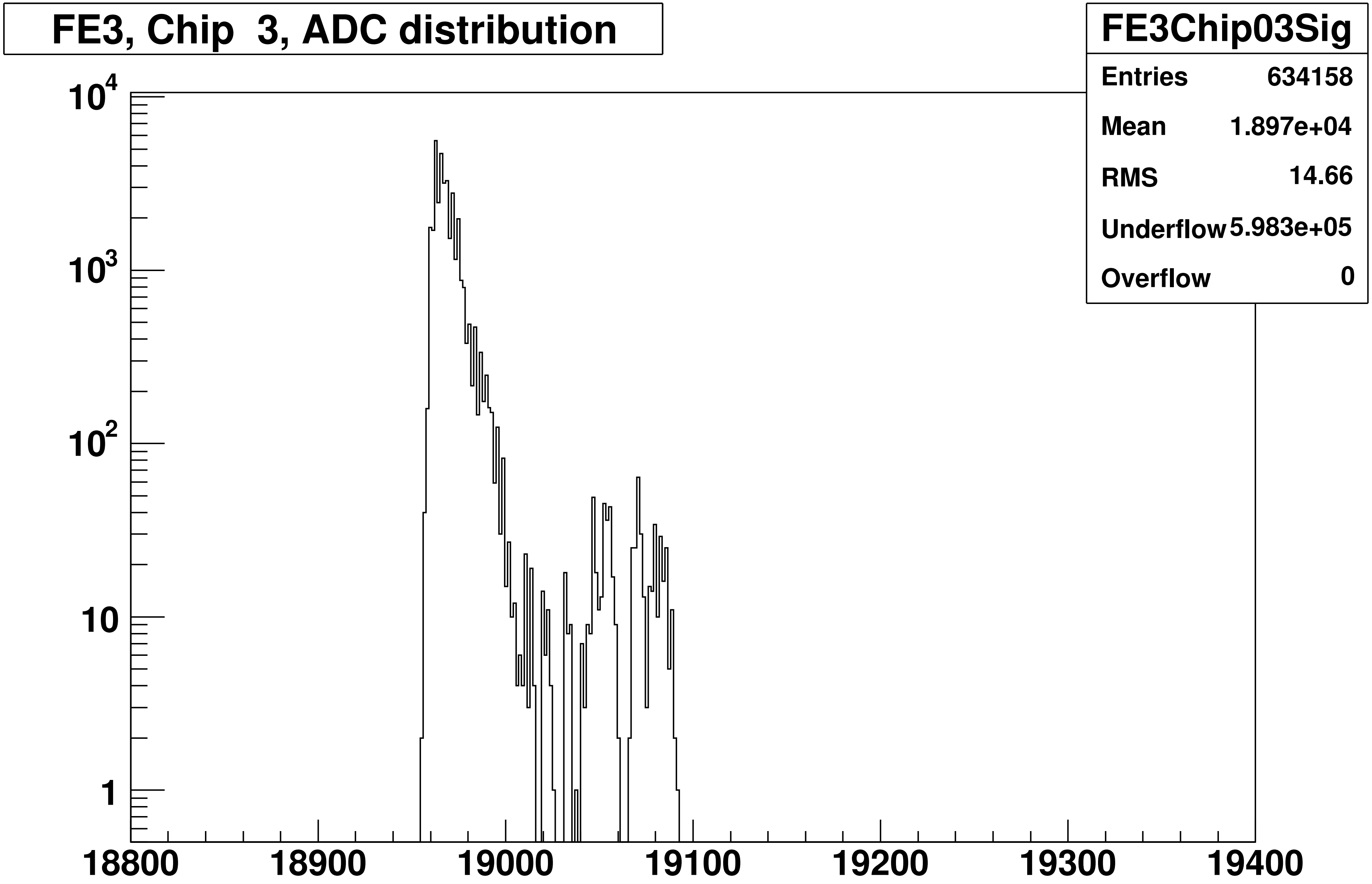
FE3, Chip 3, ADC distribution
FE3Chip03Sig
Entries 634158
Mean 1.897e+04
RMS 14.66
Underflow 5.983e+05
Overflow 0
10^4
10^3
10^2
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19200
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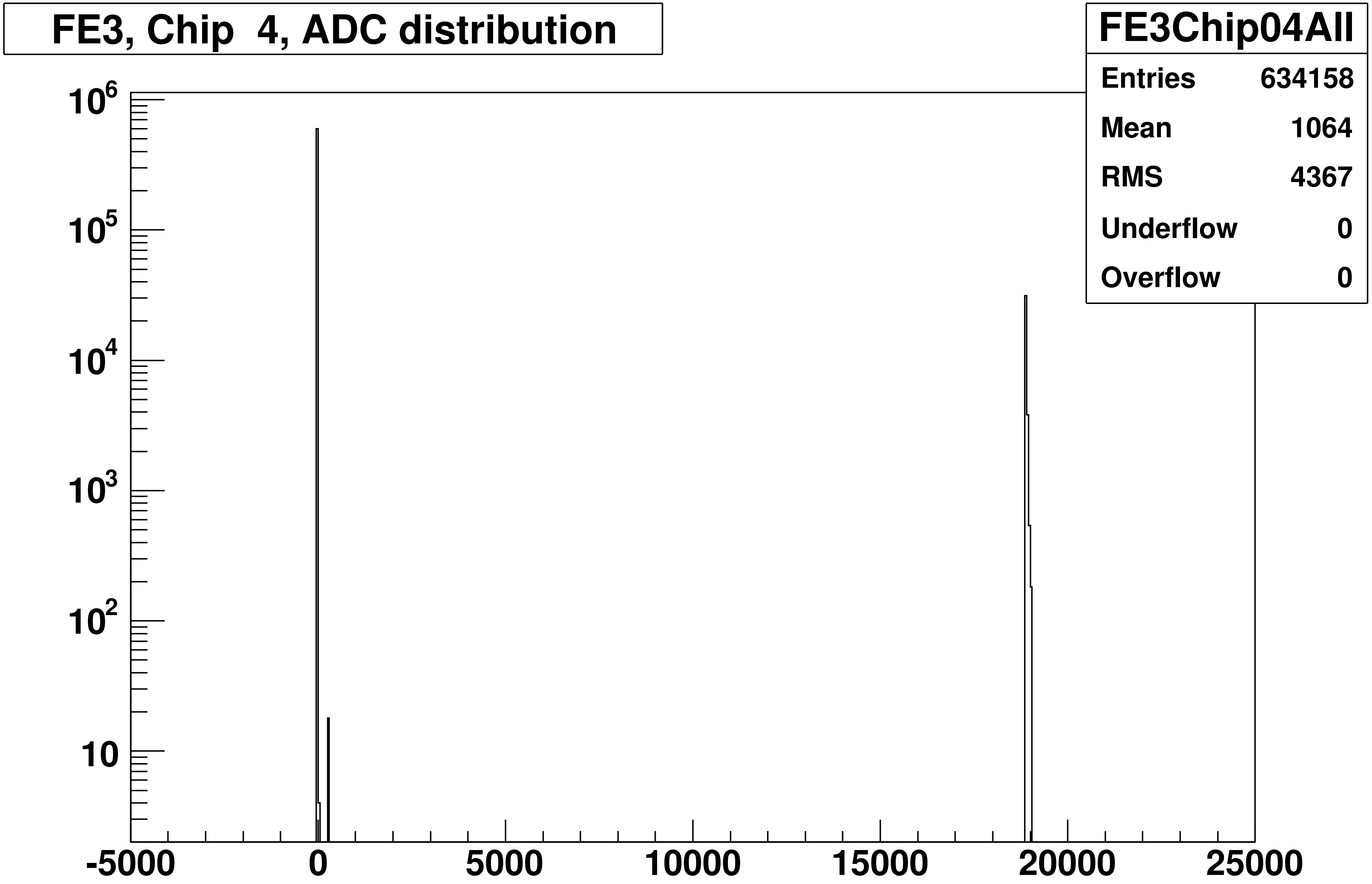
FE3, Chip 4, ADC distribution
FE3Chip04All
Entries 634158
Mean 1064
RMS 4367
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
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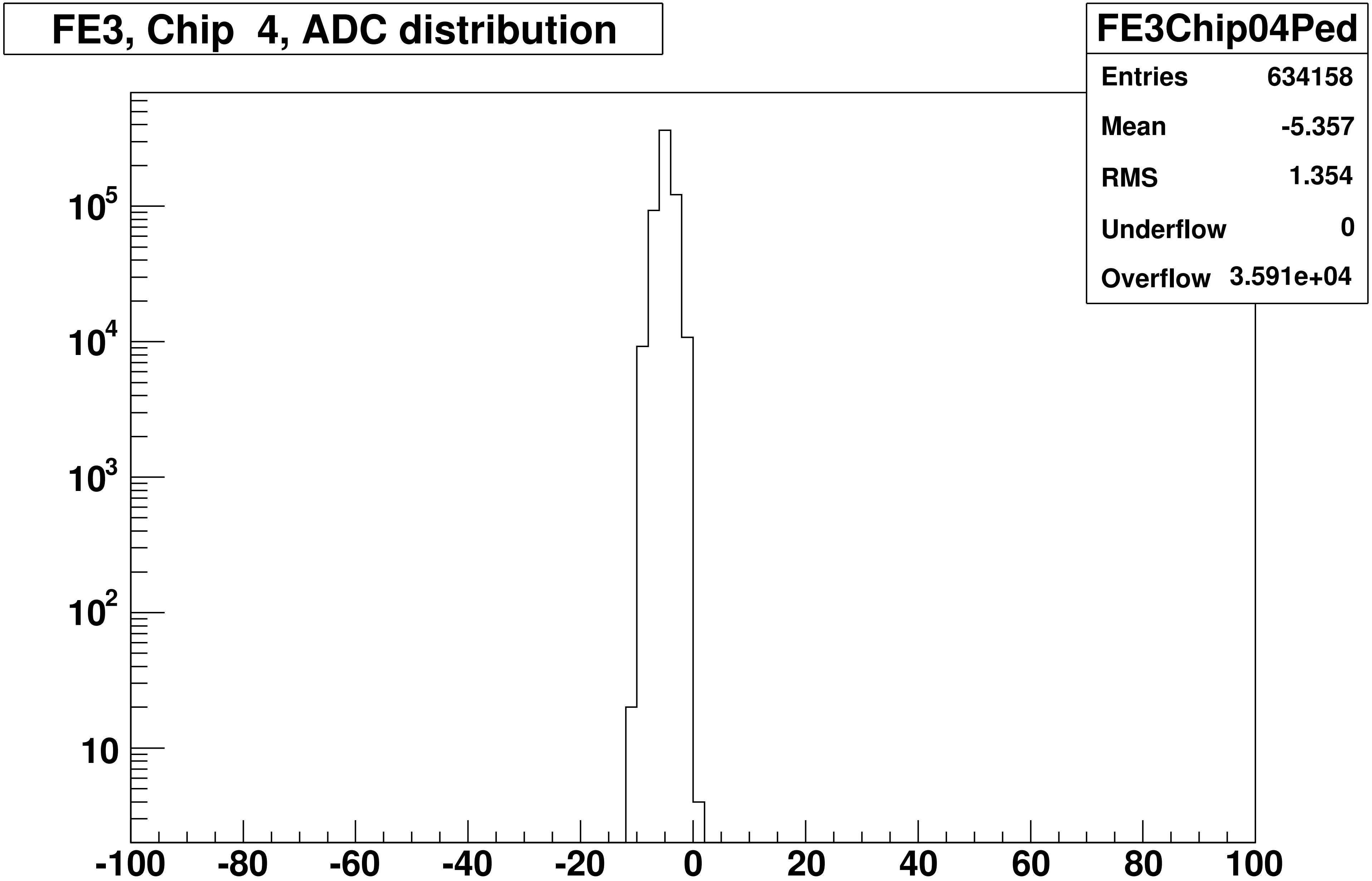
FE3, Chip 4, ADC distribution
FE3Chip04Ped
Entries 634158
Mean -5.357
RMS 1.354
Underflow 0
Overflow 3.591e+04
10^5
10^4
10^3
10^2
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80
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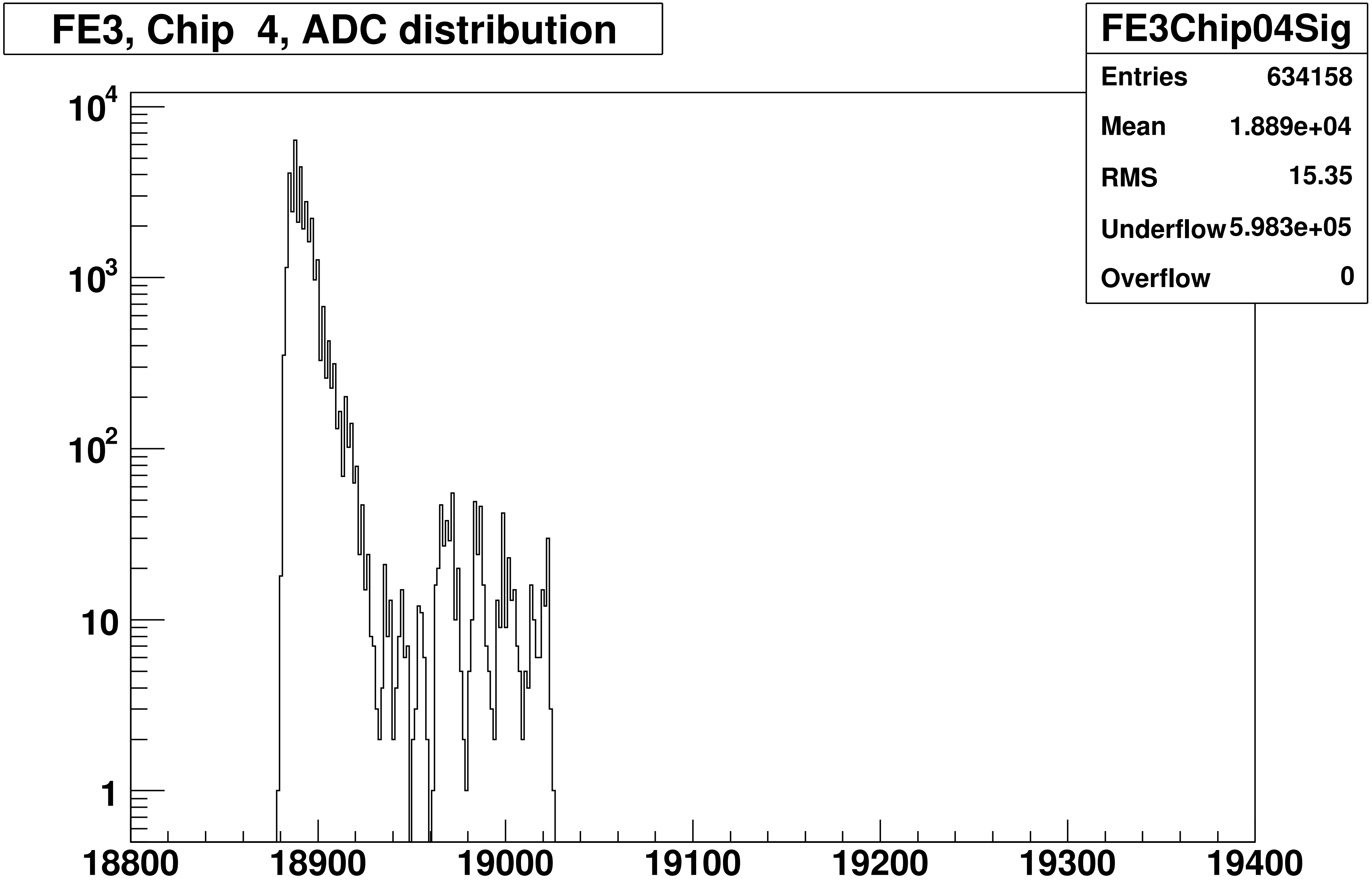
FE3, Chip 4, ADC distribution
FE3Chip04Sig
Entries 634158
Mean 1.889e+04
RMS 15.35
Underflow 5.983e+05
Overflow 0
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10^3
10^2
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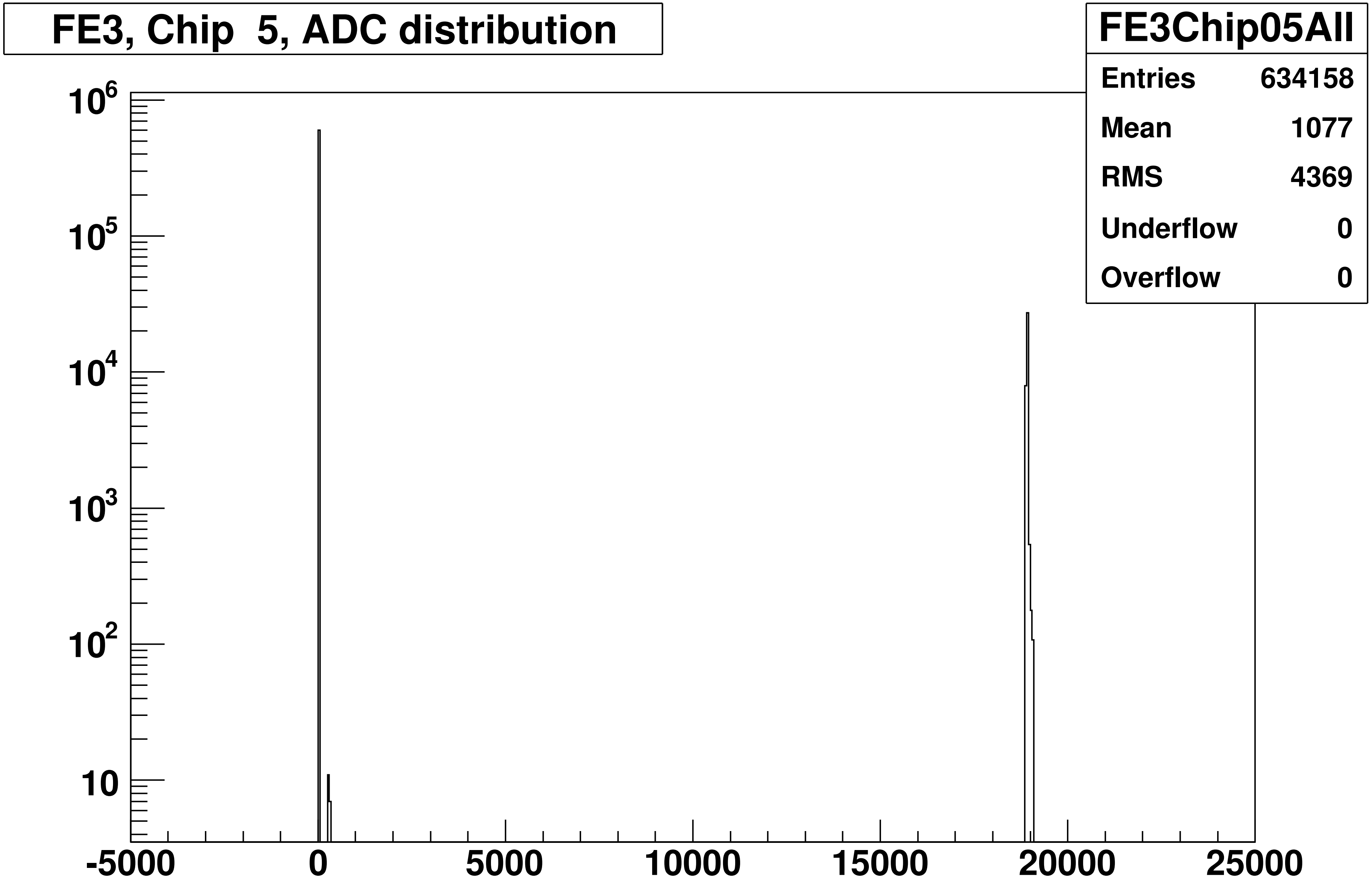
FE3, Chip 5, ADC distribution
FE3Chip05All
Entries 634158
Mean 1077
RMS 4369
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
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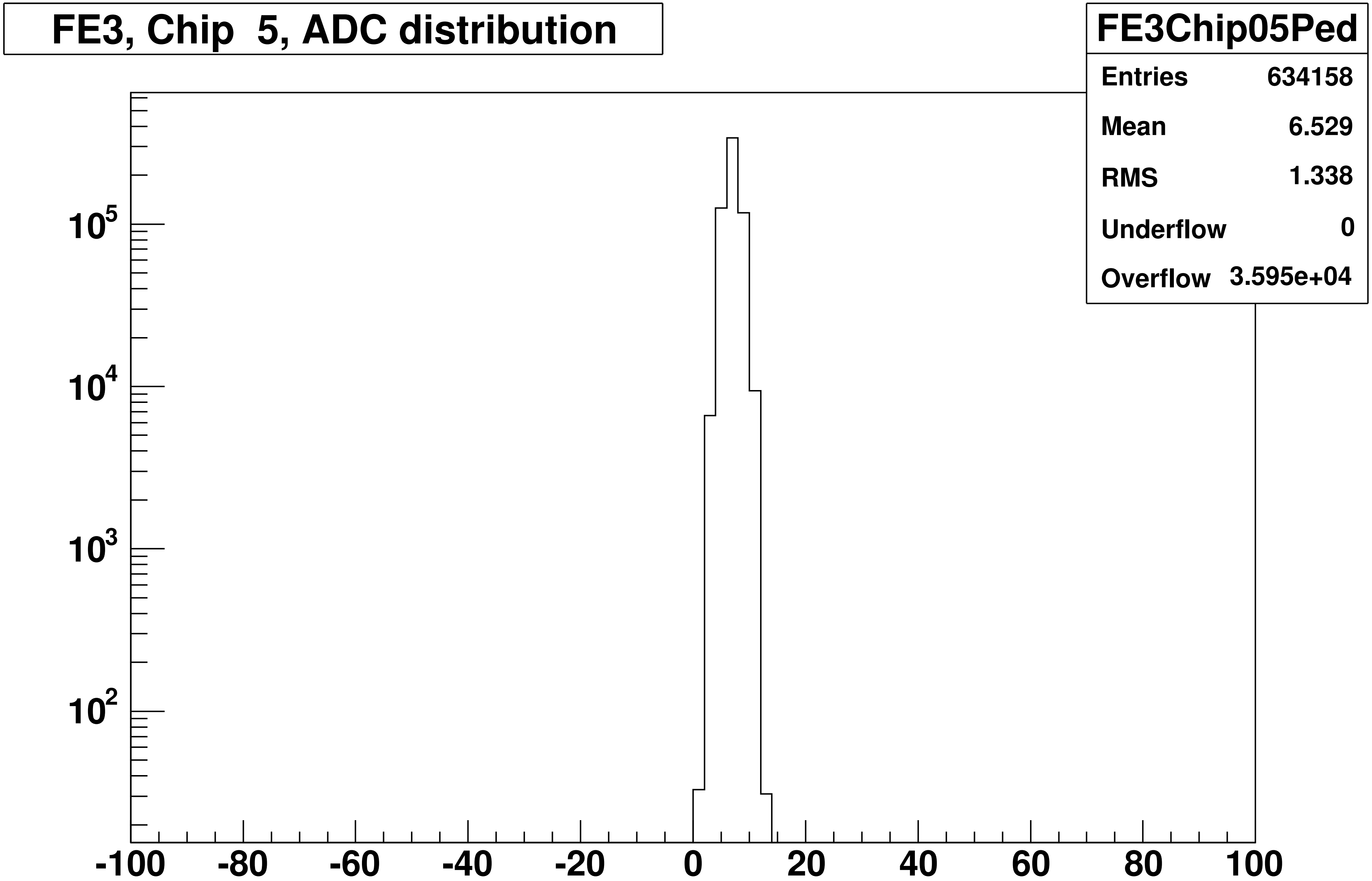
FE3, Chip 5, ADC distribution
FE3Chip05Ped
Entries 634158
Mean 6.529
RMS 1.338
Underflow 0
Overflow 3.595e+04
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10^3
10^2
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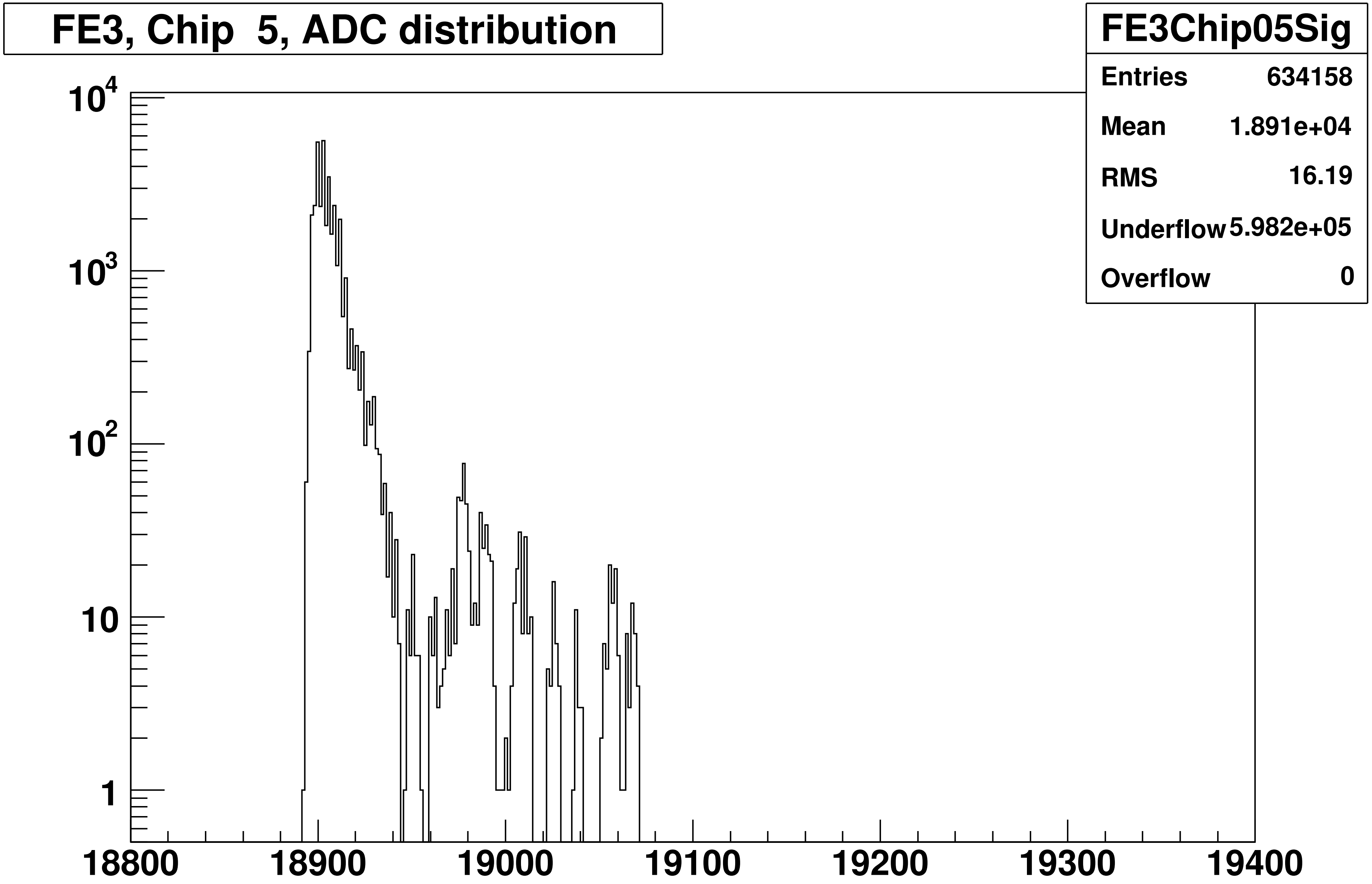
FE3, Chip 5, ADC distribution
FE3Chip05Sig
Entries 634158
Mean 1.891e+04
RMS 16.19
Underflow 5.982e+05
Overflow 0
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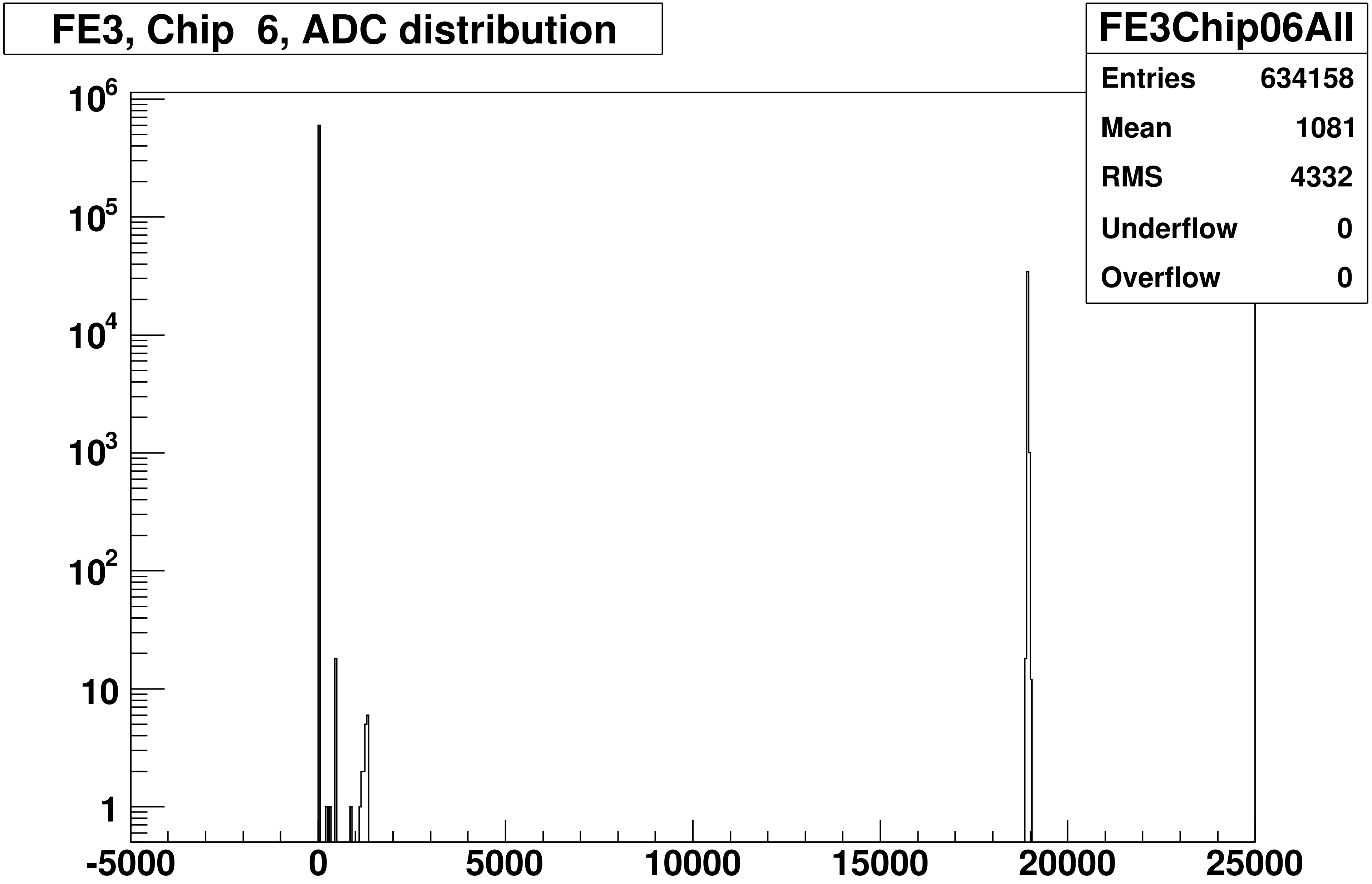

FE3, Chip 6, ADC distribution
FE3Chip06All
Entries 634158
Mean 1081
RMS 4332
Underflow 0
Overflow 0
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10^3
10^2
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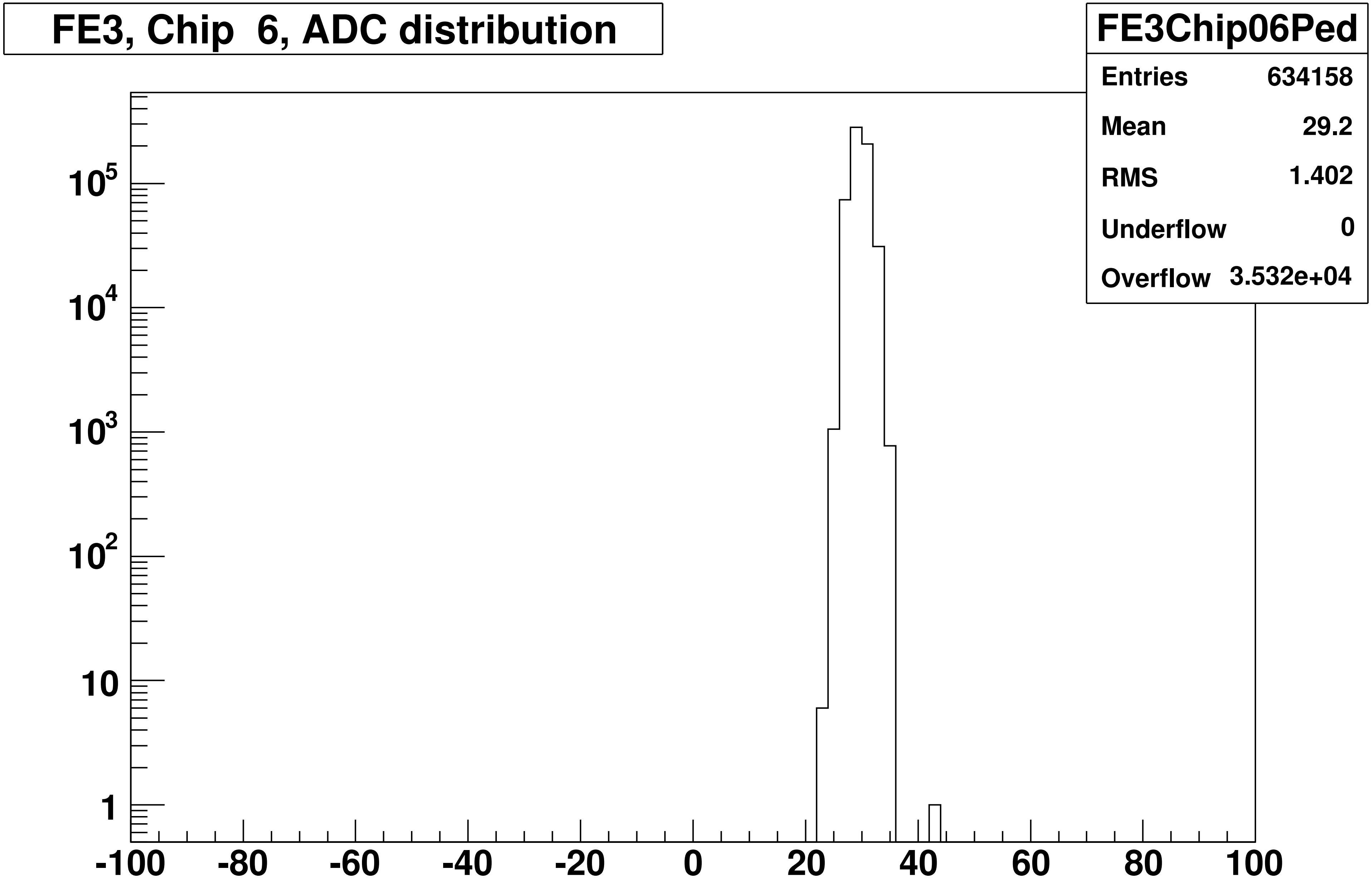
FE3, Chip 6, ADC distribution
FE3Chip06Ped
Entries 634158
Mean 29.2
RMS 1.402
Underflow 0
Overflow 3.532e+04
10^5
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1
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80
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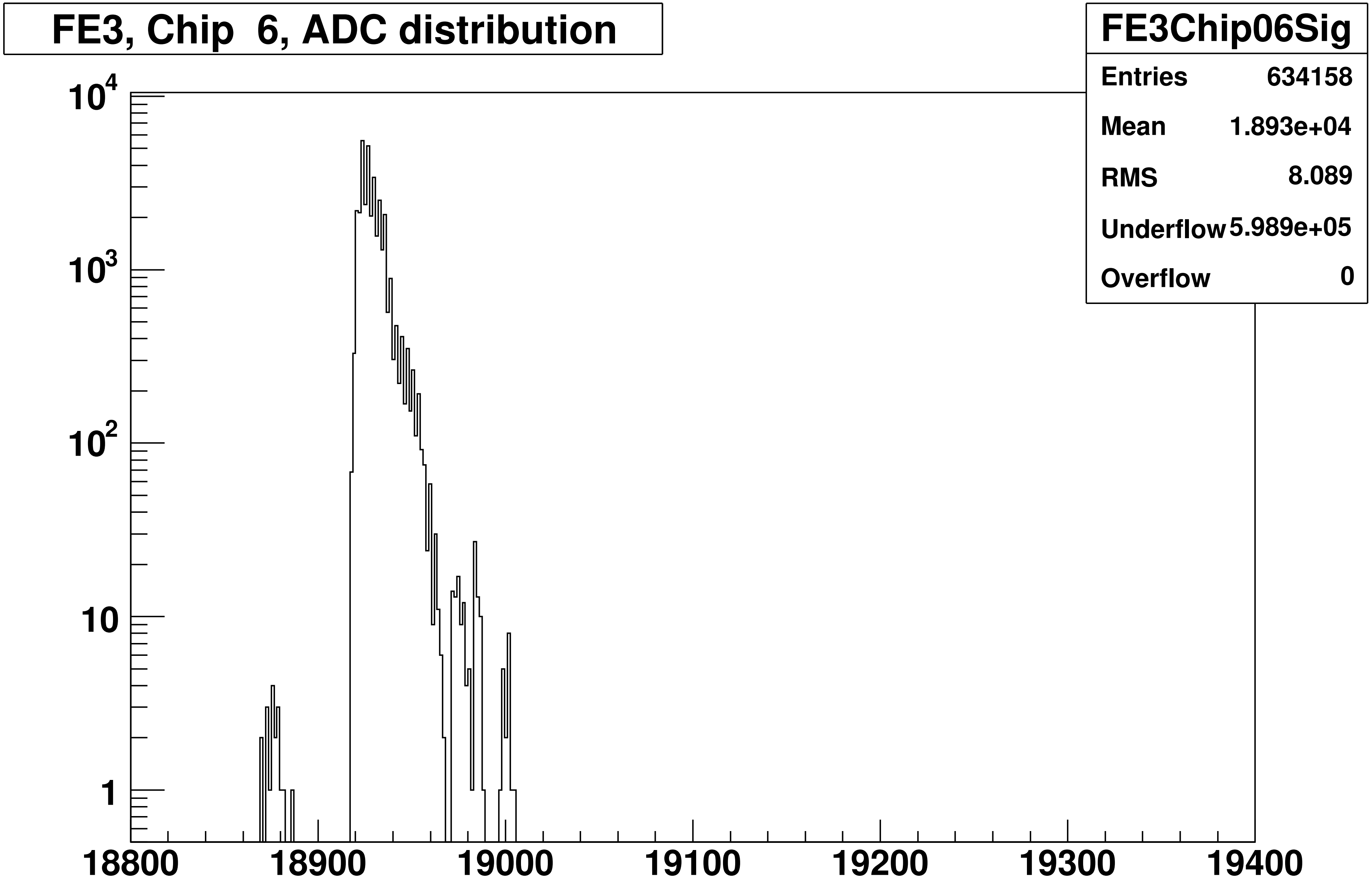
FE3, Chip 6, ADC distribution
FE3Chip06Sig
Entries 634158
Mean 1.893e+04
RMS 8.089
Underflow 5.989e+05
Overflow 0
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10^3
10^2
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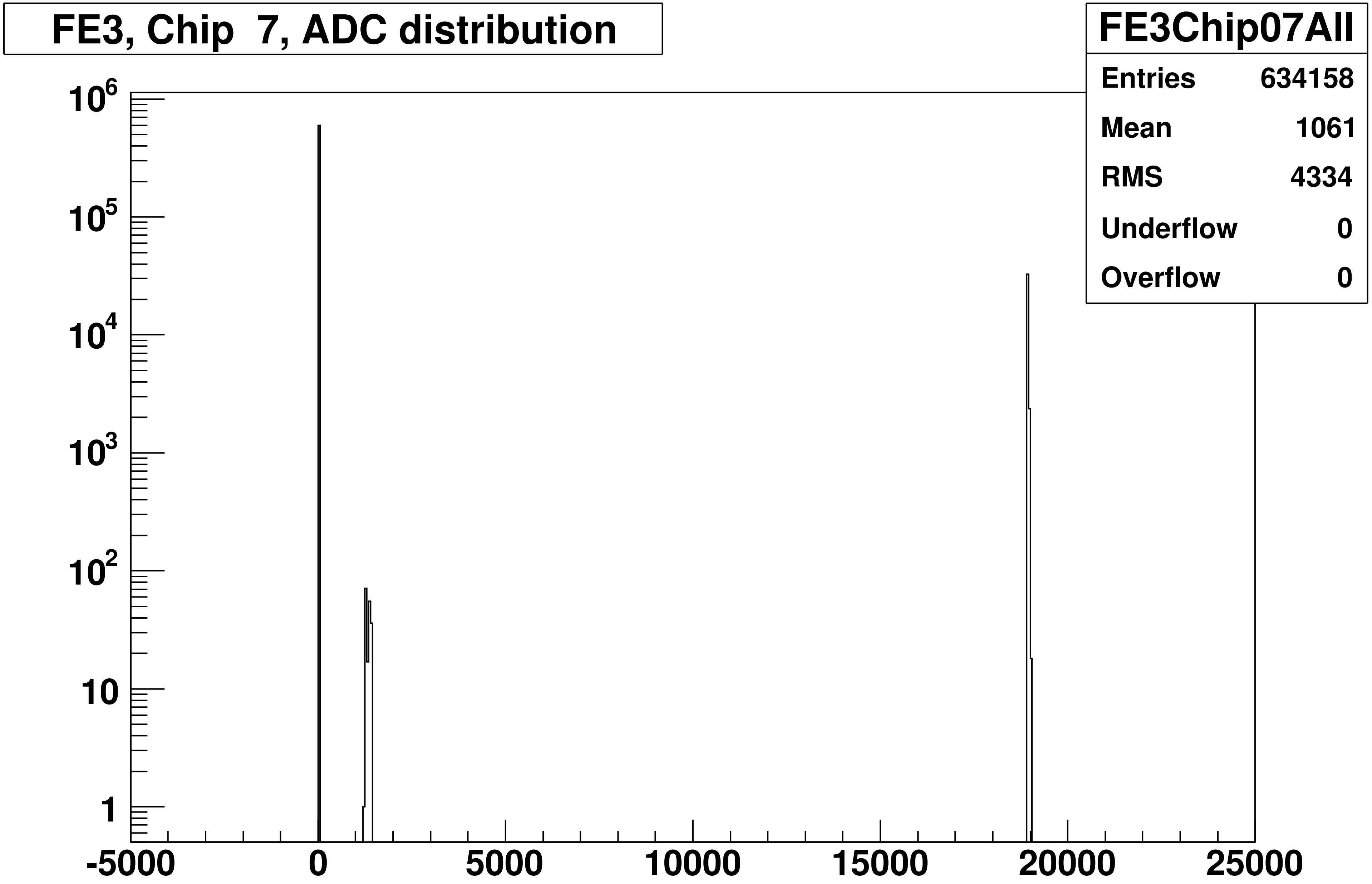
FE3, Chip 7, ADC distribution
FE3Chip07All
Entries 634158
Mean 1061
RMS 4334
Underflow 0
Overflow 0
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10^3
10^2
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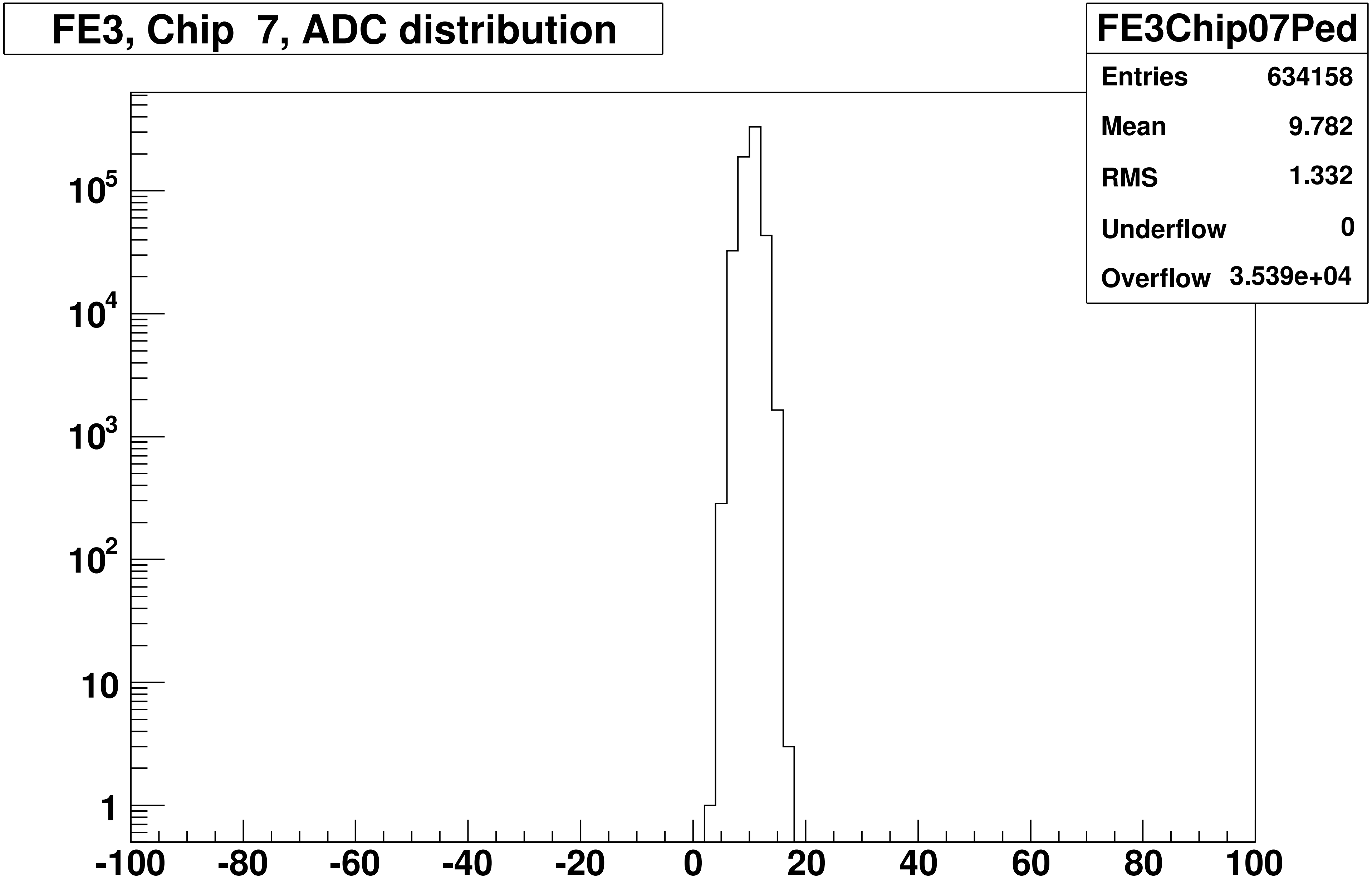

FE3, Chip 7, ADC distribution
FE3Chip07Ped
Entries 634158
Mean 9.782
RMS 1.332
Underflow 0
Overflow 3.539e+04
10^5
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10^3
10^2
10
1
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80
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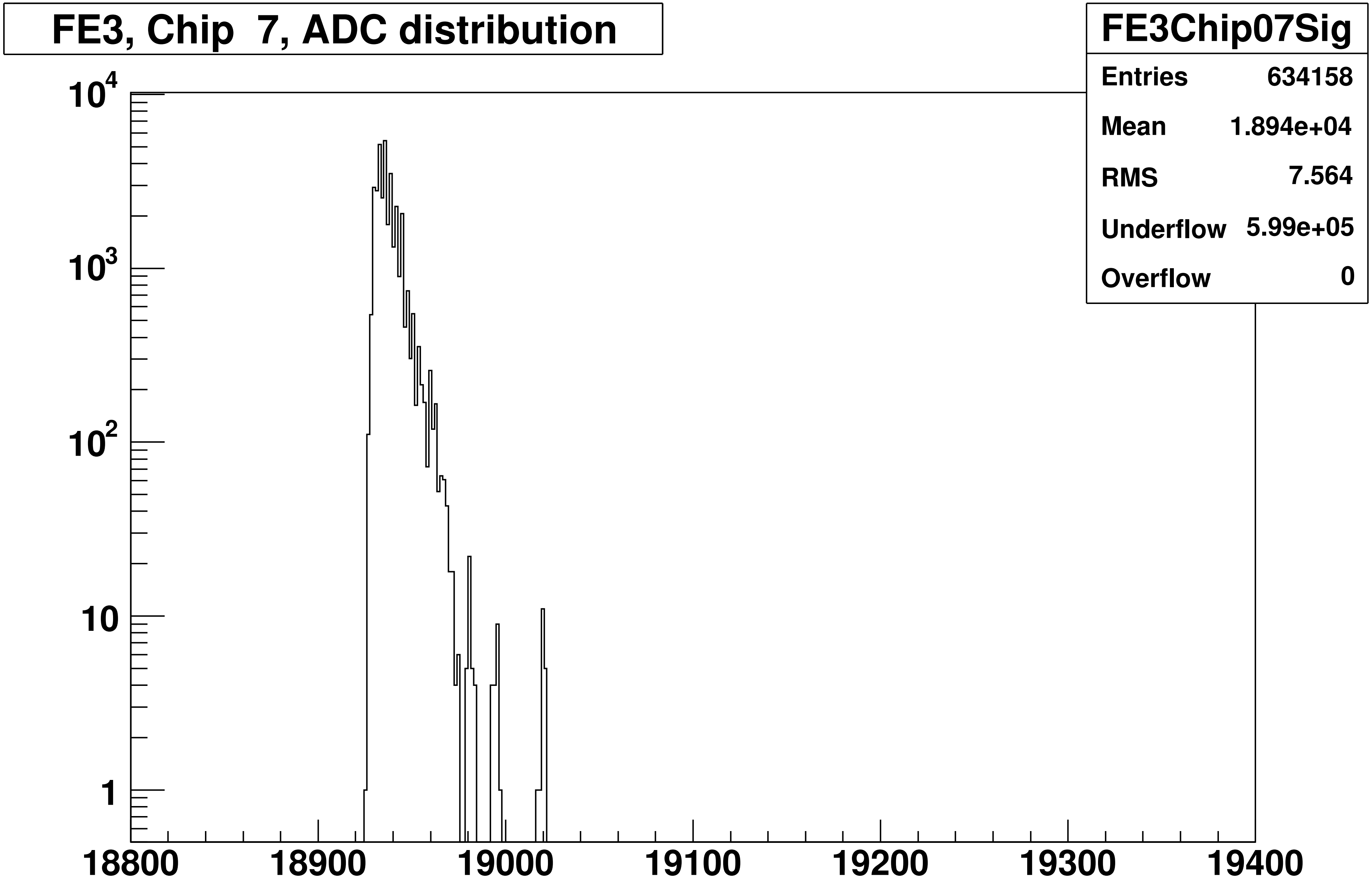

FE3, Chip 7, ADC distribution
FE3Chip07Sig
Entries 634158
Mean 1.894e+04
RMS 7.564
Underflow 5.99e+05
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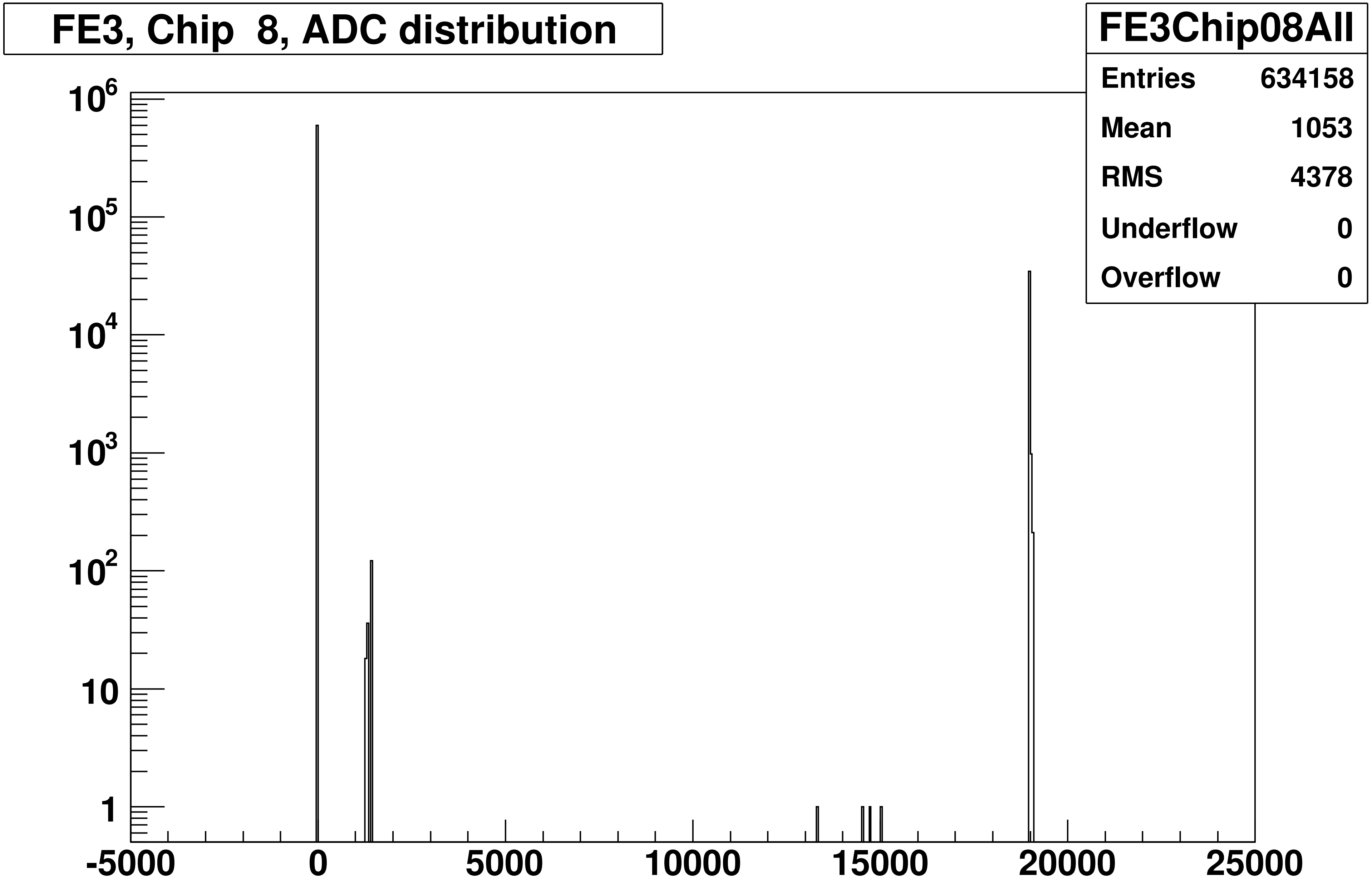
FE3, Chip 8, ADC distribution
FE3Chip08All
Entries 634158
Mean 1053
RMS 4378
Underflow 0
Overflow 0
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10^4
10^3
10^2
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10000
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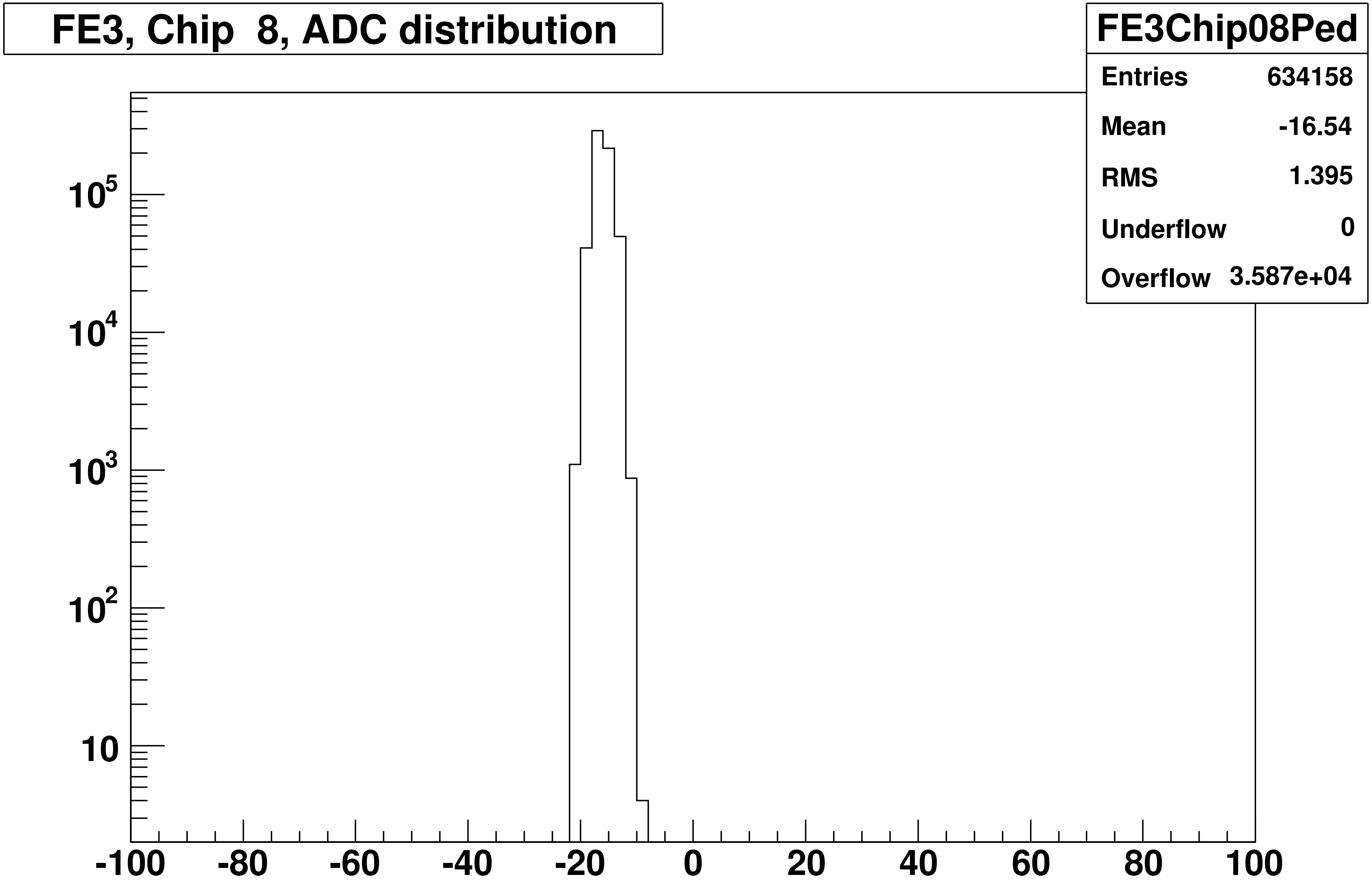
20000
25000


FE3, Chip 8, ADC distribution
FE3Chip08Ped
Entries 634158
Mean -16.54
RMS 1.395
Underflow 0
Overflow 3.587e+04
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10^2
10^3
10^4
10^5
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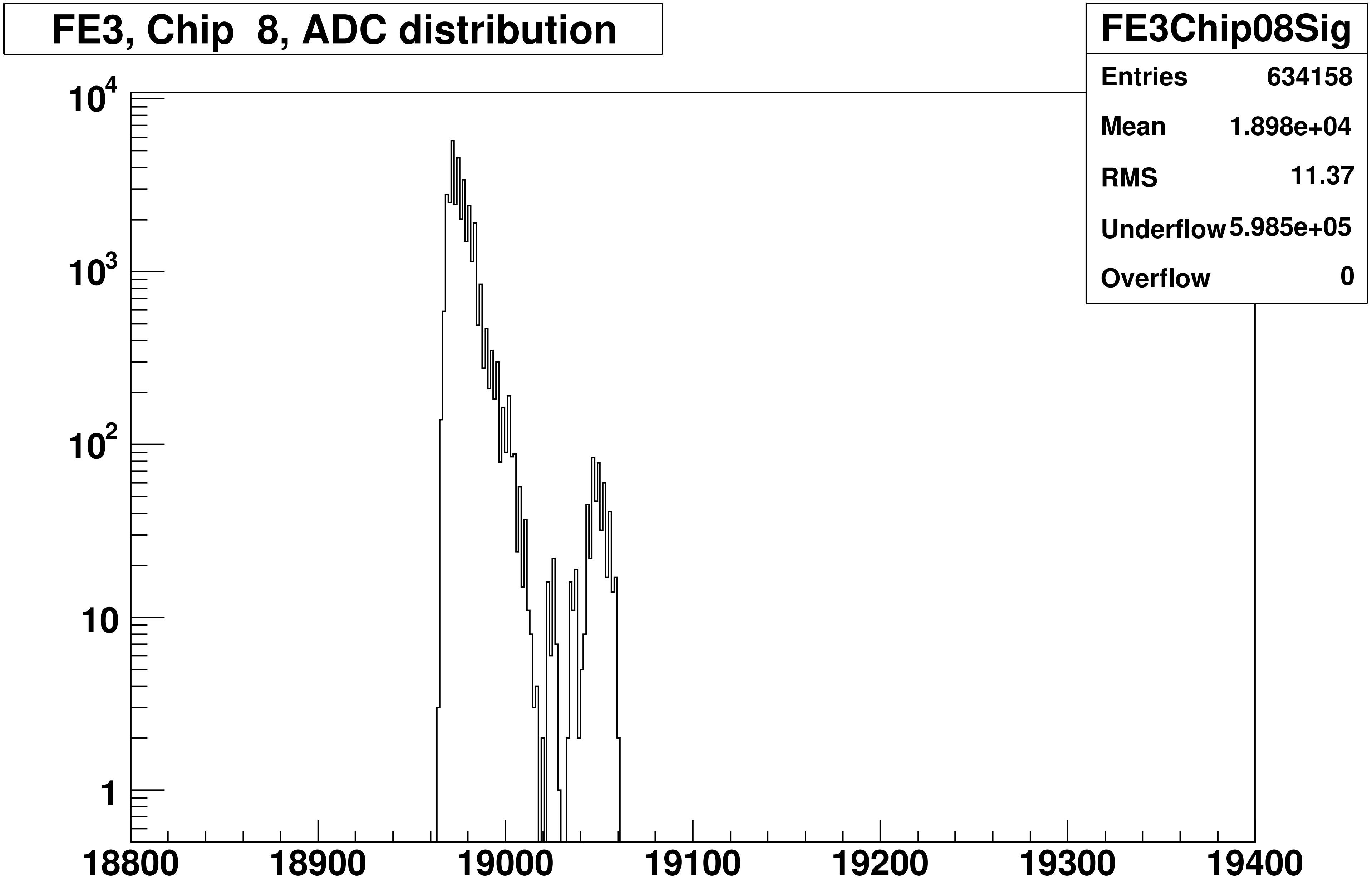
40
60
80
100



FE3, Chip 8, ADC distribution
FE3Chip08Sig
Entries 634158
Mean 1.898e+04
RMS 11.37
Underflow 5.985e+05
Overflow 0
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10^3
10^2
10
1
18800
18900
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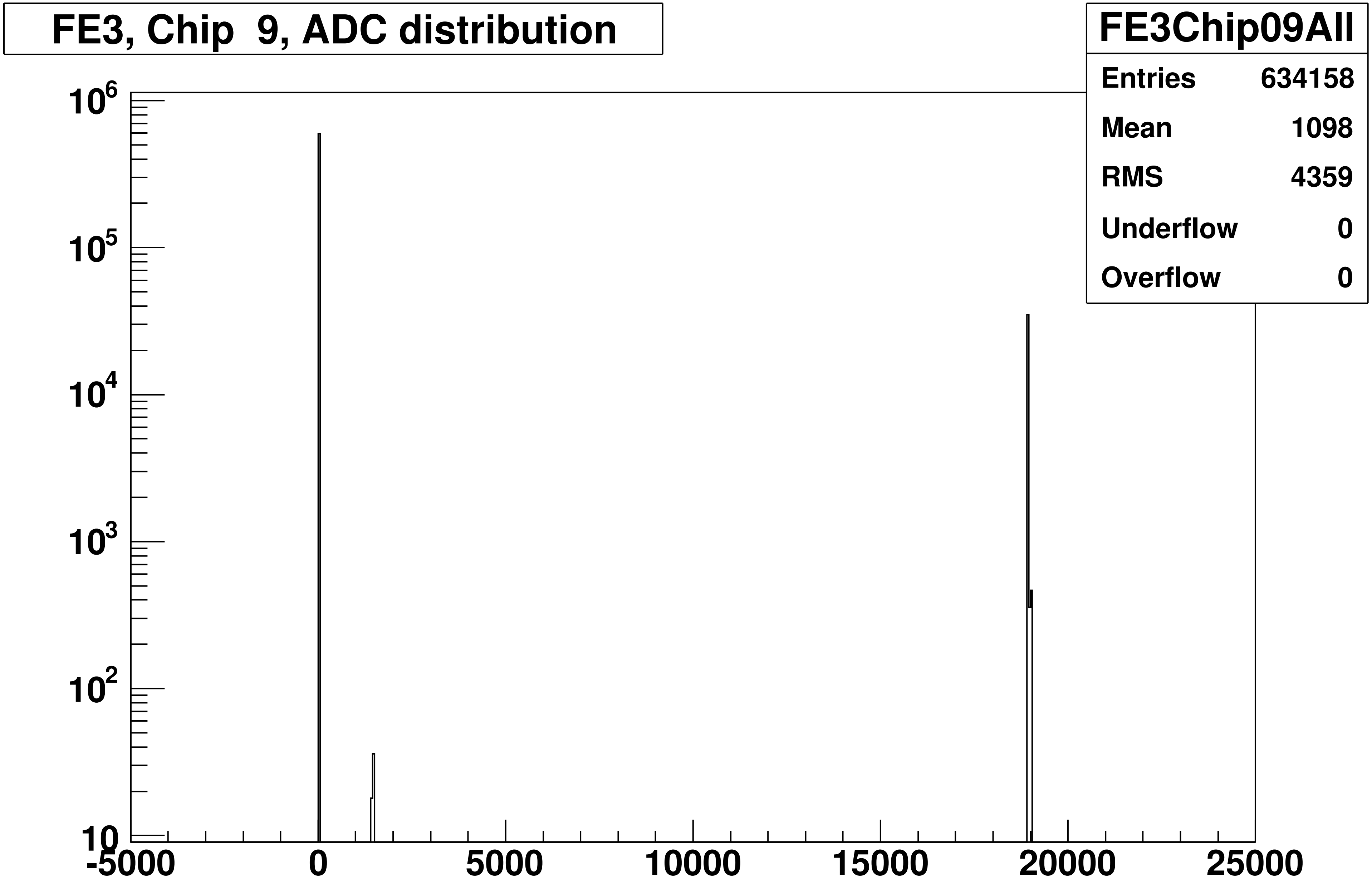

FE3, Chip 9, ADC distribution
FE3Chip09All
Entries 634158
Mean 1098
RMS 4359
Underflow 0
Overflow 0
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10^2
10^3
10^4
10^5
10^6
-5000
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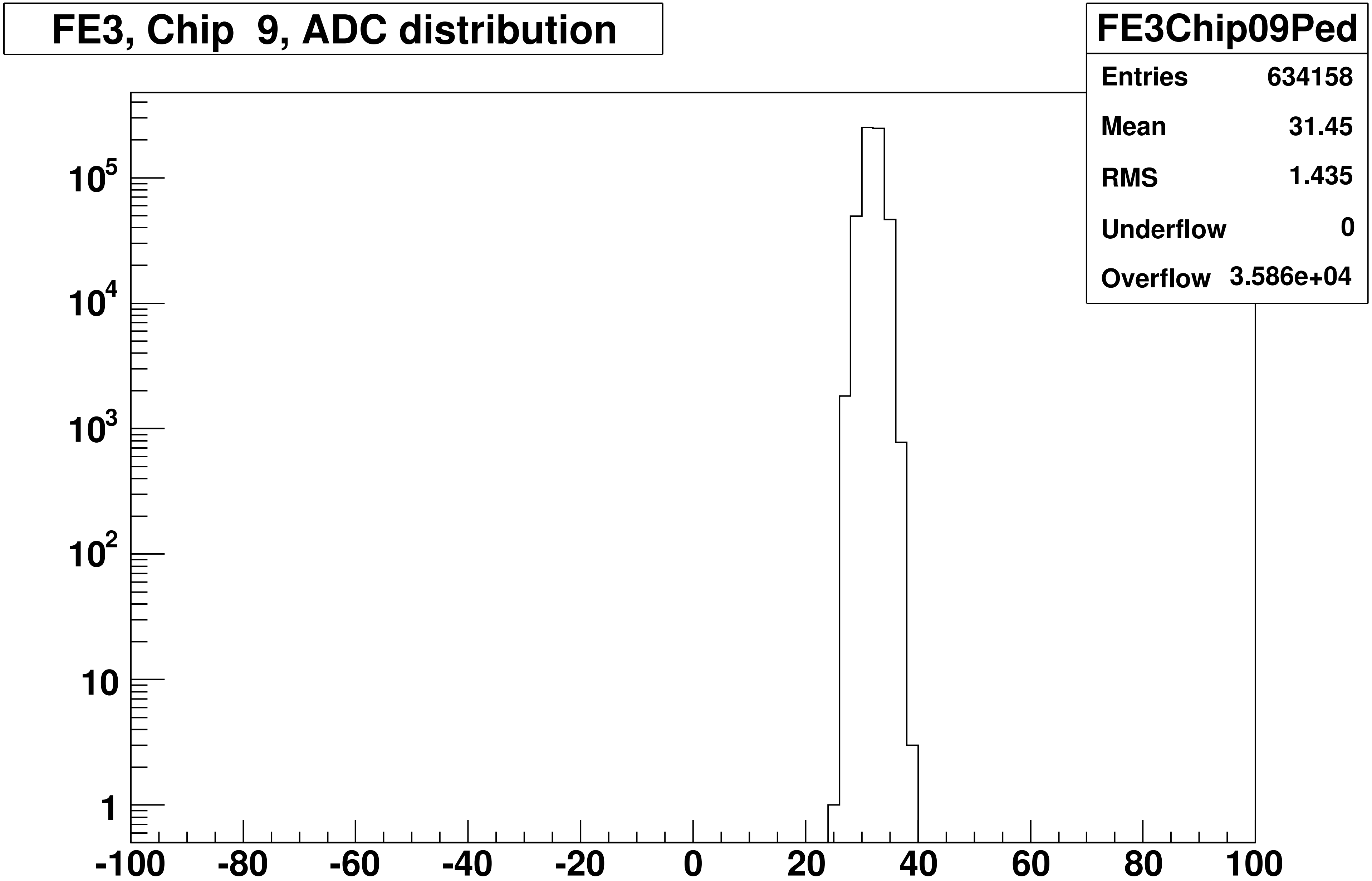
5000
10000
15000
20000
25000


FE3, Chip 9, ADC distribution
FE3Chip09Ped
Entries 634158
Mean 31.45
RMS 1.435
Underflow 0
Overflow 3.586e+04
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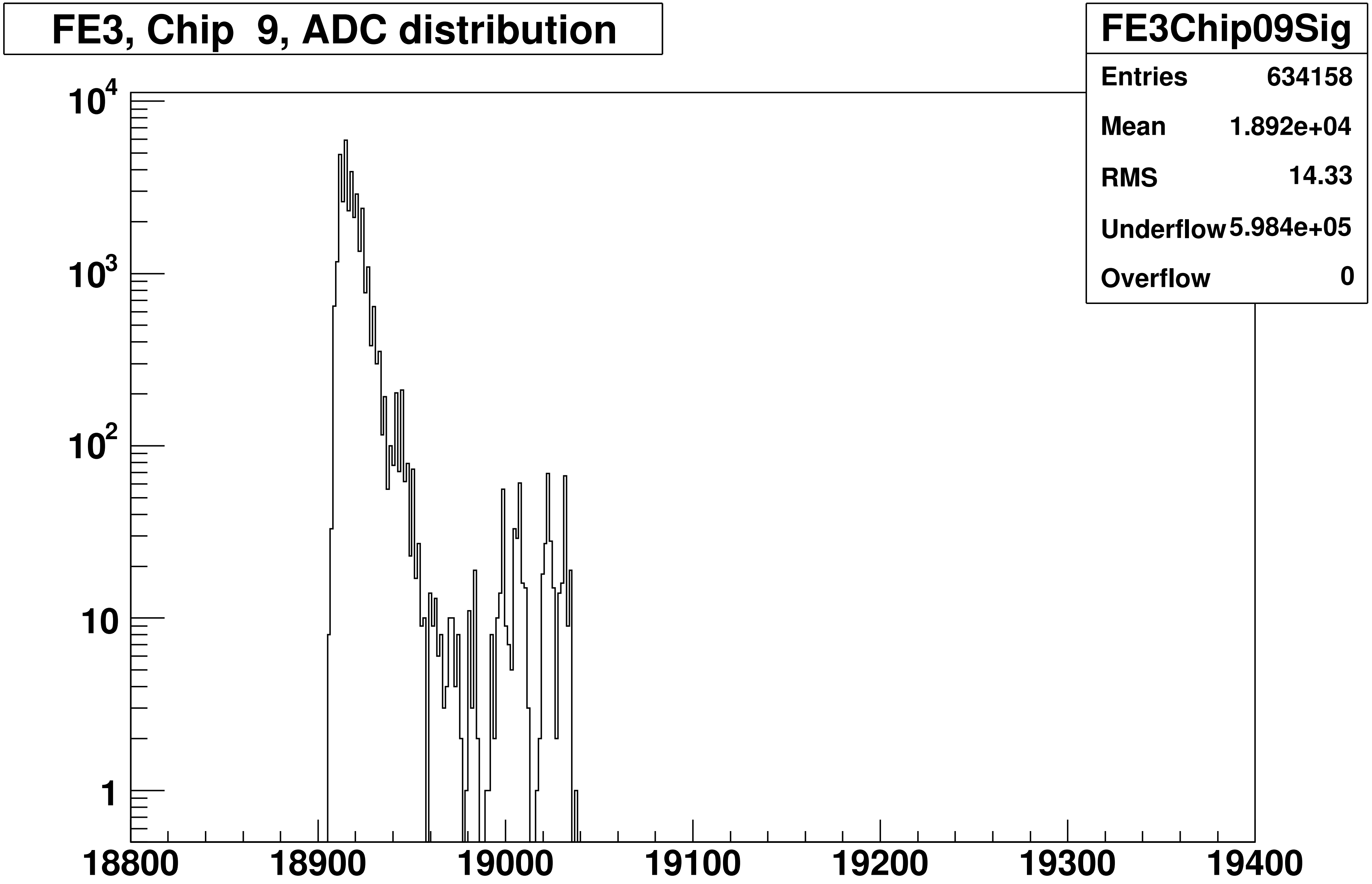
10^4
10^3
10^2
10
1
-100 -80 -60 -40 -20 0 20 40 60 80 100



FE3, Chip 9, ADC distribution
FE3Chip09Sig
Entries 634158
Mean 1.892e+04
RMS 14.33
Underflow 5.984e+05
Overflow 0
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10^3
10^2
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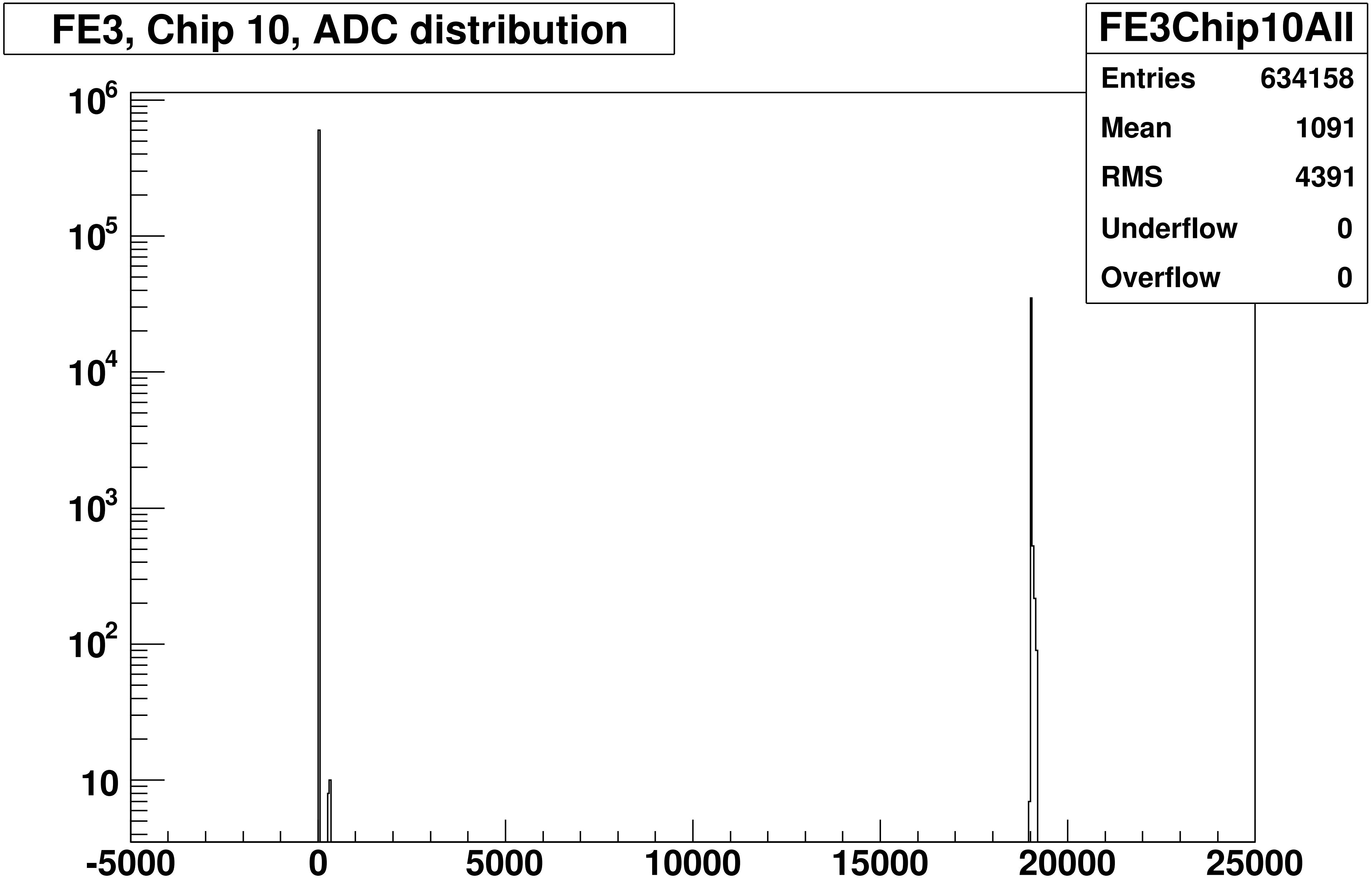
FE3, Chip 10, ADC distribution
FE3Chip10All
Entries 634158
Mean 1091
RMS 4391
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
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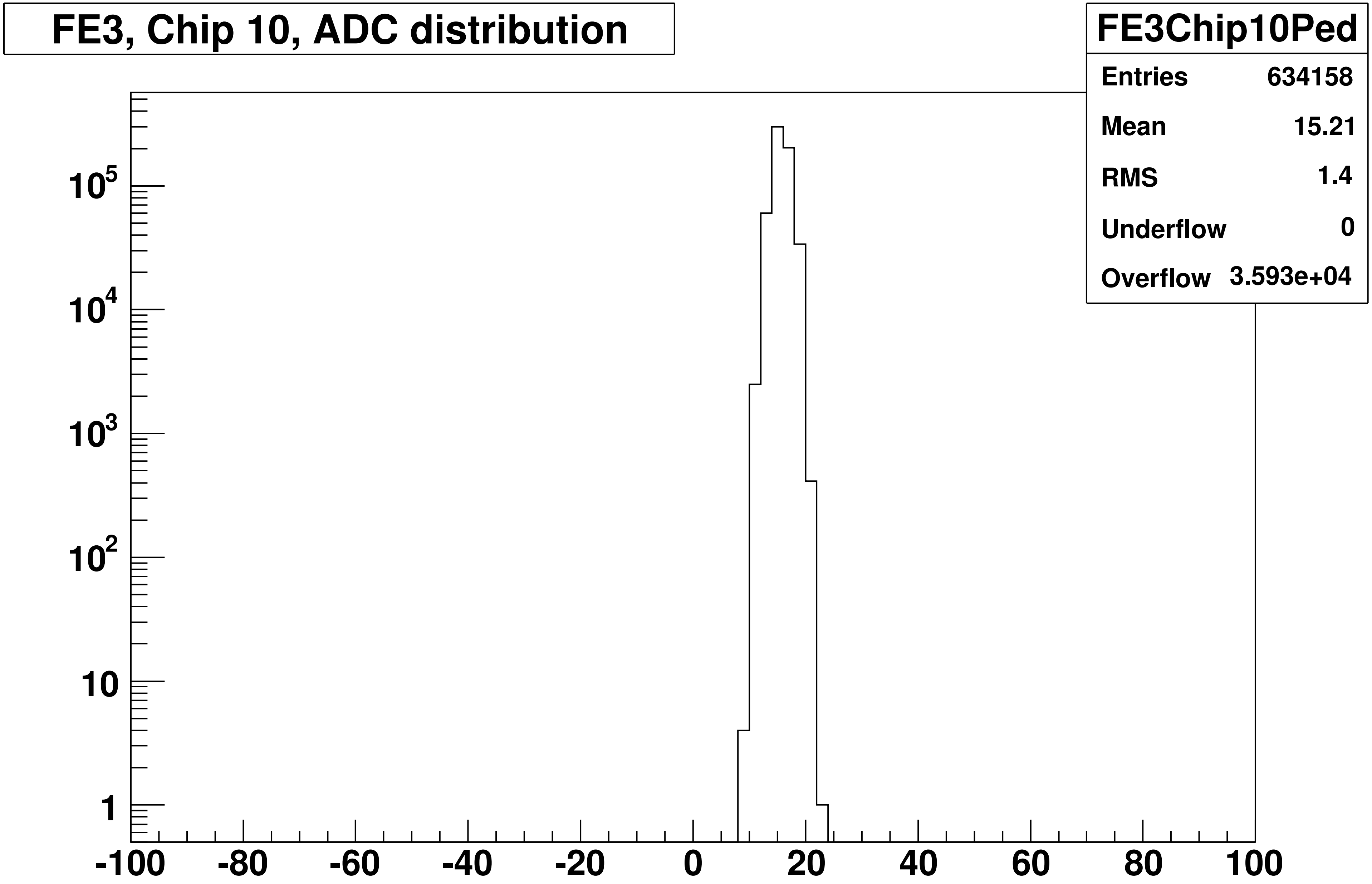
20000
25000


FE3, Chip 10, ADC distribution
FE3Chip10Ped
Entries 634158
Mean 15.21
RMS 1.4
Underflow 0
Overflow 3.593e+04
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10^3
10^2
10
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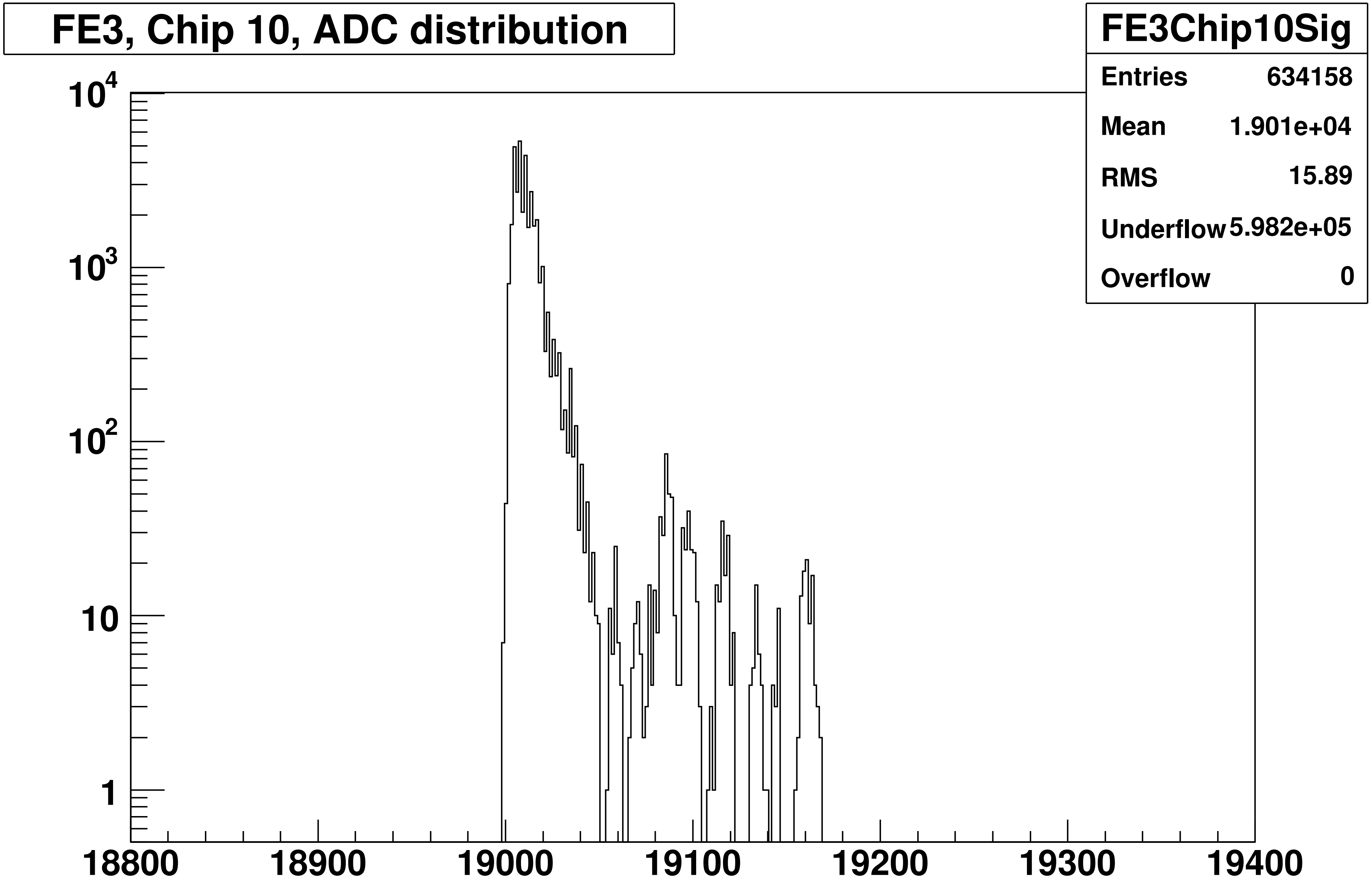
-100 -80 -60 -40 -20 0 20 40 60 80 100


FE3, Chip 10, ADC distribution
FE3Chip10Sig
Entries 634158
Mean 1.901e+04
RMS 15.89
Underflow 5.982e+05
Overflow 0
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10^3
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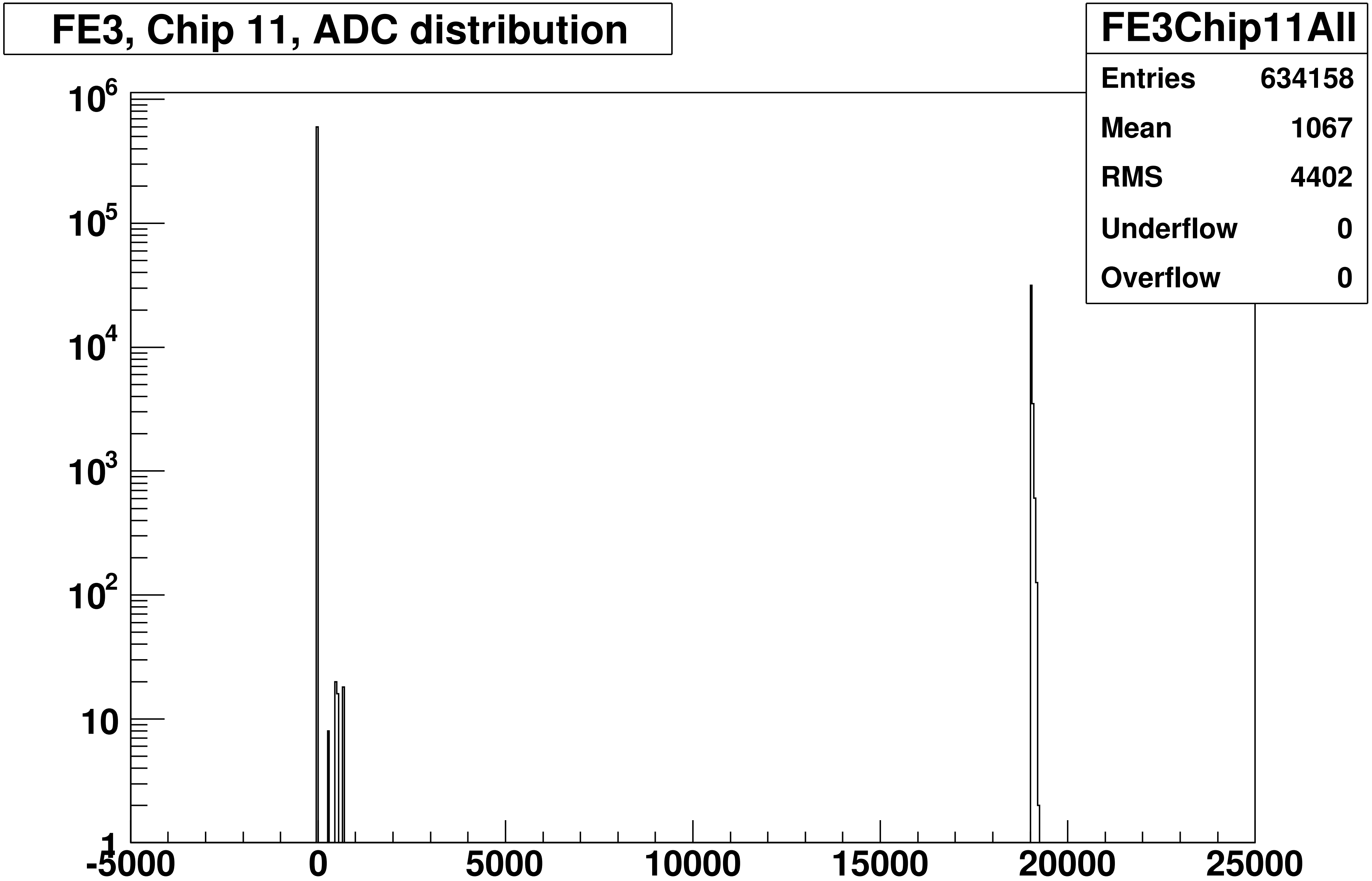
FE3, Chip 11, ADC distribution
FE3Chip11All
Entries 634158
Mean 1067
RMS 4402
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
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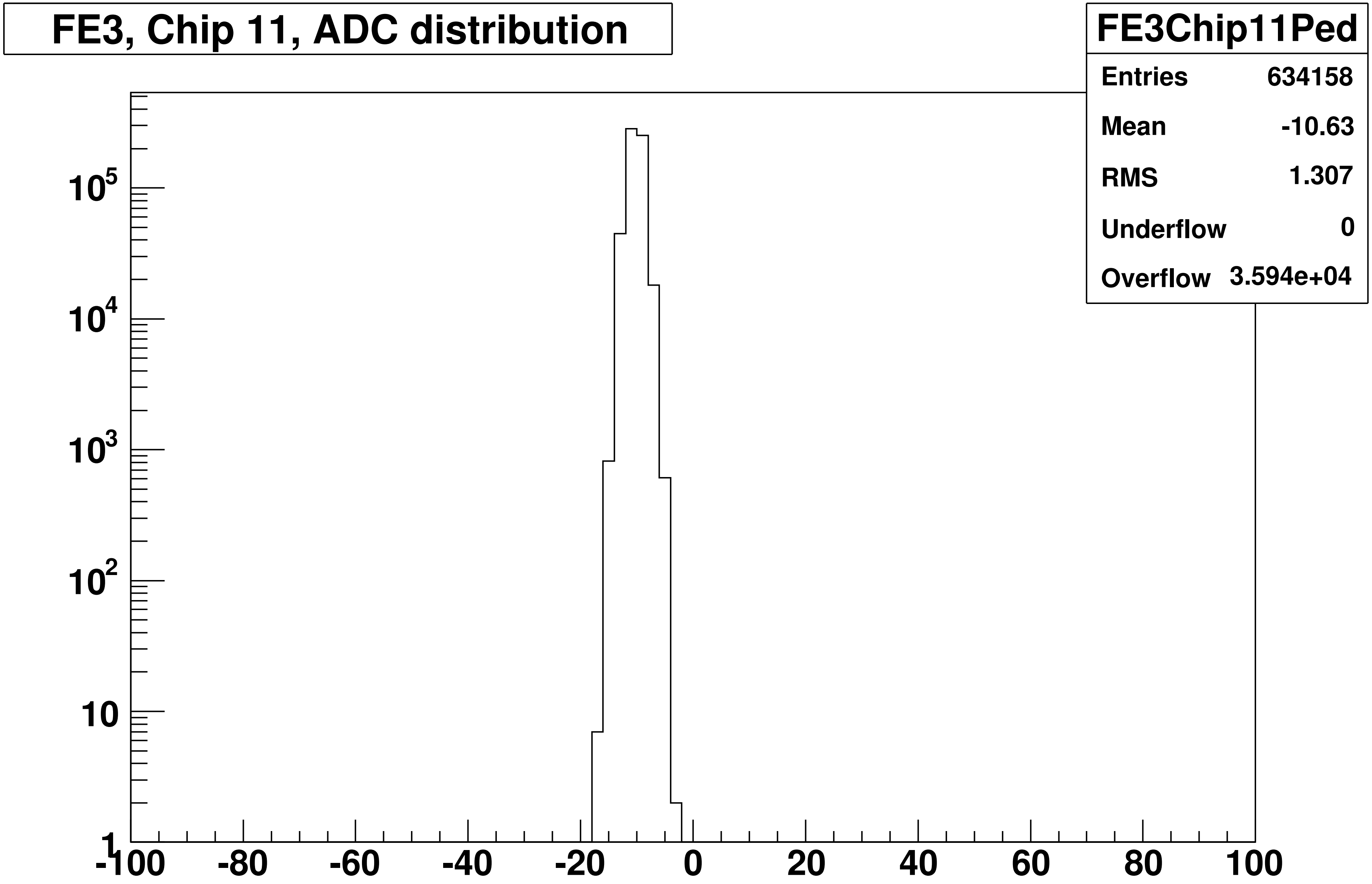
15000
20000
25000


FE3, Chip 11, ADC distribution
FE3Chip11Ped
Entries 634158
Mean -10.63
RMS 1.307
Underflow 0
Overflow 3.594e+04
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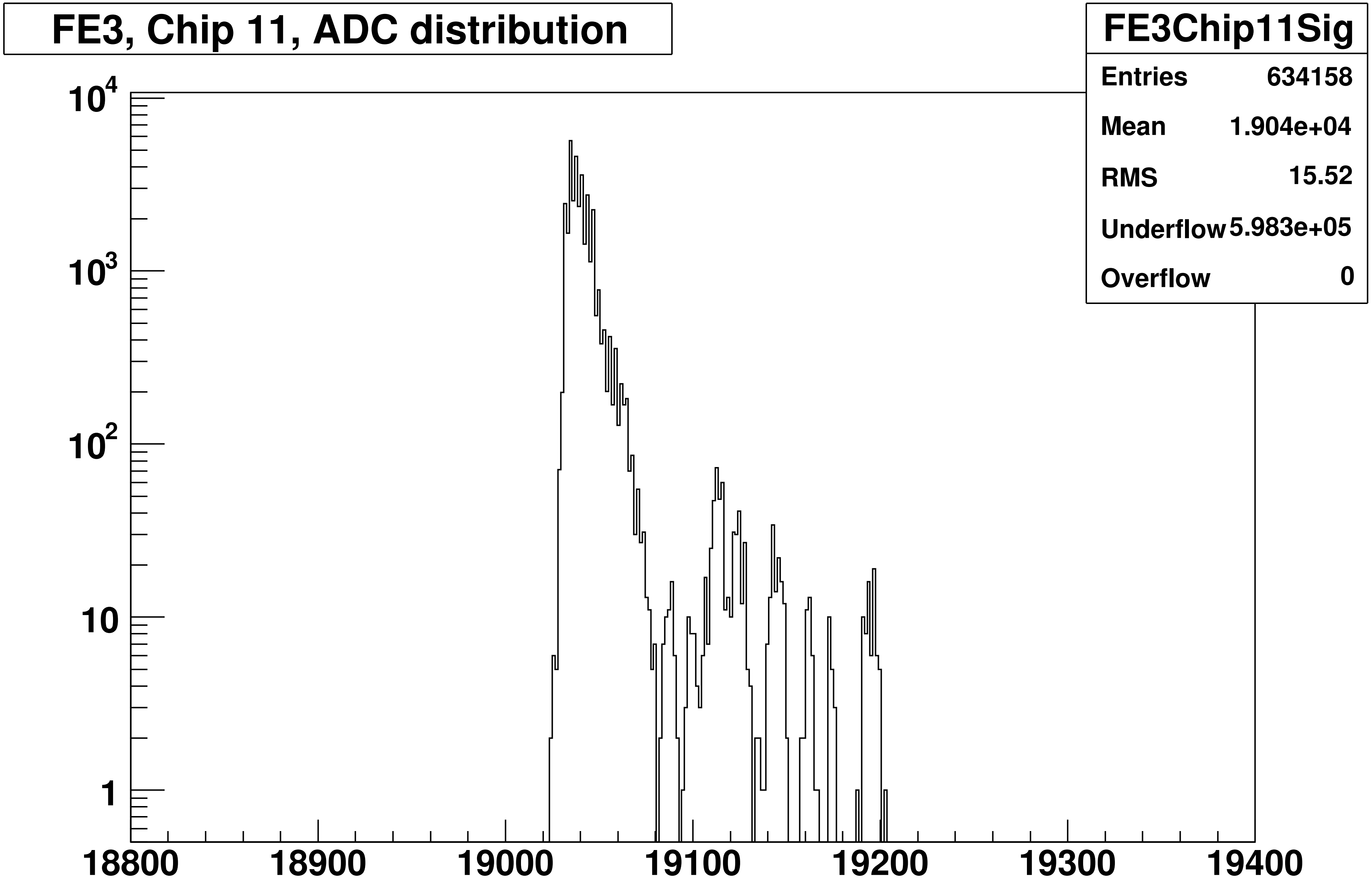
10^4
10^3
10^2
10
1
-100 -80 -60 -40 -20 0 20 40 60 80 100



FE3, Chip 11, ADC distribution
FE3Chip11Sig
Entries 634158
Mean 1.904e+04
RMS 15.52
Underflow 5.983e+05
Overflow 0
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10^3
10^2
10
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18800
18900
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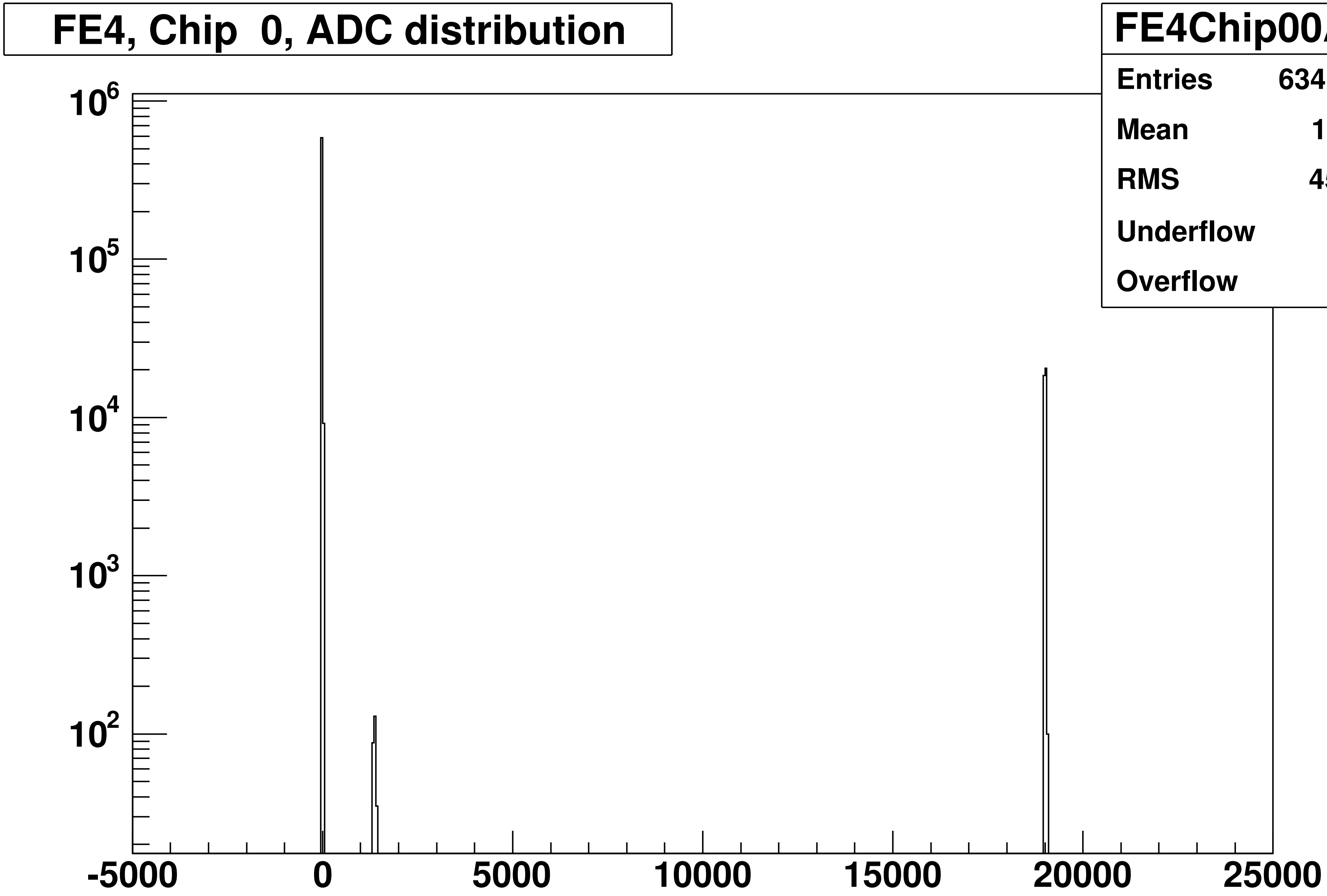
FE4, Chip 0, ADC distribution
FE4Chip00All
Entries 634158
Mean 1164
RMS 4559
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
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0
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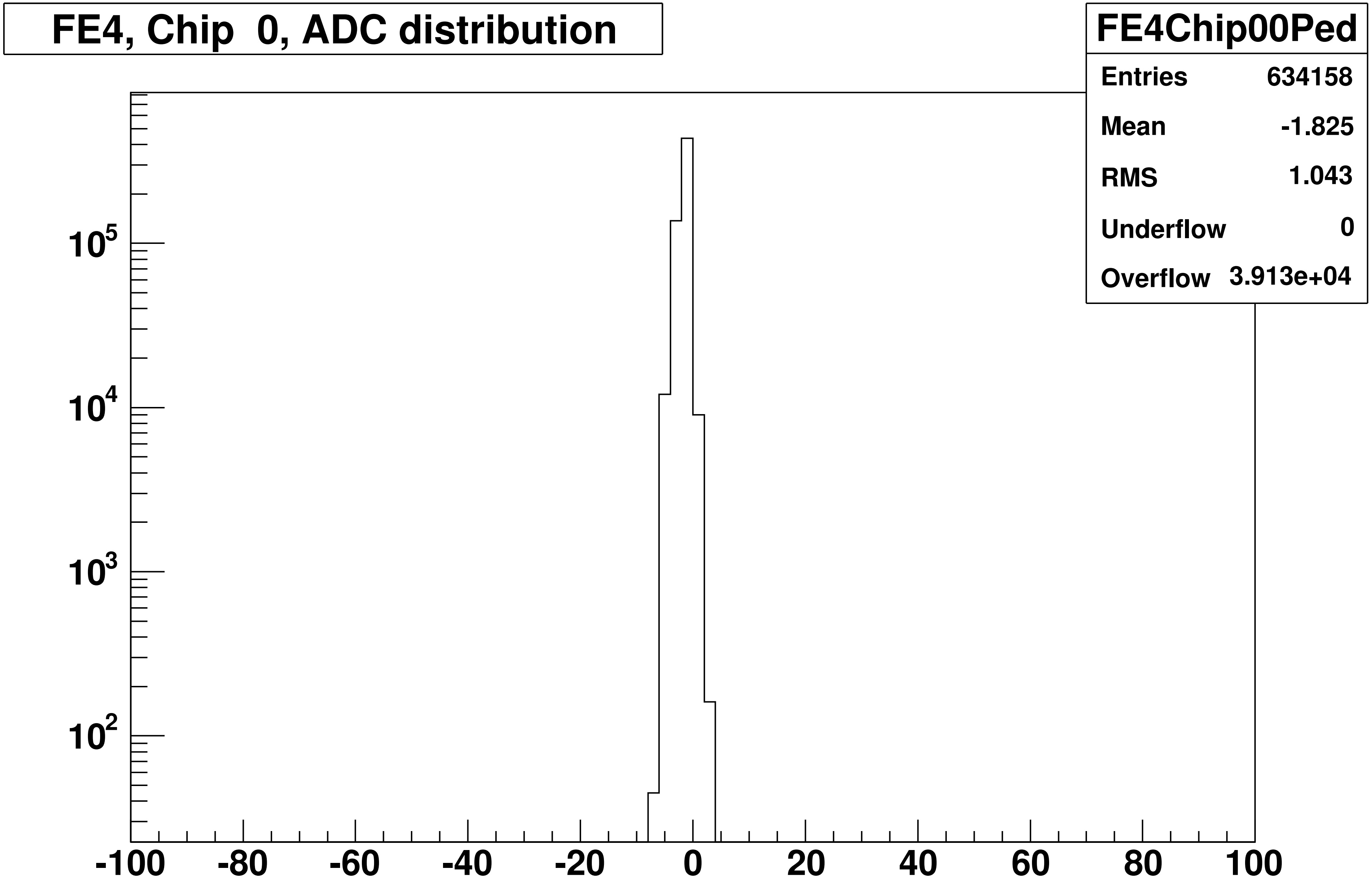
10000
15000
20000
25000


FE4, Chip 0, ADC distribution
FE4Chip00Ped
Entries 634158
Mean -1.825
RMS 1.043
Underflow 0
Overflow 3.913e+04
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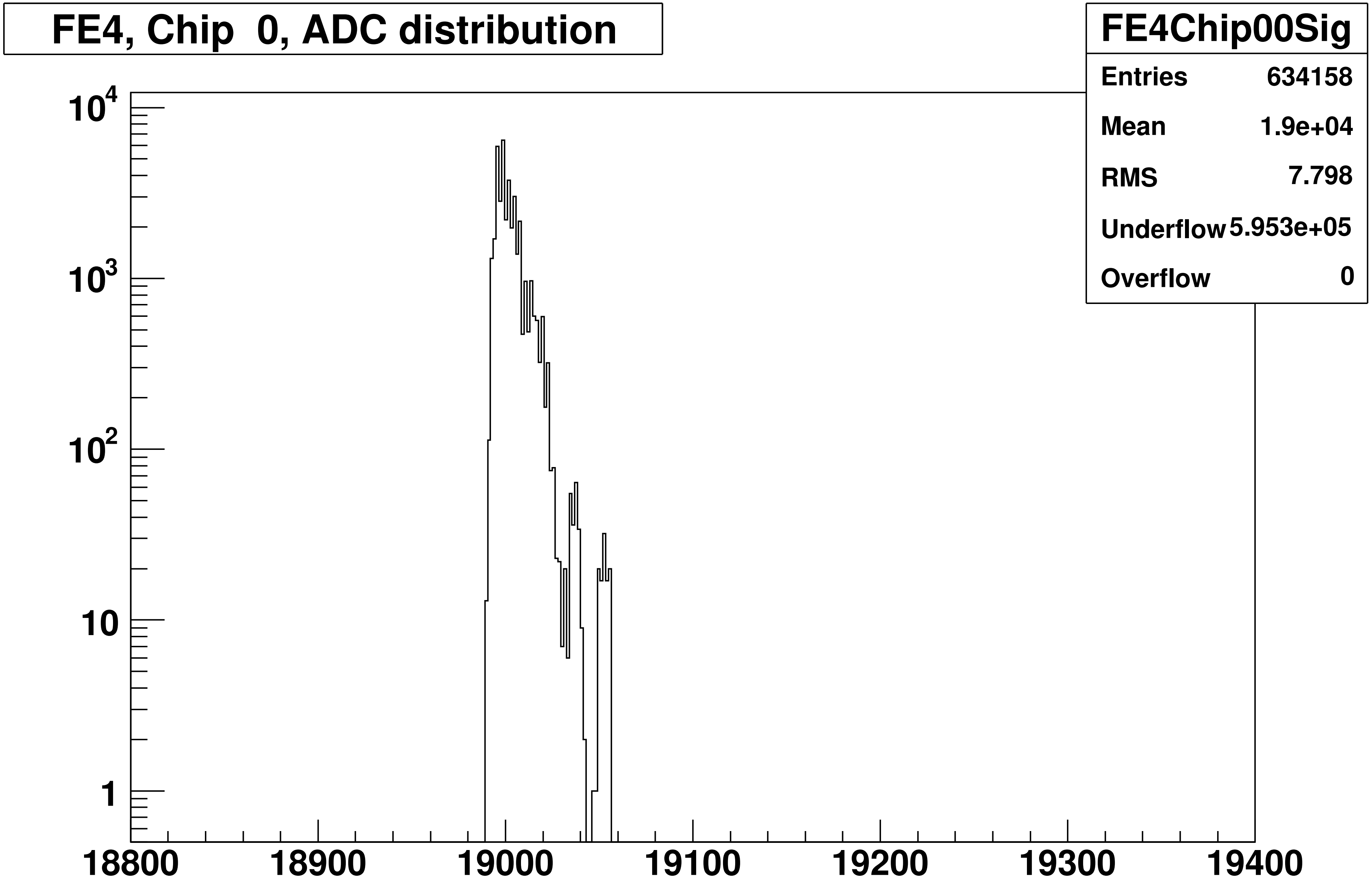
10^4
10^3
10^2
-100 -80 -60 -40 -20 0 20 40 60 80 100


FE4, Chip 0, ADC distribution
FE4Chip00Sig
Entries 634158
Mean 1.9e+04
RMS 7.798
Underflow 5.953e+05
Overflow 0
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10^3
10^2
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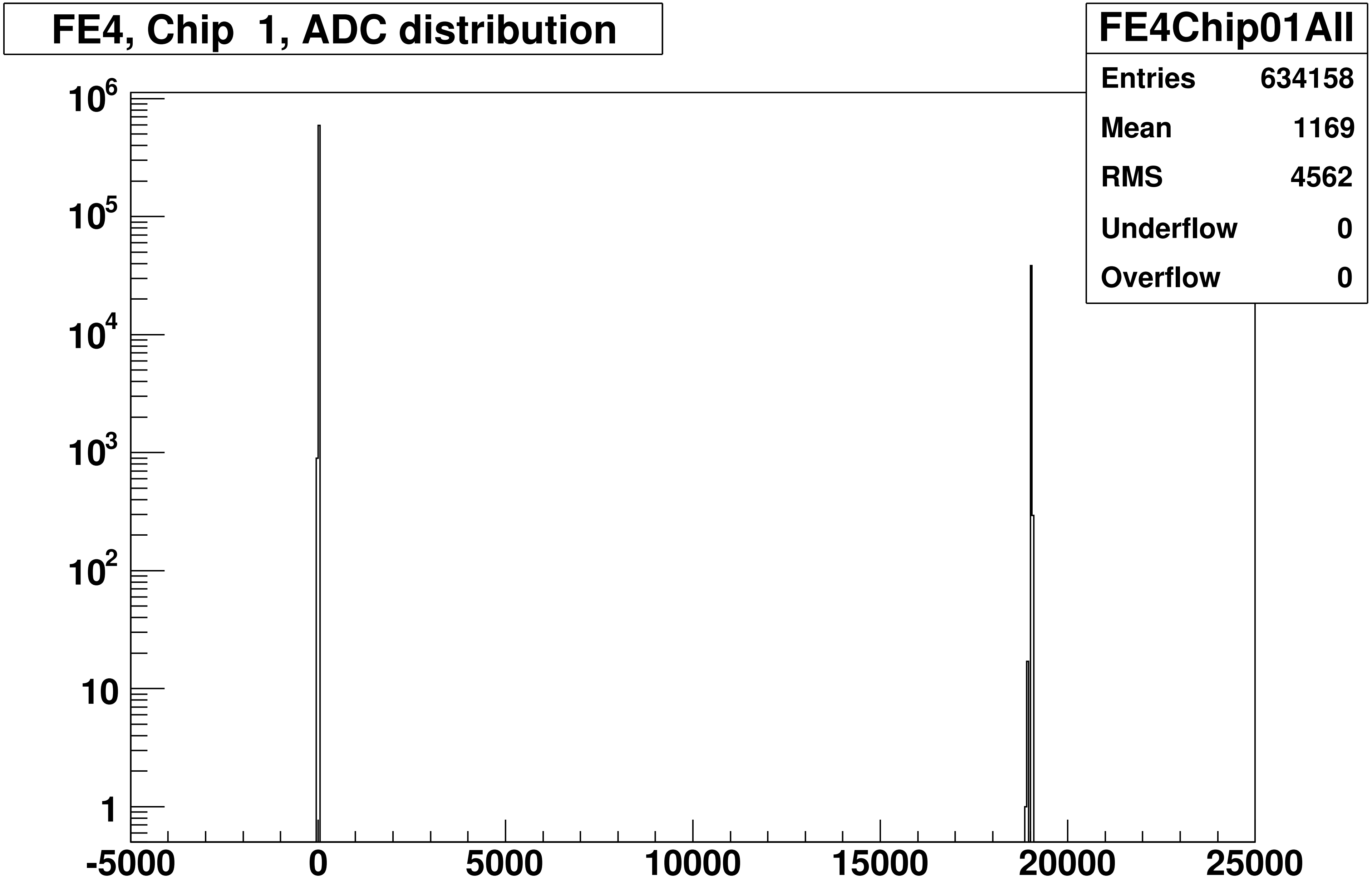
FE4, Chip 1, ADC distribution
FE4Chip01All
Entries 634158
Mean 1169
RMS 4562
Underflow 0
Overflow 0
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10^4
10^3
10^2
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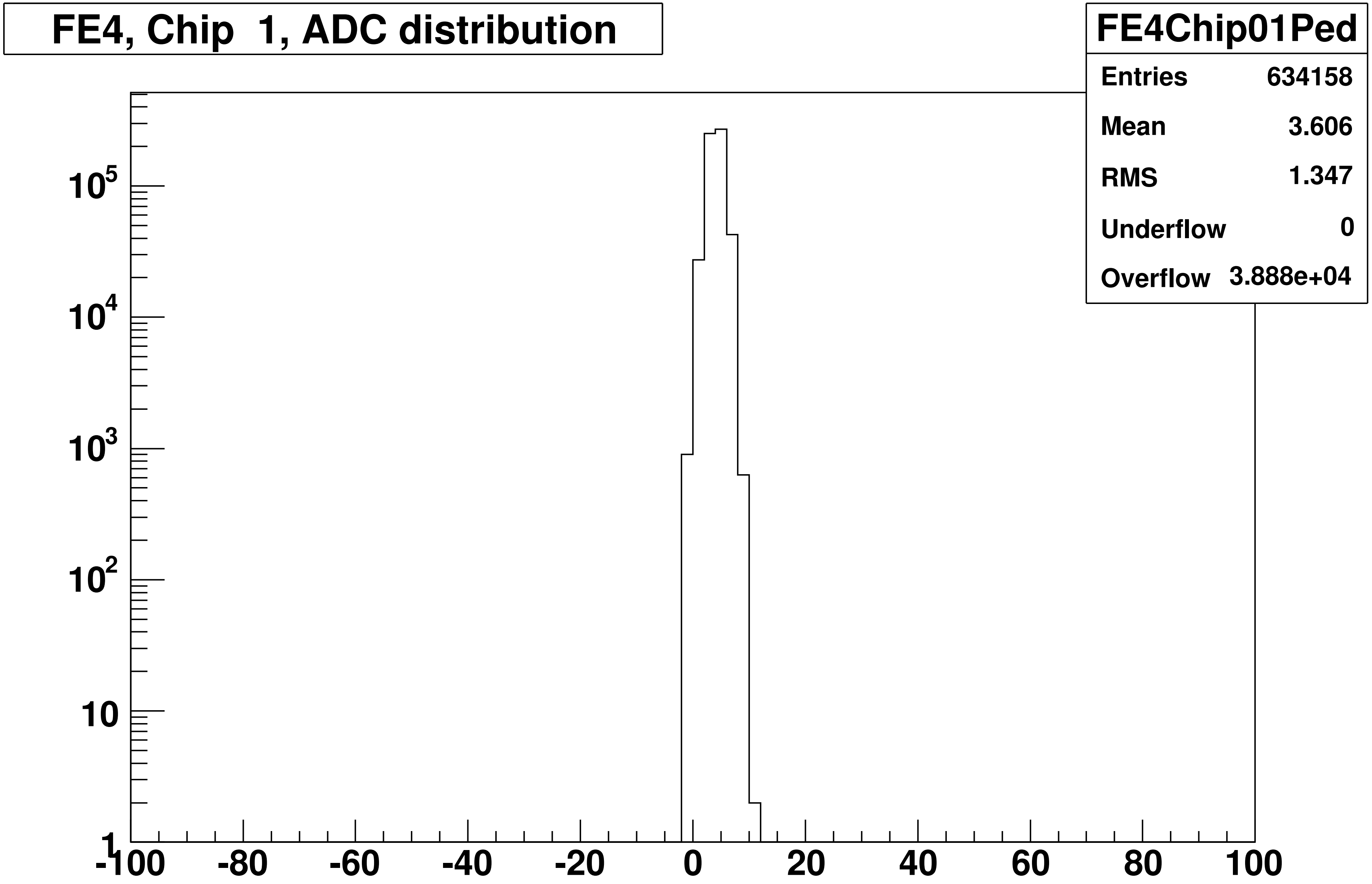

FE4, Chip 1, ADC distribution
FE4Chip01Ped
Entries 634158
Mean 3.606
RMS 1.347
Underflow 0
Overflow 3.888e+04
10^5
10^4
10^3
10^2
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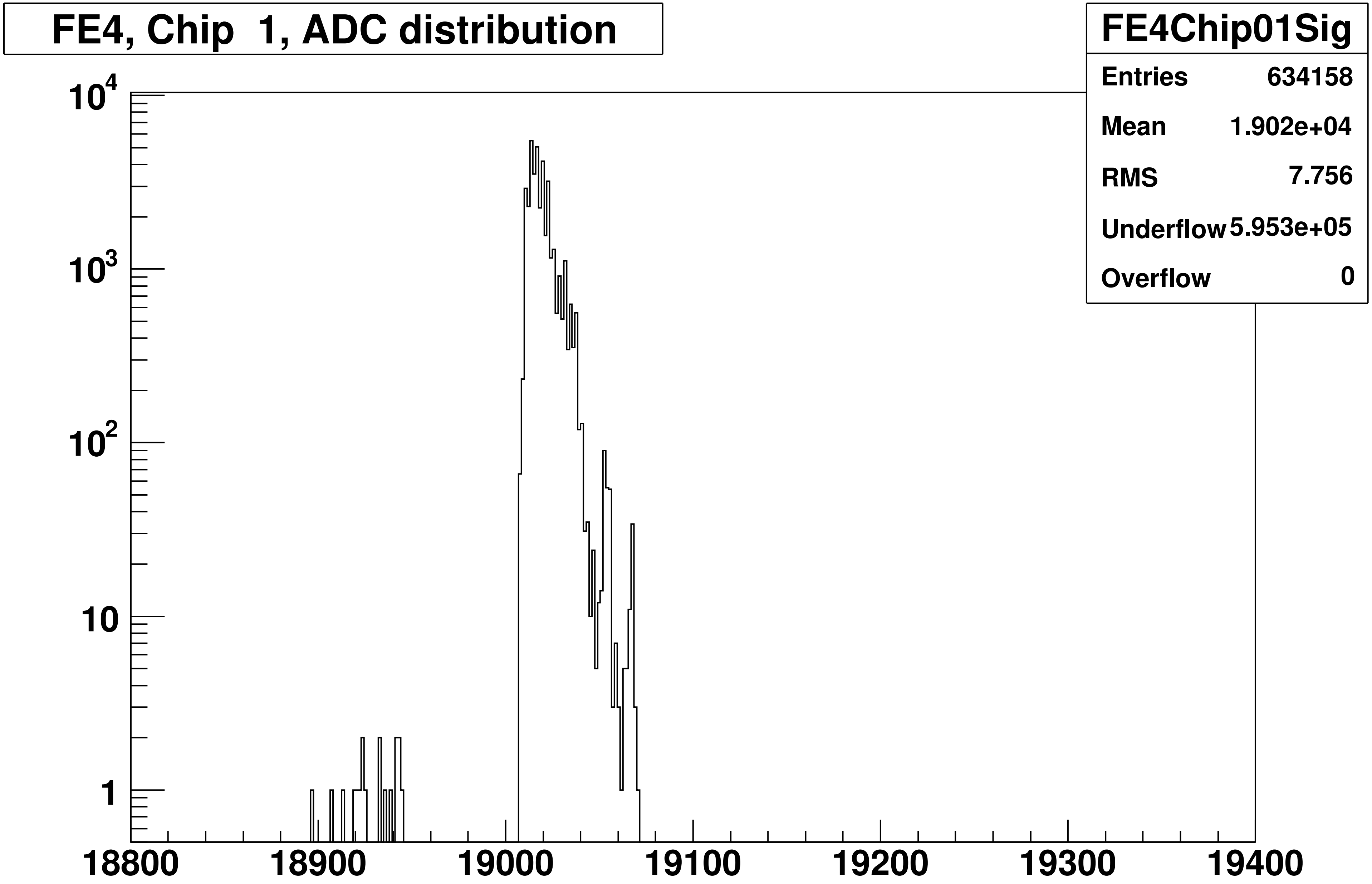
FE4, Chip 1, ADC distribution
FE4Chip01Sig
Entries 634158
Mean 1.902e+04
RMS 7.756
Underflow 5.953e+05
Overflow 0
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10^3
10^2
10
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18900
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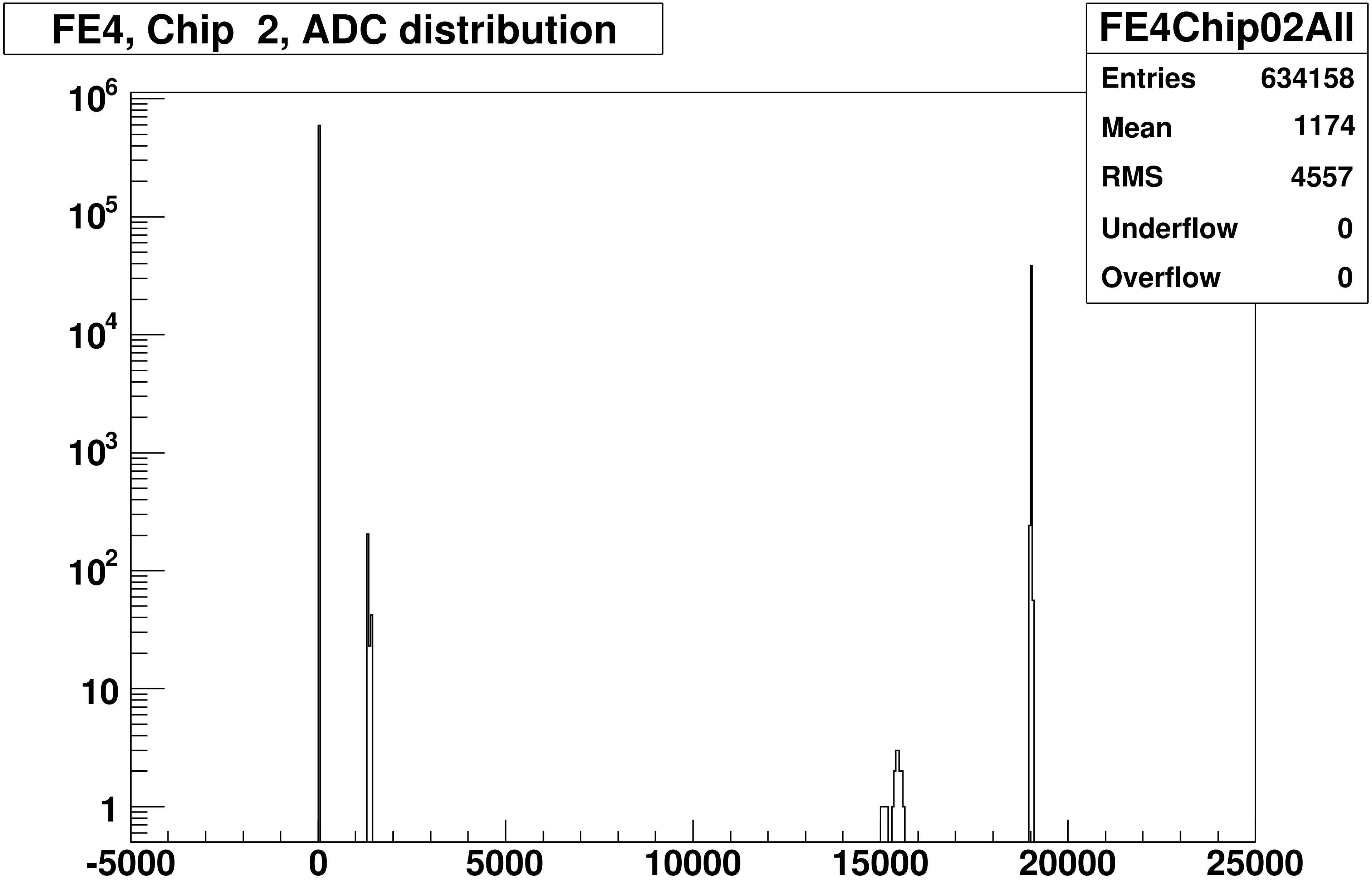
FE4, Chip 2, ADC distribution
FE4Chip02All
Entries 634158
Mean 1174
RMS 4557
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
1
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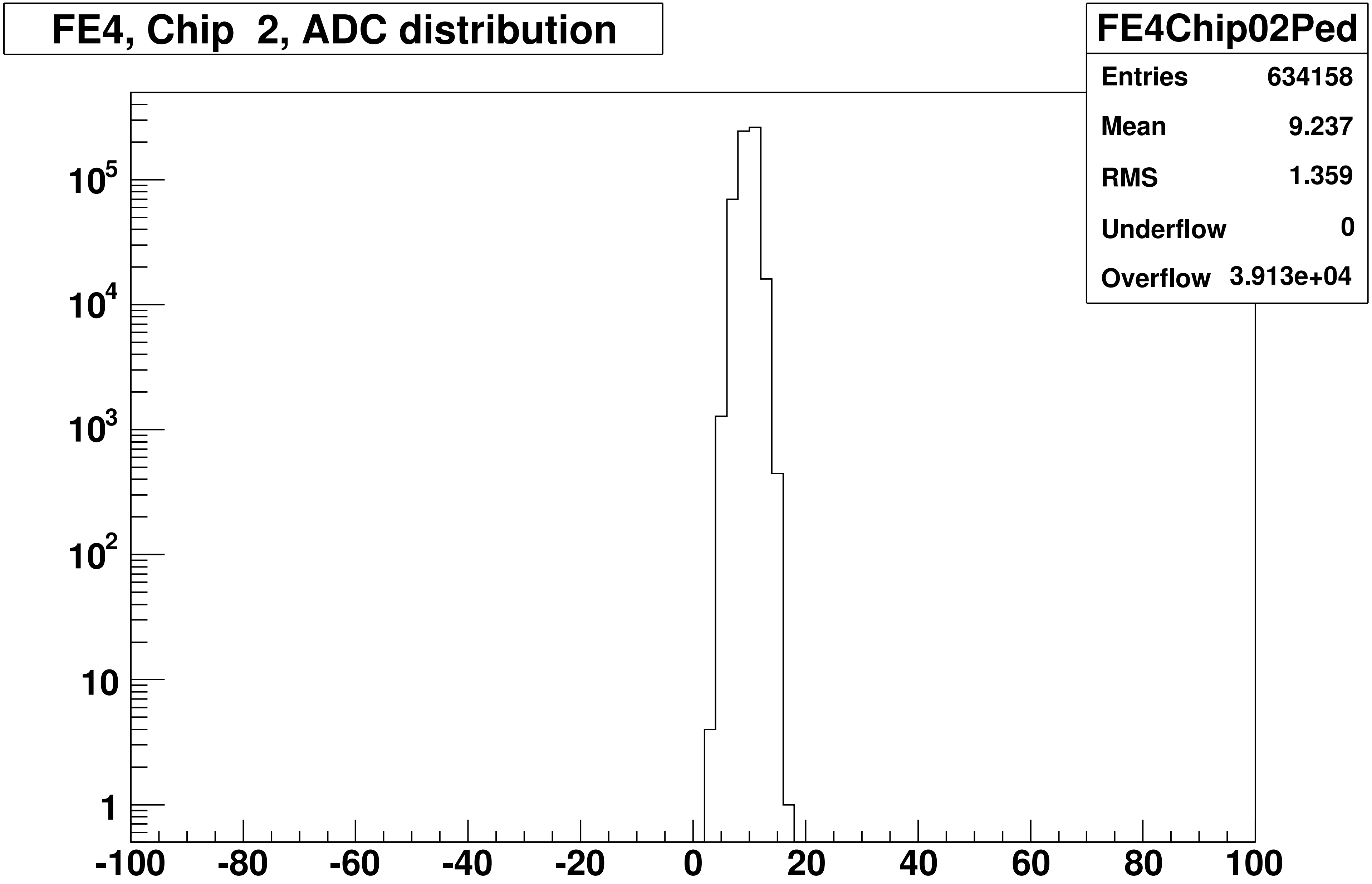

FE4, Chip 2, ADC distribution
FE4Chip02Ped
Entries 634158
Mean 9.237
RMS 1.359
Underflow 0
Overflow 3.913e+04
10^5
10^4
10^3
10^2
10
1
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-20
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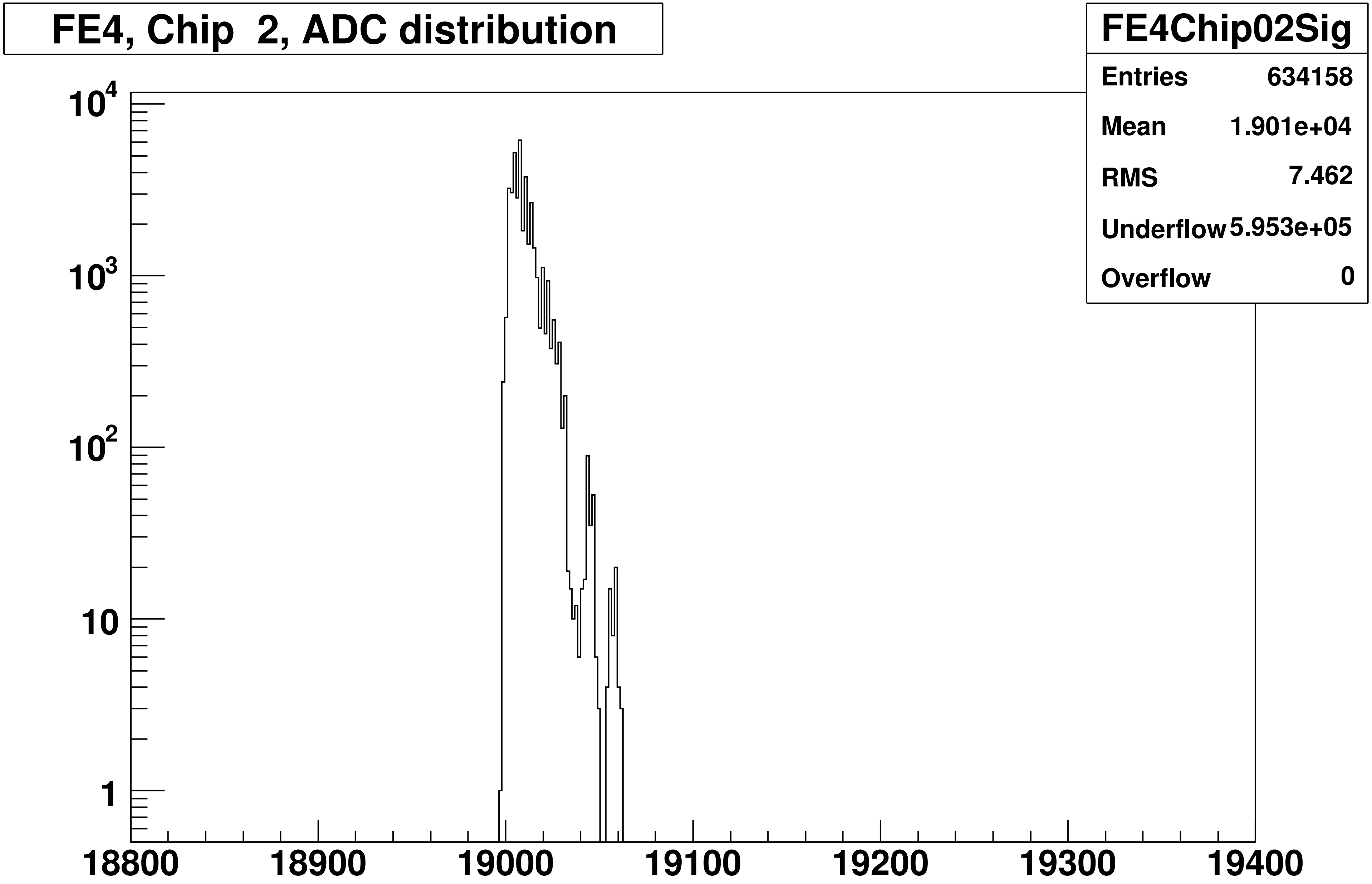

FE4, Chip 2, ADC distribution
FE4Chip02Sig
Entries 634158
Mean 1.901e+04
RMS 7.462
Underflow 5.953e+05
Overflow 0
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10^3
10^2
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18900
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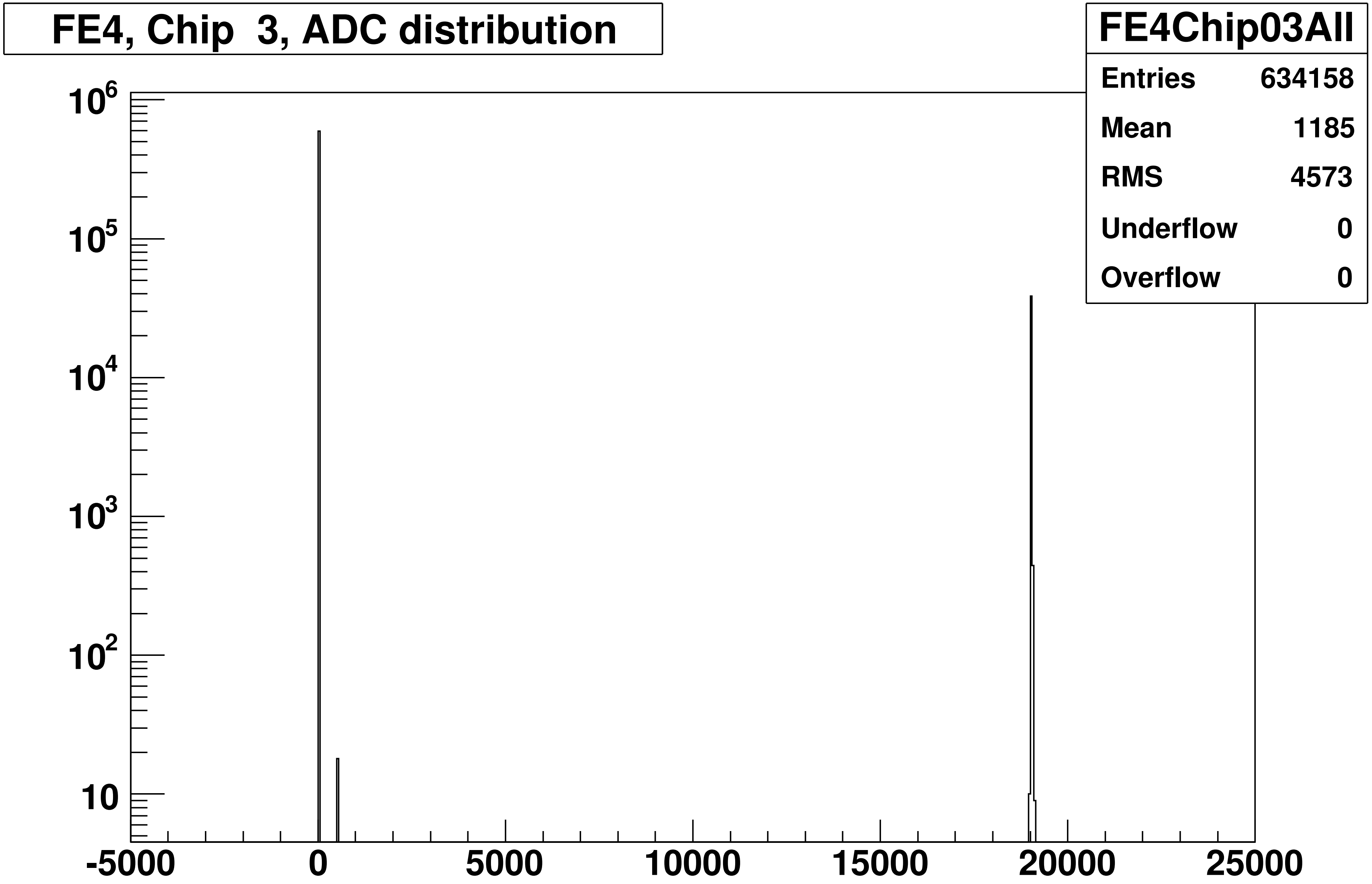
FE4, Chip 3, ADC distribution
FE4Chip03All
Entries 634158
Mean 1185
RMS 4573
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
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-5000
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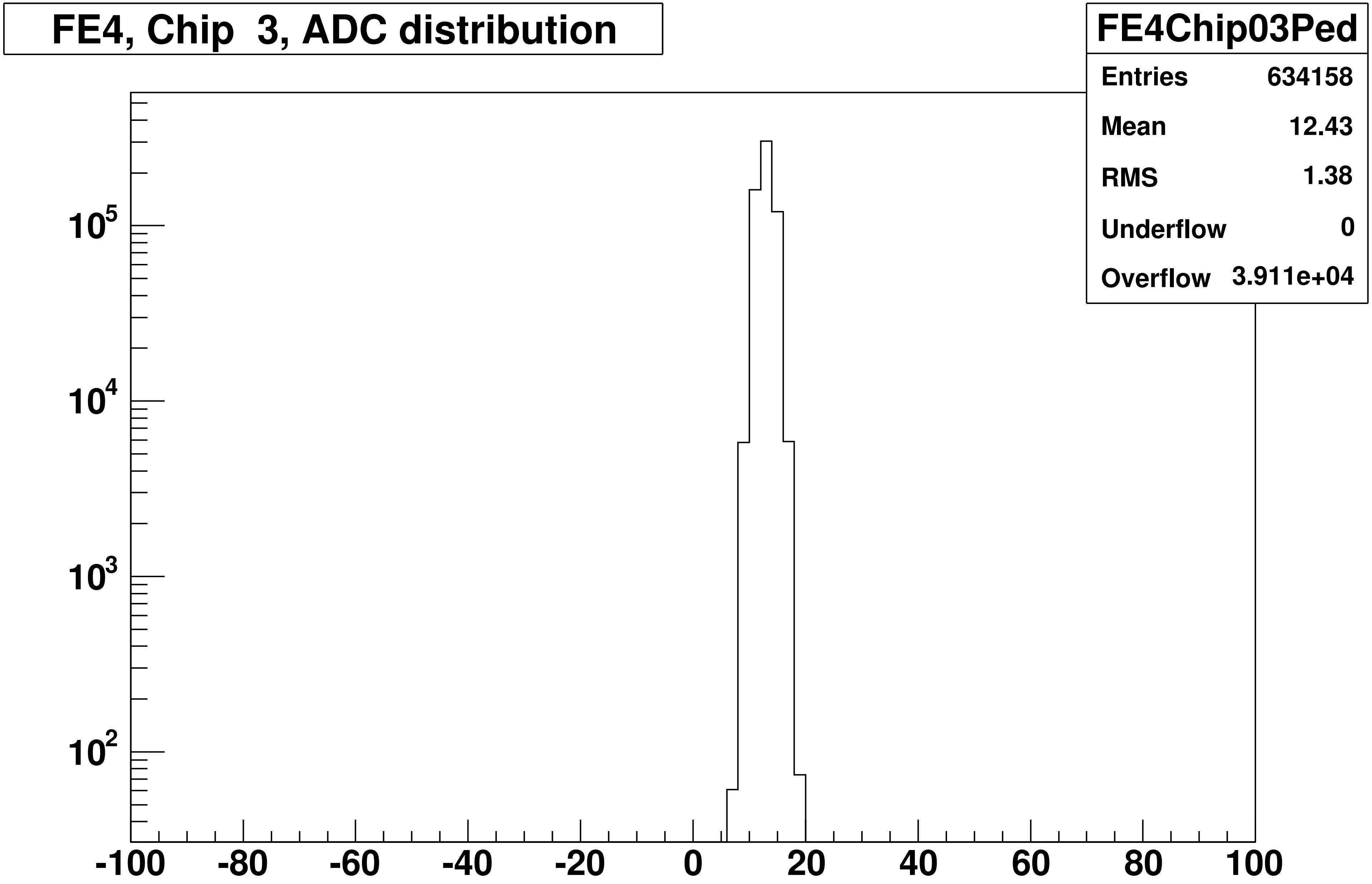
FE4, Chip 3, ADC distribution
FE4Chip03Ped
Entries 634158
Mean 12.43
RMS 1.38
Underflow 0
Overflow 3.911e+04
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10^4
10^3
10^2
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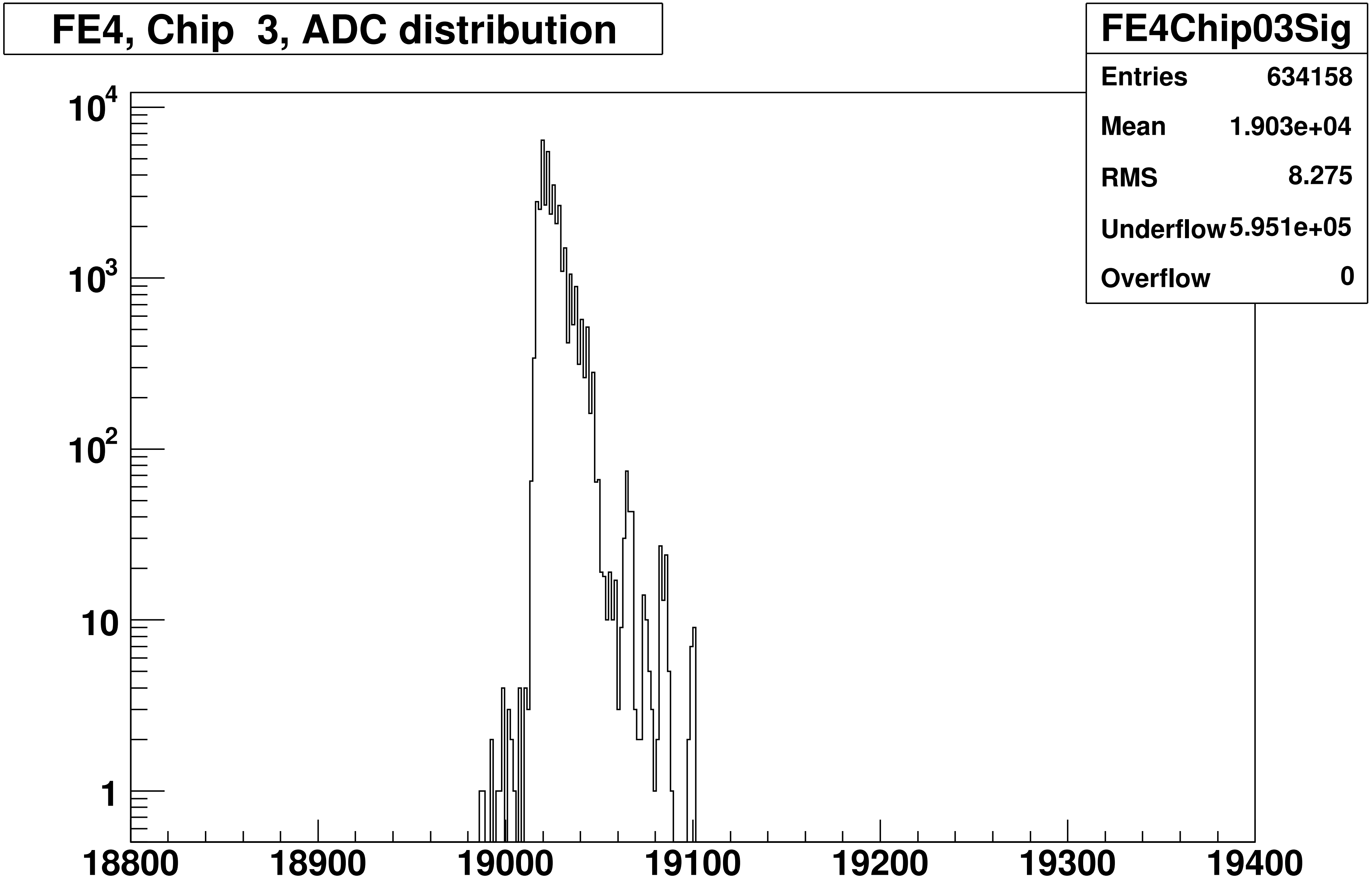
FE4, Chip 3, ADC distribution
FE4Chip03Sig
Entries 634158
Mean 1.903e+04
RMS 8.275
Underflow 5.951e+05
Overflow 0
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10^3
10^2
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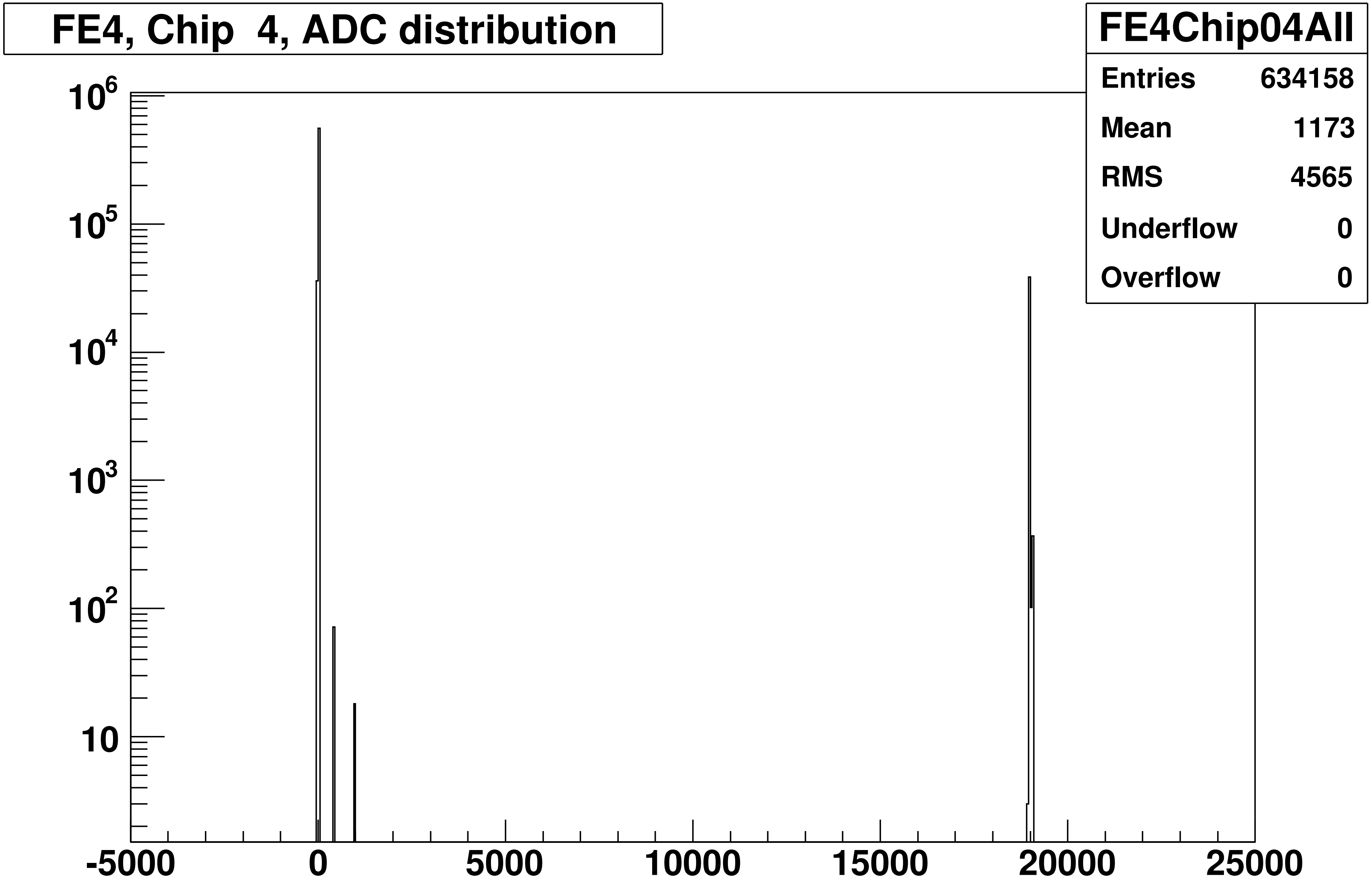
FE4, Chip 4, ADC distribution
FE4Chip04All
Entries 634158
Mean 1173
RMS 4565
Underflow 0
Overflow 0
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10^3
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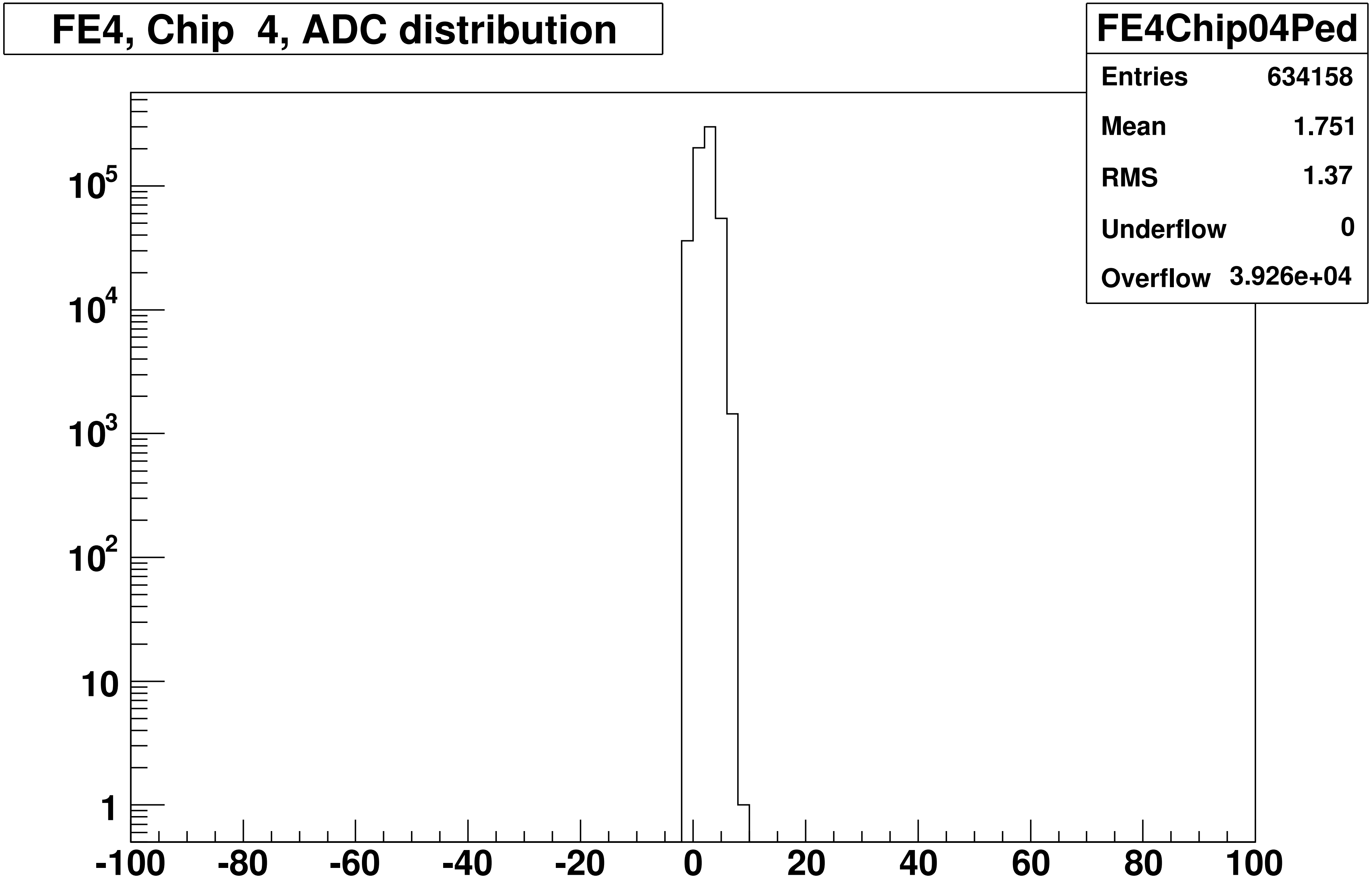
FE4, Chip 4, ADC distribution
FE4Chip04Ped
Entries 634158
Mean 1.751
RMS 1.37
Underflow 0
Overflow 3.926e+04
10^5
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10^3
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80
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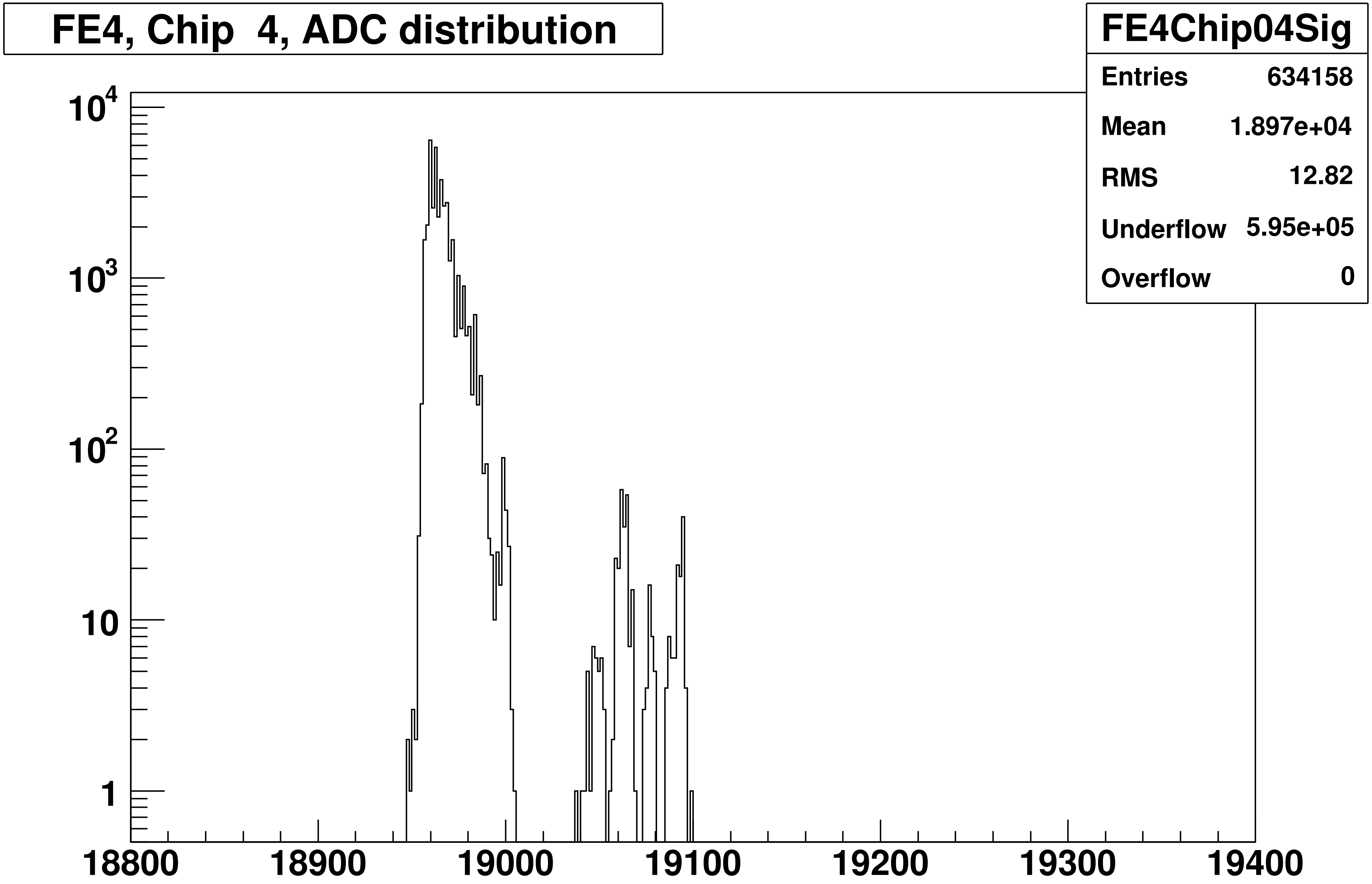
FE4, Chip 4, ADC distribution
FE4Chip04Sig
Entries 634158
Mean 1.897e+04
RMS 12.82
Underflow 5.95e+05
Overflow 0
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10^3
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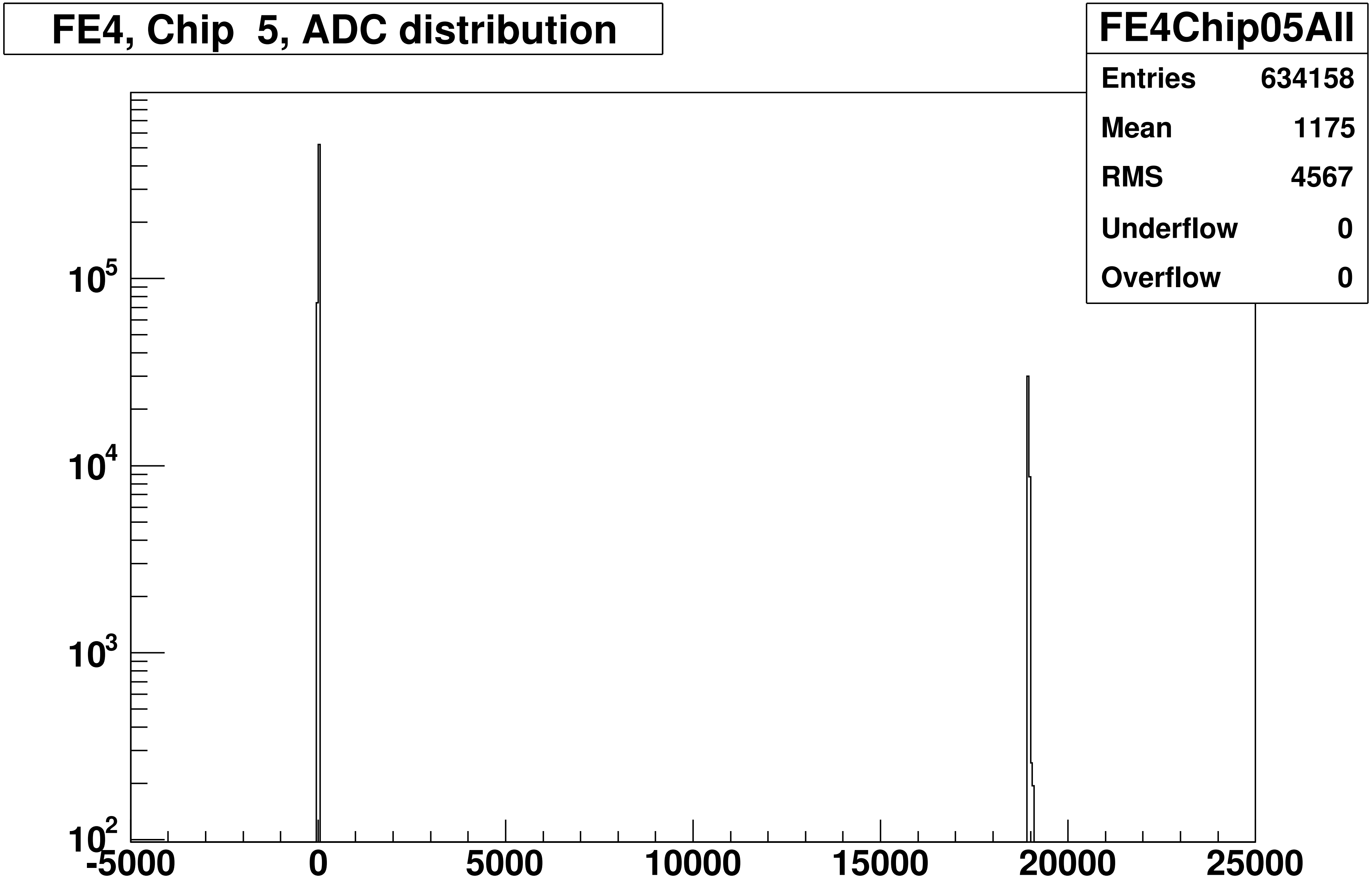
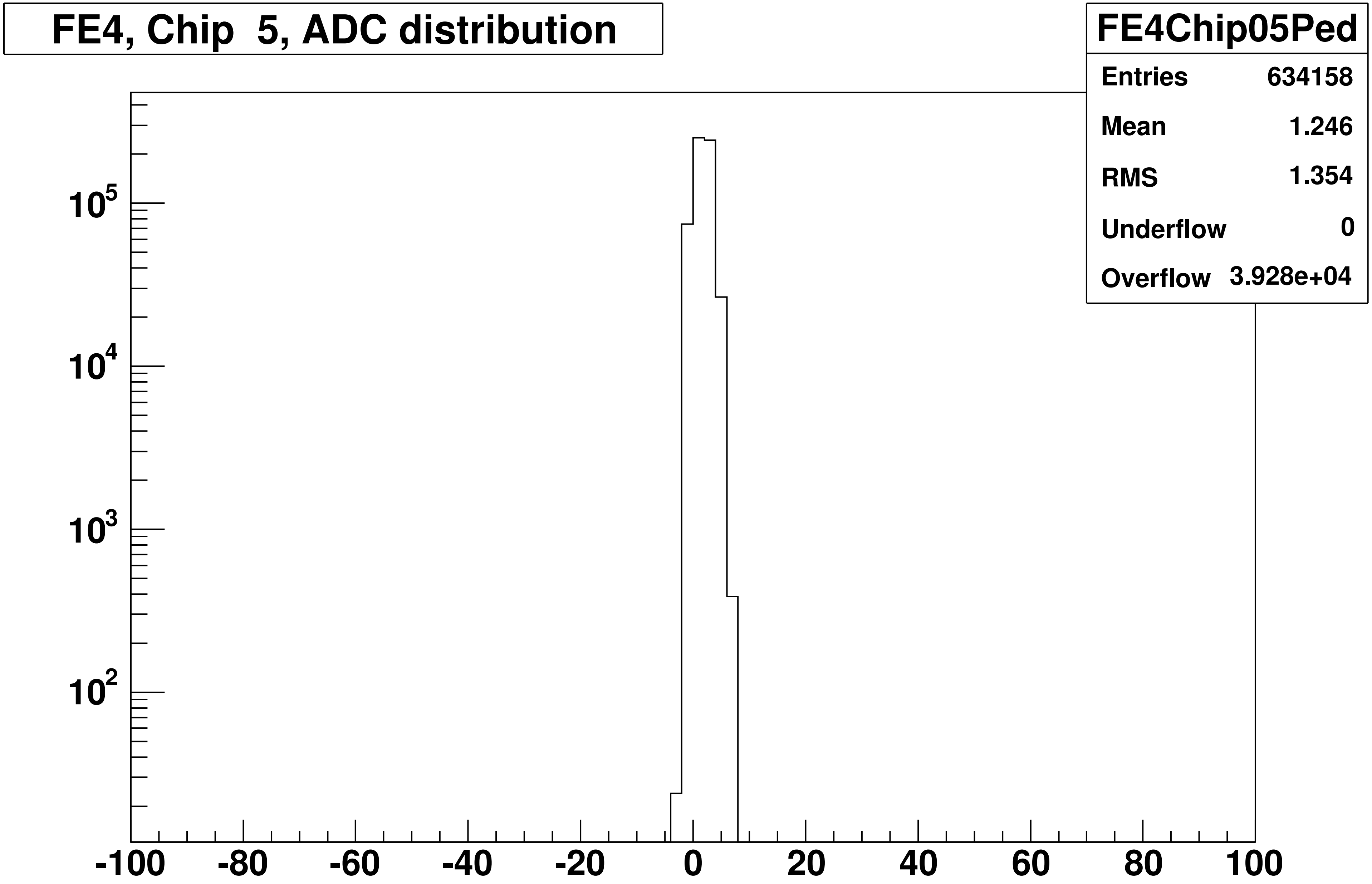
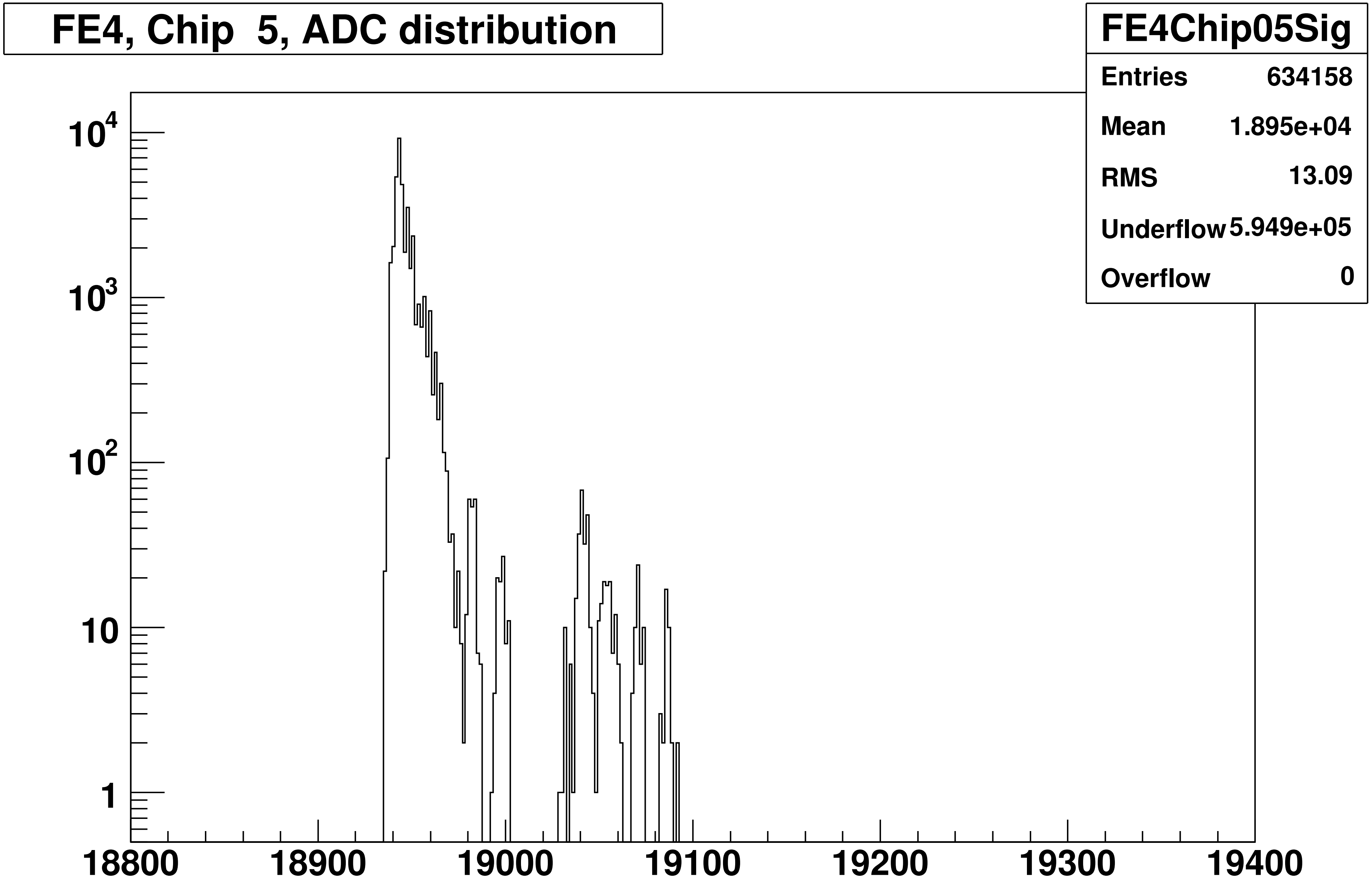

FE4, Chip 5, ADC distribution
FE4Chip05All
Entries 634158
Mean 1175
RMS 4567
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000


FE4, Chip 5, ADC distribution
FE4Chip05Ped
Entries 634158
Mean 1.246
RMS 1.354
Underflow 0
Overflow 3.928e+04
10^5
10^4
10^3
10^2
-100 -80 -60 -40 -20 0 20 40 60 80 100


FE4, Chip 5, ADC distribution
FE4Chip05Sig
Entries 634158
Mean 1.895e+04
RMS 13.09
Underflow 5.949e+05
Overflow 0
10^4
10^3
10^2
10
1
18800
18900
19000
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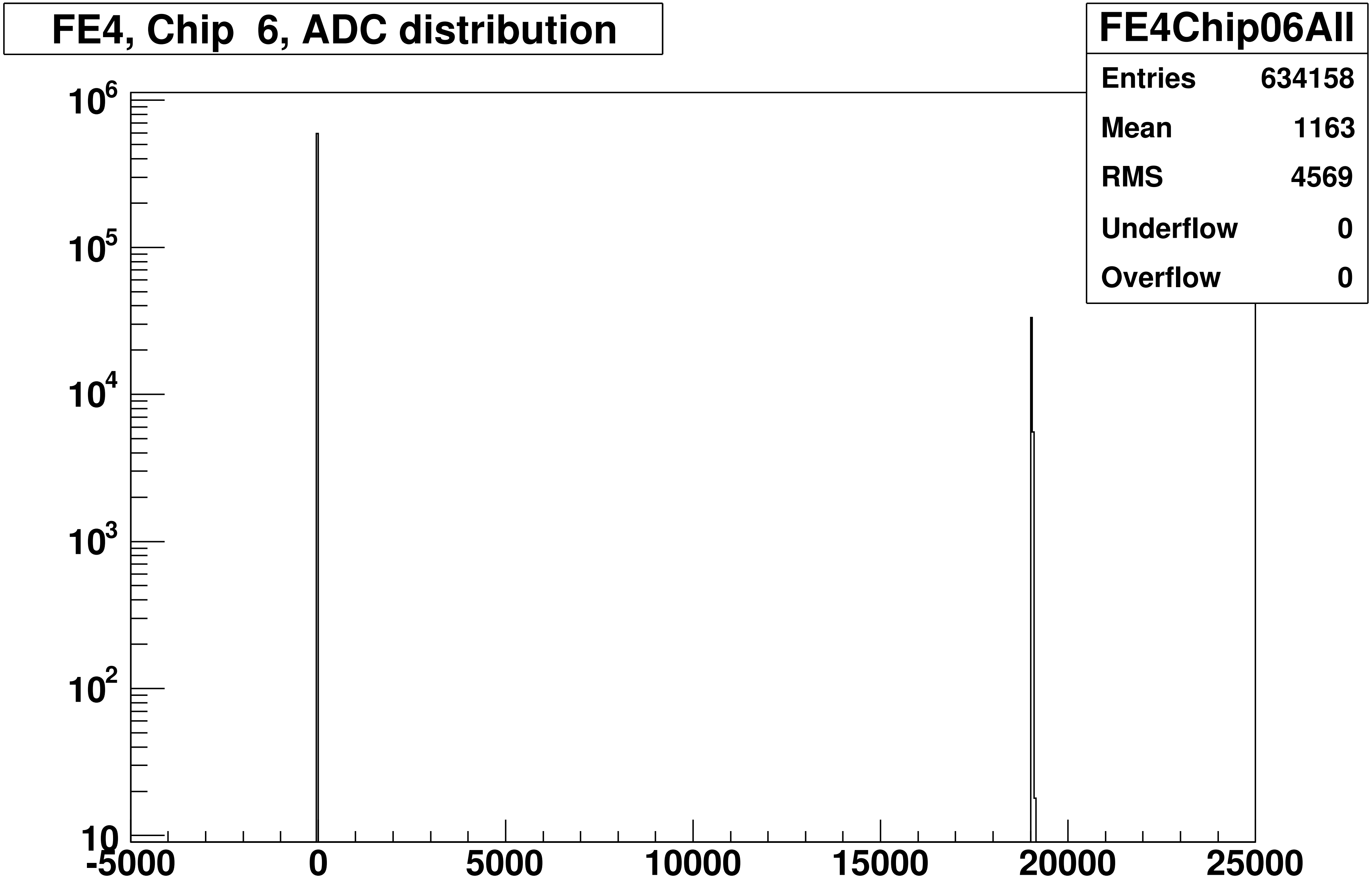
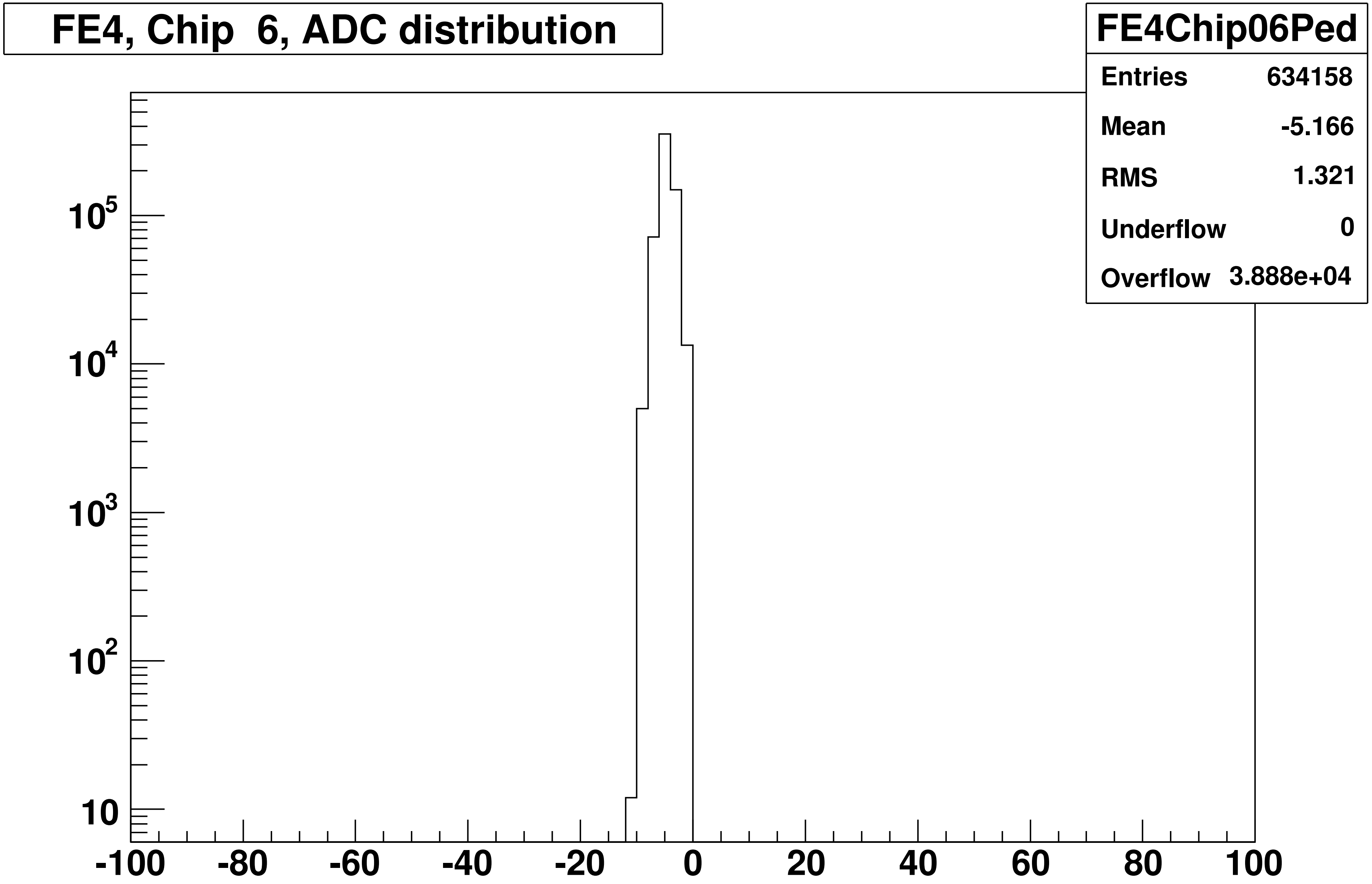
19200
19300
19400


FE4, Chip 6, ADC distribution
FE4Chip06All
Entries 634158
Mean 1163
RMS 4569
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE4, Chip 6, ADC distribution
FE4Chip06Ped
Entries 634158
Mean -5.166
RMS 1.321
Underflow 0
Overflow 3.888e+04
10^5
10^4
10^3
10^2
10
-100
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-60
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-20
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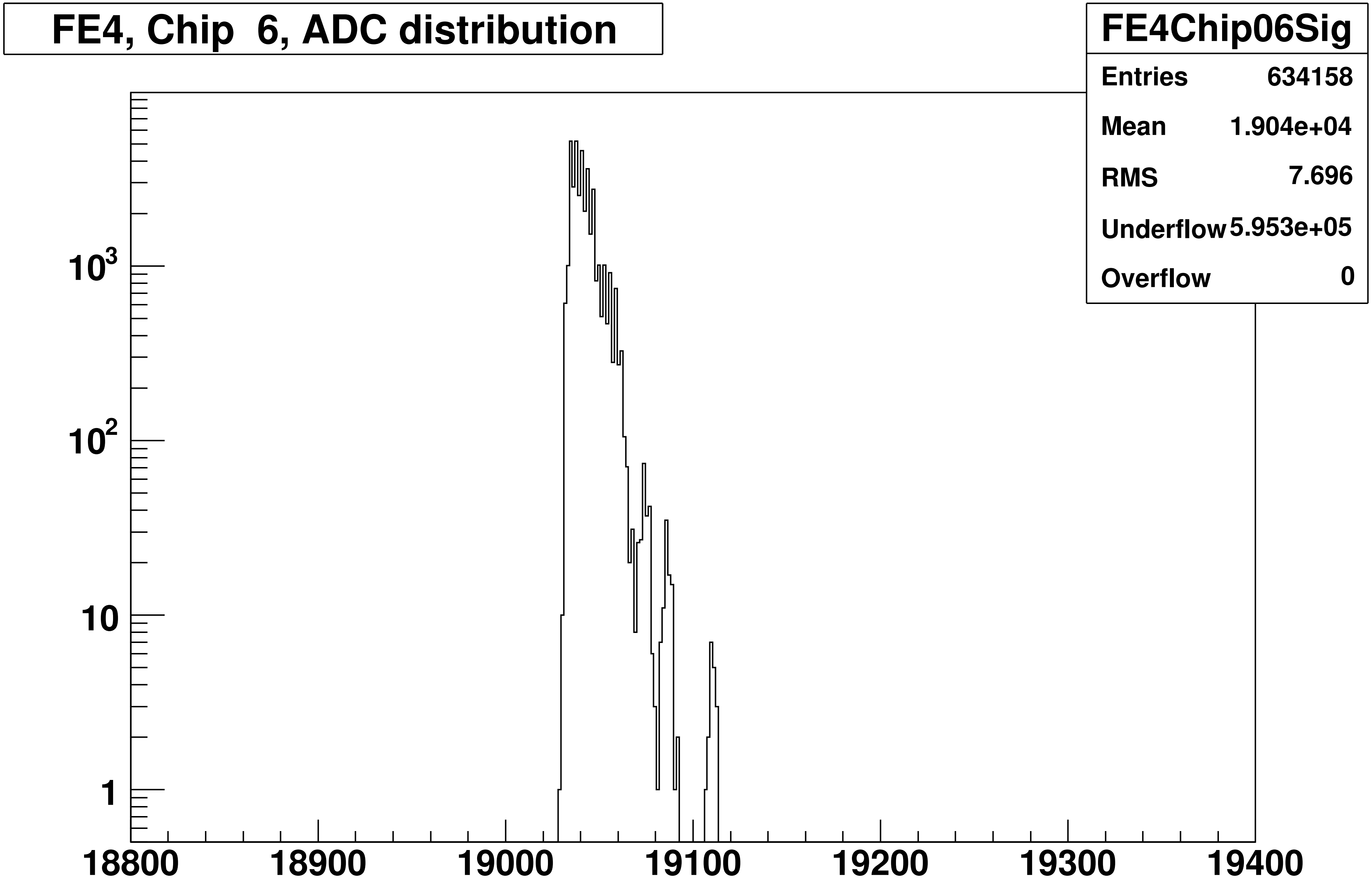
40
60
80
100


FE4, Chip 6, ADC distribution
FE4Chip06Sig
Entries 634158
Mean 1.904e+04
RMS 7.696
Underflow 5.953e+05
Overflow 0
10^3
10^2
10
1
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18900
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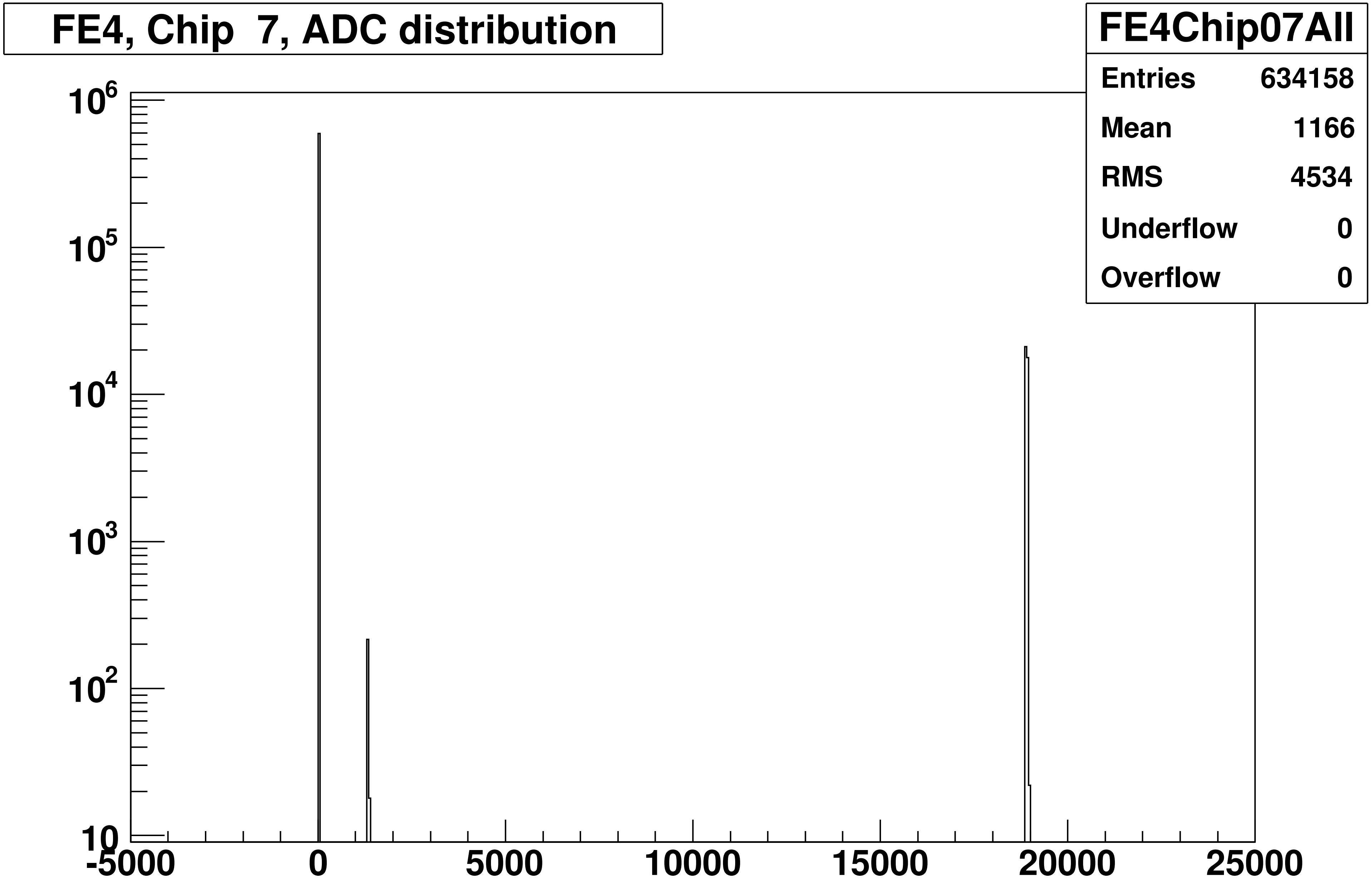
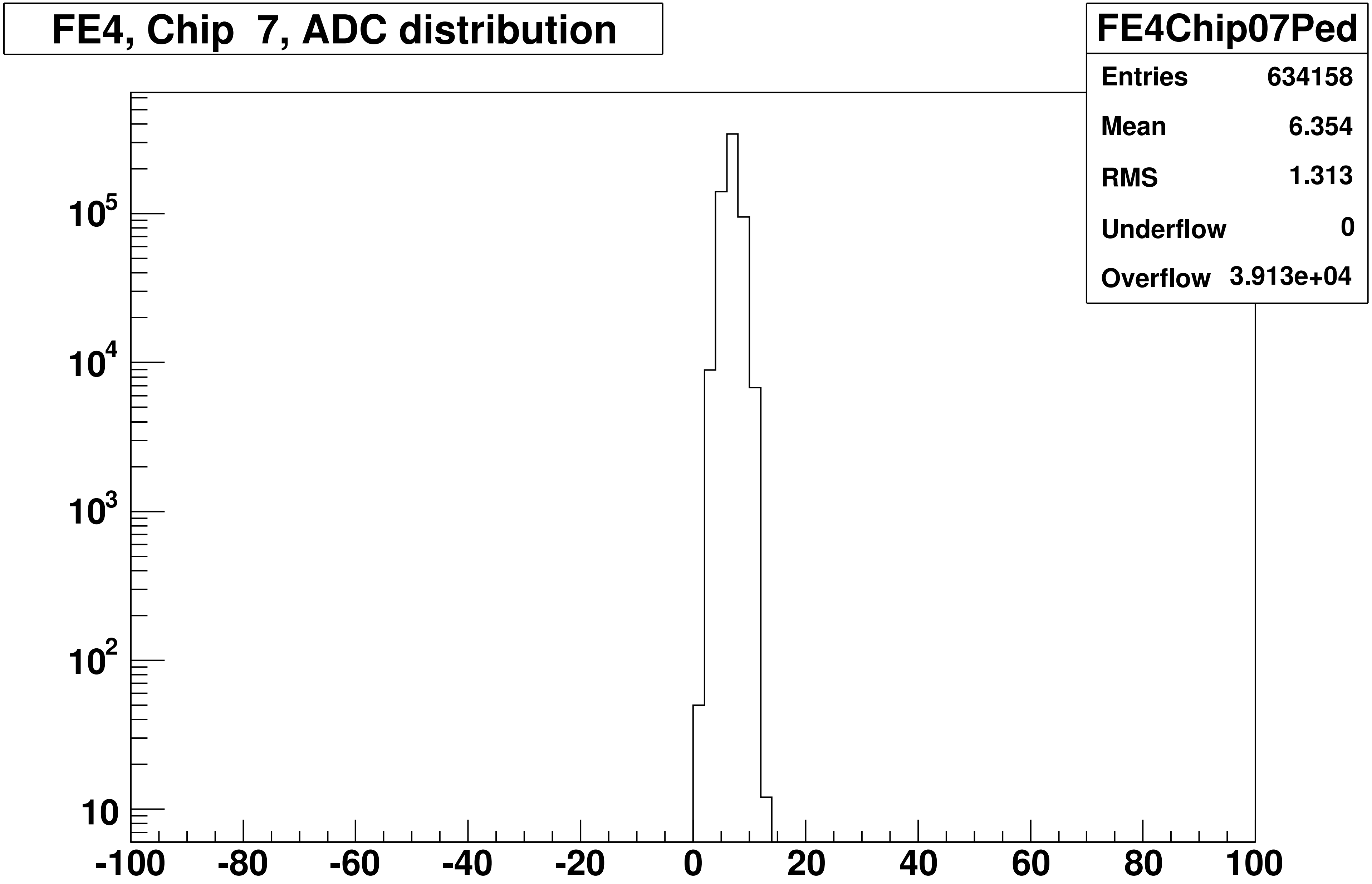


FE4, Chip 7, ADC distribution
FE4Chip07All
Entries 634158
Mean 1166
RMS 4534
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000



FE4, Chip 7, ADC distribution
FE4Chip07Ped
Entries 634158
Mean 6.354
RMS 1.313
Underflow 0
Overflow 3.913e+04
10
10^2
10^3
10^4
10^5
-100
-80
-60
-40
-20
0
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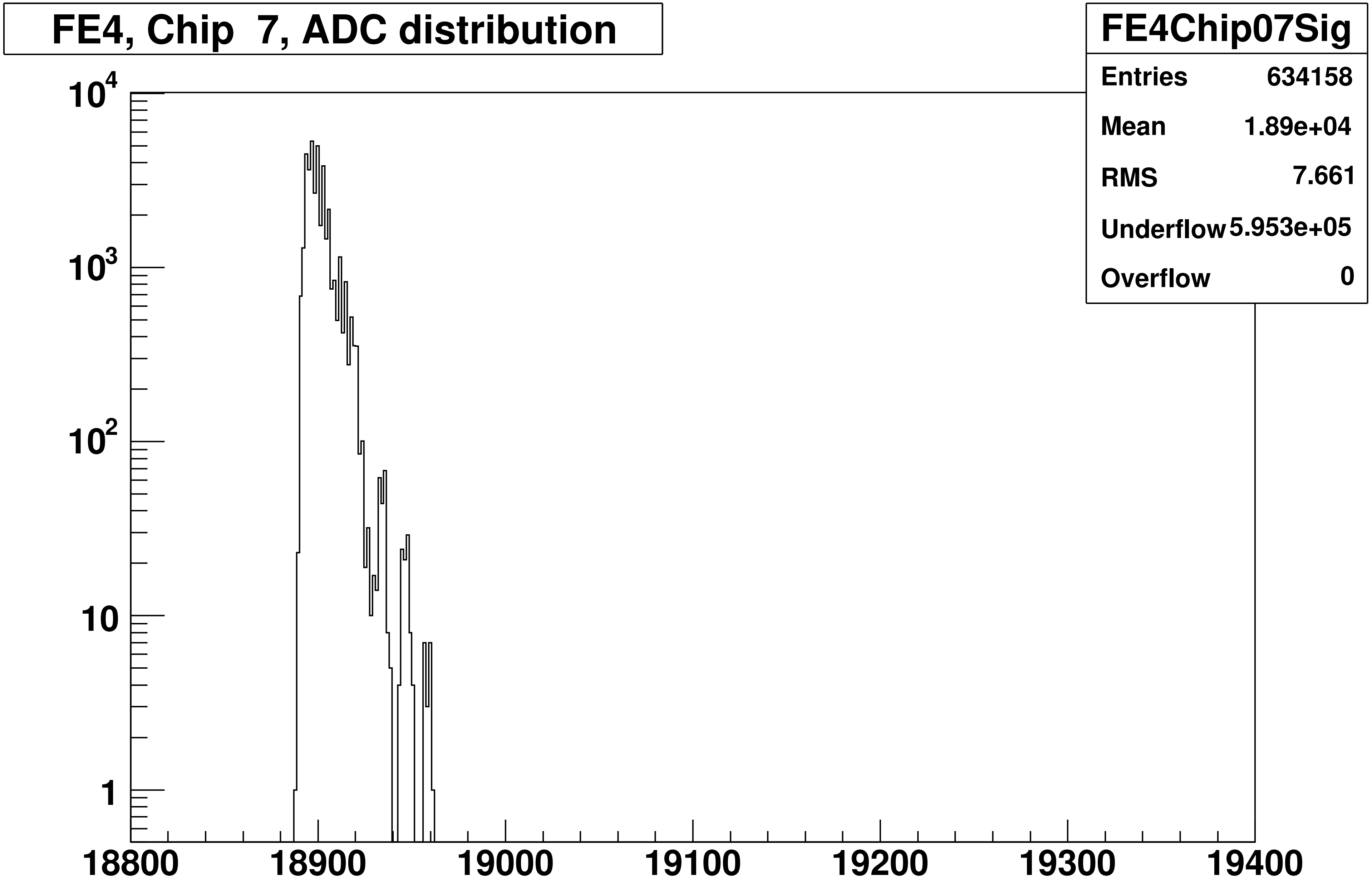
40
60
80
100



FE4, Chip 7, ADC distribution
FE4Chip07Sig
Entries 634158
Mean 1.89e+04
RMS 7.661
Underflow 5.953e+05
Overflow 0
10^4
10^3
10^2
10
1
18800
18900
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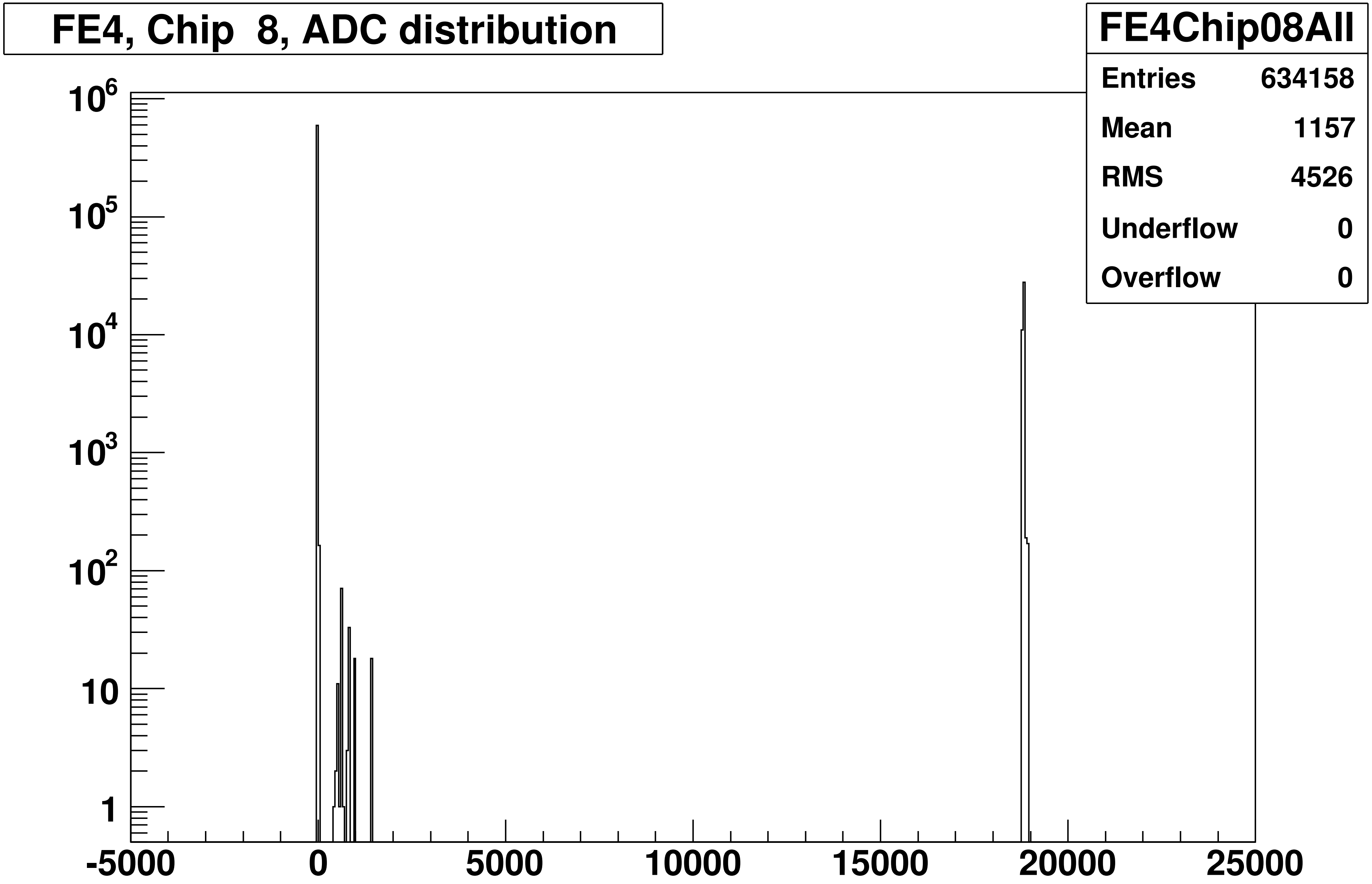
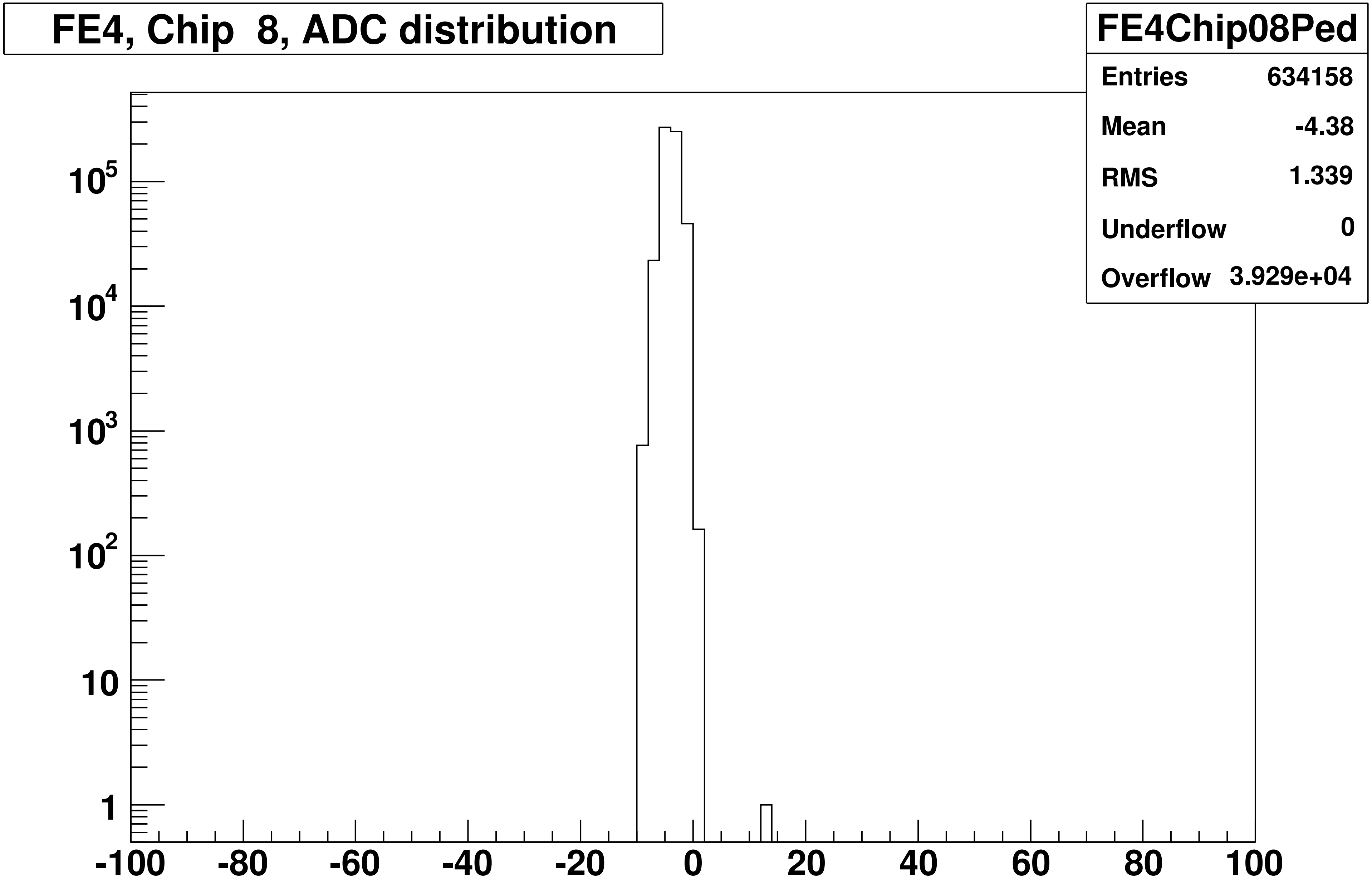
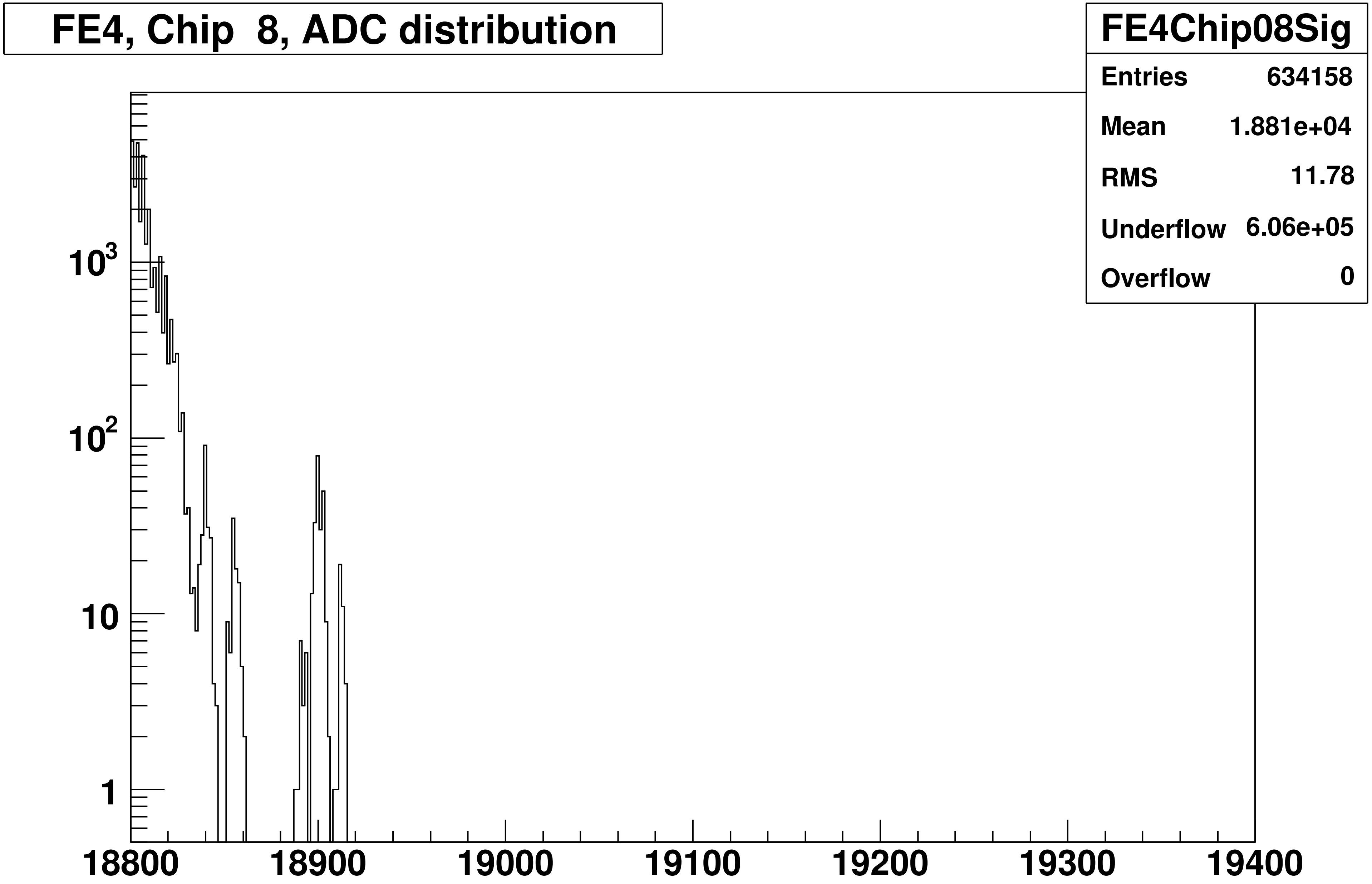

FE4, Chip 8, ADC distribution
FE4Chip08All
Entries 634158
Mean 1157
RMS 4526
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE4, Chip 8, ADC distribution
FE4Chip08Ped
Entries 634158
Mean -4.38
RMS 1.339
Underflow 0
Overflow 3.929e+04
1
10
10^2
10^3
10^4
10^5
-100
-80
-60
-40
-20
0
20
40
60
80
100


FE4, Chip 8, ADC distribution
FE4Chip08Sig
Entries 634158
Mean 1.881e+04
RMS 11.78
Underflow 6.06e+05
Overflow 0
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10^2
10
1
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18900
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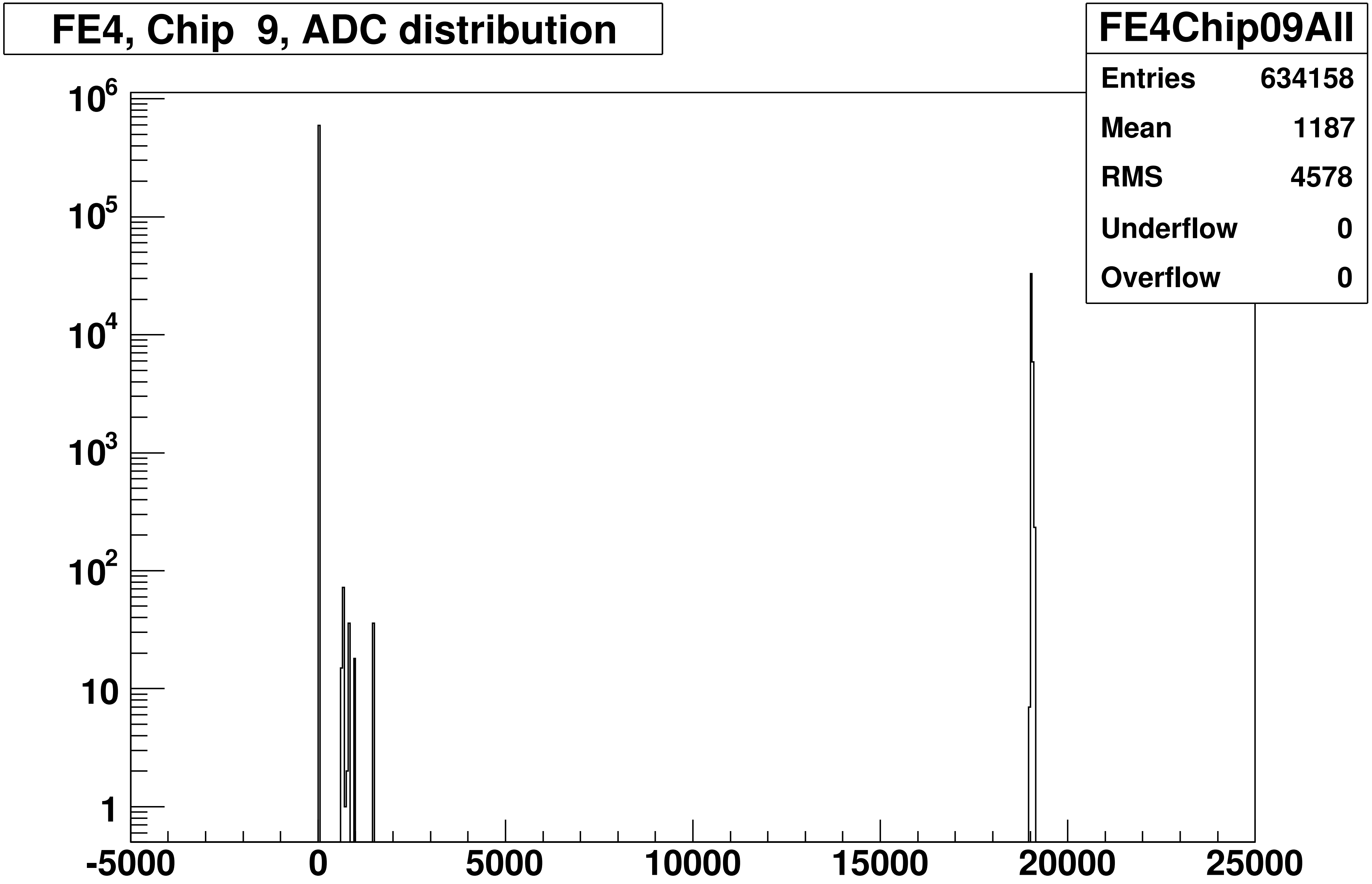
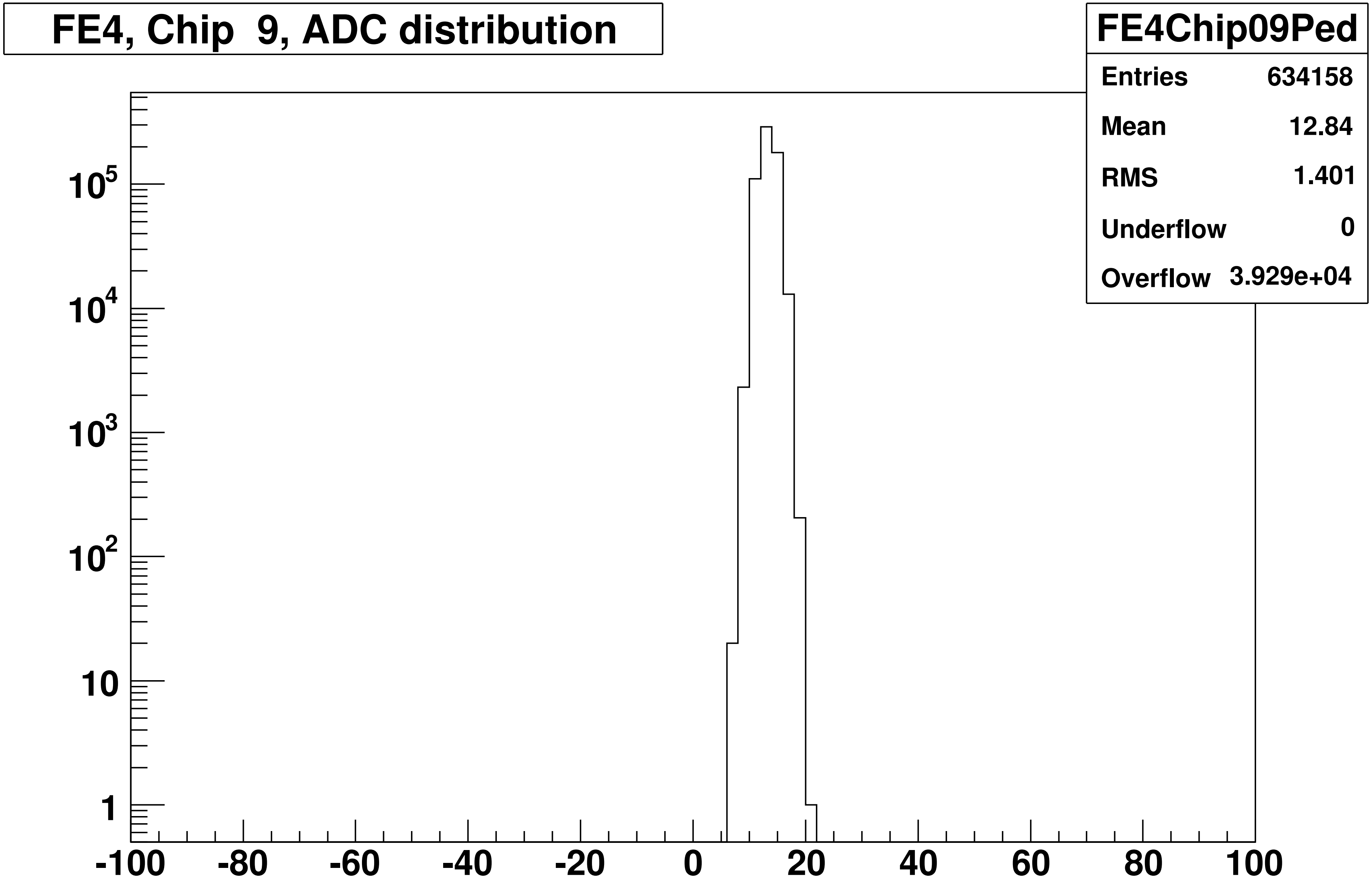
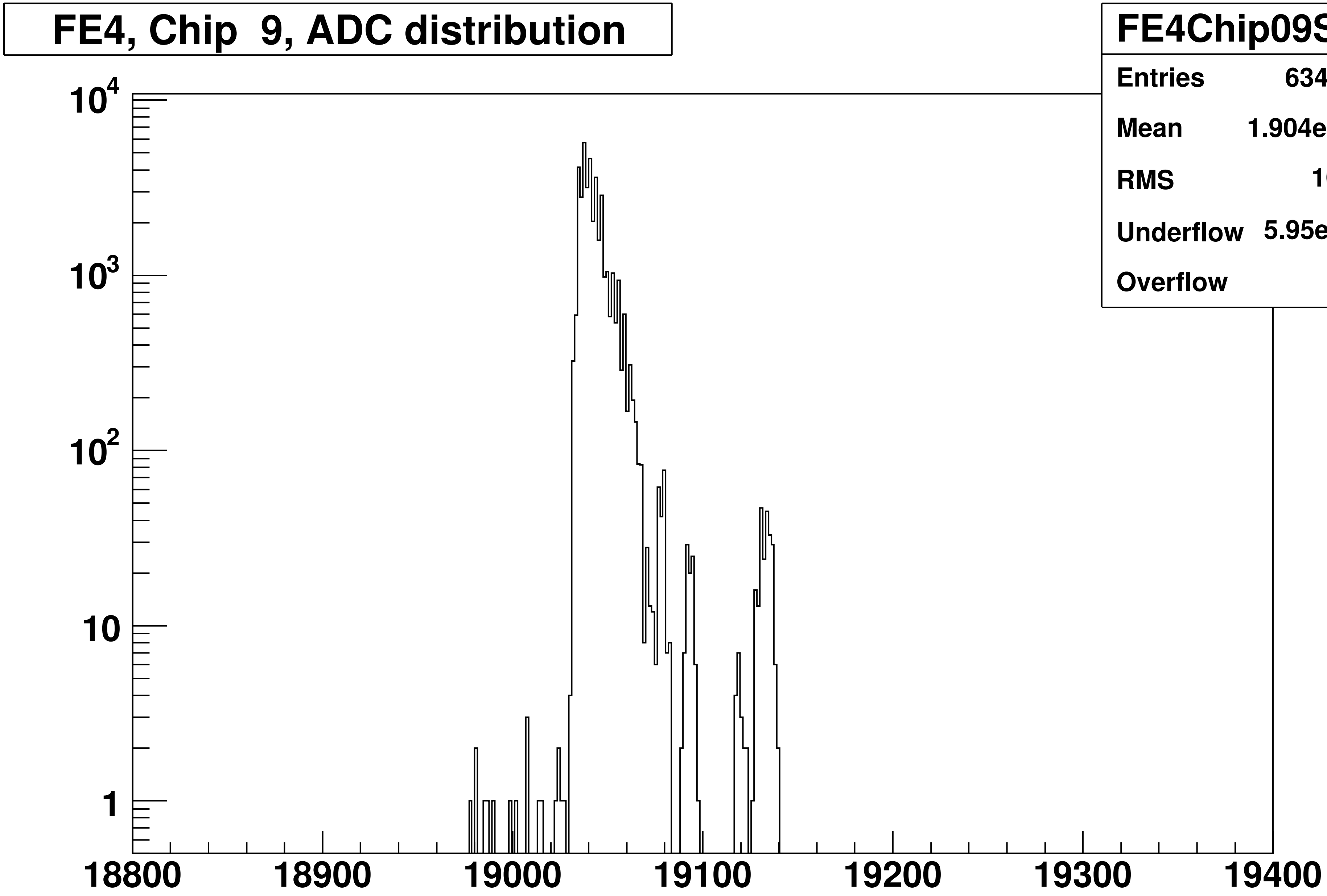
19300
19400


FE4, Chip 9, ADC distribution
FE4Chip09All
Entries 634158
Mean 1187
RMS 4578
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE4, Chip 9, ADC distribution
FE4Chip09Ped
Entries 634158
Mean 12.84
RMS 1.401
Underflow 0
Overflow 3.929e+04
10^5
10^4
10^3
10^2
10
1
-100
-80
-60
-40
-20
0
20
40
60
80
100


FE4, Chip 9, ADC distribution
FE4Chip09Sig
Entries 634158
Mean 1.904e+04
RMS 10.41
Underflow 5.95e+05
Overflow 0
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10^3
10^2
10
1
18800
18900
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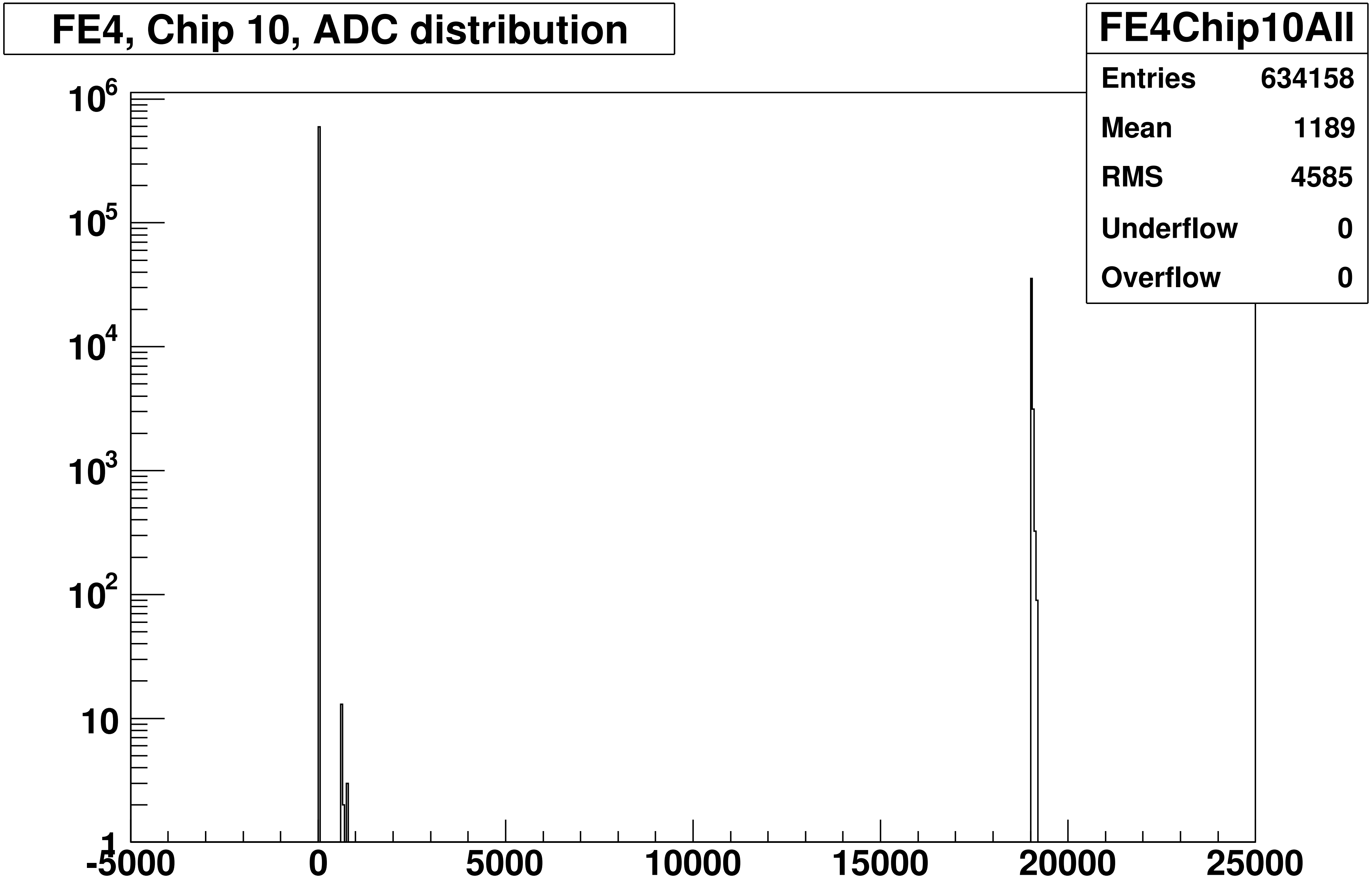
19200
19300
19400


FE4, Chip 10, ADC distribution
FE4Chip10All
Entries 634158
Mean 1189
RMS 4585
Underflow 0
Overflow 0
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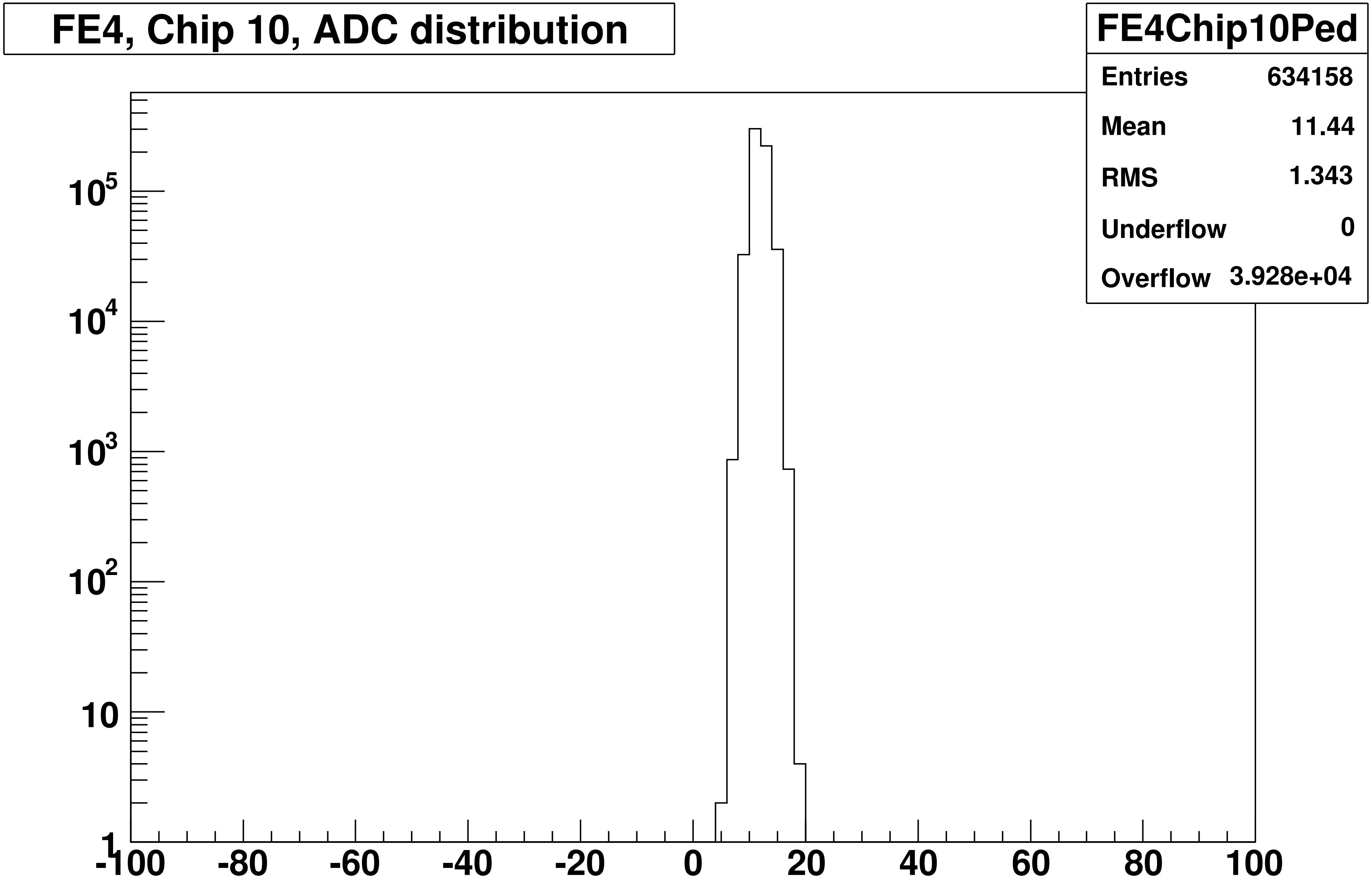
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE4, Chip 10, ADC distribution
FE4Chip10Ped
Entries 634158
Mean 11.44
RMS 1.343
Underflow 0
Overflow 3.928e+04
10^5
10^4
10^3
10^2
10
1
-100
-80
-60
-40
-20
0
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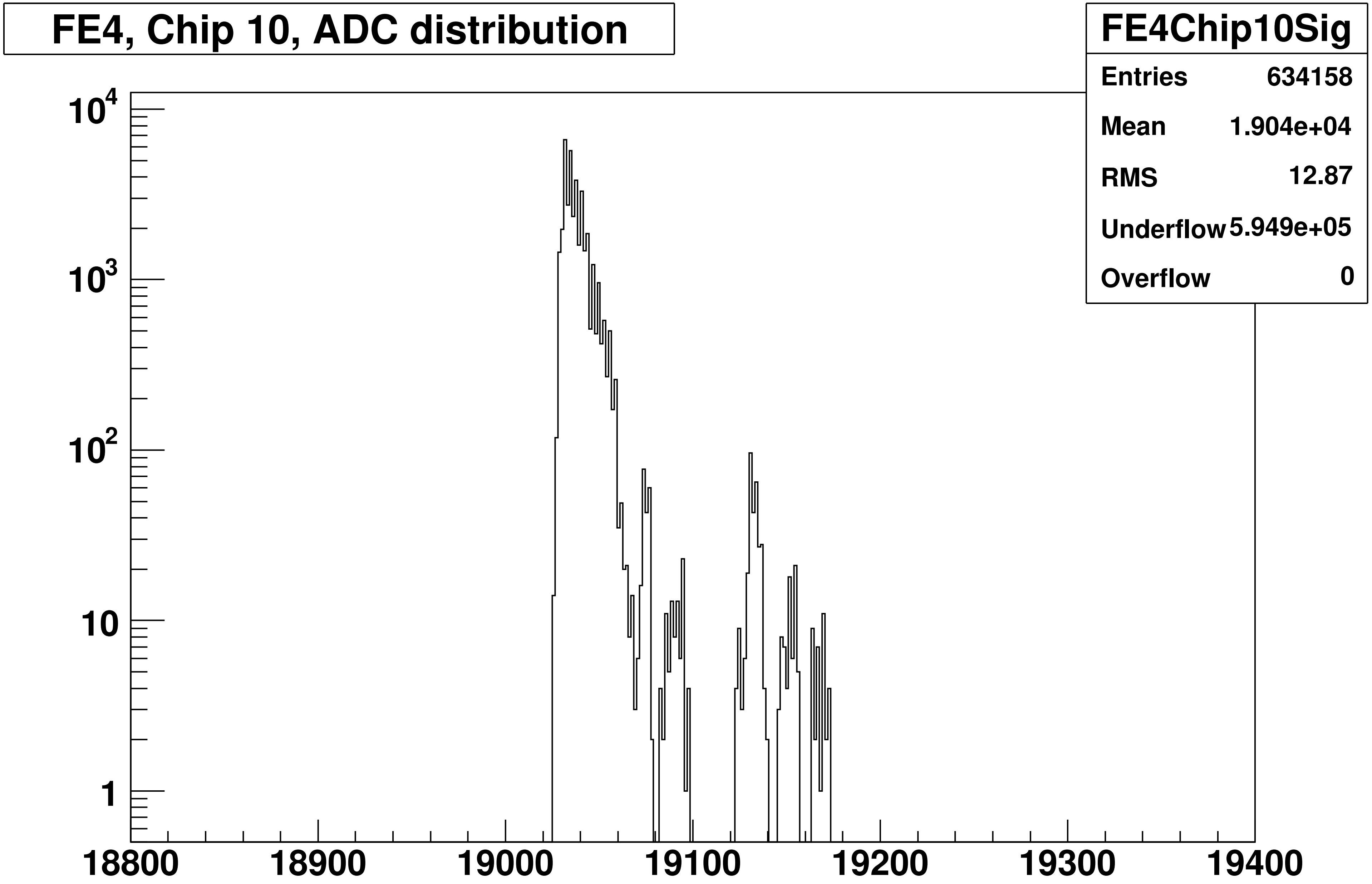
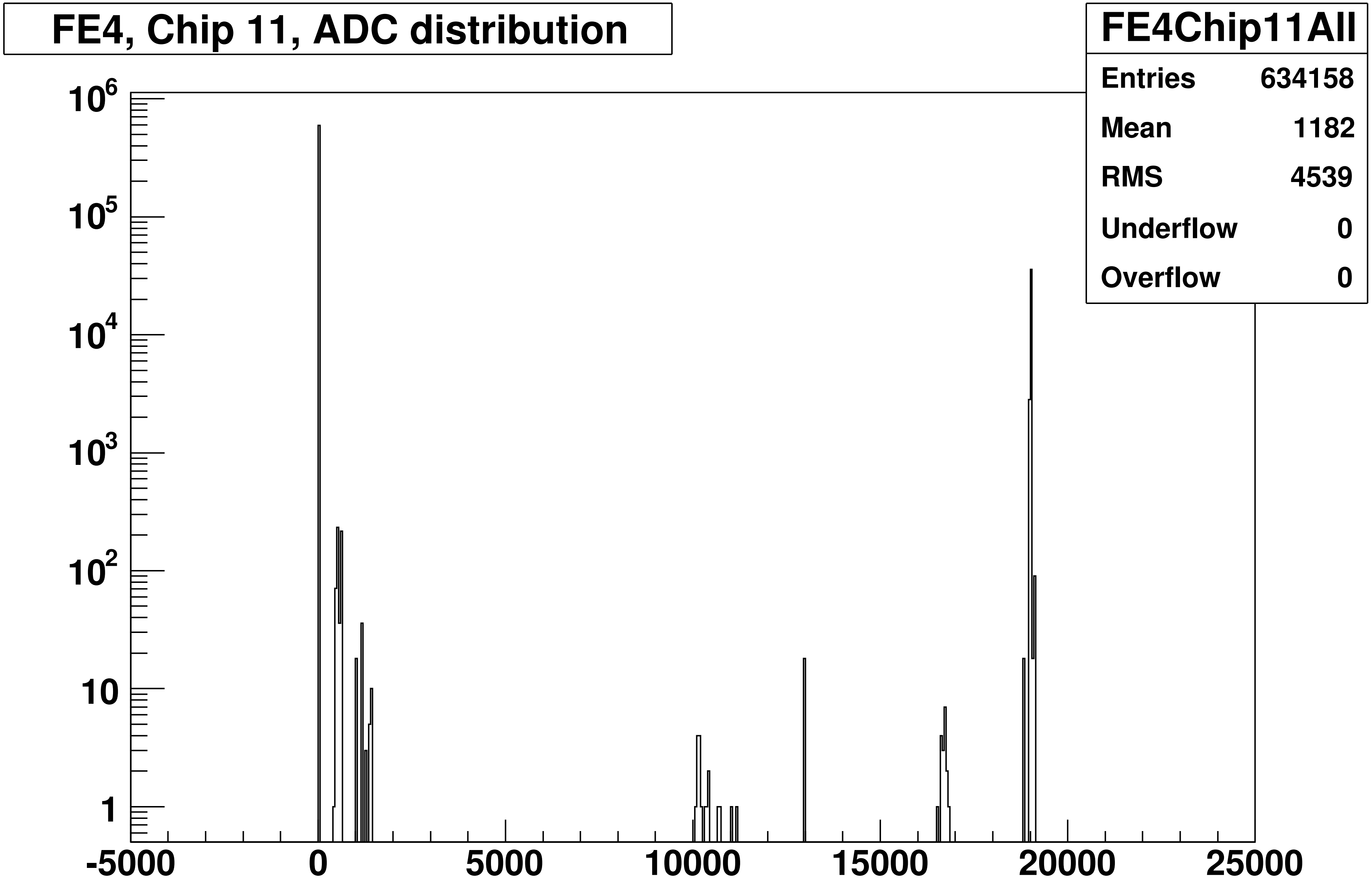
40
60
80
100


FE4, Chip 10, ADC distribution
FE4Chip10Sig
Entries 634158
Mean 1.904e+04
RMS 12.87
Underflow 5.949e+05
Overflow 0
10^4
10^3
10^2
10
1
18800
18900
19000
19100
19200
19300
19400


FE4, Chip 11, ADC distribution
FE4Chip11All
Entries 634158
Mean 1182
RMS 4539
Underflow 0
Overflow 0
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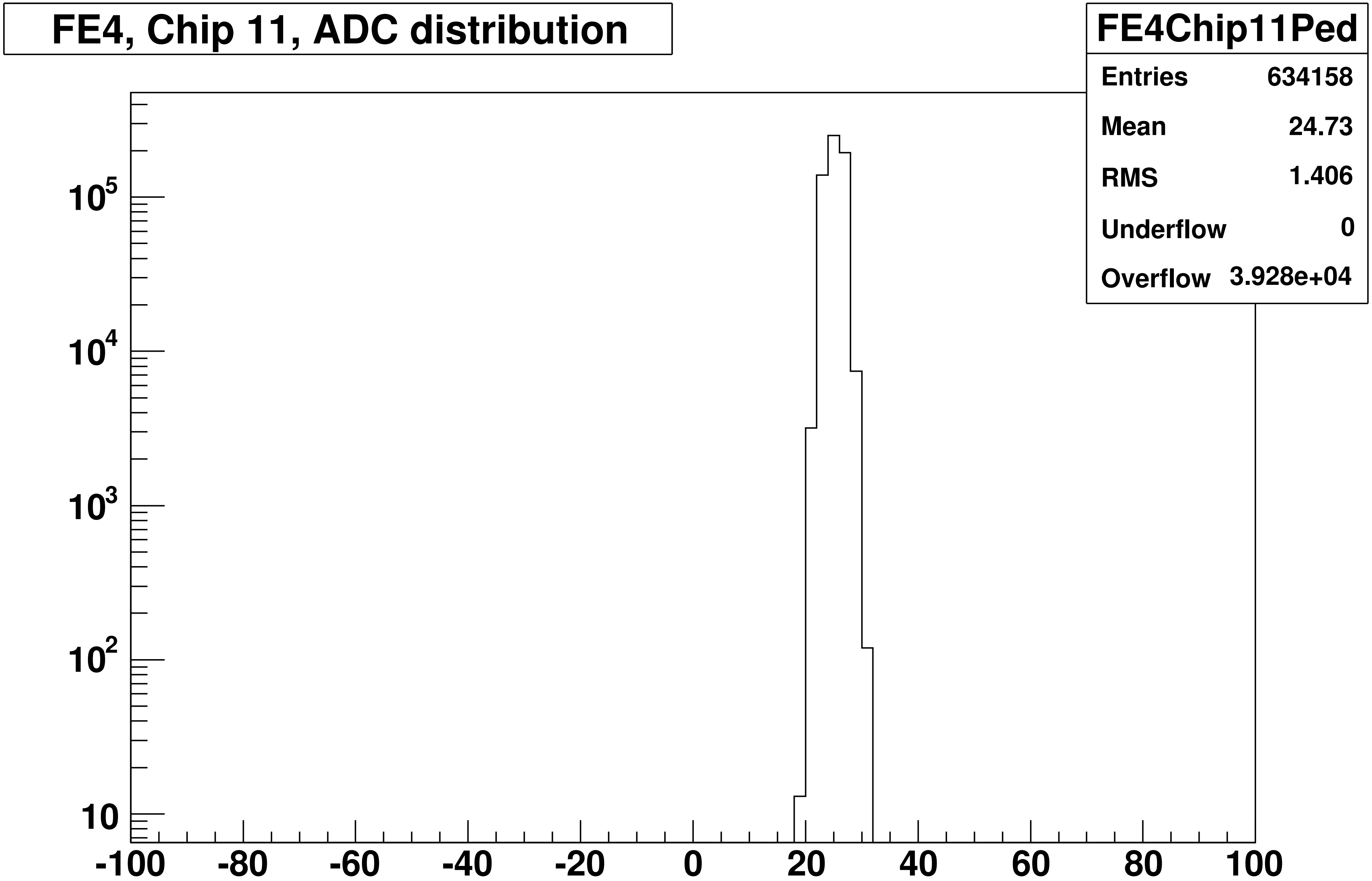
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE4, Chip 11, ADC distribution
FE4Chip11Ped
Entries 634158
Mean 24.73
RMS 1.406
Underflow 0
Overflow 3.928e+04
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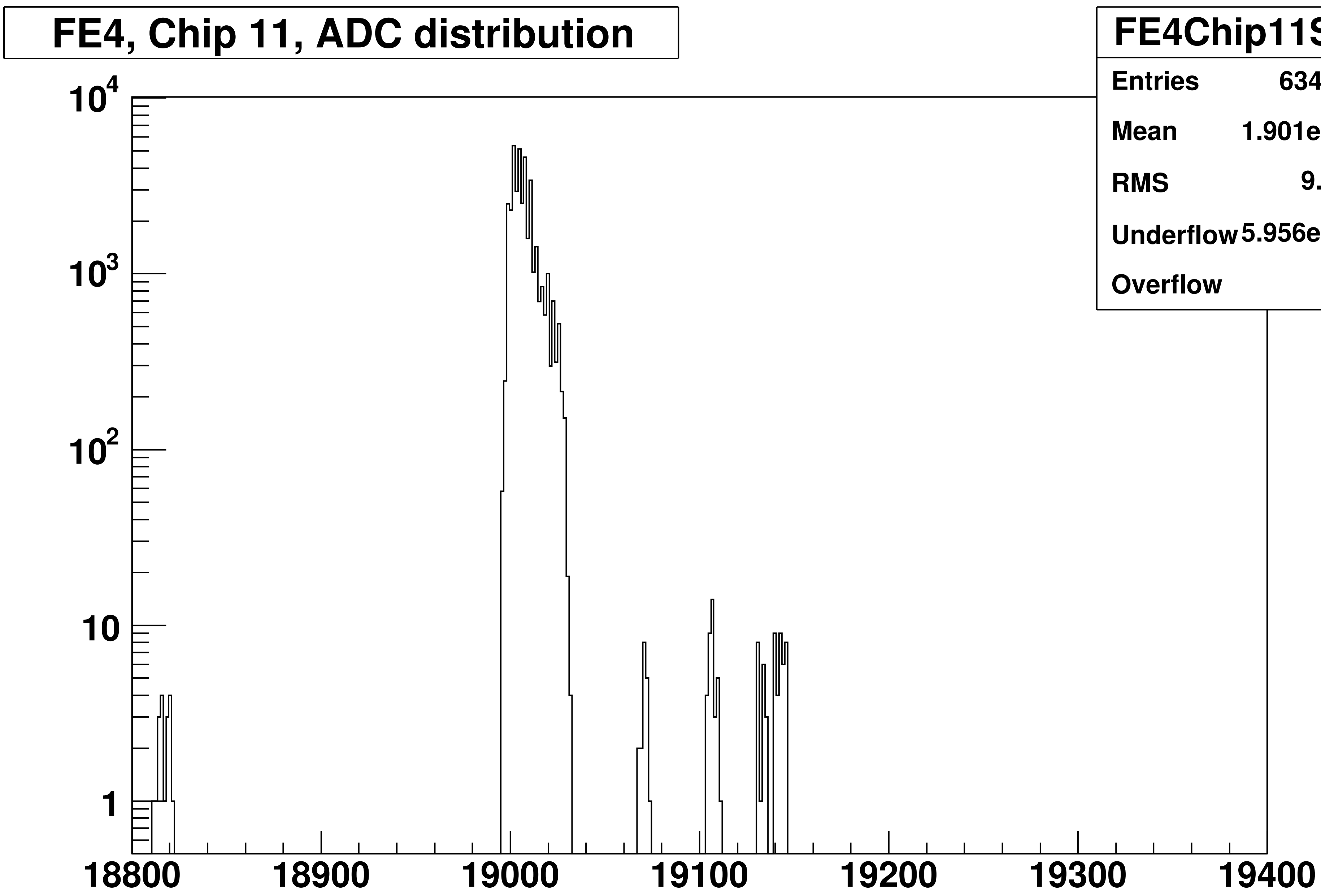
10^2
10^3
10^4
10^5
-100
-80
-60
-40
-20
0
20
40
60
80
100


FE4, Chip 11, ADC distribution
FE4Chip11Sig
Entries 634158
Mean 1.901e+04
RMS 9.822
Underflow 5.956e+05
Overflow 0
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10^3
10^2
10
1
18800
18900
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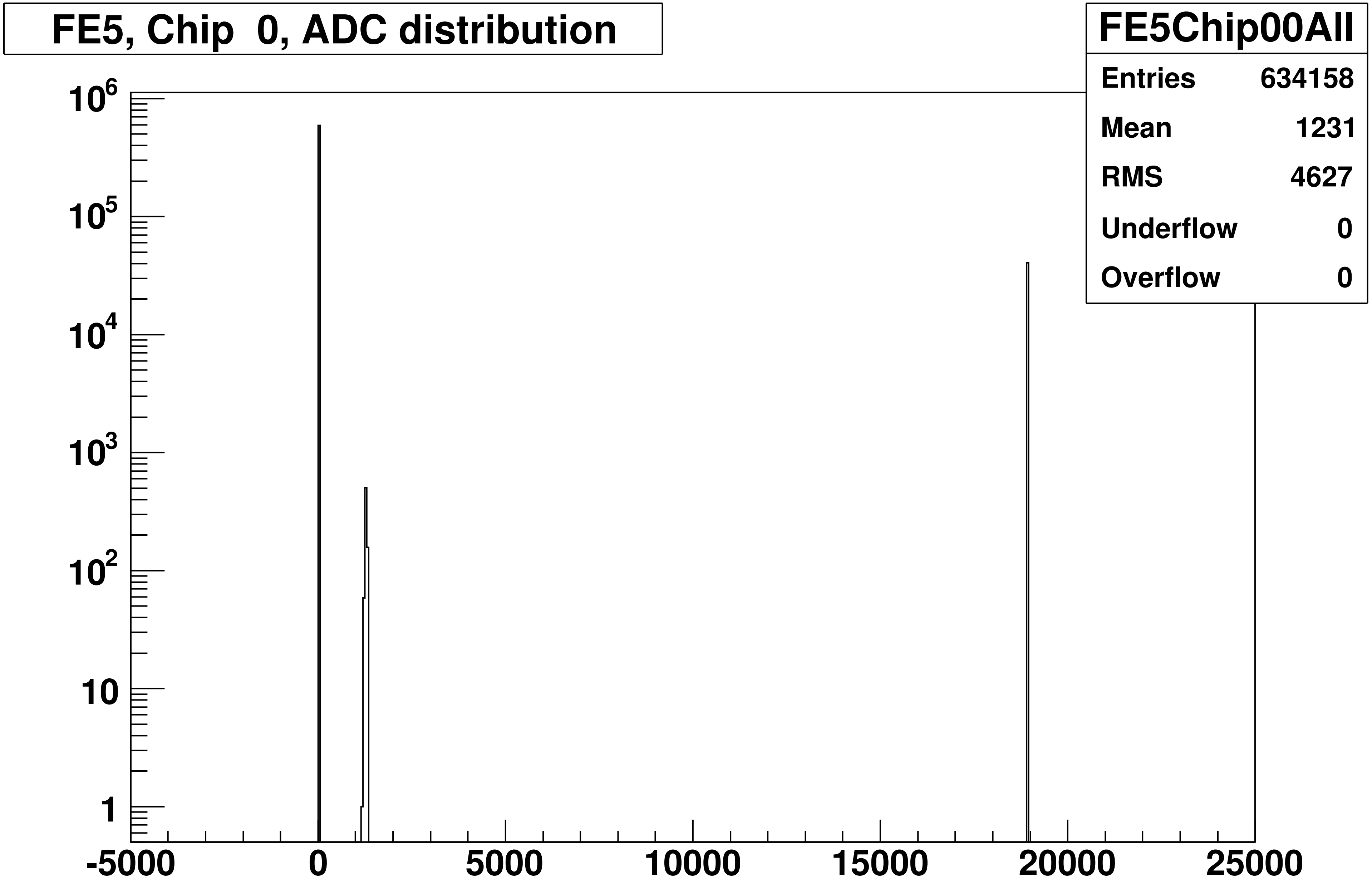
19400



FE5, Chip 0, ADC distribution
FE5Chip00All
Entries 634158
Mean 1231
RMS 4627
Underflow 0
Overflow 0
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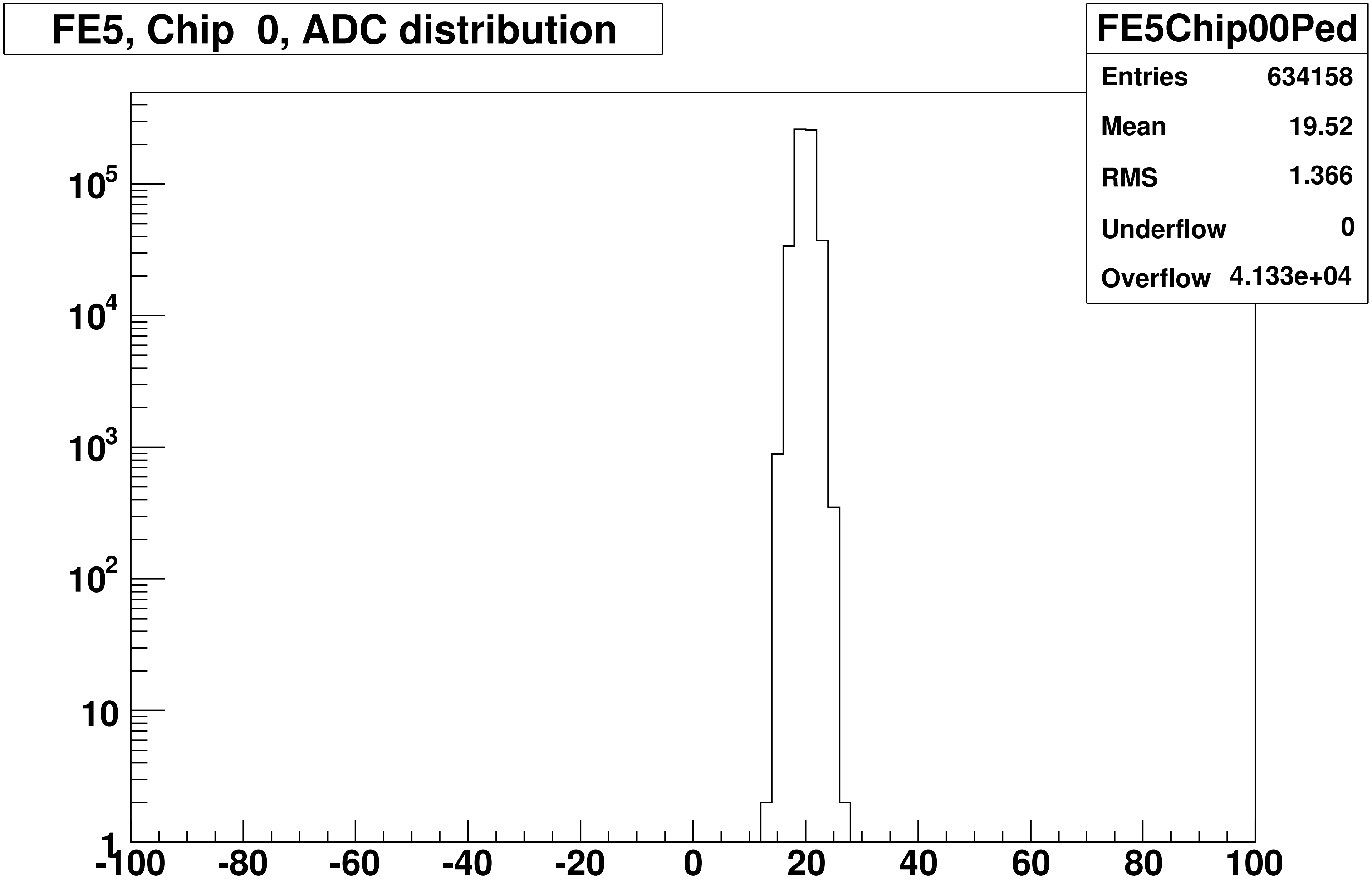
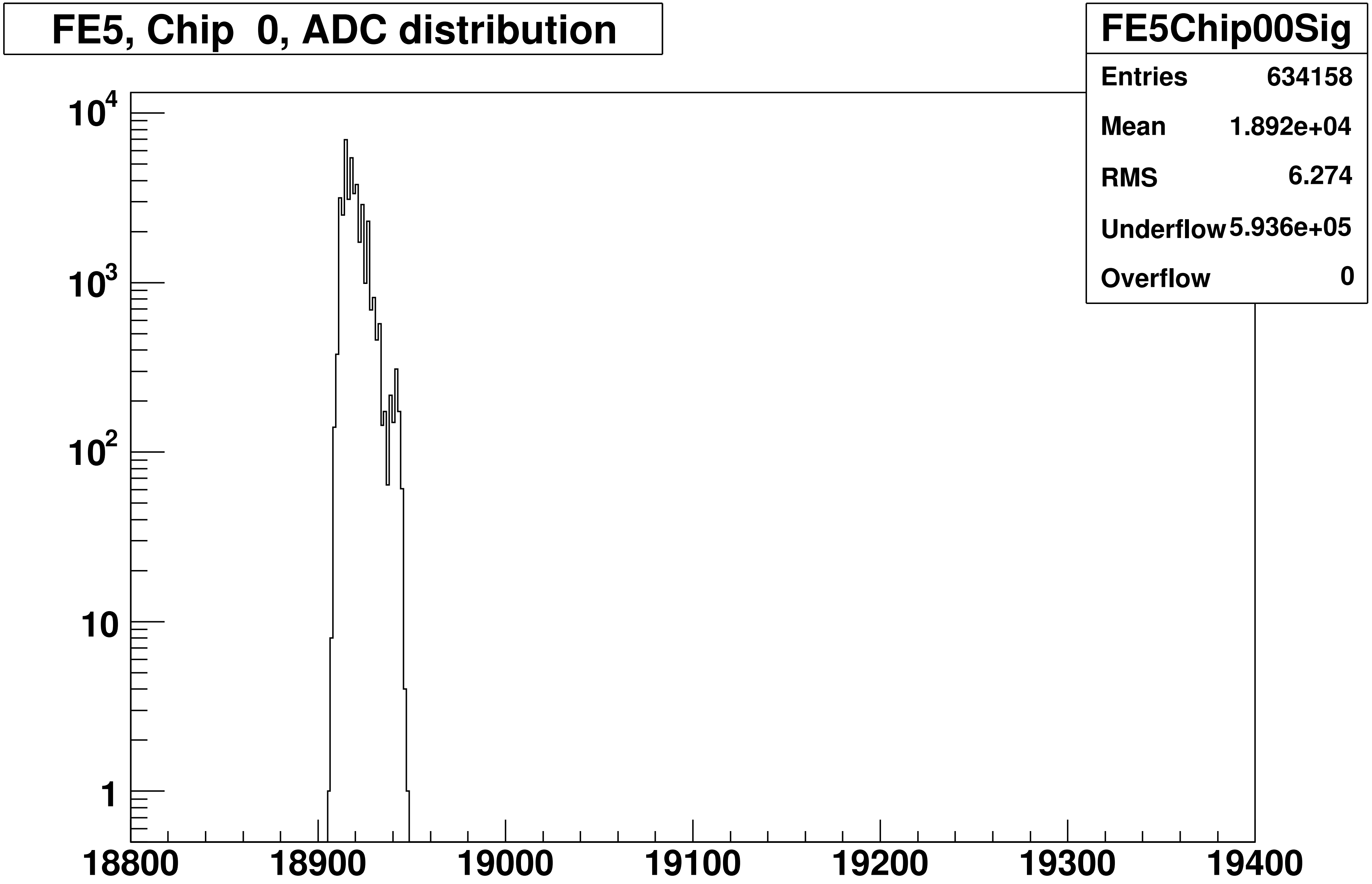
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE5, Chip 0, ADC distribution
FE5Chip00Ped
Entries 634158
Mean 19.52
RMS 1.366
Underflow 0
Overflow 4.133e+04
1
10
10^2
10^3
10^4
10^5
-100
-80
-60
-40
-20
0
20
40
60
80
100


FE5, Chip 0, ADC distribution
FE5Chip00Sig
Entries 634158
Mean 1.892e+04
RMS 6.274
Underflow 5.936e+05
Overflow 0
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10^3
10^2
10
1
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18900
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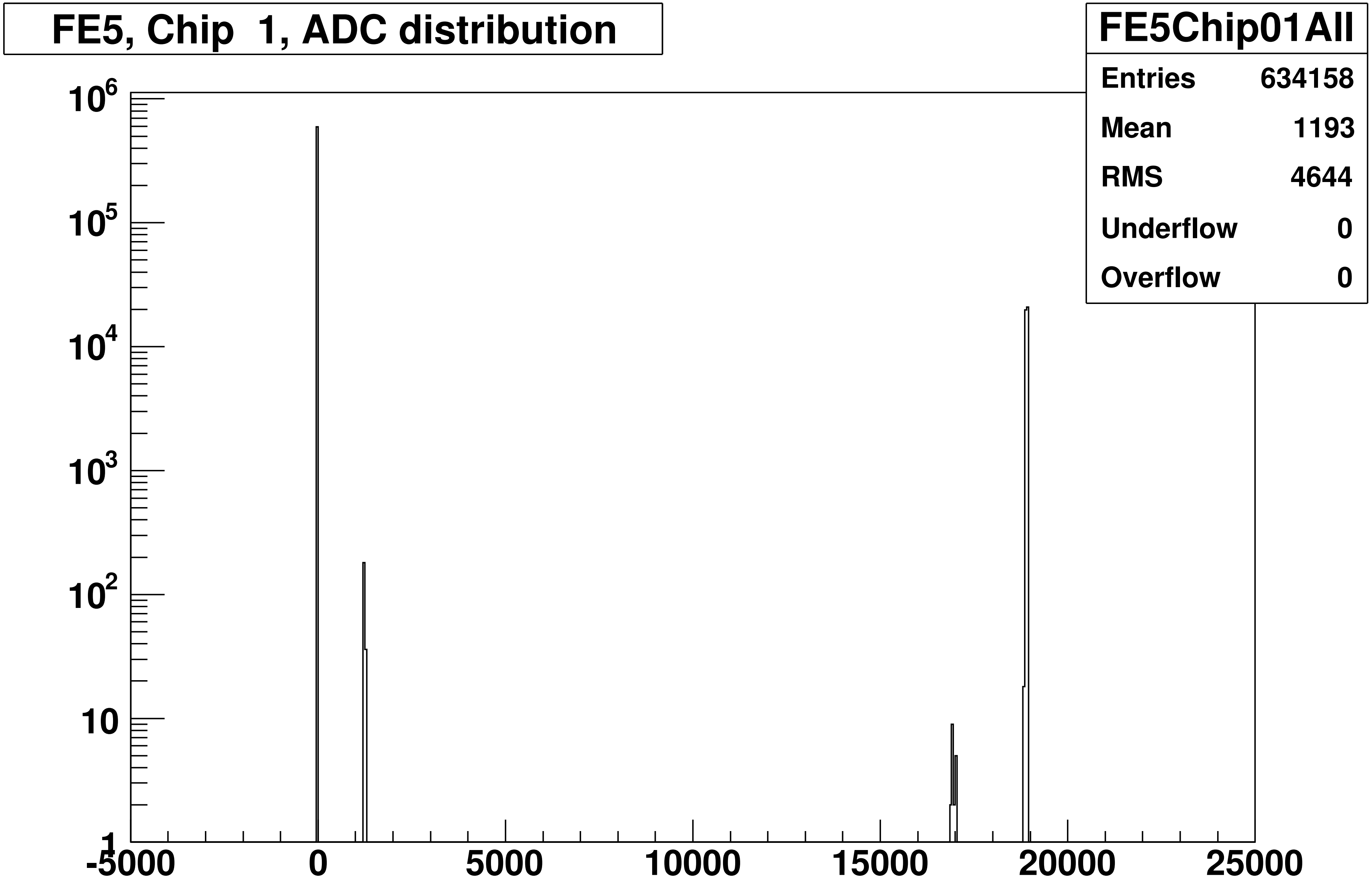
FE5, Chip 1, ADC distribution
FE5Chip01All
Entries 634158
Mean 1193
RMS 4644
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
1
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0
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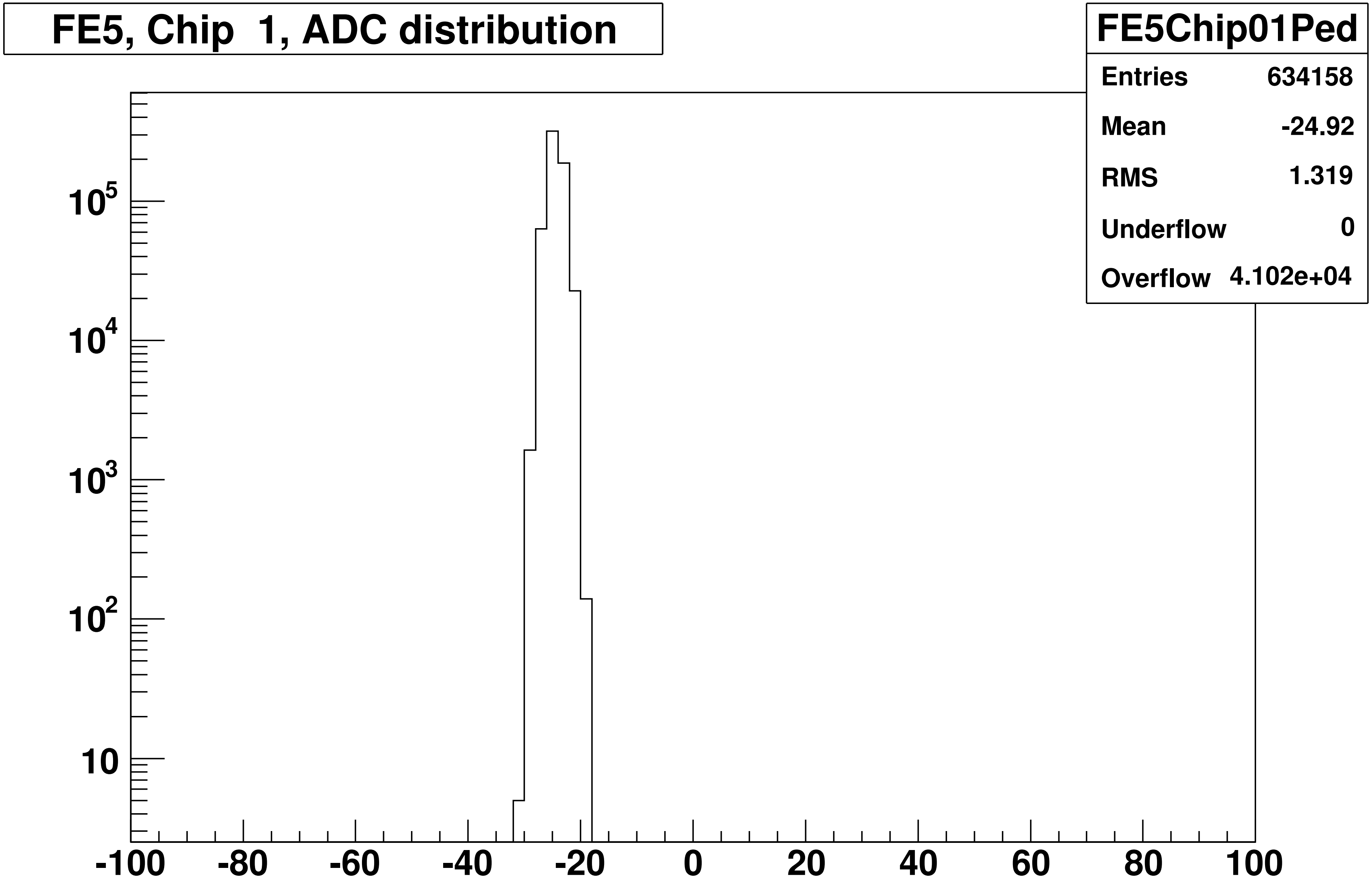
FE5, Chip 1, ADC distribution
FE5Chip01Ped
Entries 634158
Mean -24.92
RMS 1.319
Underflow 0
Overflow 4.102e+04
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10^3
10^4
10^5
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-80
-60
-40
-20
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80
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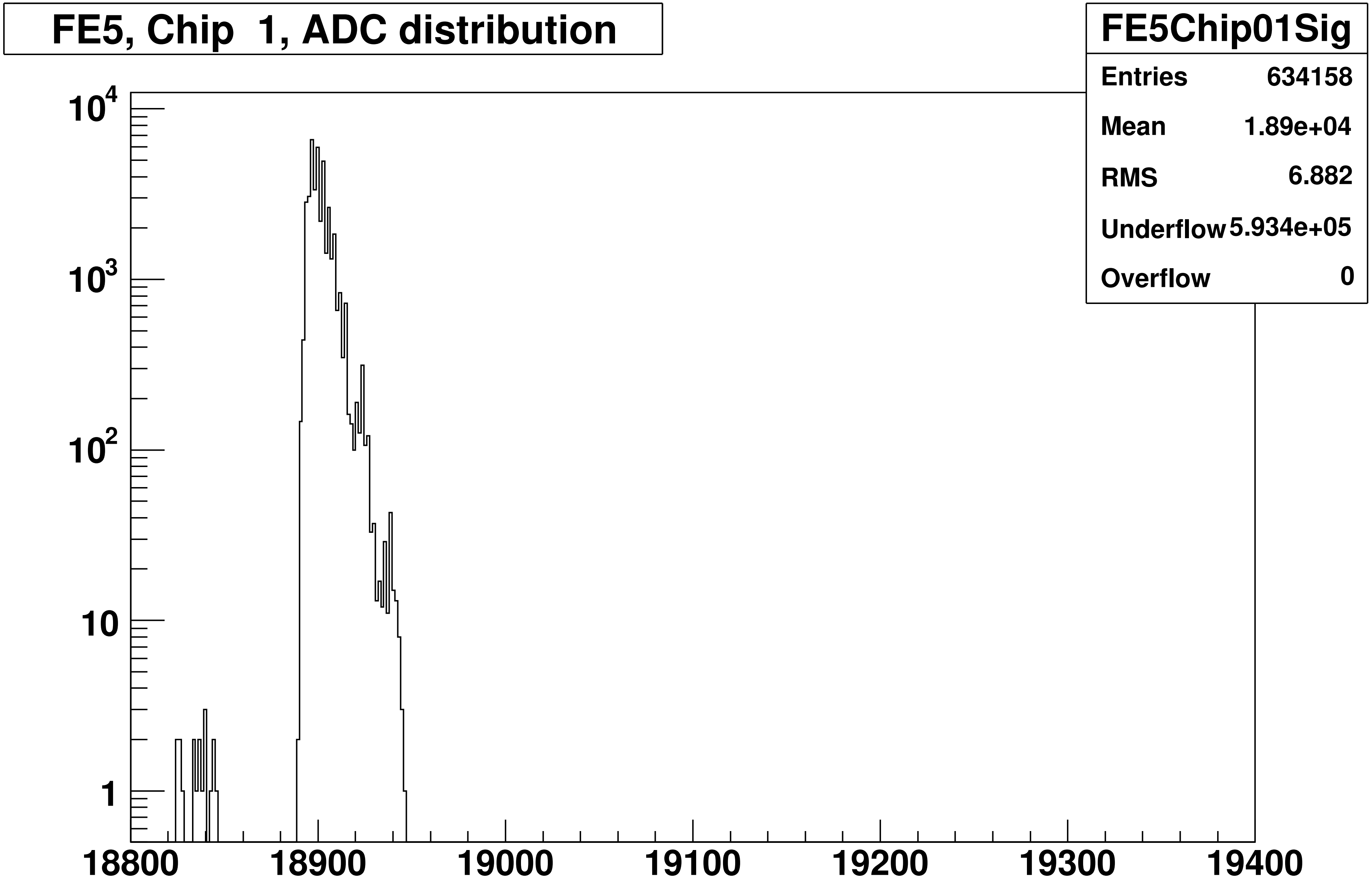
FE5, Chip 1, ADC distribution
FE5Chip01Sig
Entries 634158
Mean 1.89e+04
RMS 6.882
Underflow 5.934e+05
Overflow 0
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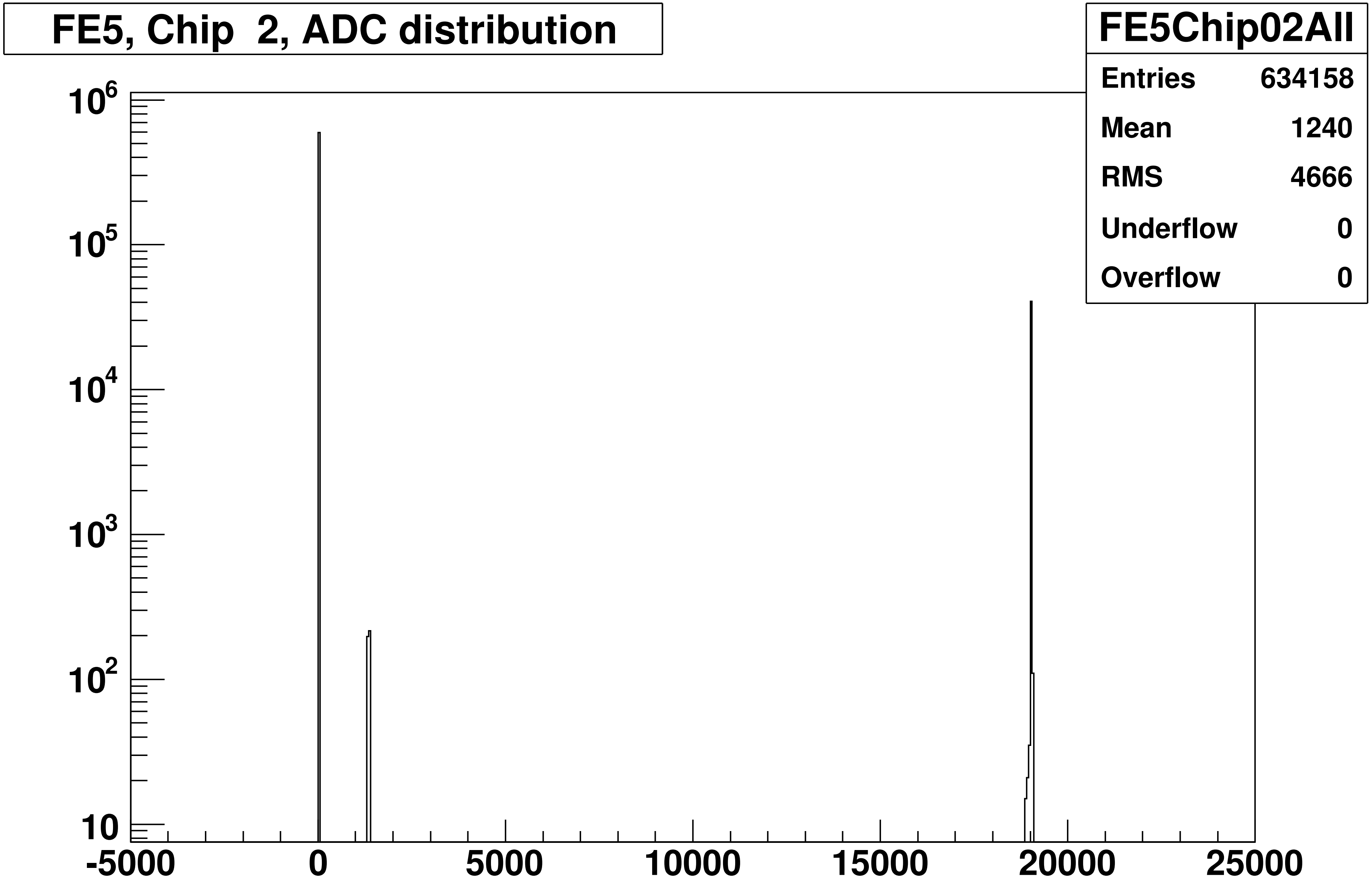
10^3
10^2
10
1
18800
18900
19000
19100
19200
19300
19400



FE5, Chip 2, ADC distribution
FE5Chip02All
Entries 634158
Mean 1240
RMS 4666
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
-5000
0
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10000
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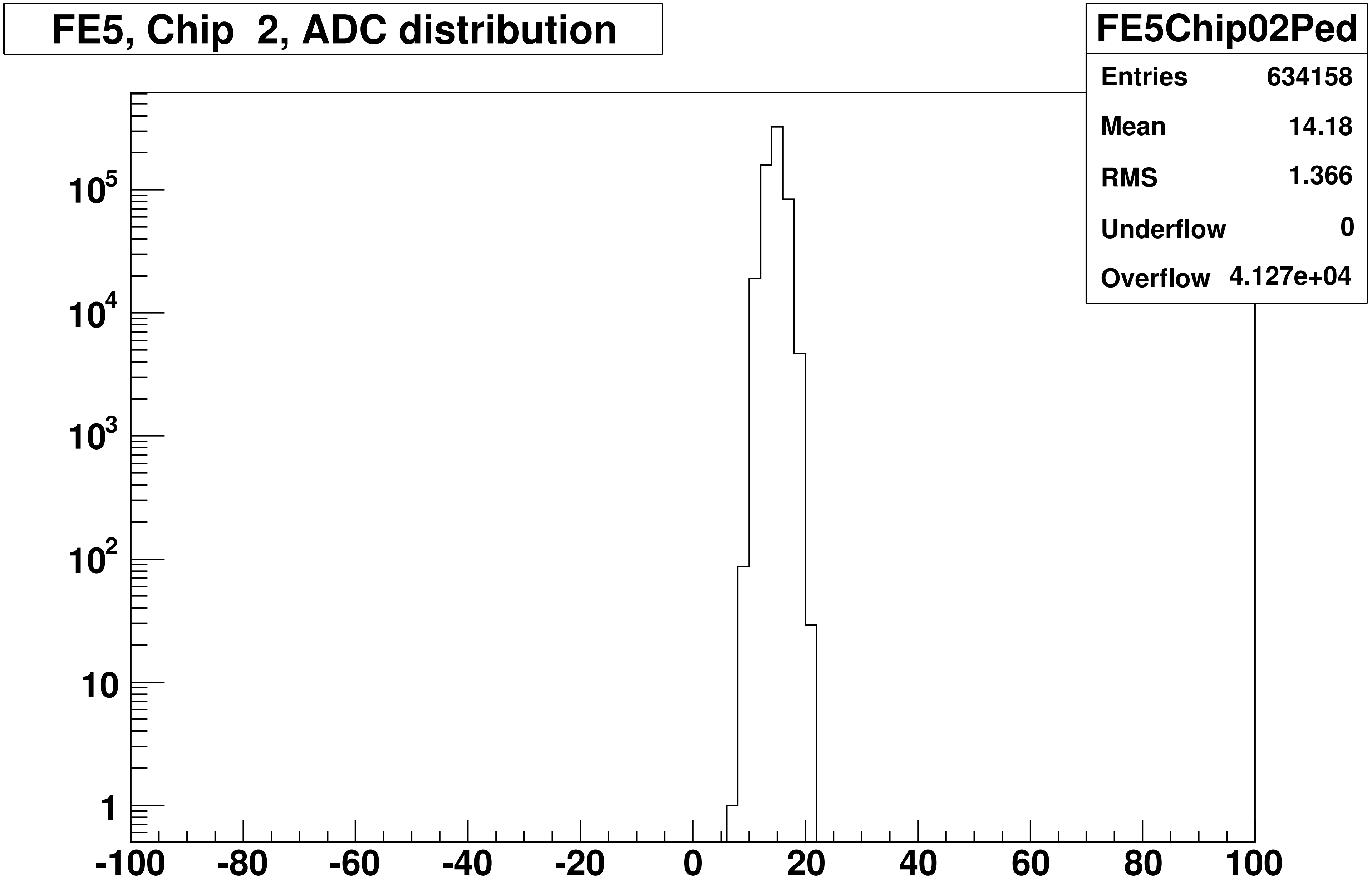
20000
25000


FE5, Chip 2, ADC distribution
FE5Chip02Ped
Entries 634158
Mean 14.18
RMS 1.366
Underflow 0
Overflow 4.127e+04
10^5
10^4
10^3
10^2
10
1
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-20
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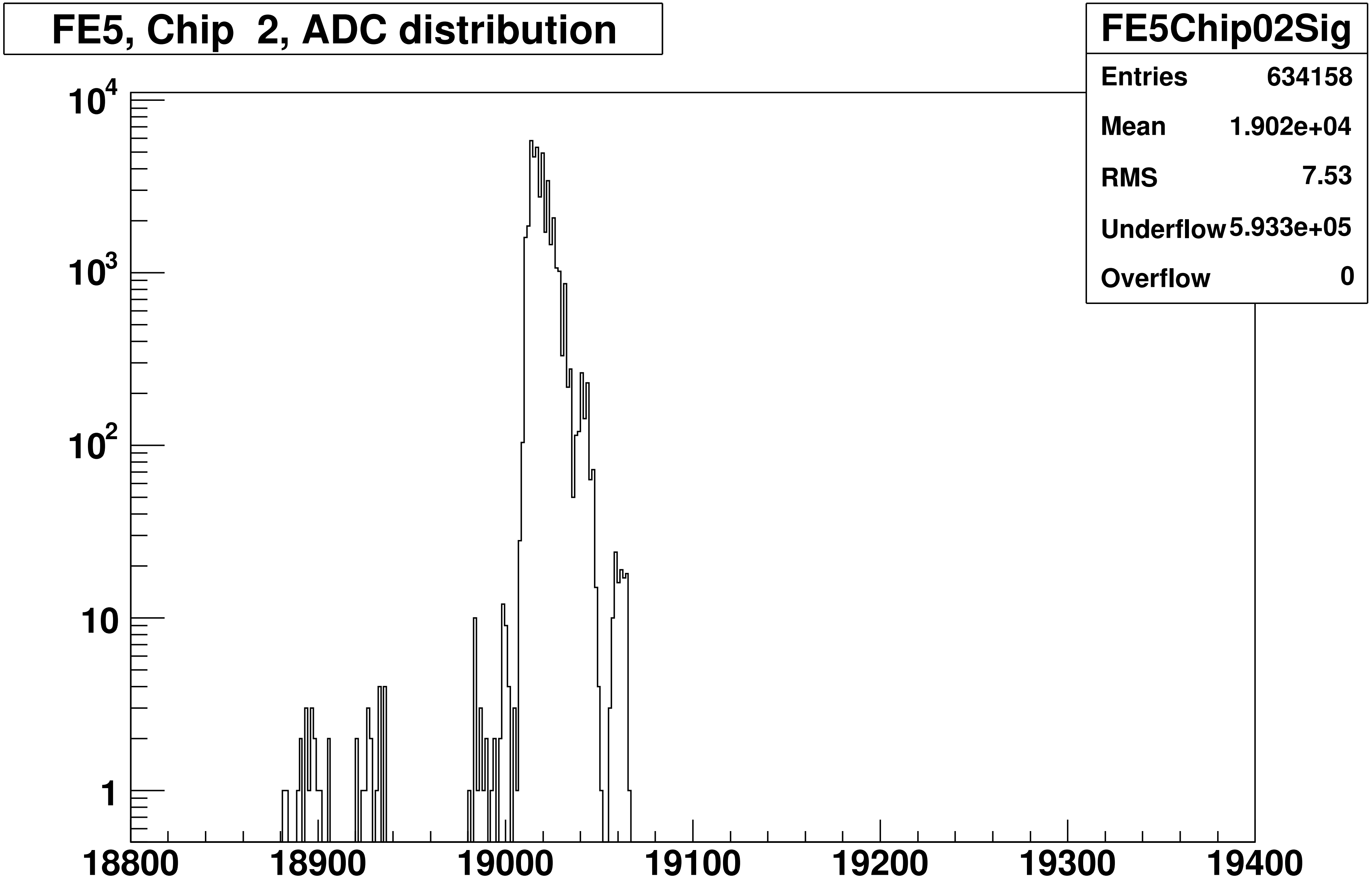

FE5, Chip 2, ADC distribution
FE5Chip02Sig
Entries 634158
Mean 1.902e+04
RMS 7.53
Underflow 5.933e+05
Overflow 0
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10^3
10^2
10
1
18800
18900
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19200
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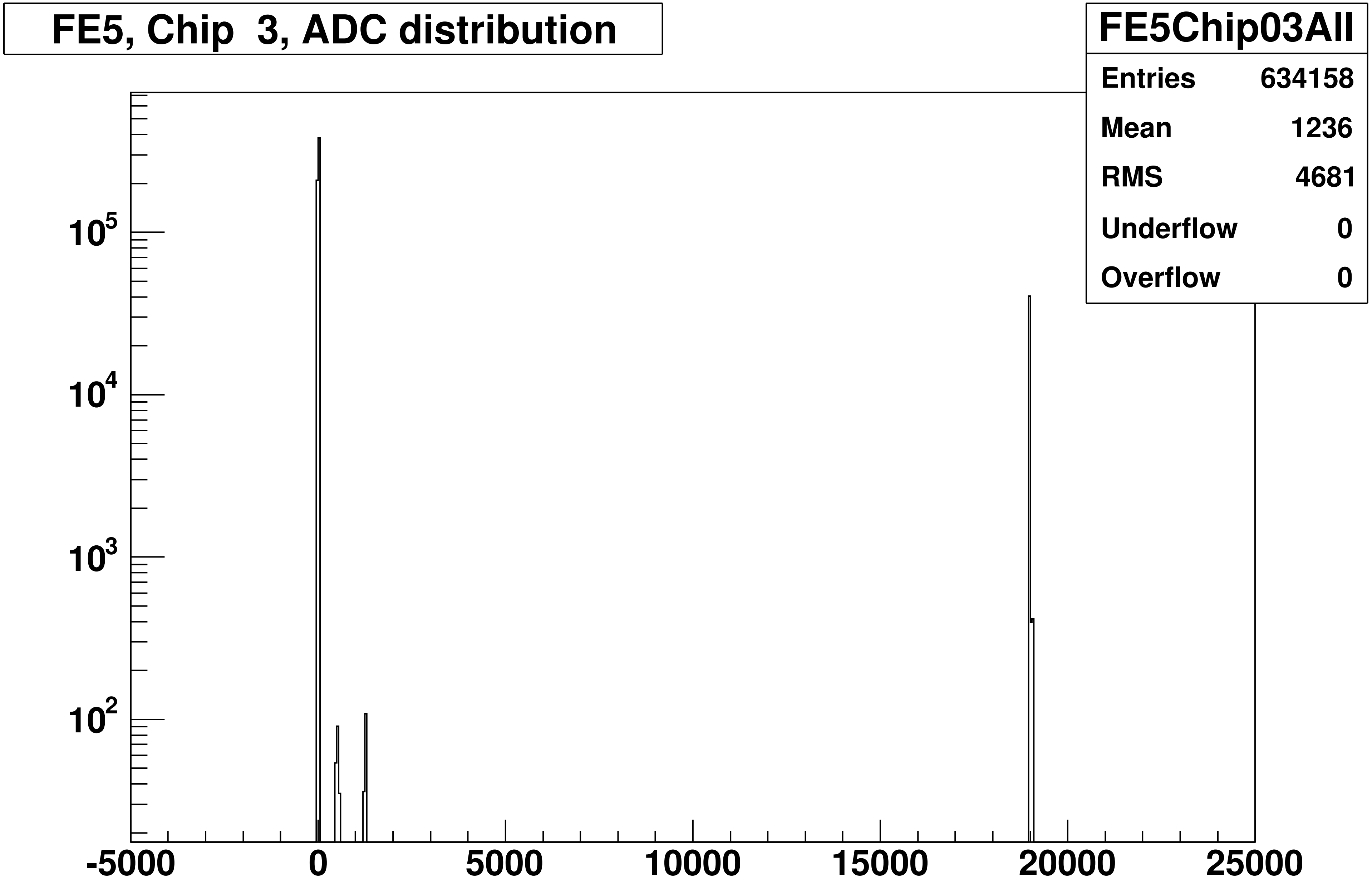
19400


FE5, Chip 3, ADC distribution
FE5Chip03All
Entries 634158
Mean 1236
RMS 4681
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
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0
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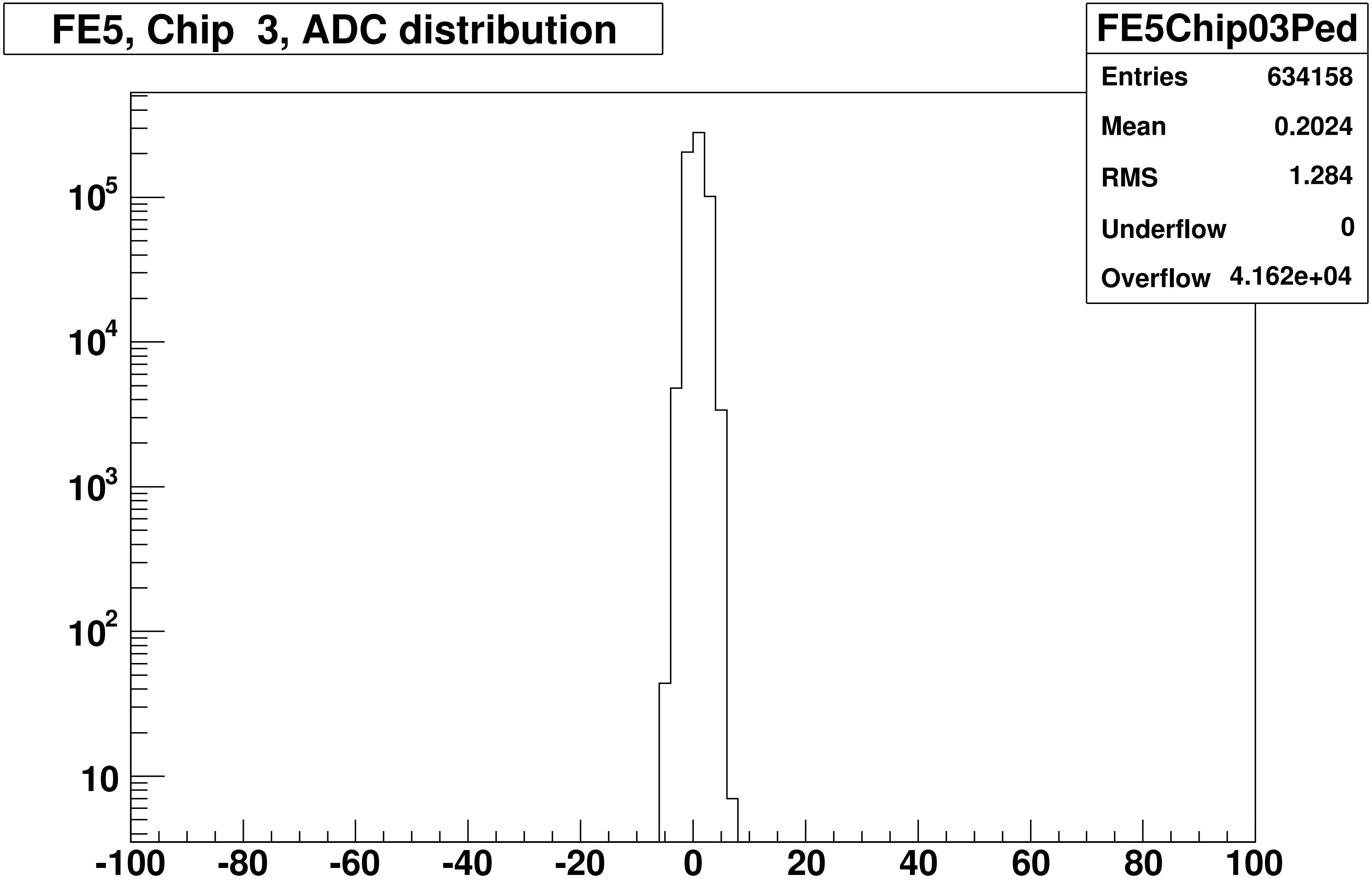
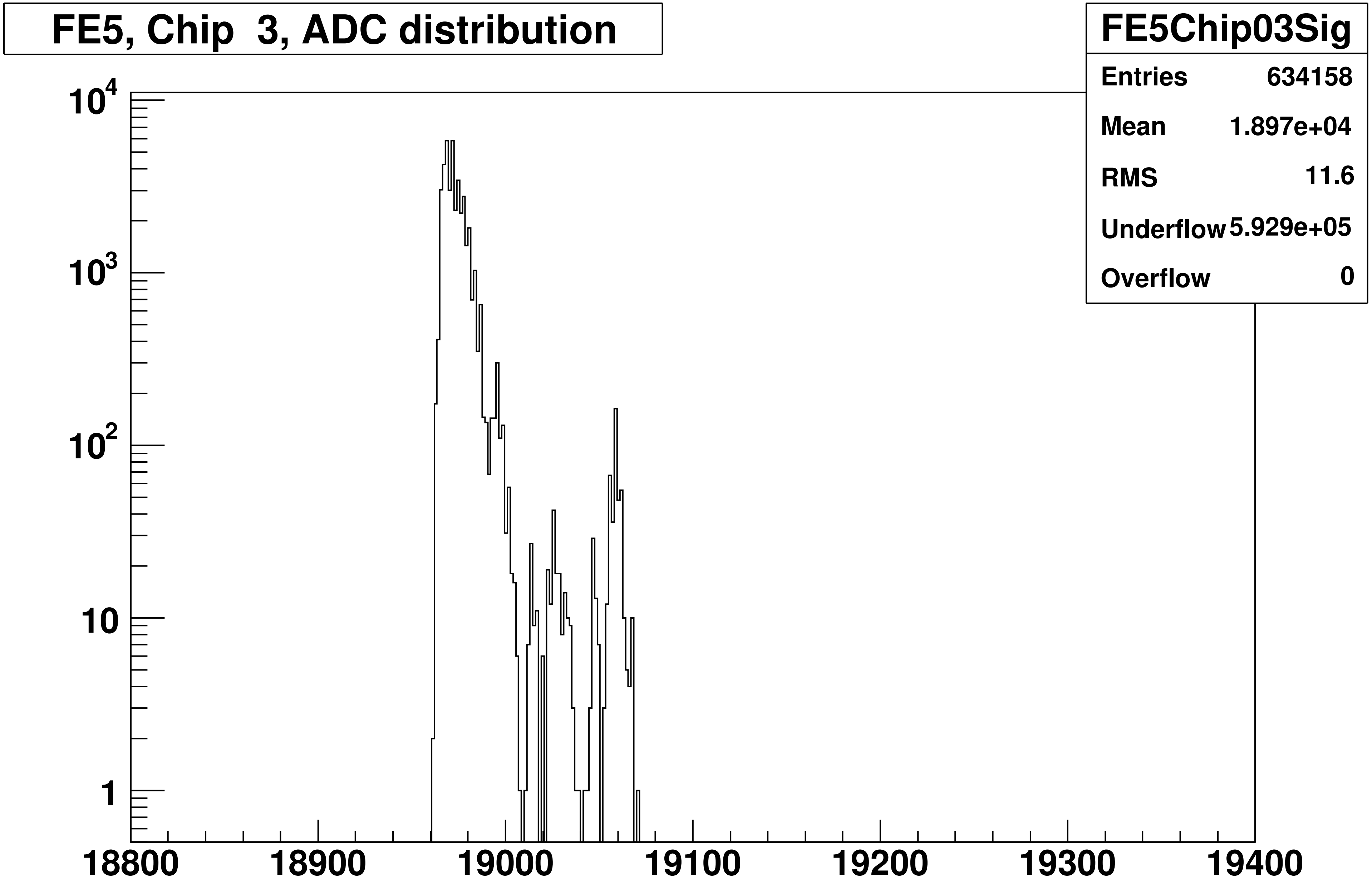
20000
25000



FE5, Chip 3, ADC distribution
FE5Chip03Ped
Entries 634158
Mean 0.2024
RMS 1.284
Underflow 0
Overflow 4.162e+04
10^5
10^4
10^3
10^2
10
-100 -80 -60 -40 -20 0 20 40 60 80 100


FE5, Chip 3, ADC distribution
FE5Chip03Sig
Entries 634158
Mean 1.897e+04
RMS 11.6
Underflow 5.929e+05
Overflow 0
10^4
10^3
10^2
10
1
18800
18900
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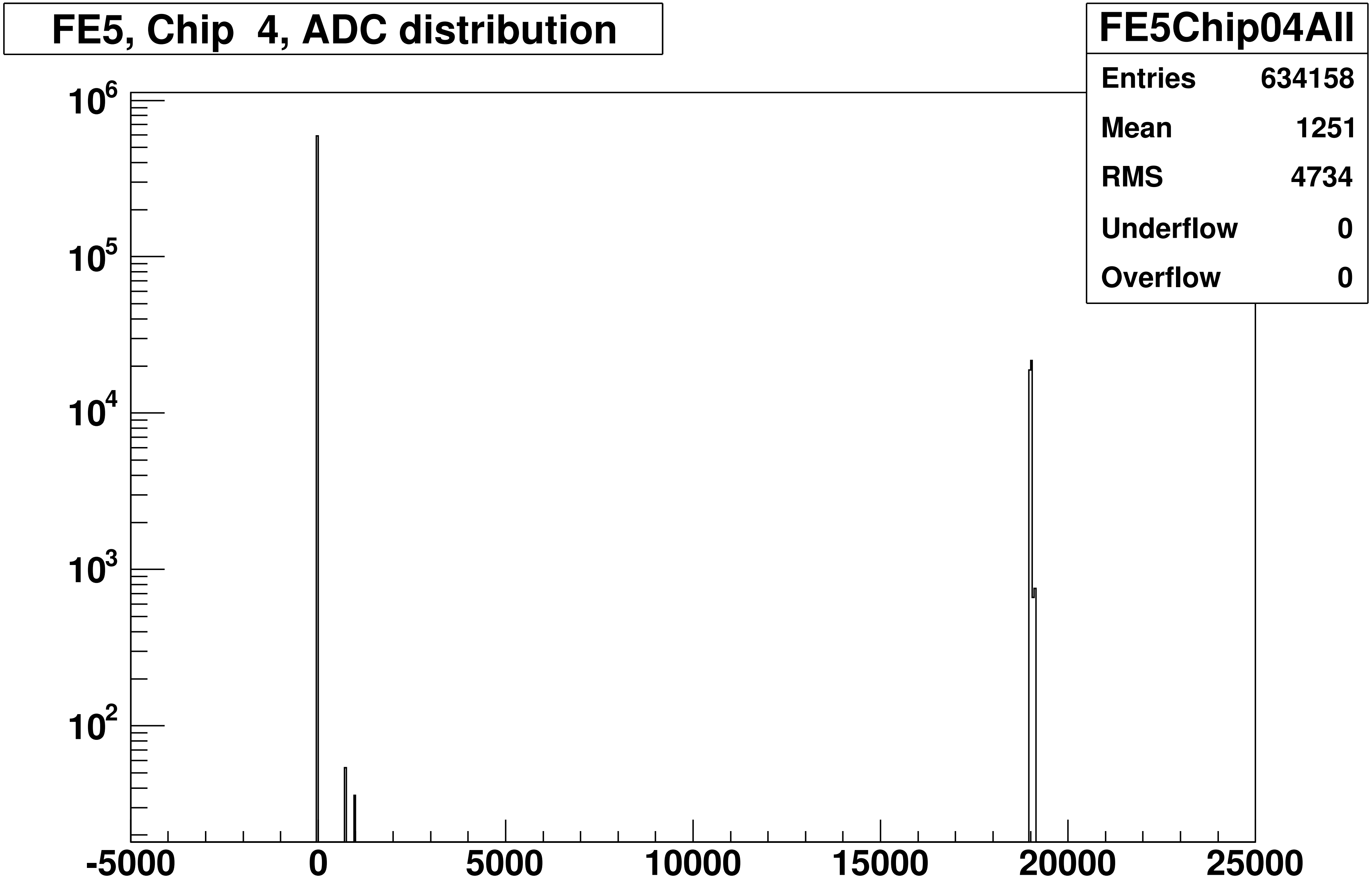
19400


FE5, Chip 4, ADC distribution
FE5Chip04All
Entries 634158
Mean 1251
RMS 4734
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
-5000
0
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10000
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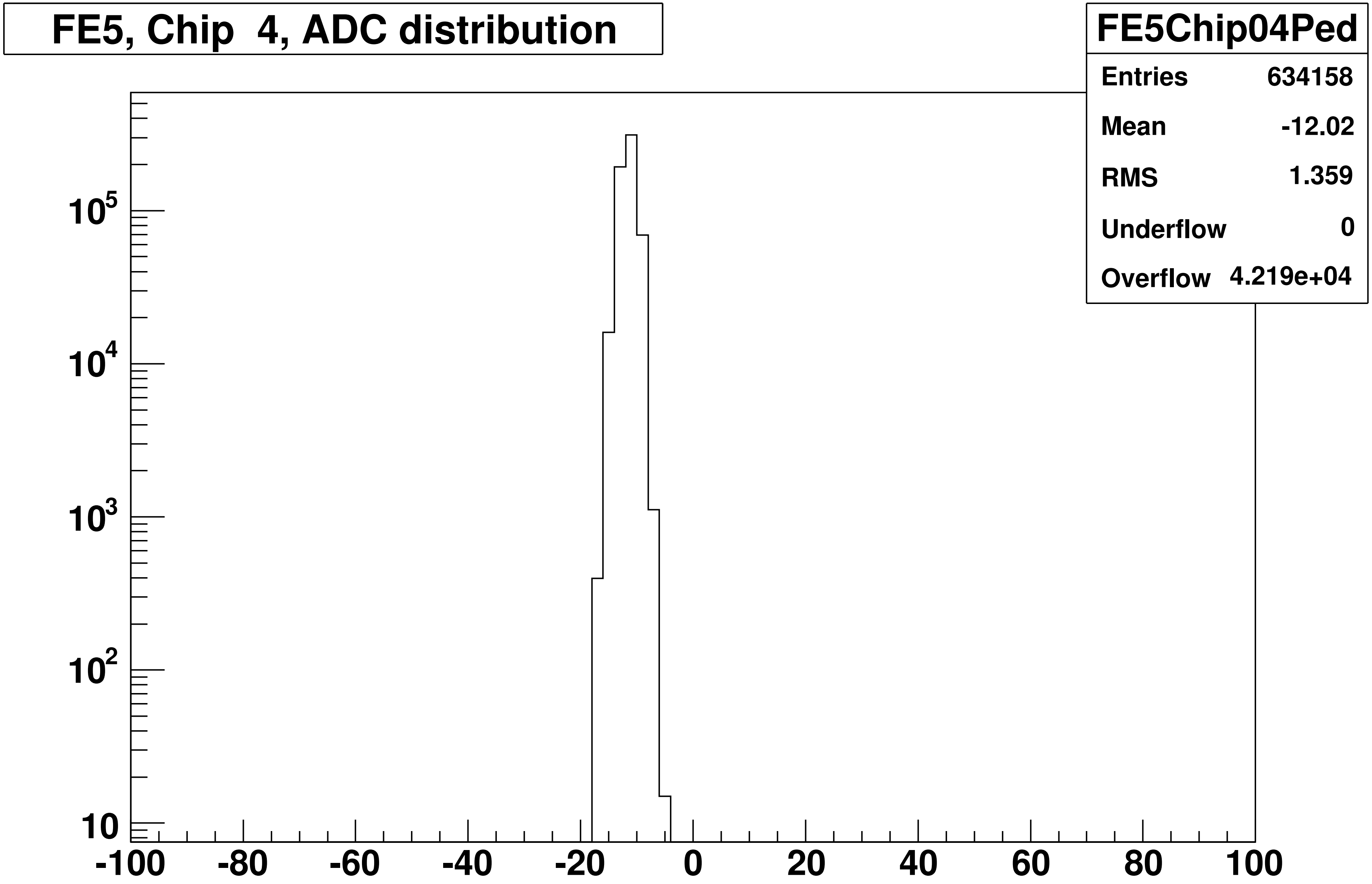
20000
25000


FE5, Chip 4, ADC distribution
FE5Chip04Ped
Entries 634158
Mean -12.02
RMS 1.359
Underflow 0
Overflow 4.219e+04
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10^4
10^3
10^2
10
-100
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-20
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40
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80
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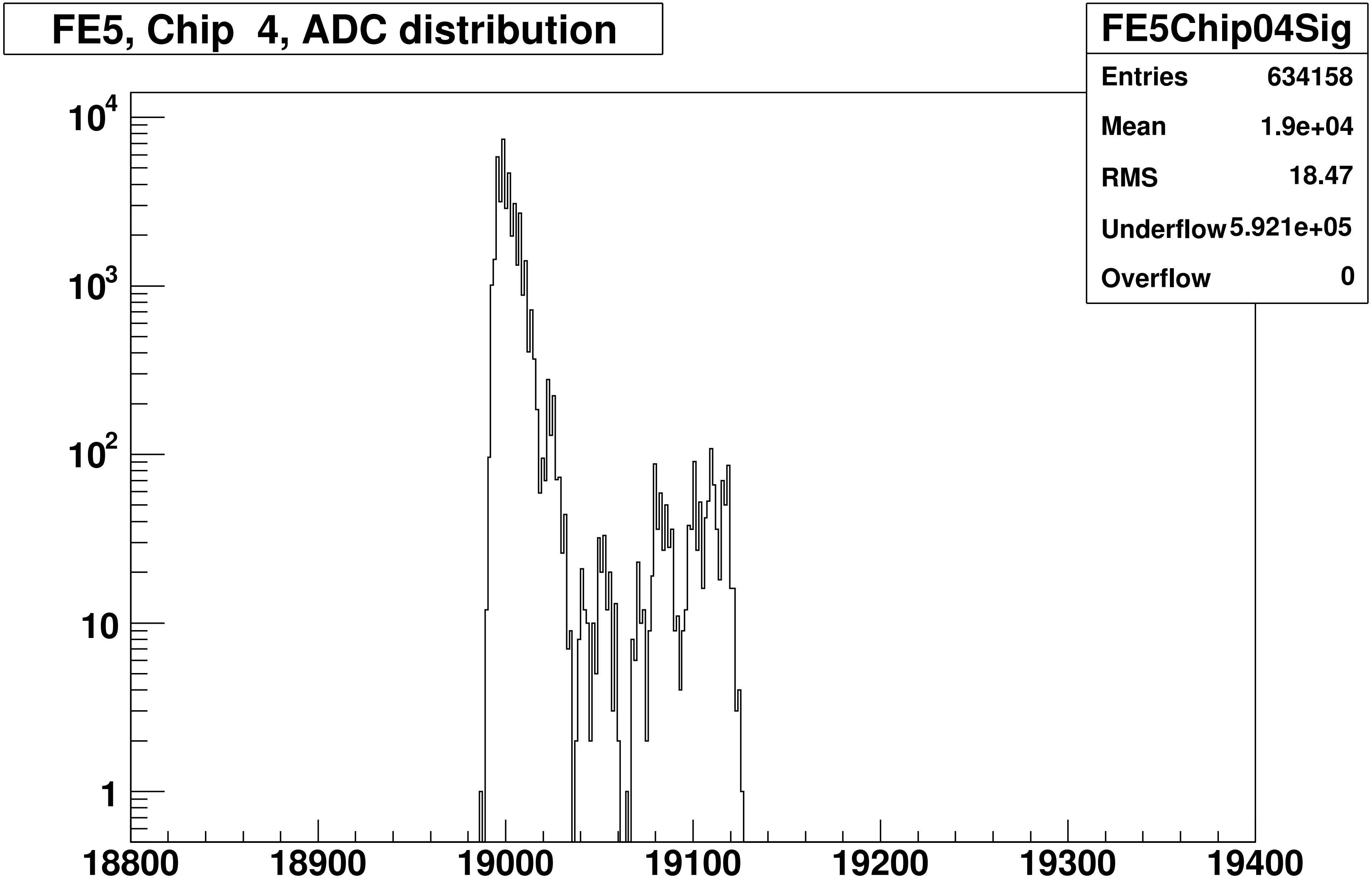
FE5, Chip 4, ADC distribution
FE5Chip04Sig
Entries 634158
Mean 1.9e+04
RMS 18.47
Underflow 5.921e+05
Overflow 0
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10^3
10^2
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18800
18900
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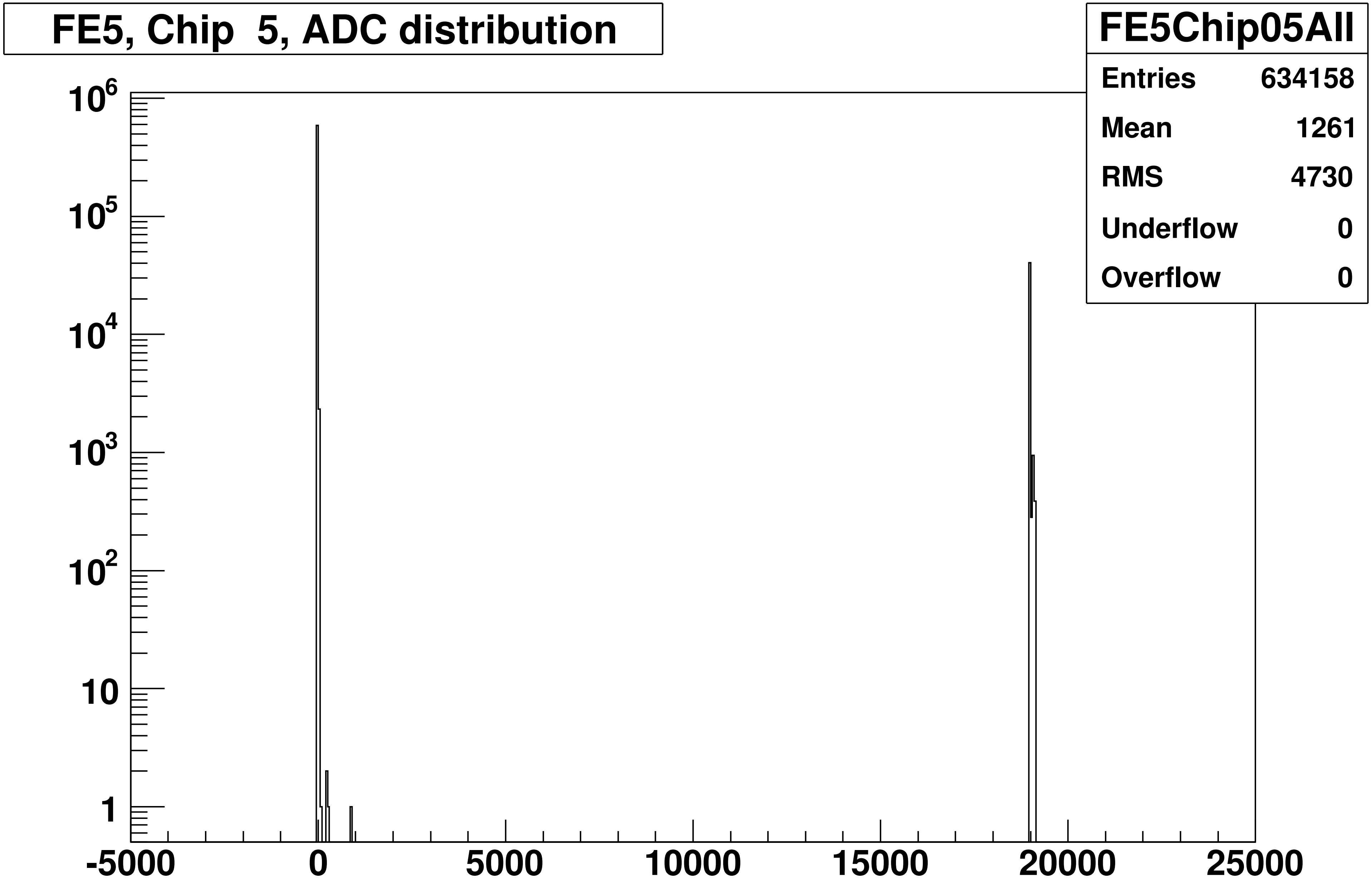
FE5, Chip 5, ADC distribution
FE5Chip05All
Entries 634158
Mean 1261
RMS 4730
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
1
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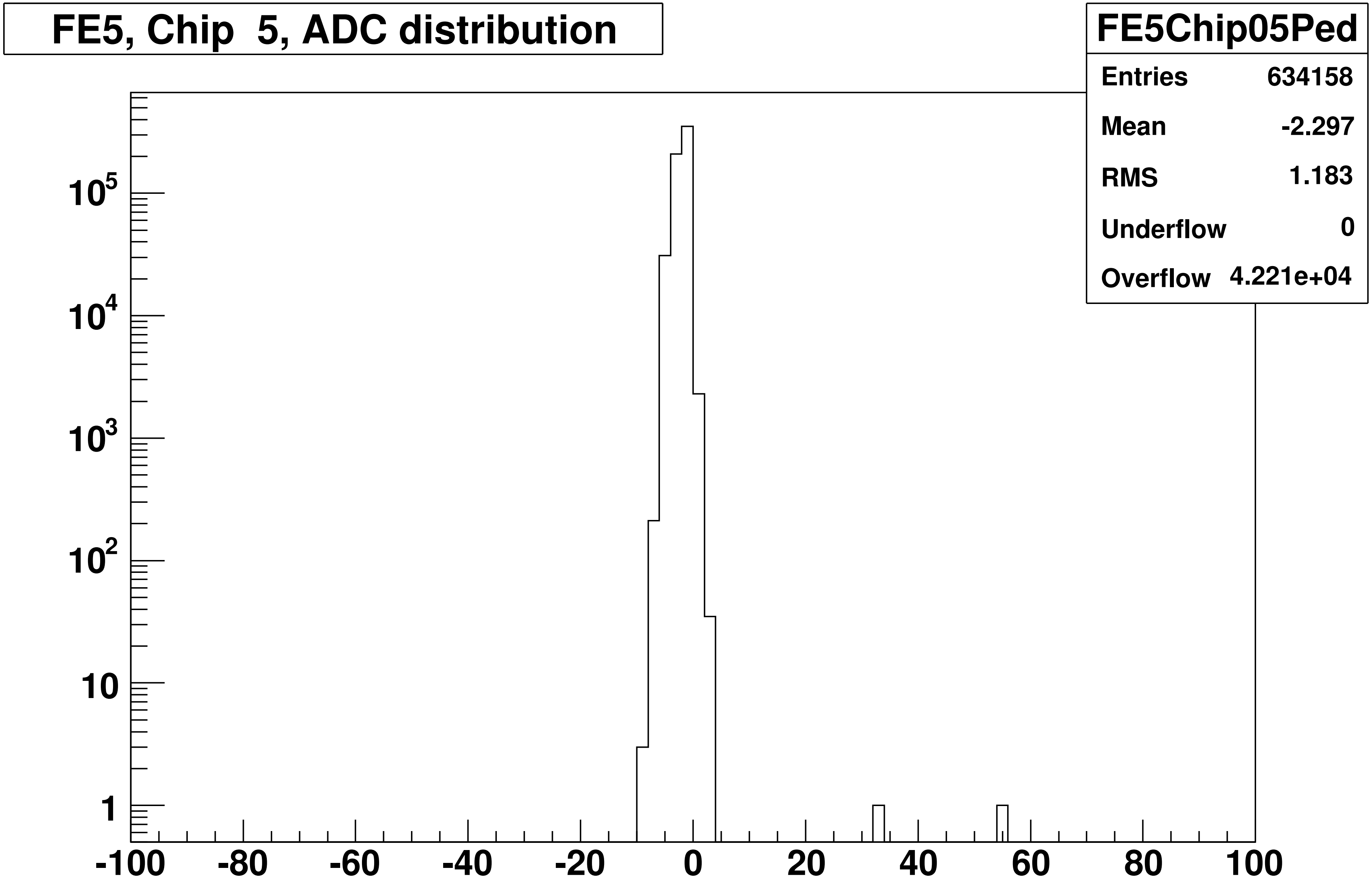
25000



FE5, Chip 5, ADC distribution
FE5Chip05Ped
Entries 634158
Mean -2.297
RMS 1.183
Underflow 0
Overflow 4.221e+04
10^5
10^4
10^3
10^2
10
1
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-20
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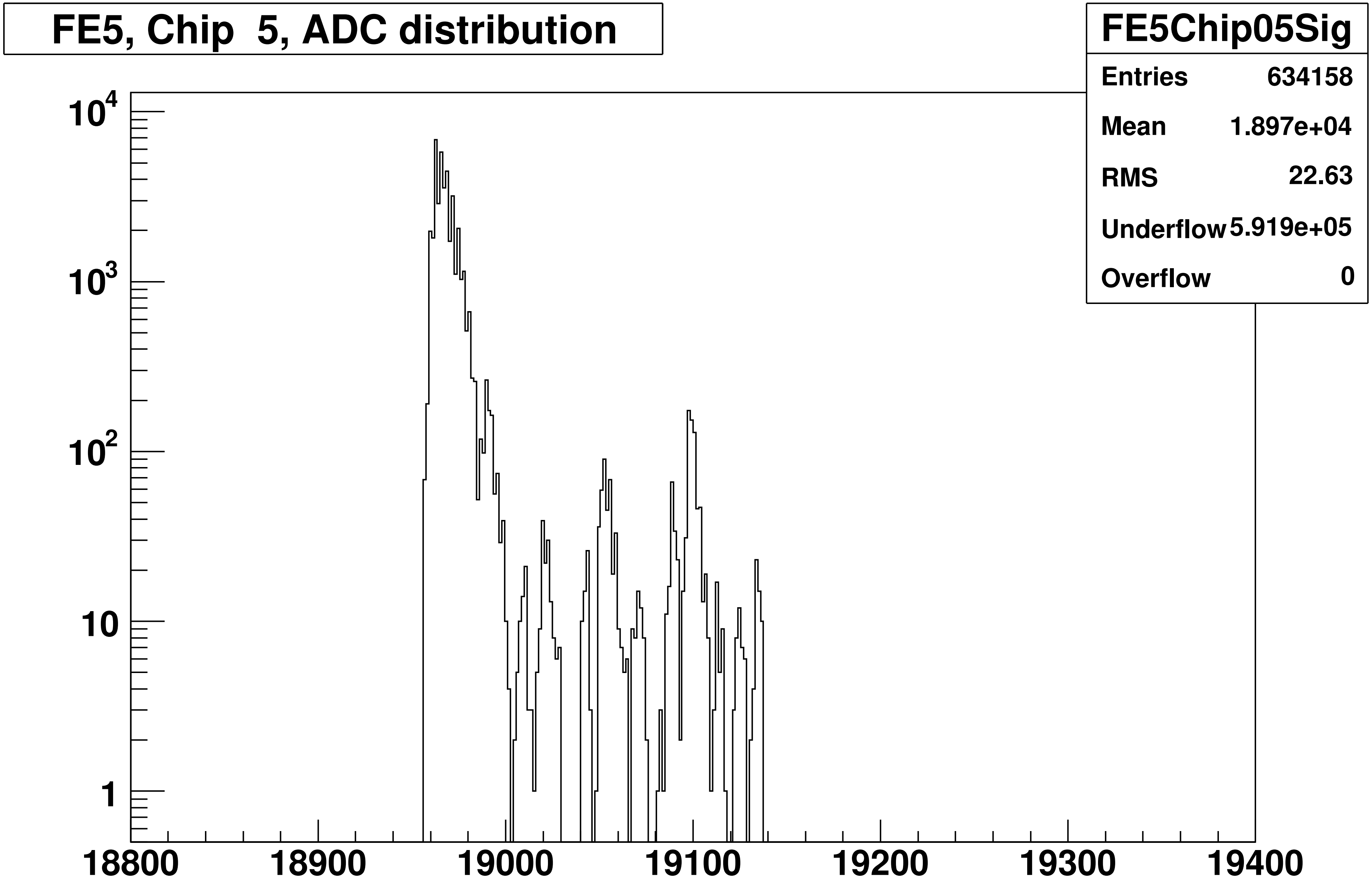
80
100



FE5, Chip 5, ADC distribution
FE5Chip05Sig
Entries 634158
Mean 1.897e+04
RMS 22.63
Underflow 5.919e+05
Overflow 0
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10^3
10^2
10
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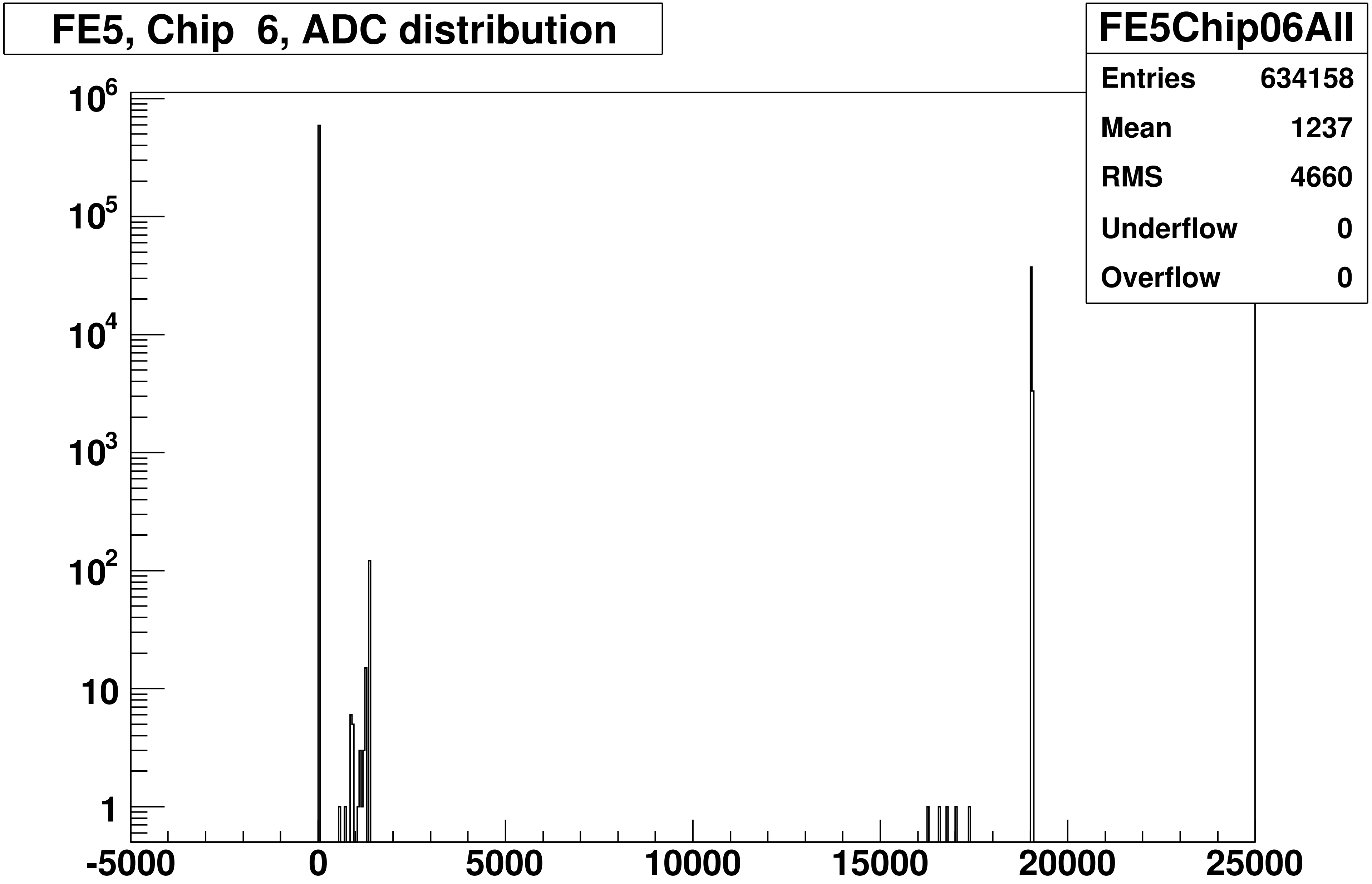
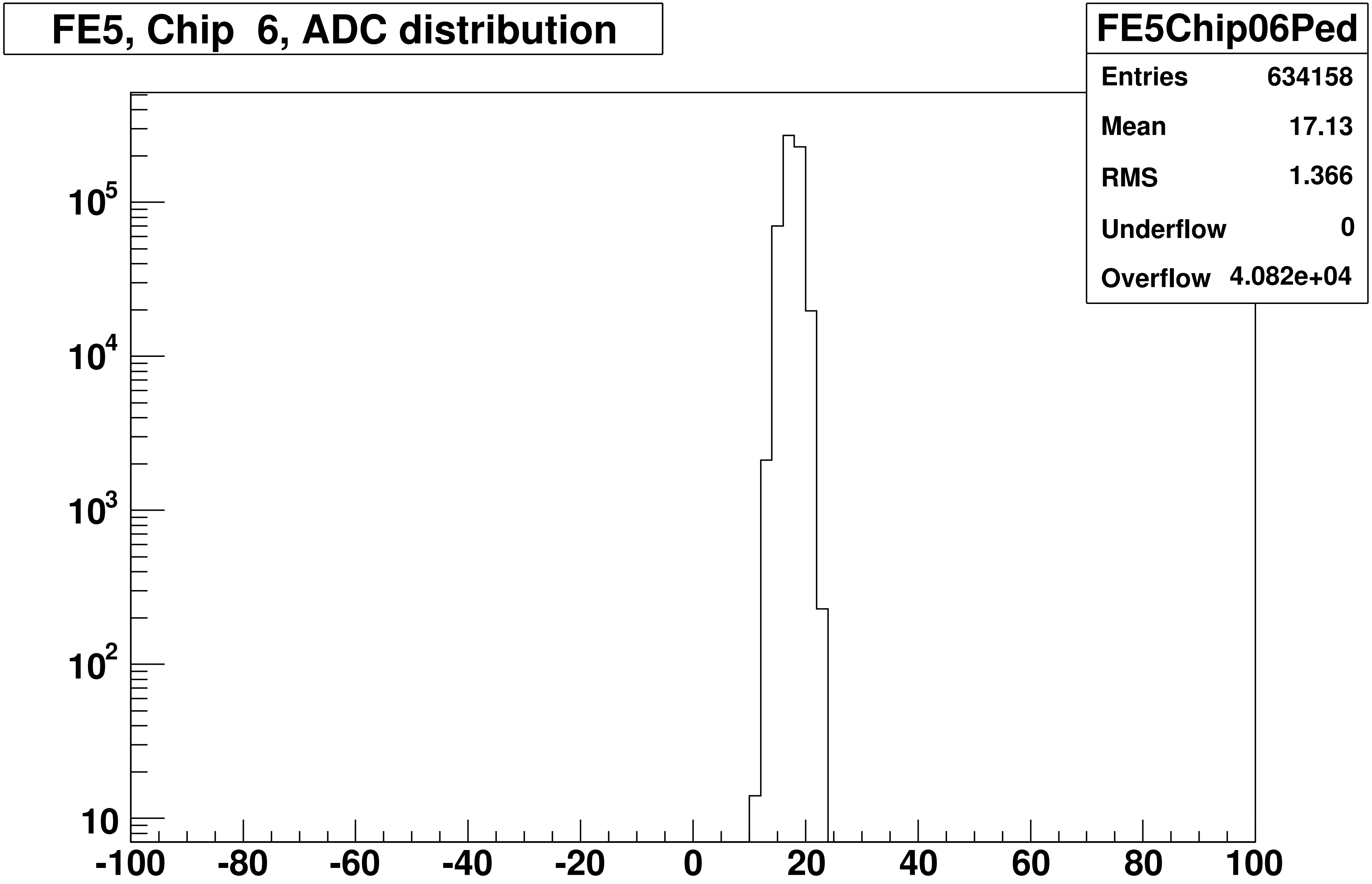

FE5, Chip 6, ADC distribution
FE5Chip06All
Entries 634158
Mean 1237
RMS 4660
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE5, Chip 6, ADC distribution
FE5Chip06Ped
Entries 634158
Mean 17.13
RMS 1.366
Underflow 0
Overflow 4.082e+04
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10^4
10^3
10^2
10
-100
-80
-60
-40
-20
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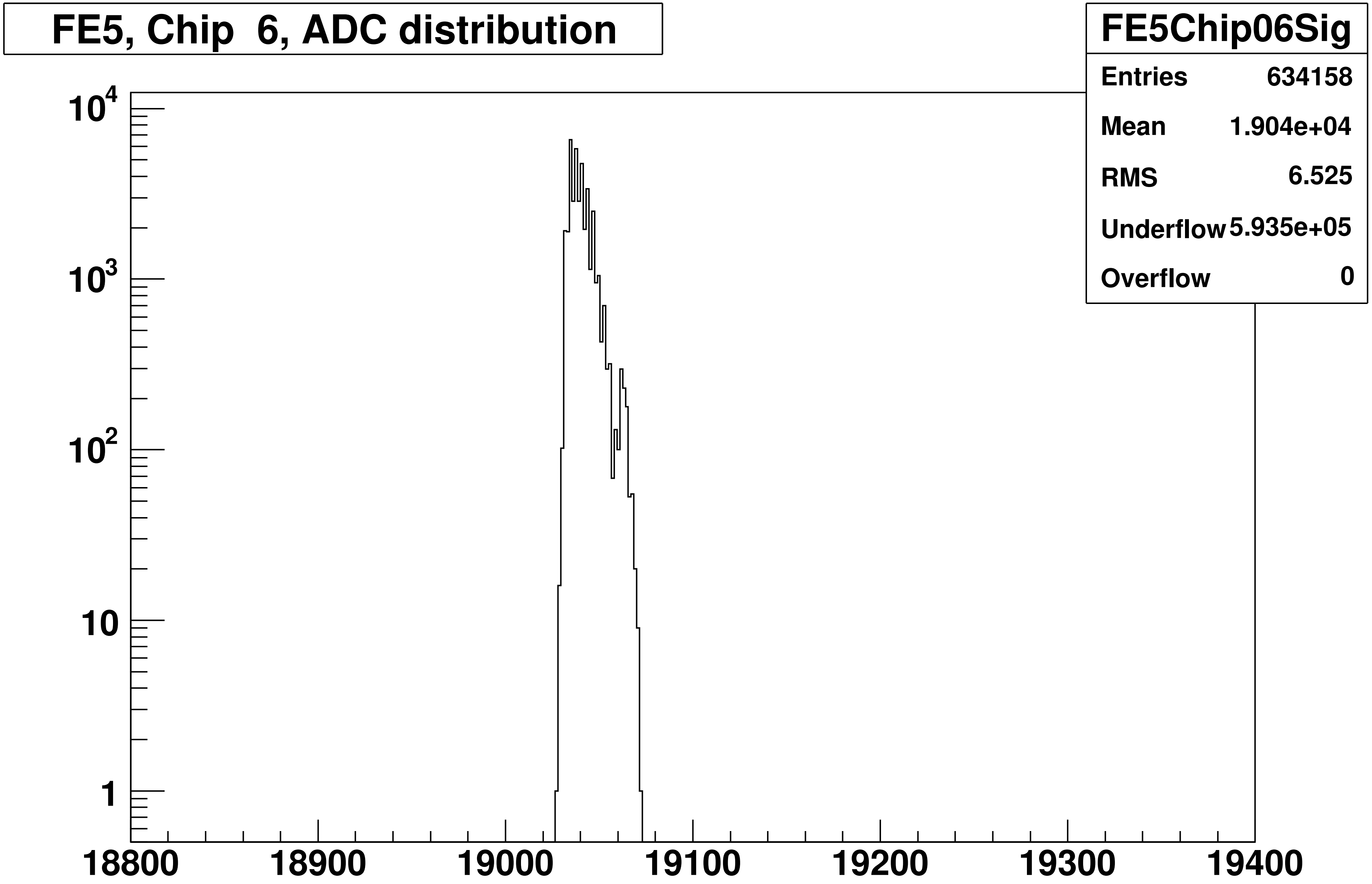
40
60
80
100


FE5, Chip 6, ADC distribution
FE5Chip06Sig
Entries 634158
Mean 1.904e+04
RMS 6.525
Underflow 5.935e+05
Overflow 0
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10^3
10^2
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18800
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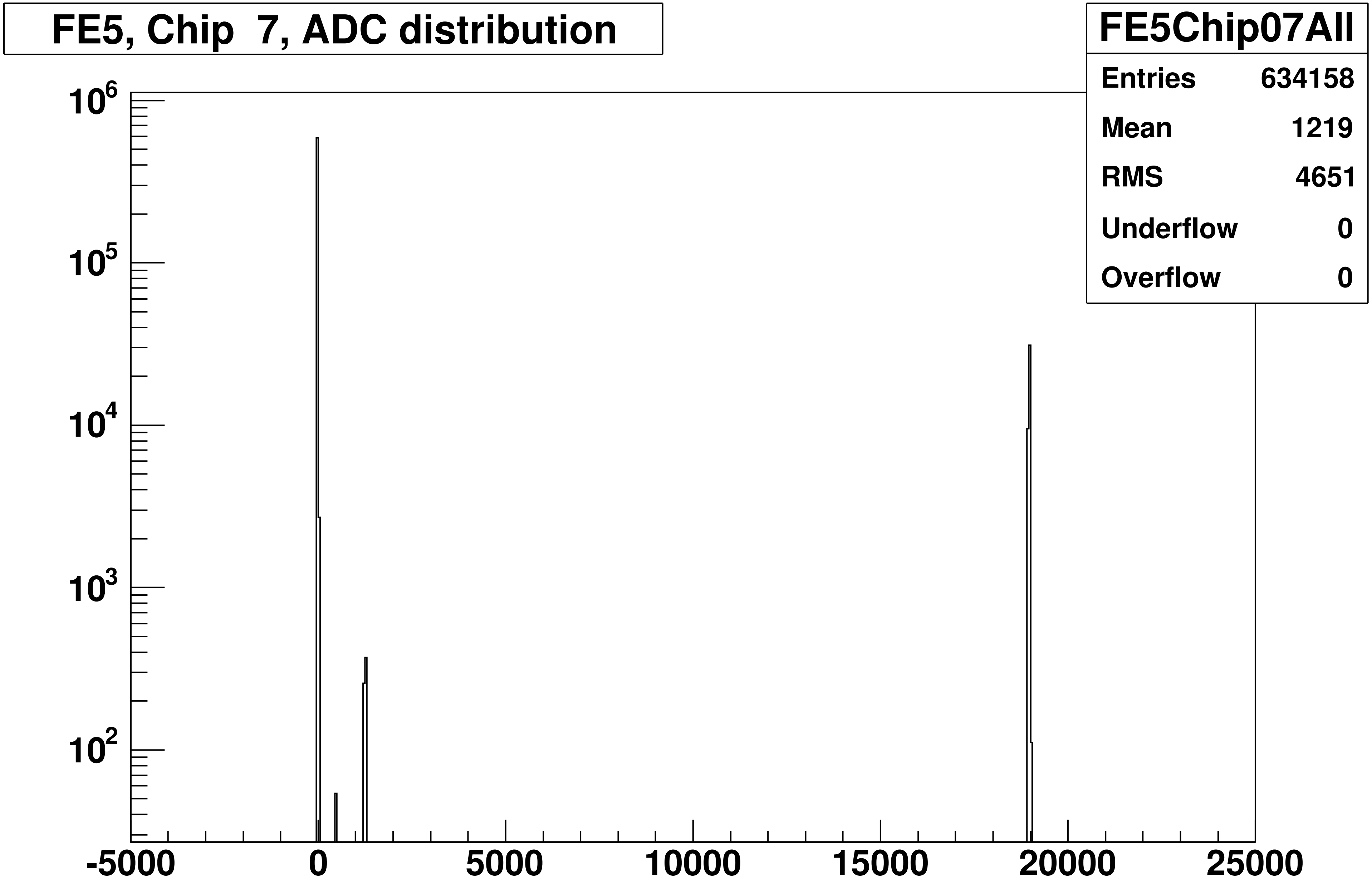
FE5, Chip 7, ADC distribution
FE5Chip07All
Entries 634158
Mean 1219
RMS 4651
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
-5000
0
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10000
15000
20000
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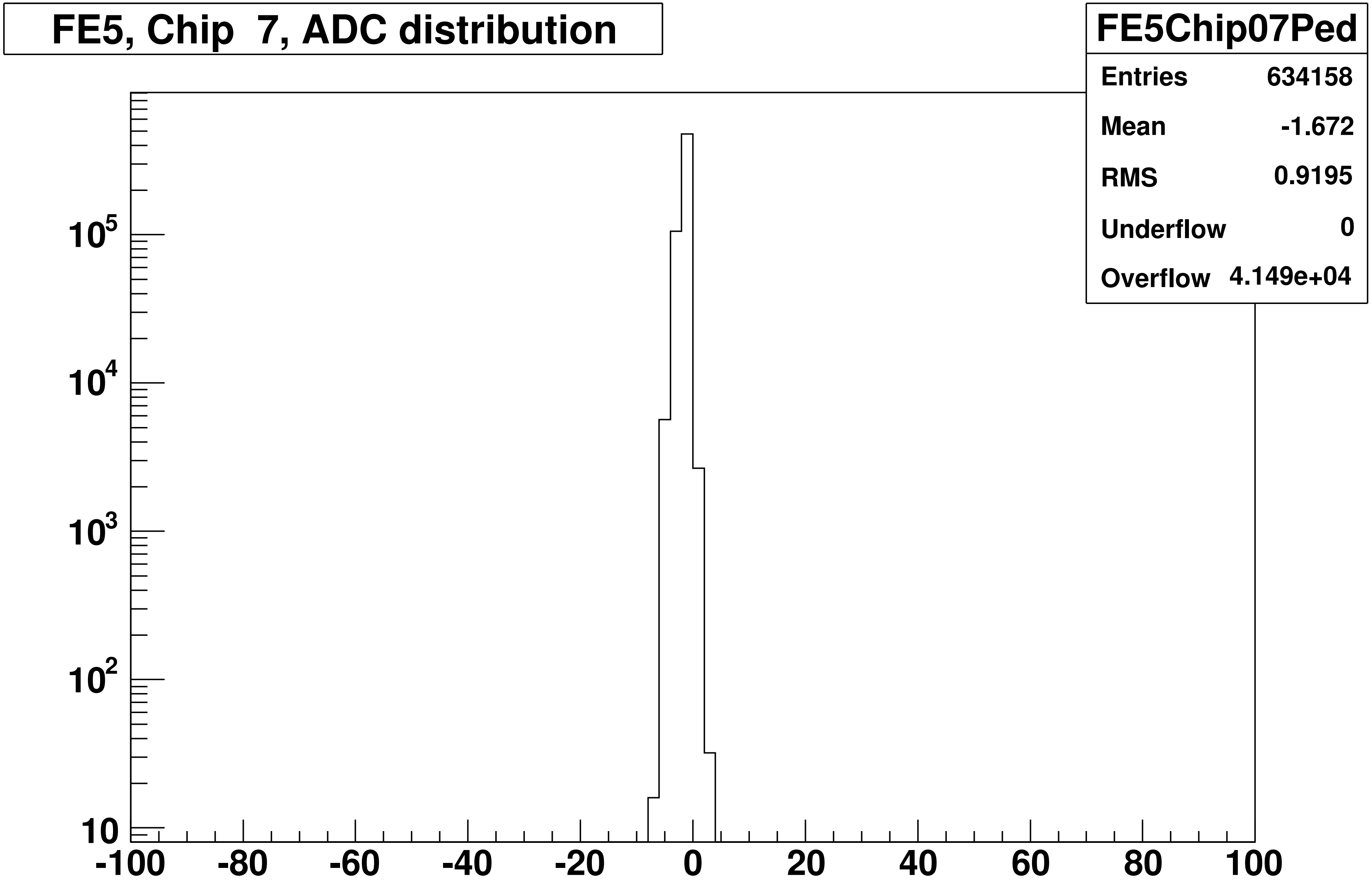
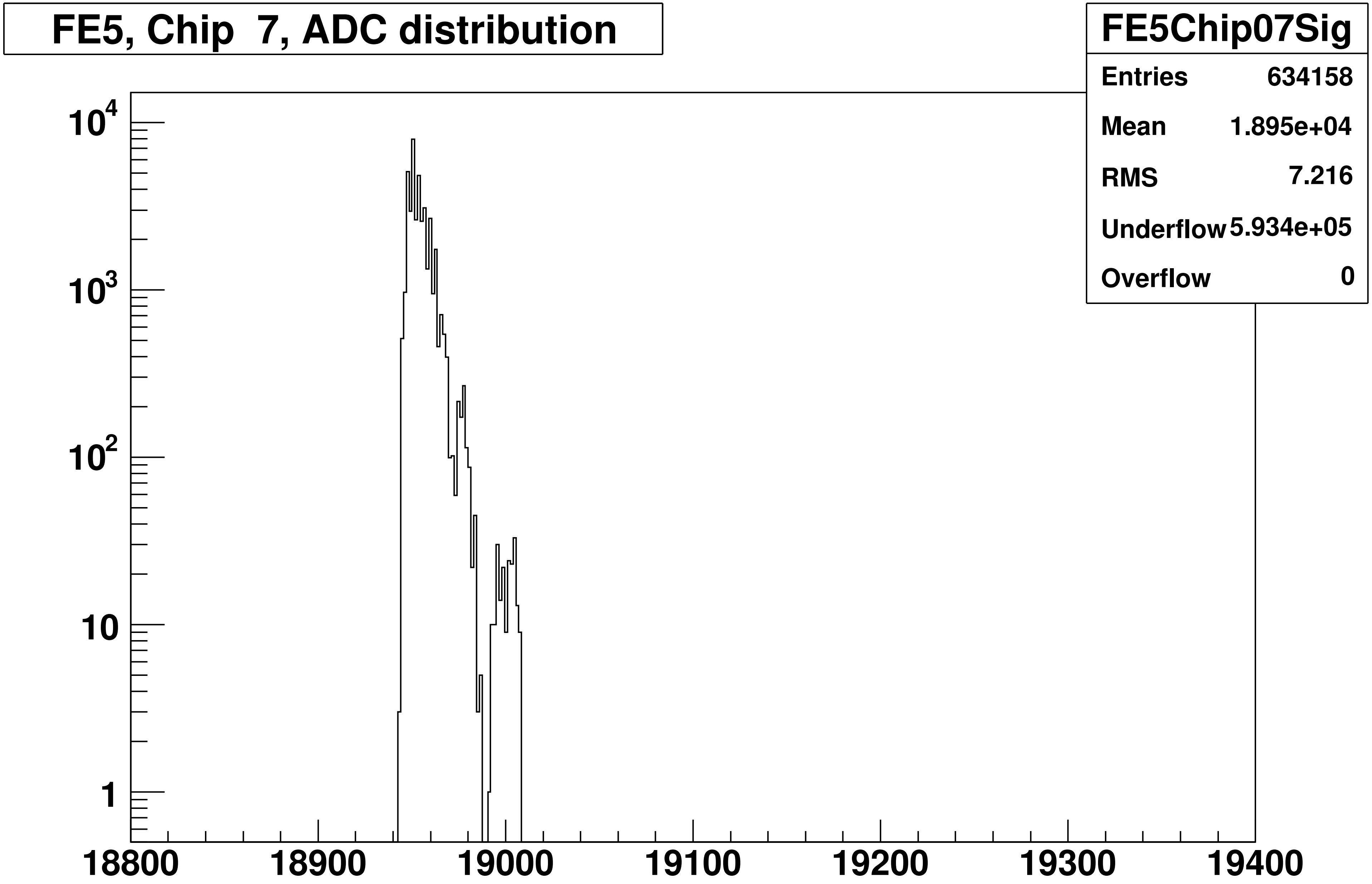

FE5, Chip 7, ADC distribution
FE5Chip07Ped
Entries 634158
Mean -1.672
RMS 0.9195
Underflow 0
Overflow 4.149e+04
10
10^2
10^3
10^4
10^5
-100
-80
-60
-40
-20
0
20
40
60
80
100


FE5, Chip 7, ADC distribution
FE5Chip07Sig
Entries 634158
Mean 1.895e+04
RMS 7.216
Underflow 5.934e+05
Overflow 0
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10^3
10^2
10
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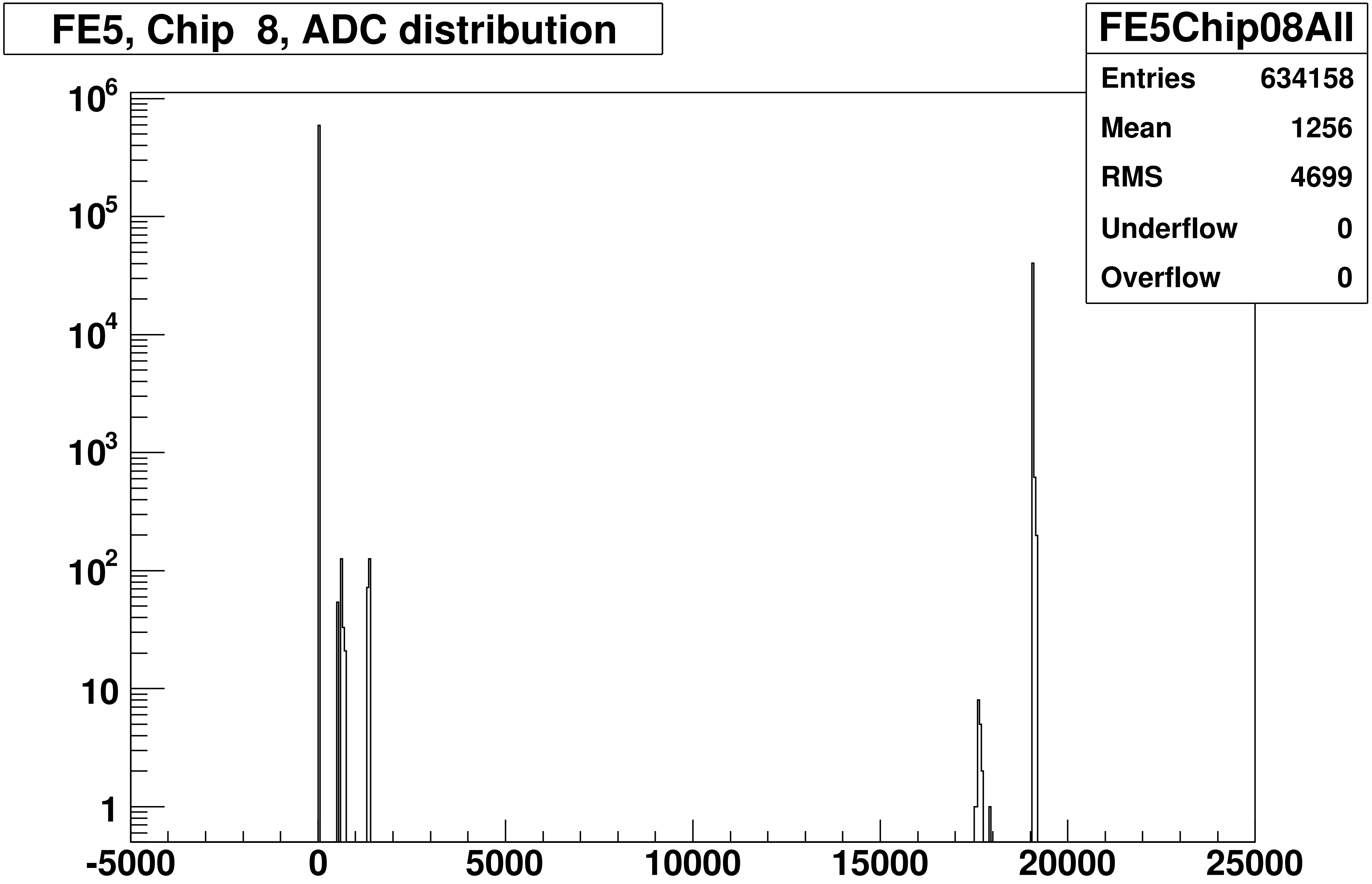
FE5, Chip 8, ADC distribution
FE5Chip08All
Entries 634158
Mean 1256
RMS 4699
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
1
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10000
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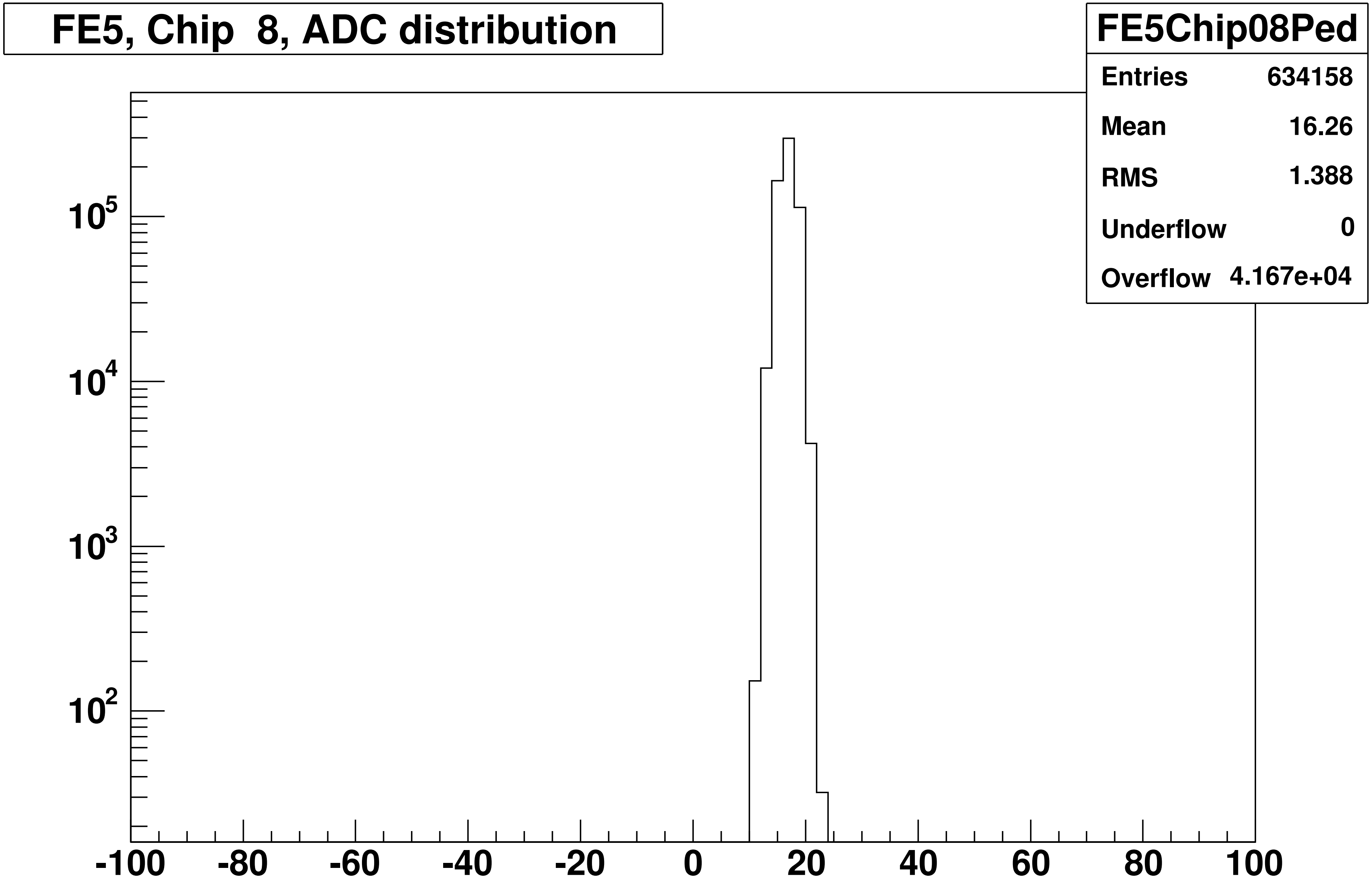
20000
25000


FE5, Chip 8, ADC distribution
FE5Chip08Ped
Entries 634158
Mean 16.26
RMS 1.388
Underflow 0
Overflow 4.167e+04
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10^4
10^3
10^2
-100
-80
-60
-40
-20
0
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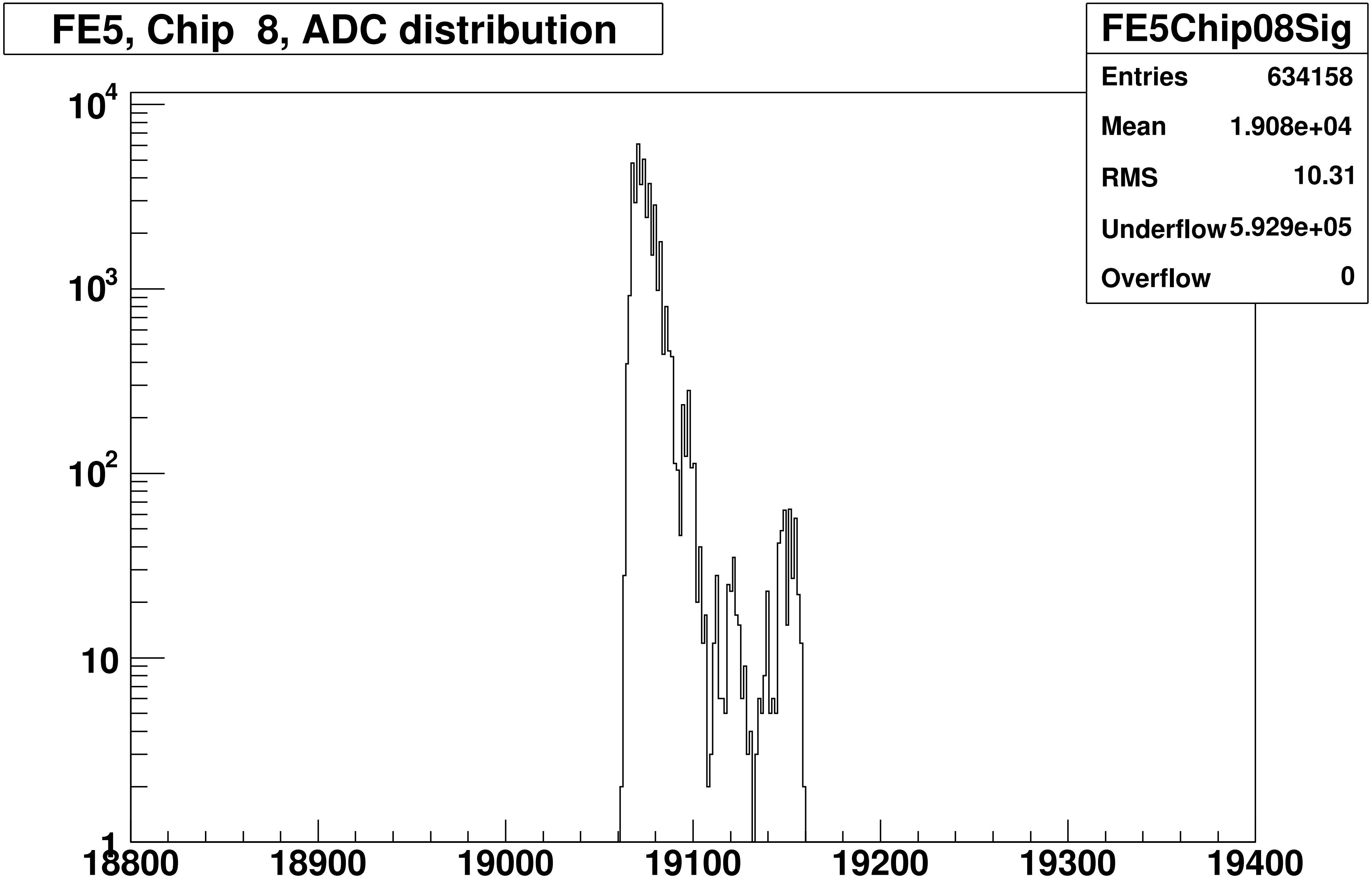
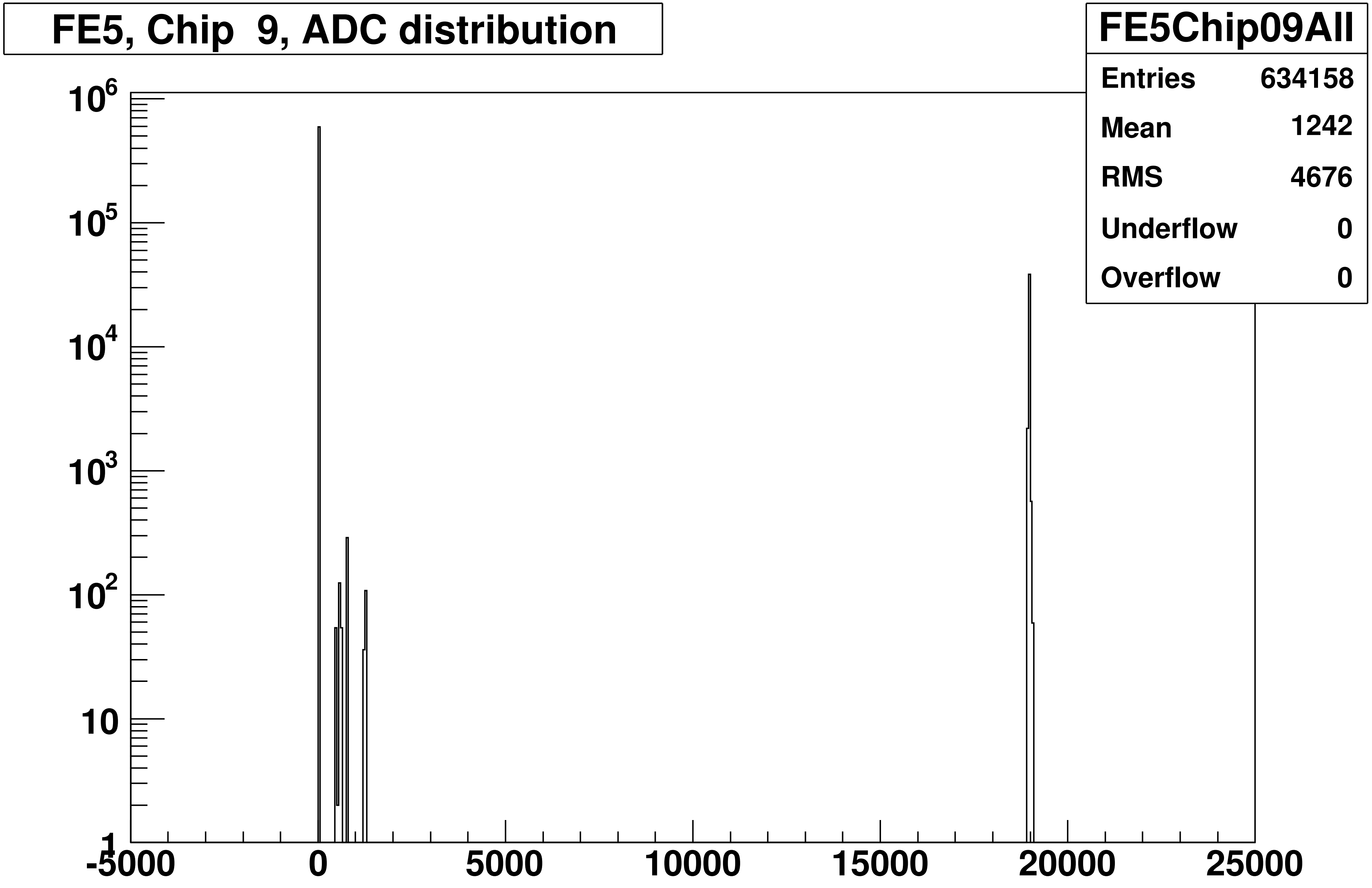
40
60
80
100


FE5, Chip 8, ADC distribution
FE5Chip08Sig
Entries 634158
Mean 1.908e+04
RMS 10.31
Underflow 5.929e+05
Overflow 0
10^4
10^3
10^2
10
1
18800
18900
19000
19100
19200
19300
19400



FE5, Chip 9, ADC distribution
FE5Chip09All
Entries 634158
Mean 1242
RMS 4676
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
1
-5000
0
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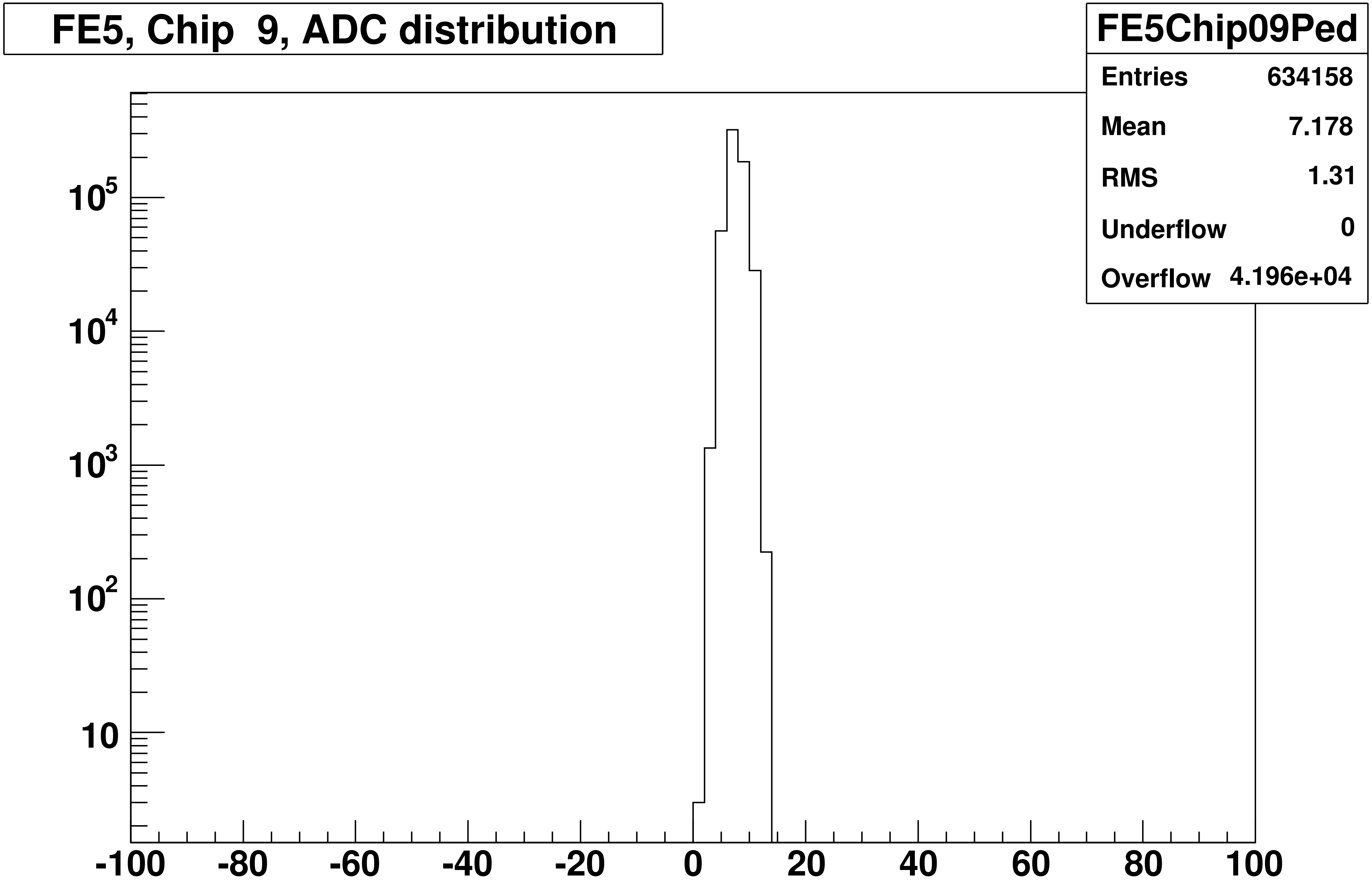
10000
15000
20000
25000


FE5, Chip 9, ADC distribution
FE5Chip09Ped
Entries 634158
Mean 7.178
RMS 1.31
Underflow 0
Overflow 4.196e+04
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10^4
10^3
10^2
10
-100
-80
-60
-40
-20
0
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40
60
80
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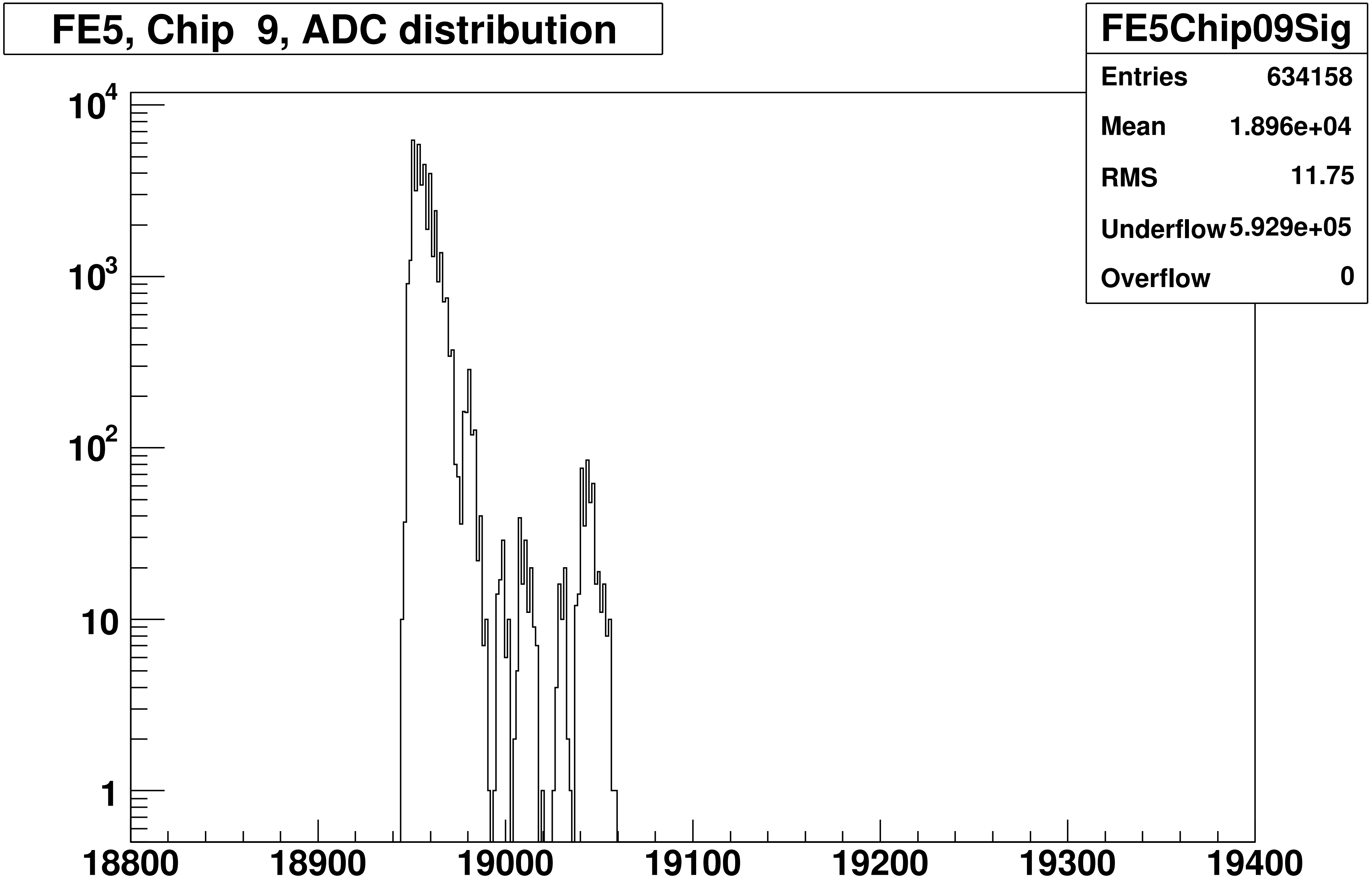
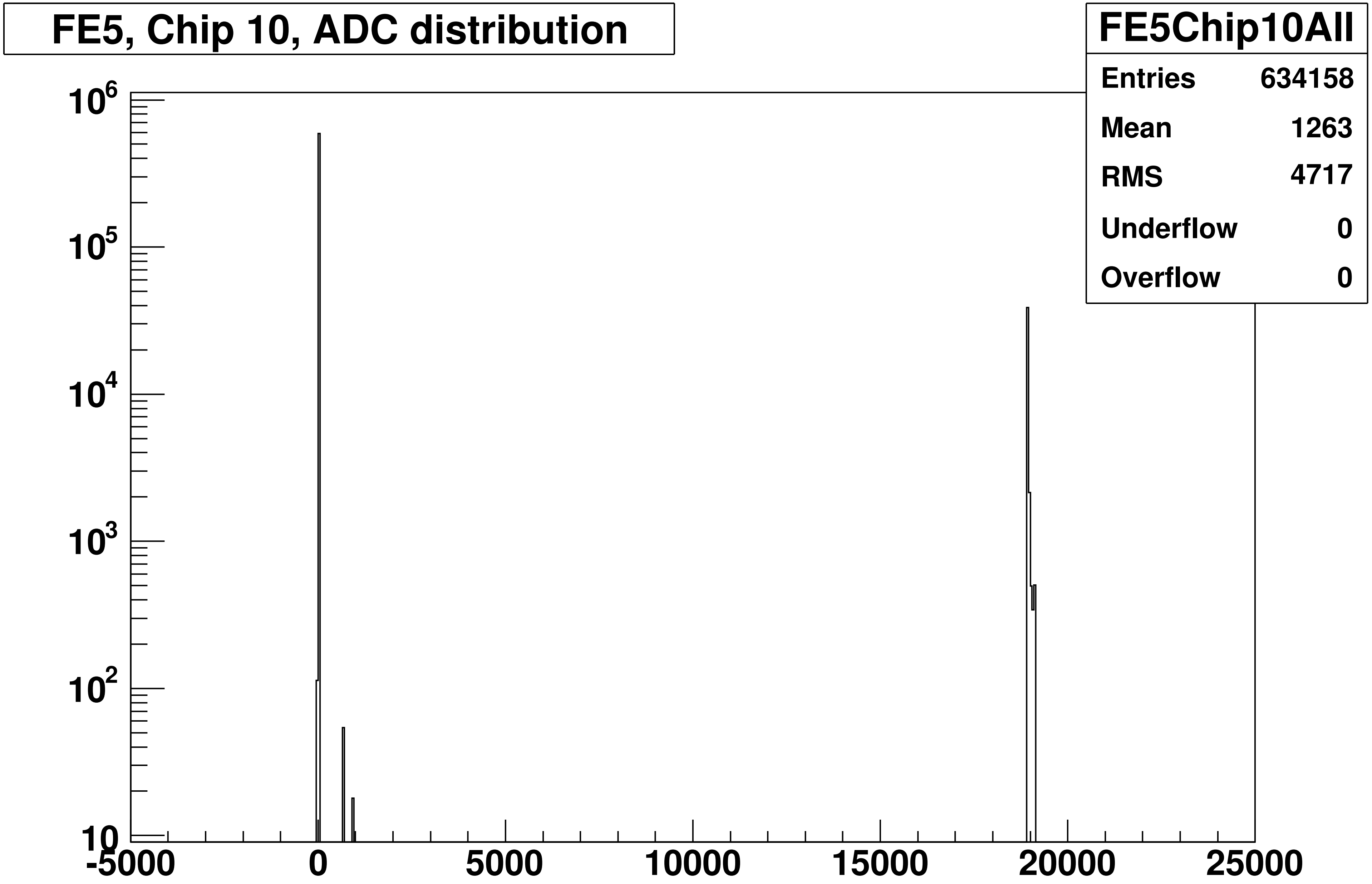

FE5, Chip 9, ADC distribution
FE5Chip09Sig
Entries 634158
Mean 1.896e+04
RMS 11.75
Underflow 5.929e+05
Overflow 0
10^4
10^3
10^2
10
1
18800
18900
19000
19100
19200
19300
19400


FE5, Chip 10, ADC distribution
FE5Chip10All
Entries 634158
Mean 1263
RMS 4717
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
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-5000
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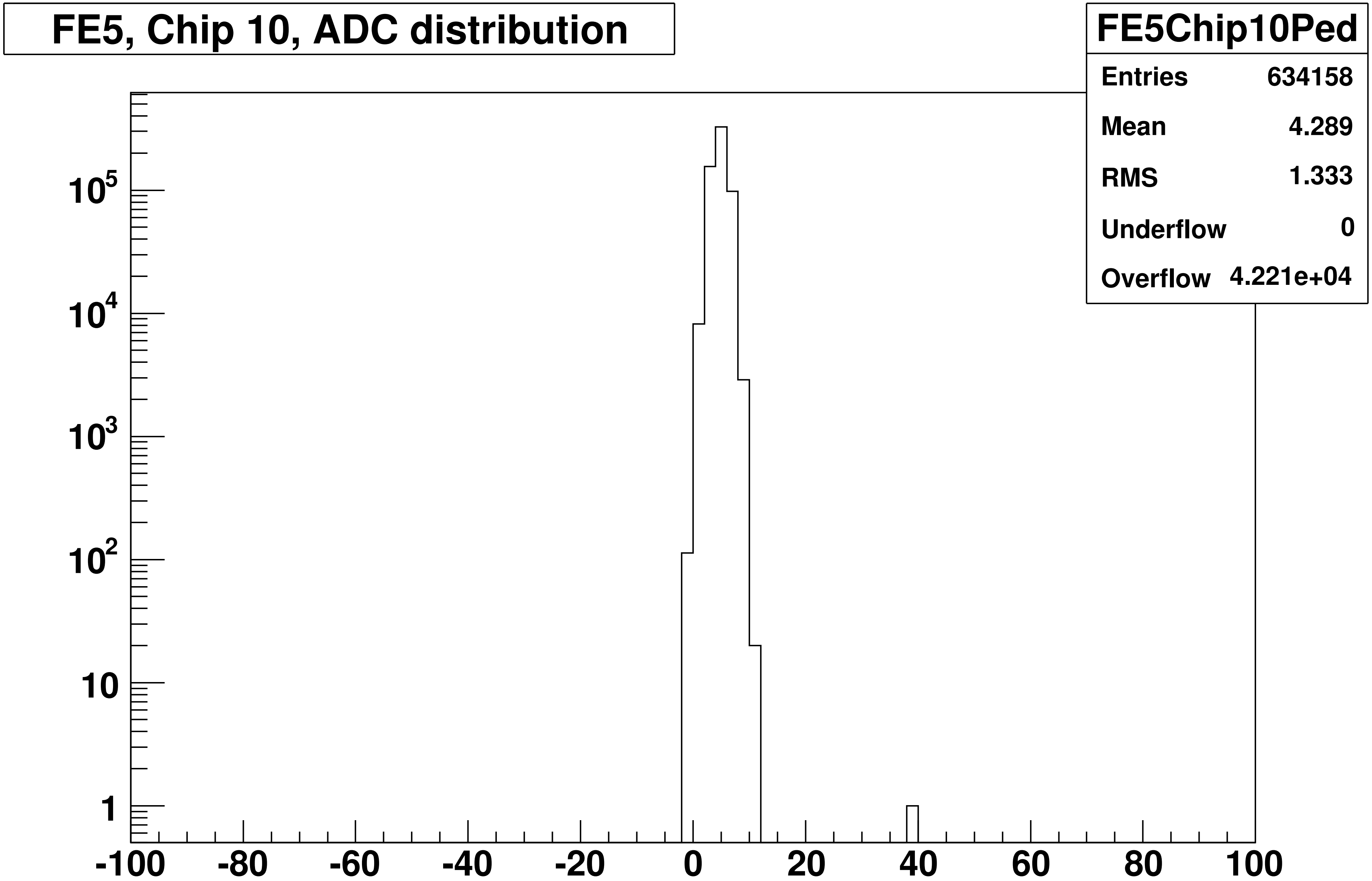
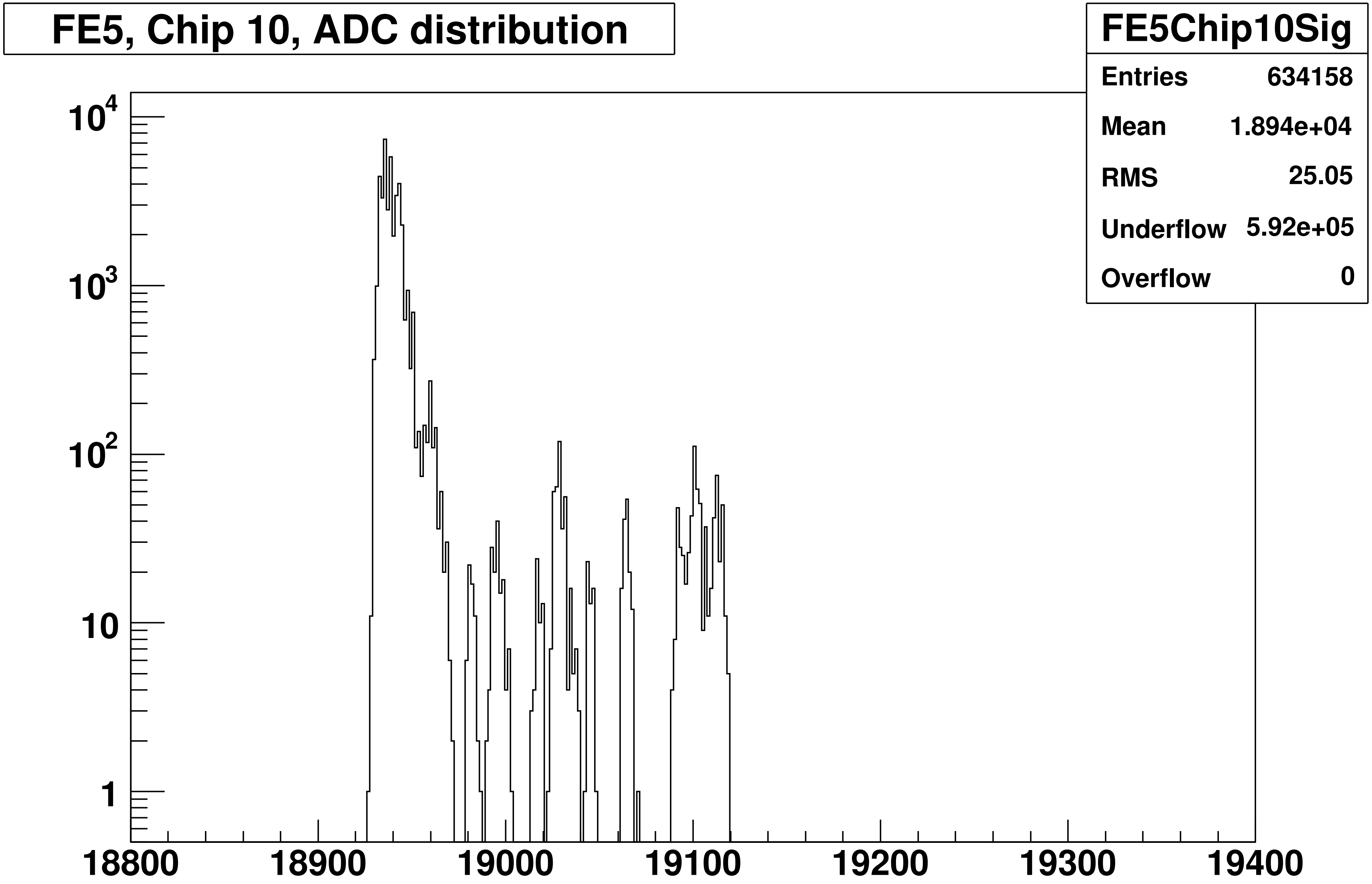
5000
10000
15000
20000
25000



FE5, Chip 10, ADC distribution
FE5Chip10Ped
Entries 634158
Mean 4.289
RMS 1.333
Underflow 0
Overflow 4.221e+04
10^5
10^4
10^3
10^2
10
1
-100
-80
-60
-40
-20
0
20
40
60
80
100


FE5, Chip 10, ADC distribution
FE5Chip10Sig
Entries 634158
Mean 1.894e+04
RMS 25.05
Underflow 5.92e+05
Overflow 0
10^4
10^3
10^2
10
1
18800
18900
19000
19100
19200
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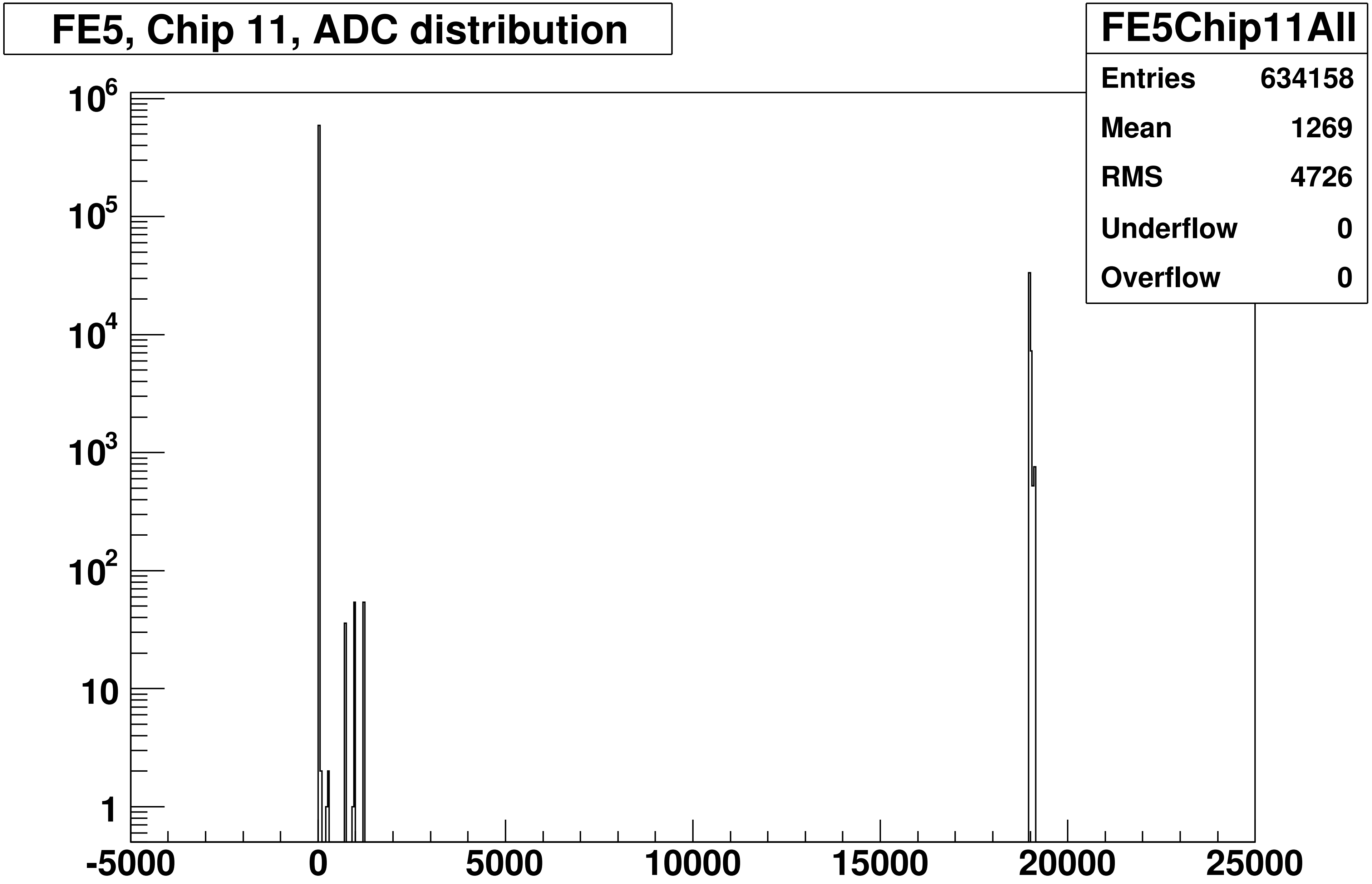
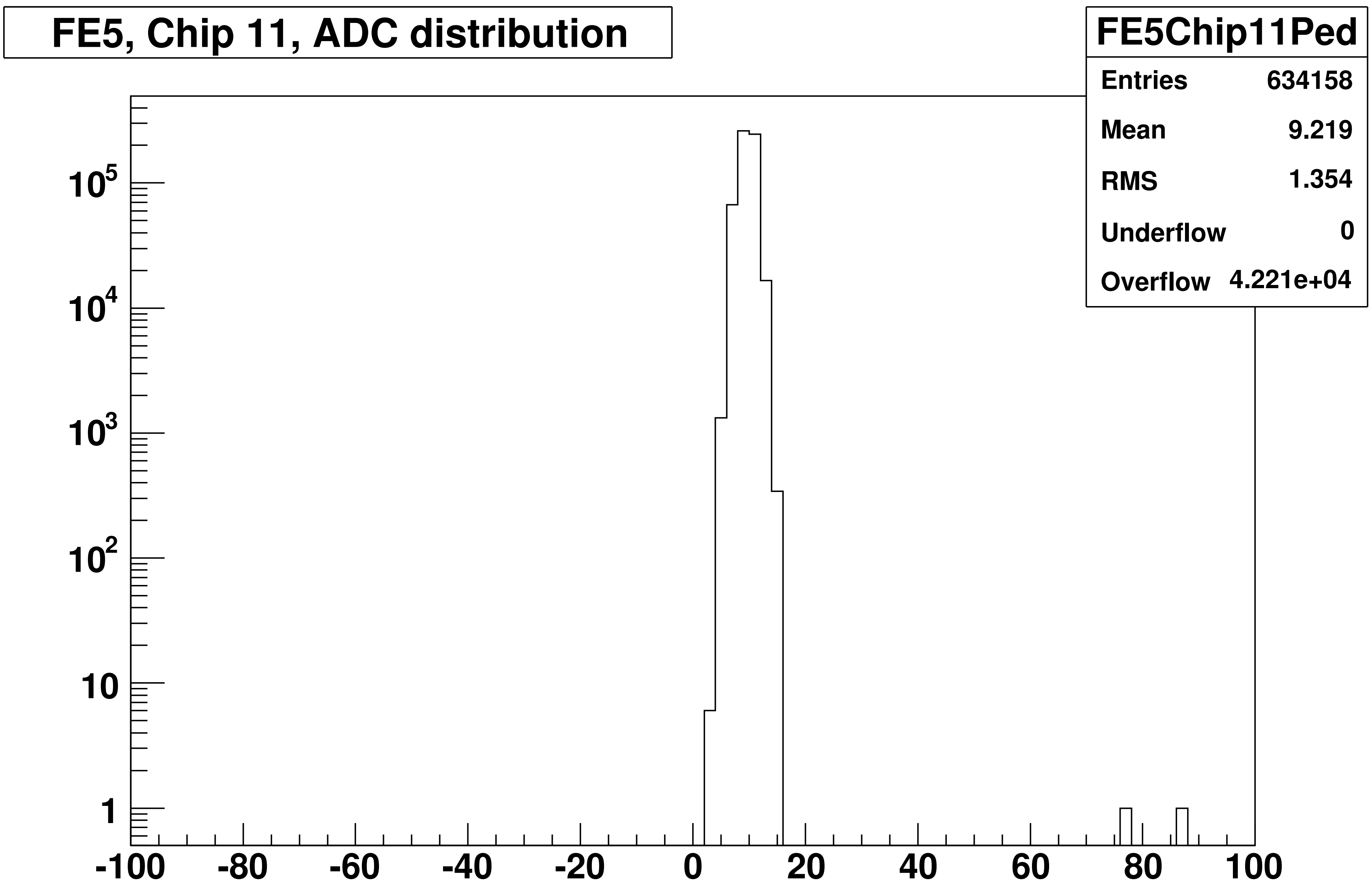
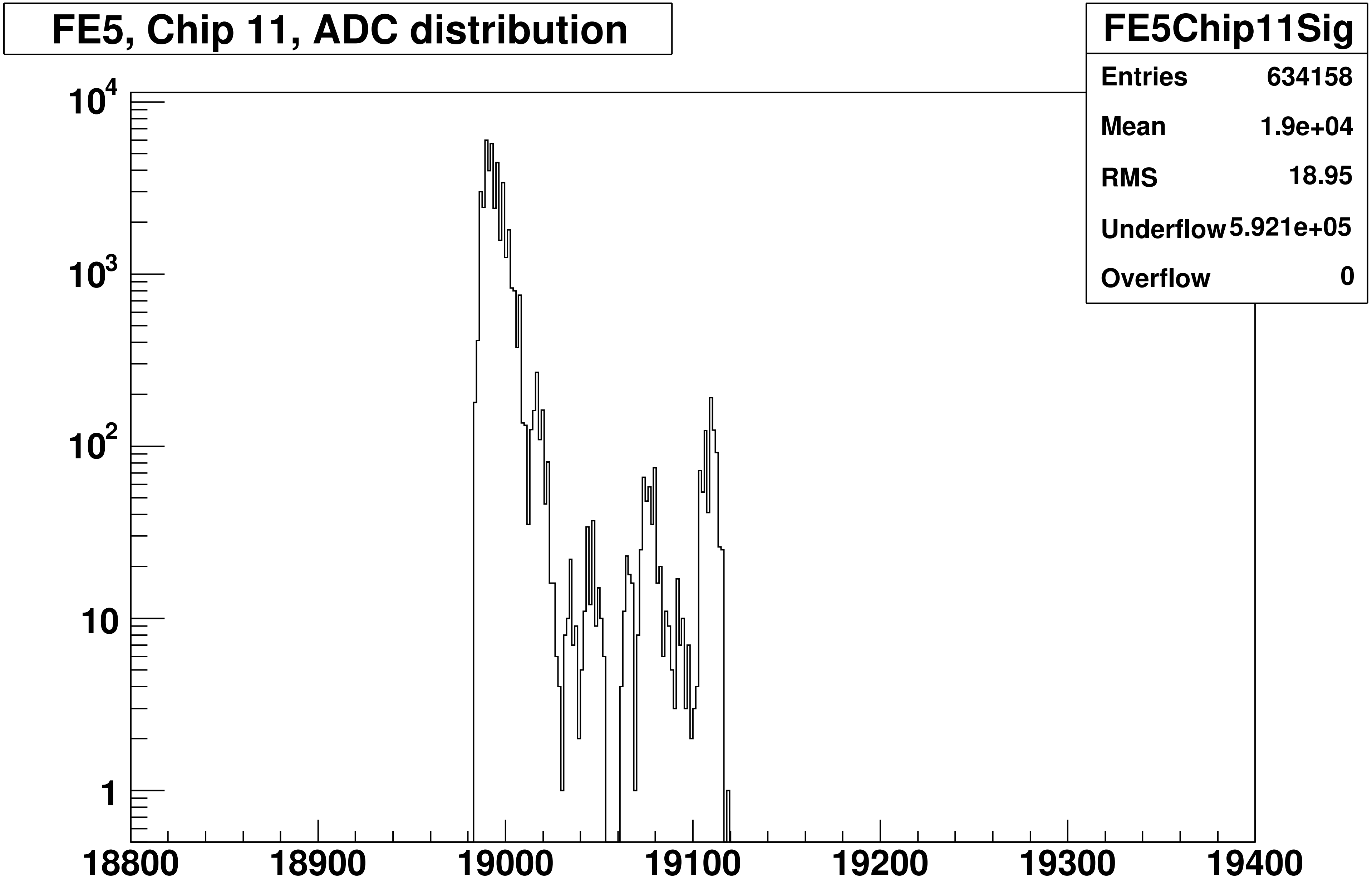
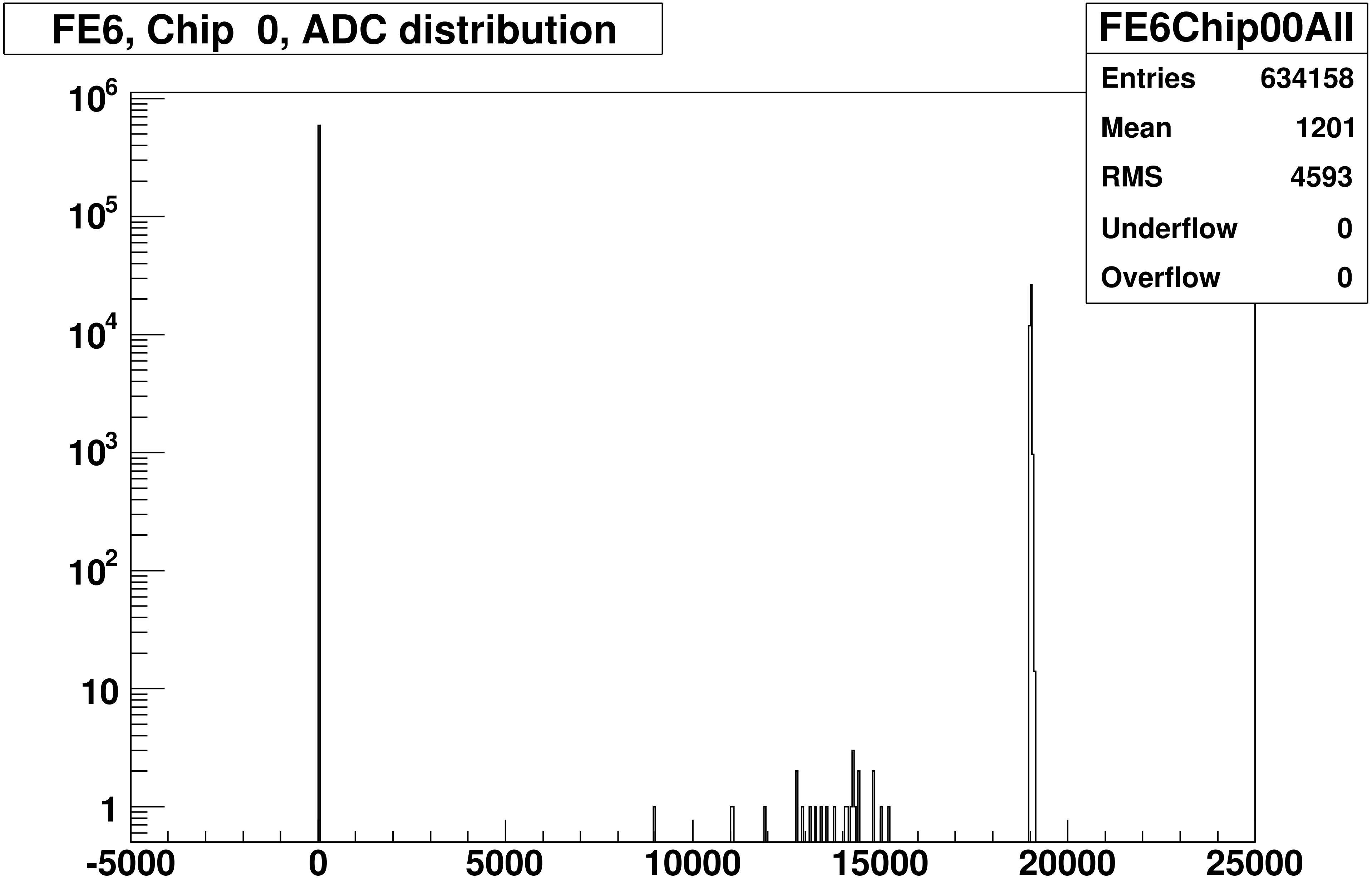
19400


FE5, Chip 11, ADC distribution
FE5Chip11All
Entries 634158
Mean 1269
RMS 4726
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000

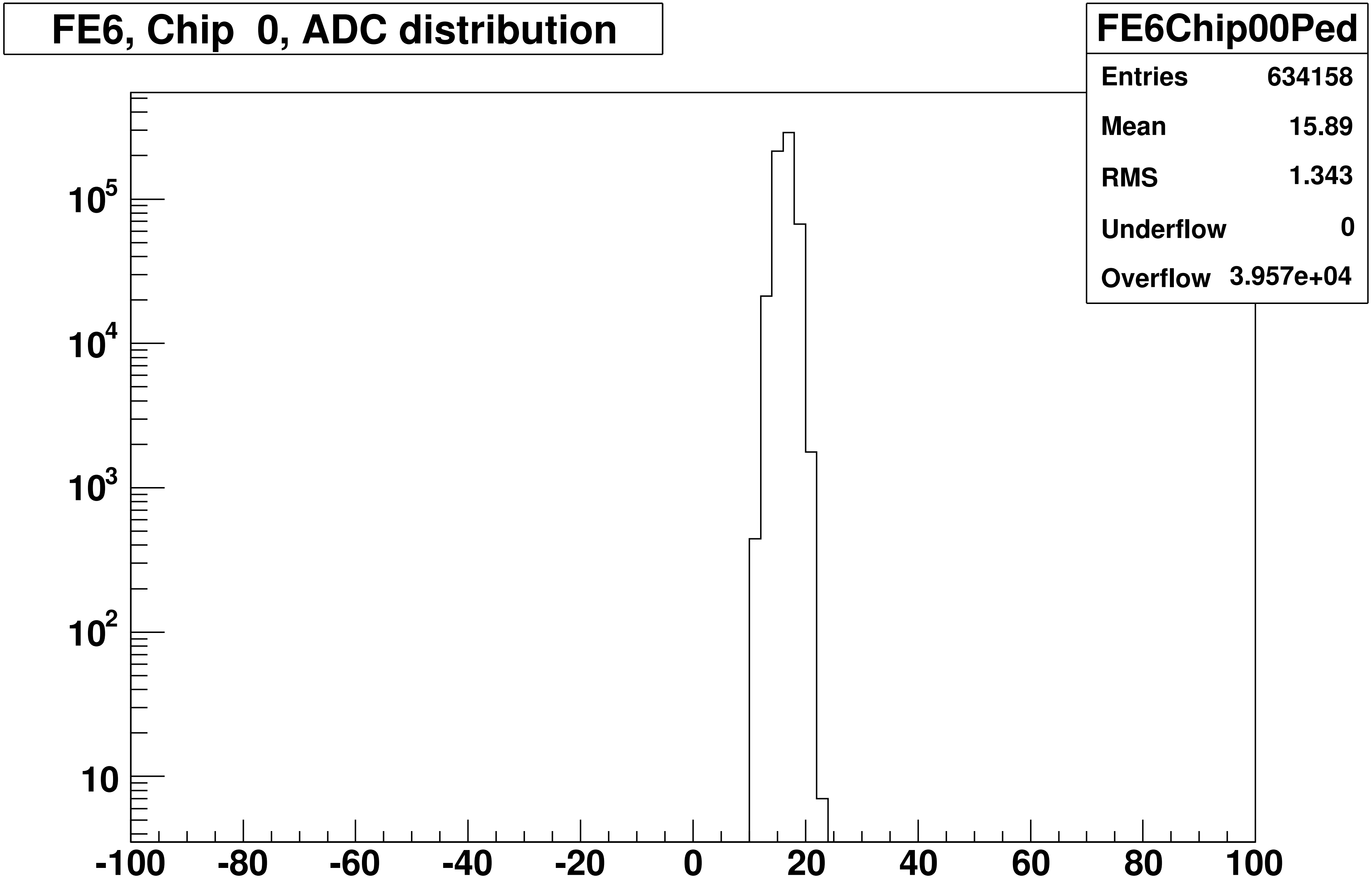

FE5, Chip 11, ADC distribution
FE5Chip11Ped
Entries 634158
Mean 9.219
RMS 1.354
Underflow 0
Overflow 4.221e+04
10^5
10^4
10^3
10^2
10
1
-100
-80
-60
-40
-20
0
20
40
60
80
100



FE5, Chip 11, ADC distribution
FE5Chip11Sig
Entries 634158
Mean 1.9e+04
RMS 18.95
Underflow 5.921e+05
Overflow 0
10^4
10^3
10^2
10
1
18800
18900
19000
19100
19200
19300
19400



FE6, Chip 0, ADC distribution
FE6Chip00All
Entries 634158
Mean 1201
RMS 4593
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE6, Chip 0, ADC distribution
FE6Chip00Ped
Entries 634158
Mean 15.89
RMS 1.343
Underflow 0
Overflow 3.957e+04
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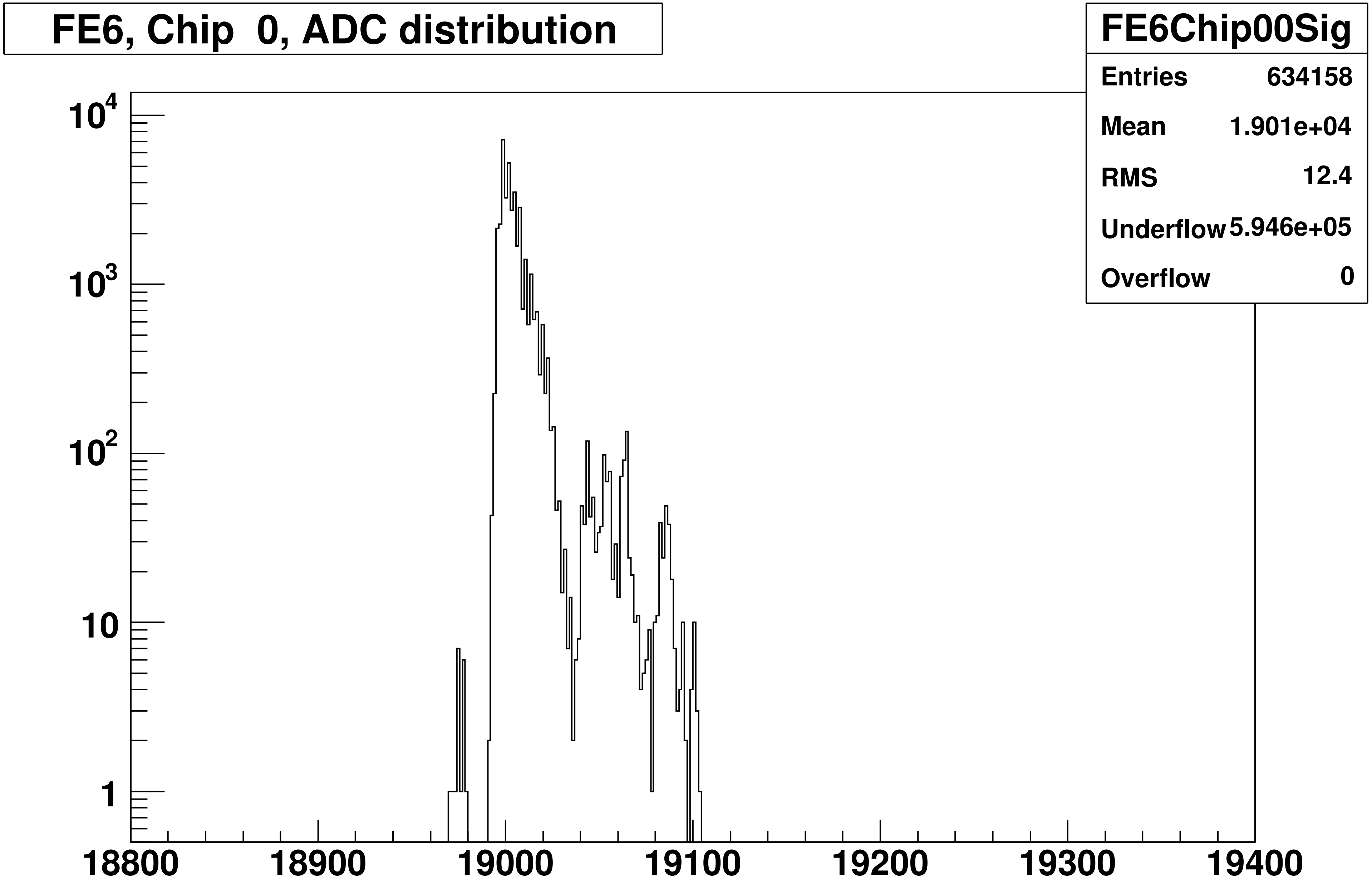
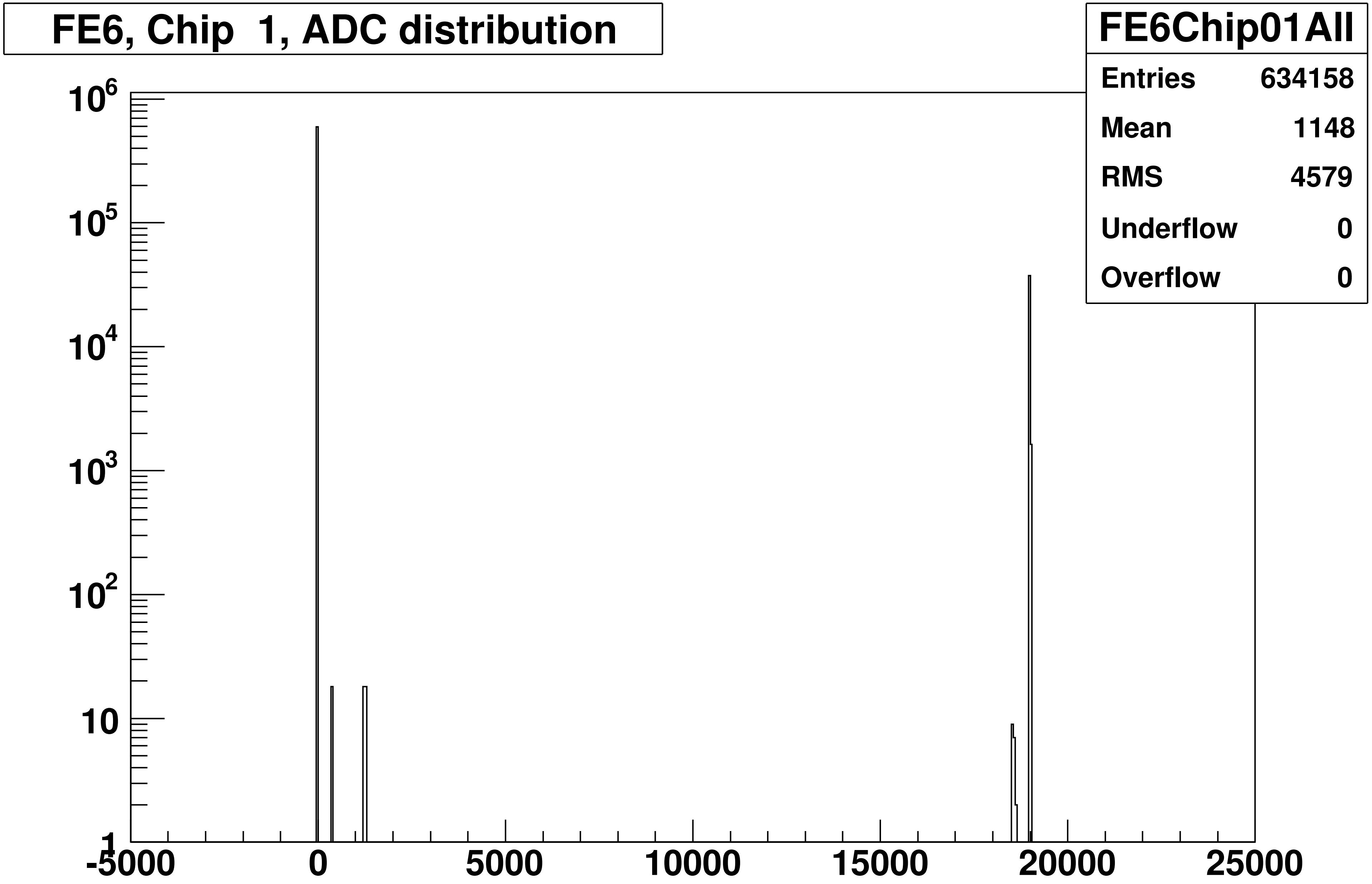
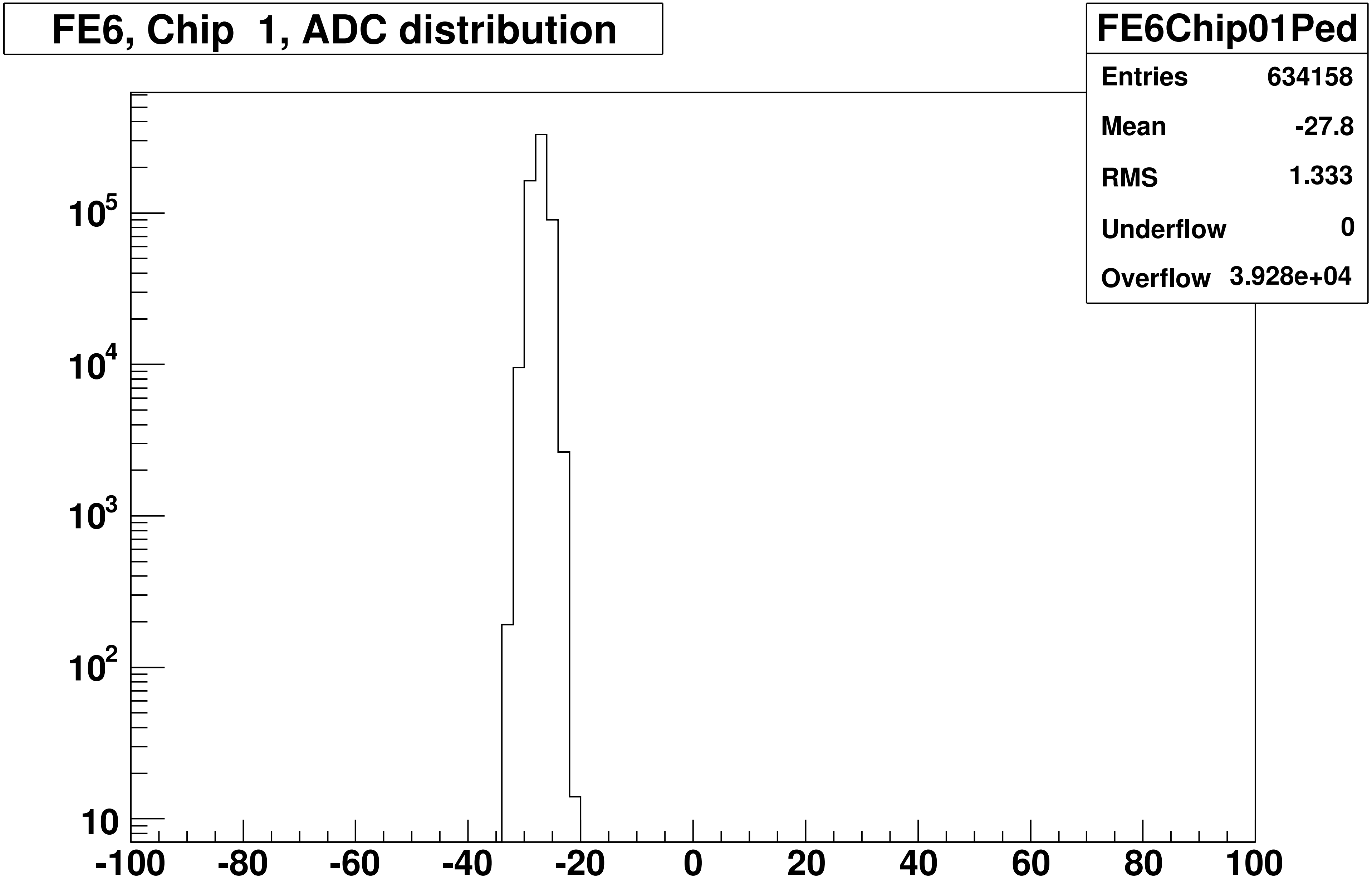
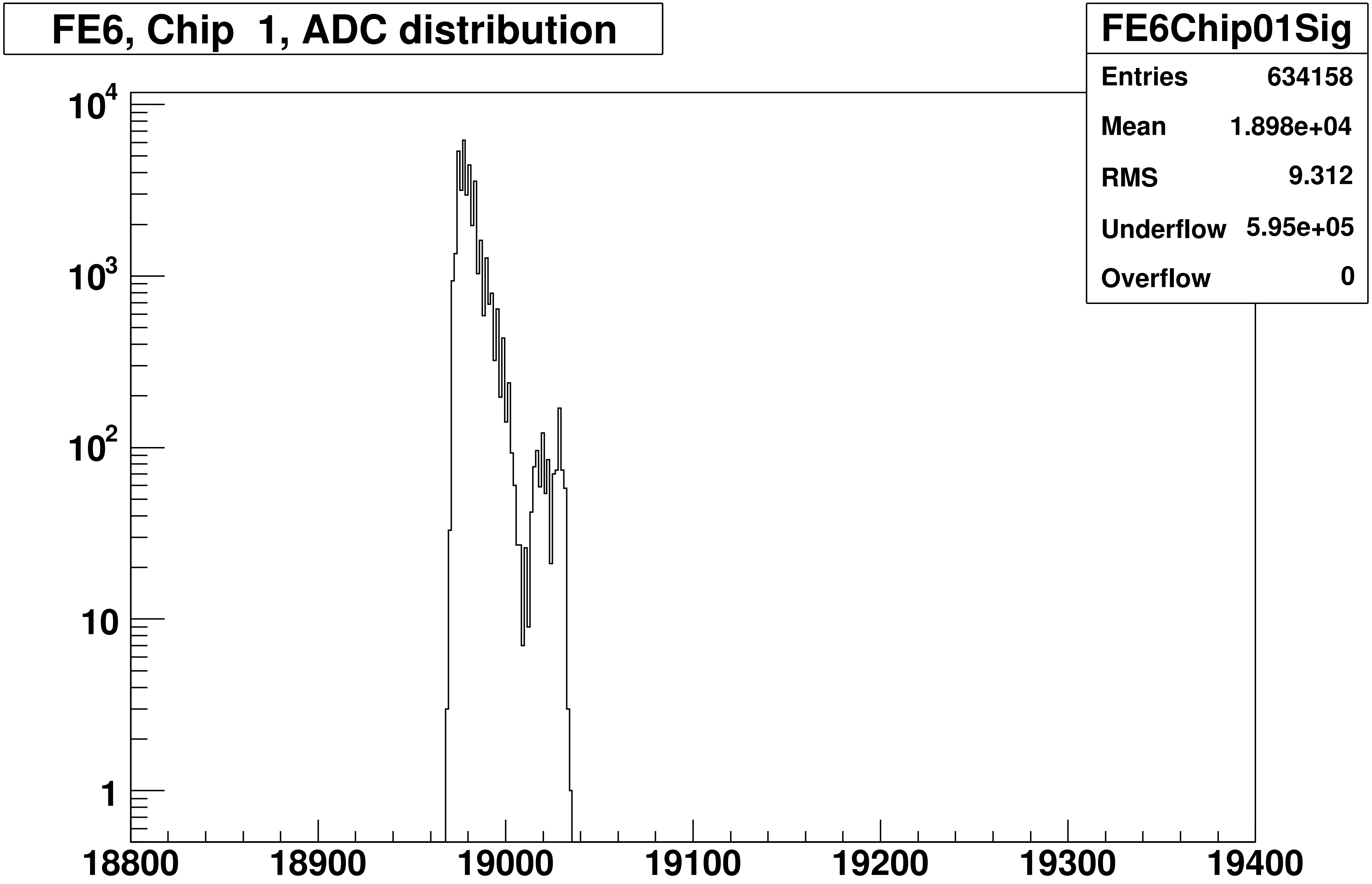
10^2
10^3
10^4
10^5
-100
-80
-60
-40
-20
0
20
40
60
80
100


FE6, Chip 0, ADC distribution
FE6Chip00Sig
Entries 634158
Mean 1.901e+04
RMS 12.4
Underflow 5.946e+05
Overflow 0
10^4
10^3
10^2
10
1
18800
18900
19000
19100
19200
19300
19400


FE6, Chip 1, ADC distribution
FE6Chip01All
Entries 634158
Mean 1148
RMS 4579
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE6, Chip 1, ADC distribution
FE6Chip01Ped
Entries 634158
Mean -27.8
RMS 1.333
Underflow 0
Overflow 3.928e+04
10^5
10^4
10^3
10^2
10
-100
-80
-60
-40
-20
0
20
40
60
80
100



FE6, Chip 1, ADC distribution
FE6Chip01Sig
Entries 634158
Mean 1.898e+04
RMS 9.312
Underflow 5.95e+05
Overflow 0
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10^3
10^2
10
1
18800
18900
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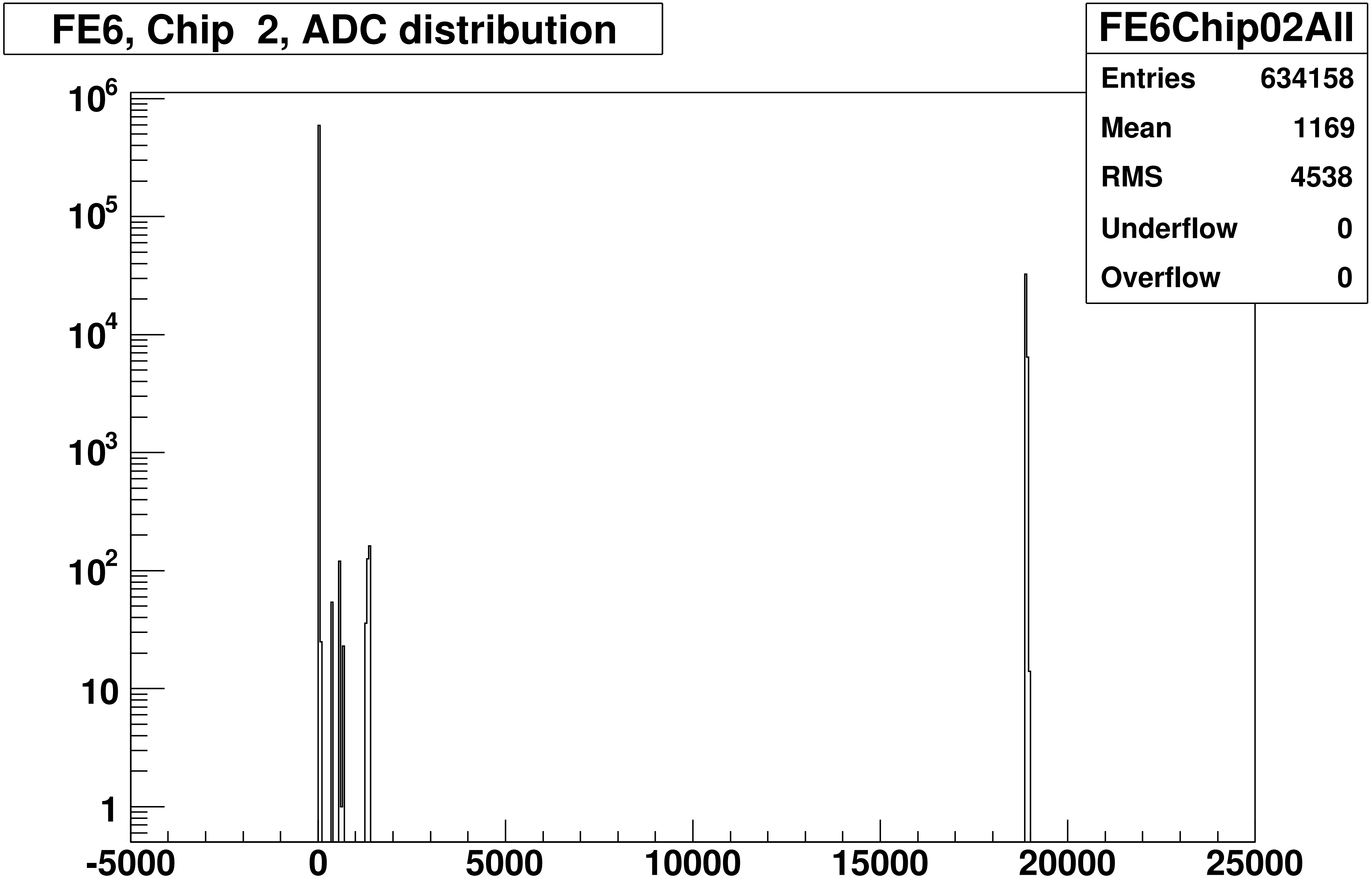

FE6, Chip 2, ADC distribution
FE6Chip02All
Entries 634158
Mean 1169
RMS 4538
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
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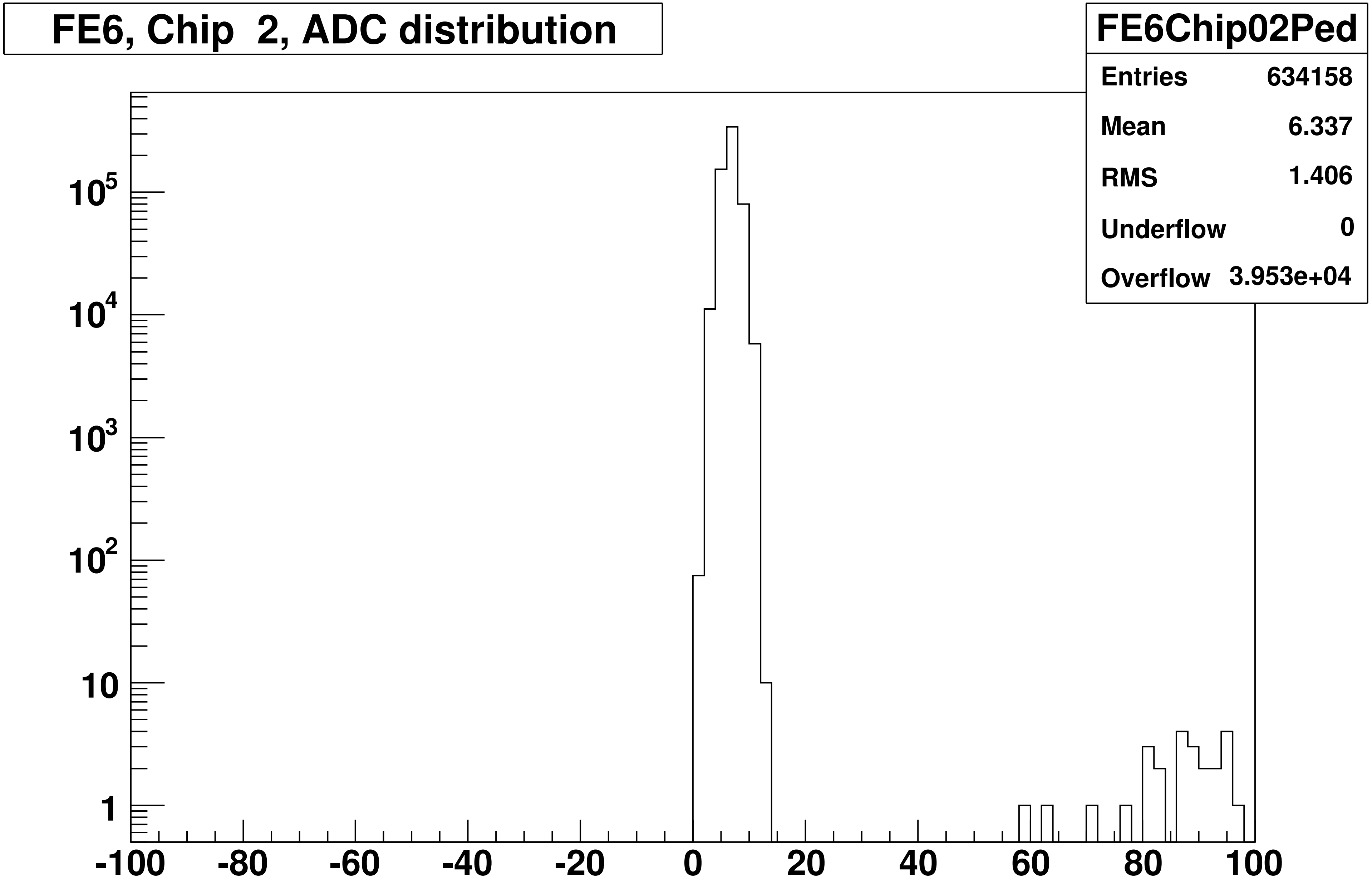
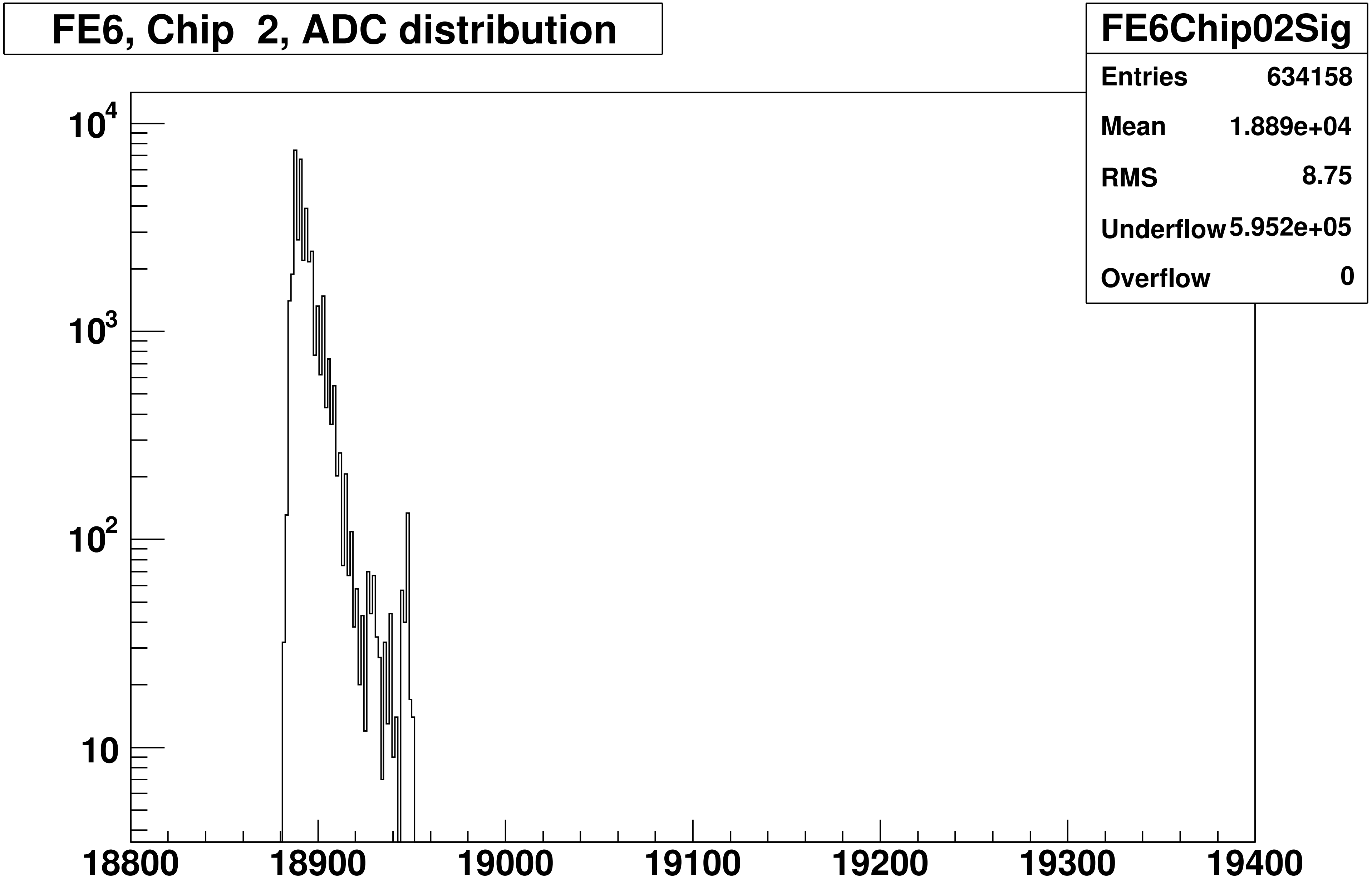
20000
25000



FE6, Chip 2, ADC distribution
FE6Chip02Ped
Entries 634158
Mean 6.337
RMS 1.406
Underflow 0
Overflow 3.953e+04
10^5
10^4
10^3
10^2
10
1
-100 -80 -60 -40 -20 0 20 40 60 80 100


FE6, Chip 2, ADC distribution
FE6Chip02Sig
Entries 634158
Mean 1.889e+04
RMS 8.75
Underflow 5.952e+05
Overflow 0
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10^3
10^2
10
18800
18900
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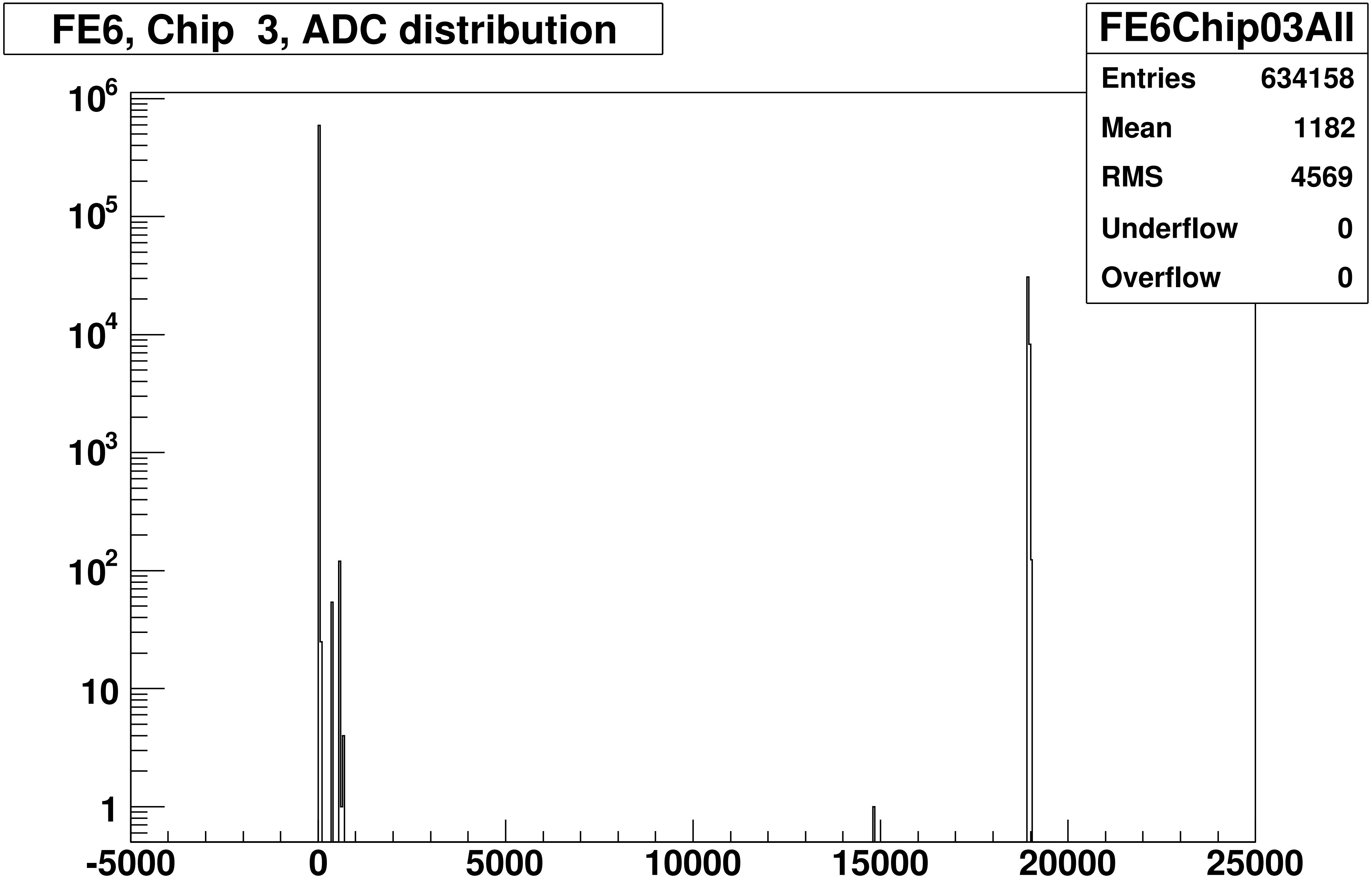
19400


FE6, Chip 3, ADC distribution
FE6Chip03All
Entries 634158
Mean 1182
RMS 4569
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
1
-5000
0
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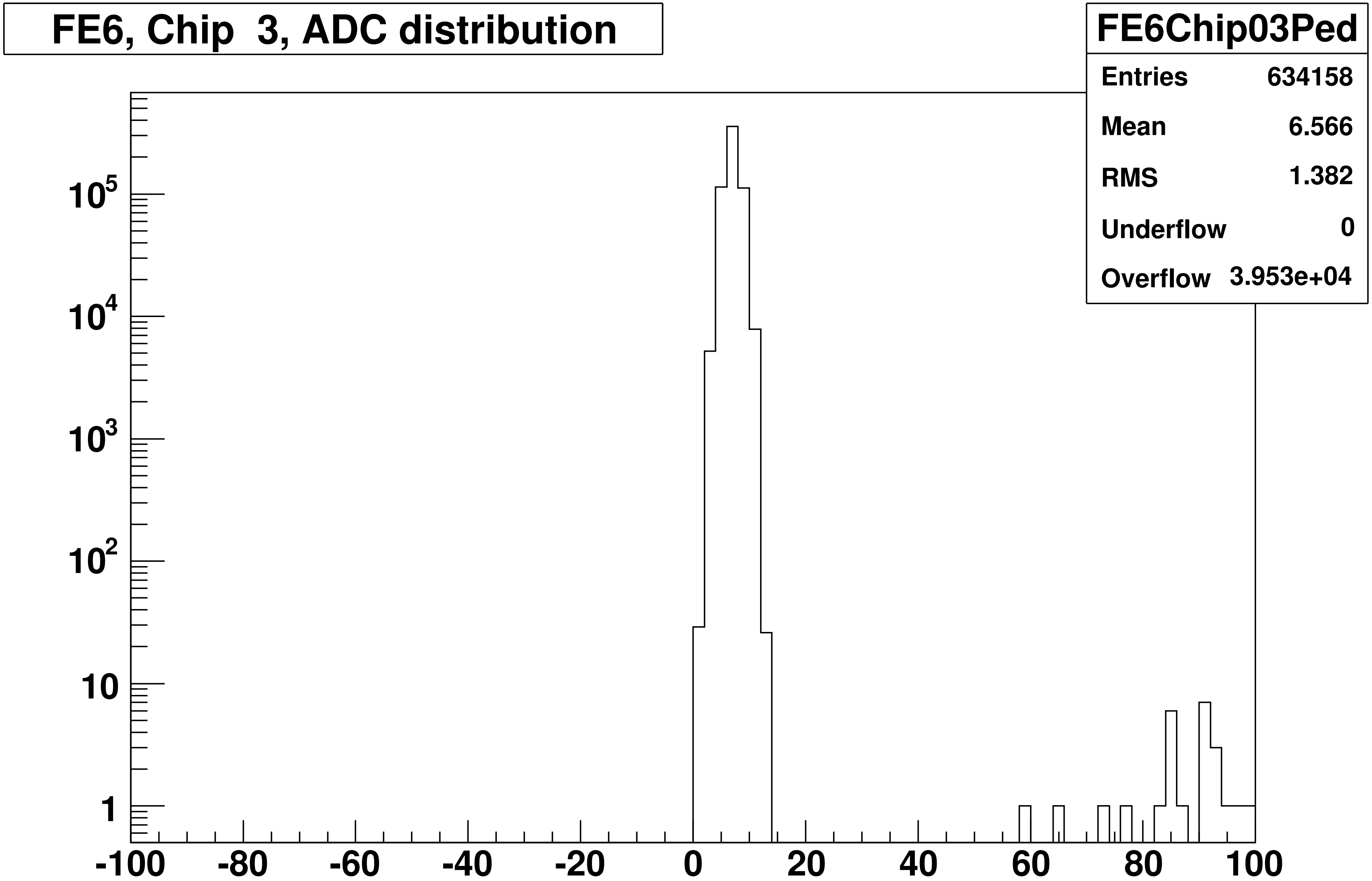
10000
15000
20000
25000


FE6, Chip 3, ADC distribution
FE6Chip03Ped
Entries 634158
Mean 6.566
RMS 1.382
Underflow 0
Overflow 3.953e+04
10^5
10^4
10^3
10^2
10
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-100
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-20
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80
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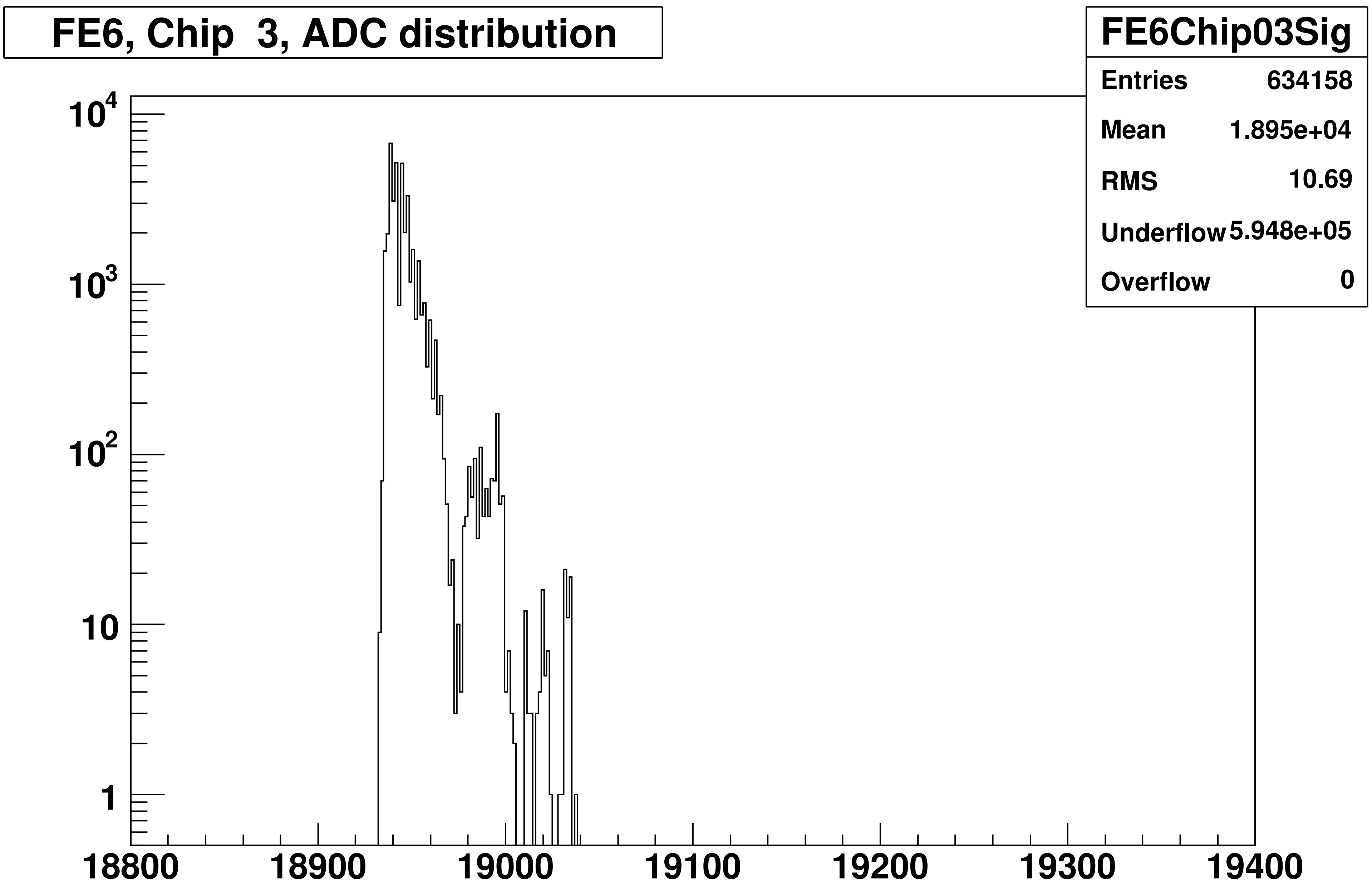

FE6, Chip 3, ADC distribution
FE6Chip03Sig
Entries 634158
Mean 1.895e+04
RMS 10.69
Underflow 5.948e+05
Overflow 0
10^4
10^3
10^2
10
1
18800
18900
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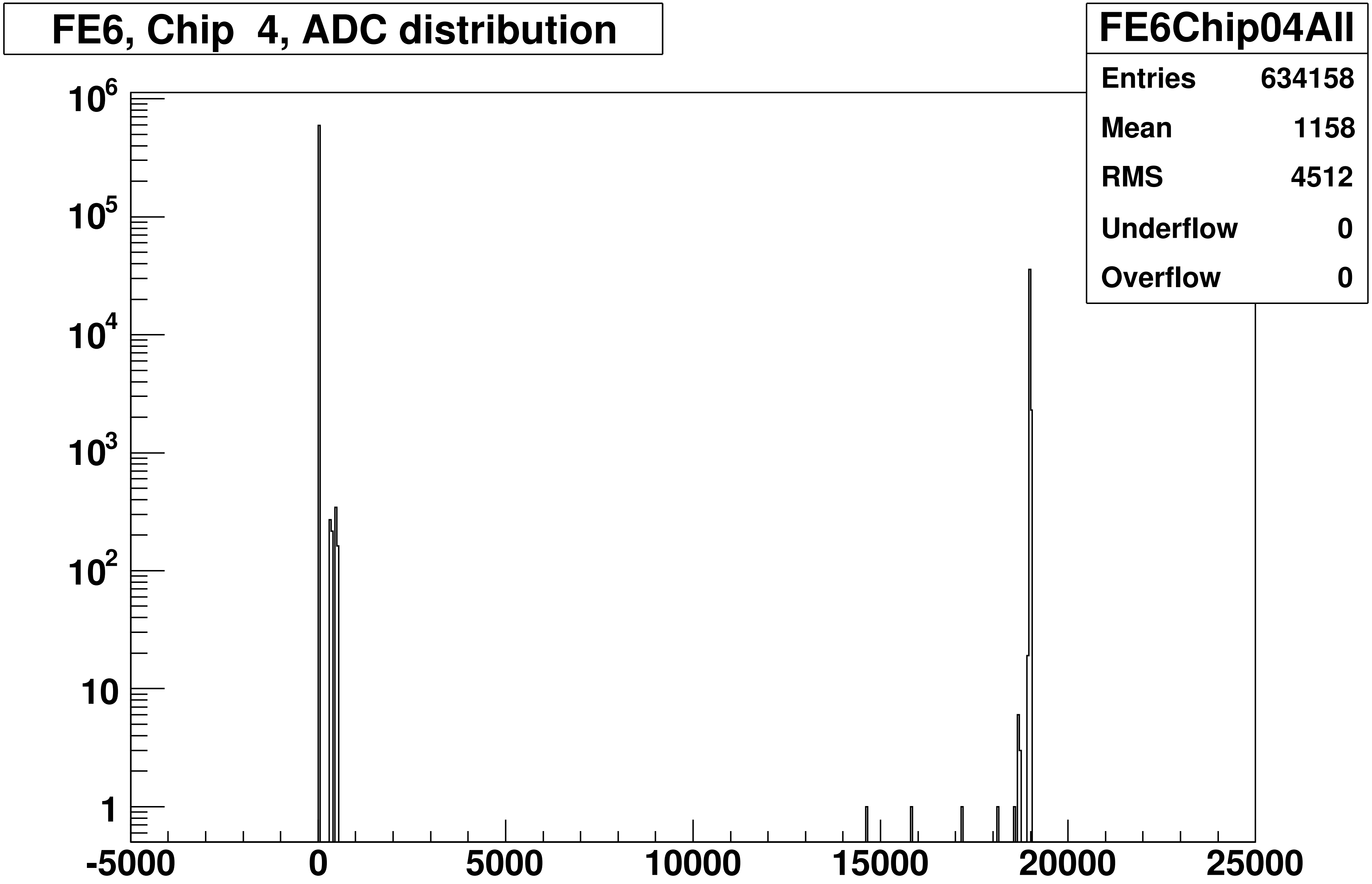
19400


FE6, Chip 4, ADC distribution
FE6Chip04All
Entries 634158
Mean 1158
RMS 4512
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
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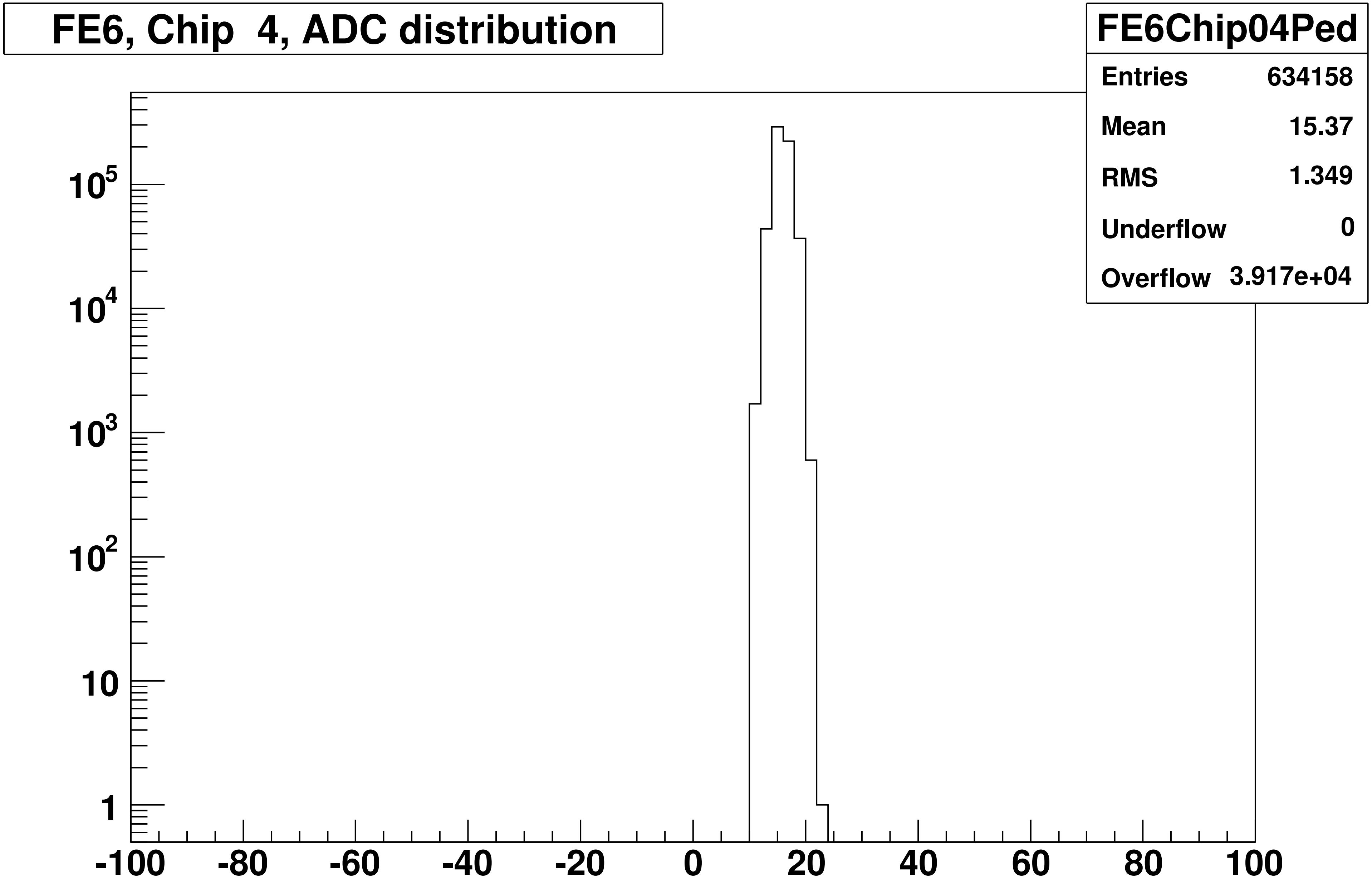
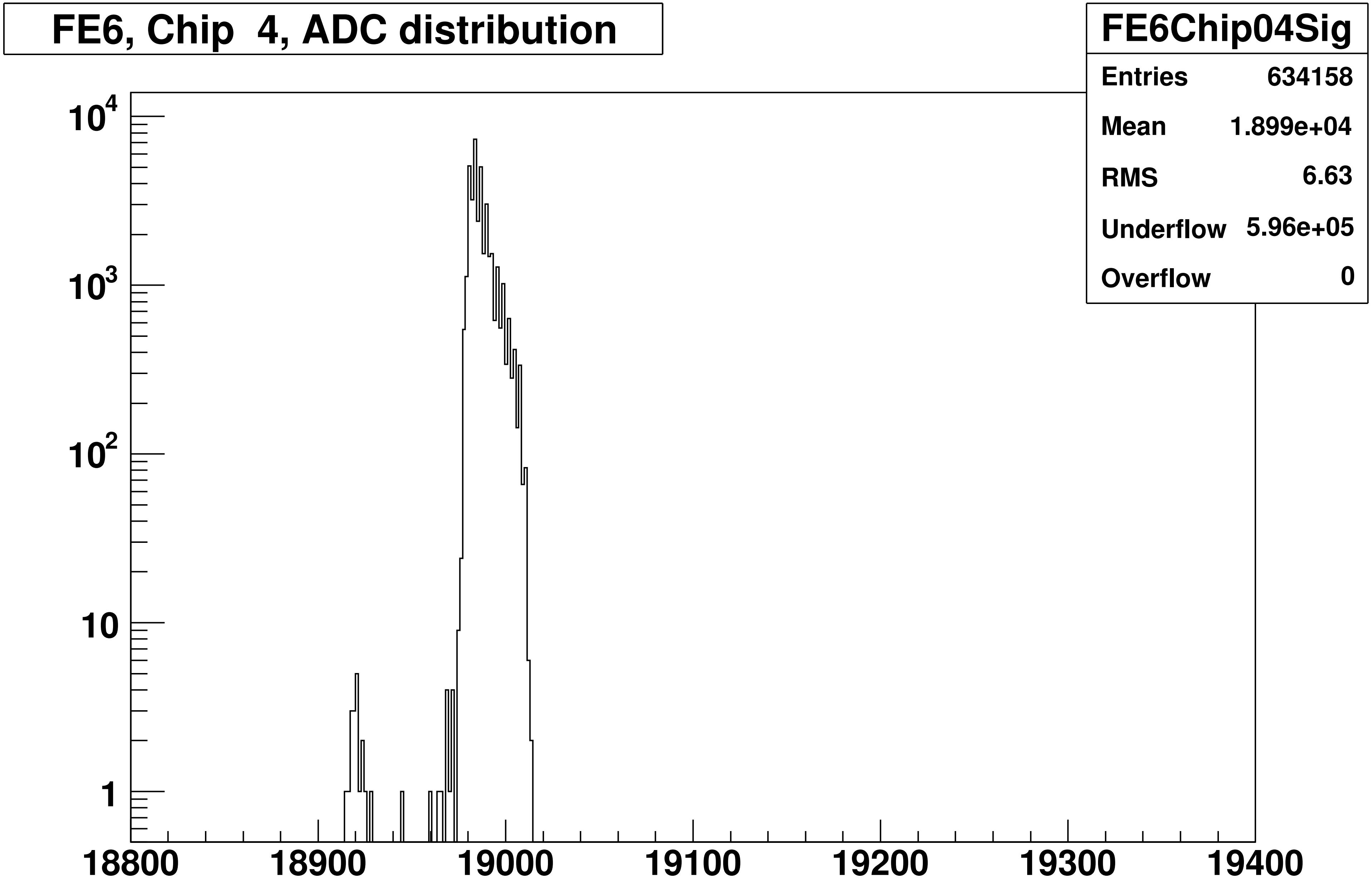
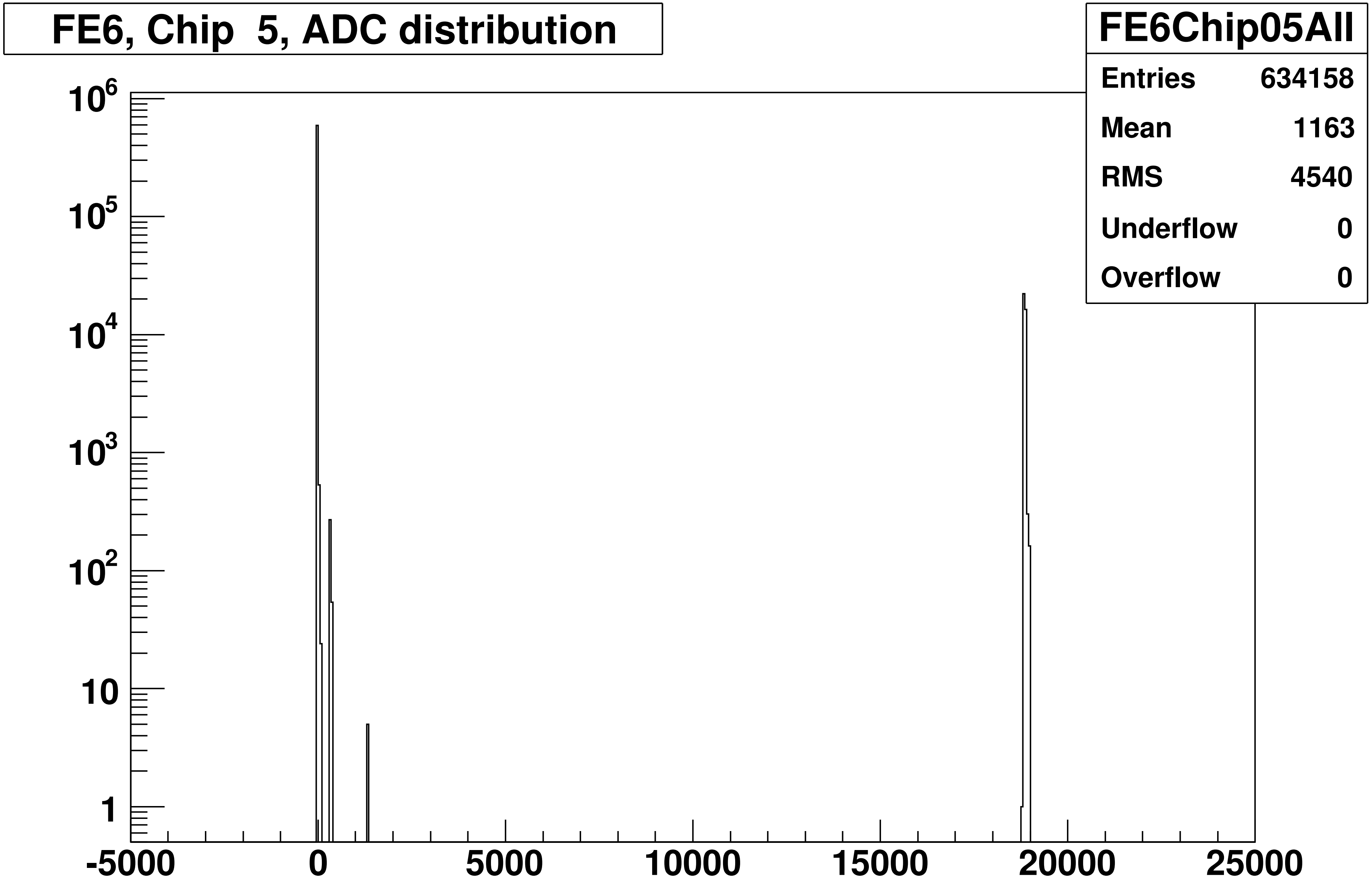

FE6, Chip 4, ADC distribution
FE6Chip04Ped
Entries 634158
Mean 15.37
RMS 1.349
Underflow 0
Overflow 3.917e+04
10^5
10^4
10^3
10^2
10
1
-100 -80 -60 -40 -20 0 20 40 60 80 100


FE6, Chip 4, ADC distribution
FE6Chip04Sig
Entries 634158
Mean 1.899e+04
RMS 6.63
Underflow 5.96e+05
Overflow 0
10^4
10^3
10^2
10
1
18800
18900
19000
19100
19200
19300
19400



FE6, Chip 5, ADC distribution
FE6Chip05All
Entries 634158
Mean 1163
RMS 4540
Underflow 0
Overflow 0
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10^4
10^3
10^2
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-5000
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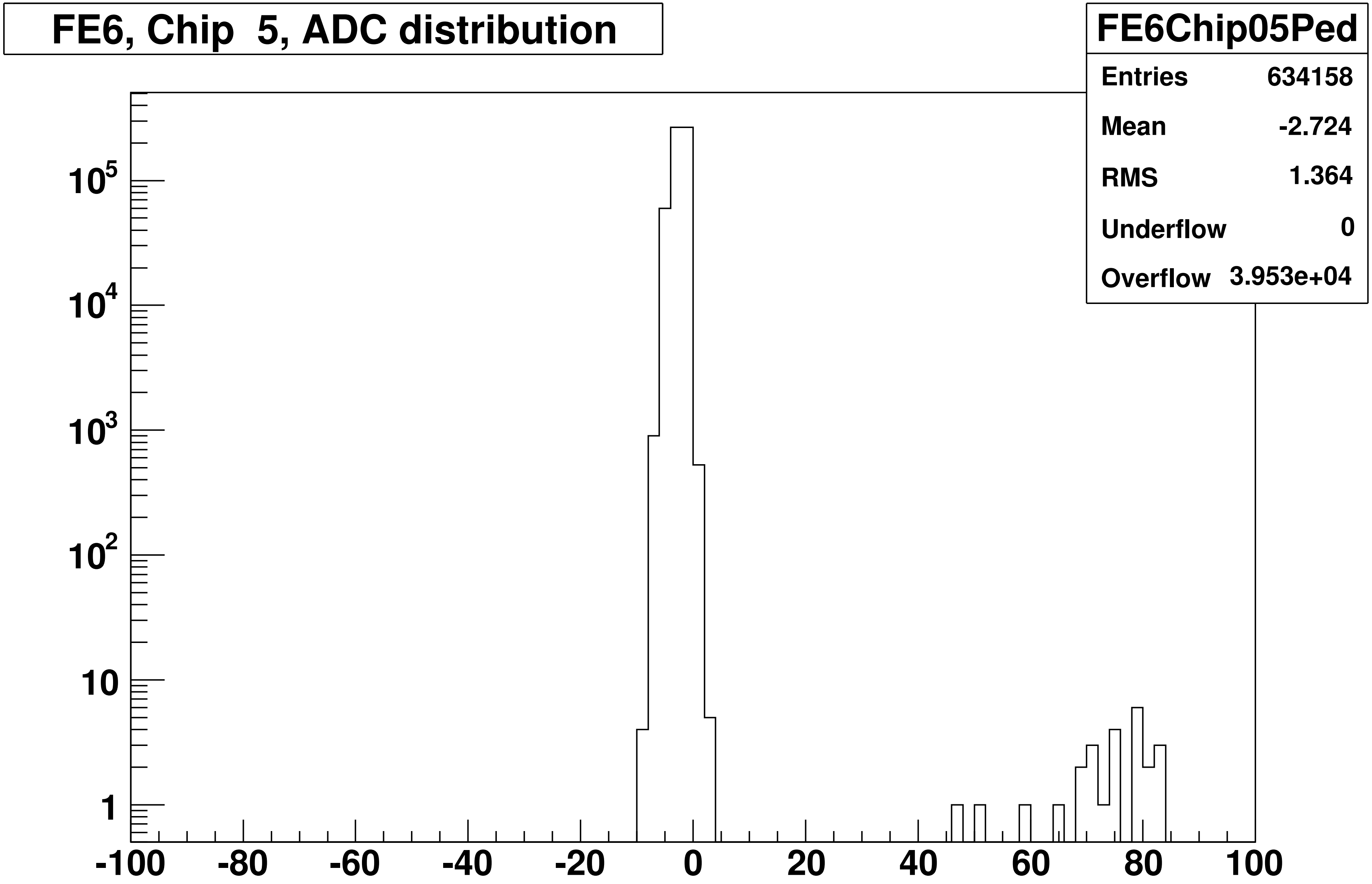

FE6, Chip 5, ADC distribution
FE6Chip05Ped
Entries 634158
Mean -2.724
RMS 1.364
Underflow 0
Overflow 3.953e+04
10^5
10^4
10^3
10^2
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1
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-20
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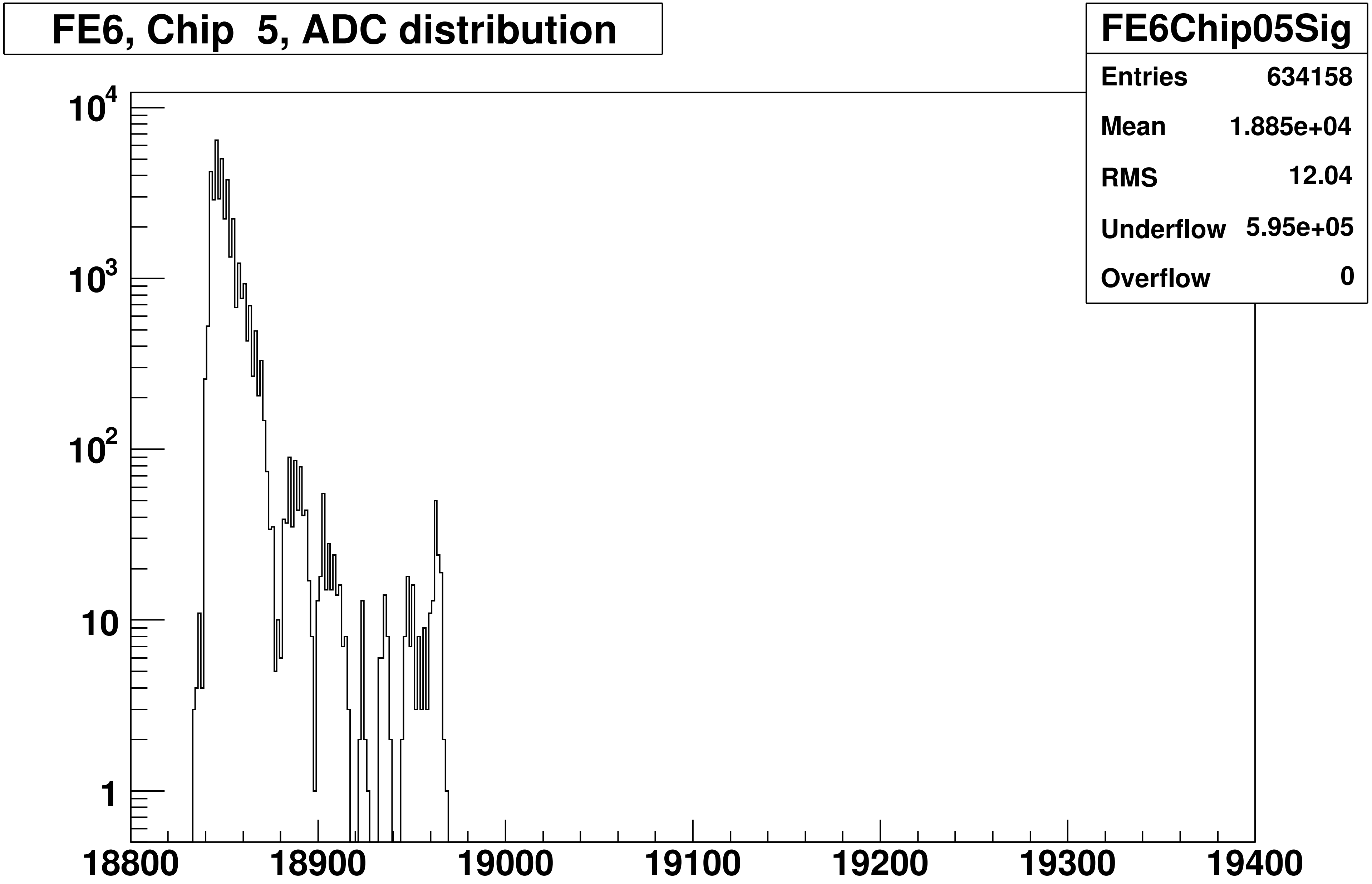
FE6, Chip 5, ADC distribution
FE6Chip05Sig
Entries 634158
Mean 1.885e+04
RMS 12.04
Underflow 5.95e+05
Overflow 0
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10^3
10^2
10
1
18800
18900
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19200
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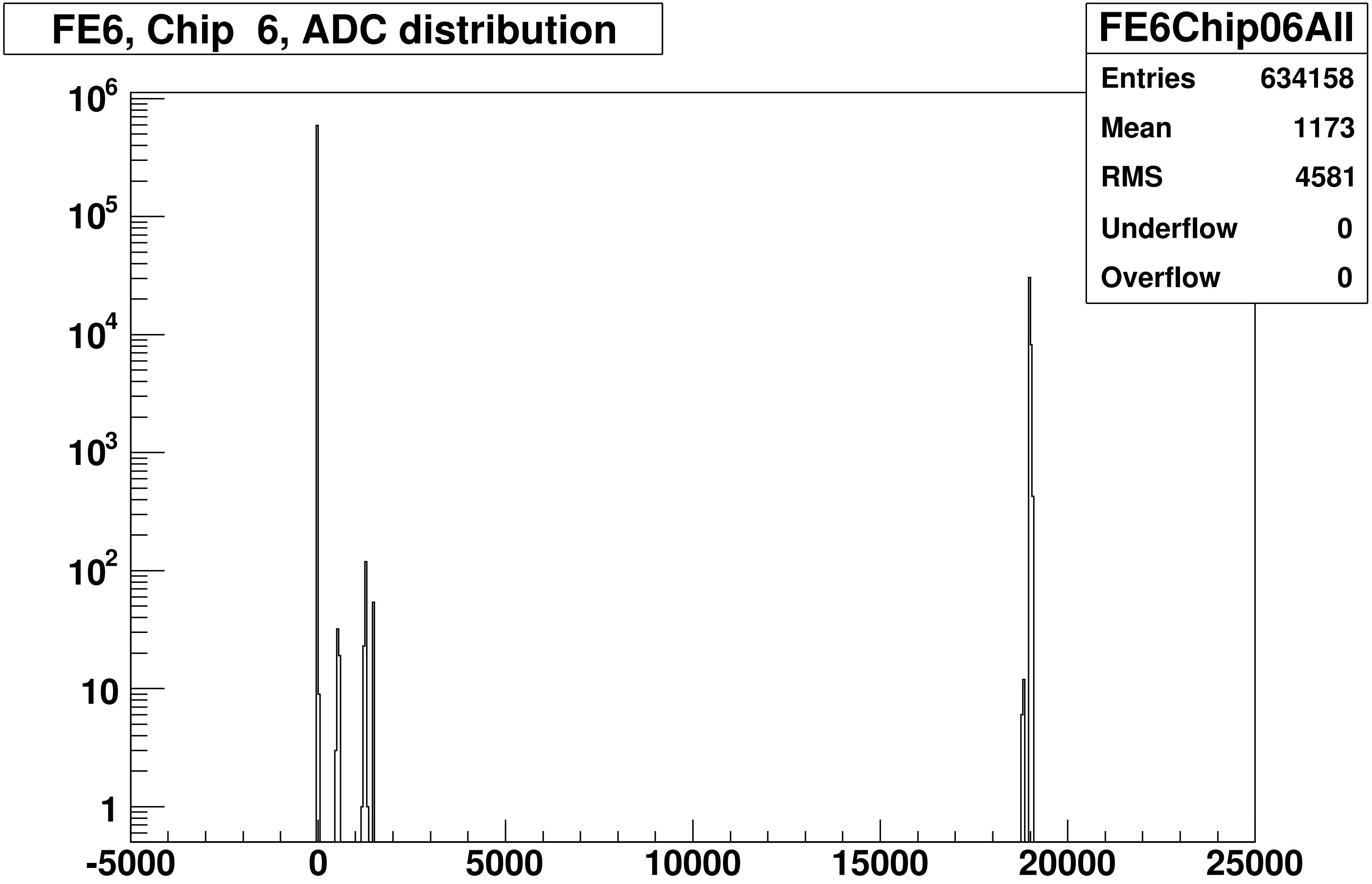
19400


FE6, Chip 6, ADC distribution
FE6Chip06All
Entries 634158
Mean 1173
RMS 4581
Underflow 0
Overflow 0
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10^4
10^3
10^2
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1
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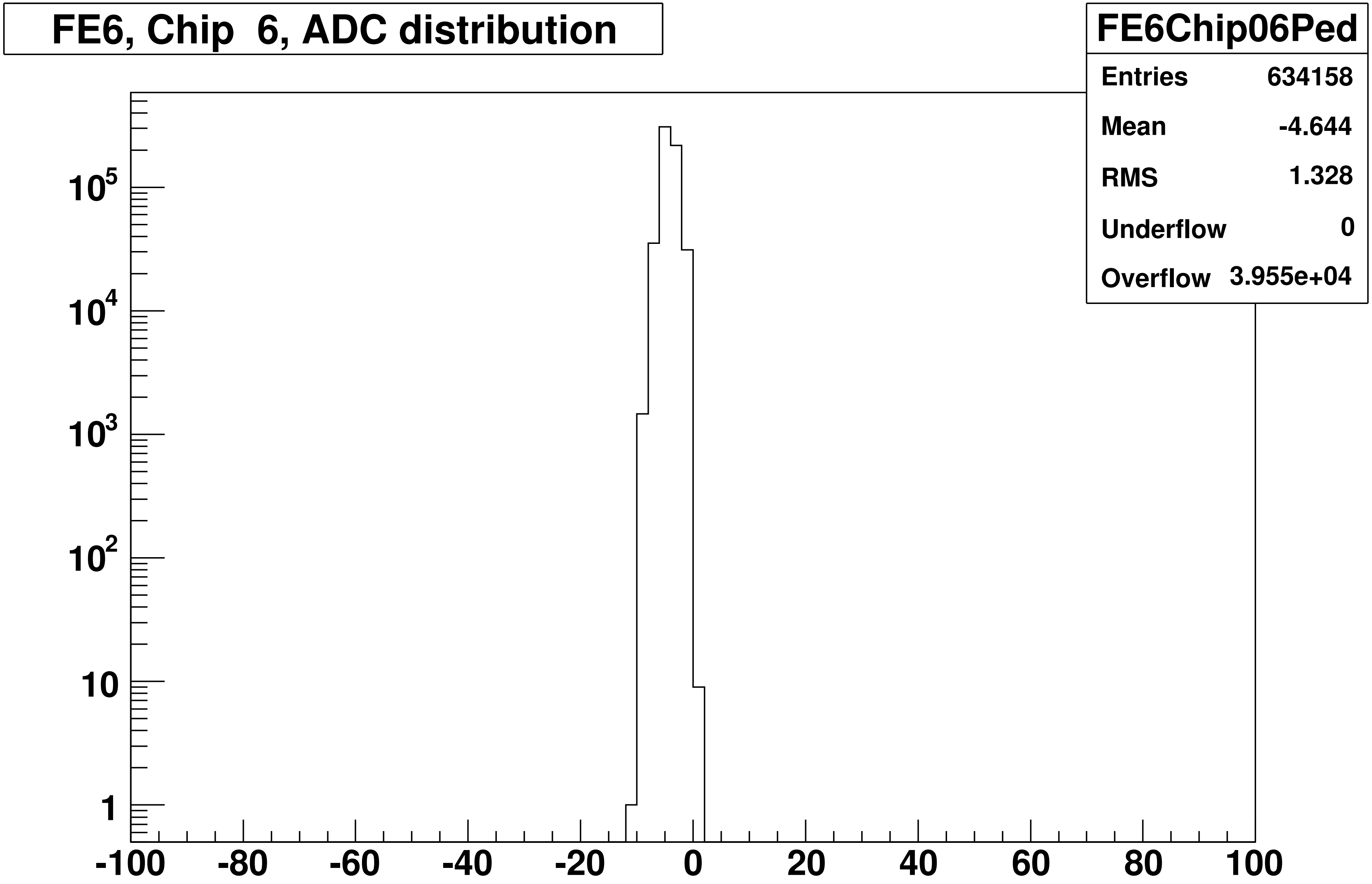
FE6, Chip 6, ADC distribution
FE6Chip06Ped
Entries 634158
Mean -4.644
RMS 1.328
Underflow 0
Overflow 3.955e+04
10^5
10^4
10^3
10^2
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-20
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80
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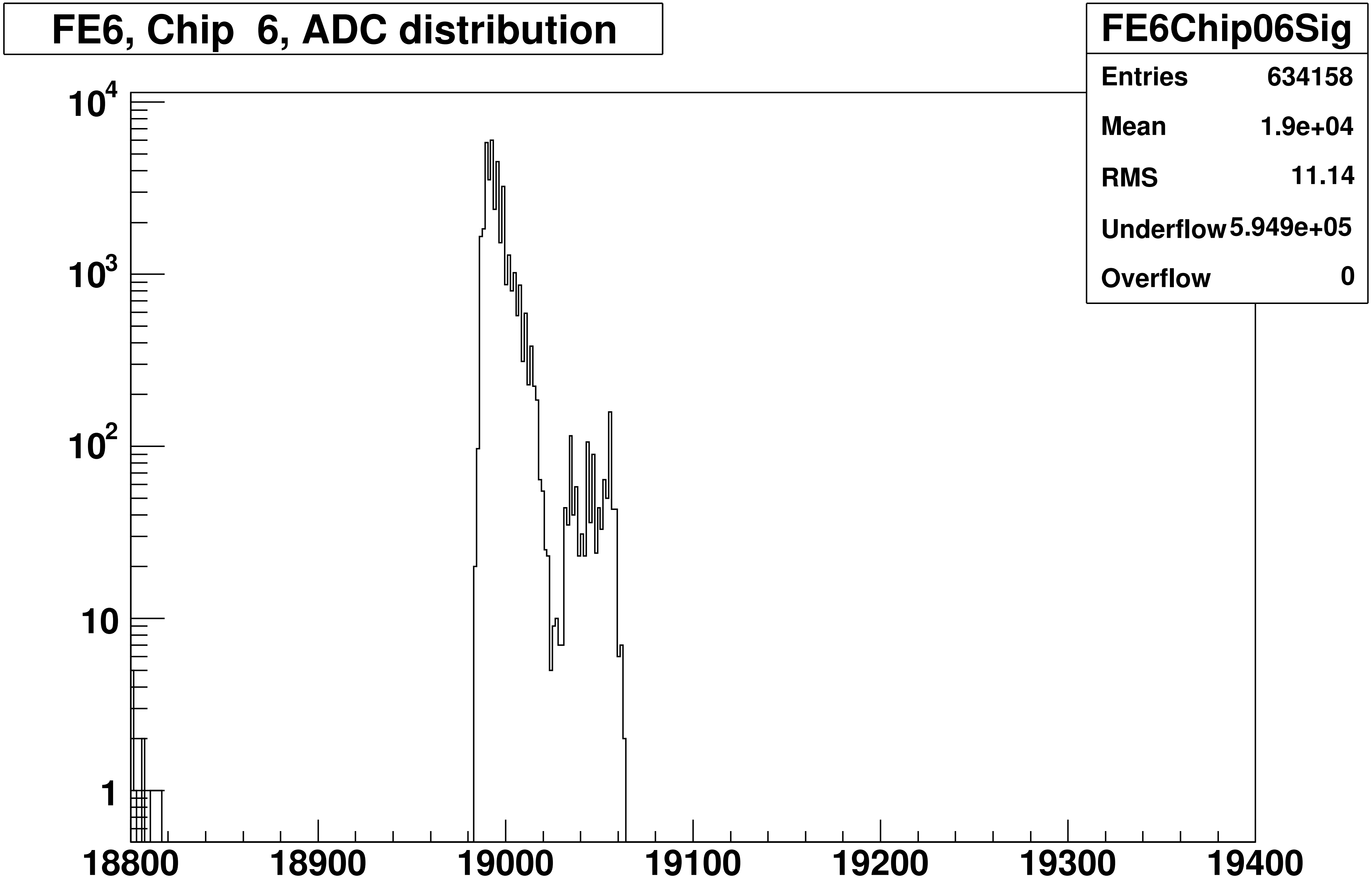

FE6, Chip 6, ADC distribution
FE6Chip06Sig
Entries 634158
Mean 1.9e+04
RMS 11.14
Underflow 5.949e+05
Overflow 0
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10^3
10^2
10
1
18800
18900
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19100
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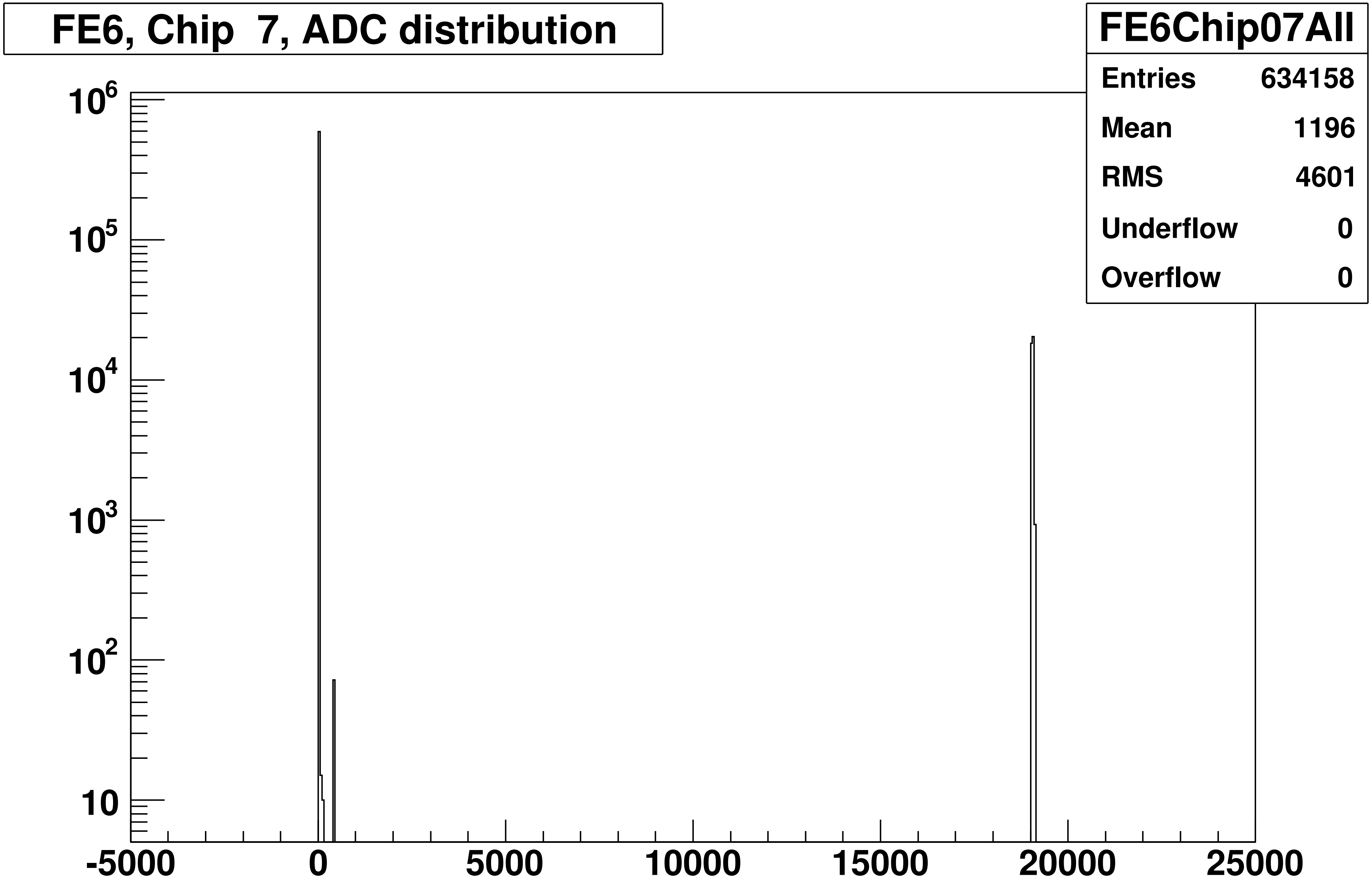
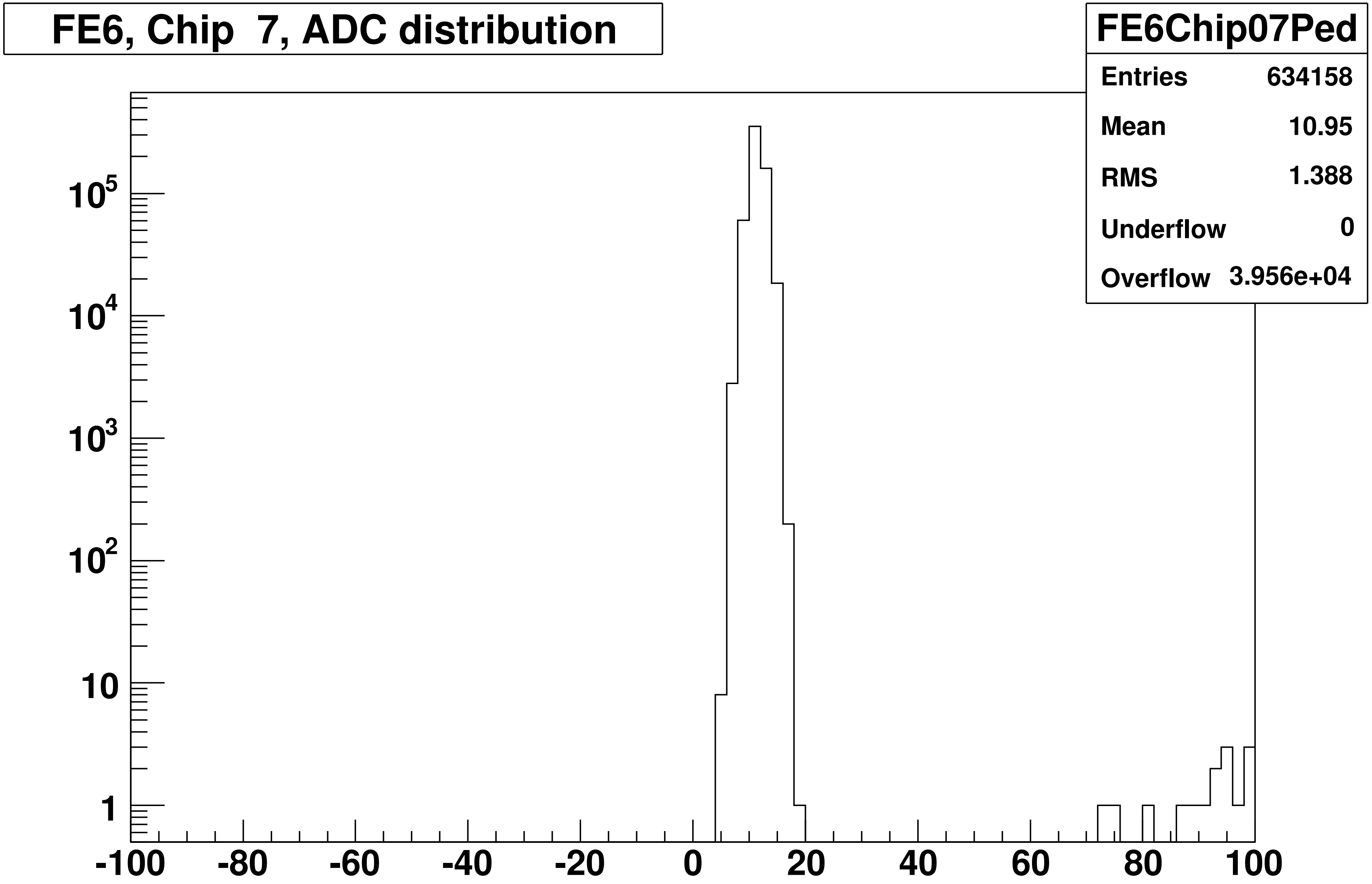
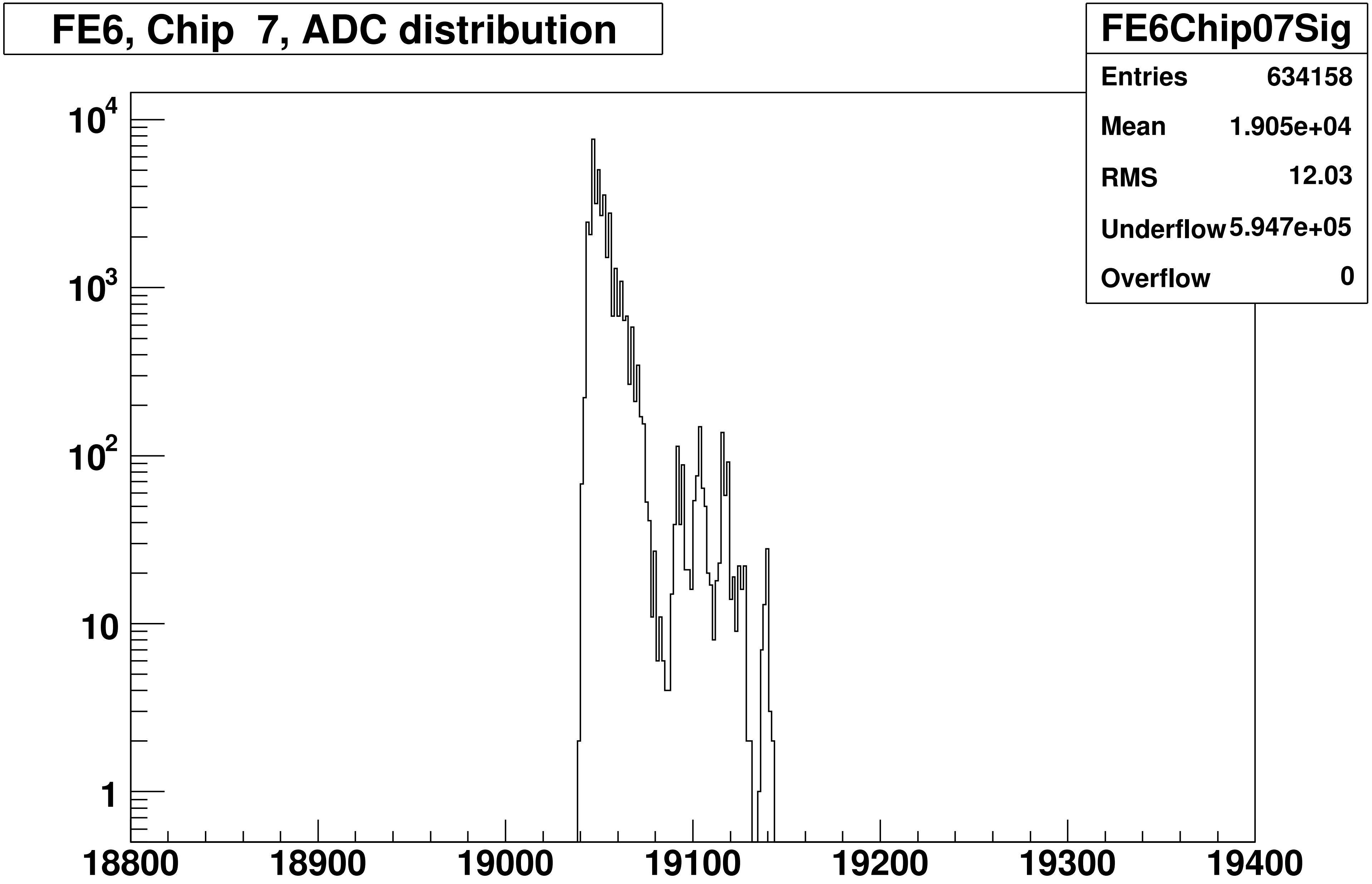
19400


FE6, Chip 7, ADC distribution
FE6Chip07All
Entries 634158
Mean 1196
RMS 4601
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE6, Chip 7, ADC distribution
FE6Chip07Ped
Entries 634158
Mean 10.95
RMS 1.388
Underflow 0
Overflow 3.956e+04
10^5
10^4
10^3
10^2
10
1
-100 -80 -60 -40 -20 0 20 40 60 80 100


FE6, Chip 7, ADC distribution
FE6Chip07Sig
Entries 634158
Mean 1.905e+04
RMS 12.03
Underflow 5.947e+05
Overflow 0
10^4
10^3
10^2
10
1
18800
18900
19000
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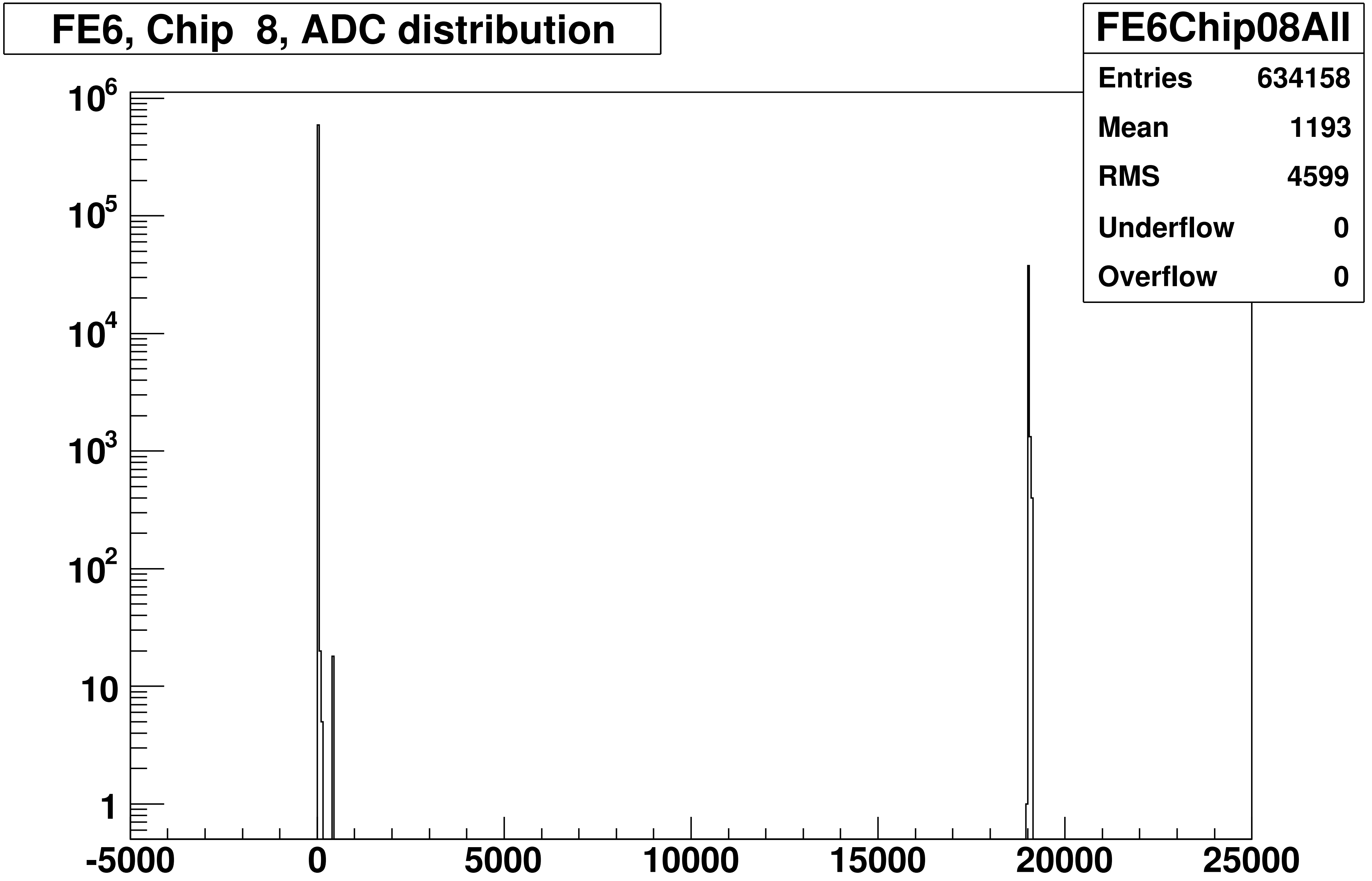

FE6, Chip 8, ADC distribution
FE6Chip08All
Entries 634158
Mean 1193
RMS 4599
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
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0
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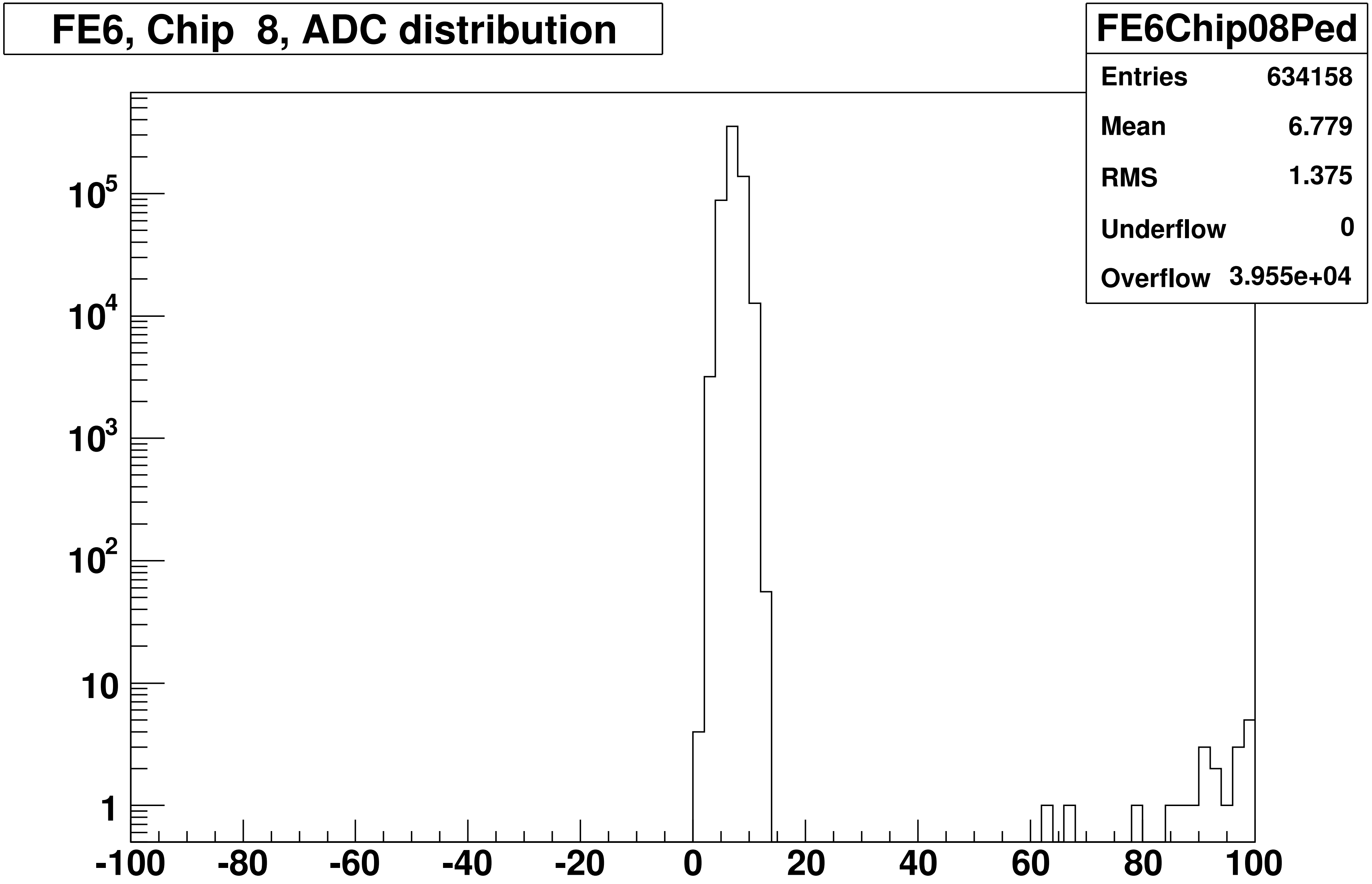
25000


FE6, Chip 8, ADC distribution
FE6Chip08Ped
Entries 634158
Mean 6.779
RMS 1.375
Underflow 0
Overflow 3.955e+04
10^5
10^4
10^3
10^2
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80
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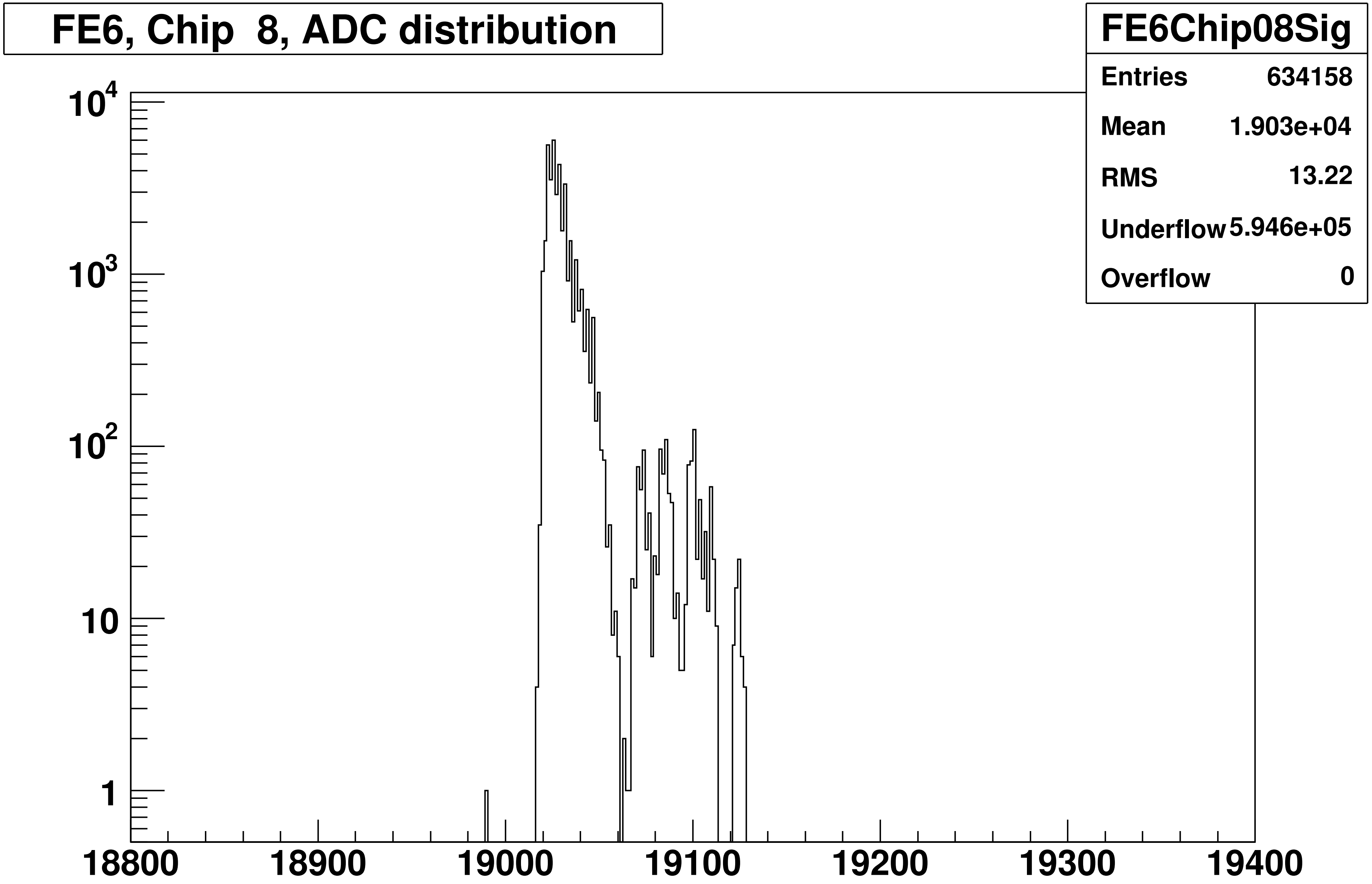
FE6, Chip 8, ADC distribution
FE6Chip08Sig
Entries 634158
Mean 1.903e+04
RMS 13.22
Underflow 5.946e+05
Overflow 0
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10^3
10^2
10
1
18800
18900
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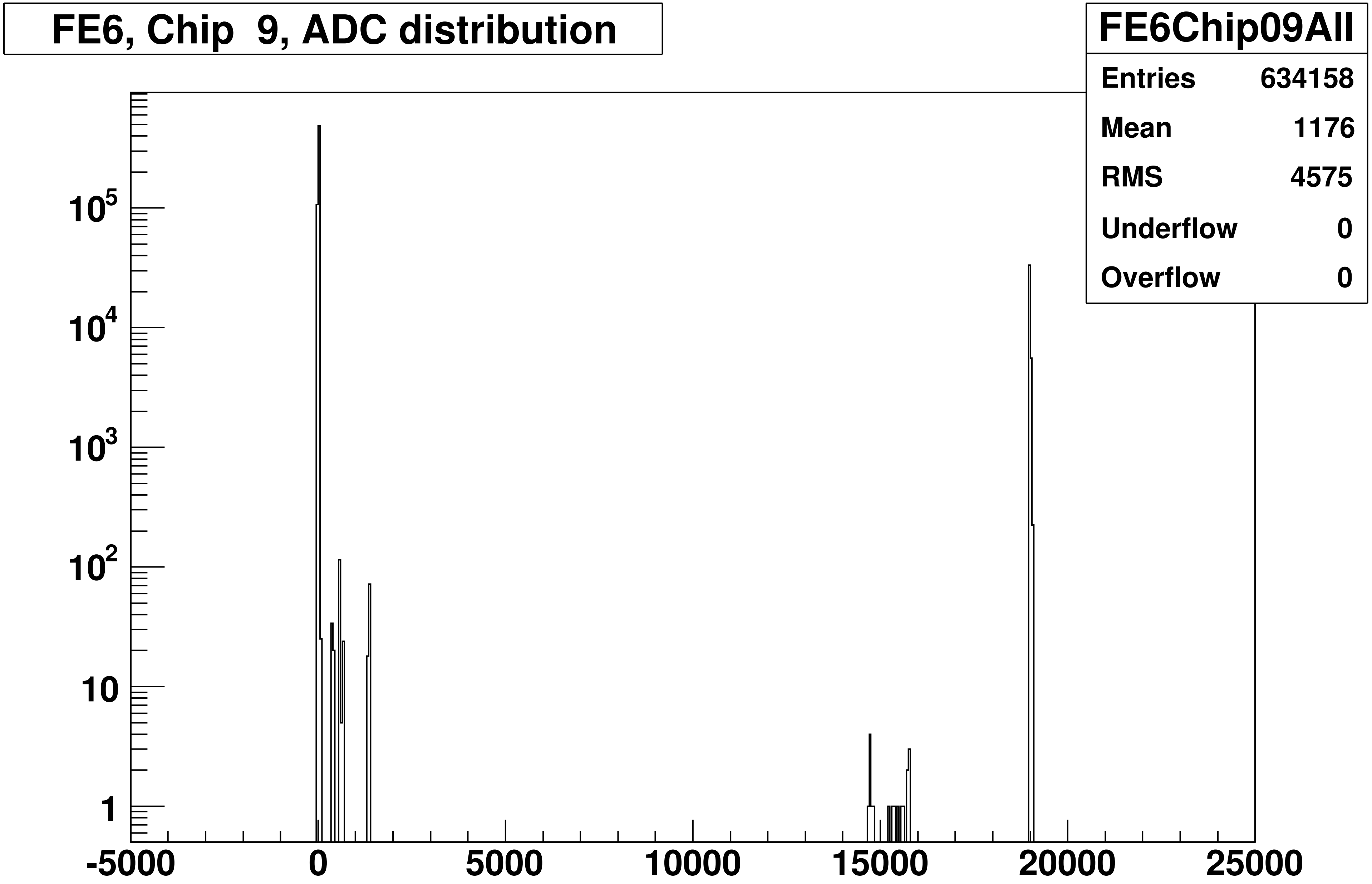

FE6, Chip 9, ADC distribution
FE6Chip09All
Entries 634158
Mean 1176
RMS 4575
Underflow 0
Overflow 0
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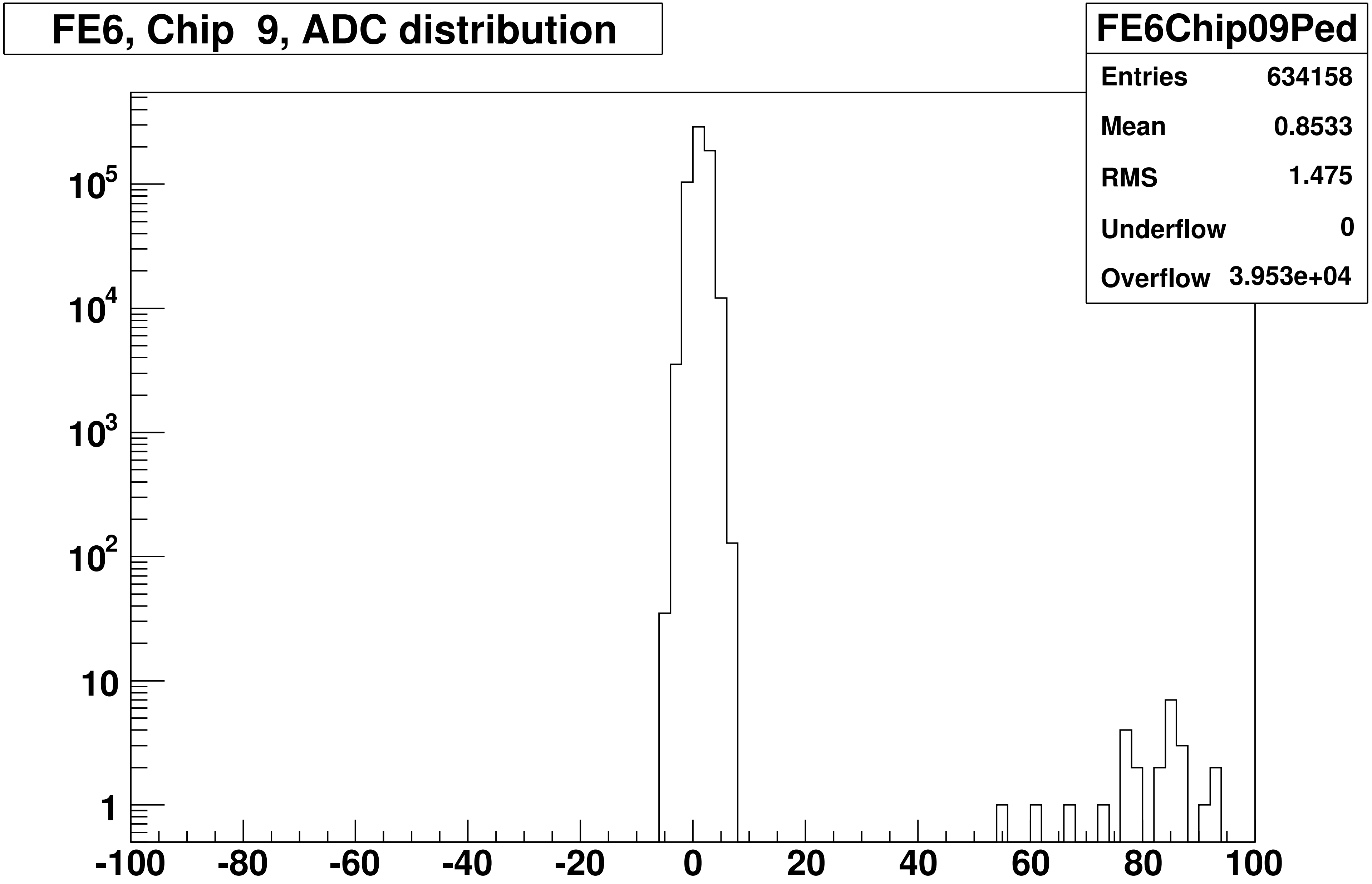
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE6, Chip 9, ADC distribution
FE6Chip09Ped
Entries 634158
Mean 0.8533
RMS 1.475
Underflow 0
Overflow 3.953e+04
10^5
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80
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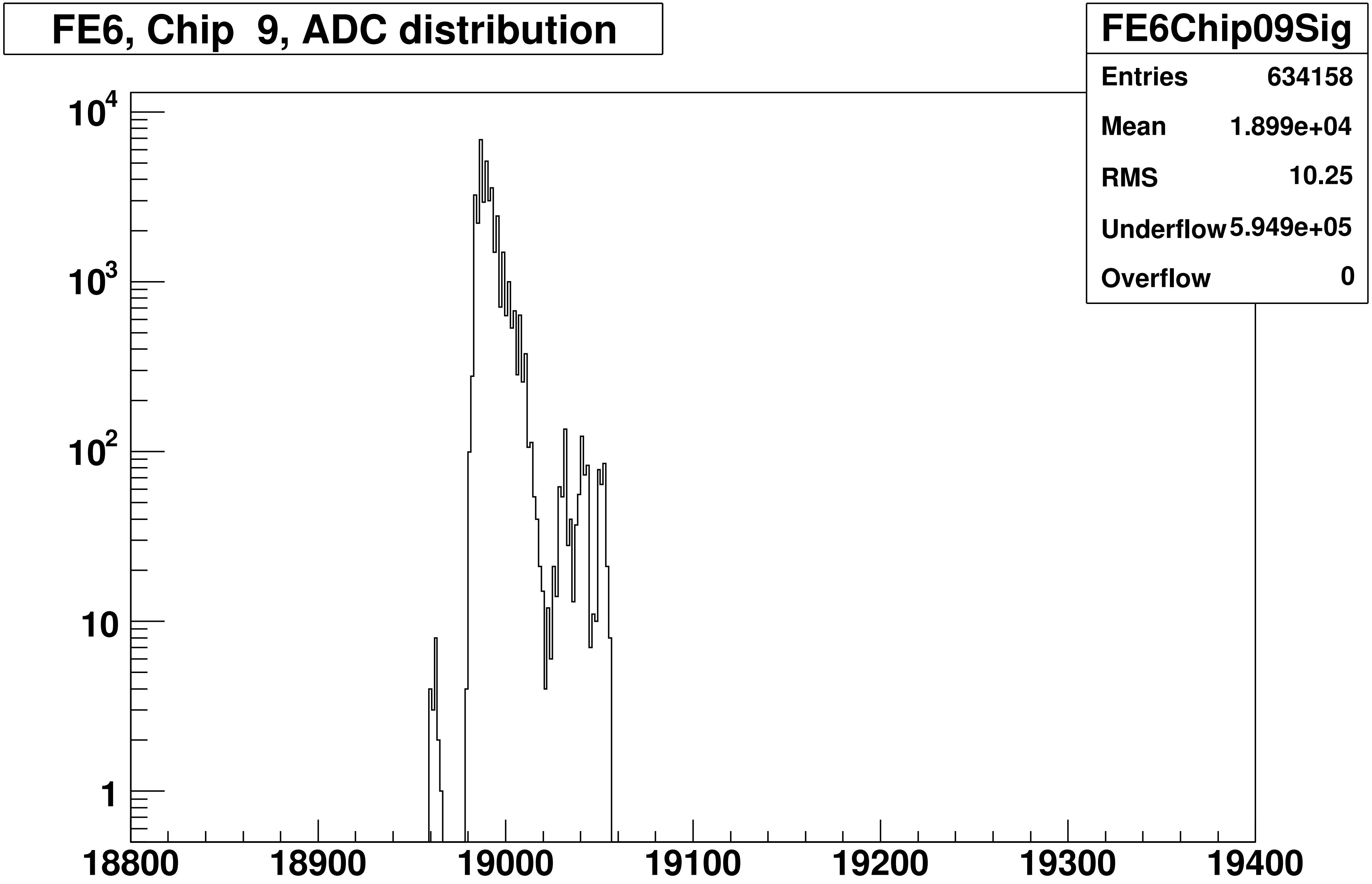
FE6, Chip 9, ADC distribution
FE6Chip09Sig
Entries 634158
Mean 1.899e+04
RMS 10.25
Underflow 5.949e+05
Overflow 0
10^4
10^3
10^2
10
1
18800
18900
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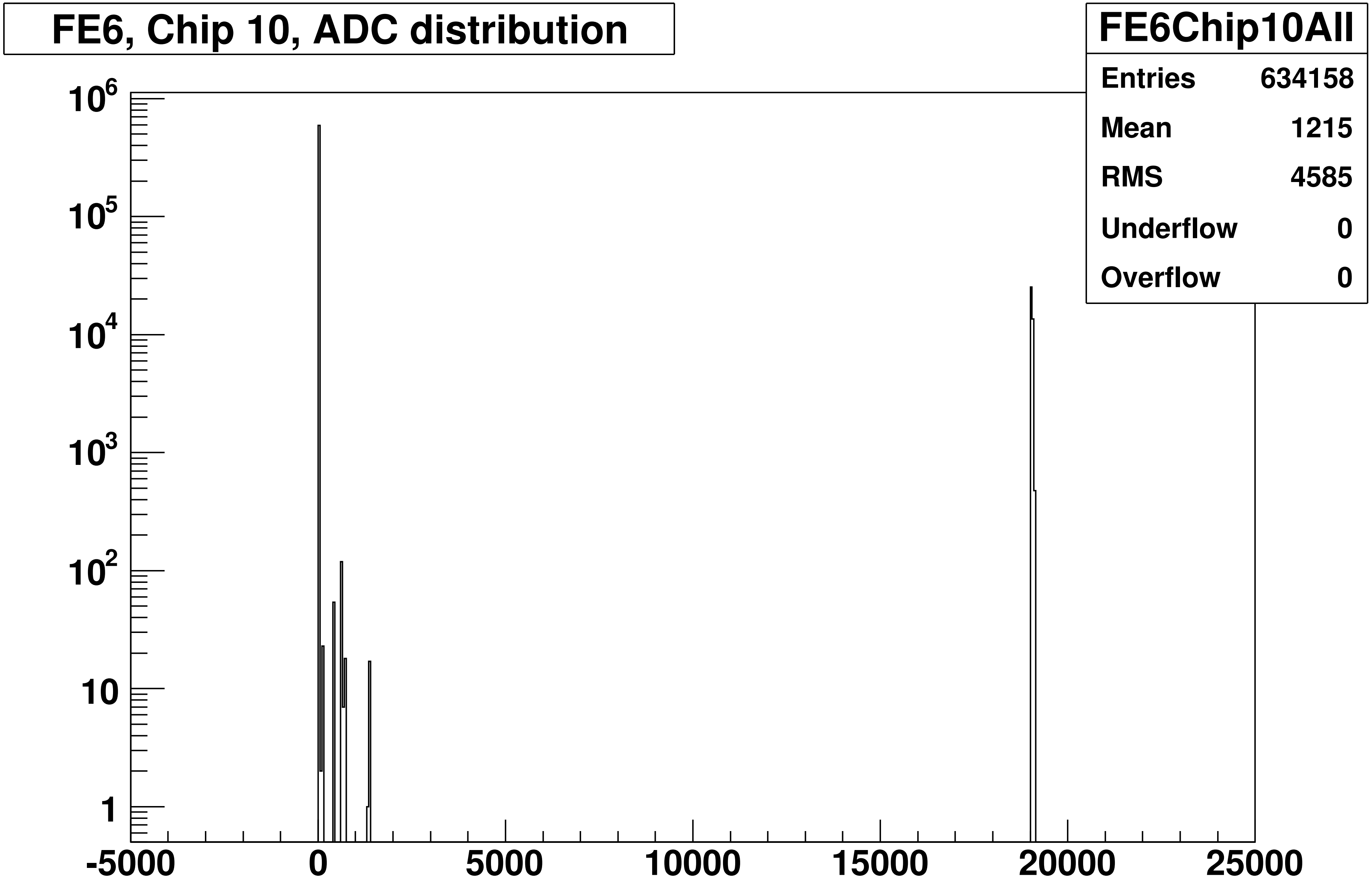
FE6, Chip 10, ADC distribution
FE6Chip10All
Entries 634158
Mean 1215
RMS 4585
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
1
-5000
0
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20000
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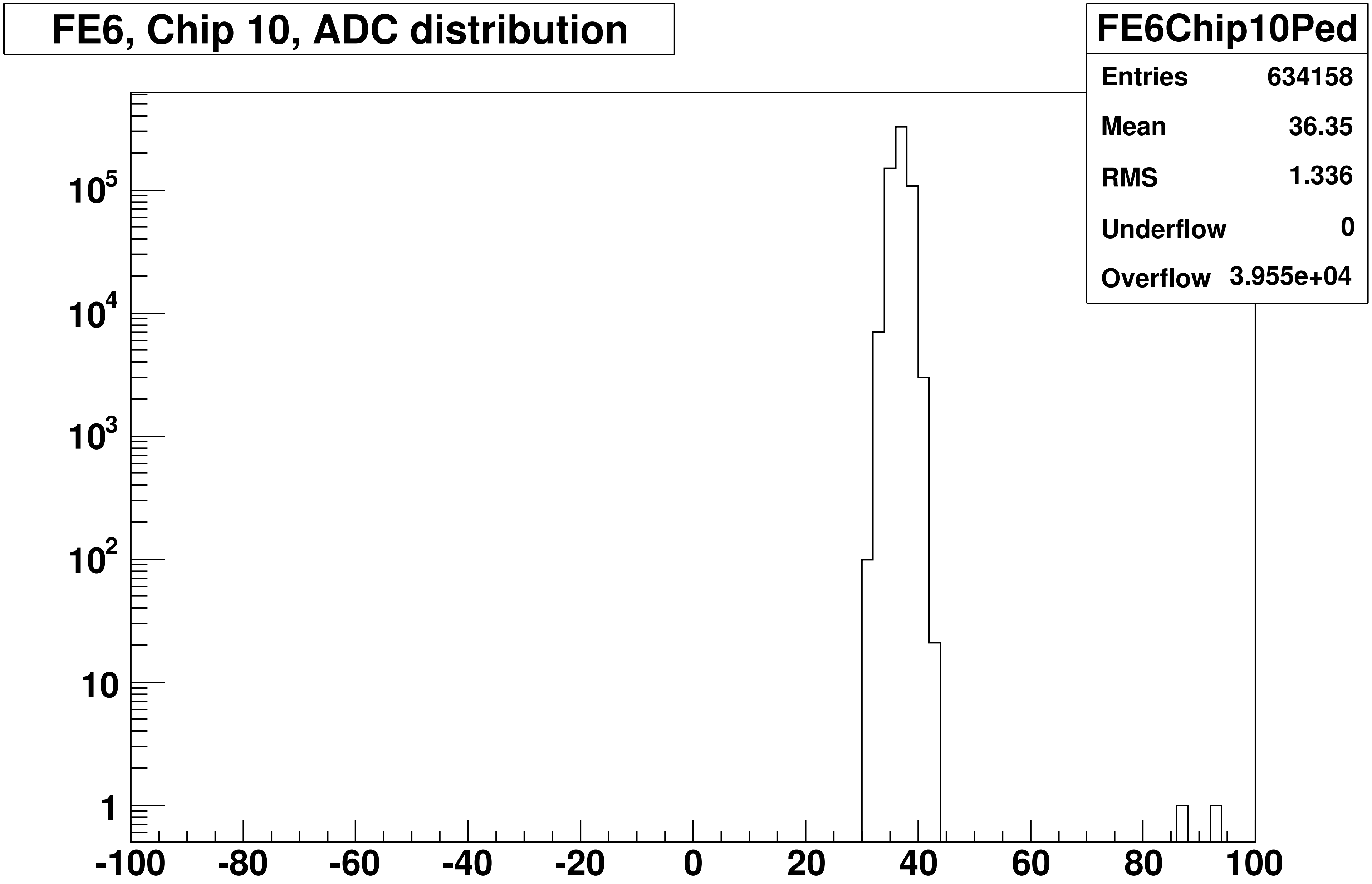
FE6, Chip 10, ADC distribution
FE6Chip10Ped
Entries 634158
Mean 36.35
RMS 1.336
Underflow 0
Overflow 3.955e+04
10^5
10^4
10^3
10^2
10
1
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-40
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80
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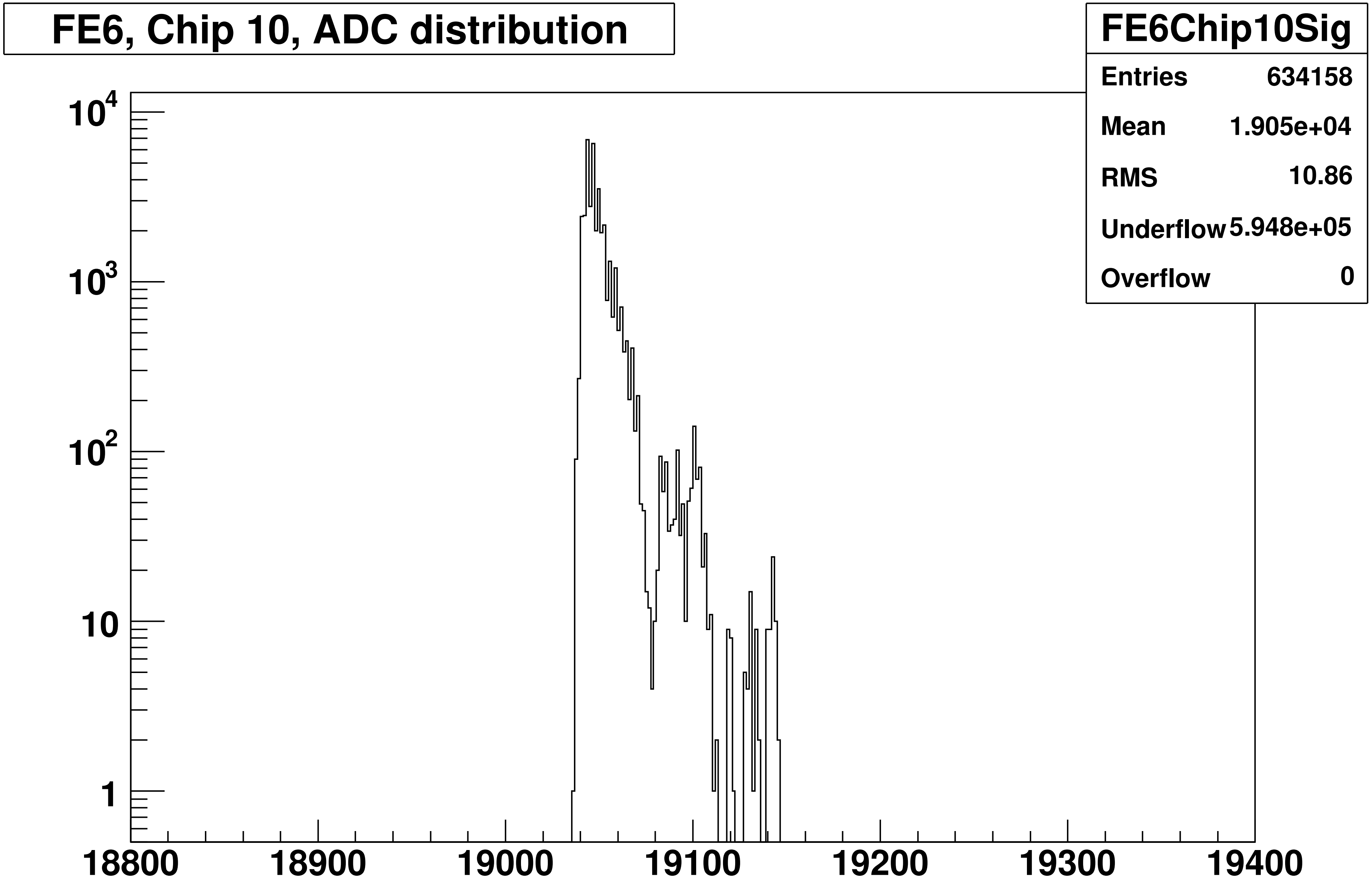

FE6, Chip 10, ADC distribution
FE6Chip10Sig
Entries 634158
Mean 1.905e+04
RMS 10.86
Underflow 5.948e+05
Overflow 0
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10^3
10^2
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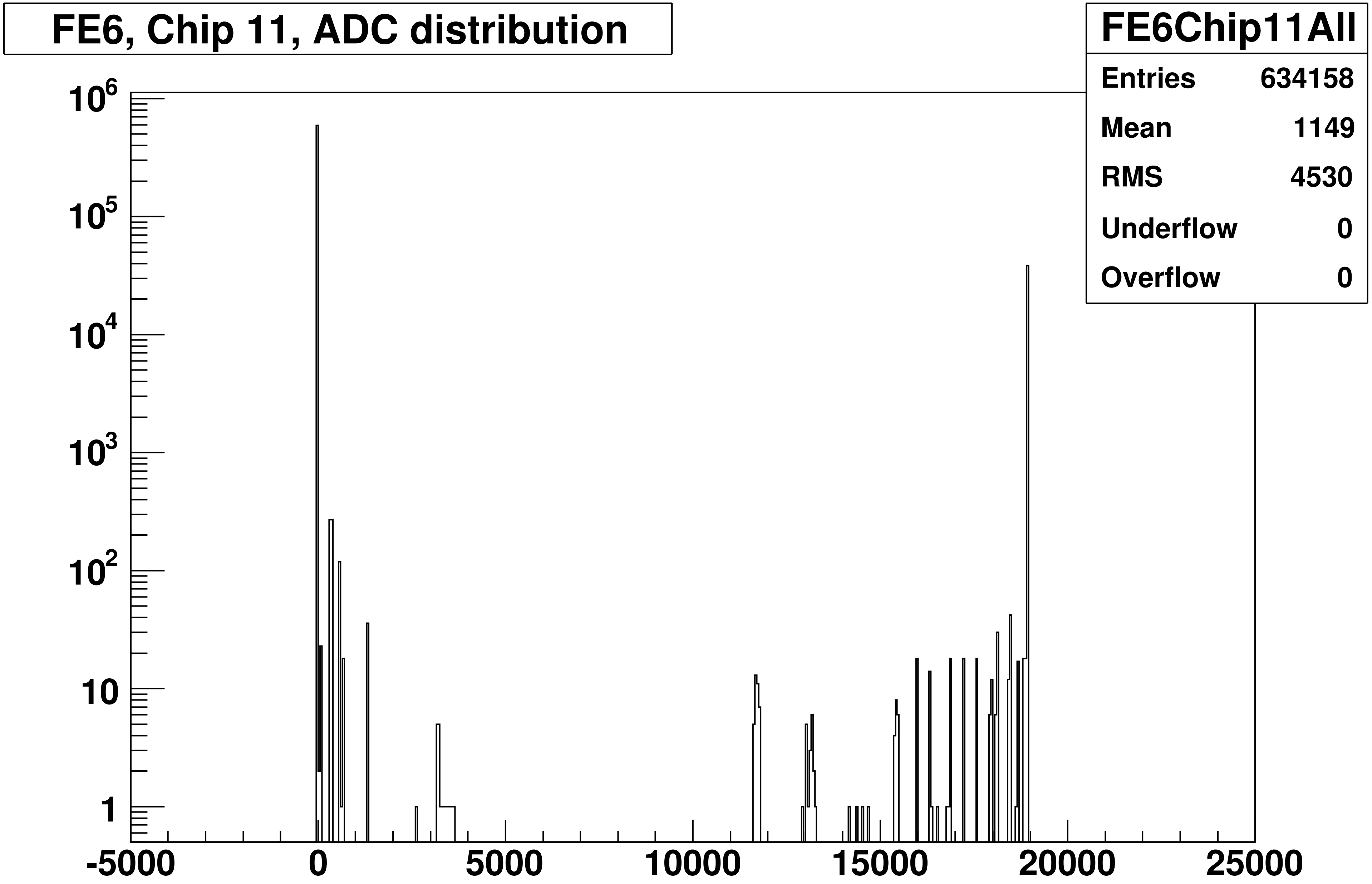
19400



FE6, Chip 11, ADC distribution
FE6Chip11All
Entries 634158
Mean 1149
RMS 4530
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
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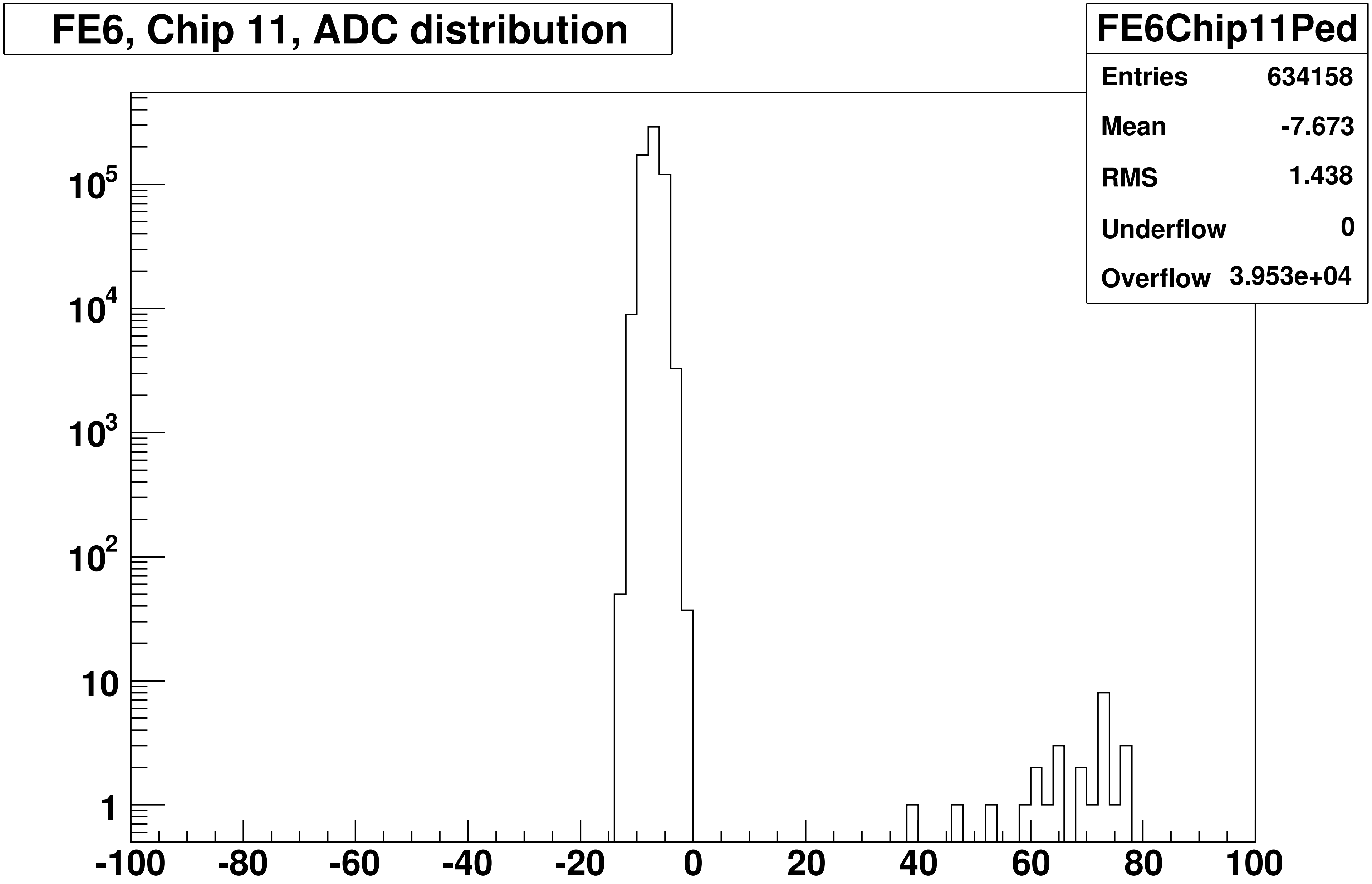
20000
25000



FE6, Chip 11, ADC distribution
FE6Chip11Ped
Entries 634158
Mean -7.673
RMS 1.438
Underflow 0
Overflow 3.953e+04
10^5
10^4
10^3
10^2
10
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-100
-80
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-40
-20
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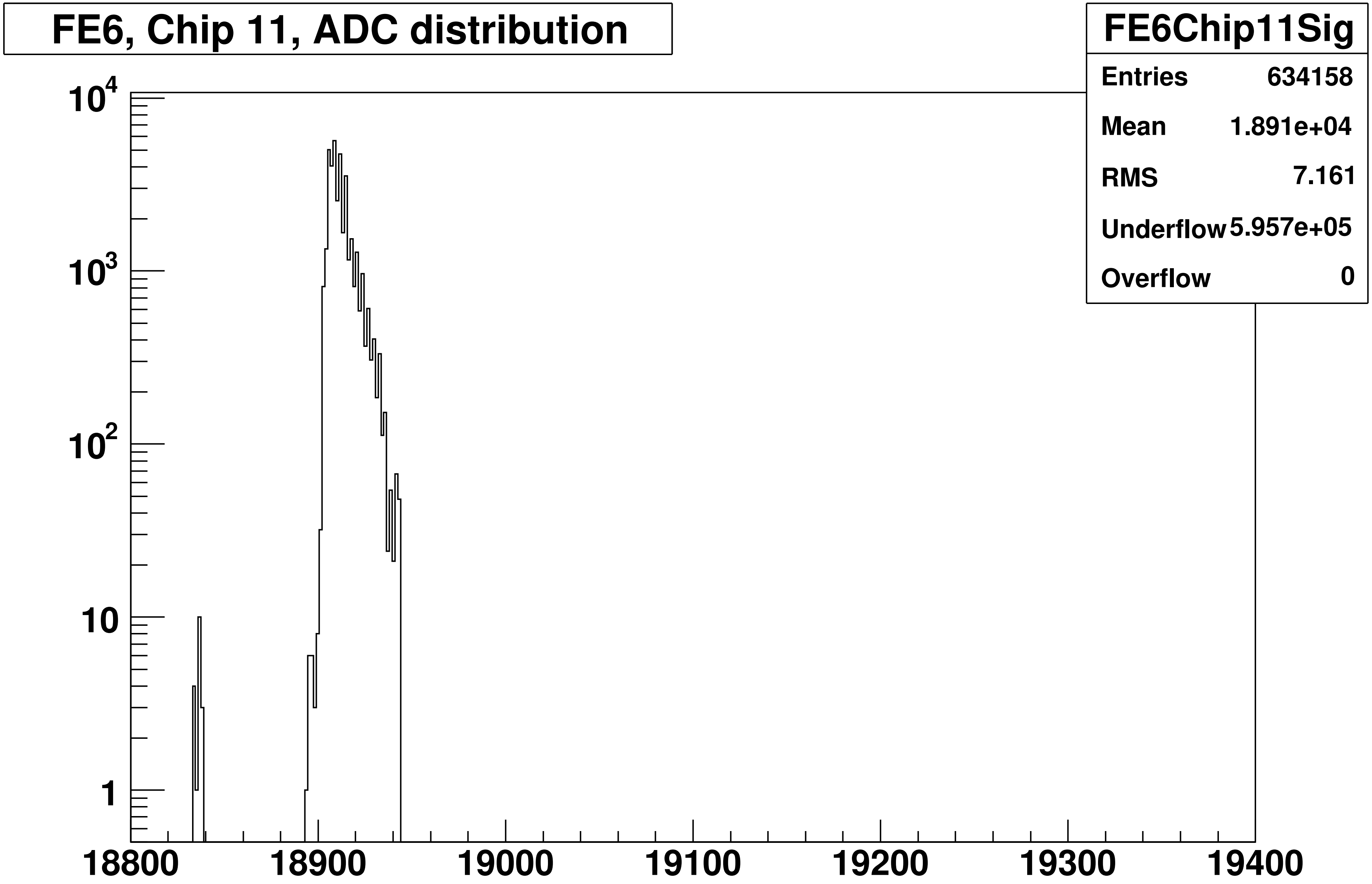
60
80
100


FE6, Chip 11, ADC distribution
FE6Chip11Sig
Entries 634158
Mean 1.891e+04
RMS 7.161
Underflow 5.957e+05
Overflow 0
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10^3
10^2
10
1
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18900
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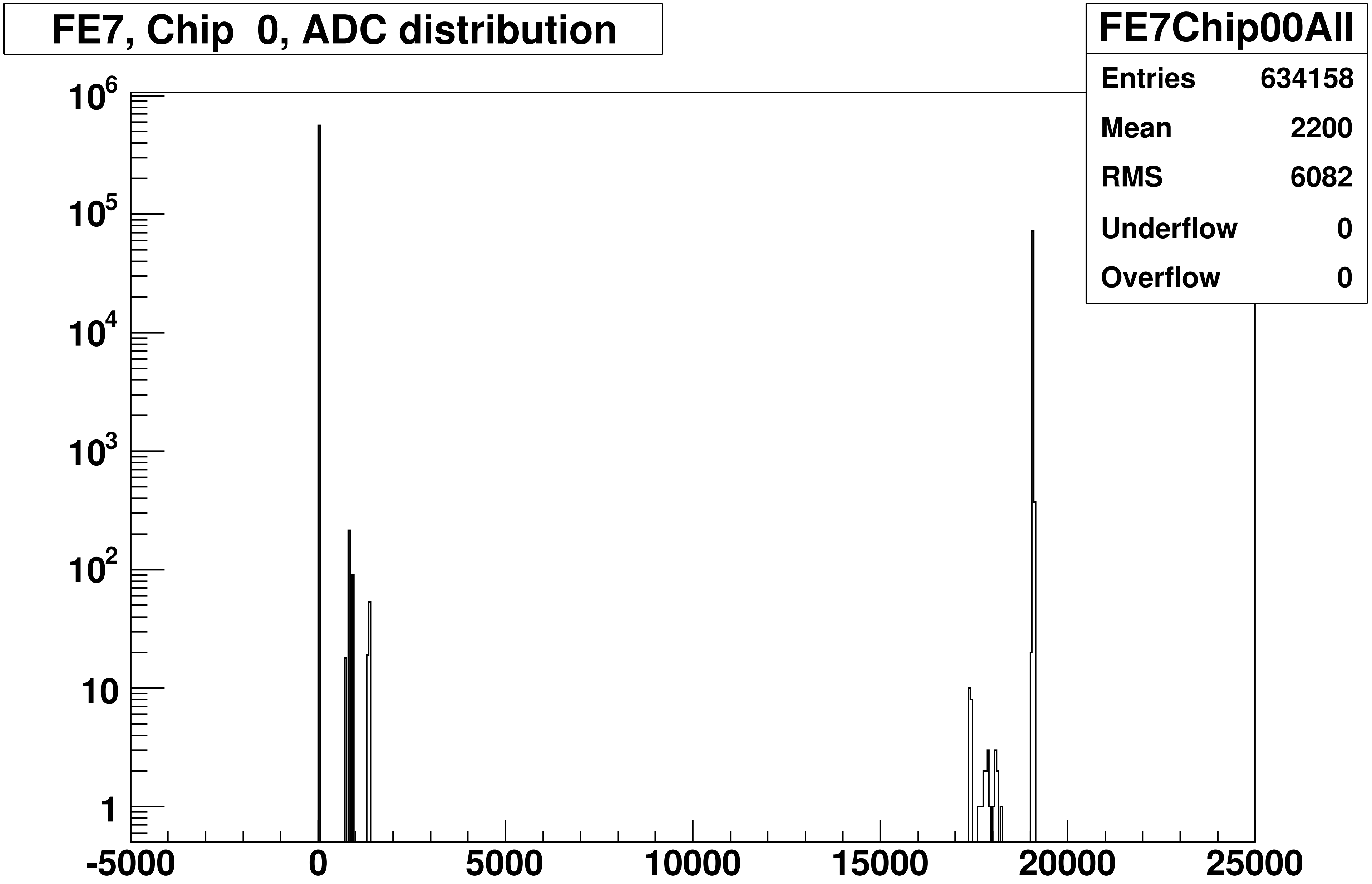
19200
19300
19400


FE7, Chip 0, ADC distribution
FE7Chip00All
Entries 634158
Mean 2200
RMS 6082
Underflow 0
Overflow 0
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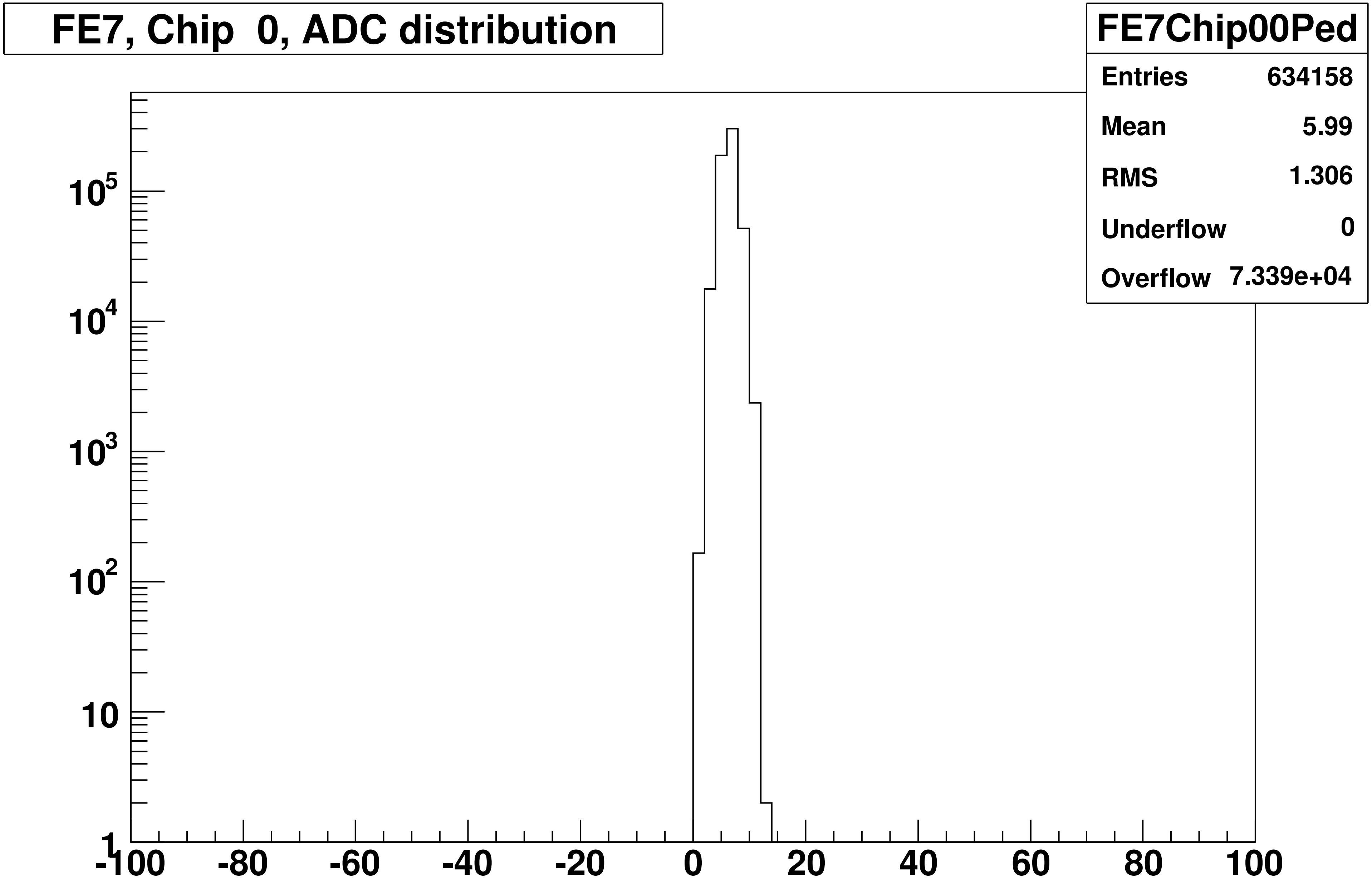
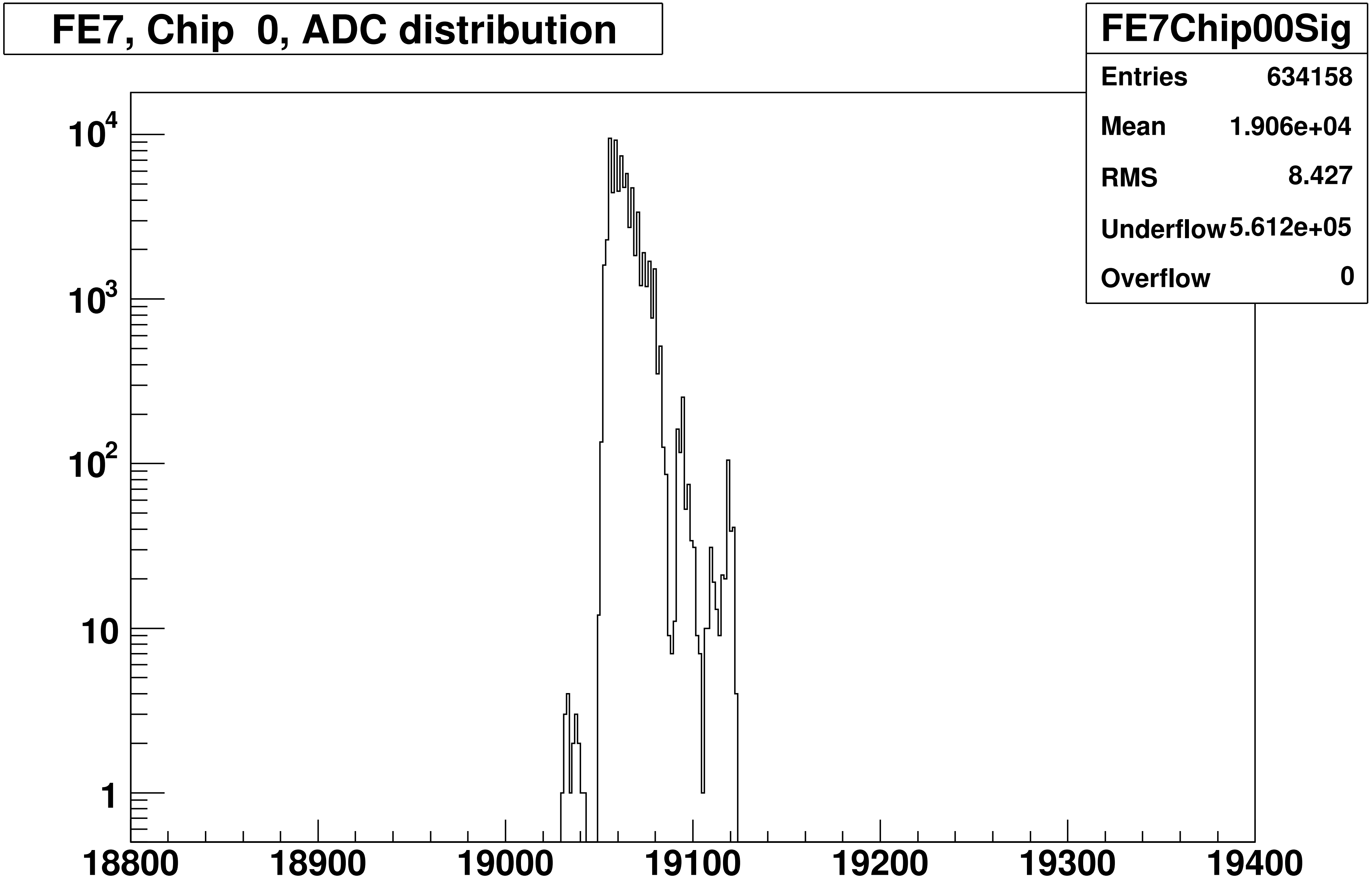
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE7, Chip 0, ADC distribution
FE7Chip00Ped
Entries 634158
Mean 5.99
RMS 1.306
Underflow 0
Overflow 7.339e+04
10^5
10^4
10^3
10^2
10
1
-100 -80 -60 -40 -20 0 20 40 60 80 100


FE7, Chip 0, ADC distribution
FE7Chip00Sig
Entries 634158
Mean 1.906e+04
RMS 8.427
Underflow 5.612e+05
Overflow 0
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10^3
10^2
10
1
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18900
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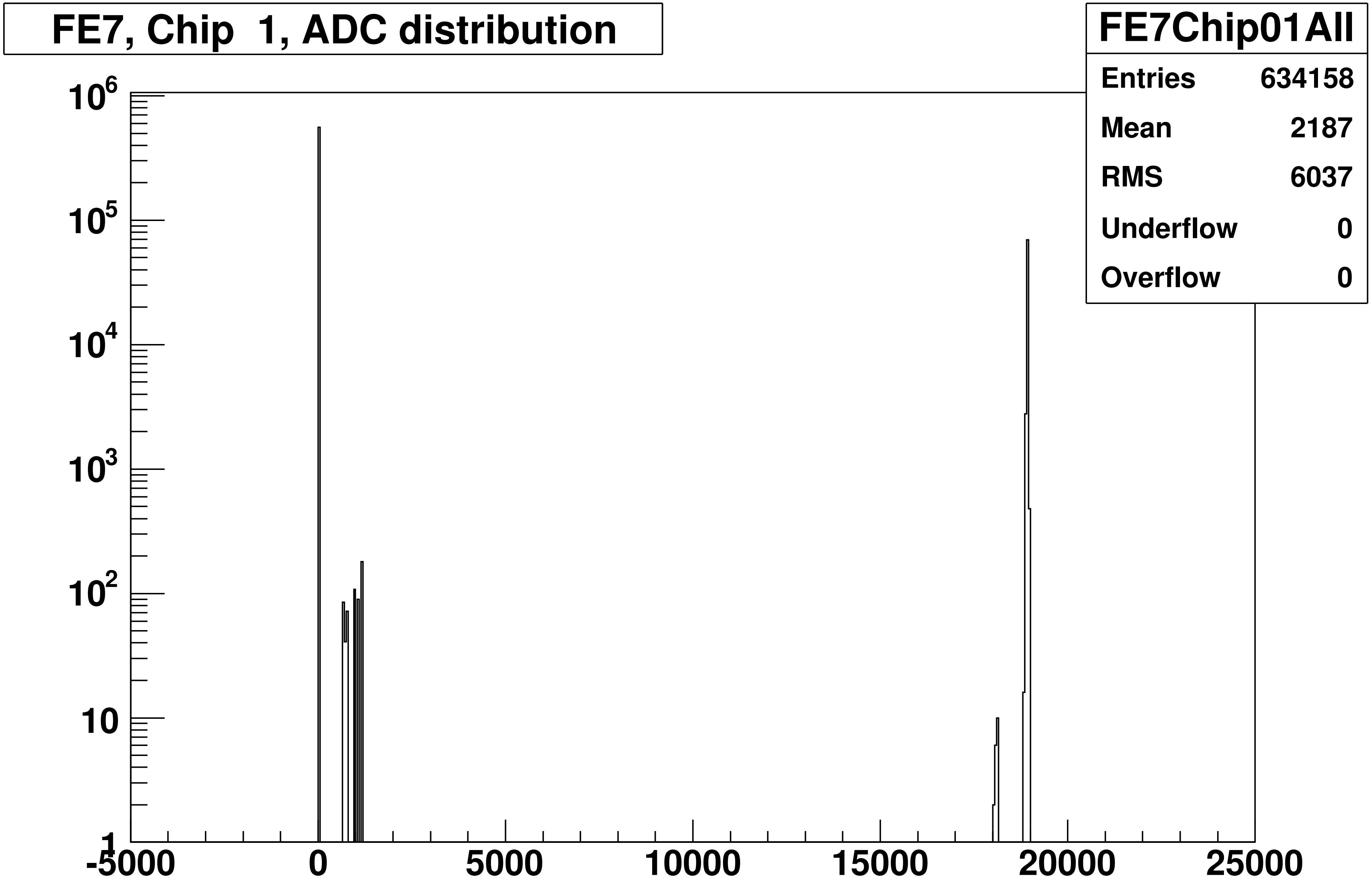
19100
19200
19300
19400


FE7, Chip 1, ADC distribution
FE7Chip01All
Entries 634158
Mean 2187
RMS 6037
Underflow 0
Overflow 0
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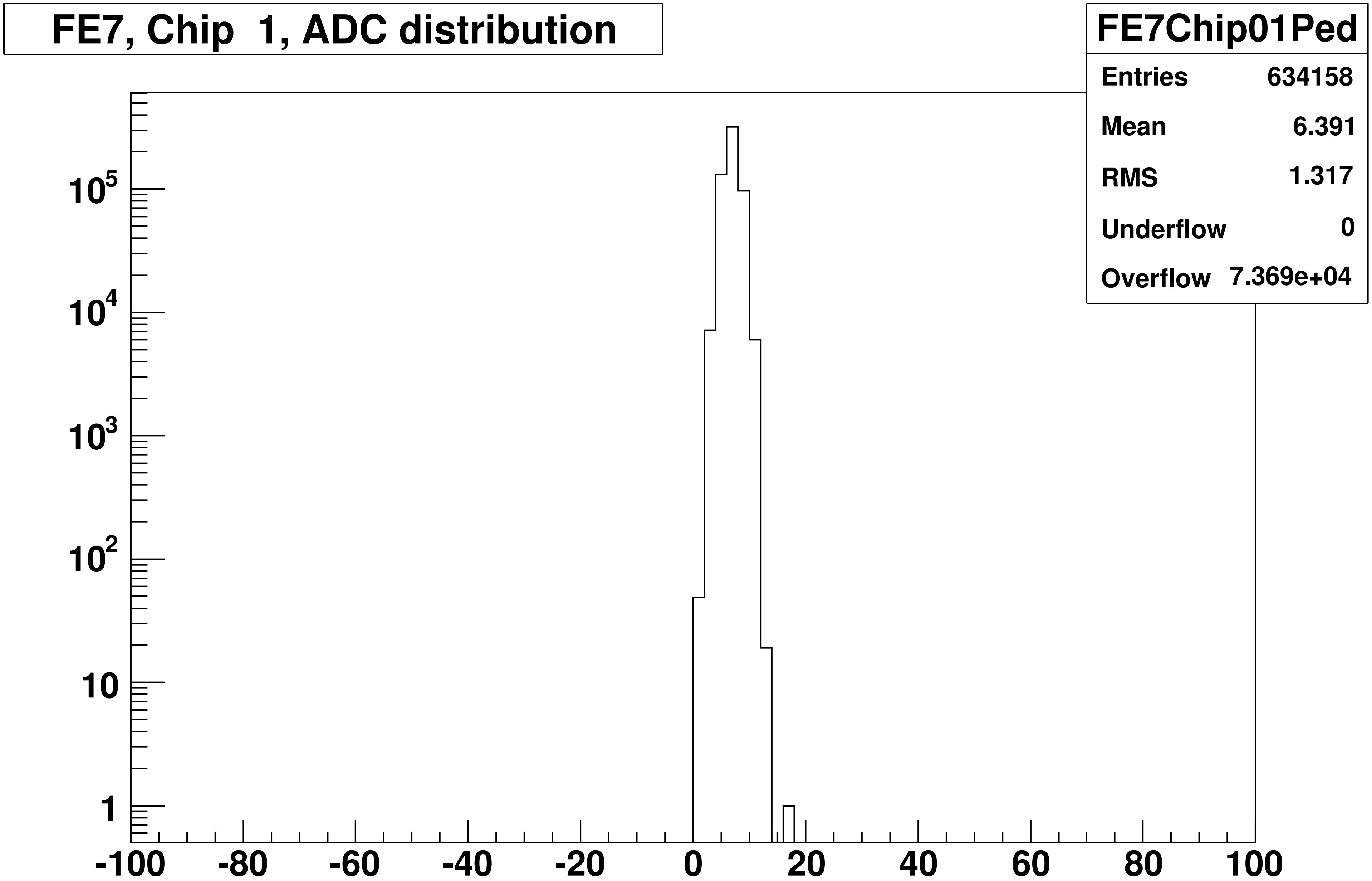
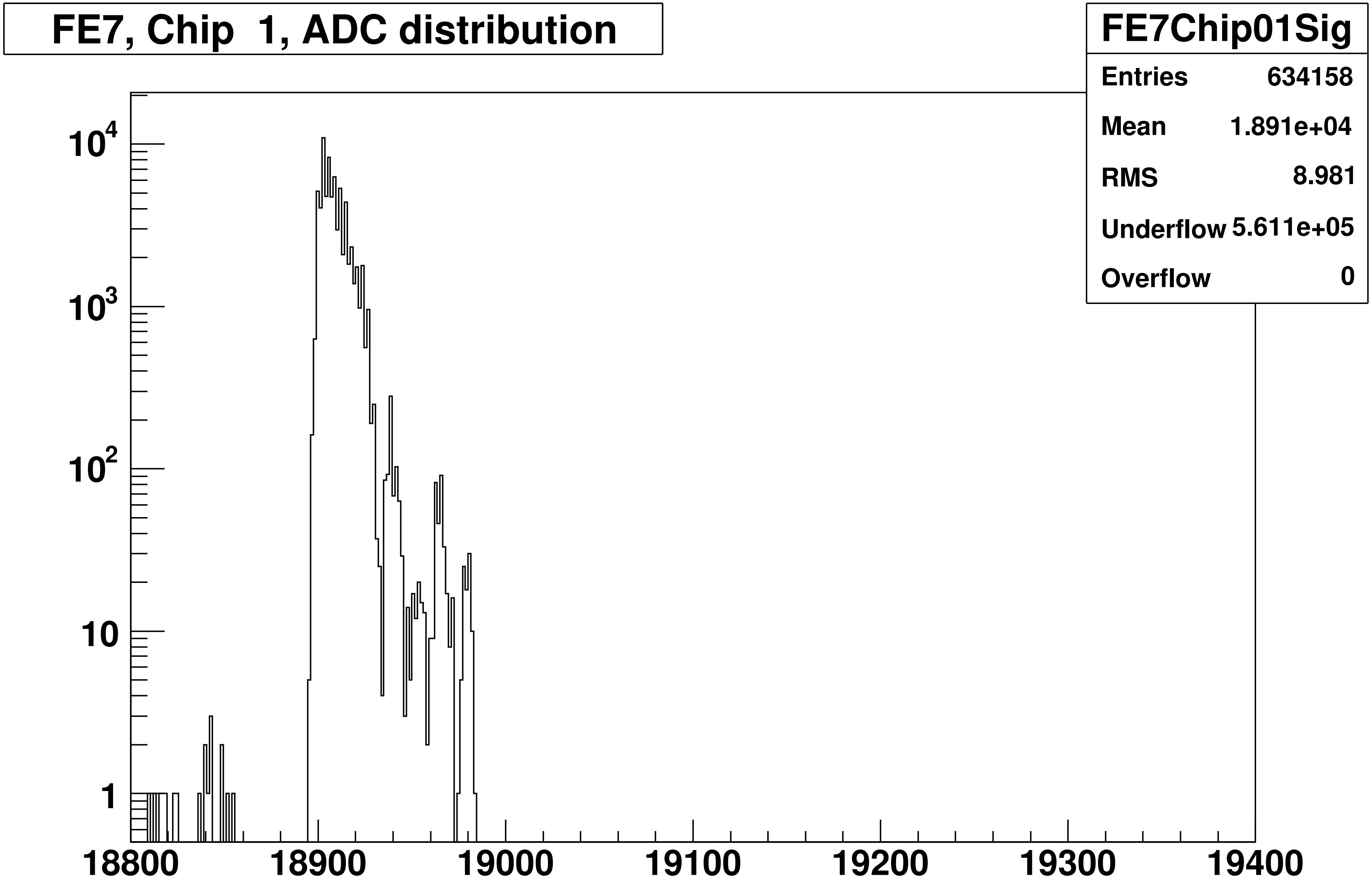
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE7, Chip 1, ADC distribution
FE7Chip01Ped
Entries 634158
Mean 6.391
RMS 1.317
Underflow 0
Overflow 7.369e+04
10^5
10^4
10^3
10^2
10
1
-100
-80
-60
-40
-20
0
20
40
60
80
100



FE7, Chip 1, ADC distribution
FE7Chip01Sig
Entries 634158
Mean 1.891e+04
RMS 8.981
Underflow 5.611e+05
Overflow 0
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10^3
10^2
10
1
18800
18900
19000
19100
19200
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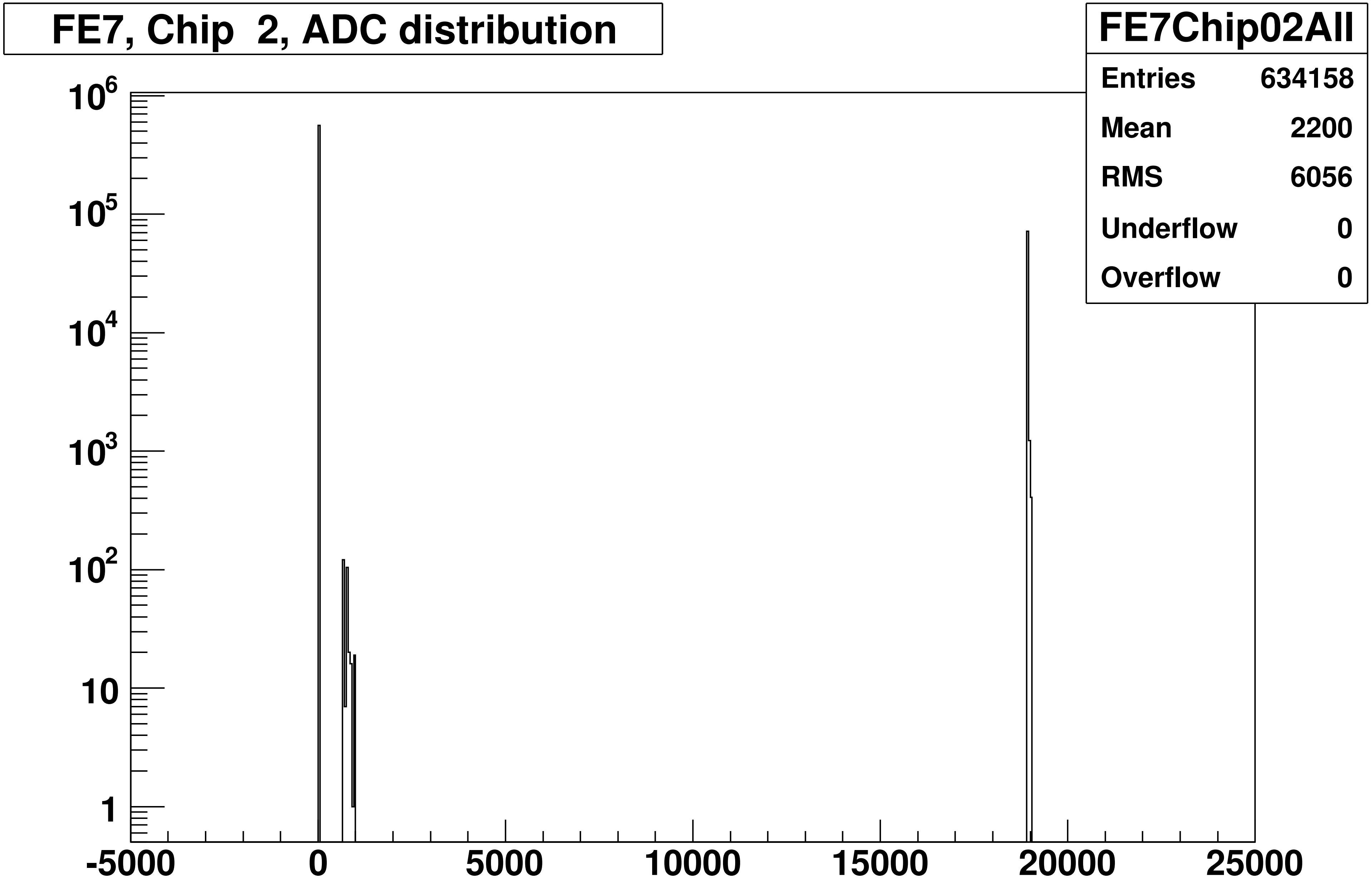

FE7, Chip 2, ADC distribution
FE7Chip02All
Entries 634158
Mean 2200
RMS 6056
Underflow 0
Overflow 0
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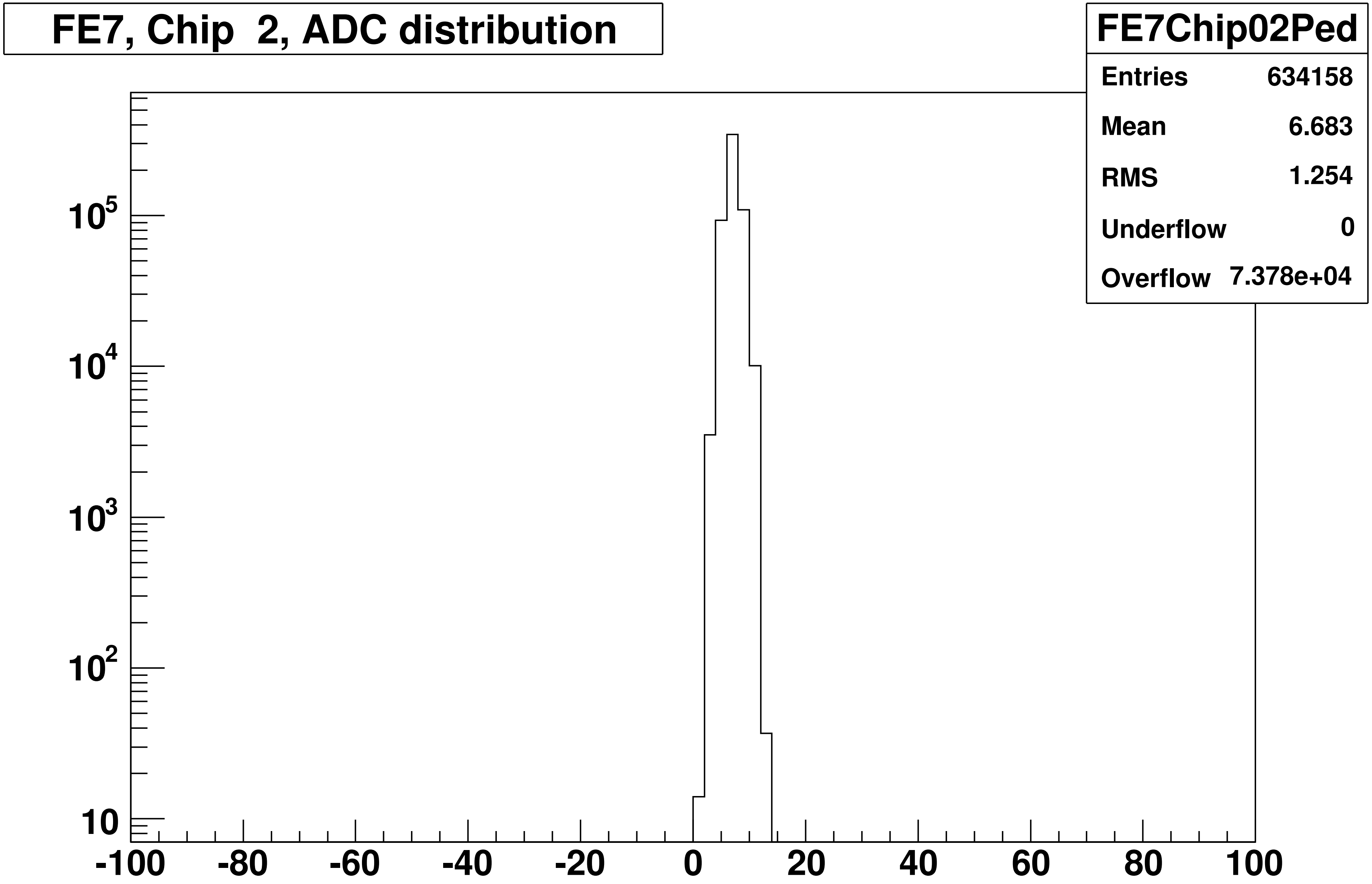
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE7, Chip 2, ADC distribution
FE7Chip02Ped
Entries 634158
Mean 6.683
RMS 1.254
Underflow 0
Overflow 7.378e+04
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10^4
10^3
10^2
10
-100
-80
-60
-40
-20
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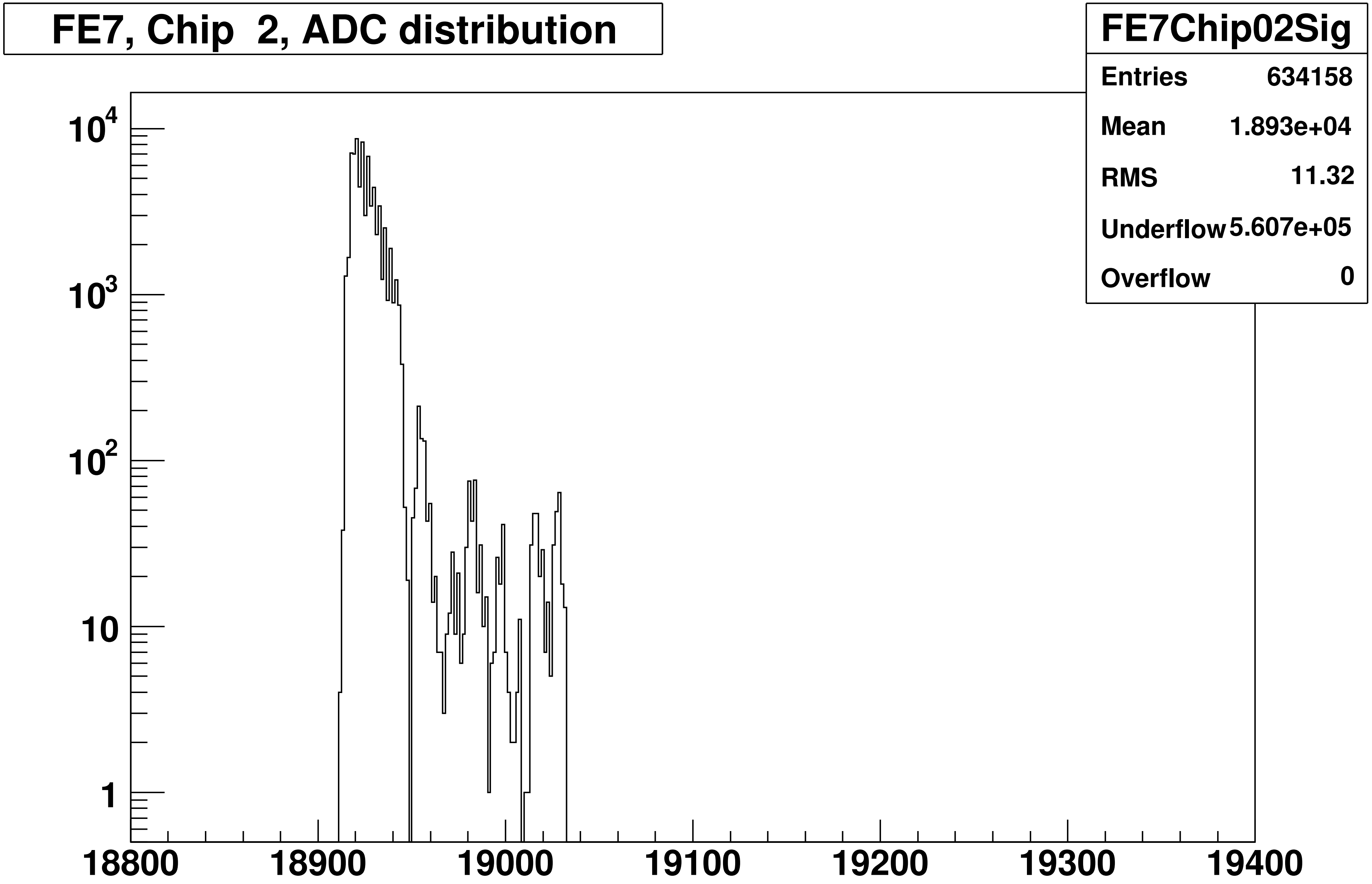
40
60
80
100


FE7, Chip 2, ADC distribution
FE7Chip02Sig
Entries 634158
Mean 1.893e+04
RMS 11.32
Underflow 5.607e+05
Overflow 0
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10^3
10^2
10
1
18800
18900
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19100
19200
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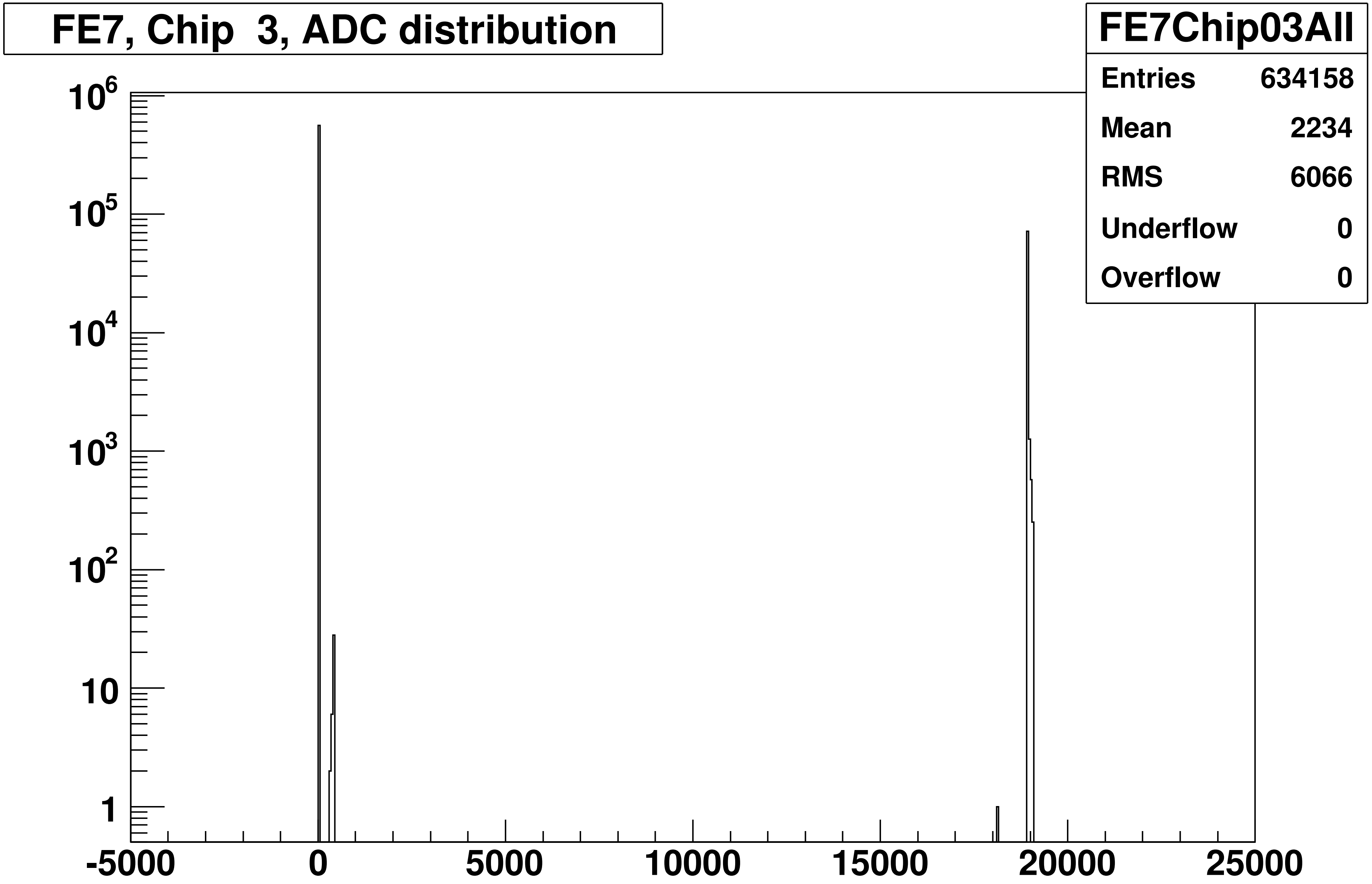
19400


FE7, Chip 3, ADC distribution
FE7Chip03All
Entries 634158
Mean 2234
RMS 6066
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
1
-5000
0
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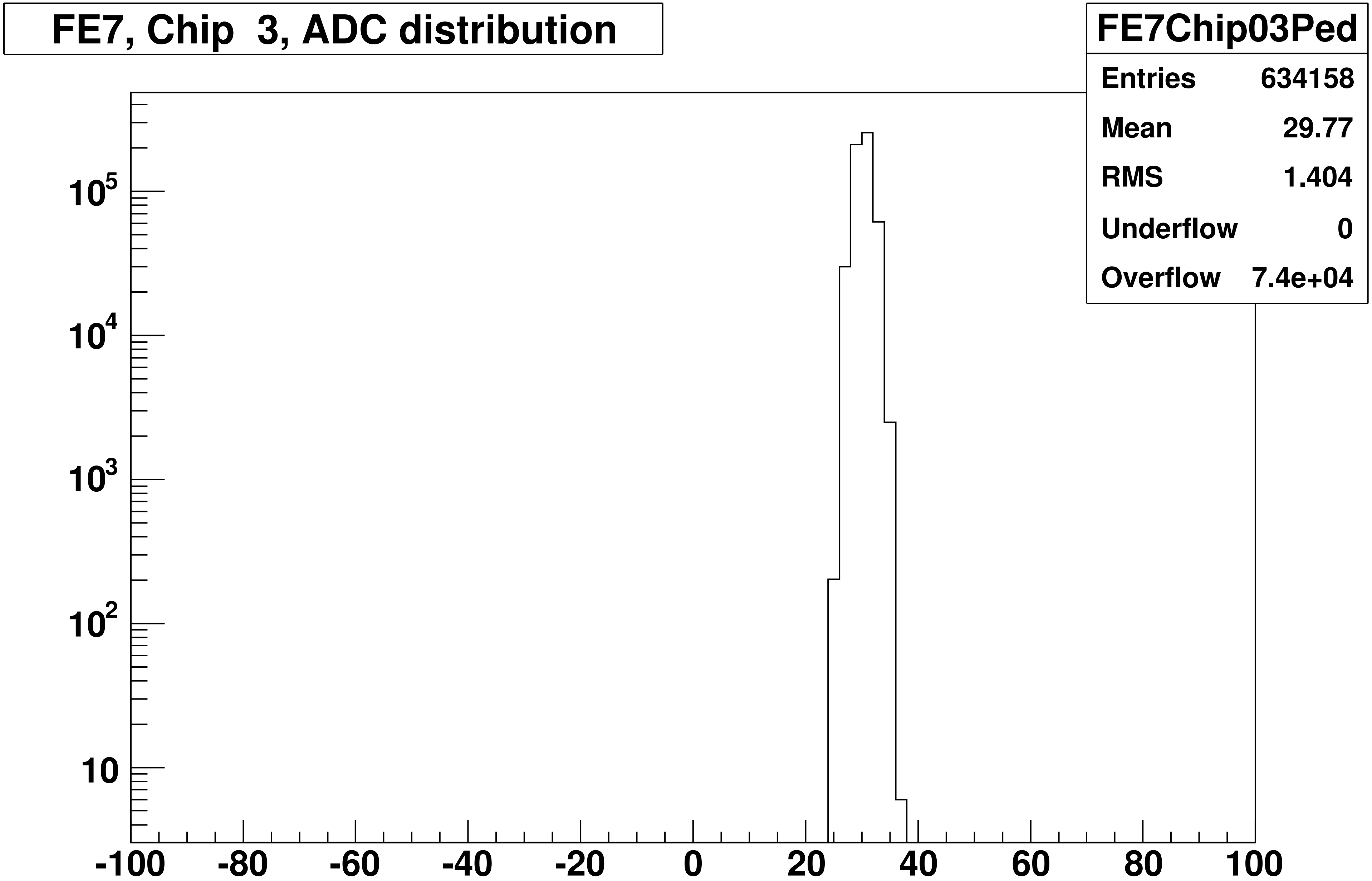
10000
15000
20000
25000


FE7, Chip 3, ADC distribution
FE7Chip03Ped
Entries 634158
Mean 29.77
RMS 1.404
Underflow 0
Overflow 7.4e+04
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10^4
10^3
10^2
10
-100
-80
-60
-40
-20
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40
60
80
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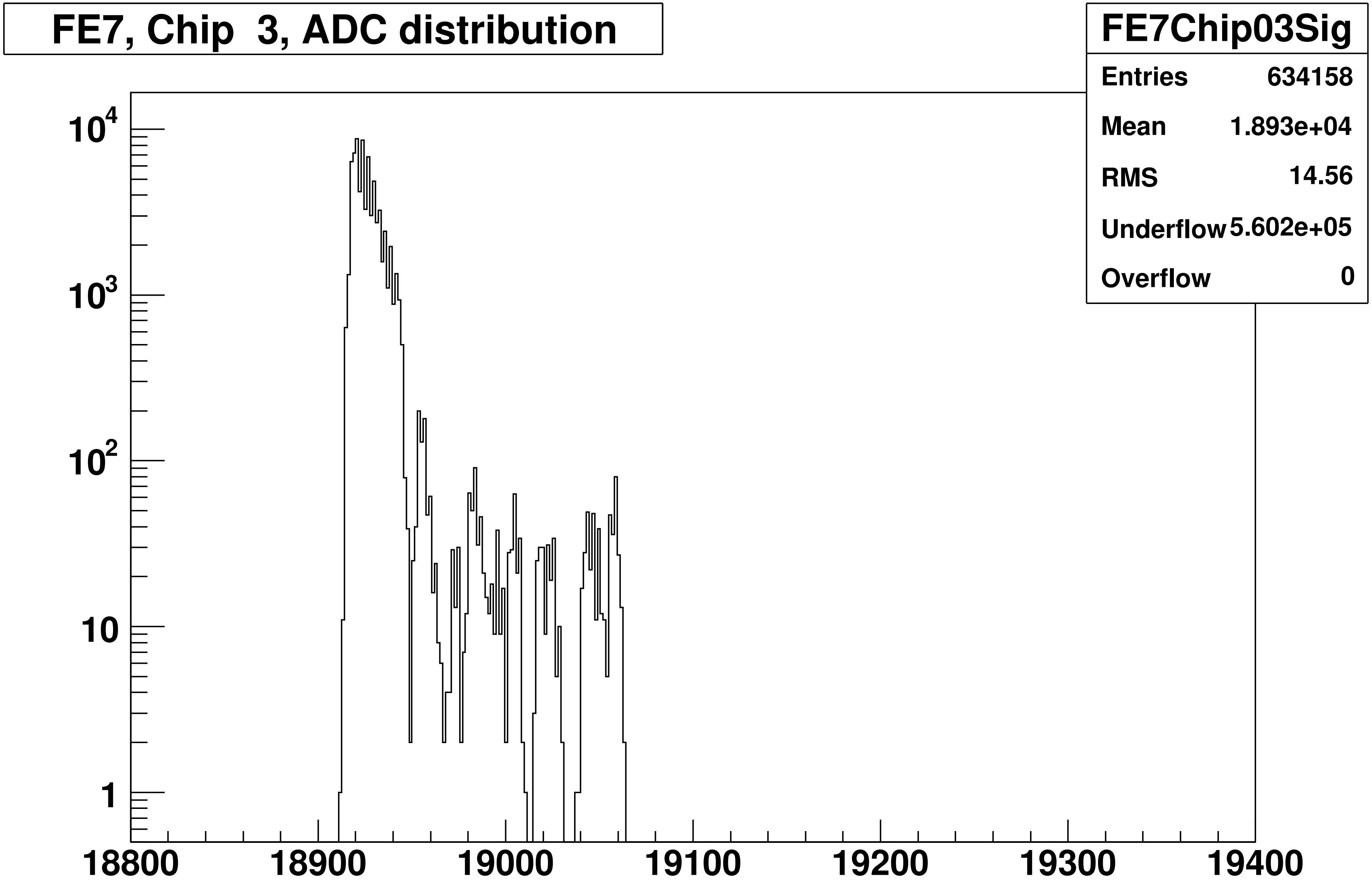

FE7, Chip 3, ADC distribution
FE7Chip03Sig
Entries 634158
Mean 1.893e+04
RMS 14.56
Underflow 5.602e+05
Overflow 0
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10^3
10^2
10
1
18800
18900
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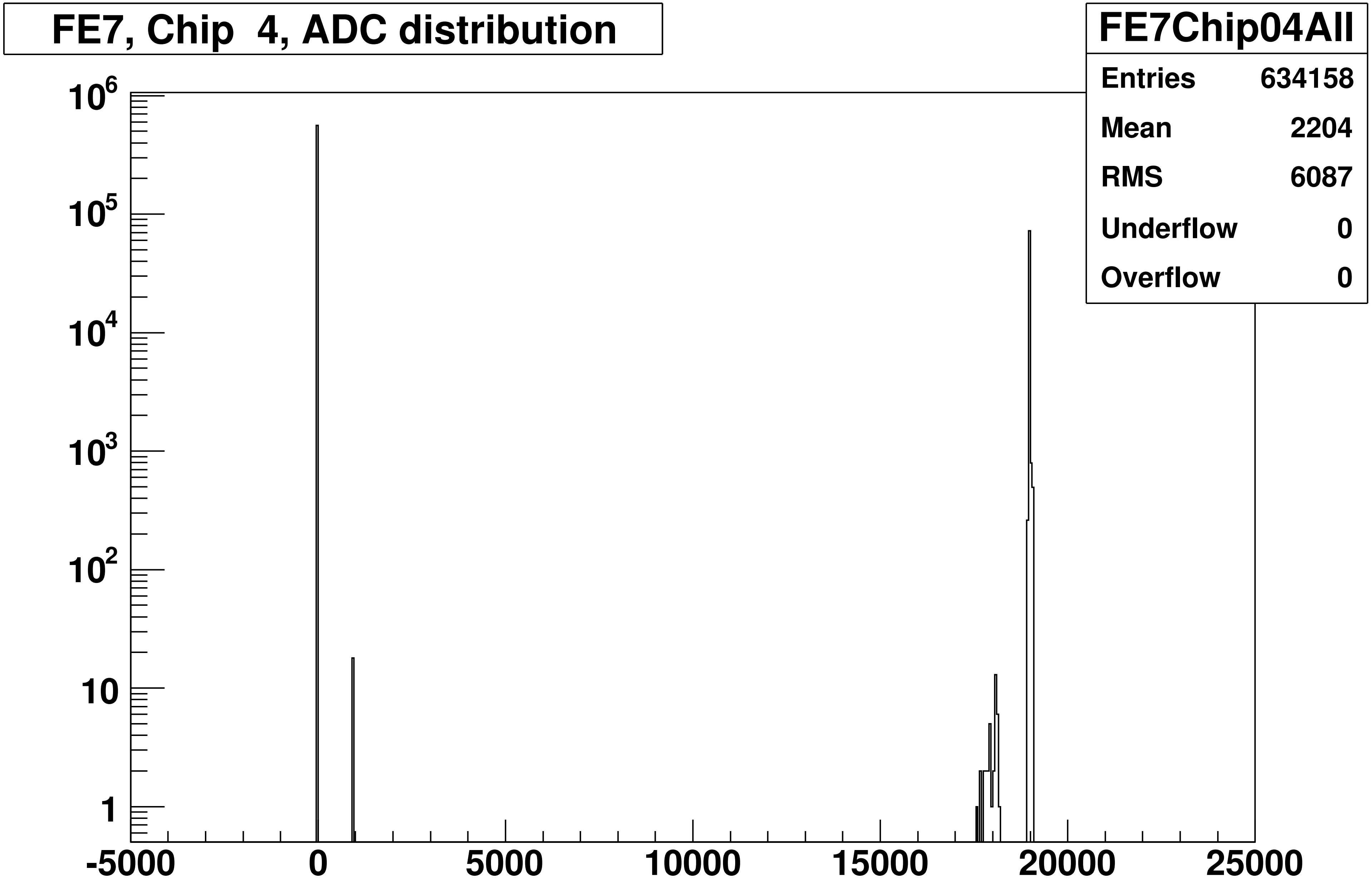
FE7, Chip 4, ADC distribution
FE7Chip04All
Entries 634158
Mean 2204
RMS 6087
Underflow 0
Overflow 0
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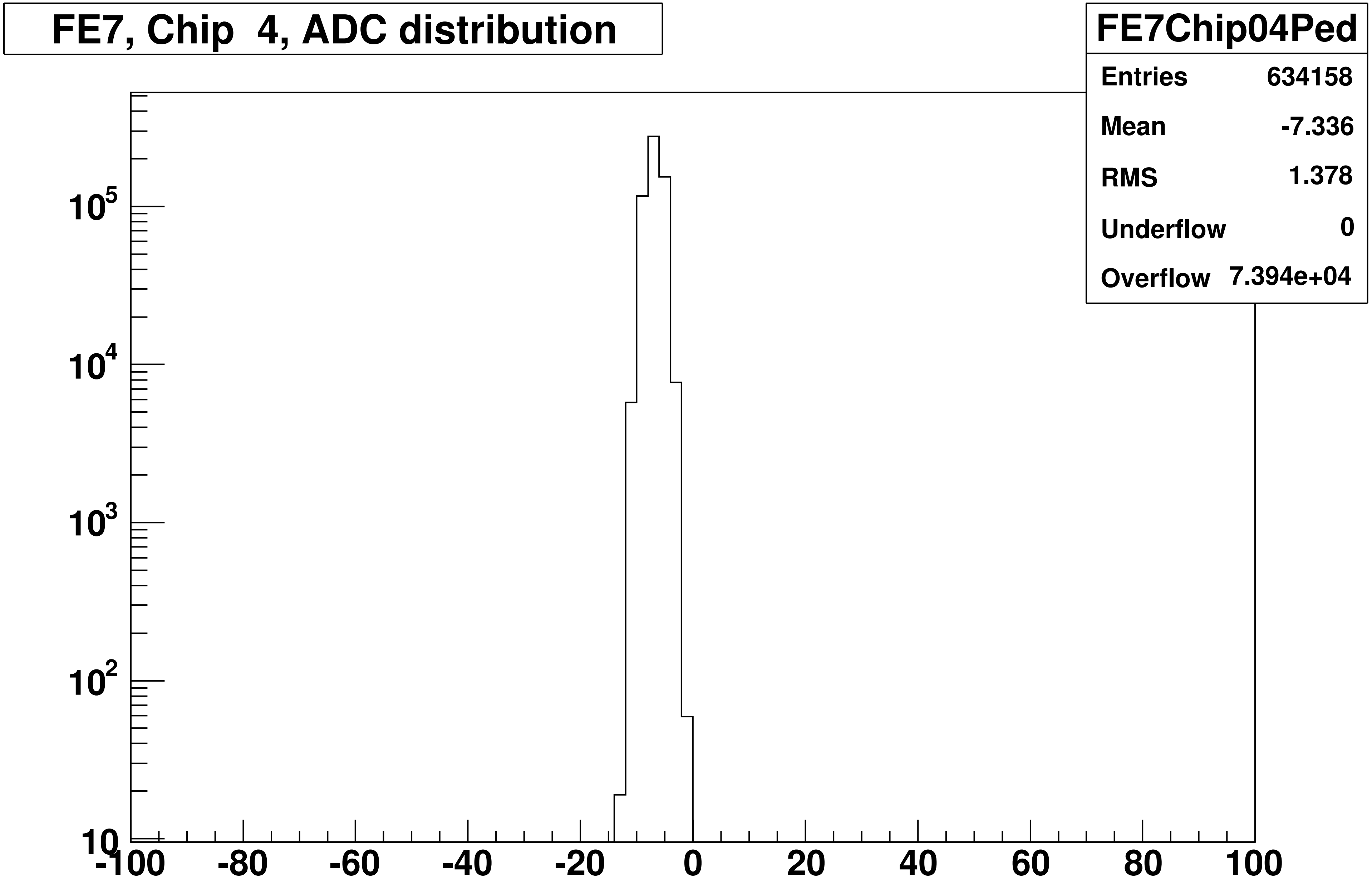
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE7, Chip 4, ADC distribution
FE7Chip04Ped
Entries 634158
Mean -7.336
RMS 1.378
Underflow 0
Overflow 7.394e+04
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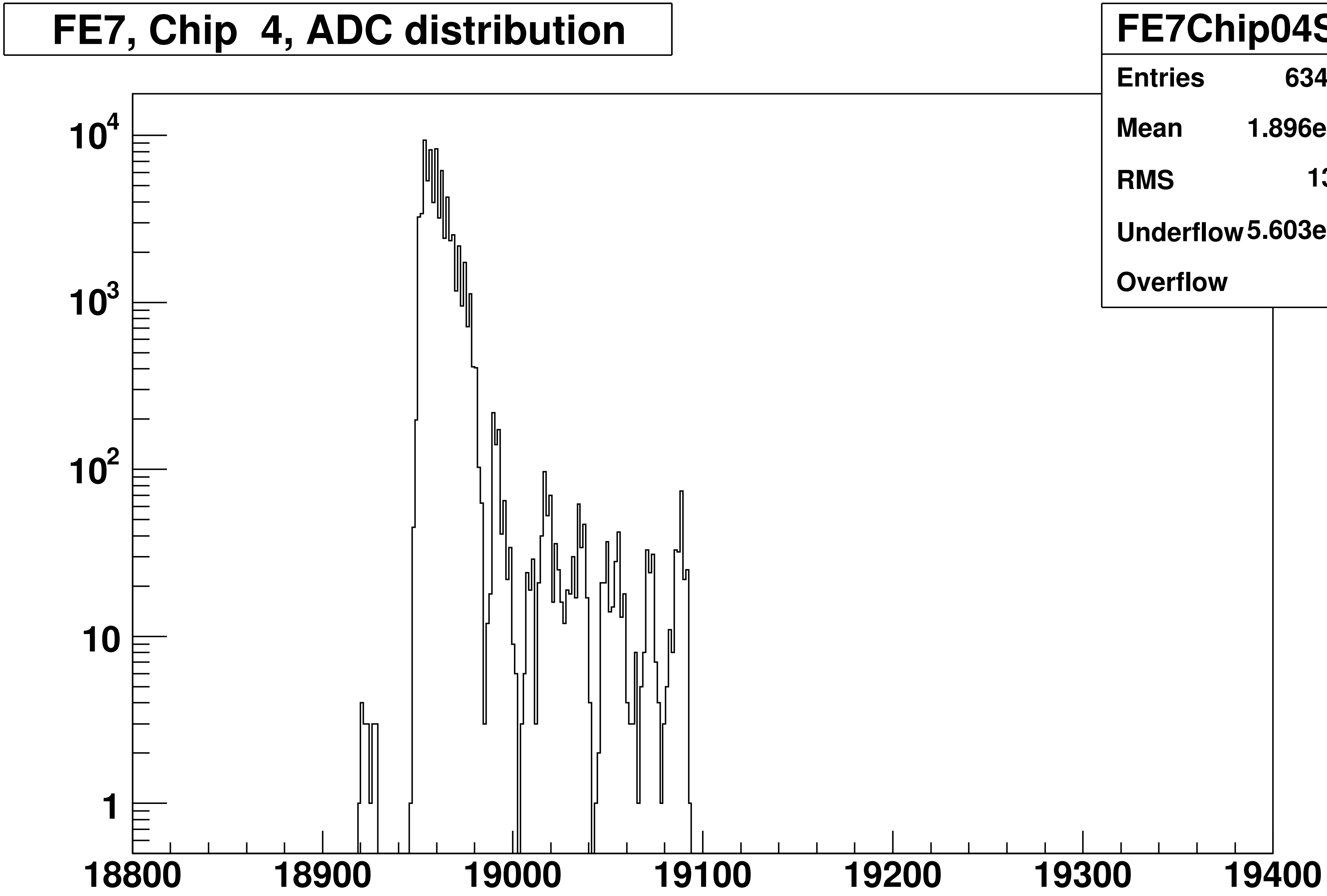
10^4
10^3
10^2
10
-100
-80
-60
-40
-20
0
20
40
60
80
100


FE7, Chip 4, ADC distribution
FE7Chip04Sig
Entries 634158
Mean 1.896e+04
RMS 13.68
Underflow 5.603e+05
Overflow 0
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10^3
10^2
10
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18900
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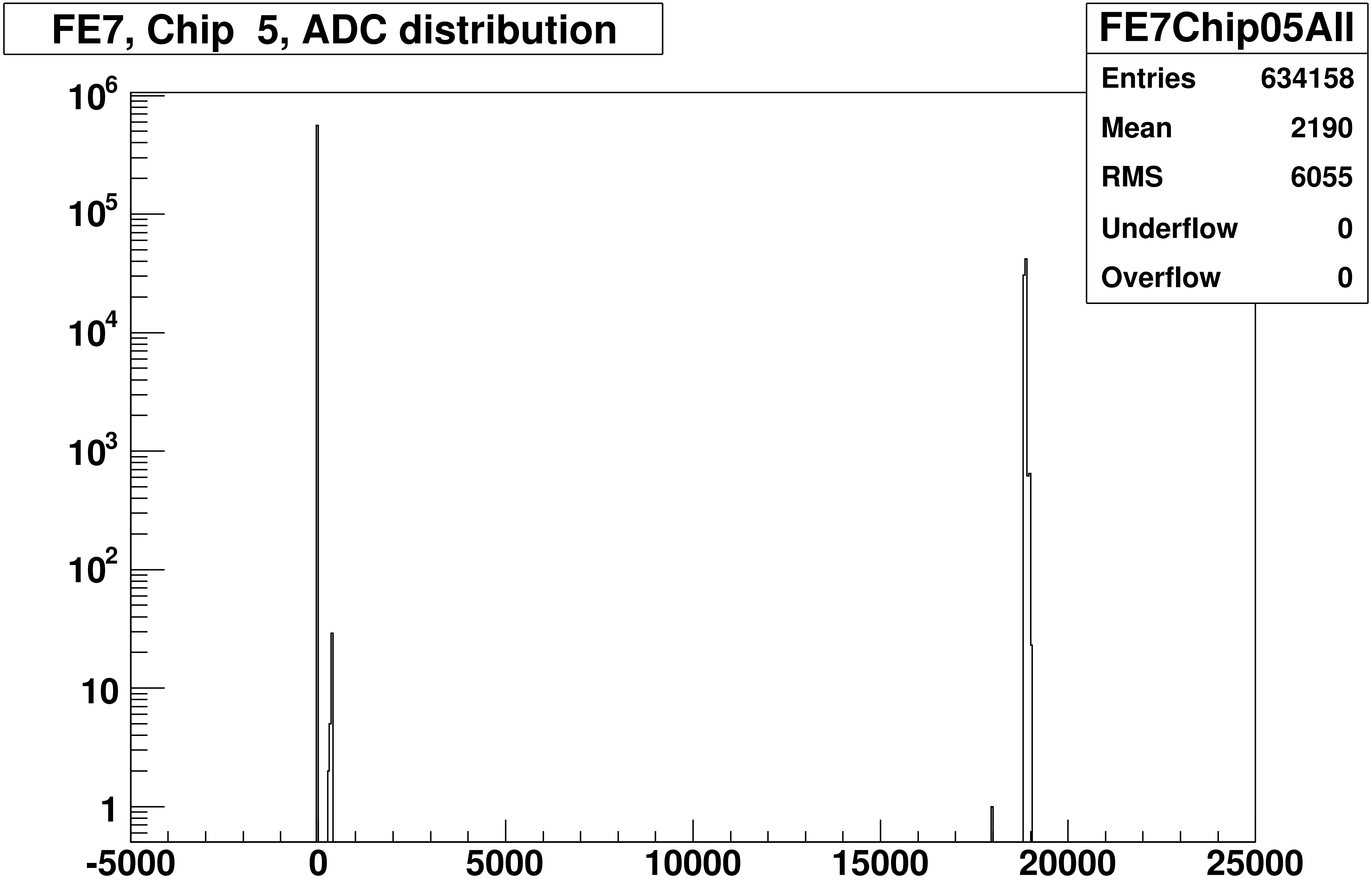
19400


FE7, Chip 5, ADC distribution
FE7Chip05All
Entries 634158
Mean 2190
RMS 6055
Underflow 0
Overflow 0
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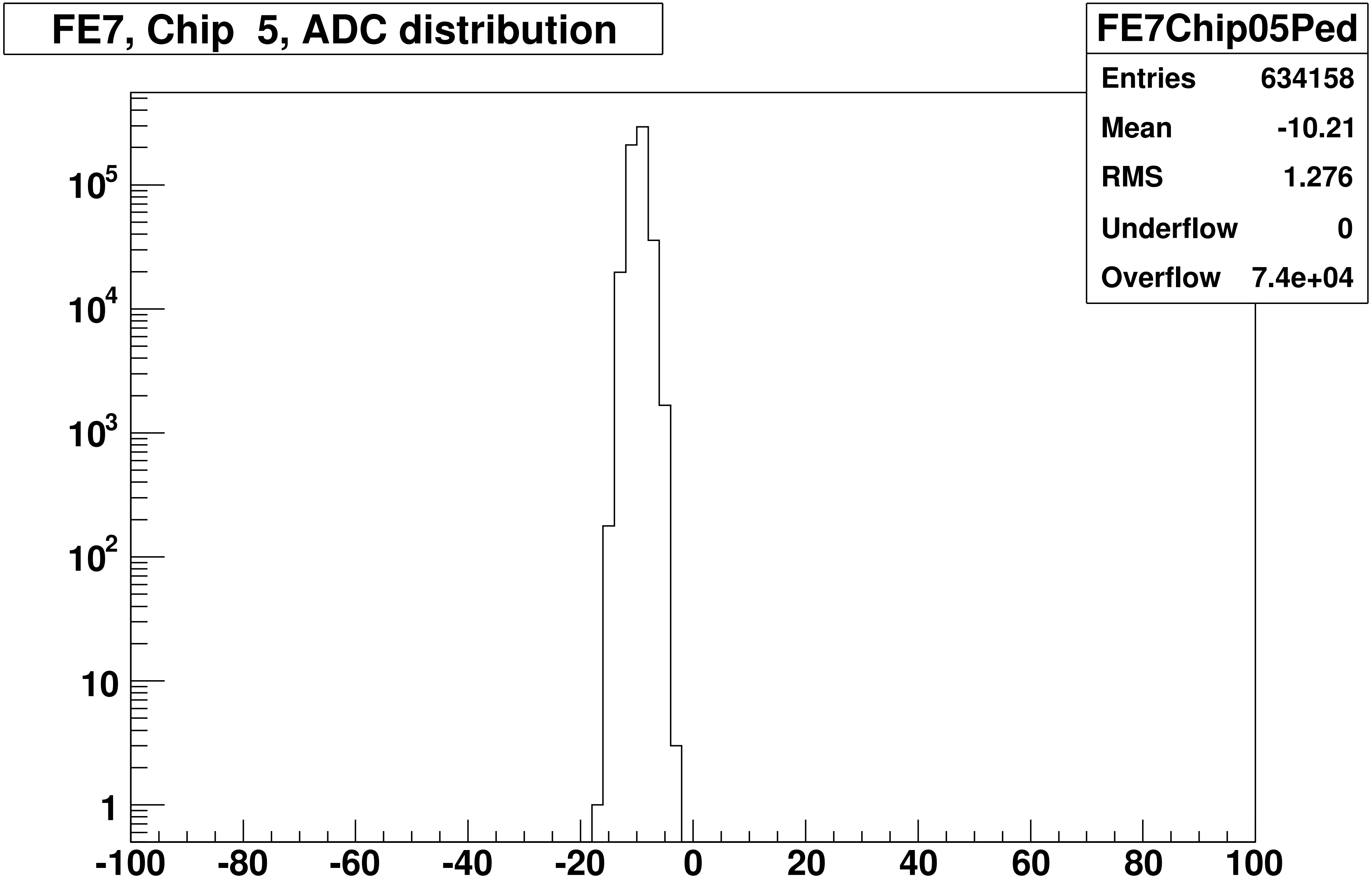
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE7, Chip 5, ADC distribution
FE7Chip05Ped
Entries 634158
Mean -10.21
RMS 1.276
Underflow 0
Overflow 7.4e+04
10^5
10^4
10^3
10^2
10
1
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-20
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60
80
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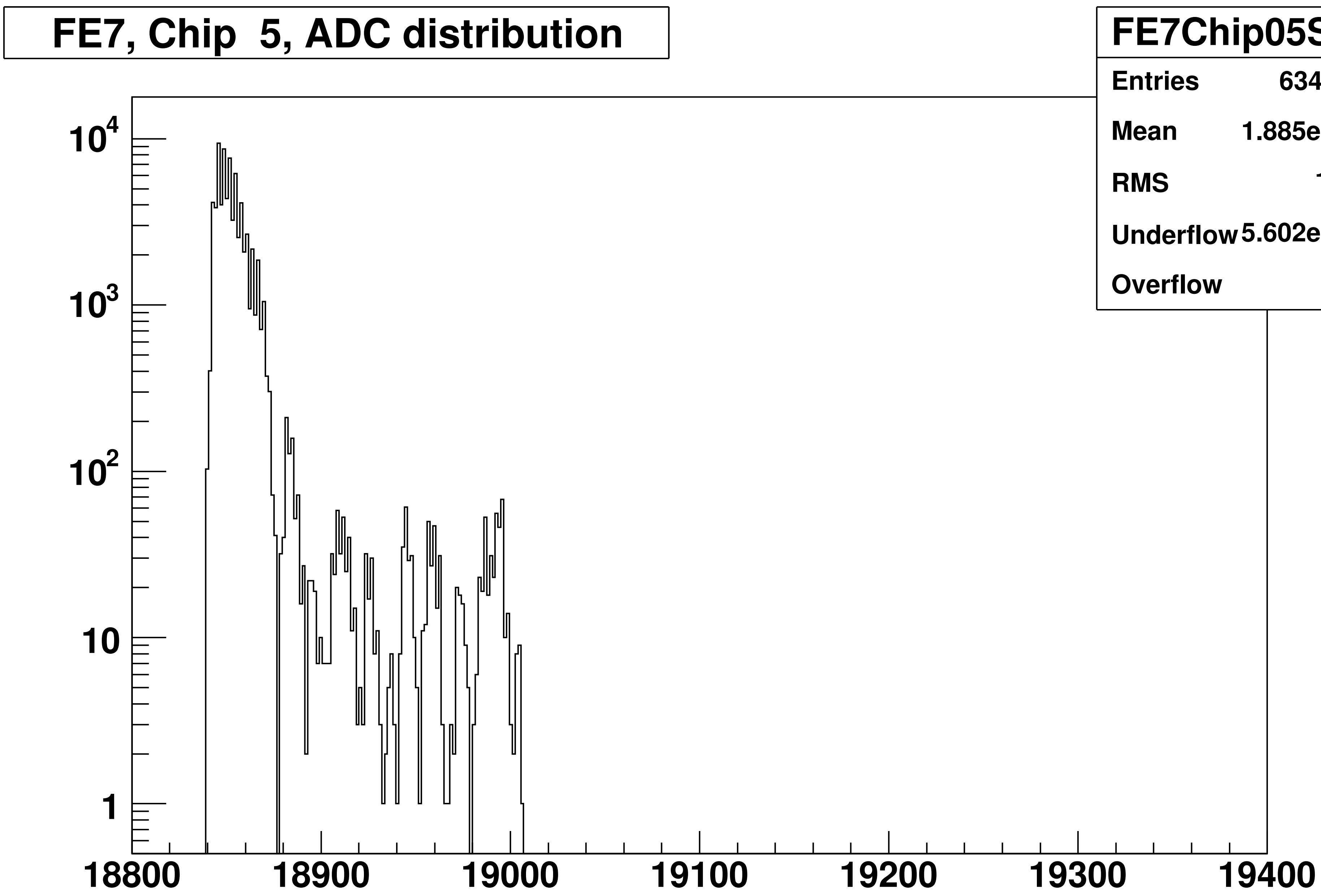
FE7, Chip 5, ADC distribution
FE7Chip05Sig
Entries 634158
Mean 1.885e+04
RMS 15.8
Underflow 5.602e+05
Overflow 0
10^4
10^3
10^2
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1
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18900
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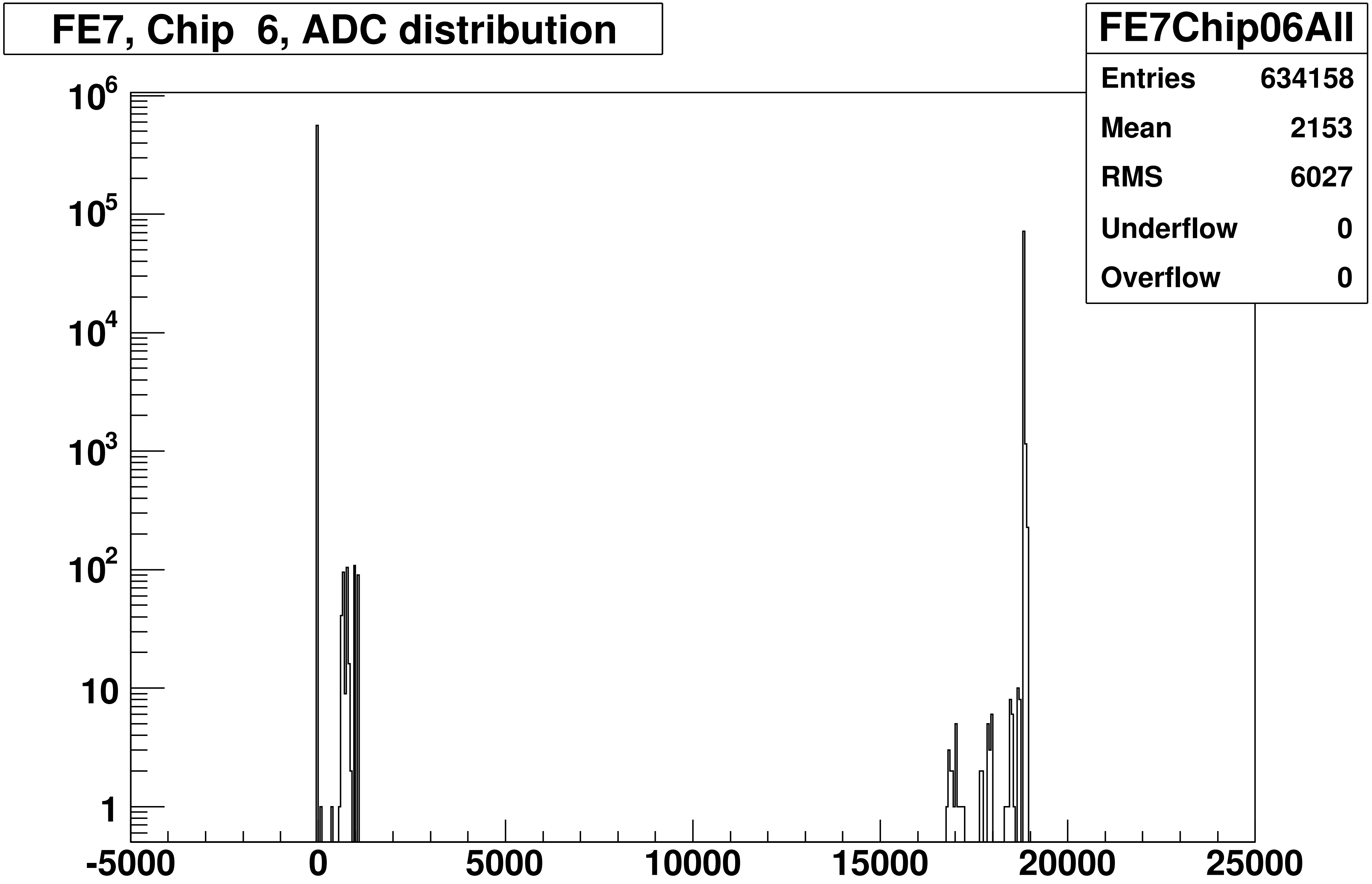
19400



FE7, Chip 6, ADC distribution
FE7Chip06All
Entries 634158
Mean 2153
RMS 6027
Underflow 0
Overflow 0
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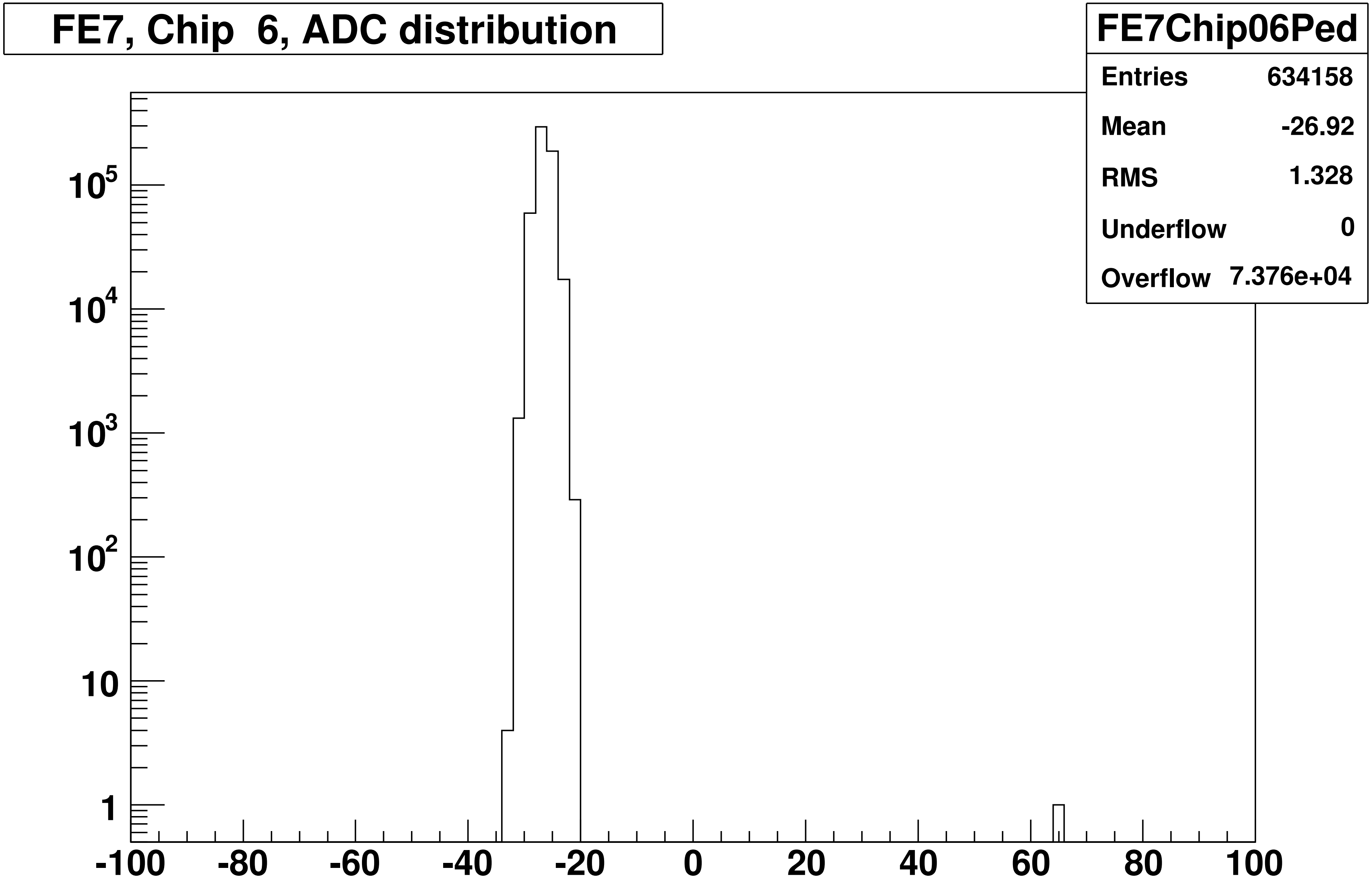
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE7, Chip 6, ADC distribution
FE7Chip06Ped
Entries 634158
Mean -26.92
RMS 1.328
Underflow 0
Overflow 7.376e+04
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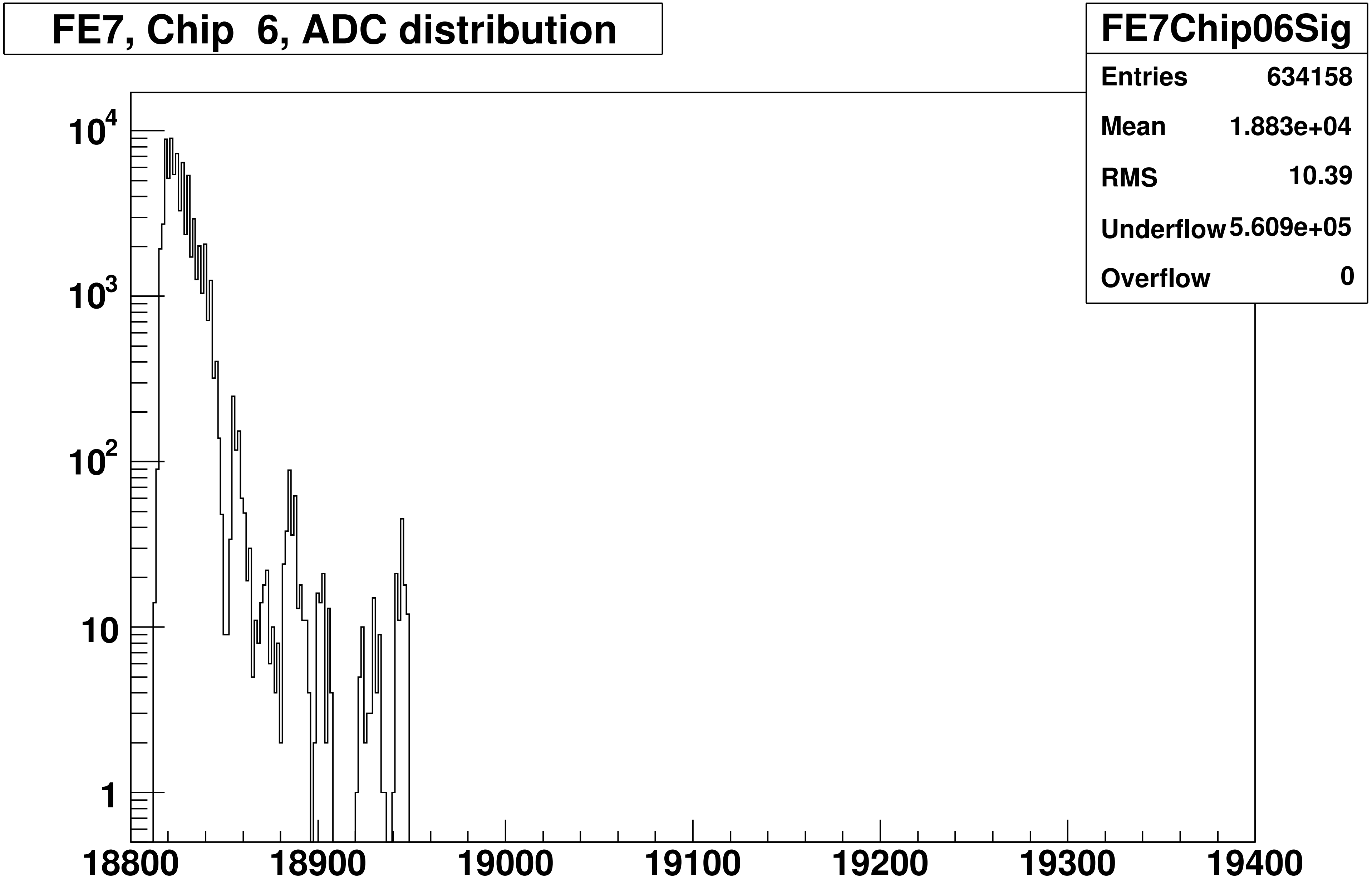
1 10 10^2 10^3 10^4 10^5


FE7, Chip 6, ADC distribution
FE7Chip06Sig
Entries 634158
Mean 1.883e+04
RMS 10.39
Underflow 5.609e+05
Overflow 0
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10^3
10^2
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1
18800
18900
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19100
19200
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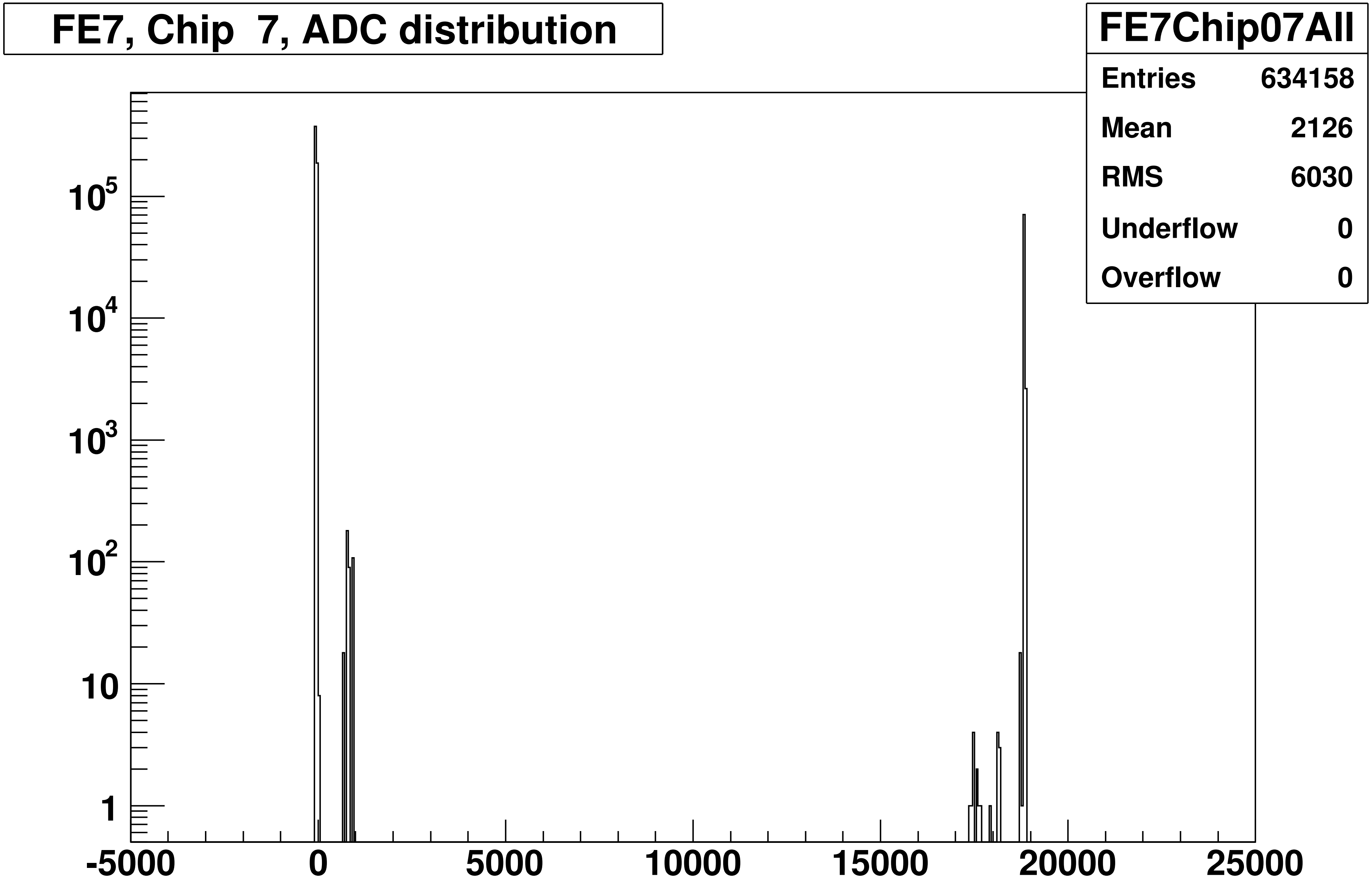
19400



FE7, Chip 7, ADC distribution
FE7Chip07All
Entries 634158
Mean 2126
RMS 6030
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
1
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5000
10000
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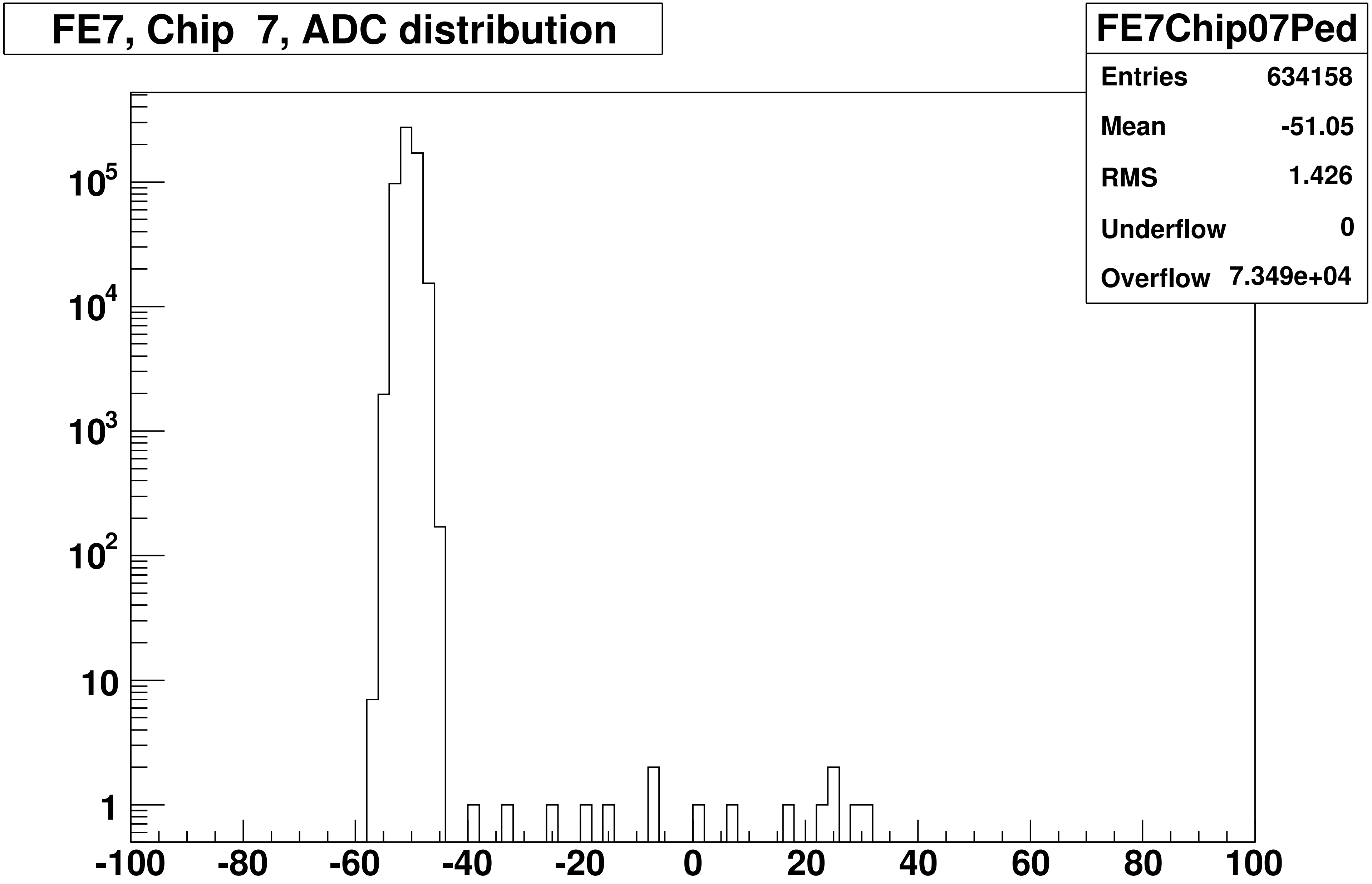
20000
25000


FE7, Chip 7, ADC distribution
FE7Chip07Ped
Entries 634158
Mean -51.05
RMS 1.426
Underflow 0
Overflow 7.349e+04
1
10
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10^3
10^4
10^5
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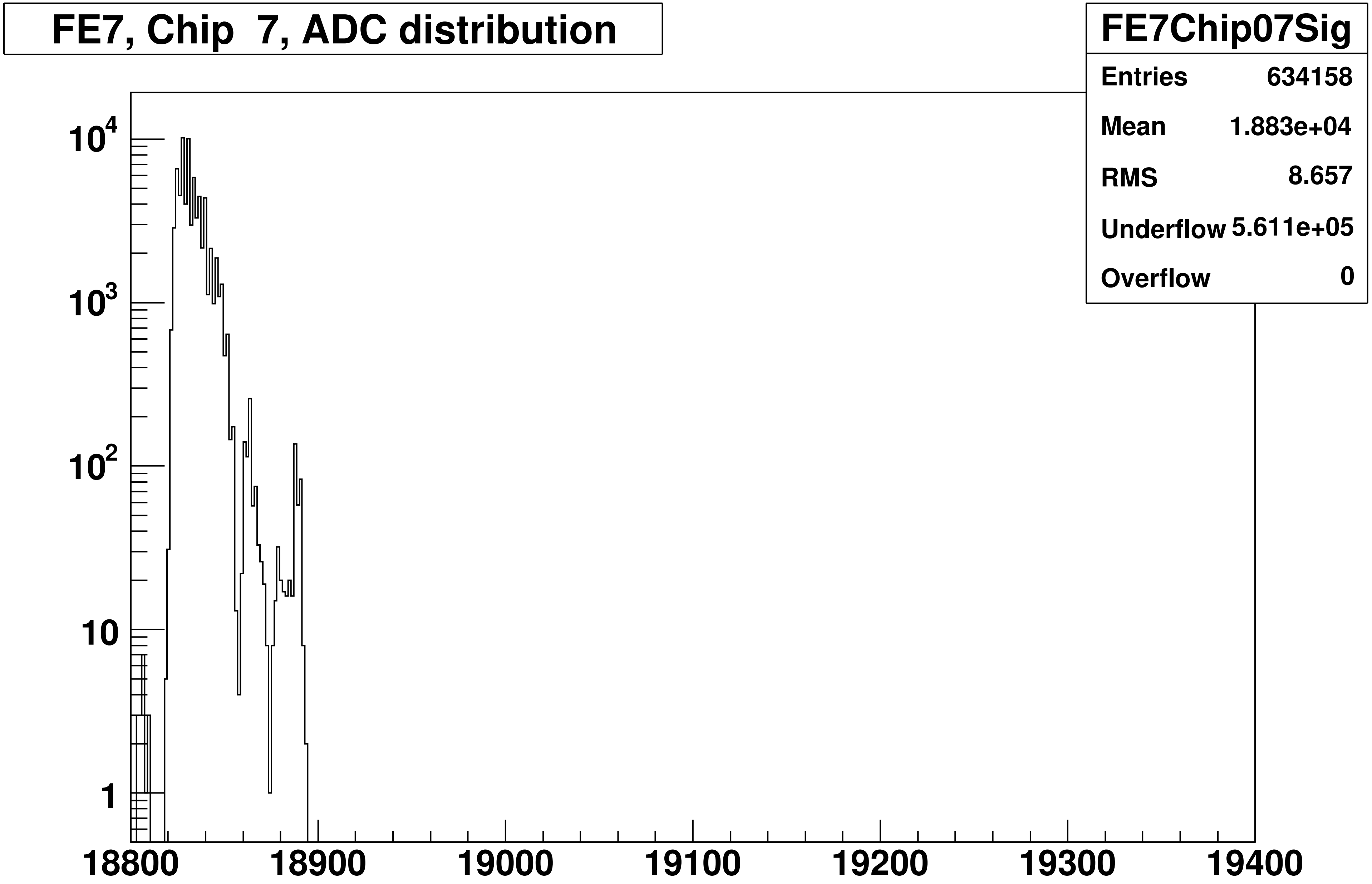
60
80
100


FE7, Chip 7, ADC distribution
FE7Chip07Sig
Entries 634158
Mean 1.883e+04
RMS 8.657
Underflow 5.611e+05
Overflow 0
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10^3
10^2
10
1
18800
18900
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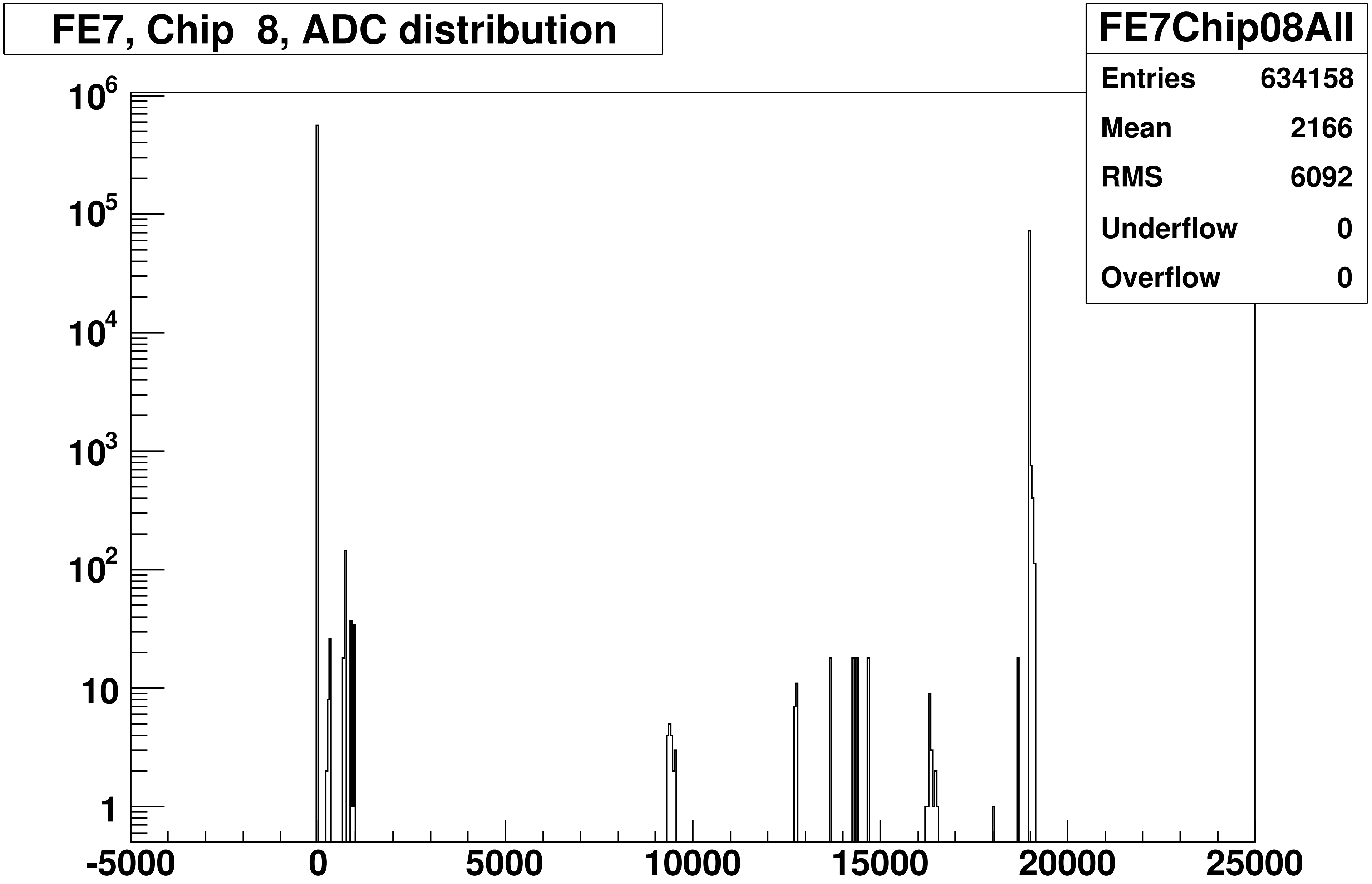
FE7, Chip 8, ADC distribution
FE7Chip08All
Entries 634158
Mean 2166
RMS 6092
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
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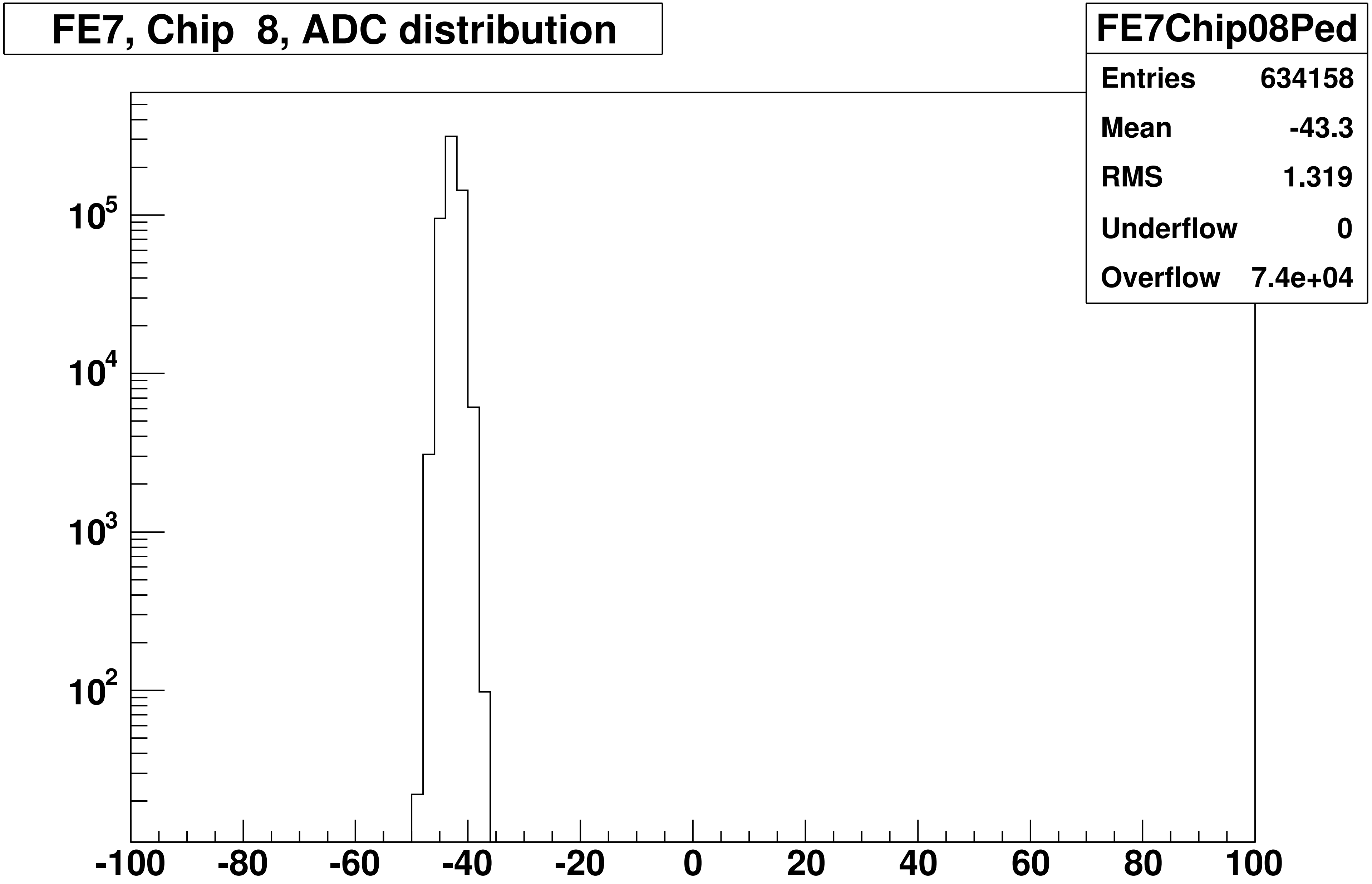
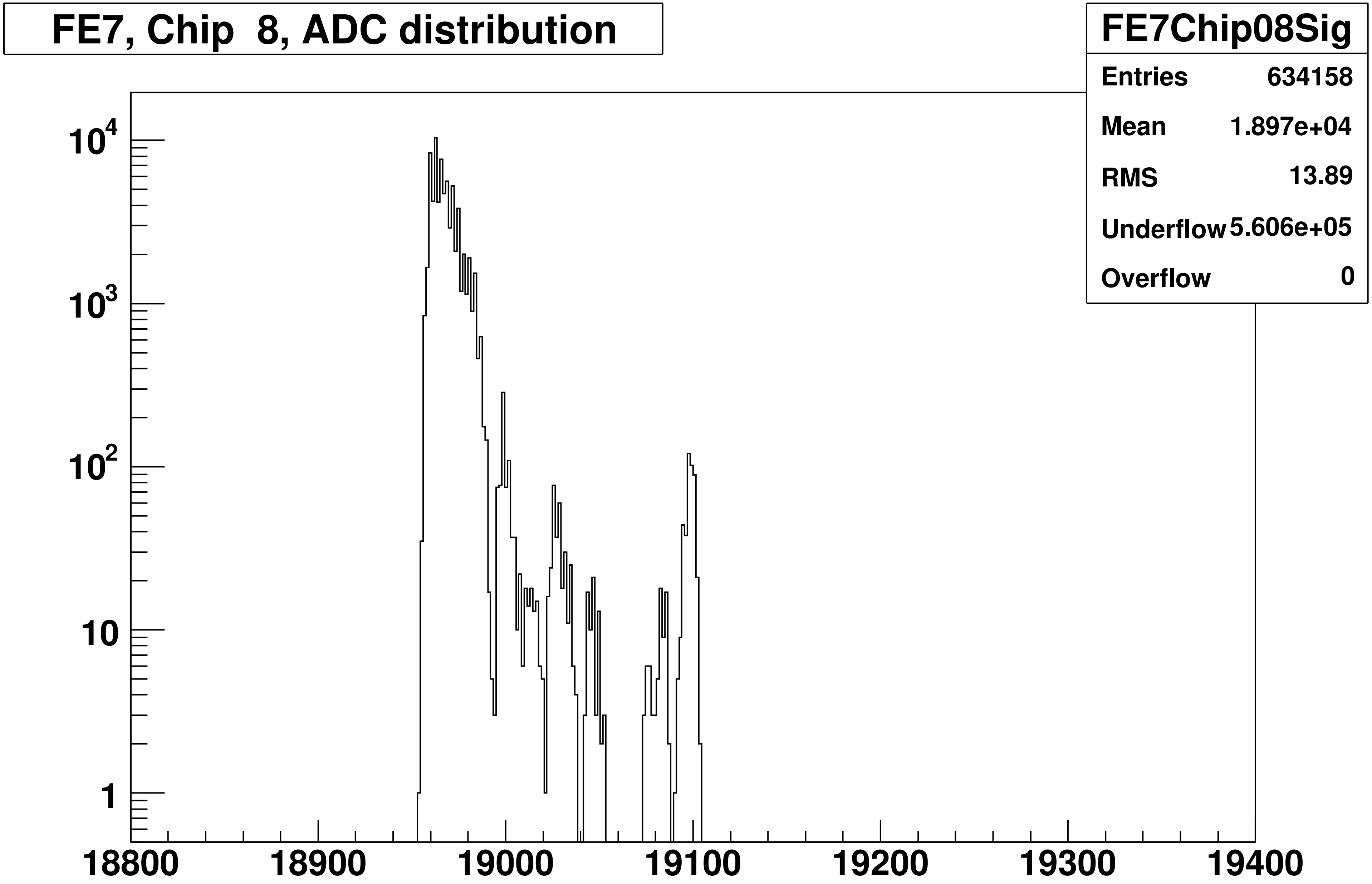
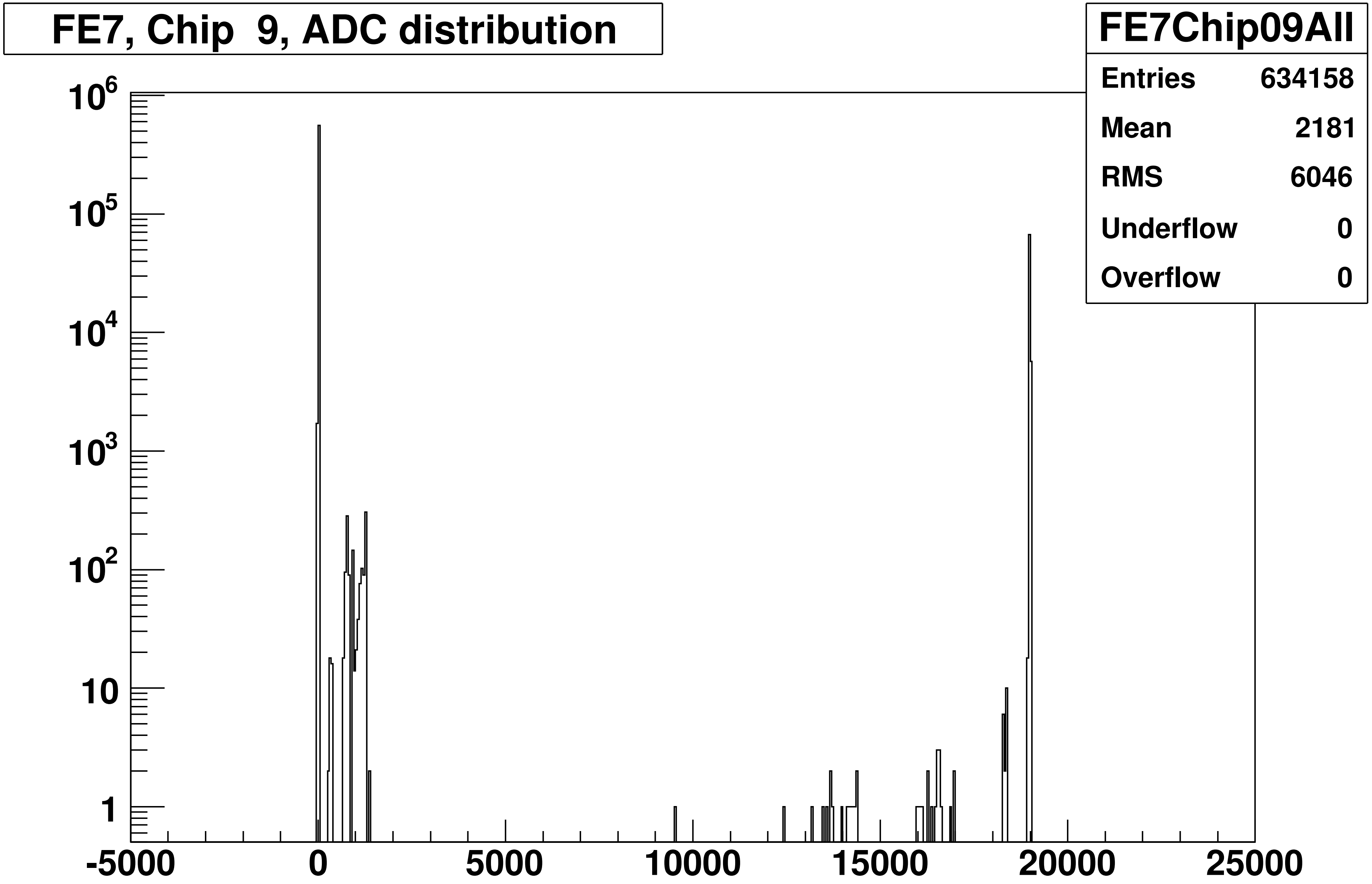
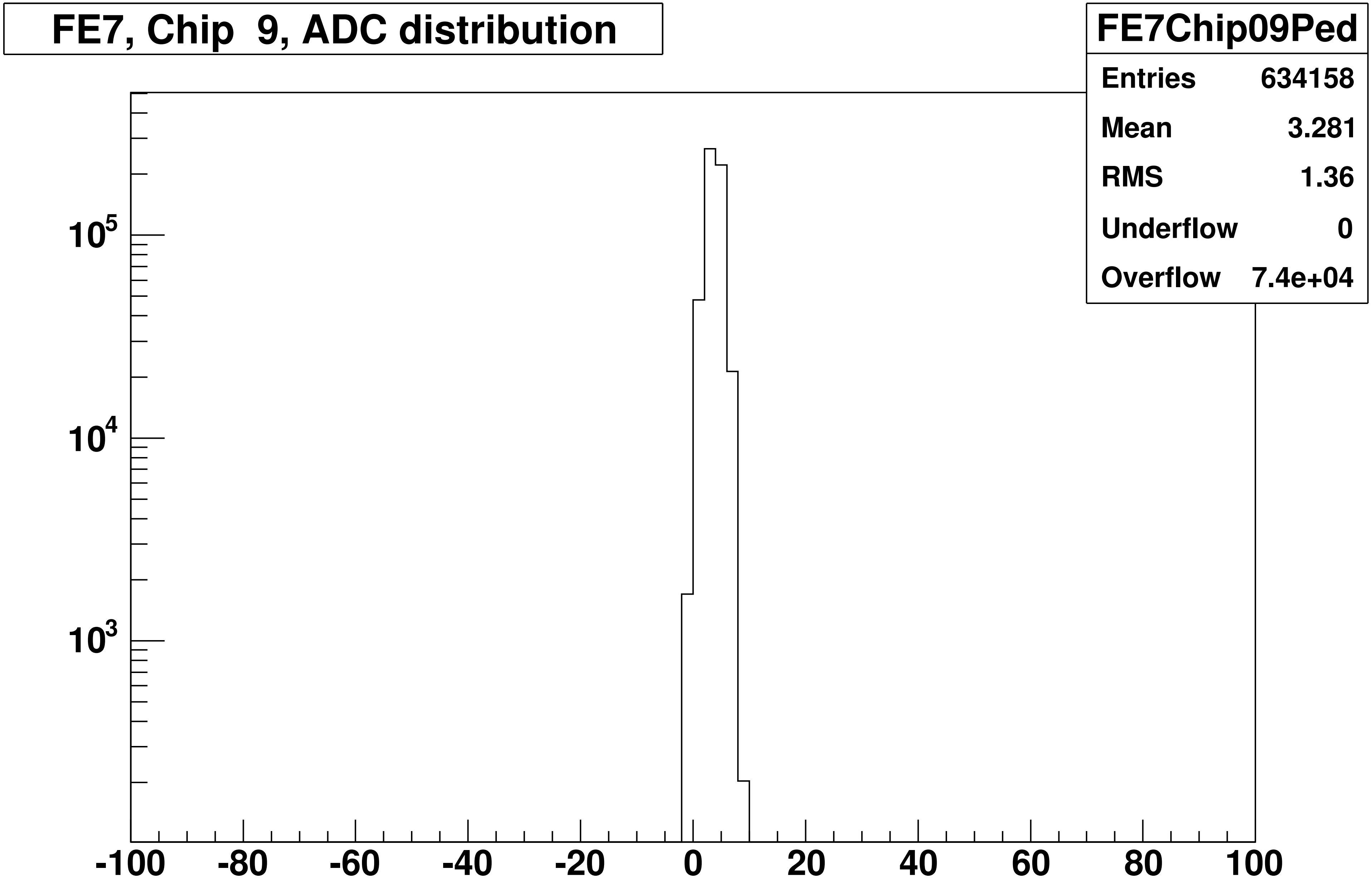


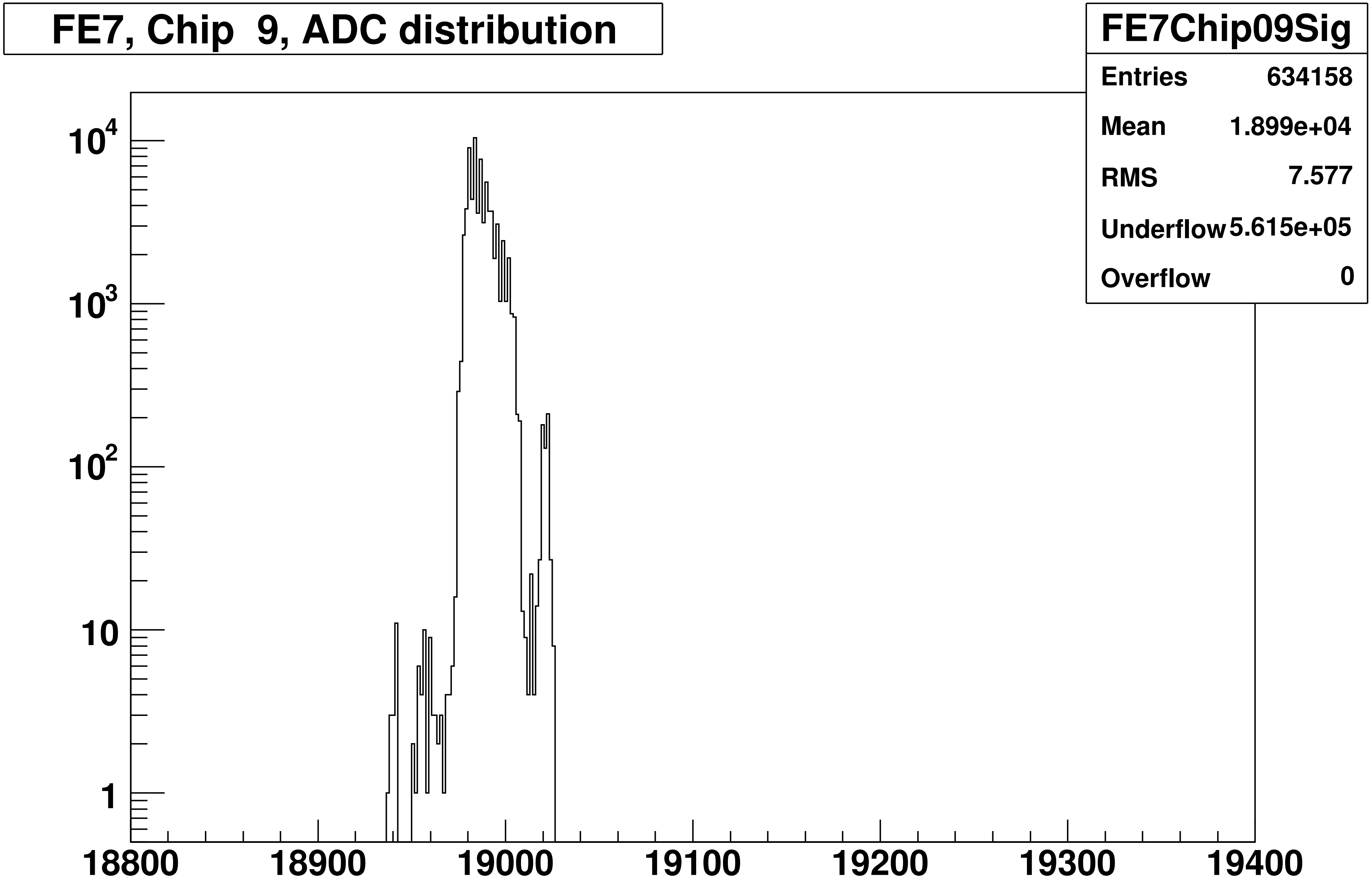
FE7, Chip 8, ADC distribution
FE7Chip08Ped
Entries 634158
Mean -43.3
RMS 1.319
Underflow 0
Overflow 7.4e+04
10^5
10^4
10^3
10^2
-100
-80
-60
-40
-20
0
20
40
60
80
100


FE7, Chip 8, ADC distribution
FE7Chip08Sig
Entries 634158
Mean 1.897e+04
RMS 13.89
Underflow 5.606e+05
Overflow 0
10^4
10^3
10^2
10
1
18800
18900
19000
19100
19200
19300
19400

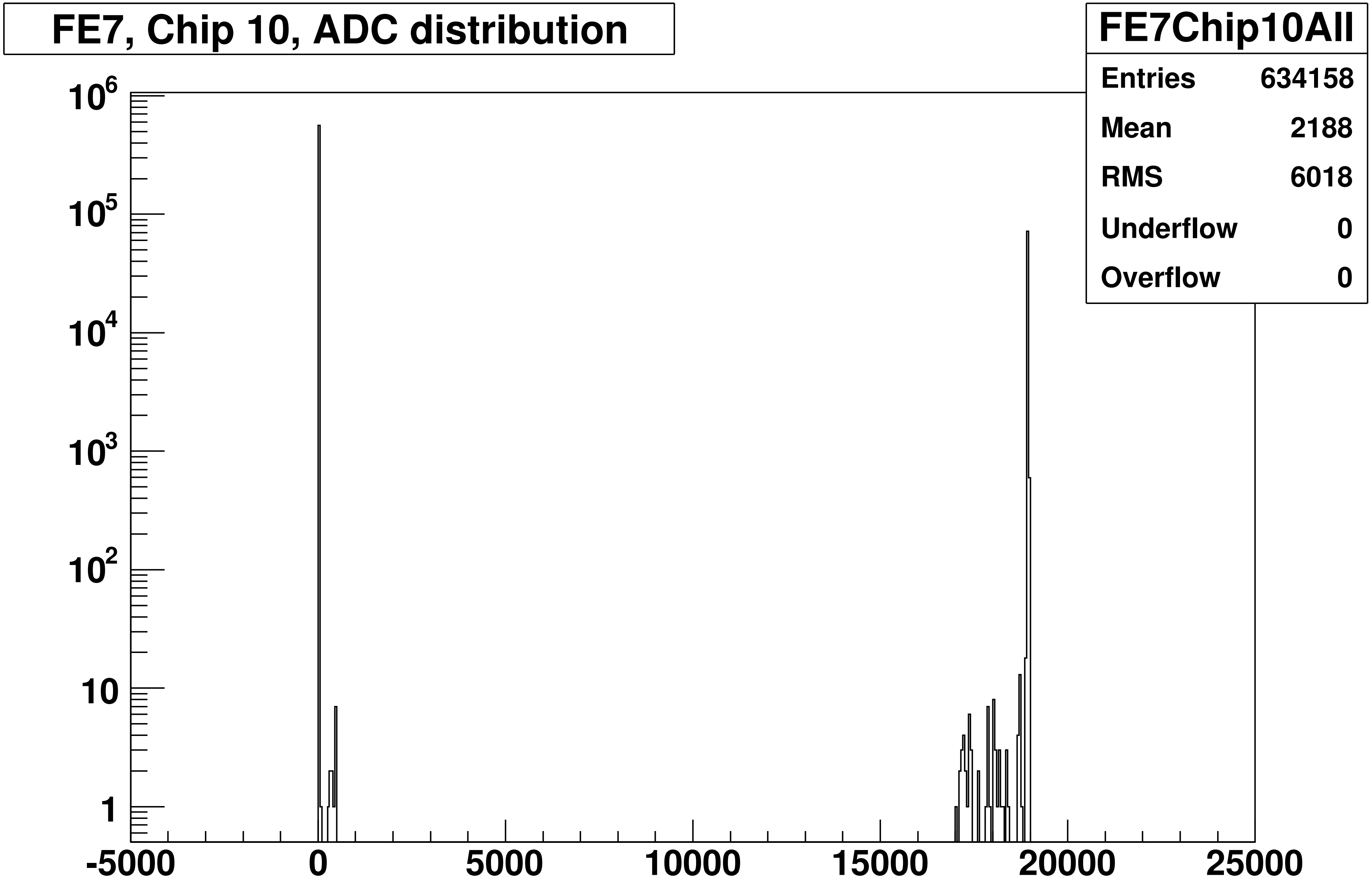


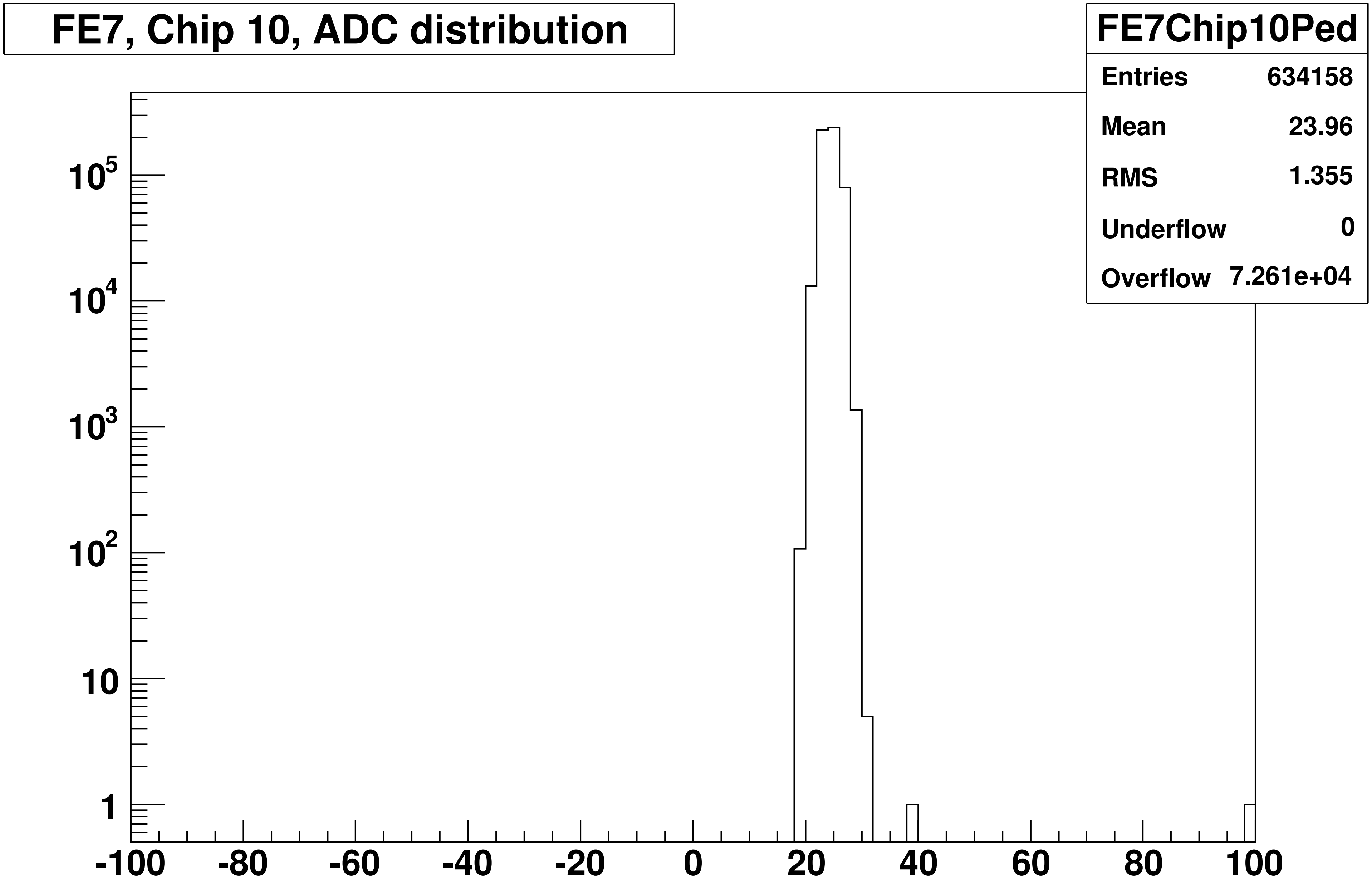
FE7, Chip 9, ADC distribution
FE7Chip09All
Entries 634158
Mean 2181
RMS 6046
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000

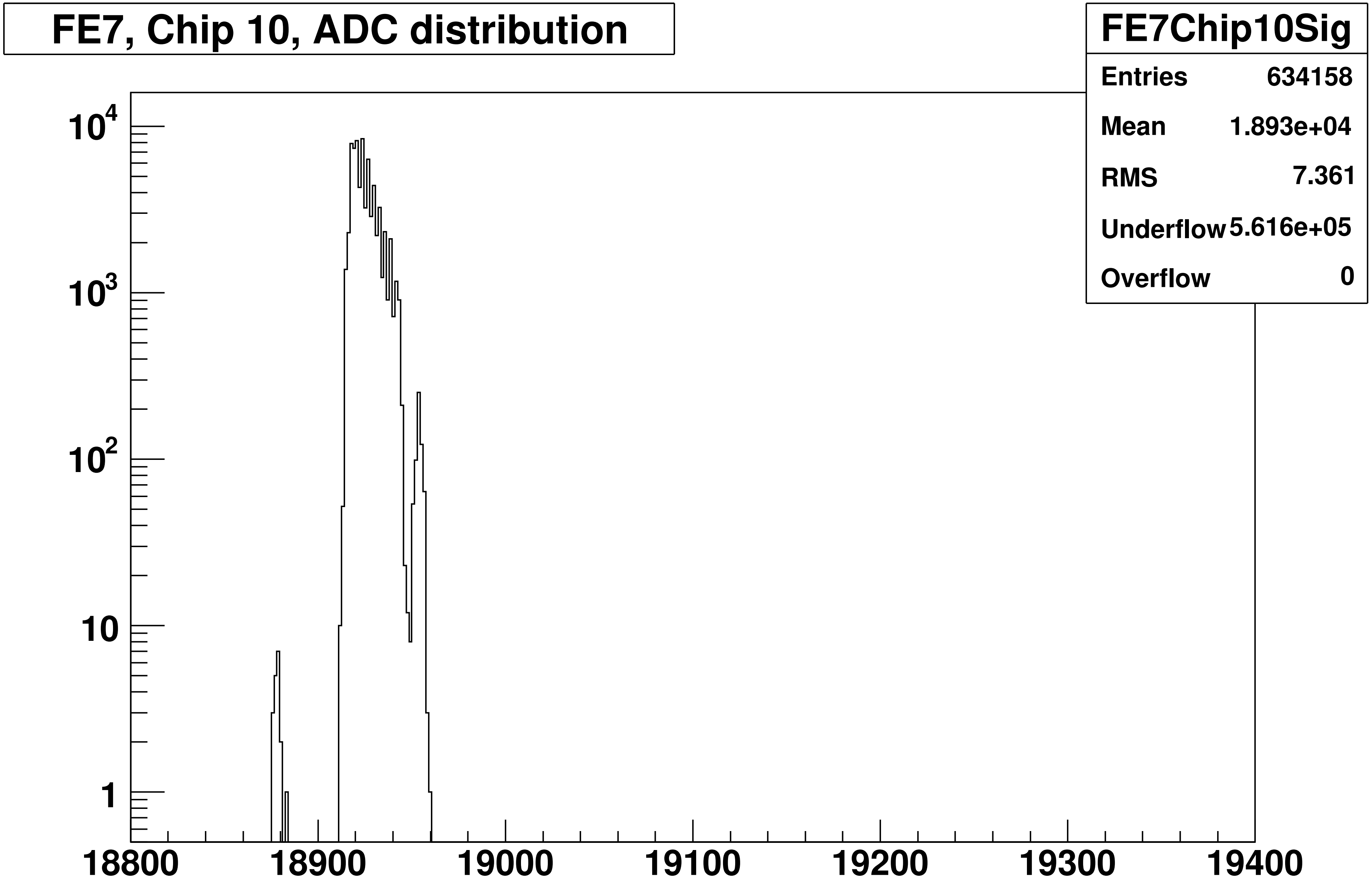

FE7, Chip 9, ADC distribution
FE7Chip09Ped
Entries 634158
Mean 3.281
RMS 1.36
Underflow 0
Overflow 7.4e+04
10^5
10^4
10^3
-100
-80
-60
-40
-20
0
20
40
60
80
100

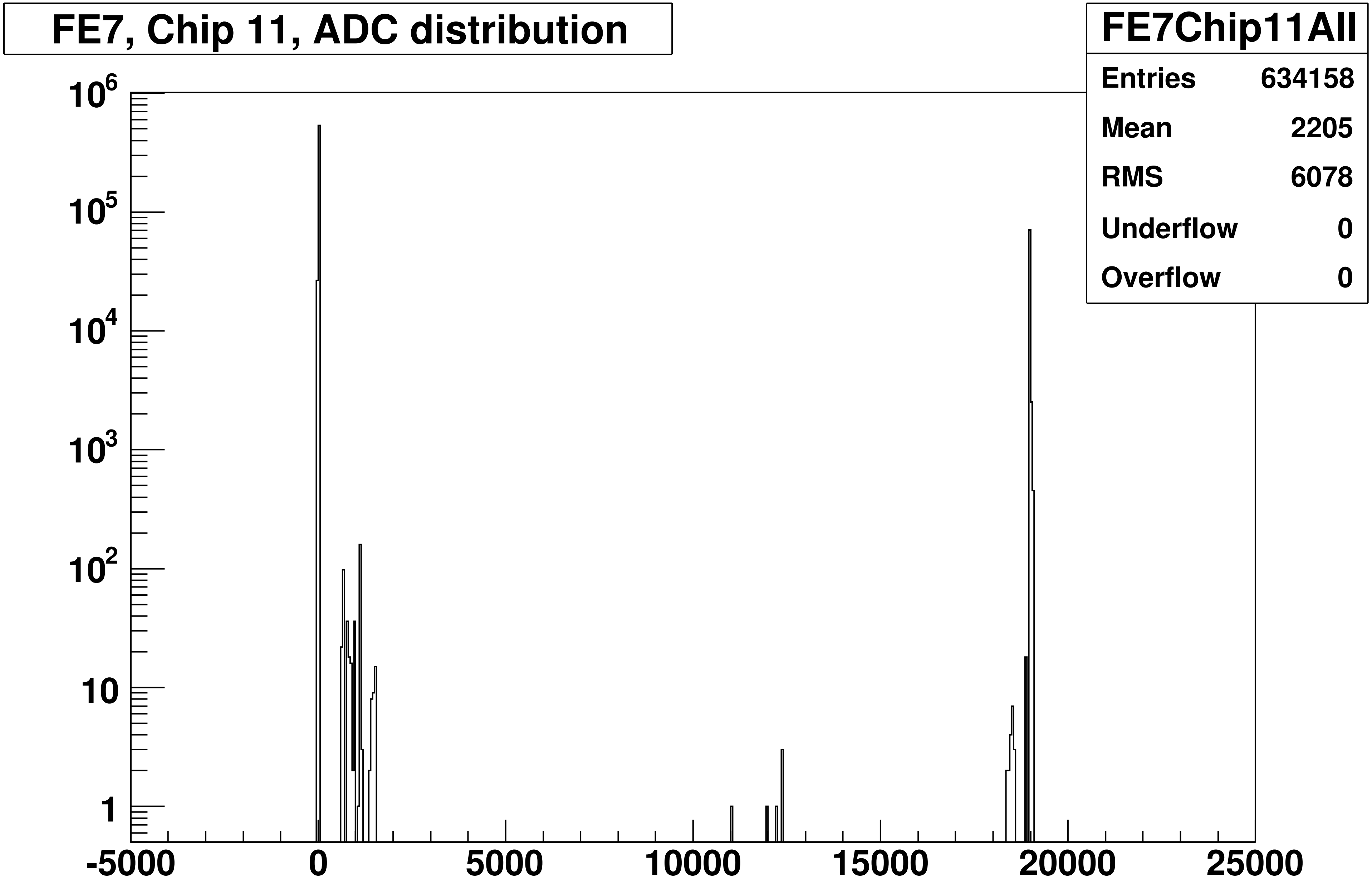


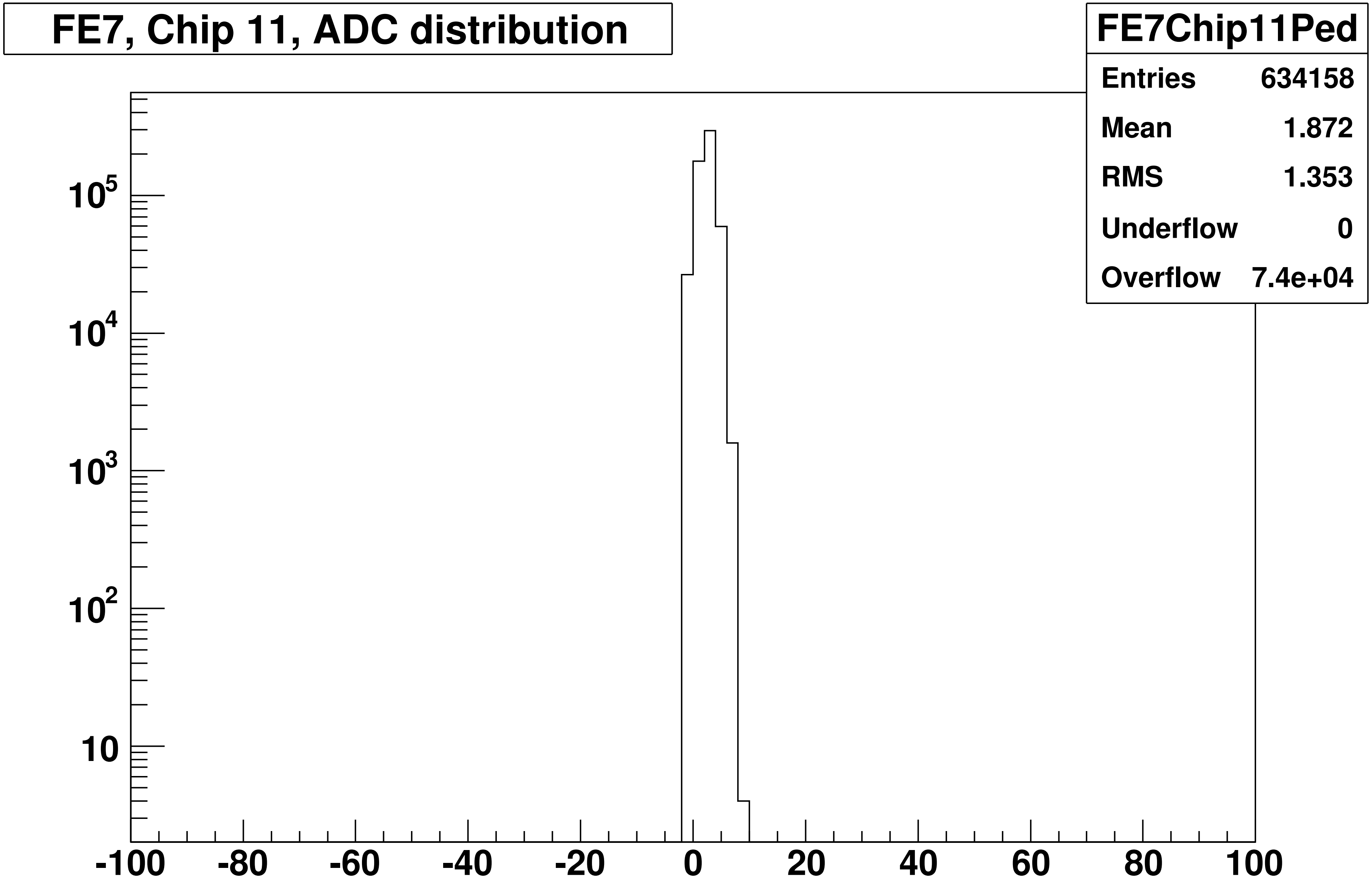
FE7, Chip 9, ADC distribution
FE7Chip09Sig
Entries 634158
Mean 1.899e+04
RMS 7.577
Underflow 5.615e+05
Overflow 0
10^4
10^3
10^2
10
1
18800
18900
19000
19100
19200
19300
19400

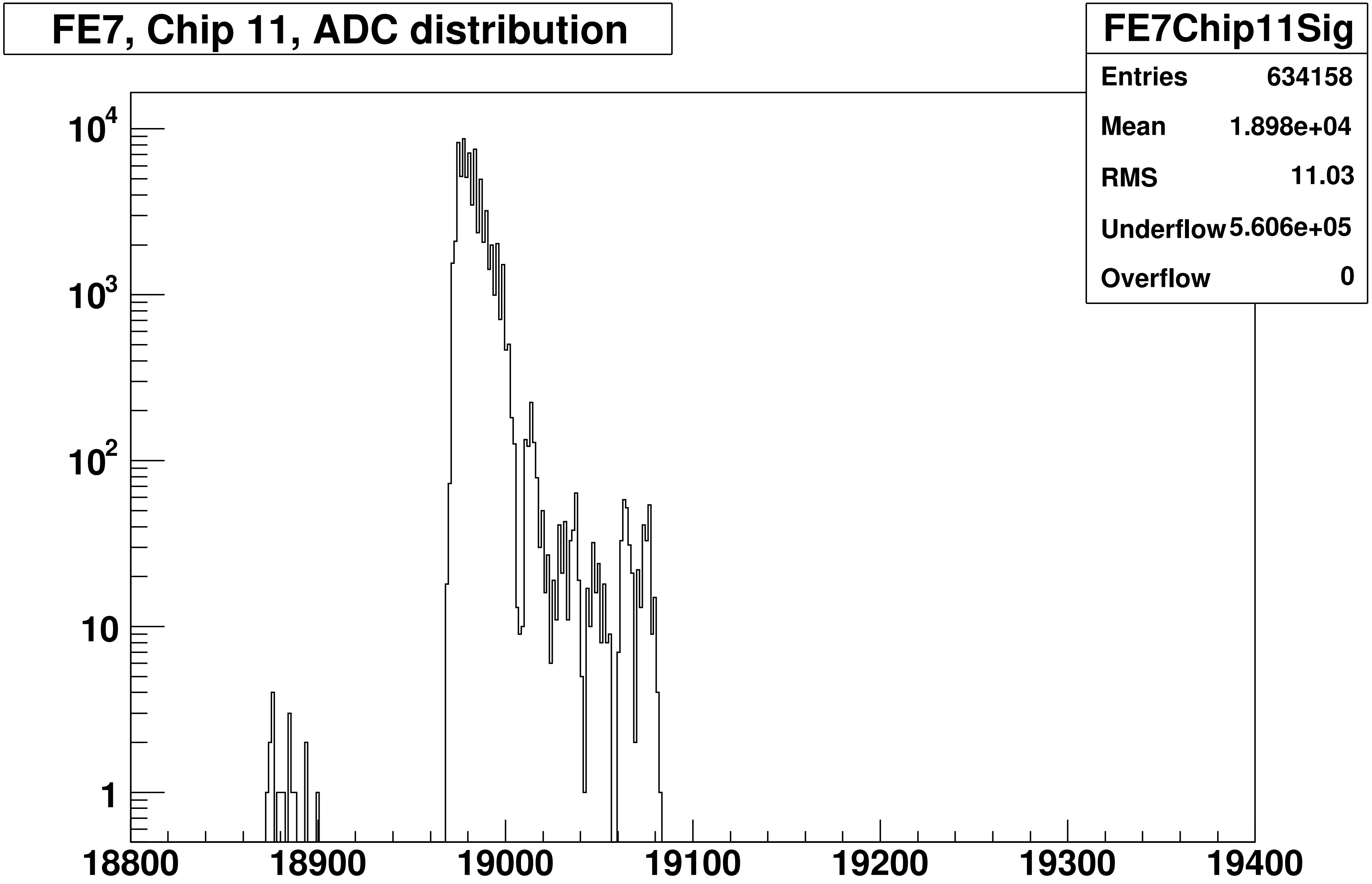

FE7, Chip 10, ADC distribution
FE7Chip10All
Entries 634158
Mean 2188
RMS 6018
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000

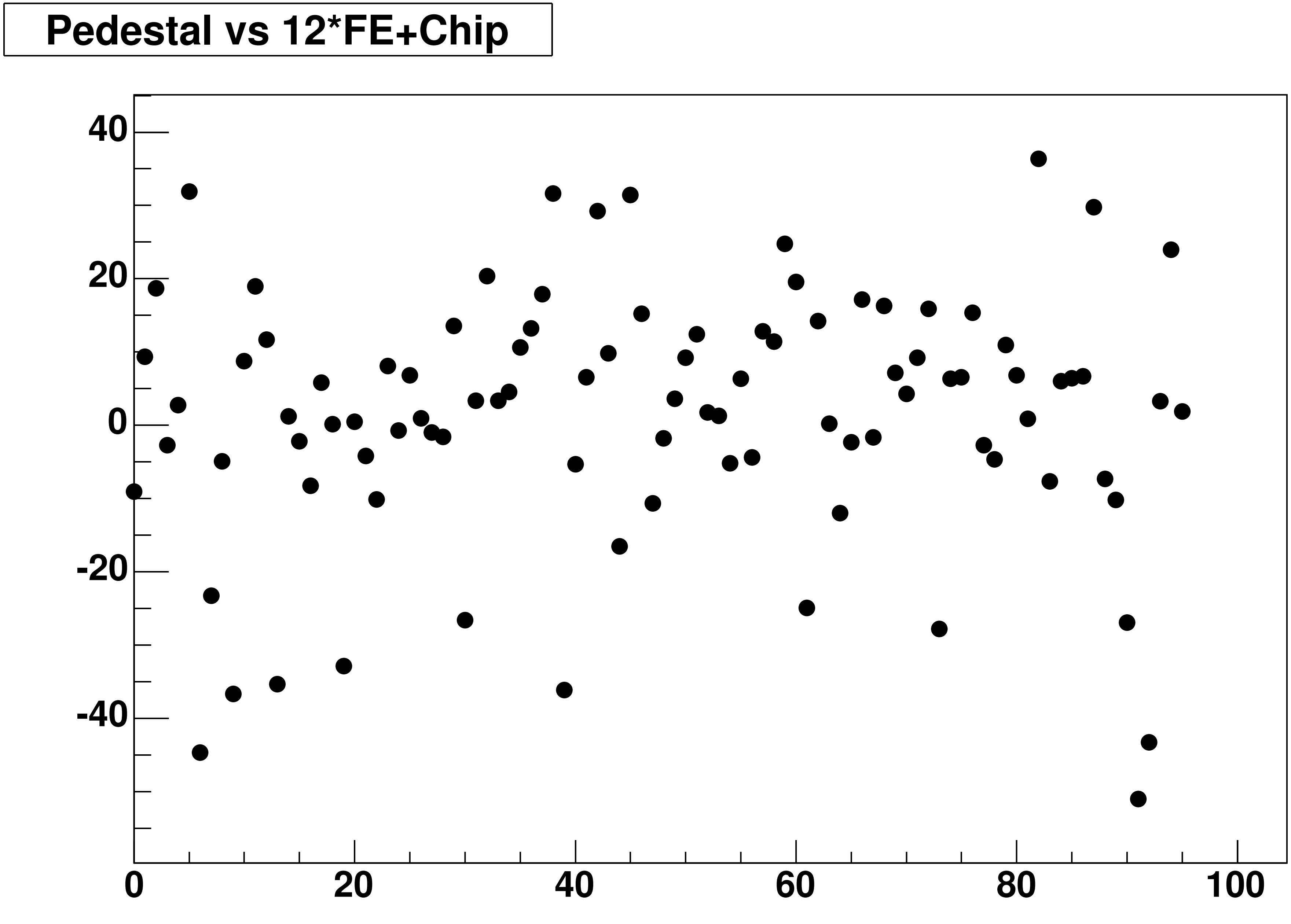

FE7, Chip 10, ADC distribution
FE7Chip10Ped
Entries 634158
Mean 23.96
RMS 1.355
Underflow 0
Overflow 7.261e+04
10^5
10^4
10^3
10^2
10
1
-100
-80
-60
-40
-20
0
20
40
60
80
100


FE7, Chip 10, ADC distribution
FE7Chip10Sig
Entries 634158
Mean 1.893e+04
RMS 7.361
Underflow 5.616e+05
Overflow 0
10^4
10^3
10^2
10
1
18800
18900
19000
19100
19200
19300
19400

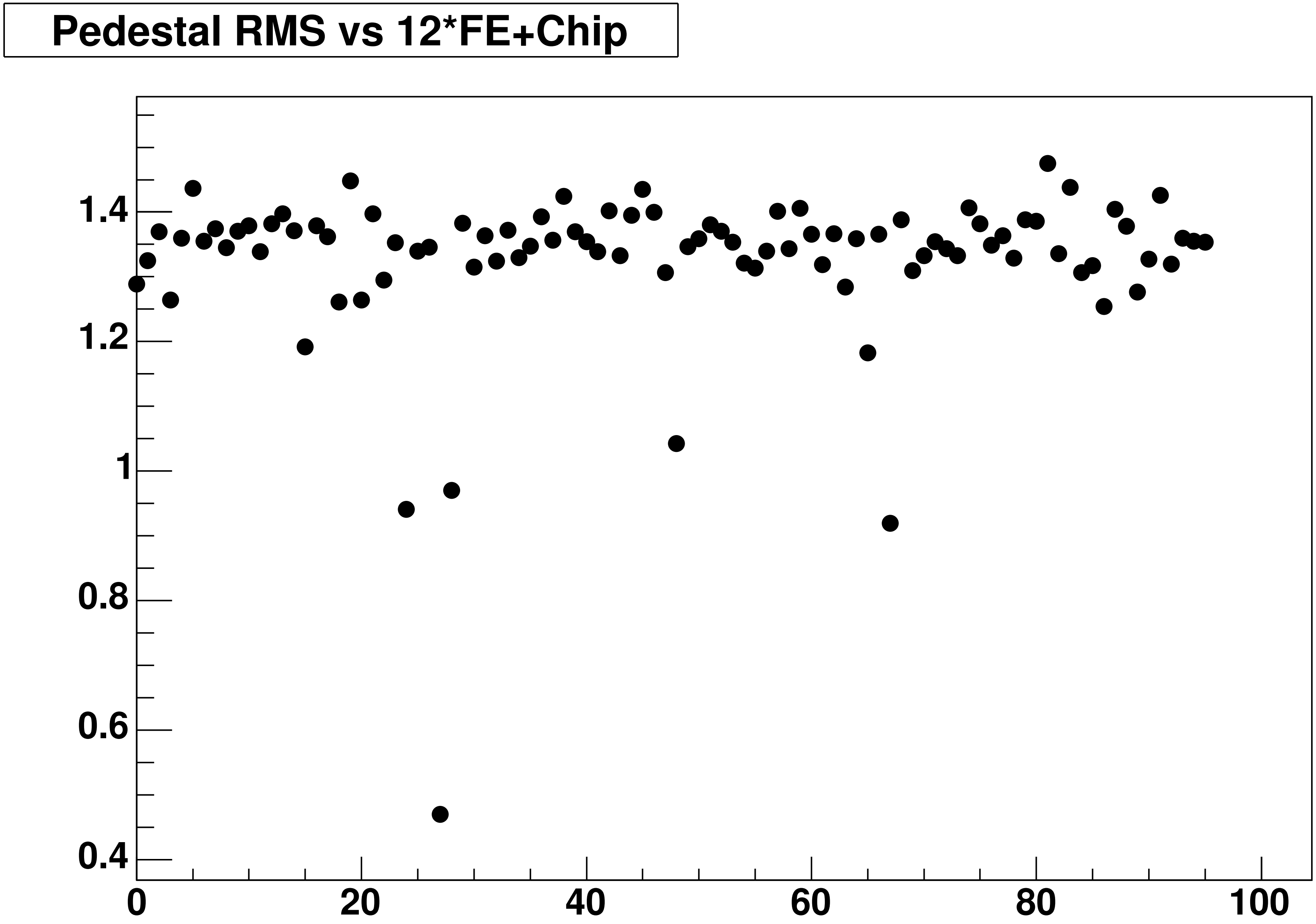

FE7, Chip 11, ADC distribution
FE7Chip11All
Entries 634158
Mean 2205
RMS 6078
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE7, Chip 11, ADC distribution
FE7Chip11Ped
Entries 634158
Mean 1.872
RMS 1.353
Underflow 0
Overflow 7.4e+04
10^5
10^4
10^3
10^2
10
-100 -80 -60 -40 -20 0 20 40 60 80 100

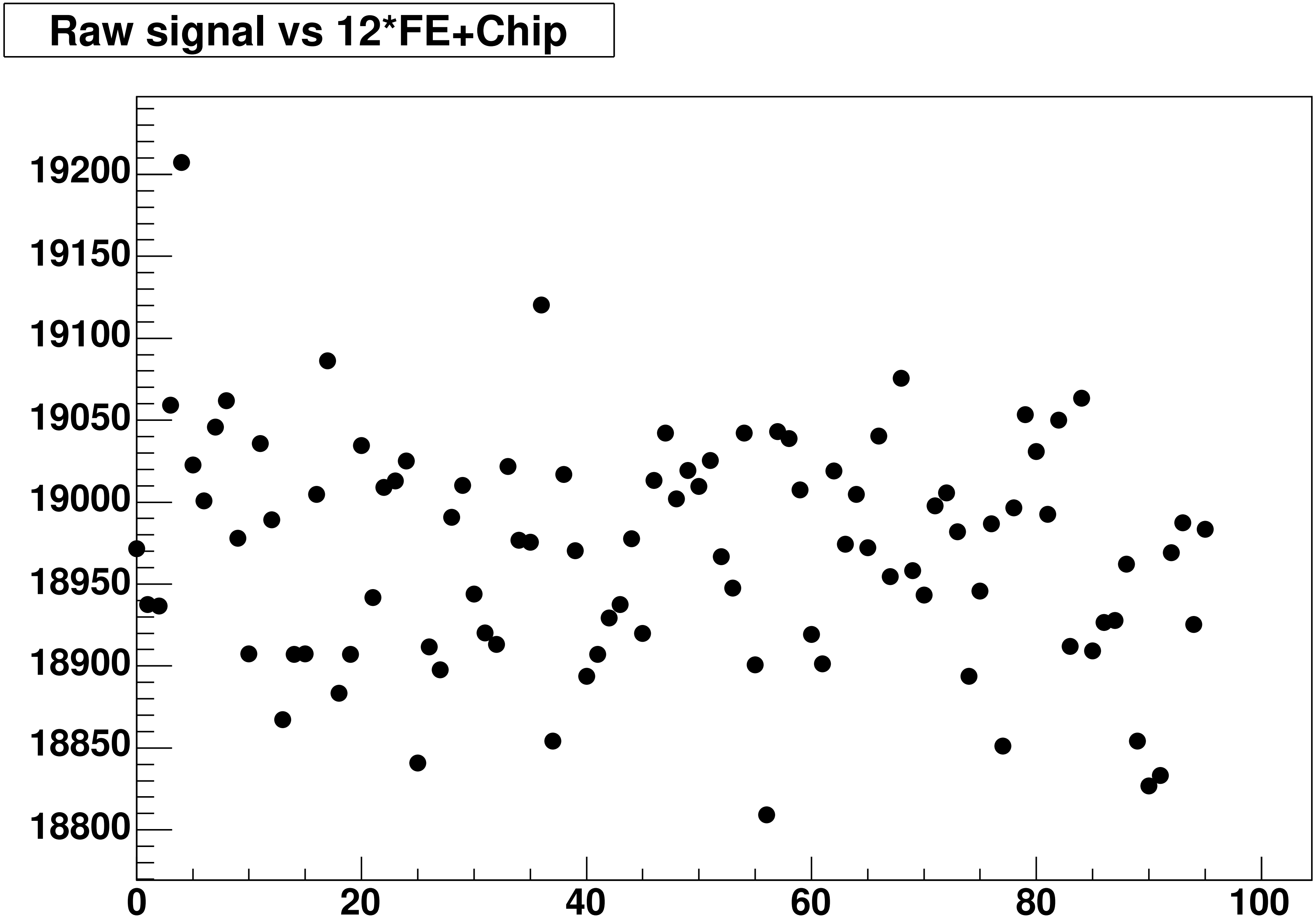

FE7, Chip 11, ADC distribution
FE7Chip11Sig
Entries 634158
Mean 1.898e+04
RMS 11.03
Underflow 5.606e+05
Overflow 0
10^4
10^3
10^2
10
1
18800
18900
19000
19100
19200
19300
19400

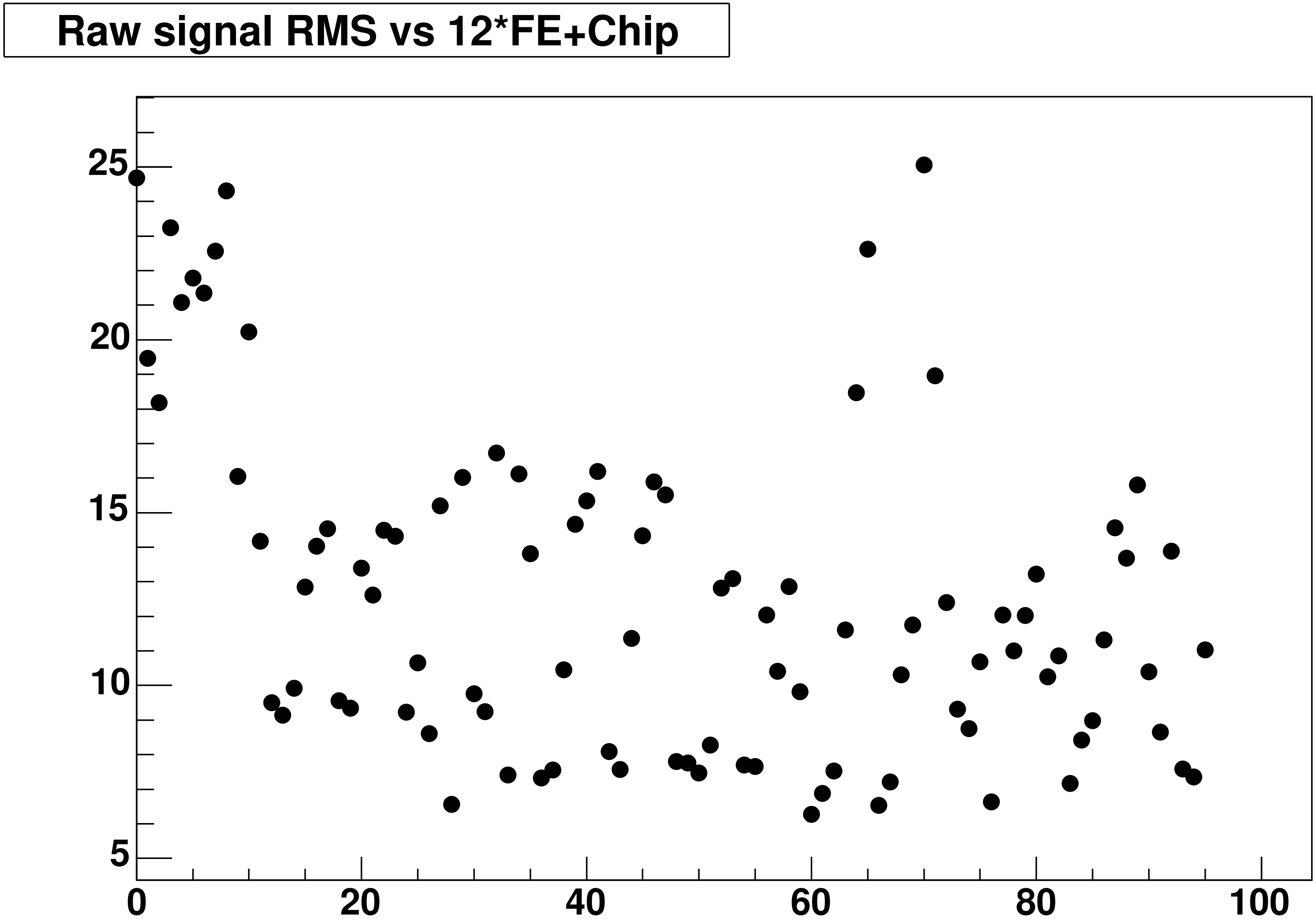


Pedestal vs 12*FE+Chip
40
20
0
-20
-40
0
20
40
60
80
100

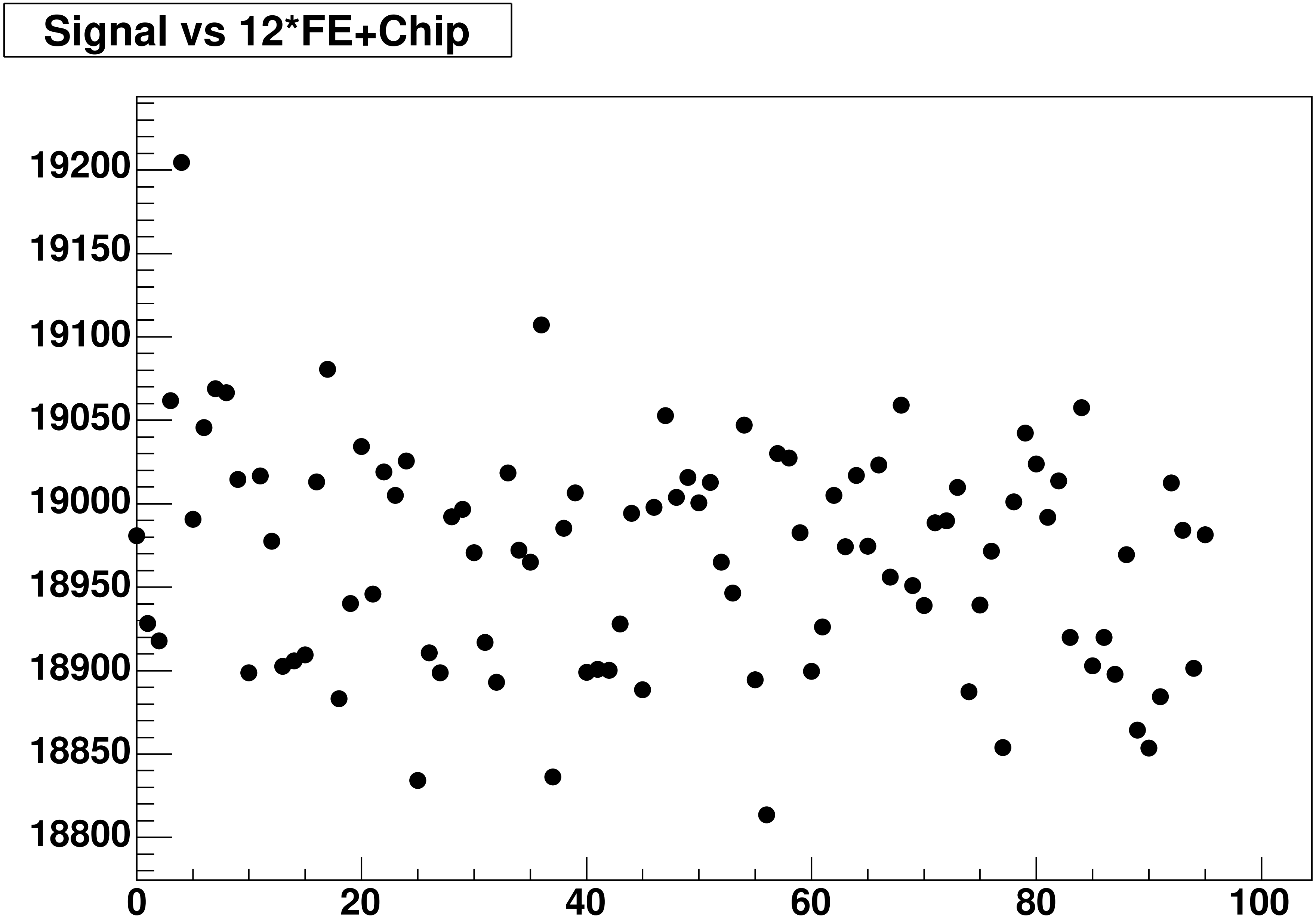


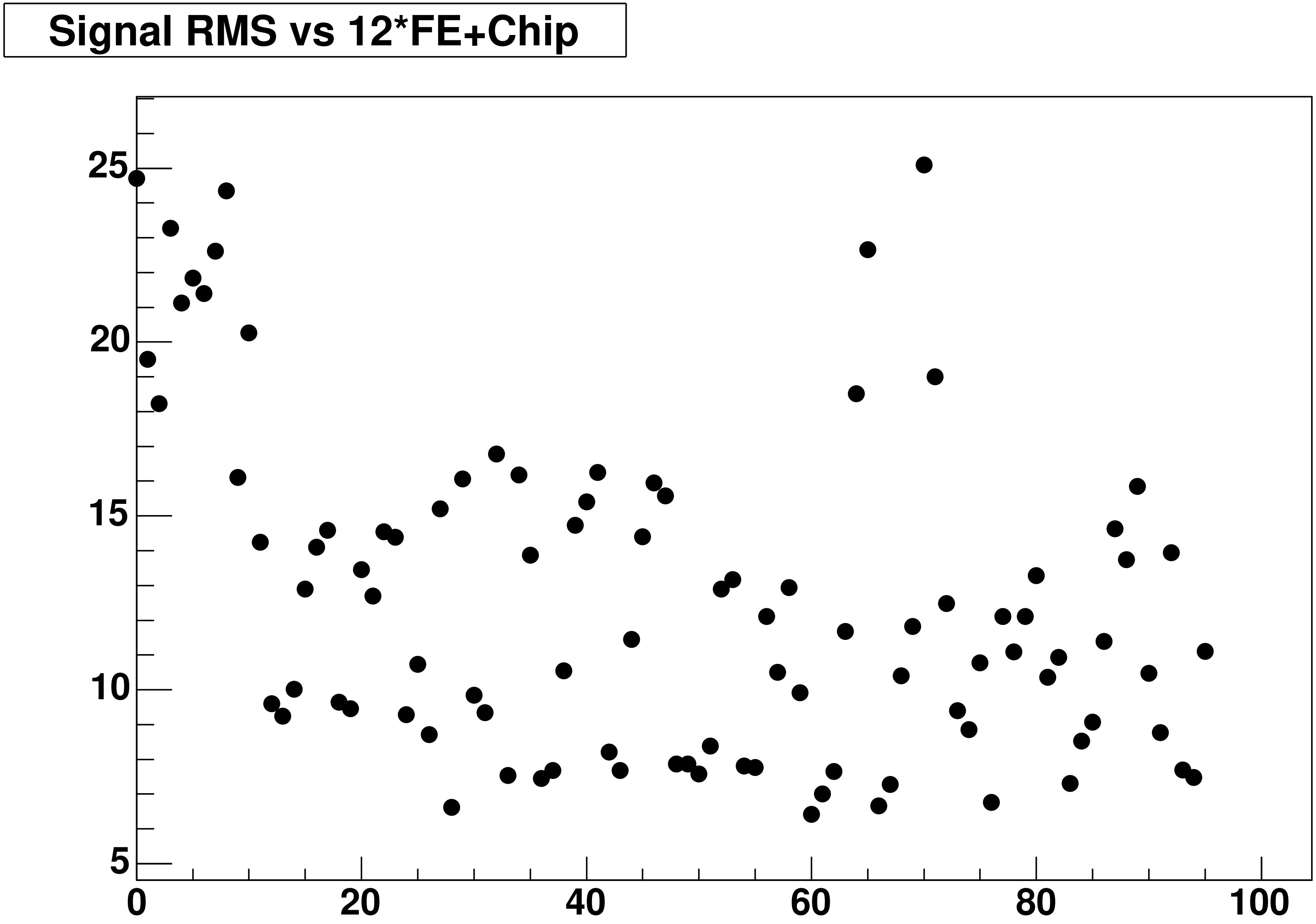
Pedestal RMS vs 12*FE+Chip
1.4
1.2
1
0.8
0.6
0.4
0
20
40
60
80
100


Raw signal vs 12*FE+Chip
19200
19150
19100
19050
19000
18950
18900
18850
18800
0
20
40
60
80
100



Raw signal RMS vs 12*FE+Chip
25
20
15
10
5
0
20
40
60
80
100


Signal vs 12*FE+Chip
19200
19150
19100
19050
19000
18950
18900
18850
18800
0
20
40
60
80
100


Signal RMS vs 12*FE+Chip
5
10
15
20
25
0
20
40
60
80
100