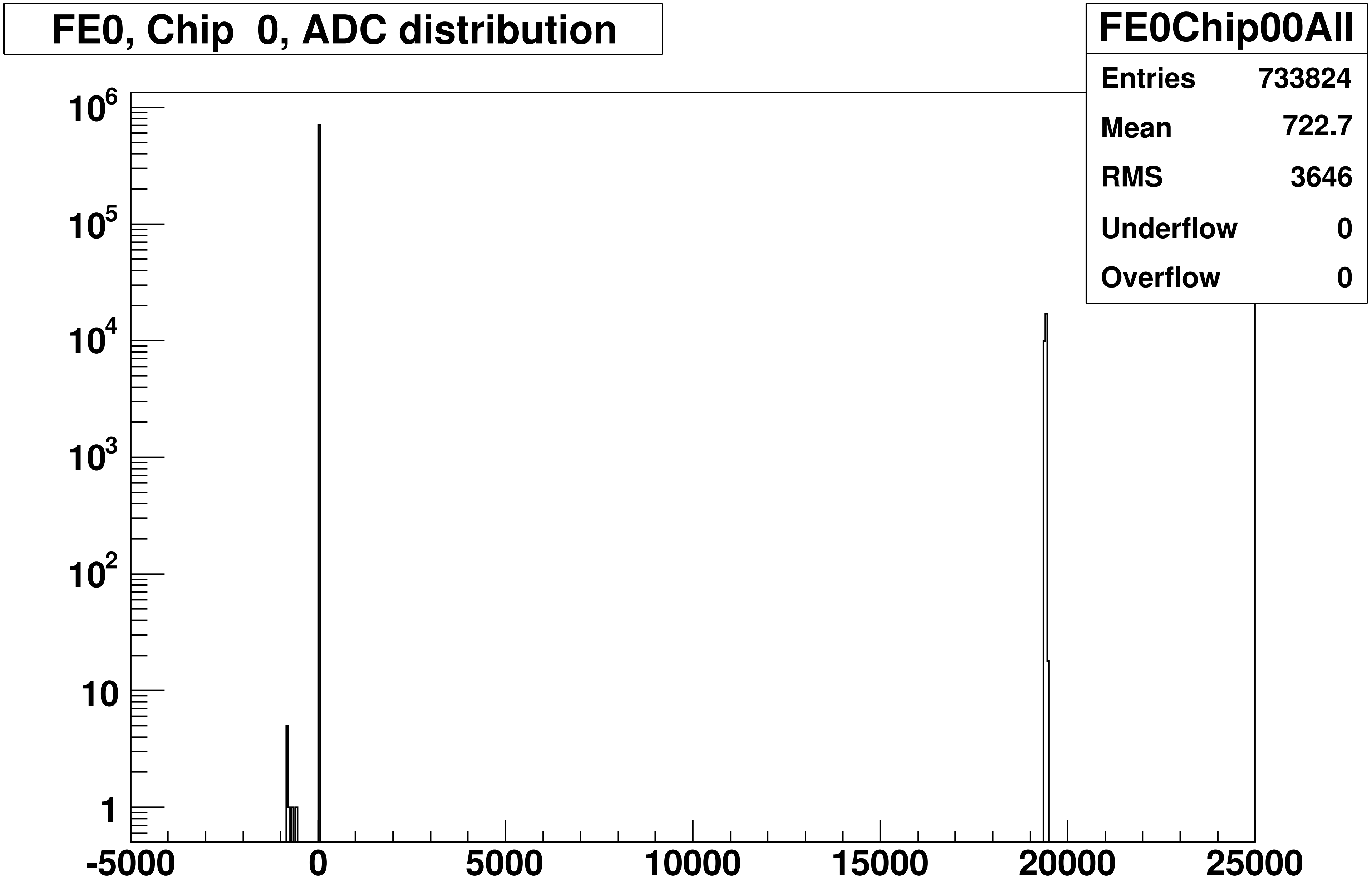

FE0, Chip 0, ADC distribution
FE0Chip00All
Entries 733824
Mean 722.7
RMS 3646
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
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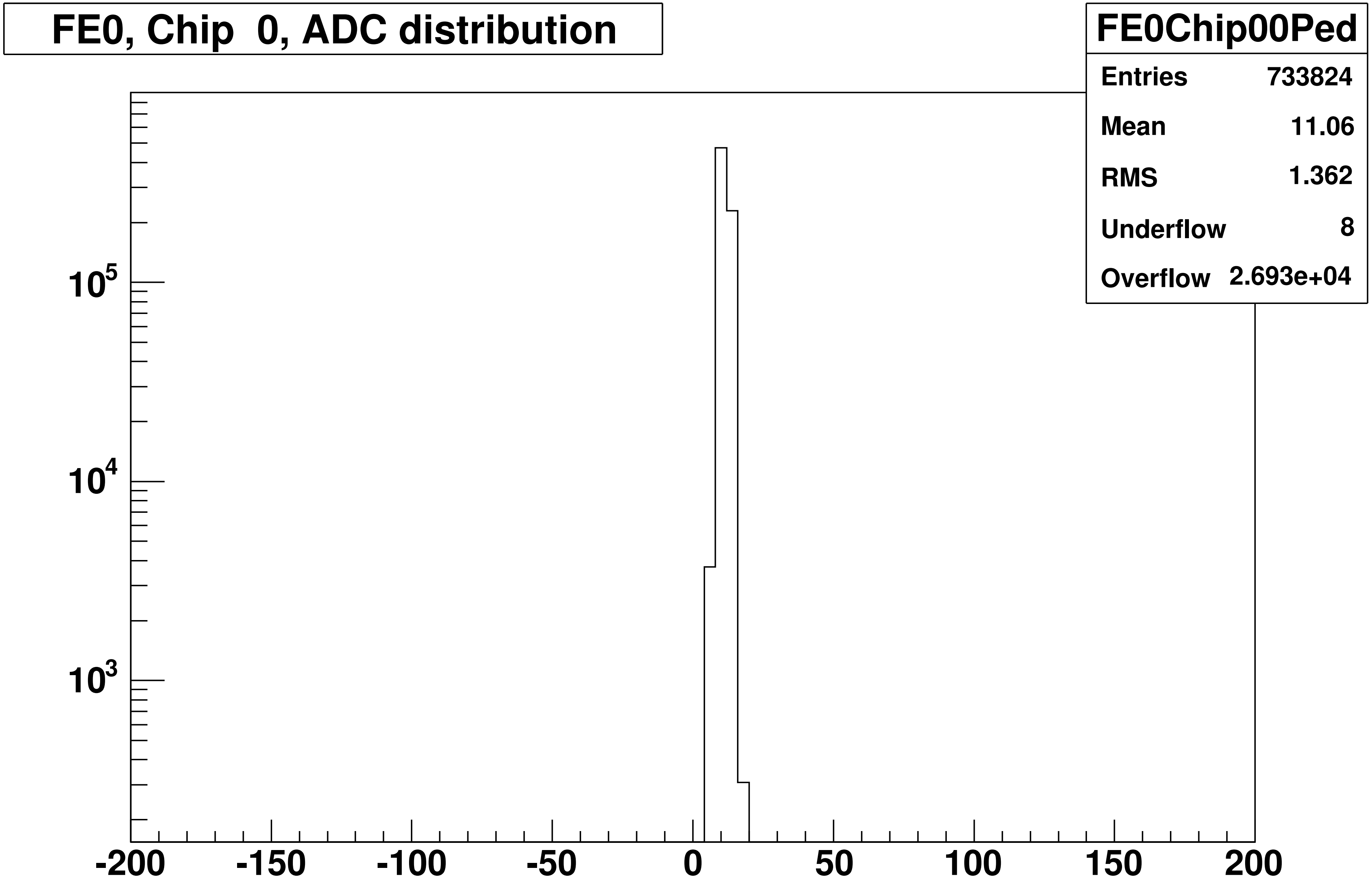
FE0, Chip 0, ADC distribution
FE0Chip00Ped
Entries 733824
Mean 11.06
RMS 1.362
Underflow 8
Overflow 2.693e+04
10^5
10^4
10^3
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-100
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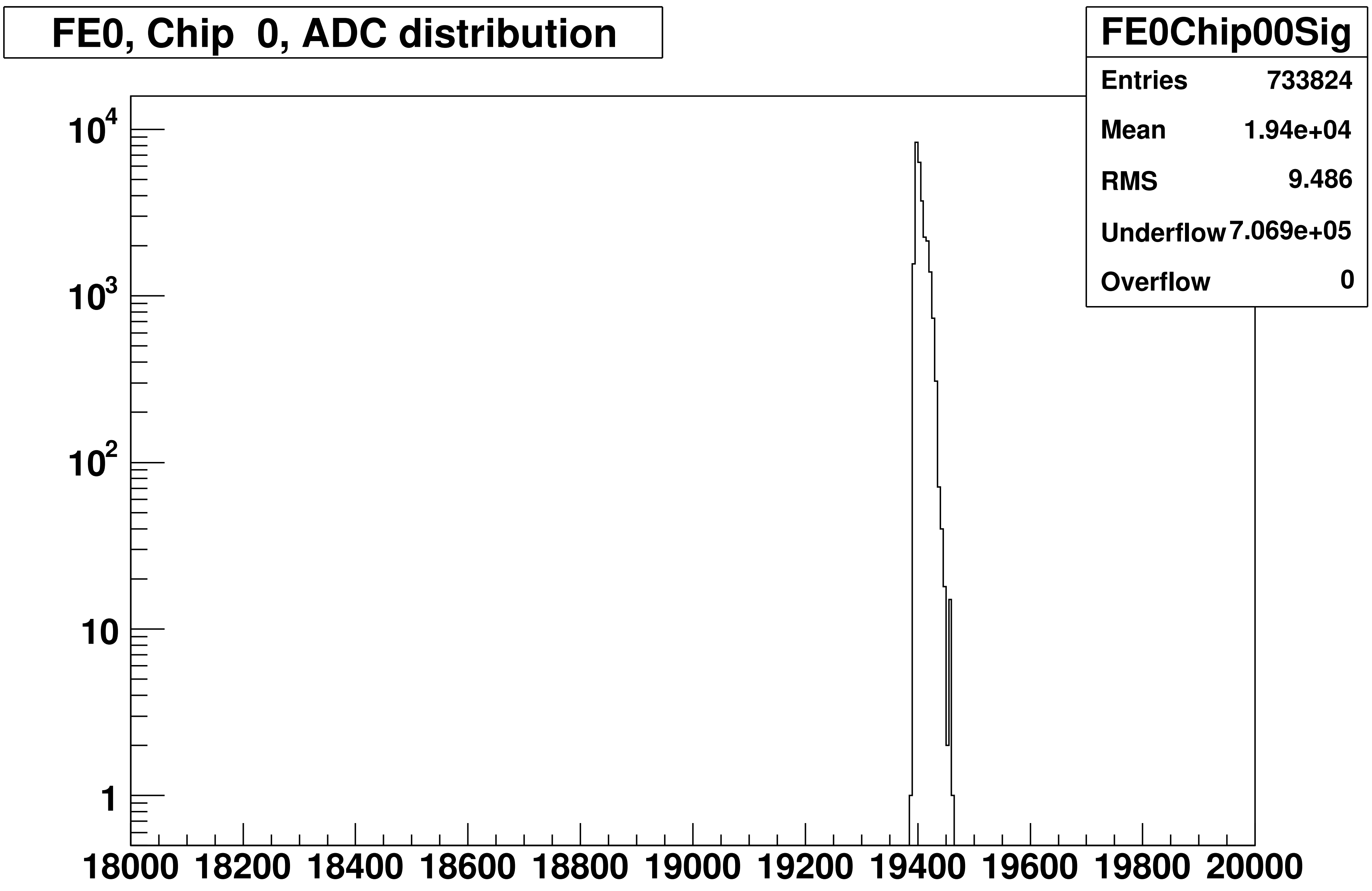

FE0, Chip 0, ADC distribution
FE0Chip00Sig
Entries 733824
Mean 1.94e+04
RMS 9.486
Underflow 7.069e+05
Overflow 0
10^4
10^3
10^2
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1
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18400
18600
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19000
19200
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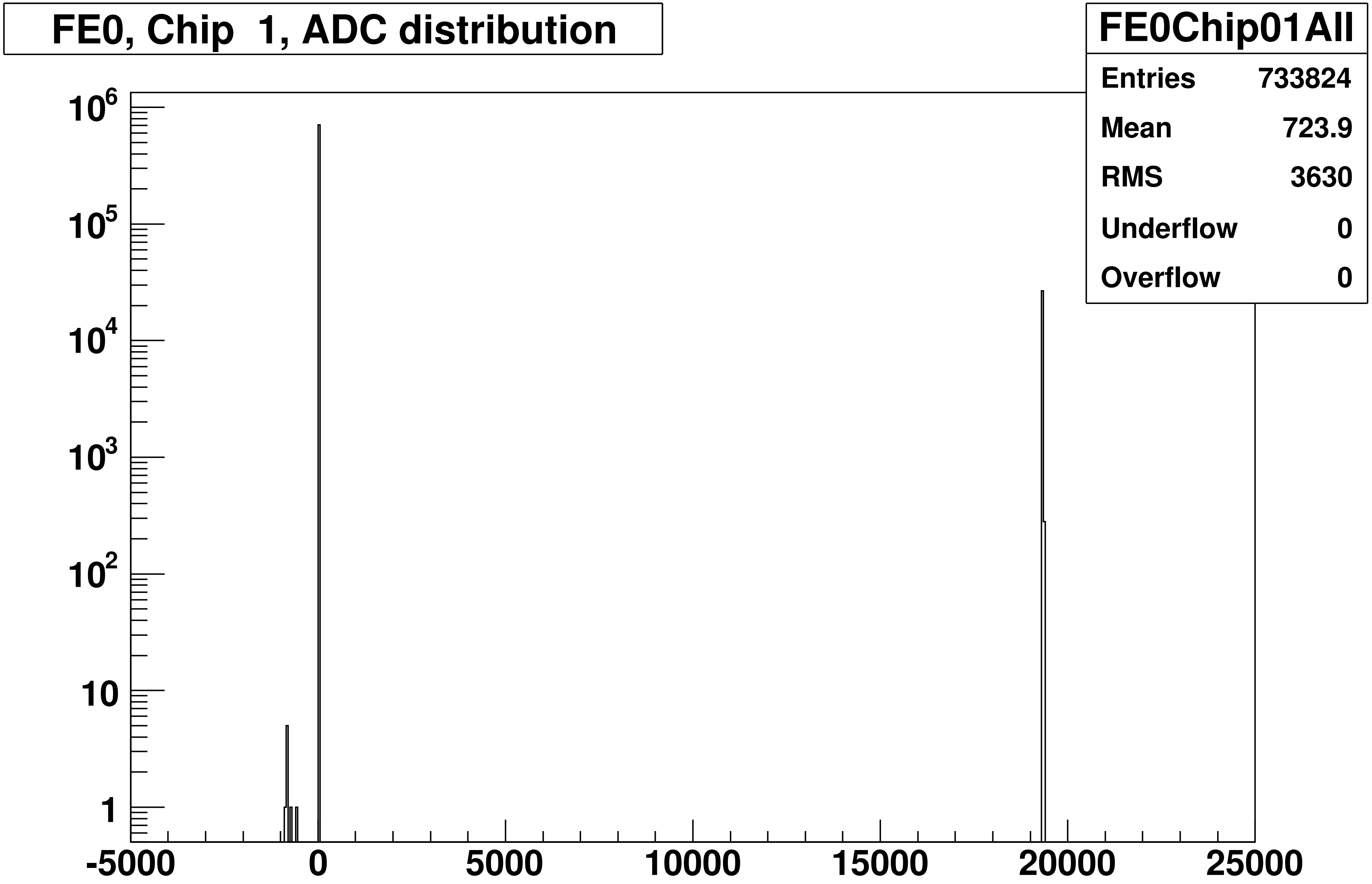
20000



FE0, Chip 1, ADC distribution
FE0Chip01All
Entries 733824
Mean 723.9
RMS 3630
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
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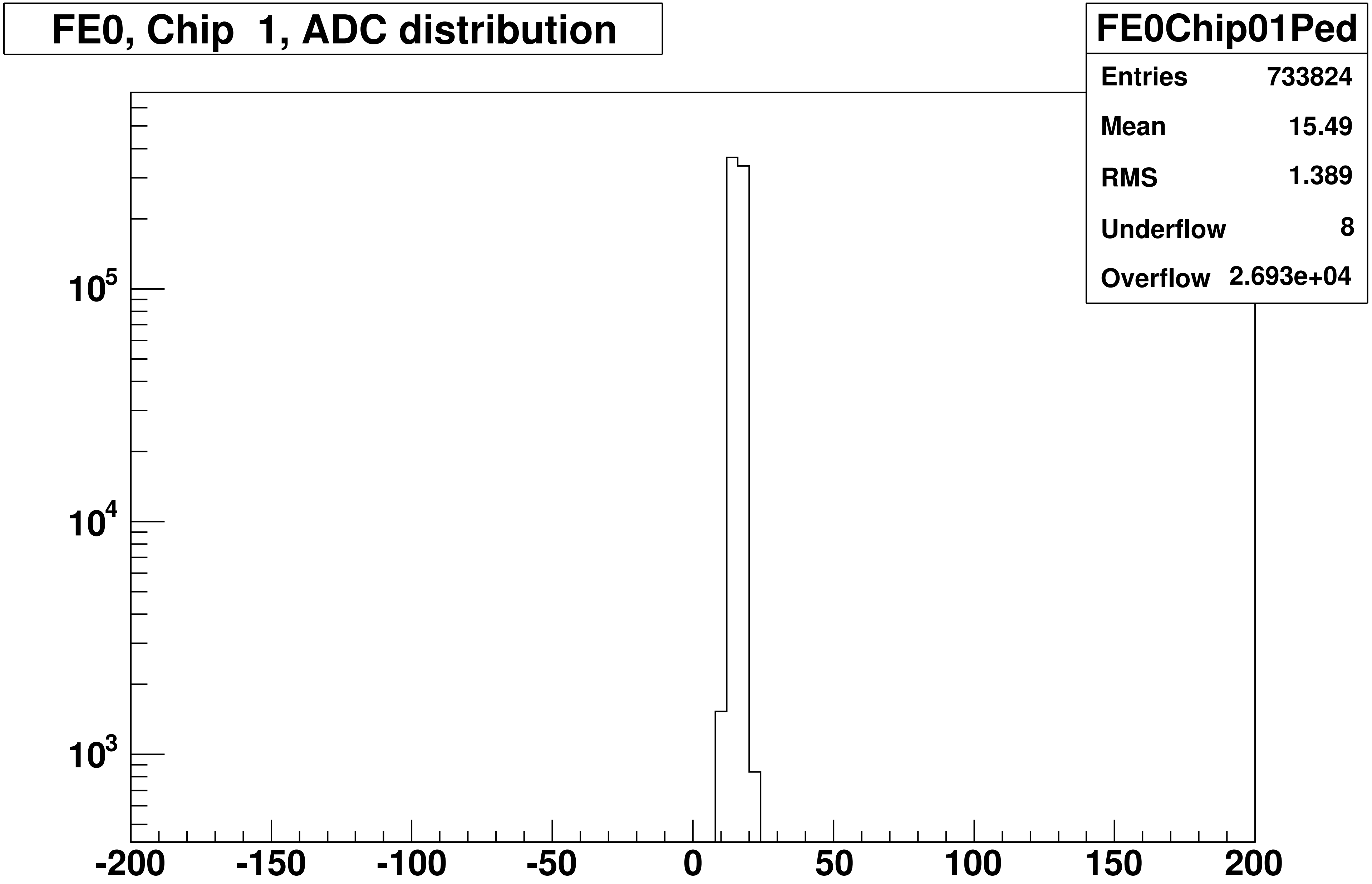
FE0, Chip 1, ADC distribution
FE0Chip01Ped
Entries 733824
Mean 15.49
RMS 1.389
Underflow 8
Overflow 2.693e+04
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10^4
10^3
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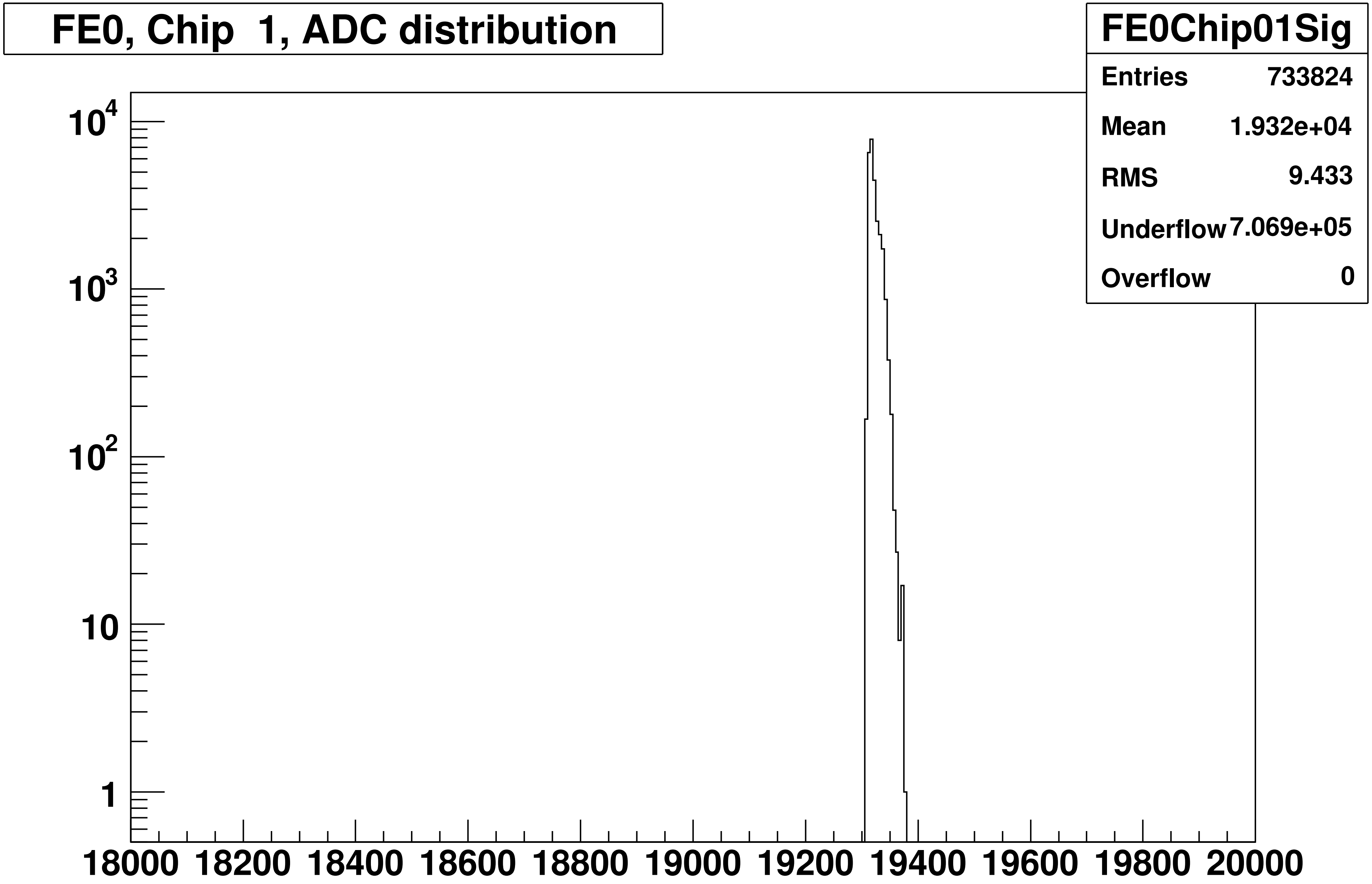

FE0, Chip 1, ADC distribution
FE0Chip01Sig
Entries 733824
Mean 1.932e+04
RMS 9.433
Underflow 7.069e+05
Overflow 0
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10^3
10^2
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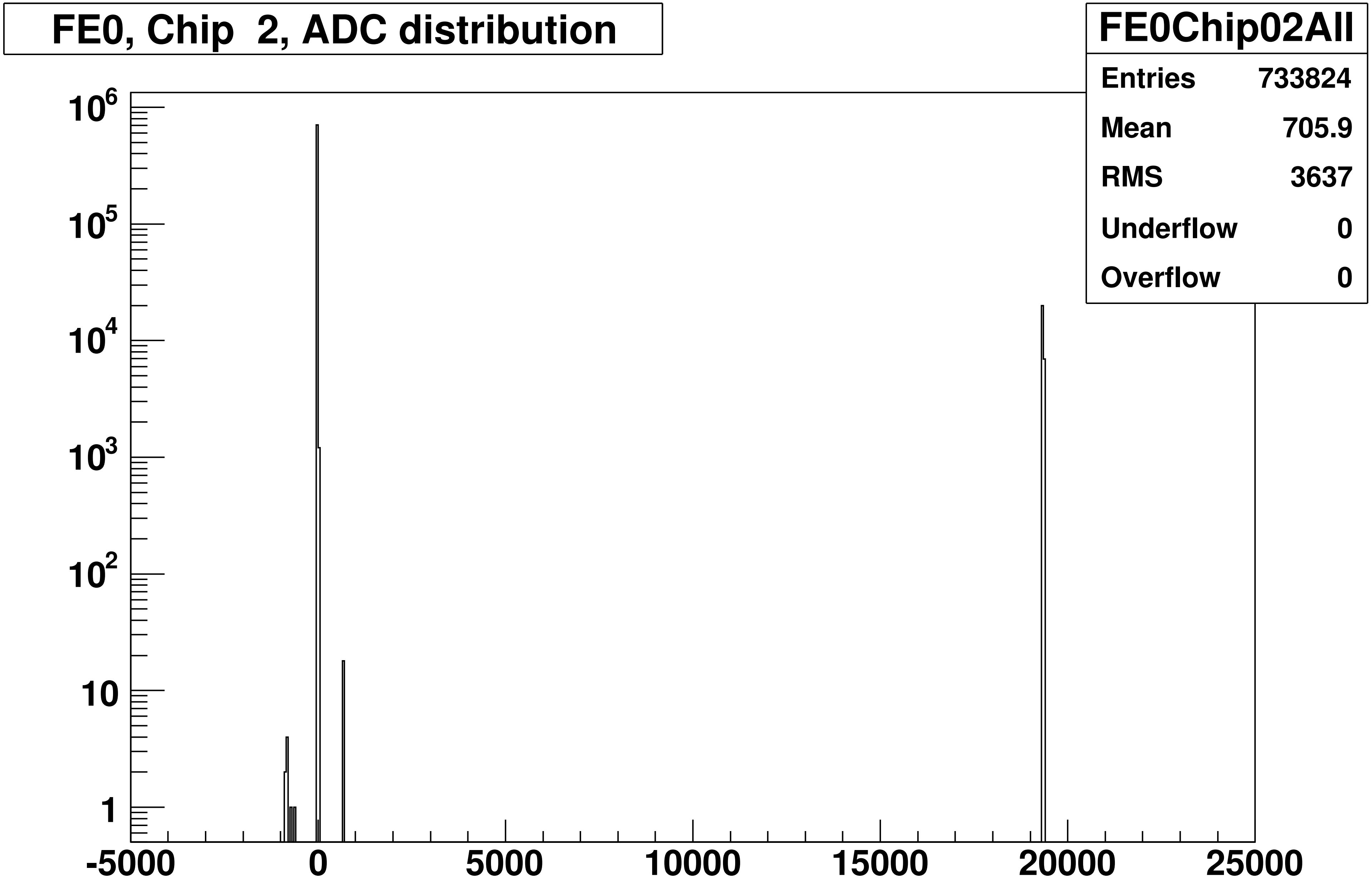

FE0, Chip 2, ADC distribution
FE0Chip02All
Entries 733824
Mean 705.9
RMS 3637
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
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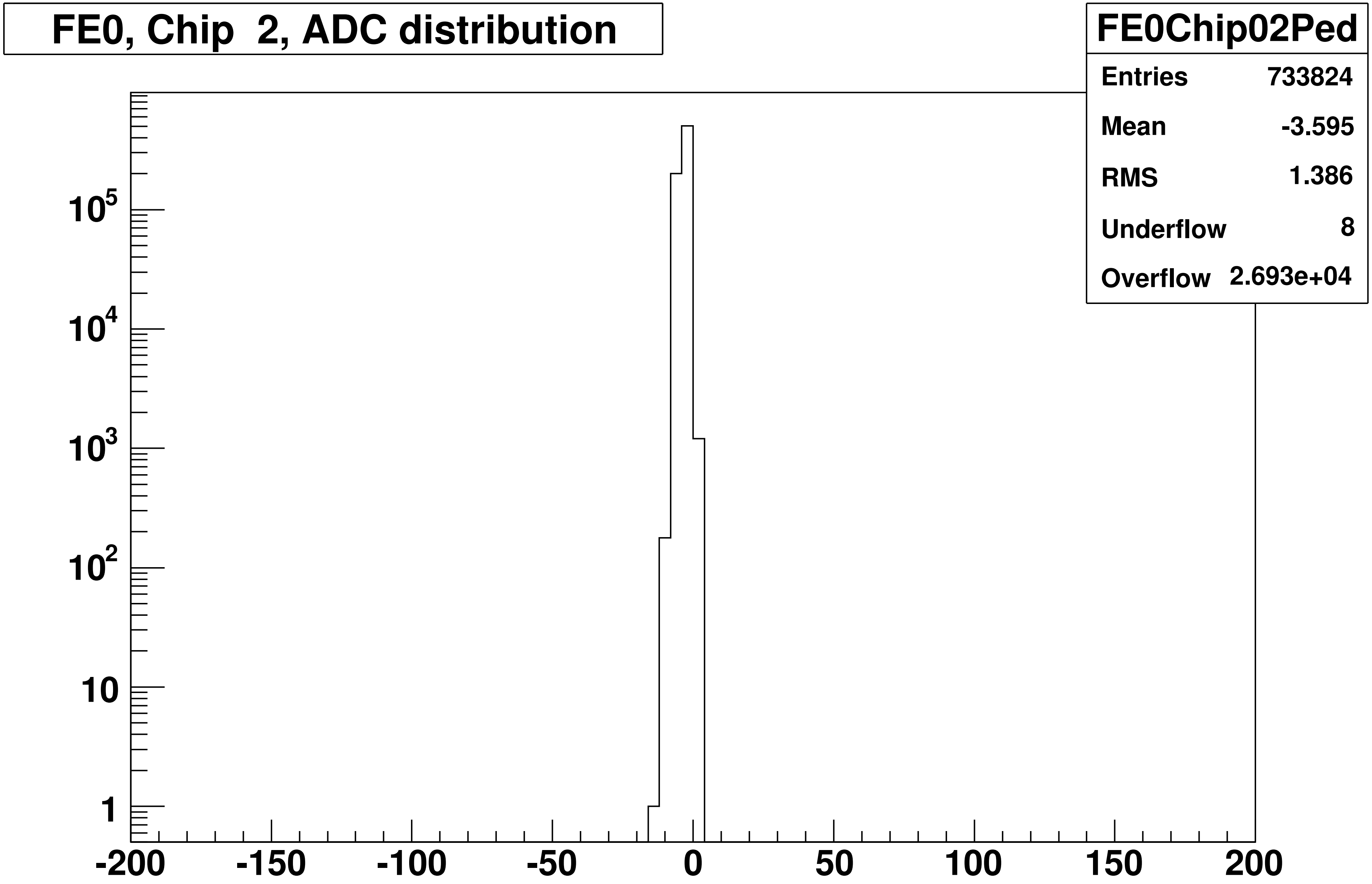
FE0, Chip 2, ADC distribution
FE0Chip02Ped
Entries 733824
Mean -3.595
RMS 1.386
Underflow 8
Overflow 2.693e+04
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10^3
10^2
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150
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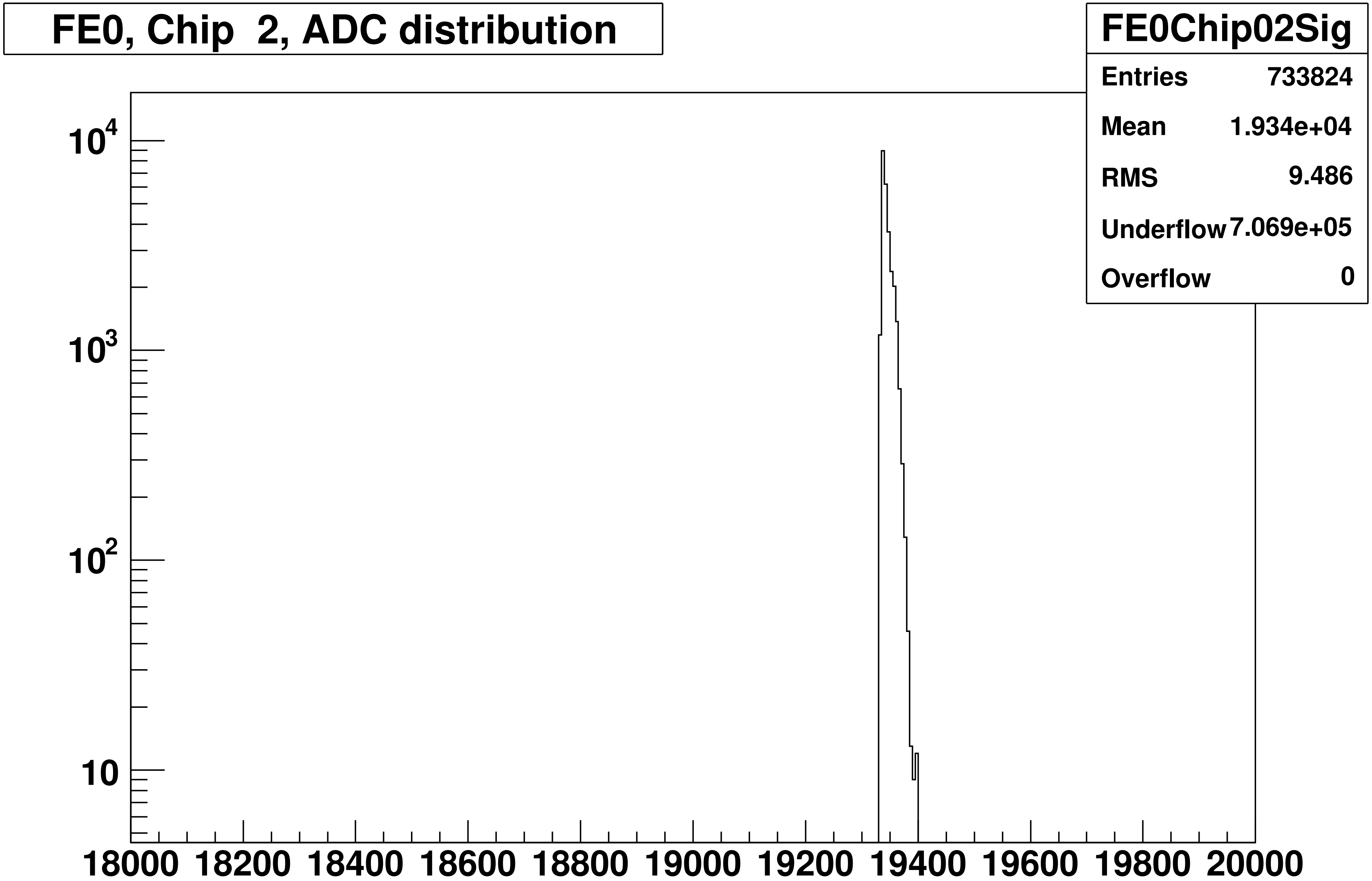
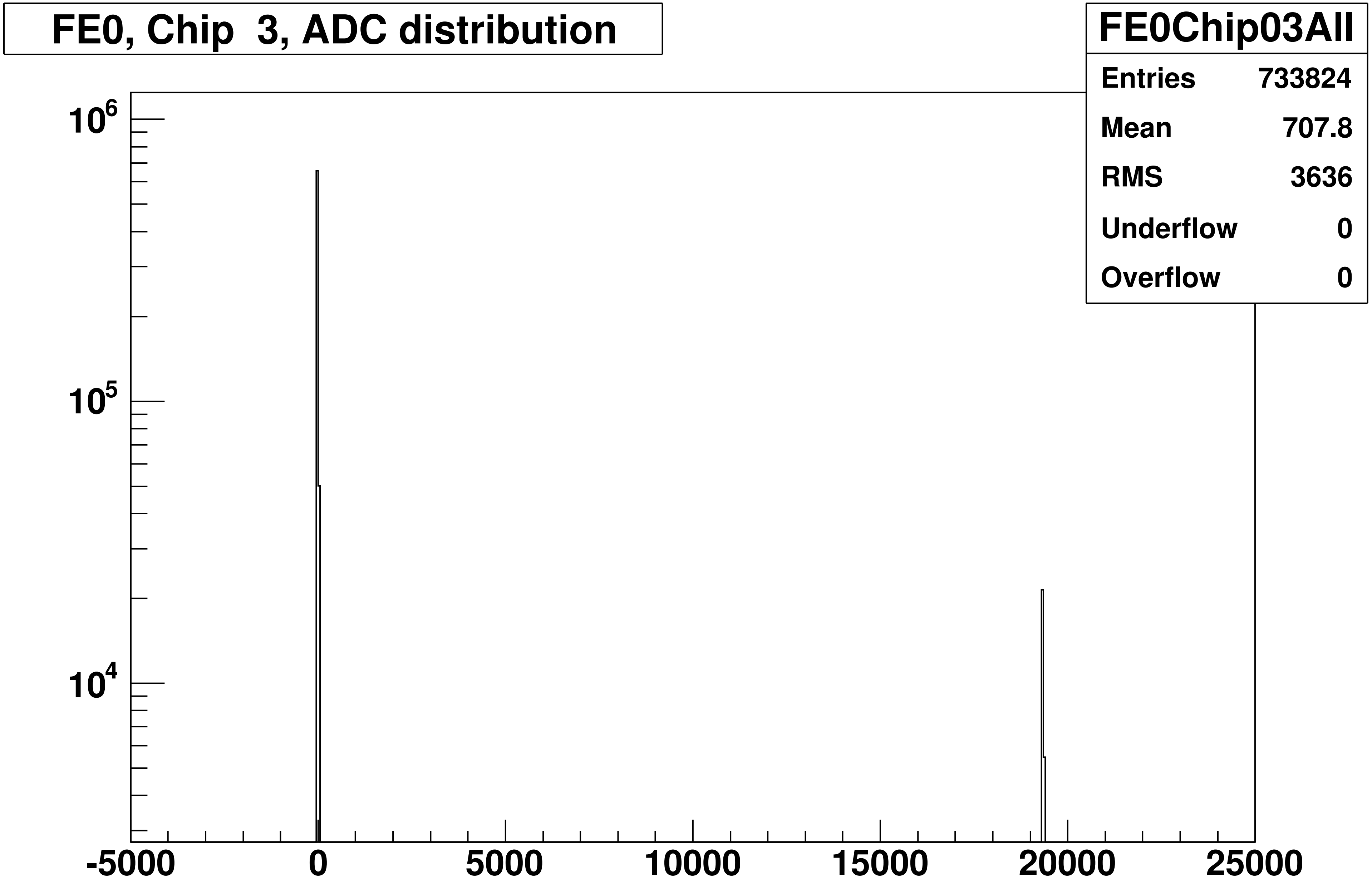


FE0, Chip 2, ADC distribution
FE0Chip02Sig
Entries 733824
Mean 1.934e+04
RMS 9.486
Underflow 7.069e+05
Overflow 0
10^4
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE0, Chip 3, ADC distribution
FE0Chip03All
Entries 733824
Mean 707.8
RMS 3636
Underflow 0
Overflow 0
10^6
10^5
10^4
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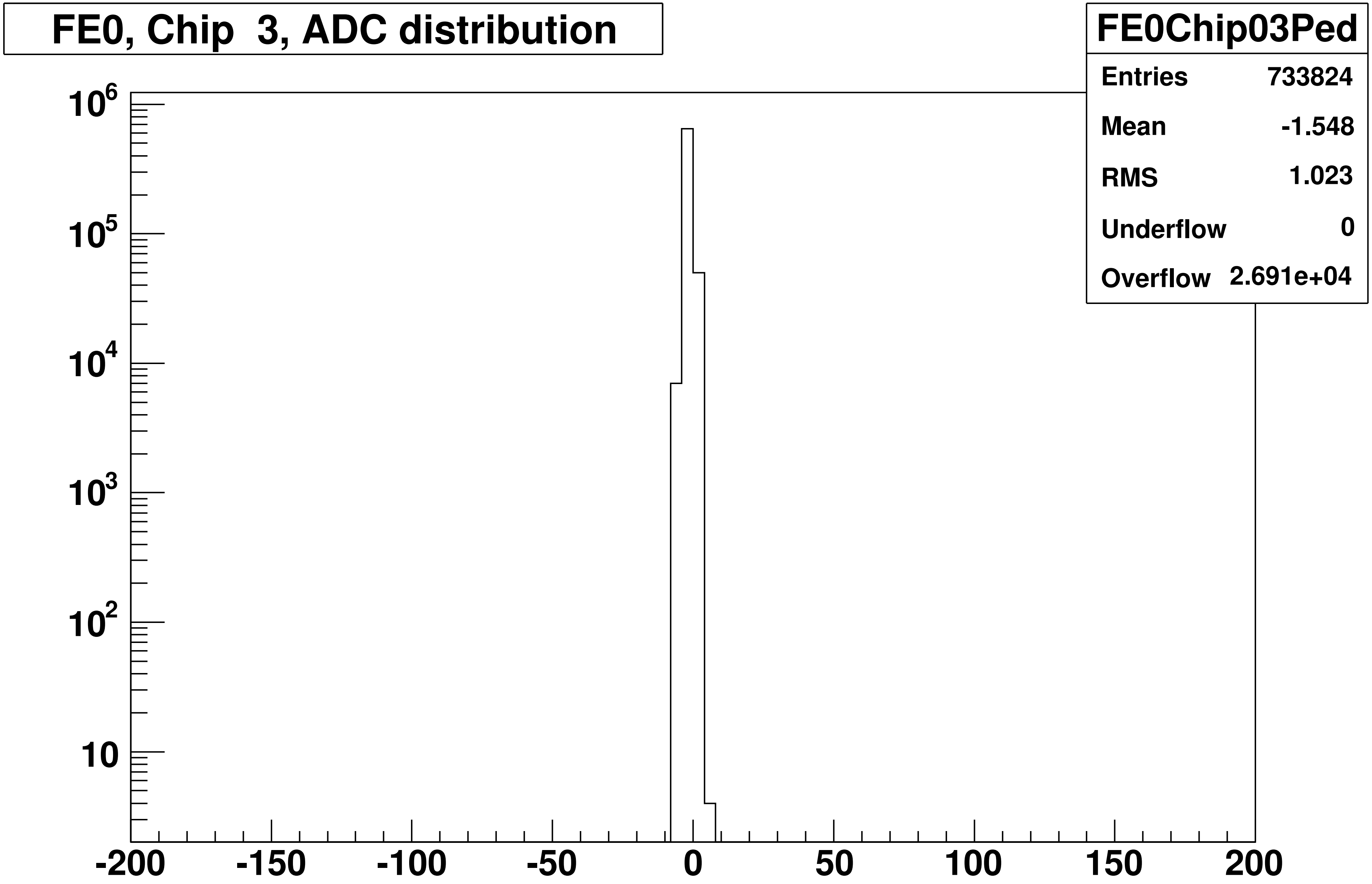
10000
15000
20000
25000


FE0, Chip 3, ADC distribution
FE0Chip03Ped
Entries 733824
Mean -1.548
RMS 1.023
Underflow 0
Overflow 2.691e+04
10
10^2
10^3
10^4
10^5
10^6
-200
-150
-100
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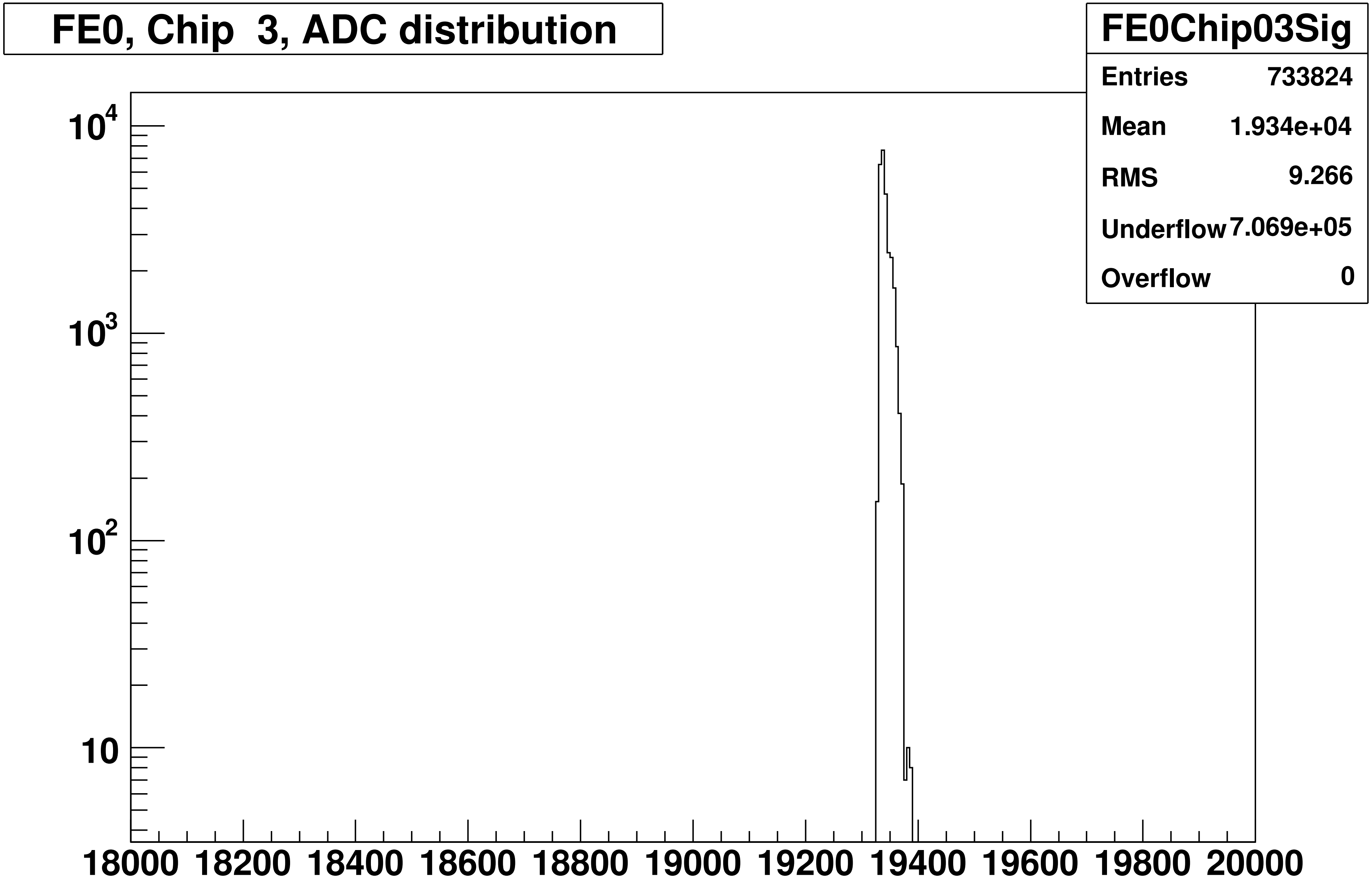
0
50
100
150
200



FE0, Chip 3, ADC distribution
FE0Chip03Sig
Entries 733824
Mean 1.934e+04
RMS 9.266
Underflow 7.069e+05
Overflow 0
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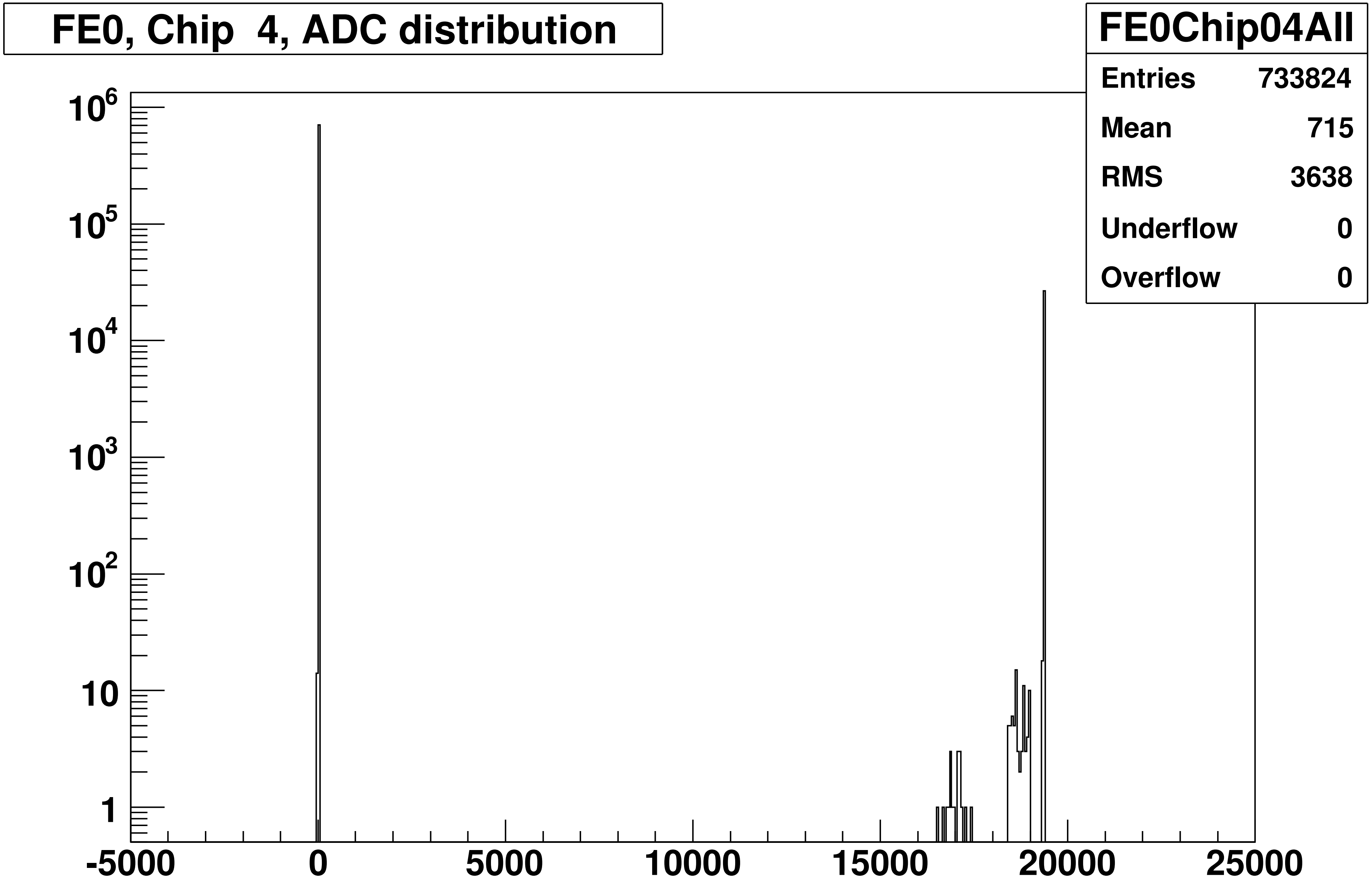
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE0, Chip 4, ADC distribution
FE0Chip04All
Entries 733824
Mean 715
RMS 3638
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
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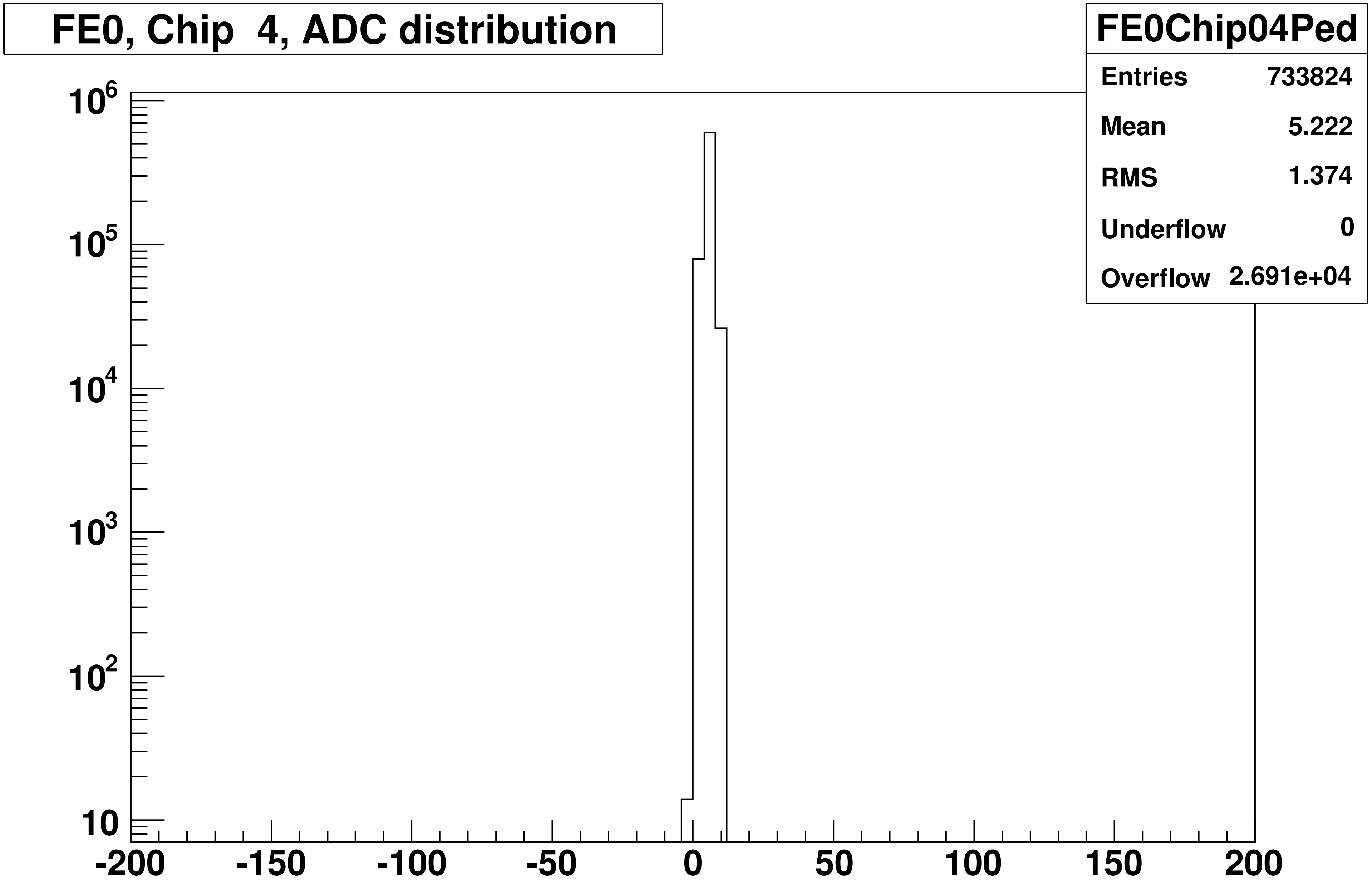
20000
25000


FE0, Chip 4, ADC distribution
FE0Chip04Ped
Entries 733824
Mean 5.222
RMS 1.374
Underflow 0
Overflow 2.691e+04
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10^4
10^3
10^2
10
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-100
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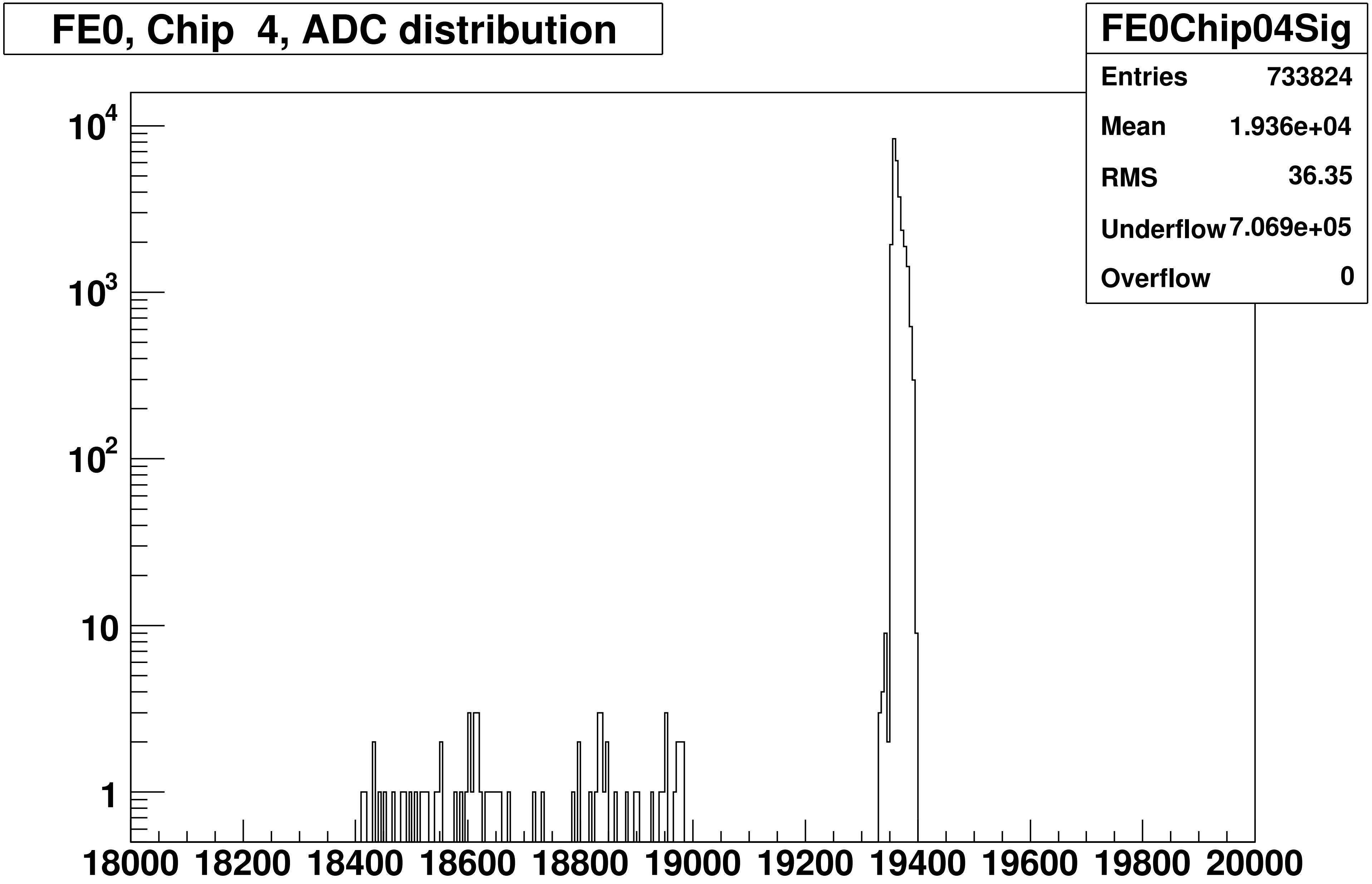
0
50
100
150
200



FE0, Chip 4, ADC distribution
FE0Chip04Sig
Entries 733824
Mean 1.936e+04
RMS 36.35
Underflow 7.069e+05
Overflow 0
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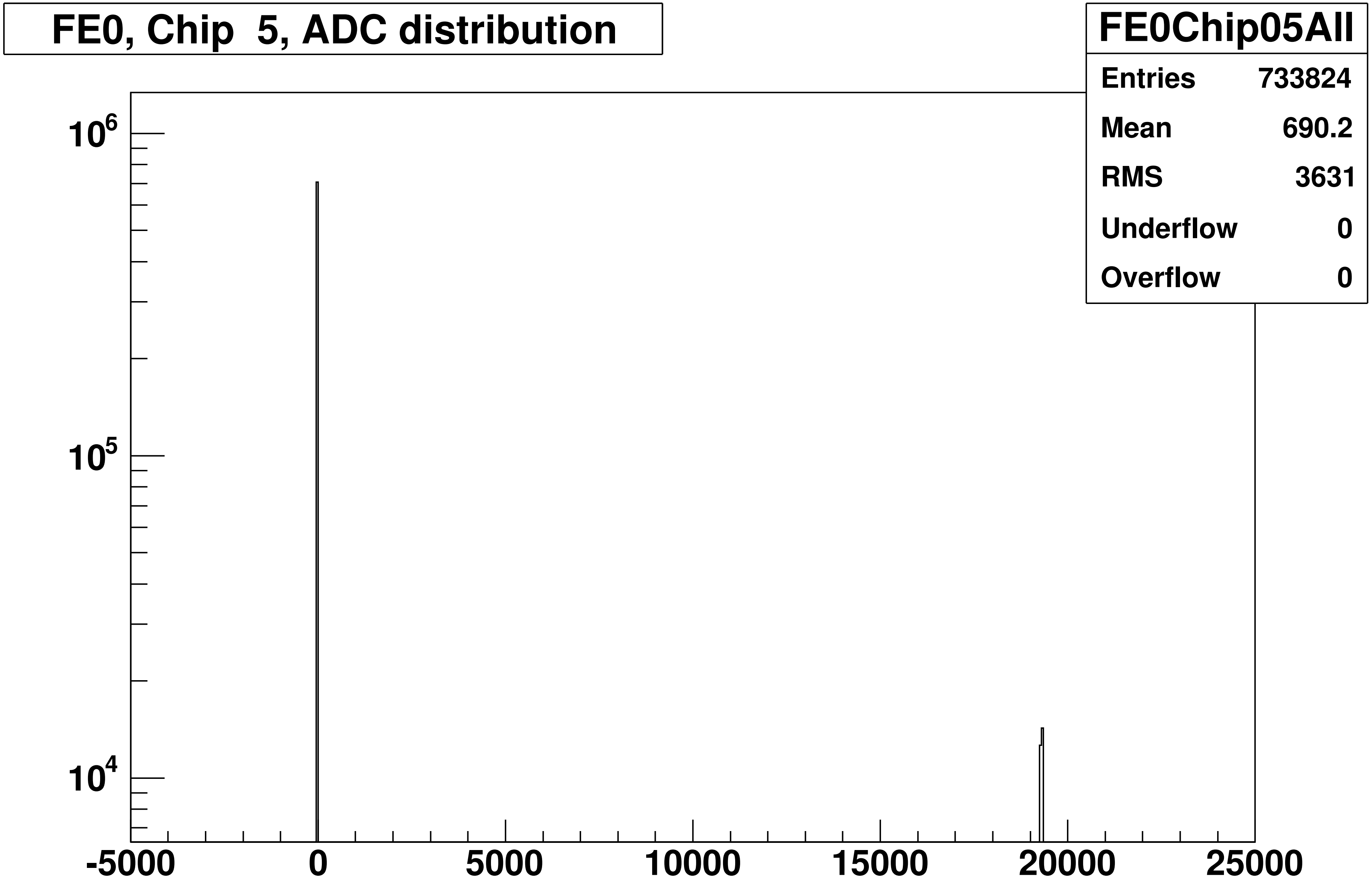
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE0, Chip 5, ADC distribution
FE0Chip05All
Entries 733824
Mean 690.2
RMS 3631
Underflow 0
Overflow 0
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10^5
10^4
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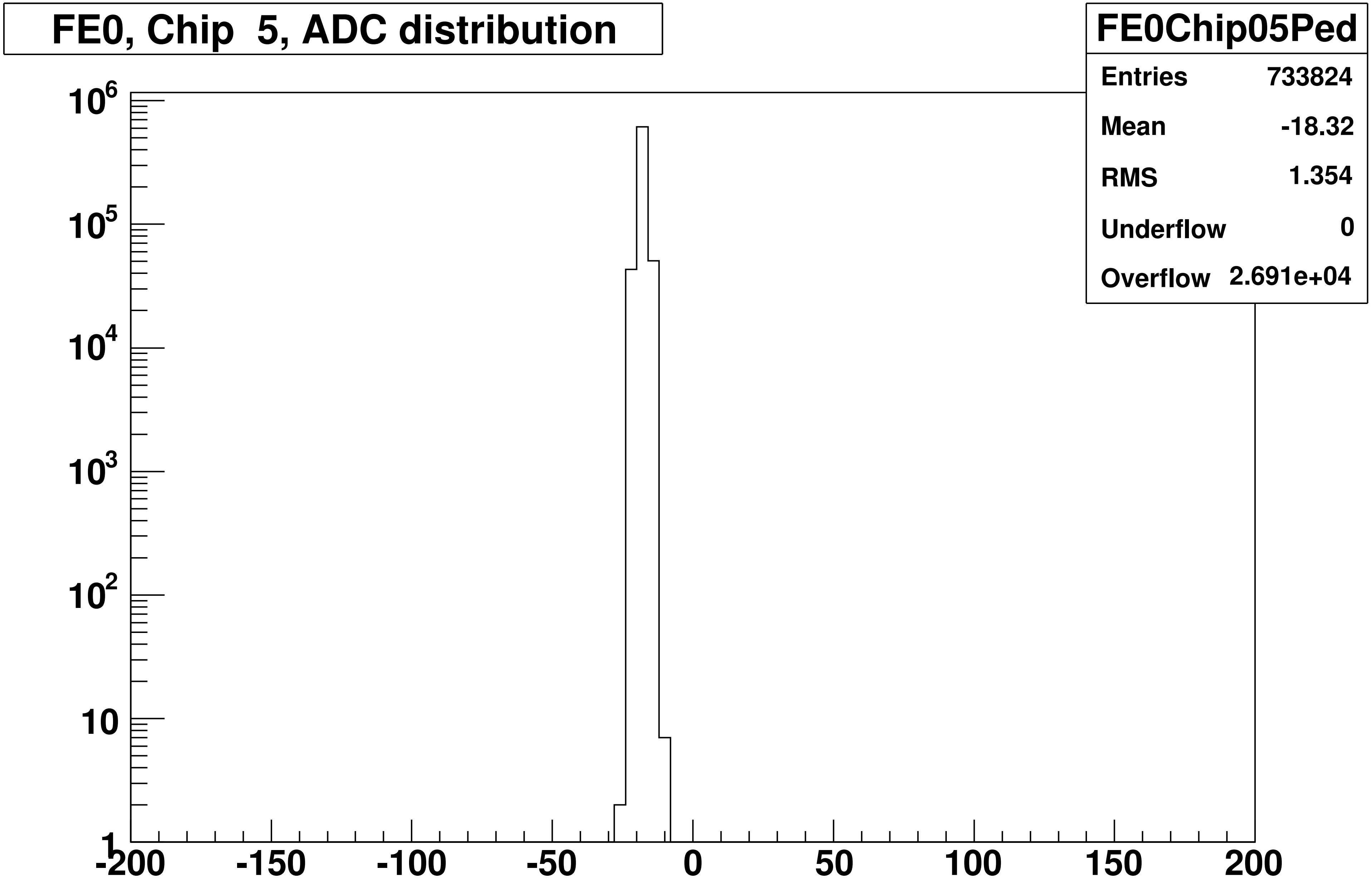
10000
15000
20000
25000



FE0, Chip 5, ADC distribution
FE0Chip05Ped
Entries 733824
Mean -18.32
RMS 1.354
Underflow 0
Overflow 2.691e+04
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10^5
10^4
10^3
10^2
10
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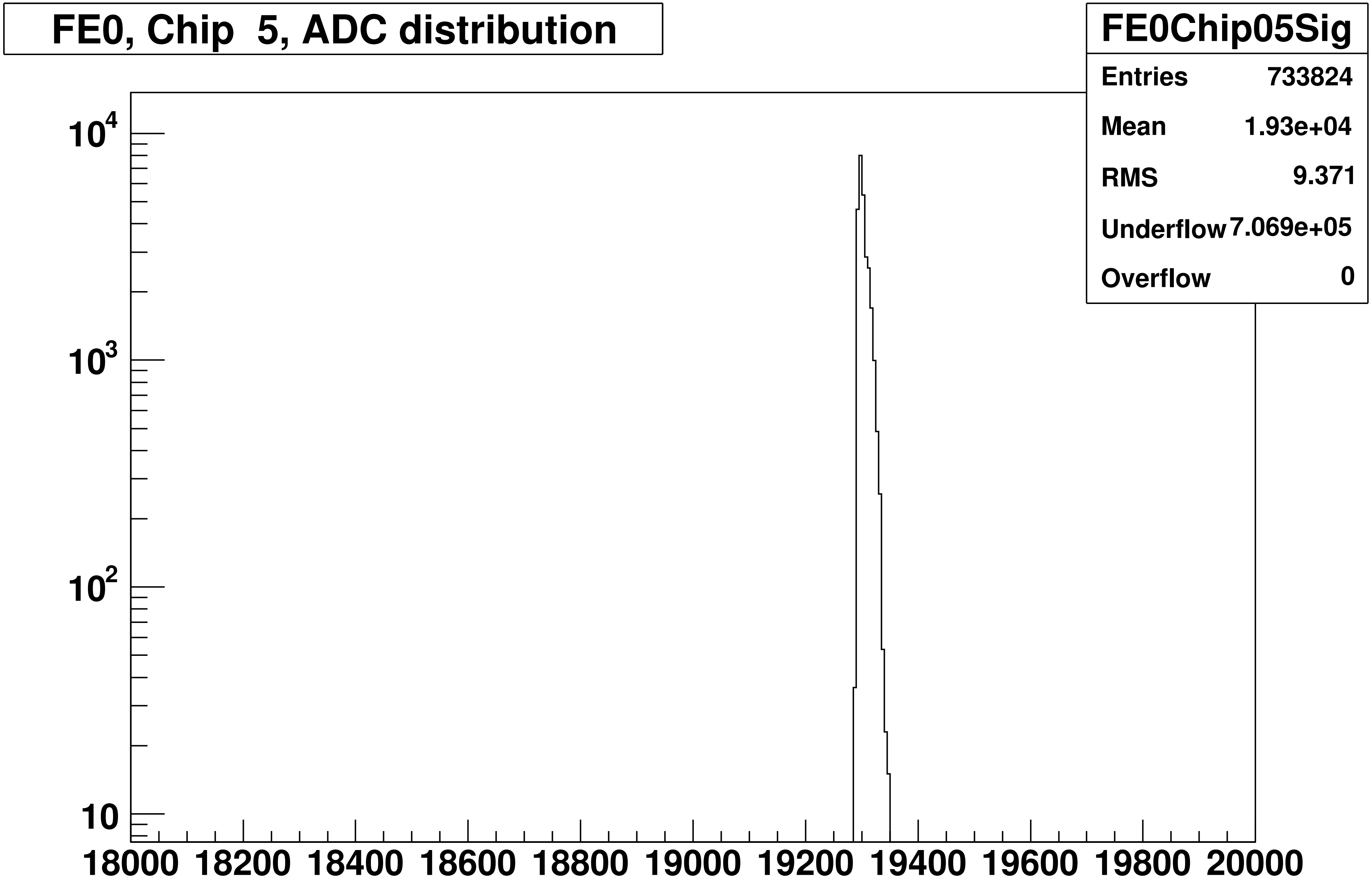
50
100
150
200


FE0, Chip 5, ADC distribution
FE0Chip05Sig
Entries 733824
Mean 1.93e+04
RMS 9.371
Underflow 7.069e+05
Overflow 0
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10^3
10^2
10
18000
18200
18400
18600
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19000
19200
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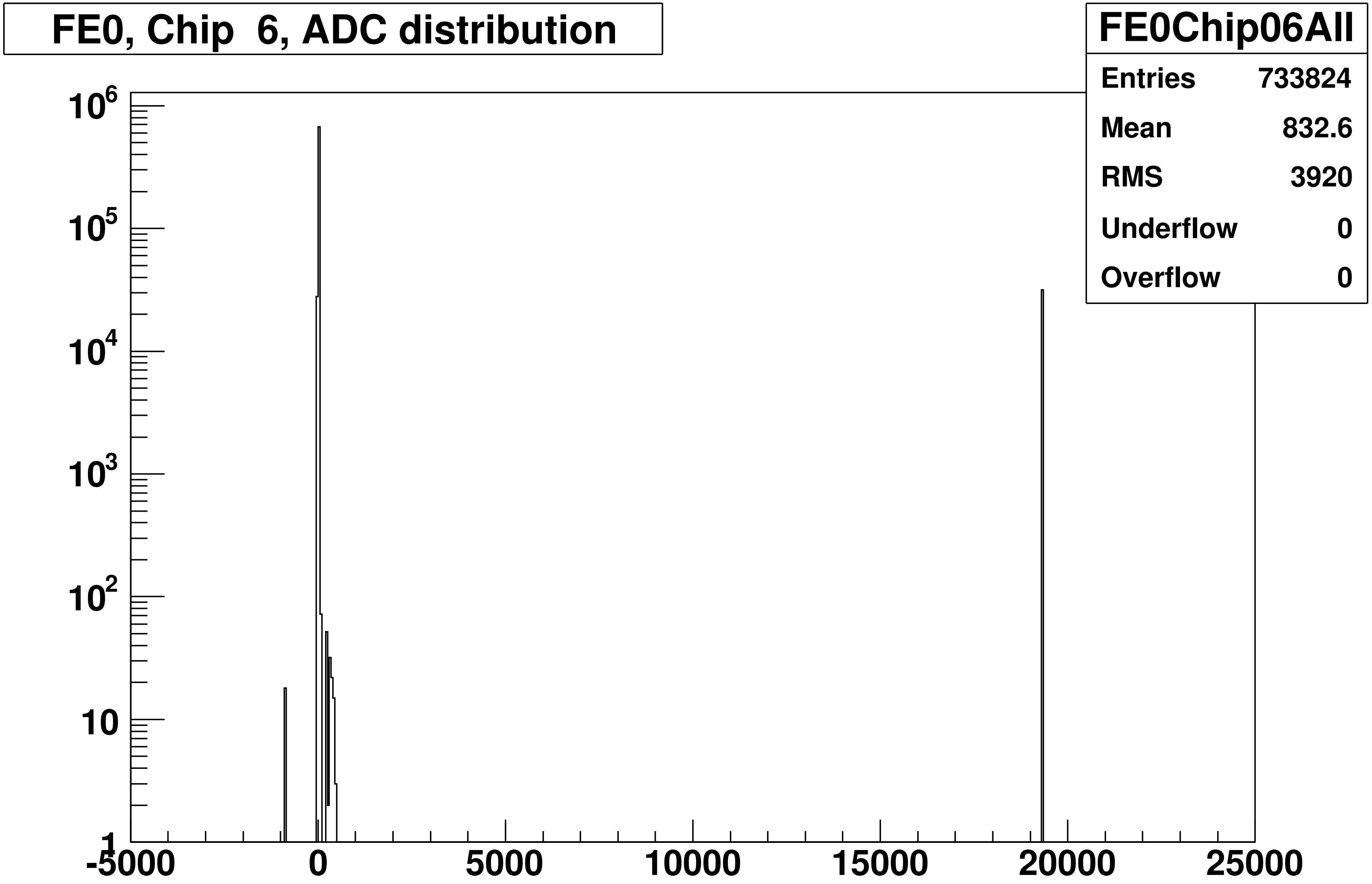
19800
20000



FE0, Chip 6, ADC distribution
FE0Chip06All
Entries 733824
Mean 832.6
RMS 3920
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
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0
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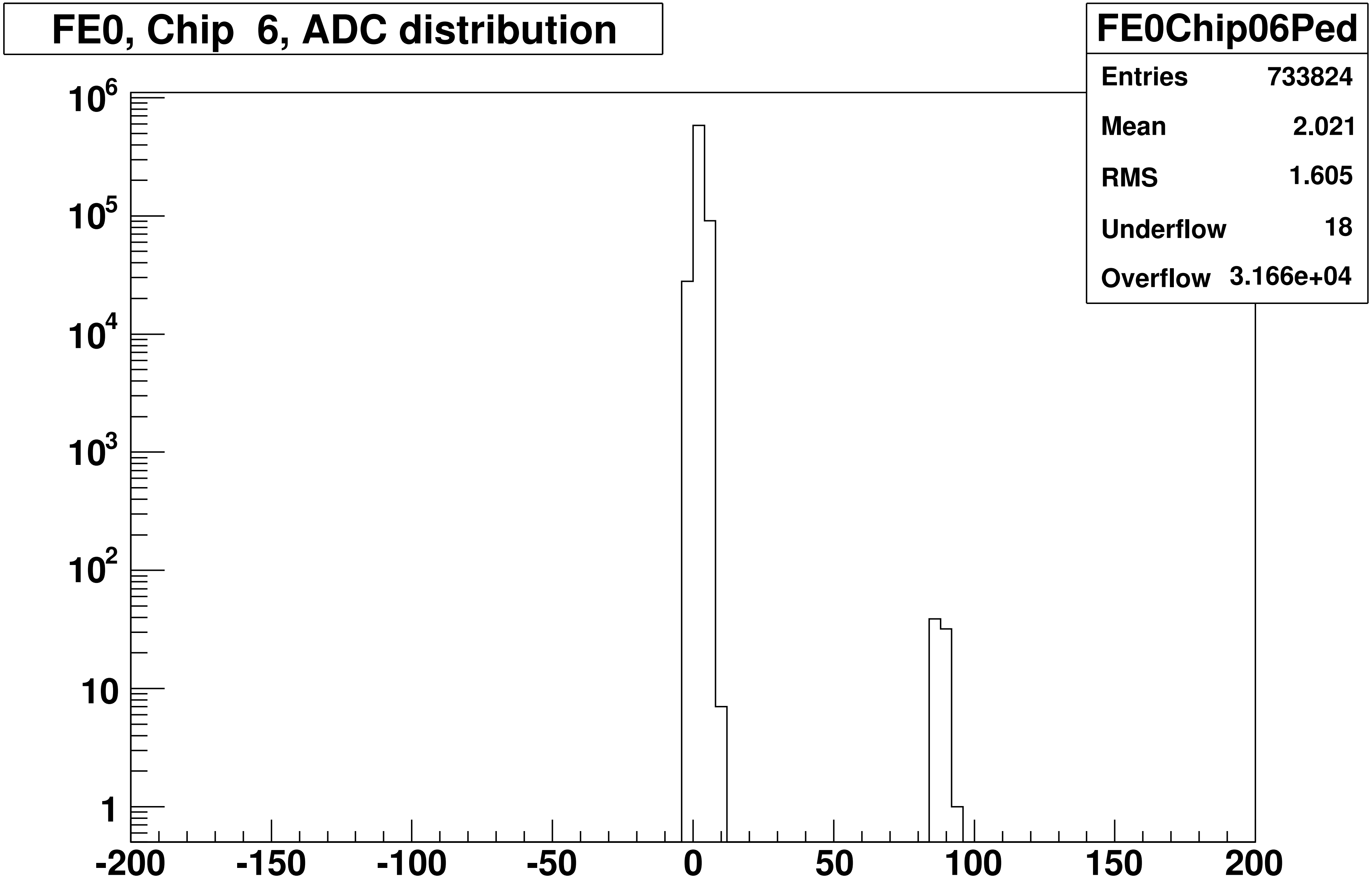
10000
15000
20000
25000


FE0, Chip 6, ADC distribution
FE0Chip06Ped
Entries 733824
Mean 2.021
RMS 1.605
Underflow 18
Overflow 3.166e+04
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10^5
10^4
10^3
10^2
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1
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150
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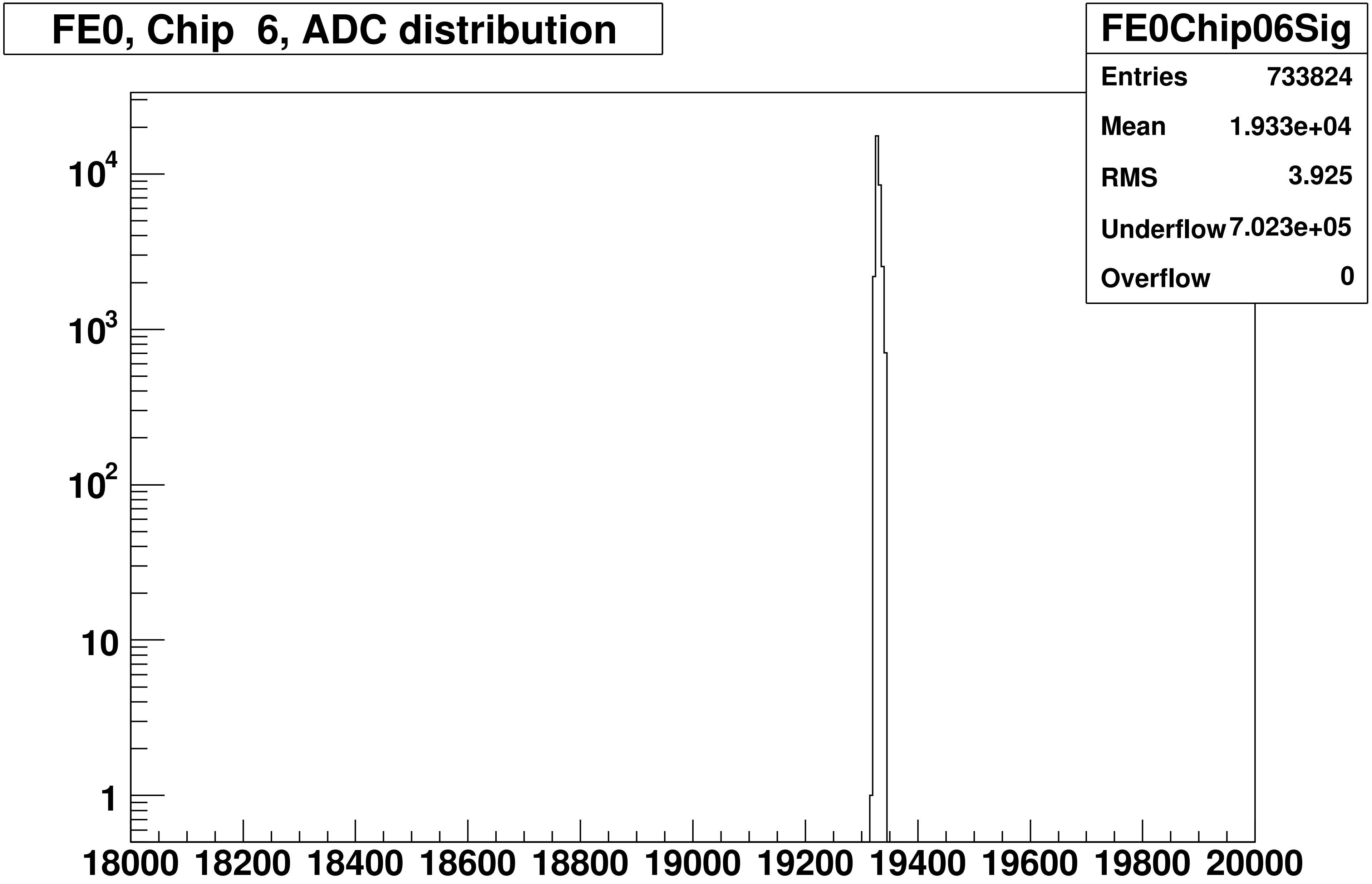
FE0, Chip 6, ADC distribution
FE0Chip06Sig
Entries 733824
Mean 1.933e+04
RMS 3.925
Underflow 7.023e+05
Overflow 0
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10^3
10^2
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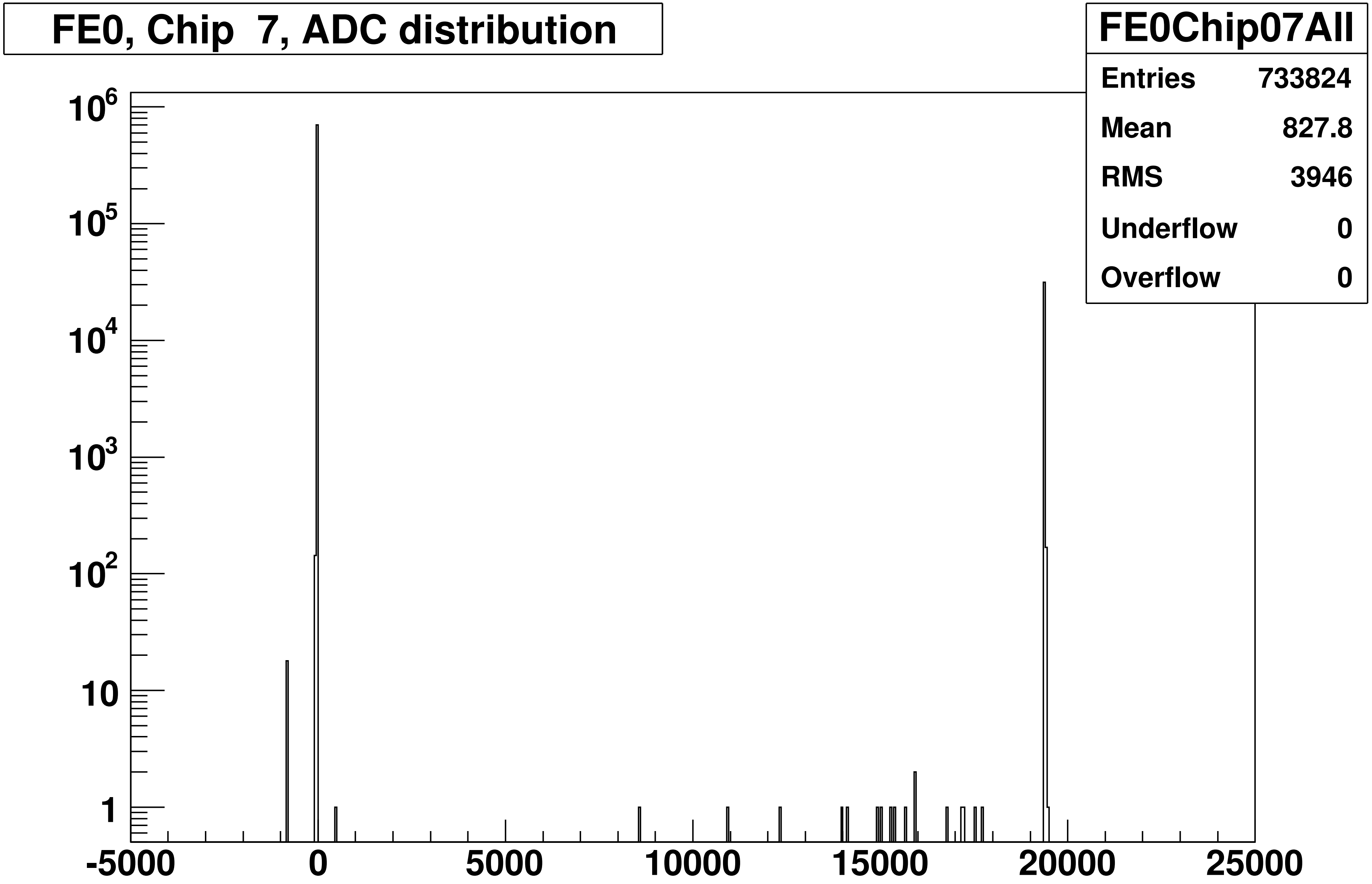
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE0, Chip 7, ADC distribution
FE0Chip07All
Entries 733824
Mean 827.8
RMS 3946
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
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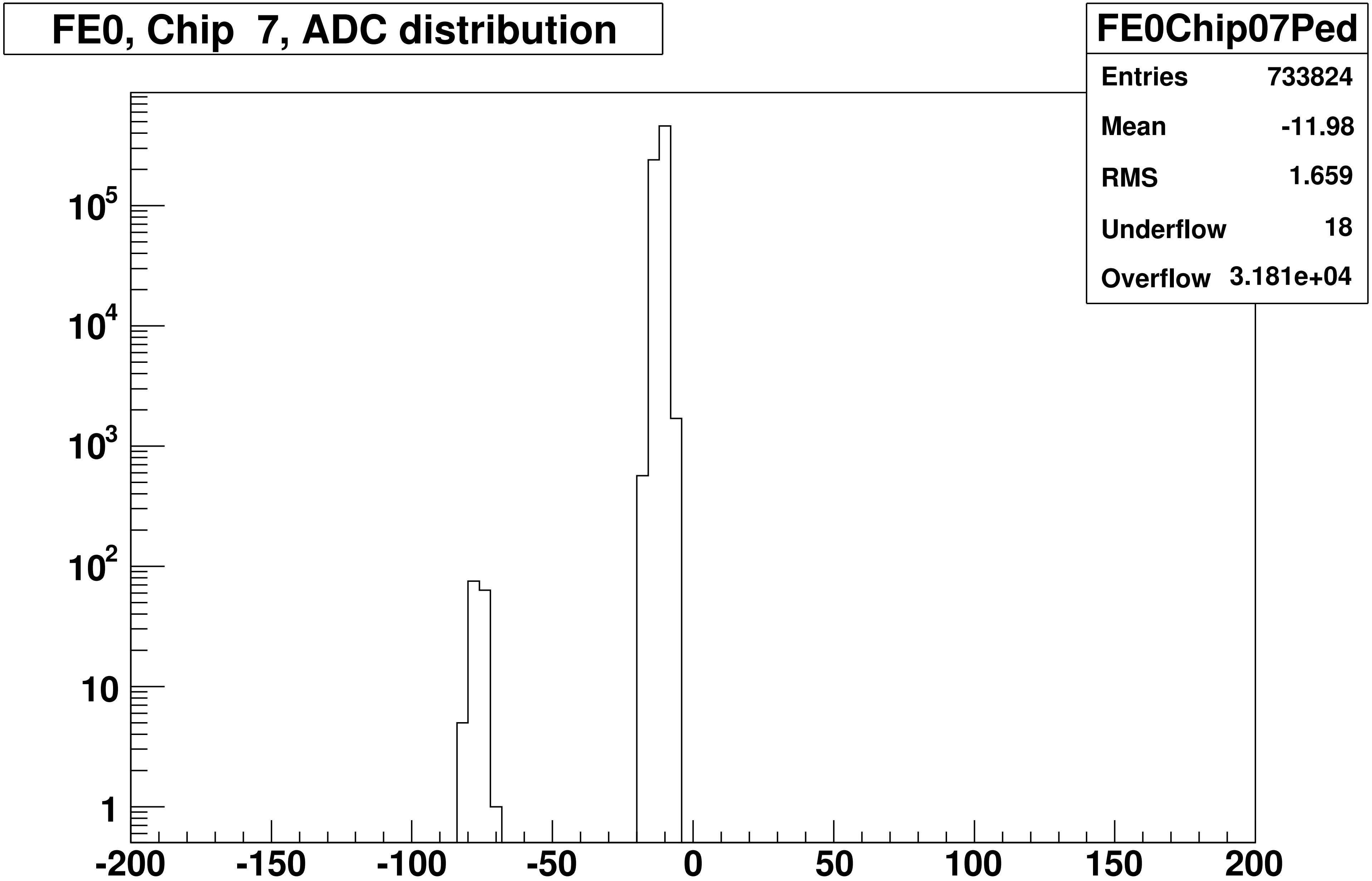
20000
25000


FE0, Chip 7, ADC distribution
FE0Chip07Ped
Entries 733824
Mean -11.98
RMS 1.659
Underflow 18
Overflow 3.181e+04
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10^3
10^2
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150
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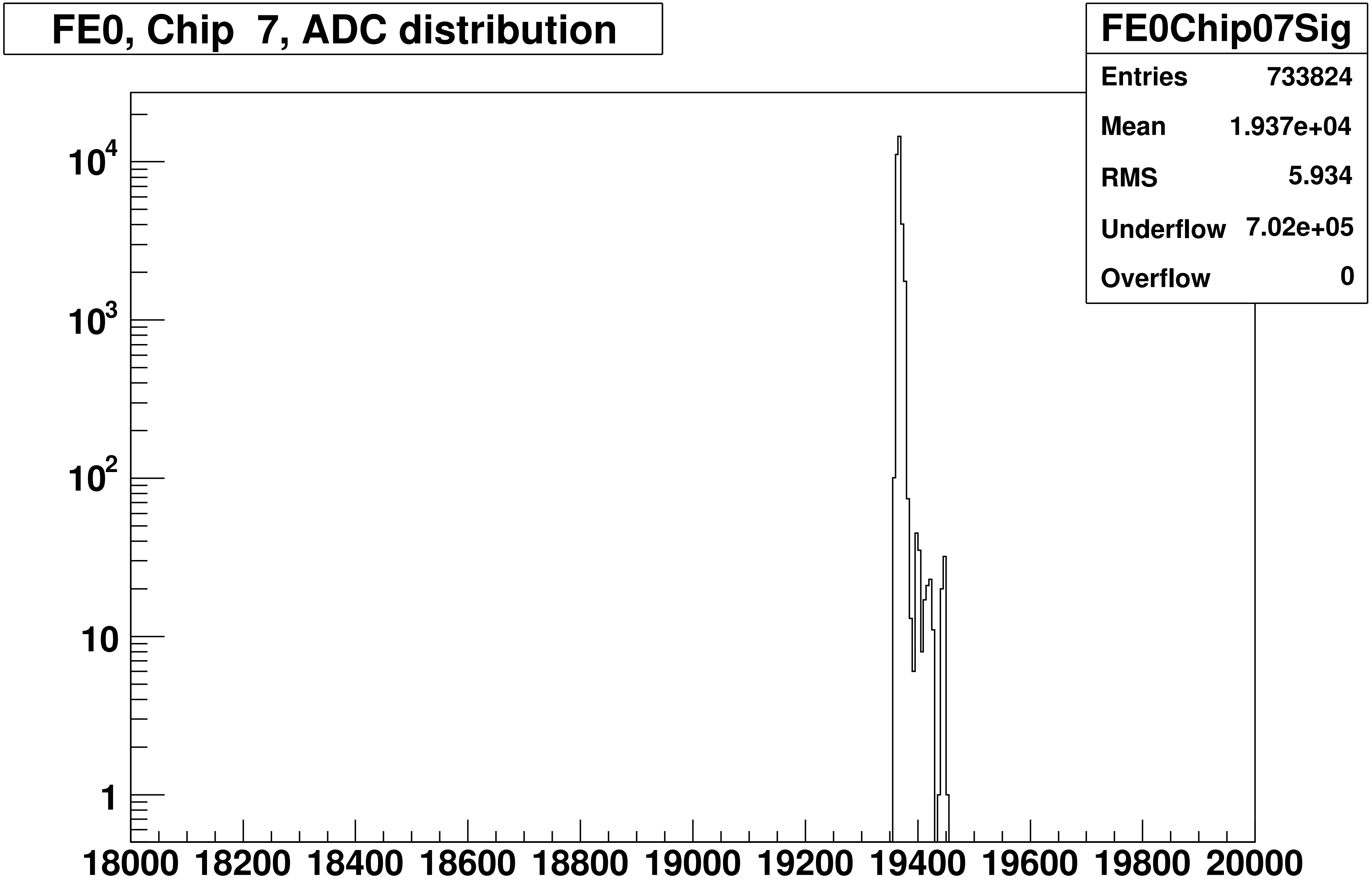
FE0, Chip 7, ADC distribution
FE0Chip07Sig
Entries 733824
Mean 1.937e+04
RMS 5.934
Underflow 7.02e+05
Overflow 0
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10^3
10^2
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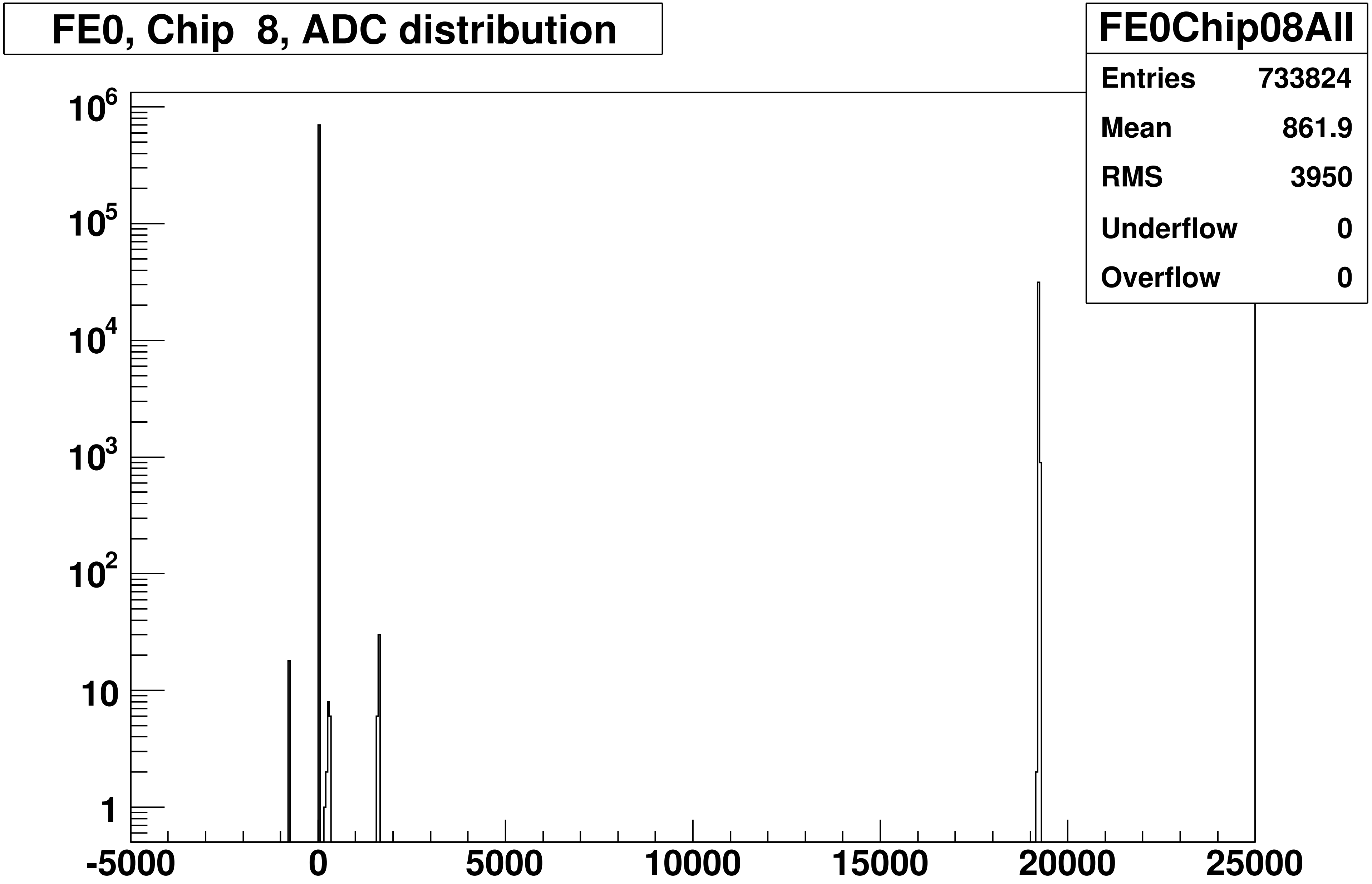
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE0, Chip 8, ADC distribution
FE0Chip08All
Entries 733824
Mean 861.9
RMS 3950
Underflow 0
Overflow 0
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10000
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20000
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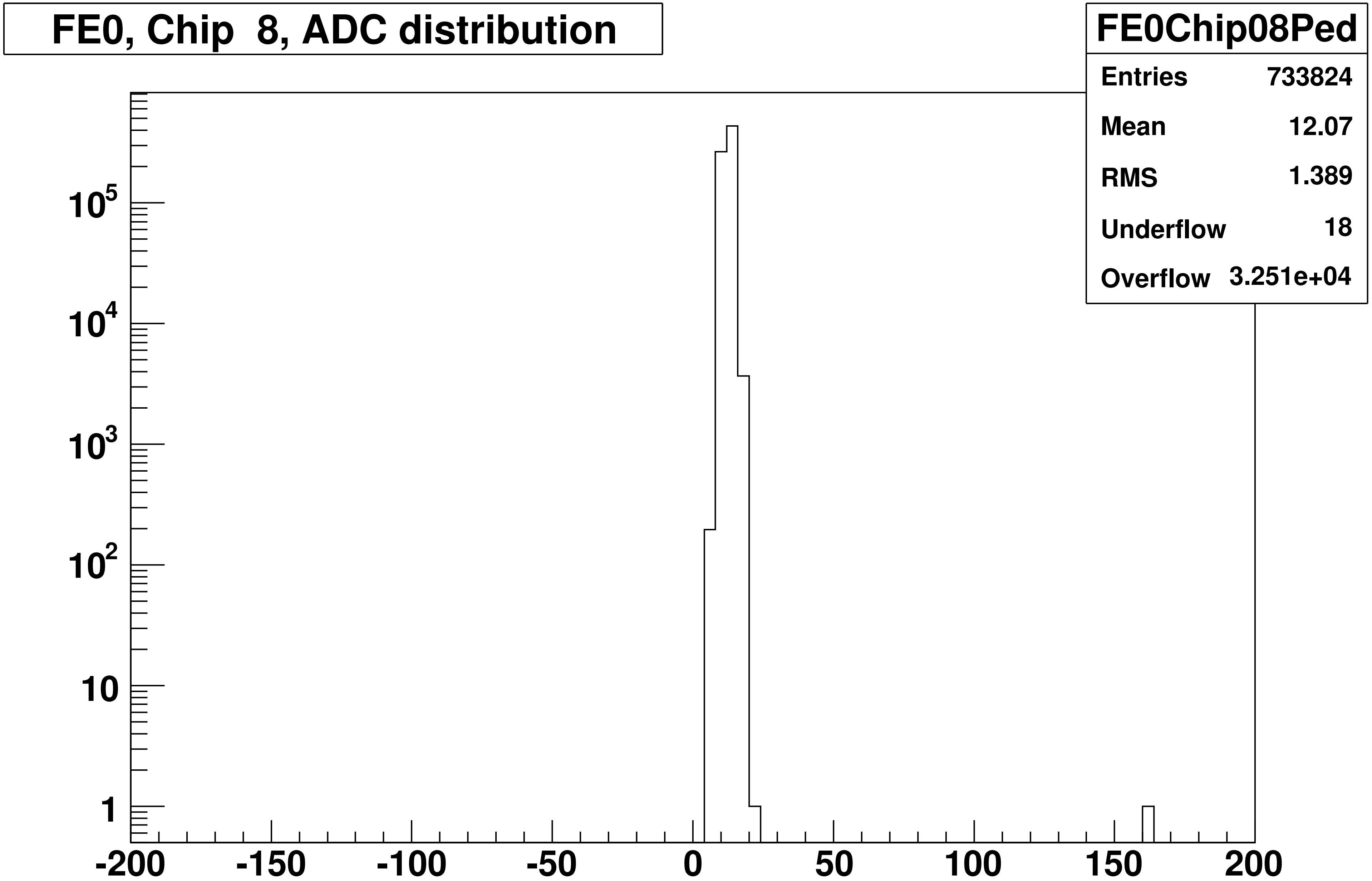
1
10
10^2
10^3
10^4
10^5
10^6


FE0, Chip 8, ADC distribution
FE0Chip08Ped
Entries 733824
Mean 12.07
RMS 1.389
Underflow 18
Overflow 3.251e+04
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10^4
10^3
10^2
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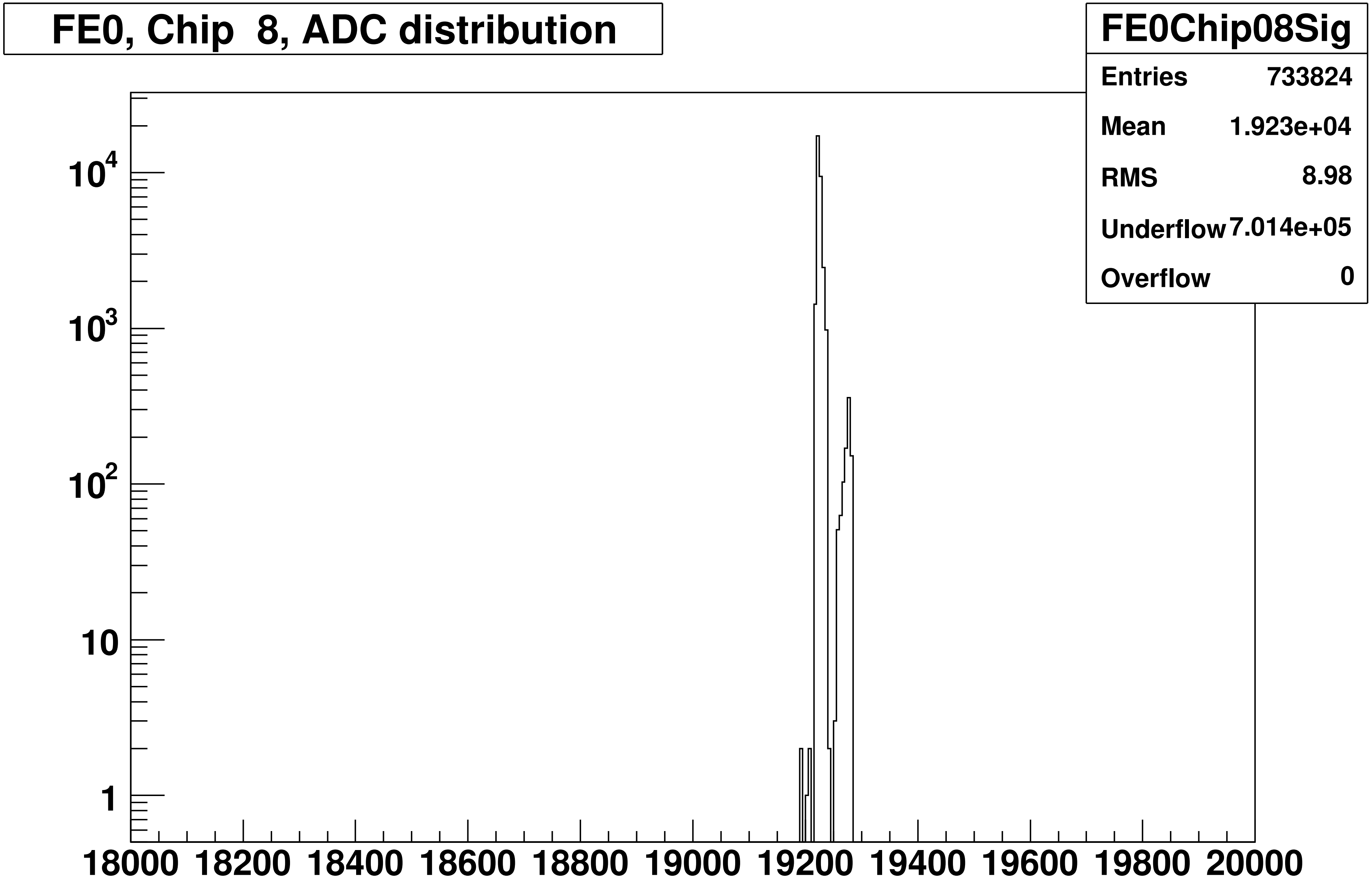

FE0, Chip 8, ADC distribution
FE0Chip08Sig
Entries 733824
Mean 1.923e+04
RMS 8.98
Underflow 7.014e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
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18600
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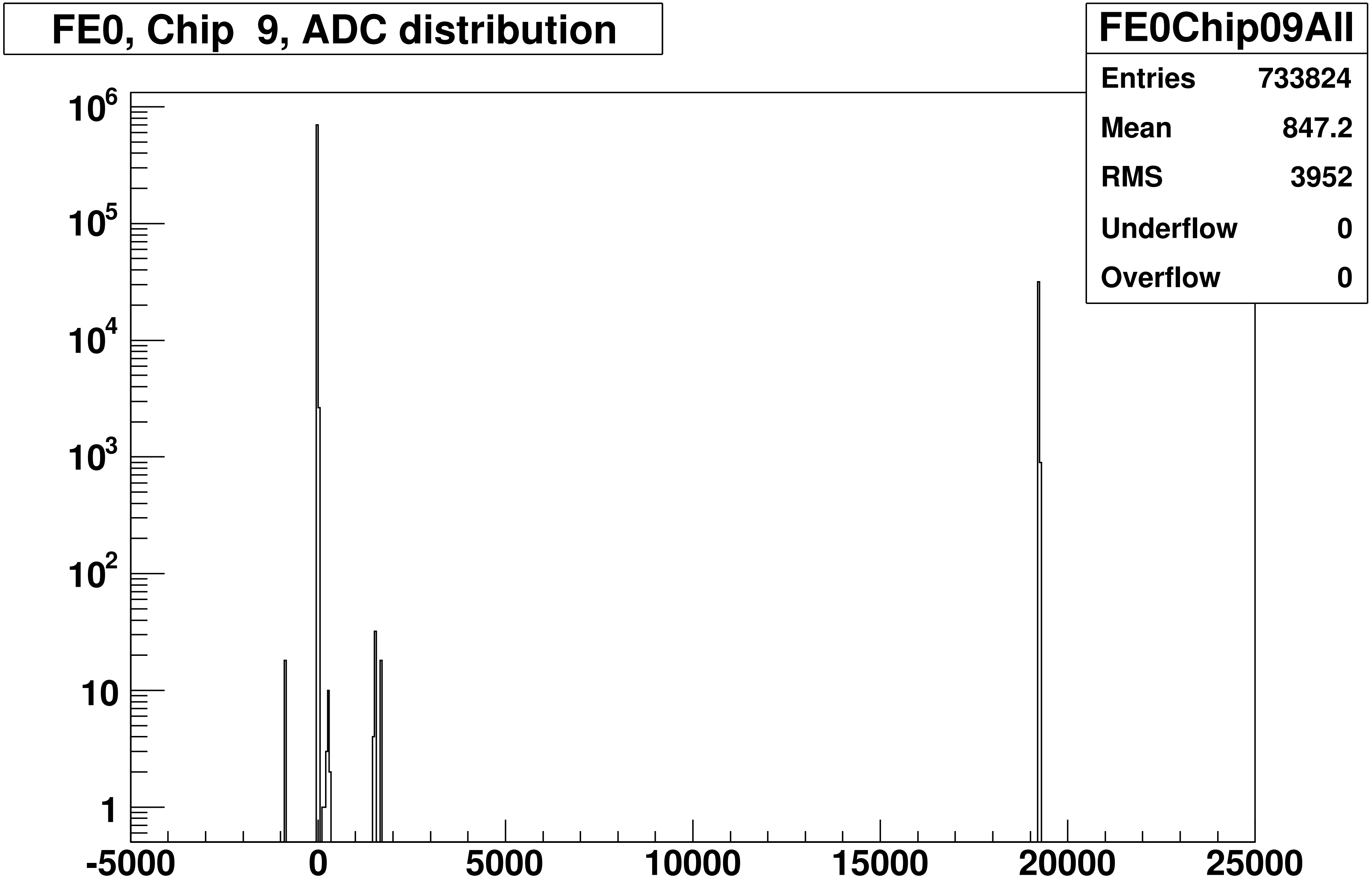
FE0, Chip 9, ADC distribution
FE0Chip09All
Entries 733824
Mean 847.2
RMS 3952
Underflow 0
Overflow 0
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10^4
10^3
10^2
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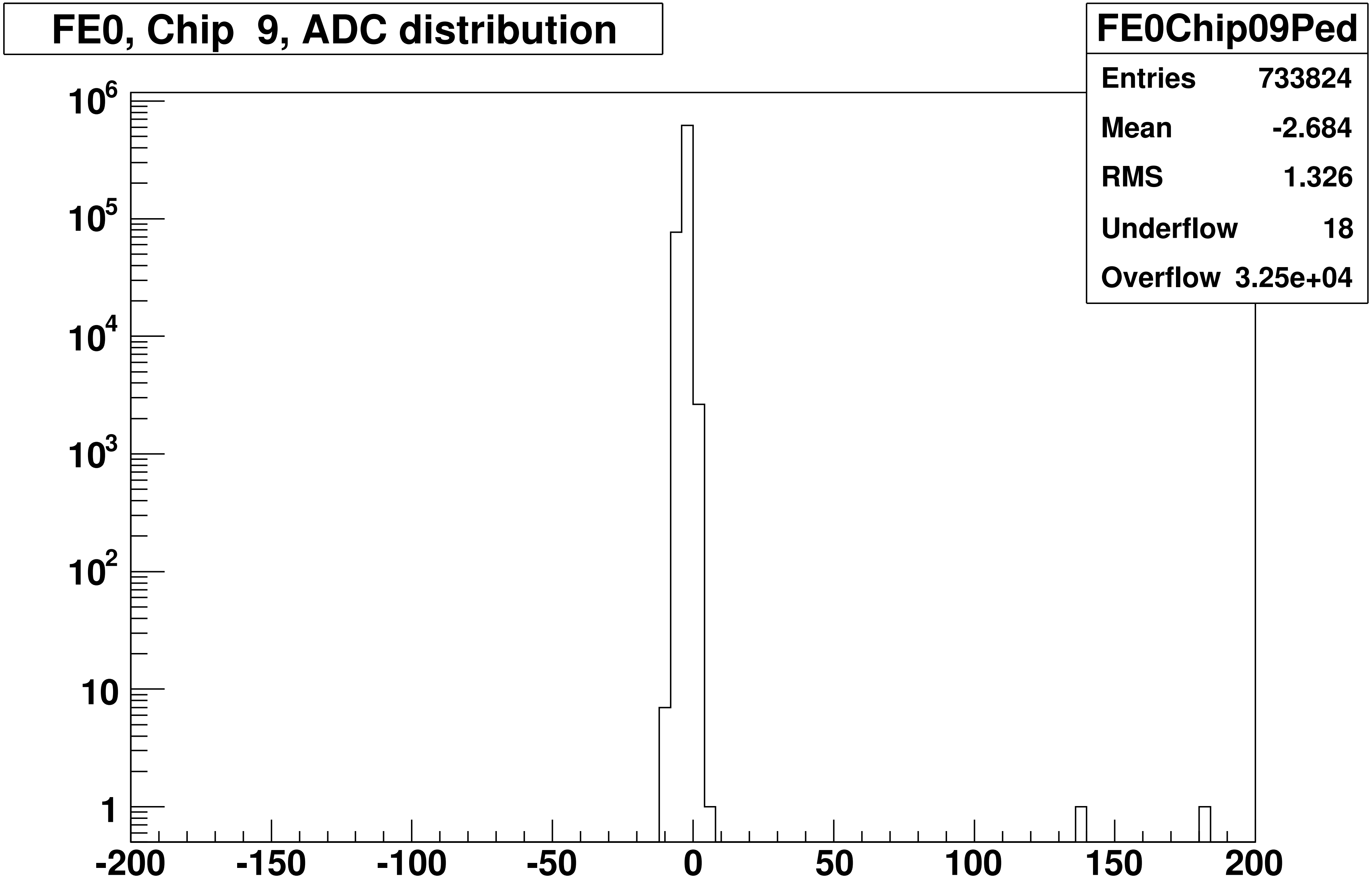

FE0, Chip 9, ADC distribution
FE0Chip09Ped
Entries 733824
Mean -2.684
RMS 1.326
Underflow 18
Overflow 3.25e+04
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10^5
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10^3
10^2
10
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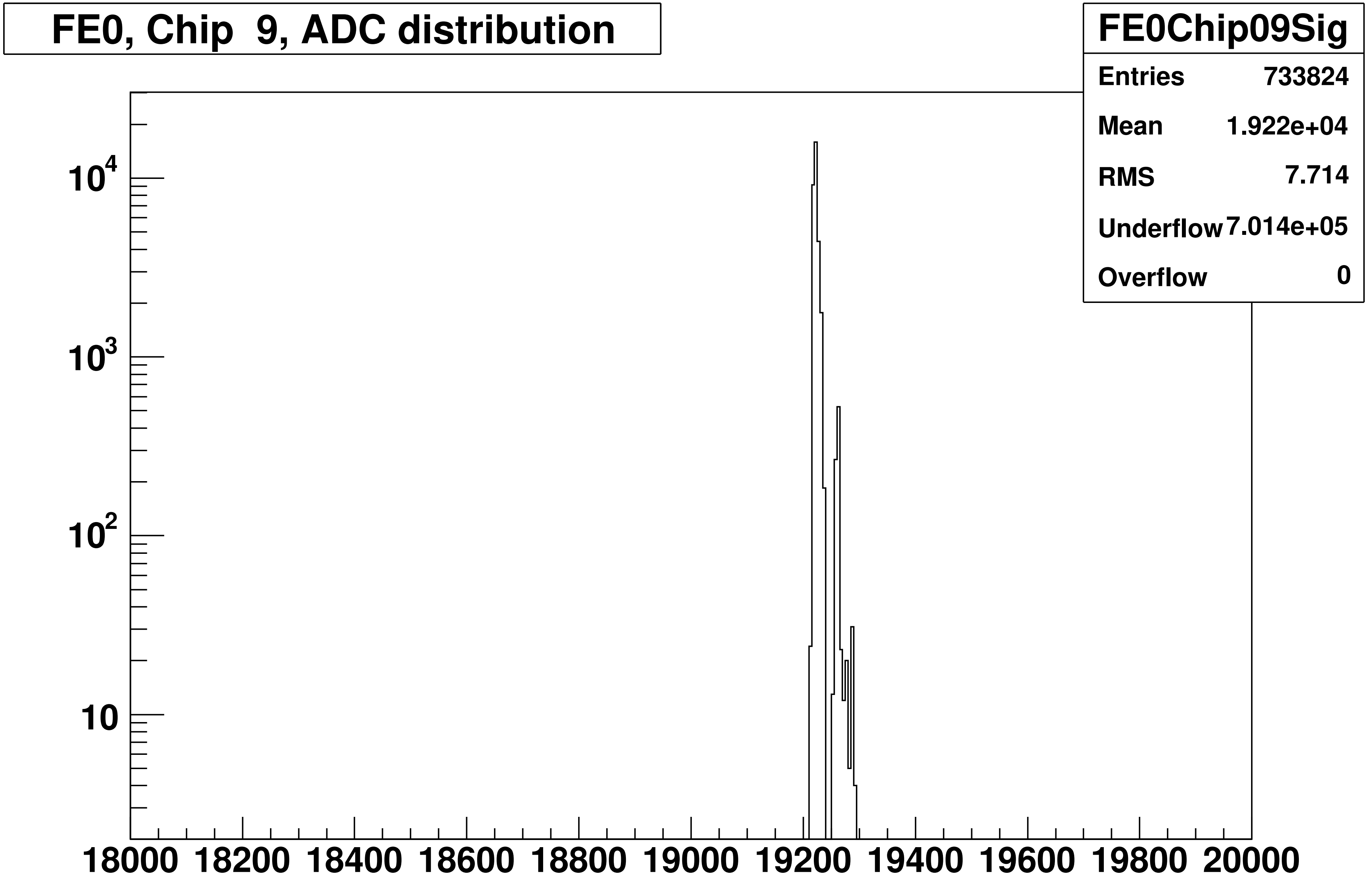
FE0, Chip 9, ADC distribution
FE0Chip09Sig
Entries 733824
Mean 1.922e+04
RMS 7.714
Underflow 7.014e+05
Overflow 0
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10^3
10^2
10
18000
18200
18400
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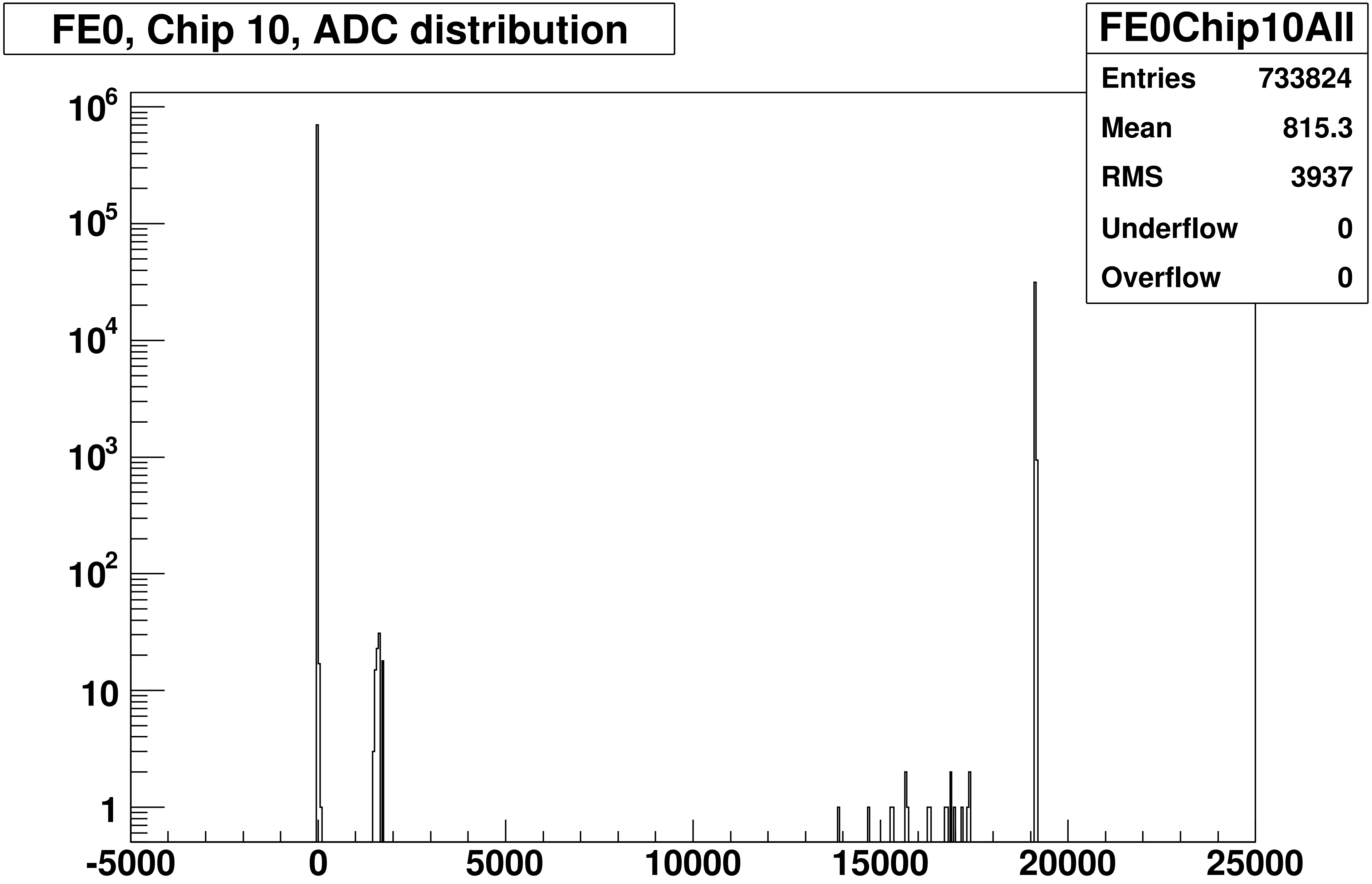
20000



FE0, Chip 10, ADC distribution
FE0Chip10All
Entries 733824
Mean 815.3
RMS 3937
Underflow 0
Overflow 0
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10
10^2
10^3
10^4
10^5
10^6
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0
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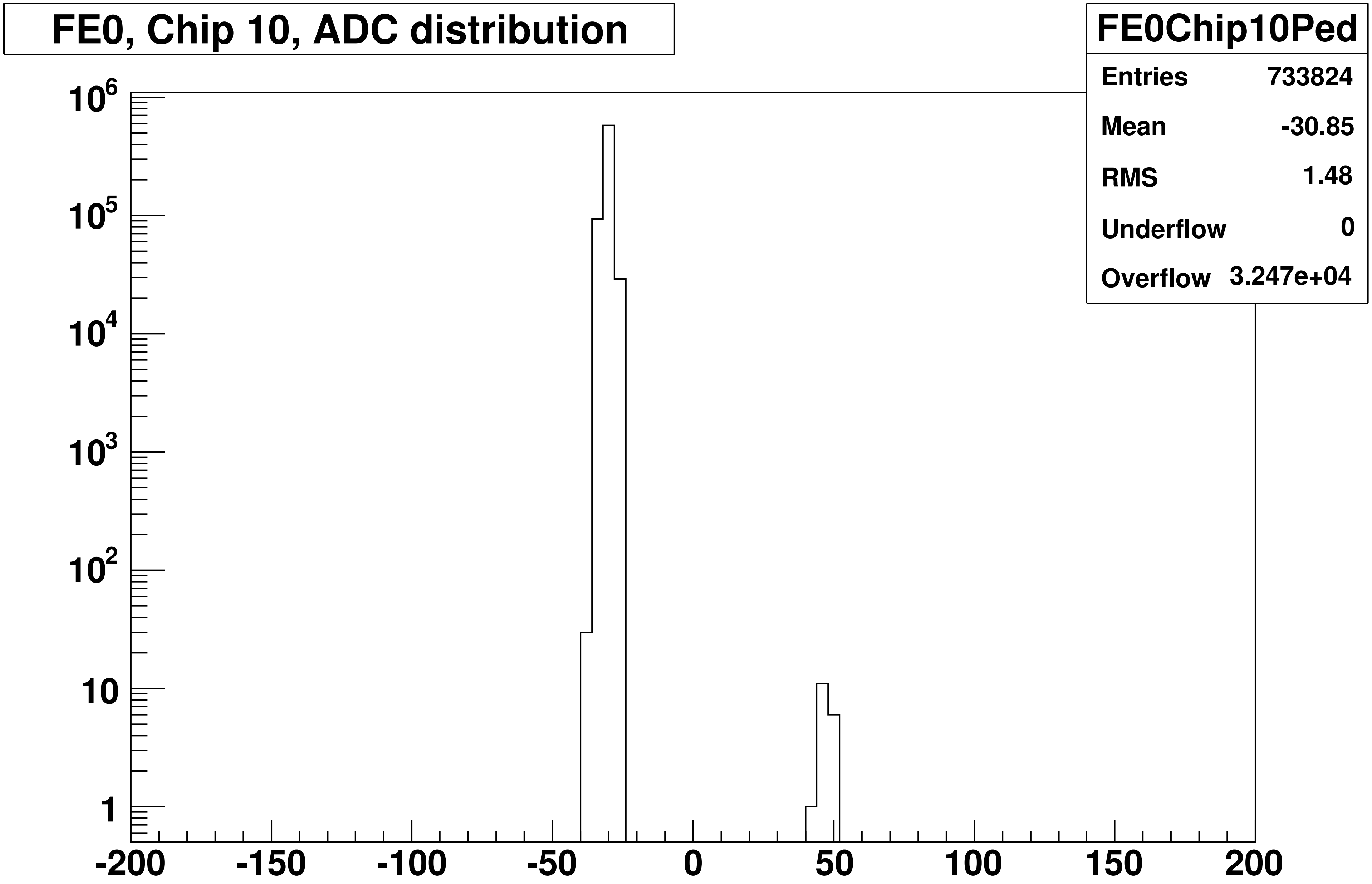
FE0, Chip 10, ADC distribution
FE0Chip10Ped
Entries 733824
Mean -30.85
RMS 1.48
Underflow 0
Overflow 3.247e+04
10^6
10^5
10^4
10^3
10^2
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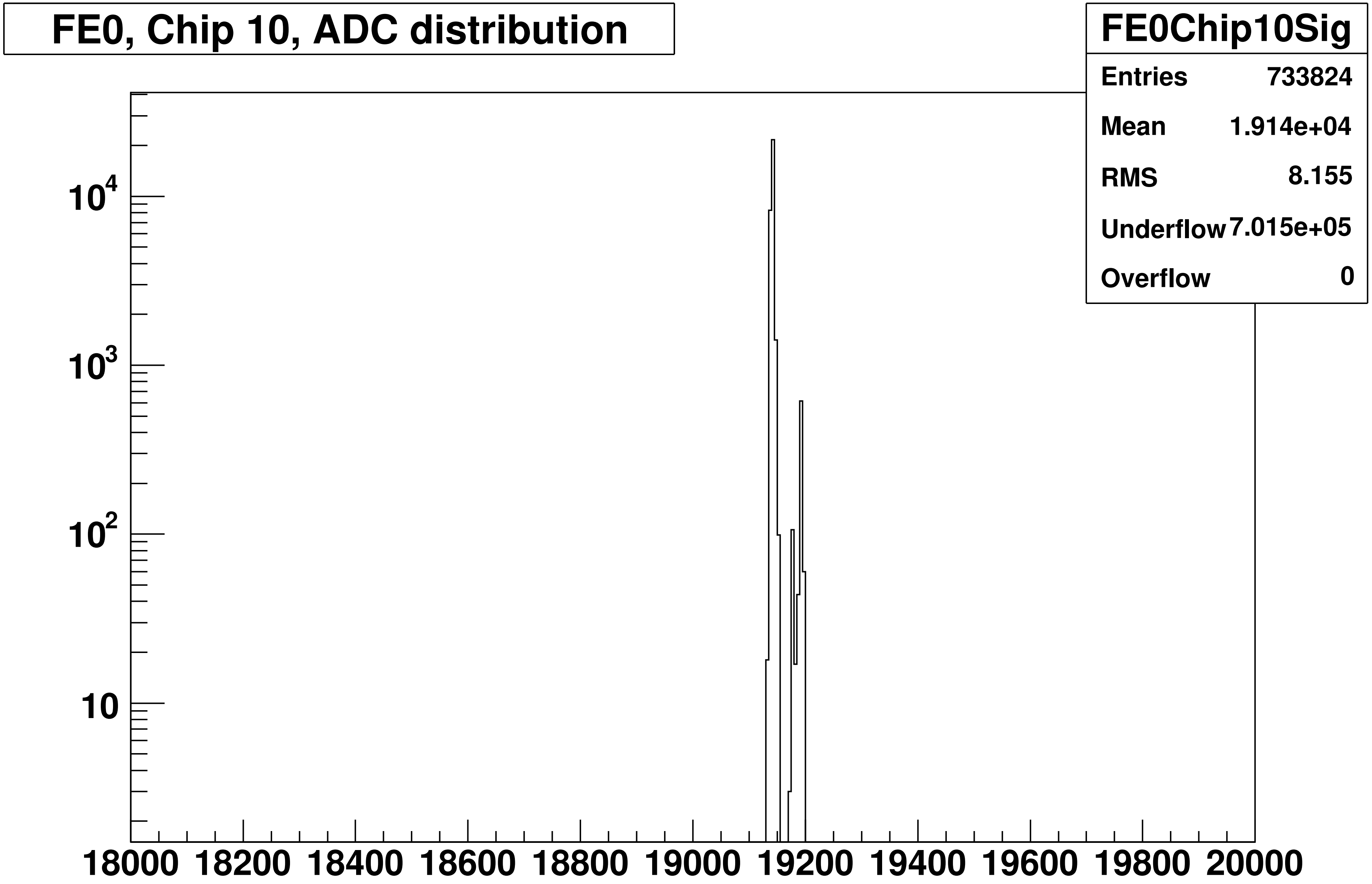
FE0, Chip 10, ADC distribution
FE0Chip10Sig
Entries 733824
Mean 1.914e+04
RMS 8.155
Underflow 7.015e+05
Overflow 0
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10^2
10^3
10^4
18000
18200
18400
18600
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19000
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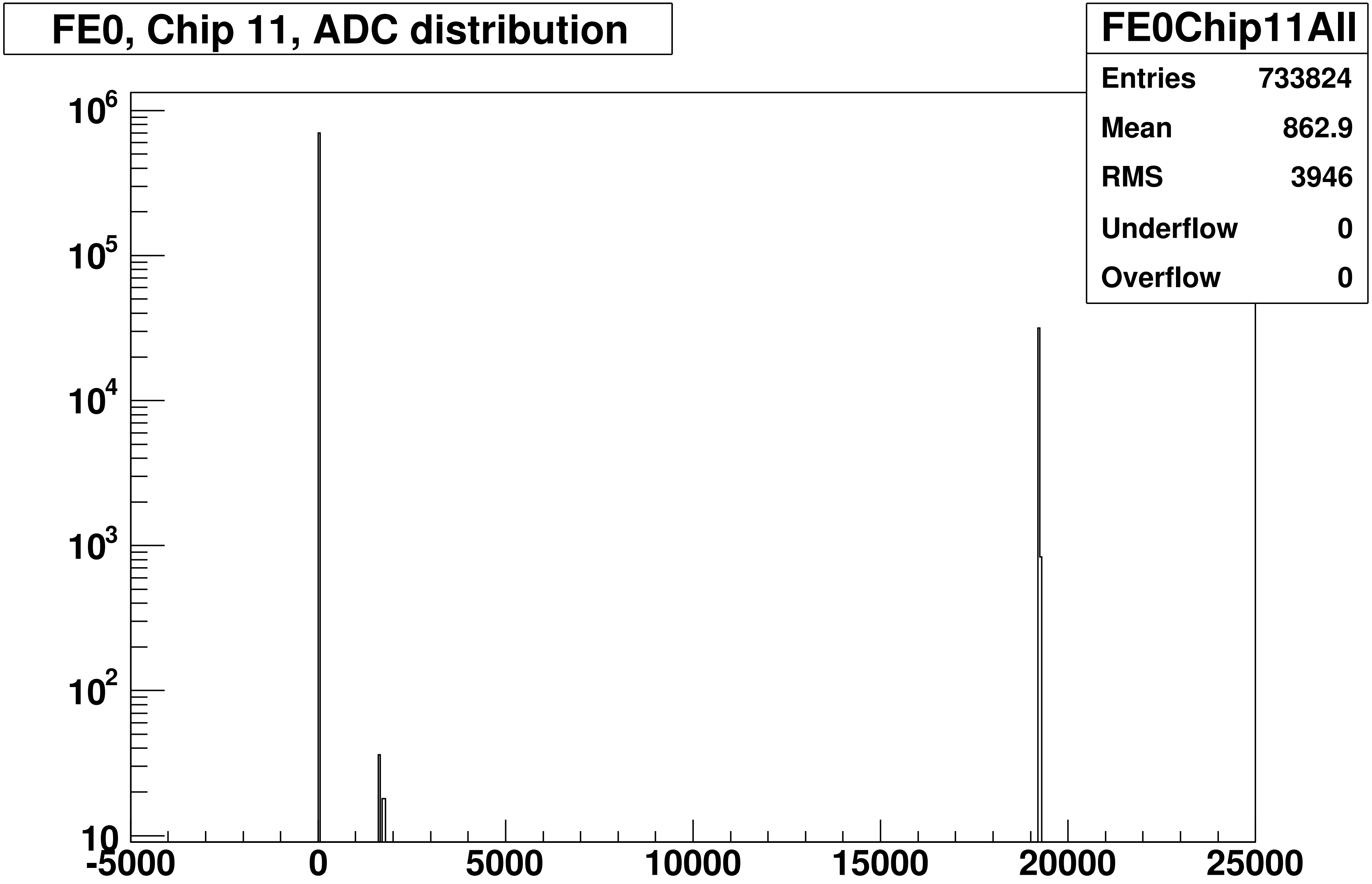

FE0, Chip 11, ADC distribution
FE0Chip11All
Entries 733824
Mean 862.9
RMS 3946
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
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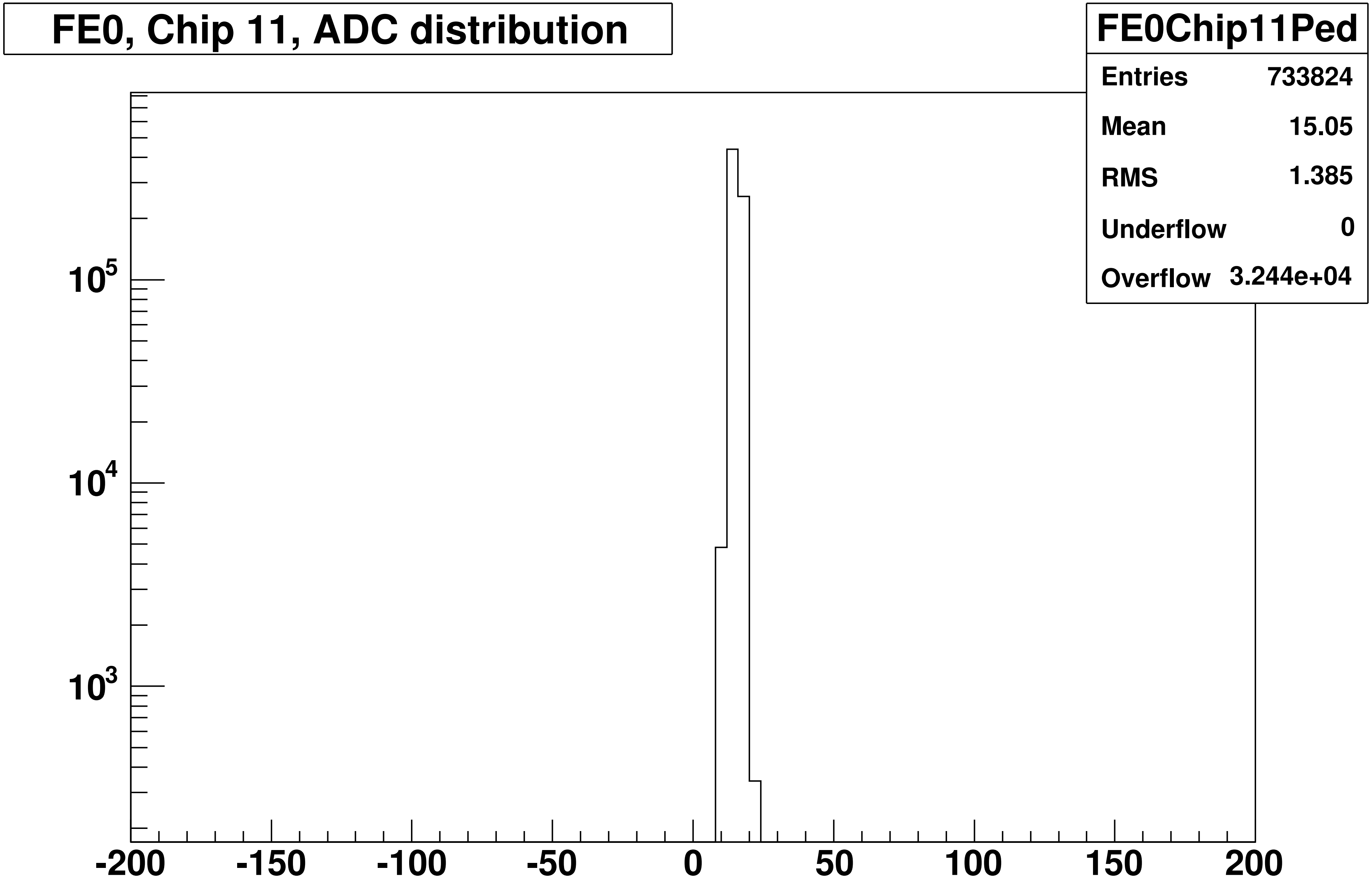
FE0, Chip 11, ADC distribution
FE0Chip11Ped
Entries 733824
Mean 15.05
RMS 1.385
Underflow 0
Overflow 3.244e+04
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10^4
10^3
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-100
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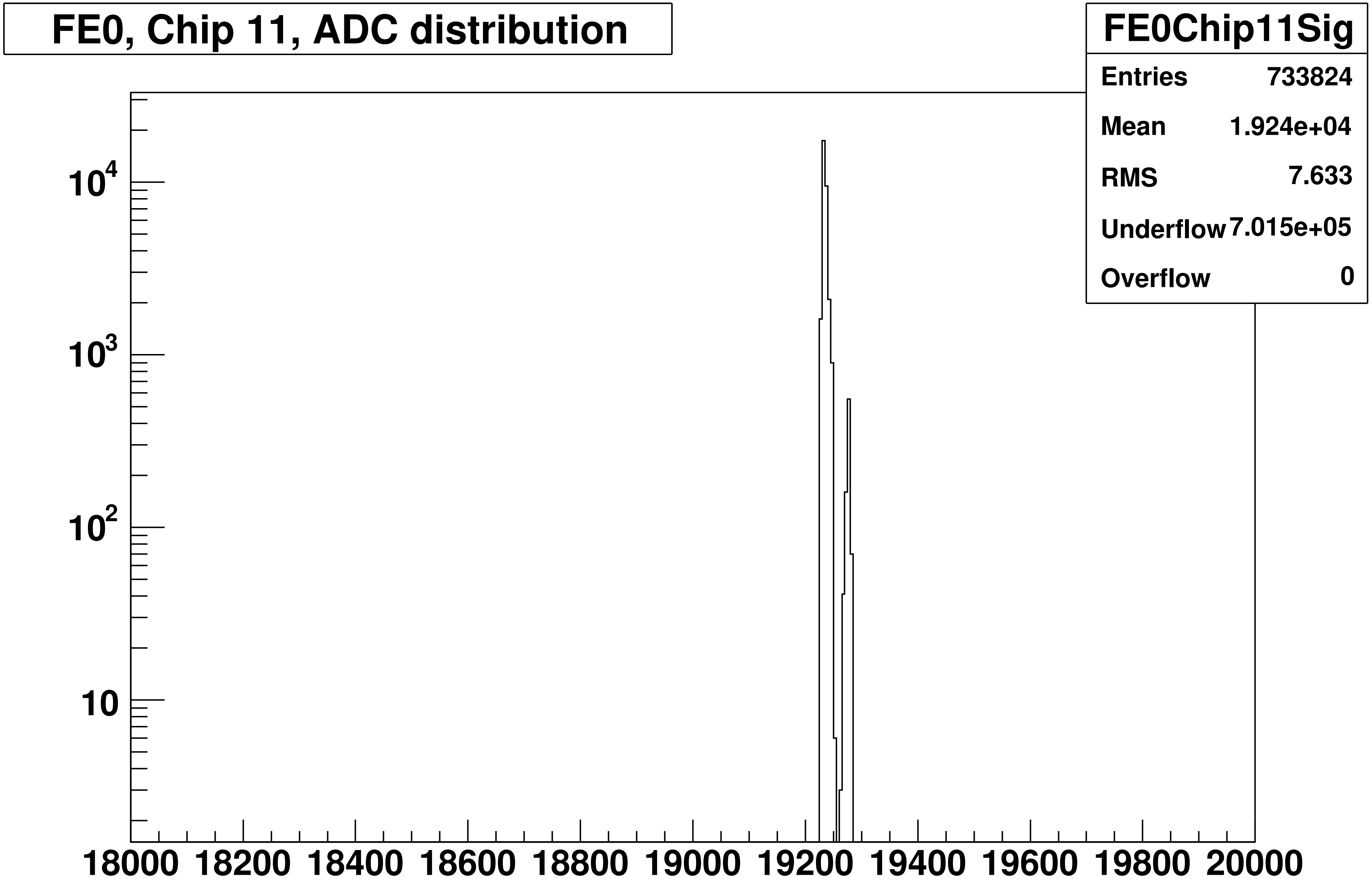
150
200



FE0, Chip 11, ADC distribution
FE0Chip11Sig
Entries 733824
Mean 1.924e+04
RMS 7.633
Underflow 7.015e+05
Overflow 0
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10^3
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10
18000
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18400
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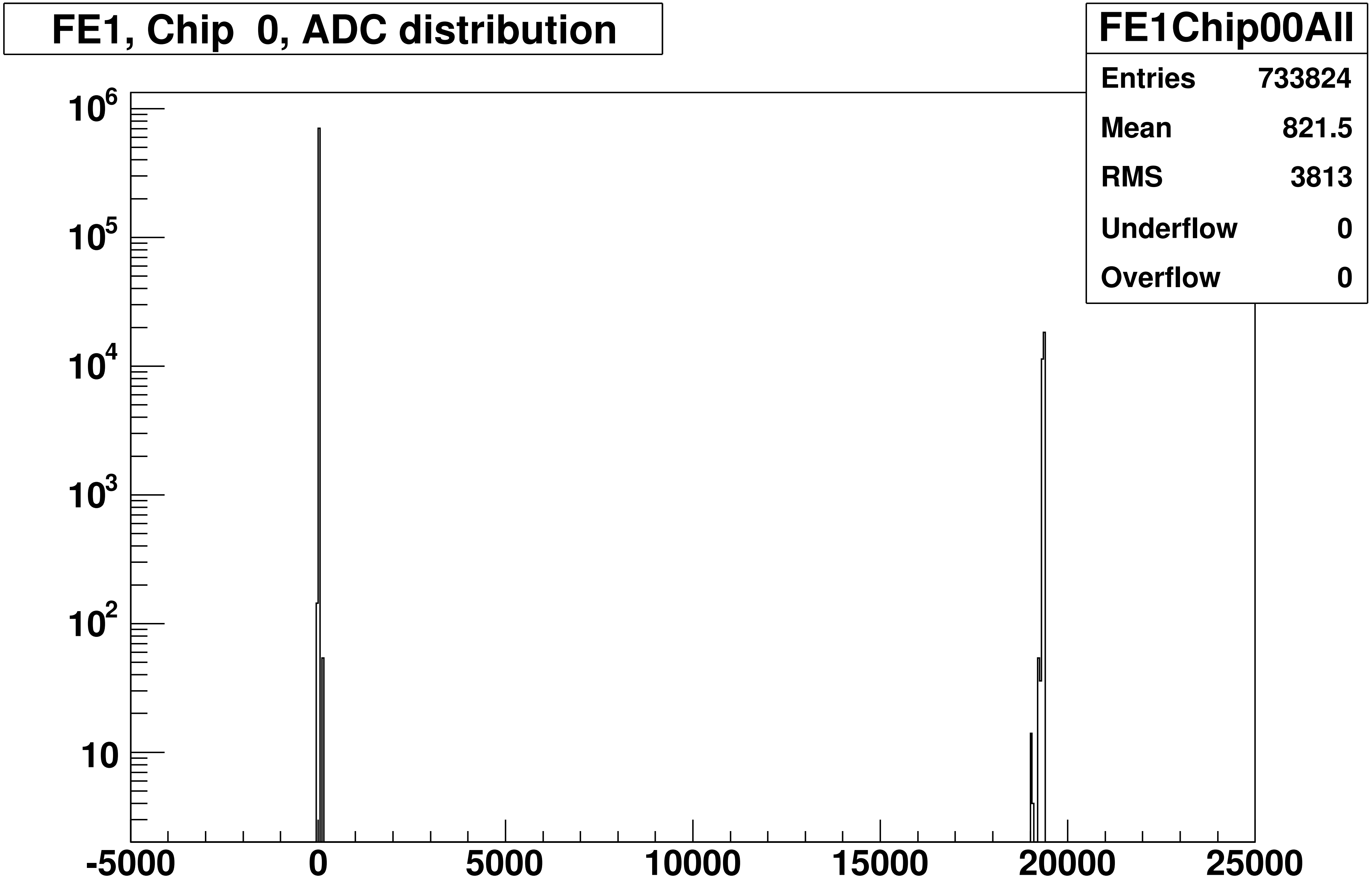

FE1, Chip 0, ADC distribution
FE1Chip00All
Entries 733824
Mean 821.5
RMS 3813
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
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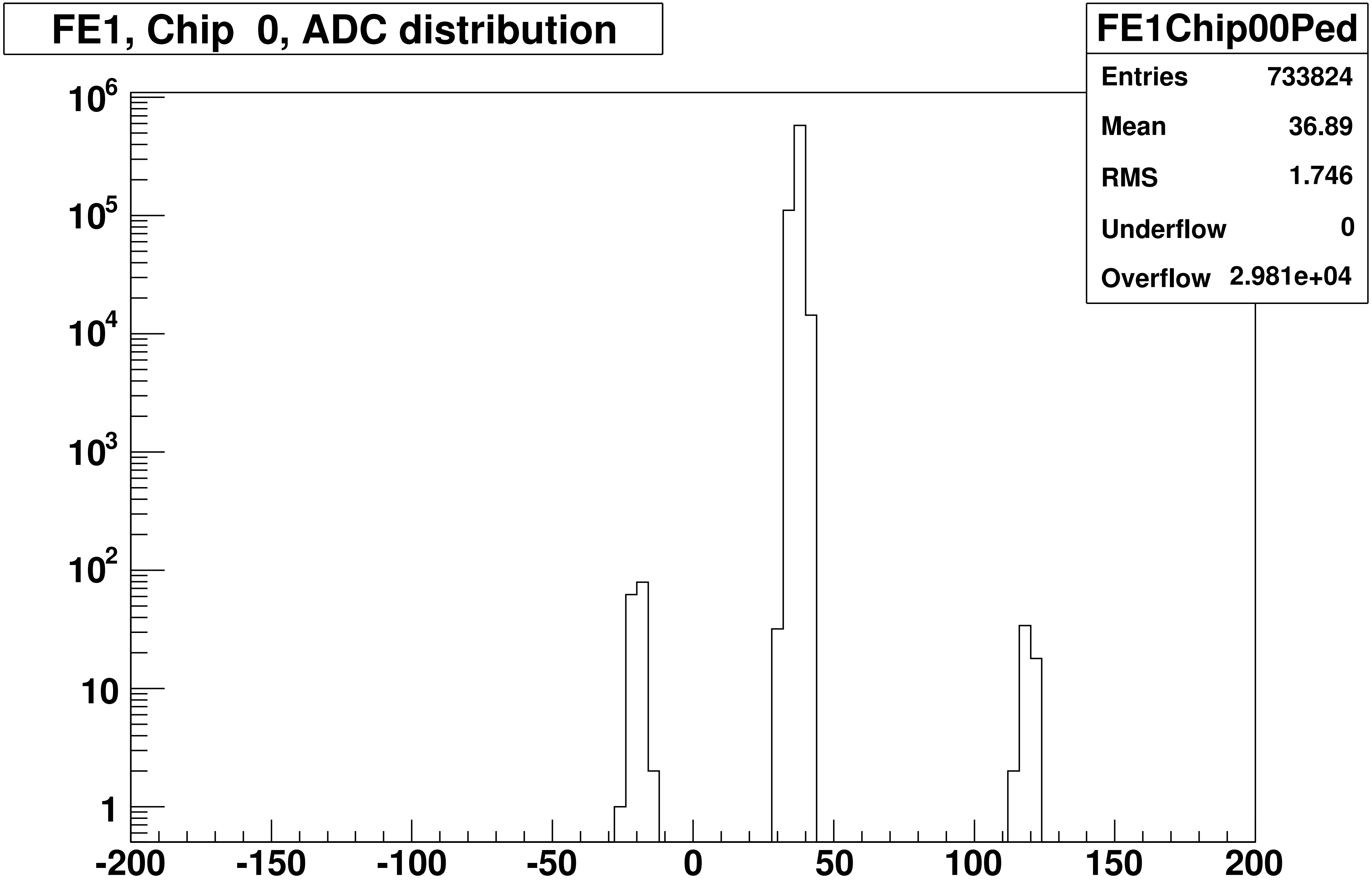
FE1, Chip 0, ADC distribution
FE1Chip00Ped
Entries 733824
Mean 36.89
RMS 1.746
Underflow 0
Overflow 2.981e+04
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10^3
10^2
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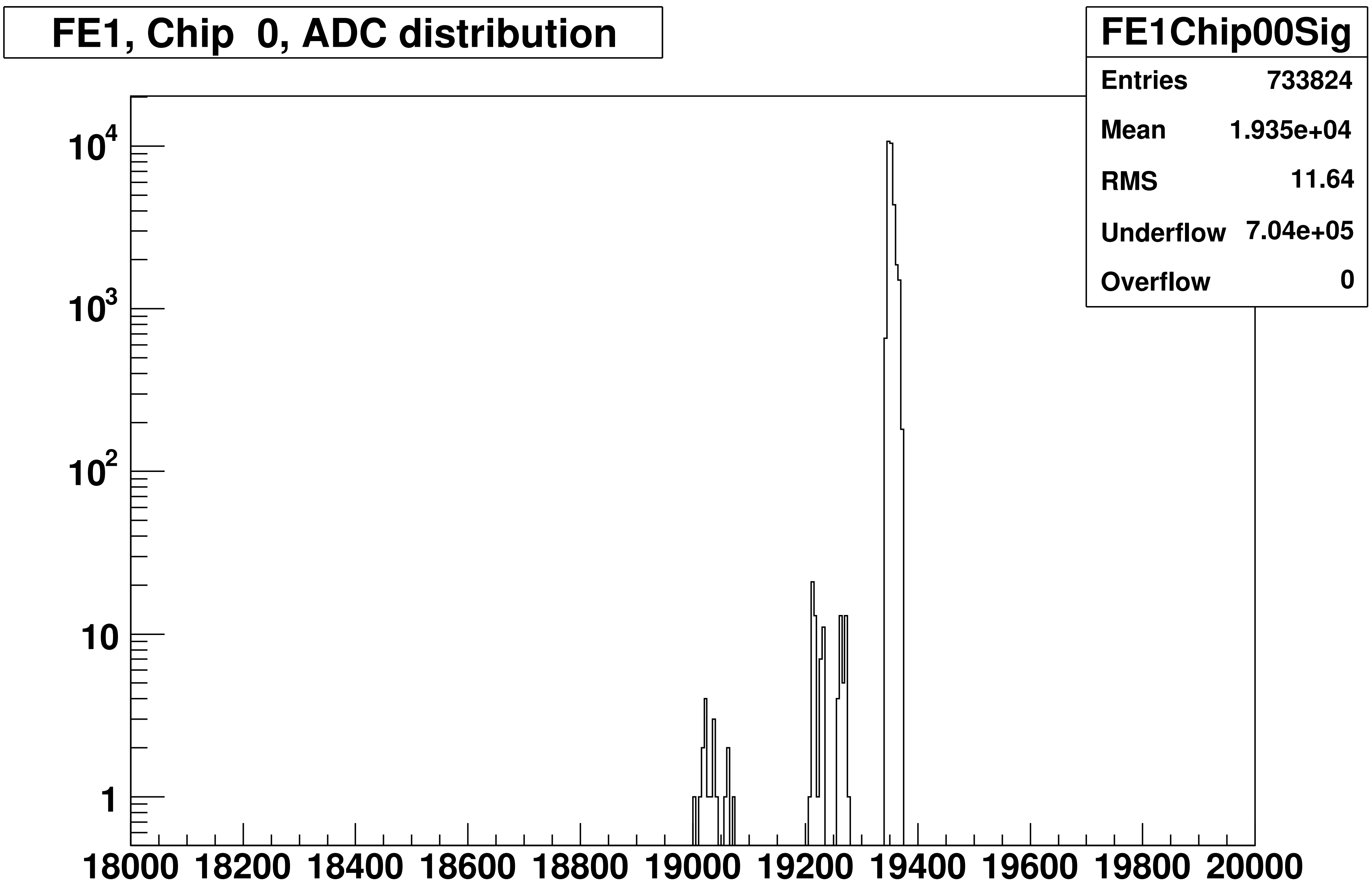
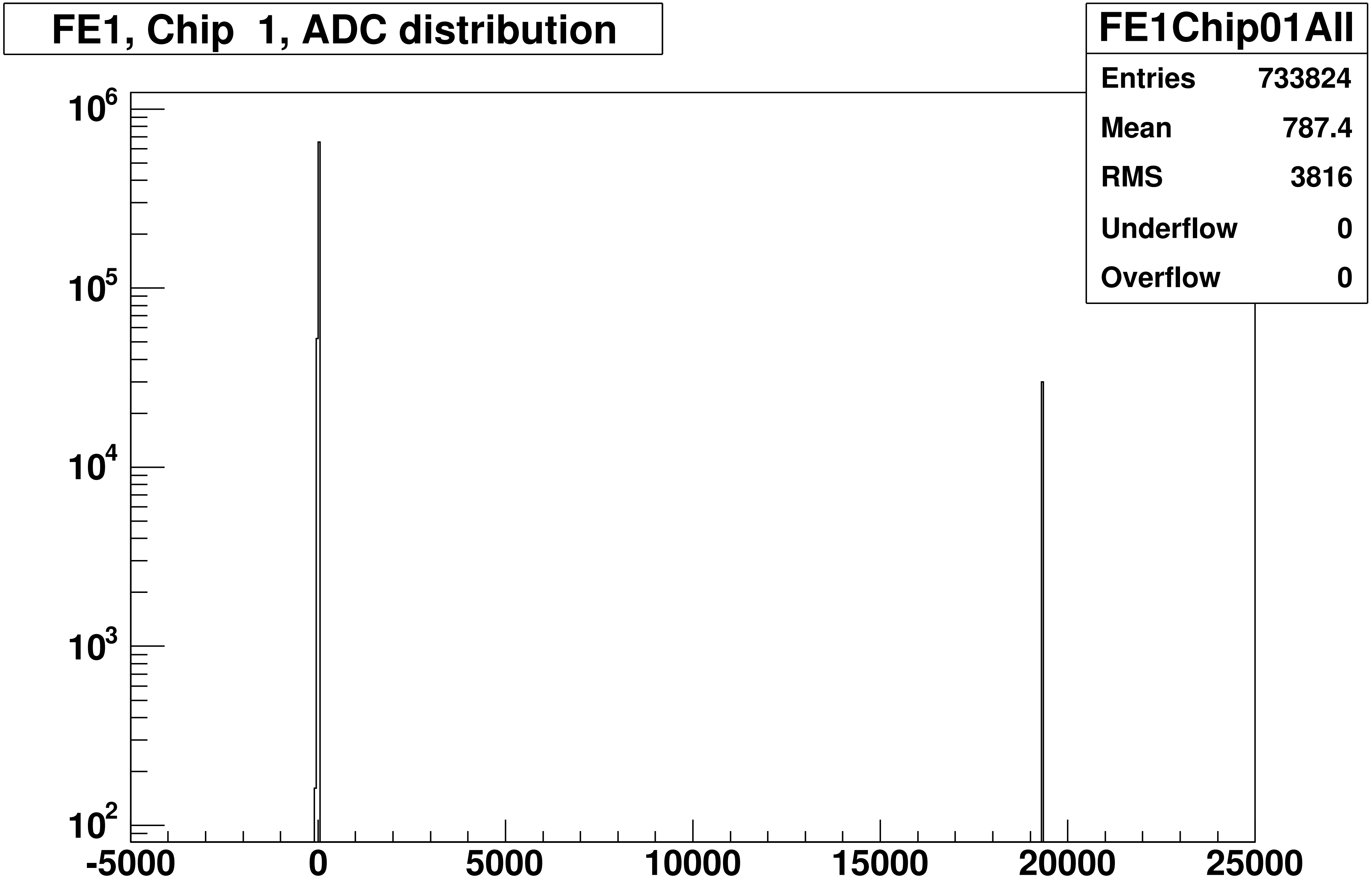
150
200


FE1, Chip 0, ADC distribution
FE1Chip00Sig
Entries 733824
Mean 1.935e+04
RMS 11.64
Underflow 7.04e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE1, Chip 1, ADC distribution
FE1Chip01All
Entries 733824
Mean 787.4
RMS 3816
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
-5000
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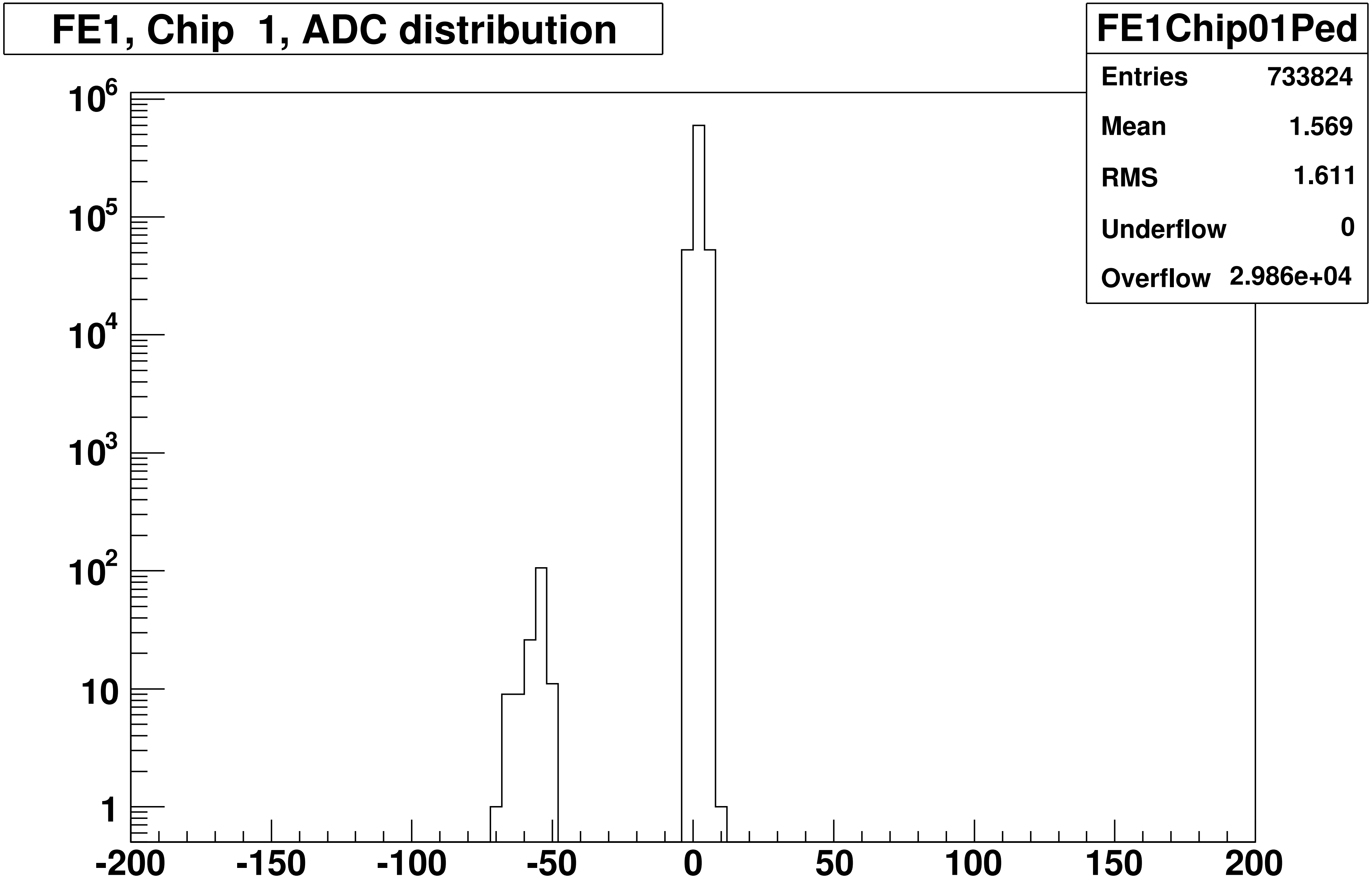
20000
25000



FE1, Chip 1, ADC distribution
FE1Chip01Ped
Entries 733824
Mean 1.569
RMS 1.611
Underflow 0
Overflow 2.986e+04
10^6
10^5
10^4
10^3
10^2
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1
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0
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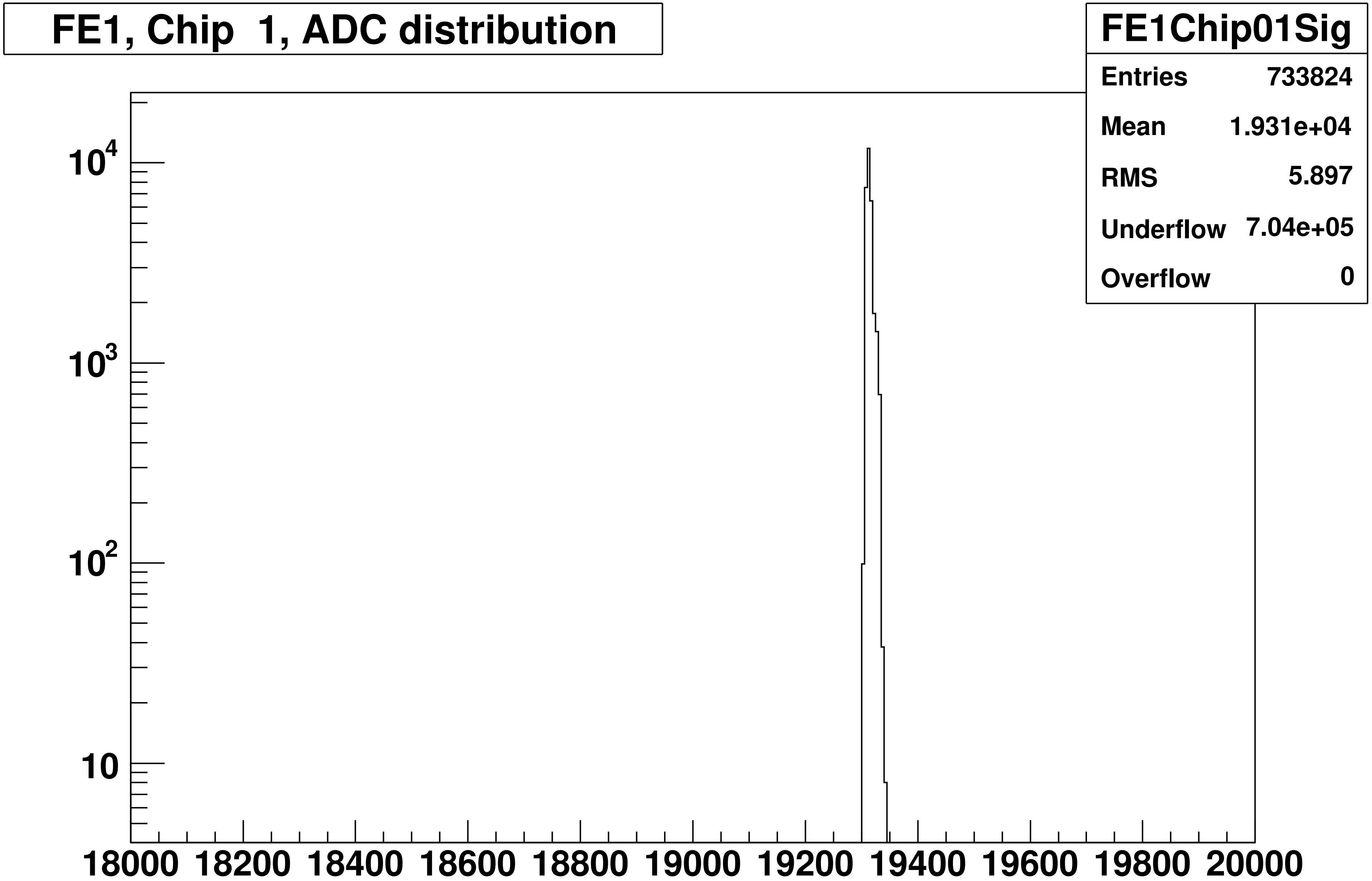
100
150
200


FE1, Chip 1, ADC distribution
FE1Chip01Sig
Entries 733824
Mean 1.931e+04
RMS 5.897
Underflow 7.04e+05
Overflow 0
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10^3
10^2
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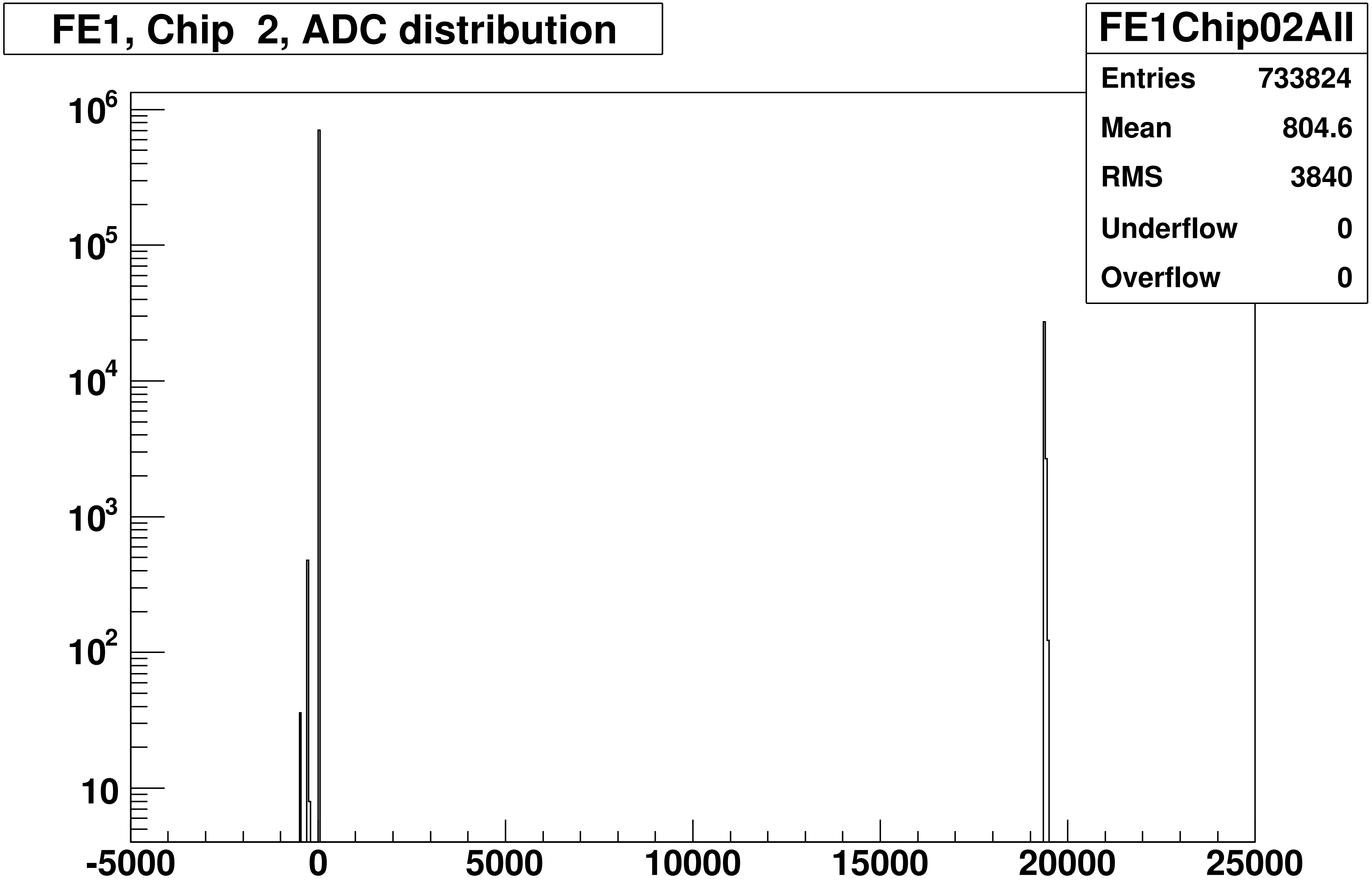
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE1, Chip 2, ADC distribution
FE1Chip02All
Entries 733824
Mean 804.6
RMS 3840
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
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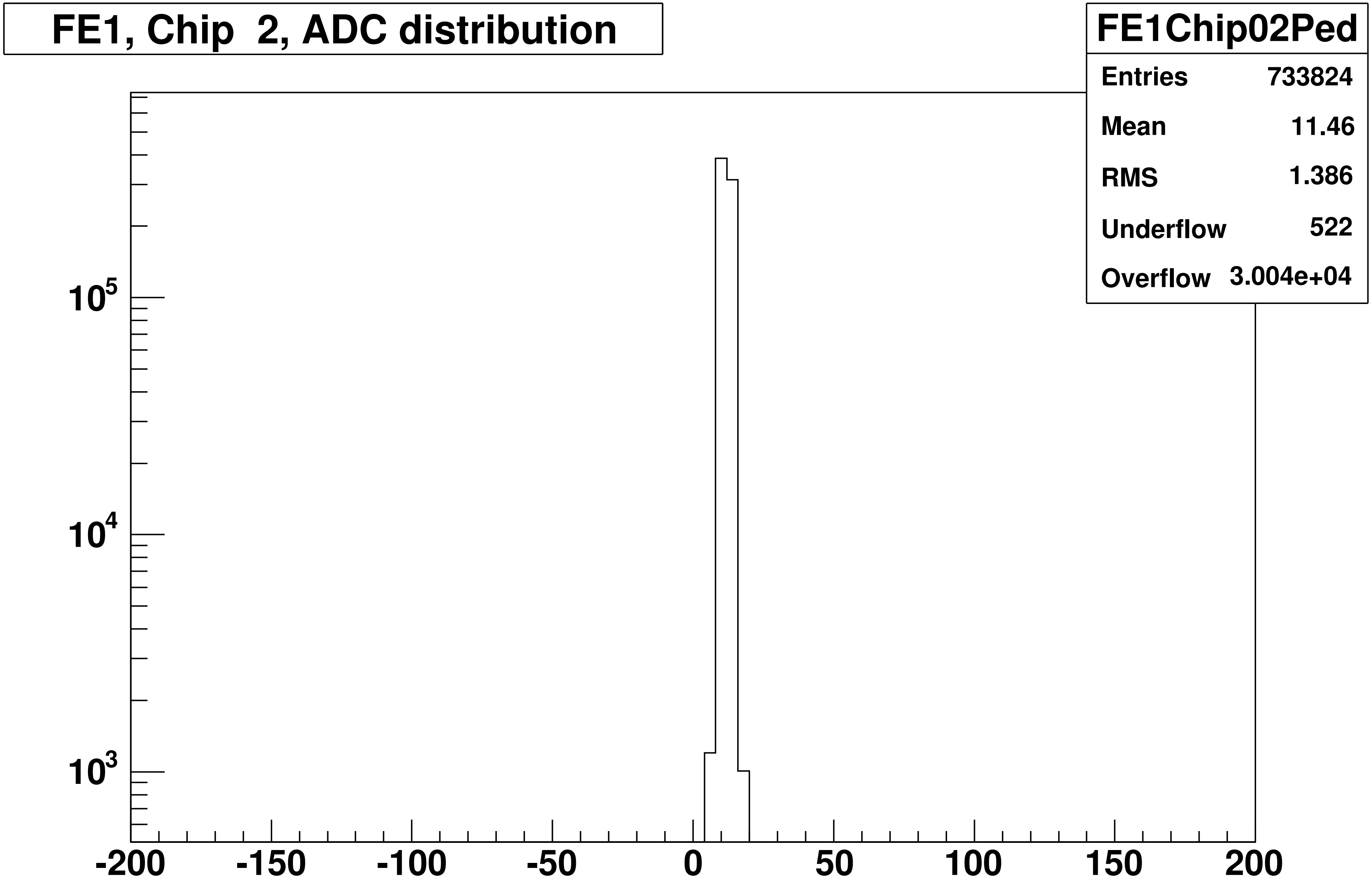
FE1, Chip 2, ADC distribution
FE1Chip02Ped
Entries 733824
Mean 11.46
RMS 1.386
Underflow 522
Overflow 3.004e+04
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10^4
10^3
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150
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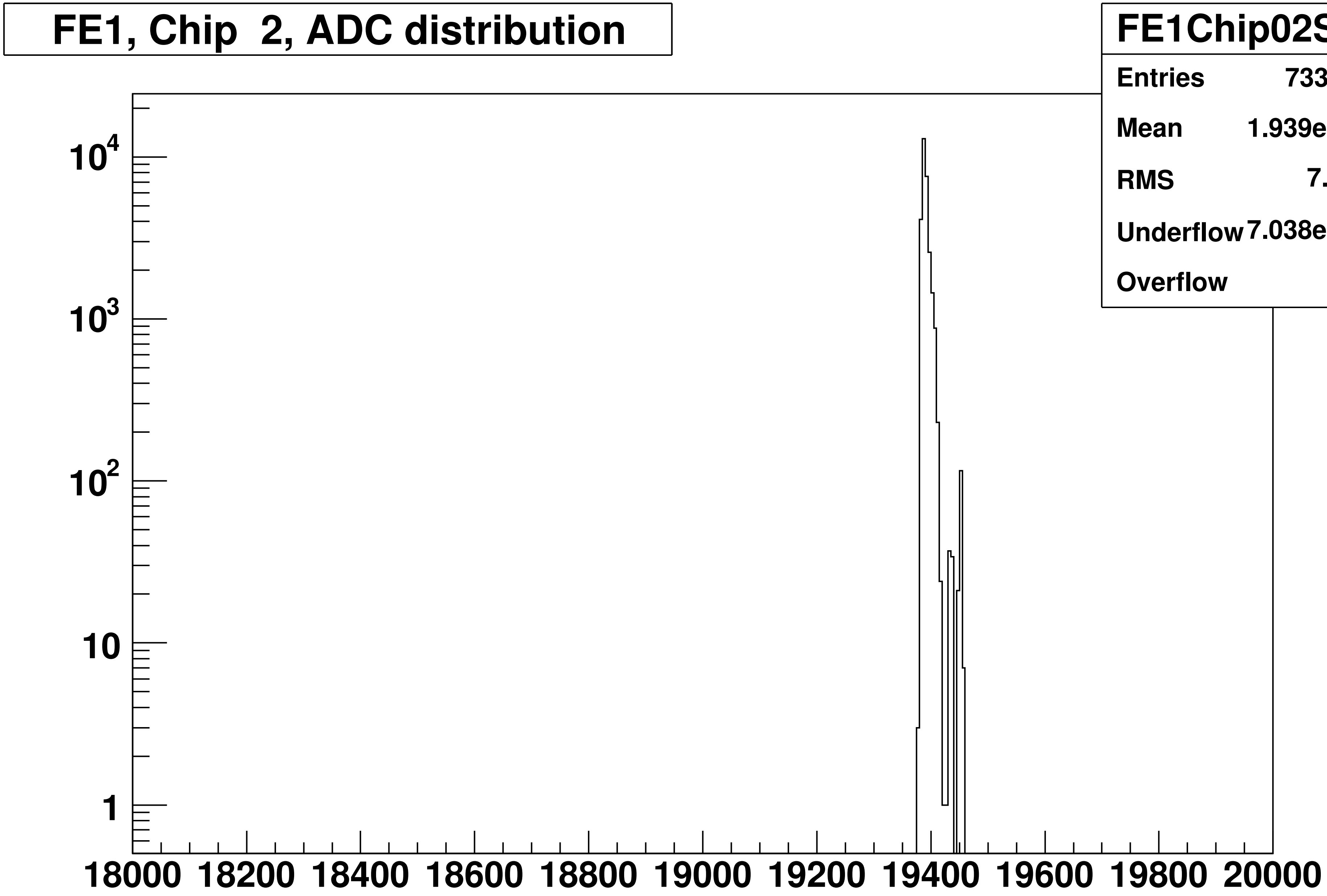
FE1, Chip 2, ADC distribution
FE1Chip02Sig
Entries 733824
Mean 1.939e+04
RMS 7.595
Underflow 7.038e+05
Overflow 0
10^4
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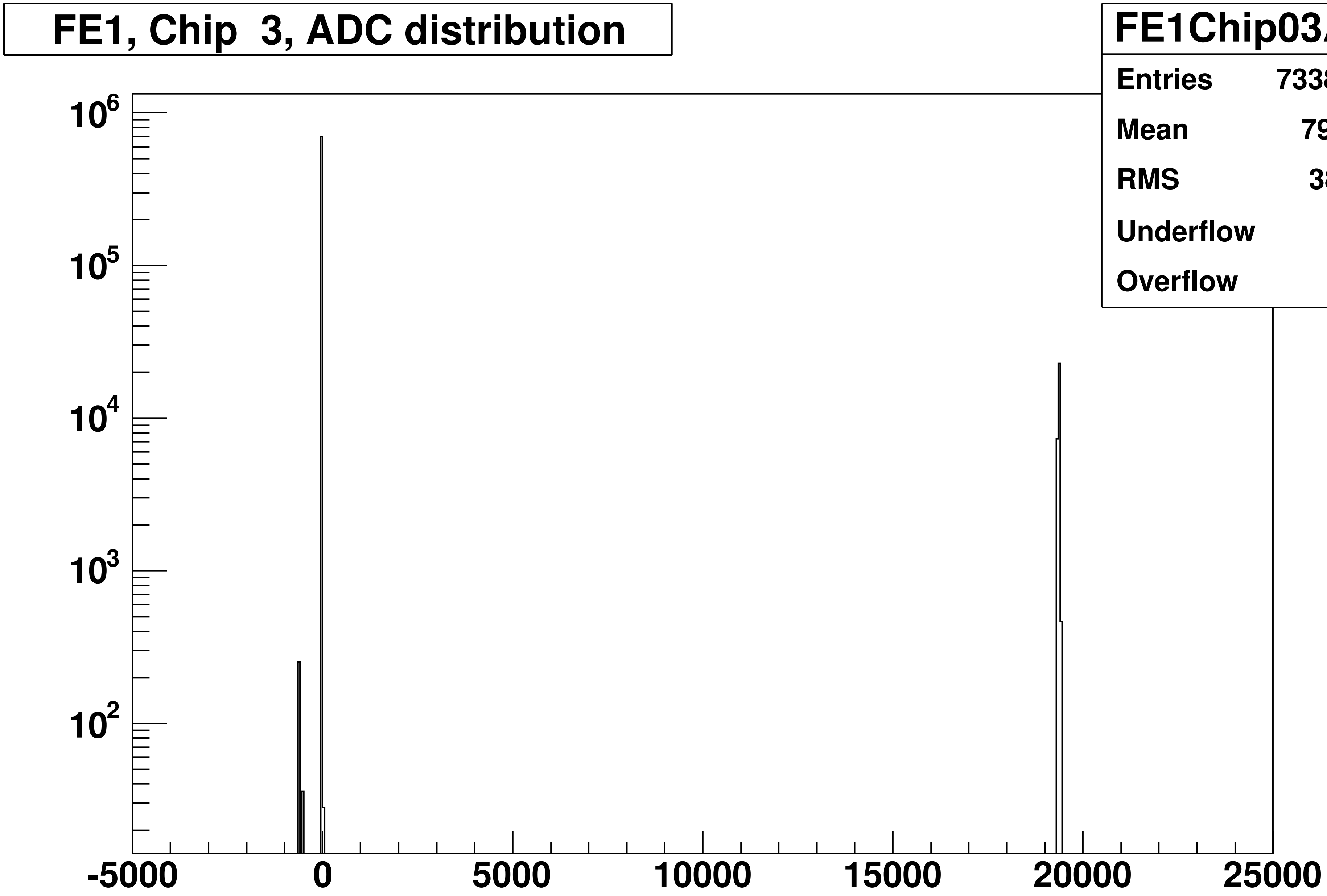
FE1, Chip 3, ADC distribution
FE1Chip03All
Entries 733824
Mean 799.3
RMS 3866
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
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20000
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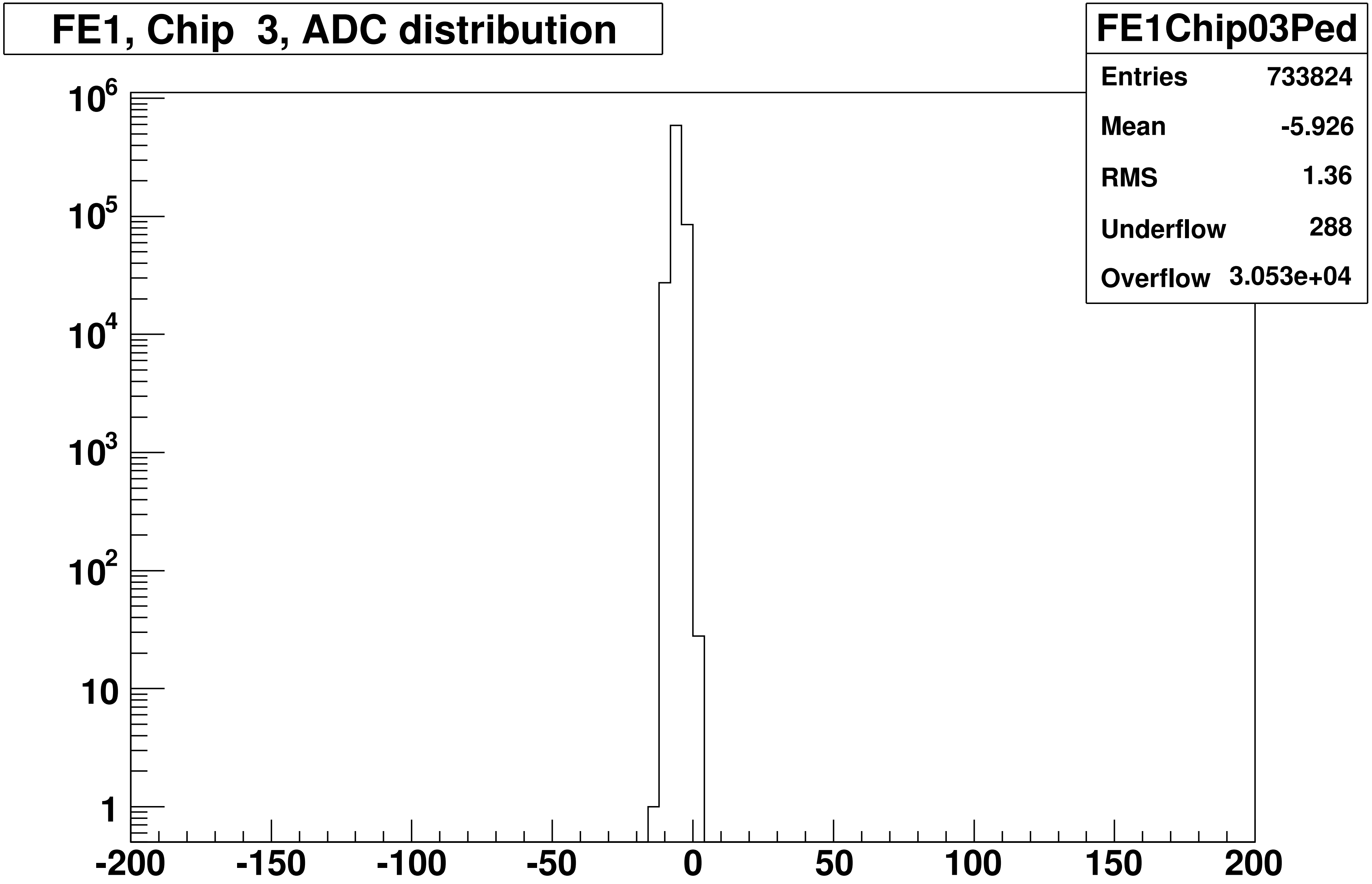

FE1, Chip 3, ADC distribution
FE1Chip03Ped
Entries 733824
Mean -5.926
RMS 1.36
Underflow 288
Overflow 3.053e+04
10^6
10^5
10^4
10^3
10^2
10
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0
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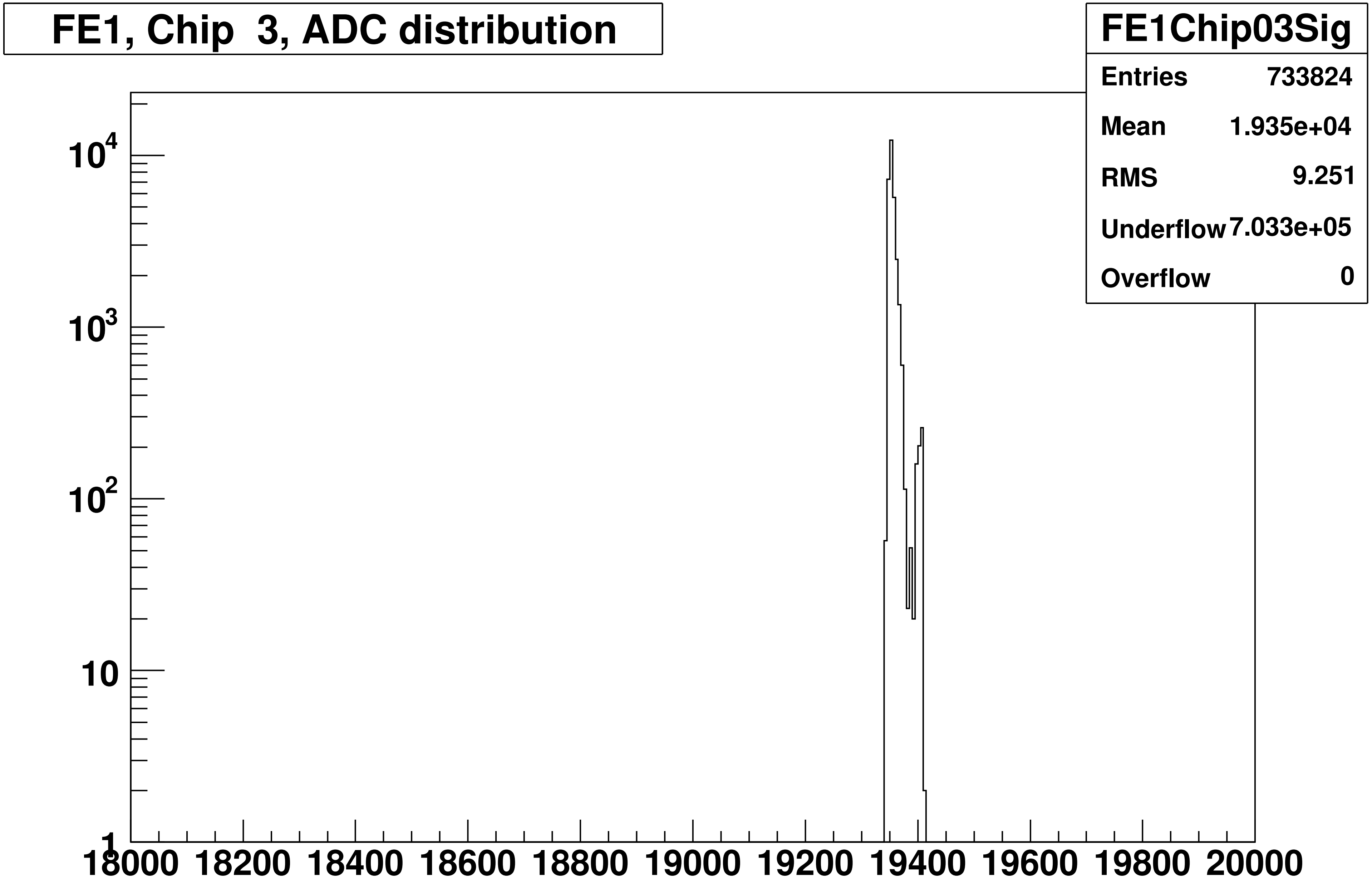
100
150
200


FE1, Chip 3, ADC distribution
FE1Chip03Sig
Entries 733824
Mean 1.935e+04
RMS 9.251
Underflow 7.033e+05
Overflow 0
10^4
10^3
10^2
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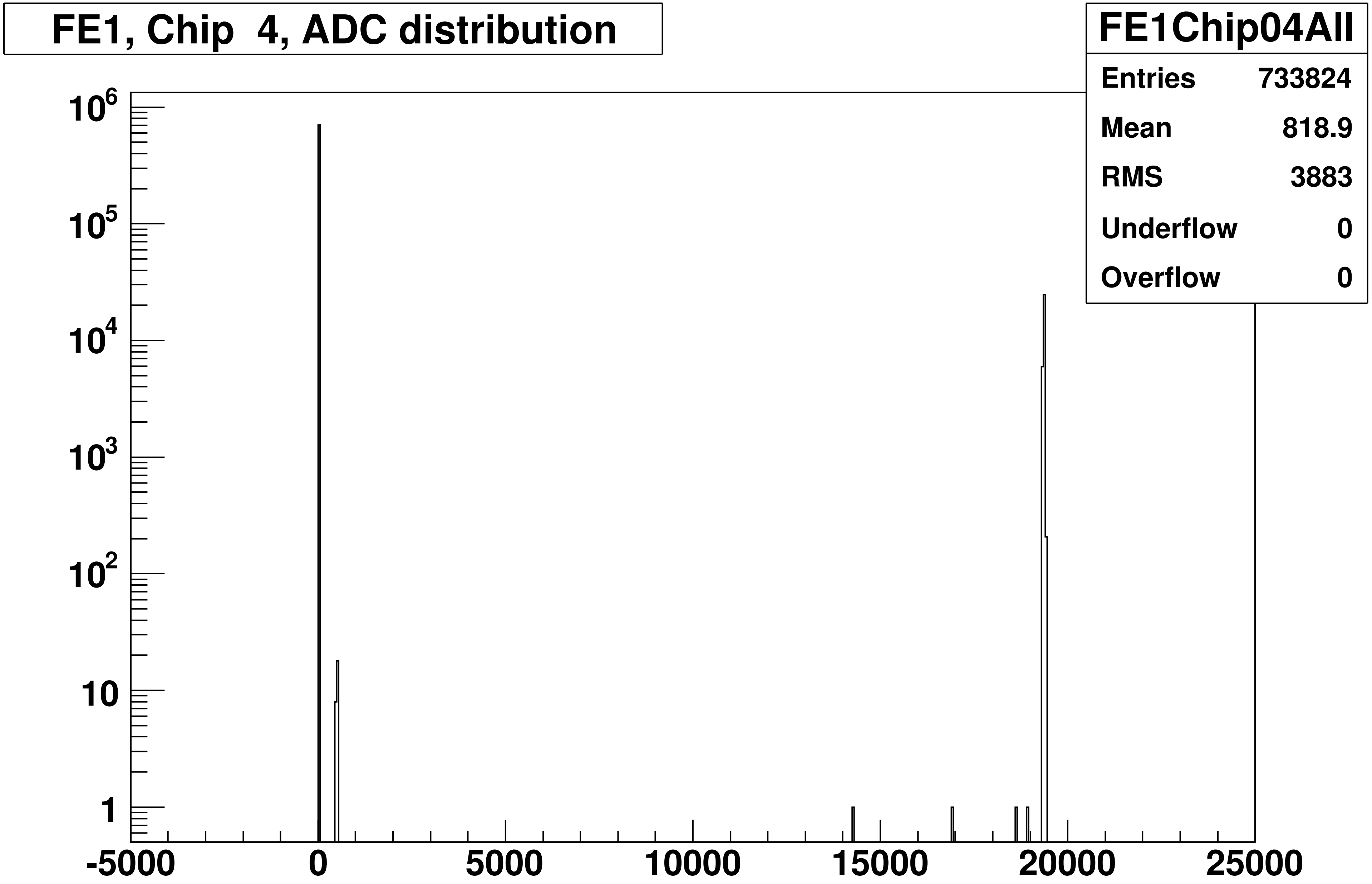
FE1, Chip 4, ADC distribution
FE1Chip04All
Entries 733824
Mean 818.9
RMS 3883
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
1
-5000
0
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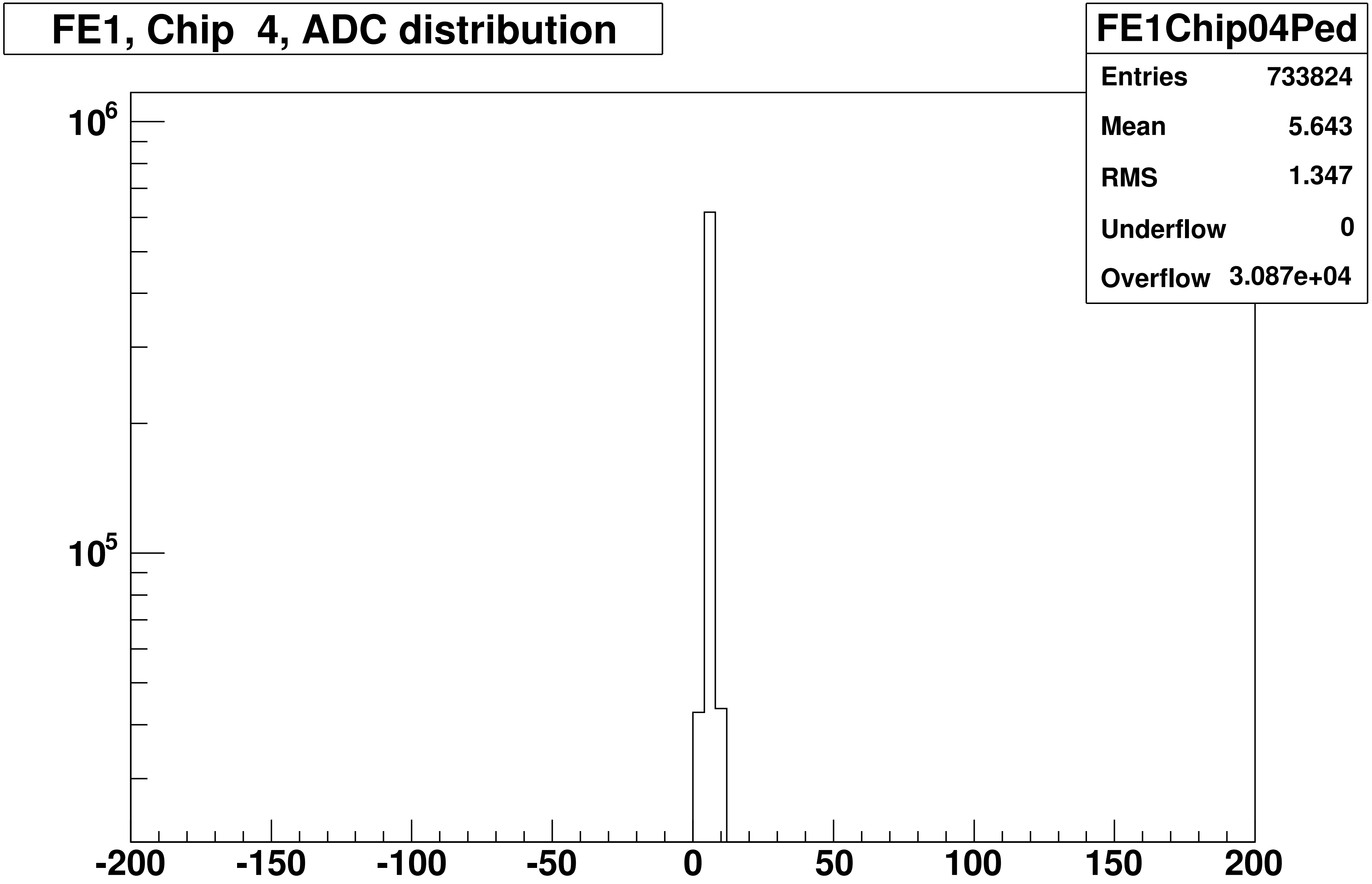
10000
15000
20000
25000


FE1, Chip 4, ADC distribution
FE1Chip04Ped
Entries 733824
Mean 5.643
RMS 1.347
Underflow 0
Overflow 3.087e+04
10^6
10^5
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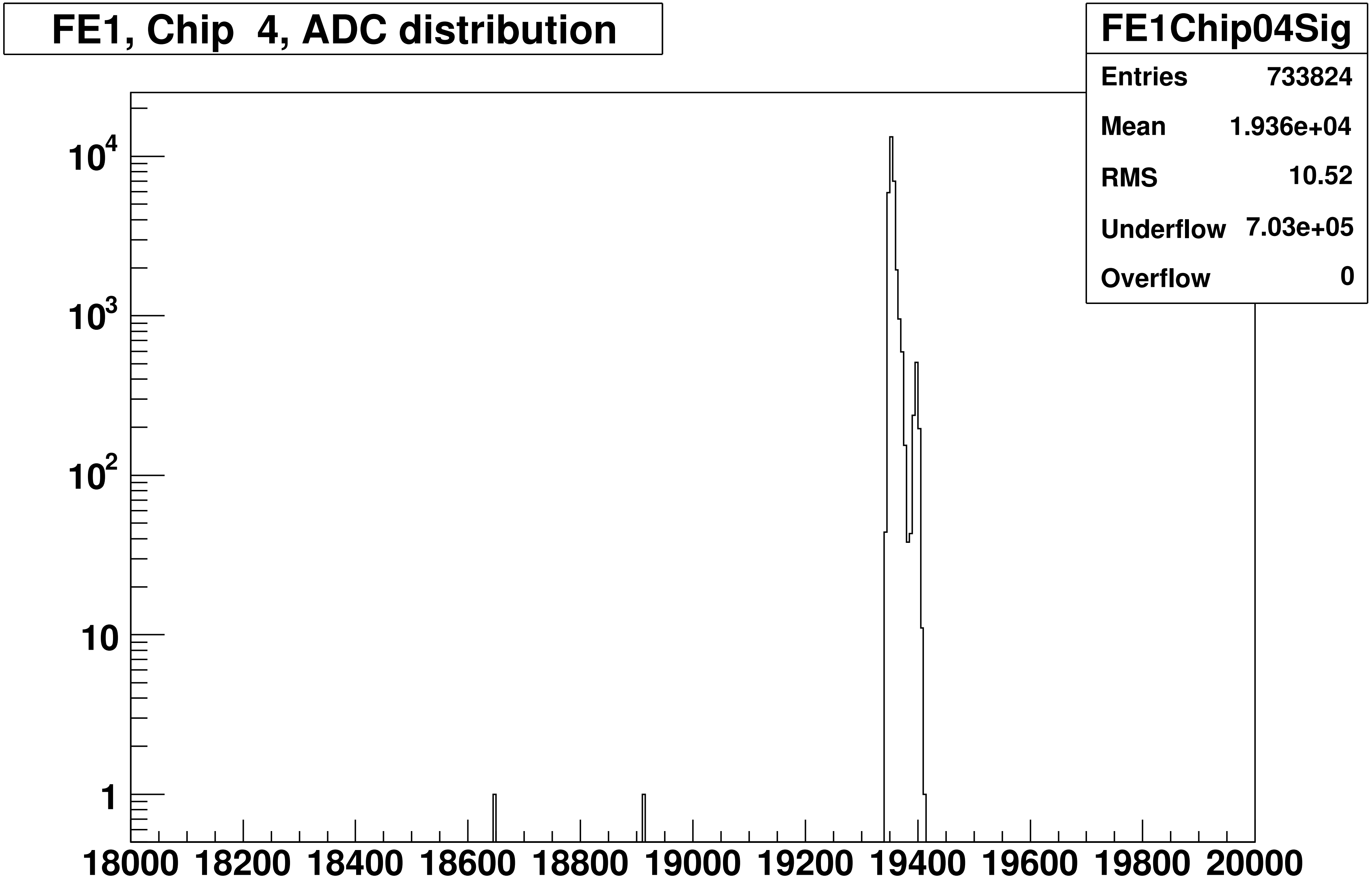
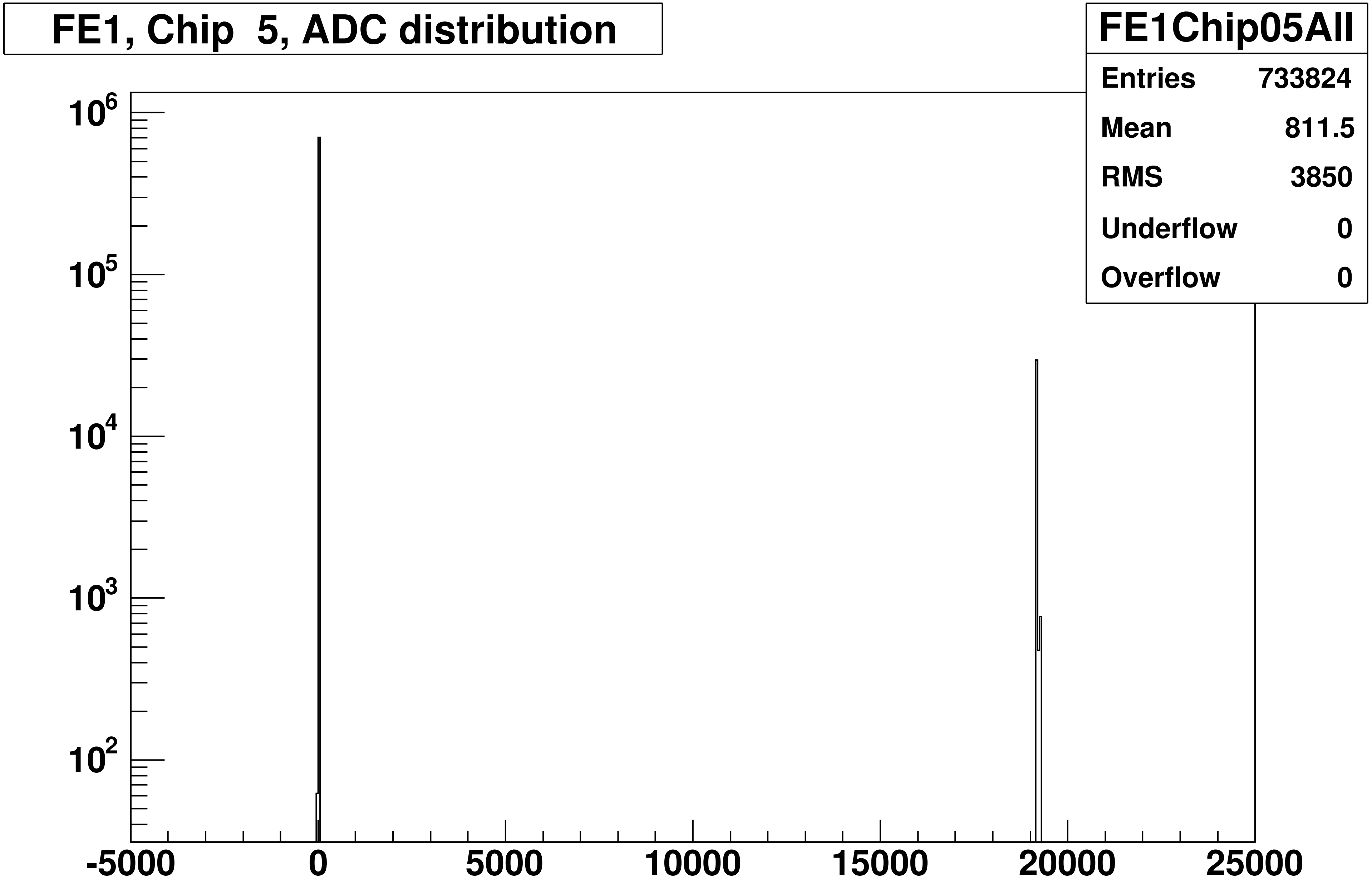
-50
0
50
100
150
200



FE1, Chip 4, ADC distribution
FE1Chip04Sig
Entries 733824
Mean 1.936e+04
RMS 10.52
Underflow 7.03e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE1, Chip 5, ADC distribution
FE1Chip05All
Entries 733824
Mean 811.5
RMS 3850
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
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0
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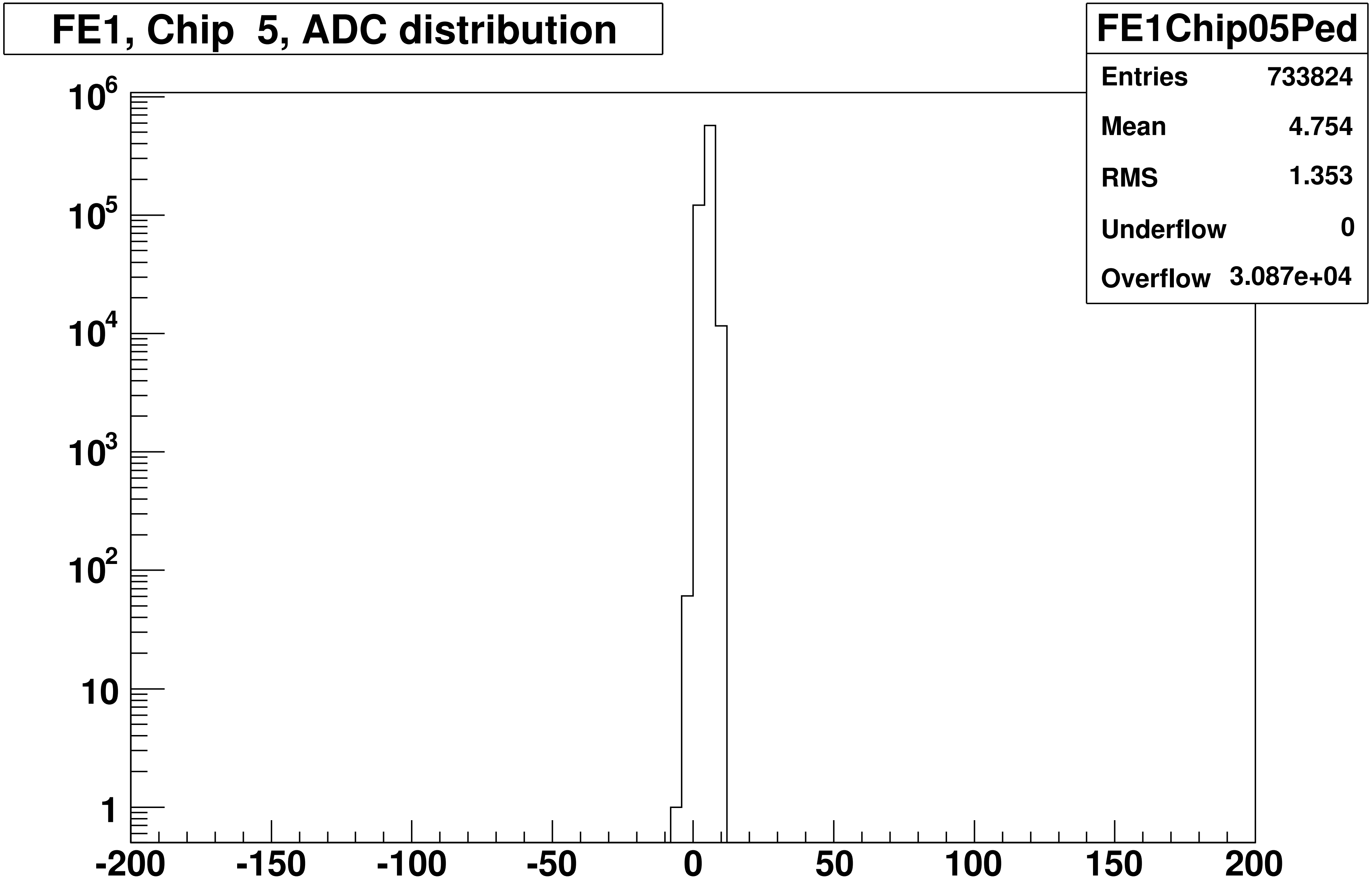
10000
15000
20000
25000



FE1, Chip 5, ADC distribution
FE1Chip05Ped
Entries 733824
Mean 4.754
RMS 1.353
Underflow 0
Overflow 3.087e+04
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10^5
10^4
10^3
10^2
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0
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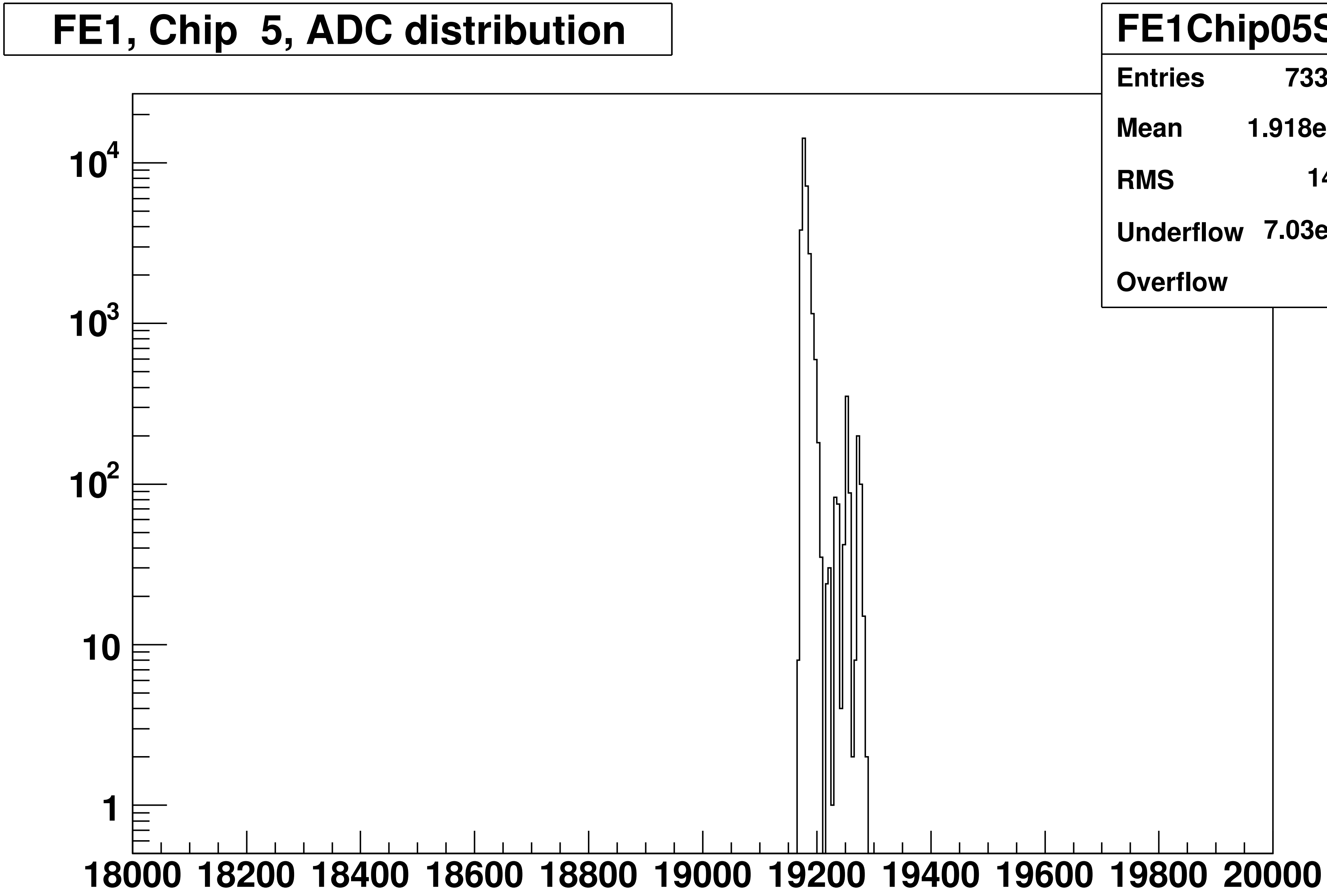
100
150
200


FE1, Chip 5, ADC distribution
FE1Chip05Sig
Entries 733824
Mean 1.918e+04
RMS 14.83
Underflow 7.03e+05
Overflow 0
10^4
10^3
10^2
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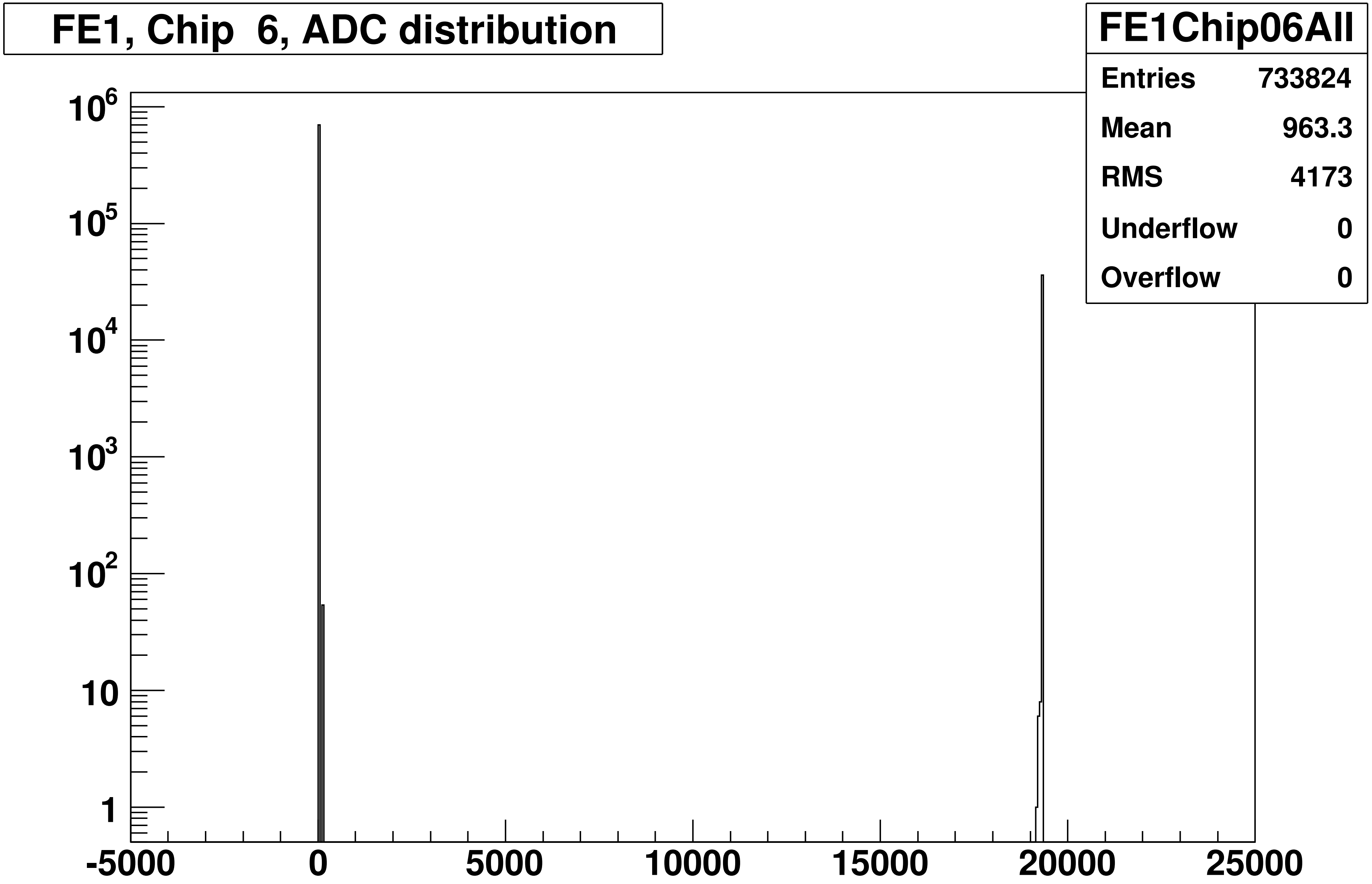
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000



FE1, Chip 6, ADC distribution
FE1Chip06All
Entries 733824
Mean 963.3
RMS 4173
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
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-5000
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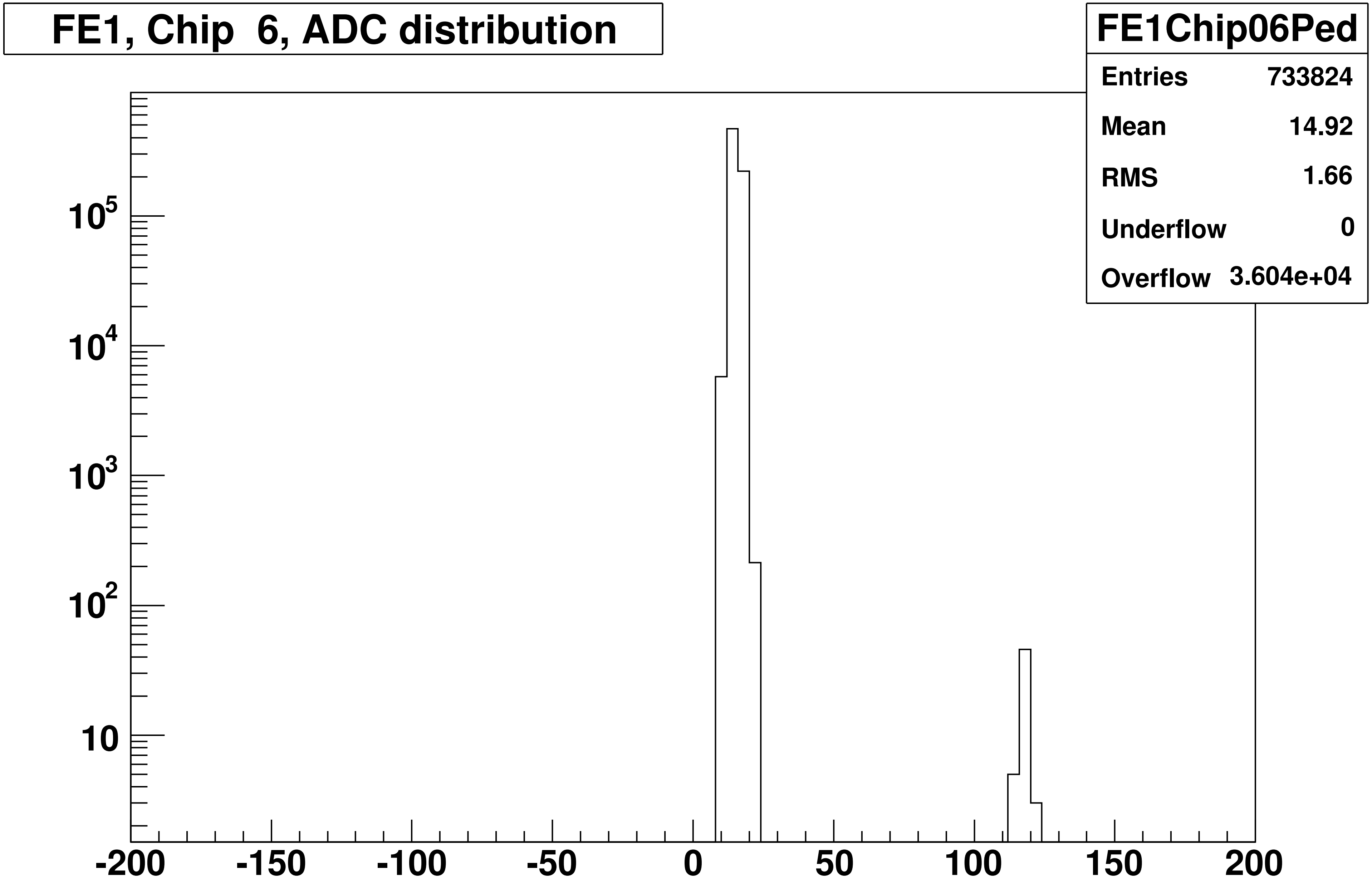
10000
15000
20000
25000


FE1, Chip 6, ADC distribution
FE1Chip06Ped
Entries 733824
Mean 14.92
RMS 1.66
Underflow 0
Overflow 3.604e+04
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10^2
10^3
10^4
10^5
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-100
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0
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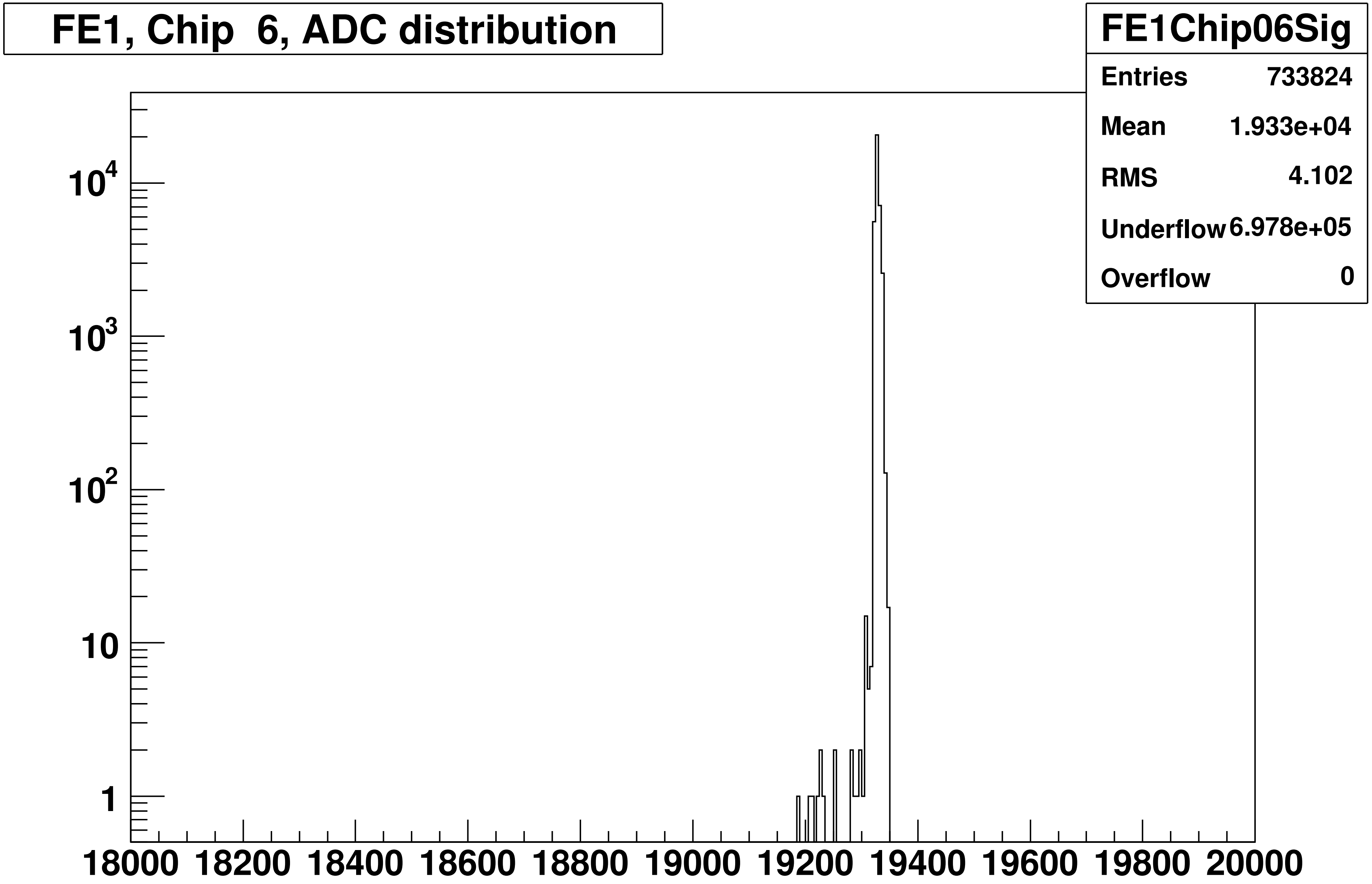
100
150
200


FE1, Chip 6, ADC distribution
FE1Chip06Sig
Entries 733824
Mean 1.933e+04
RMS 4.102
Underflow 6.978e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
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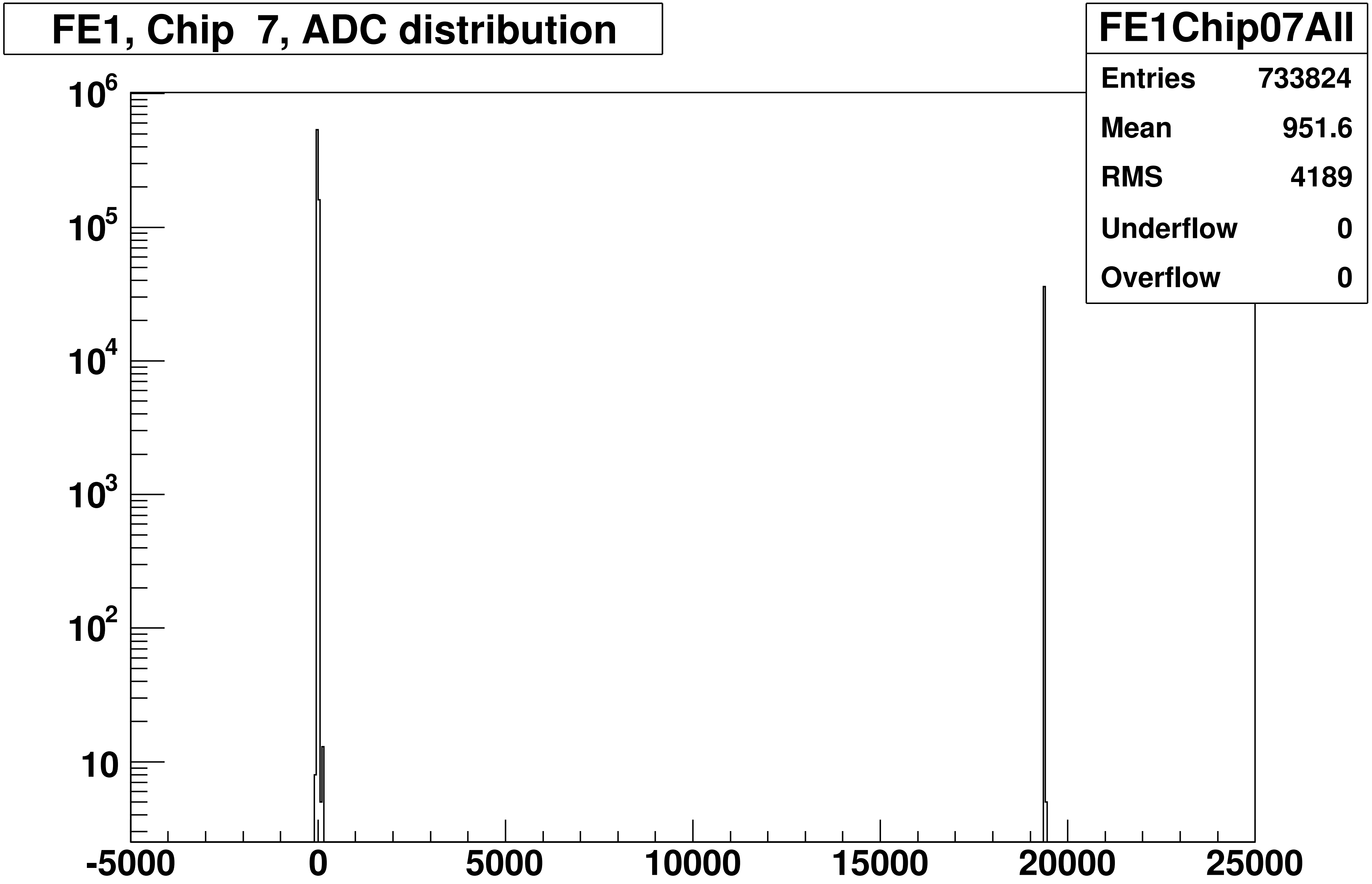
19800
20000


FE1, Chip 7, ADC distribution
FE1Chip07All
Entries 733824
Mean 951.6
RMS 4189
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
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-5000
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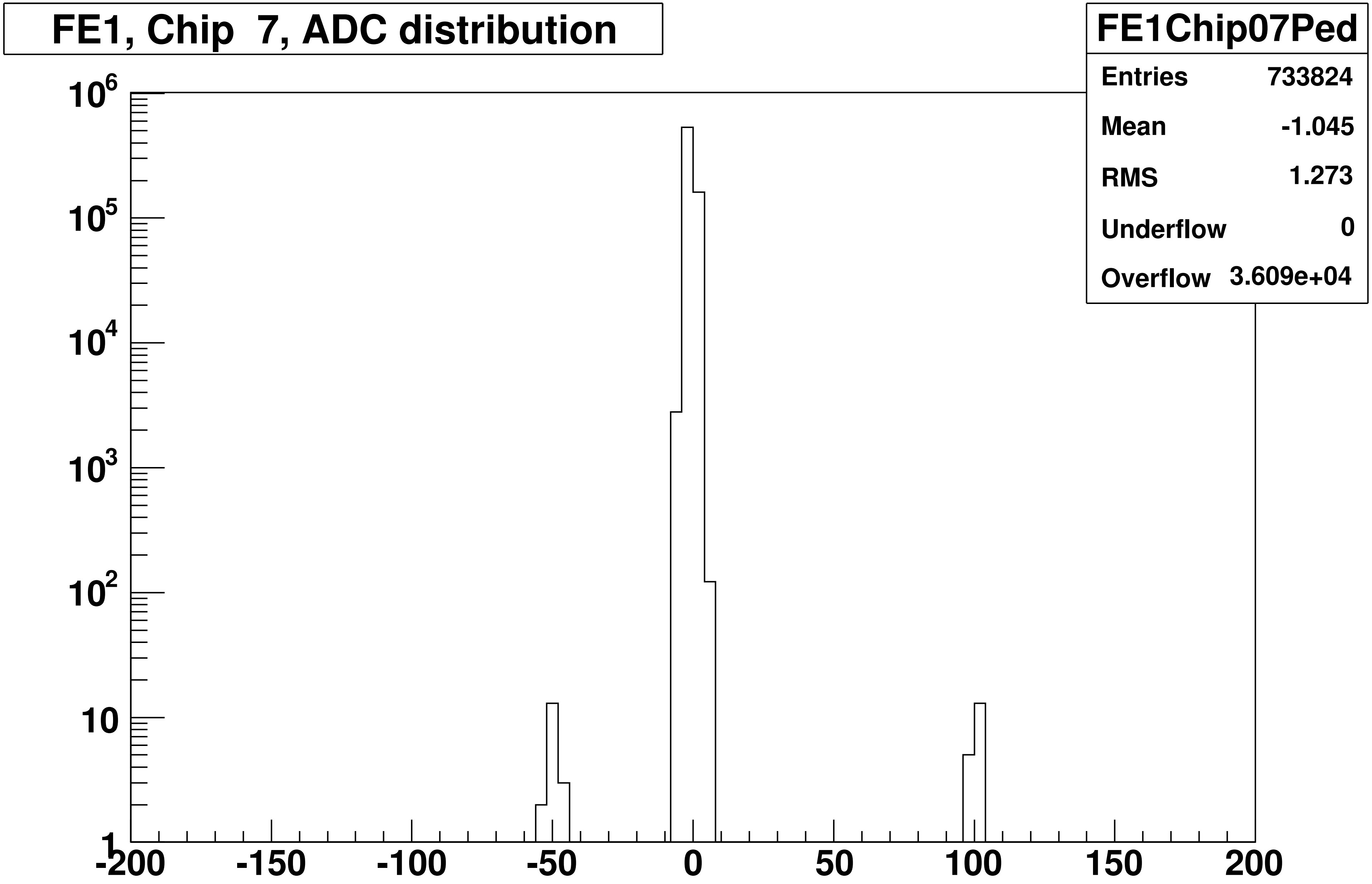
25000


FE1, Chip 7, ADC distribution
FE1Chip07Ped
Entries 733824
Mean -1.045
RMS 1.273
Underflow 0
Overflow 3.609e+04
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10^5
10^4
10^3
10^2
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1
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-100
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0
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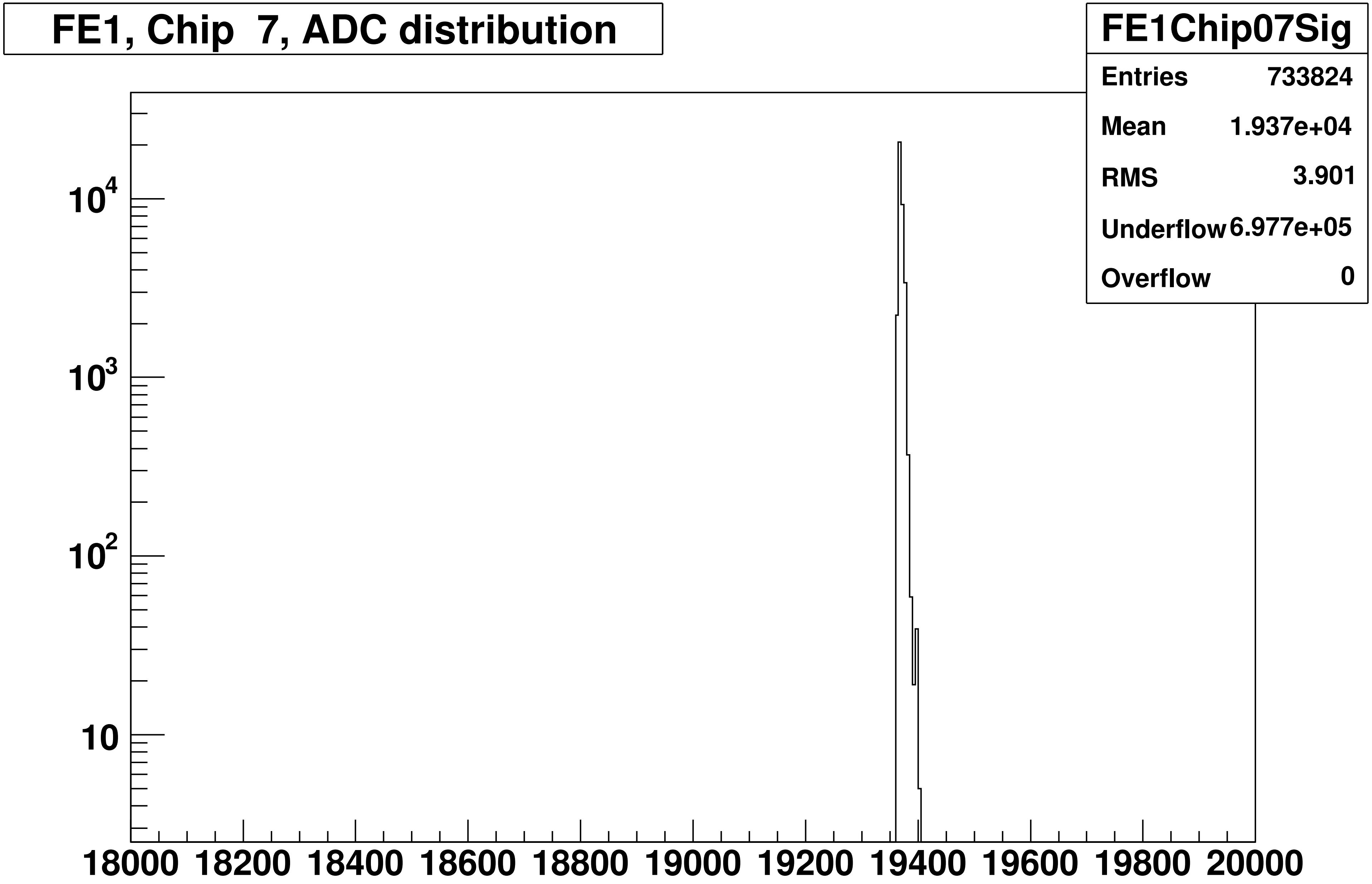
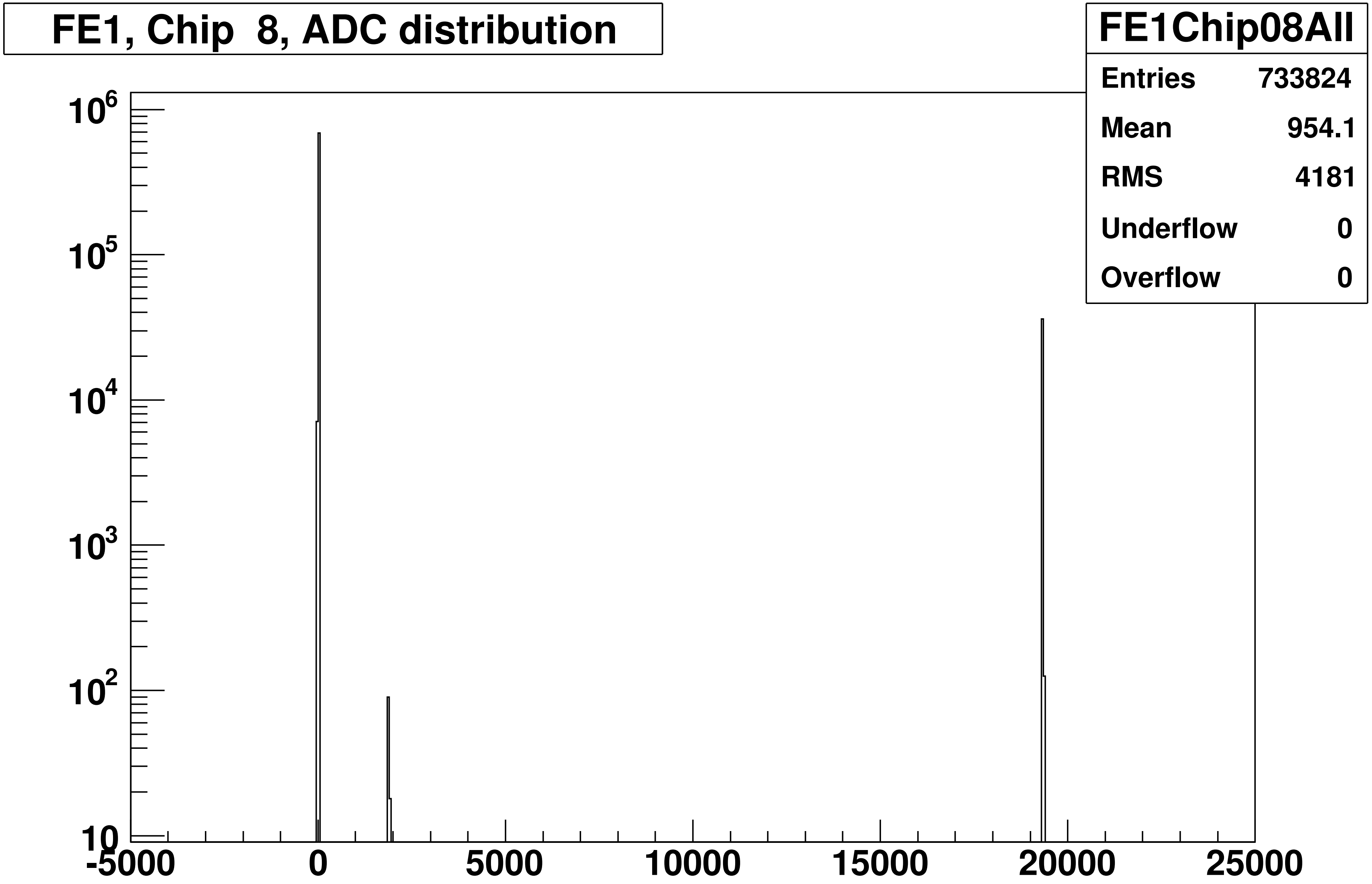
100
150
200



FE1, Chip 7, ADC distribution
FE1Chip07Sig
Entries 733824
Mean 1.937e+04
RMS 3.901
Underflow 6.977e+05
Overflow 0
10^4
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE1, Chip 8, ADC distribution
FE1Chip08All
Entries 733824
Mean 954.1
RMS 4181
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
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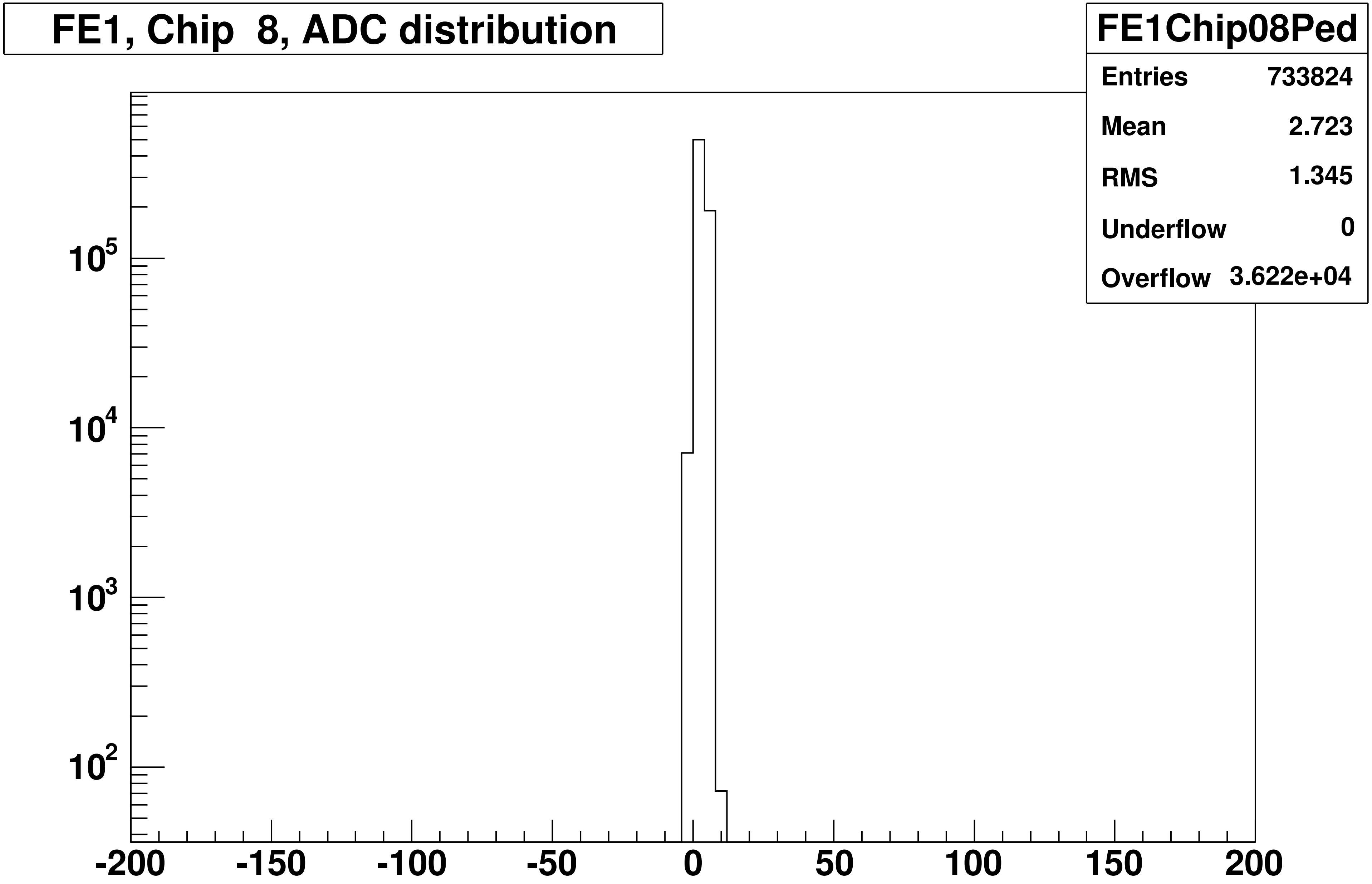
25000



FE1, Chip 8, ADC distribution
FE1Chip08Ped
Entries 733824
Mean 2.723
RMS 1.345
Underflow 0
Overflow 3.622e+04
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10^4
10^3
10^2
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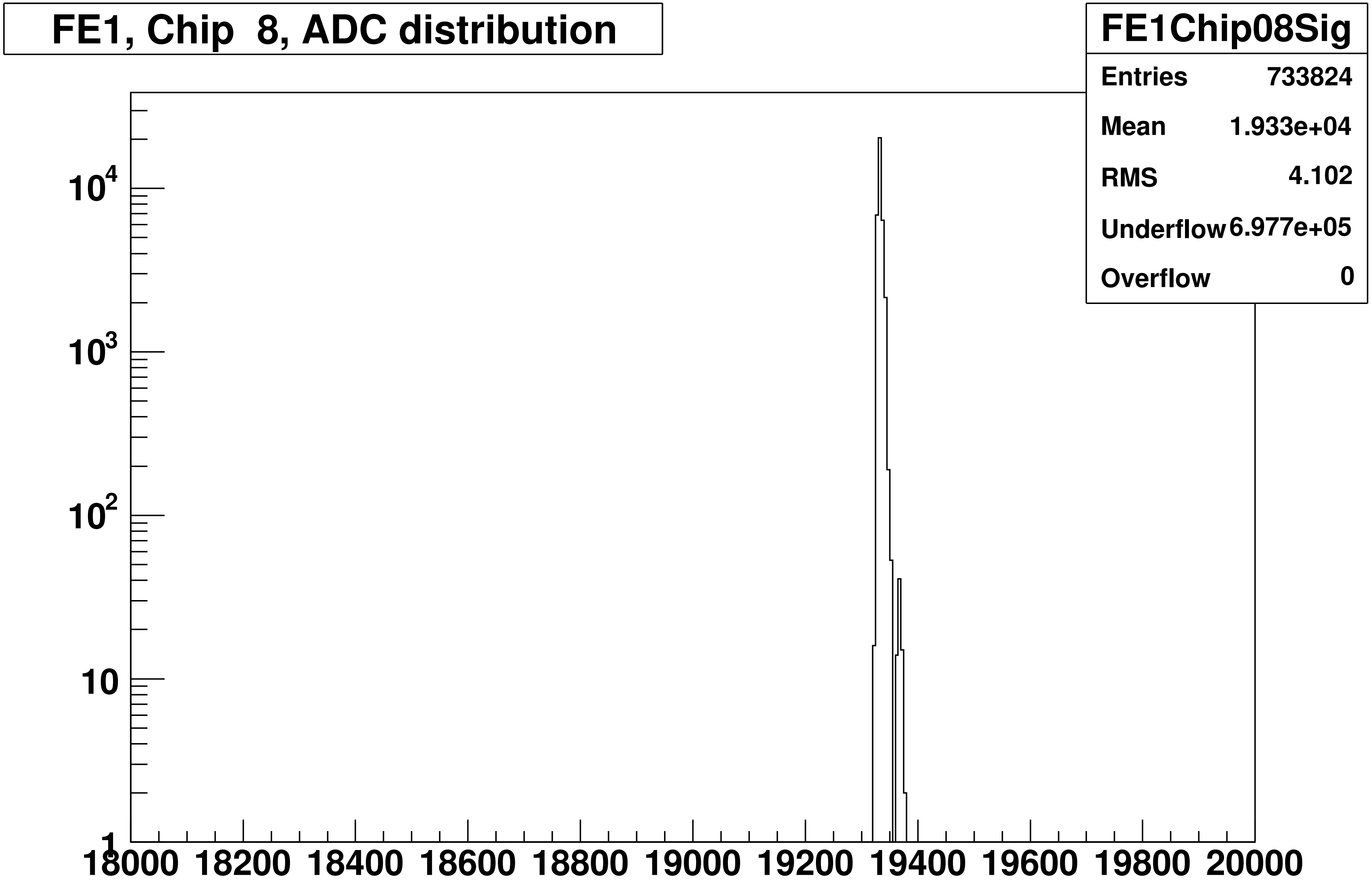
FE1, Chip 8, ADC distribution
FE1Chip08Sig
Entries 733824
Mean 1.933e+04
RMS 4.102
Underflow 6.977e+05
Overflow 0
10^4
10^3
10^2
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18400
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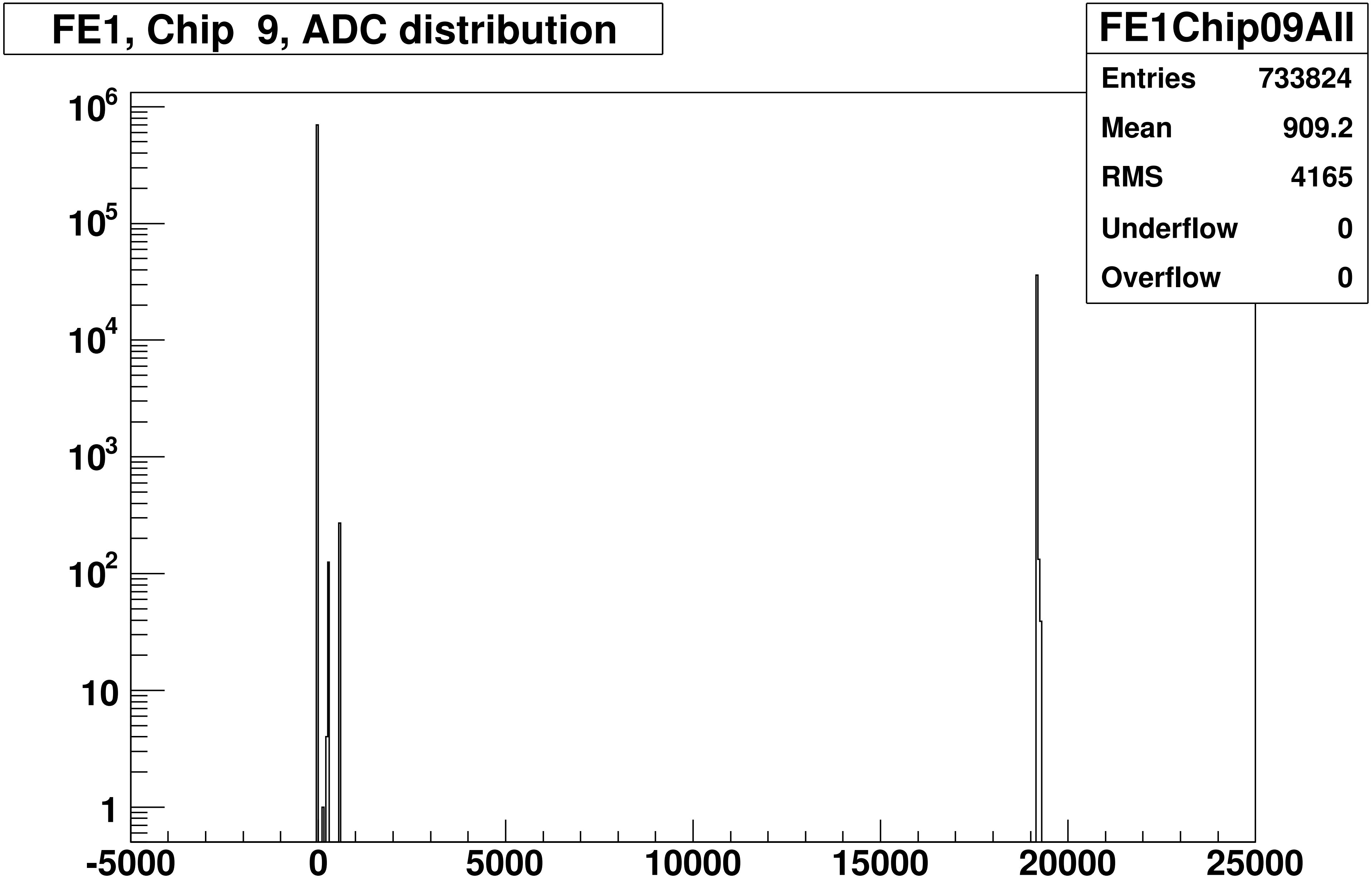
20000


FE1, Chip 9, ADC distribution
FE1Chip09All
Entries 733824
Mean 909.2
RMS 4165
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
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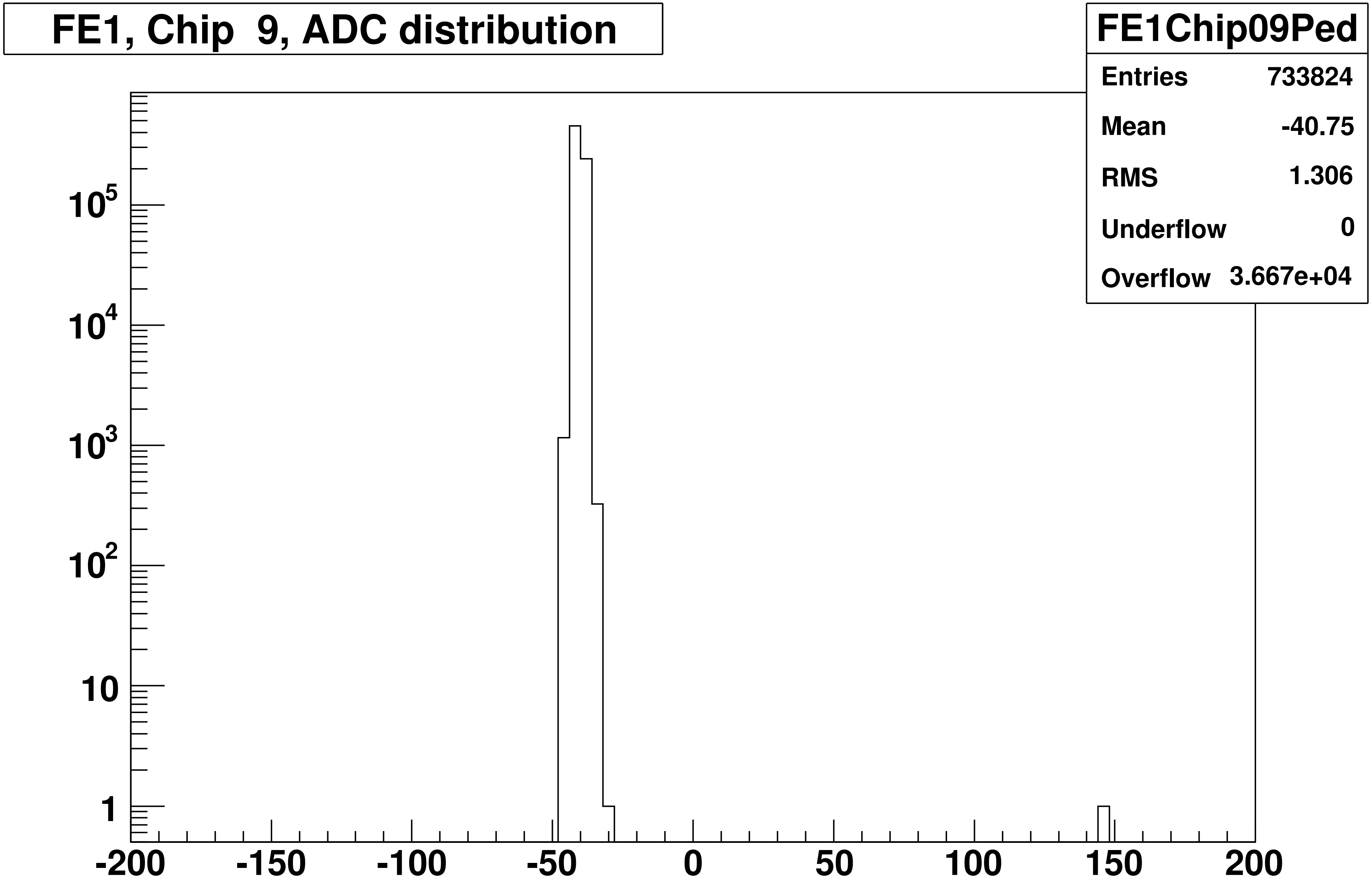
FE1, Chip 9, ADC distribution
FE1Chip09Ped
Entries 733824
Mean -40.75
RMS 1.306
Underflow 0
Overflow 3.667e+04
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10^3
10^2
10
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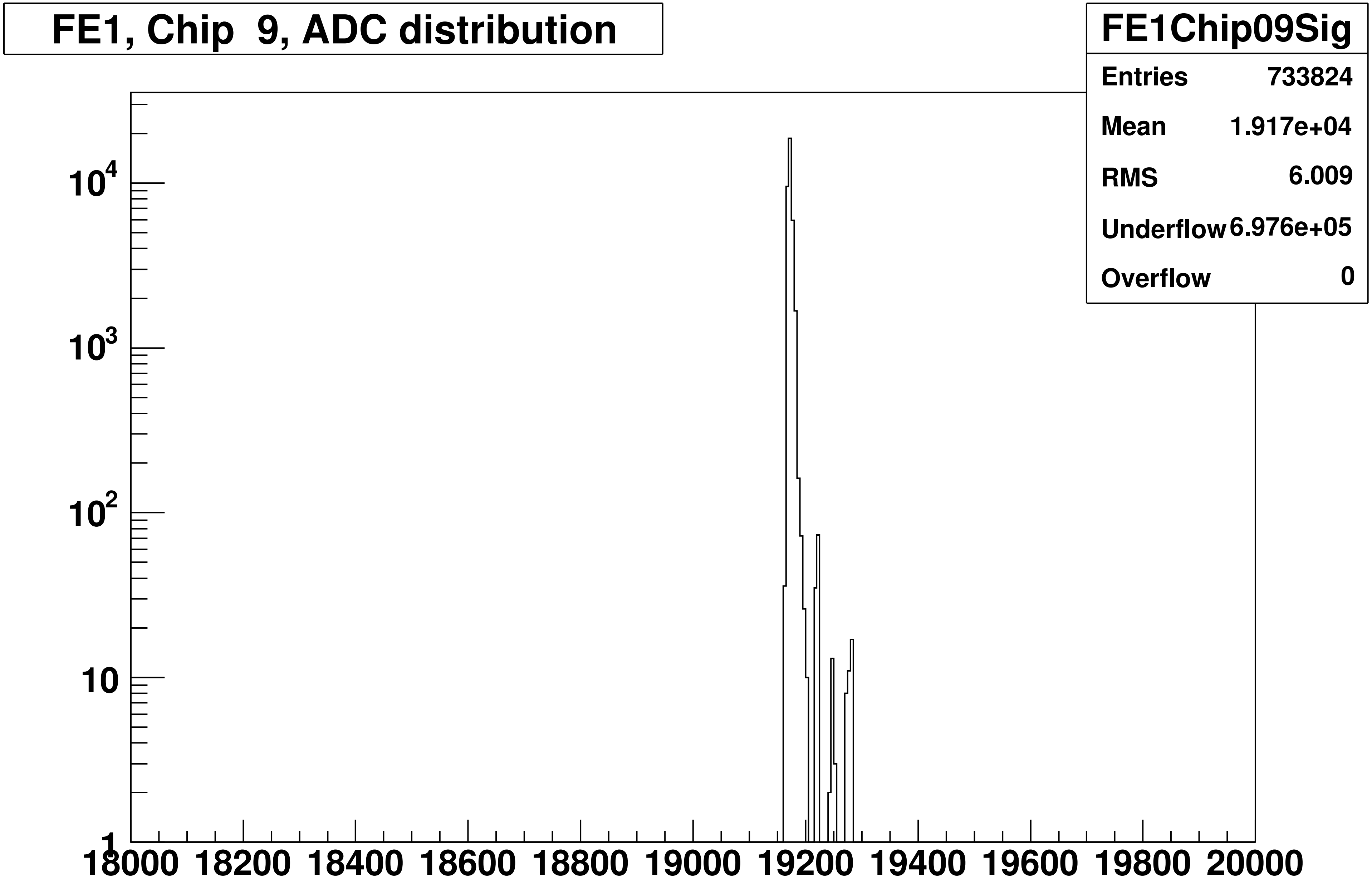

FE1, Chip 9, ADC distribution
FE1Chip09Sig
Entries 733824
Mean 1.917e+04
RMS 6.009
Underflow 6.976e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
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19000
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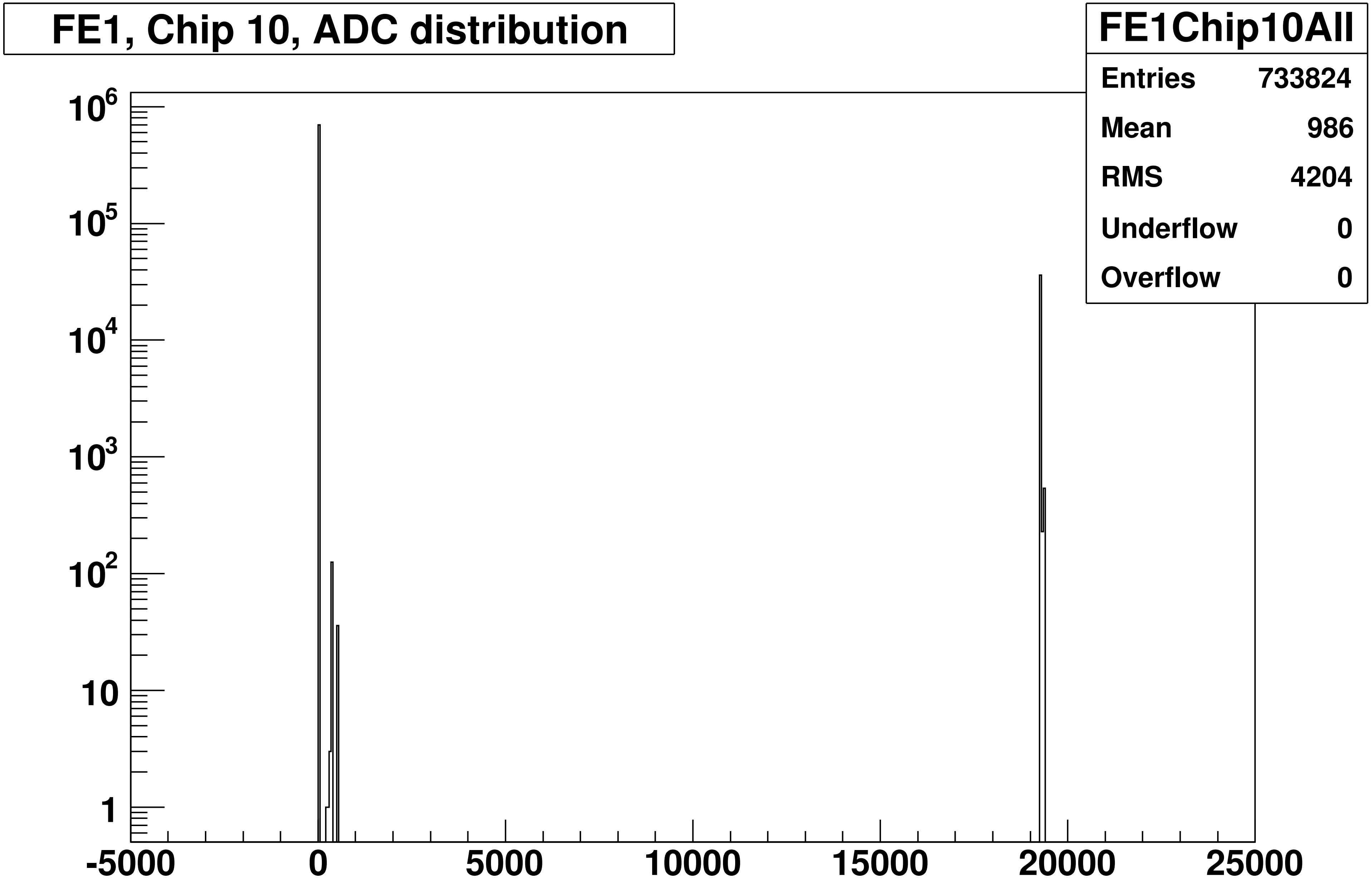
19600
19800
20000



FE1, Chip 10, ADC distribution
FE1Chip10All
Entries 733824
Mean 986
RMS 4204
Underflow 0
Overflow 0
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10^4
10^3
10^2
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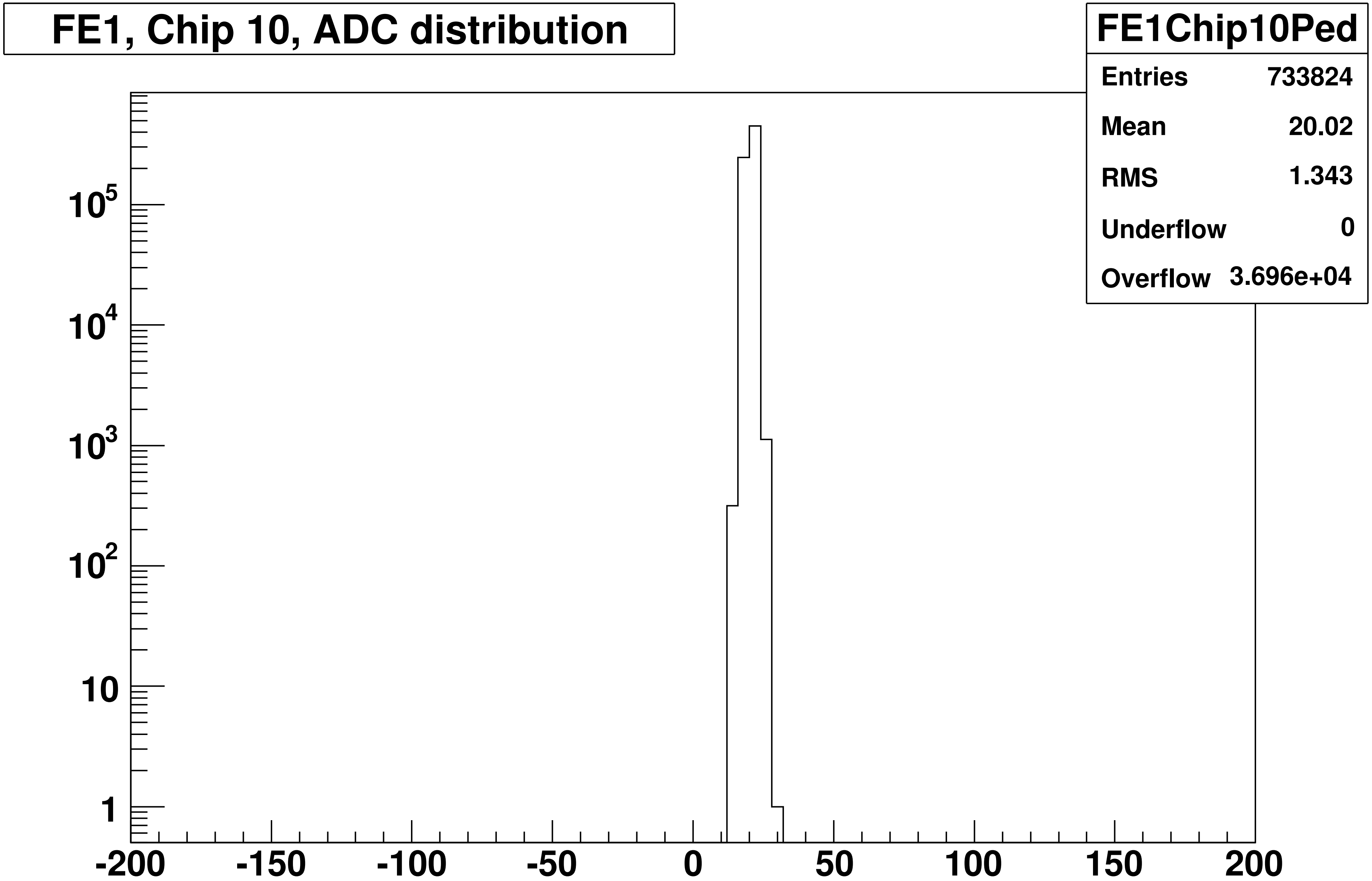
FE1, Chip 10, ADC distribution
FE1Chip10Ped
Entries 733824
Mean 20.02
RMS 1.343
Underflow 0
Overflow 3.696e+04
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10^3
10^2
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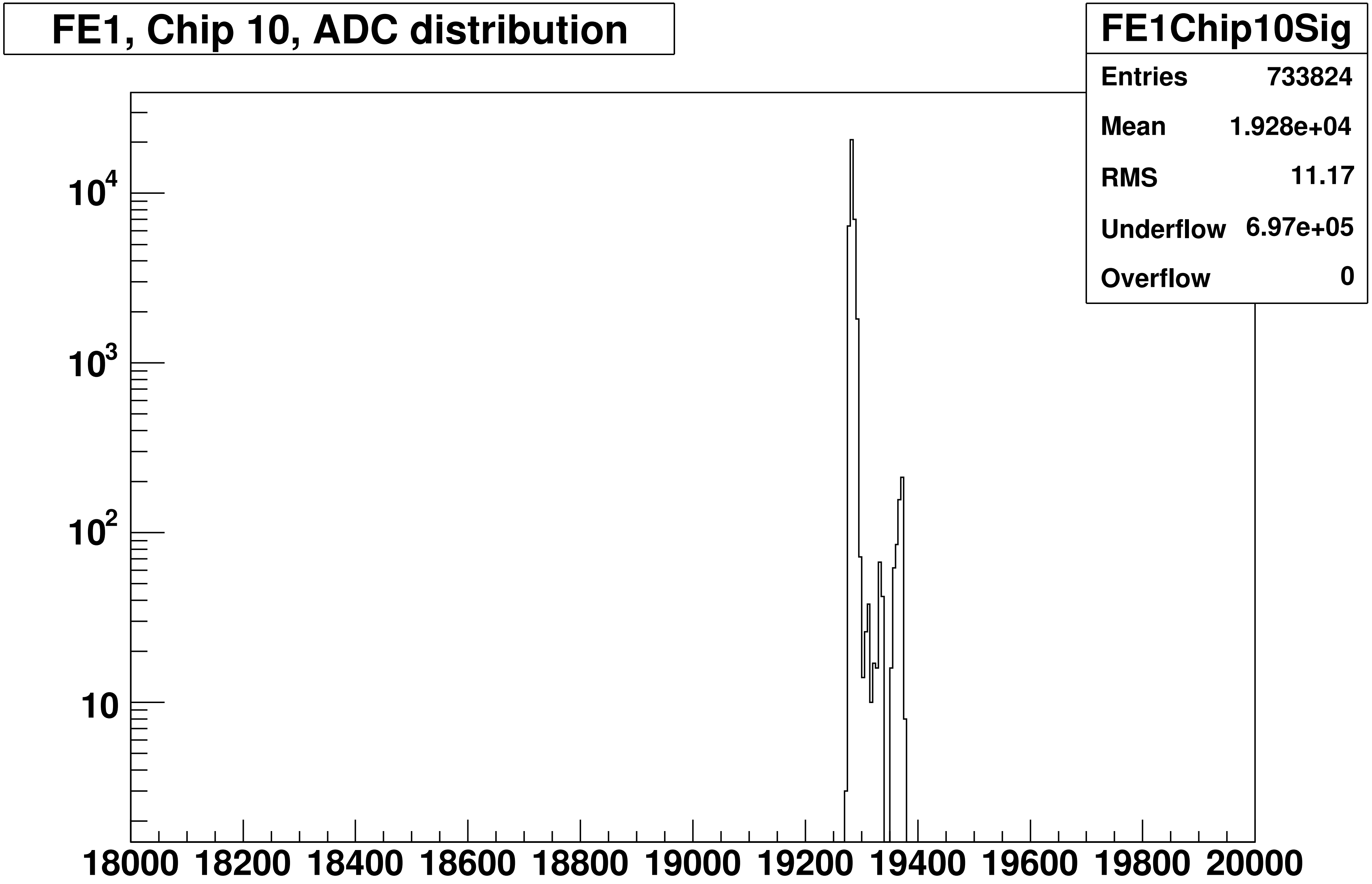
150
200



FE1, Chip 10, ADC distribution
FE1Chip10Sig
Entries 733824
Mean 1.928e+04
RMS 11.17
Underflow 6.97e+05
Overflow 0
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10^3
10^2
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18000
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18400
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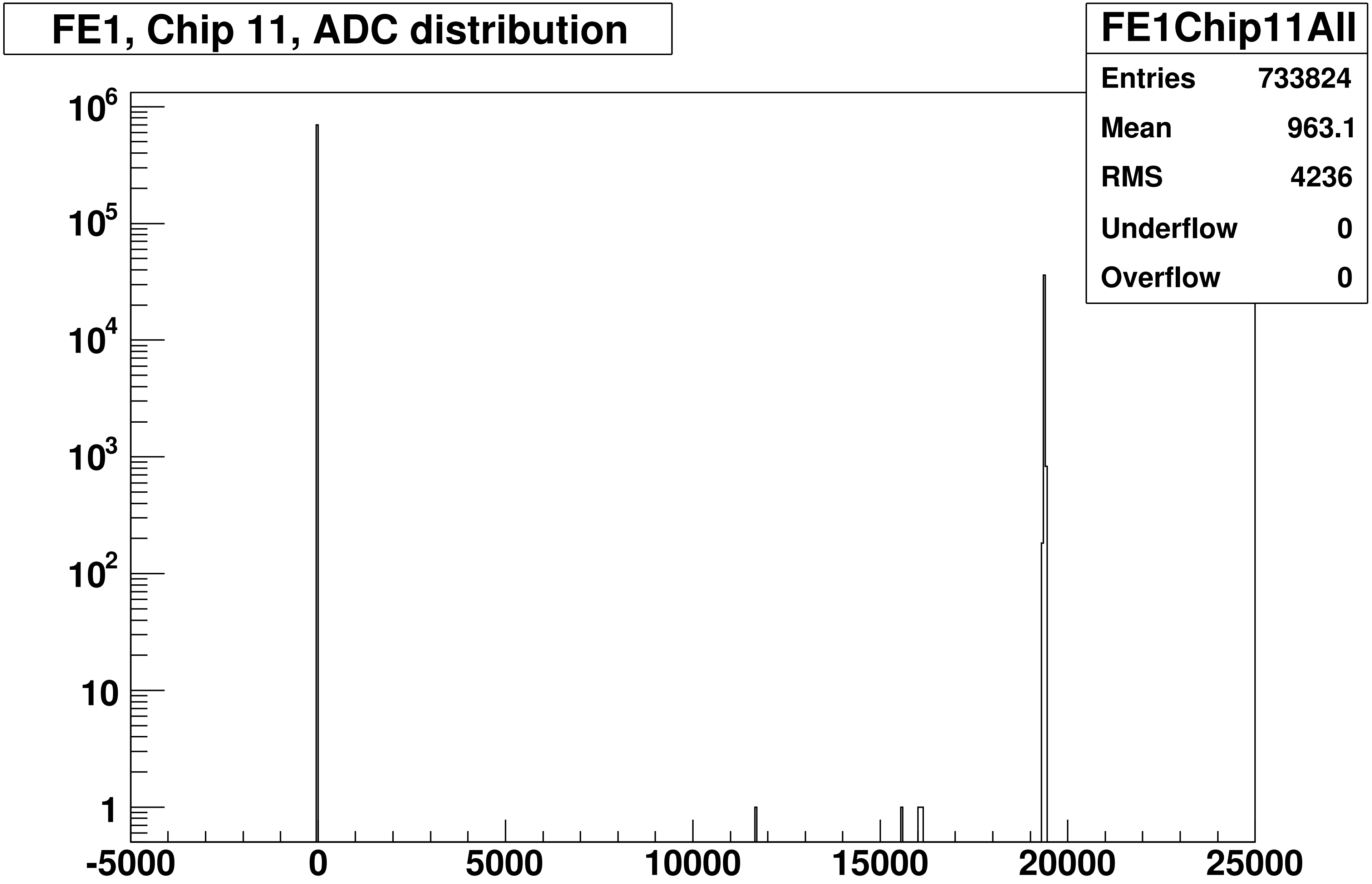
FE1, Chip 11, ADC distribution
FE1Chip11All
Entries 733824
Mean 963.1
RMS 4236
Underflow 0
Overflow 0
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10^4
10^3
10^2
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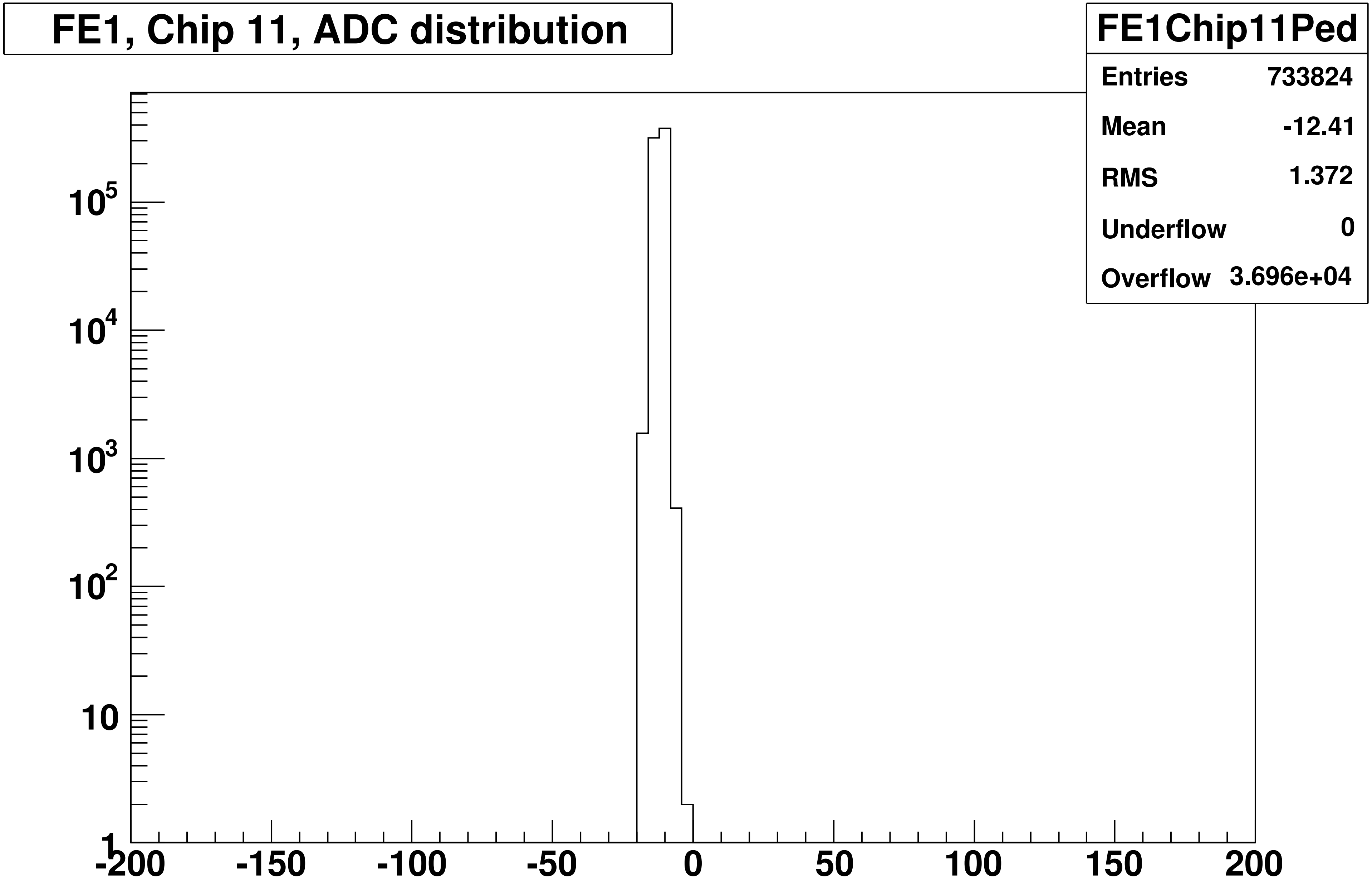
25000



FE1, Chip 11, ADC distribution
FE1Chip11Ped
Entries 733824
Mean -12.41
RMS 1.372
Underflow 0
Overflow 3.696e+04
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10^3
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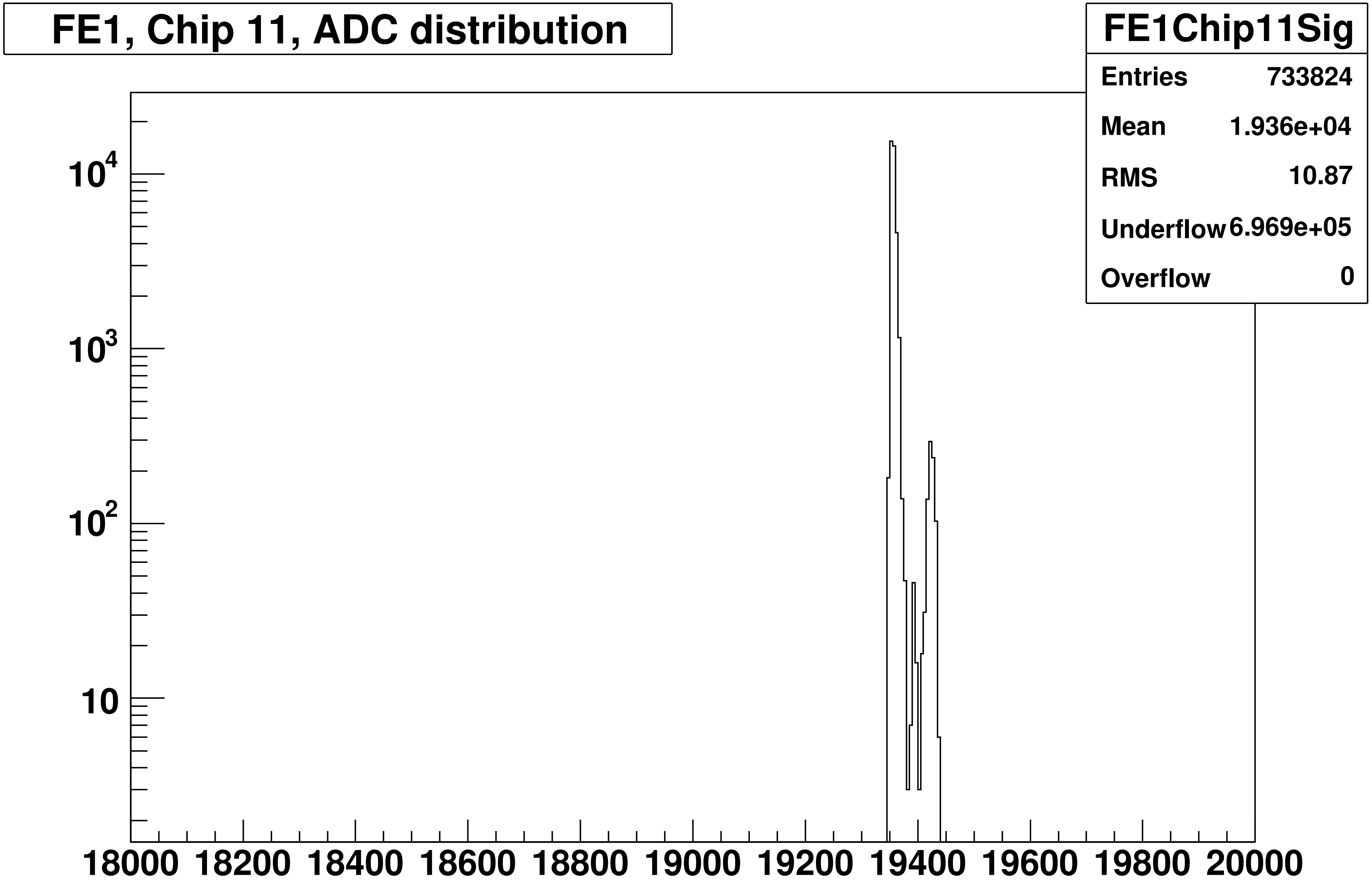
150
200


FE1, Chip 11, ADC distribution
FE1Chip11Sig
Entries 733824
Mean 1.936e+04
RMS 10.87
Underflow 6.969e+05
Overflow 0
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10^3
10^2
10
18000
18200
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18600
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19000
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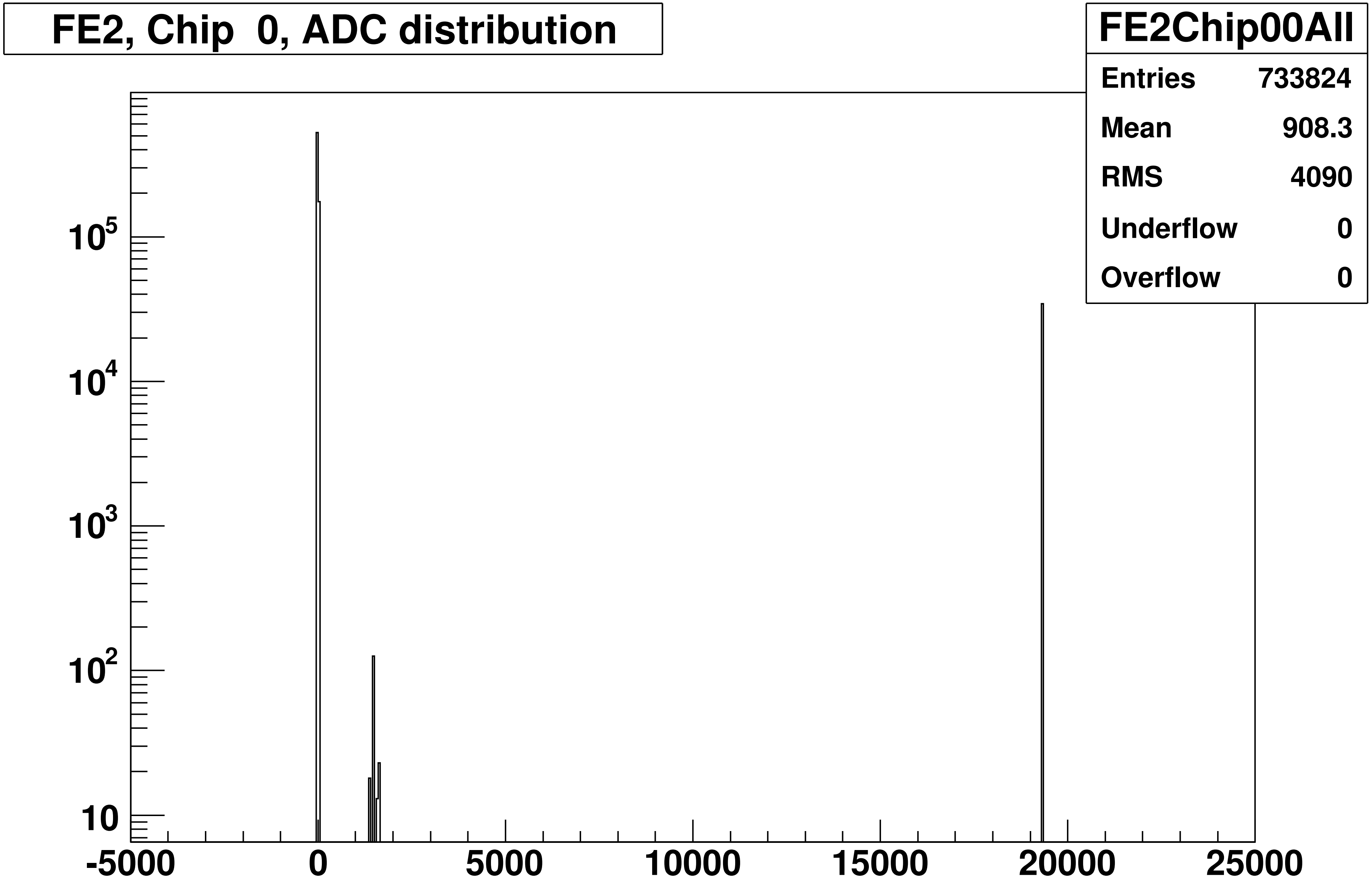
20000



FE2, Chip 0, ADC distribution
FE2Chip00All
Entries 733824
Mean 908.3
RMS 4090
Underflow 0
Overflow 0
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10^2
10^3
10^4
10^5
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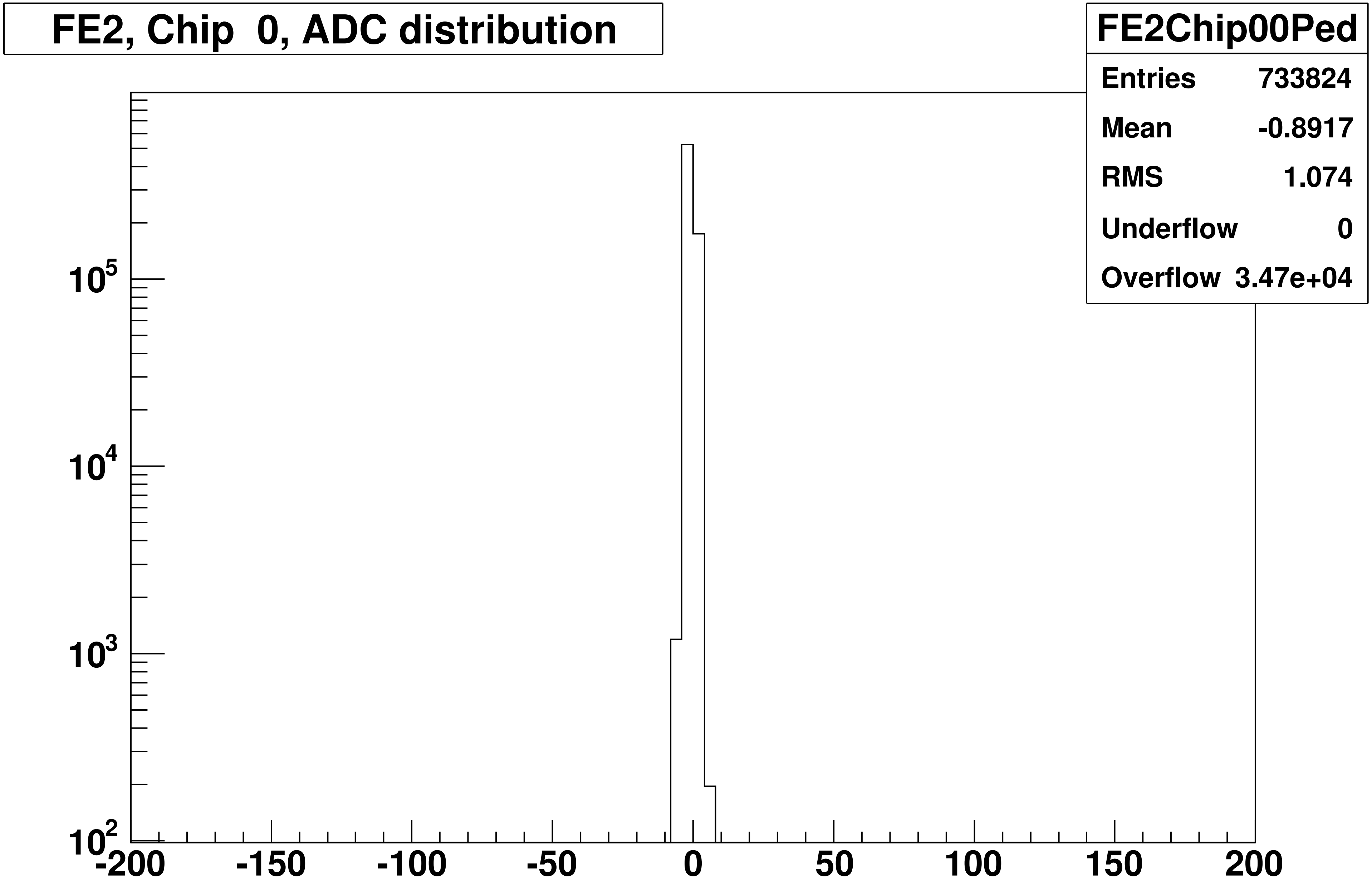
0
5000
10000
15000
20000
25000


FE2, Chip 0, ADC distribution
FE2Chip00Ped
Entries 733824
Mean -0.8917
RMS 1.074
Underflow 0
Overflow 3.47e+04
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10^4
10^3
10^2
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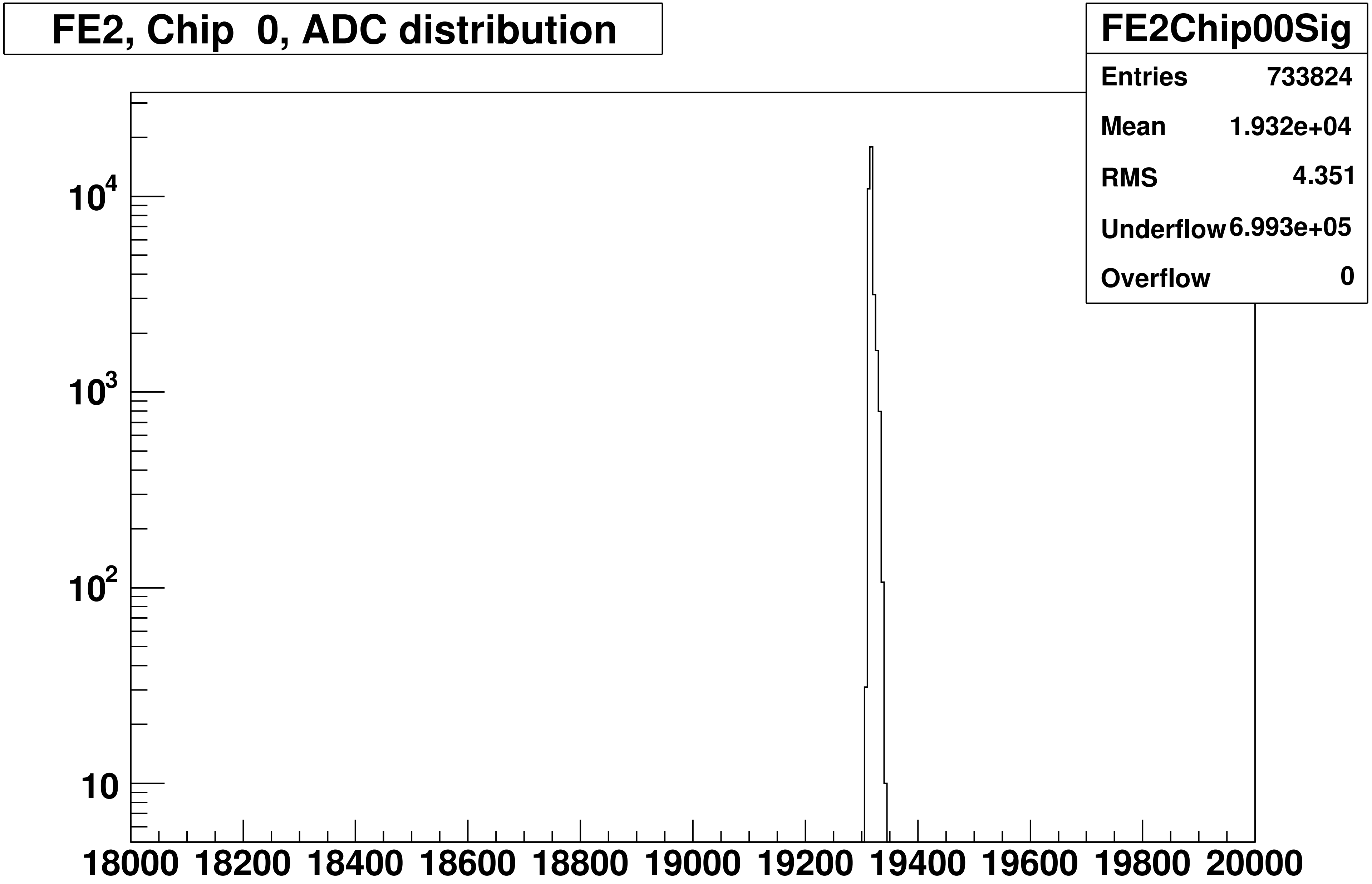
150
200


FE2, Chip 0, ADC distribution
FE2Chip00Sig
Entries 733824
Mean 1.932e+04
RMS 4.351
Underflow 6.993e+05
Overflow 0
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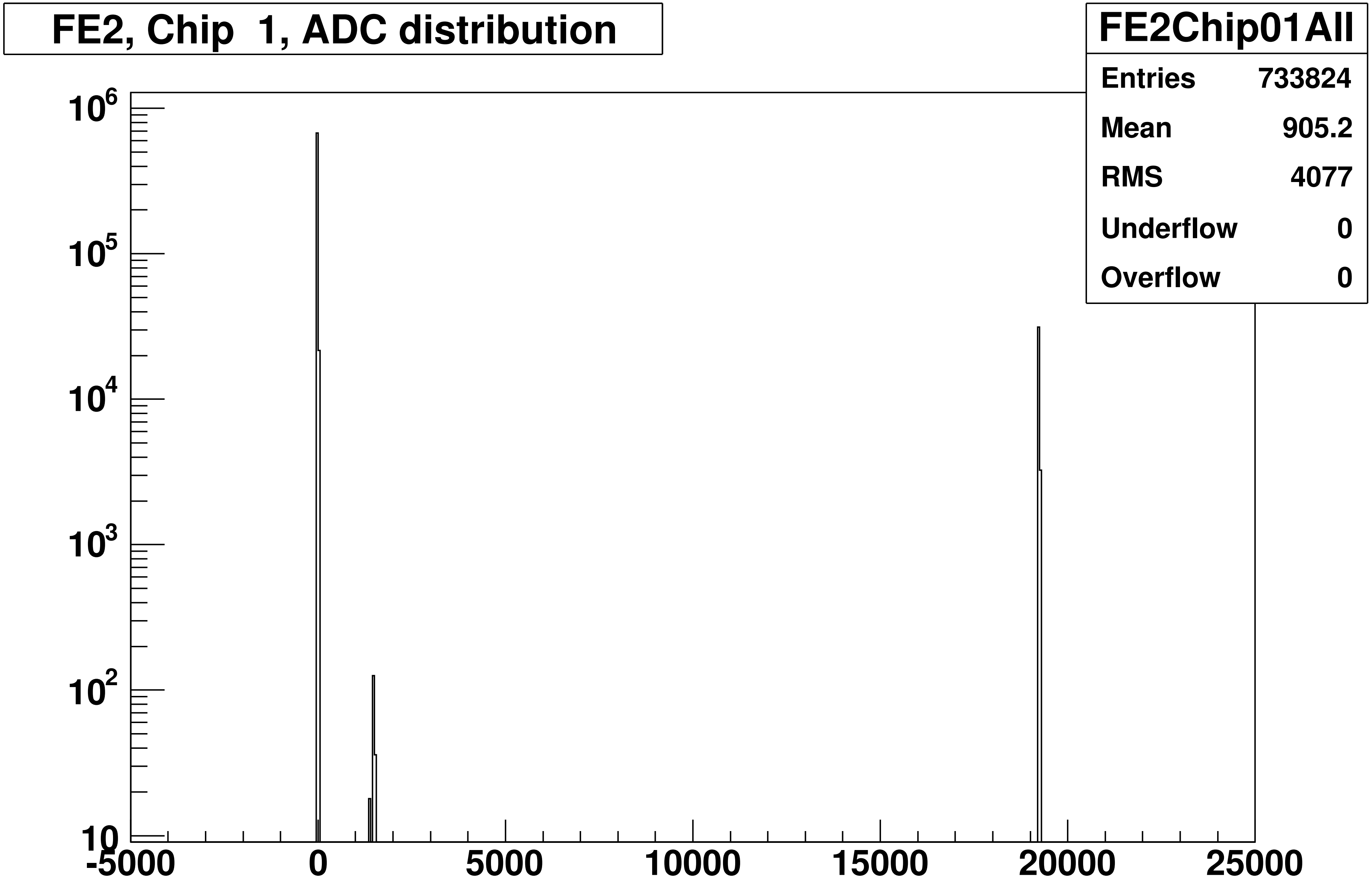
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE2, Chip 1, ADC distribution
FE2Chip01All
Entries 733824
Mean 905.2
RMS 4077
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
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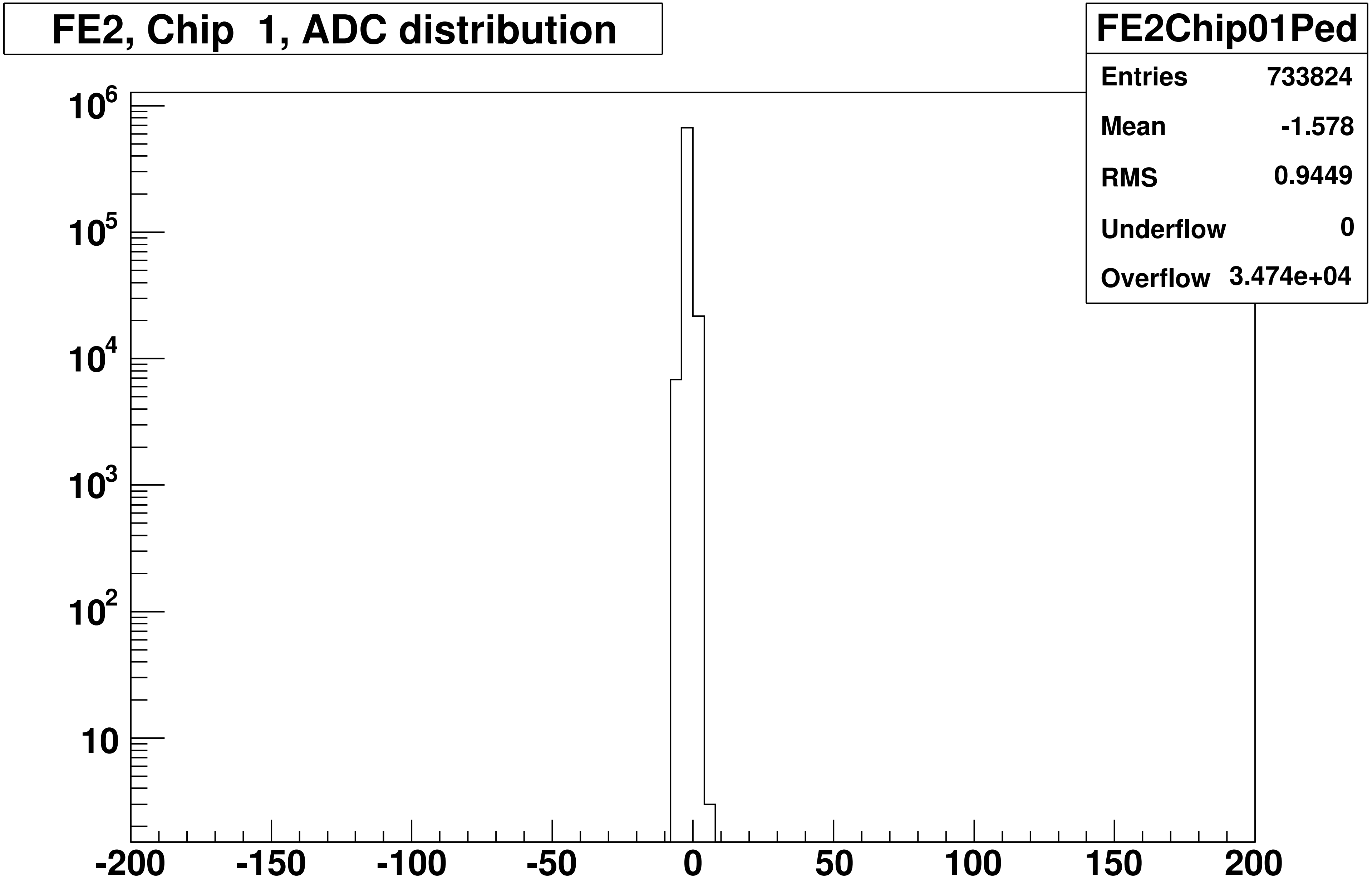
25000



FE2, Chip 1, ADC distribution
FE2Chip01Ped
Entries 733824
Mean -1.578
RMS 0.9449
Underflow 0
Overflow 3.474e+04
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10^4
10^3
10^2
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50
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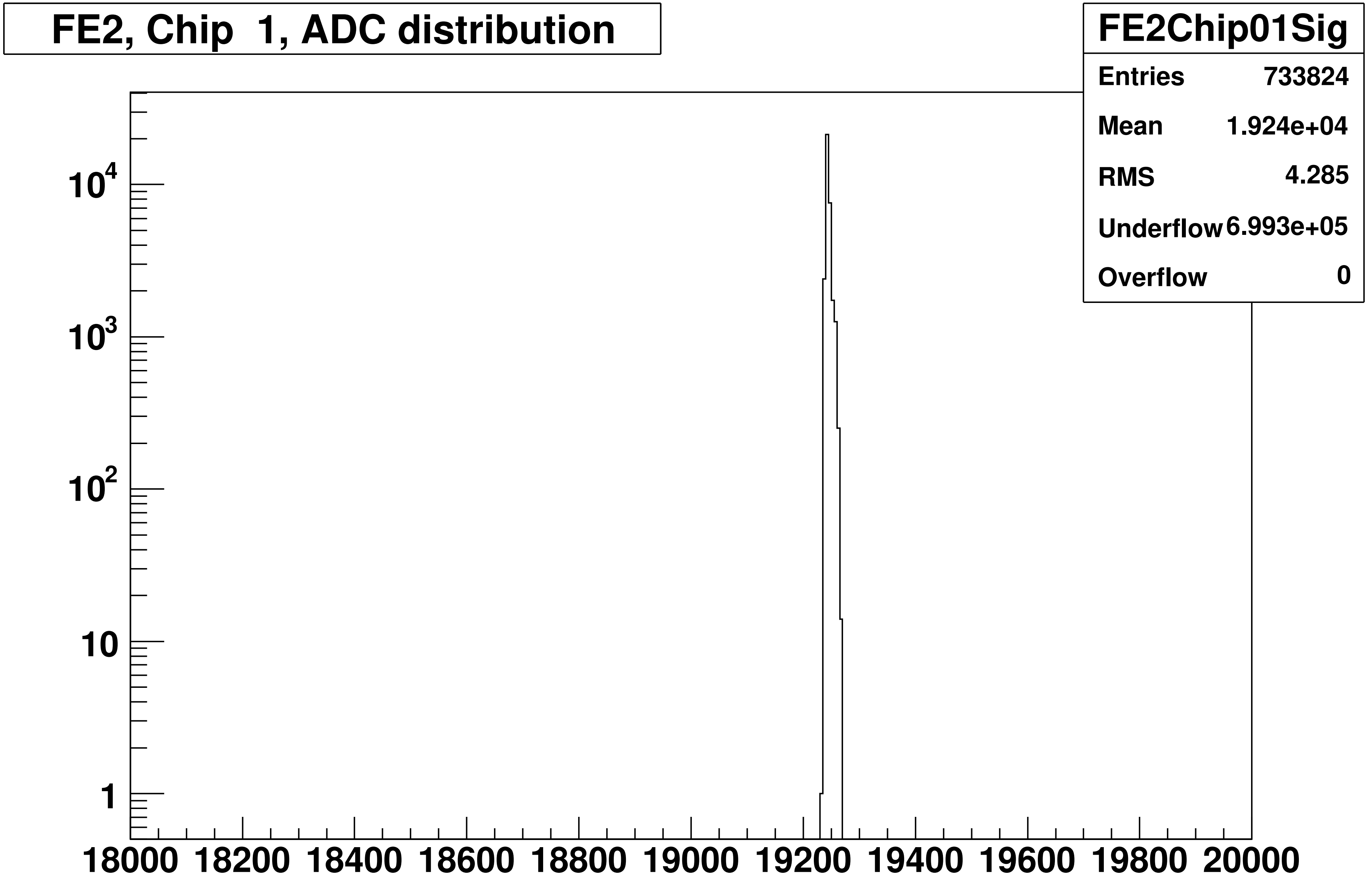
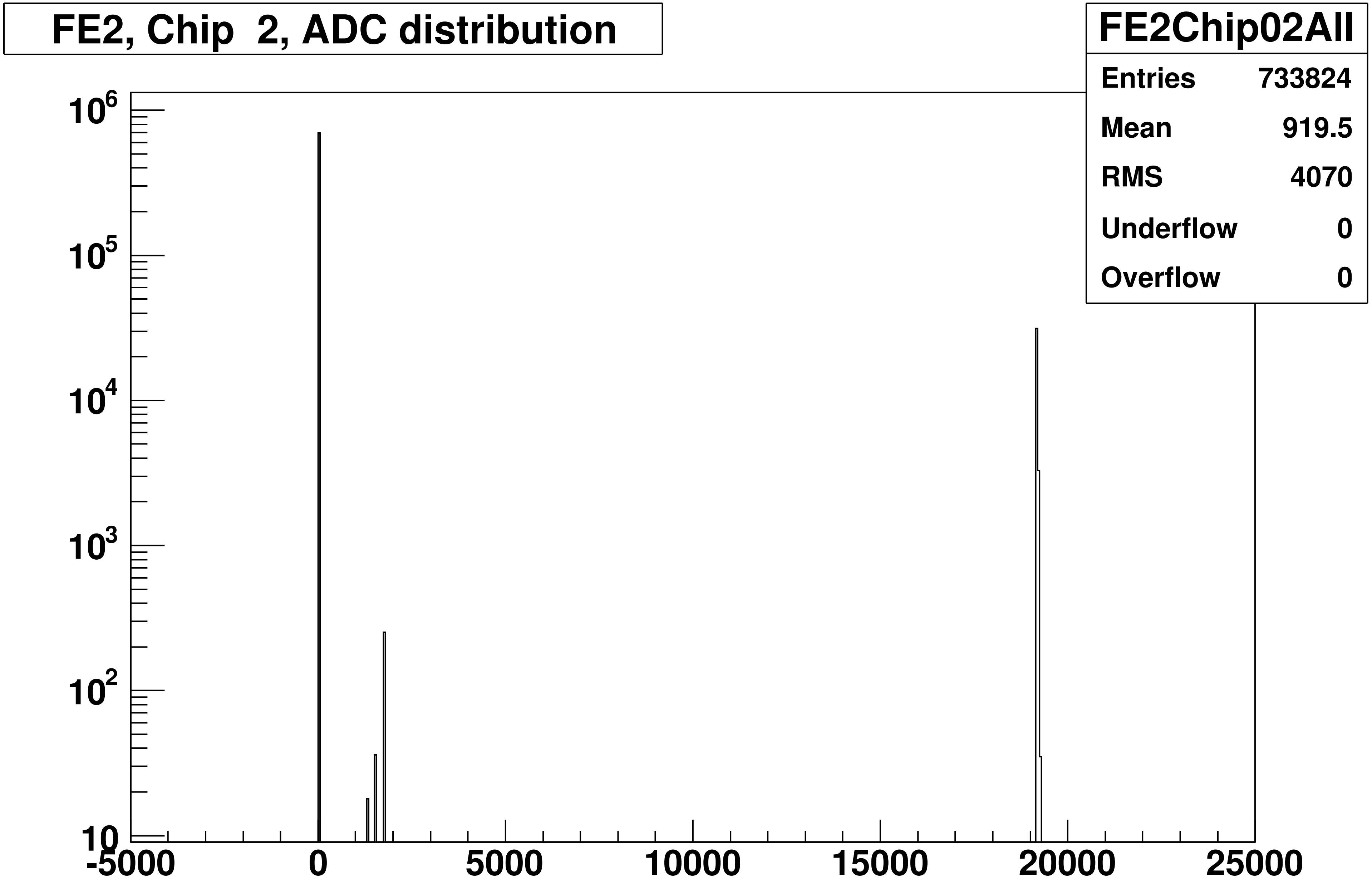
150
200


FE2, Chip 1, ADC distribution
FE2Chip01Sig
Entries 733824
Mean 1.924e+04
RMS 4.285
Underflow 6.993e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE2, Chip 2, ADC distribution
FE2Chip02All
Entries 733824
Mean 919.5
RMS 4070
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
-5000
0
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10000
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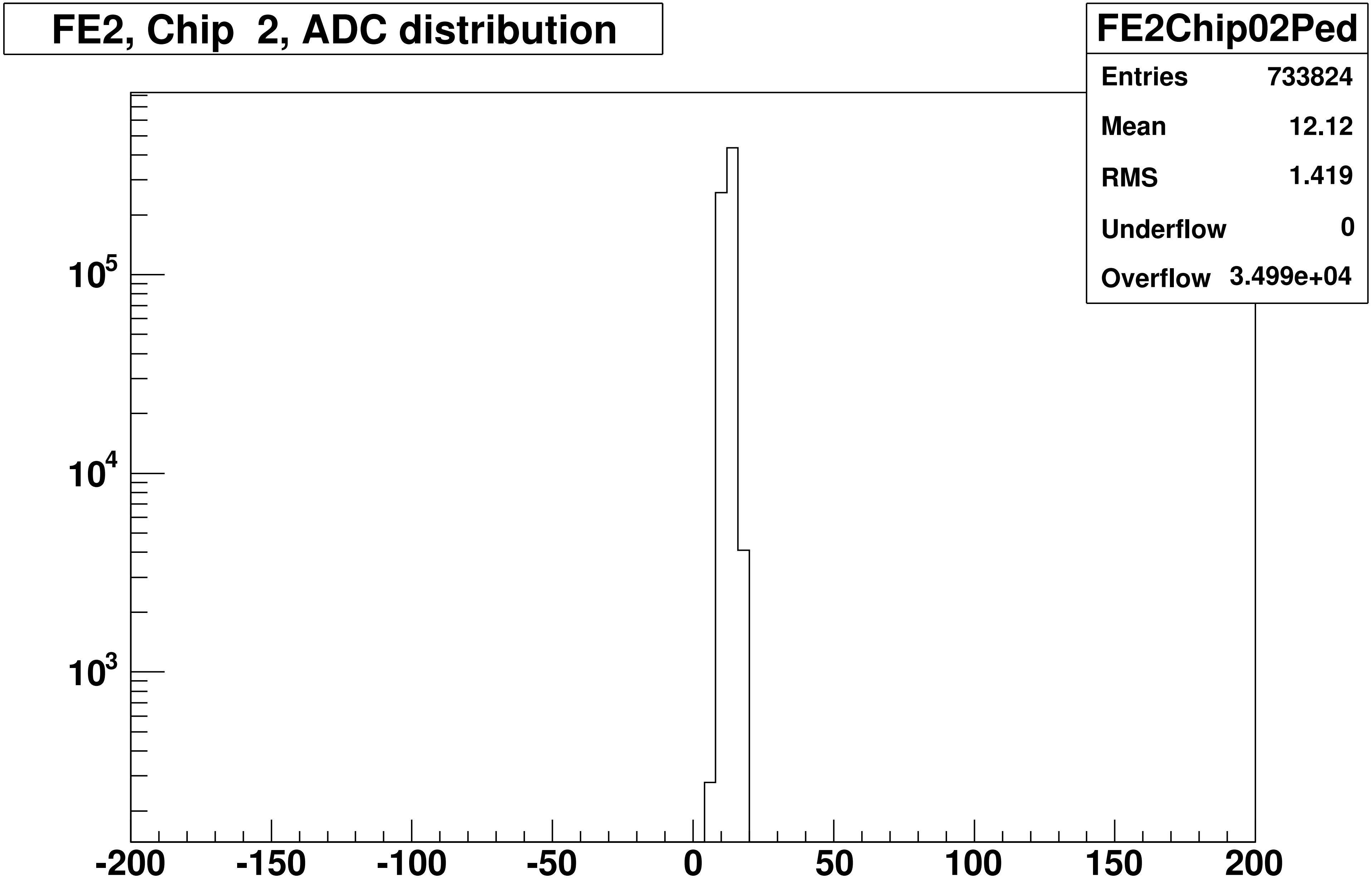
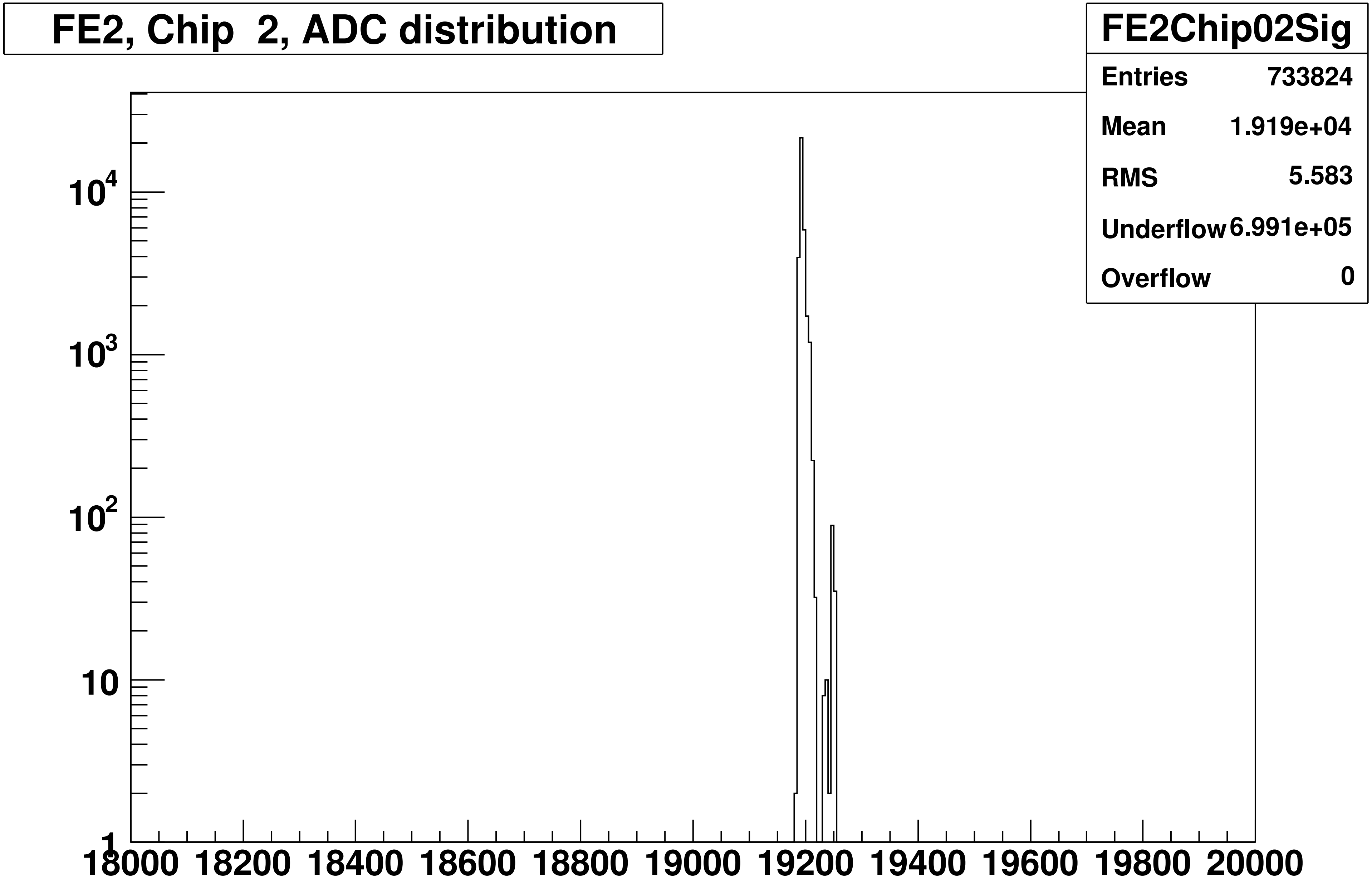
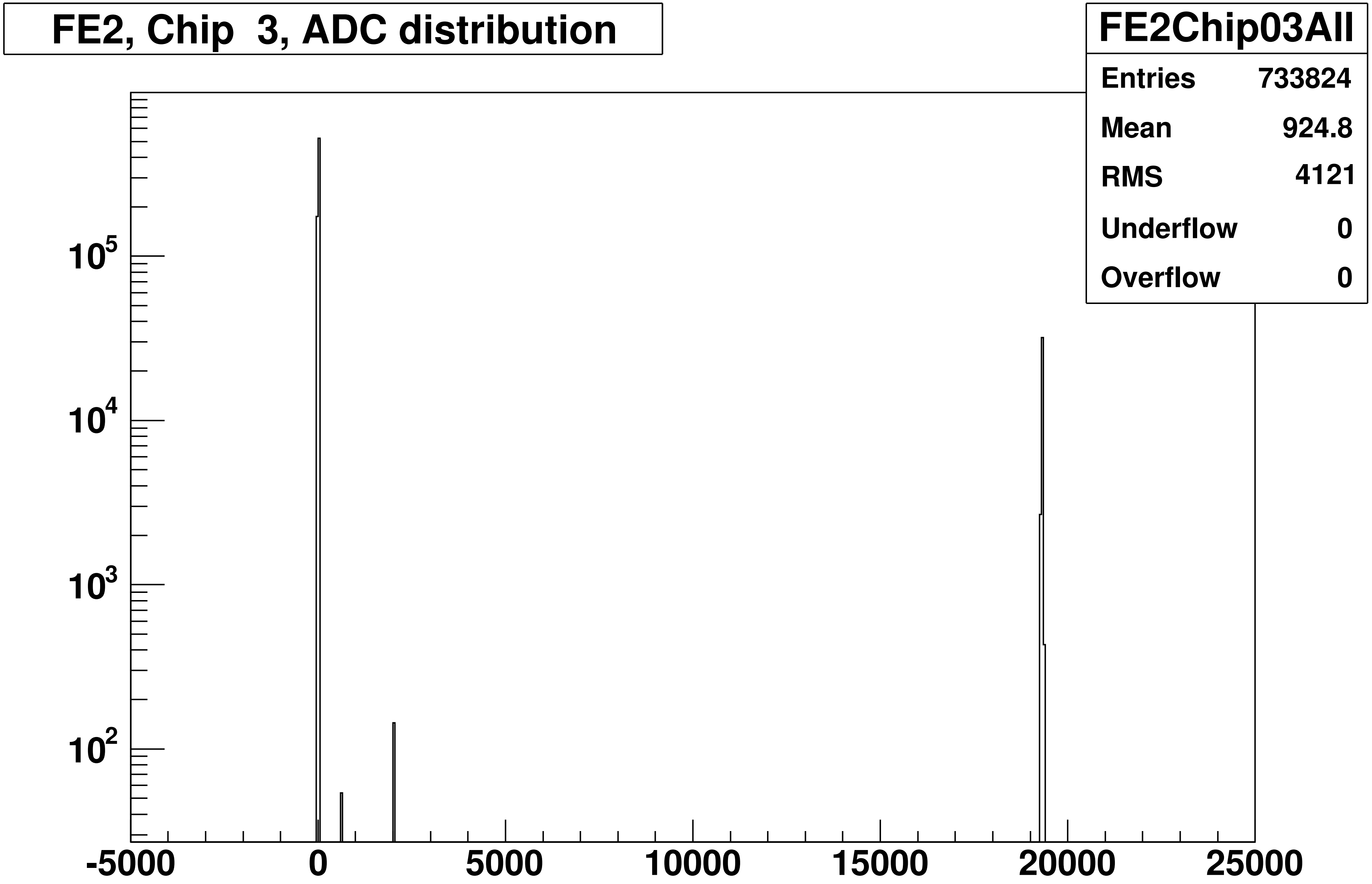
20000
25000


FE2, Chip 2, ADC distribution
FE2Chip02Ped
Entries 733824
Mean 12.12
RMS 1.419
Underflow 0
Overflow 3.499e+04
10^5
10^4
10^3
-200
-150
-100
-50
0
50
100
150
200


FE2, Chip 2, ADC distribution
FE2Chip02Sig
Entries 733824
Mean 1.919e+04
RMS 5.583
Underflow 6.991e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000



FE2, Chip 3, ADC distribution
FE2Chip03All
Entries 733824
Mean 924.8
RMS 4121
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
-5000
0
5000
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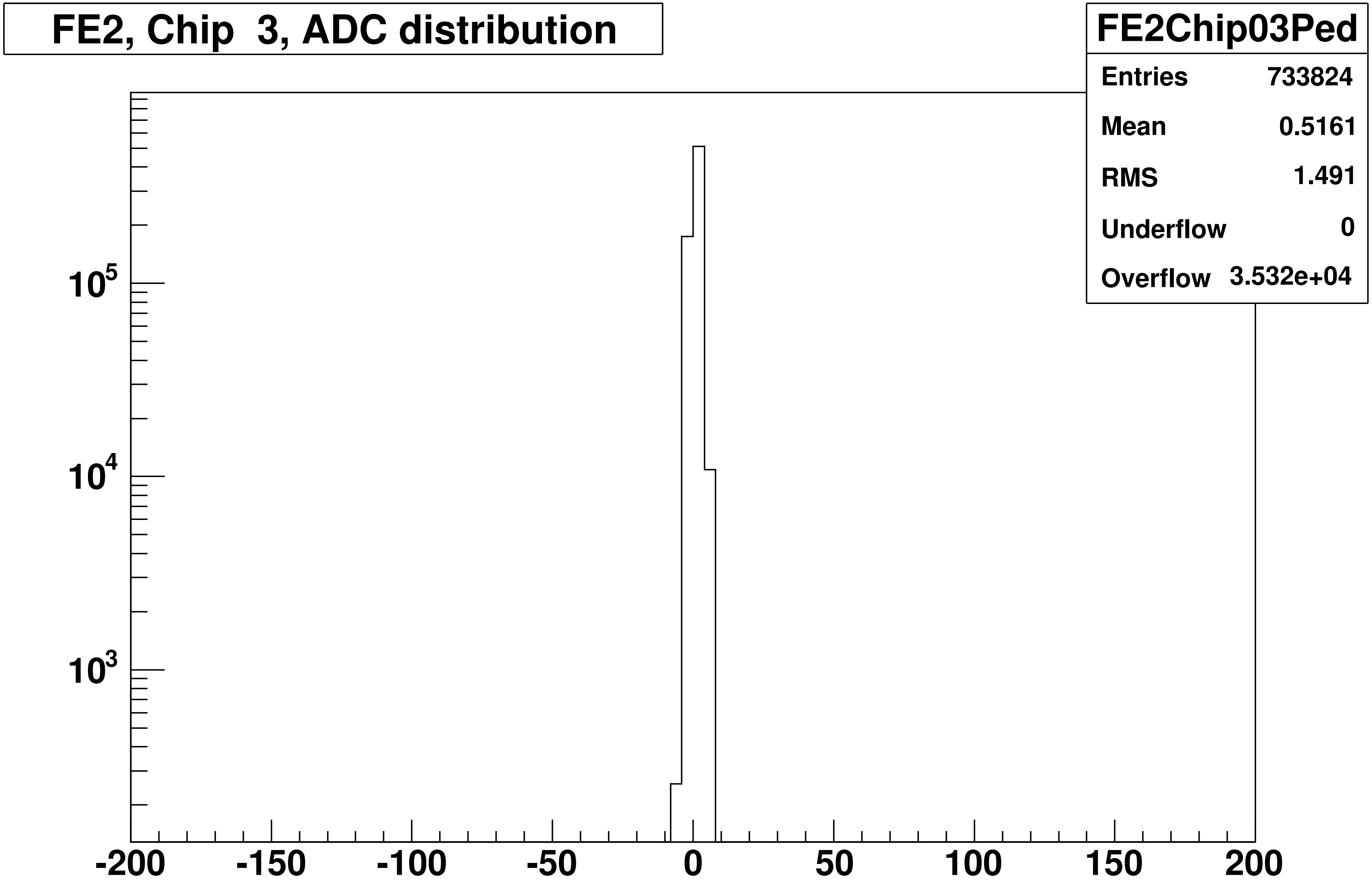

FE2, Chip 3, ADC distribution
FE2Chip03Ped
Entries 733824
Mean 0.5161
RMS 1.491
Underflow 0
Overflow 3.532e+04
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10^4
10^3
-200
-150
-100
-50
0
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100
150
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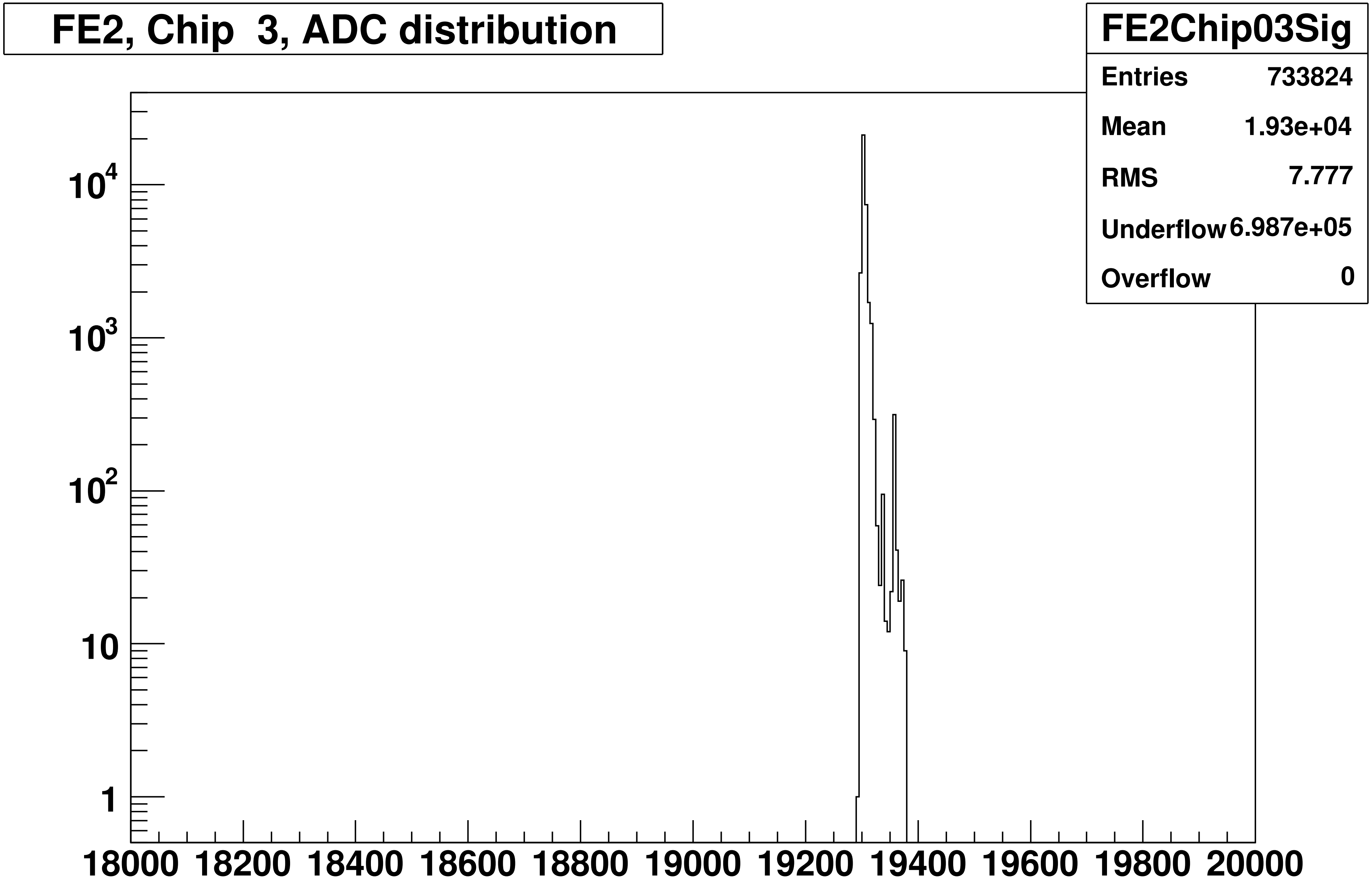
FE2, Chip 3, ADC distribution
FE2Chip03Sig
Entries 733824
Mean 1.93e+04
RMS 7.777
Underflow 6.987e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
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19800
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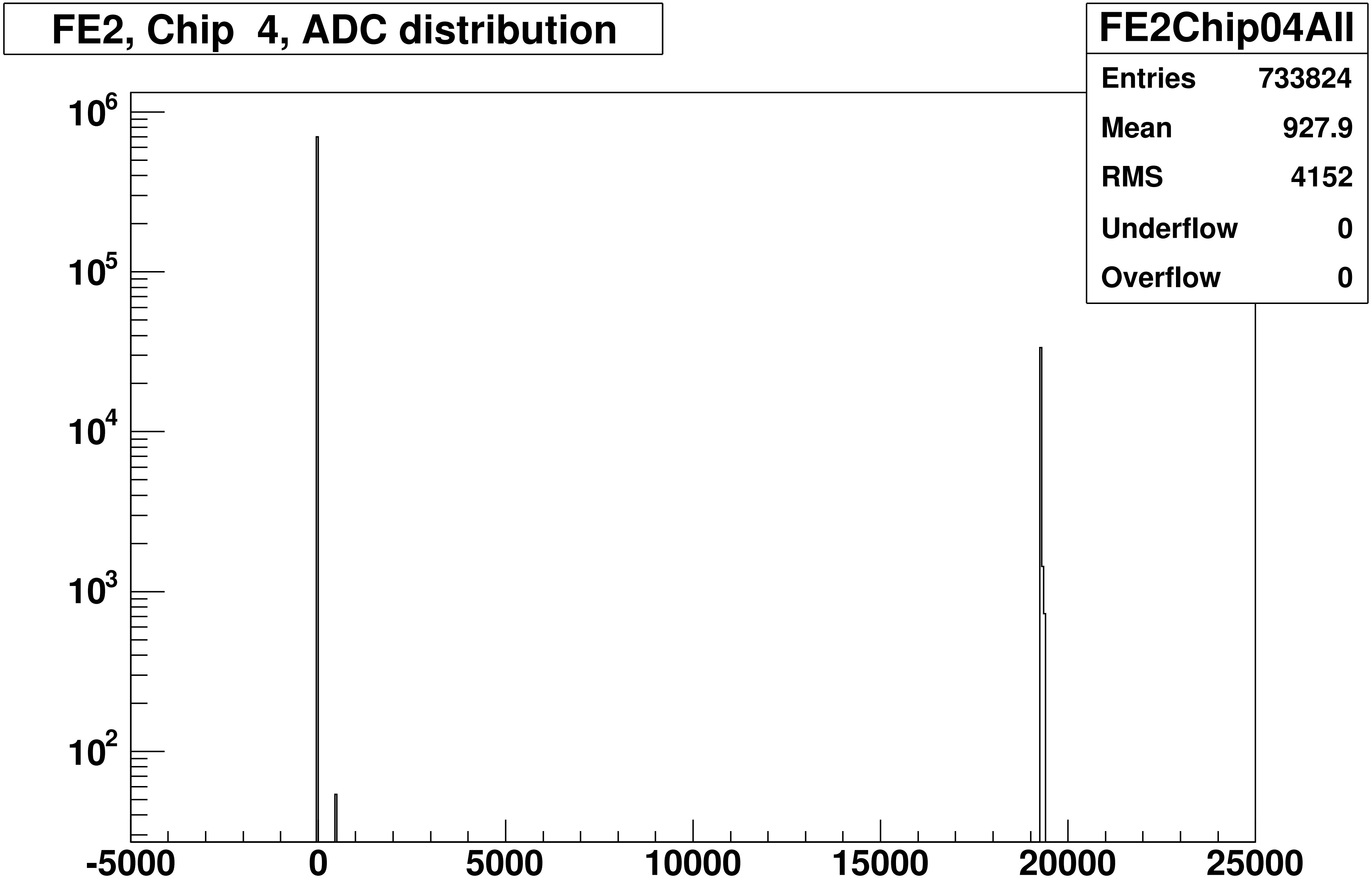
FE2, Chip 4, ADC distribution
FE2Chip04All
Entries 733824
Mean 927.9
RMS 4152
Underflow 0
Overflow 0
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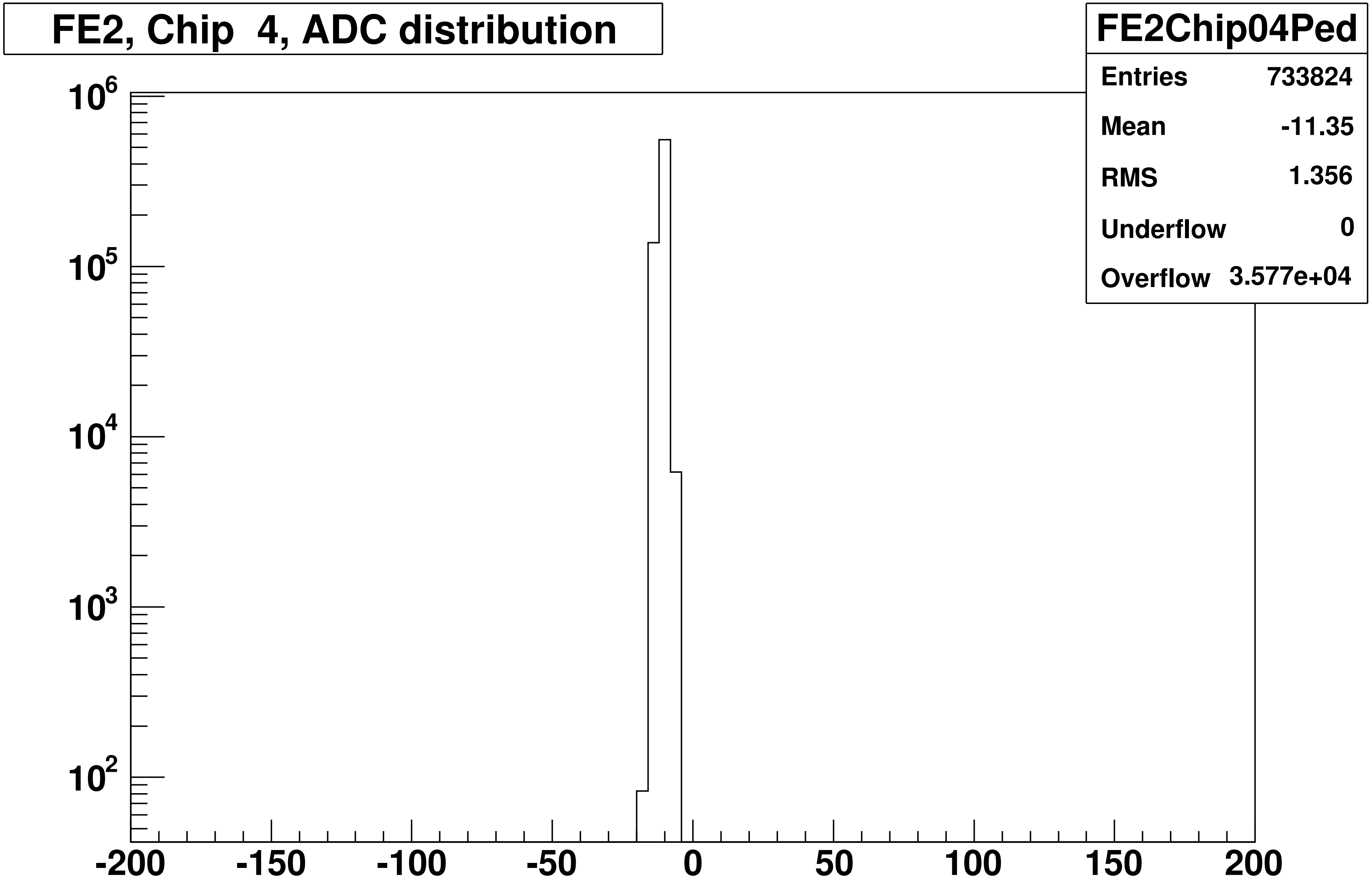
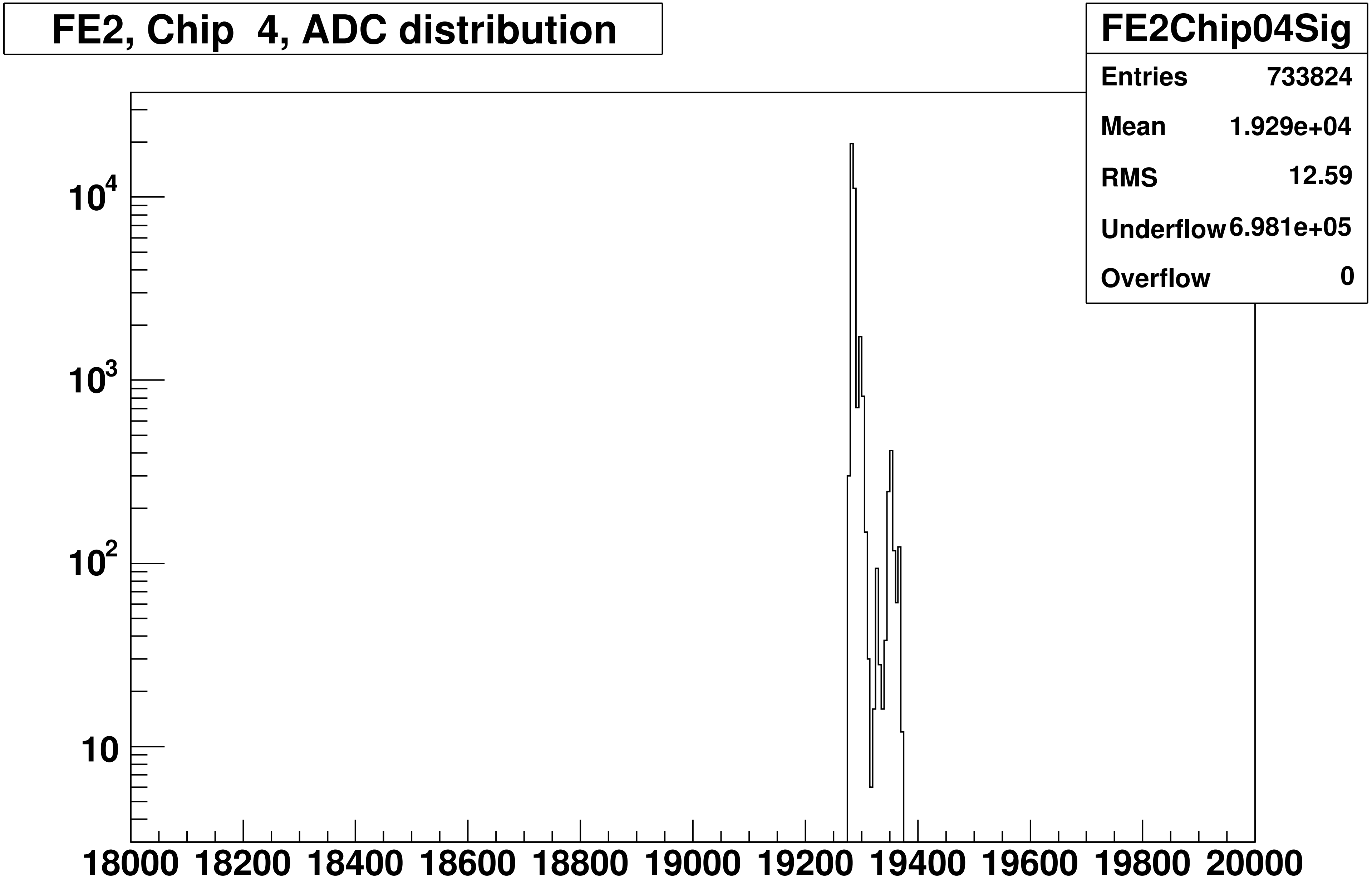
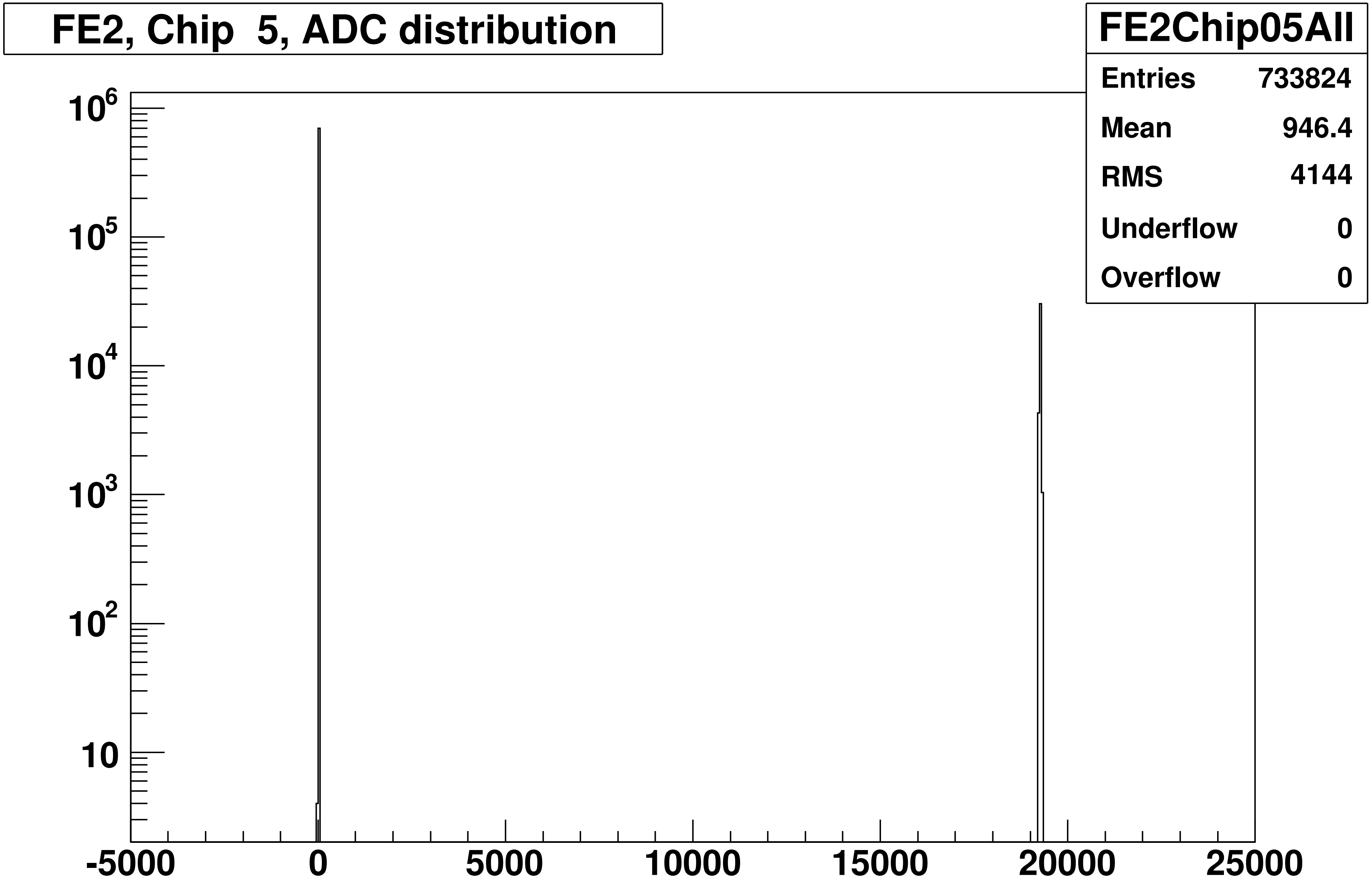
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000



FE2, Chip 4, ADC distribution
FE2Chip04Ped
Entries 733824
Mean -11.35
RMS 1.356
Underflow 0
Overflow 3.577e+04
10^6
10^5
10^4
10^3
10^2
-200 -150 -100 -50 0 50 100 150 200


FE2, Chip 4, ADC distribution
FE2Chip04Sig
Entries 733824
Mean 1.929e+04
RMS 12.59
Underflow 6.981e+05
Overflow 0
10^4
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE2, Chip 5, ADC distribution
FE2Chip05All
Entries 733824
Mean 946.4
RMS 4144
Underflow 0
Overflow 0
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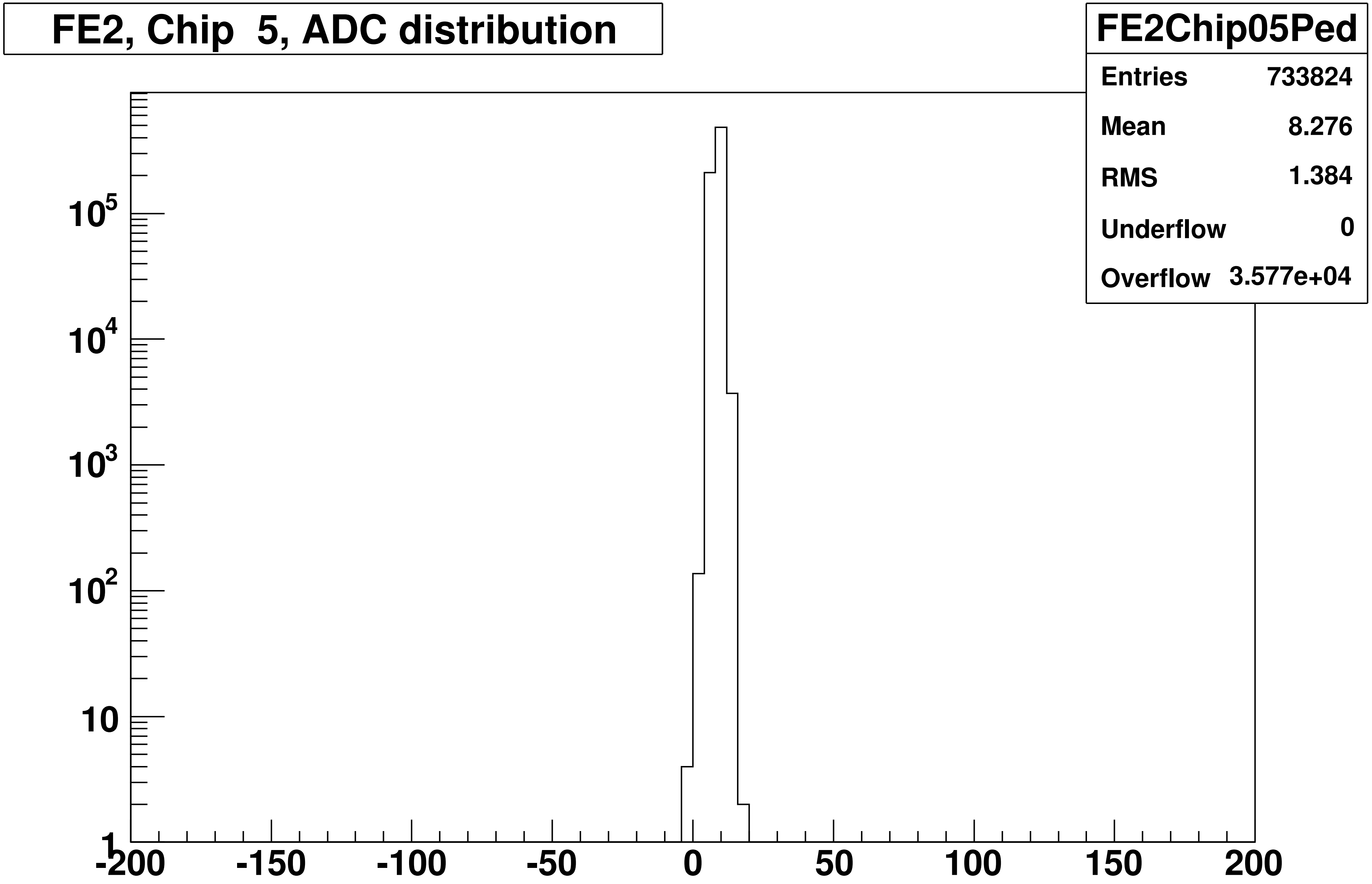
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE2, Chip 5, ADC distribution
FE2Chip05Ped
Entries 733824
Mean 8.276
RMS 1.384
Underflow 0
Overflow 3.577e+04
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10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
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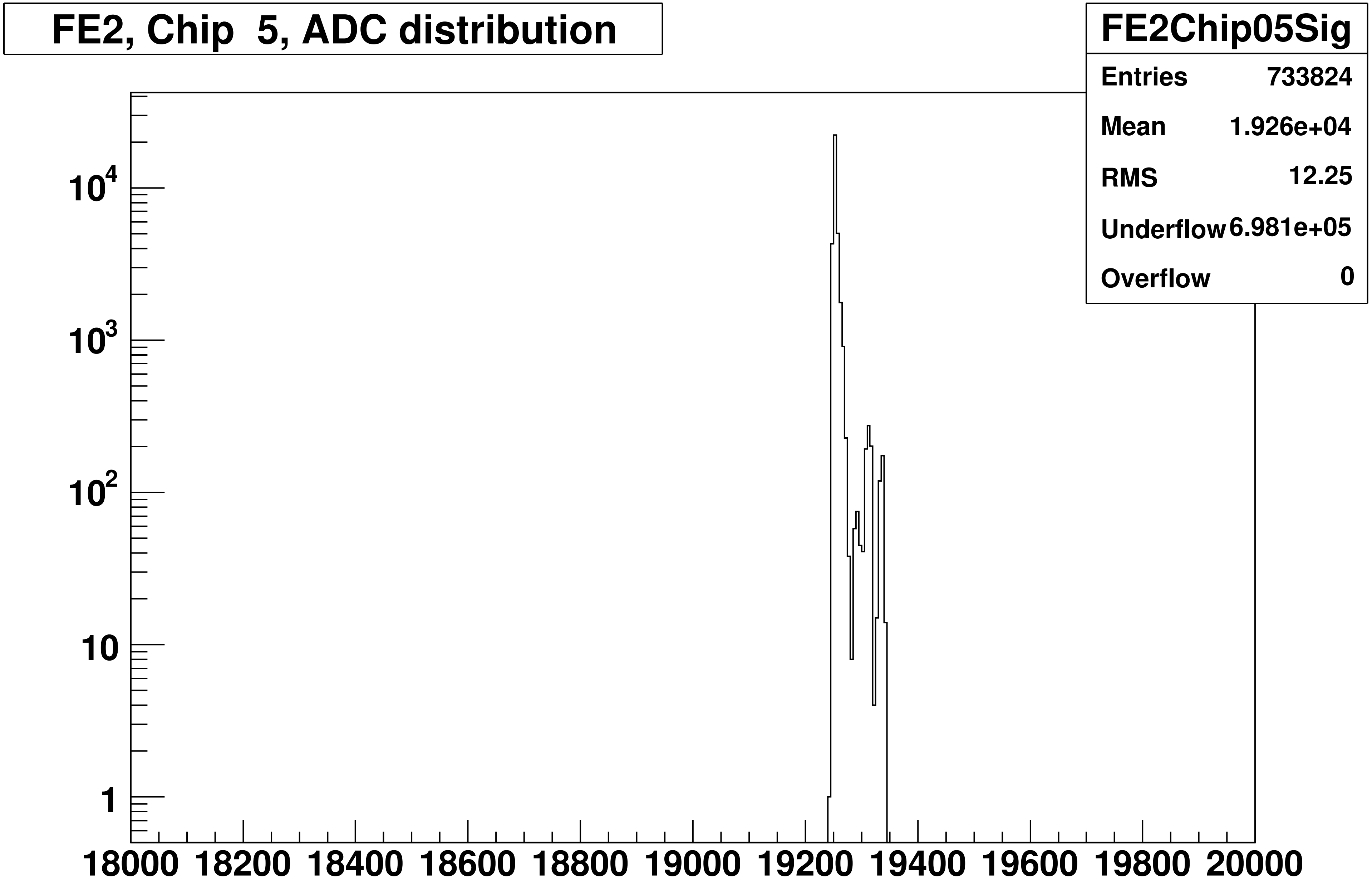
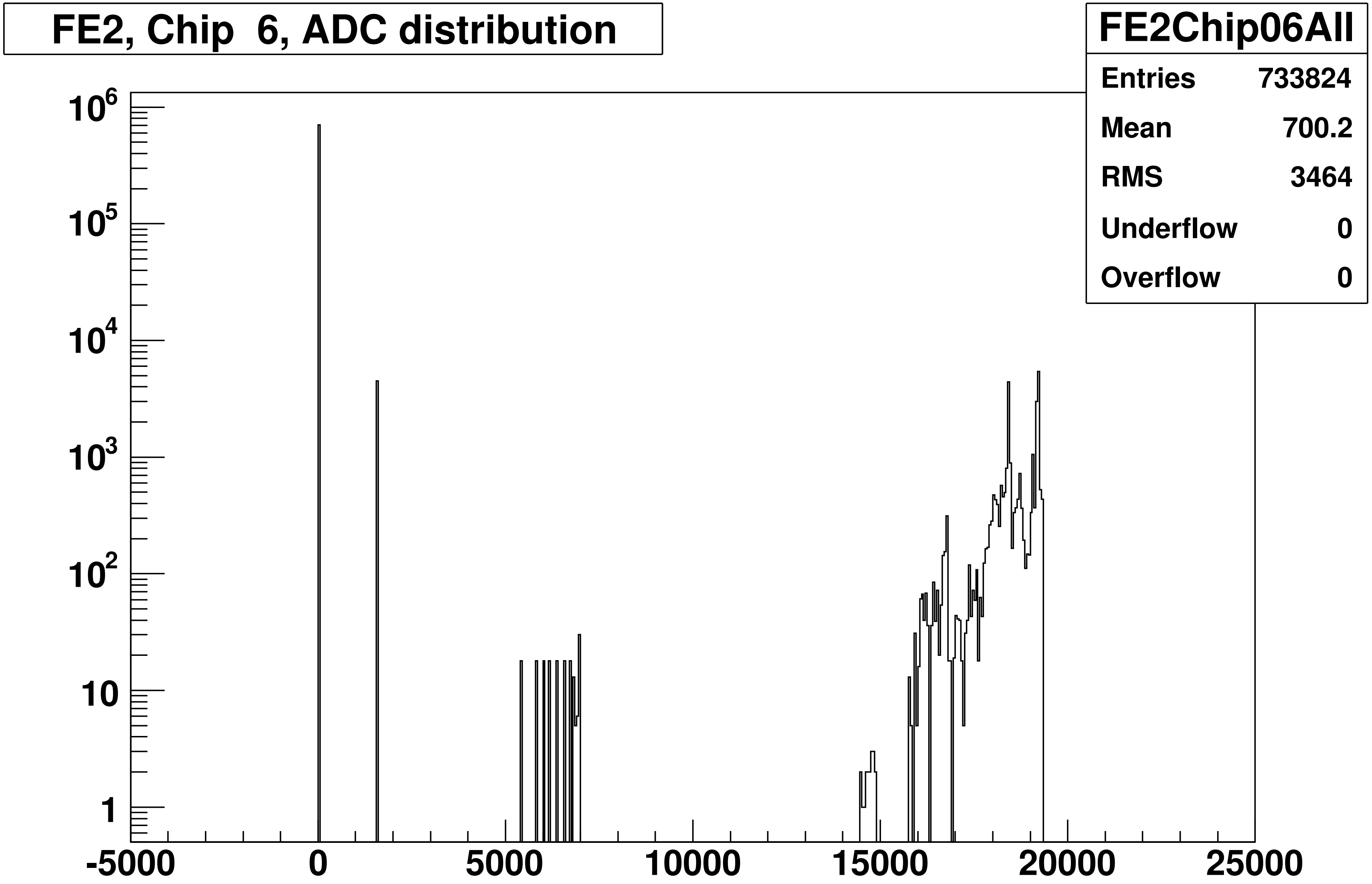
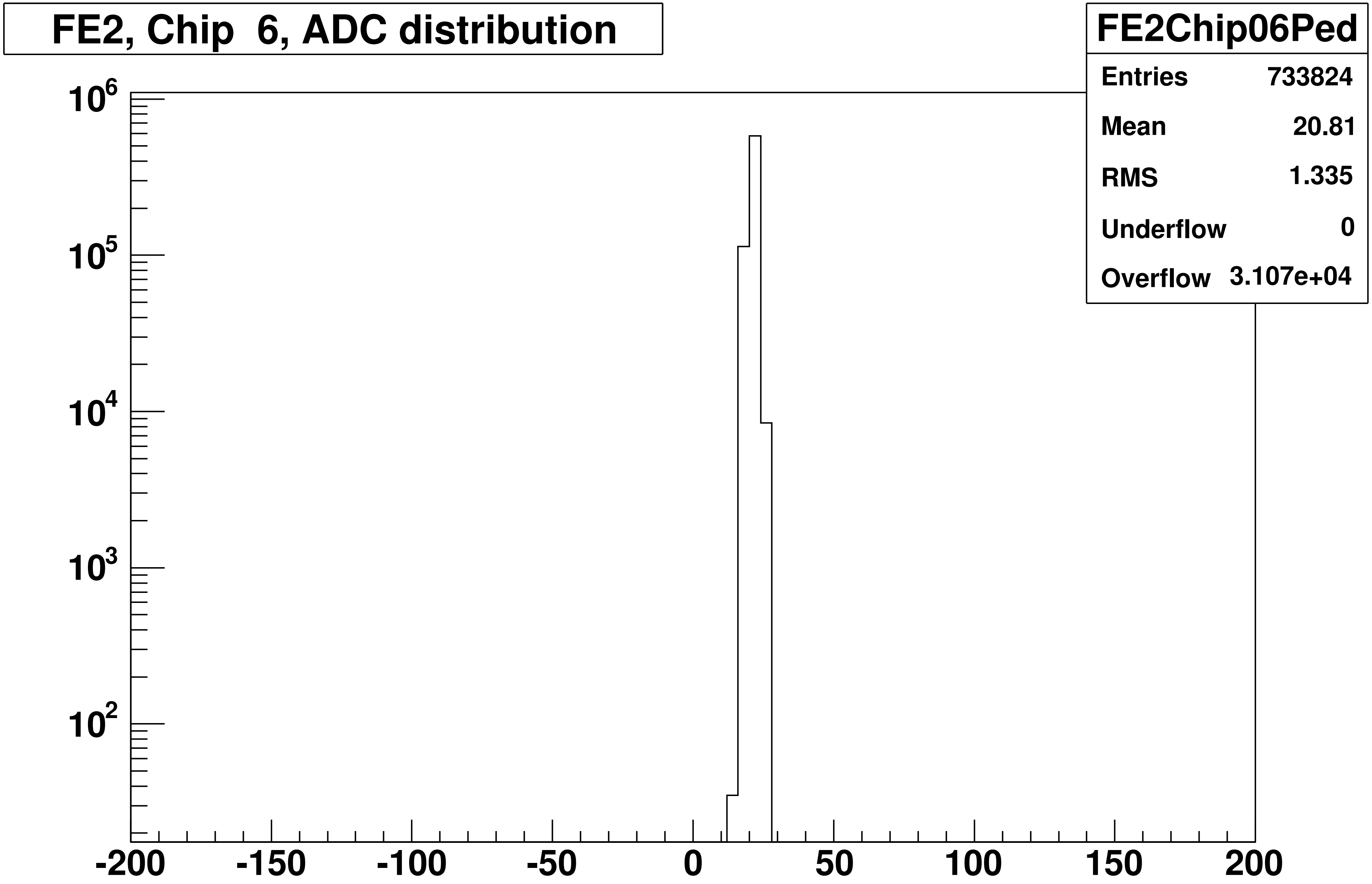
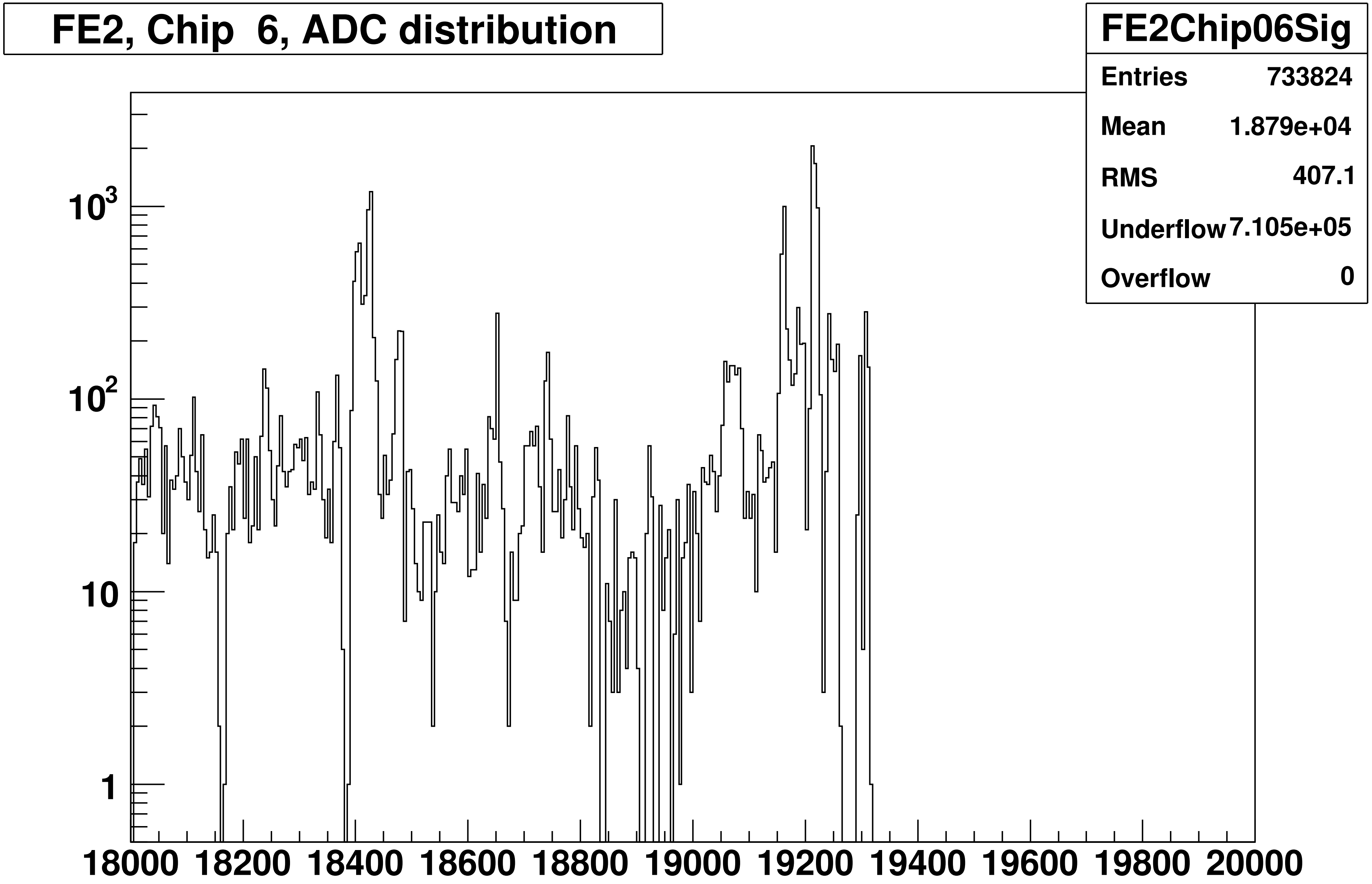
100
150
200


FE2, Chip 5, ADC distribution
FE2Chip05Sig
Entries 733824
Mean 1.926e+04
RMS 12.25
Underflow 6.981e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000


FE2, Chip 6, ADC distribution
FE2Chip06All
Entries 733824
Mean 700.2
RMS 3464
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE2, Chip 6, ADC distribution
FE2Chip06Ped
Entries 733824
Mean 20.81
RMS 1.335
Underflow 0
Overflow 3.107e+04
10^6
10^5
10^4
10^3
10^2
-200
-150
-100
-50
0
50
100
150
200



FE2, Chip 6, ADC distribution
FE2Chip06Sig
Entries 733824
Mean 1.879e+04
RMS 407.1
Underflow 7.105e+05
Overflow 0
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
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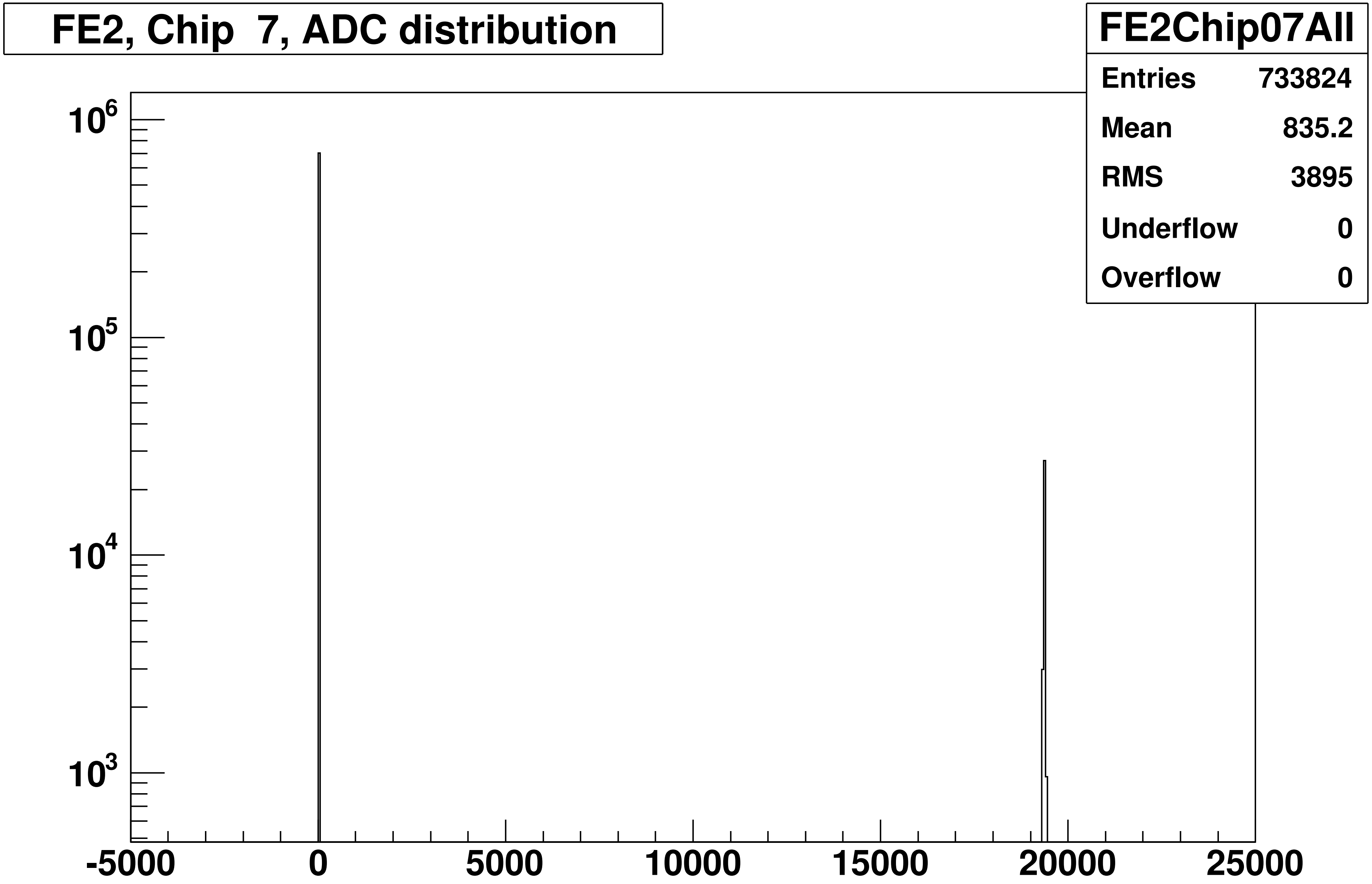
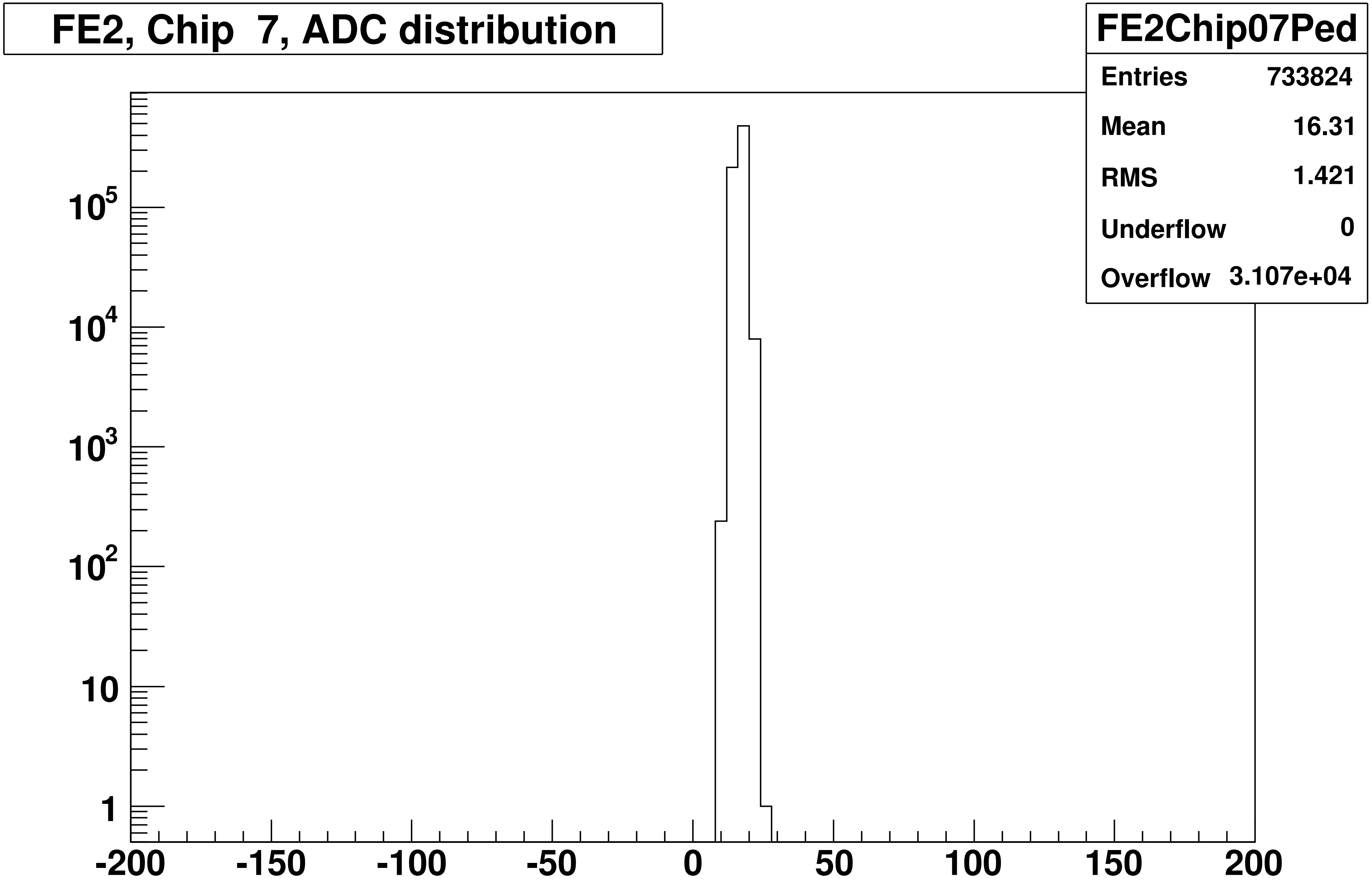
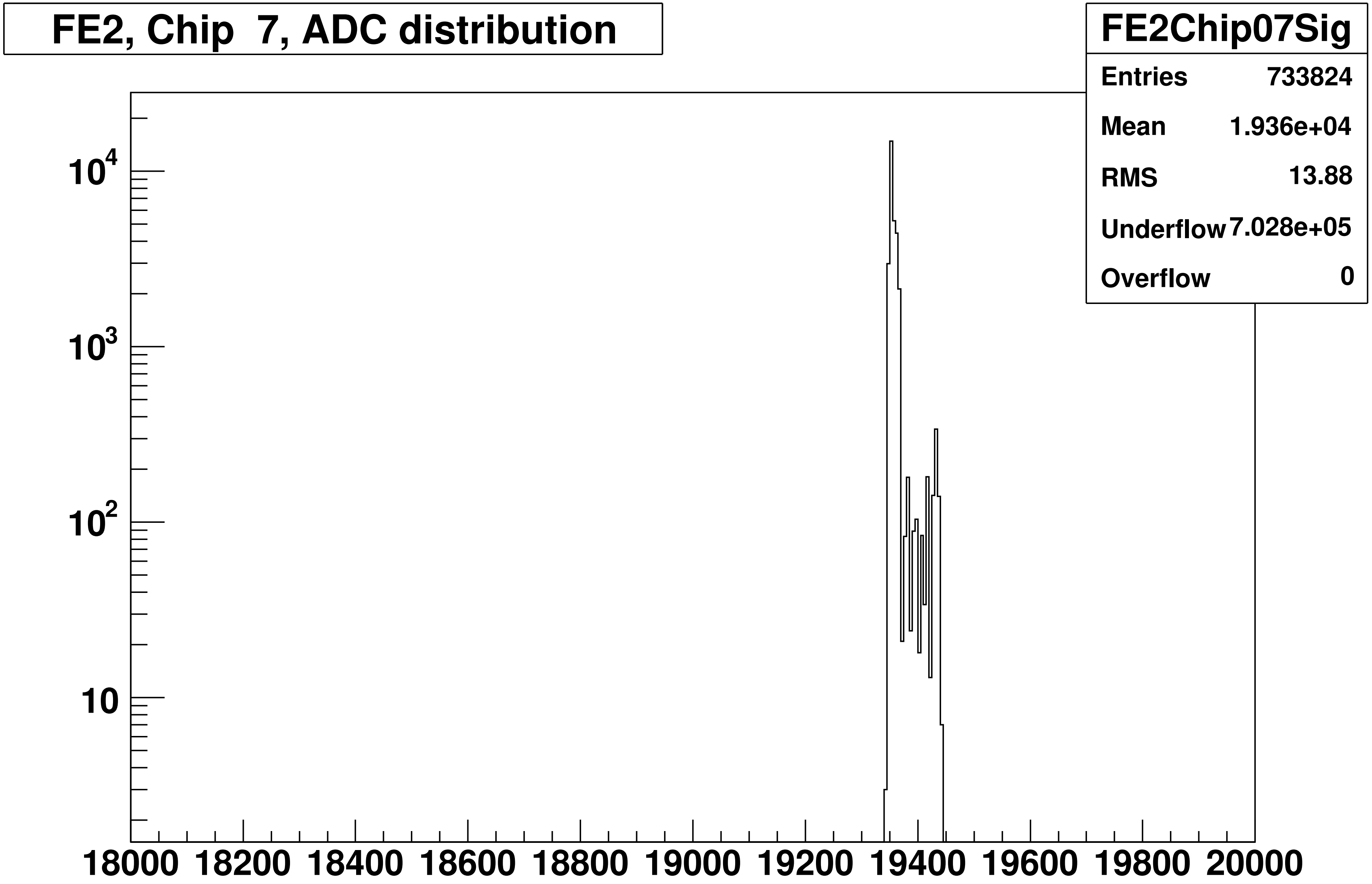
19600
19800
20000

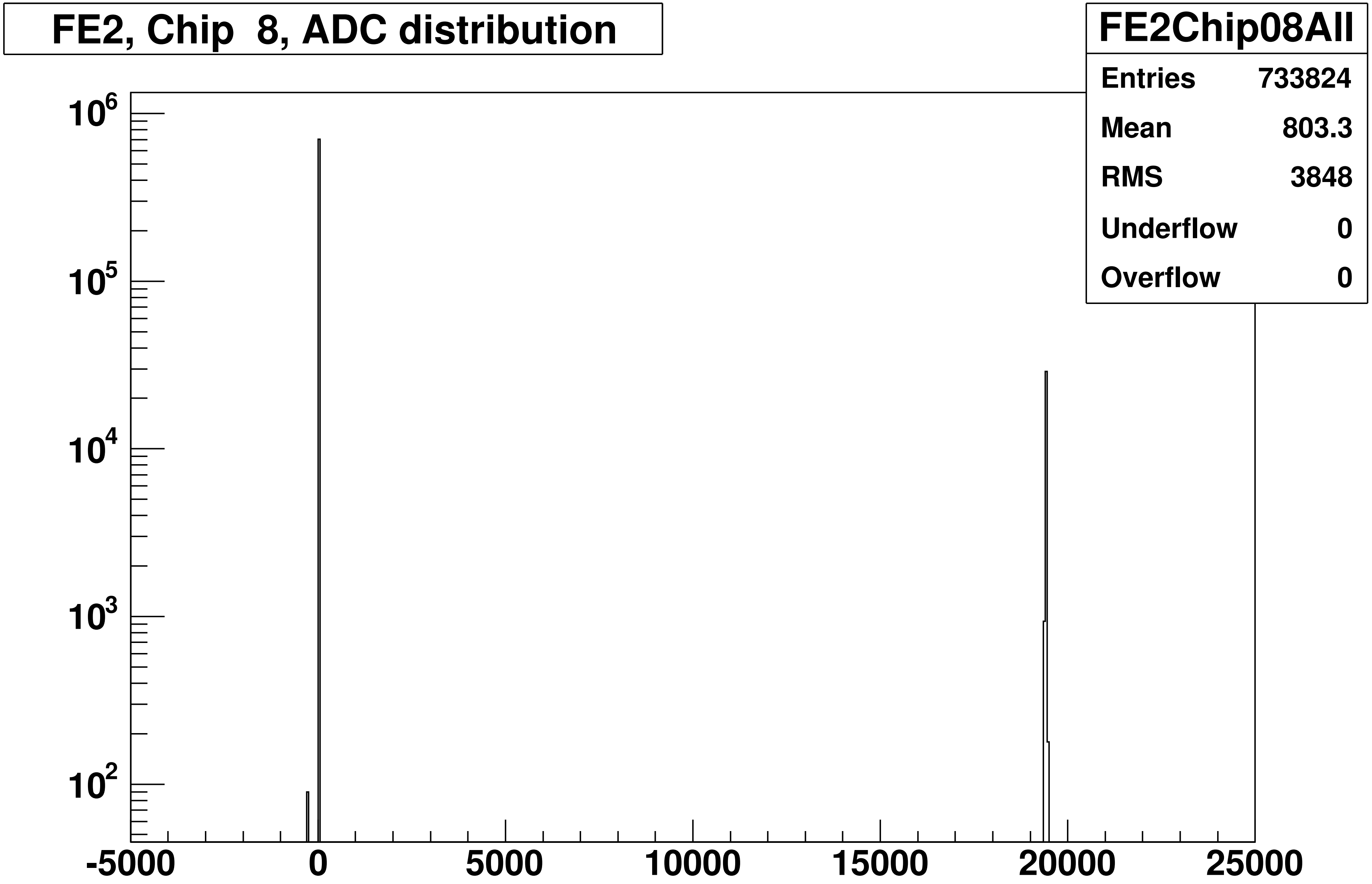

FE2, Chip 7, ADC distribution
FE2Chip07All
Entries 733824
Mean 835.2
RMS 3895
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
-5000
0
5000
10000
15000
20000
25000



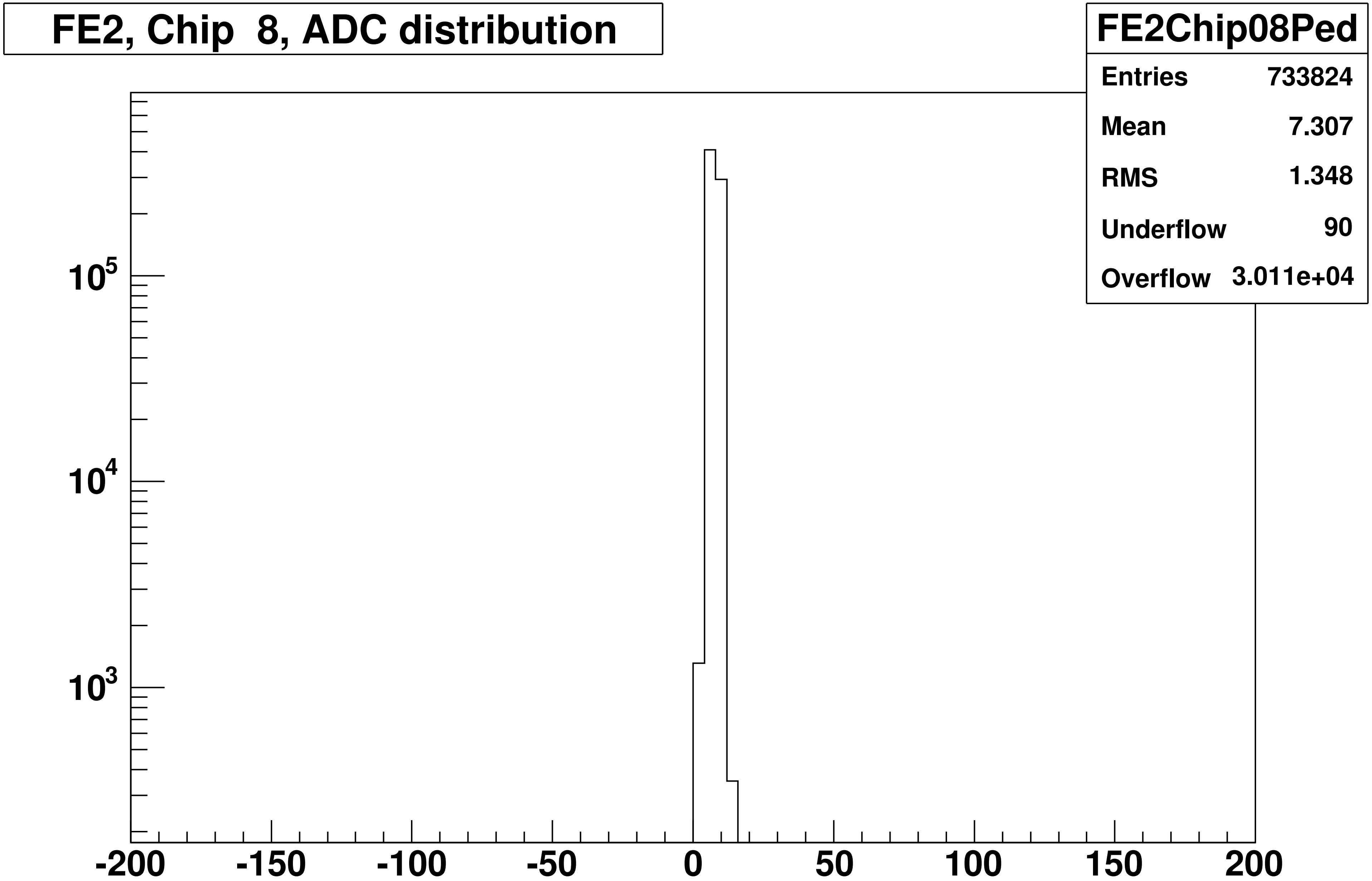
FE2, Chip 7, ADC distribution
FE2Chip07Ped
Entries 733824
Mean 16.31
RMS 1.421
Underflow 0
Overflow 3.107e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
200

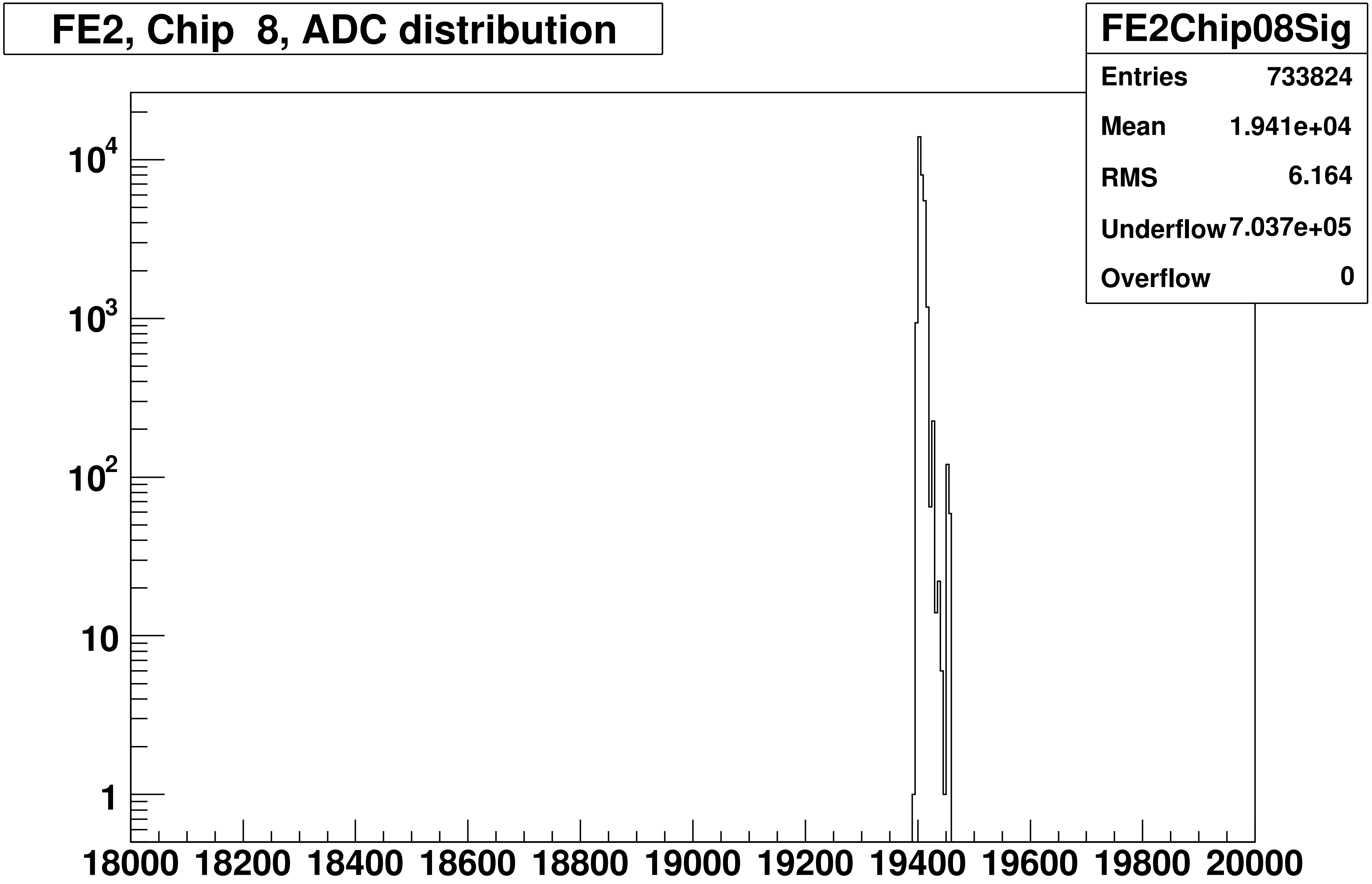


FE2, Chip 7, ADC distribution
FE2Chip07Sig
Entries 733824
Mean 1.936e+04
RMS 13.88
Underflow 7.028e+05
Overflow 0
10^4
10^3
10^2
10
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000

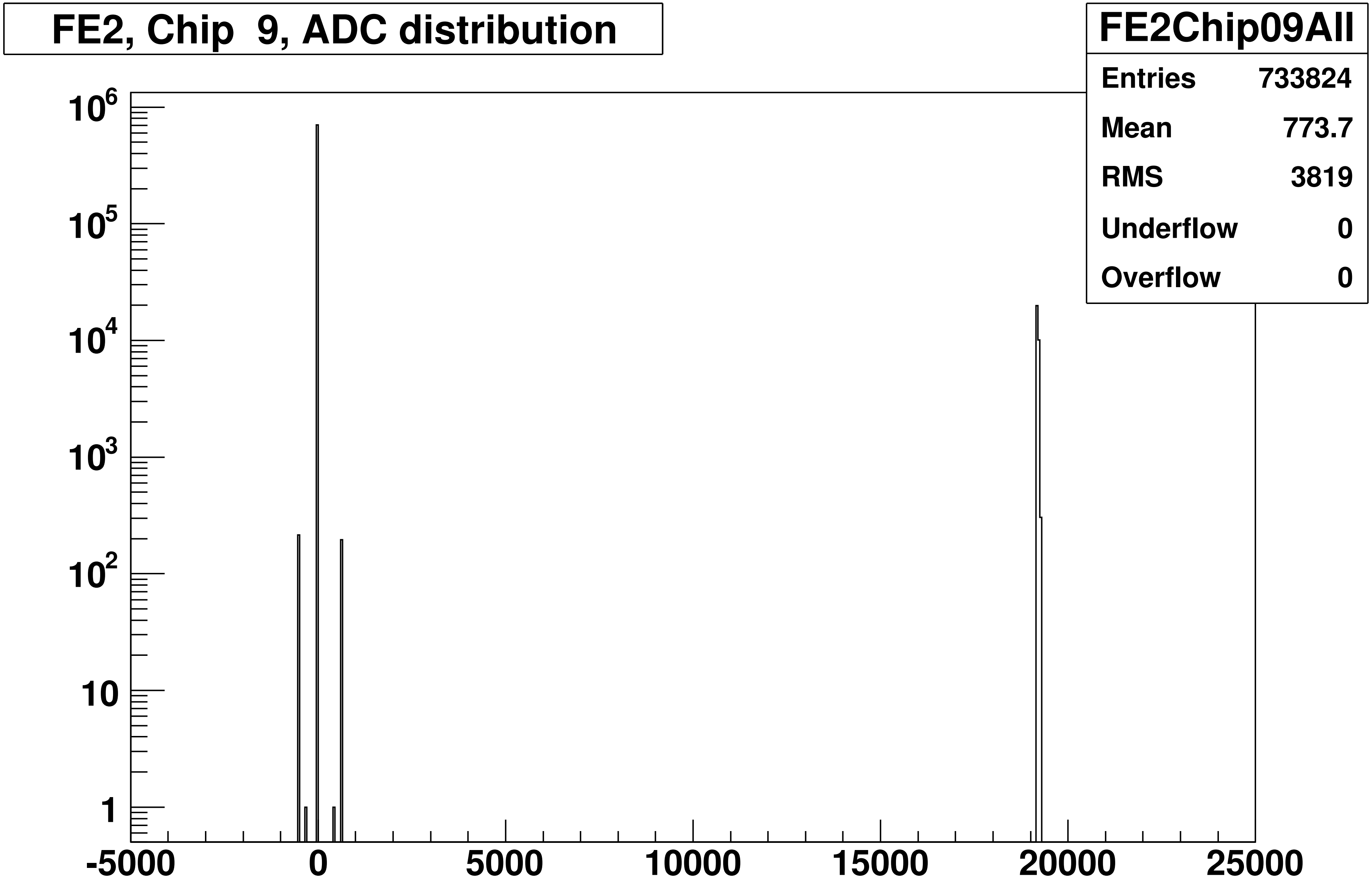


FE2, Chip 8, ADC distribution
FE2Chip08All
Entries 733824
Mean 803.3
RMS 3848
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000

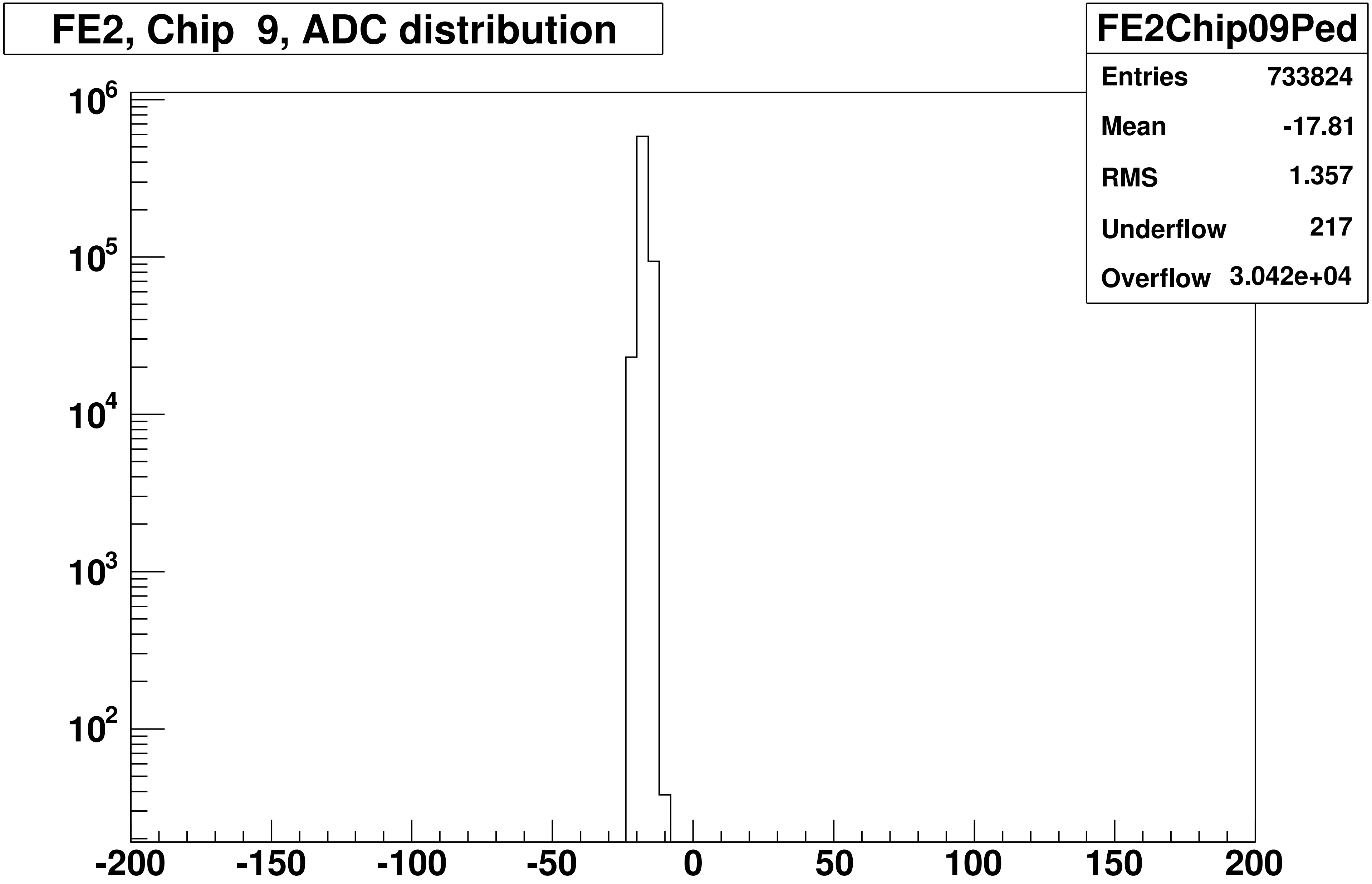

FE2, Chip 8, ADC distribution
FE2Chip08Ped
Entries 733824
Mean 7.307
RMS 1.348
Underflow 90
Overflow 3.011e+04
10^5
10^4
10^3
-200
-150
-100
-50
0
50
100
150
200



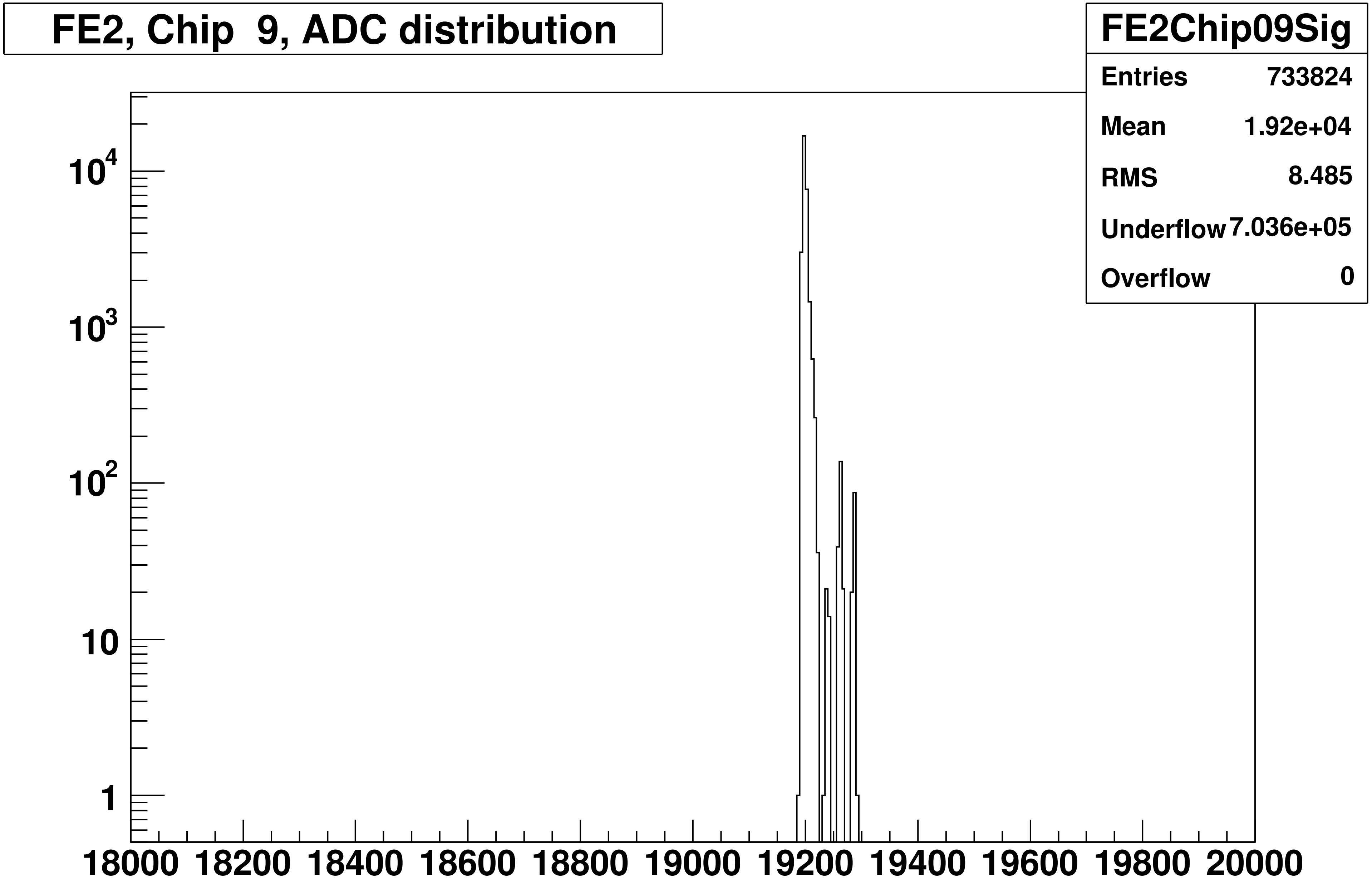
FE2, Chip 8, ADC distribution
FE2Chip08Sig
Entries 733824
Mean 1.941e+04
RMS 6.164
Underflow 7.037e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



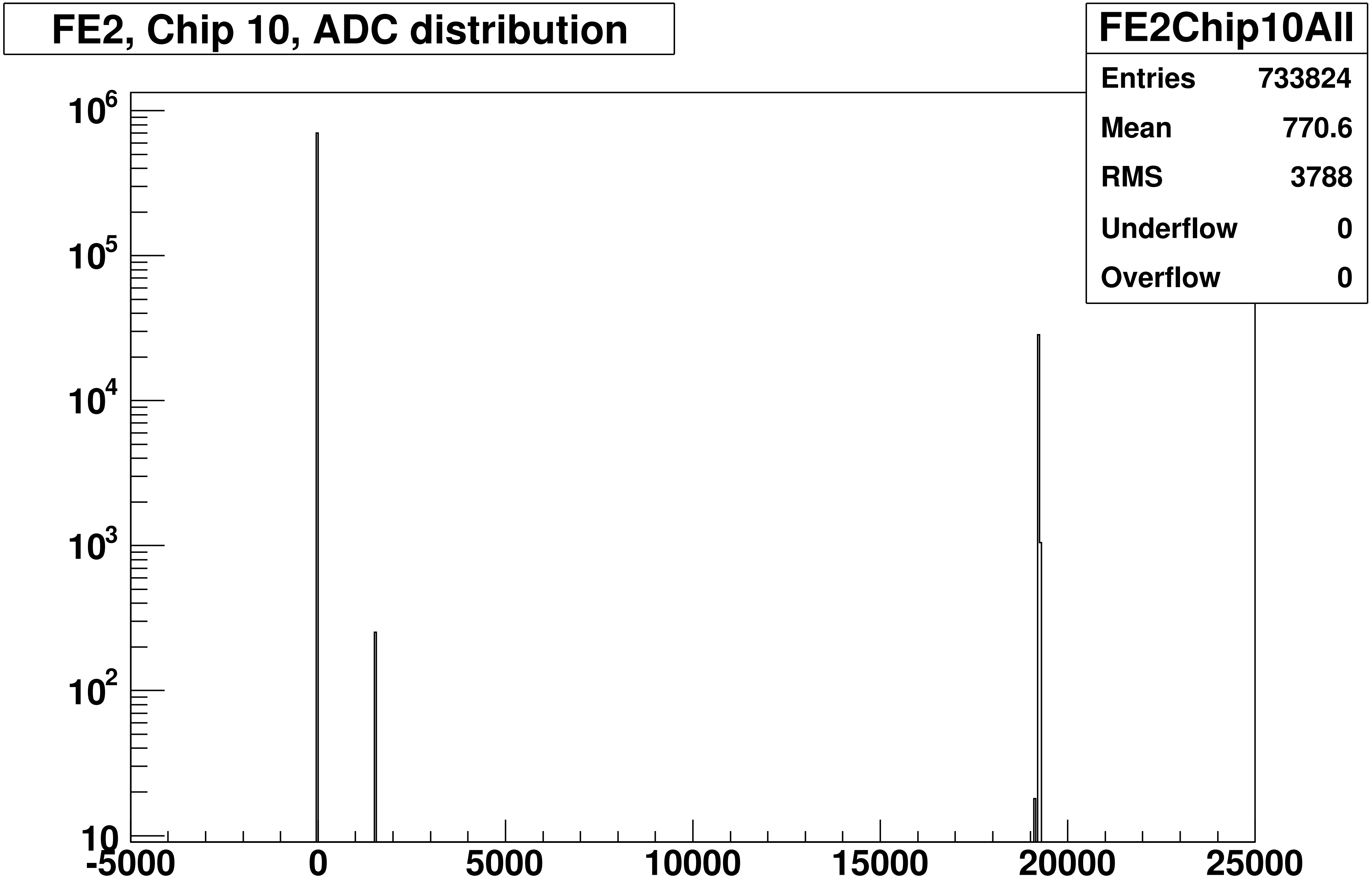
FE2, Chip 9, ADC distribution
FE2Chip09All
Entries 733824
Mean 773.7
RMS 3819
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE2, Chip 9, ADC distribution
FE2Chip09Ped
Entries 733824
Mean -17.81
RMS 1.357
Underflow 217
Overflow 3.042e+04
10^6
10^5
10^4
10^3
10^2
-200
-150
-100
-50
0
50
100
150
200



FE2, Chip 9, ADC distribution
FE2Chip09Sig
Entries 733824
Mean 1.92e+04
RMS 8.485
Underflow 7.036e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE2, Chip 10, ADC distribution
FE2Chip10All
Entries 733824
Mean 770.6
RMS 3788
Underflow 0
Overflow 0
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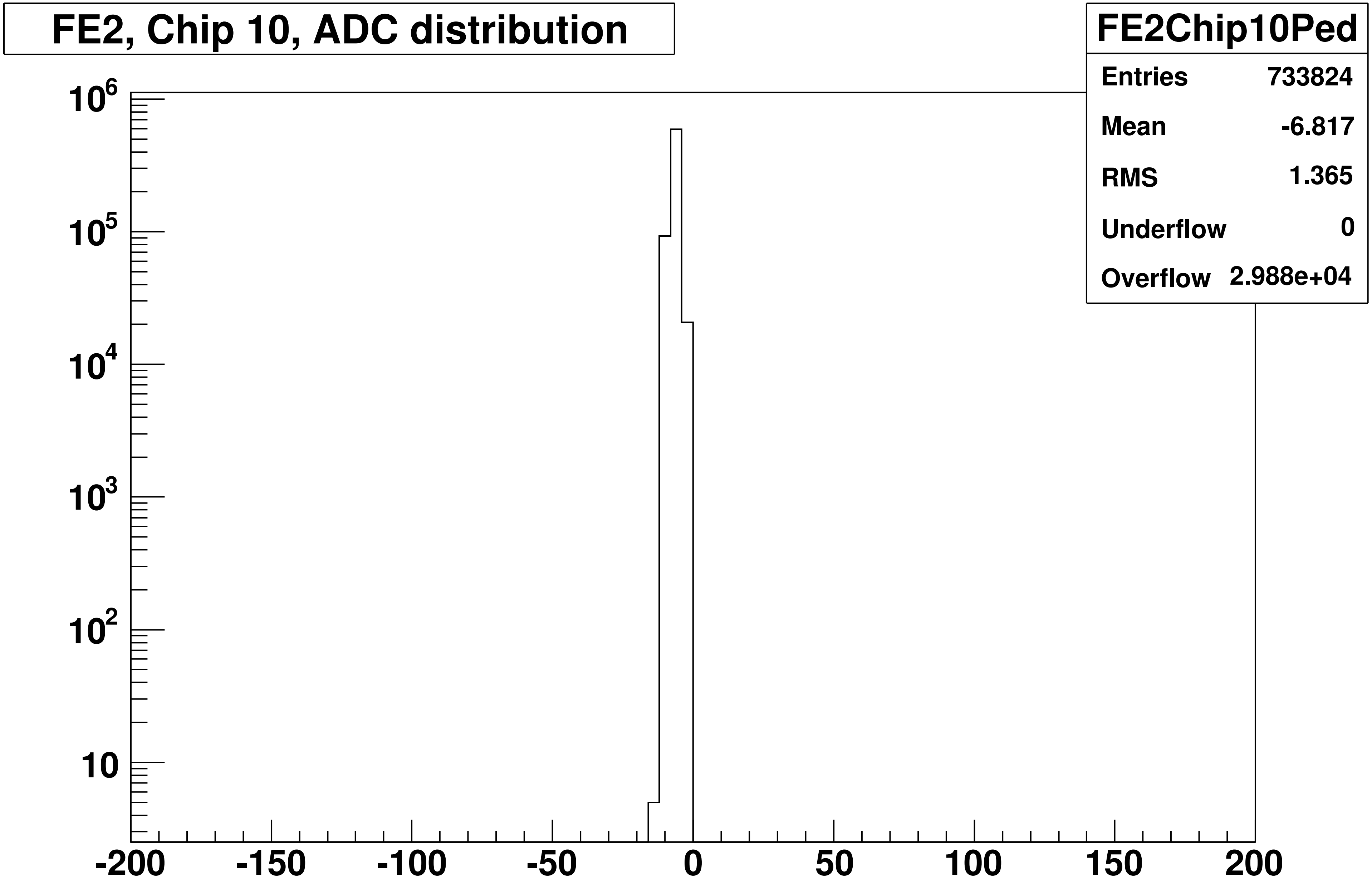
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000



FE2, Chip 10, ADC distribution
FE2Chip10Ped
Entries 733824
Mean -6.817
RMS 1.365
Underflow 0
Overflow 2.988e+04
10^6
10^5
10^4
10^3
10^2
10
-200
-150
-100
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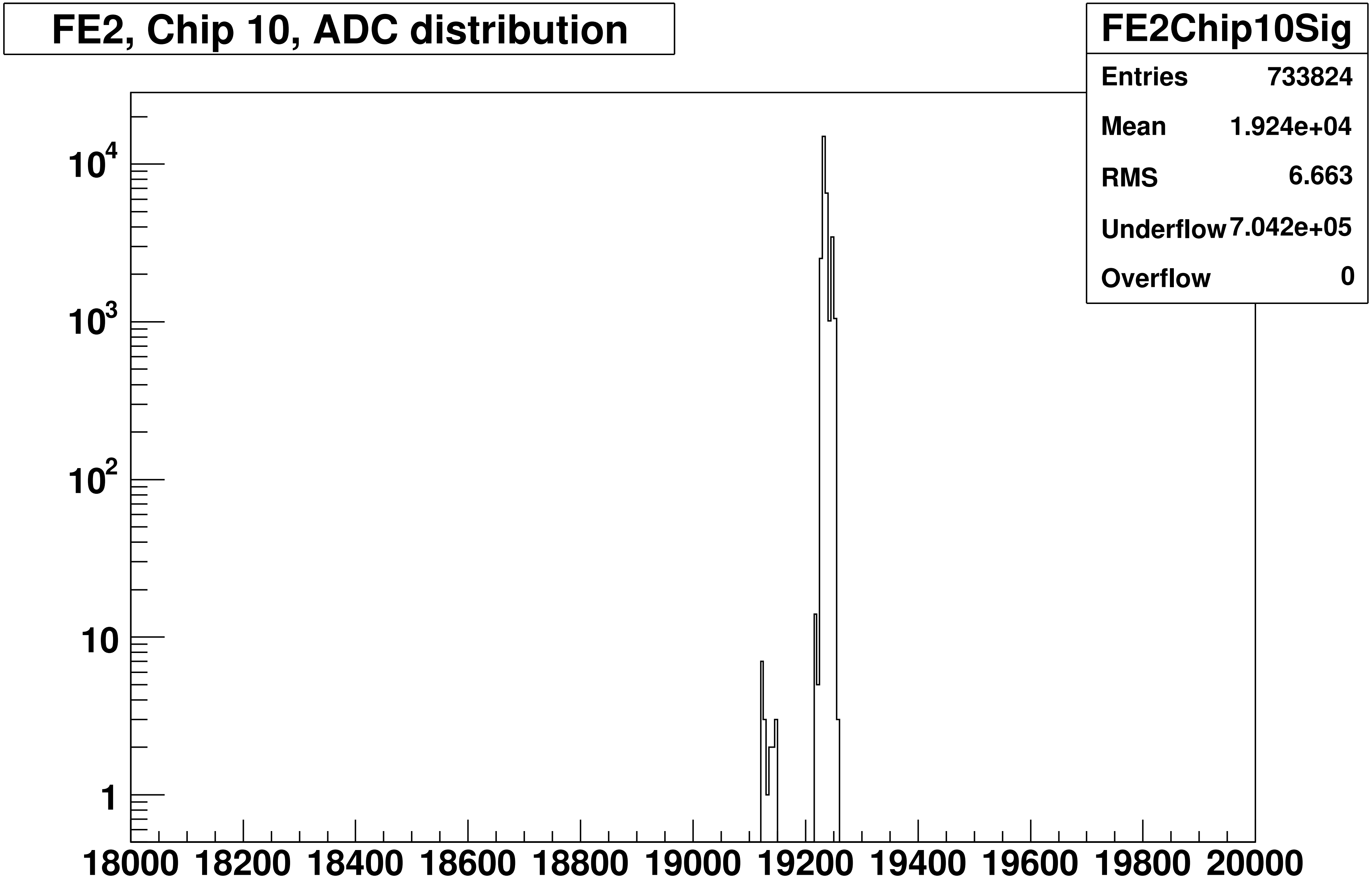
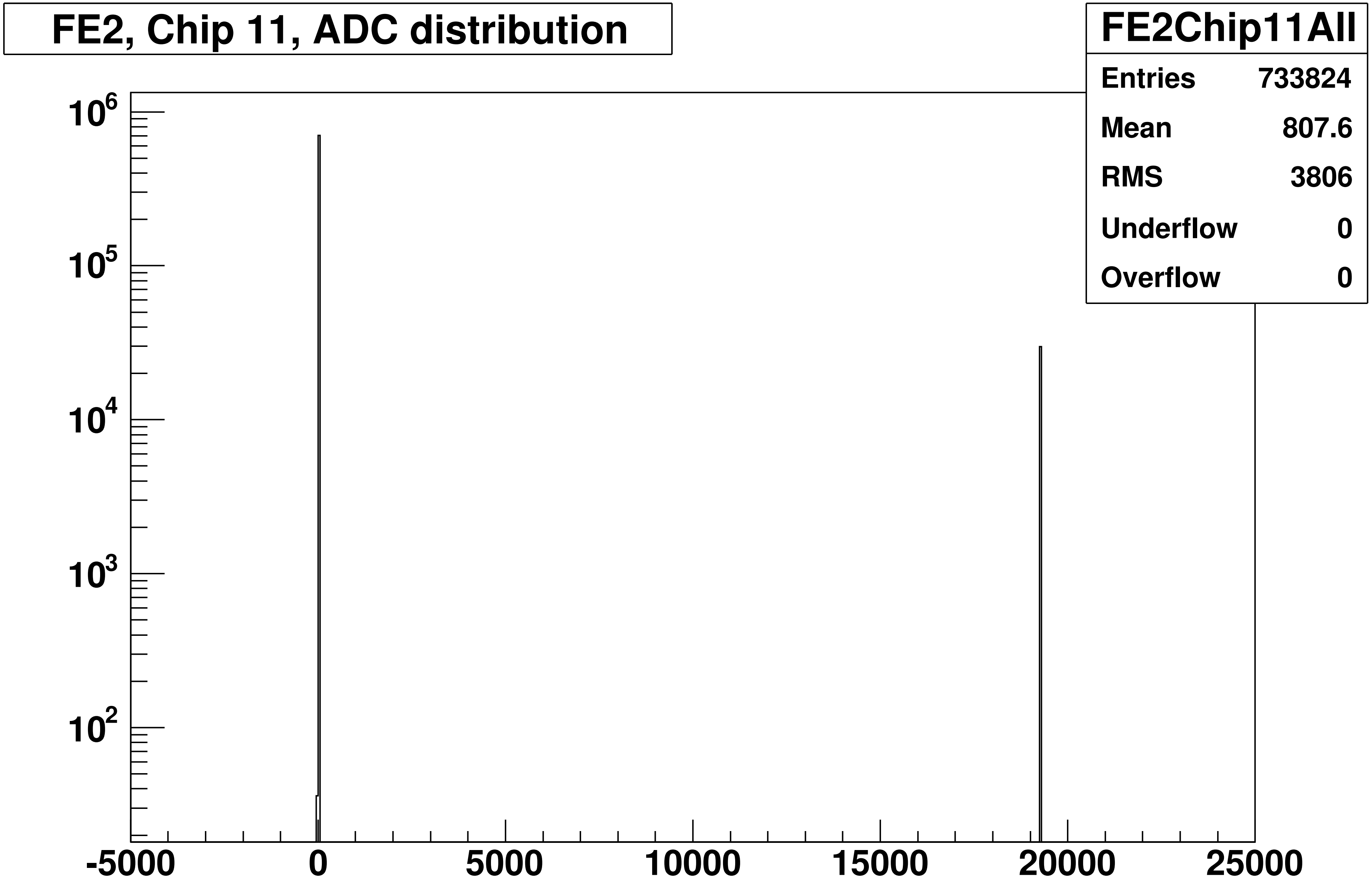
150
200


FE2, Chip 10, ADC distribution
FE2Chip10Sig
Entries 733824
Mean 1.924e+04
RMS 6.663
Underflow 7.042e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE2, Chip 11, ADC distribution
FE2Chip11All
Entries 733824
Mean 807.6
RMS 3806
Underflow 0
Overflow 0
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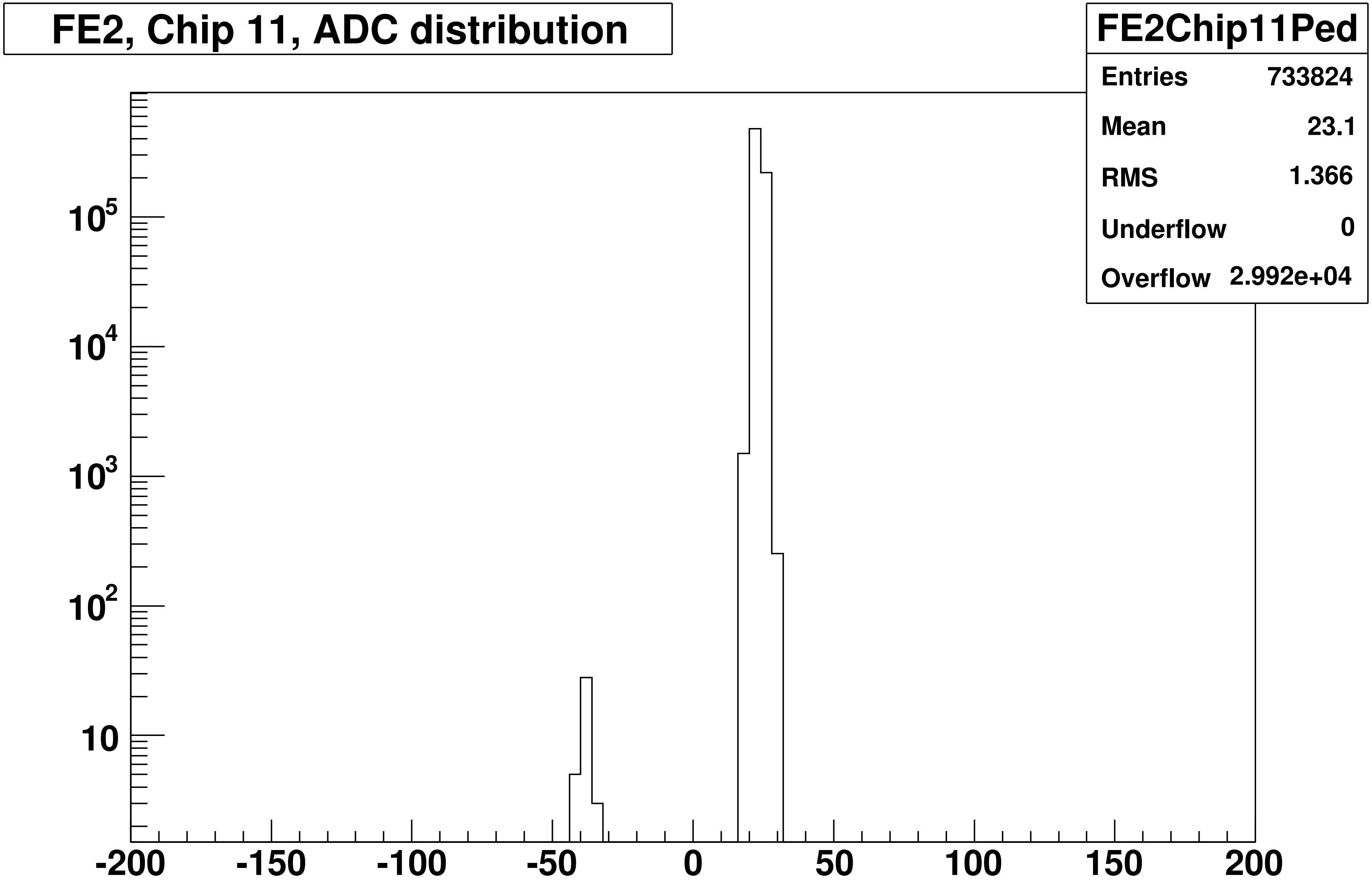
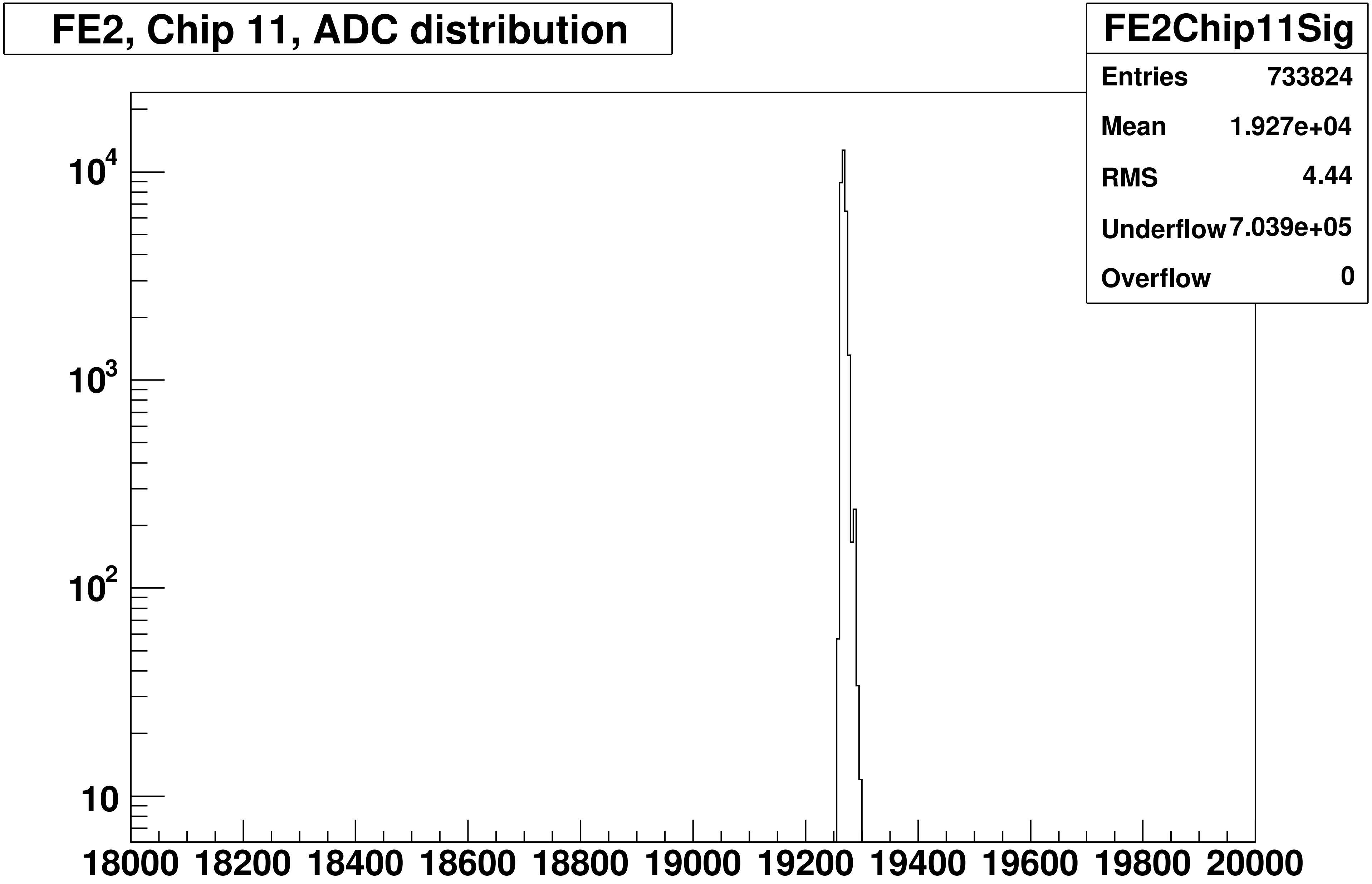
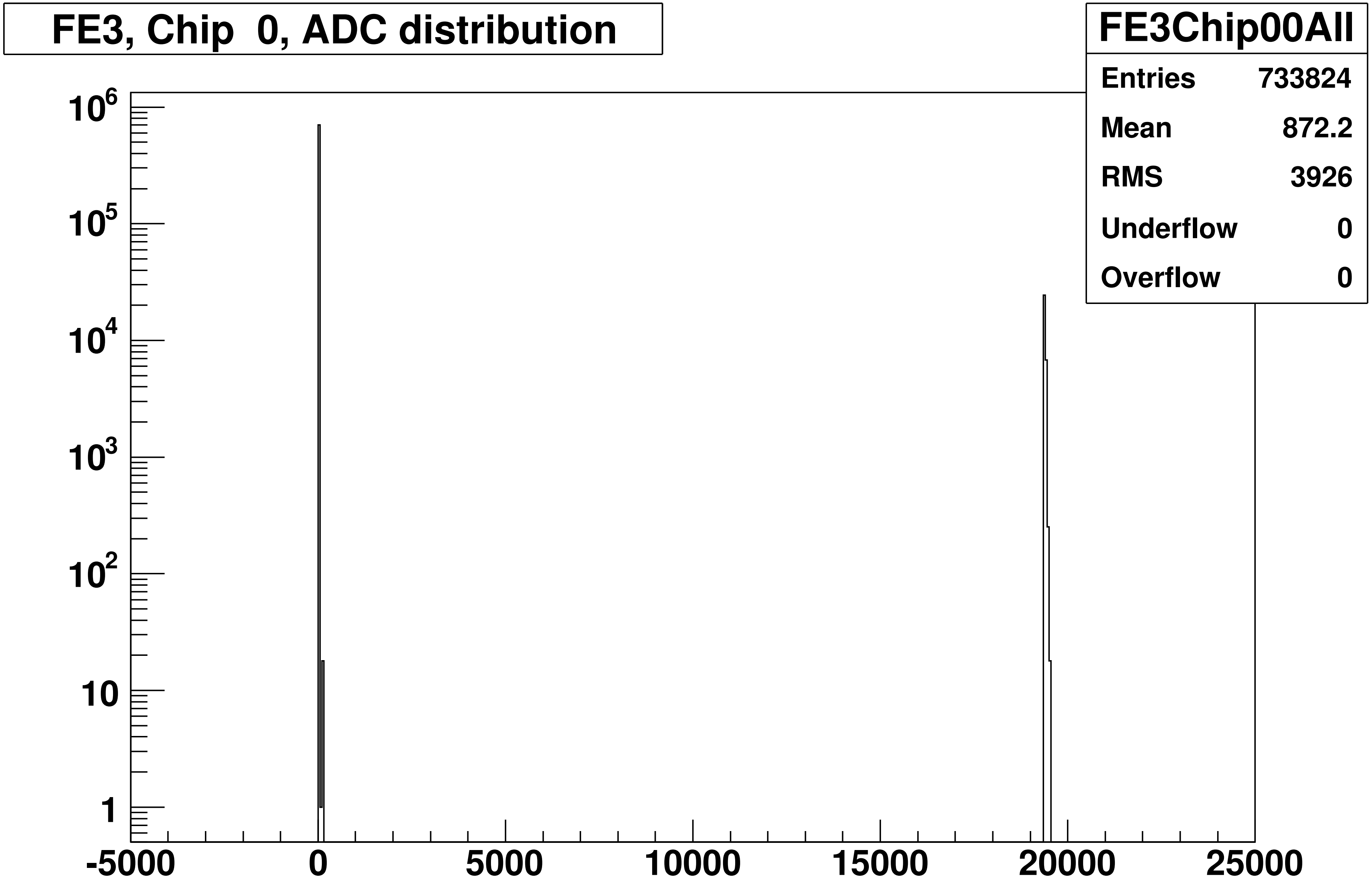
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000


FE2, Chip 11, ADC distribution
FE2Chip11Ped
Entries 733824
Mean 23.1
RMS 1.366
Underflow 0
Overflow 2.992e+04
10
10^2
10^3
10^4
10^5
-200
-150
-100
-50
0
50
100
150
200


FE2, Chip 11, ADC distribution
FE2Chip11Sig
Entries 733824
Mean 1.927e+04
RMS 4.44
Underflow 7.039e+05
Overflow 0
10^4
10^3
10^2
10
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000



FE3, Chip 0, ADC distribution
FE3Chip00All
Entries 733824
Mean 872.2
RMS 3926
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
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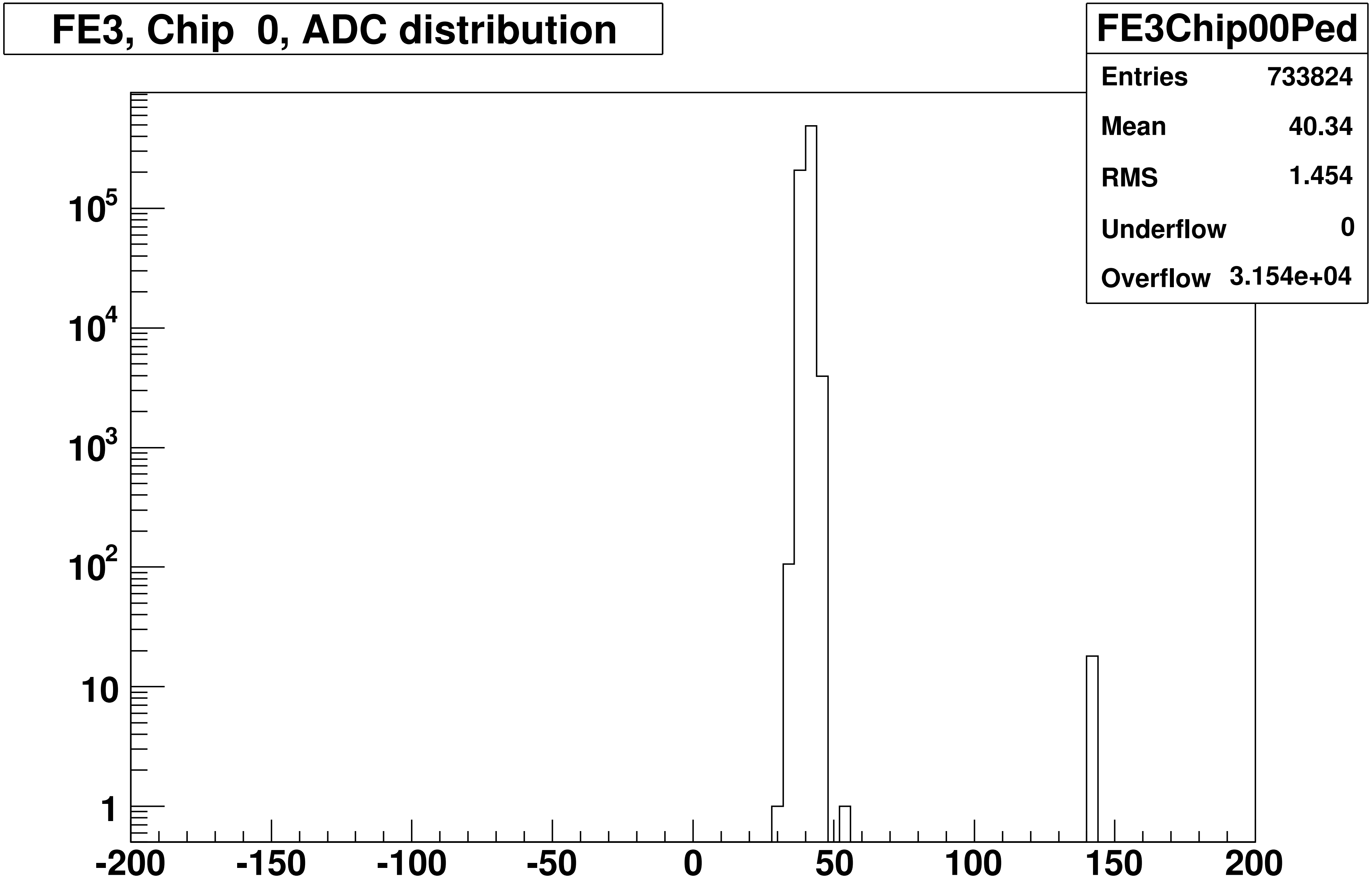
20000
25000



FE3, Chip 0, ADC distribution
FE3Chip00Ped
Entries 733824
Mean 40.34
RMS 1.454
Underflow 0
Overflow 3.154e+04
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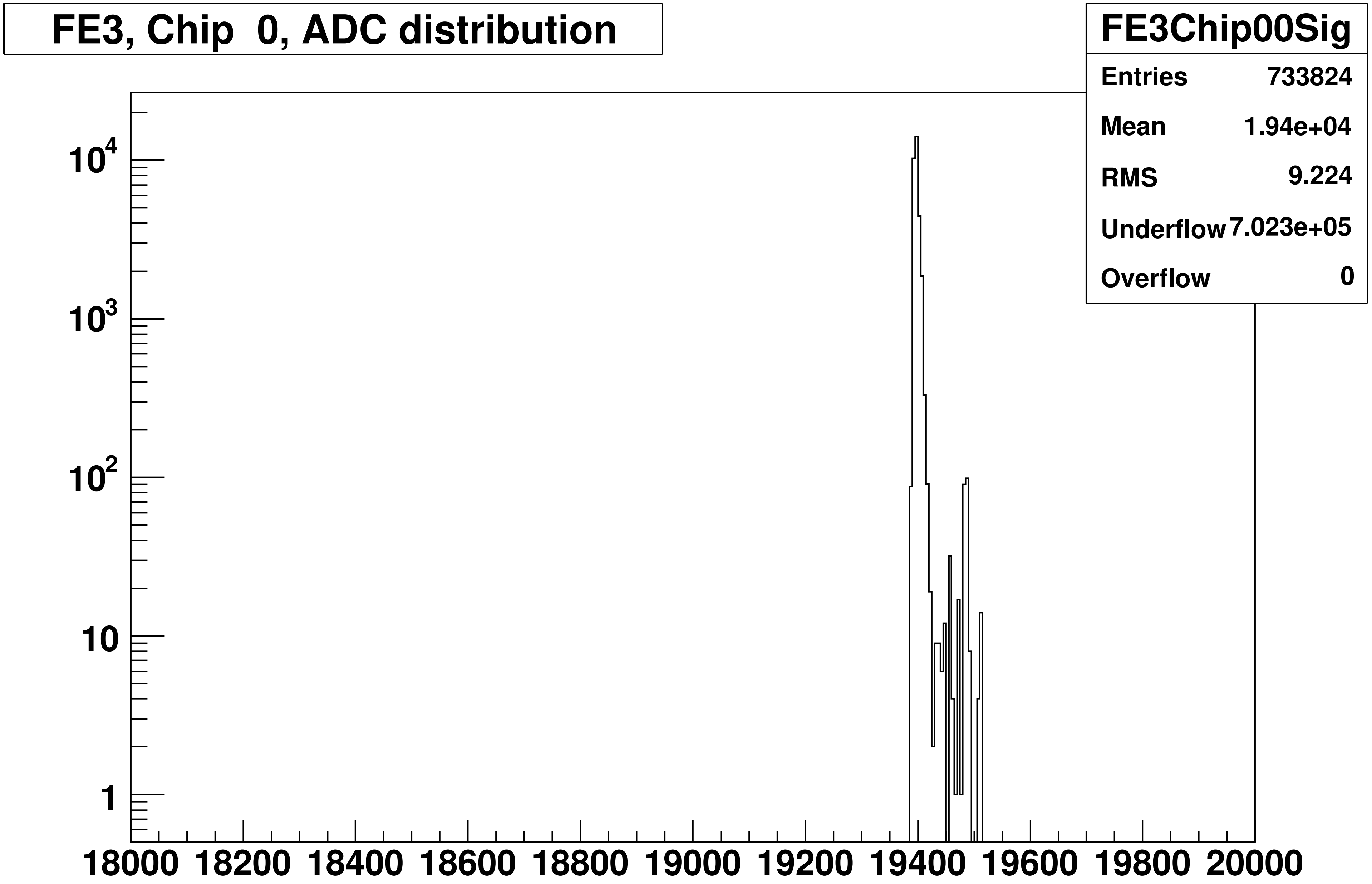
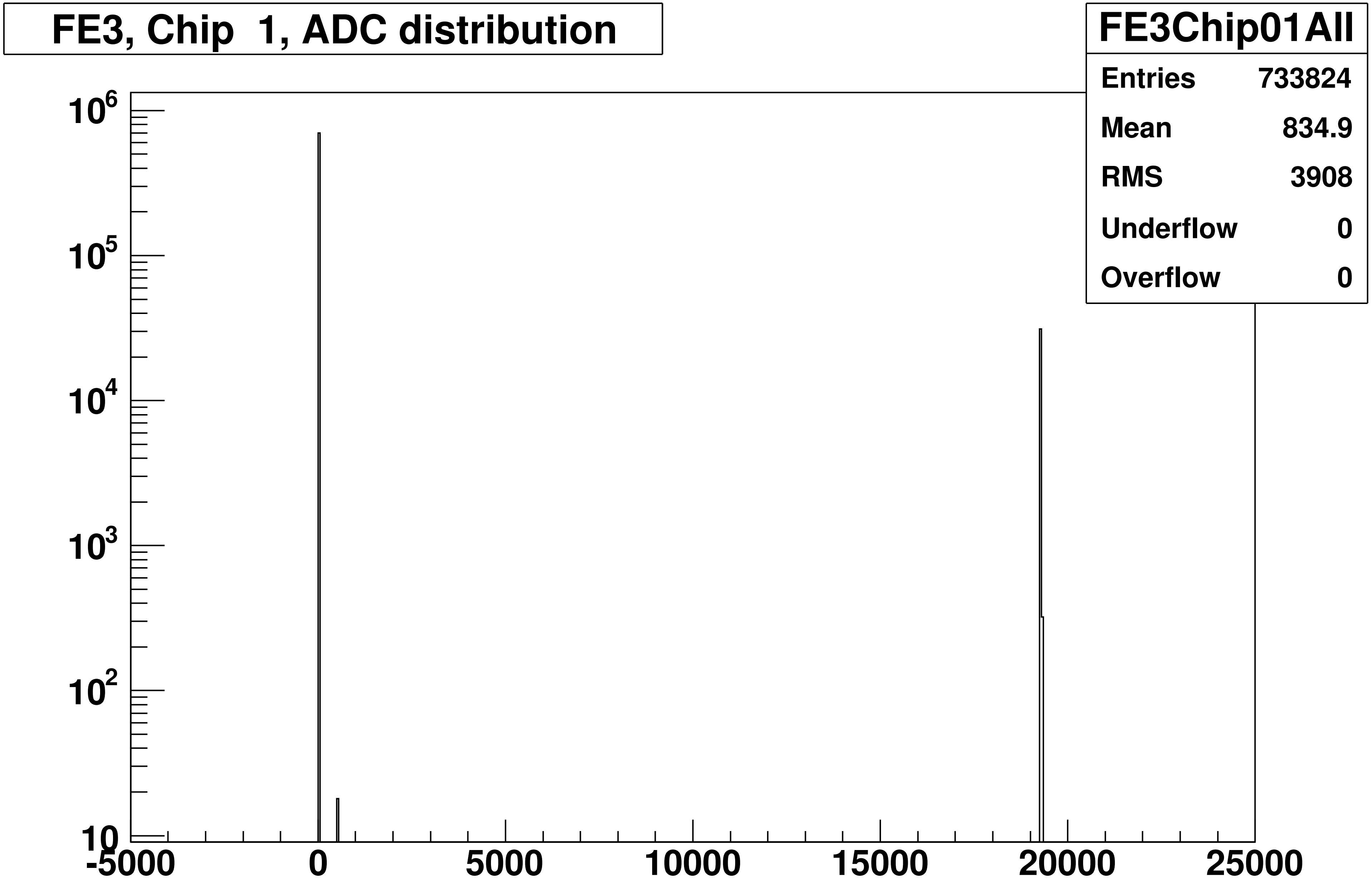
1
-200
-150
-100
-50
0
50
100
150
200



FE3, Chip 0, ADC distribution
FE3Chip00Sig
Entries 733824
Mean 1.94e+04
RMS 9.224
Underflow 7.023e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE3, Chip 1, ADC distribution
FE3Chip01All
Entries 733824
Mean 834.9
RMS 3908
Underflow 0
Overflow 0
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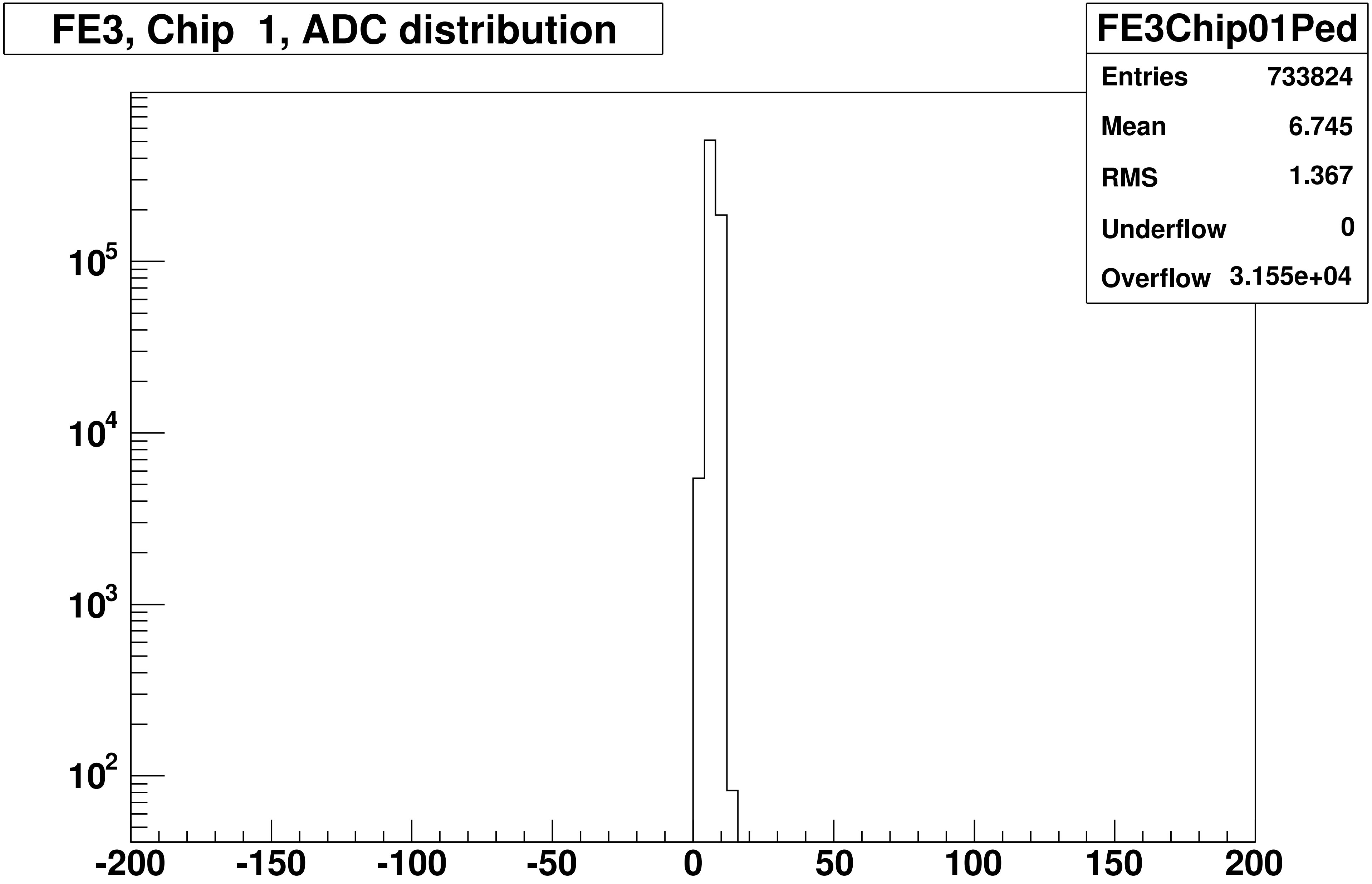
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE3, Chip 1, ADC distribution
FE3Chip01Ped
Entries 733824
Mean 6.745
RMS 1.367
Underflow 0
Overflow 3.155e+04
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10^4
10^3
10^2
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-150
-100
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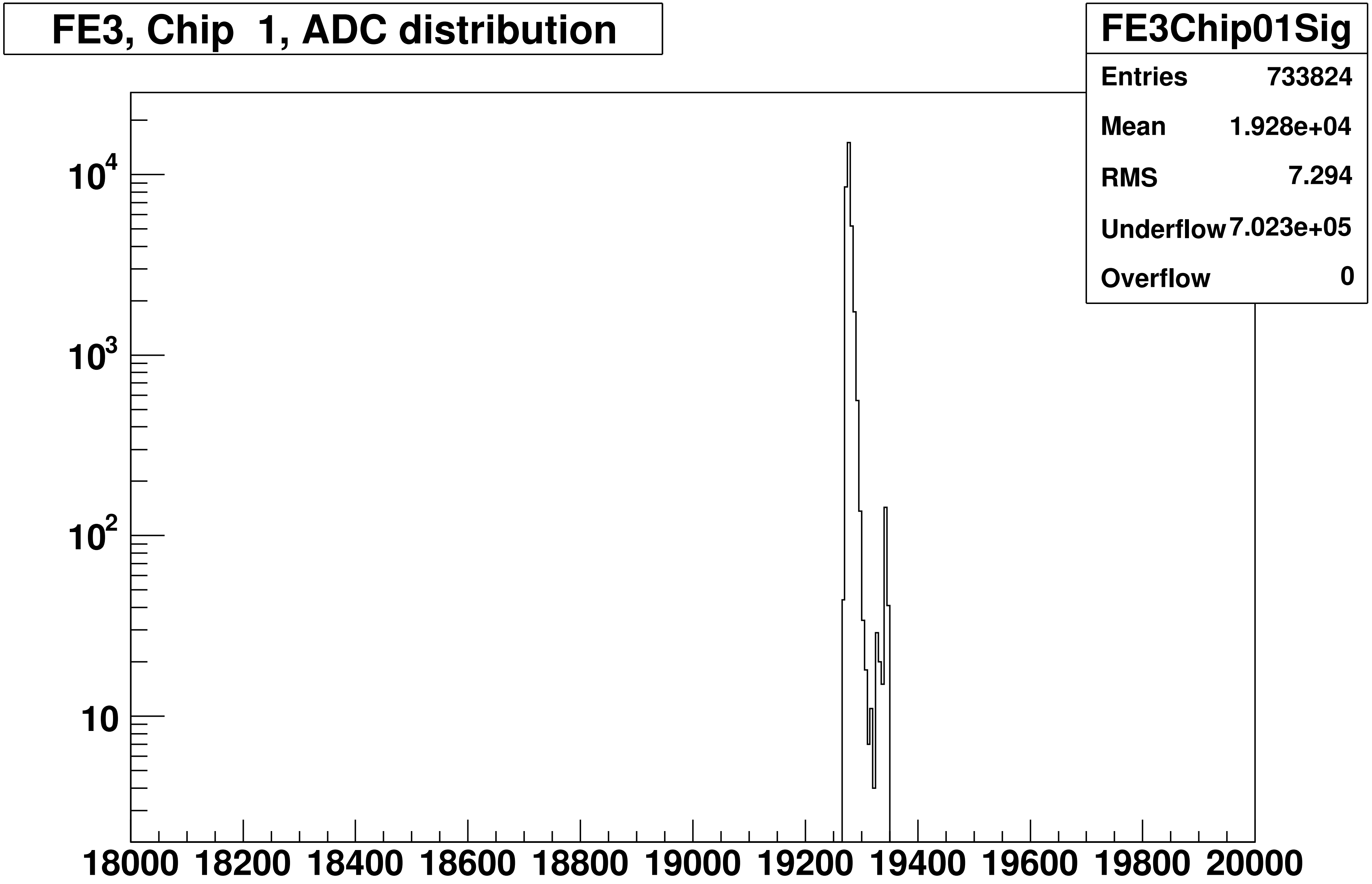
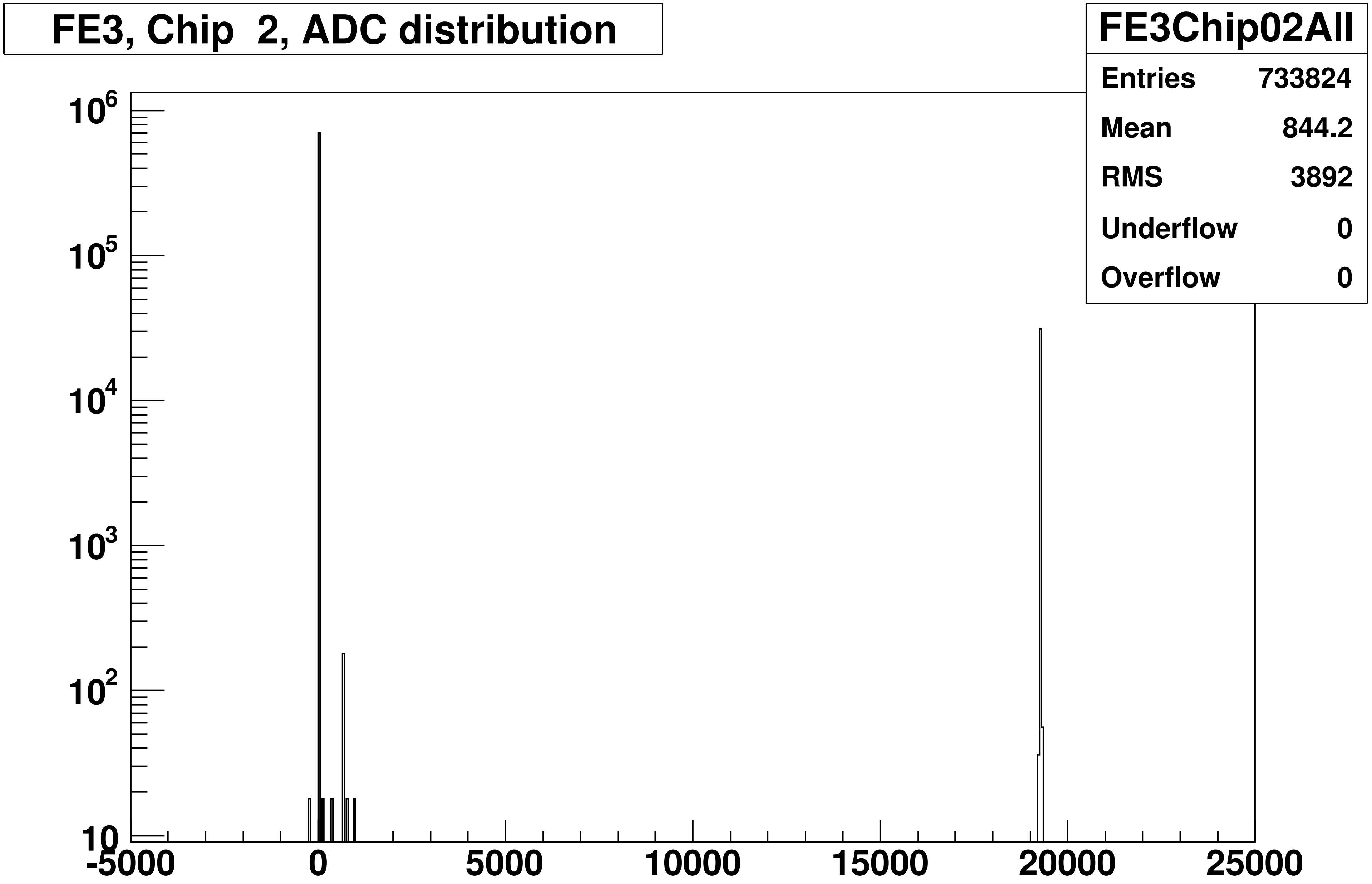
0
50
100
150
200


FE3, Chip 1, ADC distribution
FE3Chip01Sig
Entries 733824
Mean 1.928e+04
RMS 7.294
Underflow 7.023e+05
Overflow 0
10^4
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE3, Chip 2, ADC distribution
FE3Chip02All
Entries 733824
Mean 844.2
RMS 3892
Underflow 0
Overflow 0
10
10^2
10^3
10^4
10^5
10^6
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0
5000
10000
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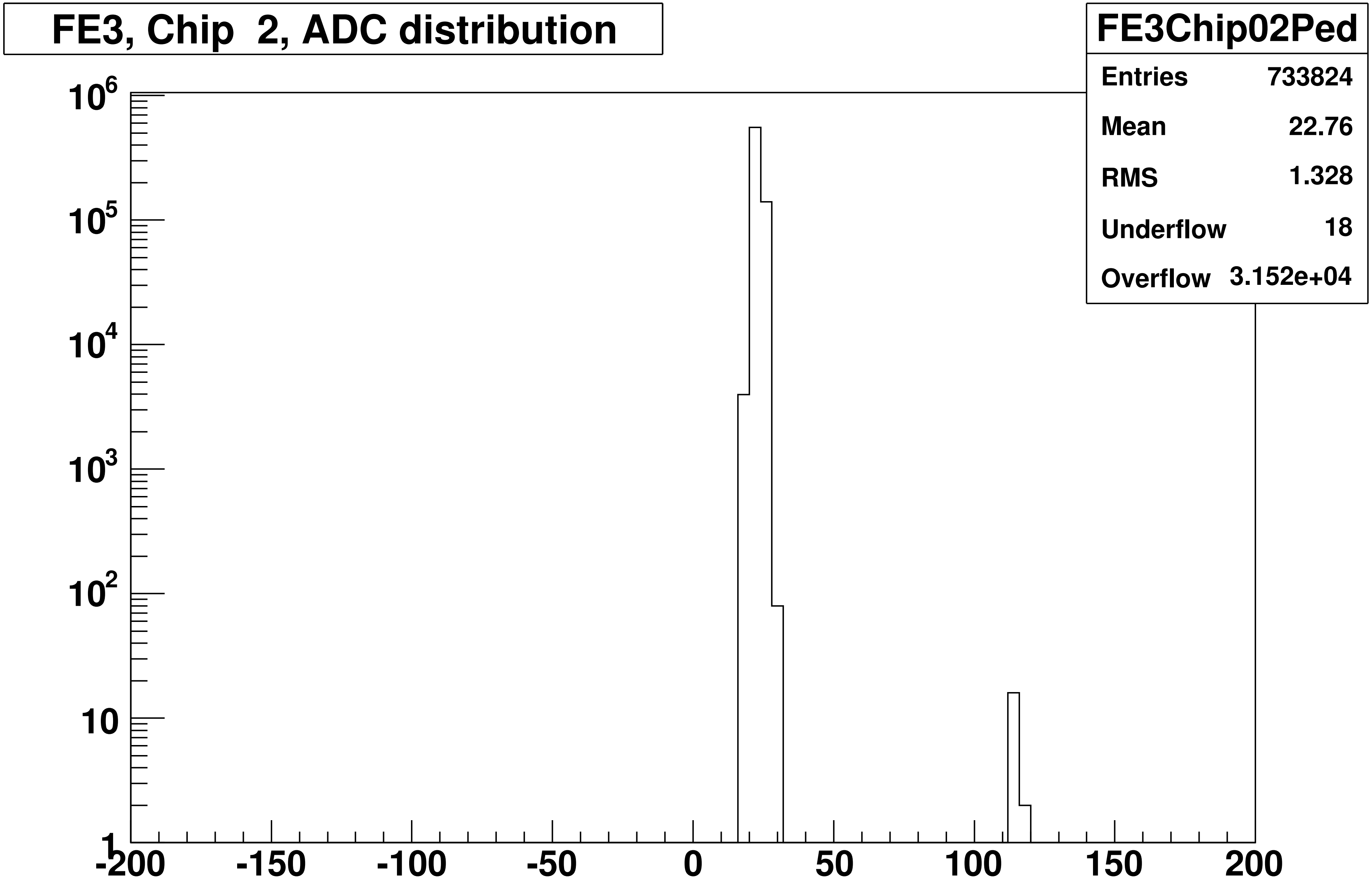
25000


FE3, Chip 2, ADC distribution
FE3Chip02Ped
Entries 733824
Mean 22.76
RMS 1.328
Underflow 18
Overflow 3.152e+04
10^6
10^5
10^4
10^3
10^2
10
1
-200
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-100
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50
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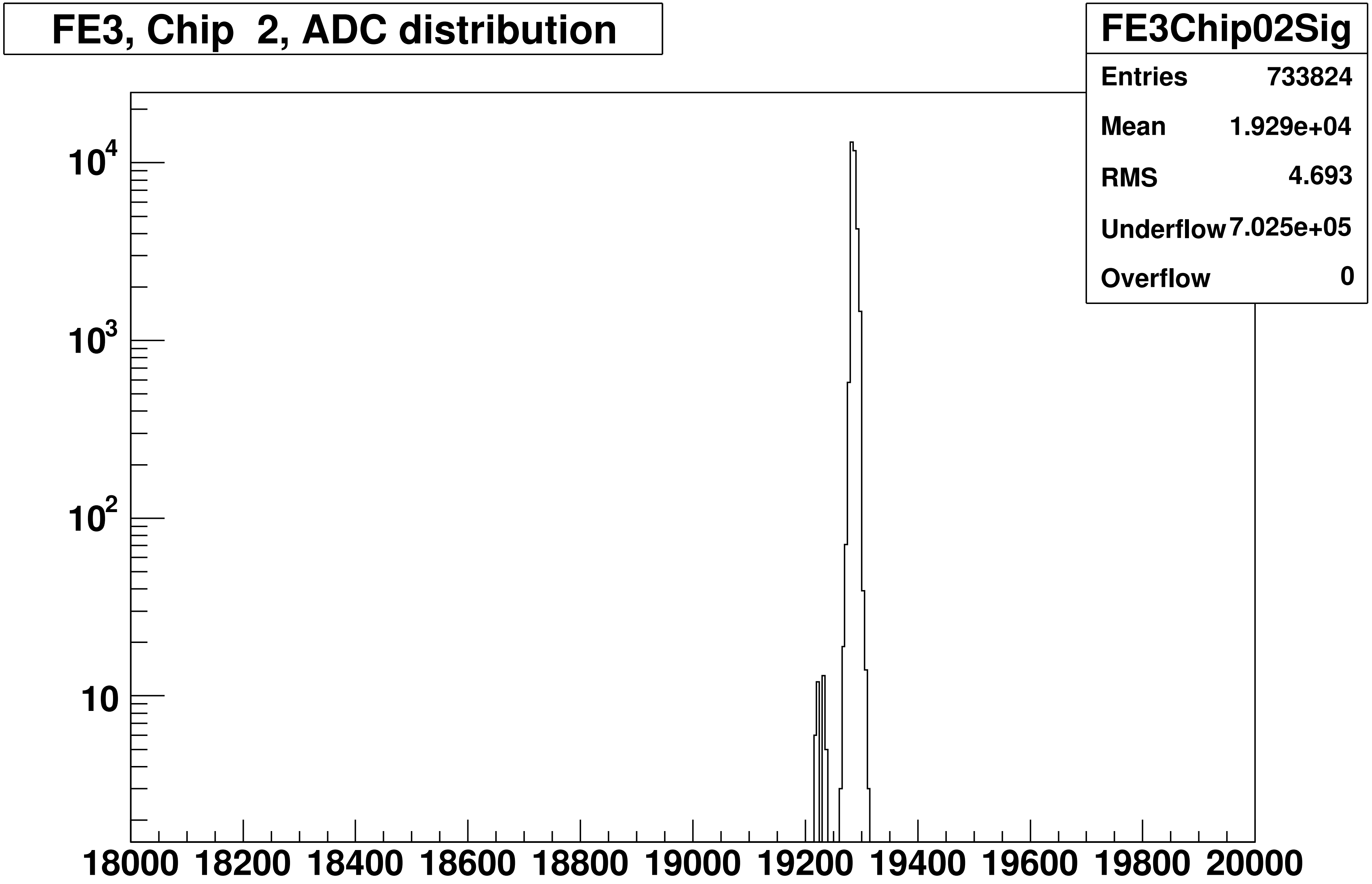
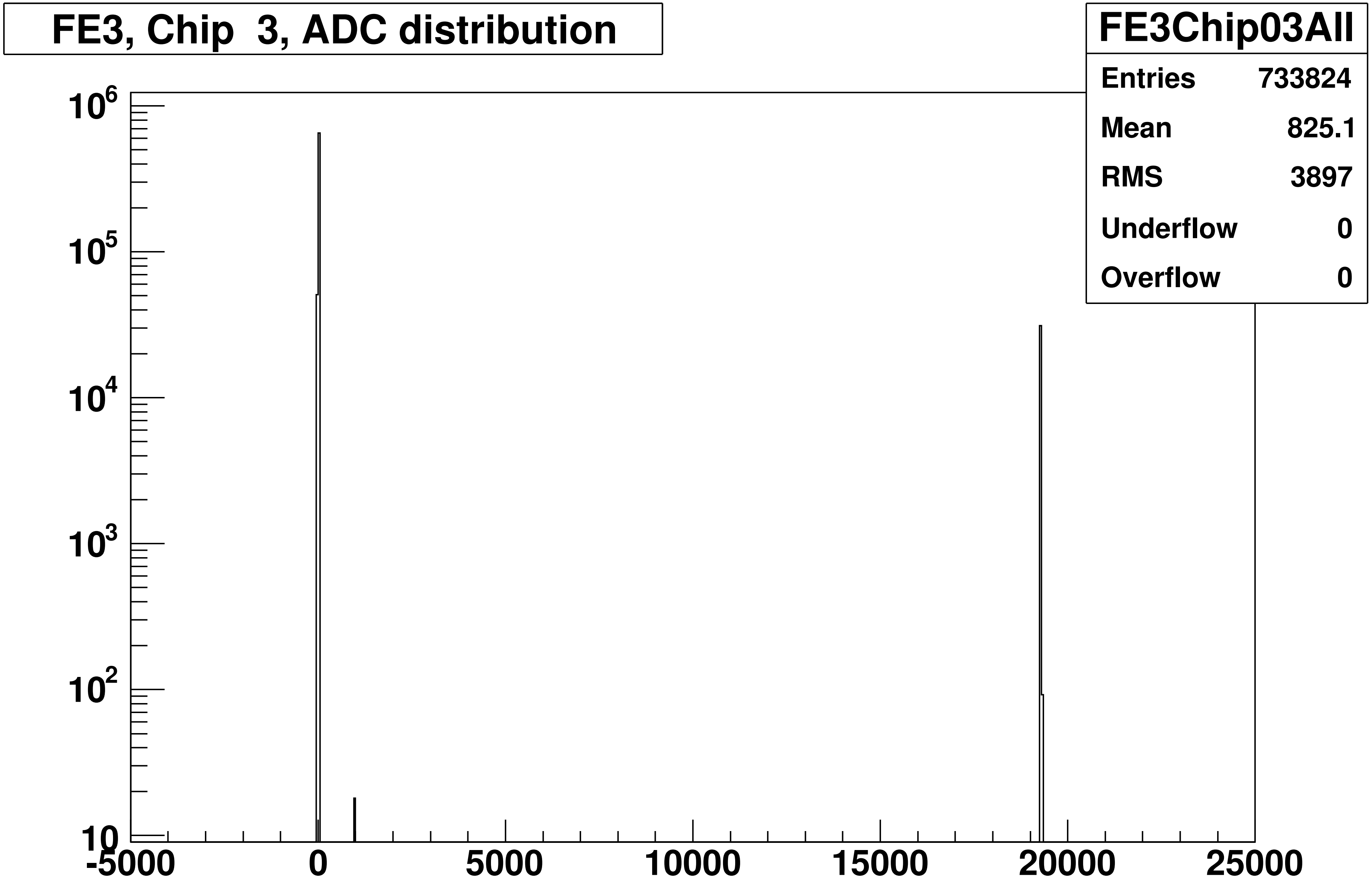
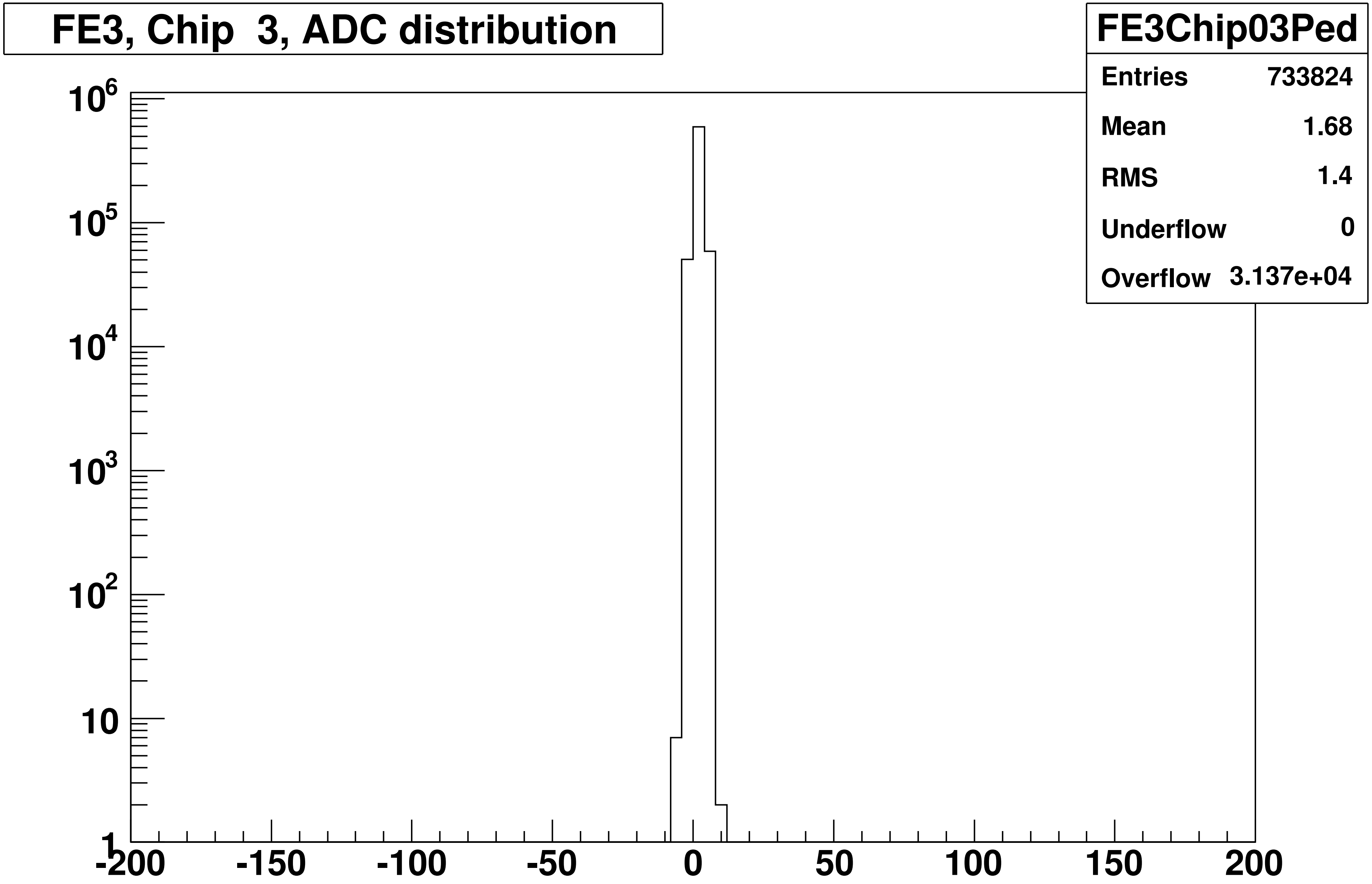
150
200



FE3, Chip 2, ADC distribution
FE3Chip02Sig
Entries 733824
Mean 1.929e+04
RMS 4.693
Underflow 7.025e+05
Overflow 0
10^4
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE3, Chip 3, ADC distribution
FE3Chip03All
Entries 733824
Mean 825.1
RMS 3897
Underflow 0
Overflow 0
10
10^2
10^3
10^4
10^5
10^6
-5000
0
5000
10000
15000
20000
25000


FE3, Chip 3, ADC distribution
FE3Chip03Ped
Entries 733824
Mean 1.68
RMS 1.4
Underflow 0
Overflow 3.137e+04
10^6
10^5
10^4
10^3
10^2
10
1
-200
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100
150
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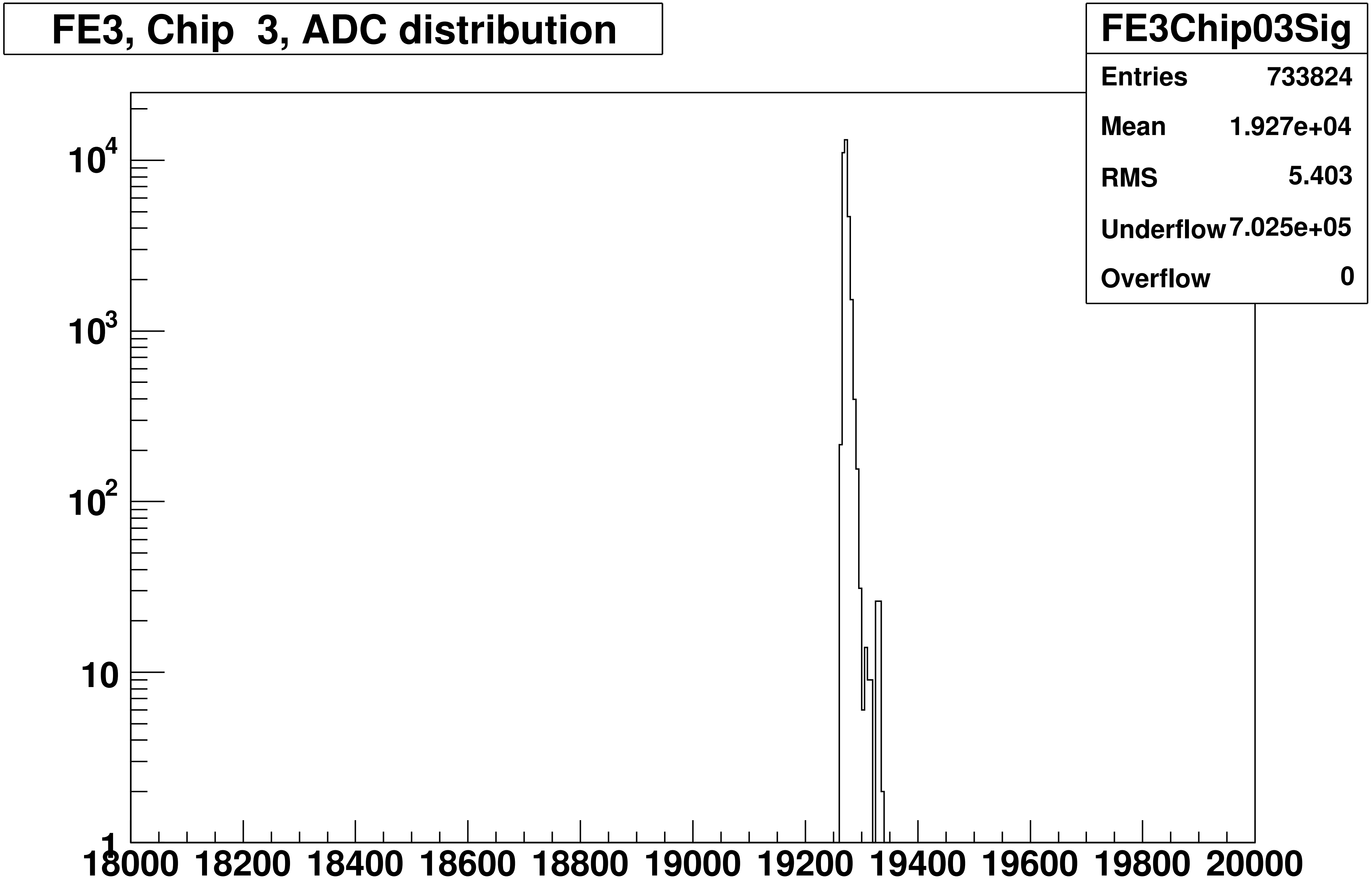
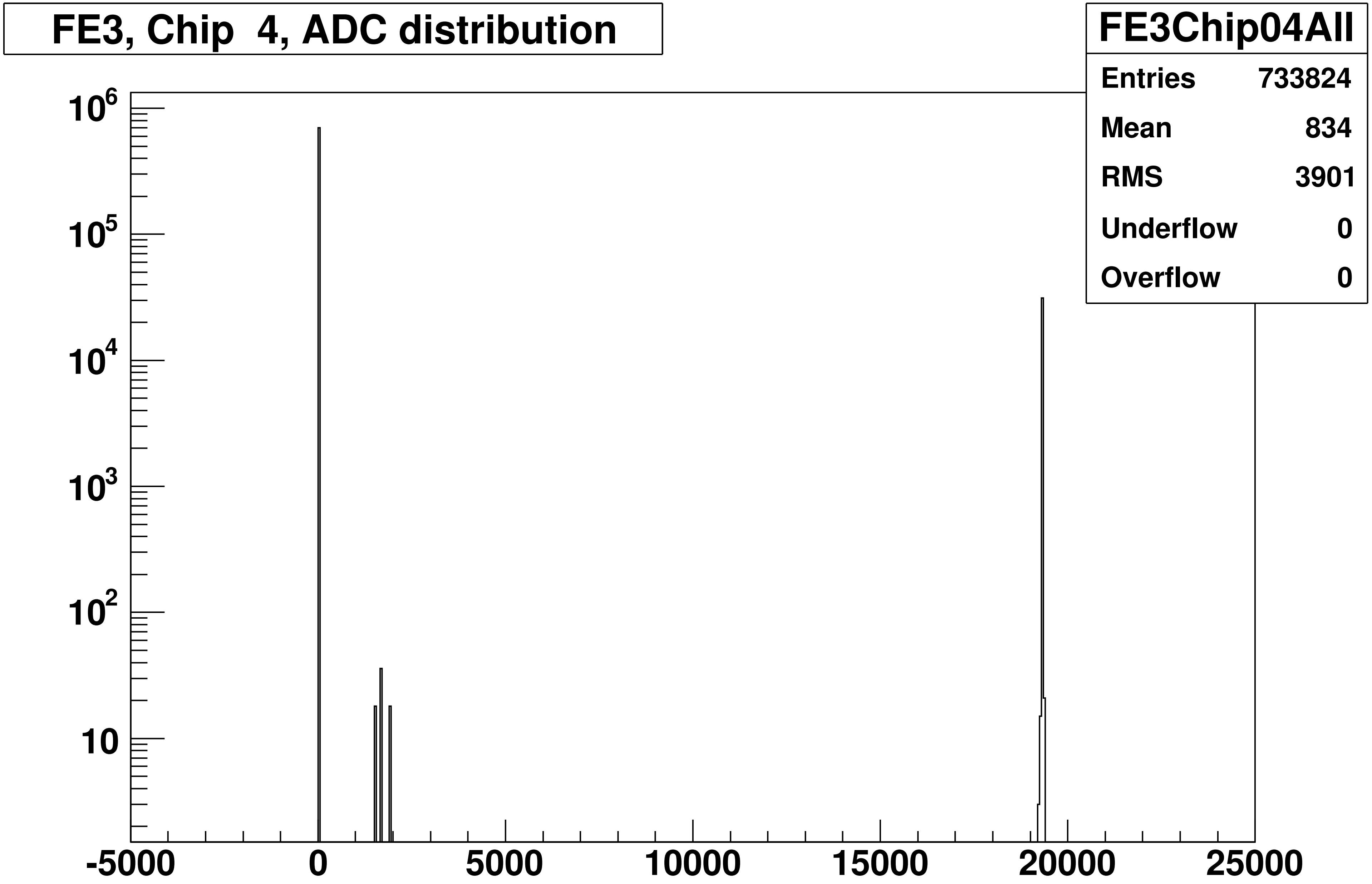


FE3, Chip 3, ADC distribution
FE3Chip03Sig
Entries 733824
Mean 1.927e+04
RMS 5.403
Underflow 7.025e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE3, Chip 4, ADC distribution
FE3Chip04All
Entries 733824
Mean 834
RMS 3901
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
-5000
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20000
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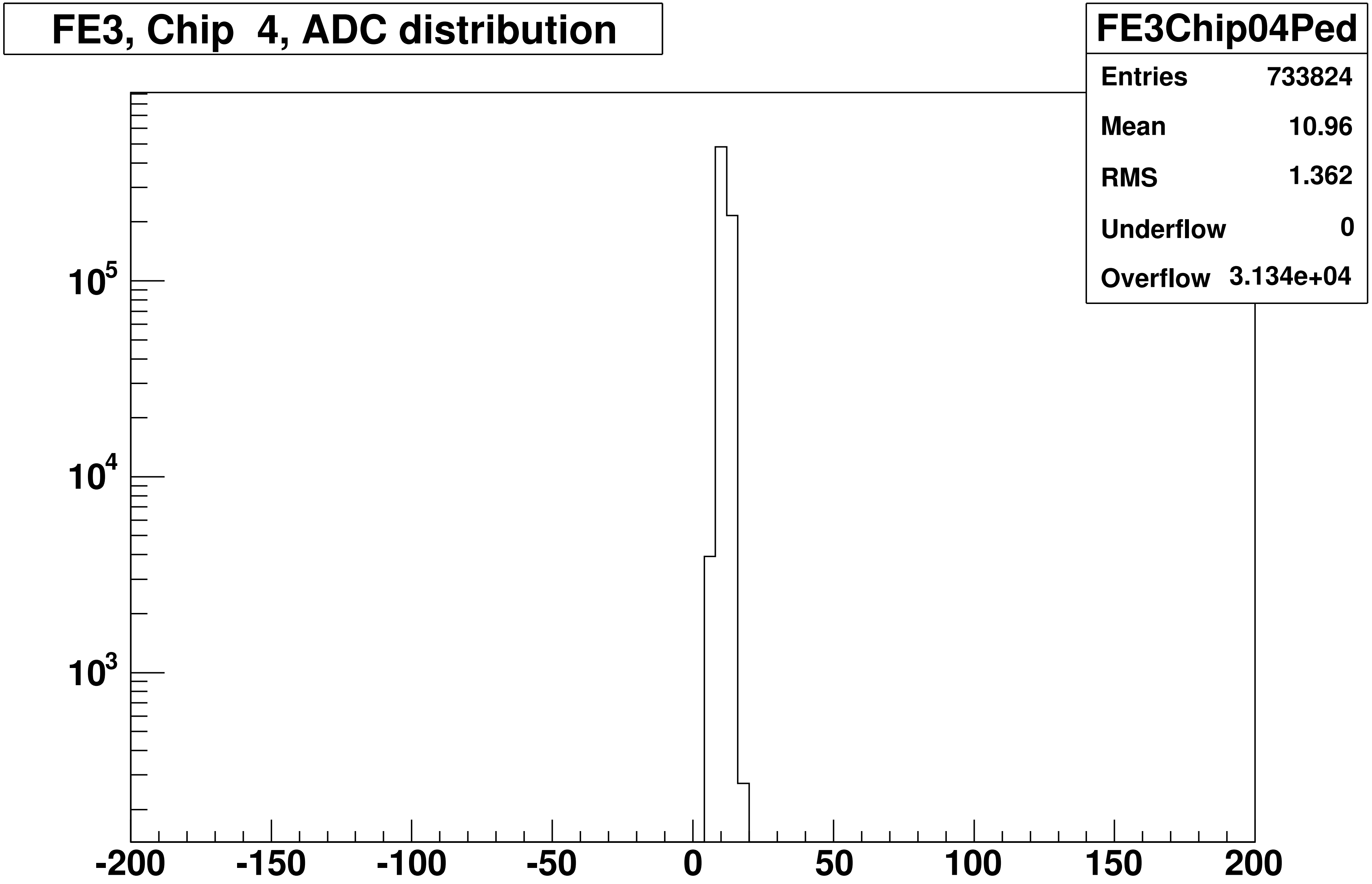

FE3, Chip 4, ADC distribution
FE3Chip04Ped
Entries 733824
Mean 10.96
RMS 1.362
Underflow 0
Overflow 3.134e+04
10^5
10^4
10^3
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-100
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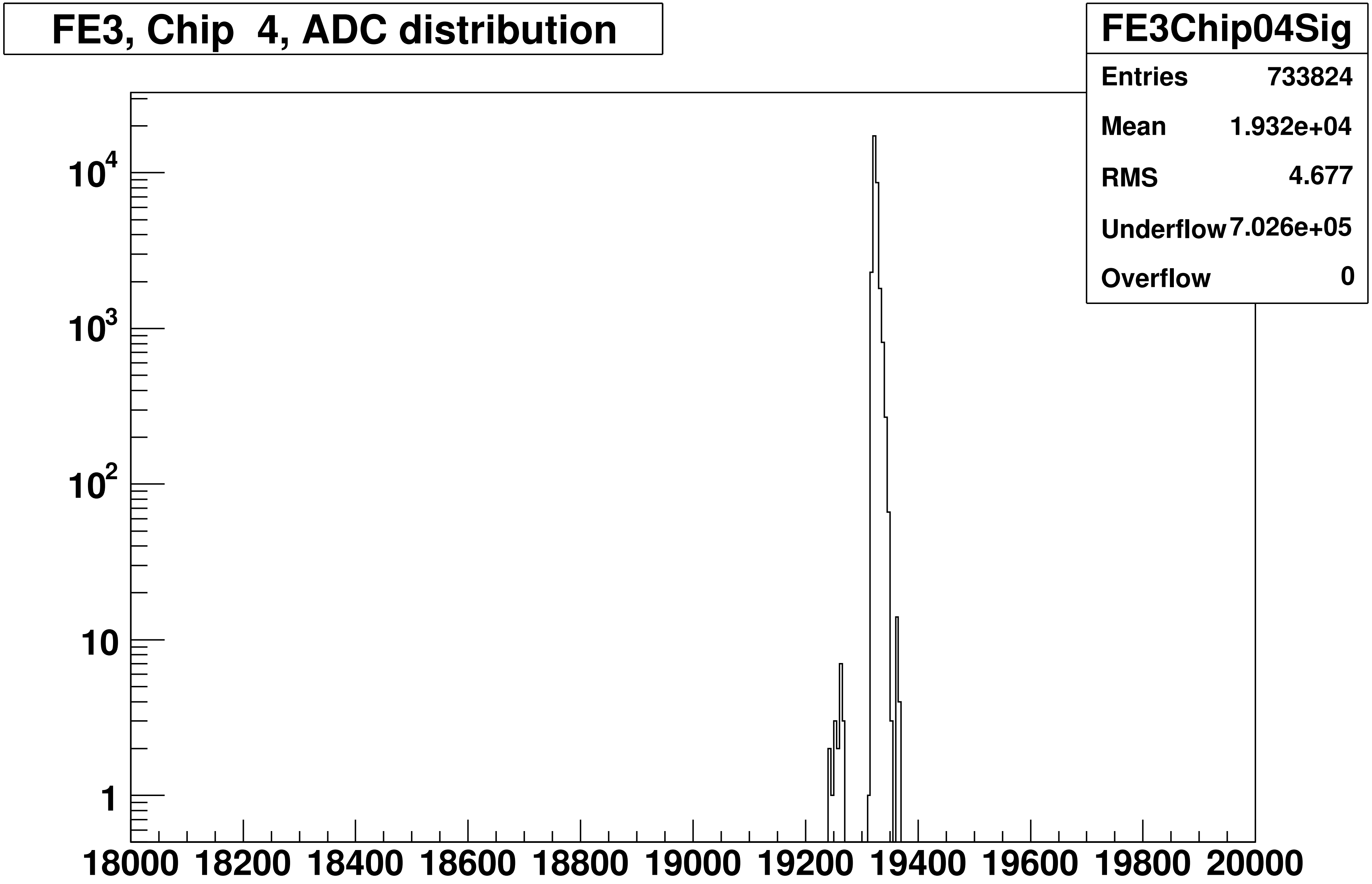
FE3, Chip 4, ADC distribution
FE3Chip04Sig
Entries 733824
Mean 1.932e+04
RMS 4.677
Underflow 7.026e+05
Overflow 0
10^4
10^3
10^2
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1
18000
18200
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18600
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19800
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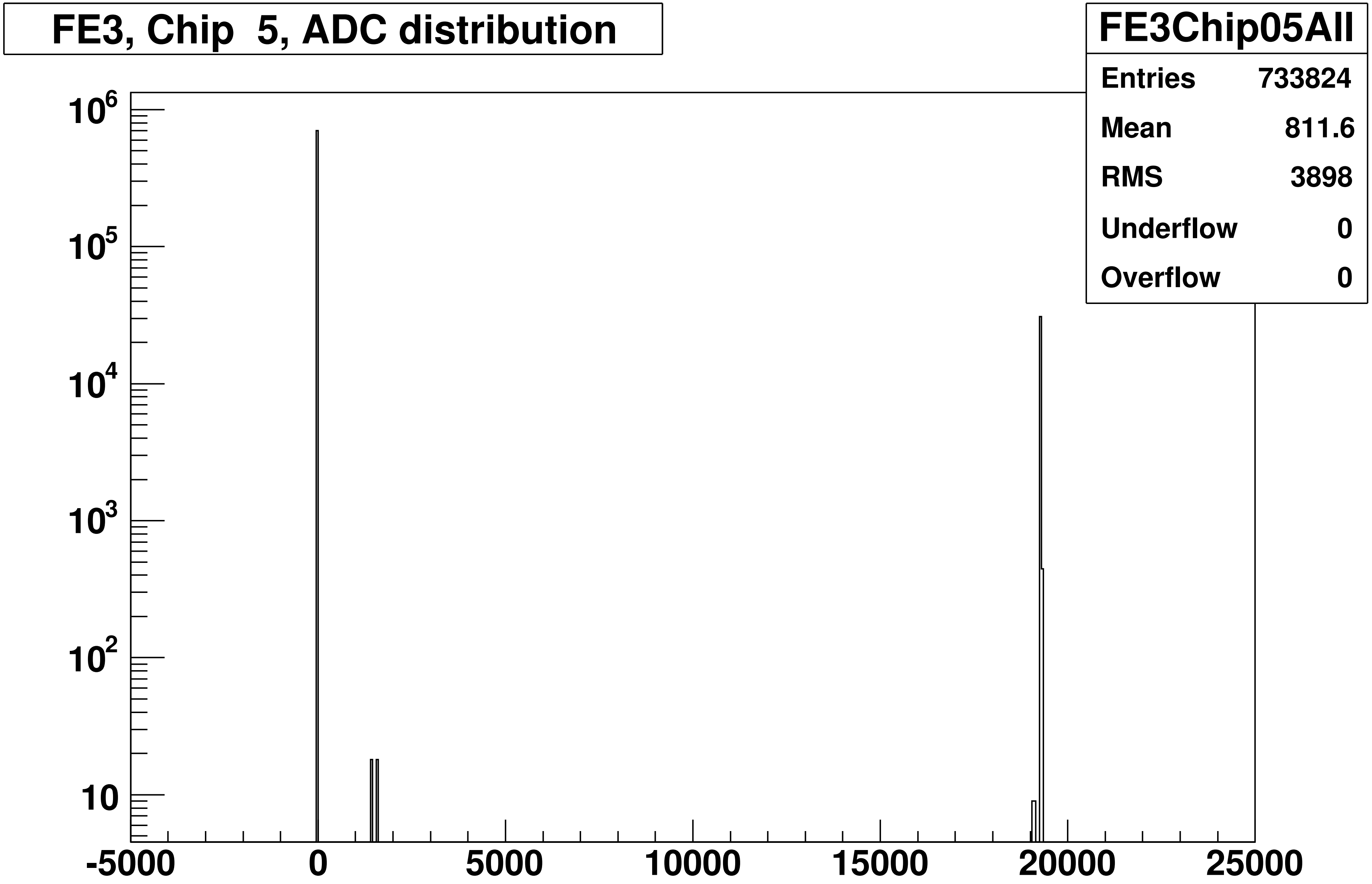

FE3, Chip 5, ADC distribution
FE3Chip05All
Entries 733824
Mean 811.6
RMS 3898
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
-5000
0
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10000
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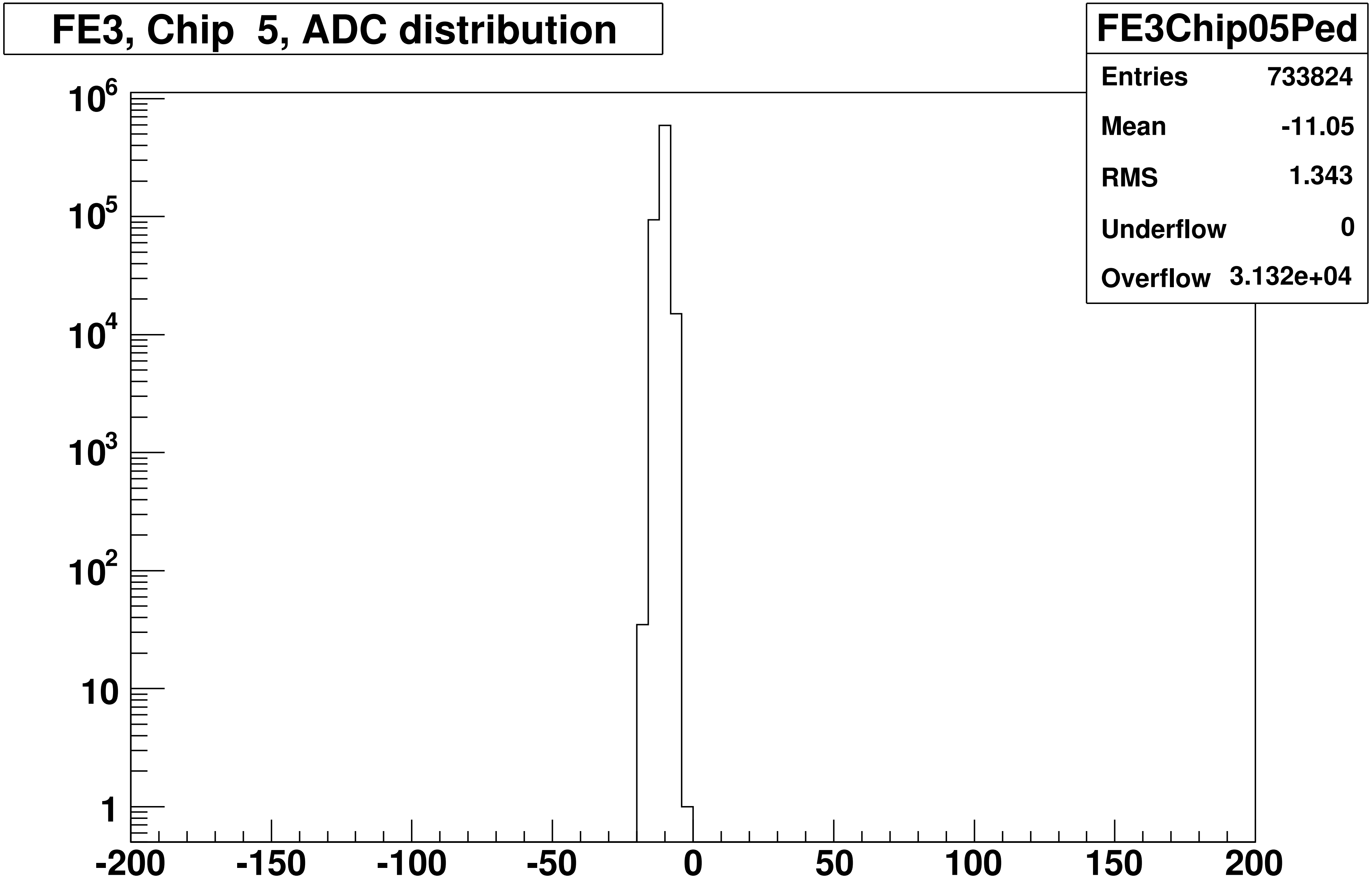
20000
25000



FE3, Chip 5, ADC distribution
FE3Chip05Ped
Entries 733824
Mean -11.05
RMS 1.343
Underflow 0
Overflow 3.132e+04
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10^5
10^4
10^3
10^2
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100
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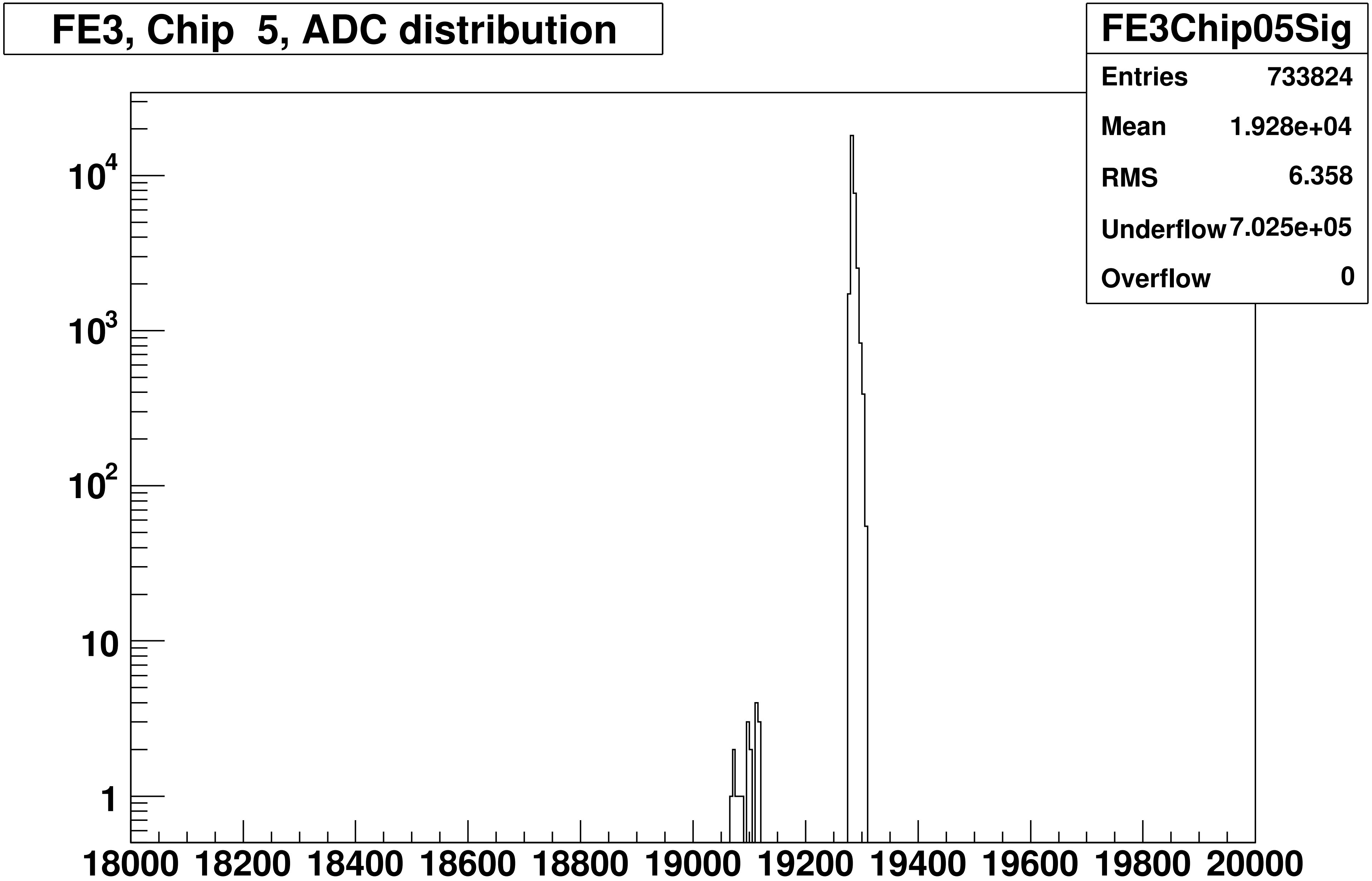

FE3, Chip 5, ADC distribution
FE3Chip05Sig
Entries 733824
Mean 1.928e+04
RMS 6.358
Underflow 7.025e+05
Overflow 0
10^4
10^3
10^2
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1
18000
18200
18400
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19000
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19800
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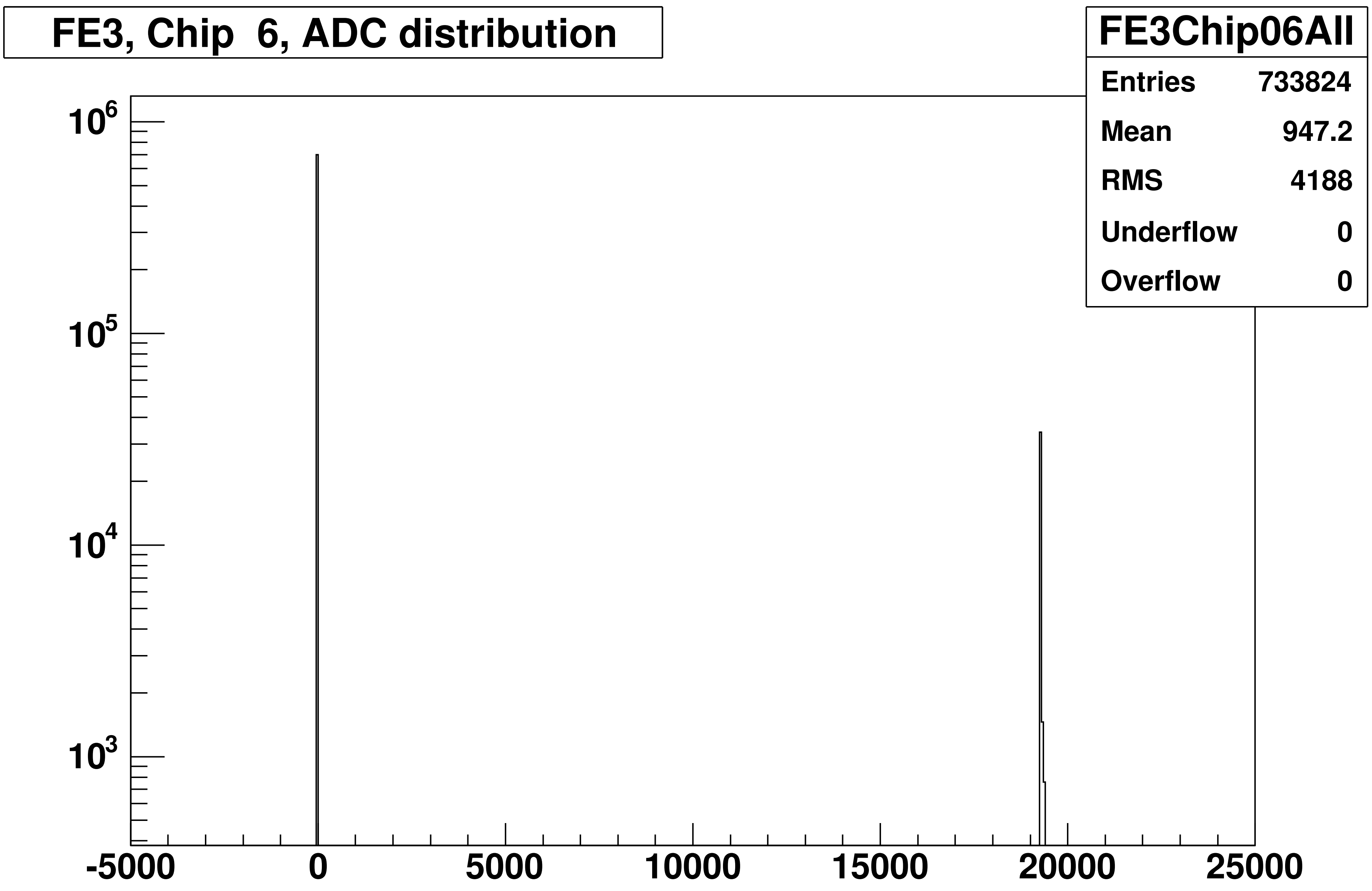
FE3, Chip 6, ADC distribution
FE3Chip06All
Entries 733824
Mean 947.2
RMS 4188
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
-5000
0
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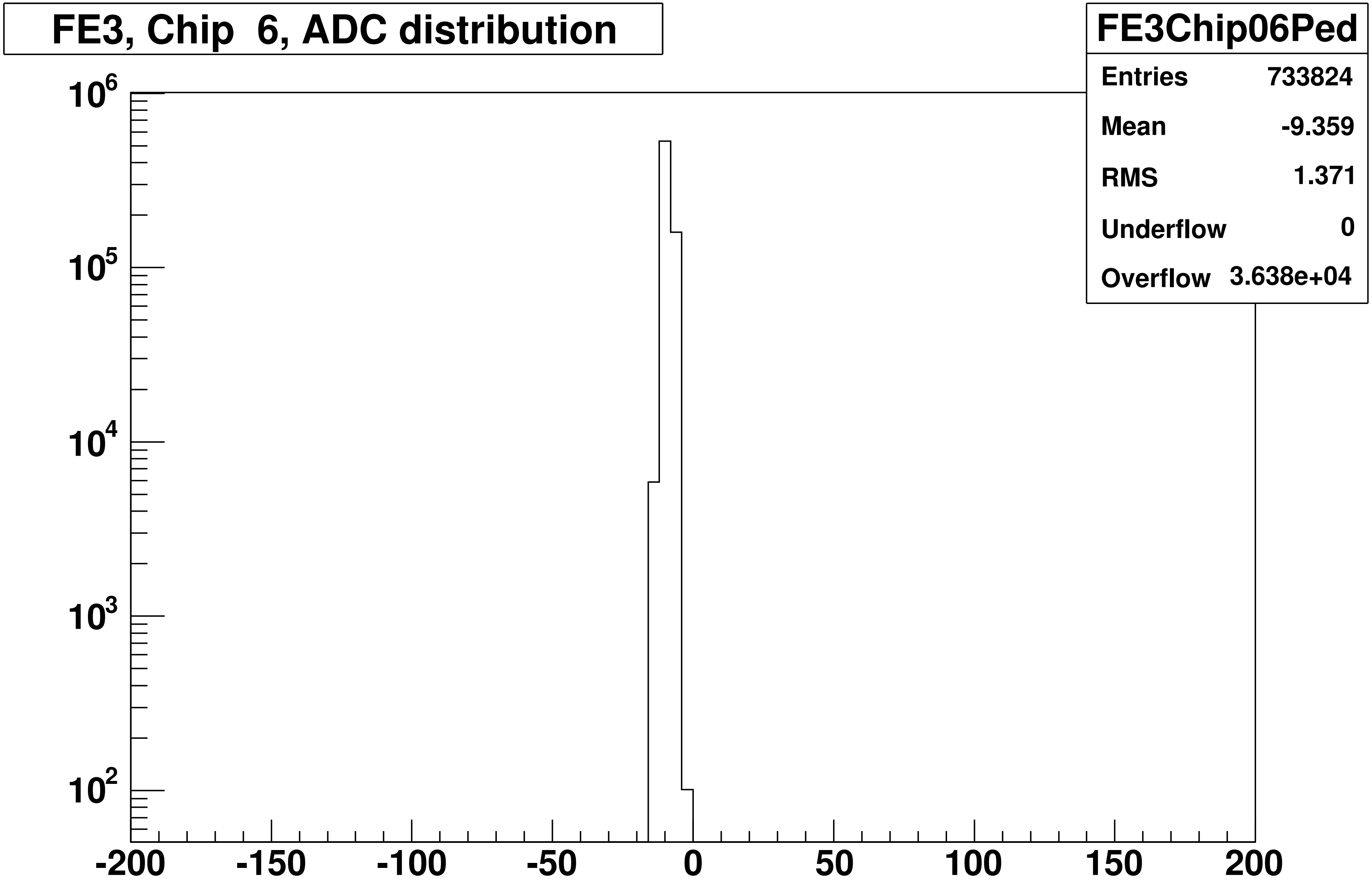
10000
15000
20000
25000



FE3, Chip 6, ADC distribution
FE3Chip06Ped
Entries 733824
Mean -9.359
RMS 1.371
Underflow 0
Overflow 3.638e+04
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10^5
10^4
10^3
10^2
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0
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100
150
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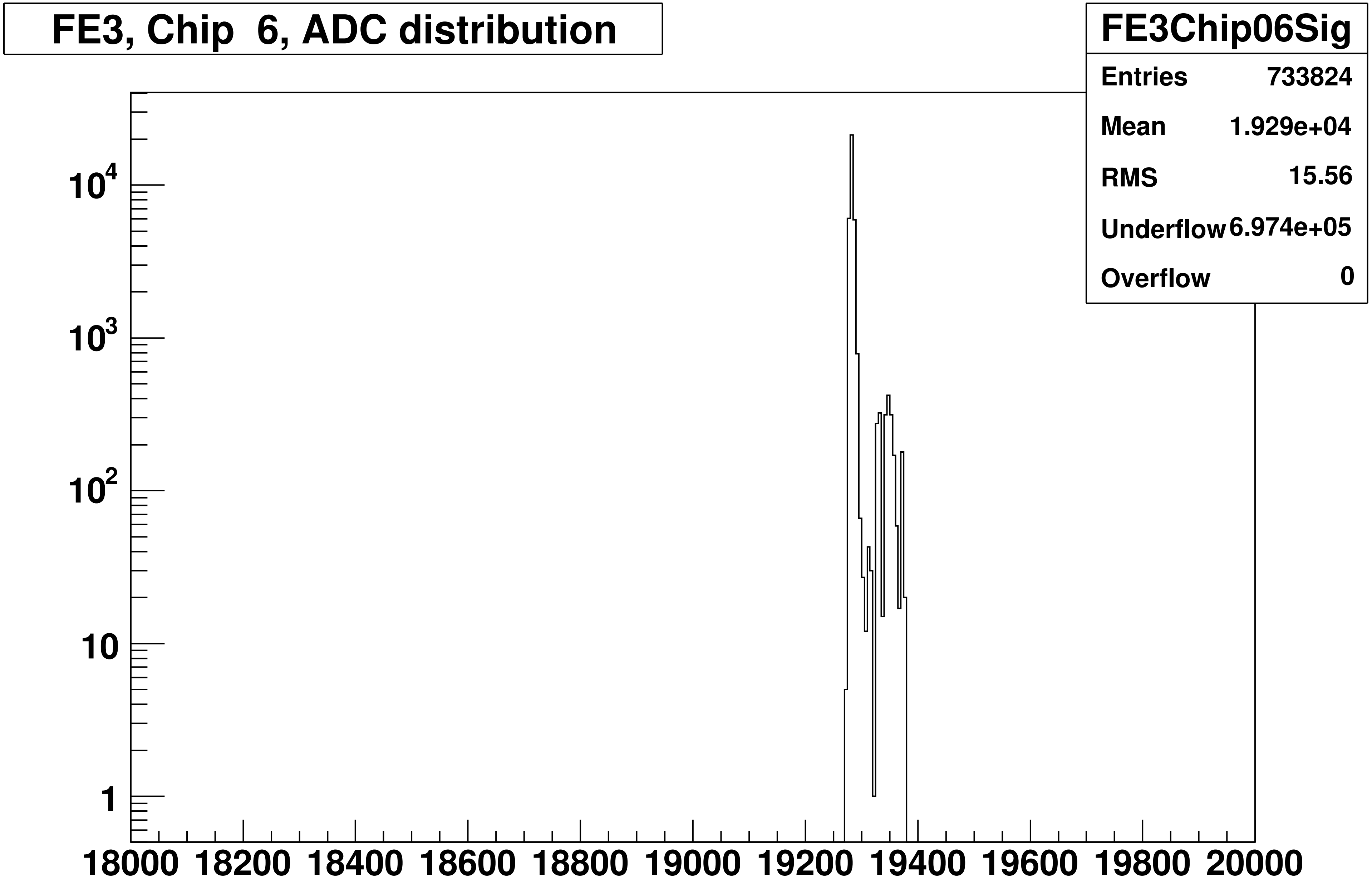
FE3, Chip 6, ADC distribution
FE3Chip06Sig
Entries 733824
Mean 1.929e+04
RMS 15.56
Underflow 6.974e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
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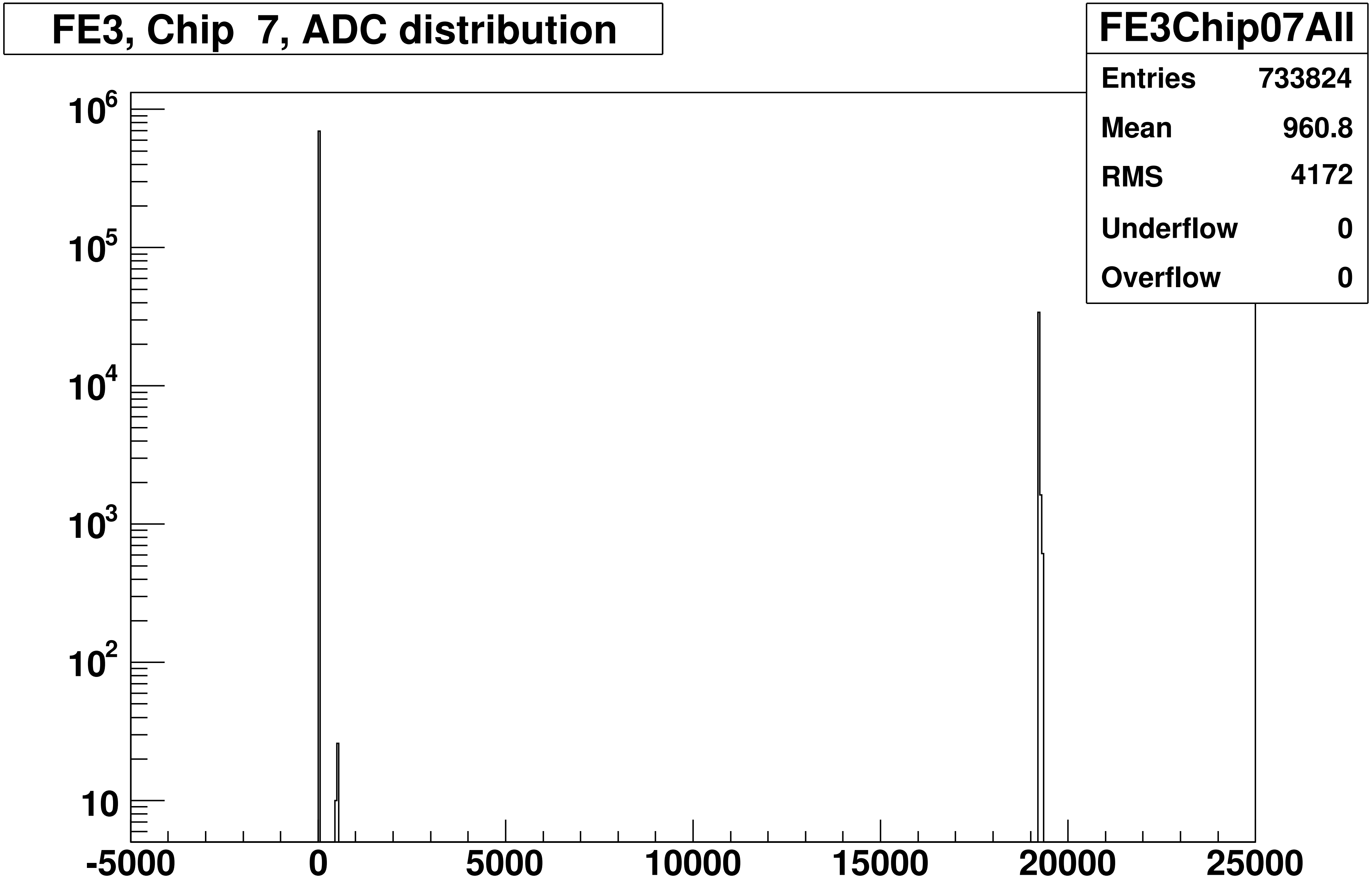
19600
19800
20000


FE3, Chip 7, ADC distribution
FE3Chip07All
Entries 733824
Mean 960.8
RMS 4172
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
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-5000
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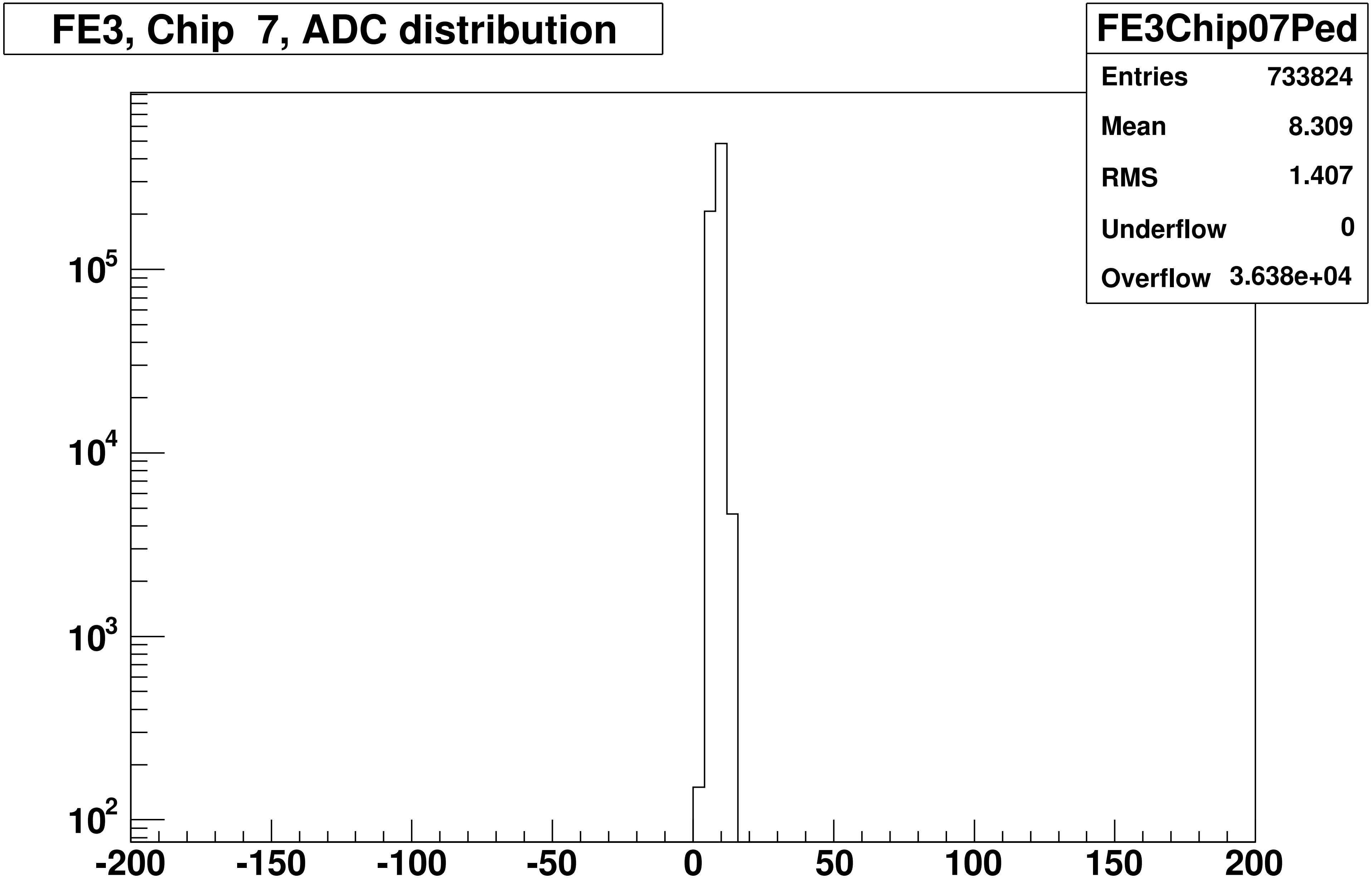

FE3, Chip 7, ADC distribution
FE3Chip07Ped
Entries 733824
Mean 8.309
RMS 1.407
Underflow 0
Overflow 3.638e+04
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10^4
10^3
10^2
-200
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-100
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0
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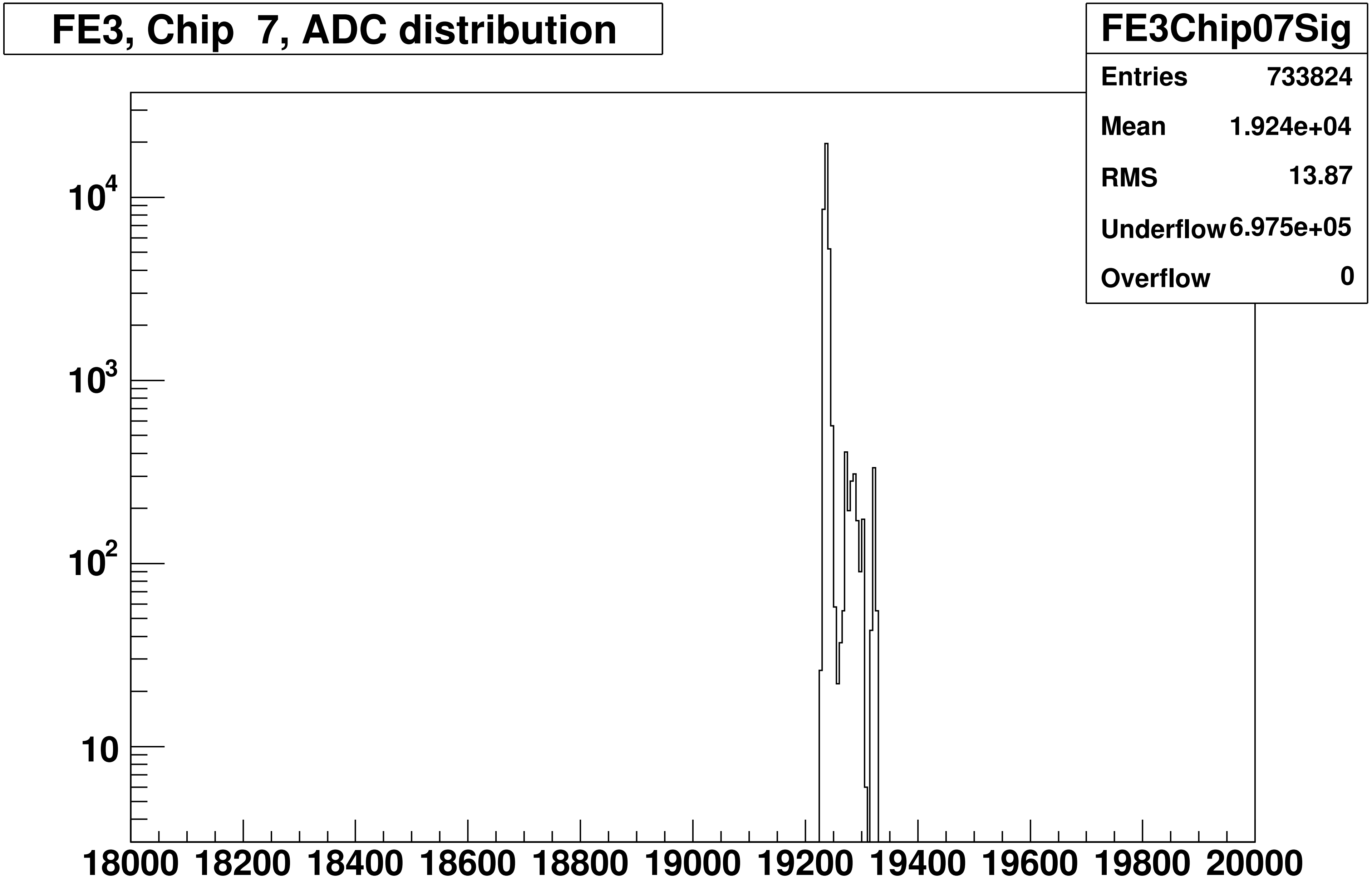
100
150
200



FE3, Chip 7, ADC distribution
FE3Chip07Sig
Entries 733824
Mean 1.924e+04
RMS 13.87
Underflow 6.975e+05
Overflow 0
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10^3
10^2
10
18000
18200
18400
18600
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19000
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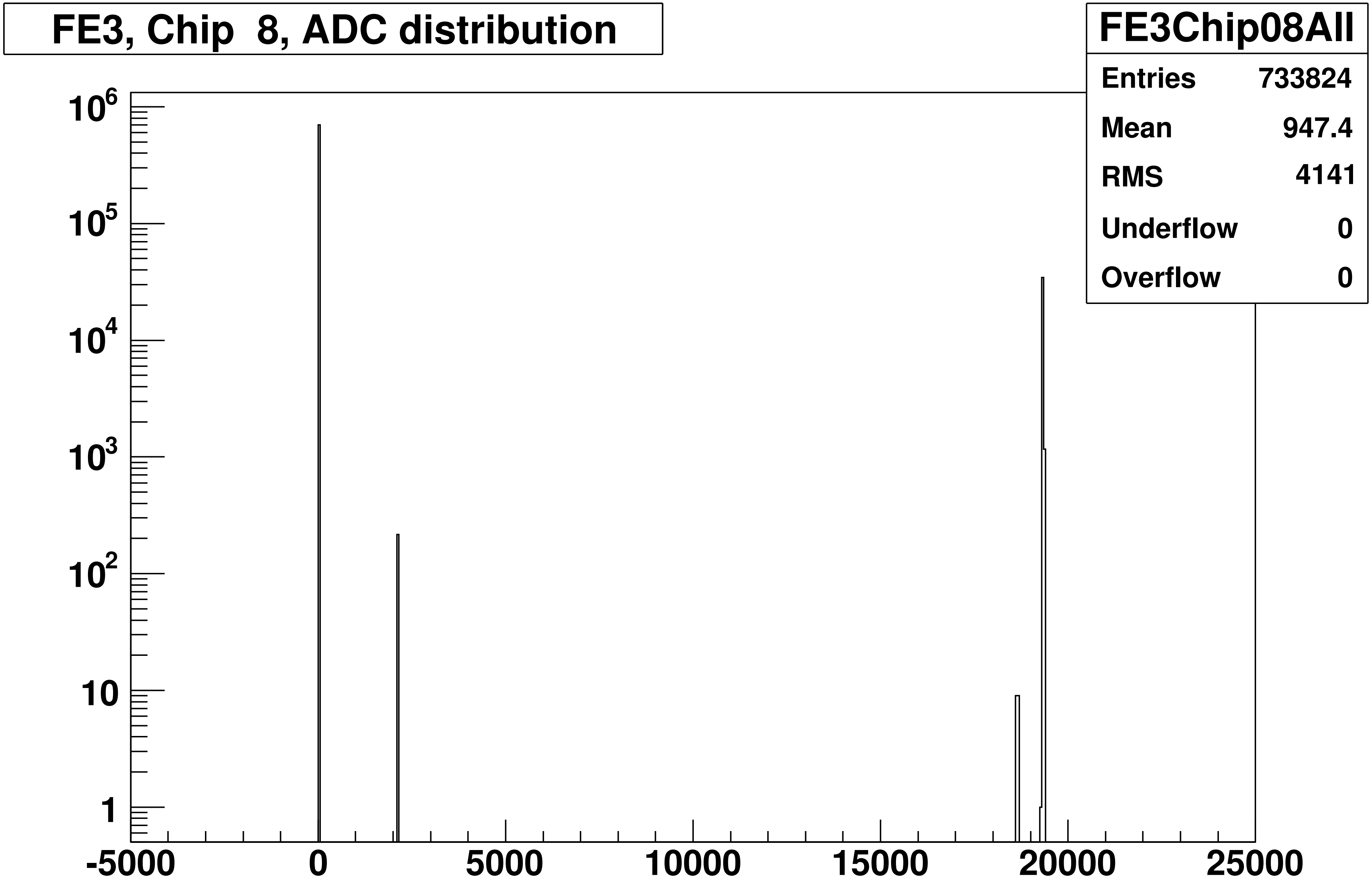

FE3, Chip 8, ADC distribution
FE3Chip08All
Entries 733824
Mean 947.4
RMS 4141
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
1
-5000
0
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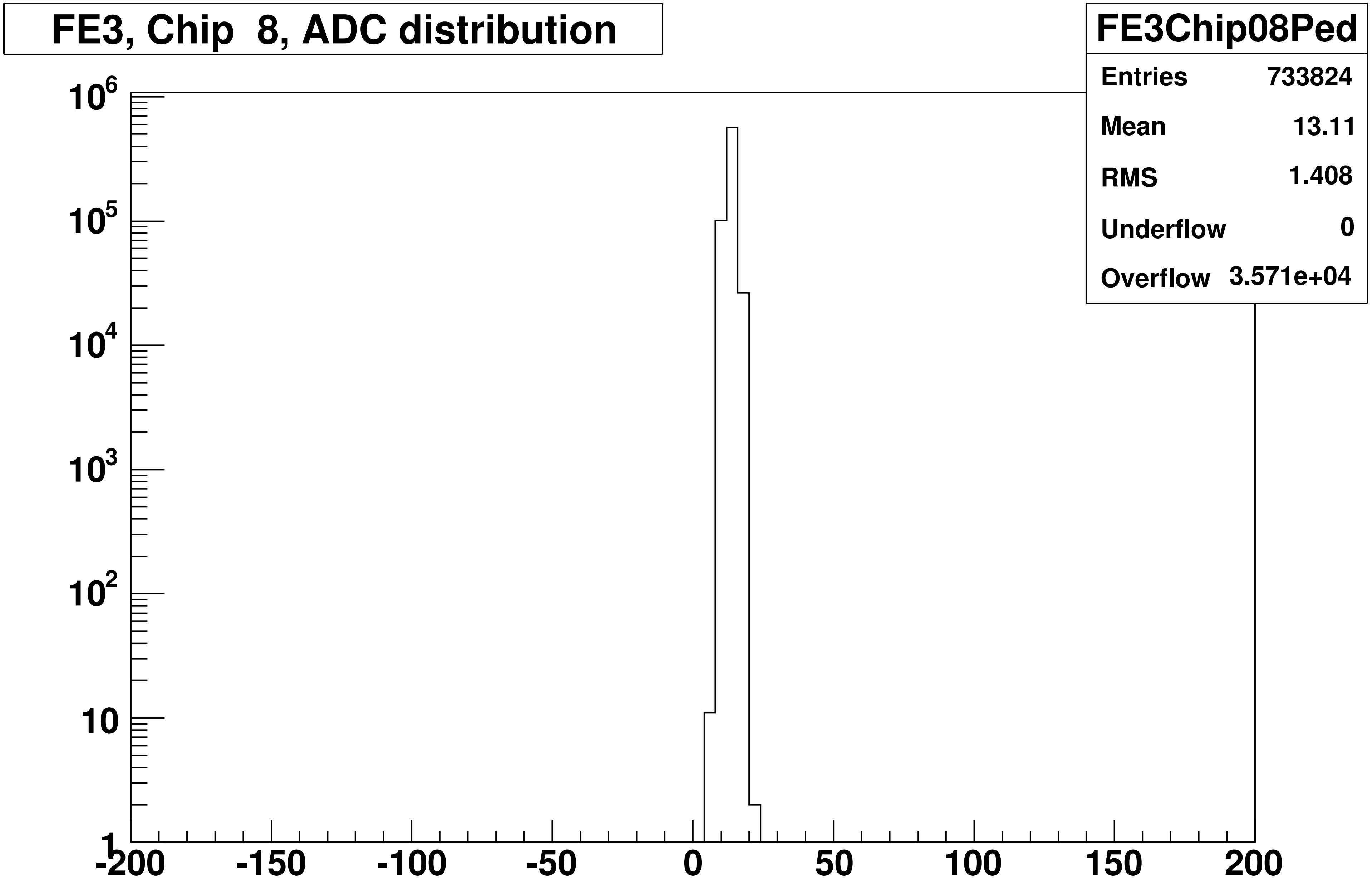
10000
15000
20000
25000



FE3, Chip 8, ADC distribution
FE3Chip08Ped
Entries 733824
Mean 13.11
RMS 1.408
Underflow 0
Overflow 3.571e+04
10^6
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
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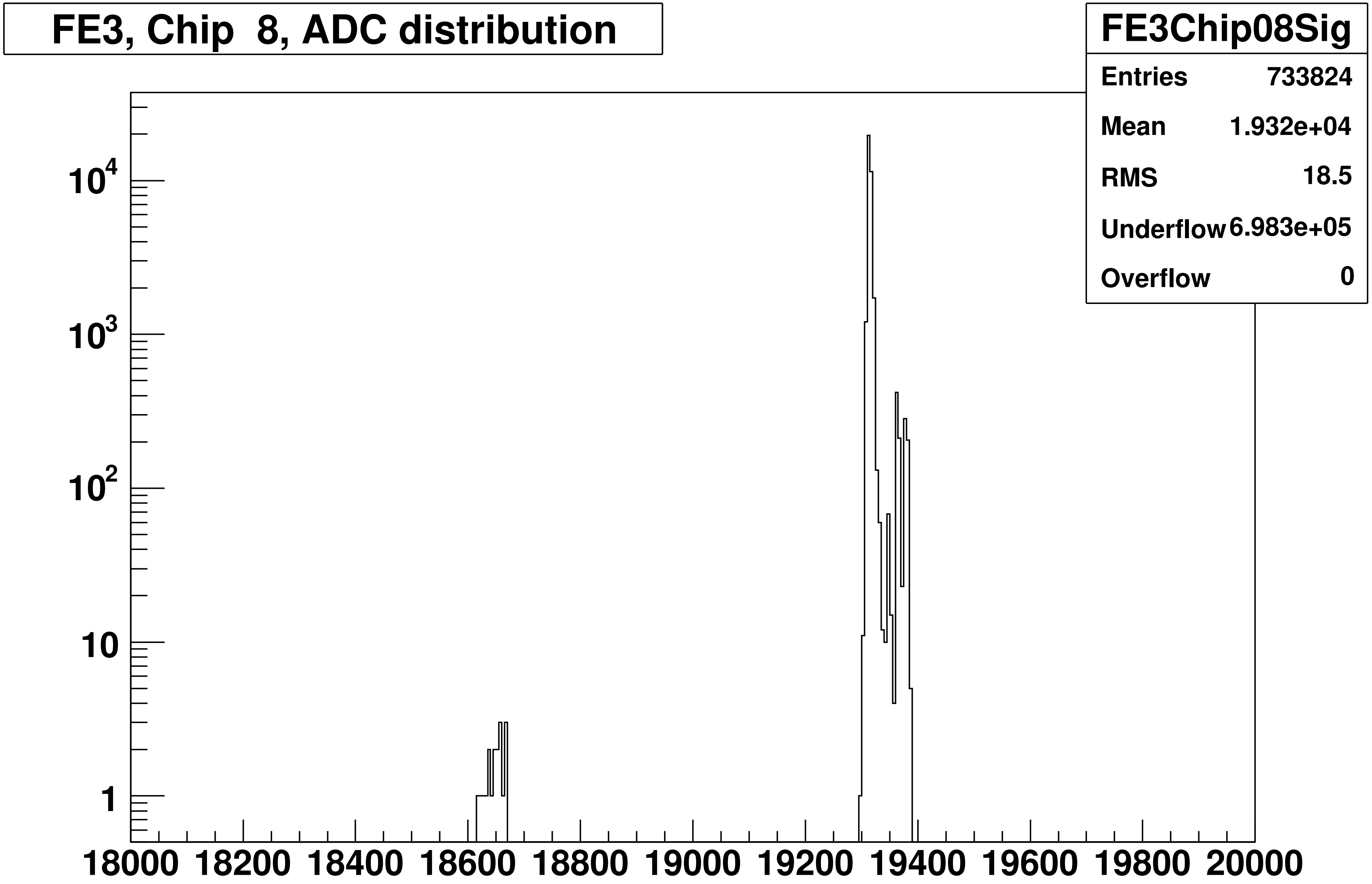
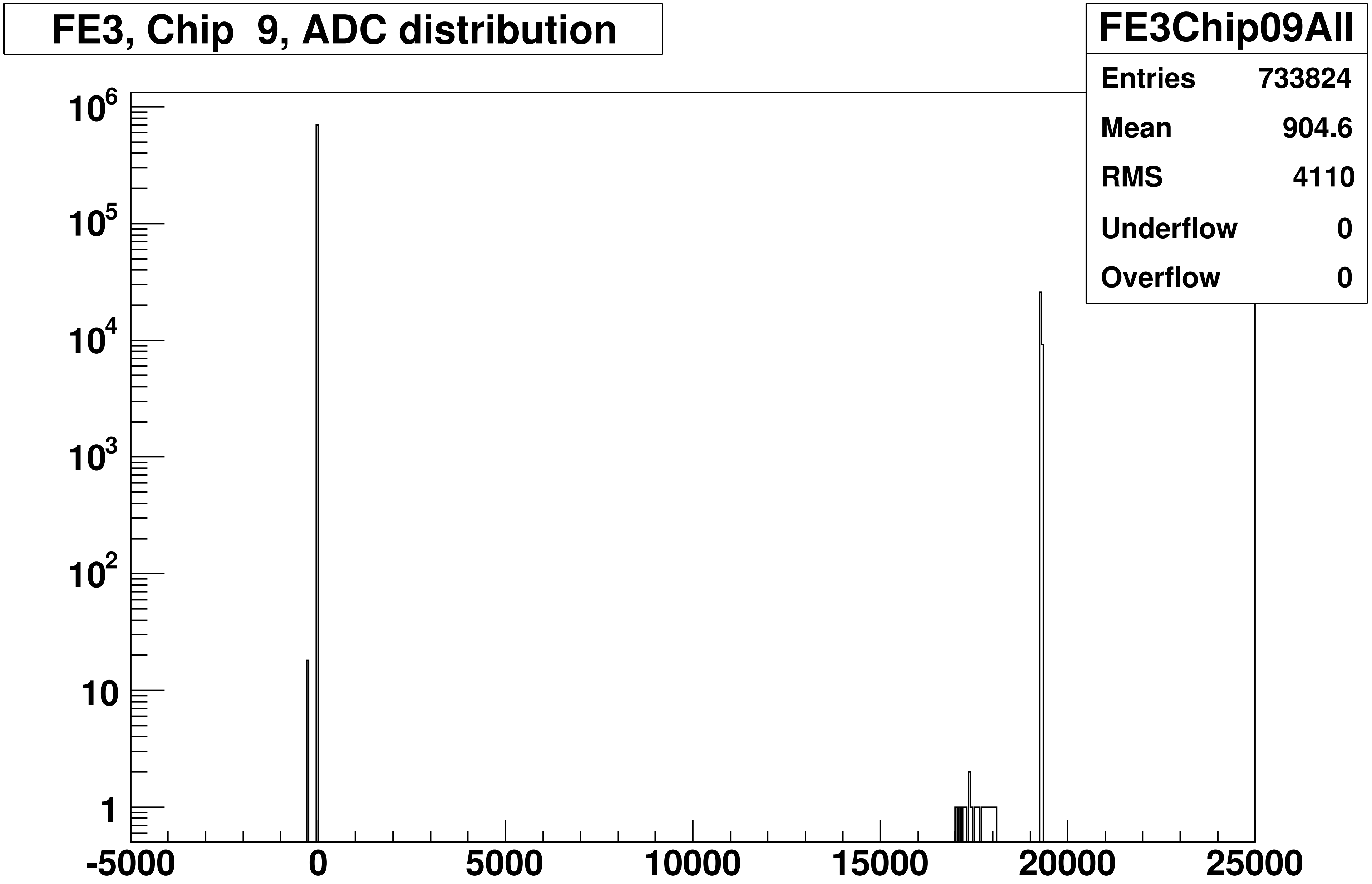
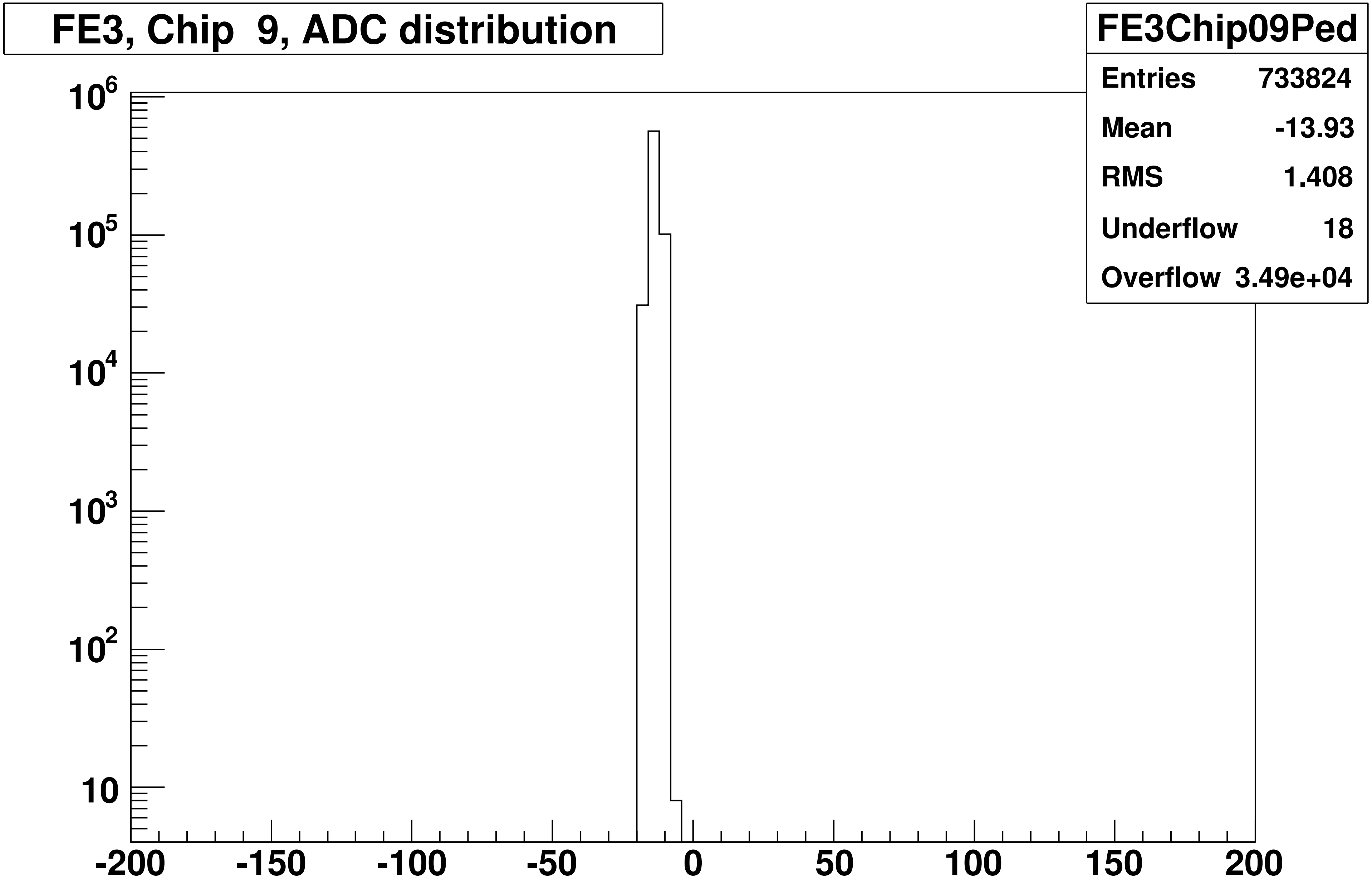
0
50
100
150
200



FE3, Chip 8, ADC distribution
FE3Chip08Sig
Entries 733824
Mean 1.932e+04
RMS 18.5
Underflow 6.983e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE3, Chip 9, ADC distribution
FE3Chip09All
Entries 733824
Mean 904.6
RMS 4110
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE3, Chip 9, ADC distribution
FE3Chip09Ped
Entries 733824
Mean -13.93
RMS 1.408
Underflow 18
Overflow 3.49e+04
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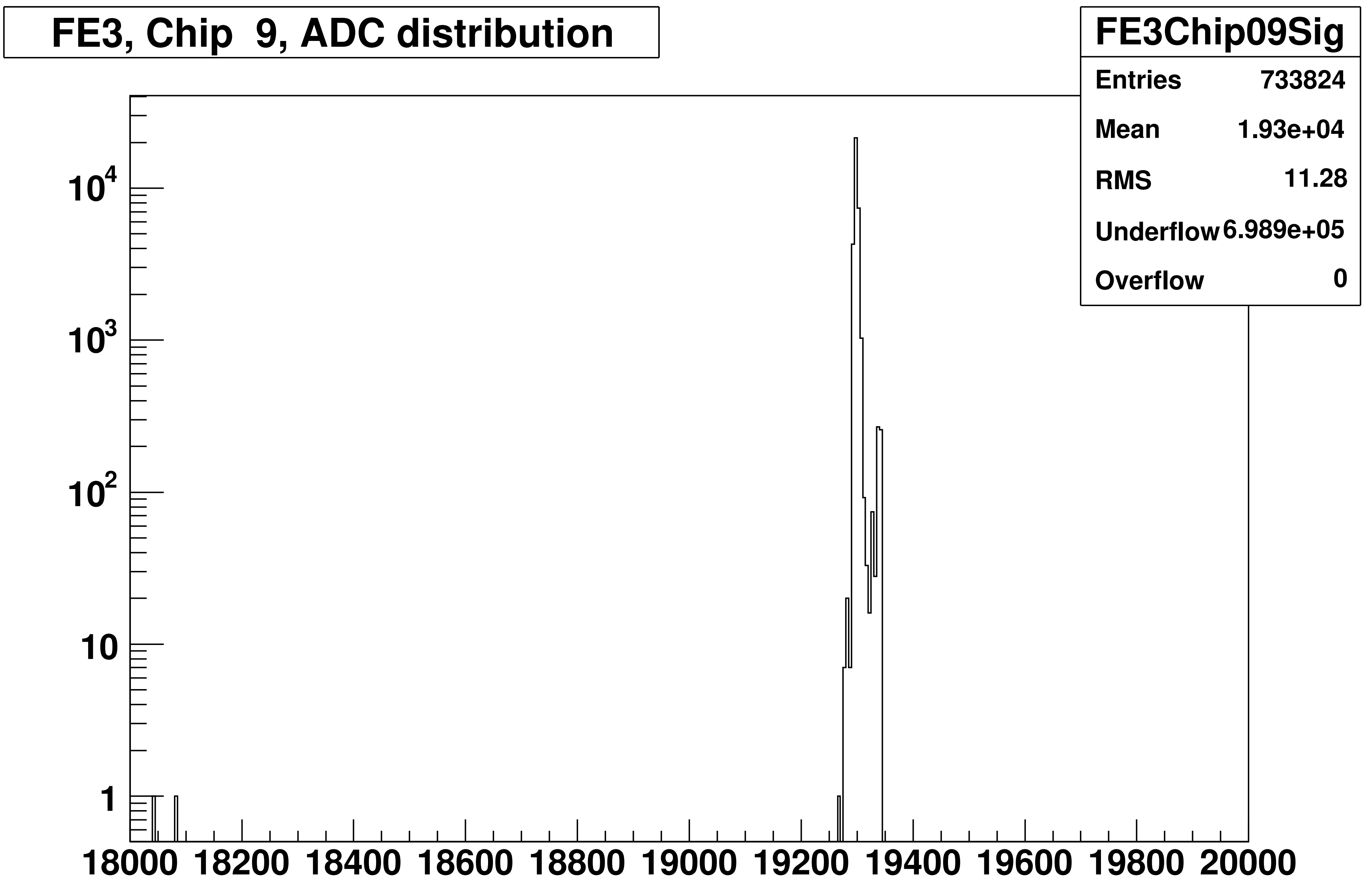
10^5
10^4
10^3
10^2
10
-200
-150
-100
-50
0
50
100
150
200


FE3, Chip 9, ADC distribution
FE3Chip09Sig
Entries 733824
Mean 1.93e+04
RMS 11.28
Underflow 6.989e+05
Overflow 0
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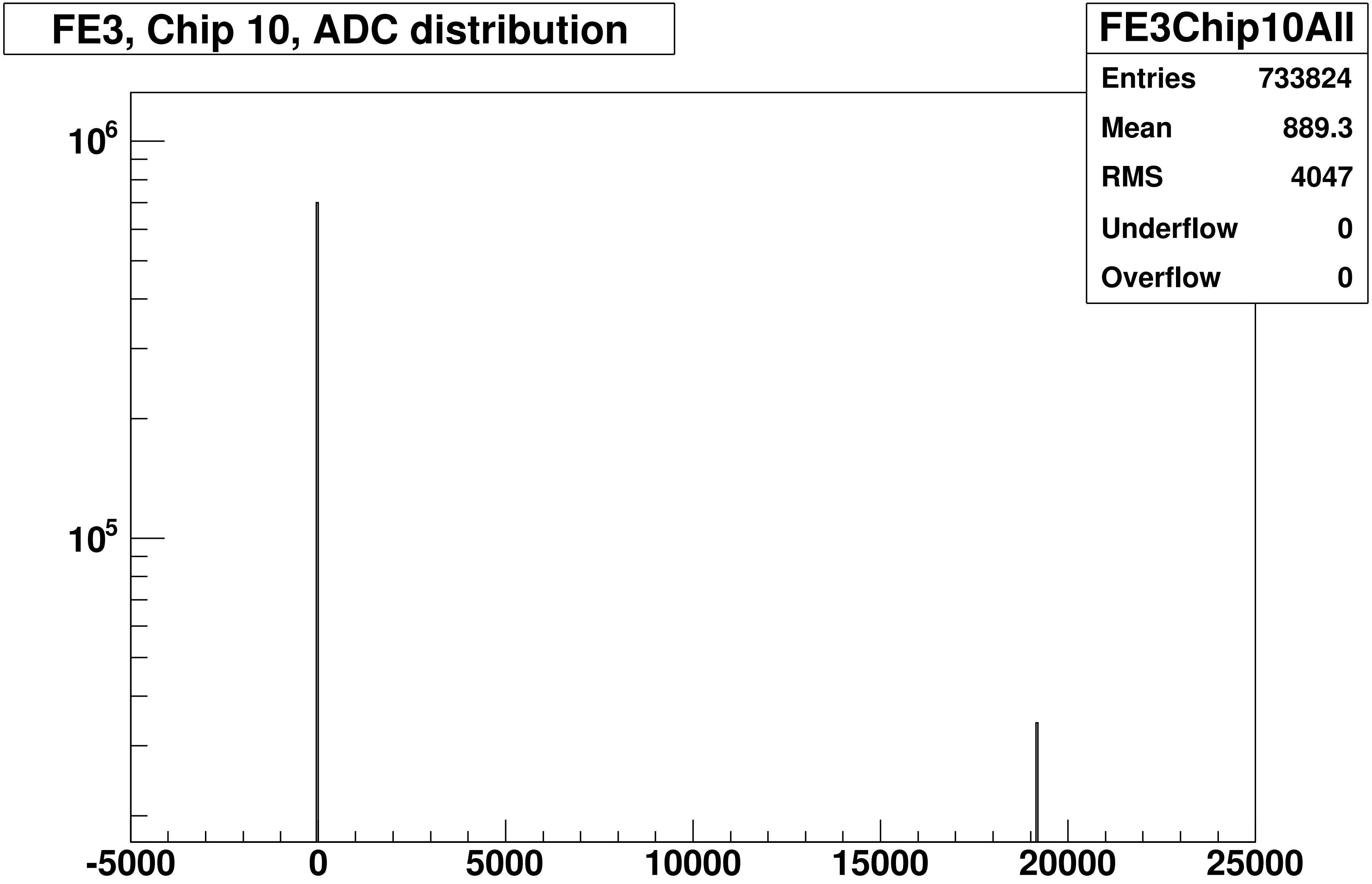
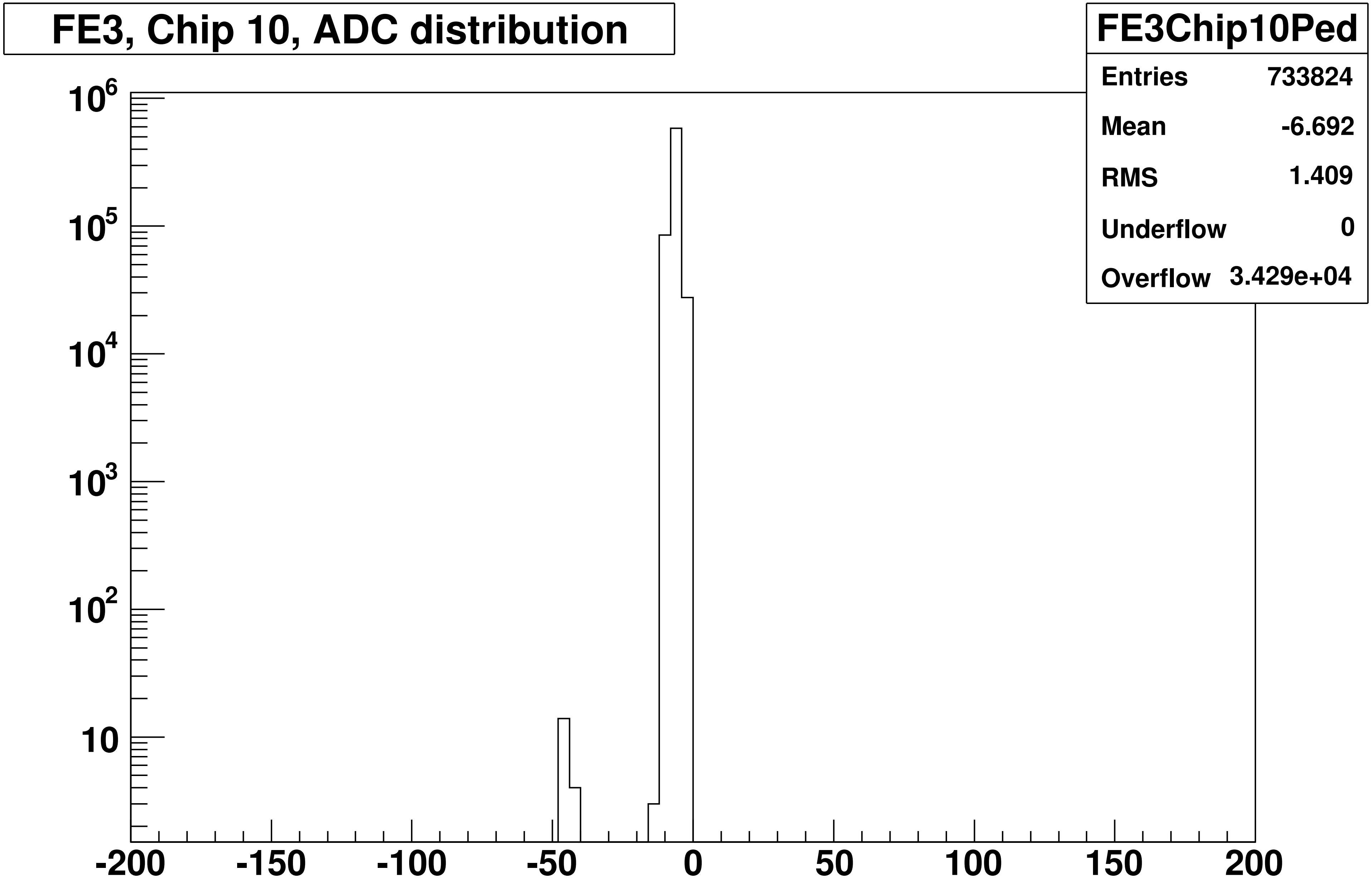
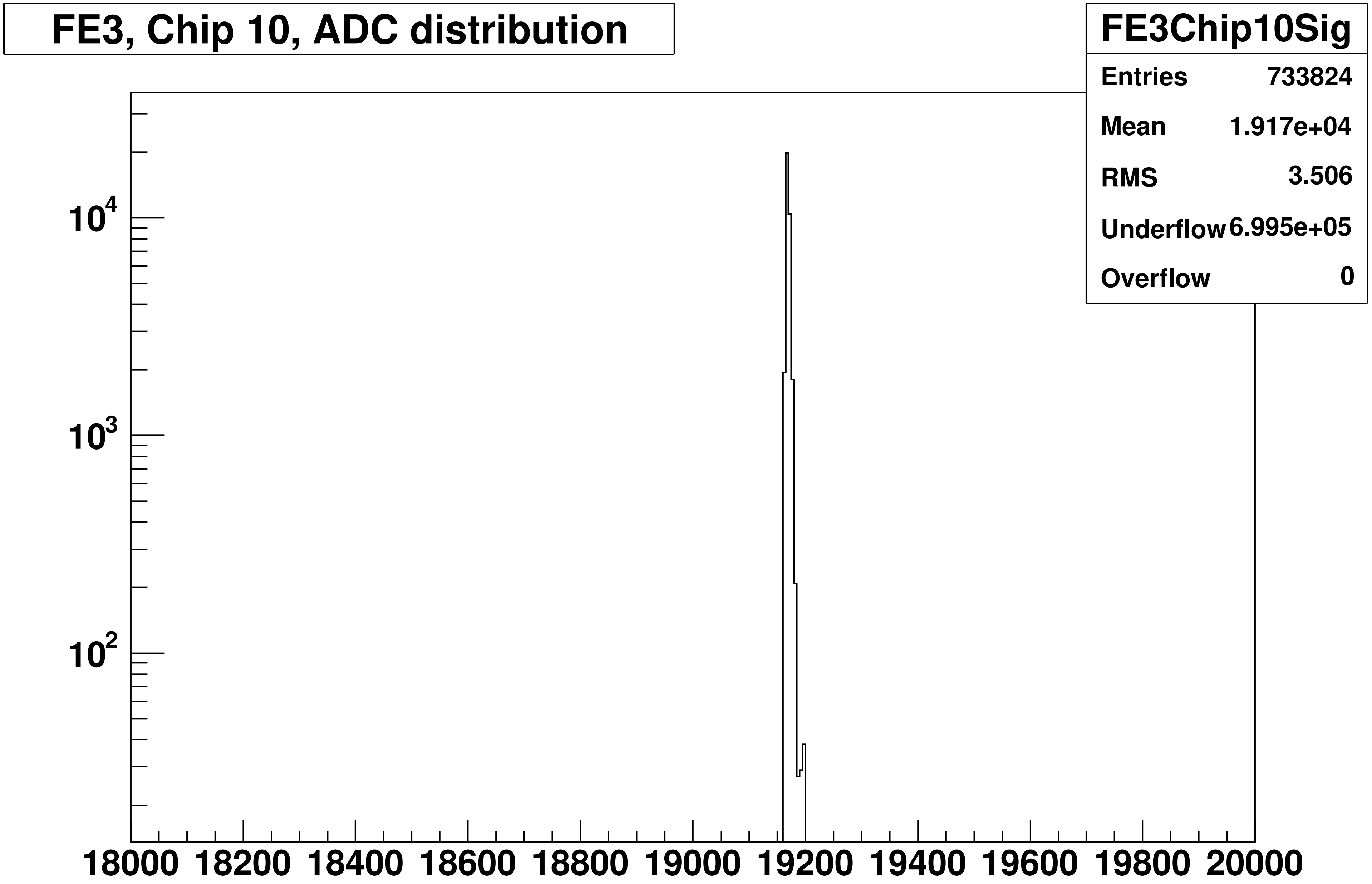
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE3, Chip 10, ADC distribution
FE3Chip10All
Entries 733824
Mean 889.3
RMS 4047
Underflow 0
Overflow 0
10^6
10^5
-5000
0
5000
10000
15000
20000
25000



FE3, Chip 10, ADC distribution
FE3Chip10Ped
Entries 733824
Mean -6.692
RMS 1.409
Underflow 0
Overflow 3.429e+04
10^6
10^5
10^4
10^3
10^2
10
-200 -150 -100 -50 0 50 100 150 200


FE3, Chip 10, ADC distribution
FE3Chip10Sig
Entries 733824
Mean 1.917e+04
RMS 3.506
Underflow 6.995e+05
Overflow 0
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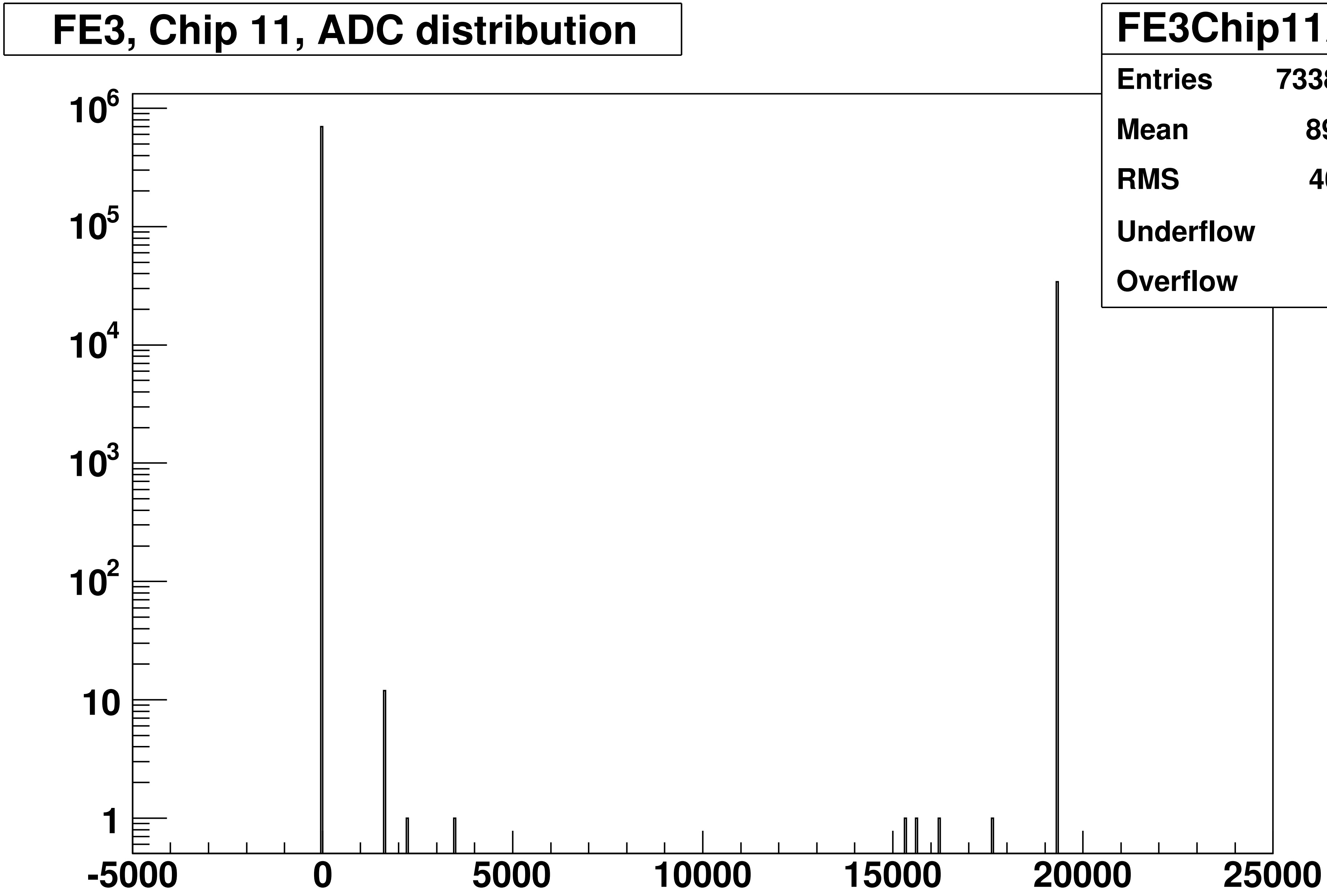
10^3
10^2
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE3, Chip 11, ADC distribution
FE3Chip11All
Entries 733824
Mean 893.1
RMS 4075
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
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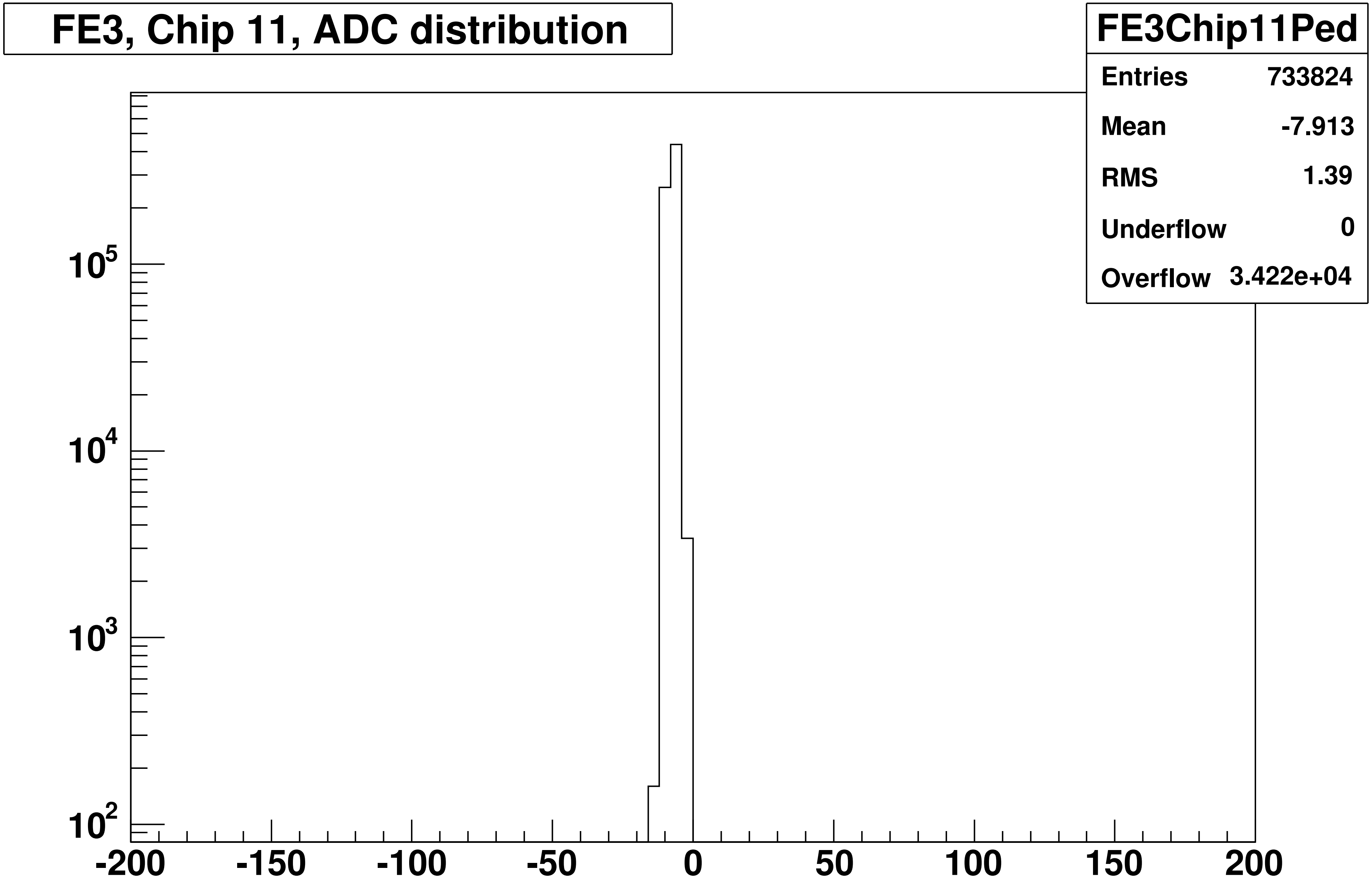
FE3, Chip 11, ADC distribution
FE3Chip11Ped
Entries 733824
Mean -7.913
RMS 1.39
Underflow 0
Overflow 3.422e+04
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10^4
10^3
10^2
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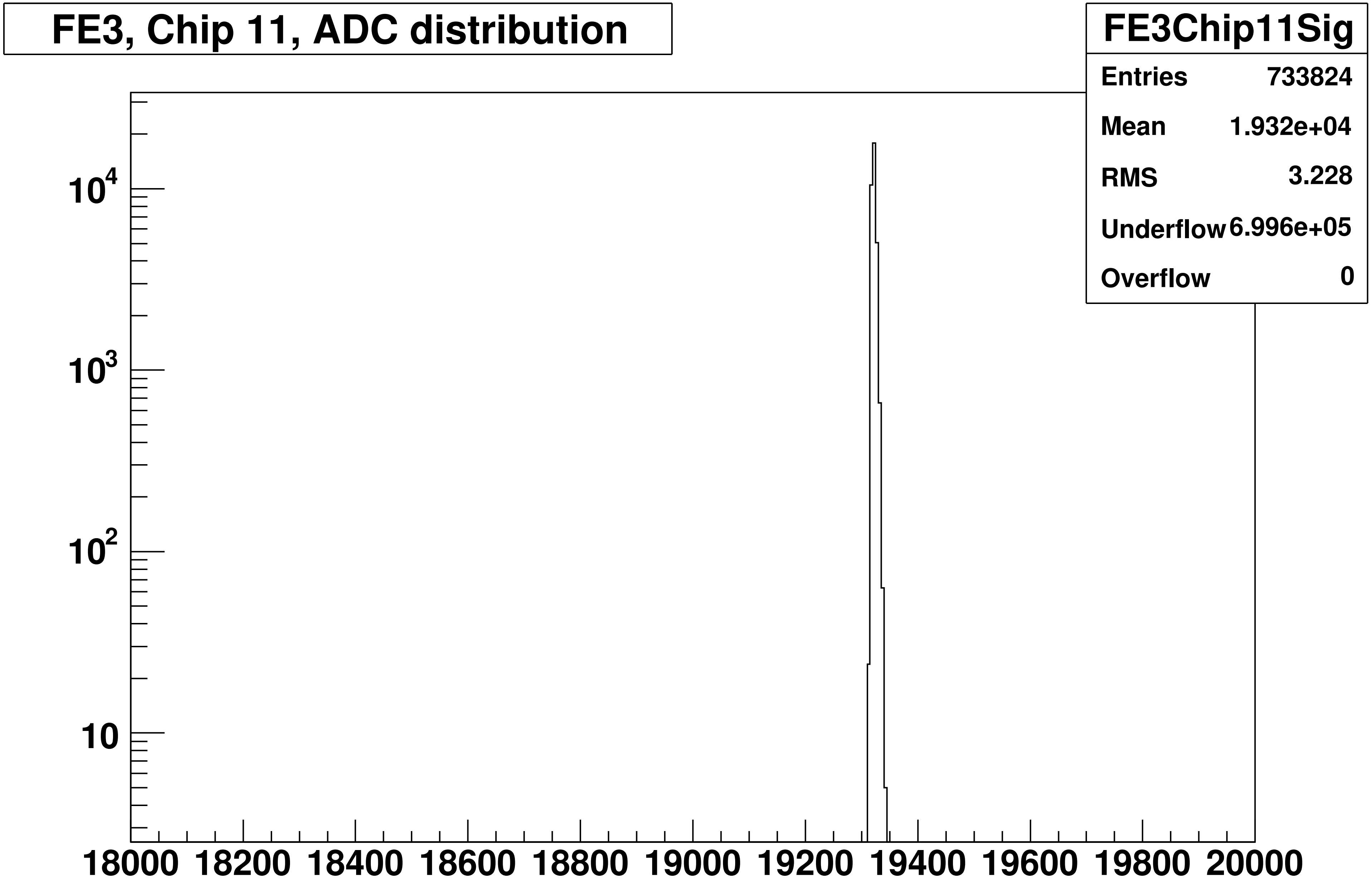

FE3, Chip 11, ADC distribution
FE3Chip11Sig
Entries 733824
Mean 1.932e+04
RMS 3.228
Underflow 6.996e+05
Overflow 0
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10^3
10^2
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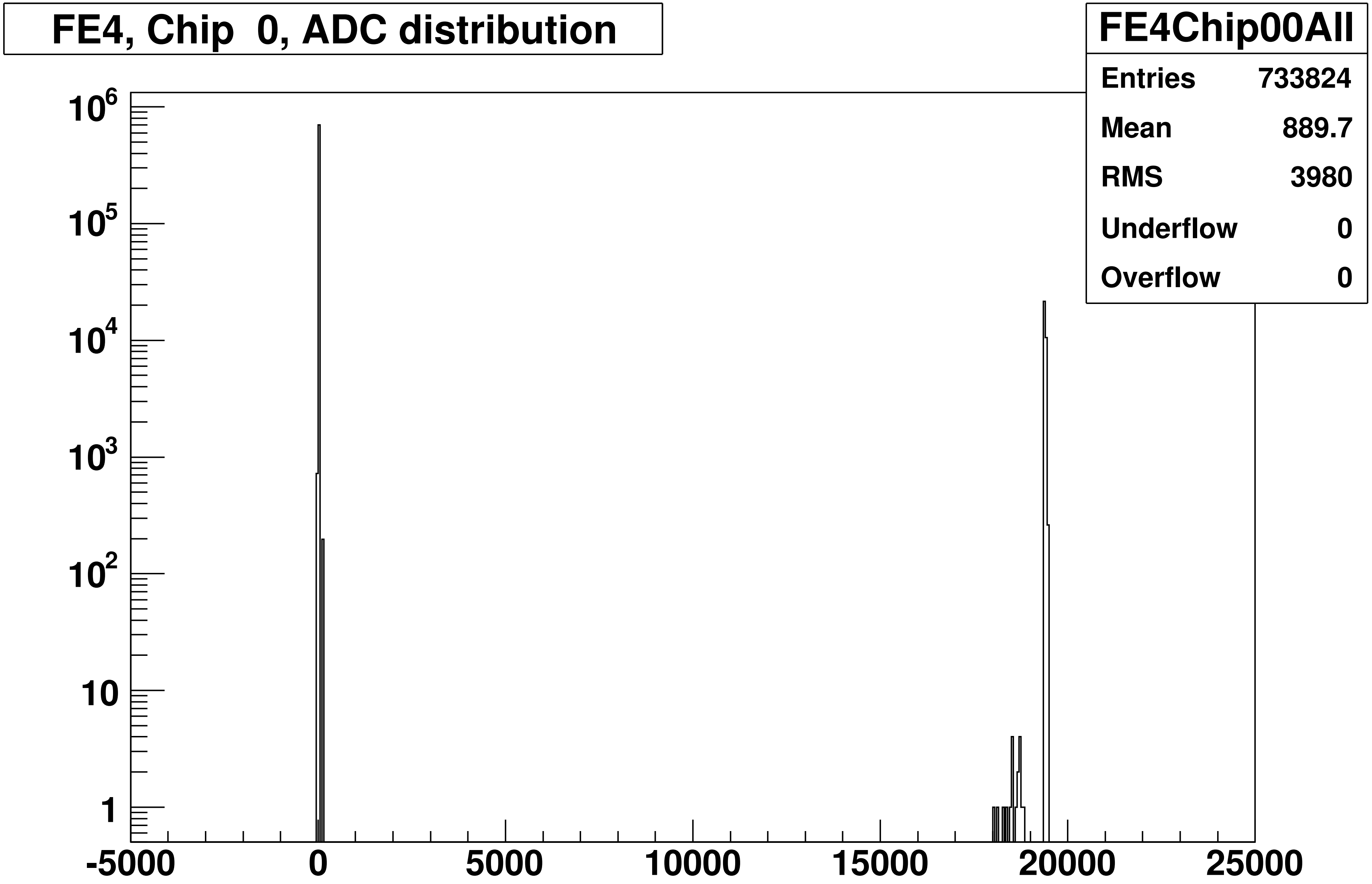
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE4, Chip 0, ADC distribution
FE4Chip00All
Entries 733824
Mean 889.7
RMS 3980
Underflow 0
Overflow 0
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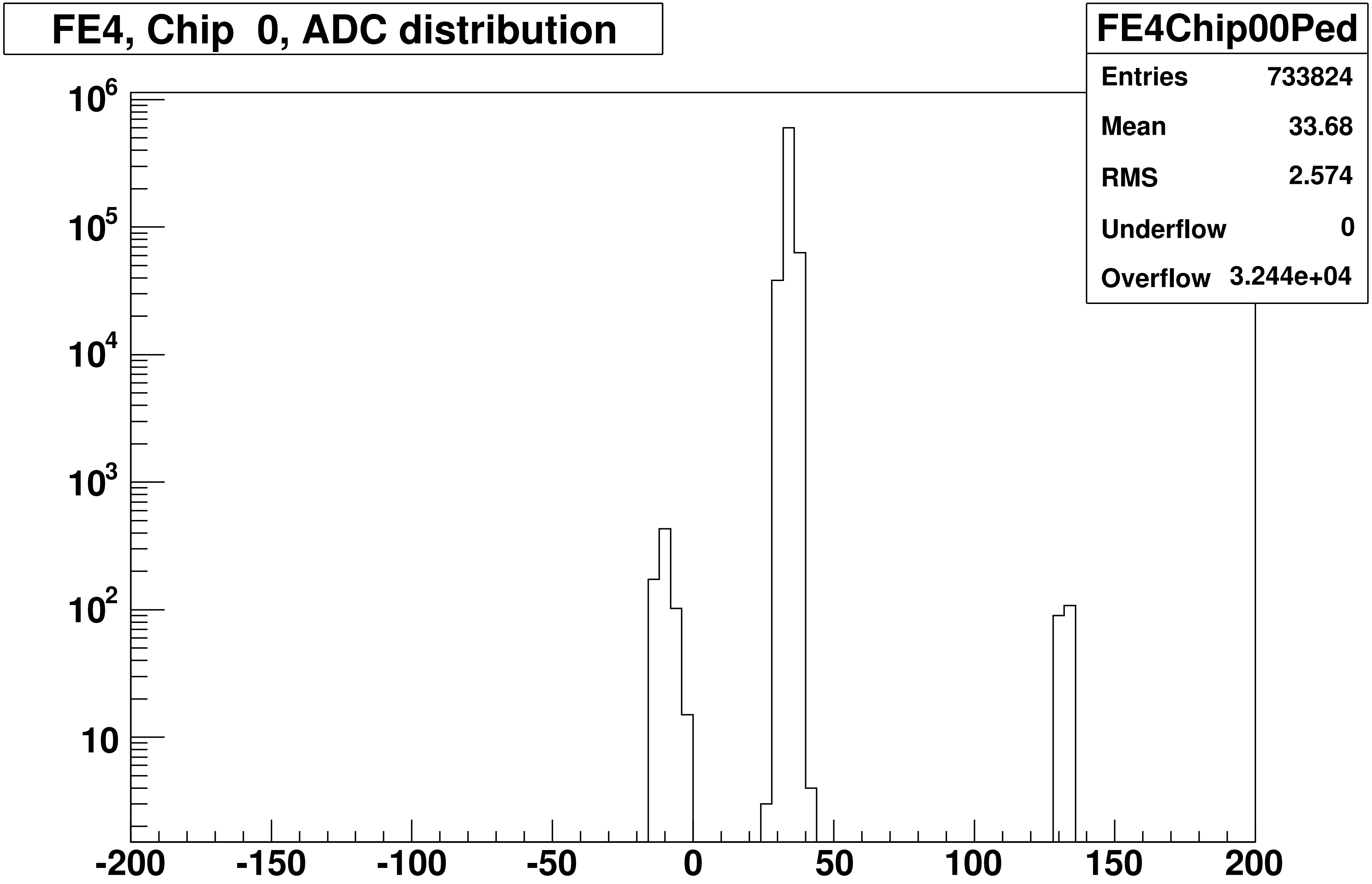
FE4, Chip 0, ADC distribution
FE4Chip00Ped
Entries 733824
Mean 33.68
RMS 2.574
Underflow 0
Overflow 3.244e+04
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10^4
10^3
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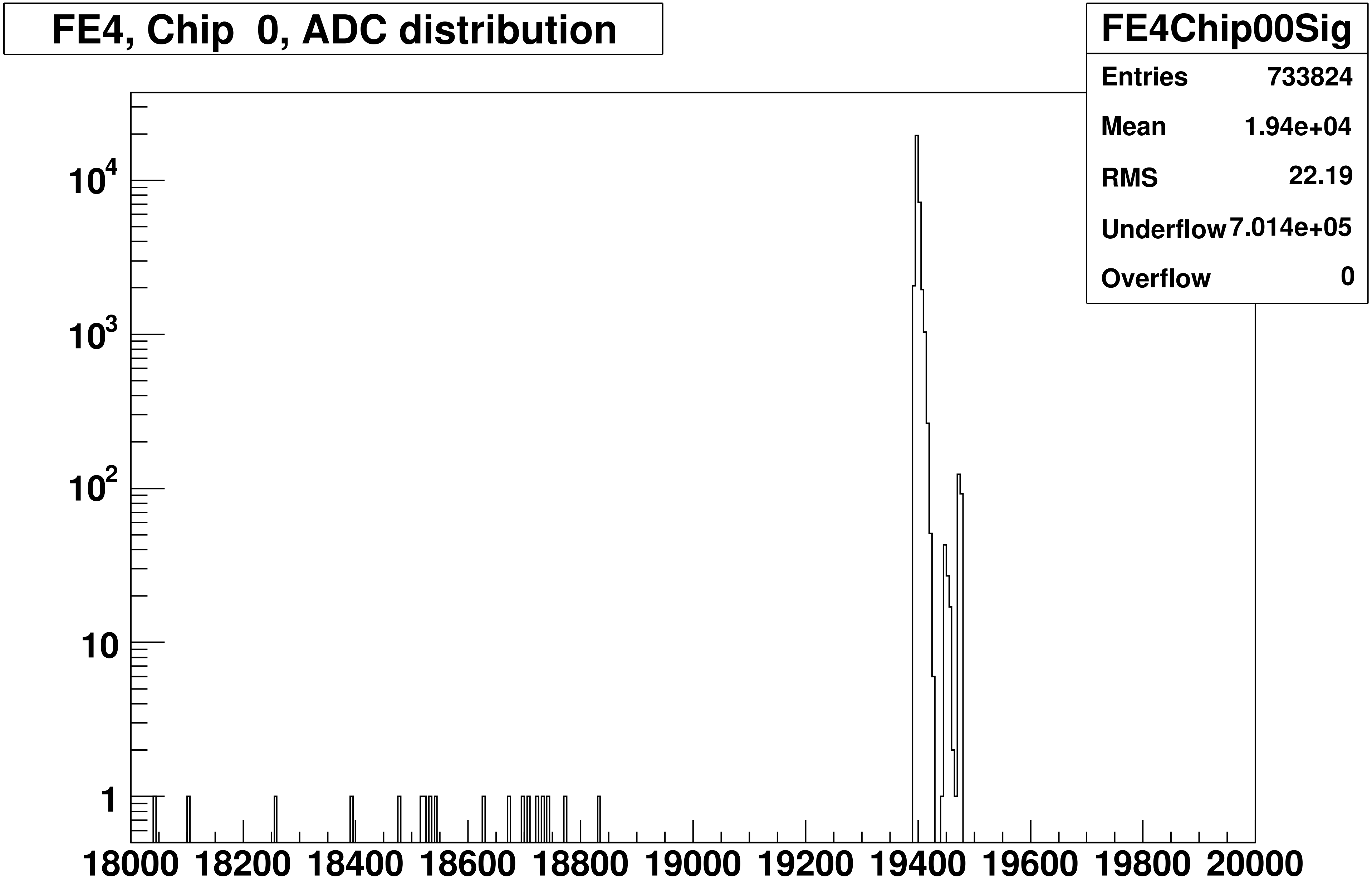
FE4, Chip 0, ADC distribution
FE4Chip00Sig
Entries 733824
Mean 1.94e+04
RMS 22.19
Underflow 7.014e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
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18400
18600
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19000
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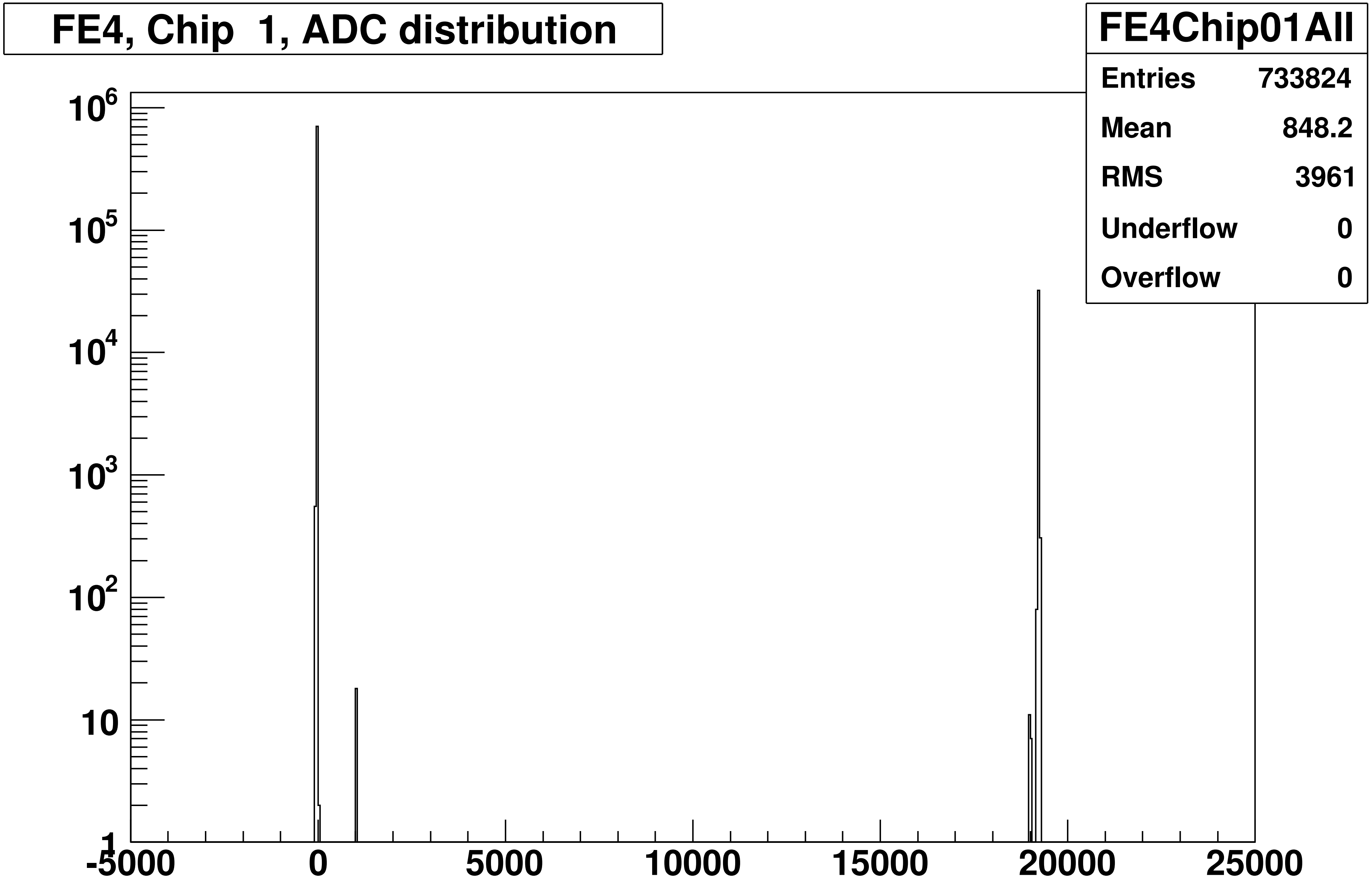
19800
20000


FE4, Chip 1, ADC distribution
FE4Chip01All
Entries 733824
Mean 848.2
RMS 3961
Underflow 0
Overflow 0
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10^3
10^2
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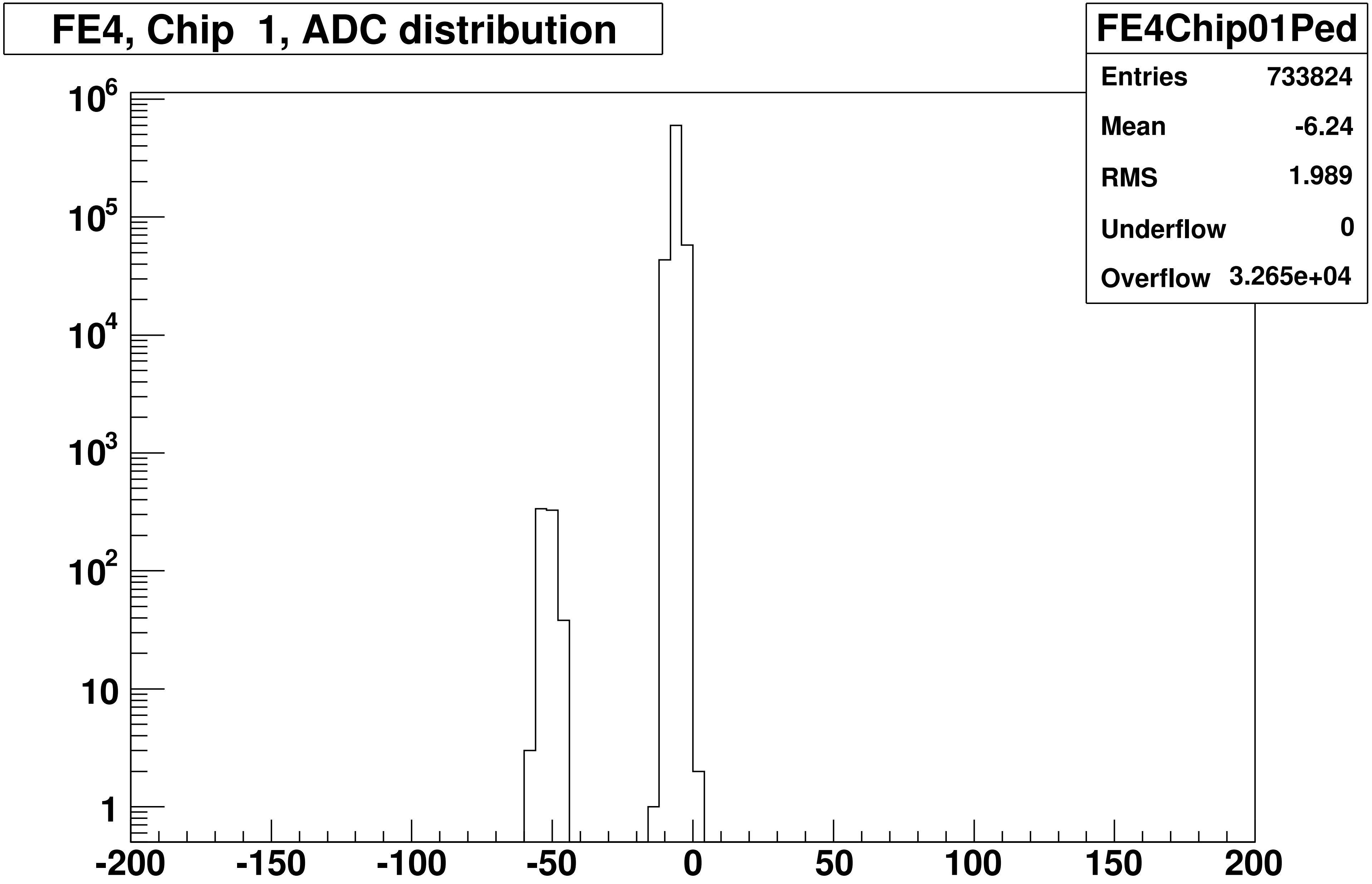

FE4, Chip 1, ADC distribution
FE4Chip01Ped
Entries 733824
Mean -6.24
RMS 1.989
Underflow 0
Overflow 3.265e+04
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150
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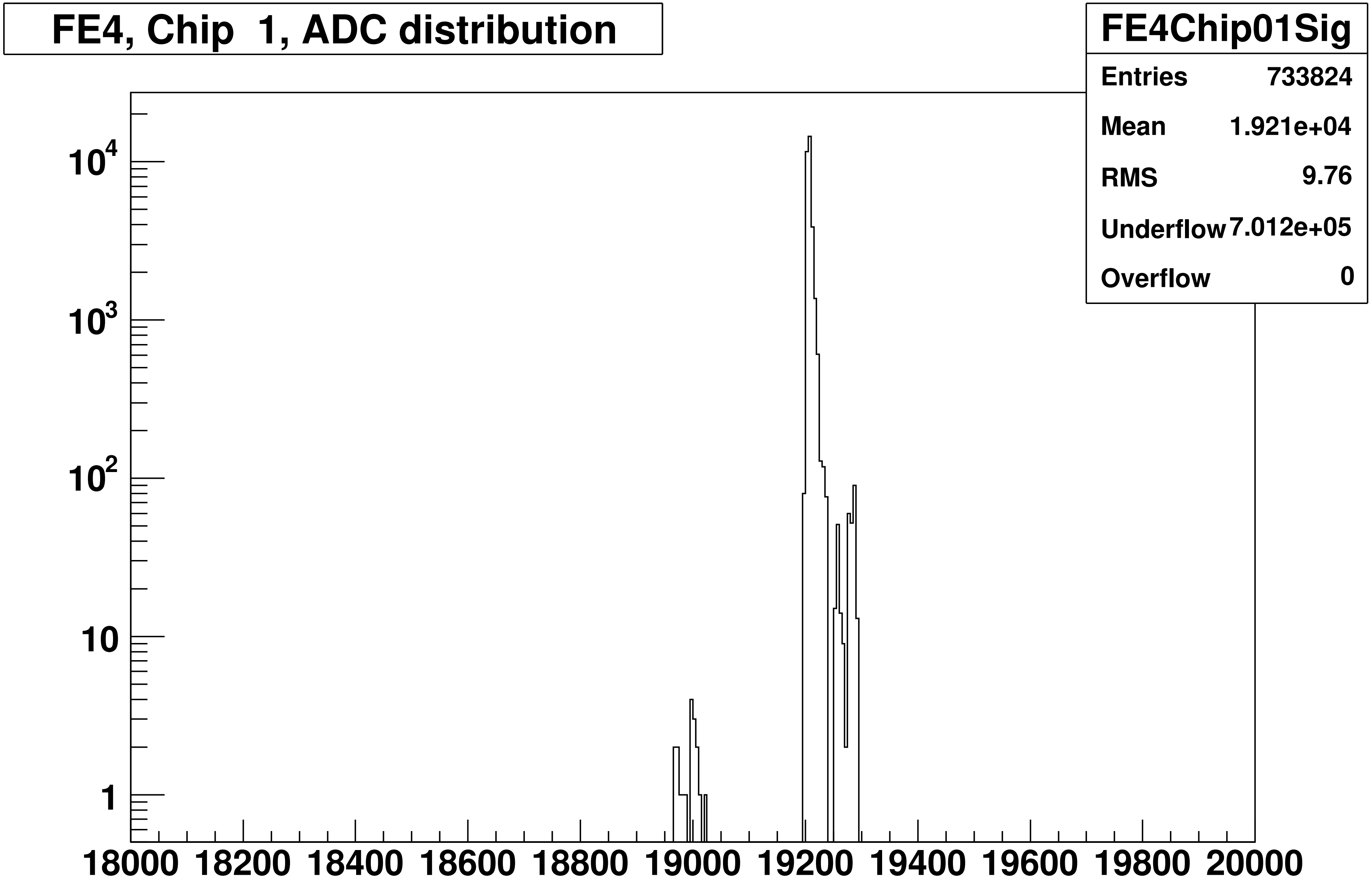

FE4, Chip 1, ADC distribution
FE4Chip01Sig
Entries 733824
Mean 1.921e+04
RMS 9.76
Underflow 7.012e+05
Overflow 0
10^4
10^3
10^2
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1
18000
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19000
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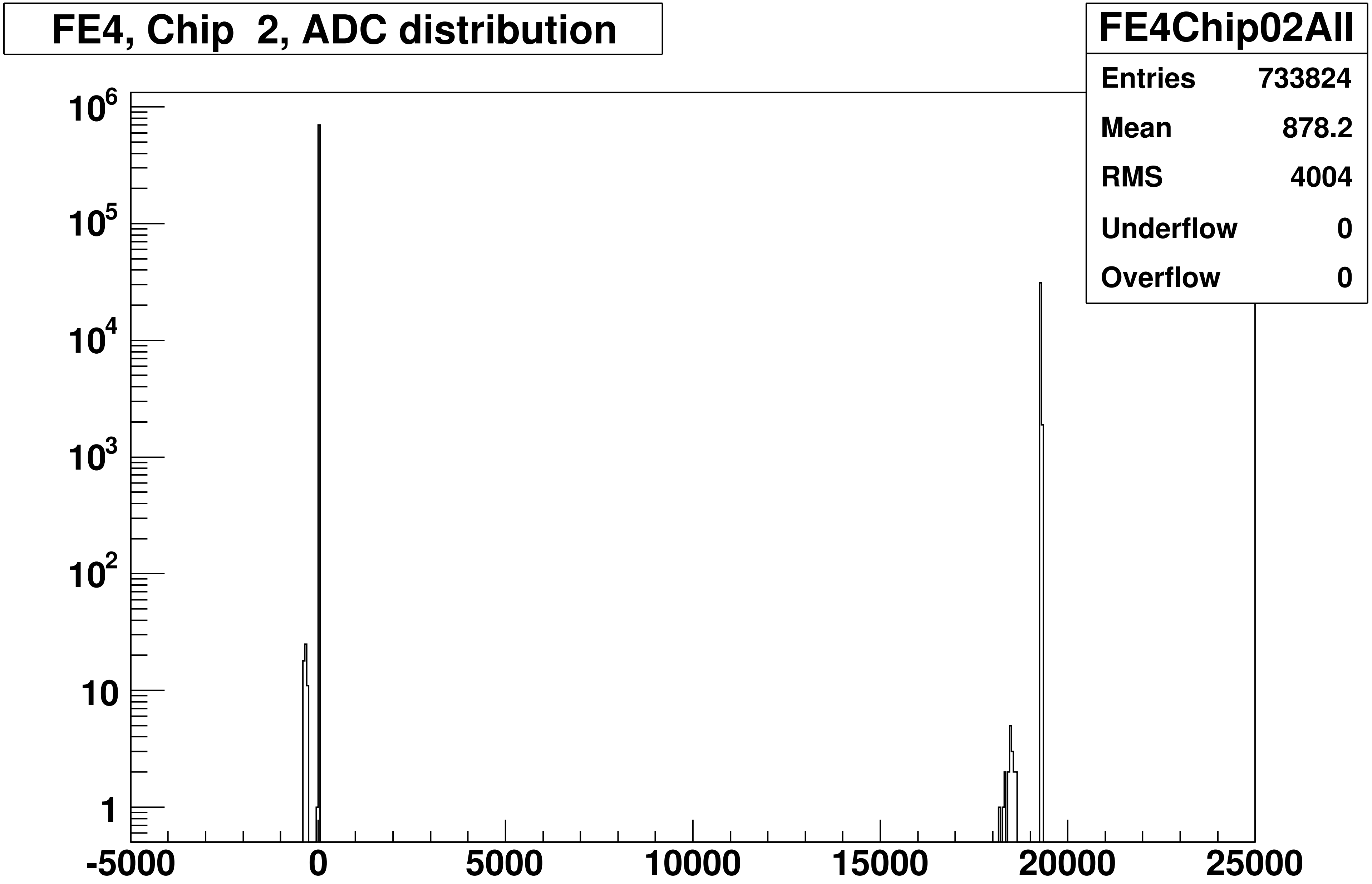
20000



FE4, Chip 2, ADC distribution
FE4Chip02All
Entries 733824
Mean 878.2
RMS 4004
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
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-5000
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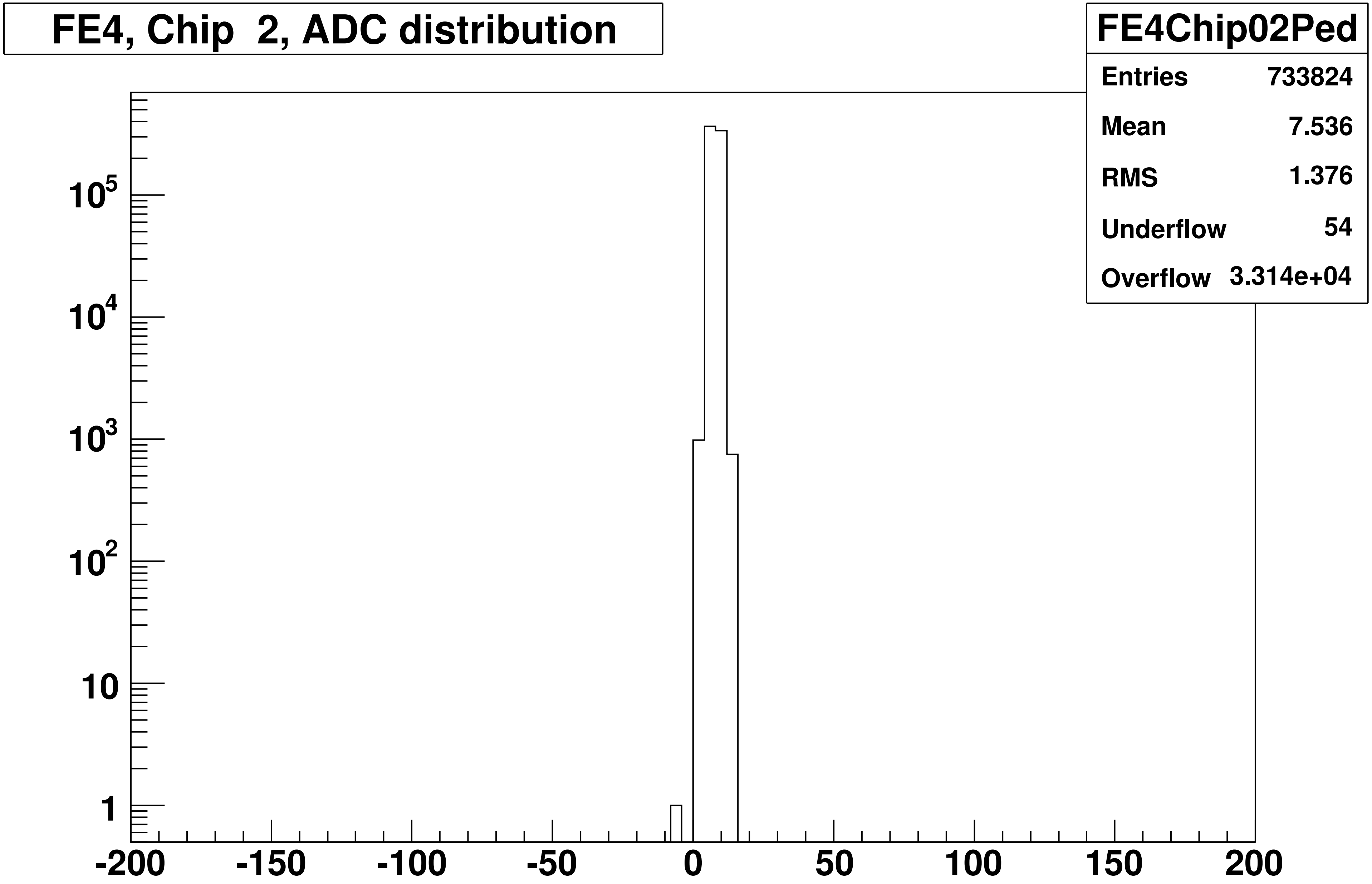
25000



FE4, Chip 2, ADC distribution
FE4Chip02Ped
Entries 733824
Mean 7.536
RMS 1.376
Underflow 54
Overflow 3.314e+04
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10^3
10^2
10
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150
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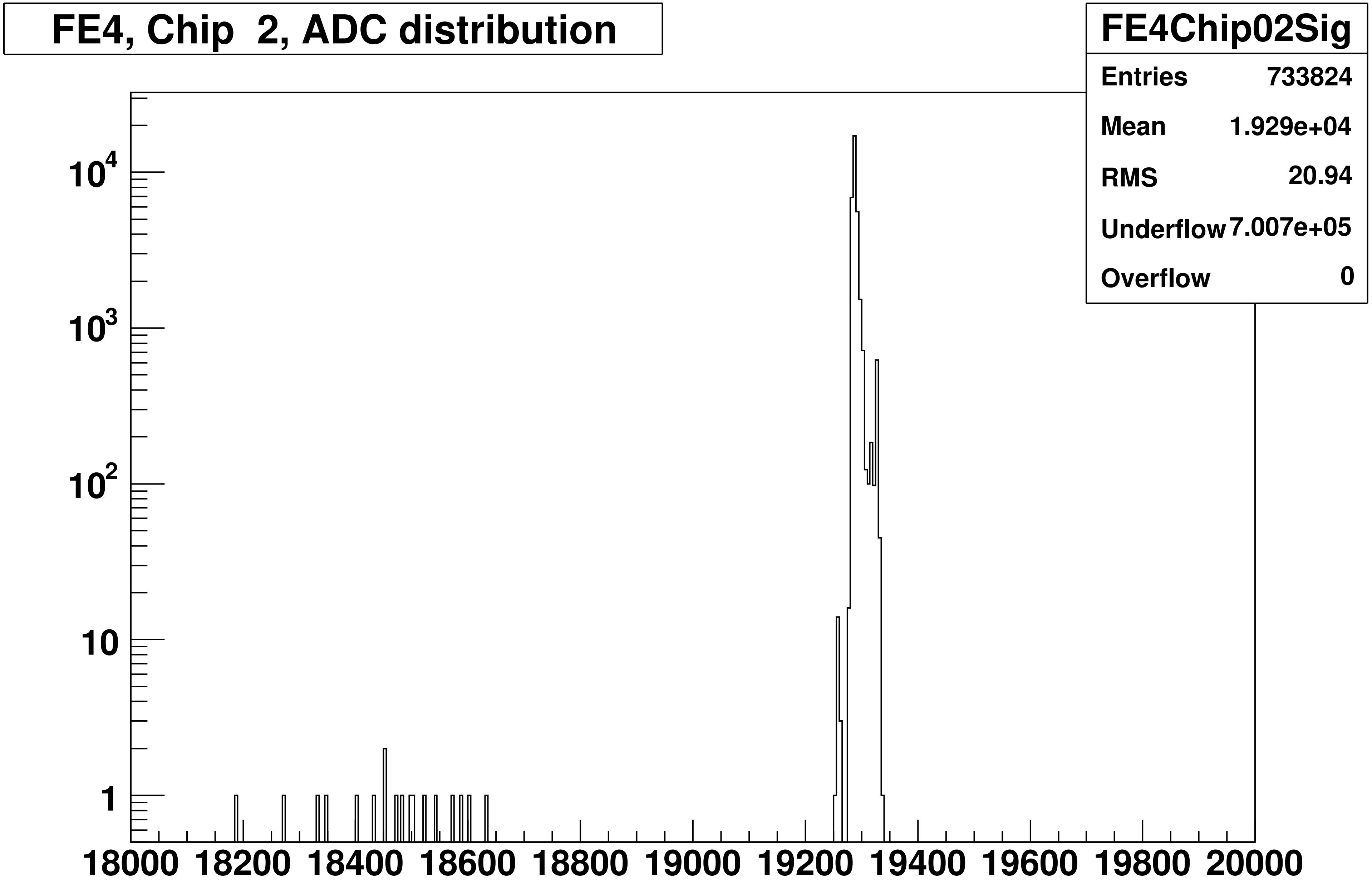

FE4, Chip 2, ADC distribution
FE4Chip02Sig
Entries 733824
Mean 1.929e+04
RMS 20.94
Underflow 7.007e+05
Overflow 0
10^4
10^3
10^2
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1
18000
18200
18400
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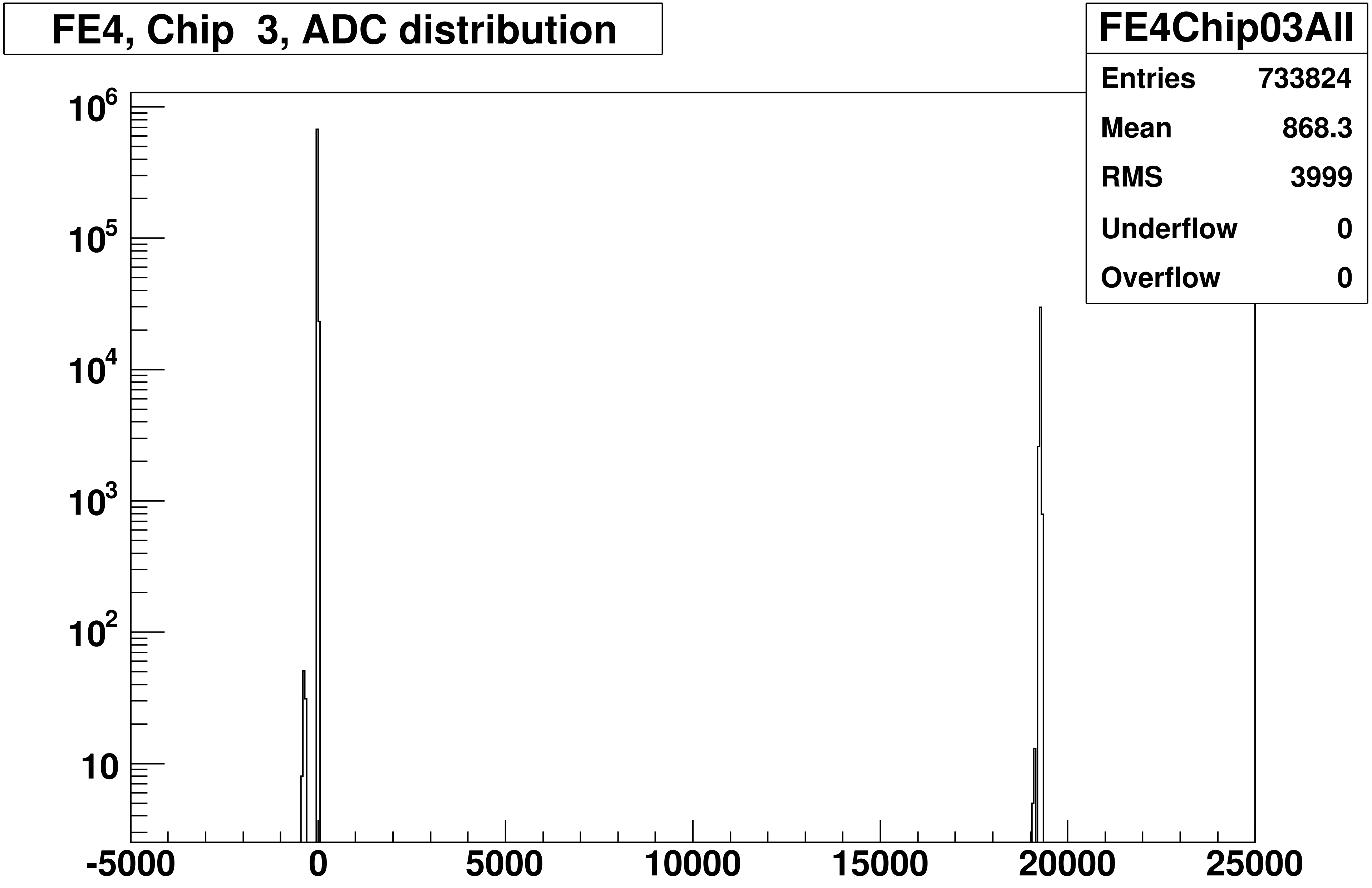
19400
19600
19800
20000


FE4, Chip 3, ADC distribution
FE4Chip03All
Entries 733824
Mean 868.3
RMS 3999
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
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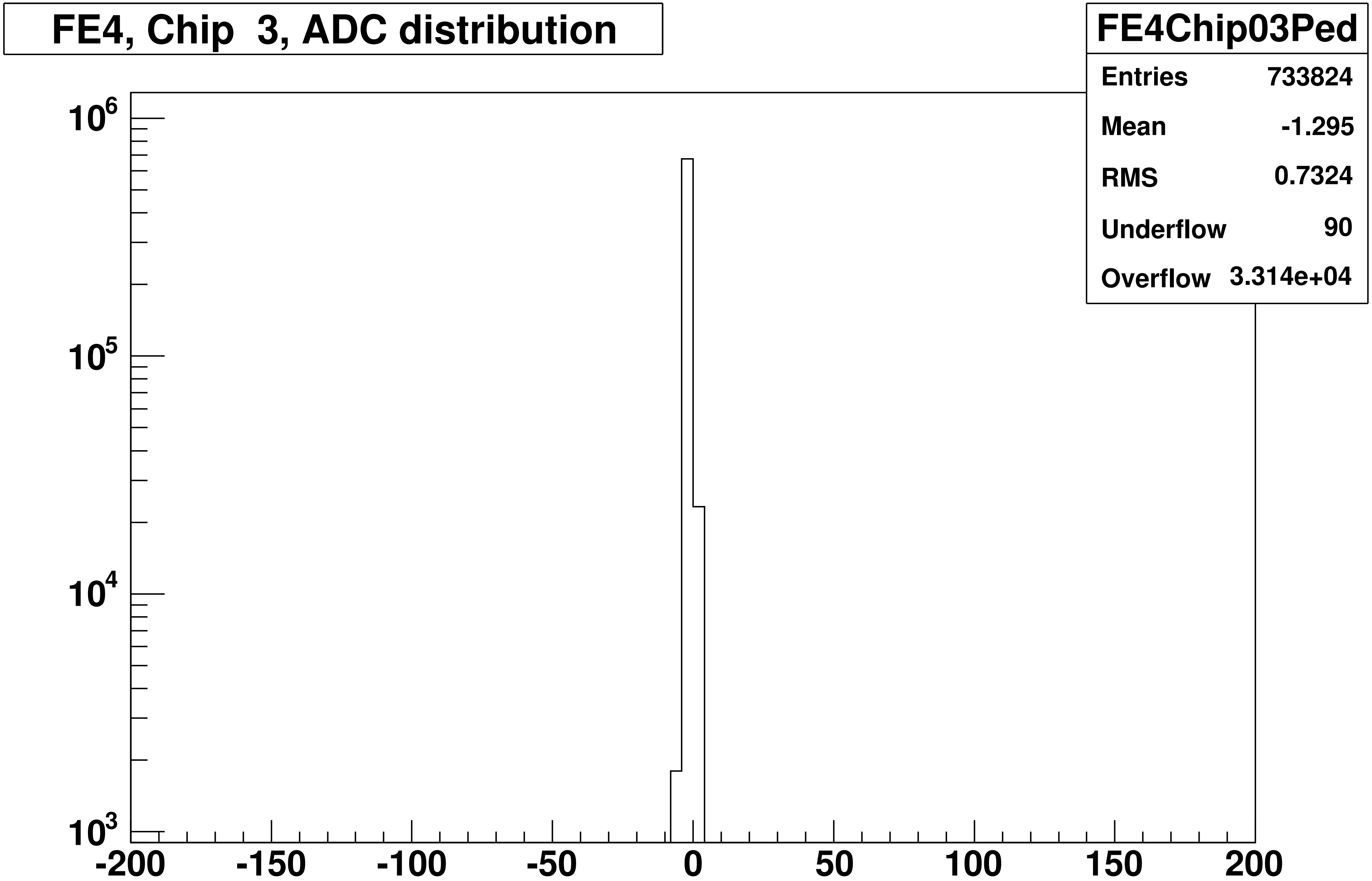
FE4, Chip 3, ADC distribution
FE4Chip03Ped
Entries 733824
Mean -1.295
RMS 0.7324
Underflow 90
Overflow 3.314e+04
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10^5
10^4
10^3
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-100
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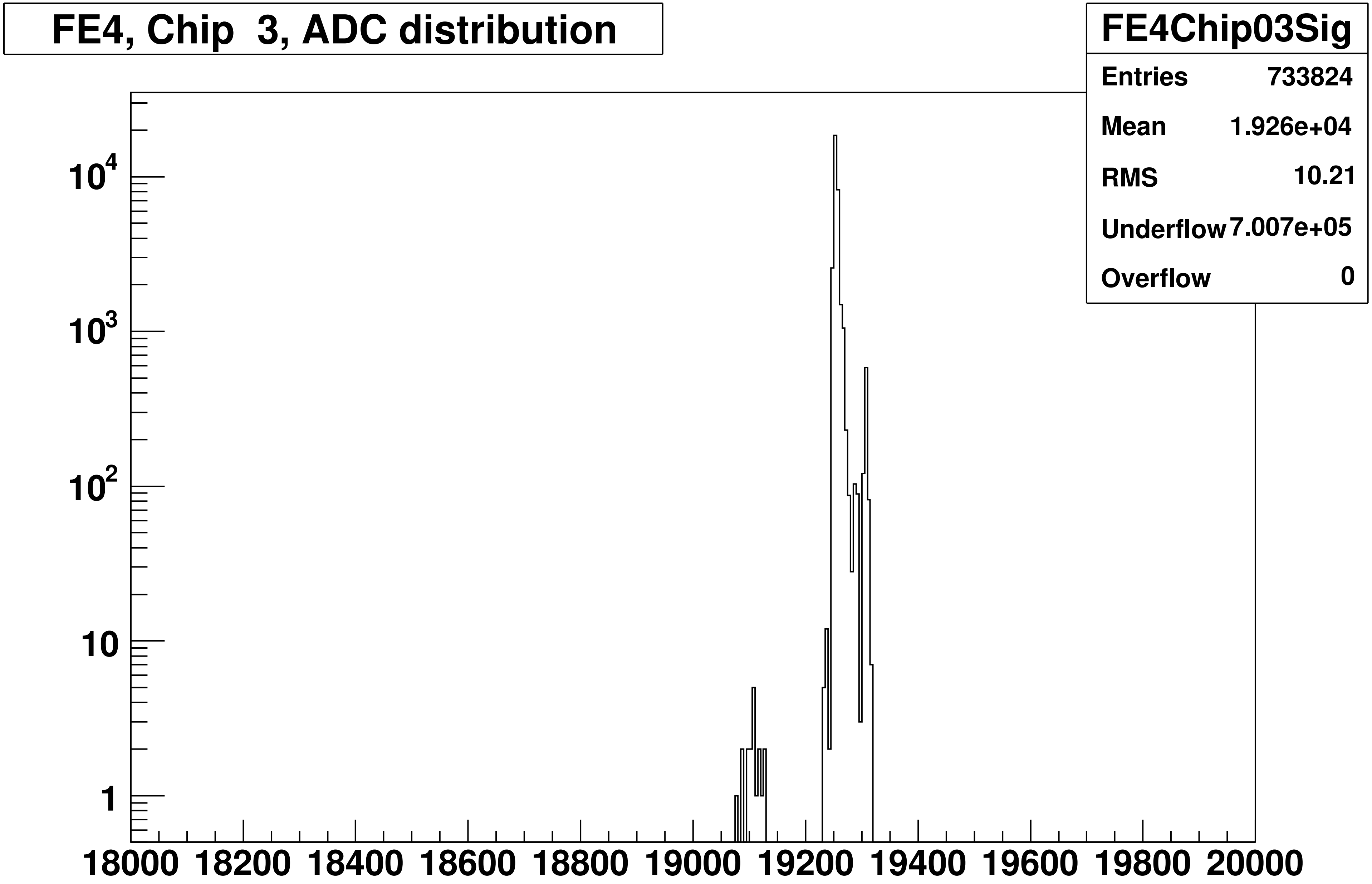
150
200


FE4, Chip 3, ADC distribution
FE4Chip03Sig
Entries 733824
Mean 1.926e+04
RMS 10.21
Underflow 7.007e+05
Overflow 0
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10^3
10^2
10
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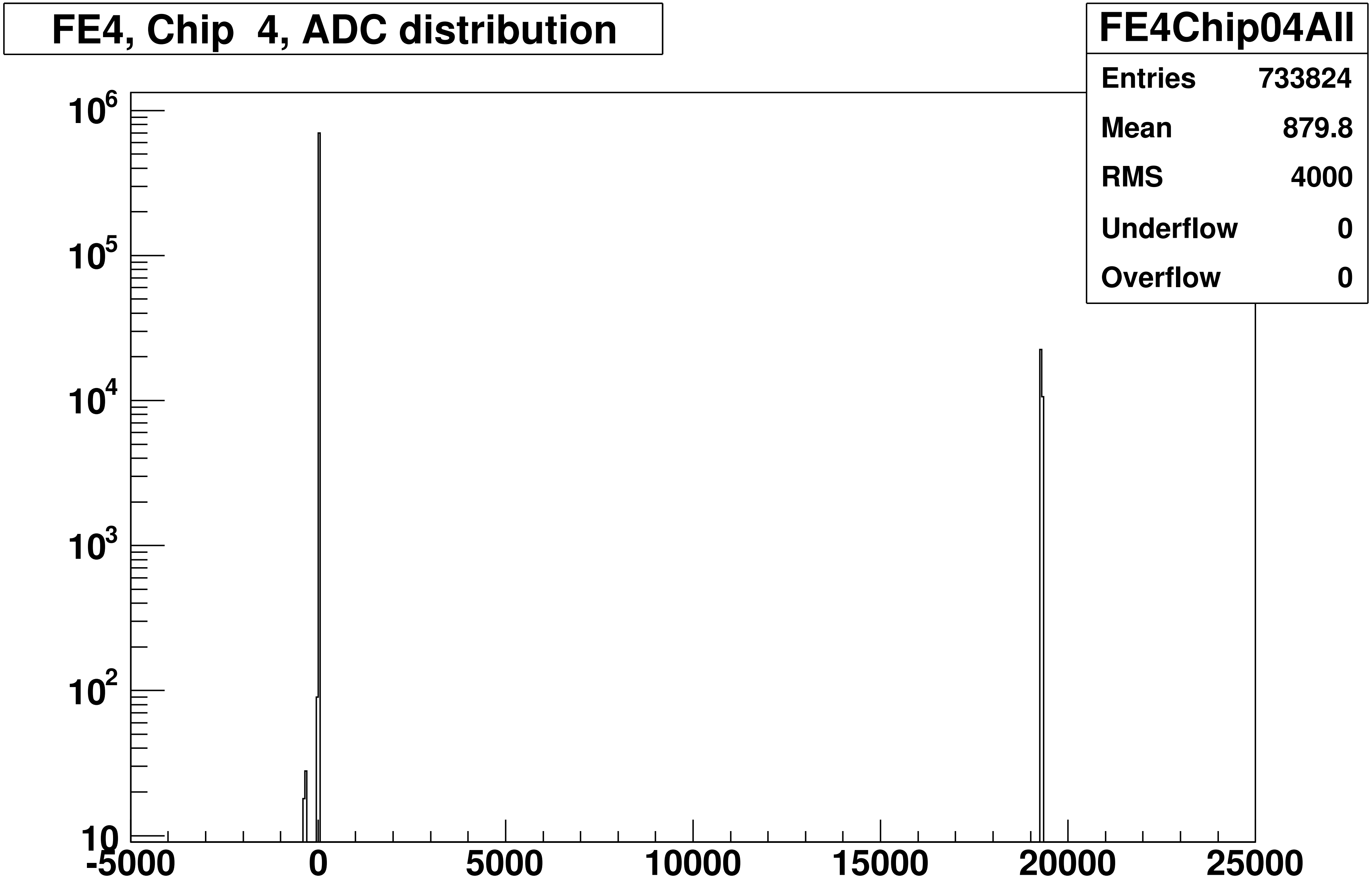
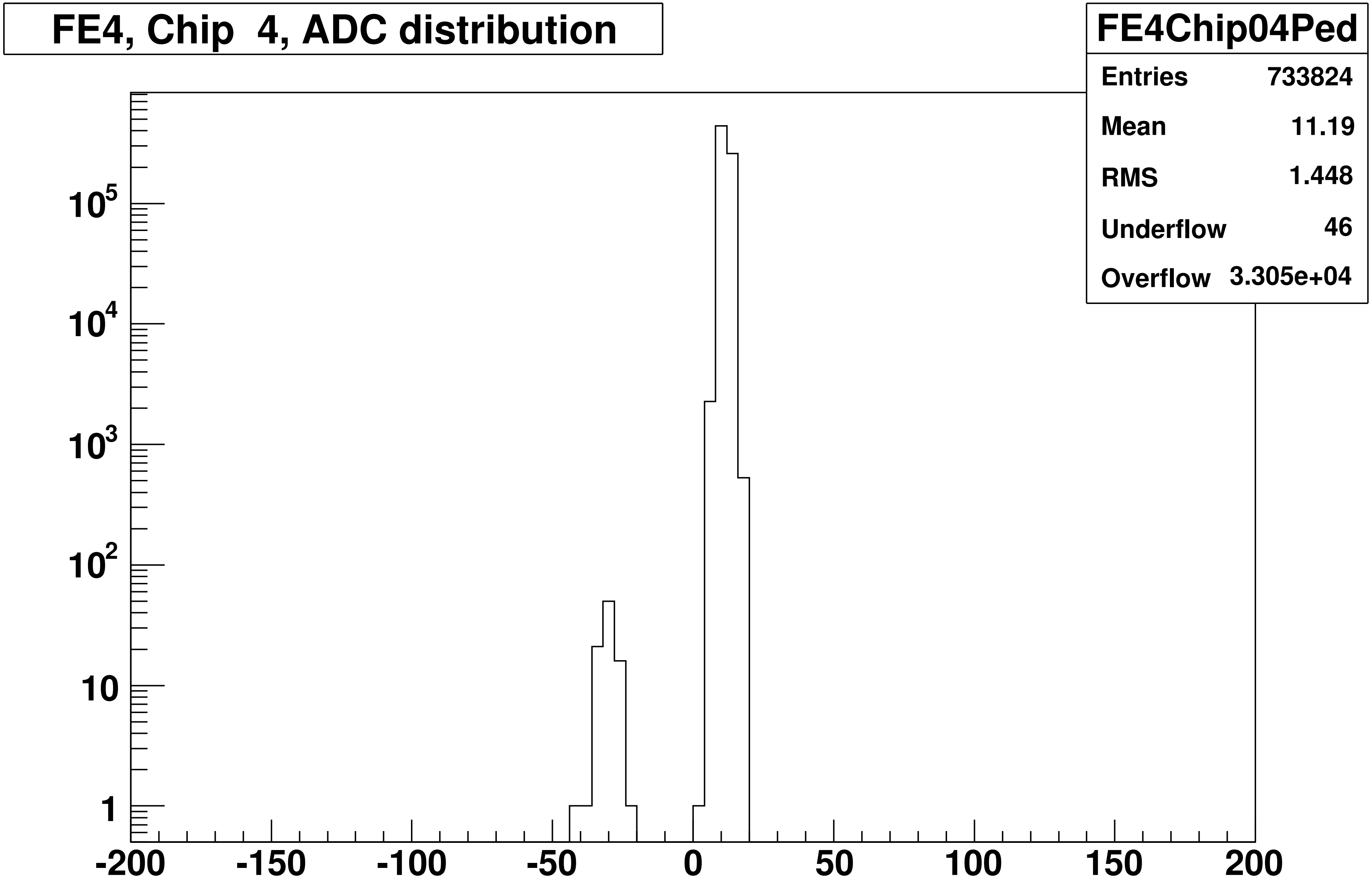
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE4, Chip 4, ADC distribution
FE4Chip04All
Entries 733824
Mean 879.8
RMS 4000
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE4, Chip 4, ADC distribution
FE4Chip04Ped
Entries 733824
Mean 11.19
RMS 1.448
Underflow 46
Overflow 3.305e+04
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10^3
10^2
10
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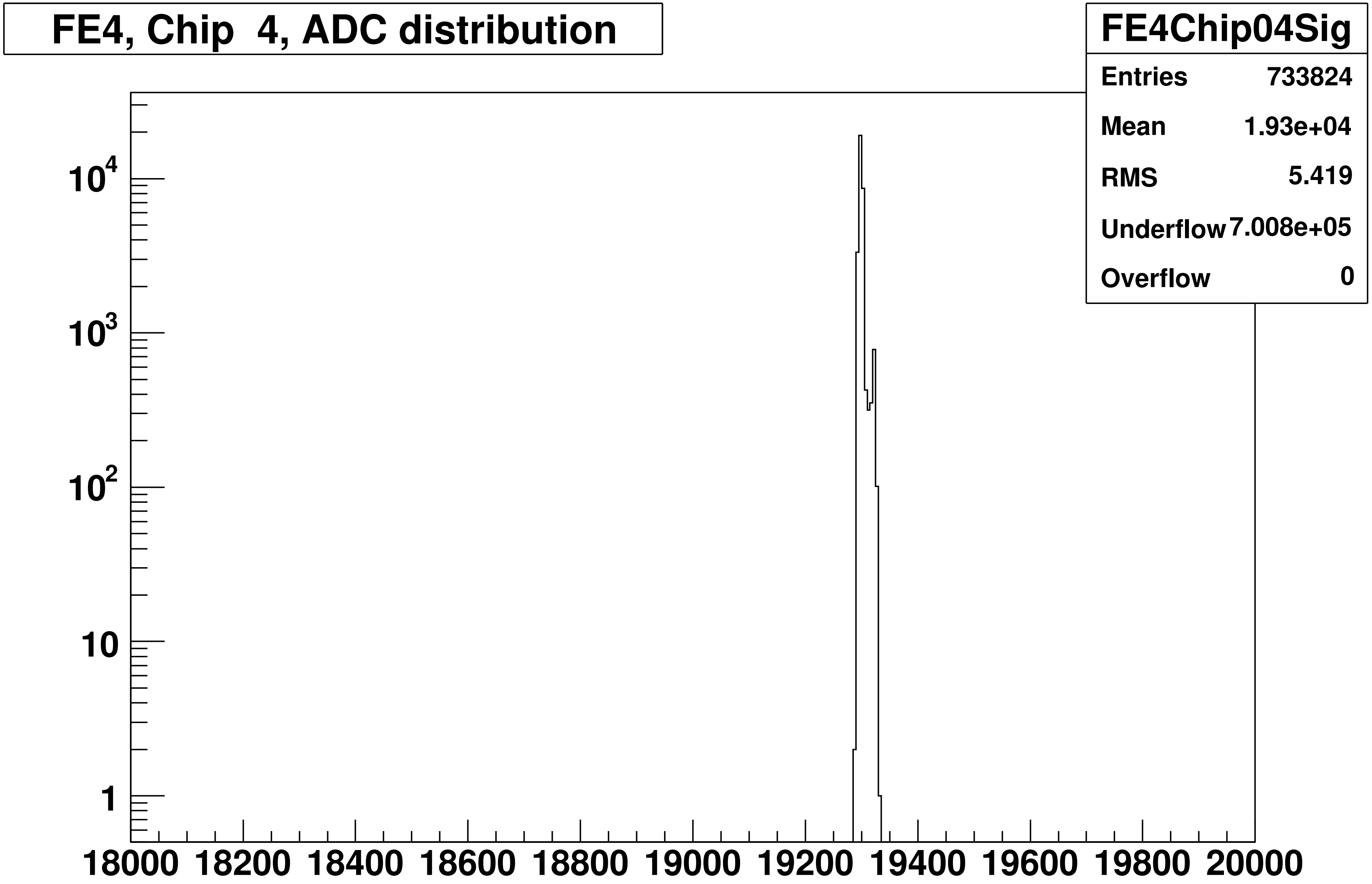
FE4, Chip 4, ADC distribution
FE4Chip04Sig
Entries 733824
Mean 1.93e+04
RMS 5.419
Underflow 7.008e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
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19000
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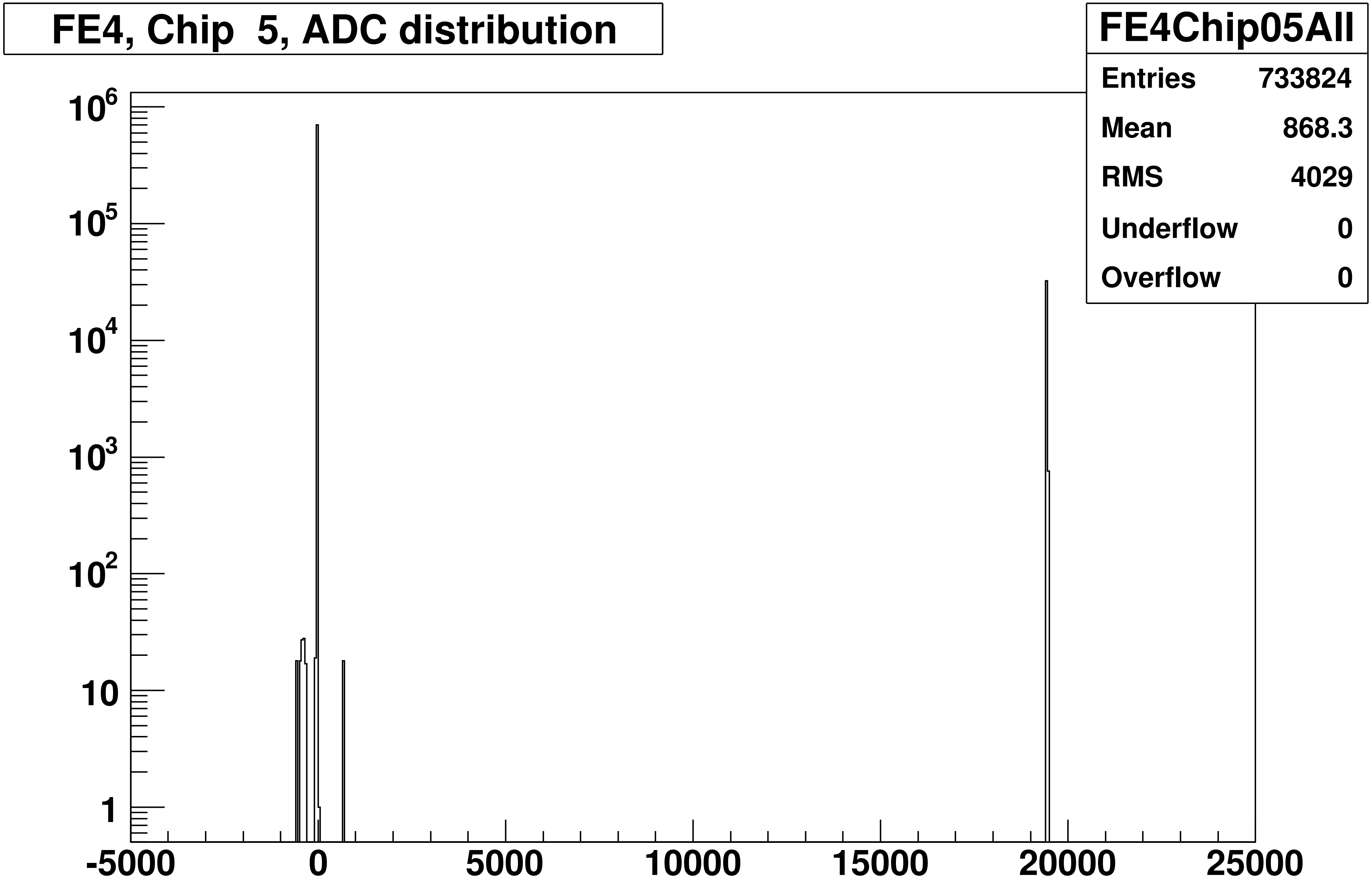
19600
19800
20000



FE4, Chip 5, ADC distribution
FE4Chip05All
Entries 733824
Mean 868.3
RMS 4029
Underflow 0
Overflow 0
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10^4
10^3
10^2
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0
5000
10000
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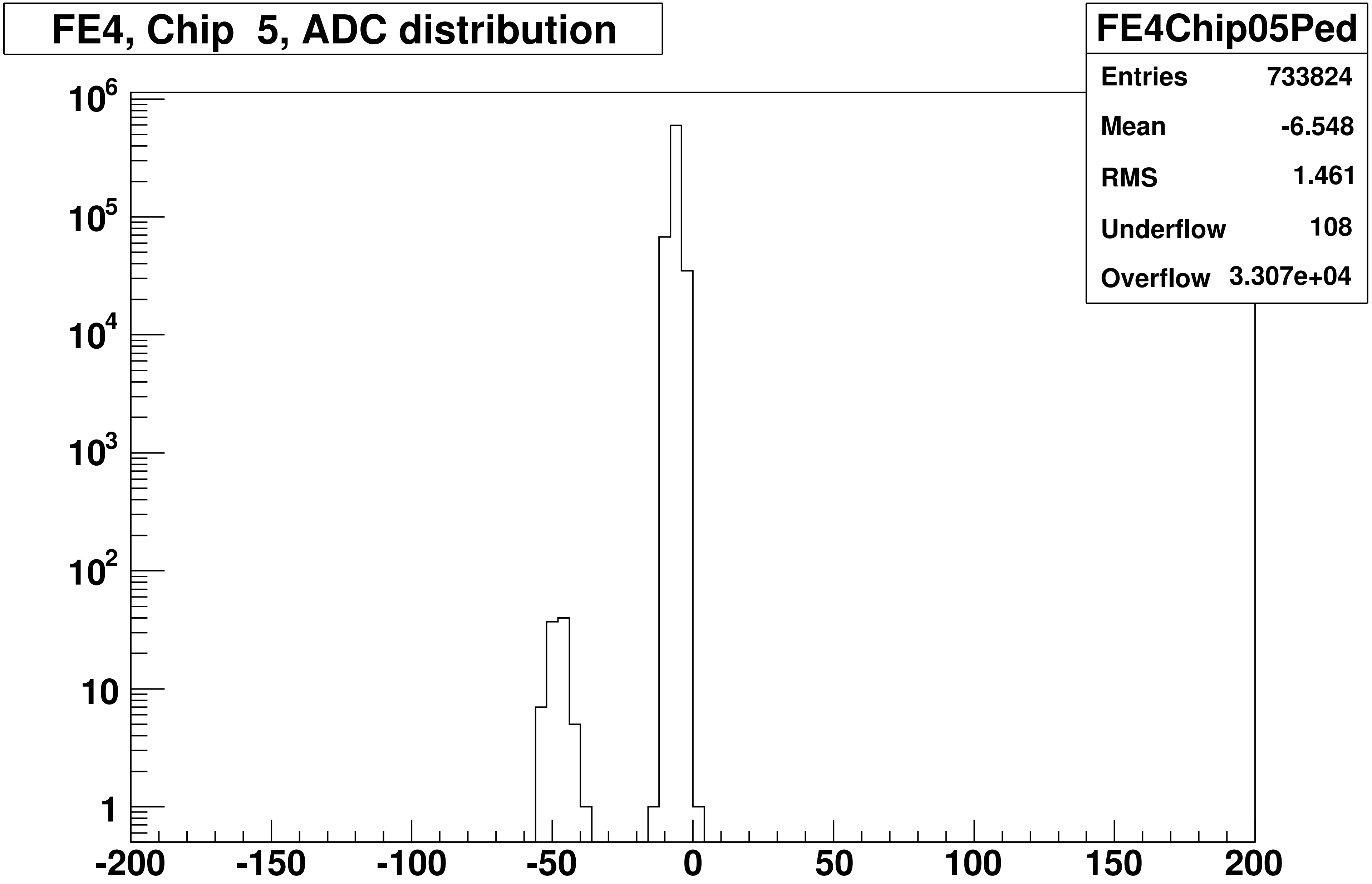
20000
25000



FE4, Chip 5, ADC distribution
FE4Chip05Ped
Entries 733824
Mean -6.548
RMS 1.461
Underflow 108
Overflow 3.307e+04
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10^3
10^2
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150
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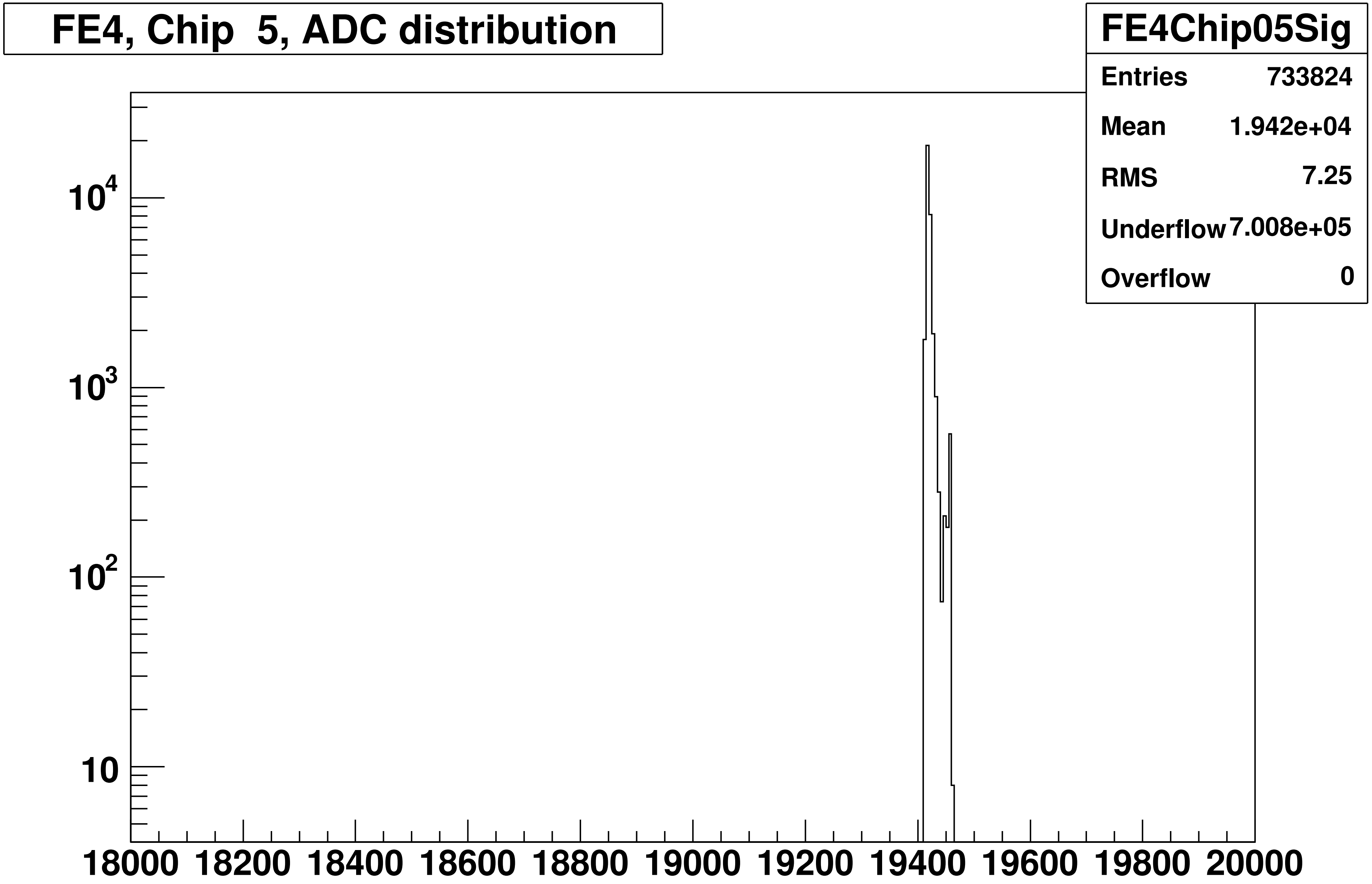

FE4, Chip 5, ADC distribution
FE4Chip05Sig
Entries 733824
Mean 1.942e+04
RMS 7.25
Underflow 7.008e+05
Overflow 0
10^4
10^3
10^2
10
18000
18200
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19000
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19800
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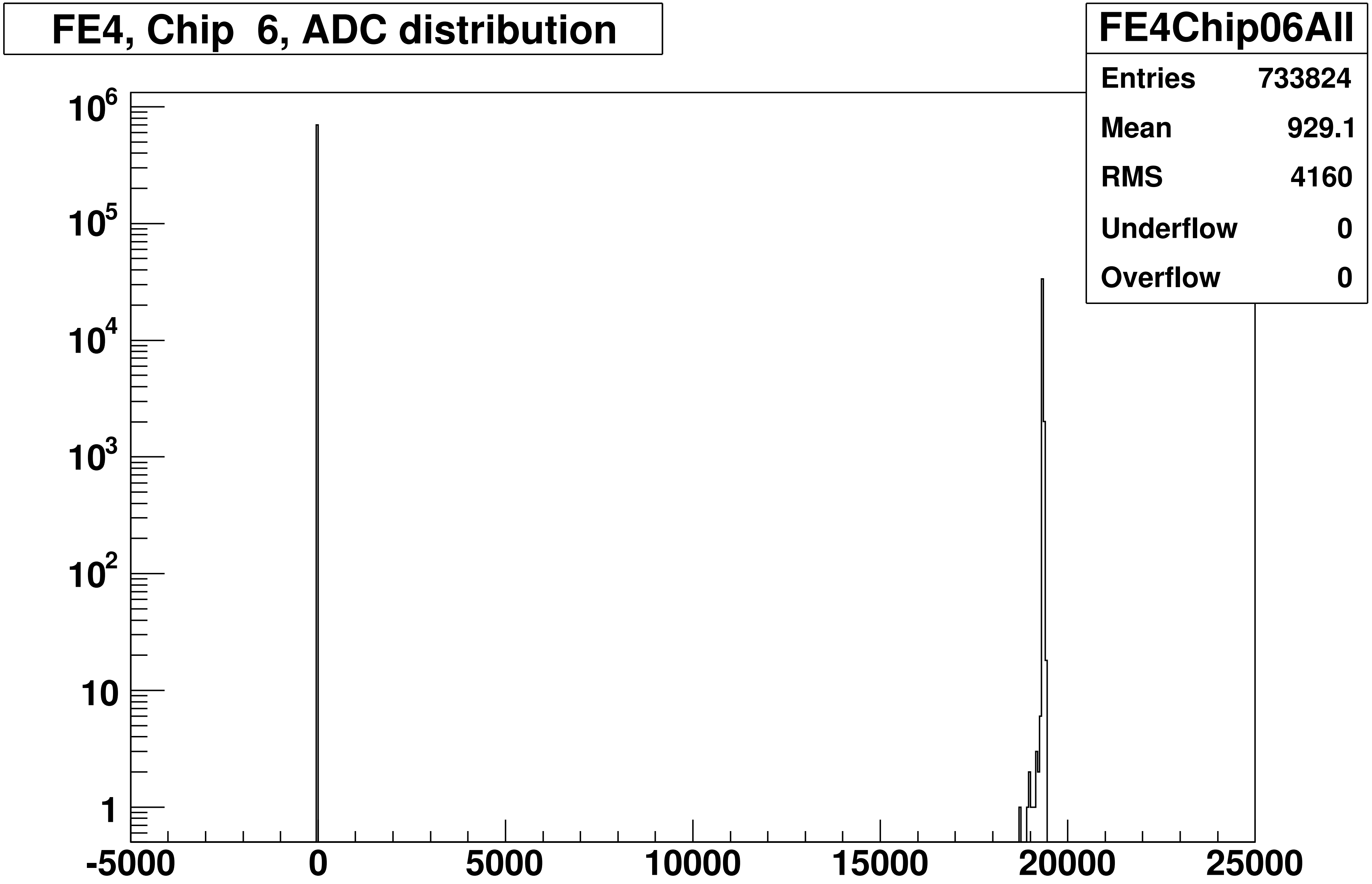

FE4, Chip 6, ADC distribution
FE4Chip06All
Entries 733824
Mean 929.1
RMS 4160
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
1
-5000
0
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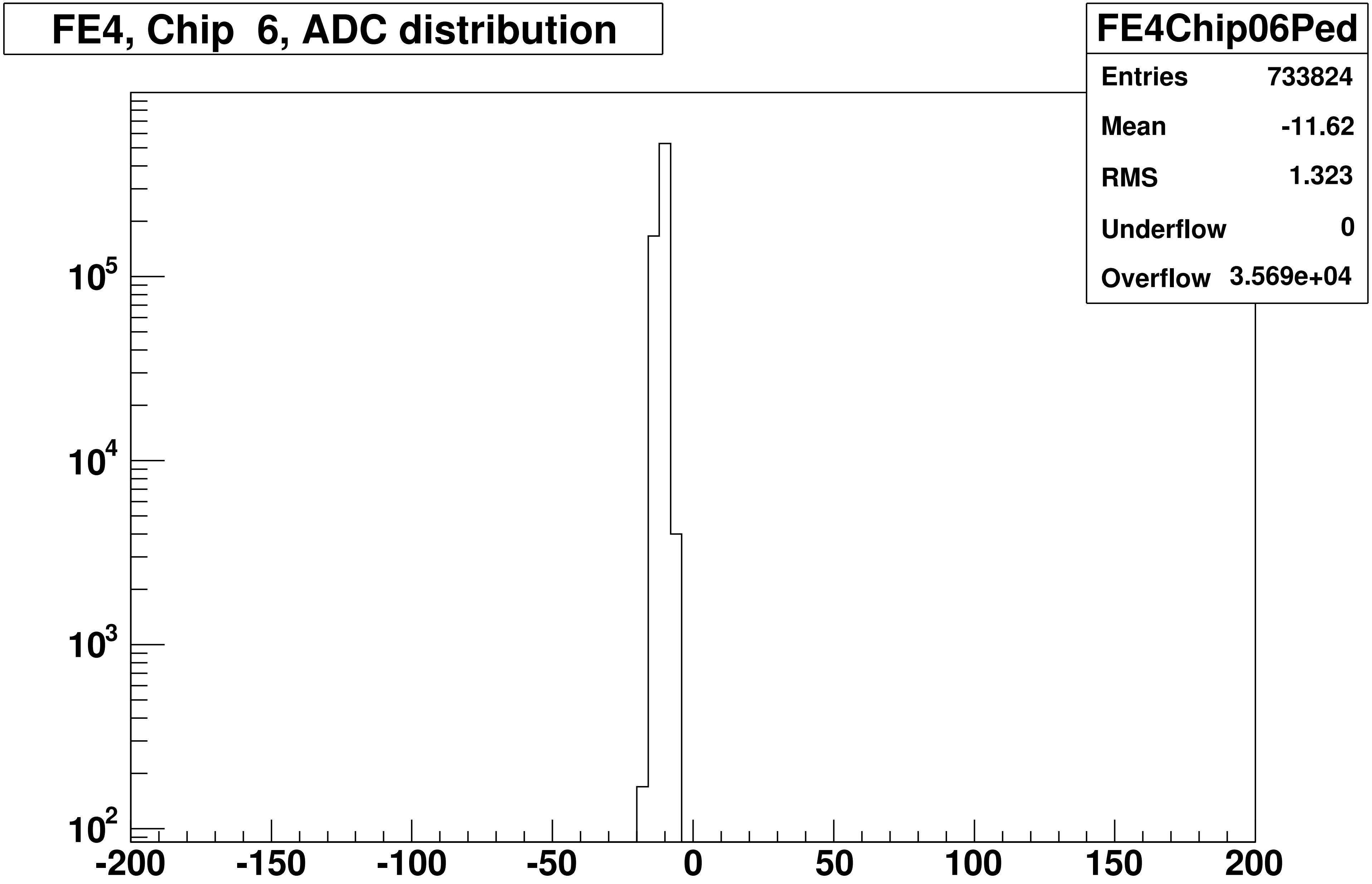
10000
15000
20000
25000



FE4, Chip 6, ADC distribution
FE4Chip06Ped
Entries 733824
Mean -11.62
RMS 1.323
Underflow 0
Overflow 3.569e+04
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10^4
10^3
10^2
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-100
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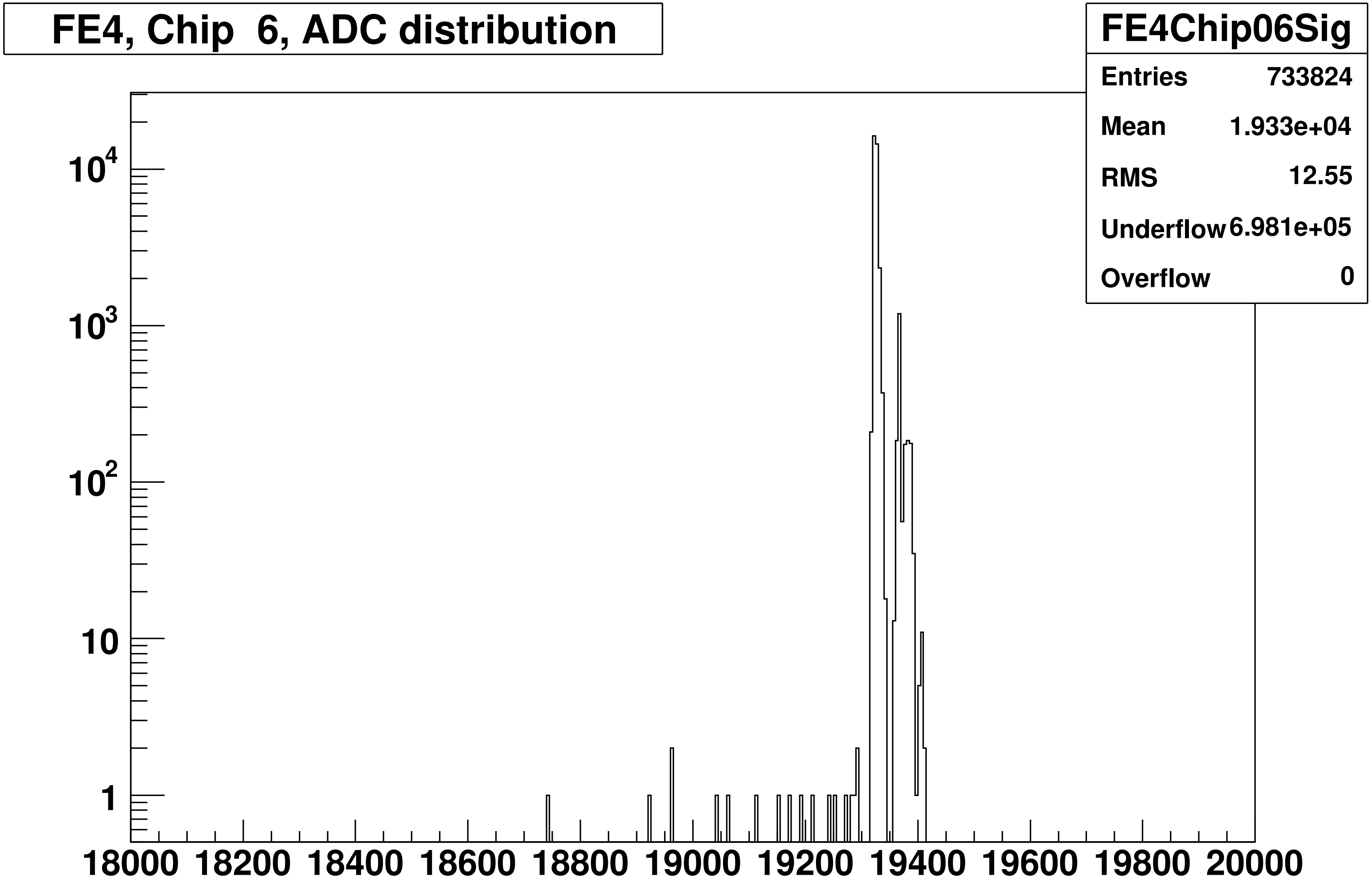
0
50
100
150
200



FE4, Chip 6, ADC distribution
FE4Chip06Sig
Entries 733824
Mean 1.933e+04
RMS 12.55
Underflow 6.981e+05
Overflow 0
10^4
10^3
10^2
10
1
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18200
18400
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19000
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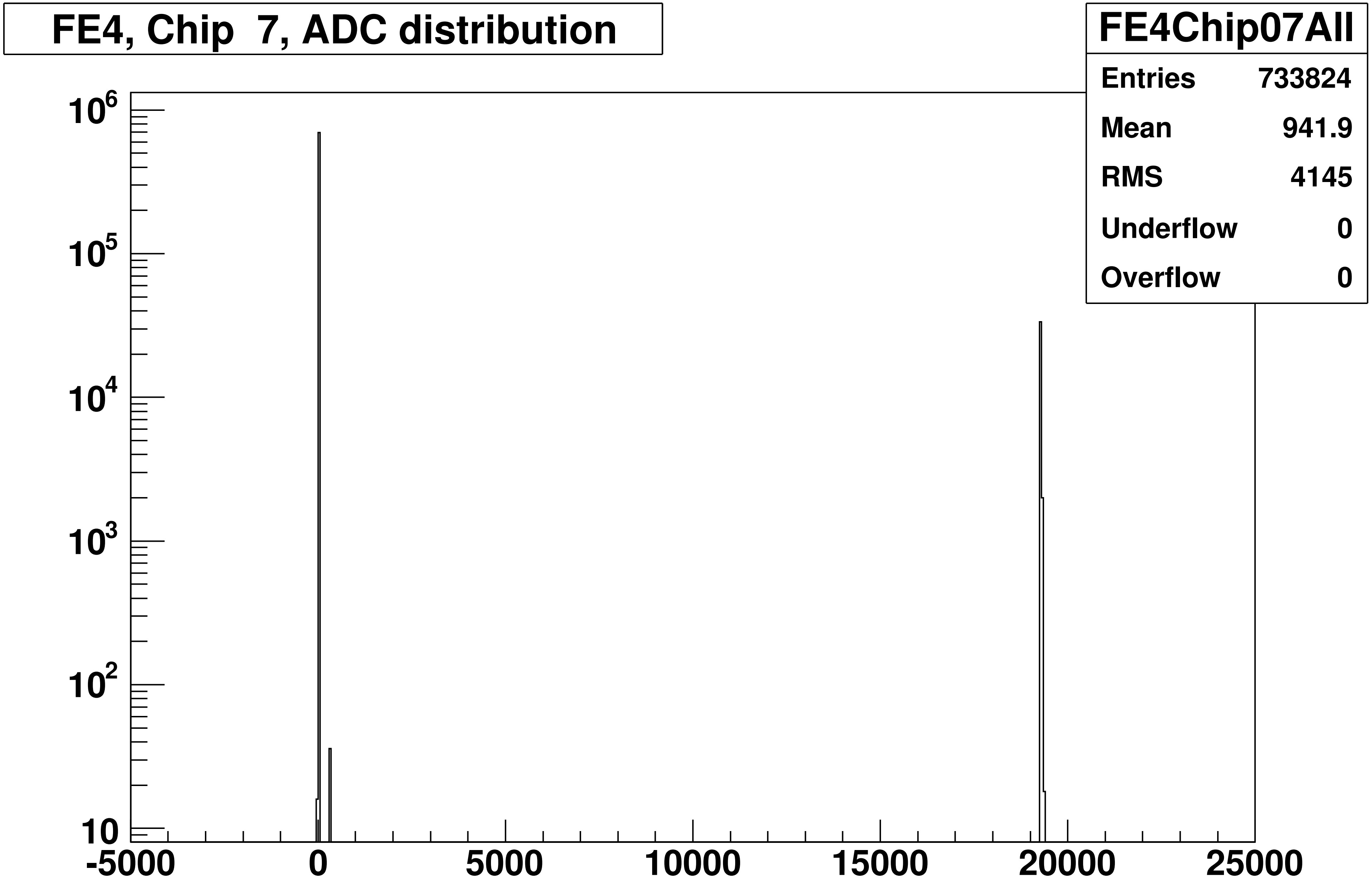
19800
20000


FE4, Chip 7, ADC distribution
FE4Chip07All
Entries 733824
Mean 941.9
RMS 4145
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
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-5000
0
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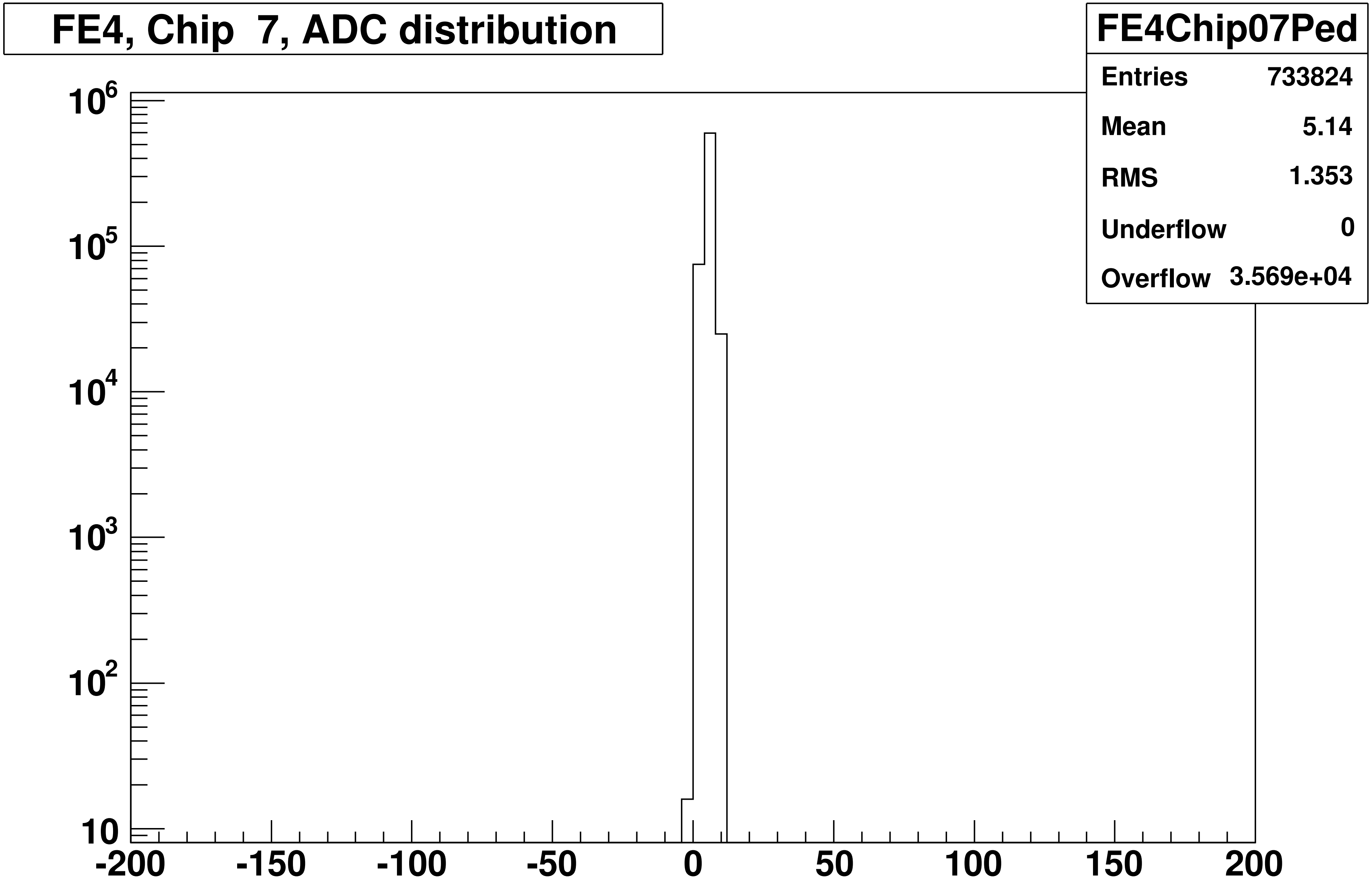
15000
20000
25000


FE4, Chip 7, ADC distribution
FE4Chip07Ped
Entries 733824
Mean 5.14
RMS 1.353
Underflow 0
Overflow 3.569e+04
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10^2
10^3
10^4
10^5
10^6
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-100
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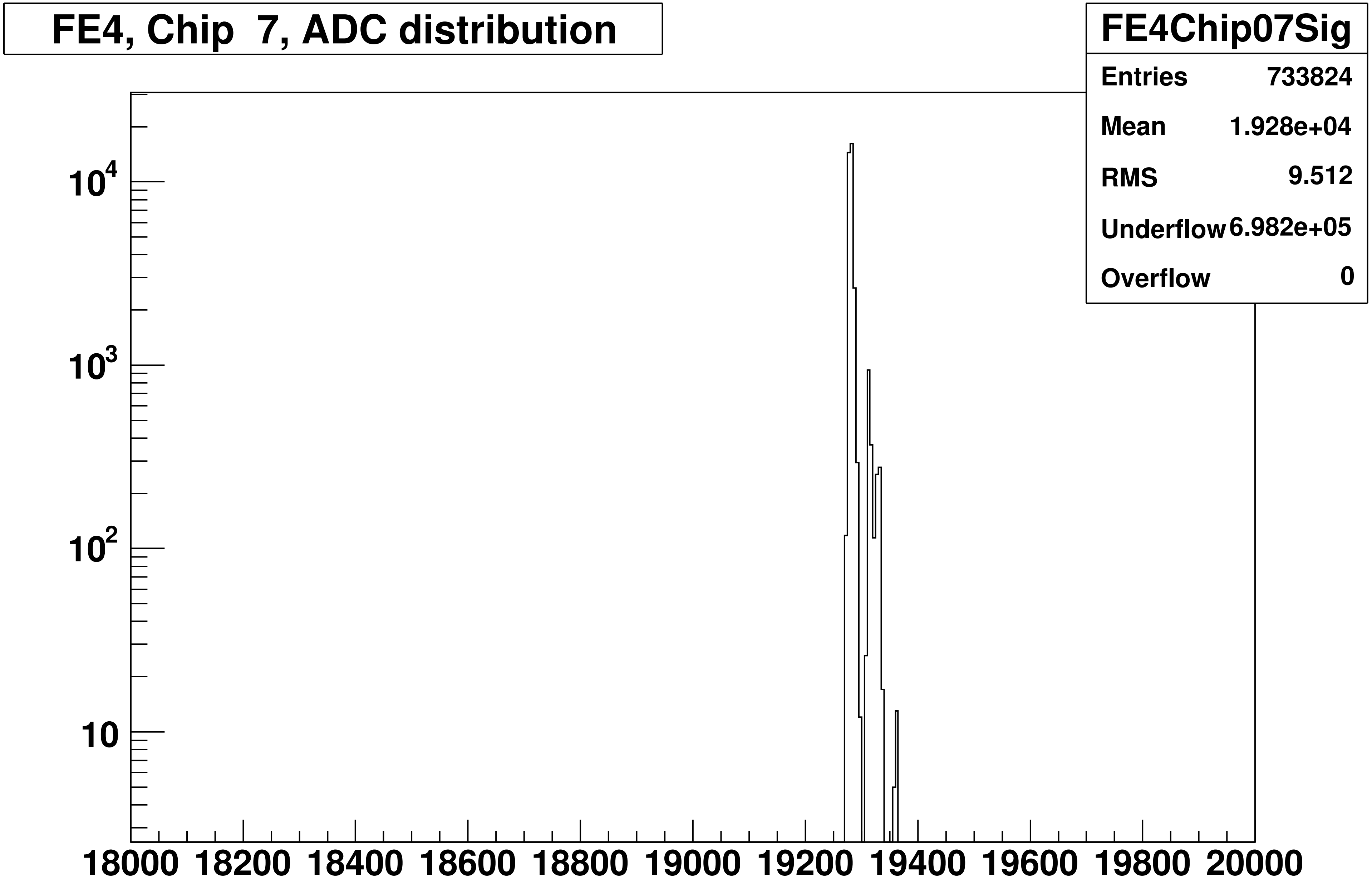
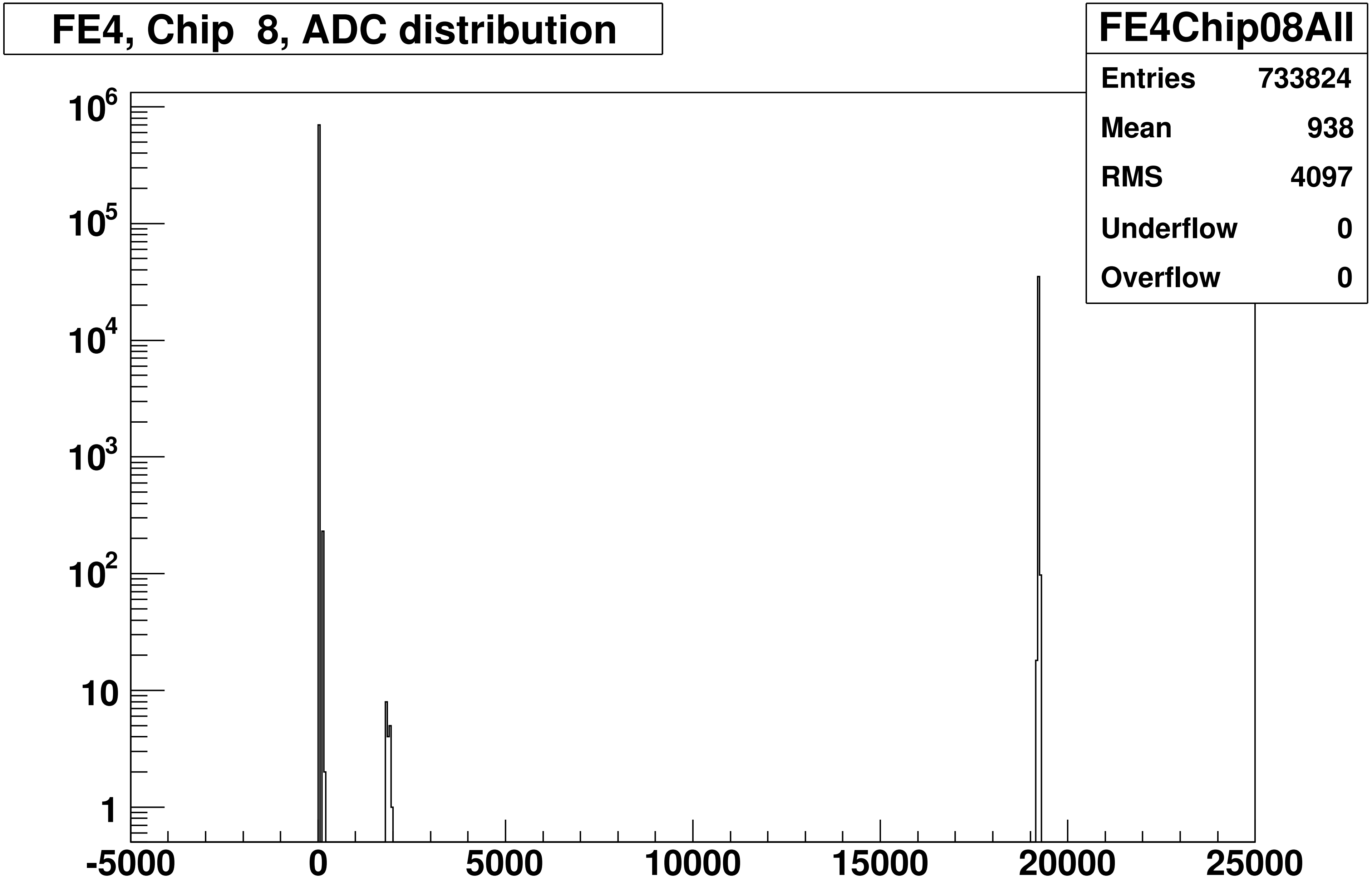
0
50
100
150
200



FE4, Chip 7, ADC distribution
FE4Chip07Sig
Entries 733824
Mean 1.928e+04
RMS 9.512
Underflow 6.982e+05
Overflow 0
10^4
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE4, Chip 8, ADC distribution
FE4Chip08All
Entries 733824
Mean 938
RMS 4097
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
1
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0
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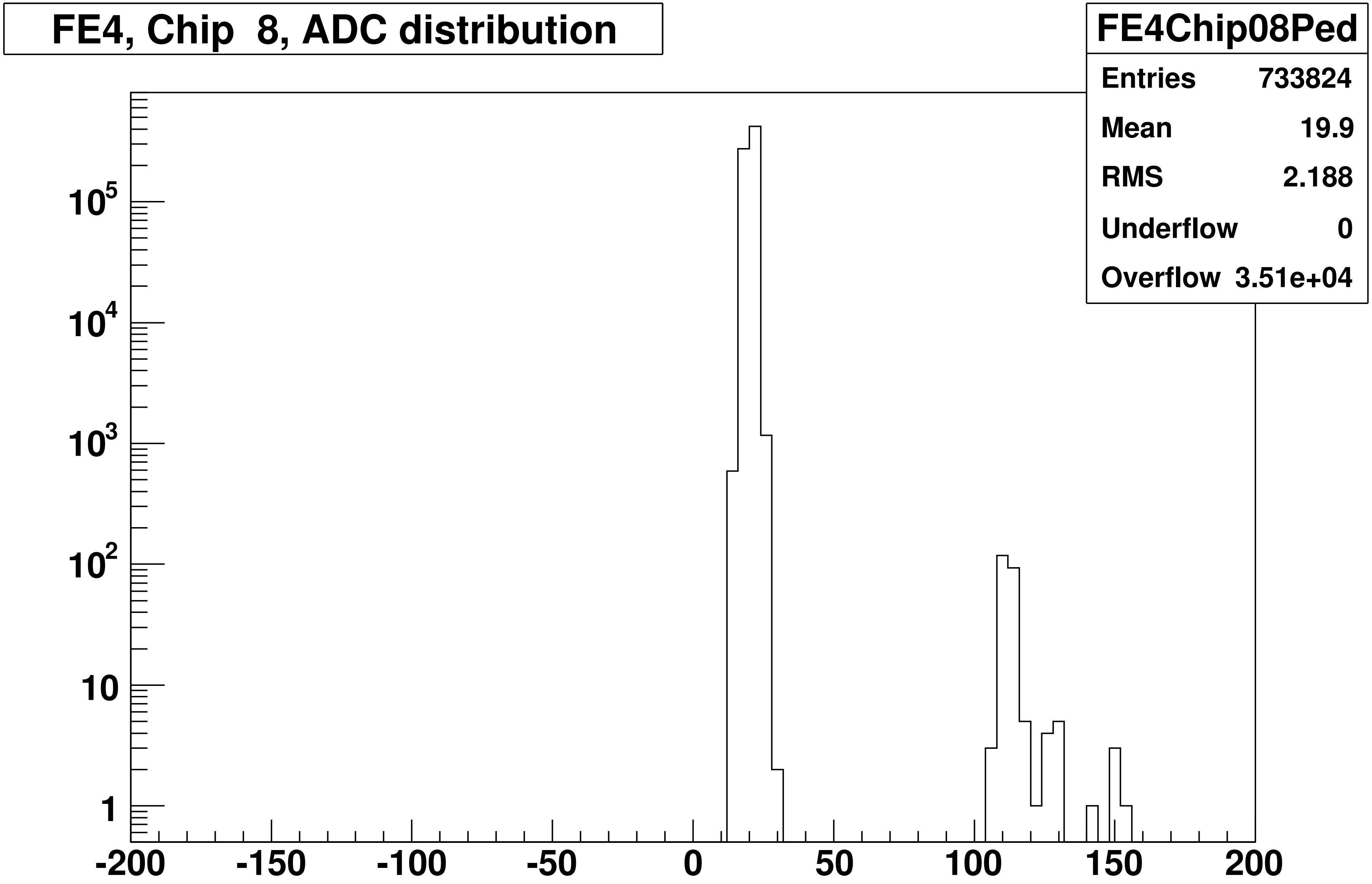
10000
15000
20000
25000


FE4, Chip 8, ADC distribution
FE4Chip08Ped
Entries 733824
Mean 19.9
RMS 2.188
Underflow 0
Overflow 3.51e+04
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10^3
10^2
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-100
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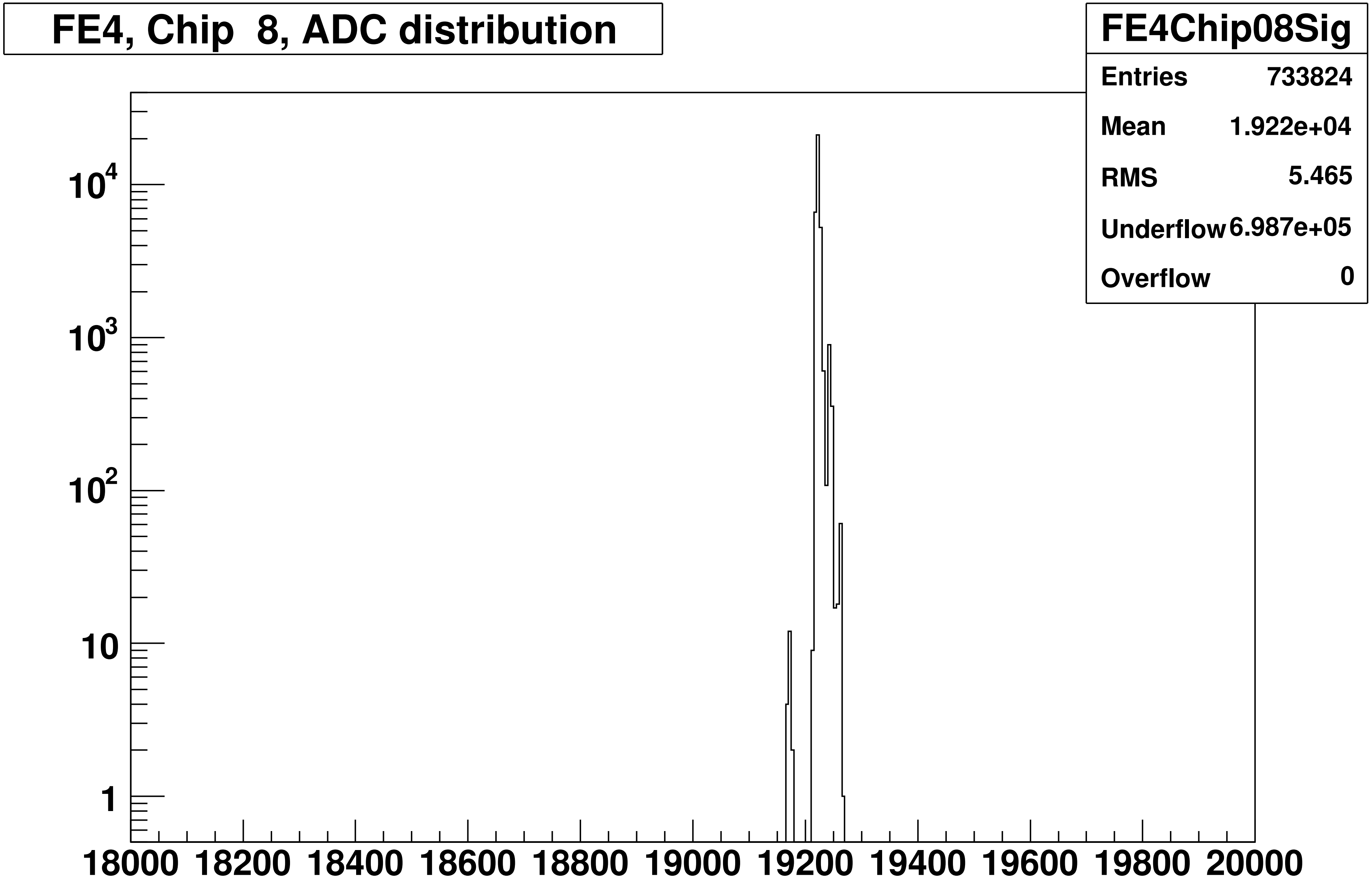
0
50
100
150
200



FE4, Chip 8, ADC distribution
FE4Chip08Sig
Entries 733824
Mean 1.922e+04
RMS 5.465
Underflow 6.987e+05
Overflow 0
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10^3
10^2
10
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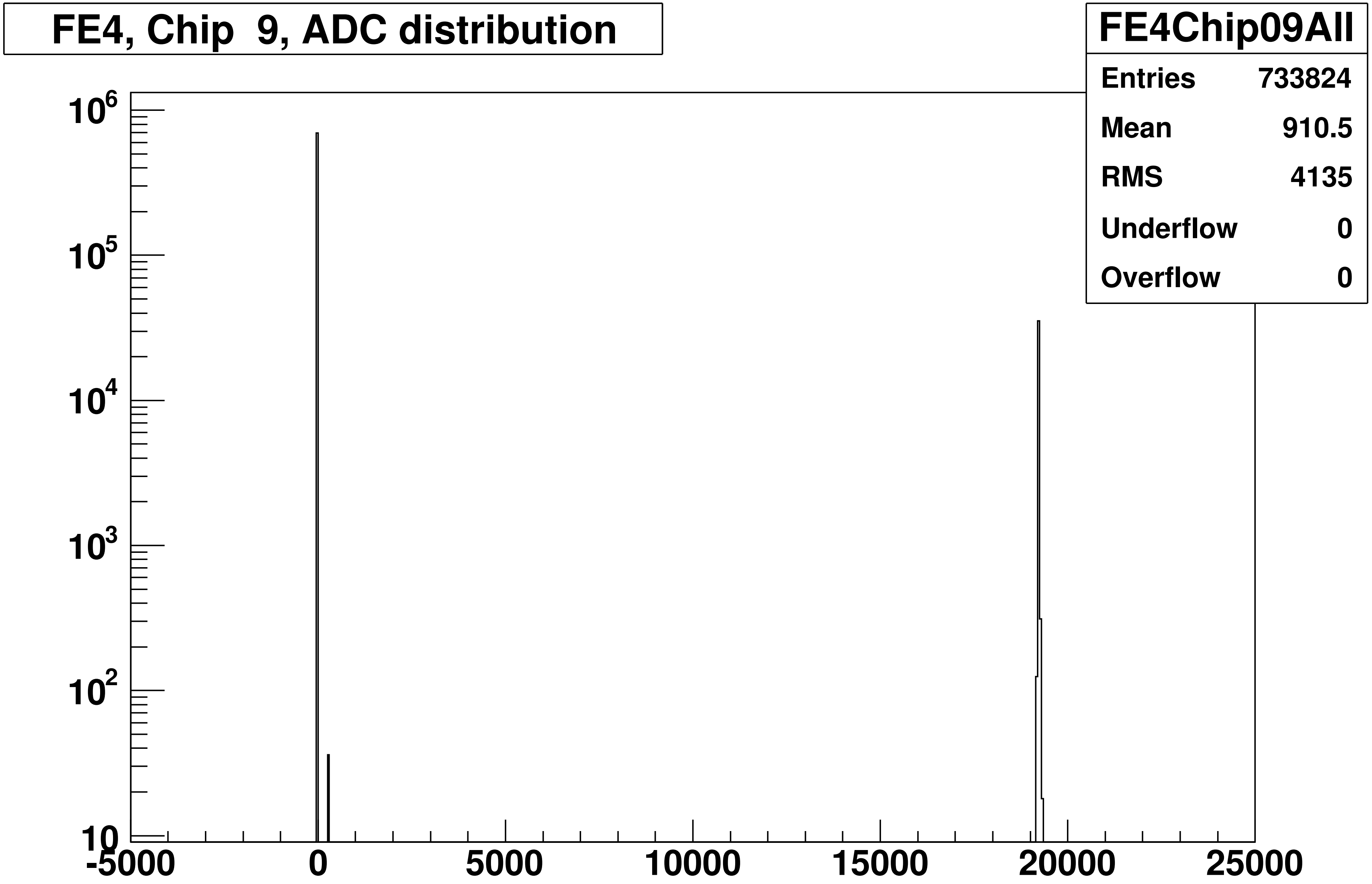
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE4, Chip 9, ADC distribution
FE4Chip09All
Entries 733824
Mean 910.5
RMS 4135
Underflow 0
Overflow 0
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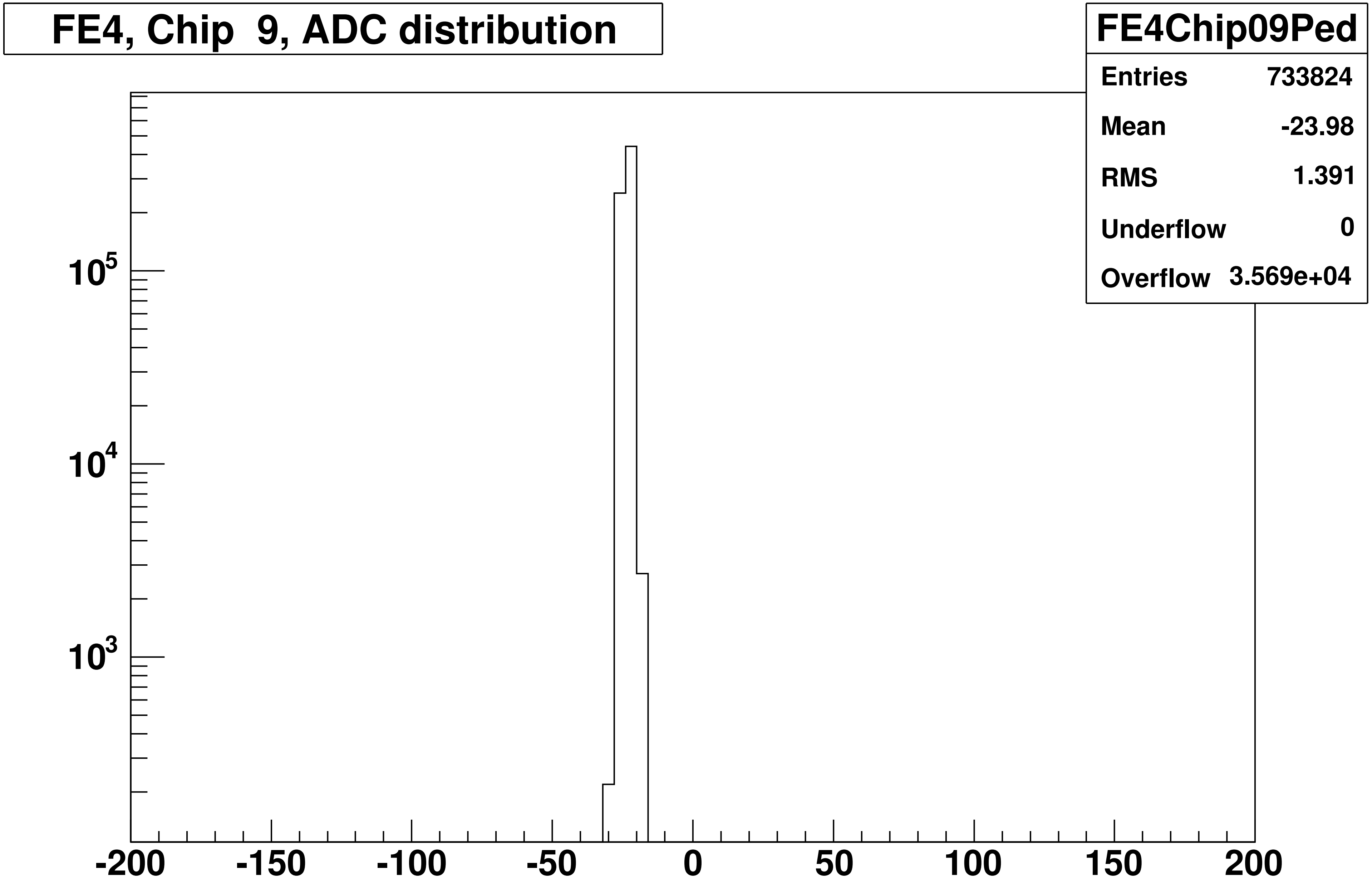
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000



FE4, Chip 9, ADC distribution
FE4Chip09Ped
Entries 733824
Mean -23.98
RMS 1.391
Underflow 0
Overflow 3.569e+04
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10^4
10^3
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0
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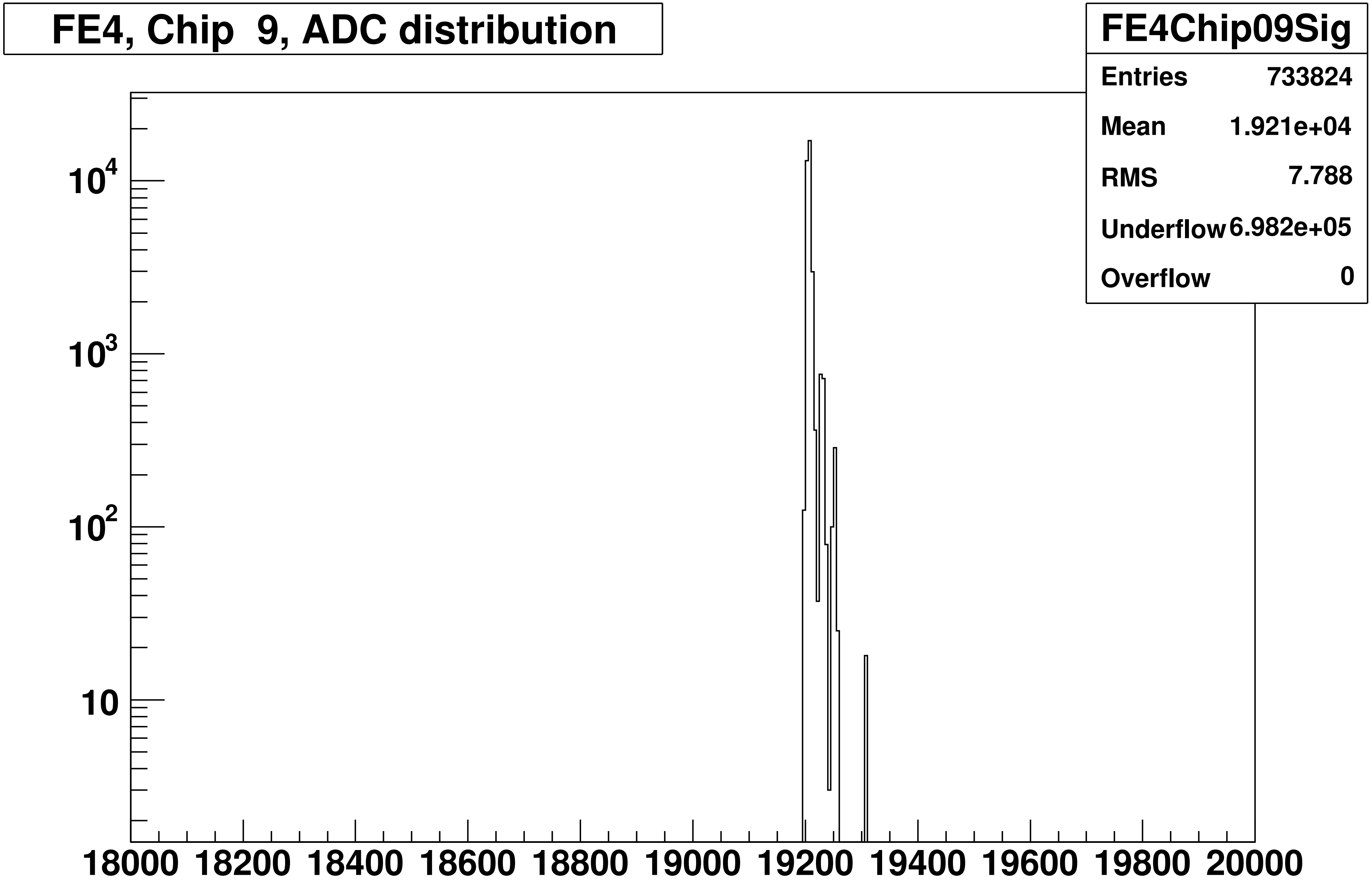
100
150
200



FE4, Chip 9, ADC distribution
FE4Chip09Sig
Entries 733824
Mean 1.921e+04
RMS 7.788
Underflow 6.982e+05
Overflow 0
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10^3
10^2
10
18000
18200
18400
18600
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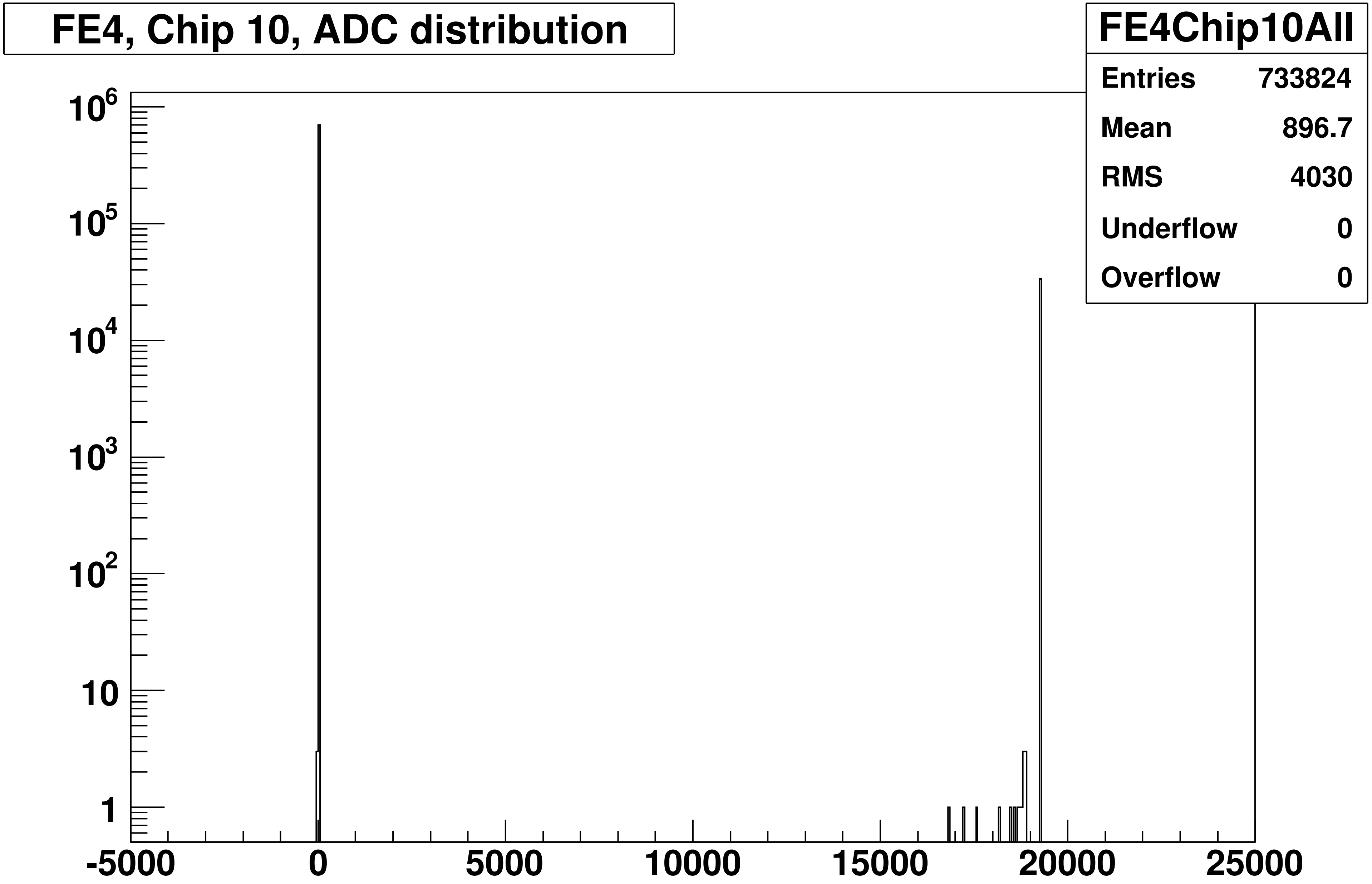
19600
19800
20000



FE4, Chip 10, ADC distribution
FE4Chip10All
Entries 733824
Mean 896.7
RMS 4030
Underflow 0
Overflow 0
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10^4
10^3
10^2
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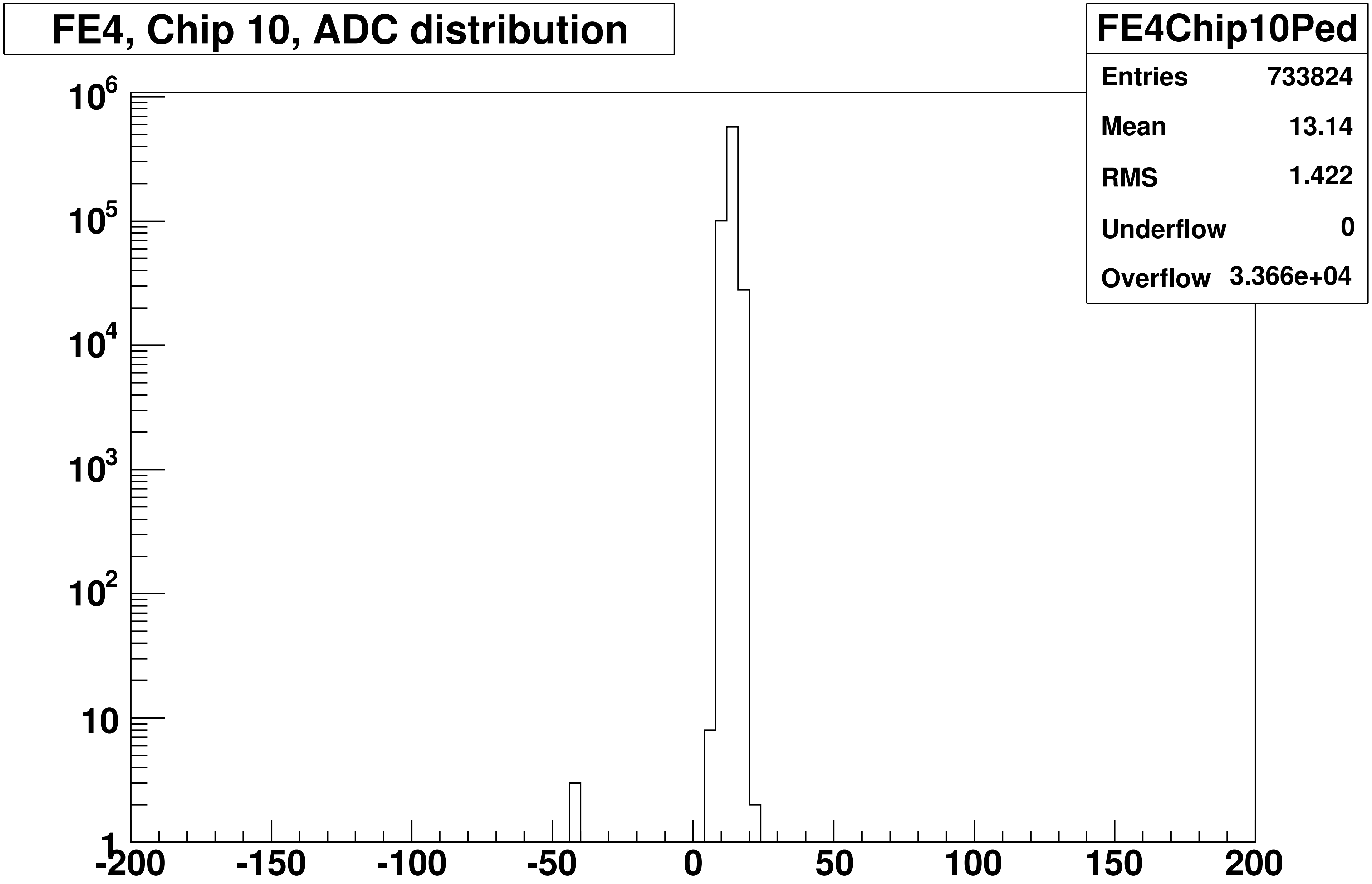
FE4, Chip 10, ADC distribution
FE4Chip10Ped
Entries 733824
Mean 13.14
RMS 1.422
Underflow 0
Overflow 3.366e+04
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10^3
10^2
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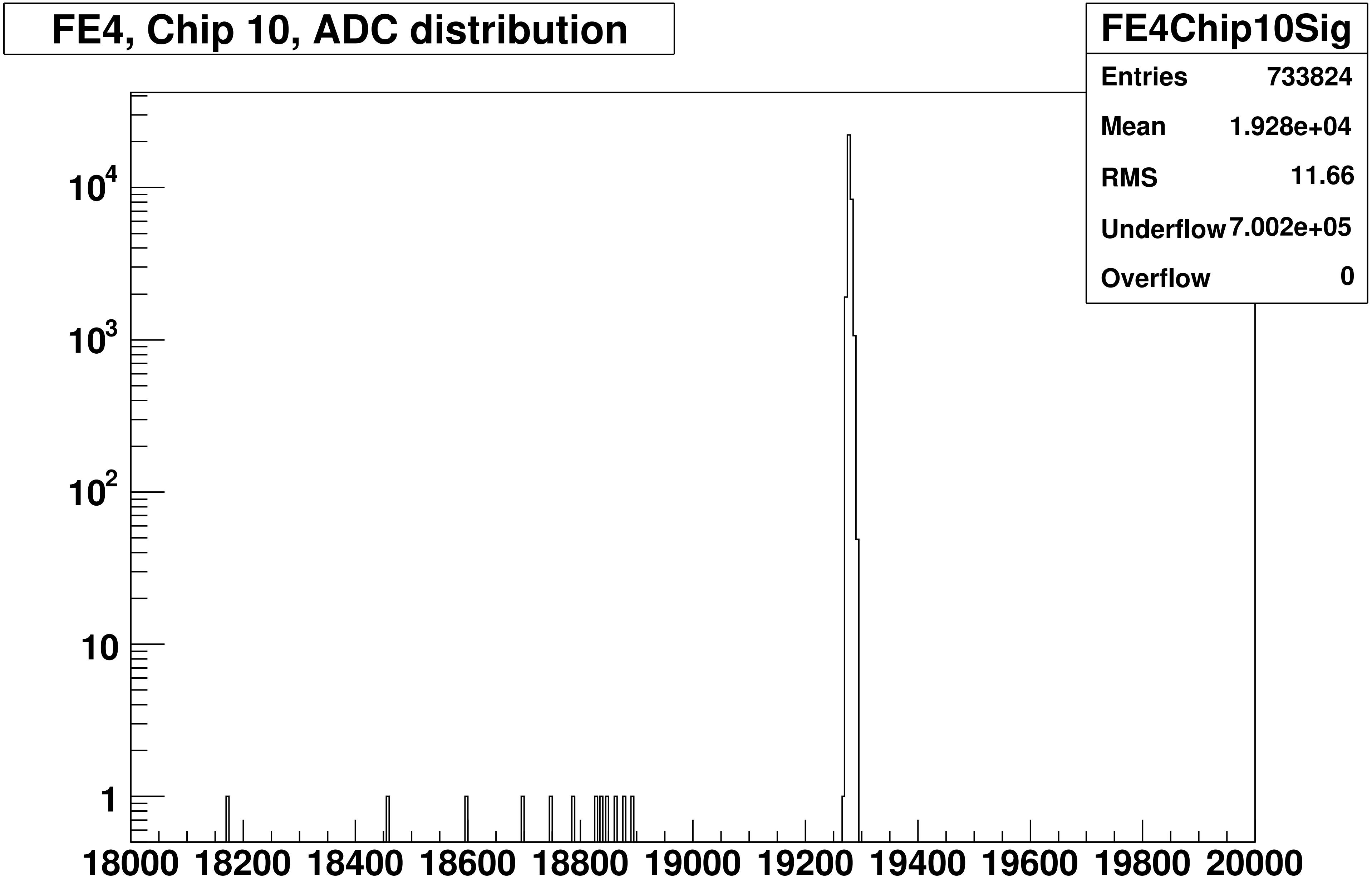
150
200


FE4, Chip 10, ADC distribution
FE4Chip10Sig
Entries 733824
Mean 1.928e+04
RMS 11.66
Underflow 7.002e+05
Overflow 0
10^4
10^3
10^2
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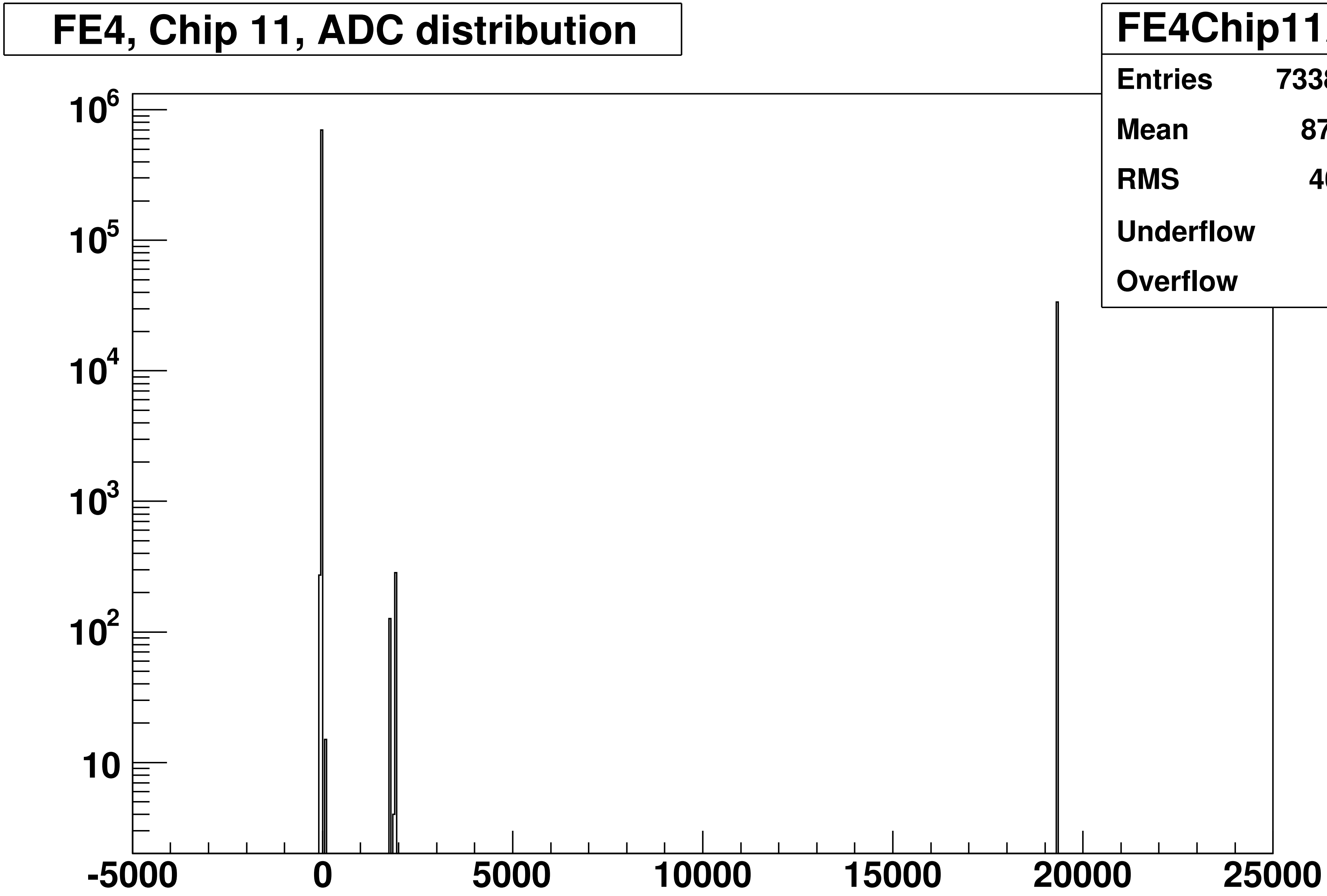
FE4, Chip 11, ADC distribution
FE4Chip11All
Entries 733824
Mean 877.8
RMS 4043
Underflow 0
Overflow 0
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10^4
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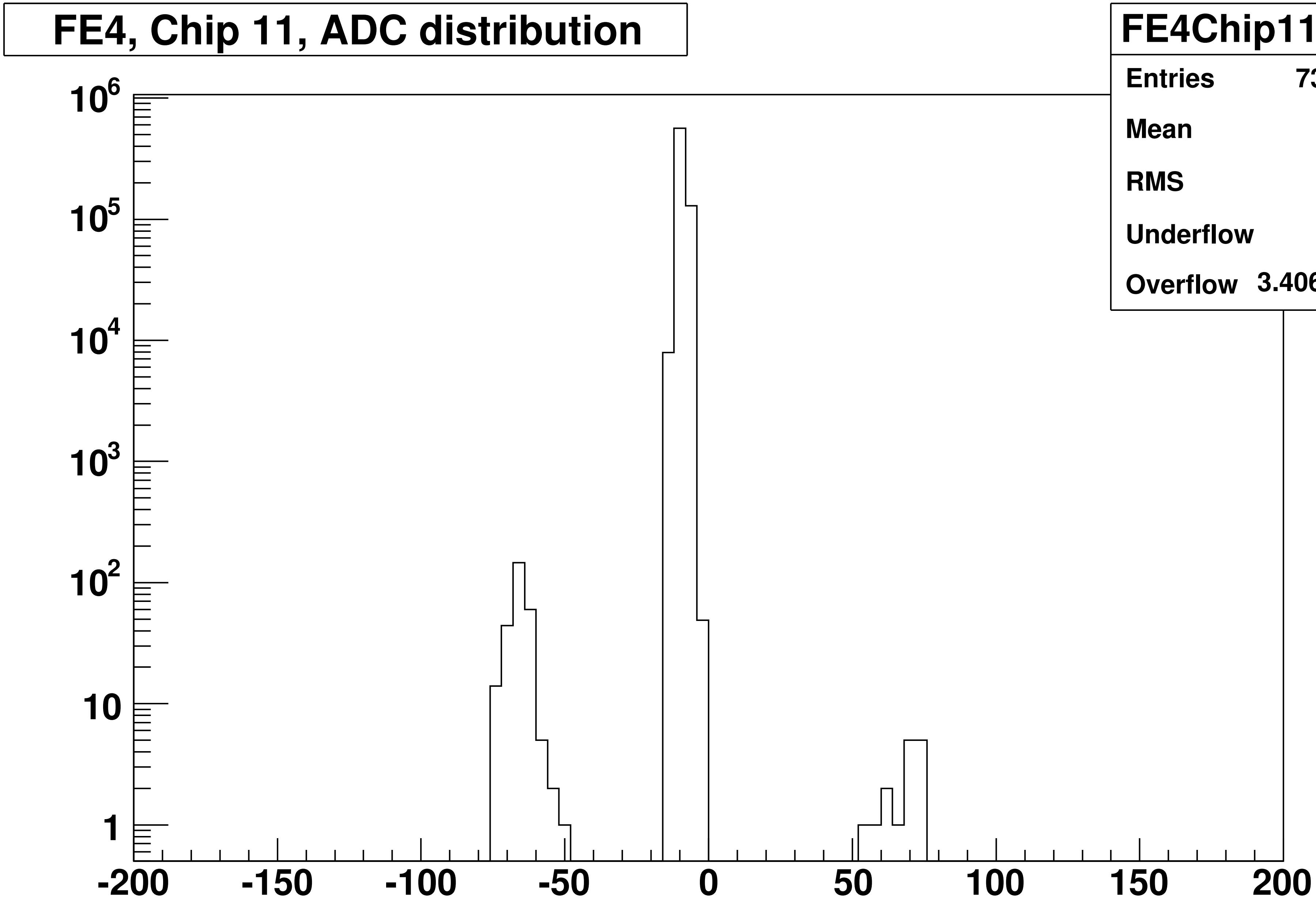
FE4, Chip 11, ADC distribution
FE4Chip11Ped
Entries 733824
Mean -9.47
RMS 1.761
Underflow 0
Overflow 3.406e+04
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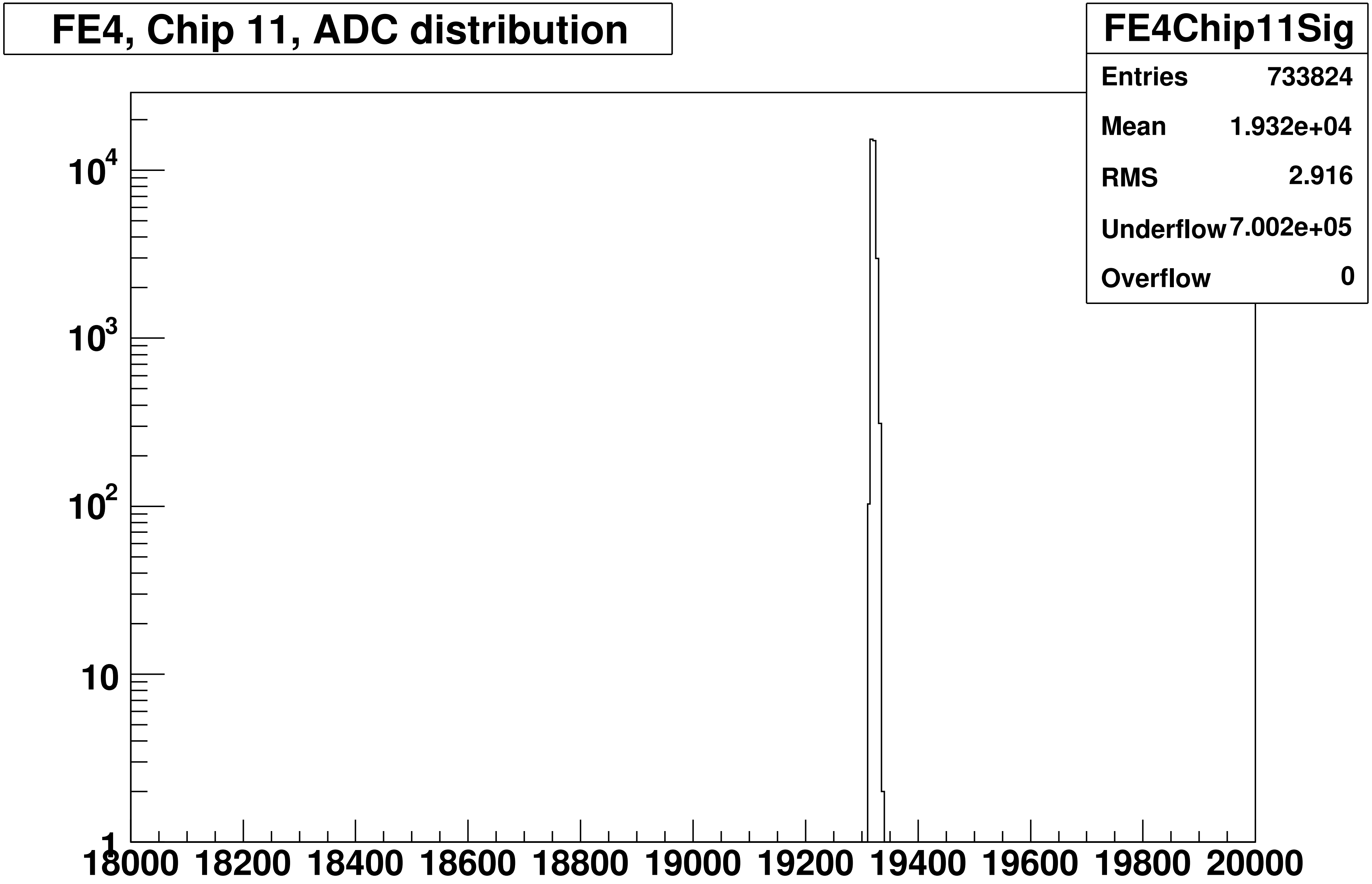
FE4, Chip 11, ADC distribution
FE4Chip11Sig
Entries 733824
Mean 1.932e+04
RMS 2.916
Underflow 7.002e+05
Overflow 0
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10^3
10^2
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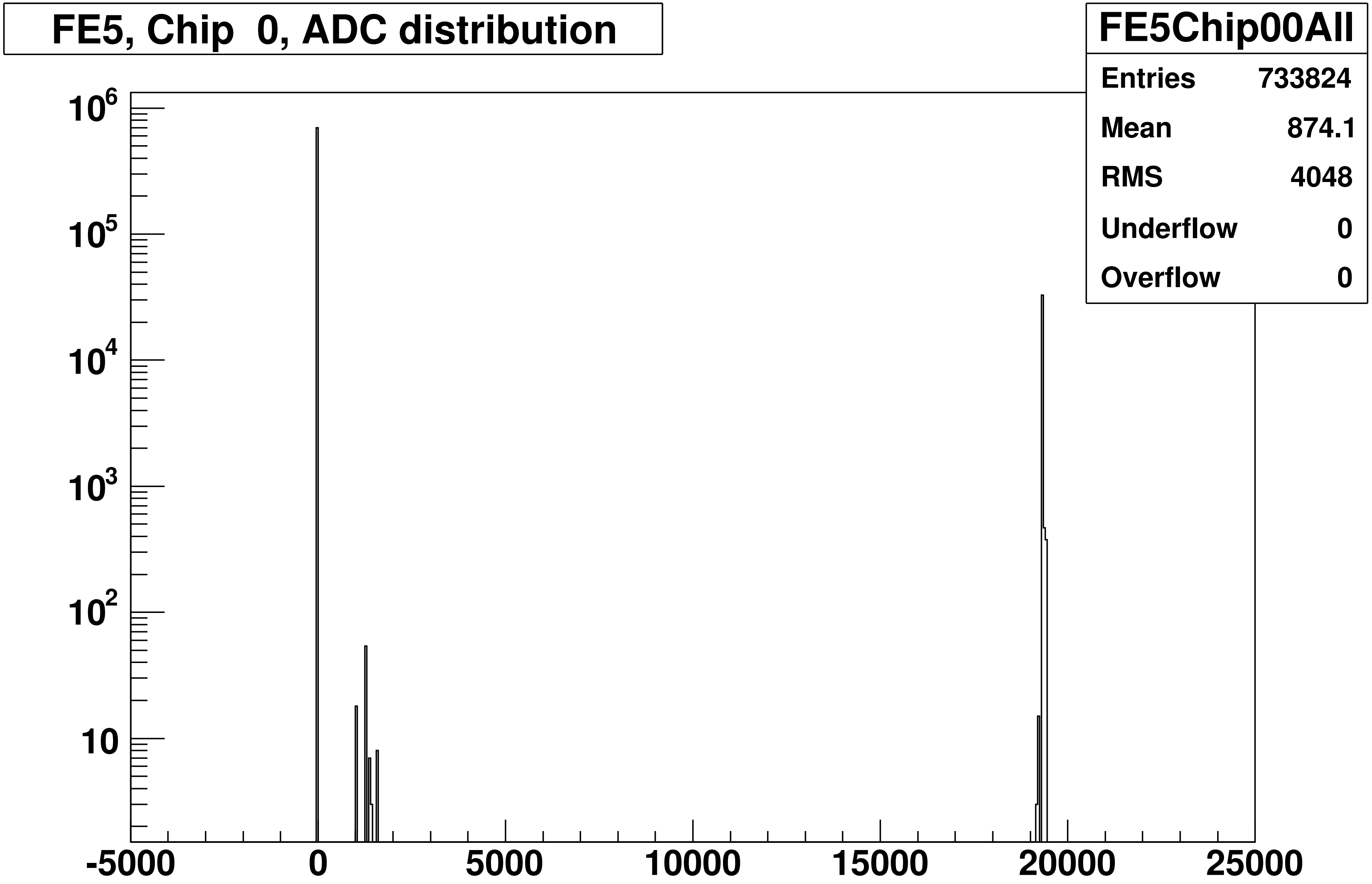

FE5, Chip 0, ADC distribution
FE5Chip00All
Entries 733824
Mean 874.1
RMS 4048
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
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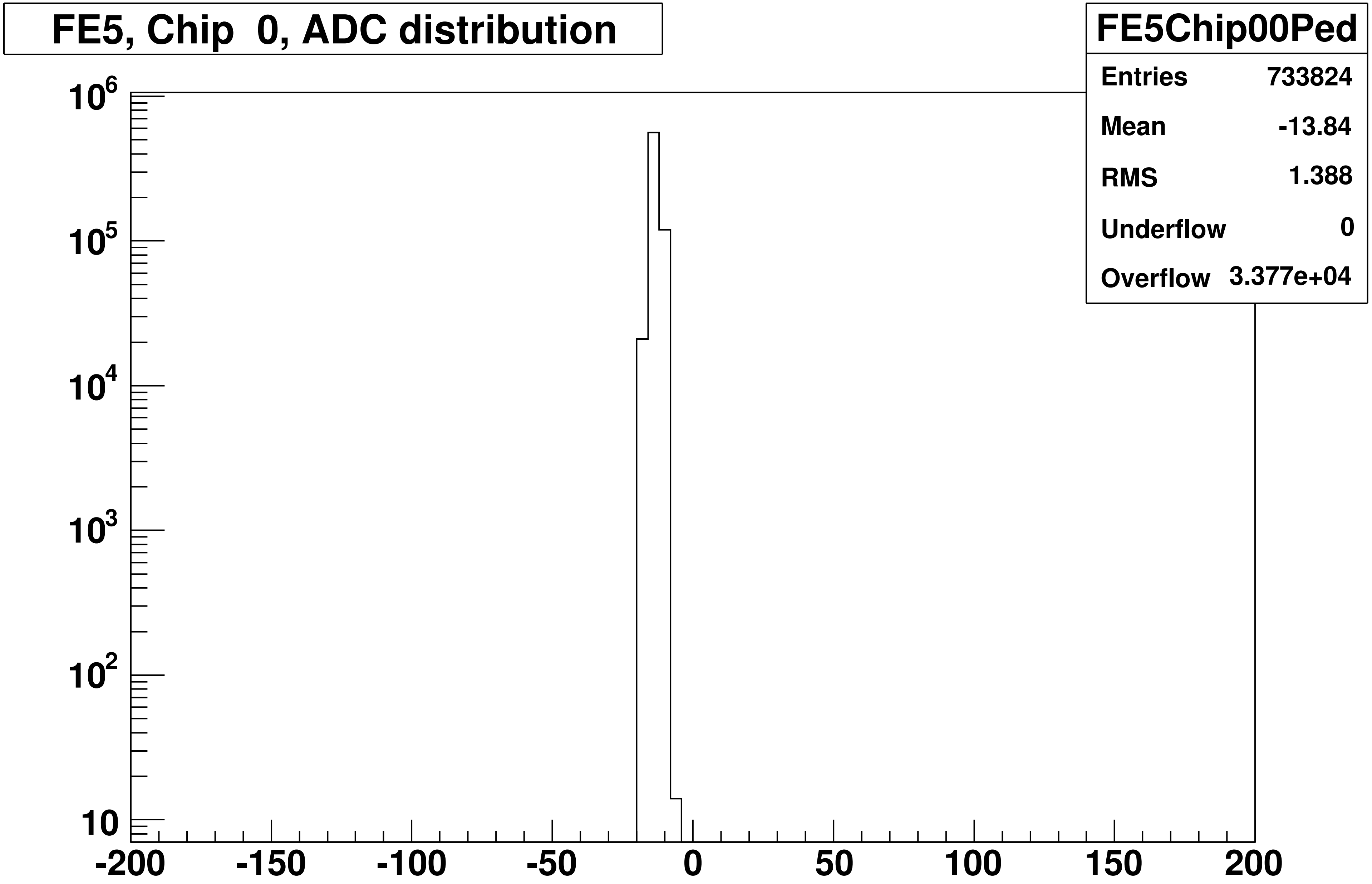

FE5, Chip 0, ADC distribution
FE5Chip00Ped
Entries 733824
Mean -13.84
RMS 1.388
Underflow 0
Overflow 3.377e+04
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10^4
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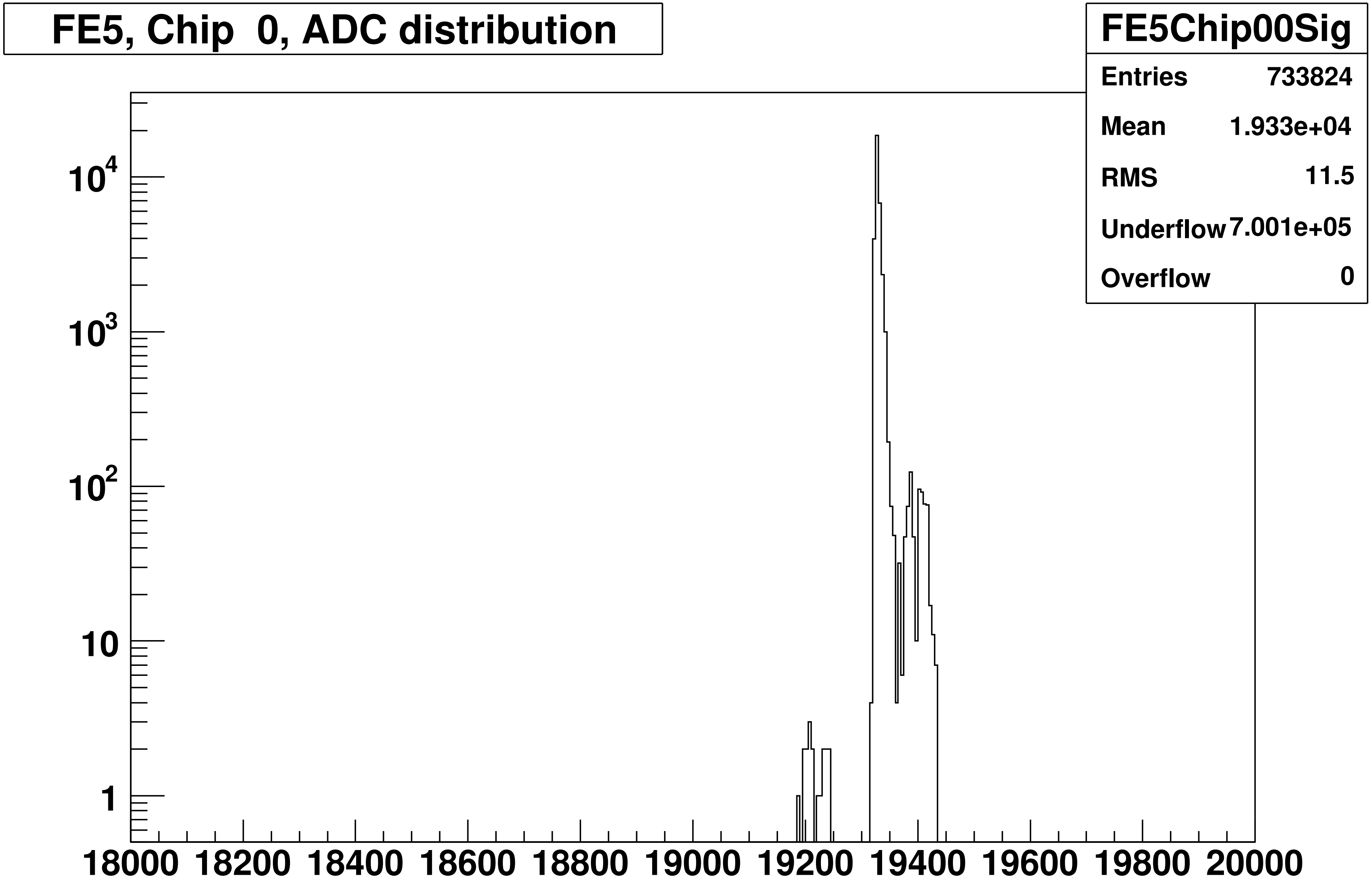

FE5, Chip 0, ADC distribution
FE5Chip00Sig
Entries 733824
Mean 1.933e+04
RMS 11.5
Underflow 7.001e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
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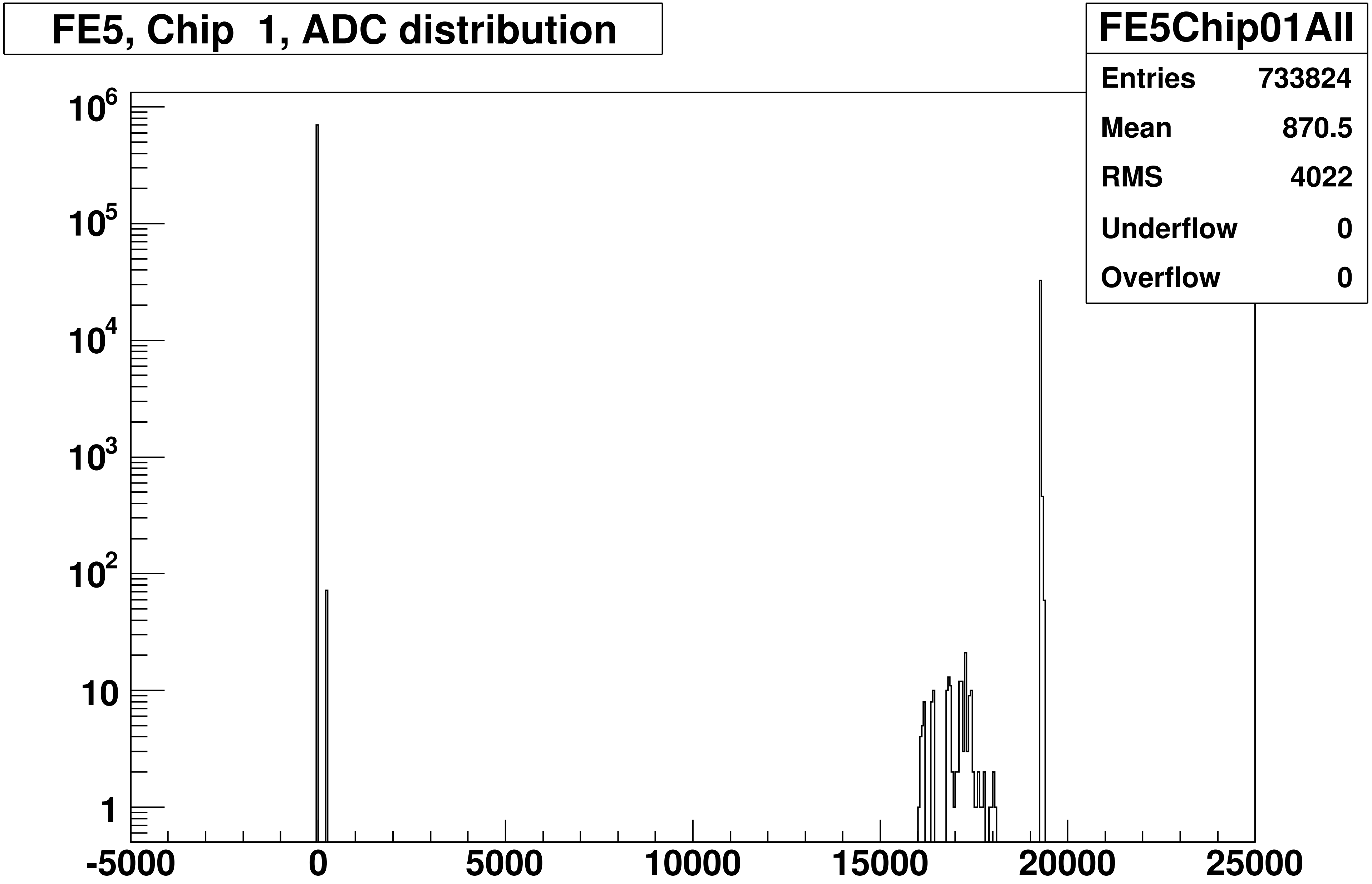
FE5, Chip 1, ADC distribution
FE5Chip01All
Entries 733824
Mean 870.5
RMS 4022
Underflow 0
Overflow 0
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10^4
10^3
10^2
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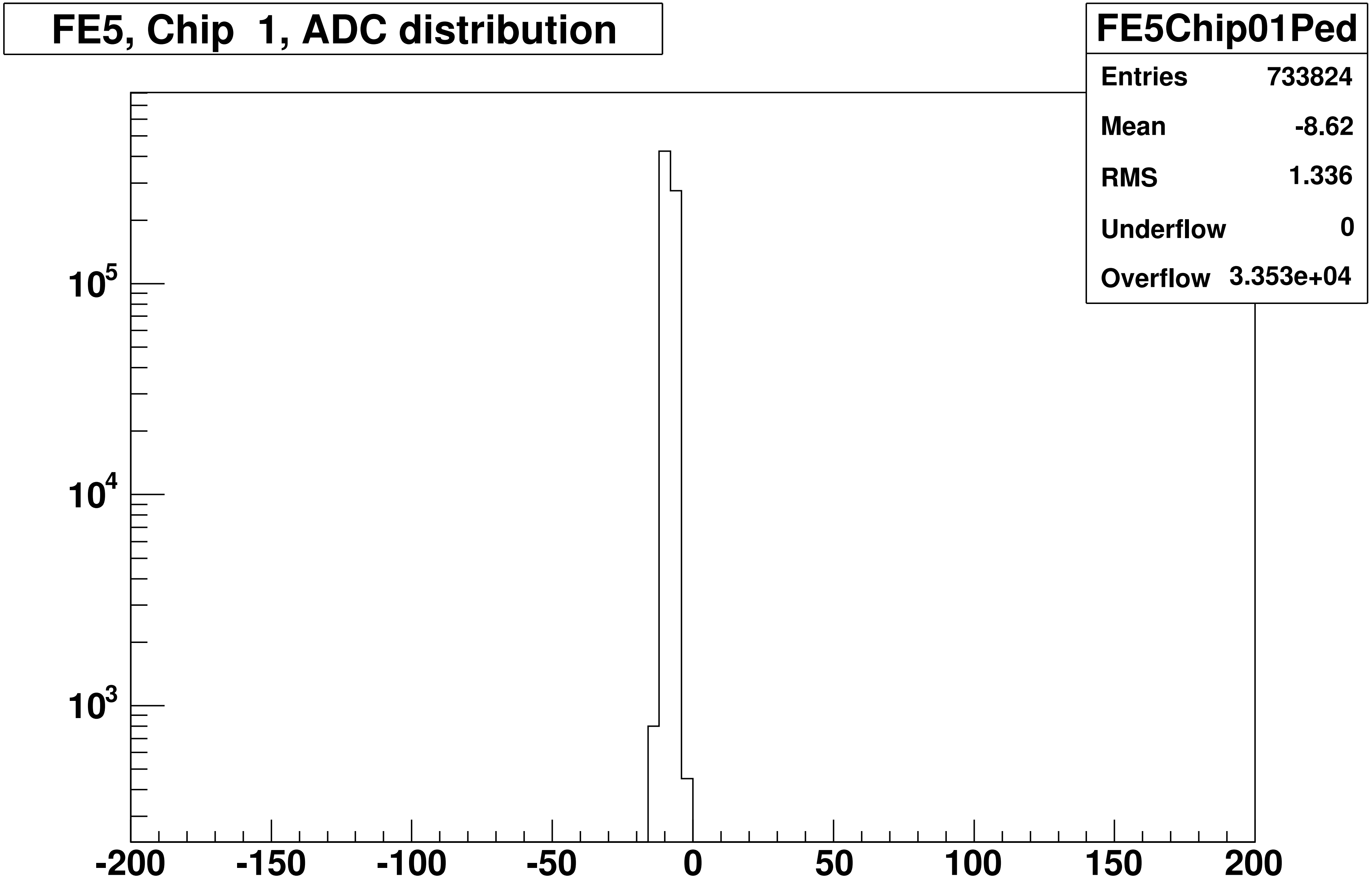

FE5, Chip 1, ADC distribution
FE5Chip01Ped
Entries 733824
Mean -8.62
RMS 1.336
Underflow 0
Overflow 3.353e+04
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10^3
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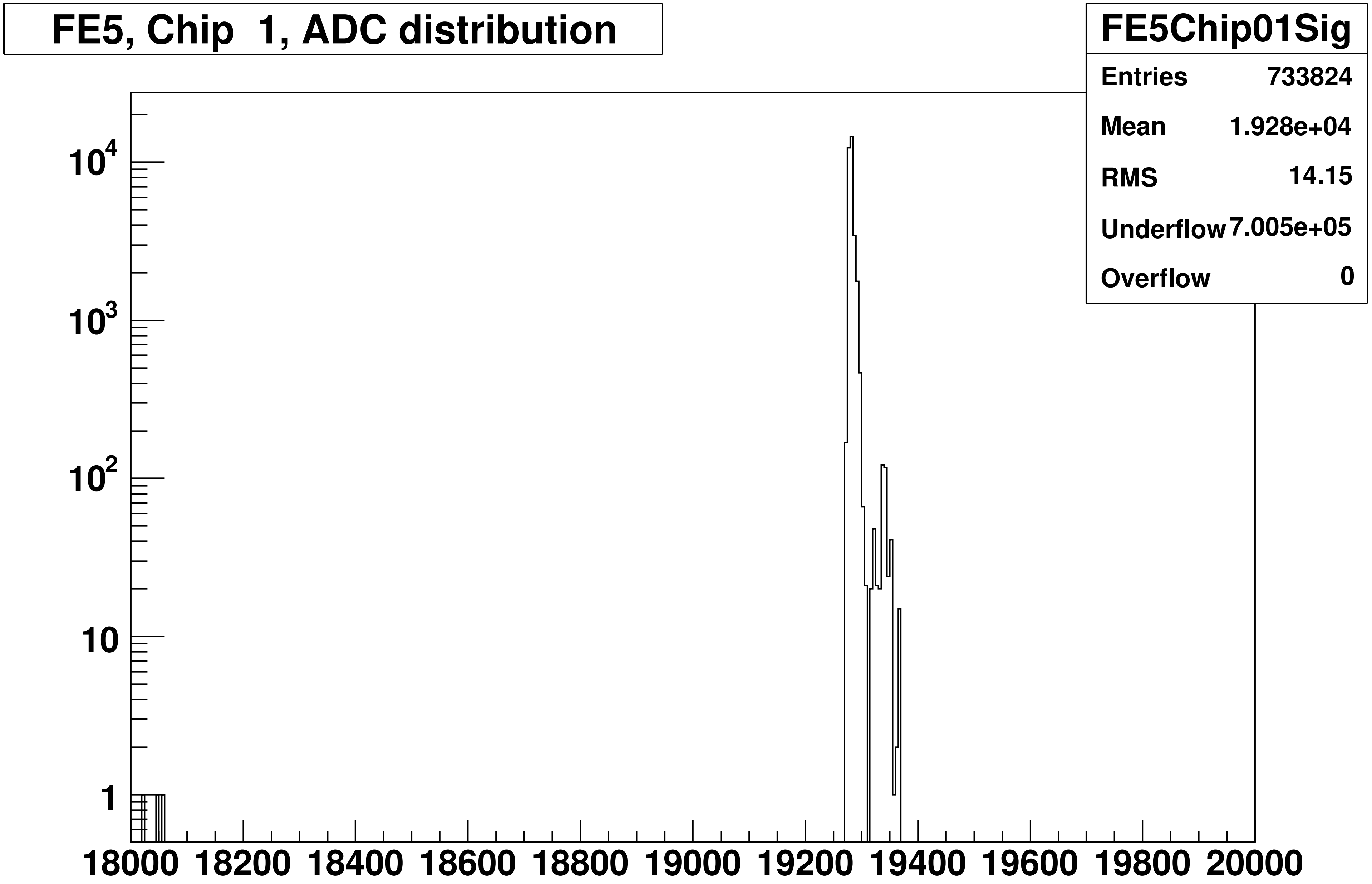
150
200



FE5, Chip 1, ADC distribution
FE5Chip01Sig
Entries 733824
Mean 1.928e+04
RMS 14.15
Underflow 7.005e+05
Overflow 0
10^4
10^3
10^2
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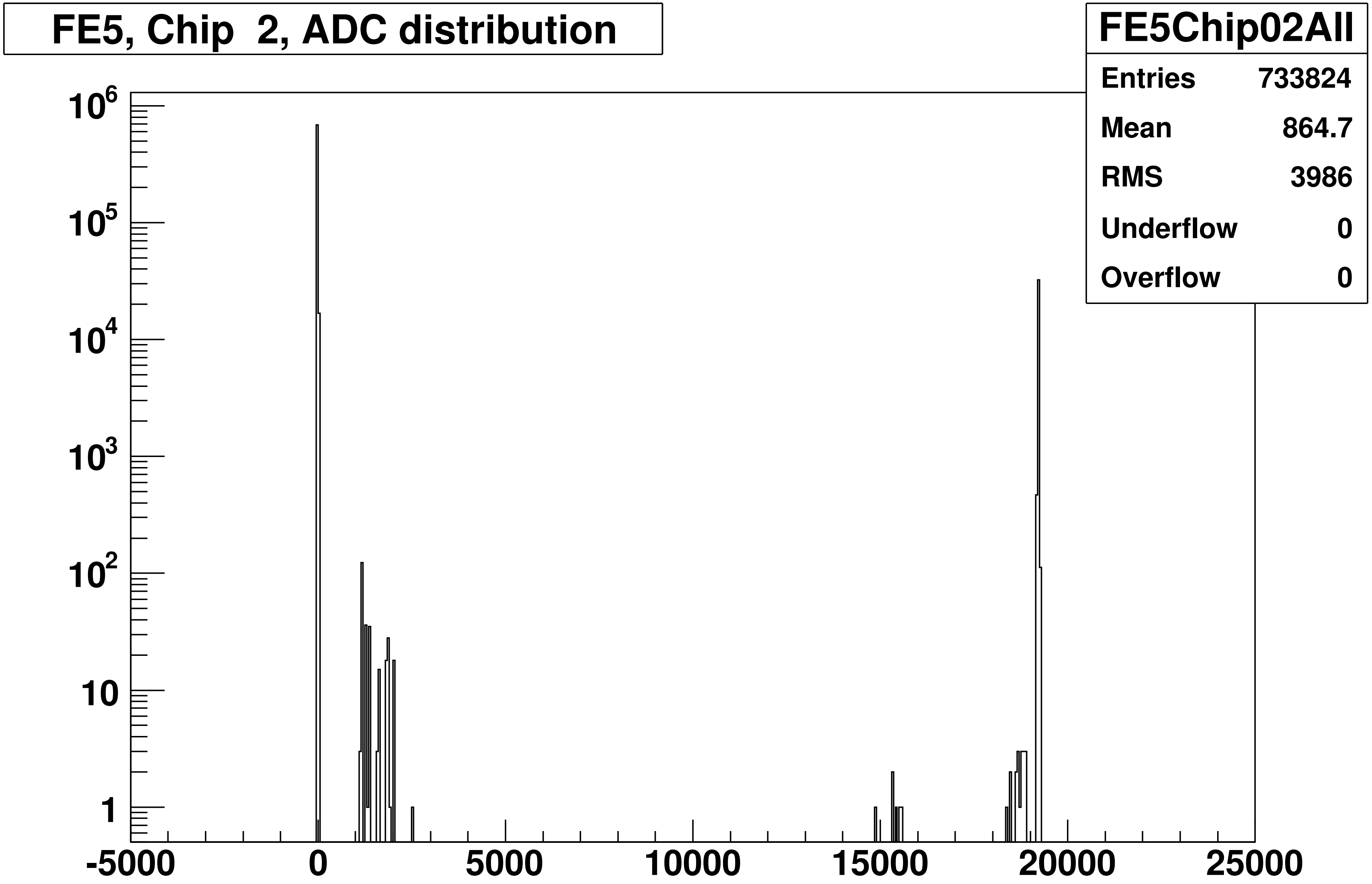
FE5, Chip 2, ADC distribution
FE5Chip02All
Entries 733824
Mean 864.7
RMS 3986
Underflow 0
Overflow 0
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10^4
10^3
10^2
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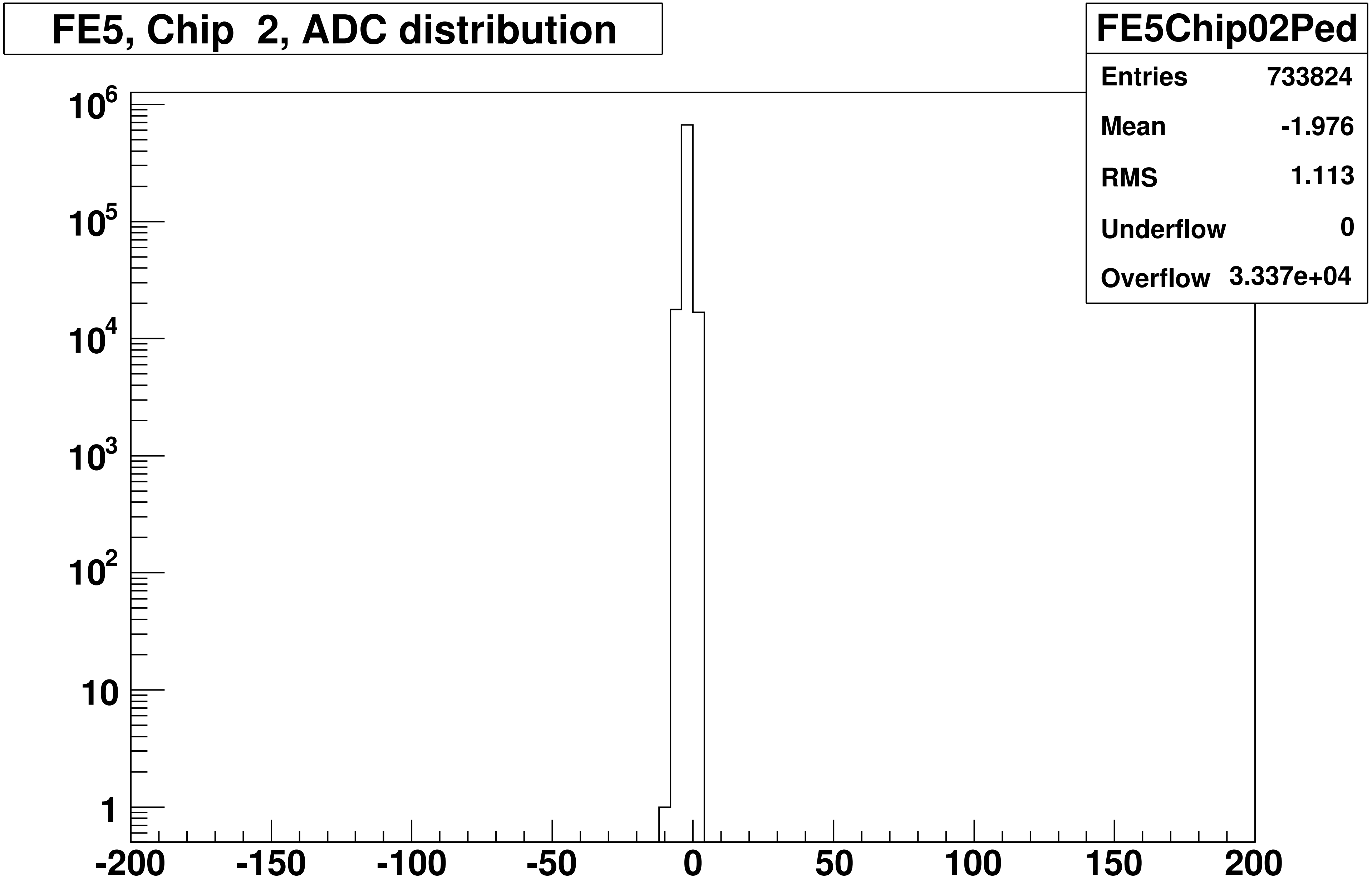
FE5, Chip 2, ADC distribution
FE5Chip02Ped
Entries 733824
Mean -1.976
RMS 1.113
Underflow 0
Overflow 3.337e+04
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10^3
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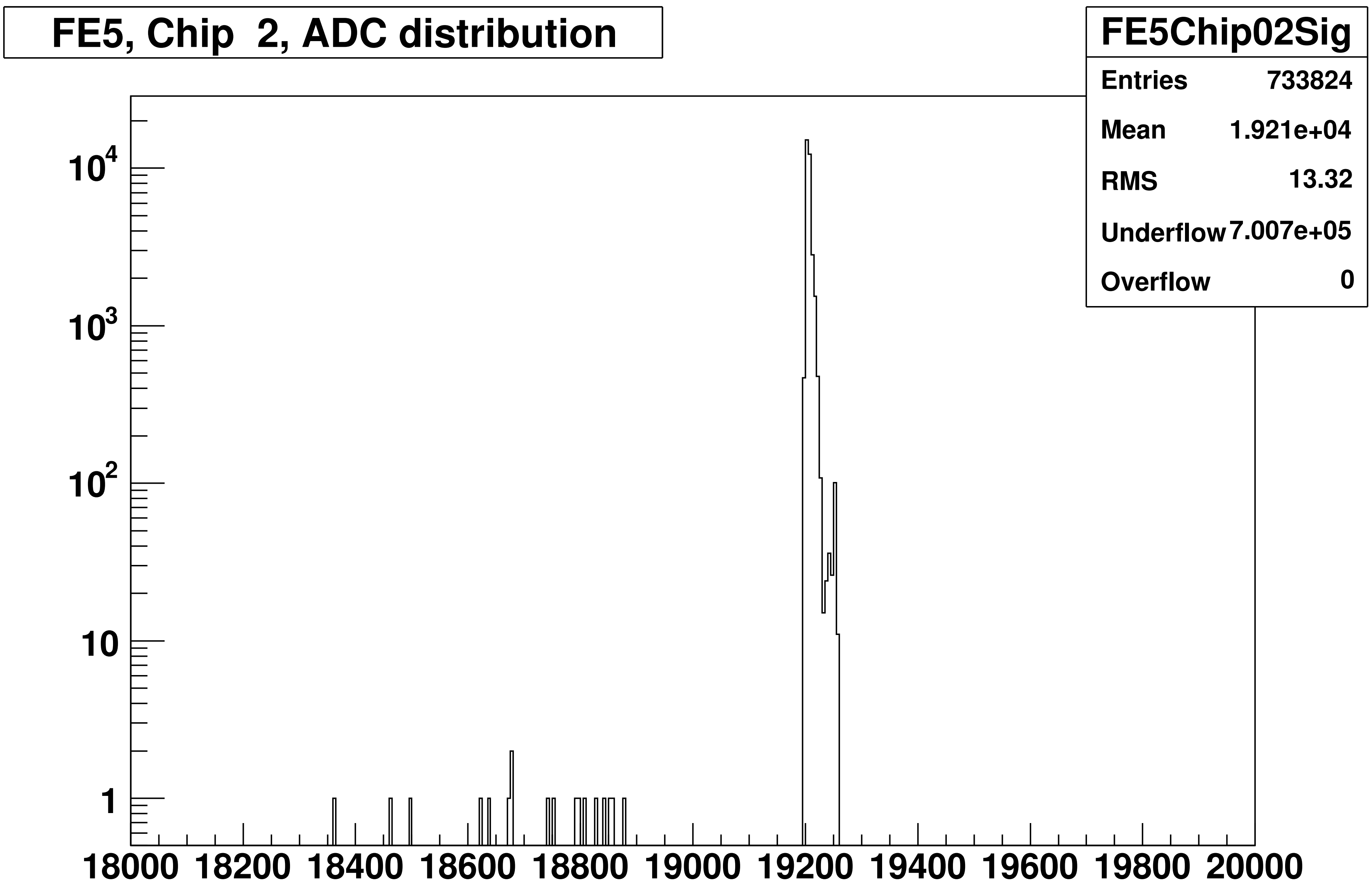
200



FE5, Chip 2, ADC distribution
FE5Chip02Sig
Entries 733824
Mean 1.921e+04
RMS 13.32
Underflow 7.007e+05
Overflow 0
10^4
10^3
10^2
10
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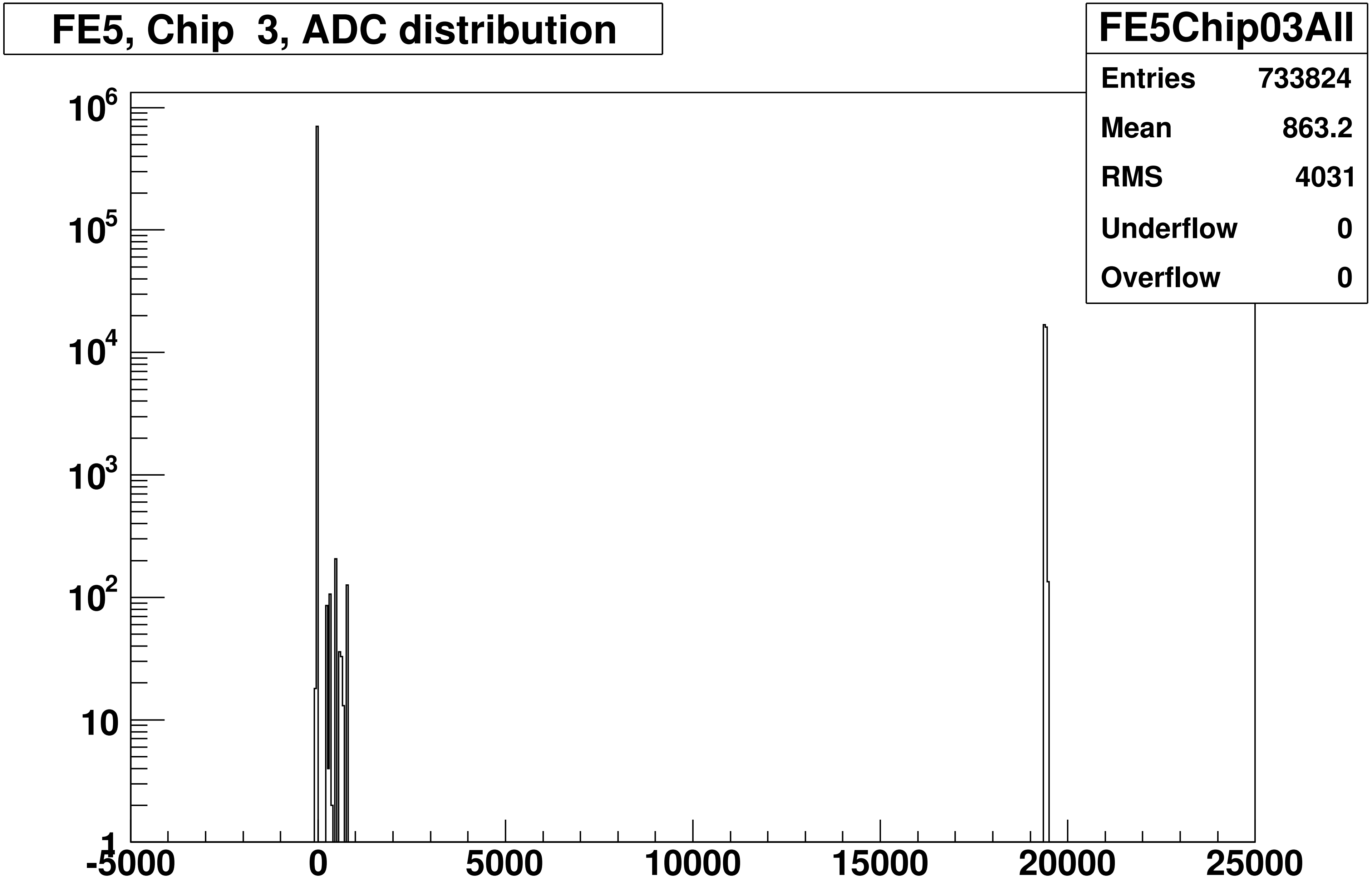
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE5, Chip 3, ADC distribution
FE5Chip03All
Entries 733824
Mean 863.2
RMS 4031
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
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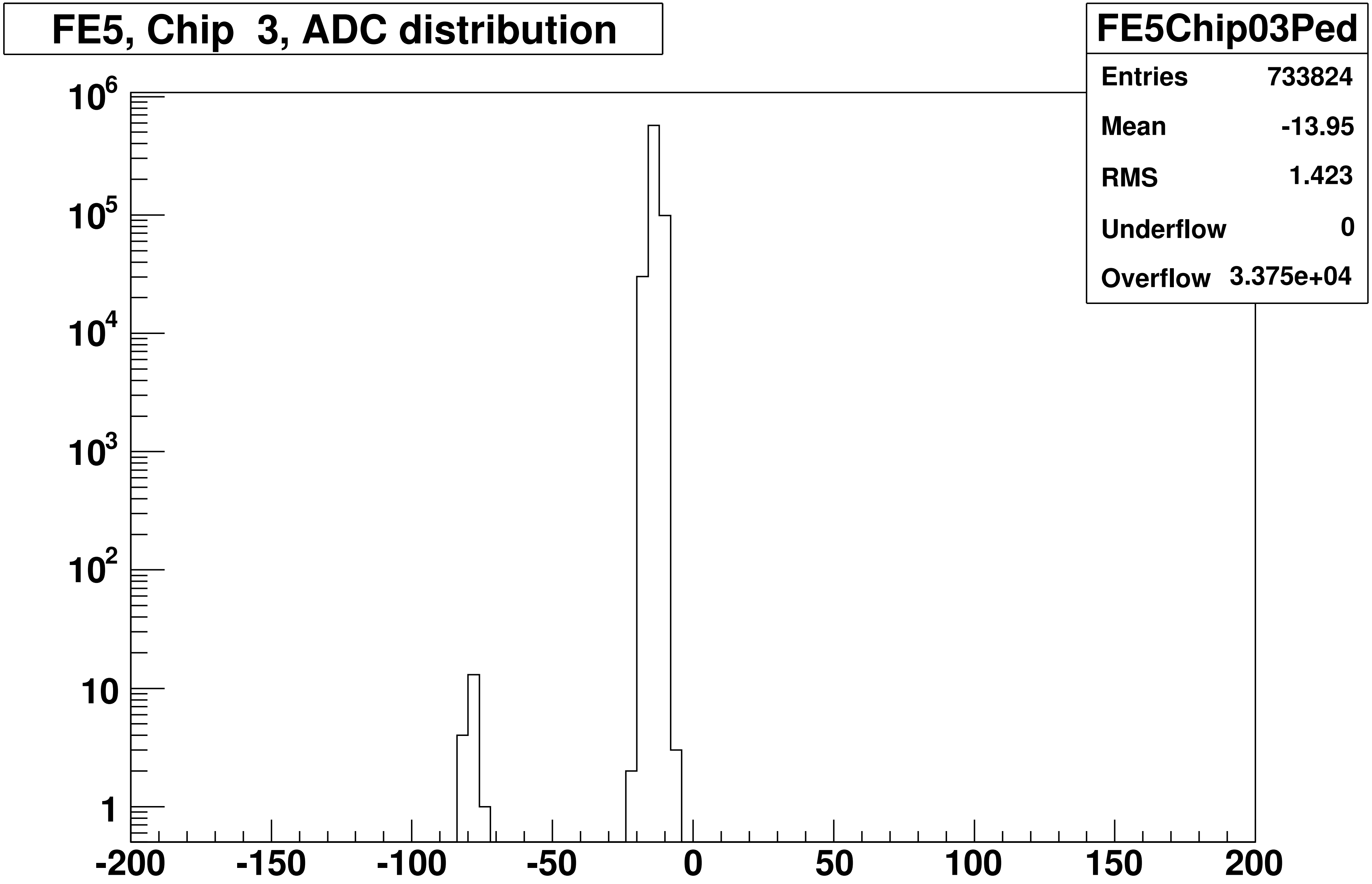
25000


FE5, Chip 3, ADC distribution
FE5Chip03Ped
Entries 733824
Mean -13.95
RMS 1.423
Underflow 0
Overflow 3.375e+04
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10^5
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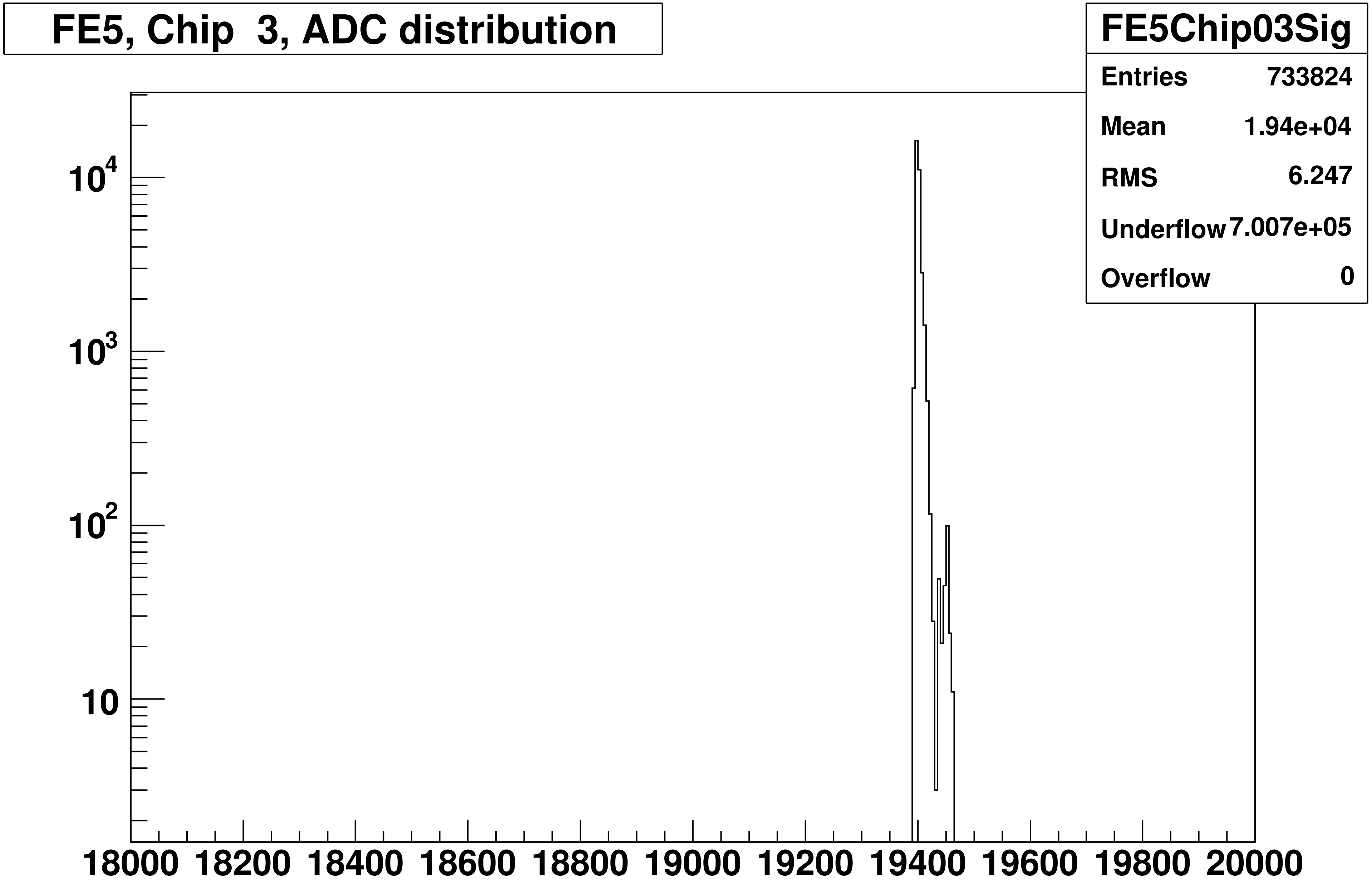
200



FE5, Chip 3, ADC distribution
FE5Chip03Sig
Entries 733824
Mean 1.94e+04
RMS 6.247
Underflow 7.007e+05
Overflow 0
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10^3
10^2
10
18000
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18400
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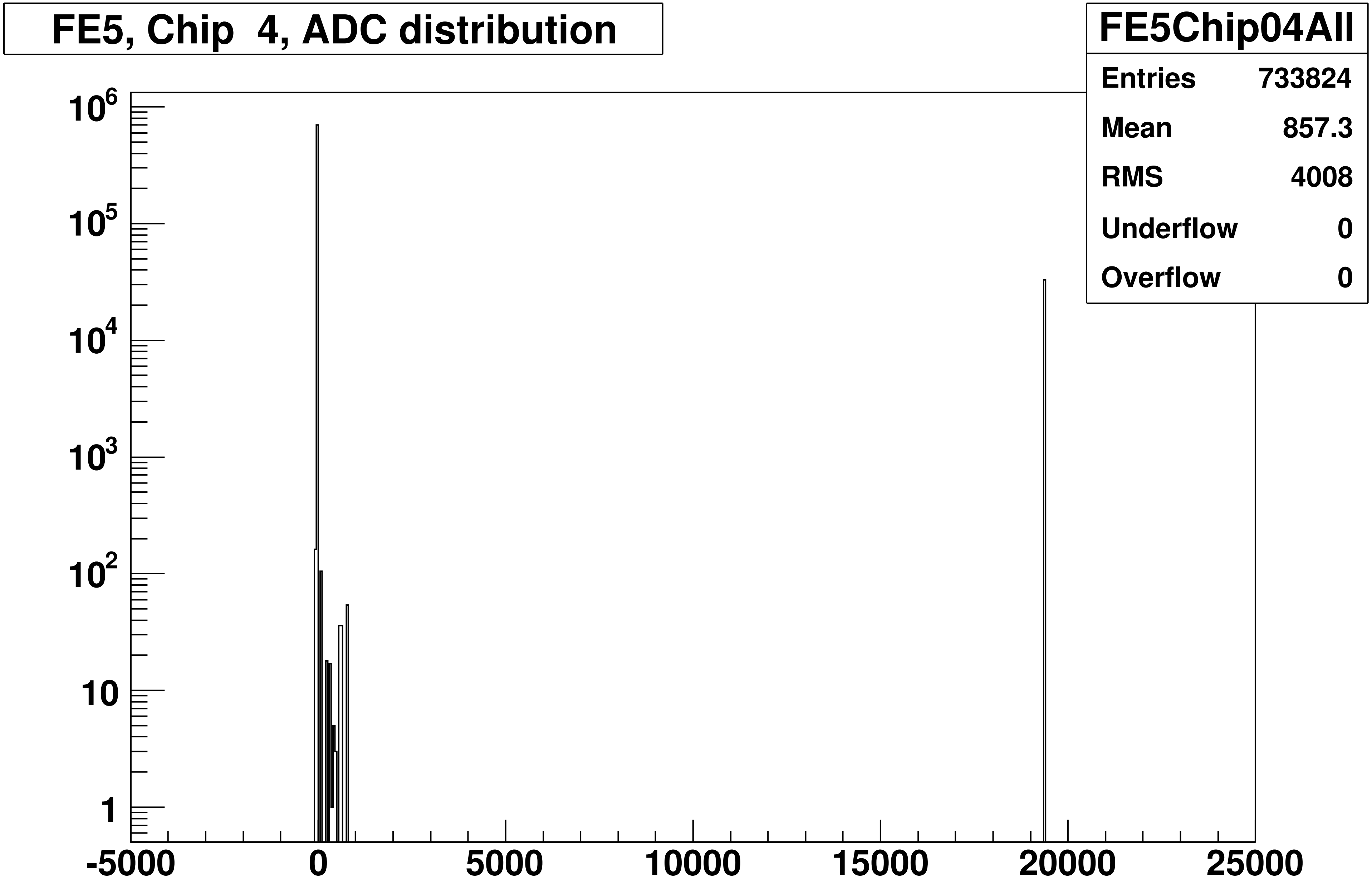
20000


FE5, Chip 4, ADC distribution
FE5Chip04All
Entries 733824
Mean 857.3
RMS 4008
Underflow 0
Overflow 0
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10^3
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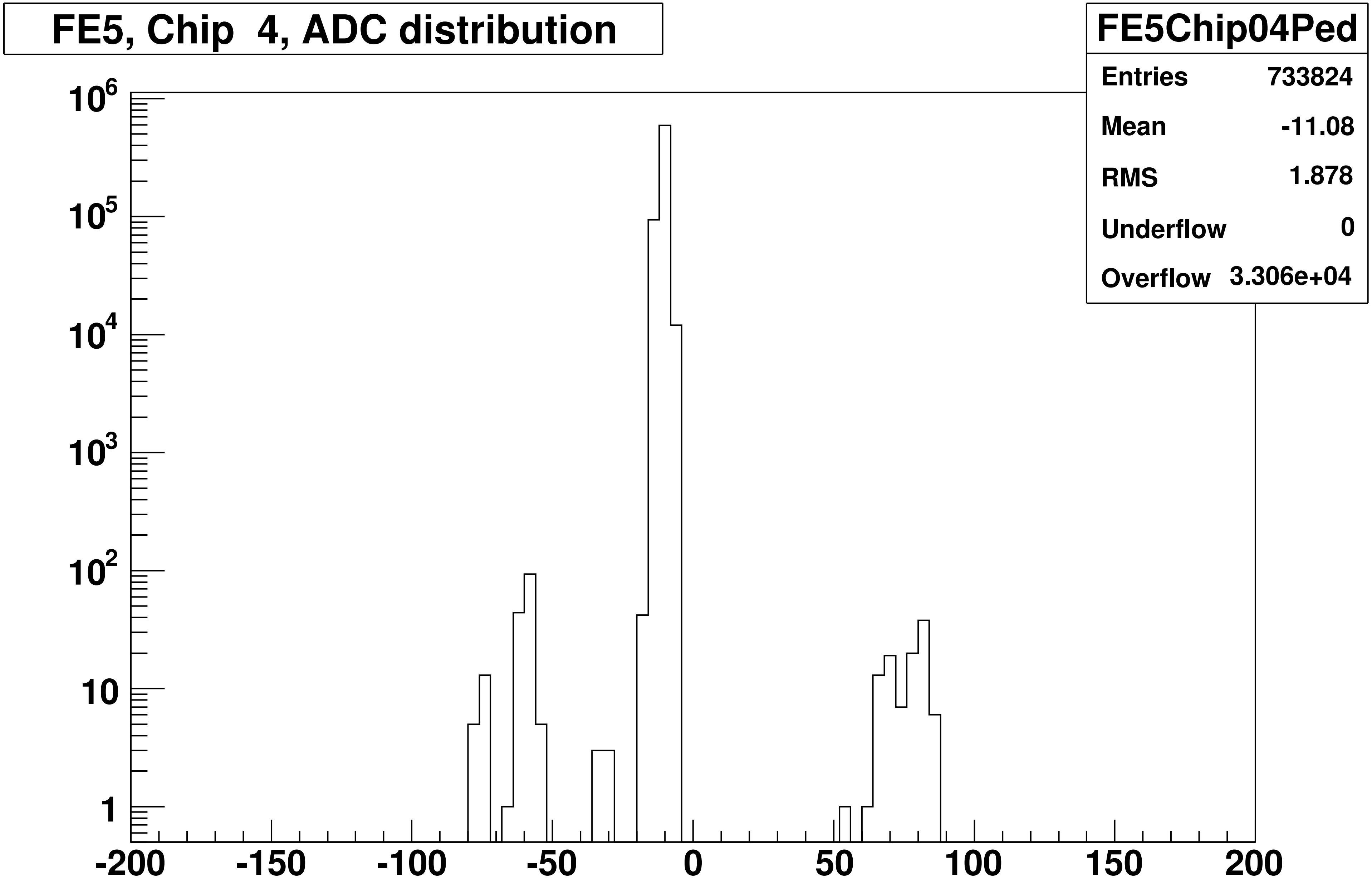
FE5, Chip 4, ADC distribution
FE5Chip04Ped
Entries 733824
Mean -11.08
RMS 1.878
Underflow 0
Overflow 3.306e+04
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10^2
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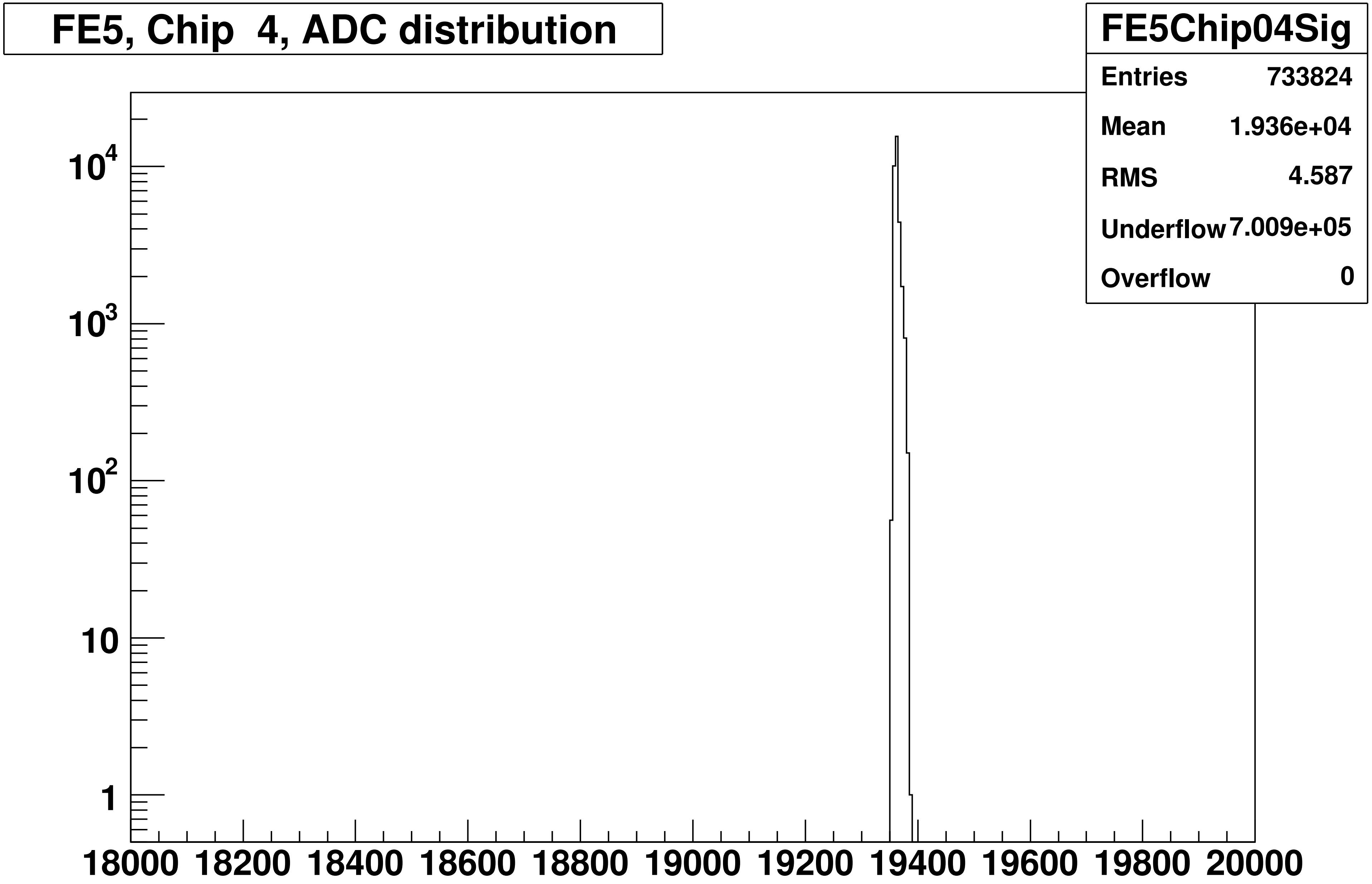
150
200



FE5, Chip 4, ADC distribution
FE5Chip04Sig
Entries 733824
Mean 1.936e+04
RMS 4.587
Underflow 7.009e+05
Overflow 0
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10^3
10^2
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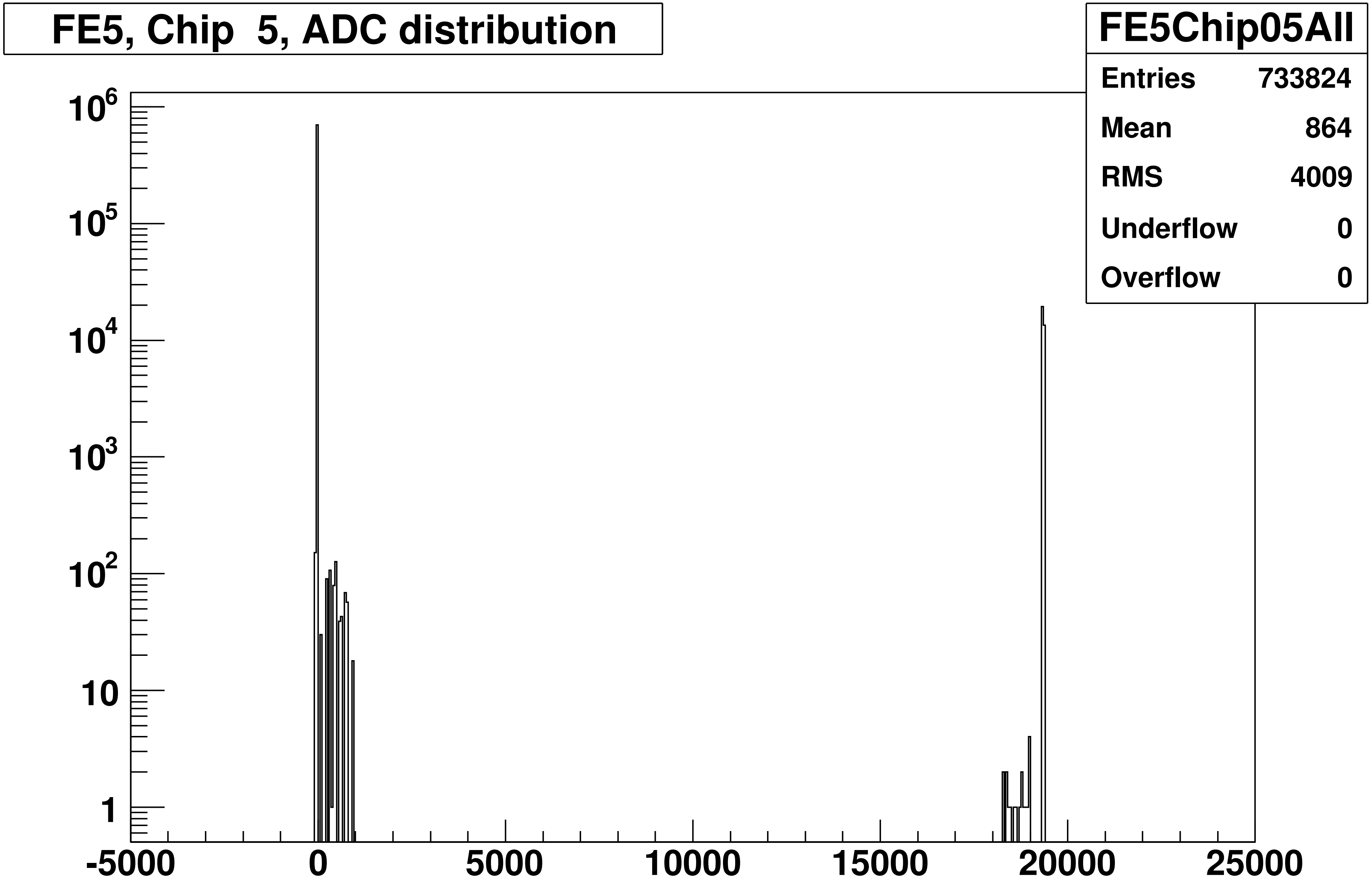
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE5, Chip 5, ADC distribution
FE5Chip05All
Entries 733824
Mean 864
RMS 4009
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
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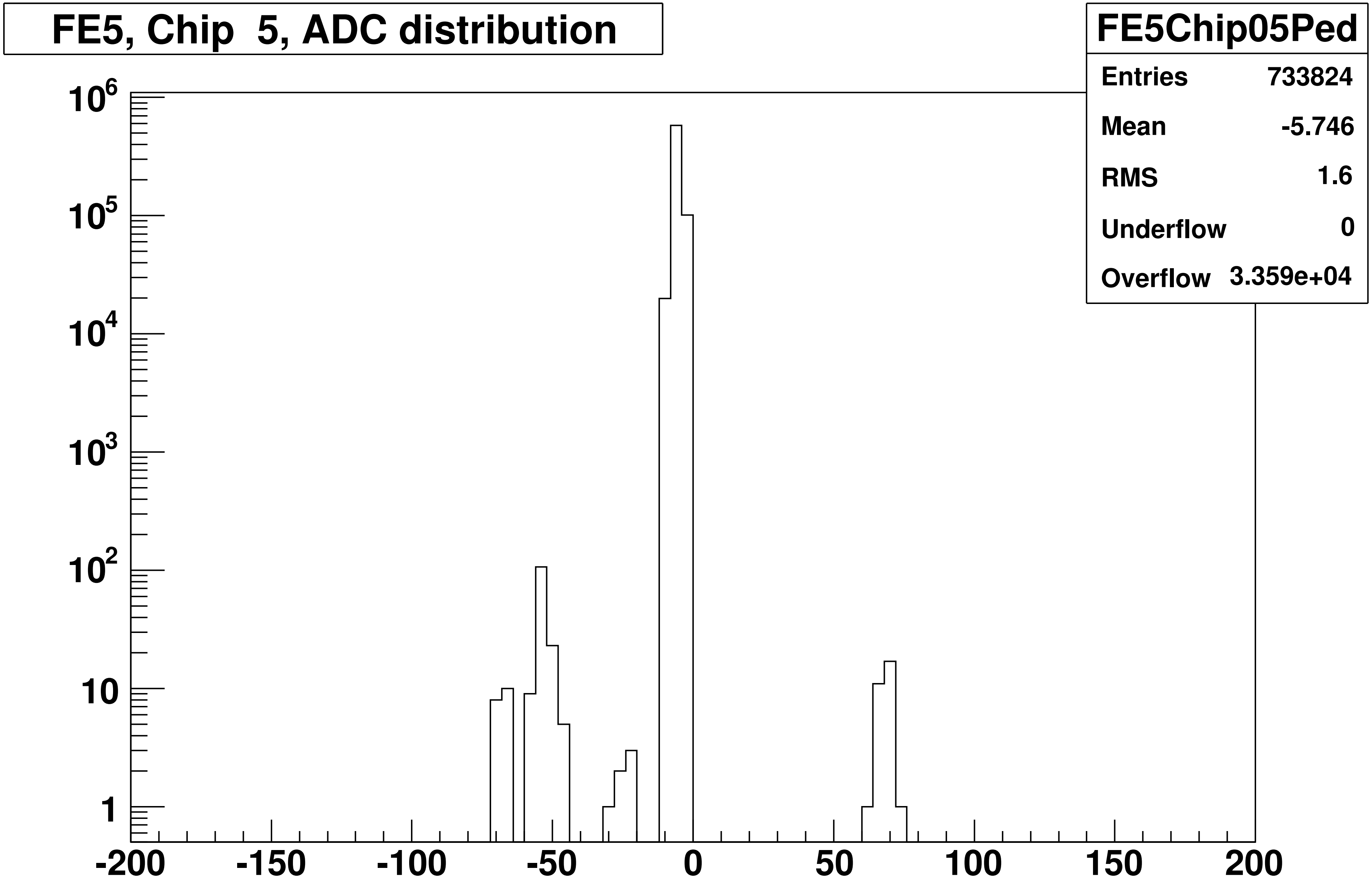
20000
25000


FE5, Chip 5, ADC distribution
FE5Chip05Ped
Entries 733824
Mean -5.746
RMS 1.6
Underflow 0
Overflow 3.359e+04
10^6
10^5
10^4
10^3
10^2
10
1
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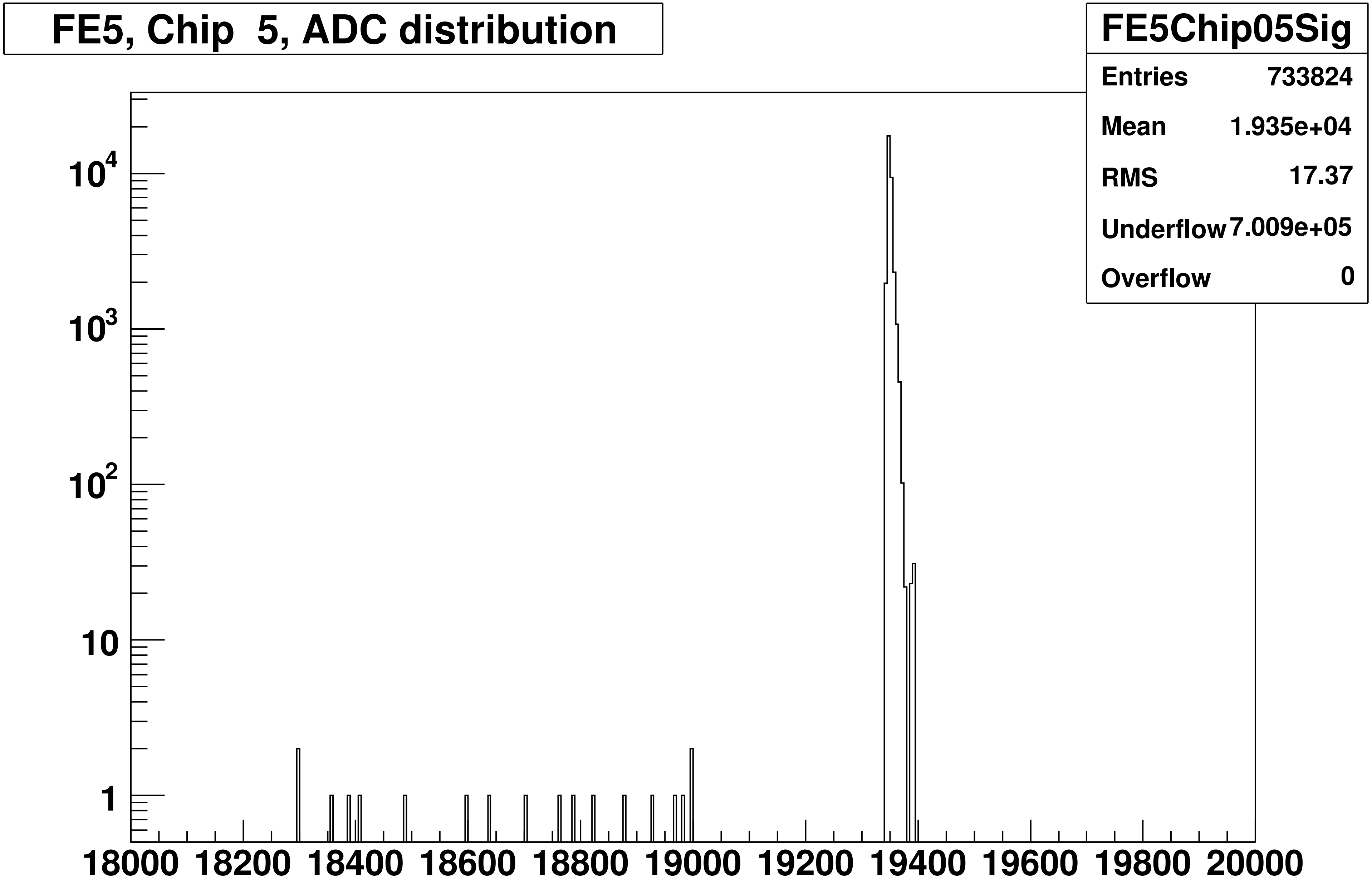

FE5, Chip 5, ADC distribution
FE5Chip05Sig
Entries 733824
Mean 1.935e+04
RMS 17.37
Underflow 7.009e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
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19000
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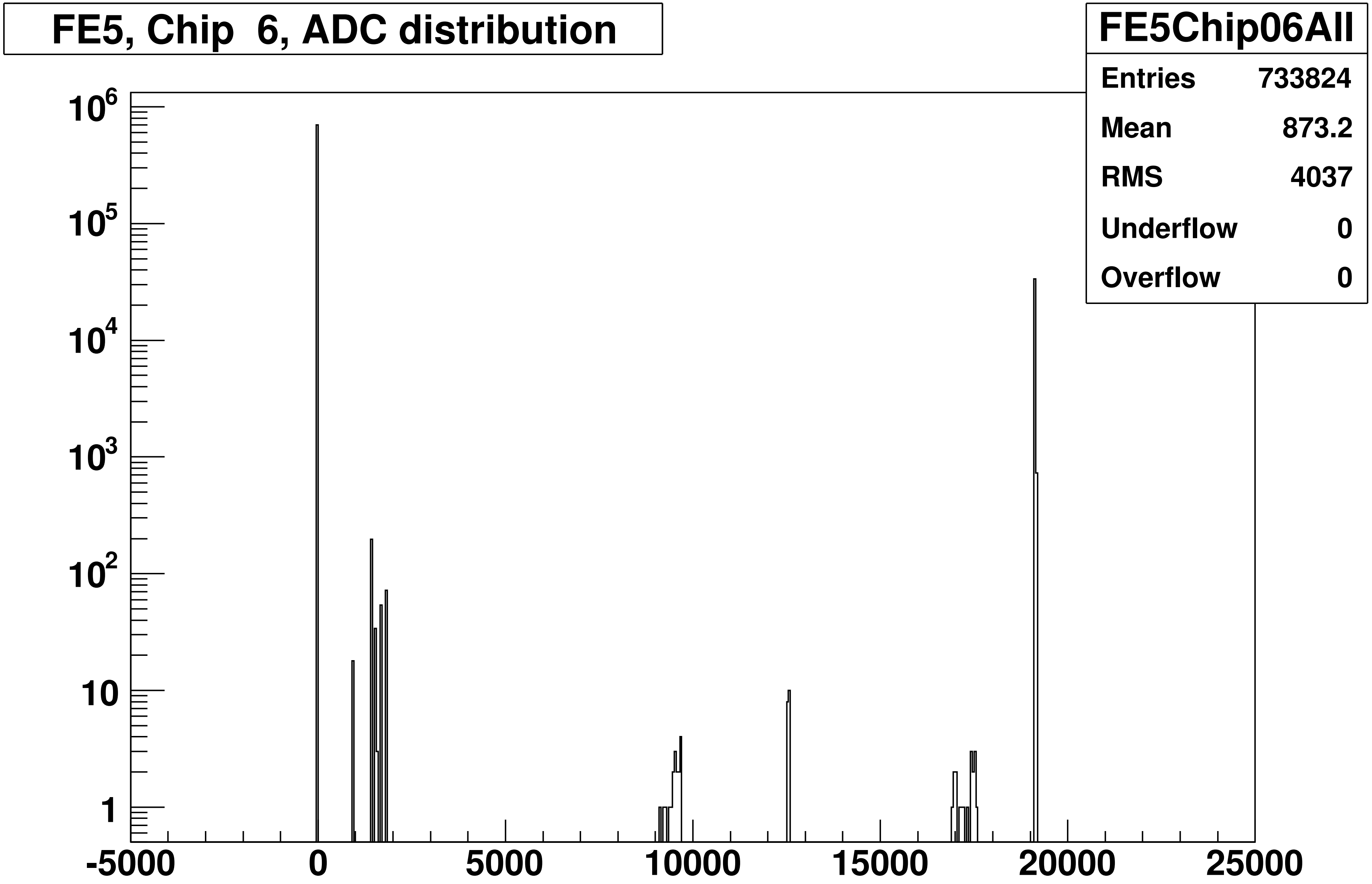
FE5, Chip 6, ADC distribution
FE5Chip06All
Entries 733824
Mean 873.2
RMS 4037
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
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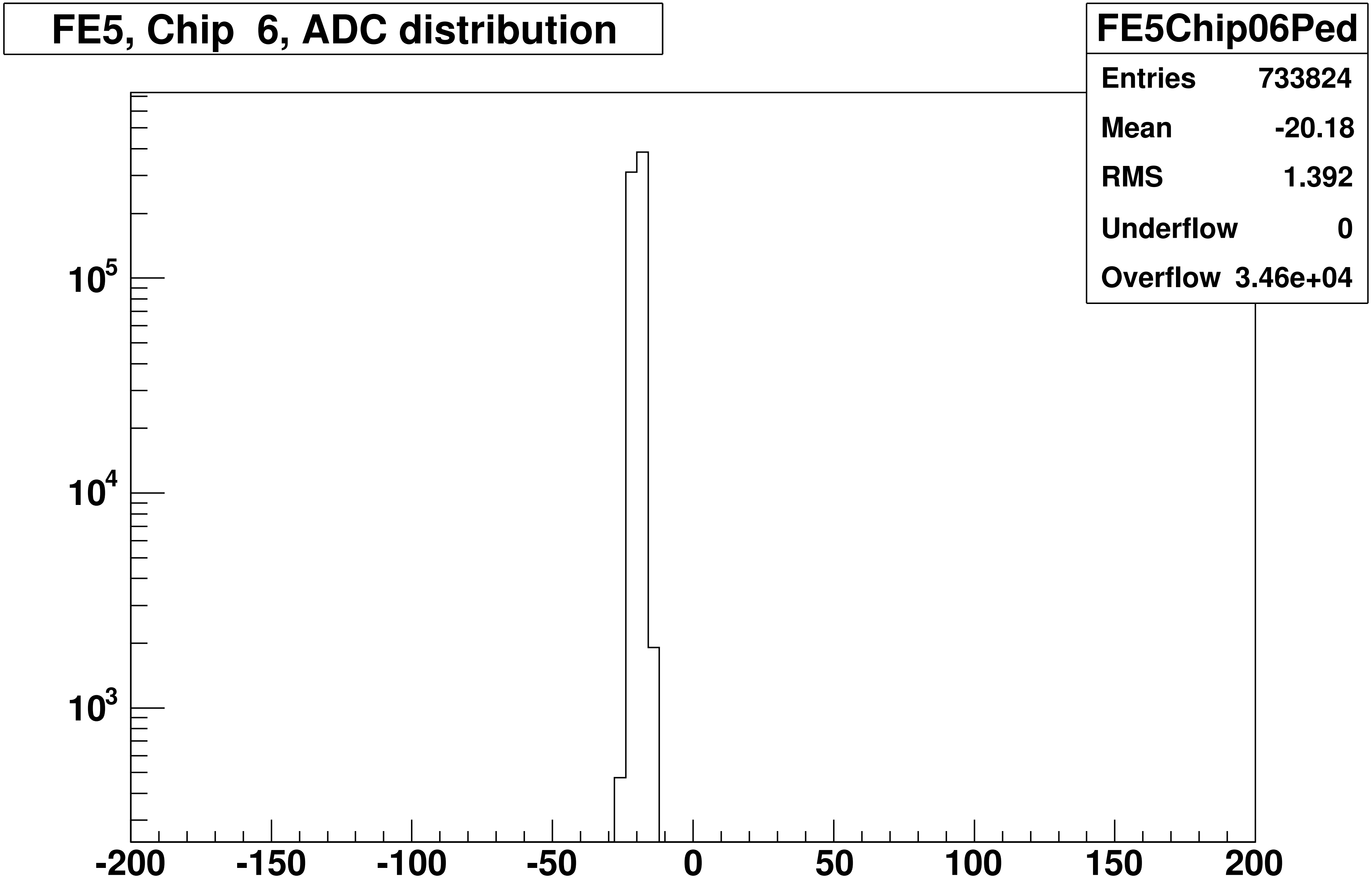
FE5, Chip 6, ADC distribution
FE5Chip06Ped
Entries 733824
Mean -20.18
RMS 1.392
Underflow 0
Overflow 3.46e+04
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10^4
10^3
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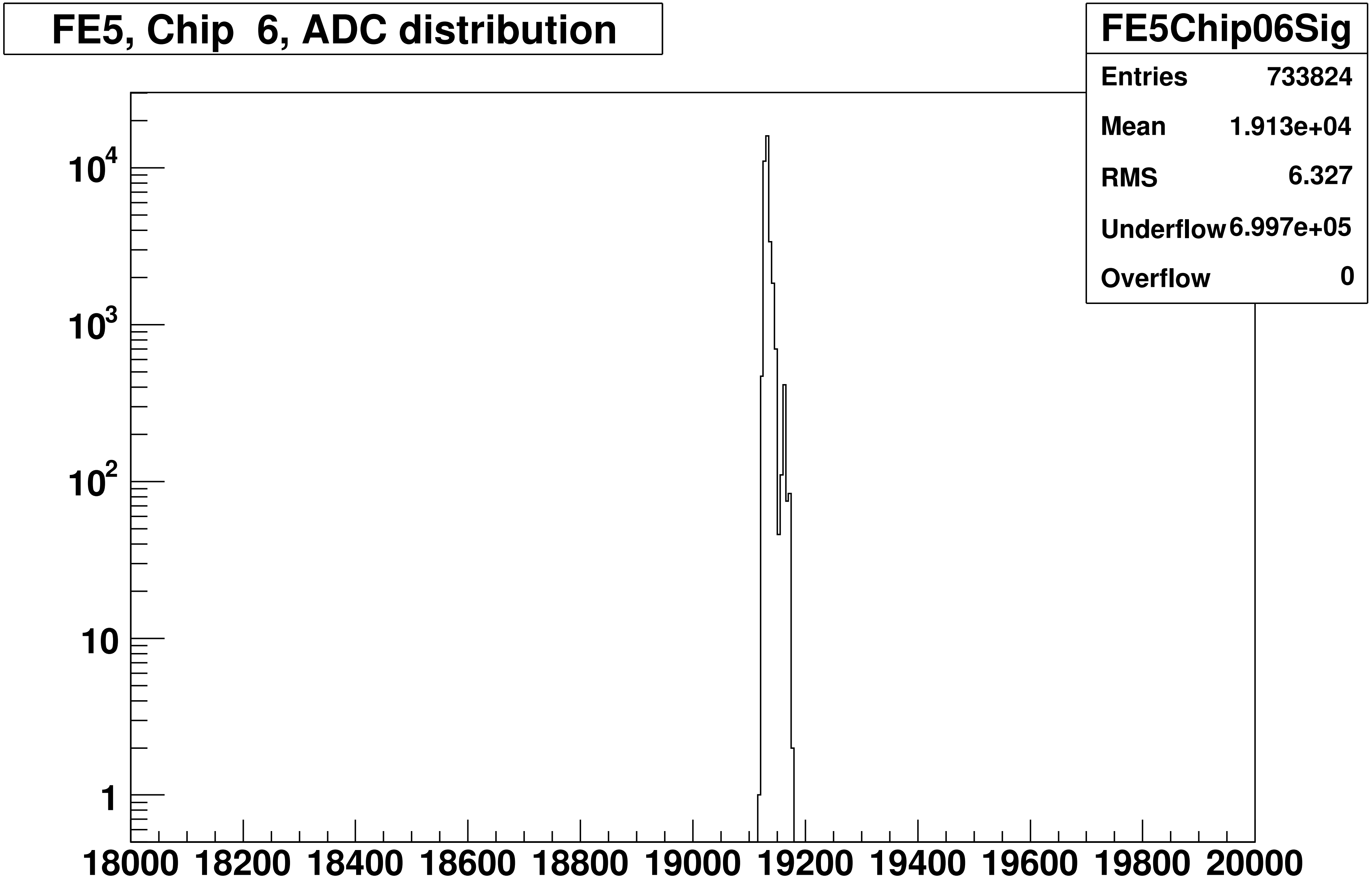
FE5, Chip 6, ADC distribution
FE5Chip06Sig
Entries 733824
Mean 1.913e+04
RMS 6.327
Underflow 6.997e+05
Overflow 0
10^4
10^3
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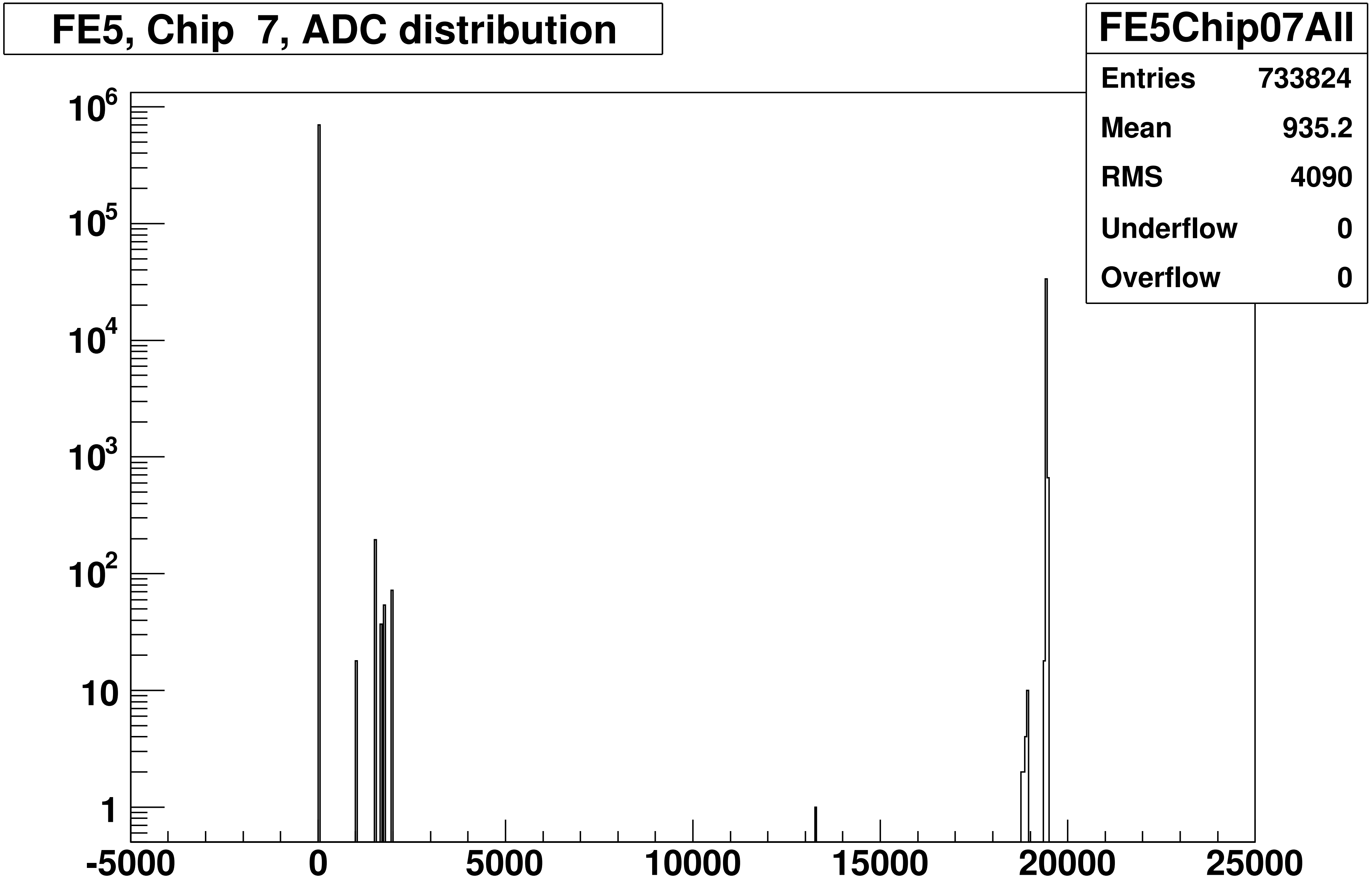
FE5, Chip 7, ADC distribution
FE5Chip07All
Entries 733824
Mean 935.2
RMS 4090
Underflow 0
Overflow 0
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10^4
10^3
10^2
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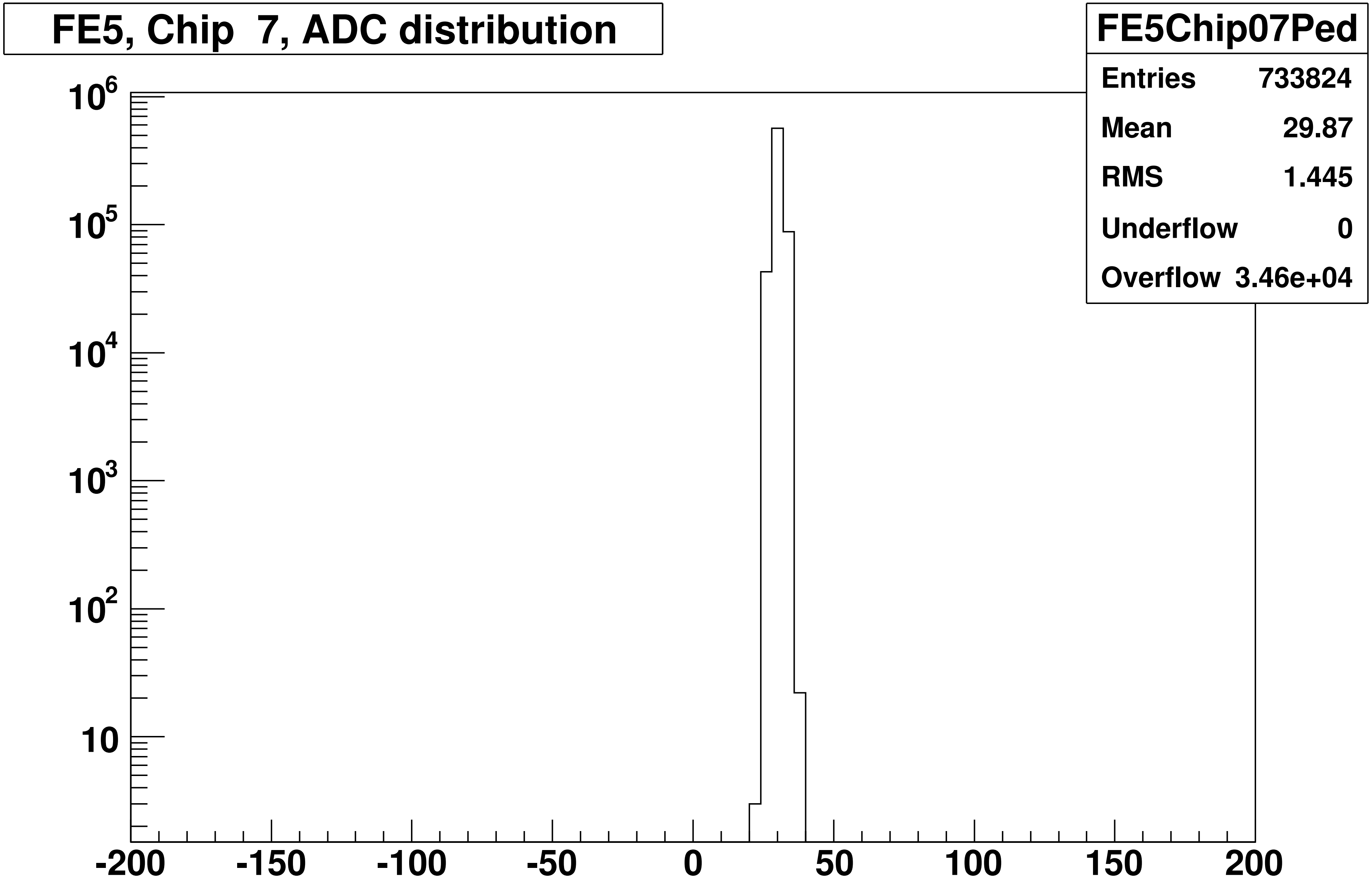

FE5, Chip 7, ADC distribution
FE5Chip07Ped
Entries 733824
Mean 29.87
RMS 1.445
Underflow 0
Overflow 3.46e+04
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10^4
10^3
10^2
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-200
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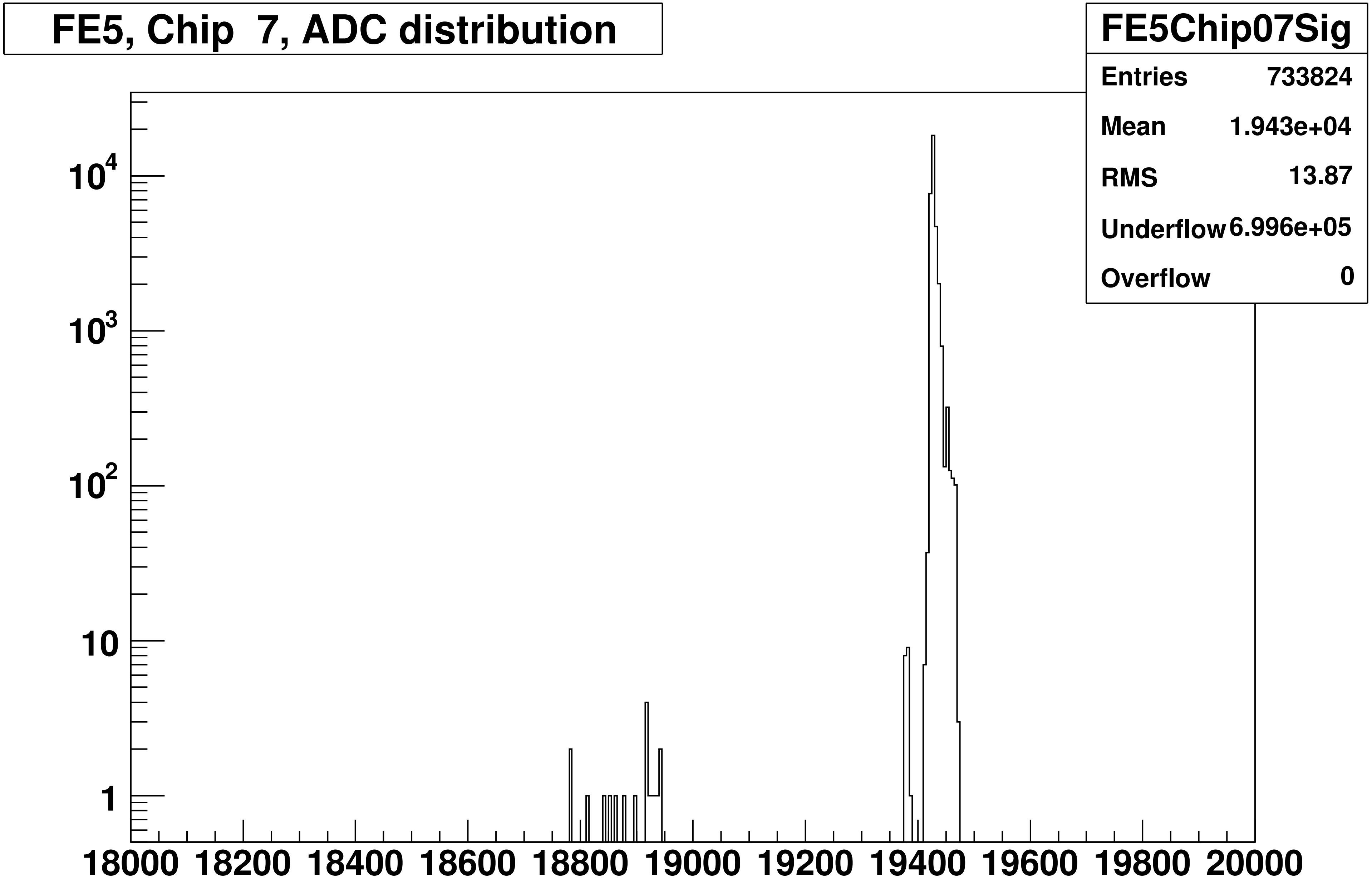
FE5, Chip 7, ADC distribution
FE5Chip07Sig
Entries 733824
Mean 1.943e+04
RMS 13.87
Underflow 6.996e+05
Overflow 0
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10^3
10^2
10
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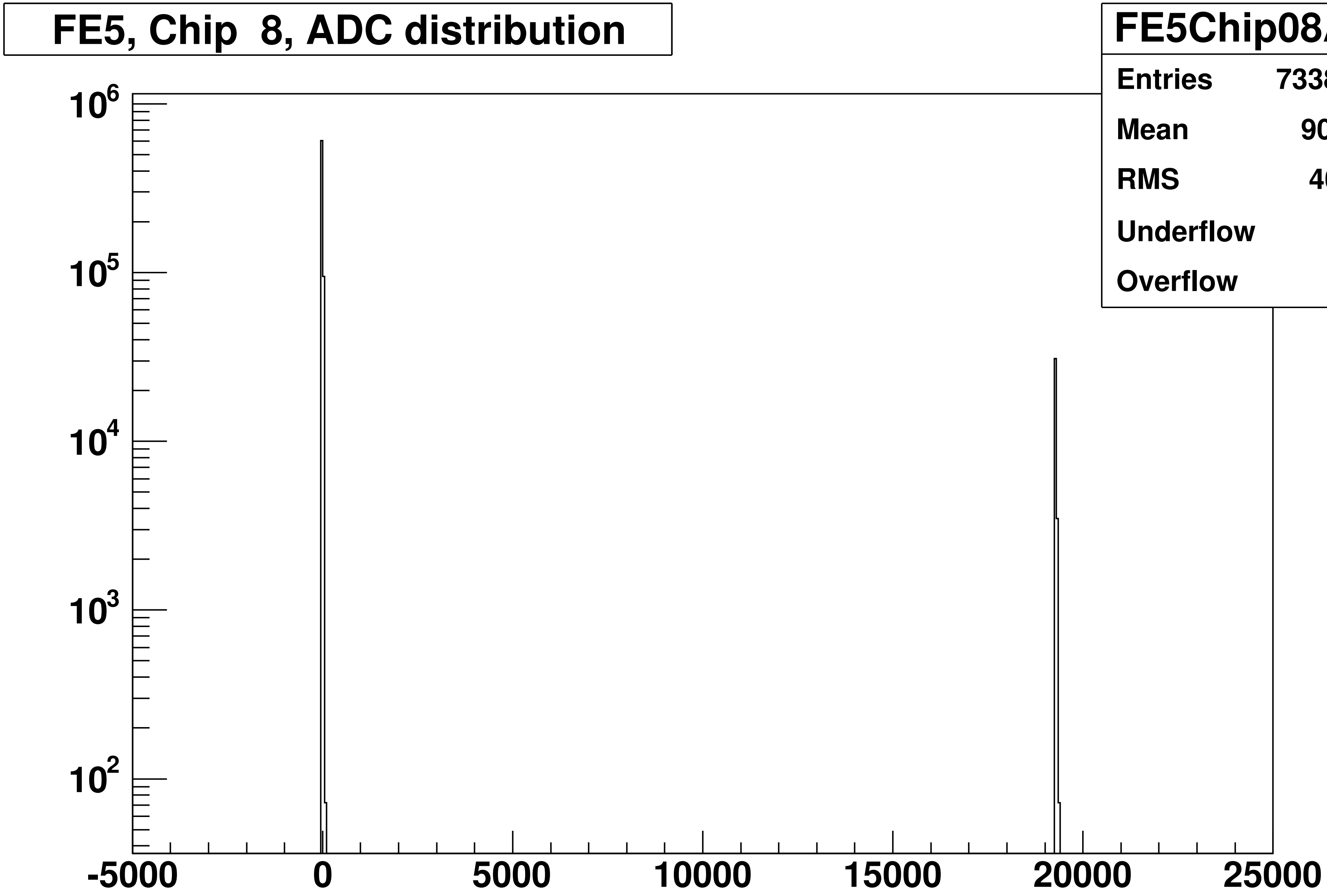
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE5, Chip 8, ADC distribution
FE5Chip08All
Entries 733824
Mean 905.7
RMS 4084
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
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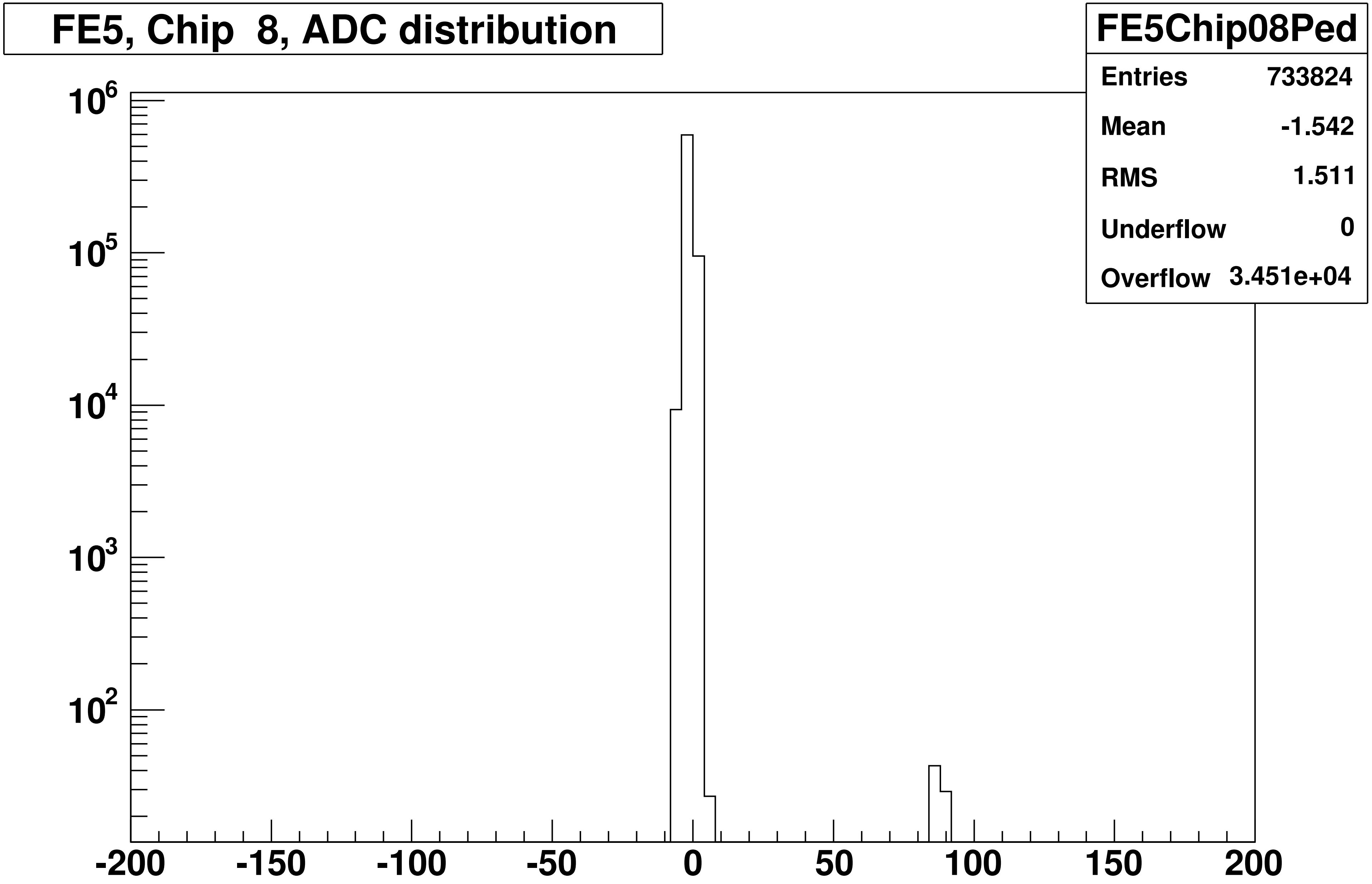

FE5, Chip 8, ADC distribution
FE5Chip08Ped
Entries 733824
Mean -1.542
RMS 1.511
Underflow 0
Overflow 3.451e+04
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10^4
10^3
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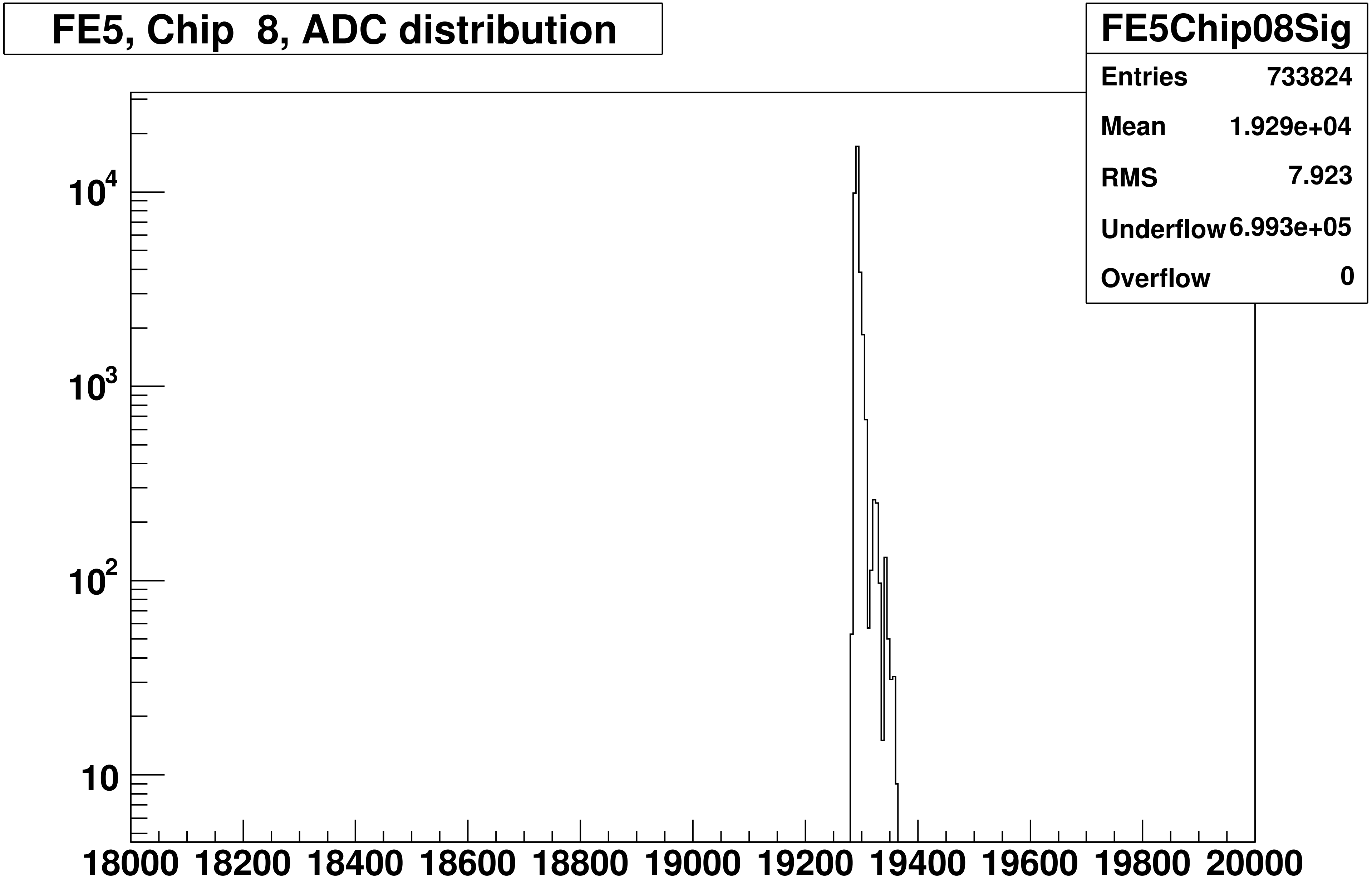
FE5, Chip 8, ADC distribution
FE5Chip08Sig
Entries 733824
Mean 1.929e+04
RMS 7.923
Underflow 6.993e+05
Overflow 0
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10^3
10^2
10
18000
18200
18400
18600
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19000
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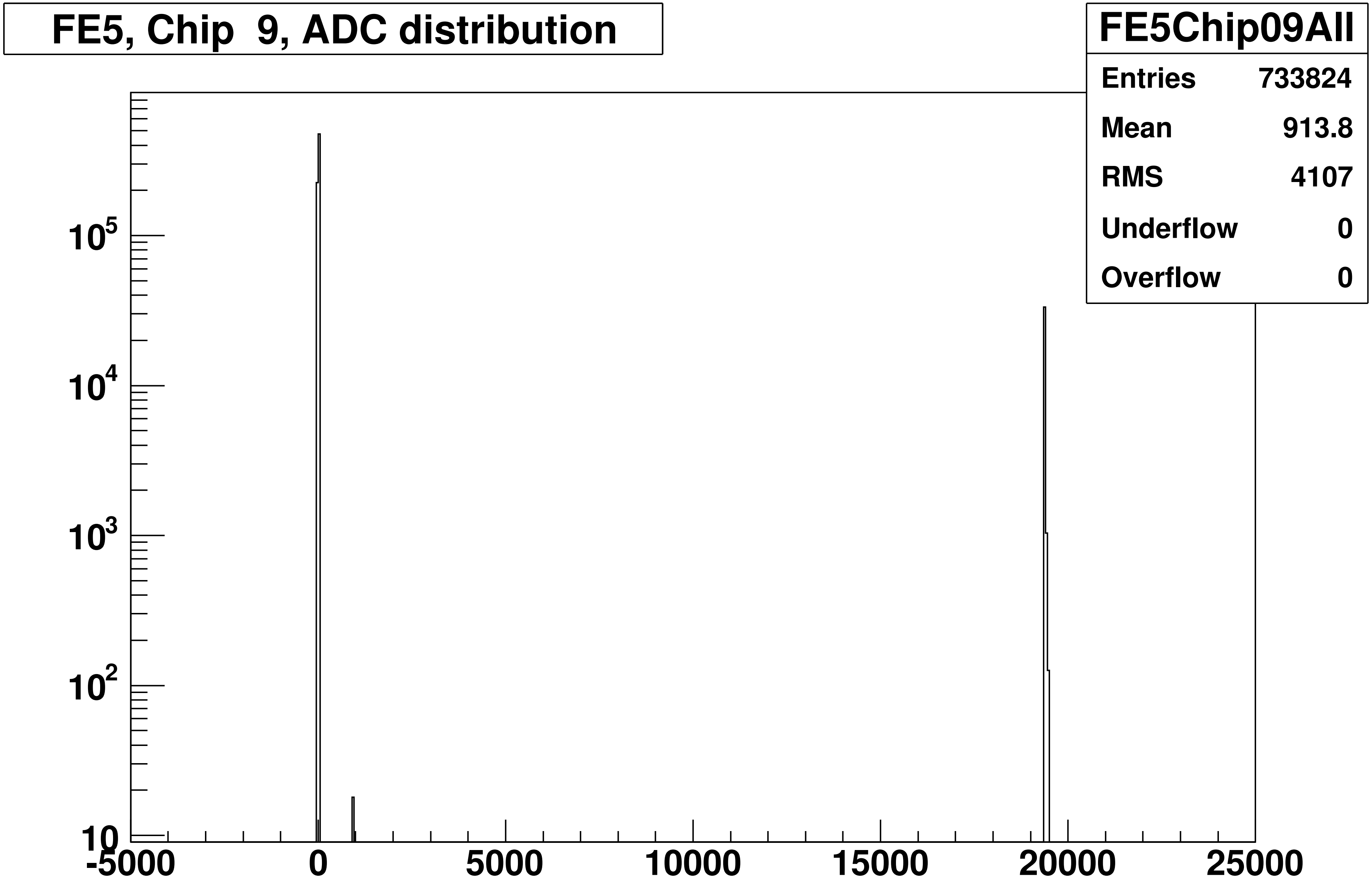
19800
20000



FE5, Chip 9, ADC distribution
FE5Chip09All
Entries 733824
Mean 913.8
RMS 4107
Underflow 0
Overflow 0
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10^3
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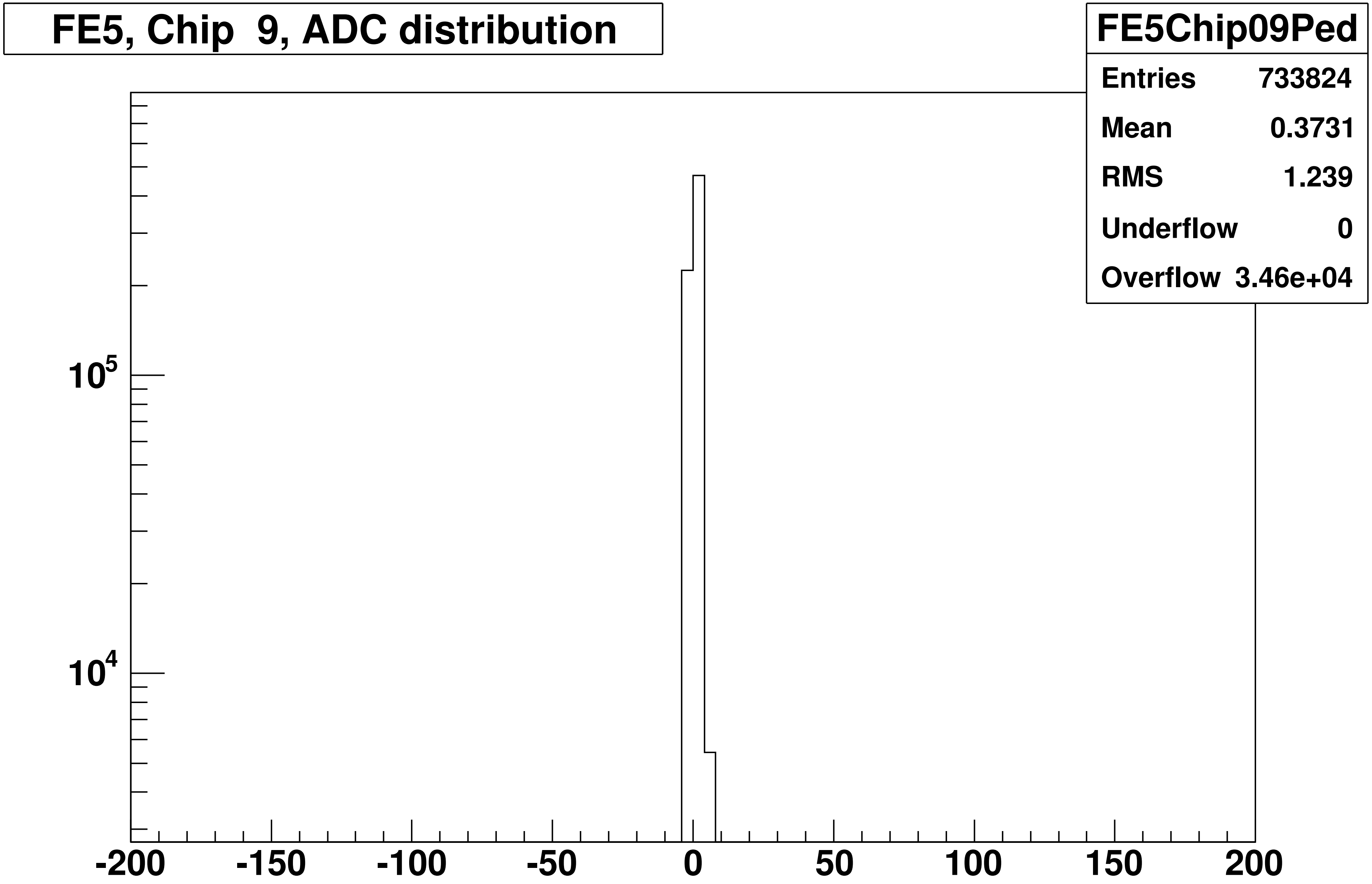
FE5, Chip 9, ADC distribution
FE5Chip09Ped
Entries 733824
Mean 0.3731
RMS 1.239
Underflow 0
Overflow 3.46e+04
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10^4
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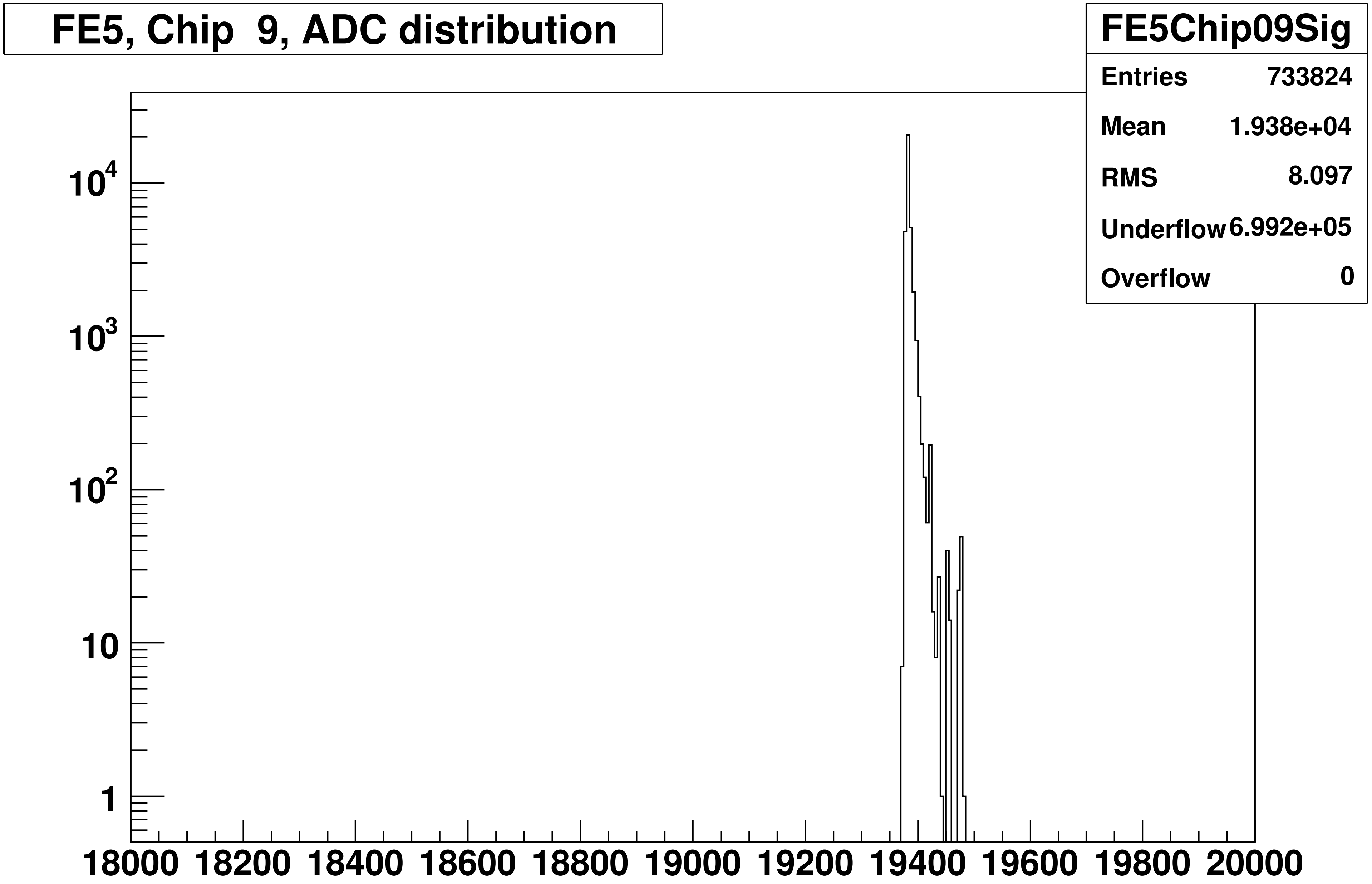
FE5, Chip 9, ADC distribution
FE5Chip09Sig
Entries 733824
Mean 1.938e+04
RMS 8.097
Underflow 6.992e+05
Overflow 0
10^4
10^3
10^2
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18000
18200
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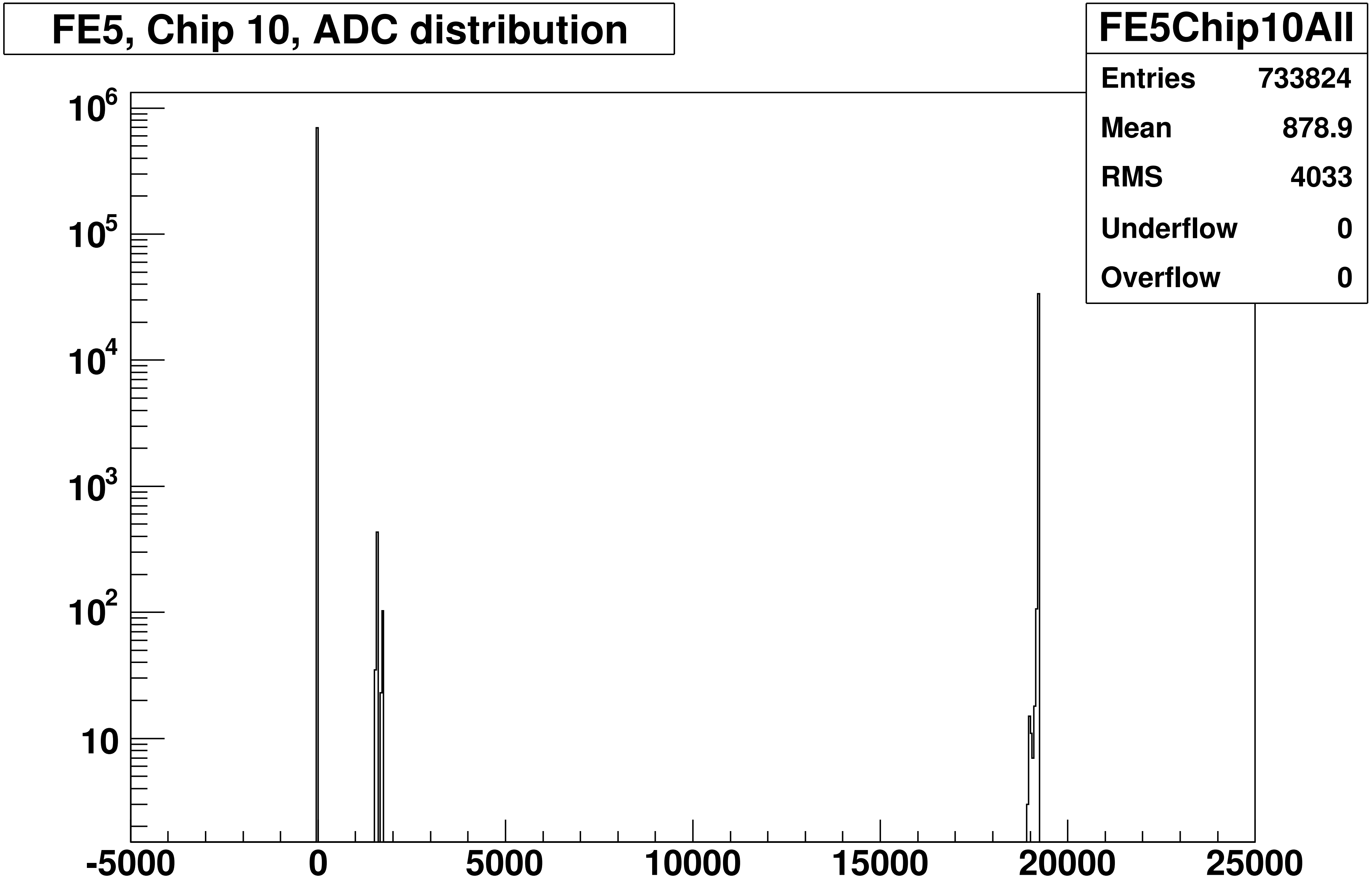

FE5, Chip 10, ADC distribution
FE5Chip10All
Entries 733824
Mean 878.9
RMS 4033
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
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-5000
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10000
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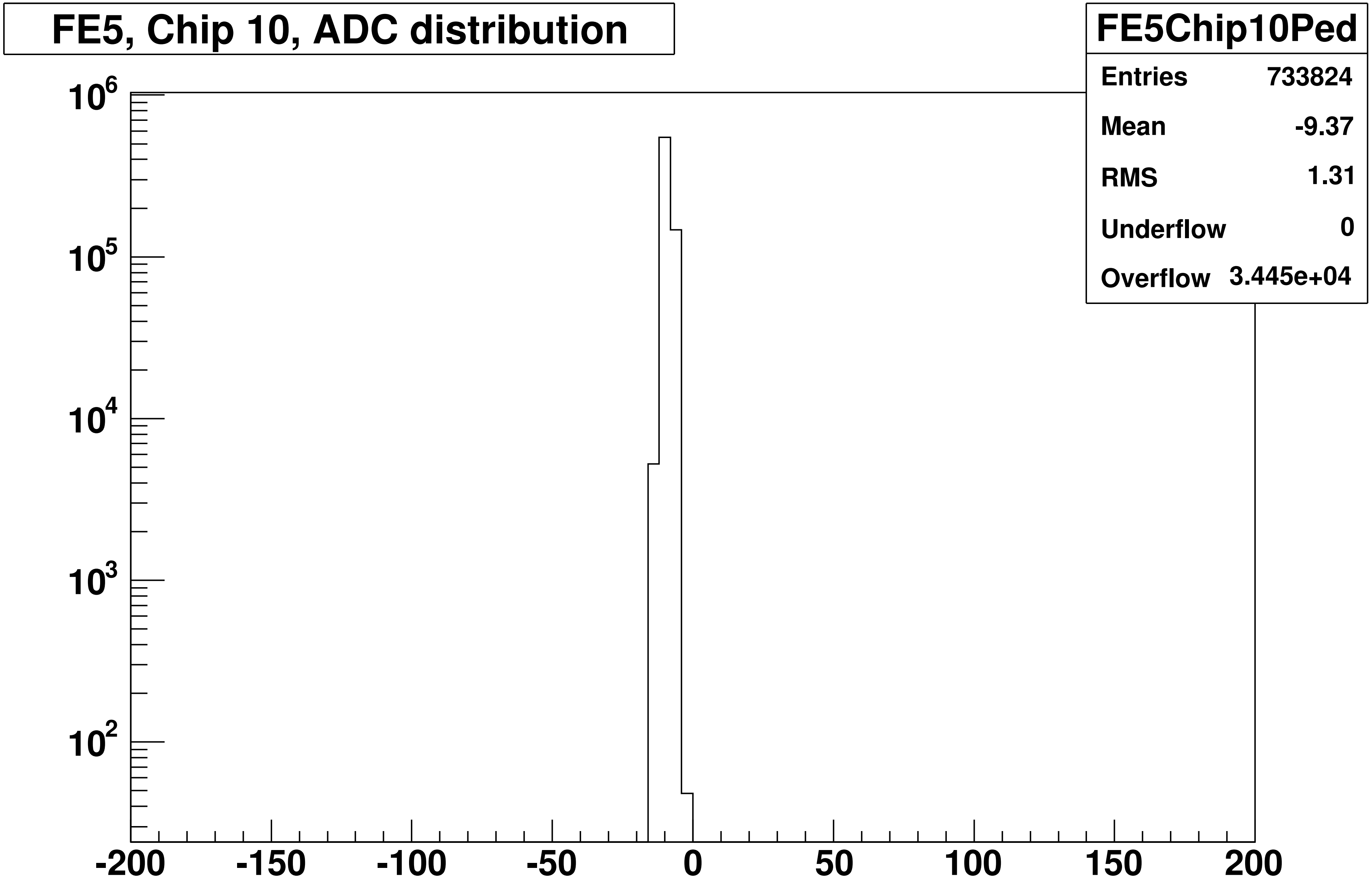
20000
25000


FE5, Chip 10, ADC distribution
FE5Chip10Ped
Entries 733824
Mean -9.37
RMS 1.31
Underflow 0
Overflow 3.445e+04
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10^5
10^4
10^3
10^2
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150
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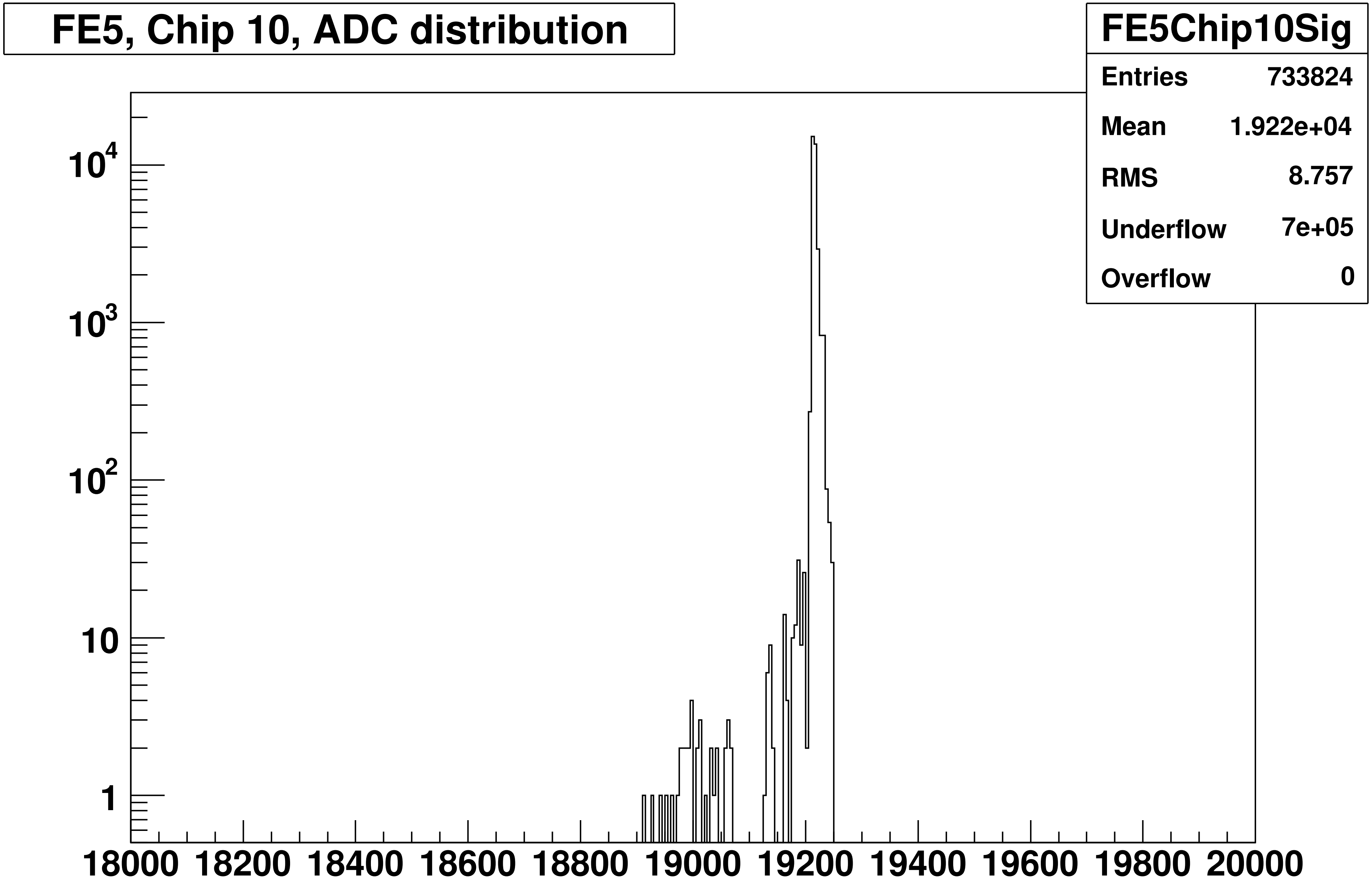
FE5, Chip 10, ADC distribution
FE5Chip10Sig
Entries 733824
Mean 1.922e+04
RMS 8.757
Underflow 7e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
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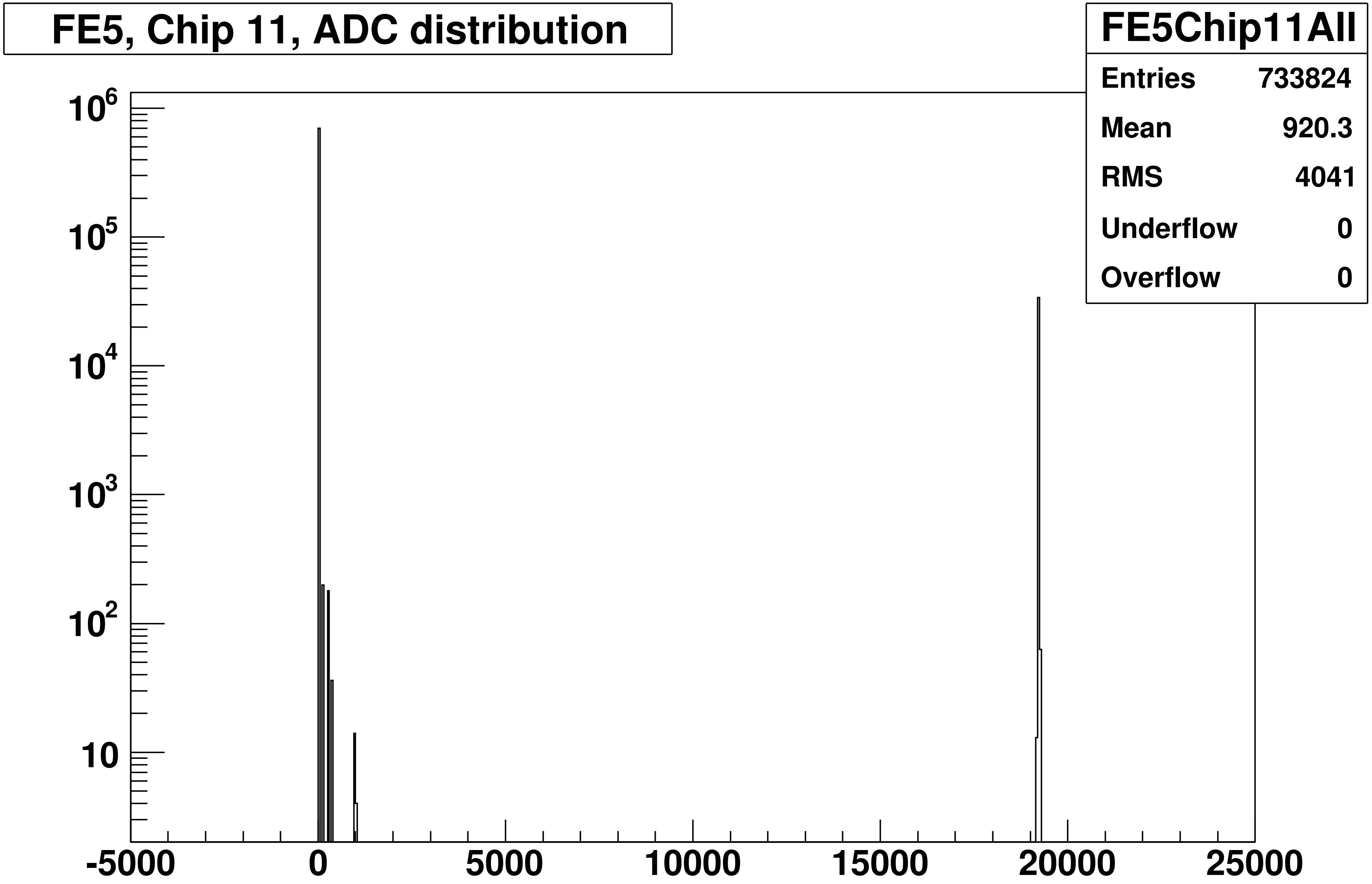
FE5, Chip 11, ADC distribution
FE5Chip11All
Entries 733824
Mean 920.3
RMS 4041
Underflow 0
Overflow 0
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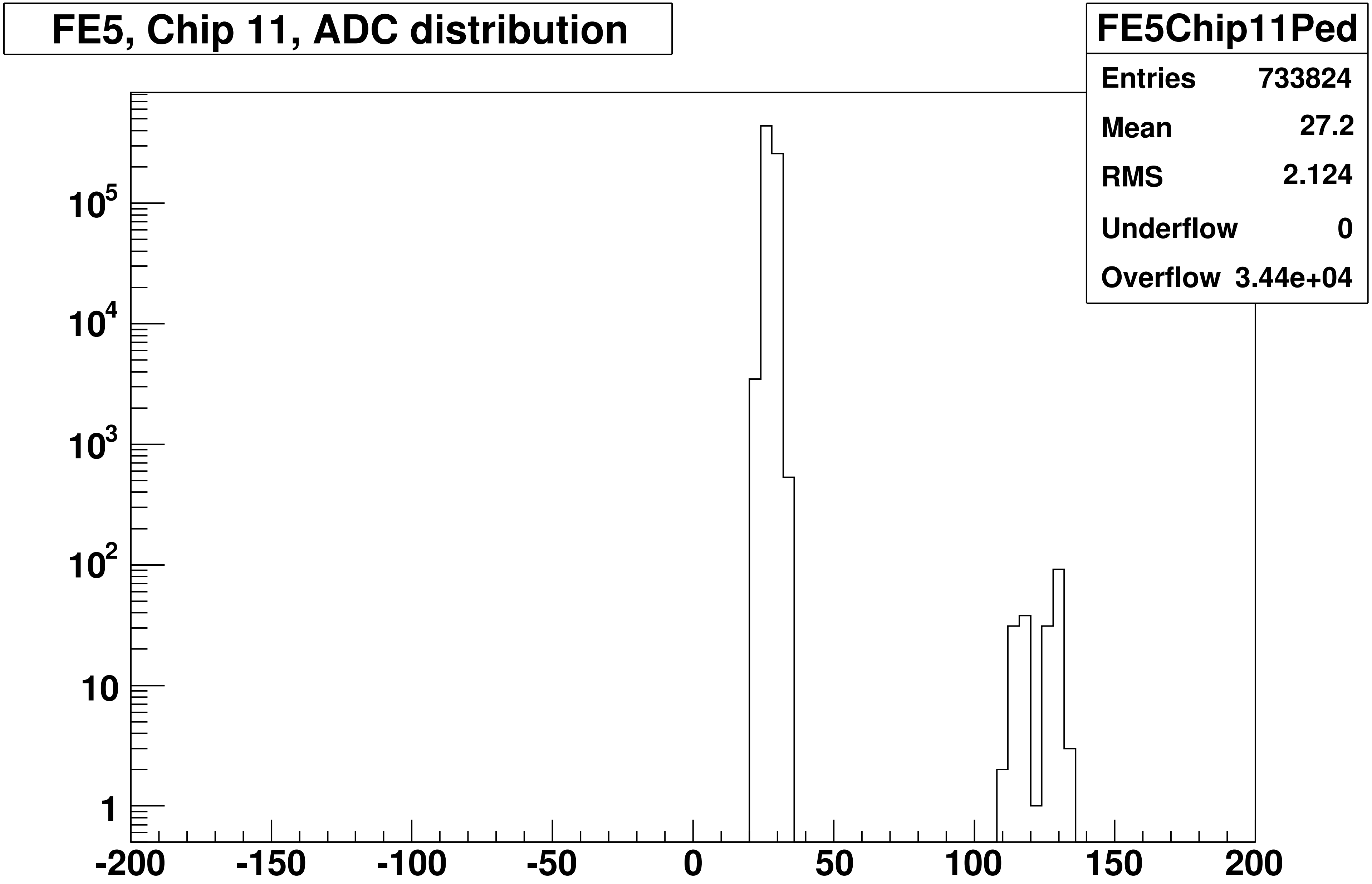
0
5000
10000
15000
20000
25000
10^6
10^5
10^4
10^3
10^2
10



FE5, Chip 11, ADC distribution
FE5Chip11Ped
Entries 733824
Mean 27.2
RMS 2.124
Underflow 0
Overflow 3.44e+04
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10^4
10^3
10^2
10
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0
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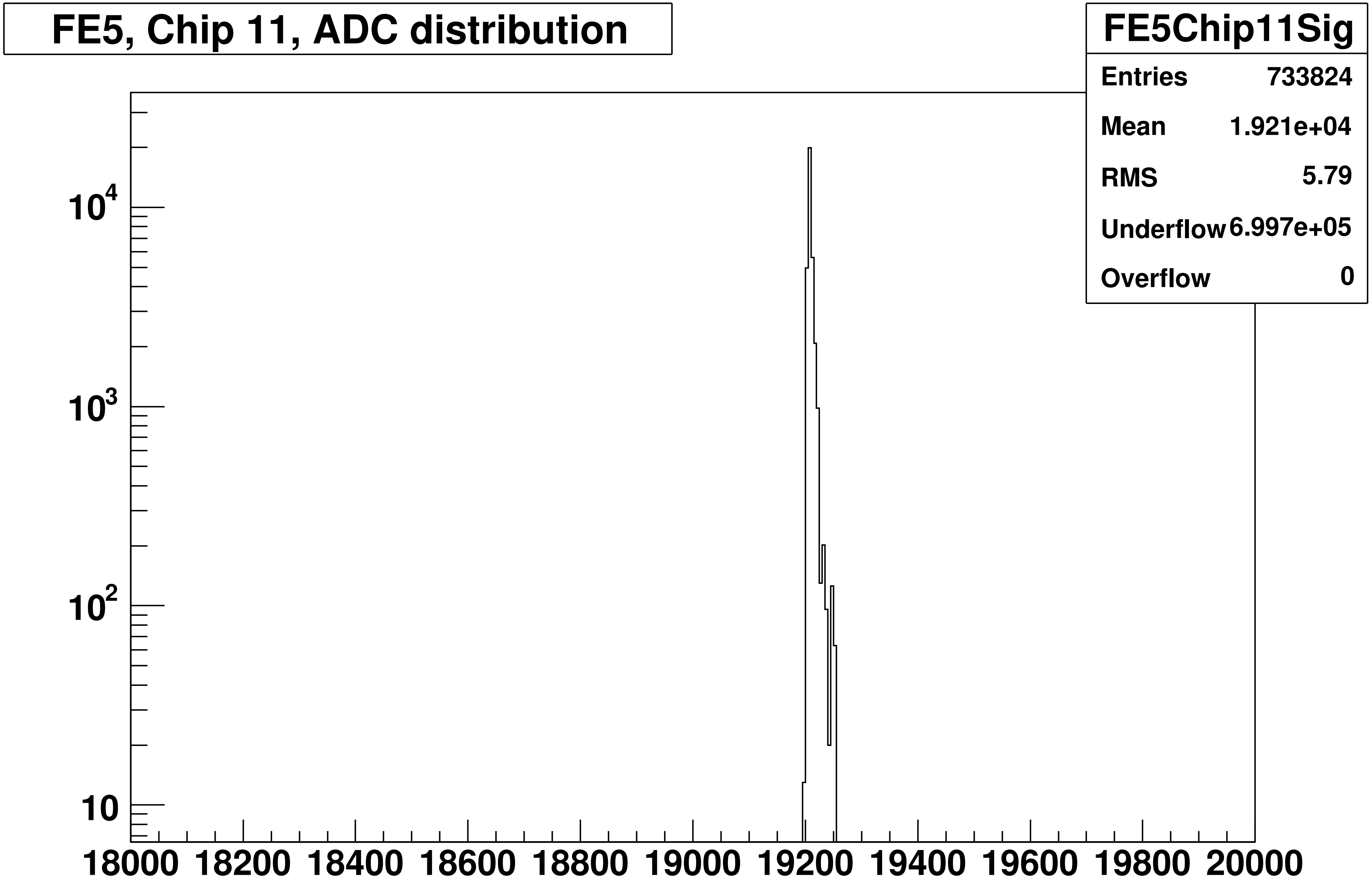
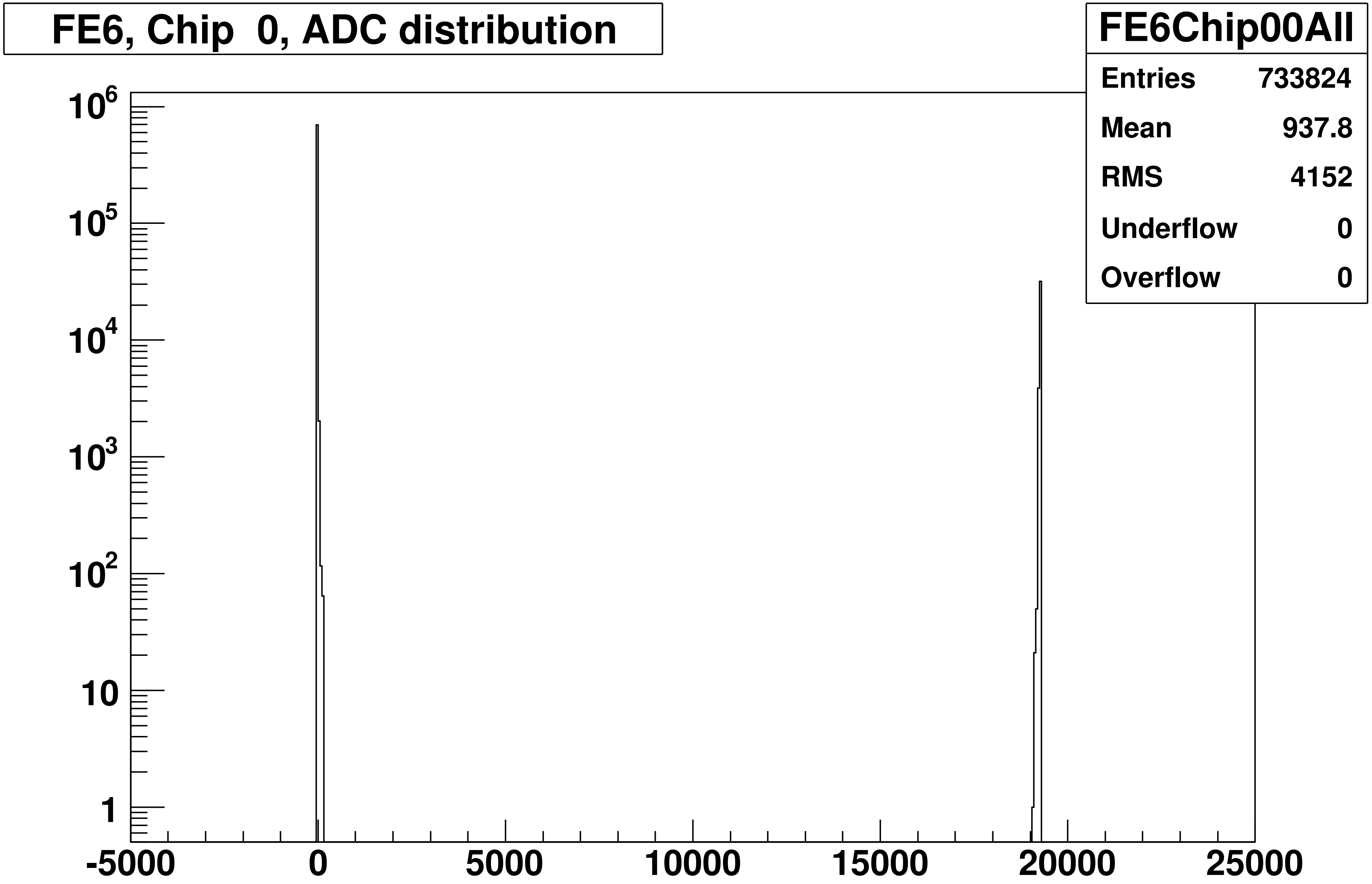
150
200


FE5, Chip 11, ADC distribution
FE5Chip11Sig
Entries 733824
Mean 1.921e+04
RMS 5.79
Underflow 6.997e+05
Overflow 0
10
10^2
10^3
10^4
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE6, Chip 0, ADC distribution
FE6Chip00All
Entries 733824
Mean 937.8
RMS 4152
Underflow 0
Overflow 0
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10^4
10^3
10^2
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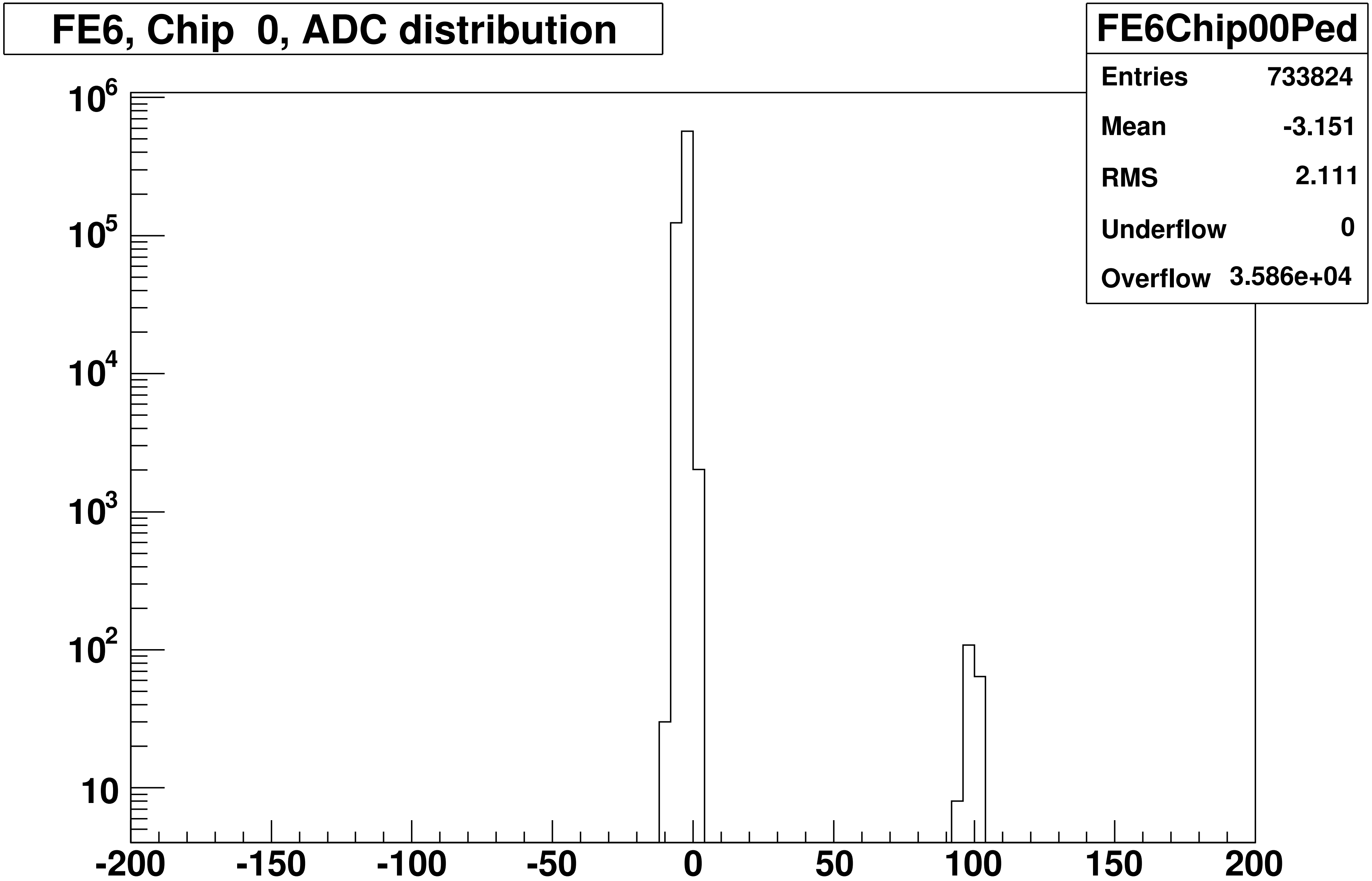
FE6, Chip 0, ADC distribution
FE6Chip00Ped
Entries 733824
Mean -3.151
RMS 2.111
Underflow 0
Overflow 3.586e+04
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10^4
10^3
10^2
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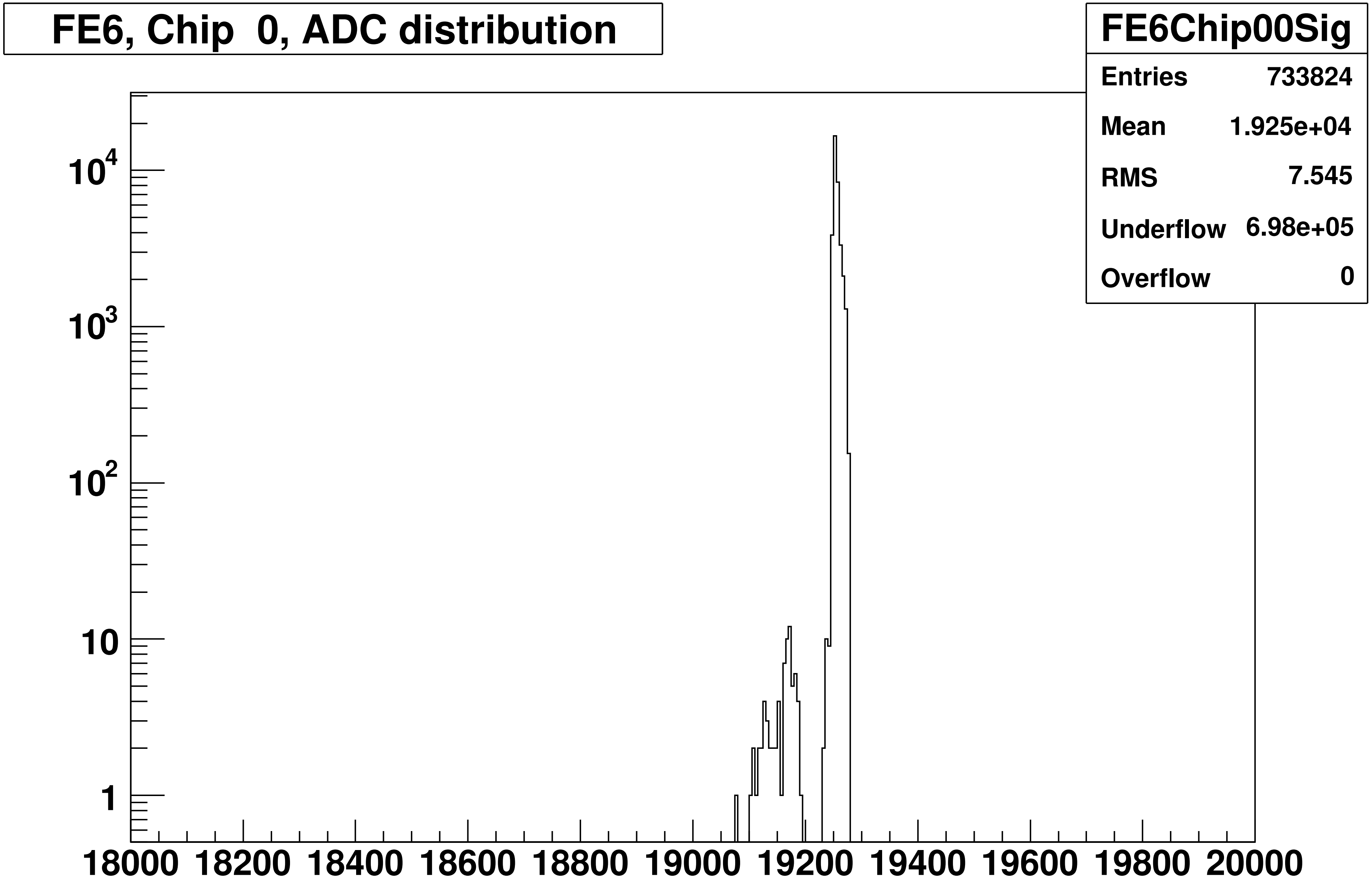

FE6, Chip 0, ADC distribution
FE6Chip00Sig
Entries 733824
Mean 1.925e+04
RMS 7.545
Underflow 6.98e+05
Overflow 0
10^4
10^3
10^2
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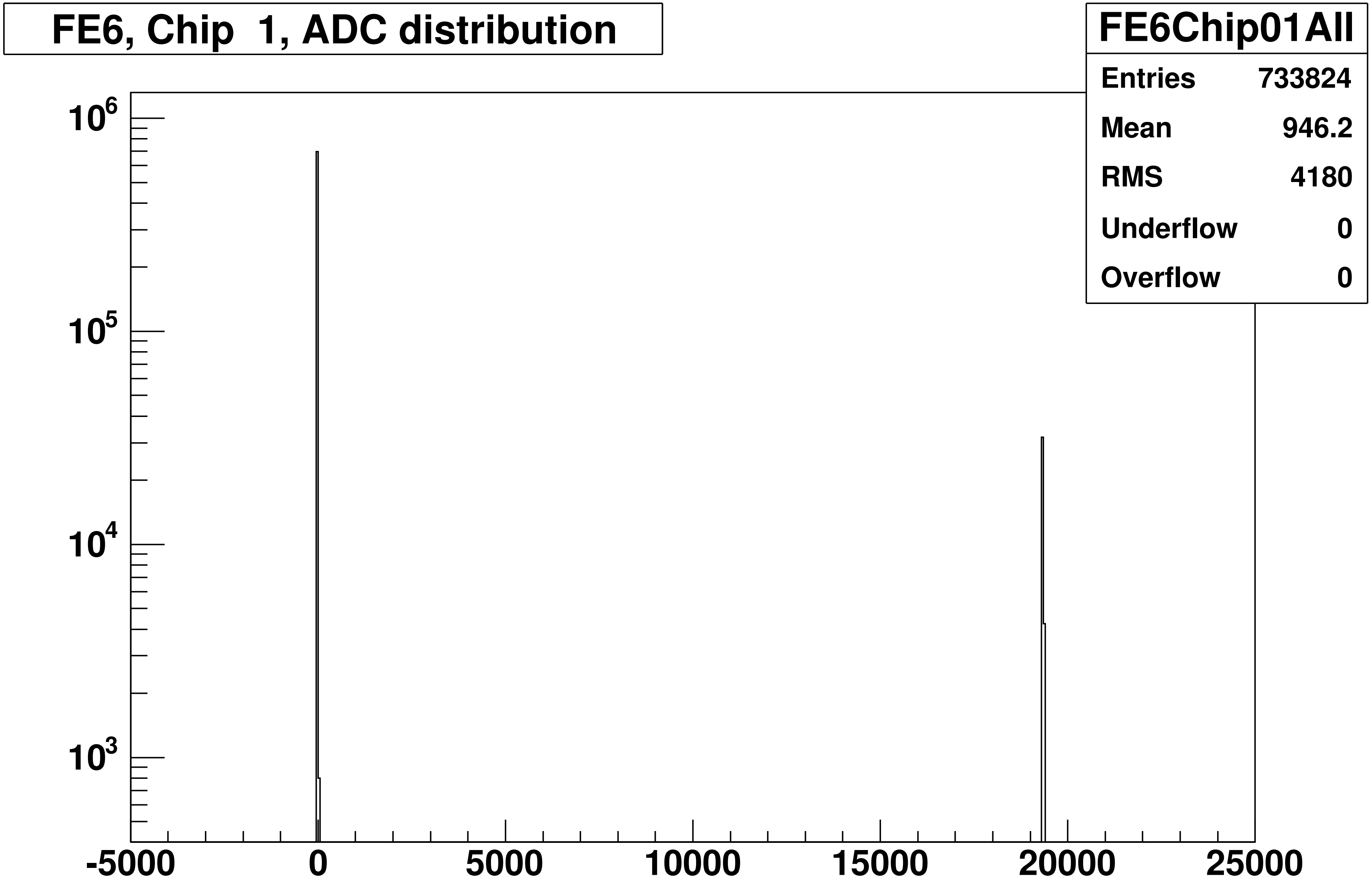

FE6, Chip 1, ADC distribution
FE6Chip01All
Entries 733824
Mean 946.2
RMS 4180
Underflow 0
Overflow 0
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10^4
10^3
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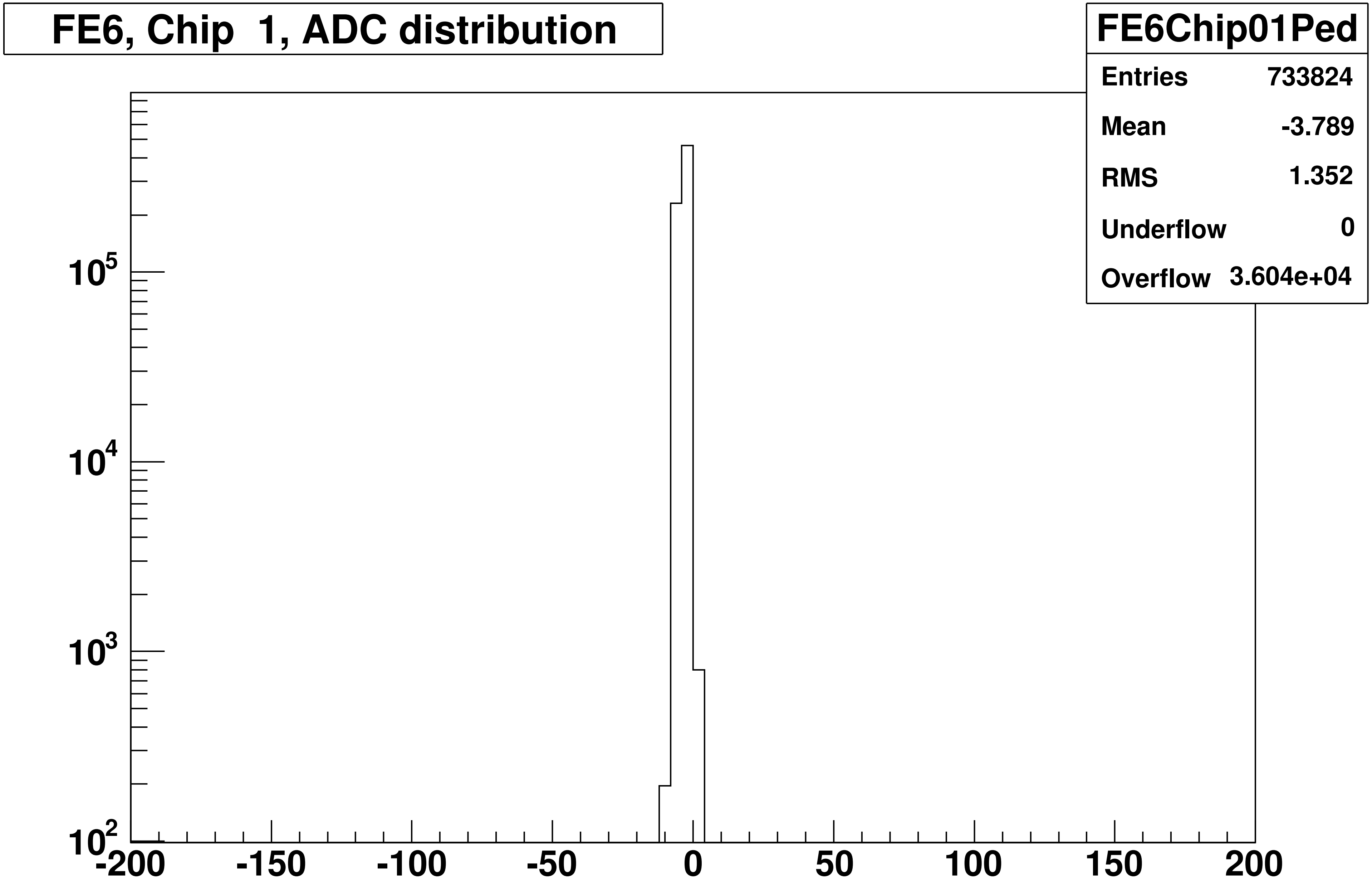
25000



FE6, Chip 1, ADC distribution
FE6Chip01Ped
Entries 733824
Mean -3.789
RMS 1.352
Underflow 0
Overflow 3.604e+04
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10^4
10^3
10^2
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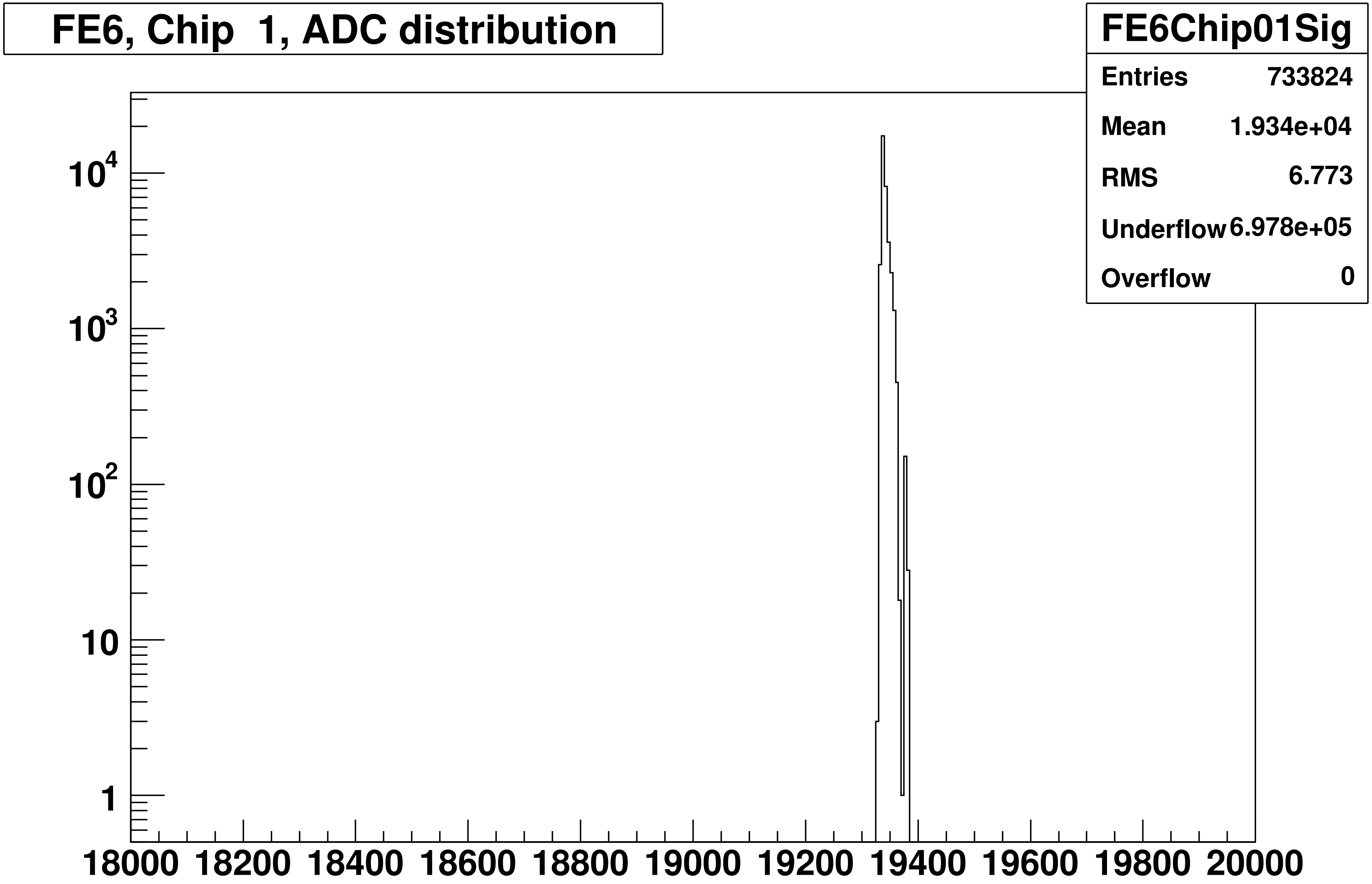

FE6, Chip 1, ADC distribution
FE6Chip01Sig
Entries 733824
Mean 1.934e+04
RMS 6.773
Underflow 6.978e+05
Overflow 0
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10^3
10^2
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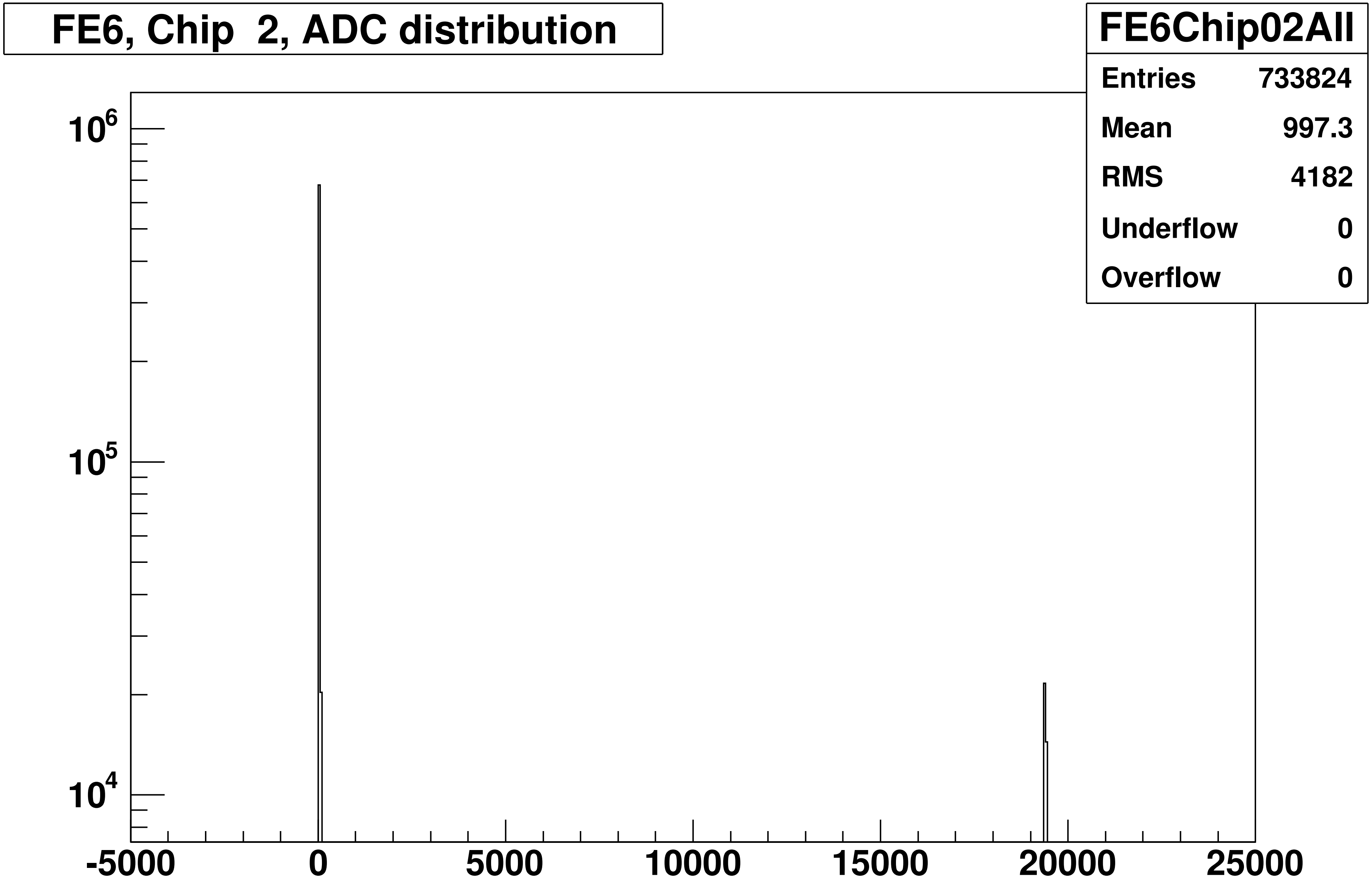
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE6, Chip 2, ADC distribution
FE6Chip02All
Entries 733824
Mean 997.3
RMS 4182
Underflow 0
Overflow 0
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10^5
10^4
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0
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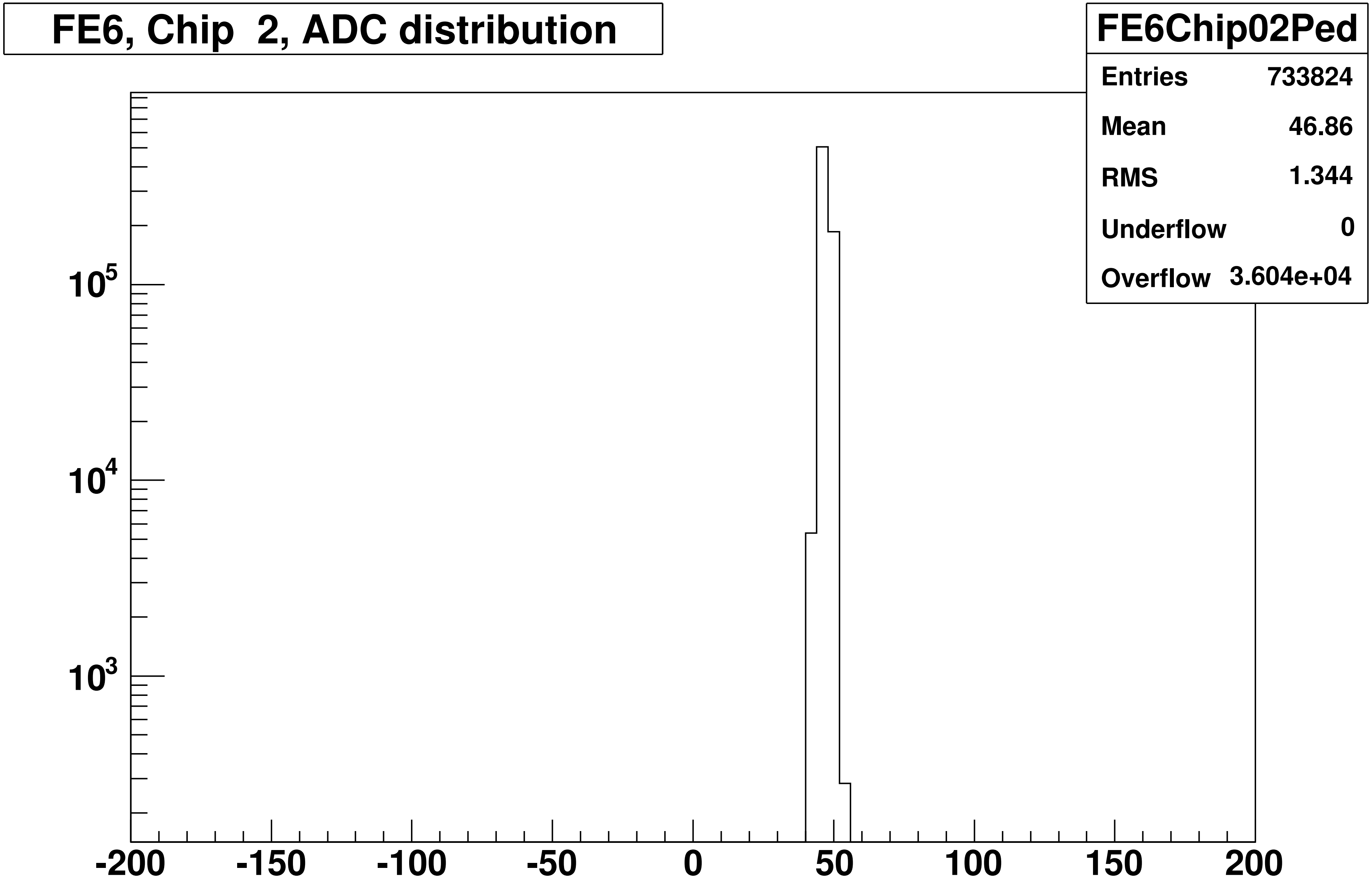
15000
20000
25000


FE6, Chip 2, ADC distribution
FE6Chip02Ped
Entries 733824
Mean 46.86
RMS 1.344
Underflow 0
Overflow 3.604e+04
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10^4
10^3
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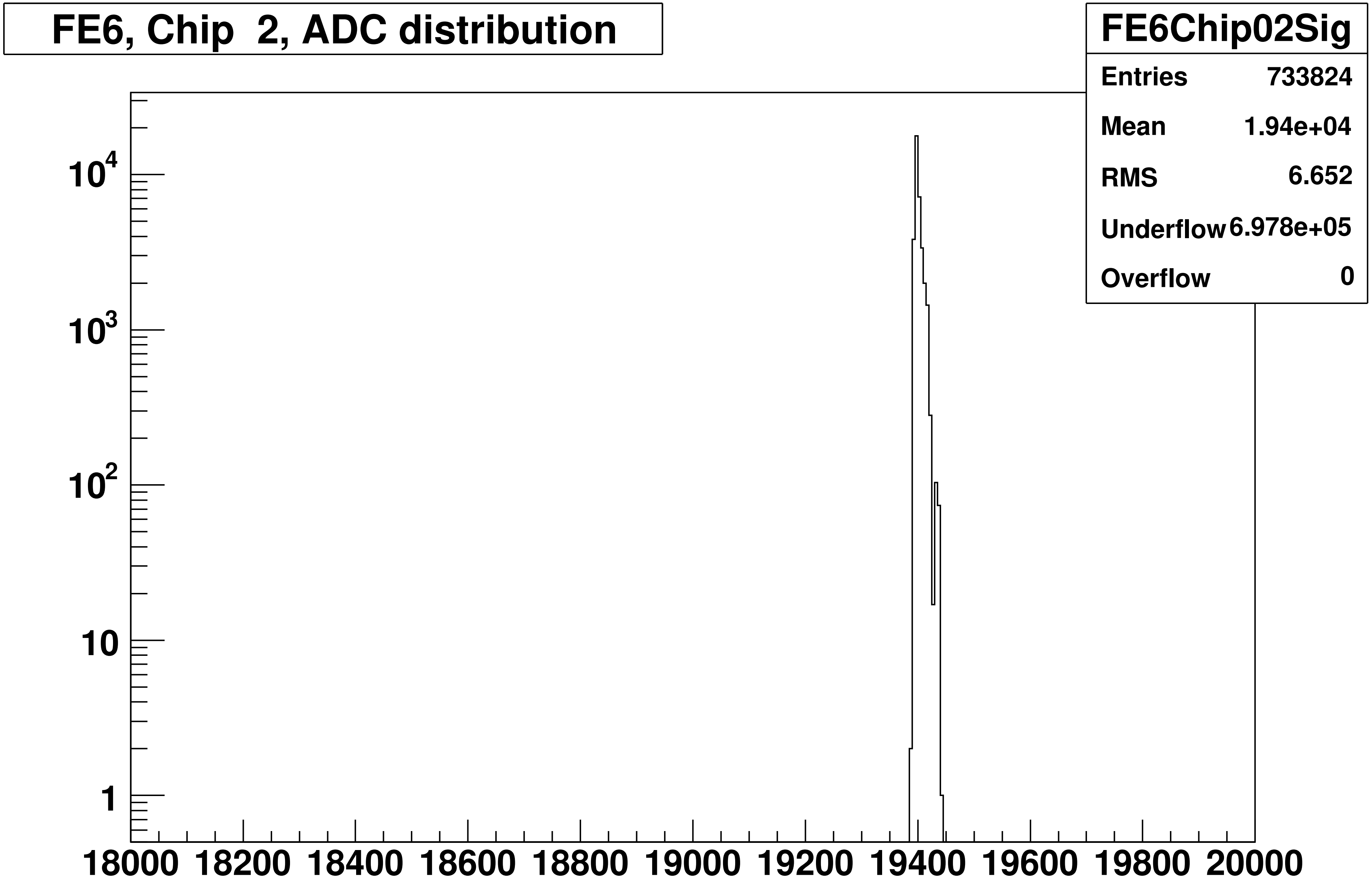
FE6, Chip 2, ADC distribution
FE6Chip02Sig
Entries 733824
Mean 1.94e+04
RMS 6.652
Underflow 6.978e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
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18400
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19000
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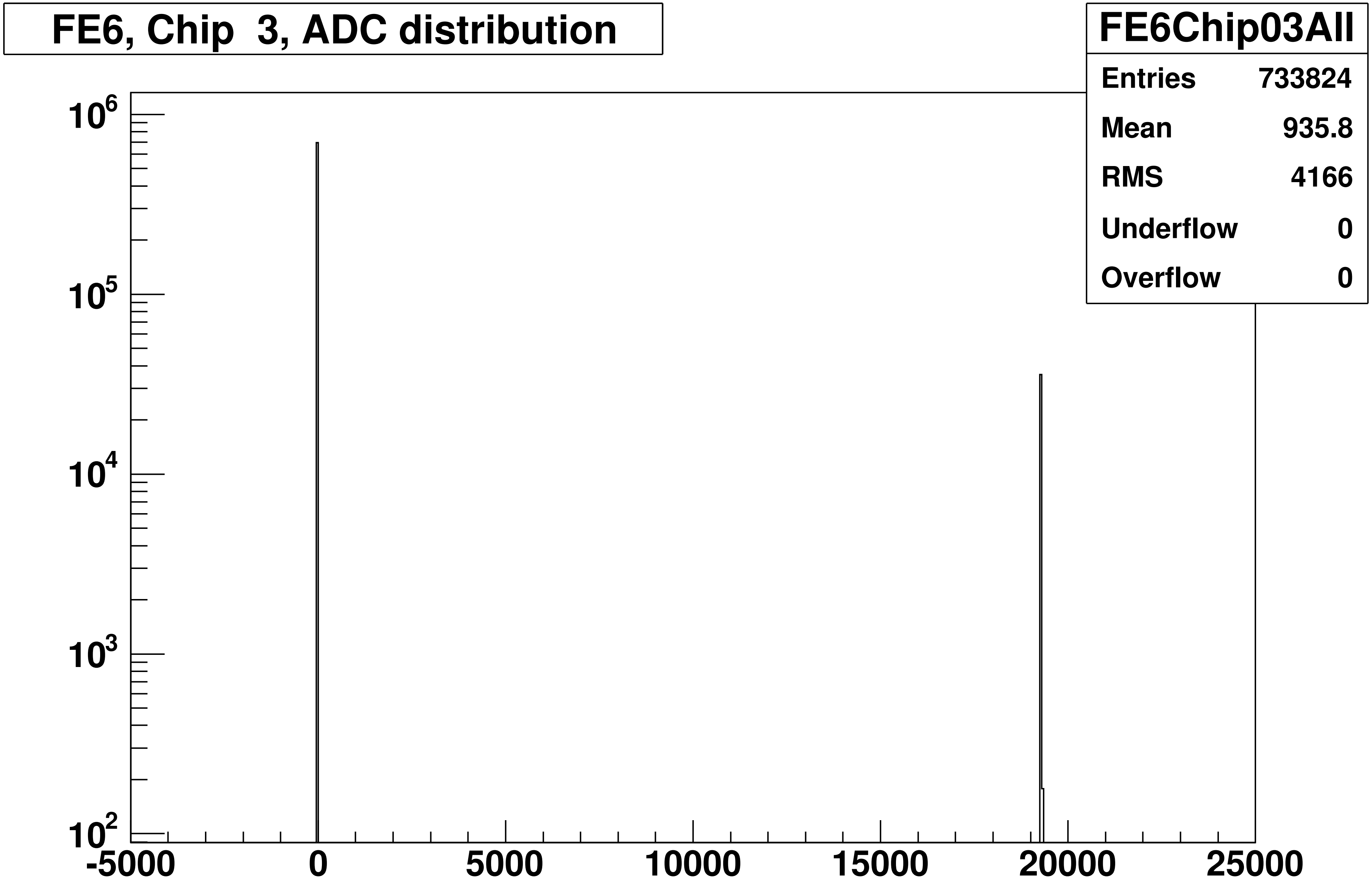
19800
20000



FE6, Chip 3, ADC distribution
FE6Chip03All
Entries 733824
Mean 935.8
RMS 4166
Underflow 0
Overflow 0
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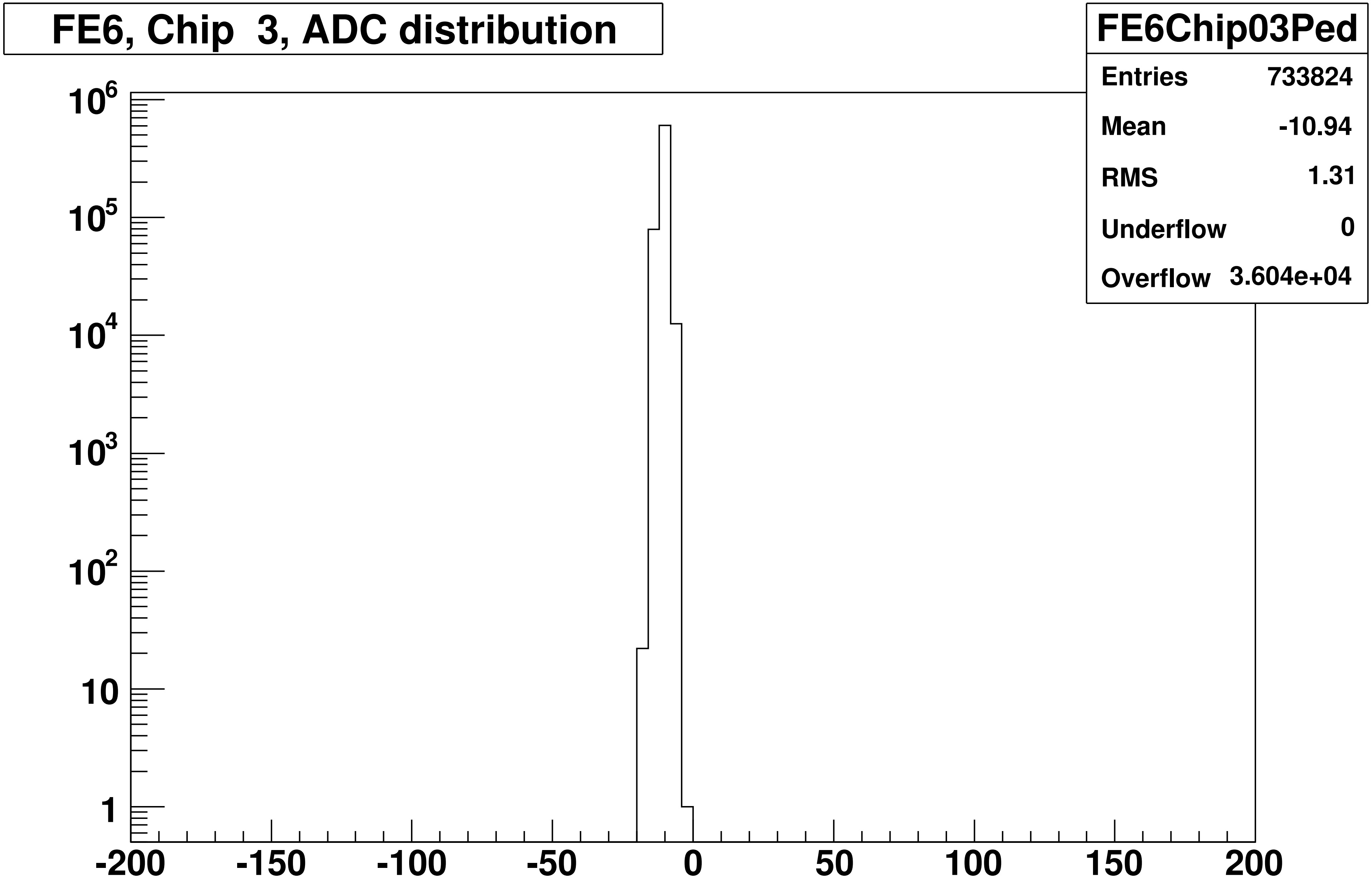

FE6, Chip 3, ADC distribution
FE6Chip03Ped
Entries 733824
Mean -10.94
RMS 1.31
Underflow 0
Overflow 3.604e+04
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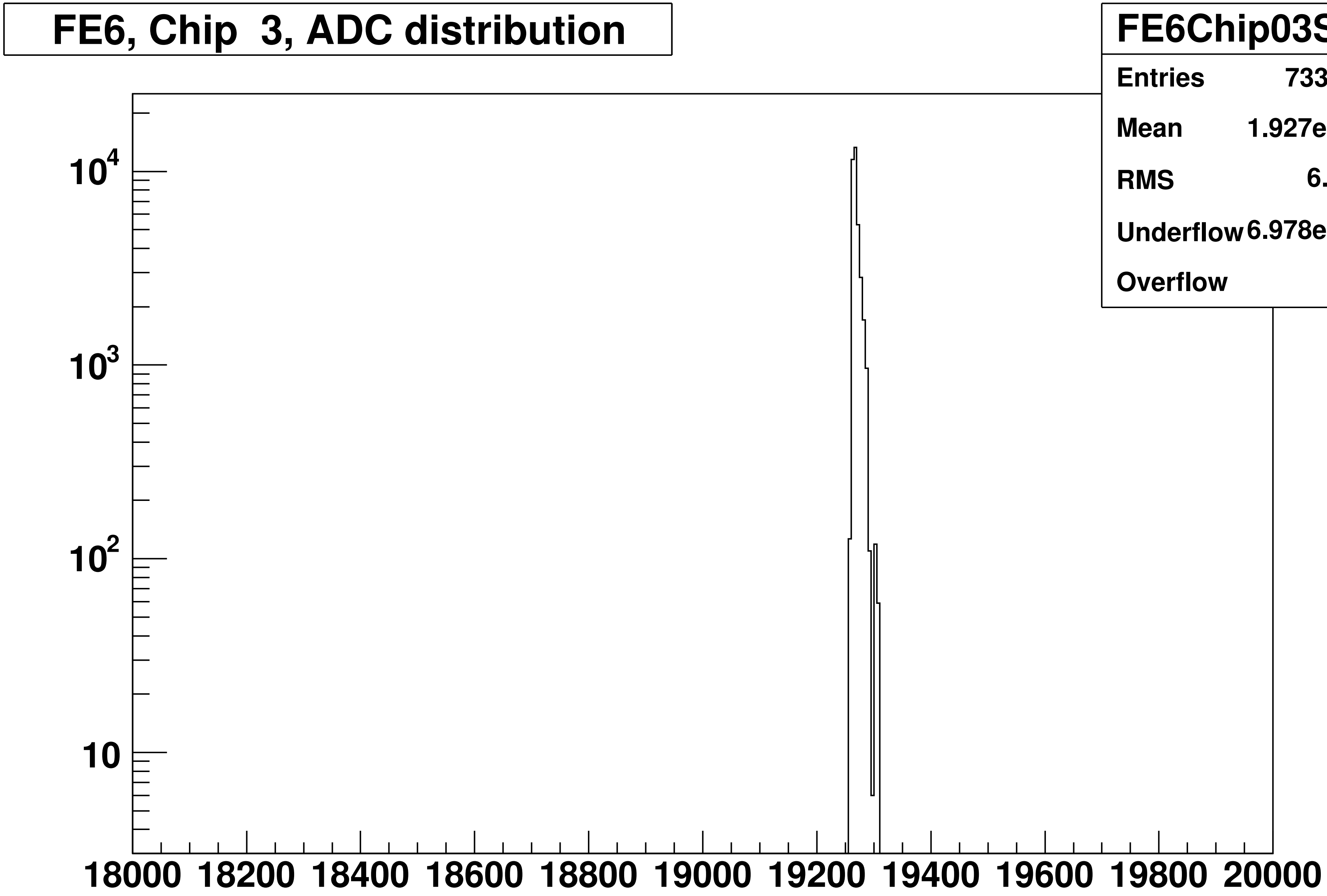
FE6, Chip 3, ADC distribution
FE6Chip03Sig
Entries 733824
Mean 1.927e+04
RMS 6.709
Underflow 6.978e+05
Overflow 0
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10^3
10^2
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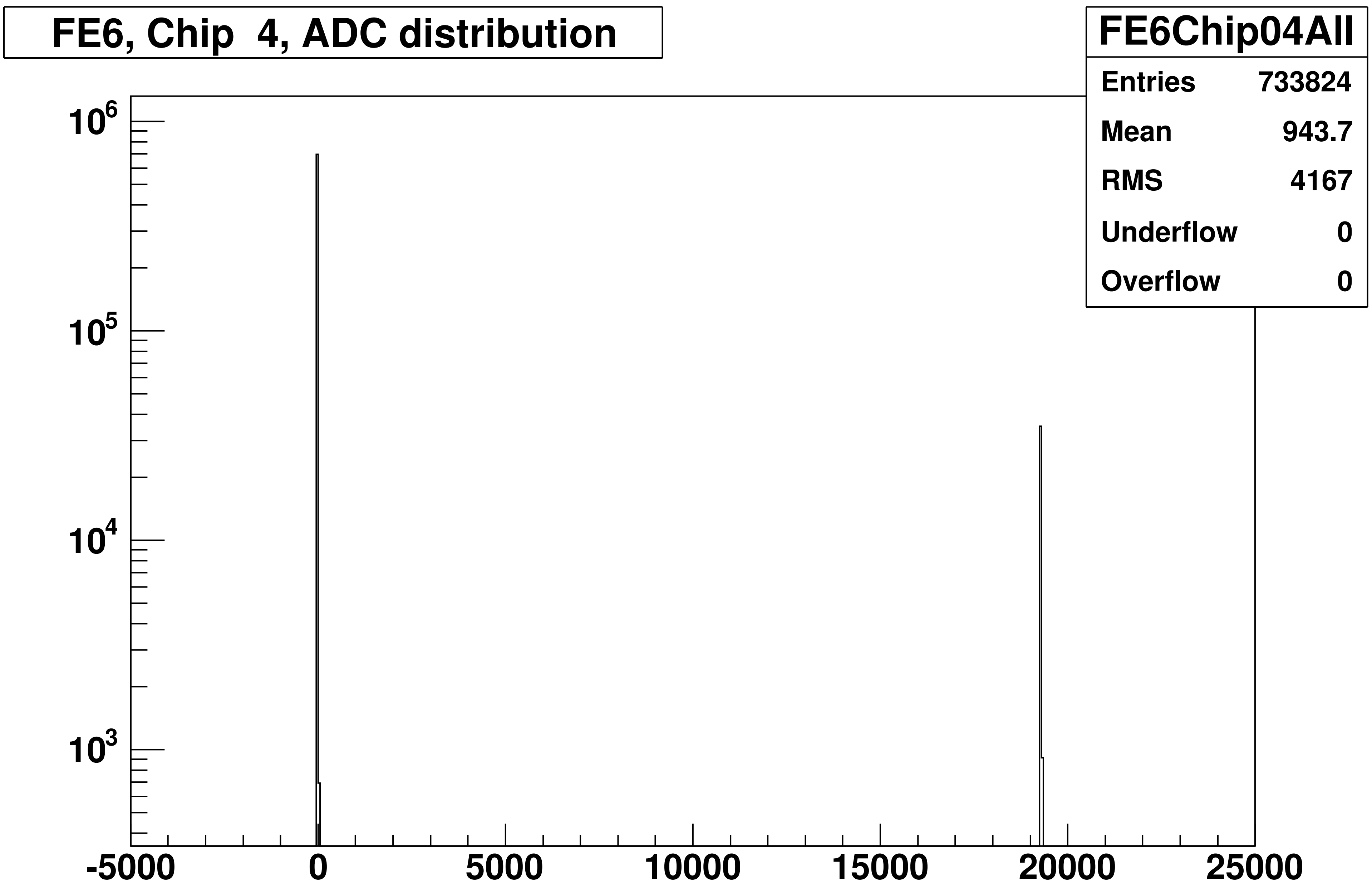
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE6, Chip 4, ADC distribution
FE6Chip04All
Entries 733824
Mean 943.7
RMS 4167
Underflow 0
Overflow 0
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10^4
10^3
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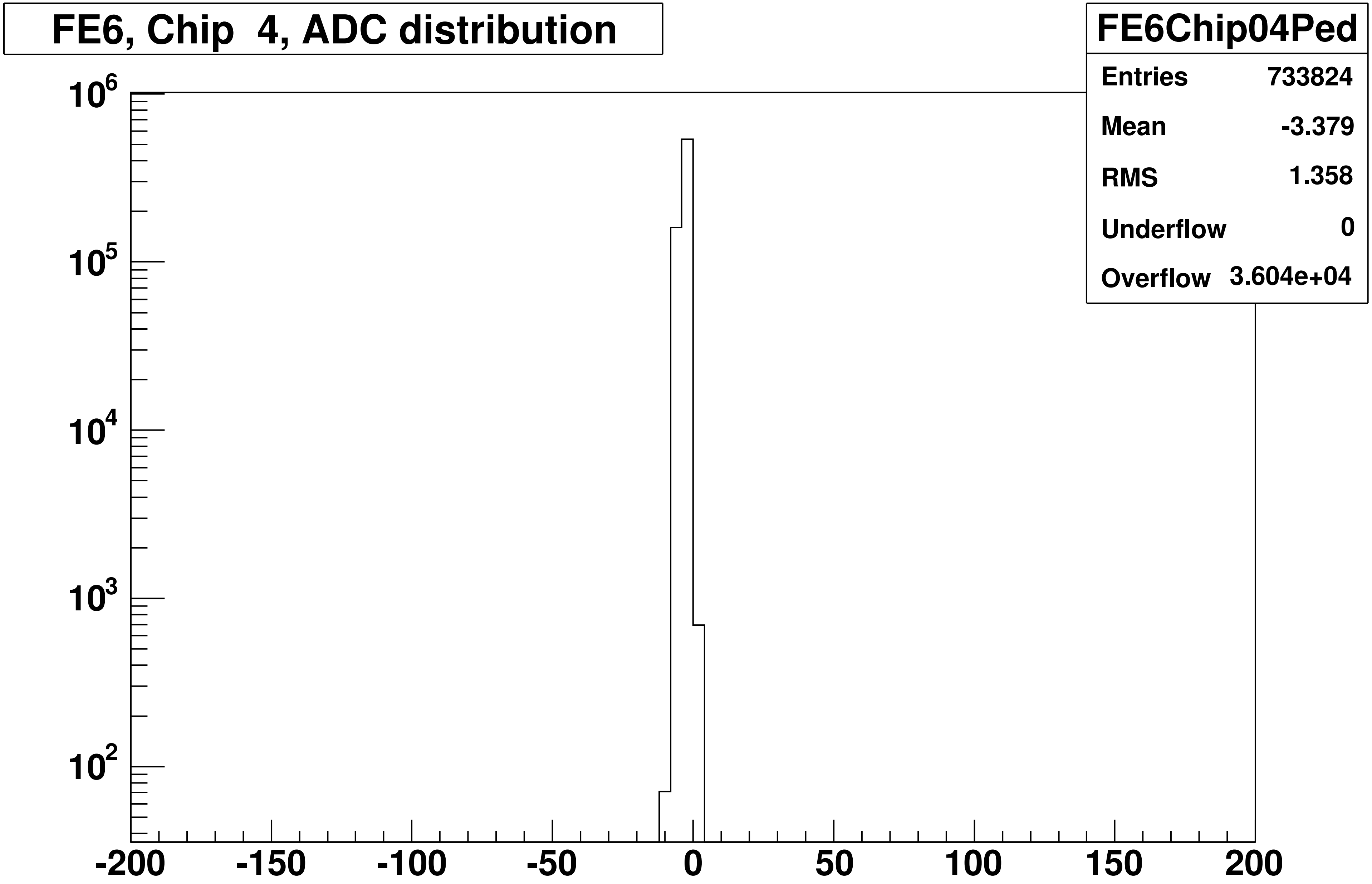

FE6, Chip 4, ADC distribution
FE6Chip04Ped
Entries 733824
Mean -3.379
RMS 1.358
Underflow 0
Overflow 3.604e+04
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10^3
10^2
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150
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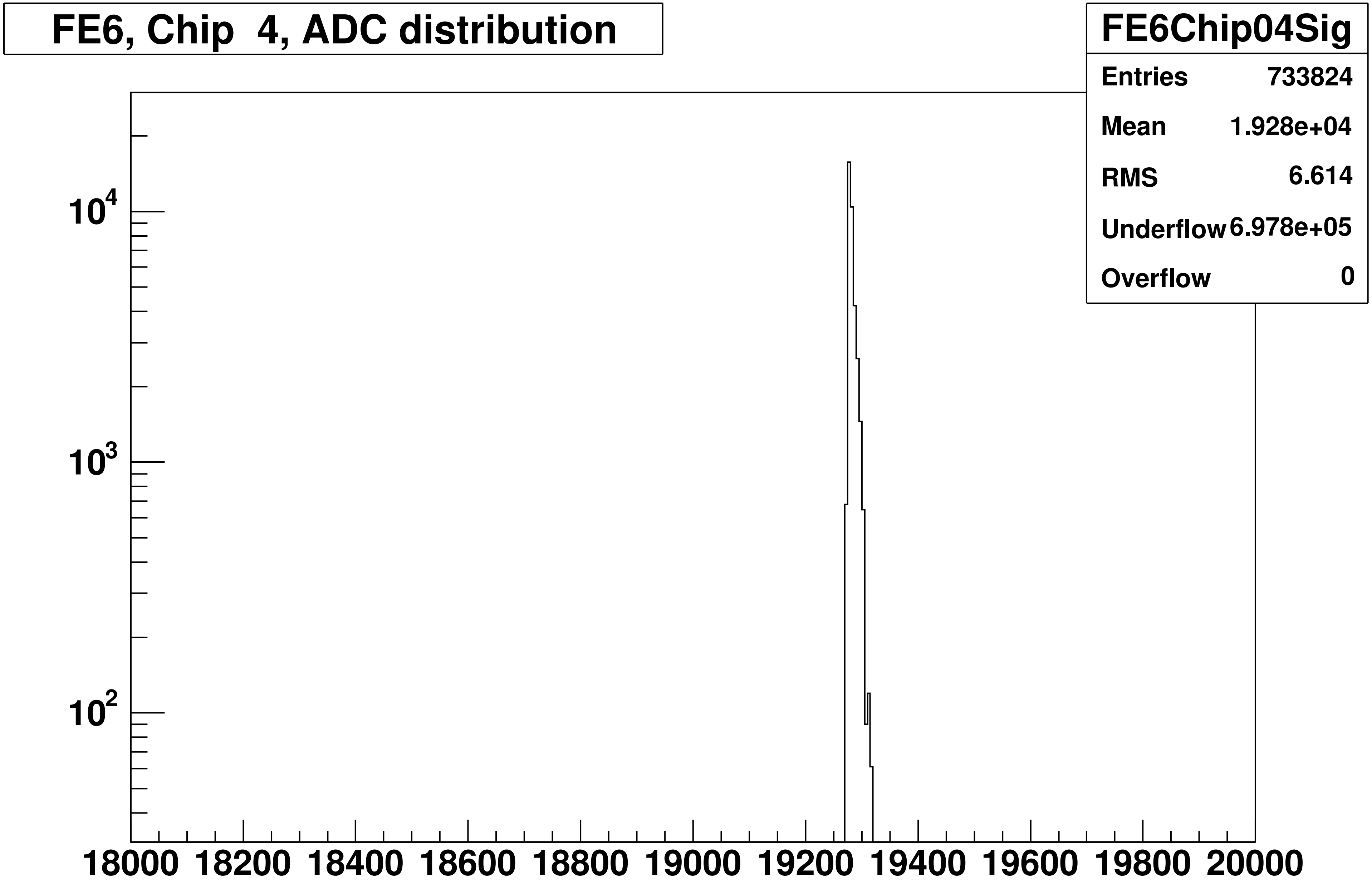

FE6, Chip 4, ADC distribution
FE6Chip04Sig
Entries 733824
Mean 1.928e+04
RMS 6.614
Underflow 6.978e+05
Overflow 0
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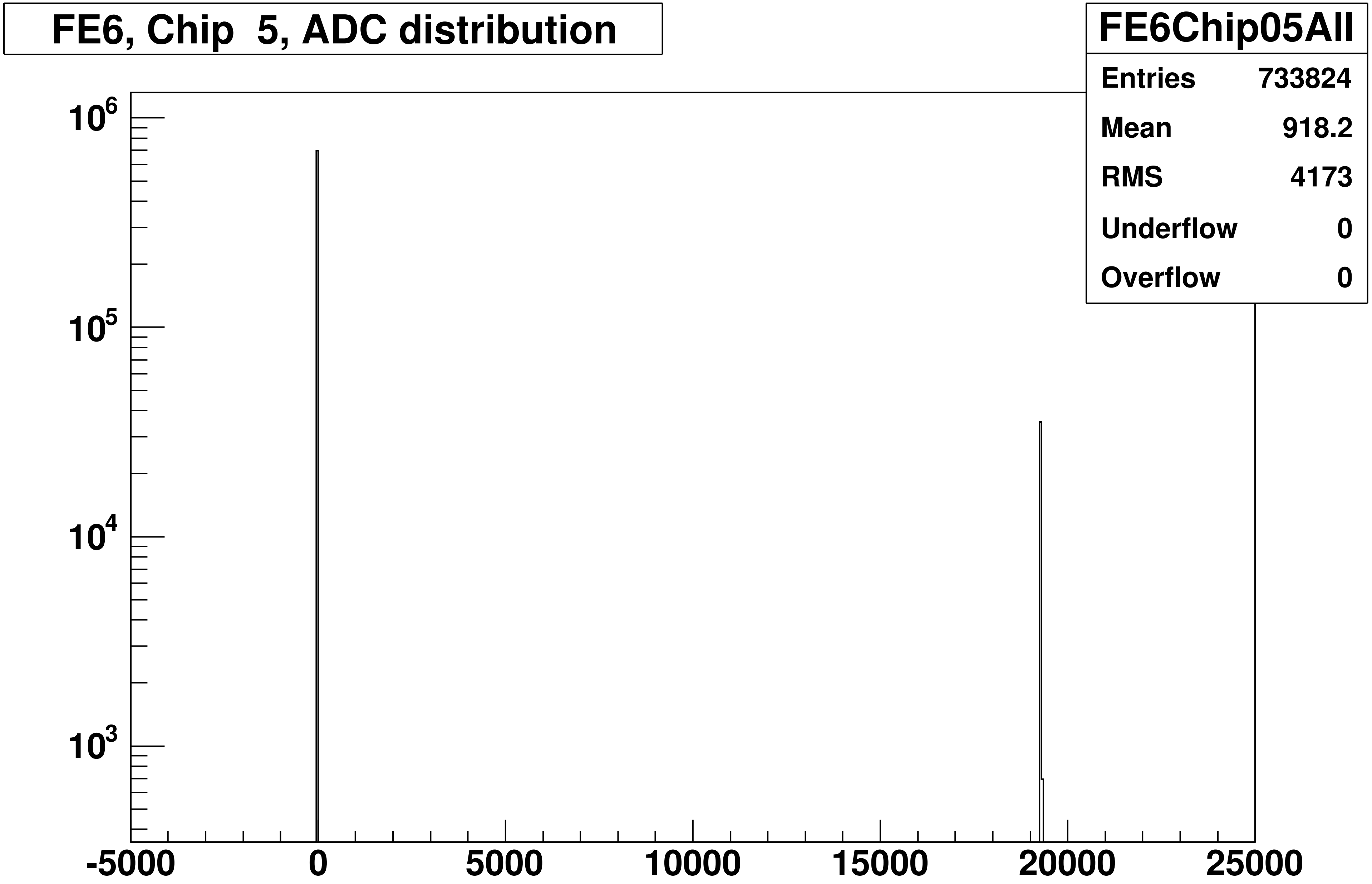
10^3
10^2
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE6, Chip 5, ADC distribution
FE6Chip05All
Entries 733824
Mean 918.2
RMS 4173
Underflow 0
Overflow 0
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10^3
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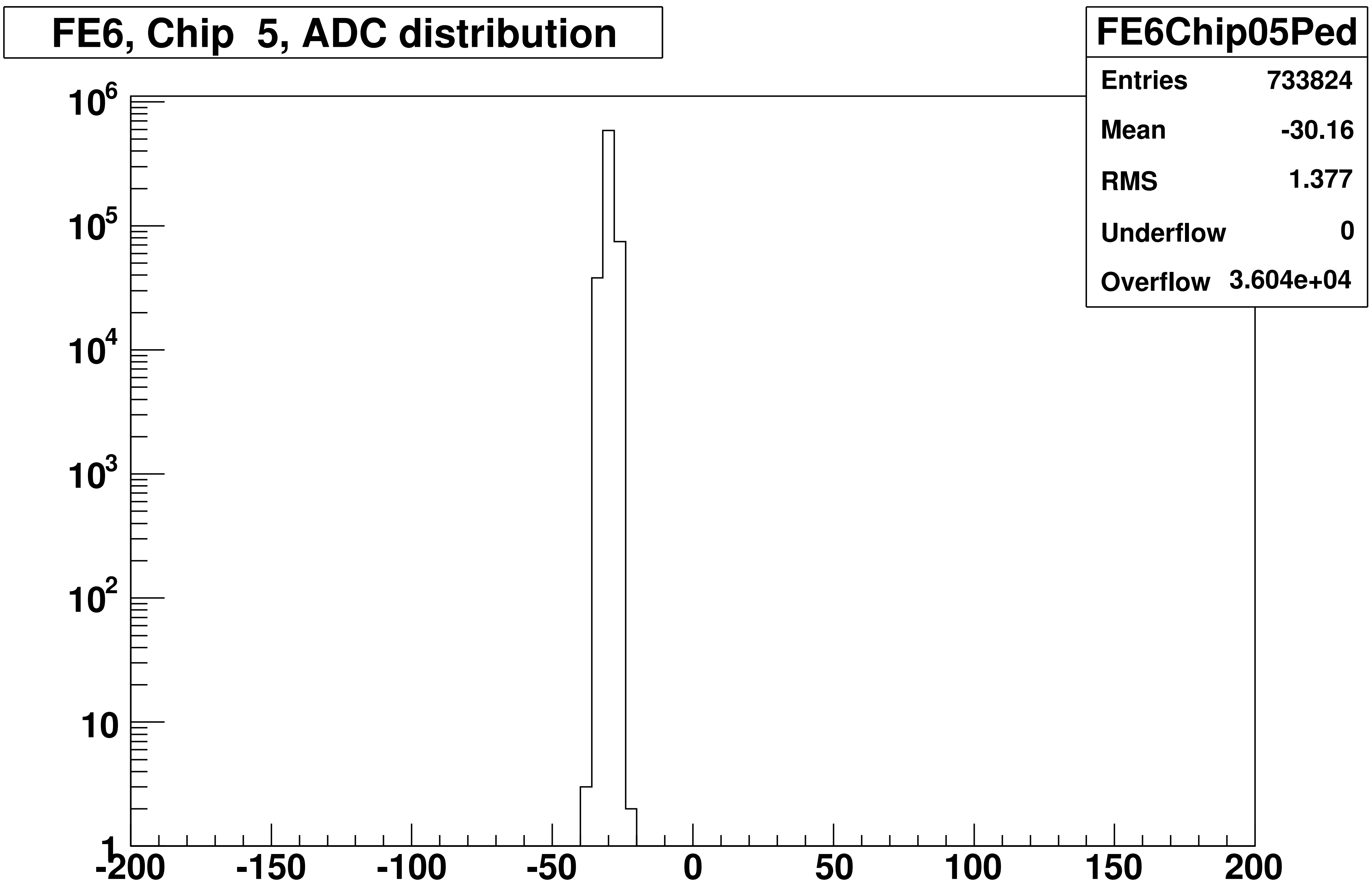
25000



FE6, Chip 5, ADC distribution
FE6Chip05Ped
Entries 733824
Mean -30.16
RMS 1.377
Underflow 0
Overflow 3.604e+04
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10^5
10^4
10^3
10^2
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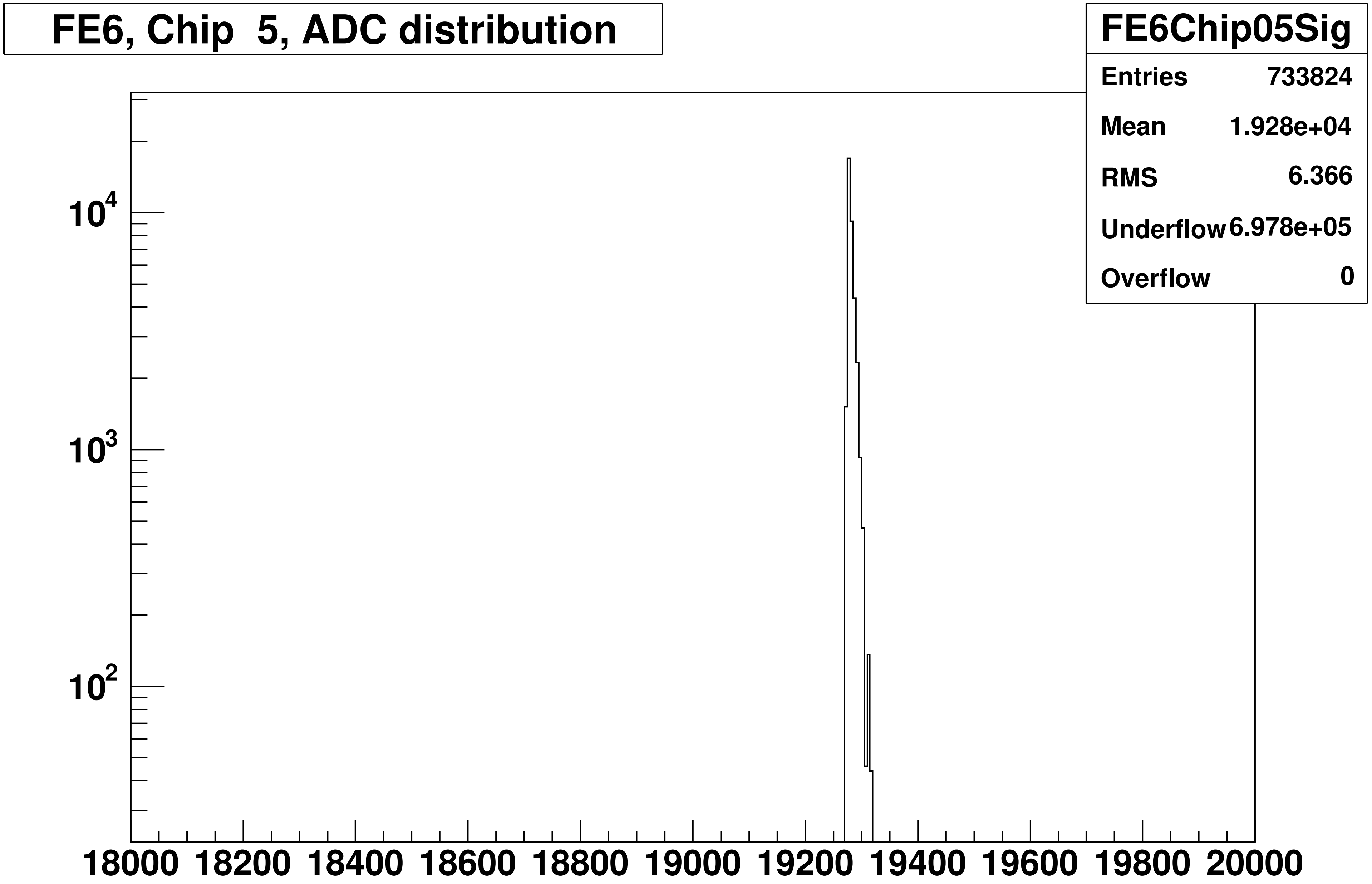
50
100
150
200


FE6, Chip 5, ADC distribution
FE6Chip05Sig
Entries 733824
Mean 1.928e+04
RMS 6.366
Underflow 6.978e+05
Overflow 0
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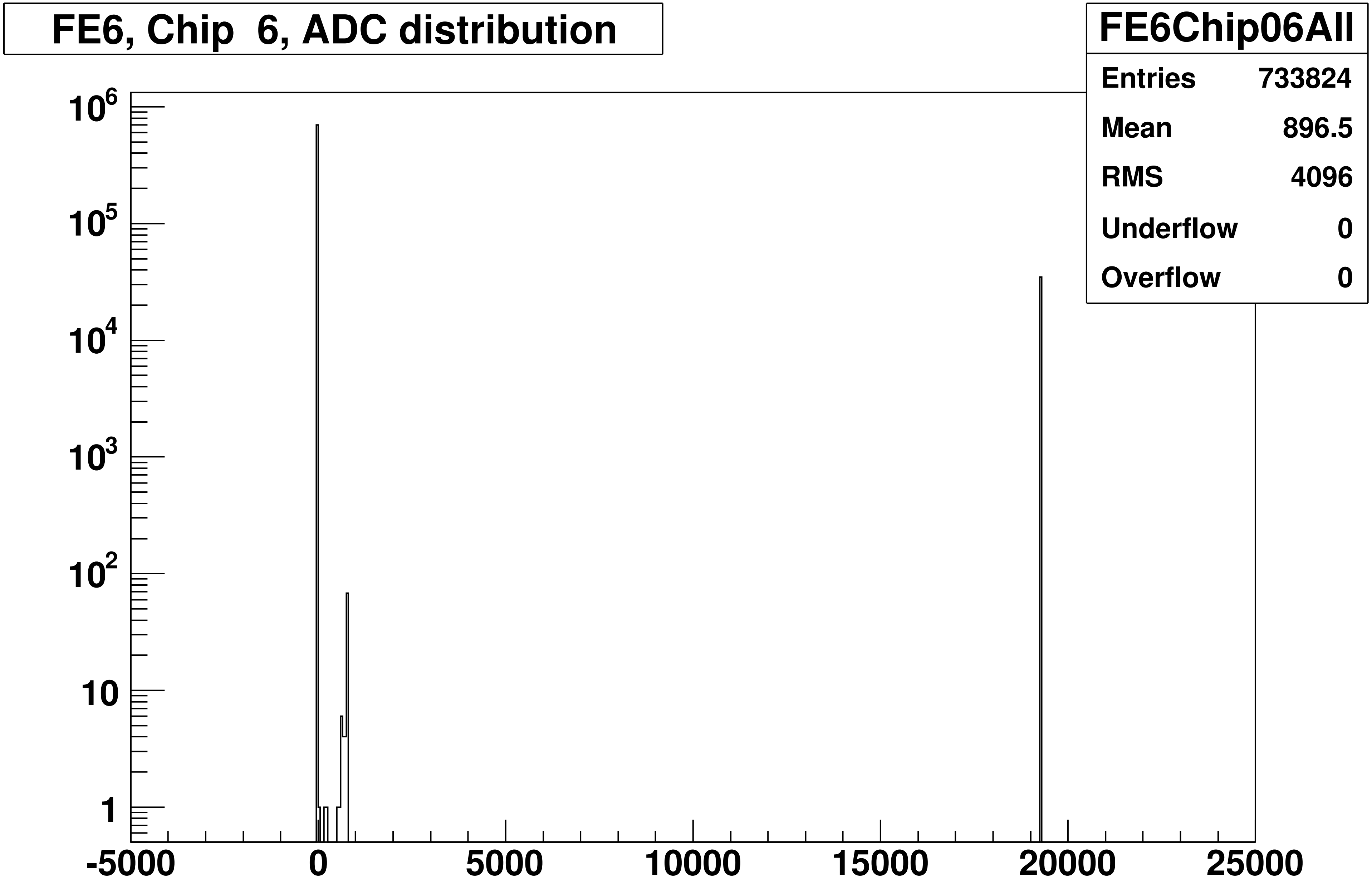
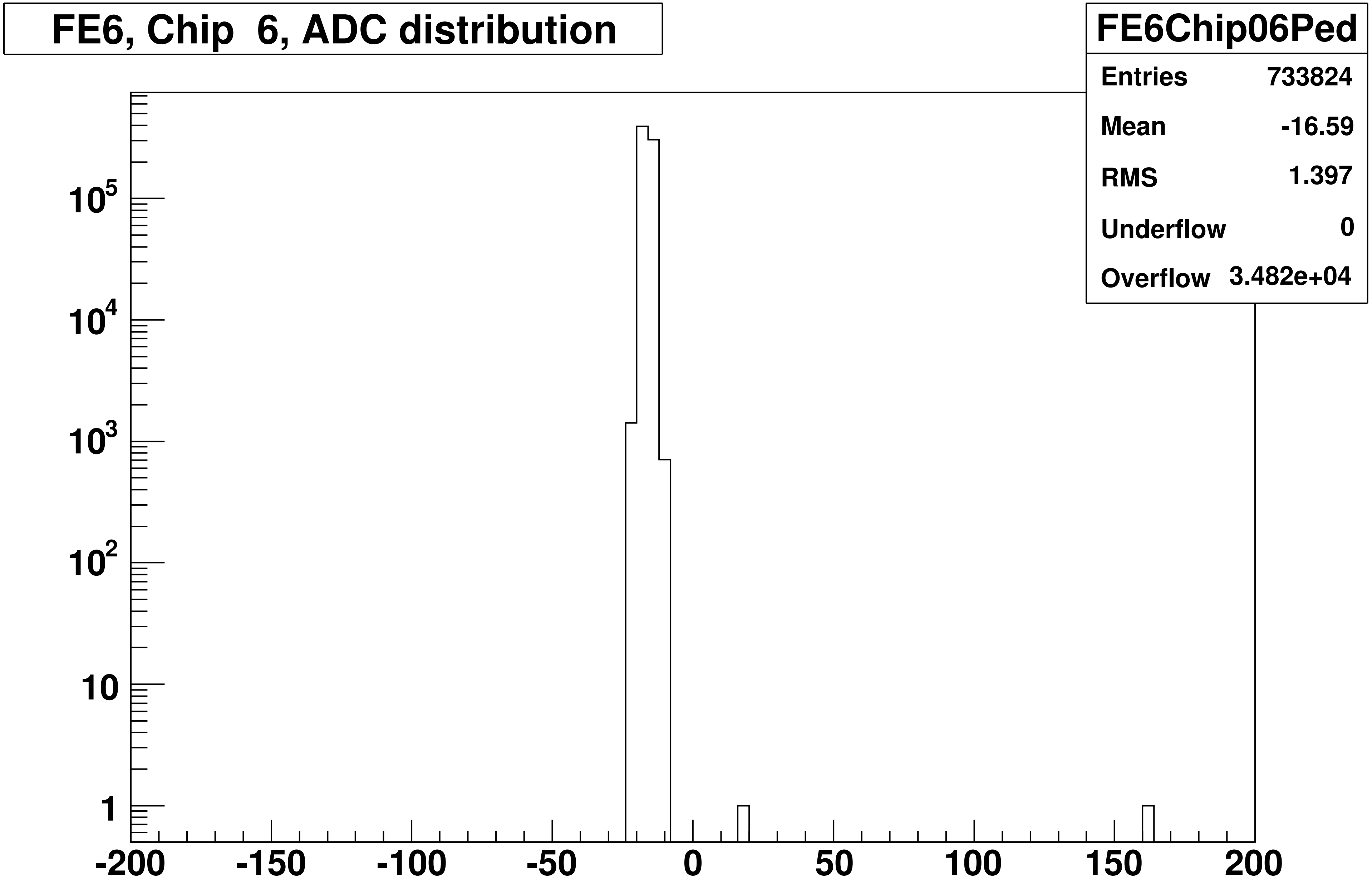
10^3
10^2
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE6, Chip 6, ADC distribution
FE6Chip06All
Entries 733824
Mean 896.5
RMS 4096
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE6, Chip 6, ADC distribution
FE6Chip06Ped
Entries 733824
Mean -16.59
RMS 1.397
Underflow 0
Overflow 3.482e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
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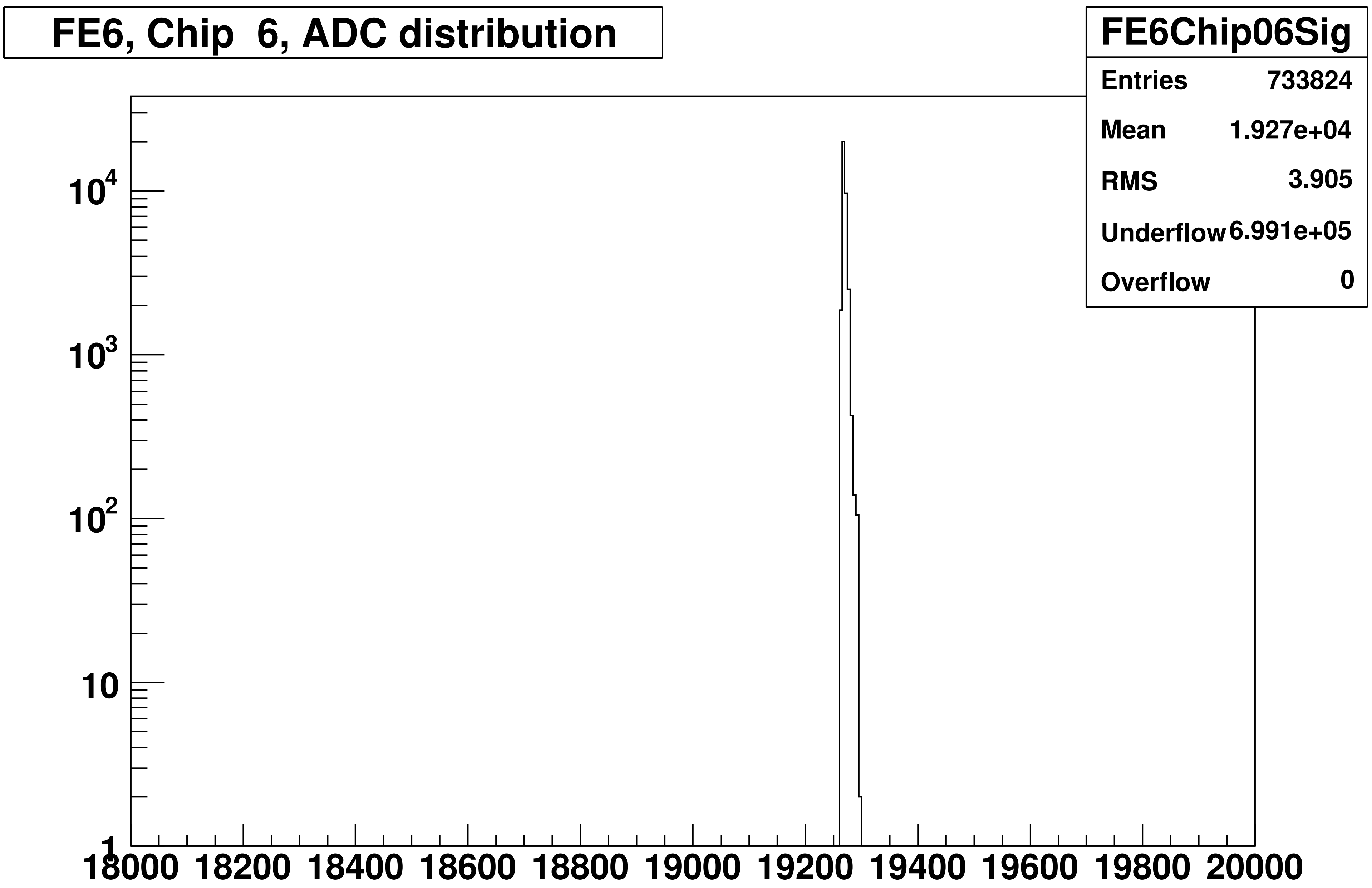
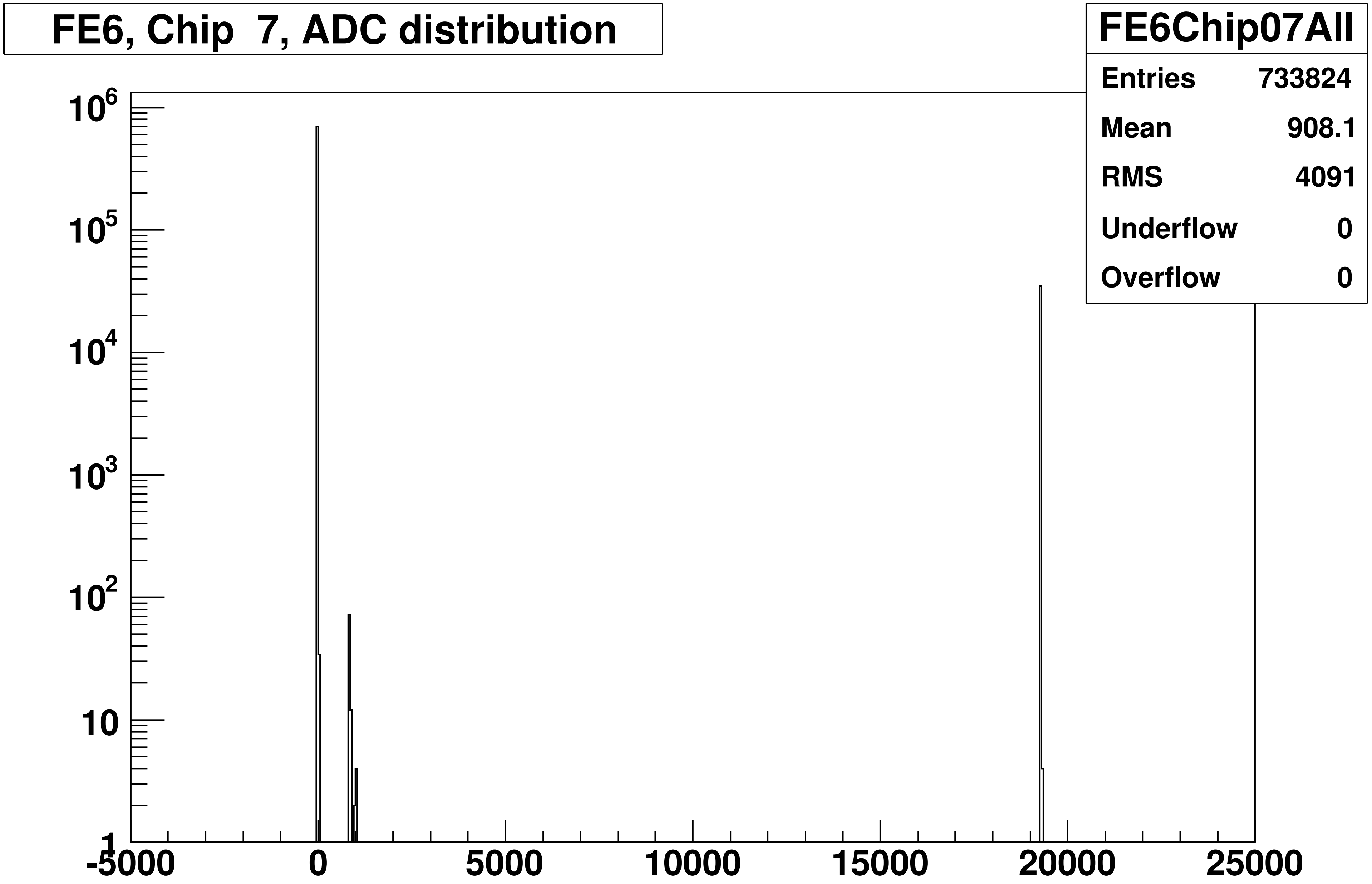
100
150
200



FE6, Chip 6, ADC distribution
FE6Chip06Sig
Entries 733824
Mean 1.927e+04
RMS 3.905
Underflow 6.991e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE6, Chip 7, ADC distribution
FE6Chip07All
Entries 733824
Mean 908.1
RMS 4091
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
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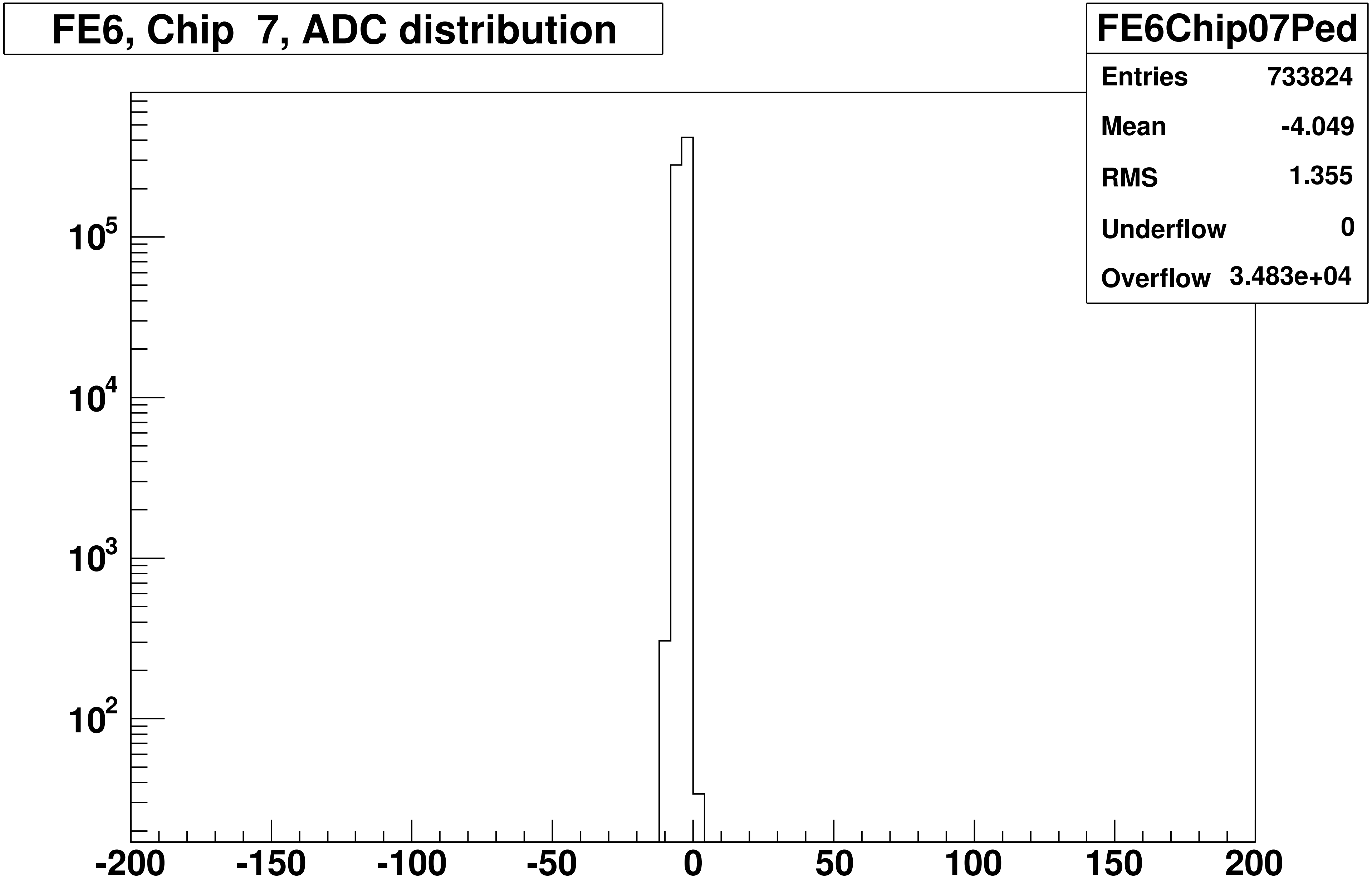
20000
25000


FE6, Chip 7, ADC distribution
FE6Chip07Ped
Entries 733824
Mean -4.049
RMS 1.355
Underflow 0
Overflow 3.483e+04
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10^4
10^3
10^2
-200
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-100
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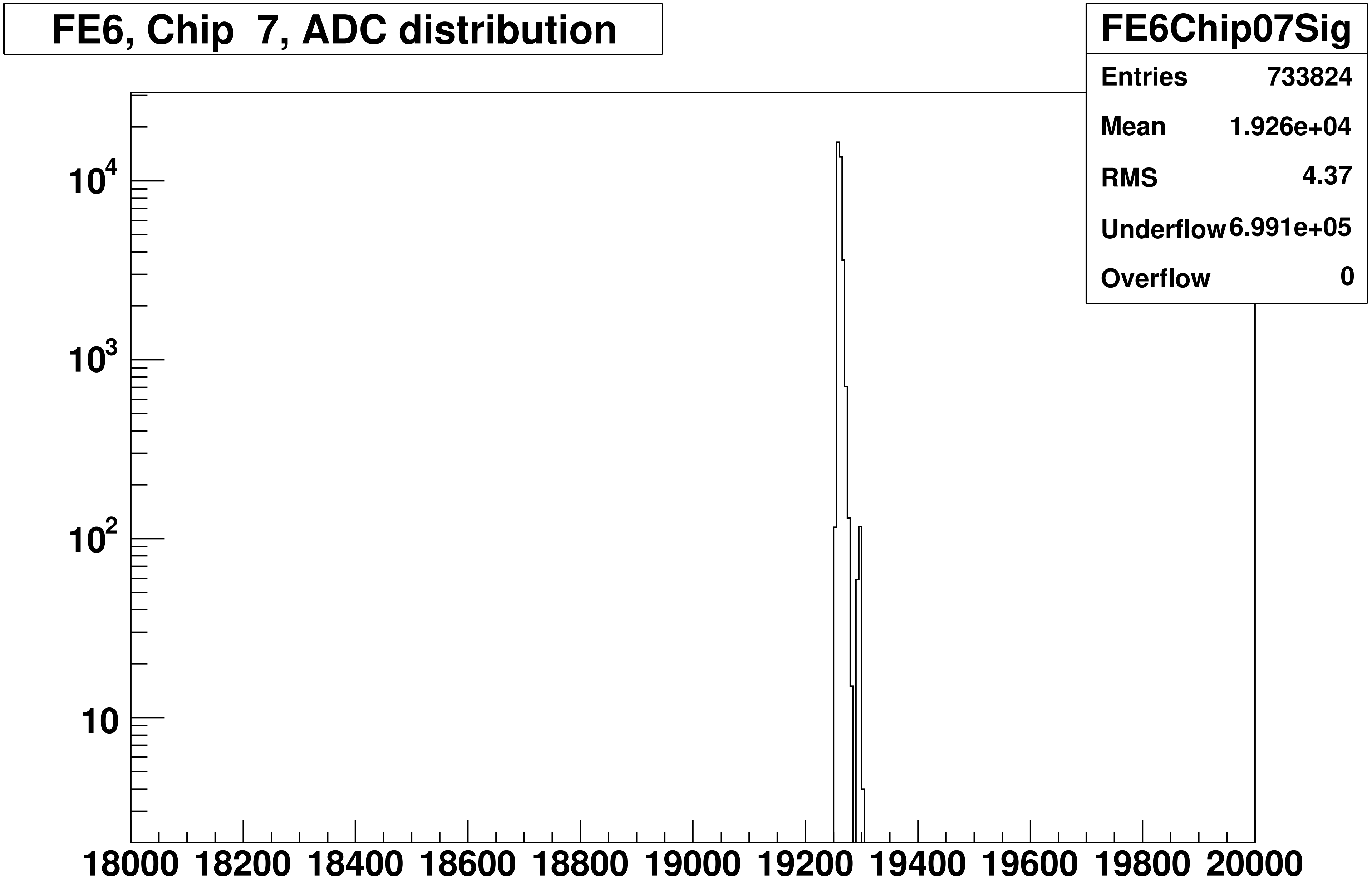
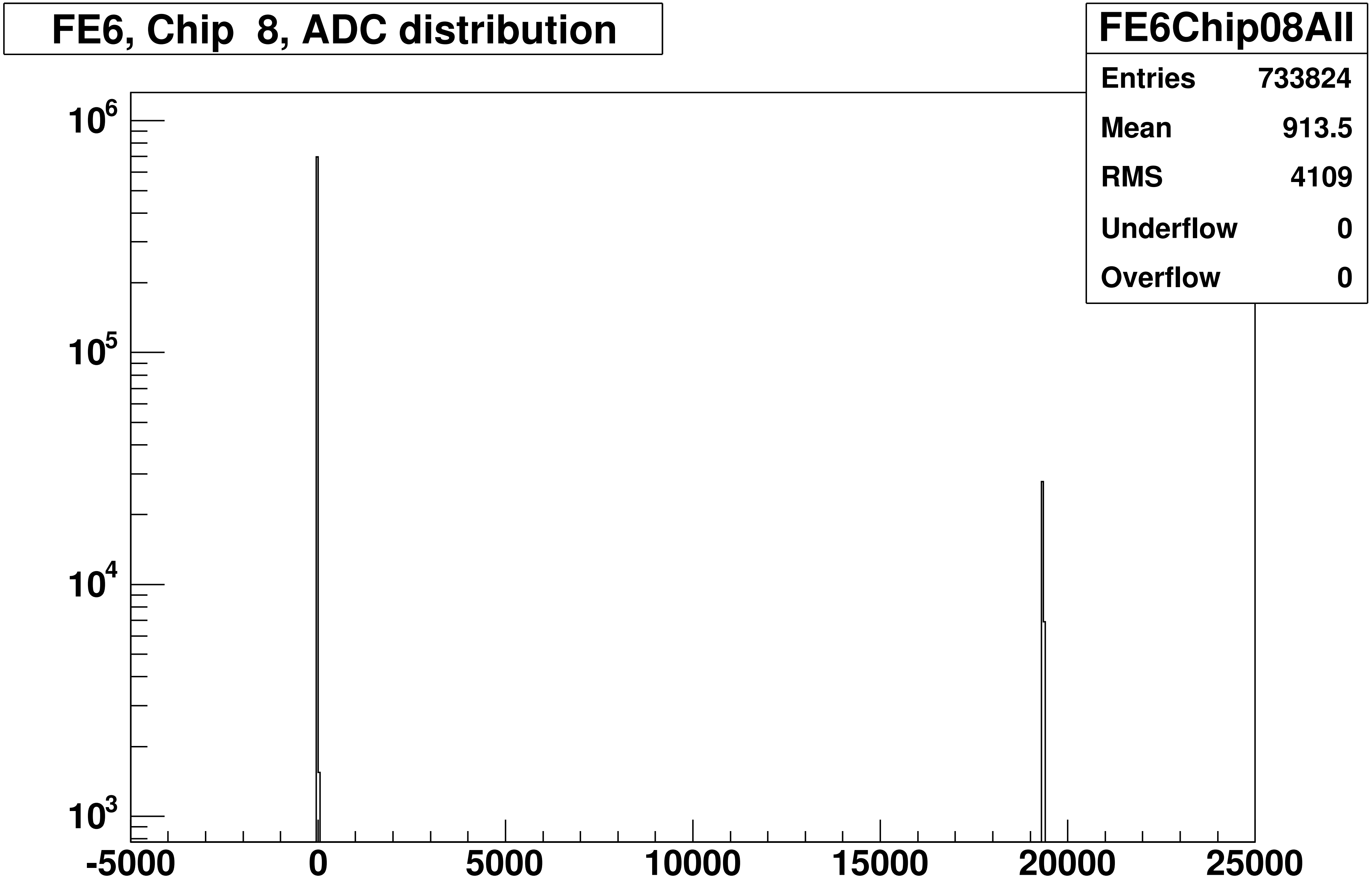
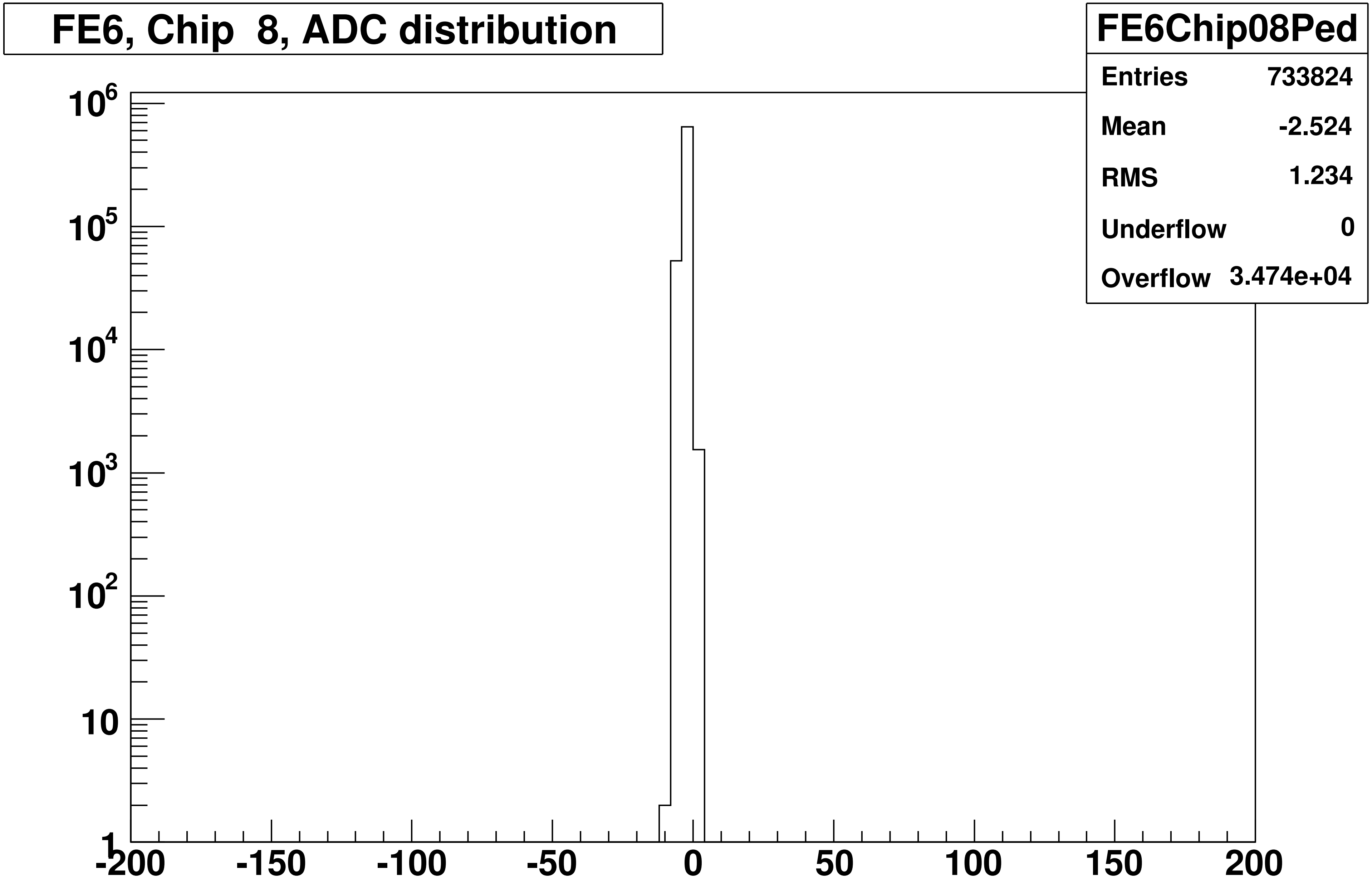
100
150
200


FE6, Chip 7, ADC distribution
FE6Chip07Sig
Entries 733824
Mean 1.926e+04
RMS 4.37
Underflow 6.991e+05
Overflow 0
10^4
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE6, Chip 8, ADC distribution
FE6Chip08All
Entries 733824
Mean 913.5
RMS 4109
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
-5000
0
5000
10000
15000
20000
25000


FE6, Chip 8, ADC distribution
FE6Chip08Ped
Entries 733824
Mean -2.524
RMS 1.234
Underflow 0
Overflow 3.474e+04
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10
10^2
10^3
10^4
10^5
10^6
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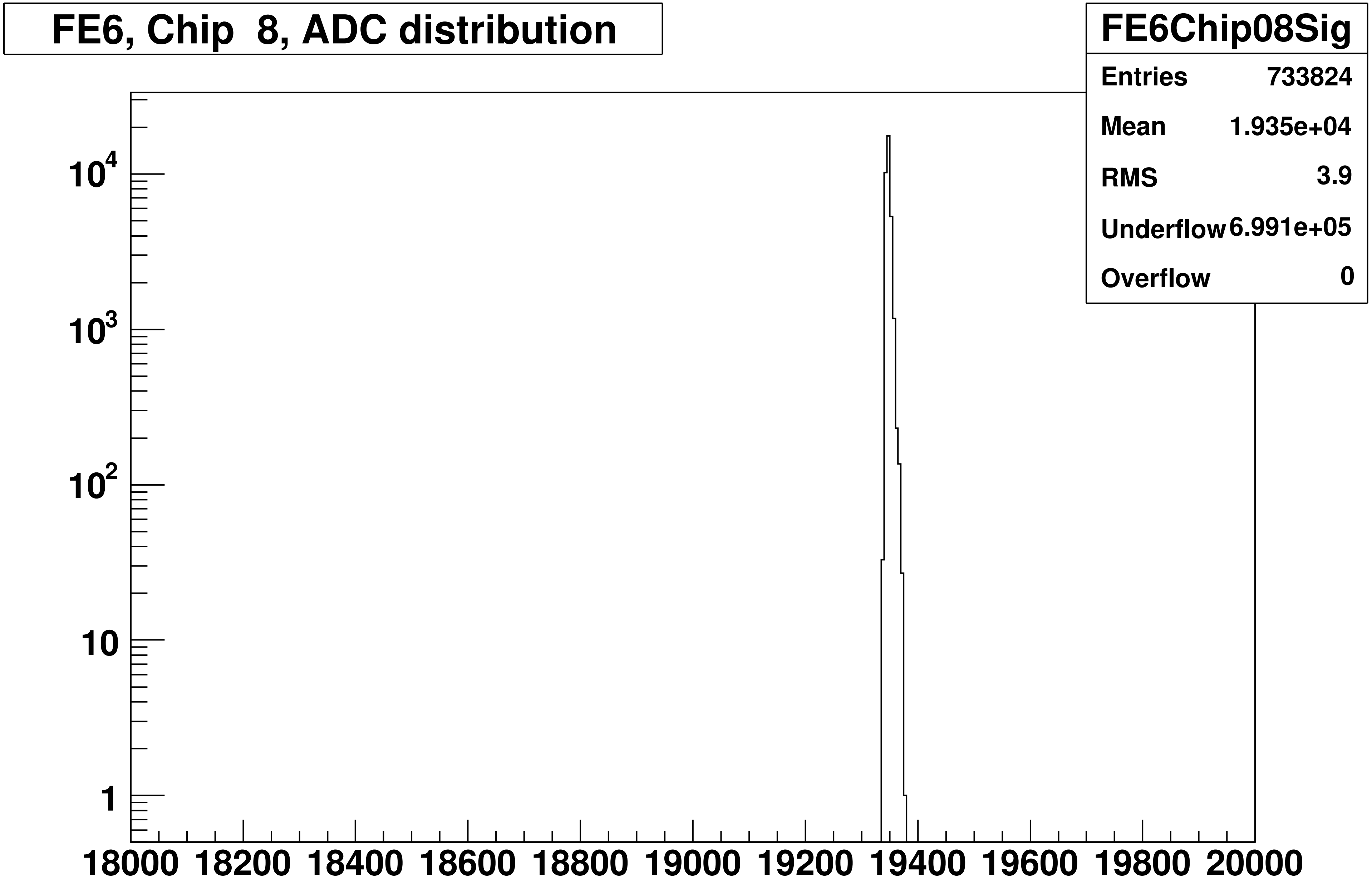
100
150
200


FE6, Chip 8, ADC distribution
FE6Chip08Sig
Entries 733824
Mean 1.935e+04
RMS 3.9
Underflow 6.991e+05
Overflow 0
10^4
10^3
10^2
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1
18000
18200
18400
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19800
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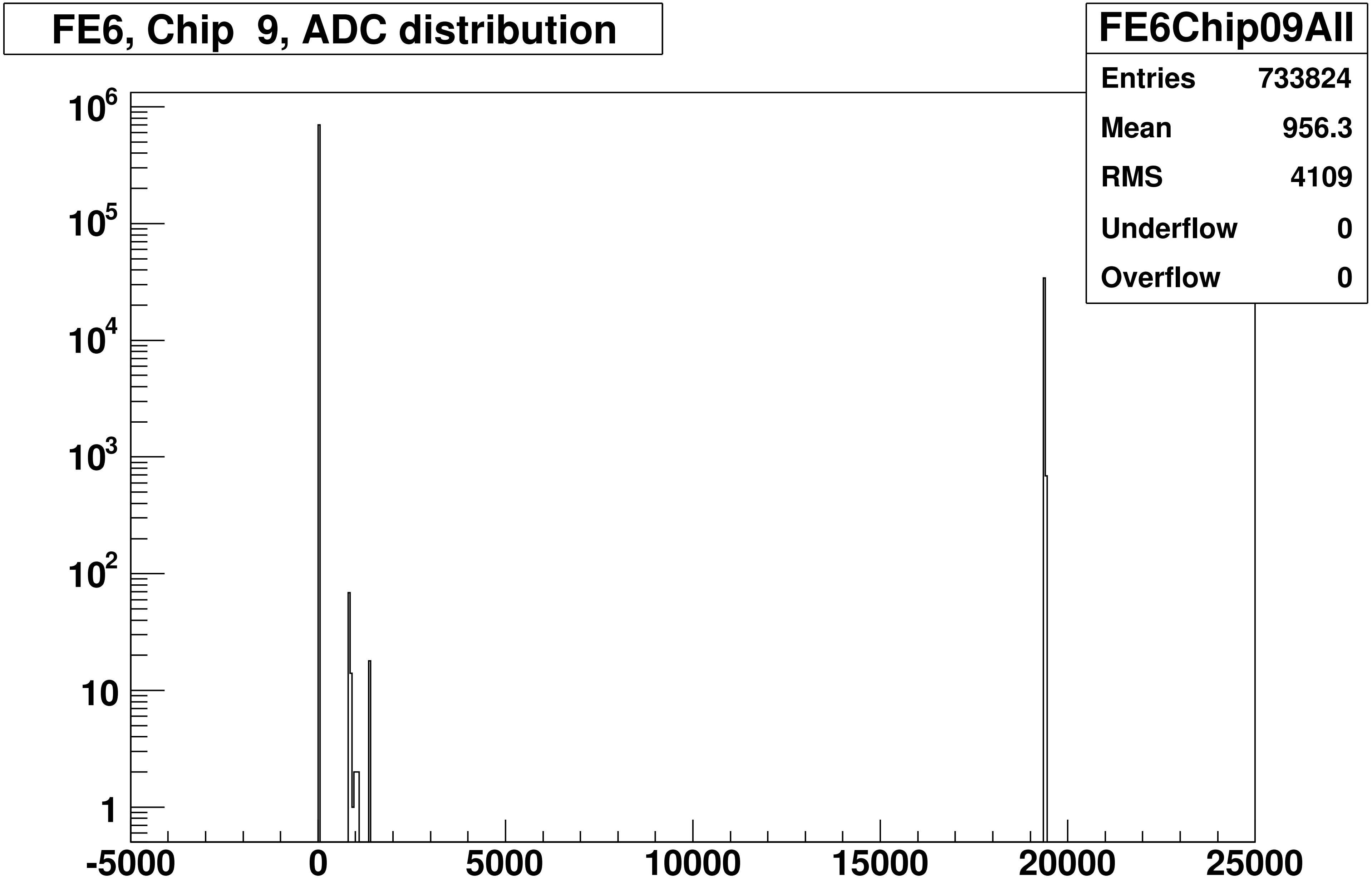

FE6, Chip 9, ADC distribution
FE6Chip09All
Entries 733824
Mean 956.3
RMS 4109
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
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10000
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20000
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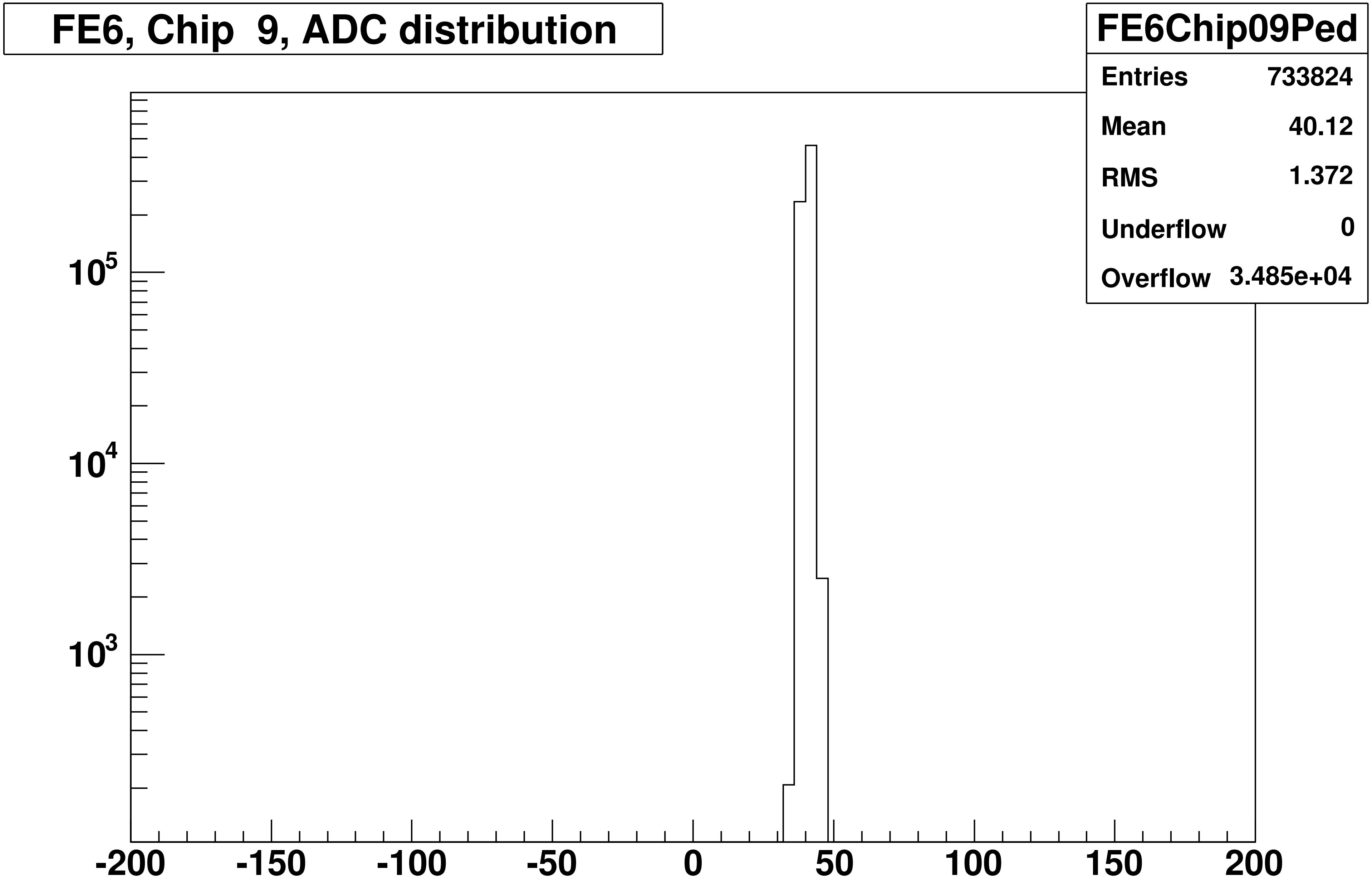
FE6, Chip 9, ADC distribution
FE6Chip09Ped
Entries 733824
Mean 40.12
RMS 1.372
Underflow 0
Overflow 3.485e+04
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10^4
10^3
-200
-150
-100
-50
0
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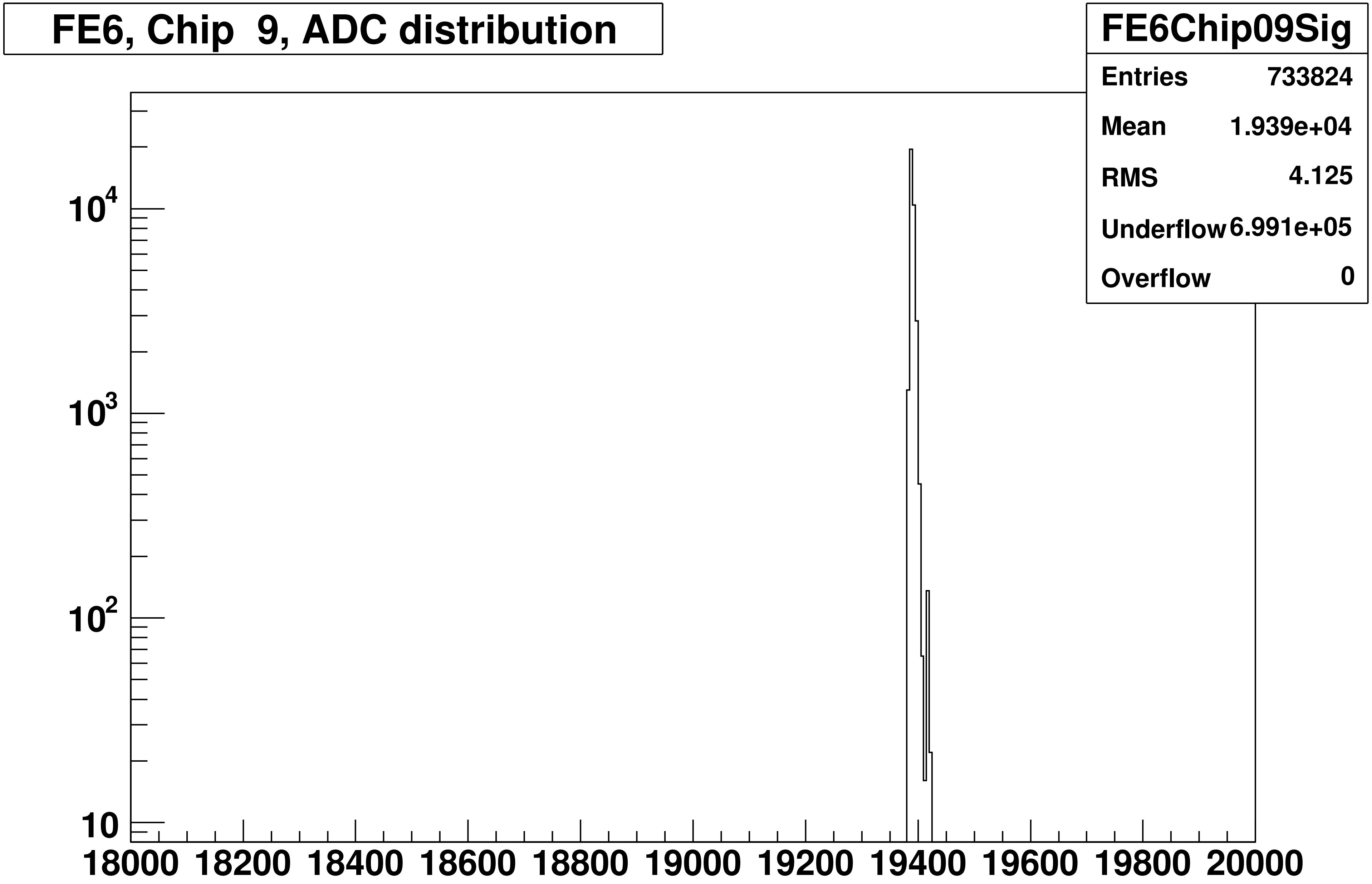
150
200


FE6, Chip 9, ADC distribution
FE6Chip09Sig
Entries 733824
Mean 1.939e+04
RMS 4.125
Underflow 6.991e+05
Overflow 0
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10^3
10^2
10
18000
18200
18400
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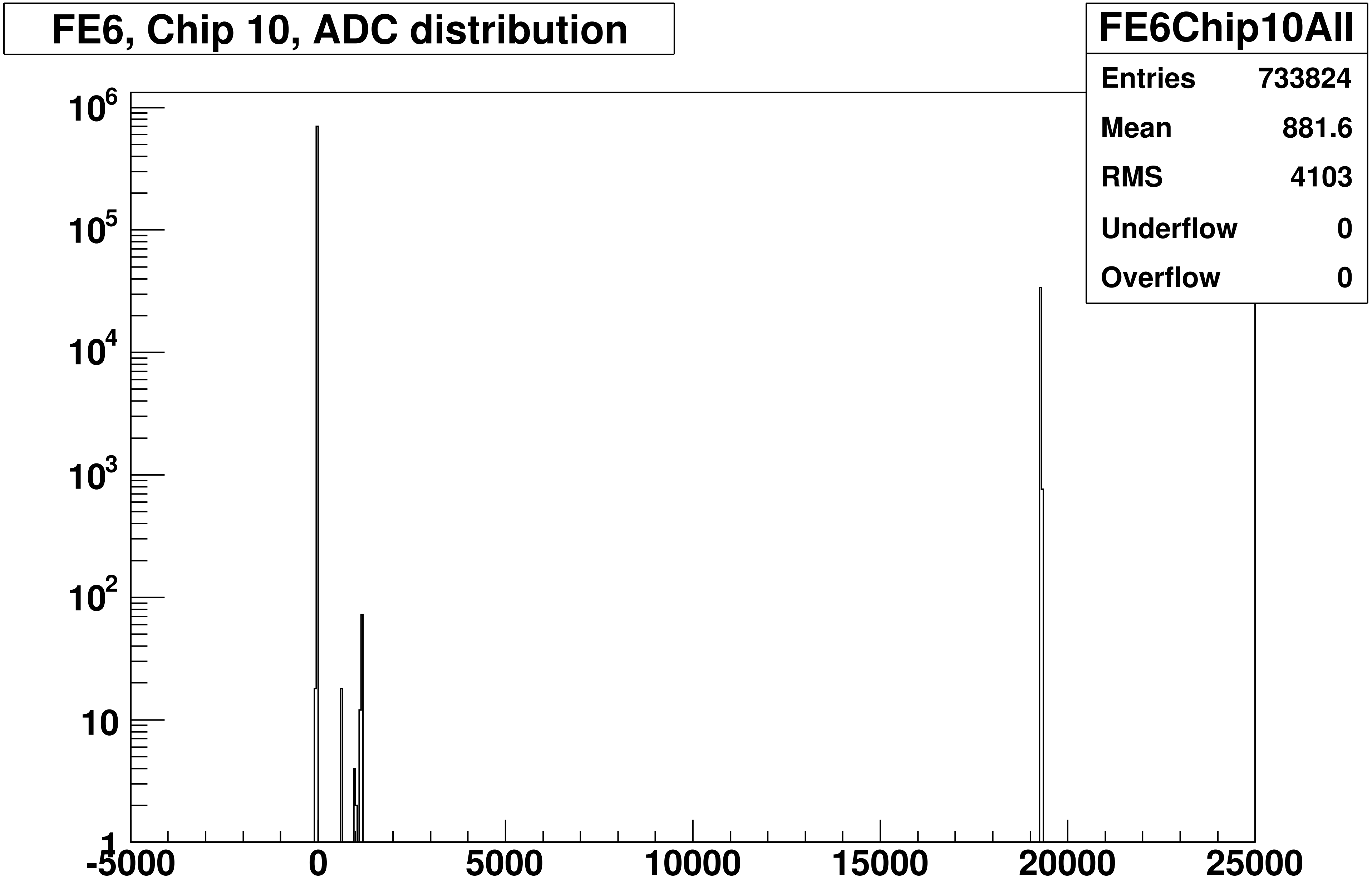
19600
19800
20000



FE6, Chip 10, ADC distribution
FE6Chip10All
Entries 733824
Mean 881.6
RMS 4103
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
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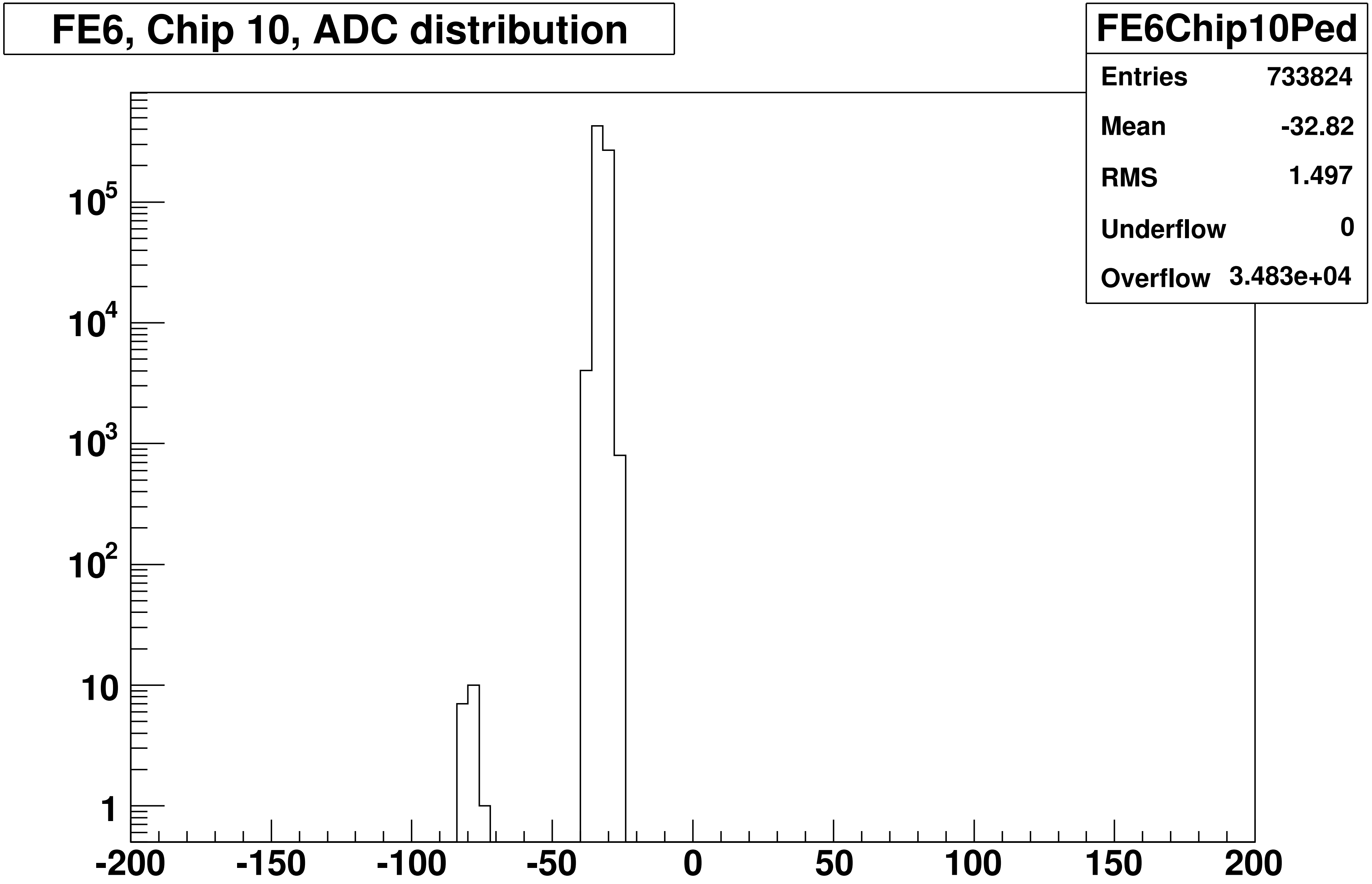
10000
15000
20000
25000


FE6, Chip 10, ADC distribution
FE6Chip10Ped
Entries 733824
Mean -32.82
RMS 1.497
Underflow 0
Overflow 3.483e+04
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10^4
10^3
10^2
10
1
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-150
-100
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0
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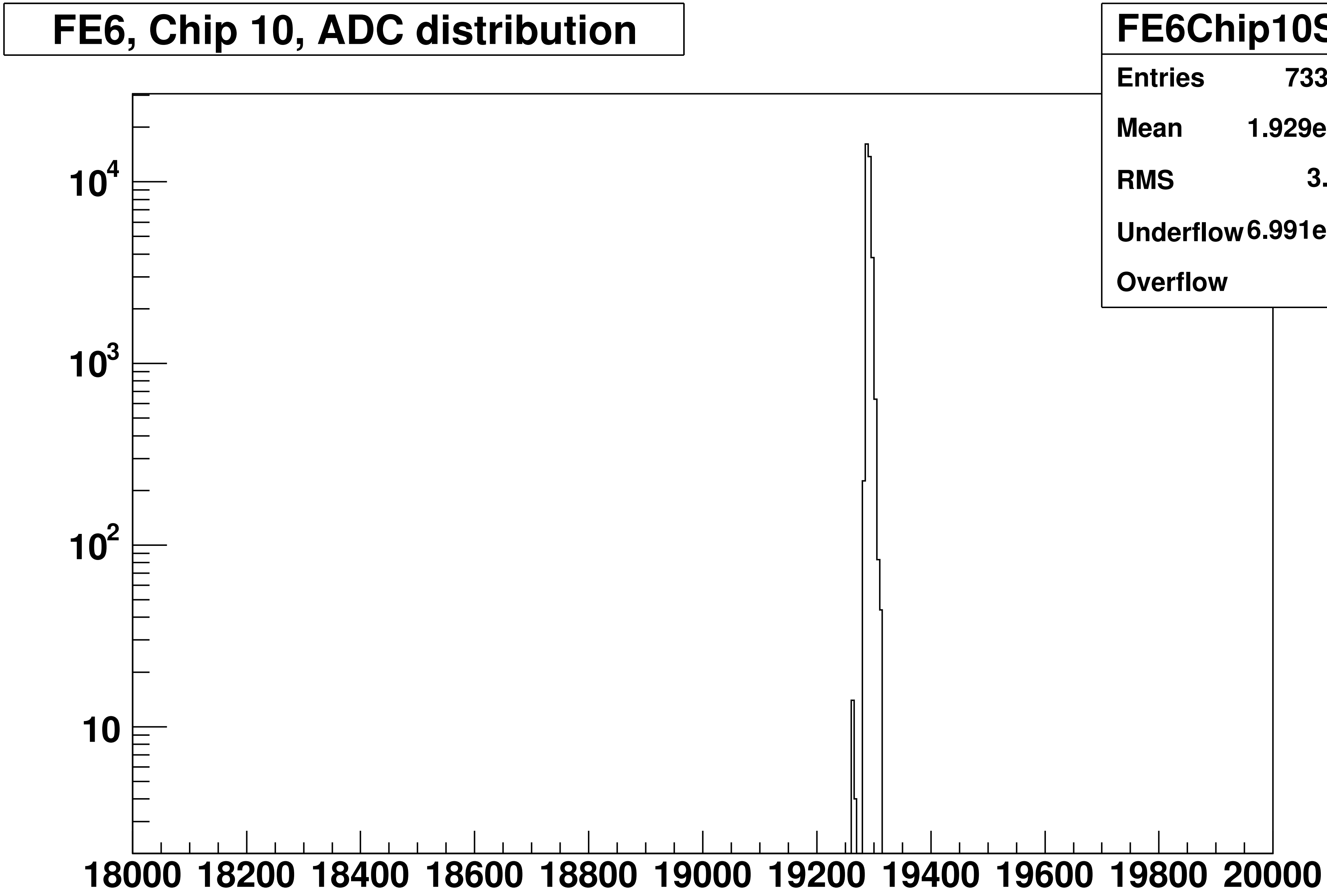
100
150
200



FE6, Chip 10, ADC distribution
FE6Chip10Sig
Entries 733824
Mean 1.929e+04
RMS 3.663
Underflow 6.991e+05
Overflow 0
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10^3
10^2
10
18000
18200
18400
18600
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19000
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19600
19800
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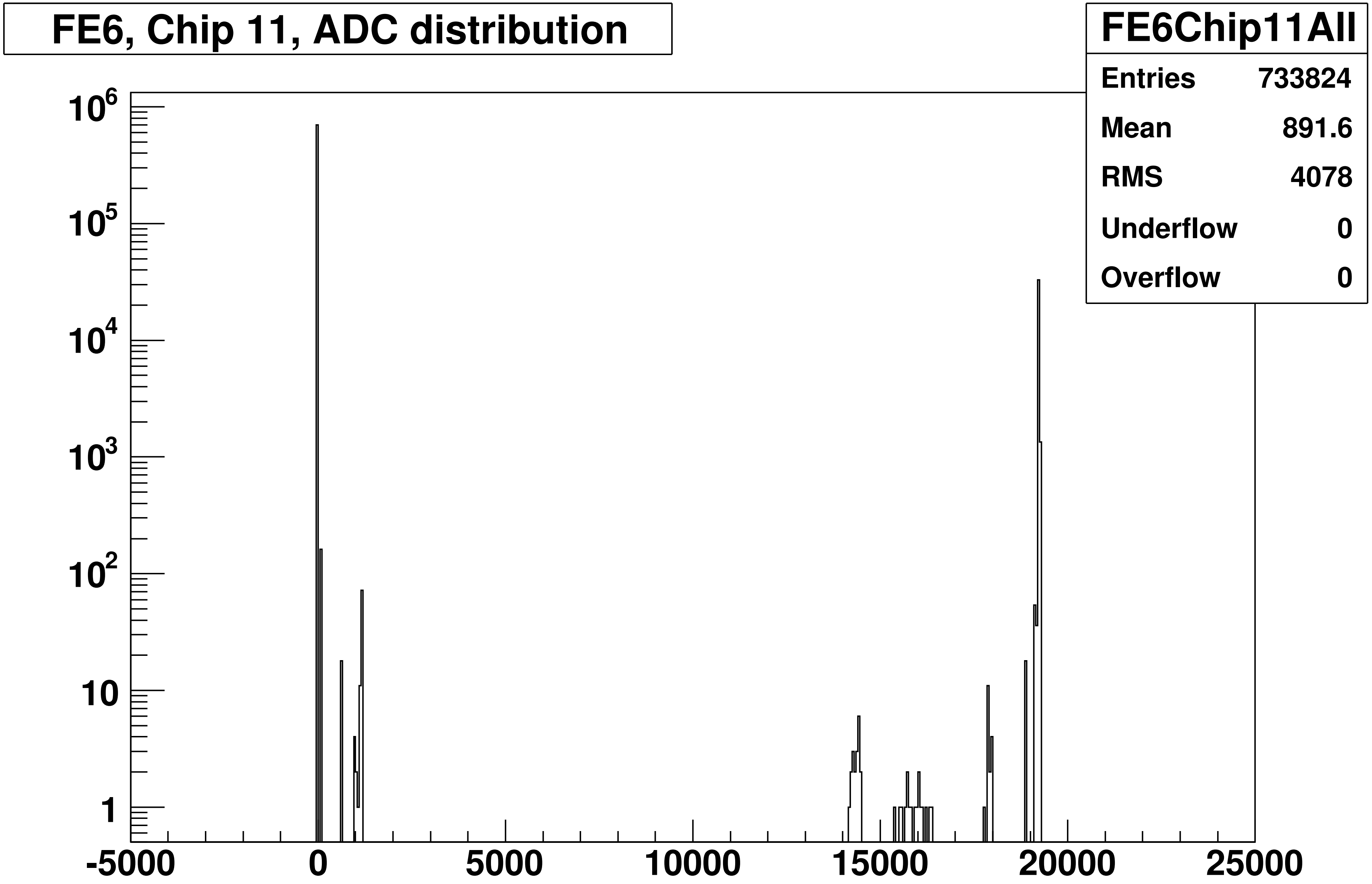
FE6, Chip 11, ADC distribution
FE6Chip11All
Entries 733824
Mean 891.6
RMS 4078
Underflow 0
Overflow 0
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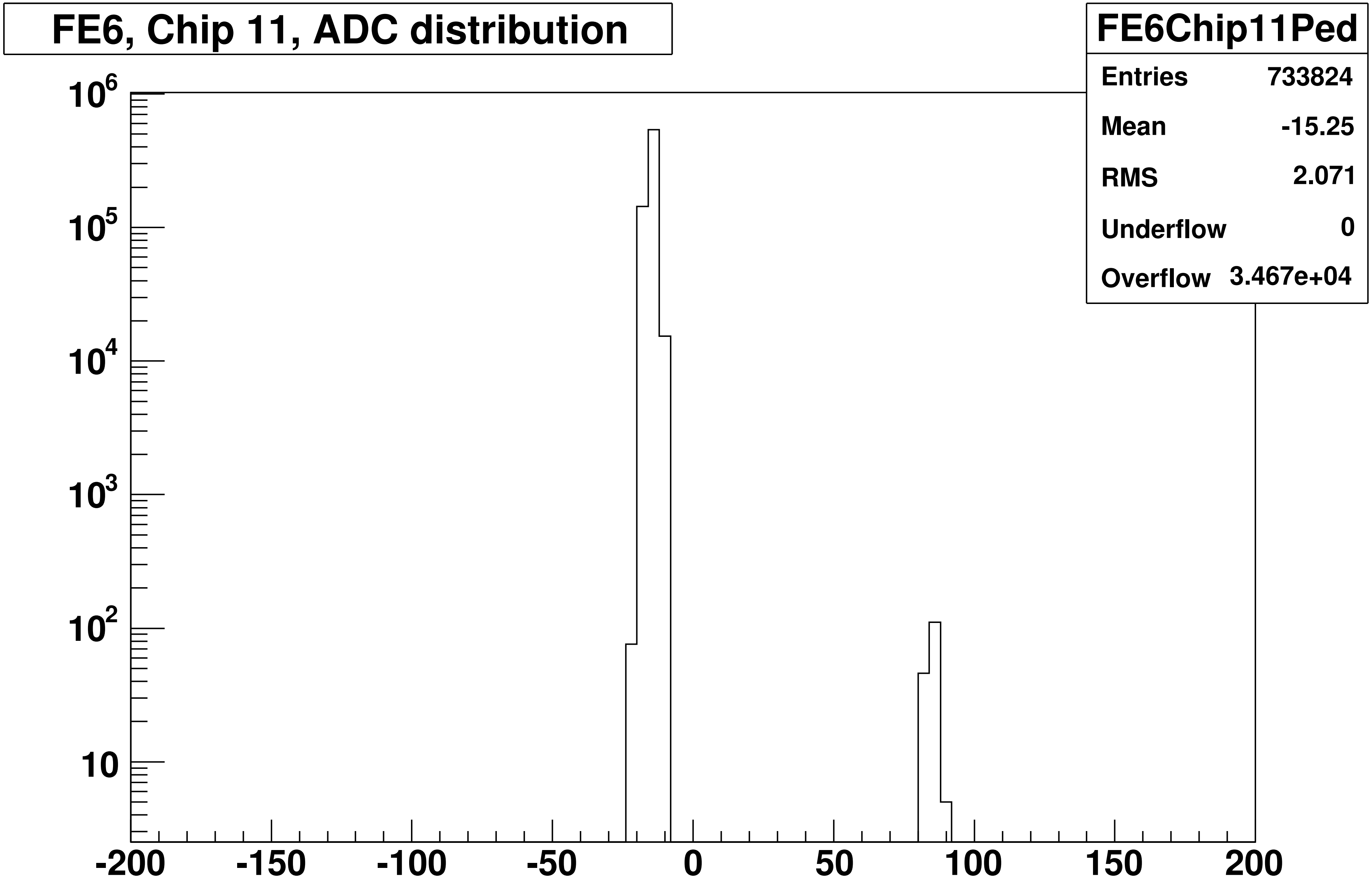
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE6, Chip 11, ADC distribution
FE6Chip11Ped
Entries 733824
Mean -15.25
RMS 2.071
Underflow 0
Overflow 3.467e+04
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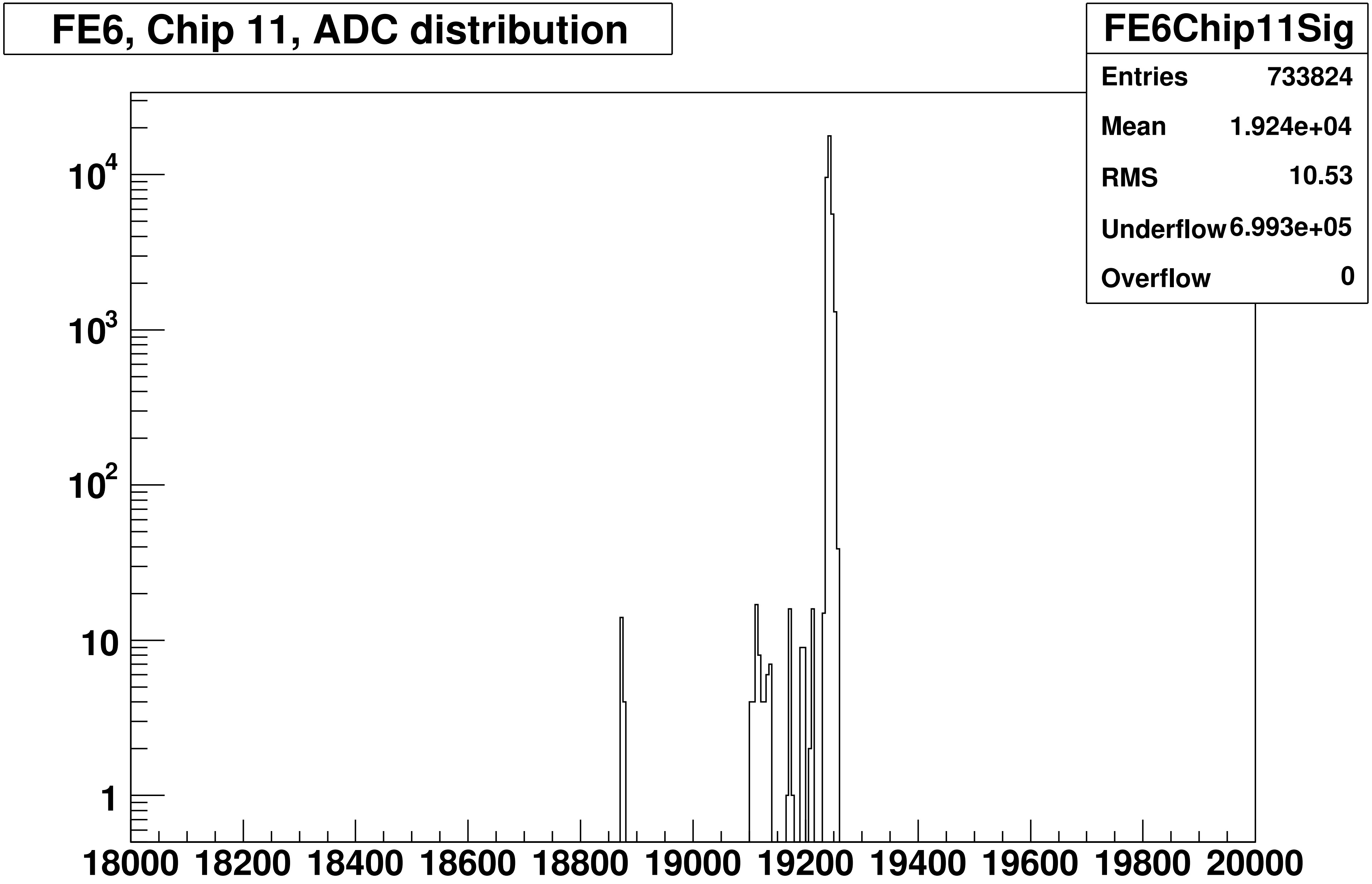
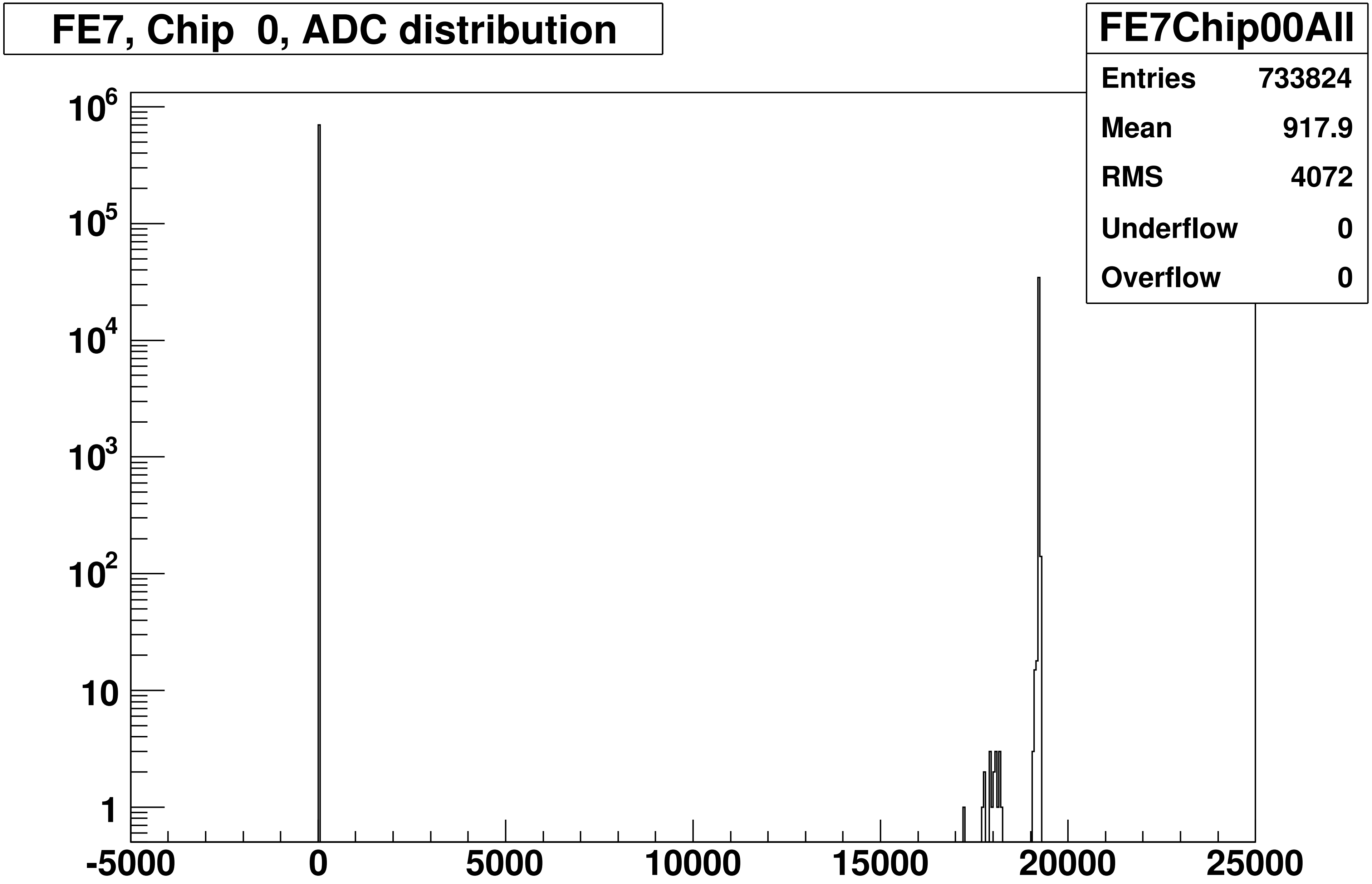
10^5
10^4
10^3
10^2
10
-200
-150
-100
-50
0
50
100
150
200



FE6, Chip 11, ADC distribution
FE6Chip11Sig
Entries 733824
Mean 1.924e+04
RMS 10.53
Underflow 6.993e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000



FE7, Chip 0, ADC distribution
FE7Chip00All
Entries 733824
Mean 917.9
RMS 4072
Underflow 0
Overflow 0
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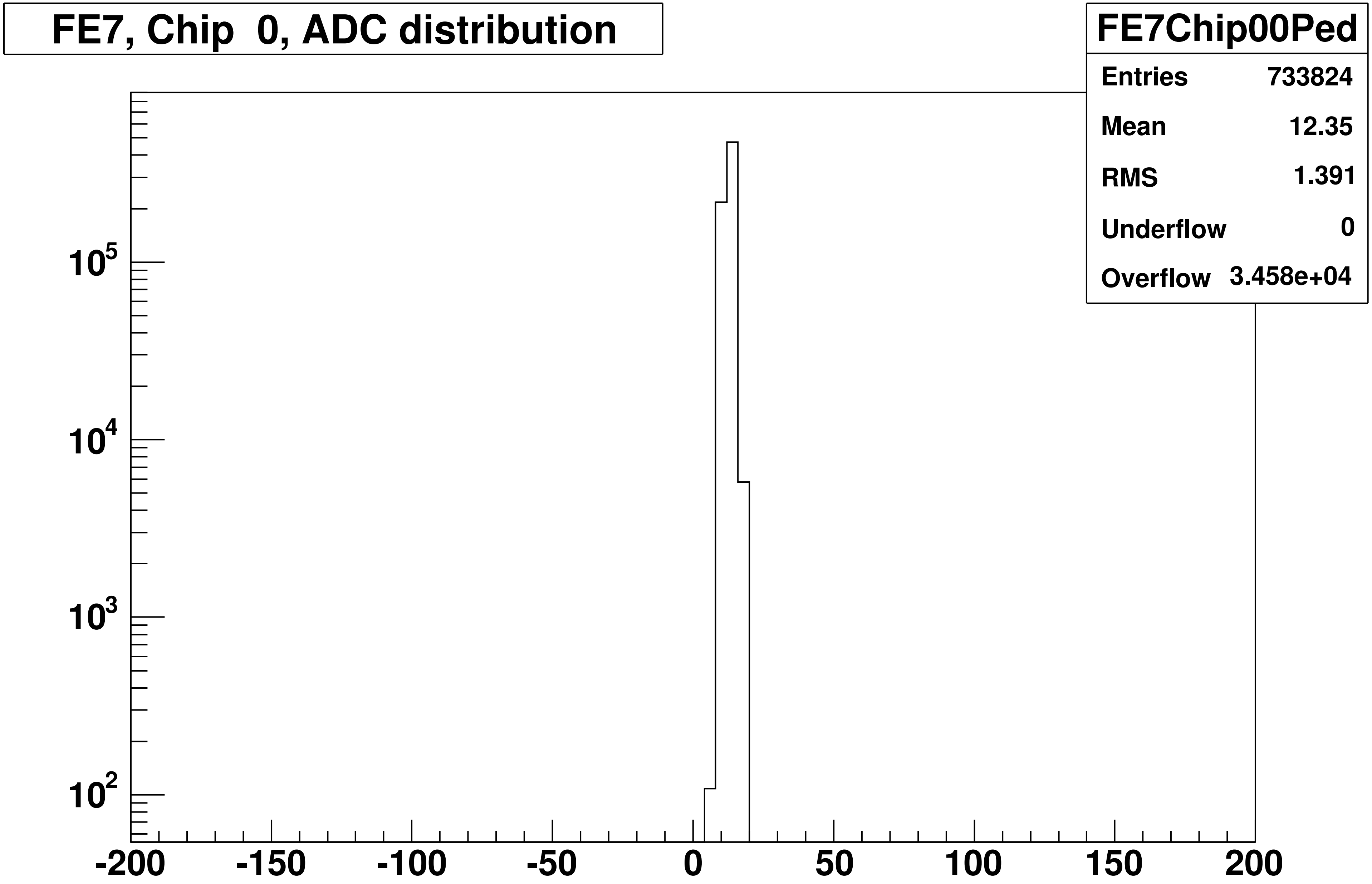
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE7, Chip 0, ADC distribution
FE7Chip00Ped
Entries 733824
Mean 12.35
RMS 1.391
Underflow 0
Overflow 3.458e+04
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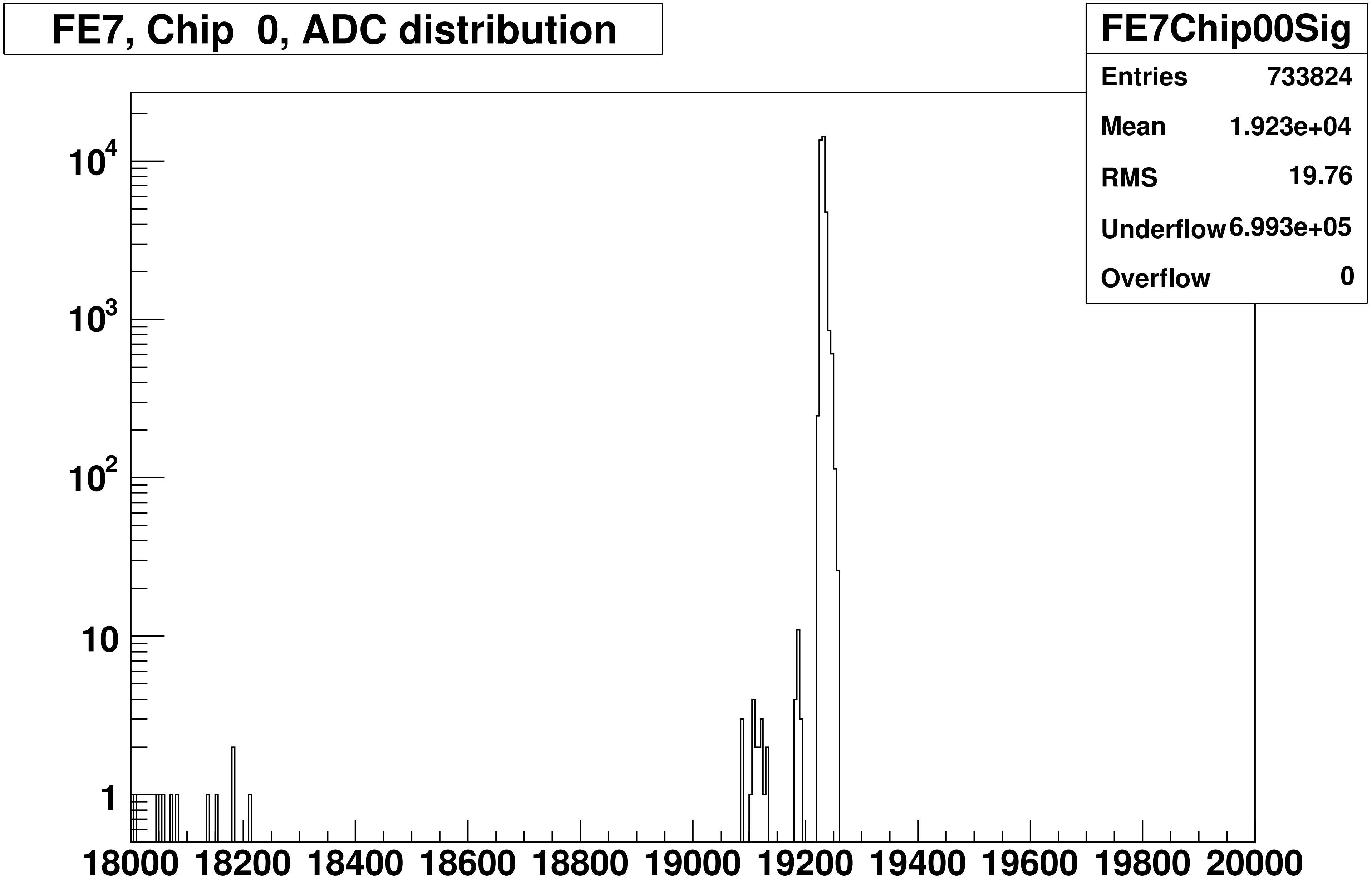
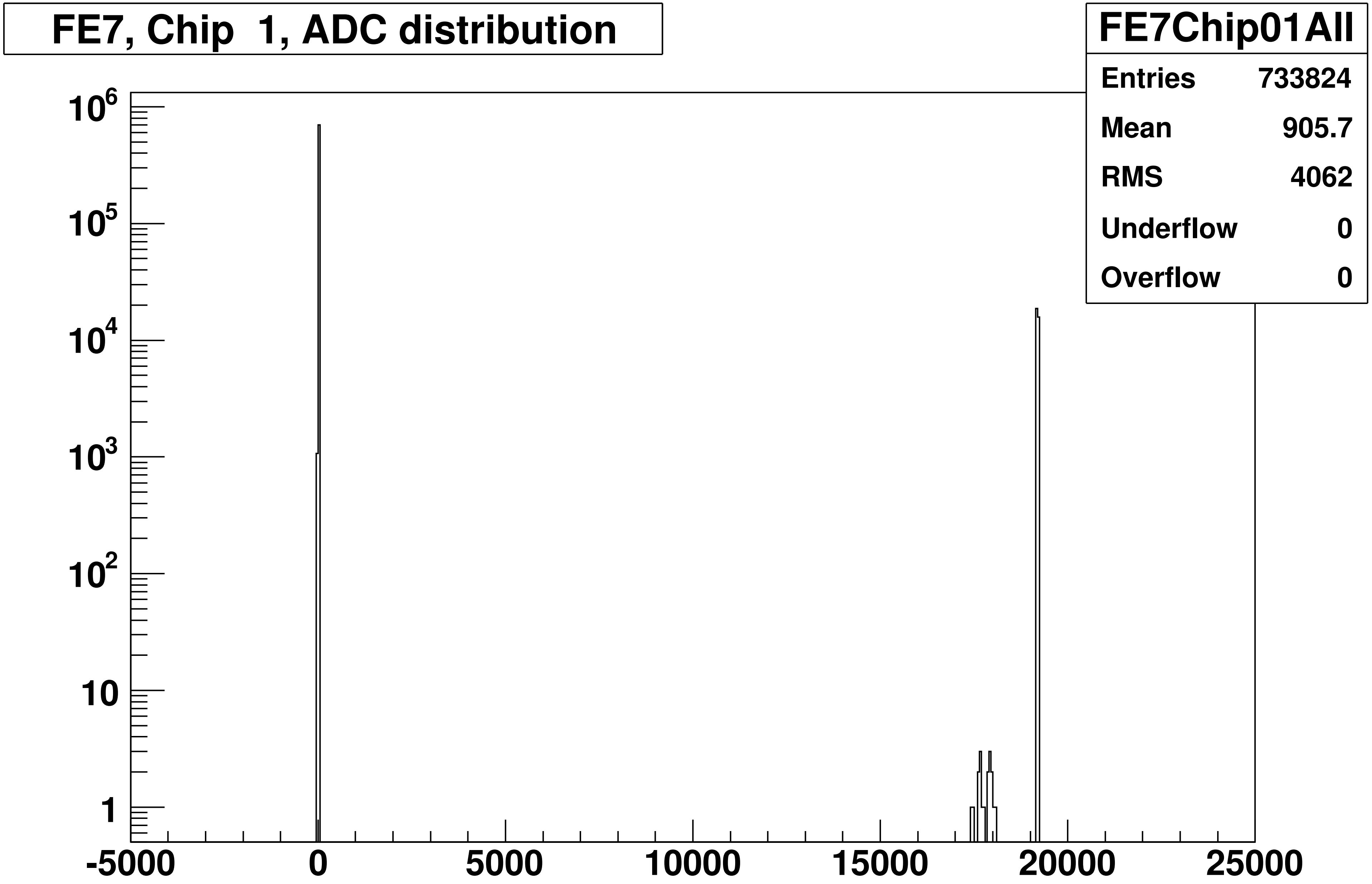
10^4
10^3
10^2
-200
-150
-100
-50
0
50
100
150
200


FE7, Chip 0, ADC distribution
FE7Chip00Sig
Entries 733824
Mean 1.923e+04
RMS 19.76
Underflow 6.993e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE7, Chip 1, ADC distribution
FE7Chip01All
Entries 733824
Mean 905.7
RMS 4062
Underflow 0
Overflow 0
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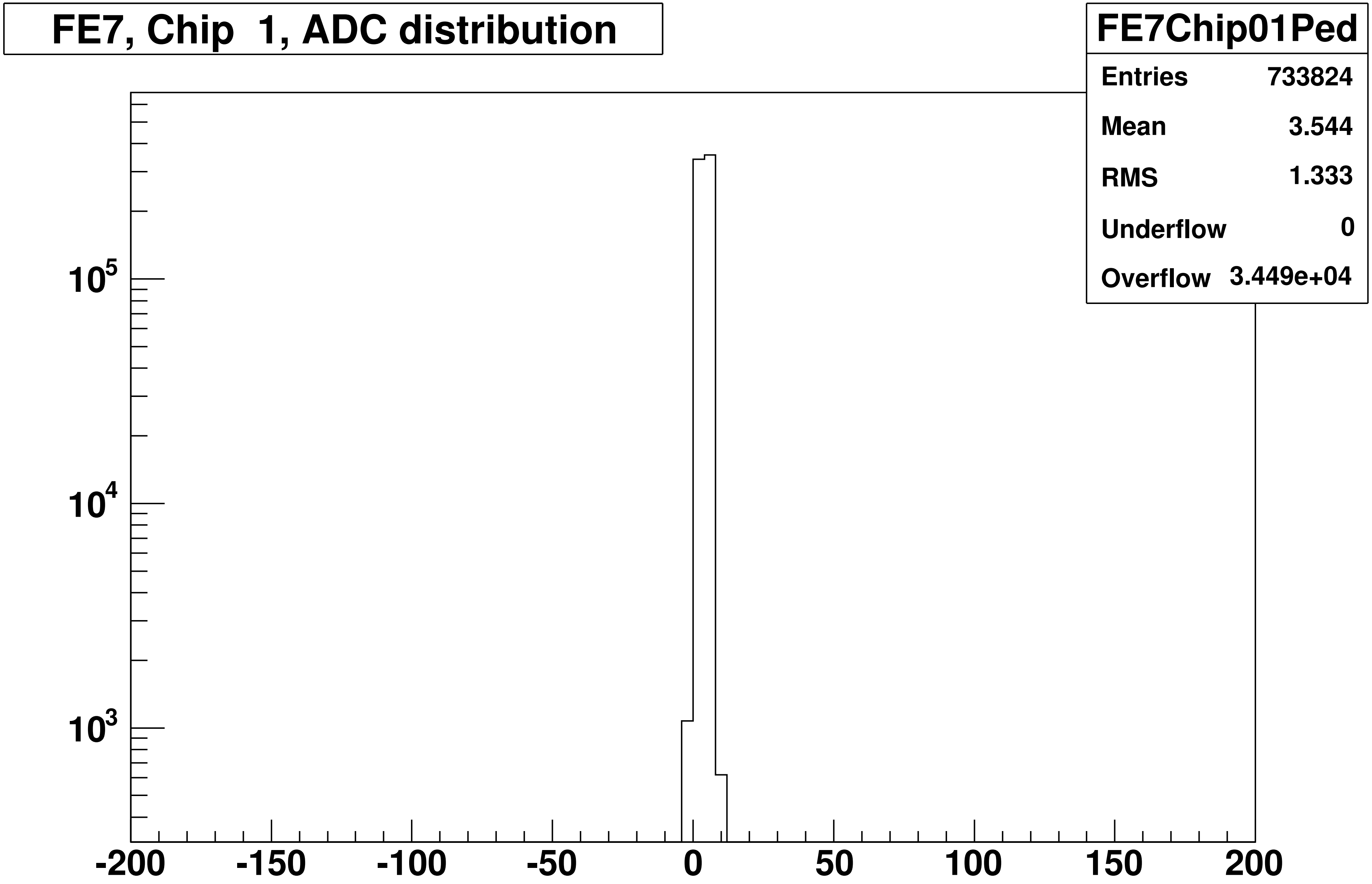
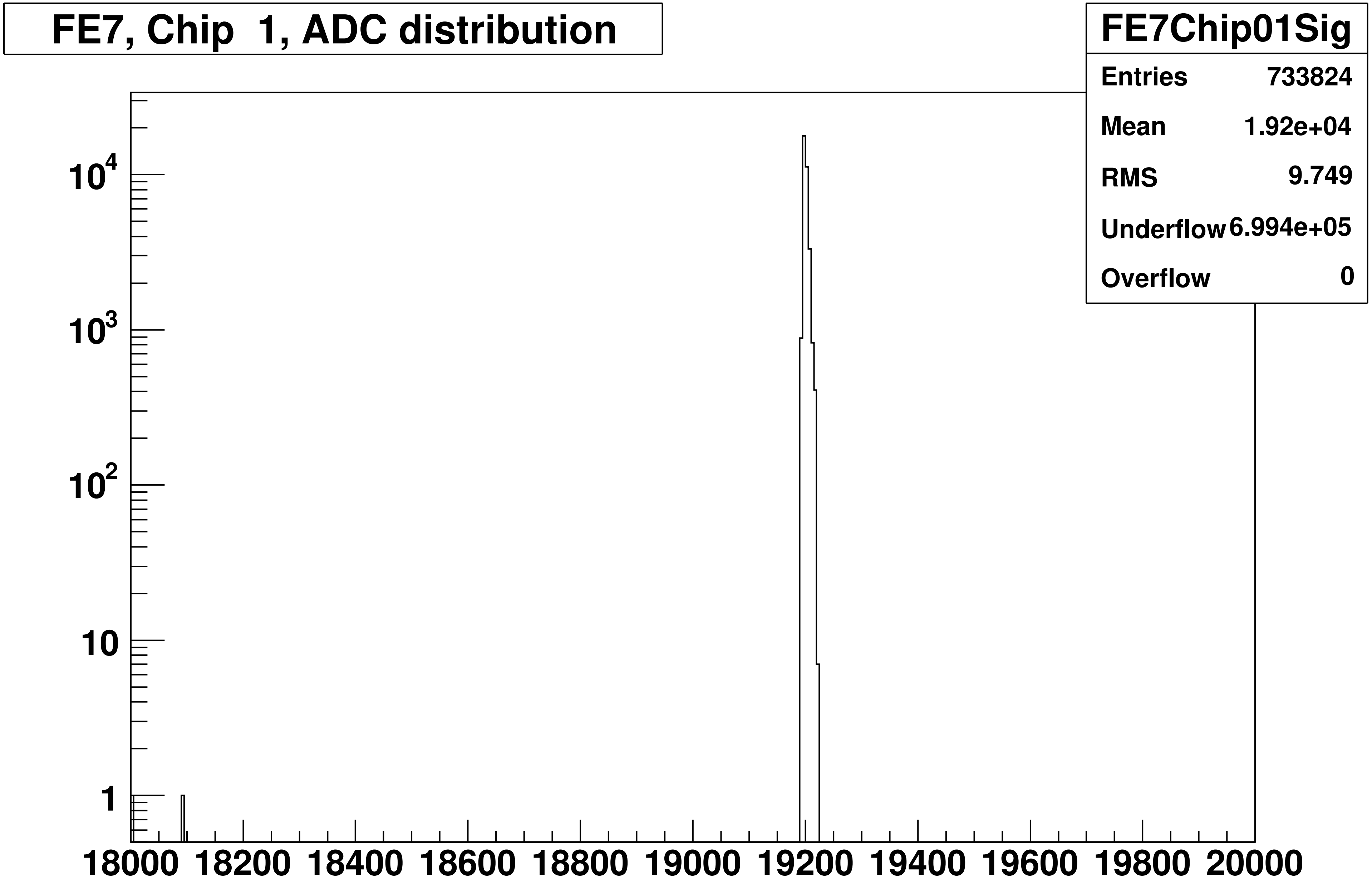
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE7, Chip 1, ADC distribution
FE7Chip01Ped
Entries 733824
Mean 3.544
RMS 1.333
Underflow 0
Overflow 3.449e+04
10^5
10^4
10^3
-200
-150
-100
-50
0
50
100
150
200


FE7, Chip 1, ADC distribution
FE7Chip01Sig
Entries 733824
Mean 1.92e+04
RMS 9.749
Underflow 6.994e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
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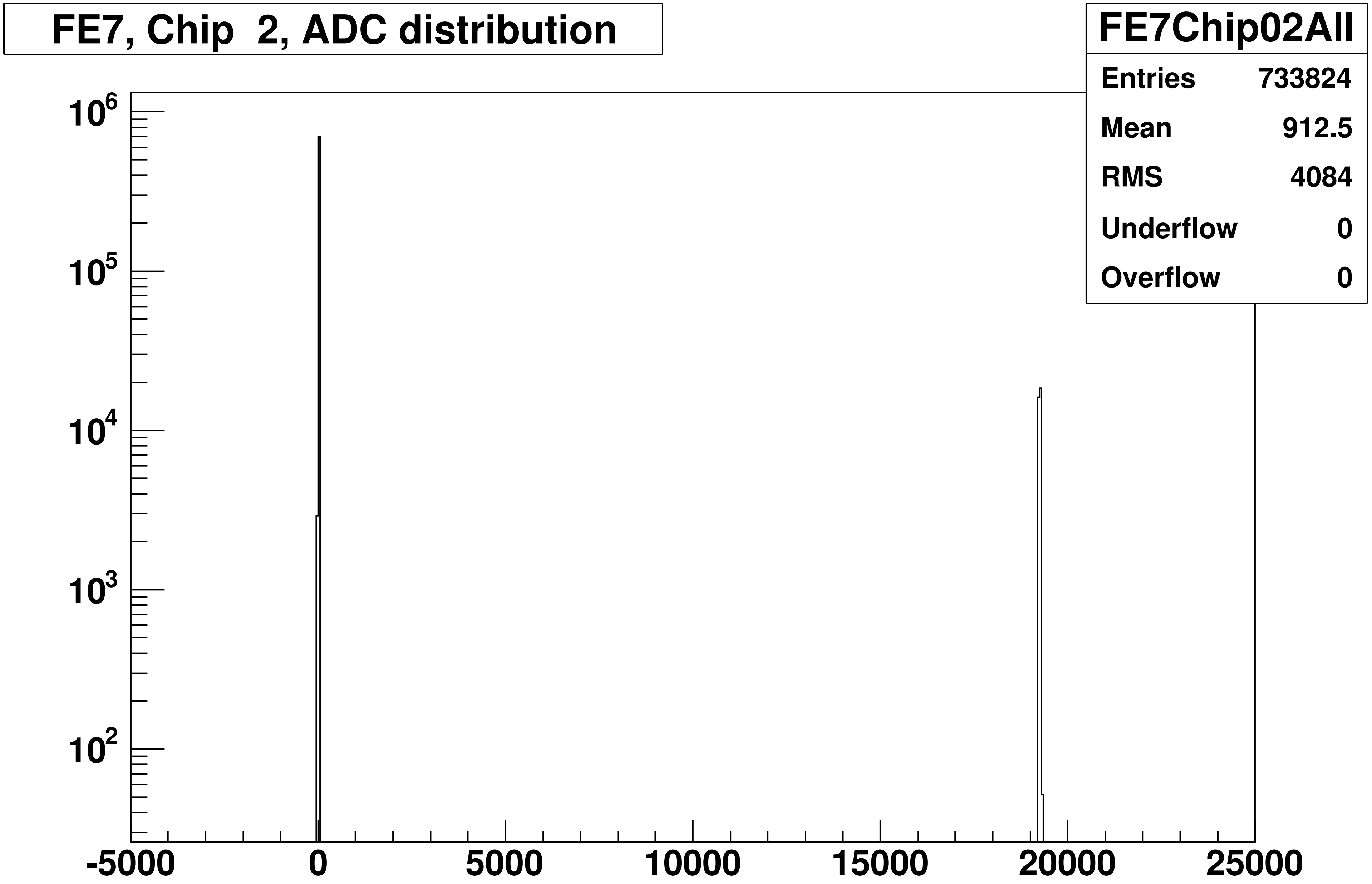
18800
19000
19200
19400
19600
19800
20000


FE7, Chip 2, ADC distribution
FE7Chip02All
Entries 733824
Mean 912.5
RMS 4084
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
-5000
0
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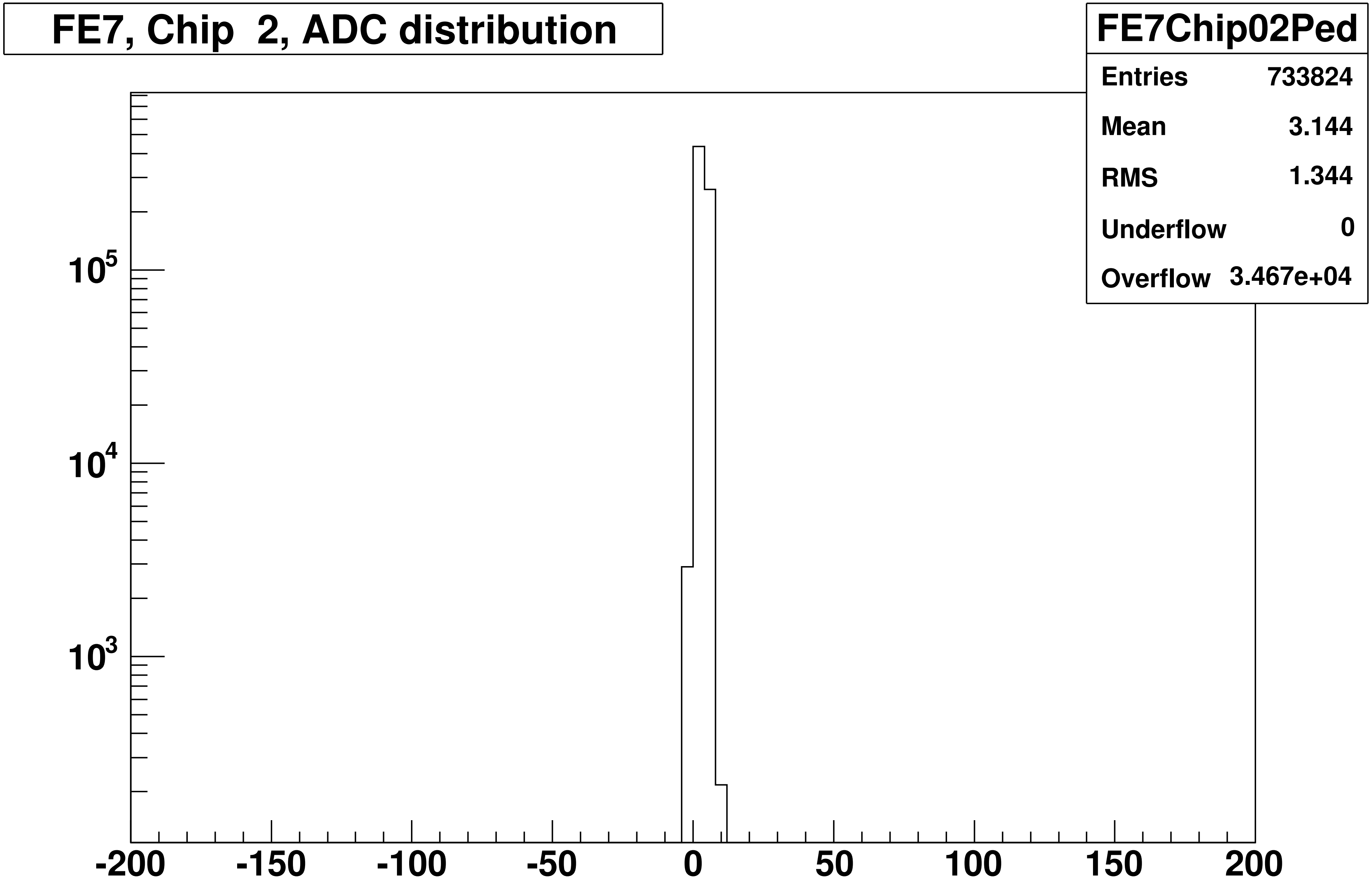
10000
15000
20000
25000


FE7, Chip 2, ADC distribution
FE7Chip02Ped
Entries 733824
Mean 3.144
RMS 1.344
Underflow 0
Overflow 3.467e+04
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10^4
10^3
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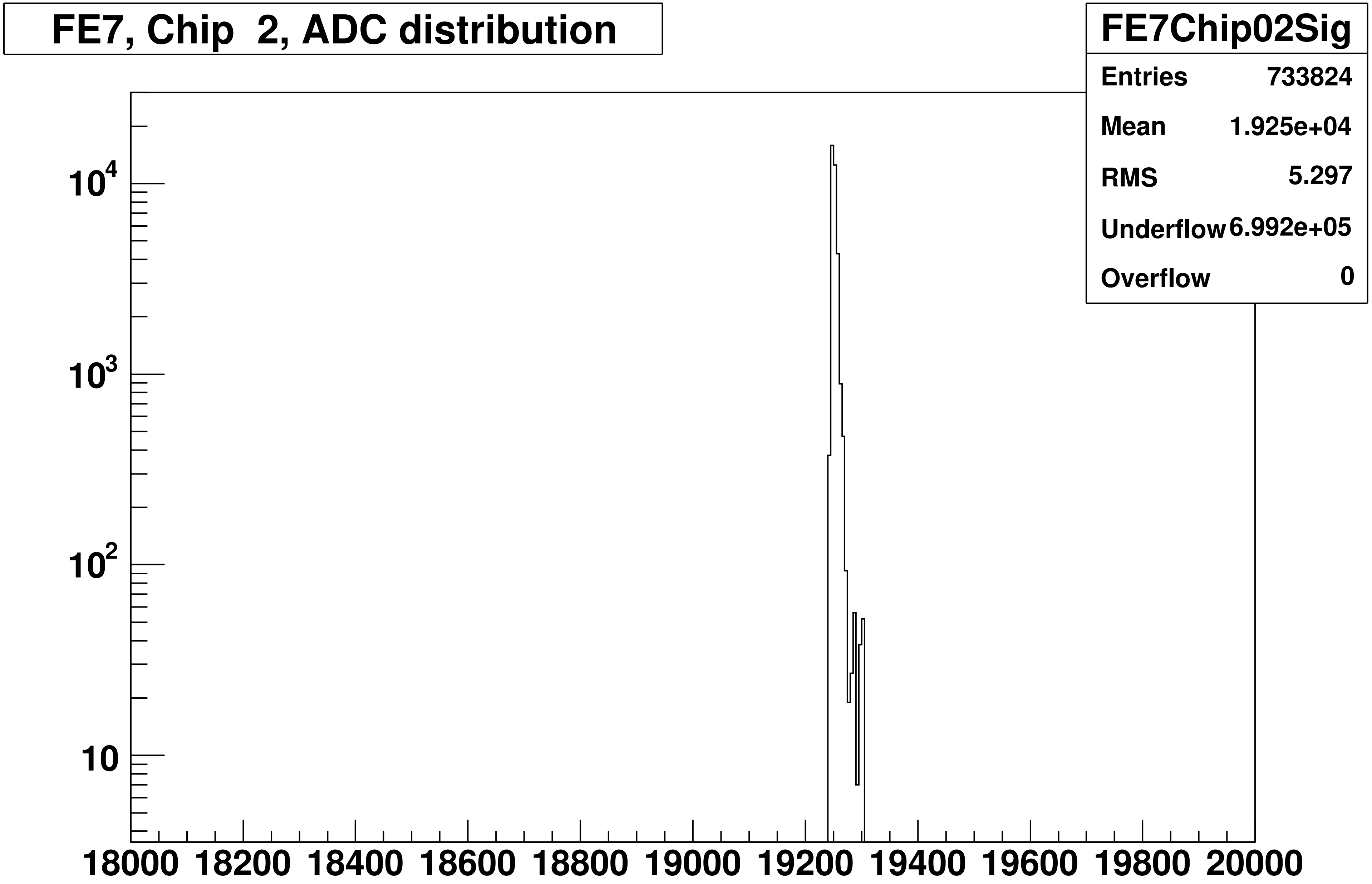
-150
-100
-50
0
50
100
150
200



FE7, Chip 2, ADC distribution
FE7Chip02Sig
Entries 733824
Mean 1.925e+04
RMS 5.297
Underflow 6.992e+05
Overflow 0
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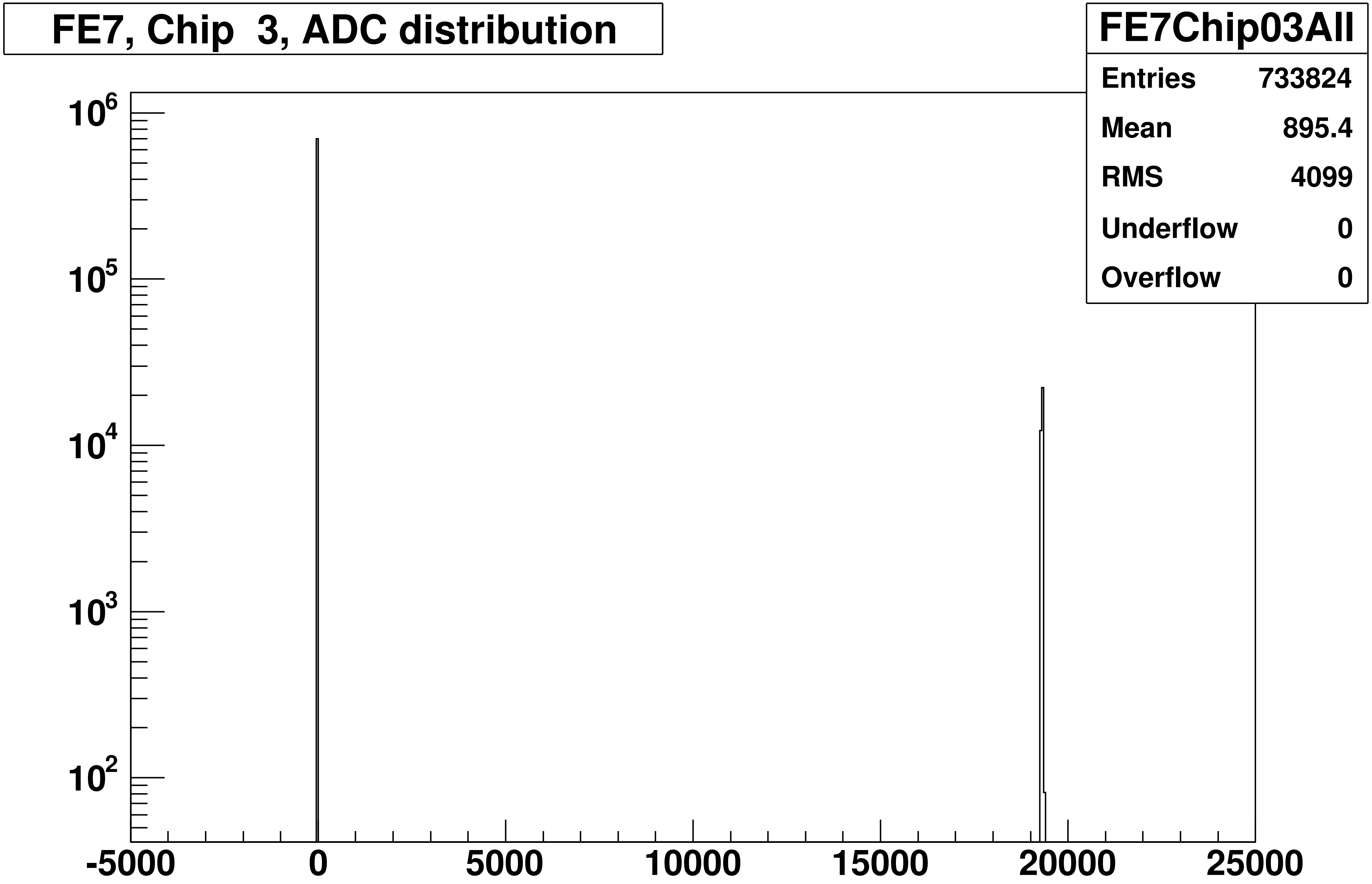
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE7, Chip 3, ADC distribution
FE7Chip03All
Entries 733824
Mean 895.4
RMS 4099
Underflow 0
Overflow 0
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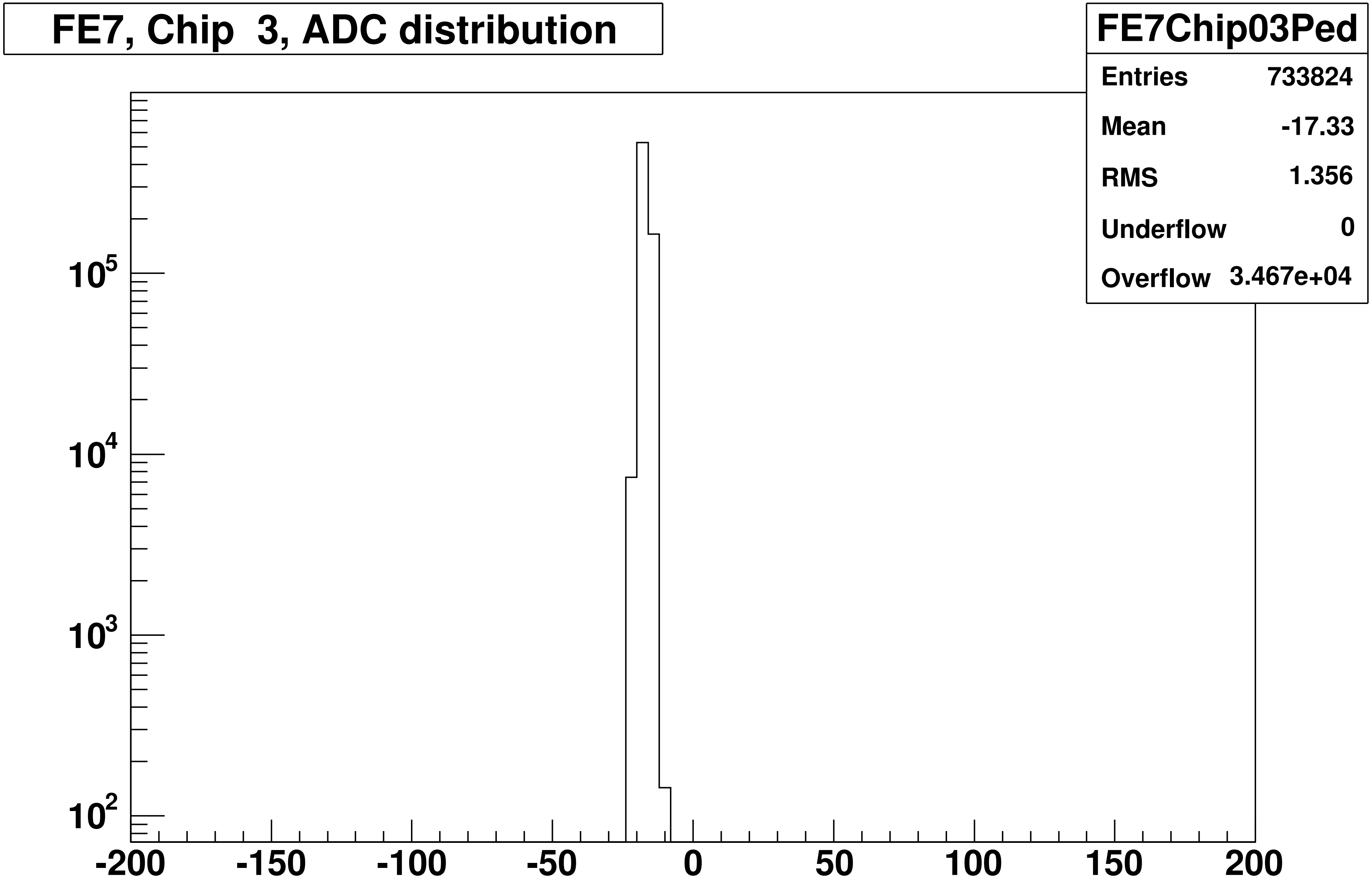
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000


FE7, Chip 3, ADC distribution
FE7Chip03Ped
Entries 733824
Mean -17.33
RMS 1.356
Underflow 0
Overflow 3.467e+04
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10^4
10^3
10^2
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-100
-50
0
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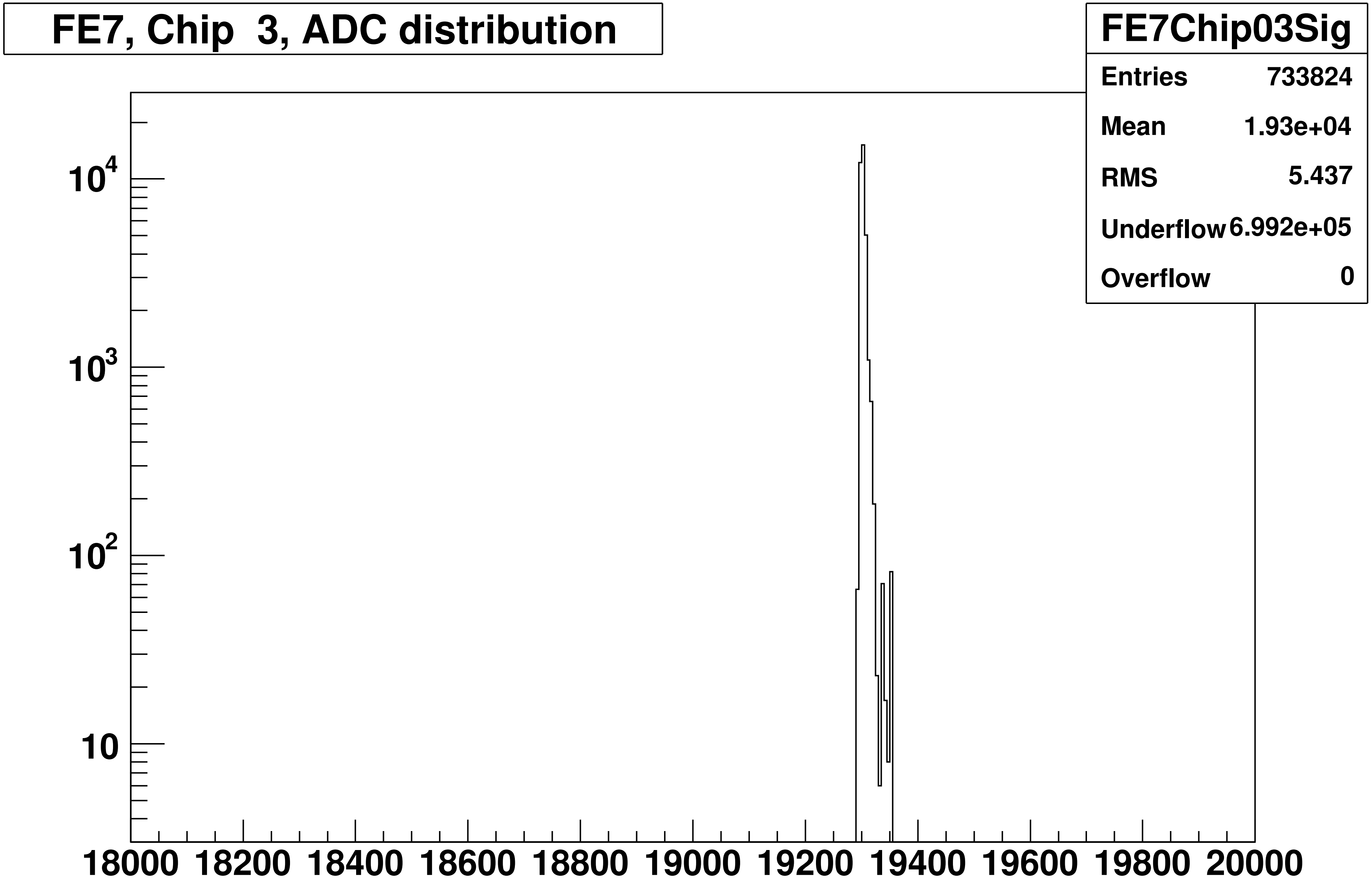
100
150
200



FE7, Chip 3, ADC distribution
FE7Chip03Sig
Entries 733824
Mean 1.93e+04
RMS 5.437
Underflow 6.992e+05
Overflow 0
10^4
10^3
10^2
10
18000
18200
18400
18600
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19000
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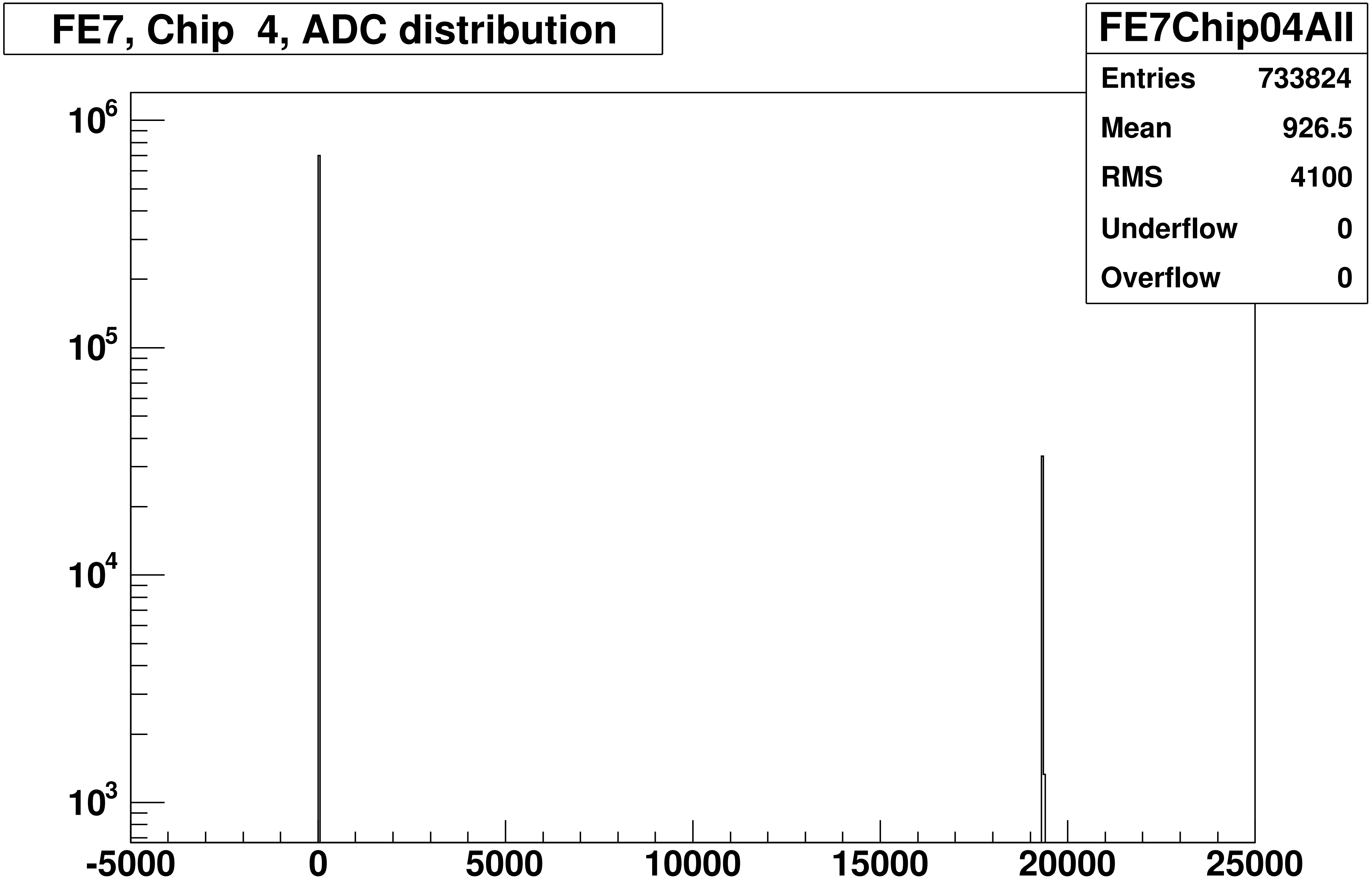
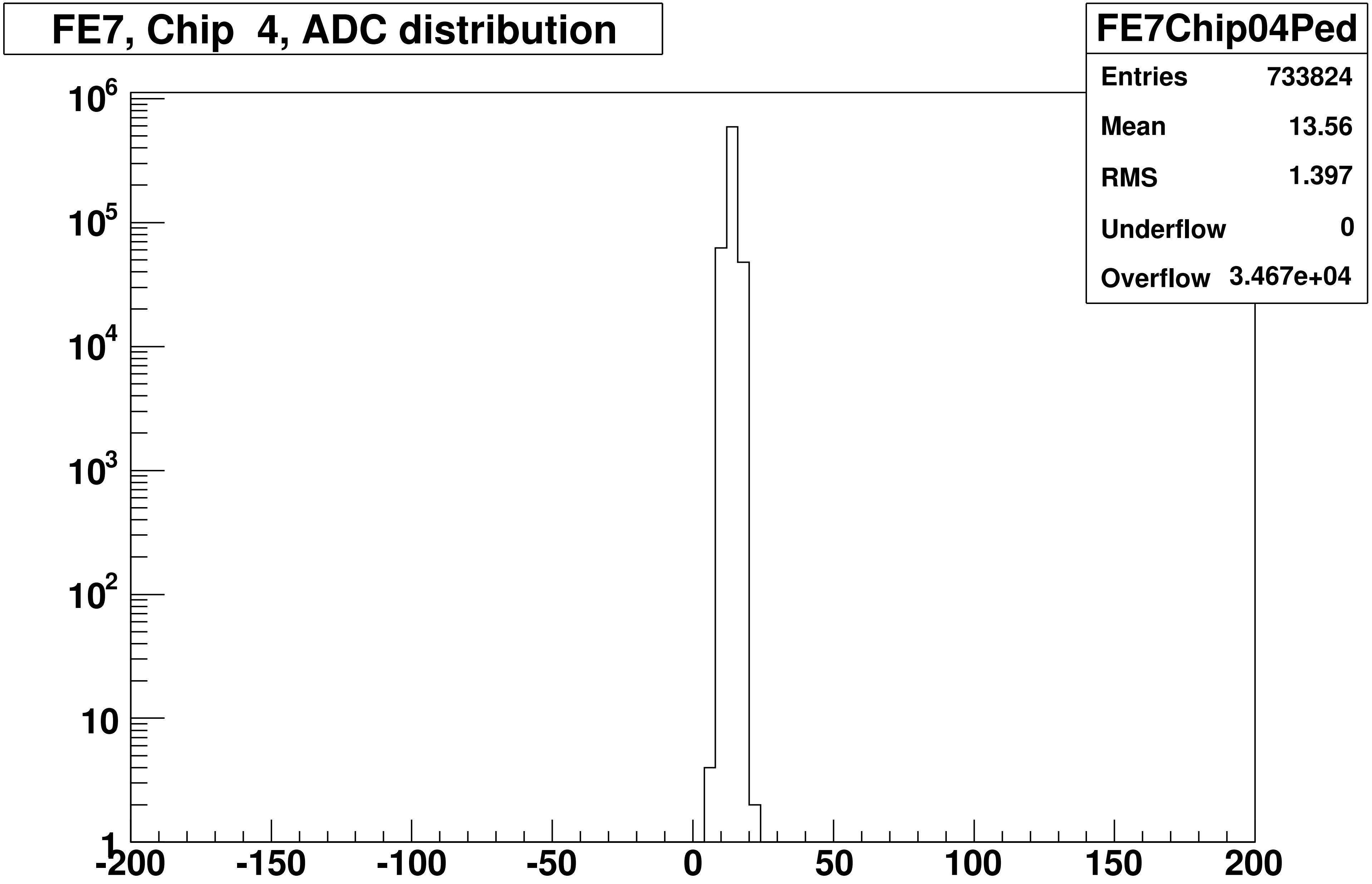
19600
19800
20000



FE7, Chip 4, ADC distribution
FE7Chip04All
Entries 733824
Mean 926.5
RMS 4100
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
-5000
0
5000
10000
15000
20000
25000



FE7, Chip 4, ADC distribution
FE7Chip04Ped
Entries 733824
Mean 13.56
RMS 1.397
Underflow 0
Overflow 3.467e+04
10^6
10^5
10^4
10^3
10^2
10
1
-200
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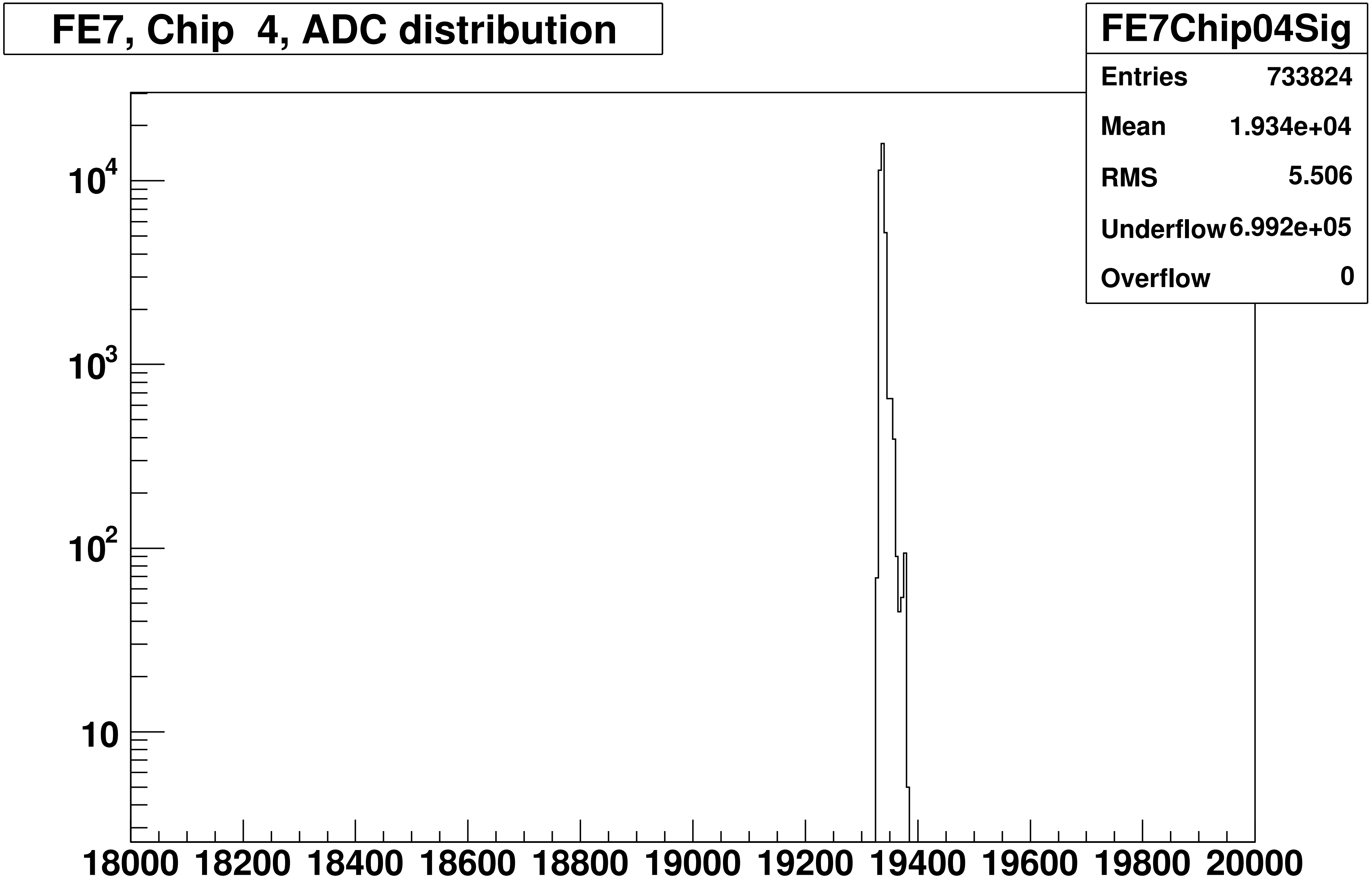
-100
-50
0
50
100
150
200


FE7, Chip 4, ADC distribution
FE7Chip04Sig
Entries 733824
Mean 1.934e+04
RMS 5.506
Underflow 6.992e+05
Overflow 0
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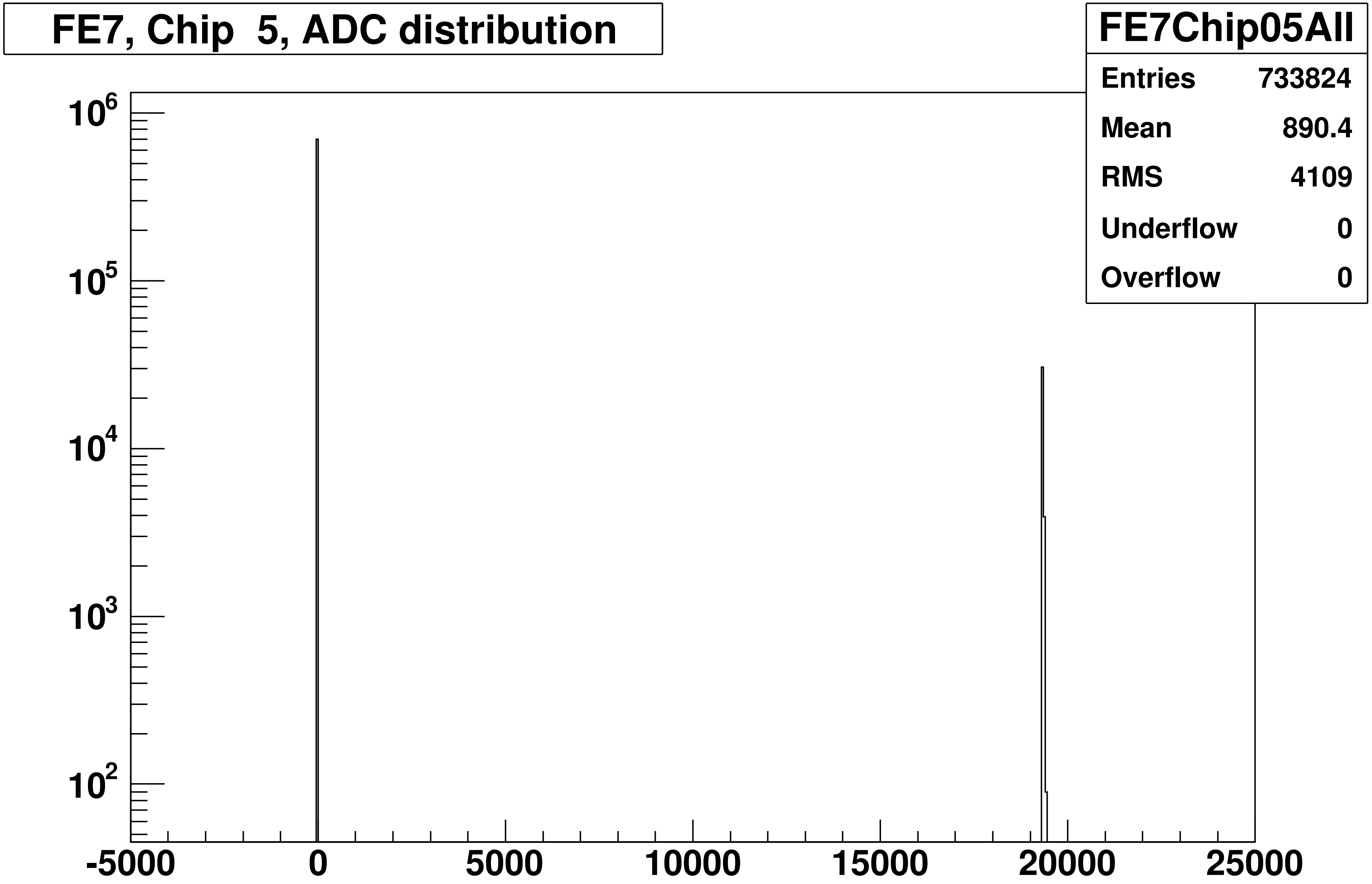
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE7, Chip 5, ADC distribution
FE7Chip05All
Entries 733824
Mean 890.4
RMS 4109
Underflow 0
Overflow 0
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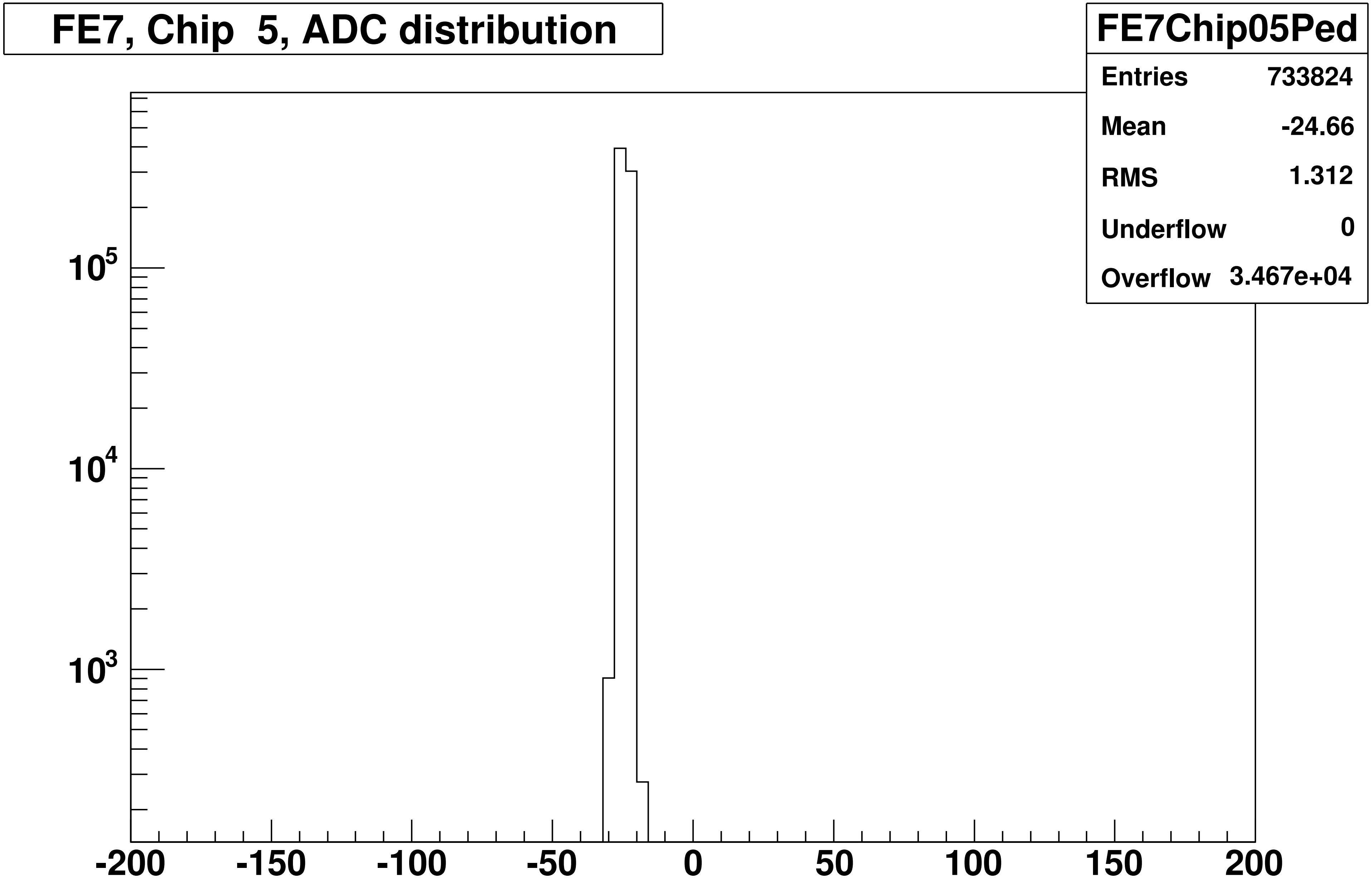
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000


FE7, Chip 5, ADC distribution
FE7Chip05Ped
Entries 733824
Mean -24.66
RMS 1.312
Underflow 0
Overflow 3.467e+04
10^5
10^4
10^3
-200
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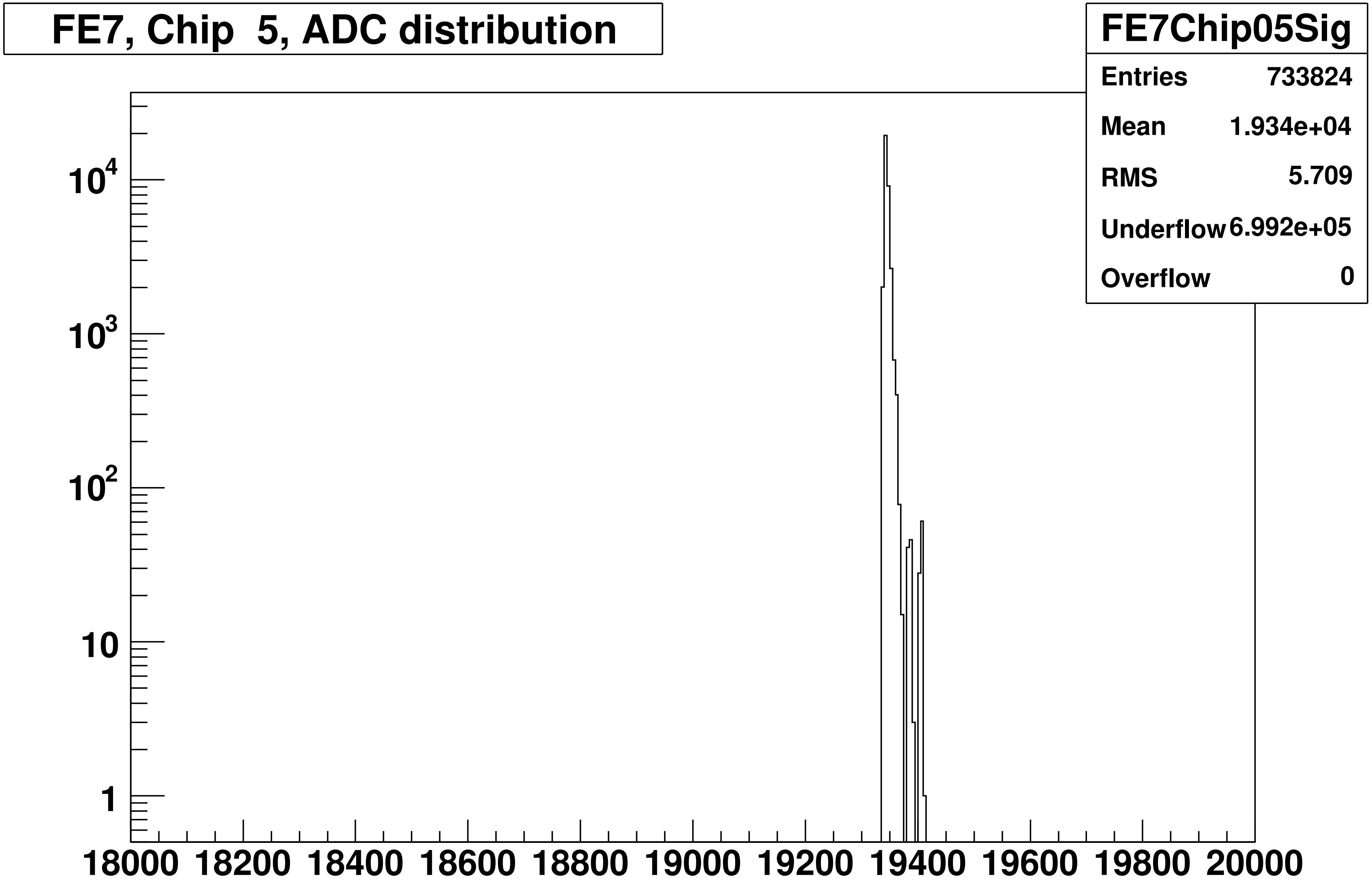
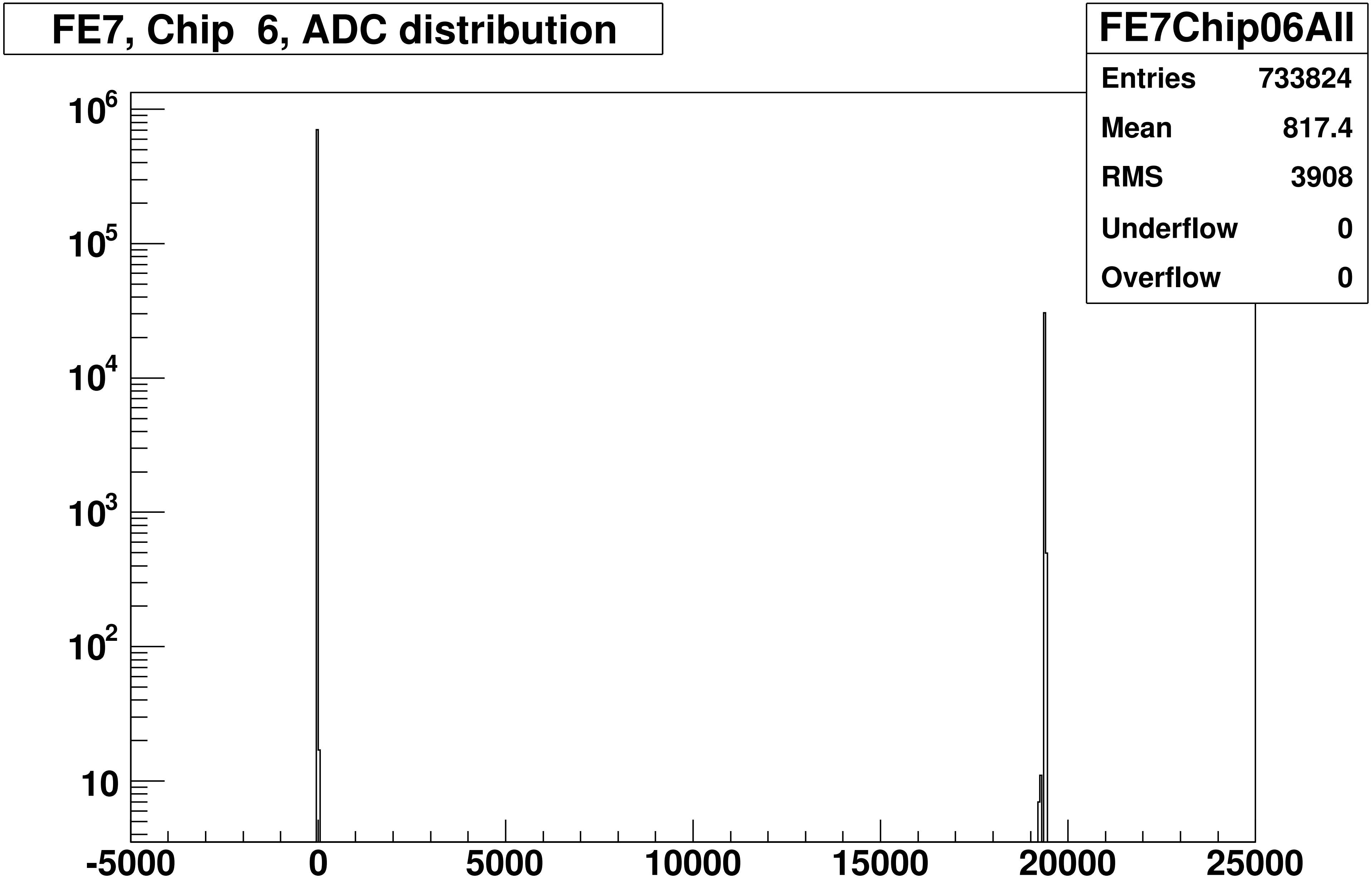
-100
-50
0
50
100
150
200


FE7, Chip 5, ADC distribution
FE7Chip05Sig
Entries 733824
Mean 1.934e+04
RMS 5.709
Underflow 6.992e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000



FE7, Chip 6, ADC distribution
FE7Chip06All
Entries 733824
Mean 817.4
RMS 3908
Underflow 0
Overflow 0
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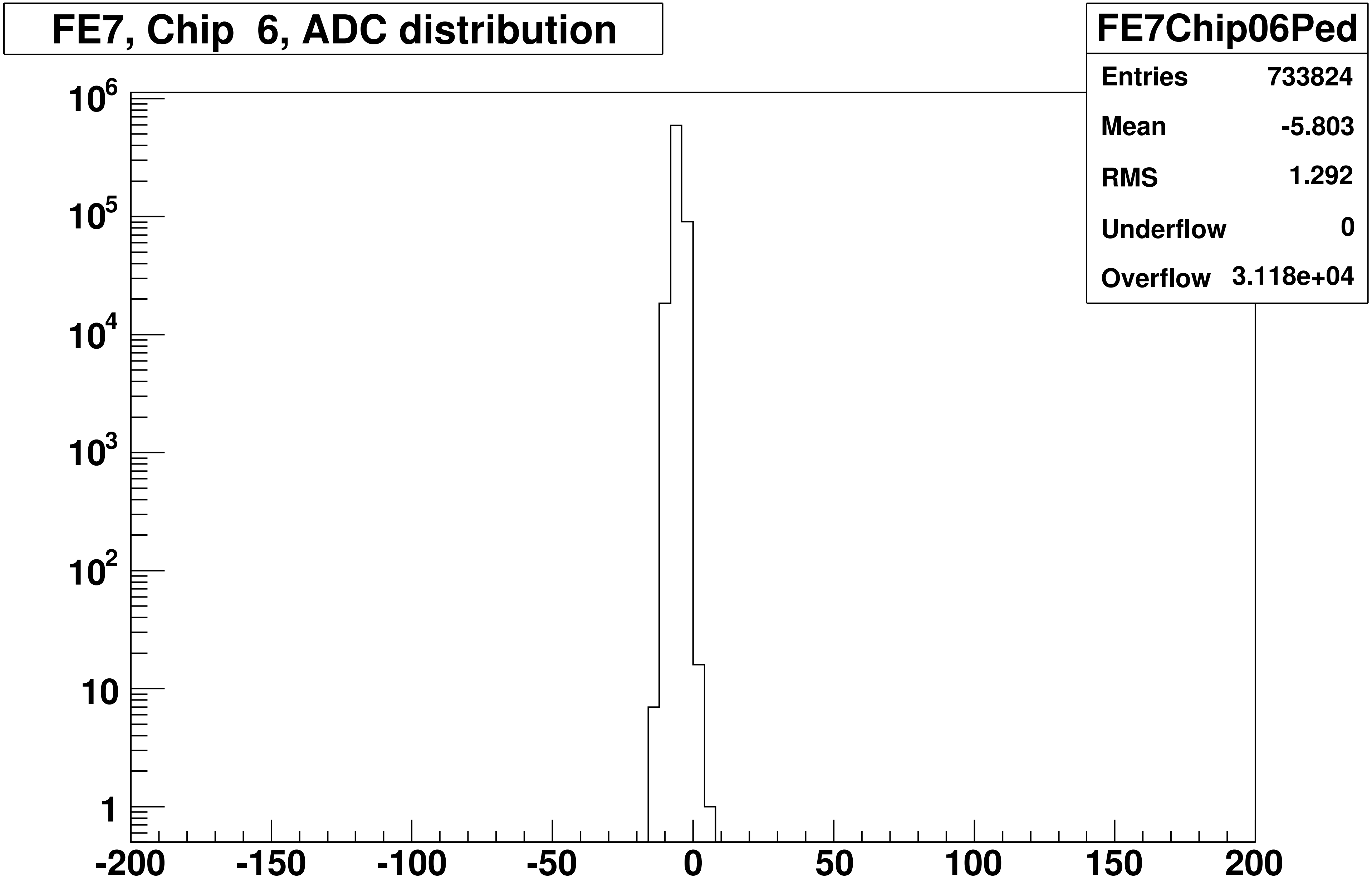
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000



FE7, Chip 6, ADC distribution
FE7Chip06Ped
Entries 733824
Mean -5.803
RMS 1.292
Underflow 0
Overflow 3.118e+04
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10^5
10^4
10^3
10^2
10
1
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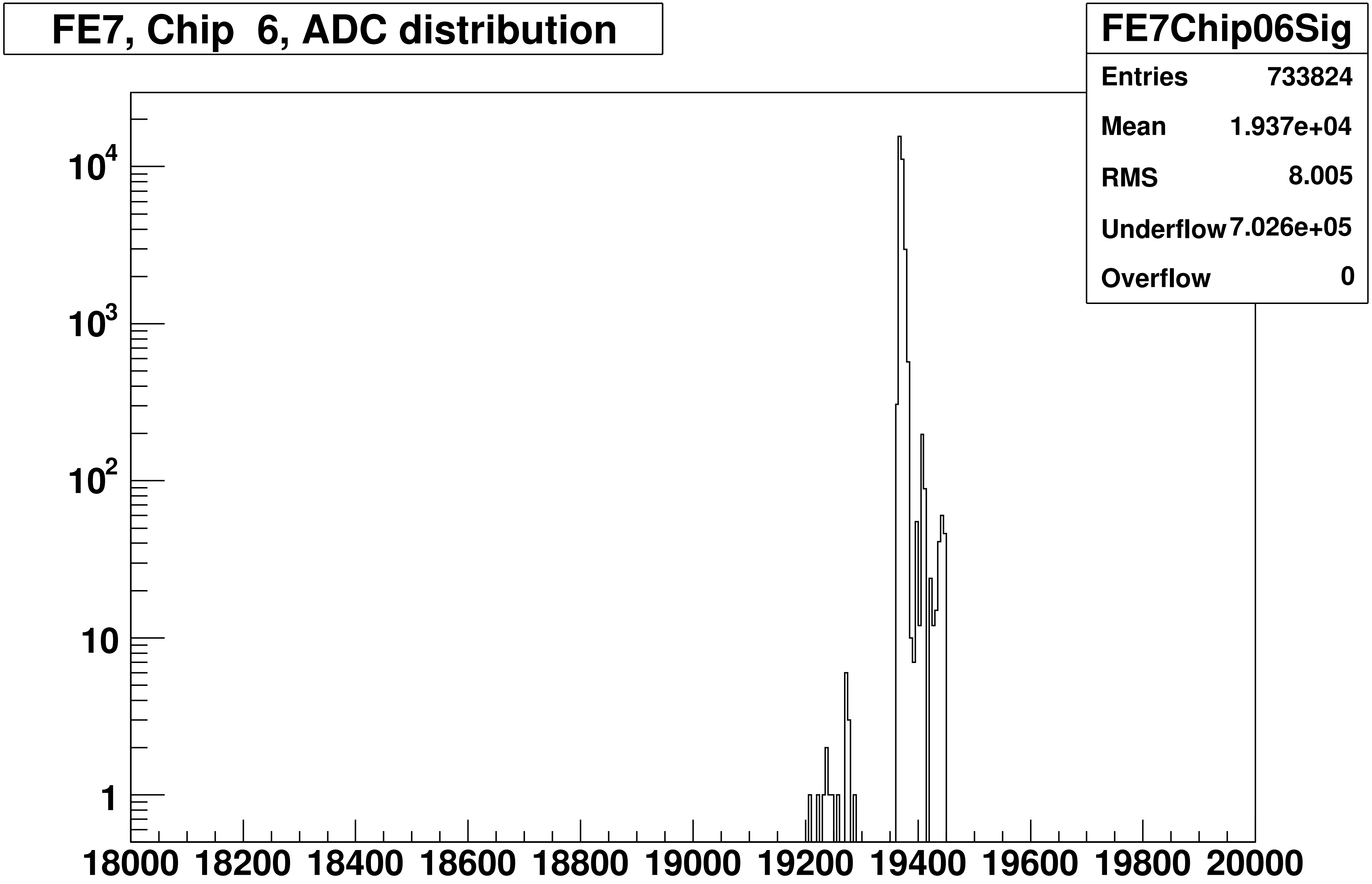
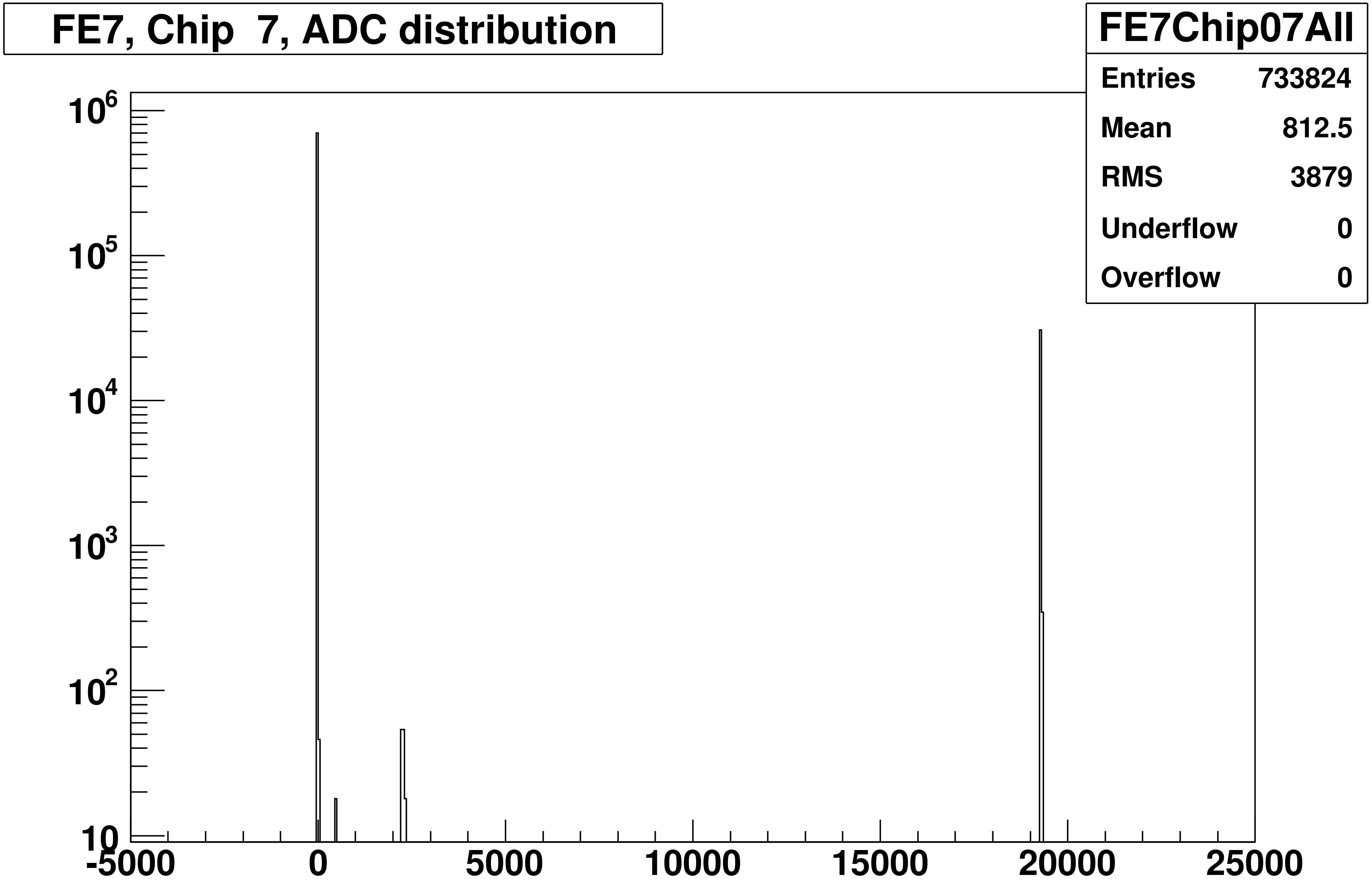
-150
-100
-50
0
50
100
150
200



FE7, Chip 6, ADC distribution
FE7Chip06Sig
Entries 733824
Mean 1.937e+04
RMS 8.005
Underflow 7.026e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE7, Chip 7, ADC distribution
FE7Chip07All
Entries 733824
Mean 812.5
RMS 3879
Underflow 0
Overflow 0
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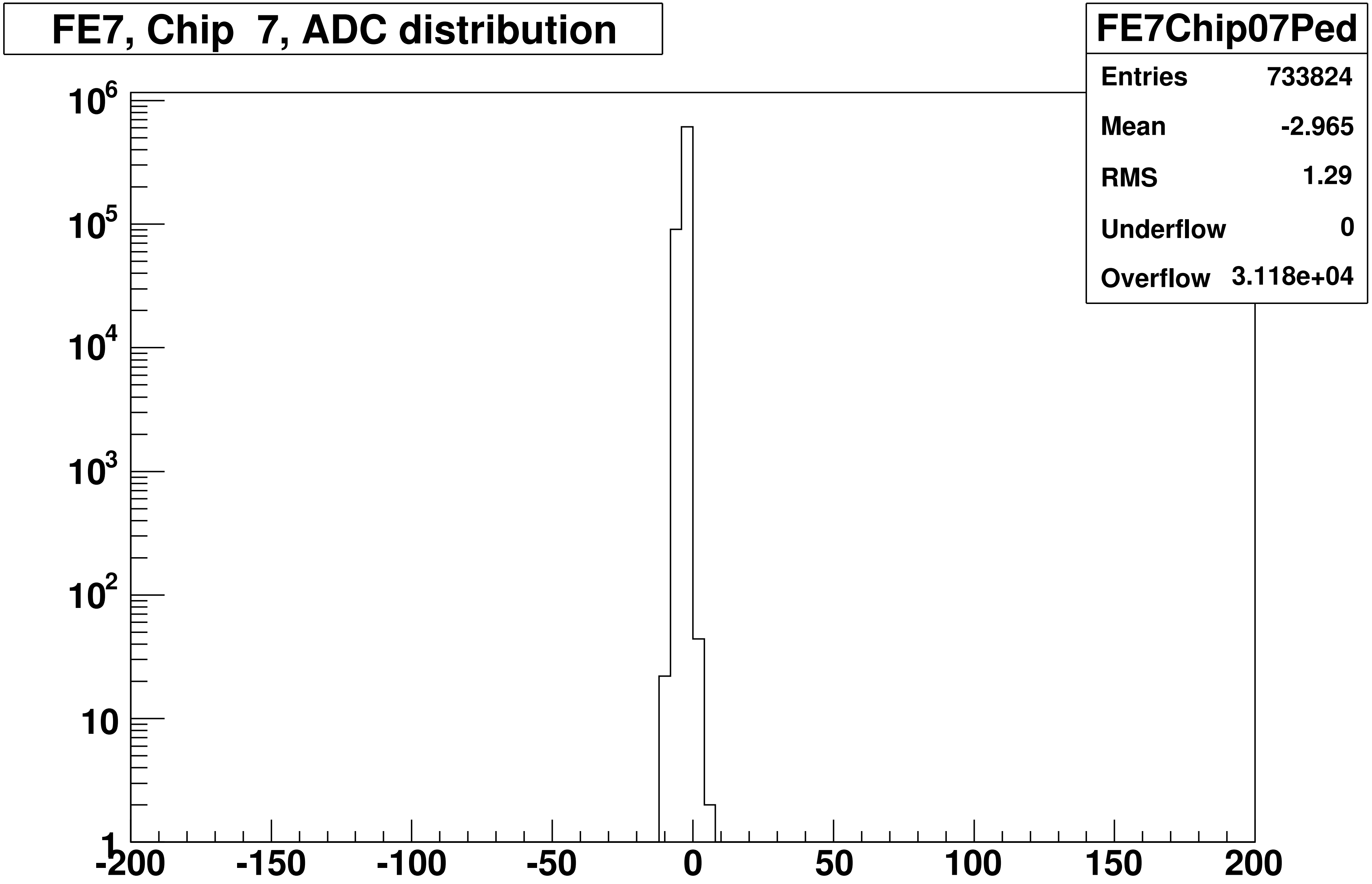
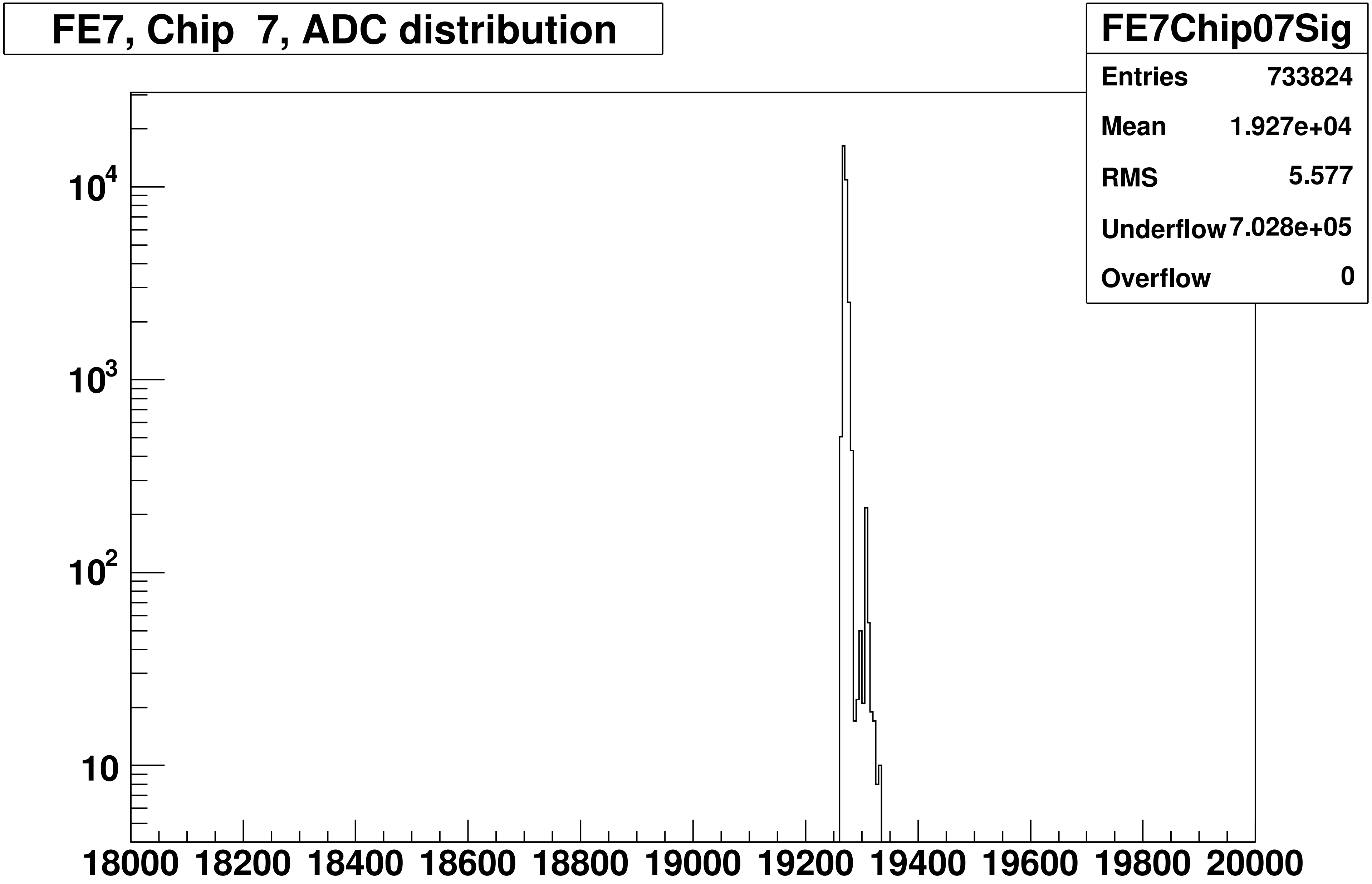
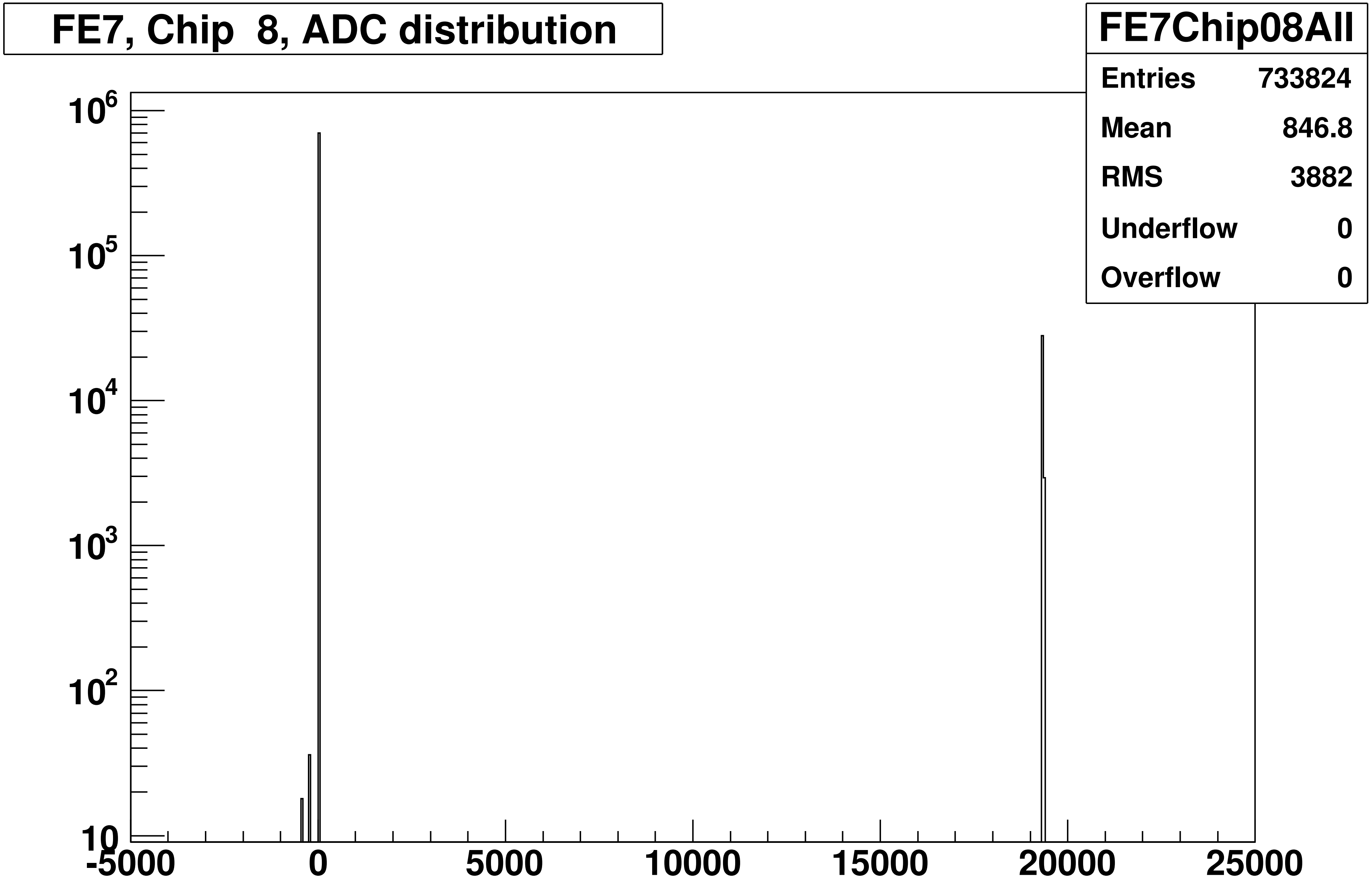
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000

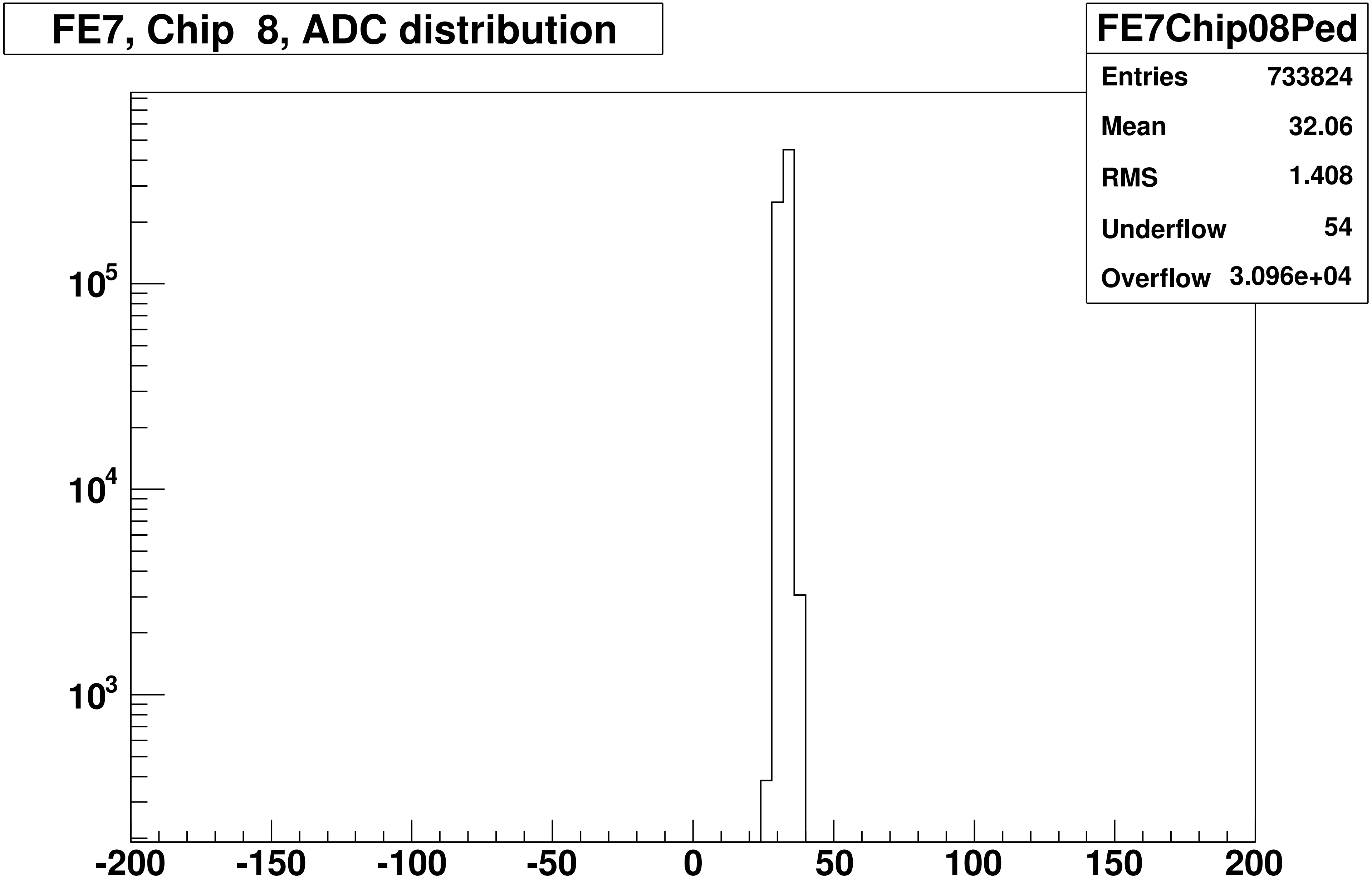


FE7, Chip 7, ADC distribution
FE7Chip07Ped
Entries 733824
Mean -2.965
RMS 1.29
Underflow 0
Overflow 3.118e+04
10^6
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
200

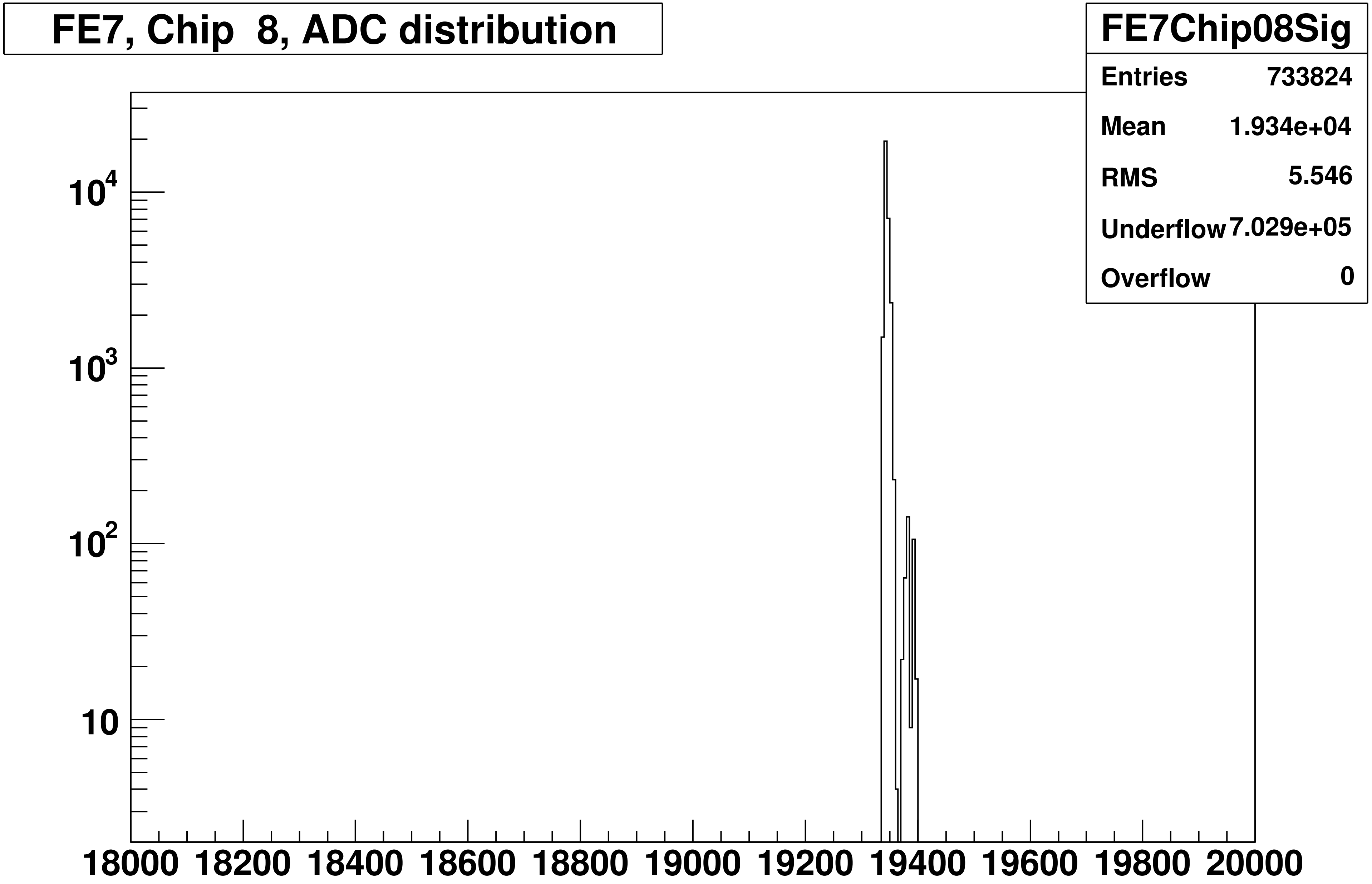

FE7, Chip 7, ADC distribution
FE7Chip07Sig
Entries 733824
Mean 1.927e+04
RMS 5.577
Underflow 7.028e+05
Overflow 0
10^4
10^3
10^2
10
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000



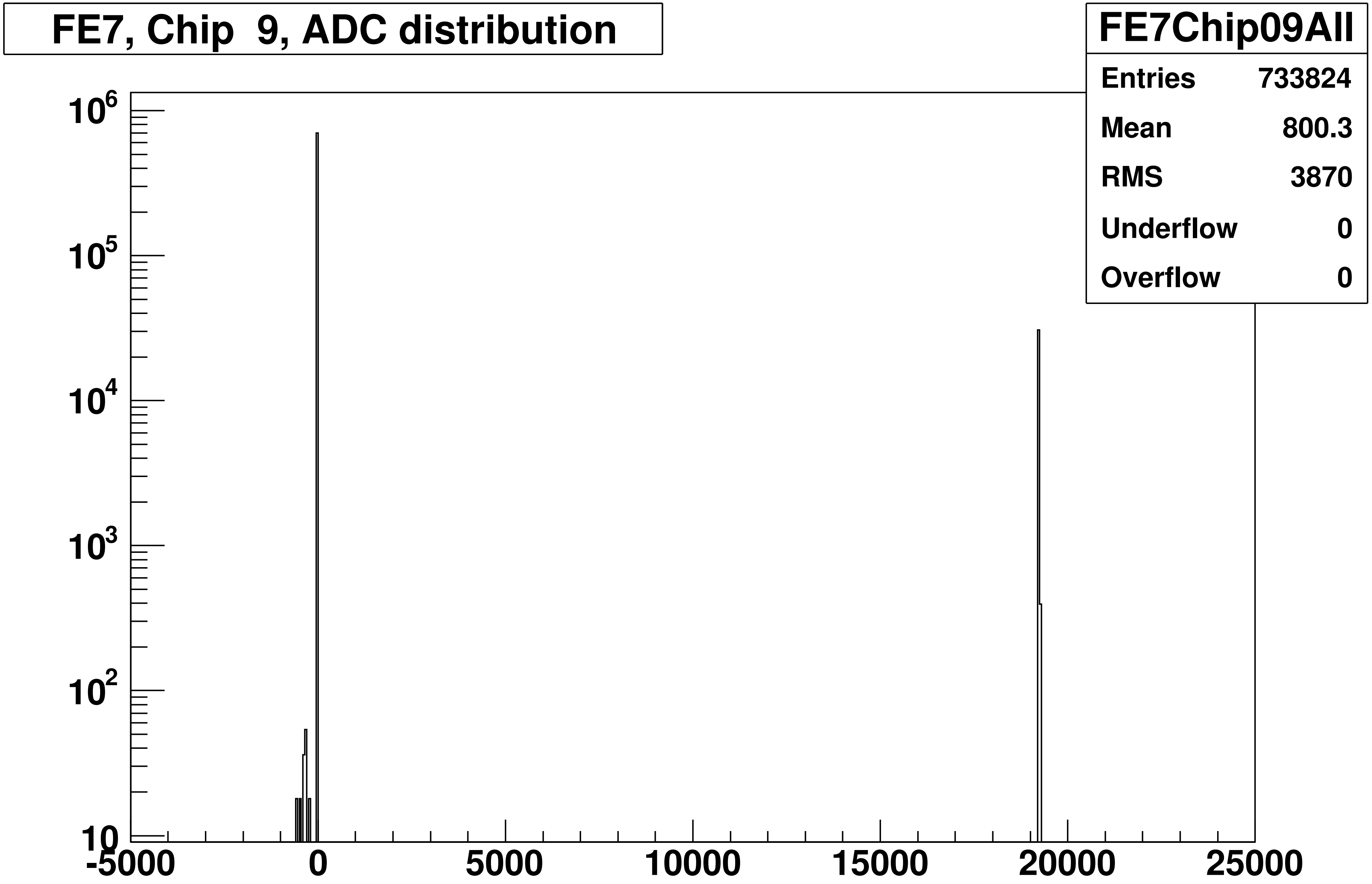
FE7, Chip 8, ADC distribution
FE7Chip08All
Entries 733824
Mean 846.8
RMS 3882
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000



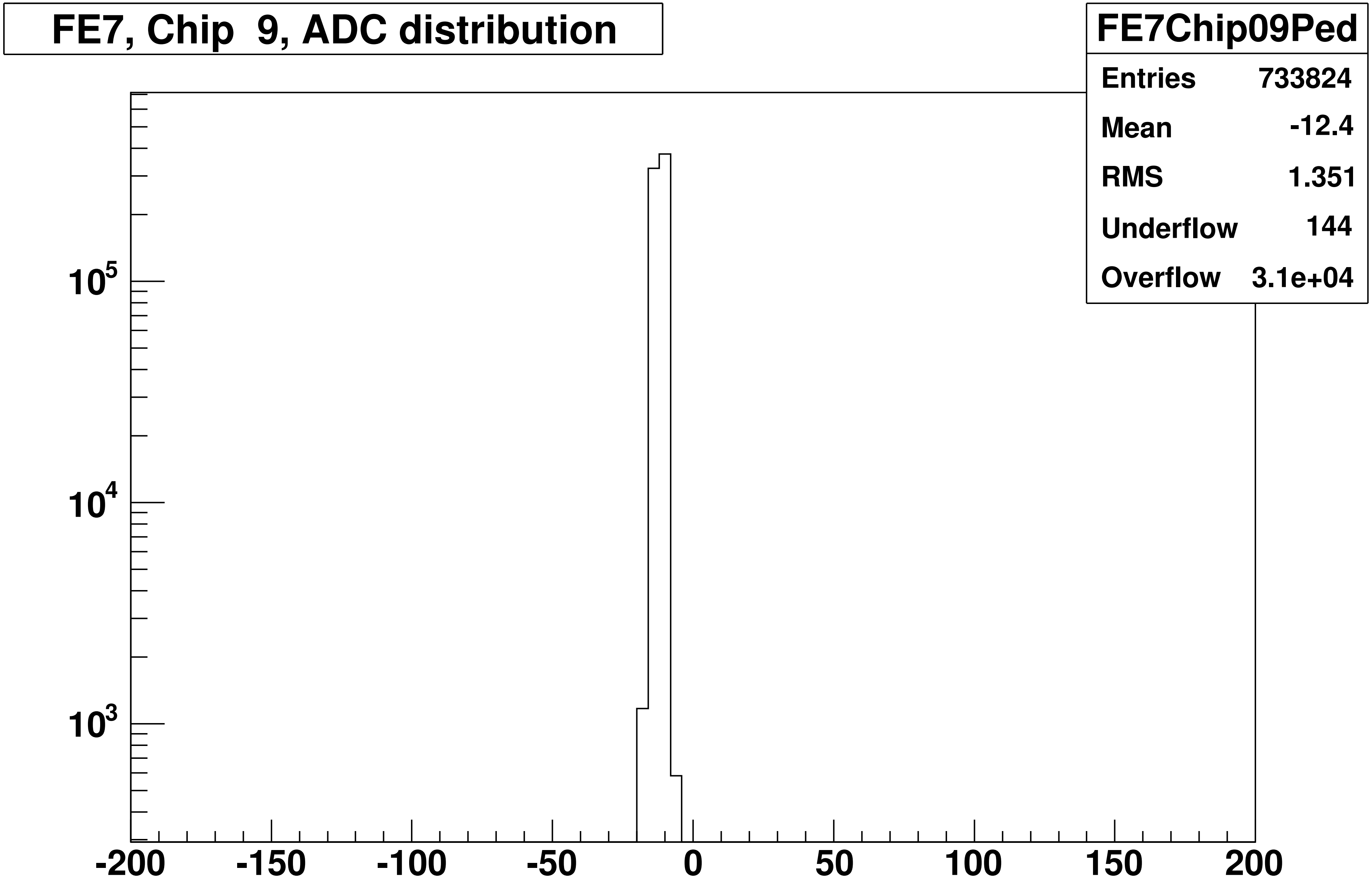
FE7, Chip 8, ADC distribution
FE7Chip08Ped
Entries 733824
Mean 32.06
RMS 1.408
Underflow 54
Overflow 3.096e+04
10^5
10^4
10^3
-200
-150
-100
-50
0
50
100
150
200

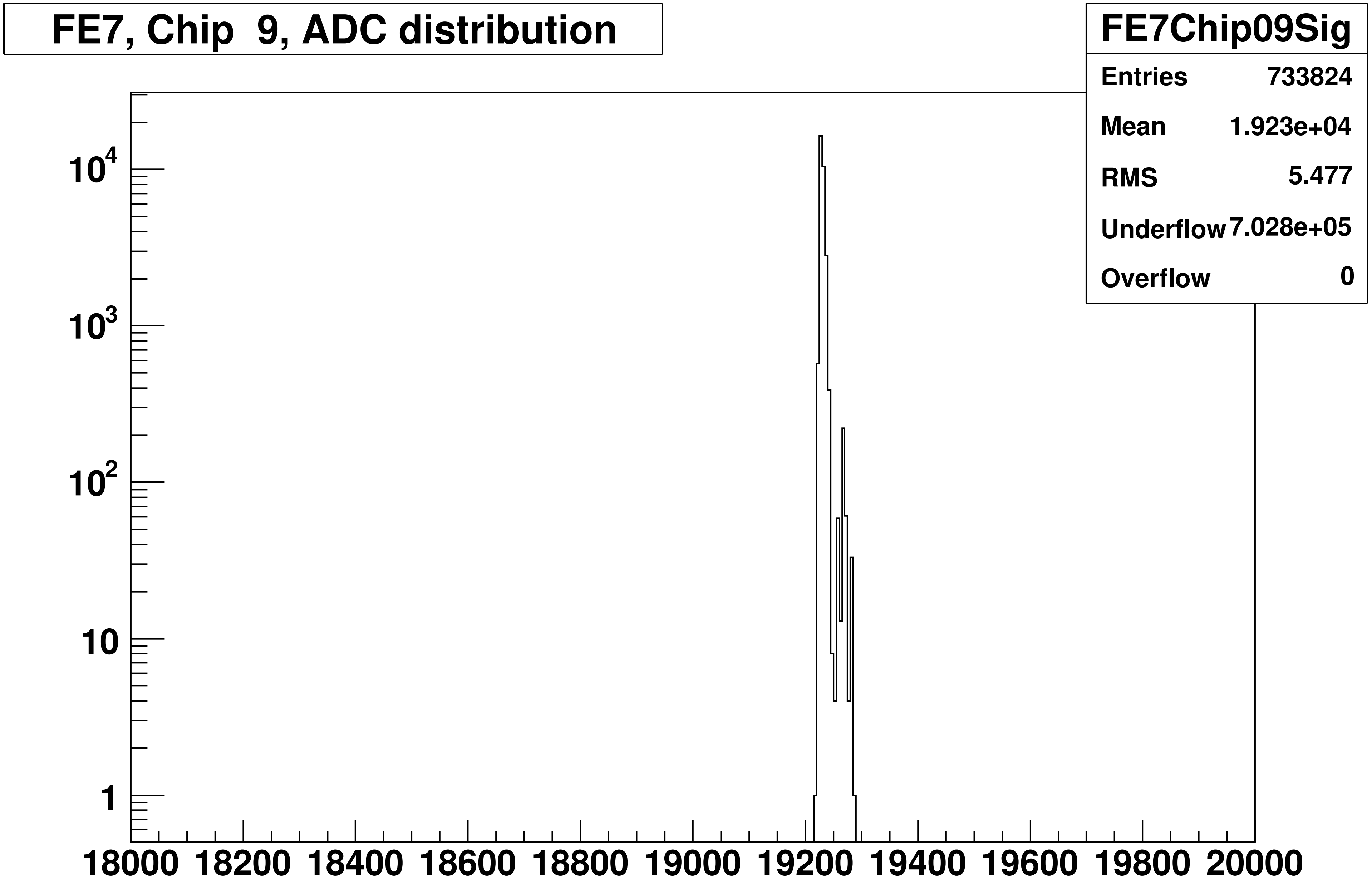


FE7, Chip 8, ADC distribution
FE7Chip08Sig
Entries 733824
Mean 1.934e+04
RMS 5.546
Underflow 7.029e+05
Overflow 0
10^4
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000

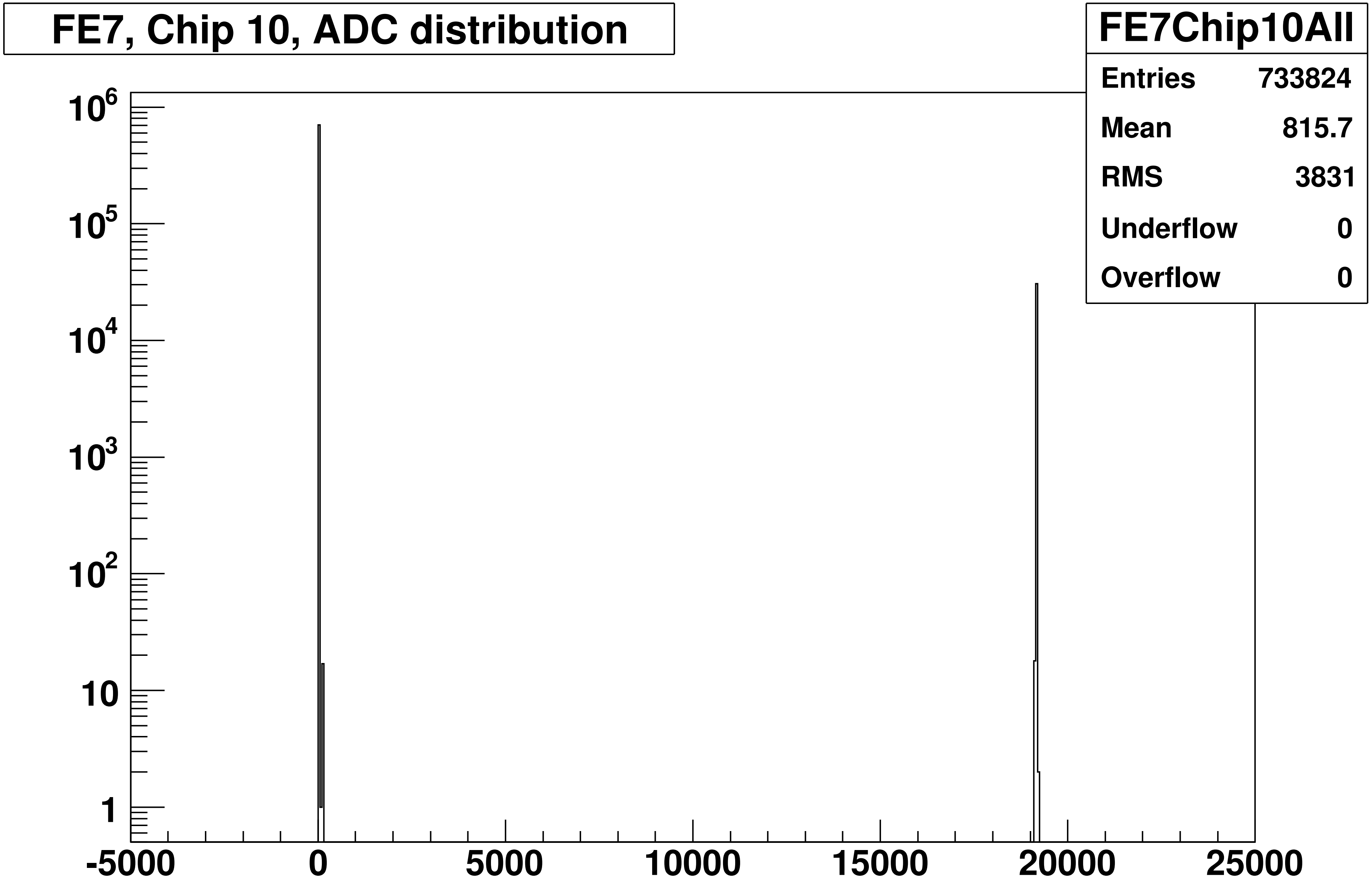


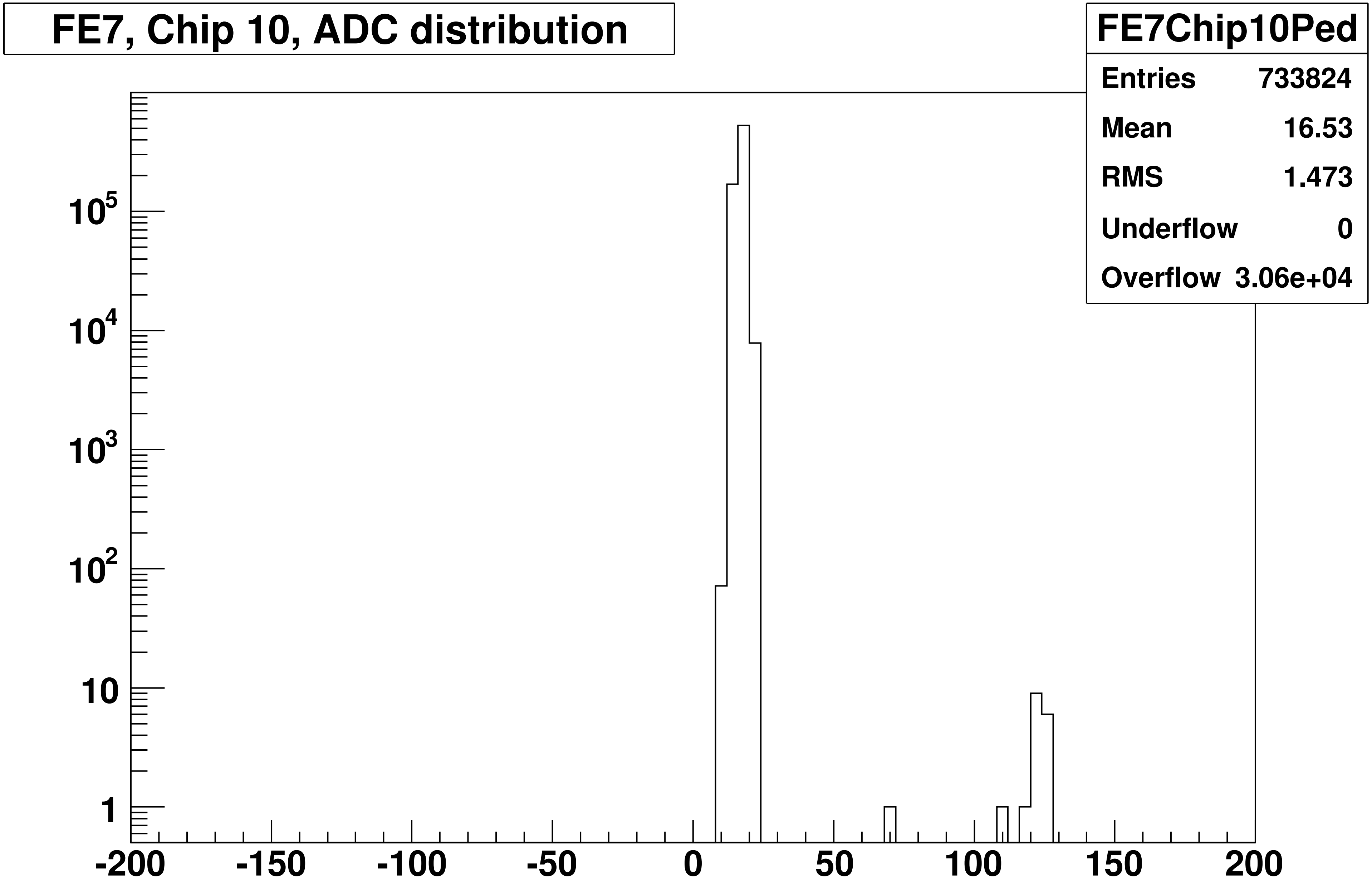
FE7, Chip 9, ADC distribution
FE7Chip09All
Entries 733824
Mean 800.3
RMS 3870
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE7, Chip 9, ADC distribution
FE7Chip09Ped
Entries 733824
Mean -12.4
RMS 1.351
Underflow 144
Overflow 3.1e+04
10^5
10^4
10^3
-200
-150
-100
-50
0
50
100
150
200

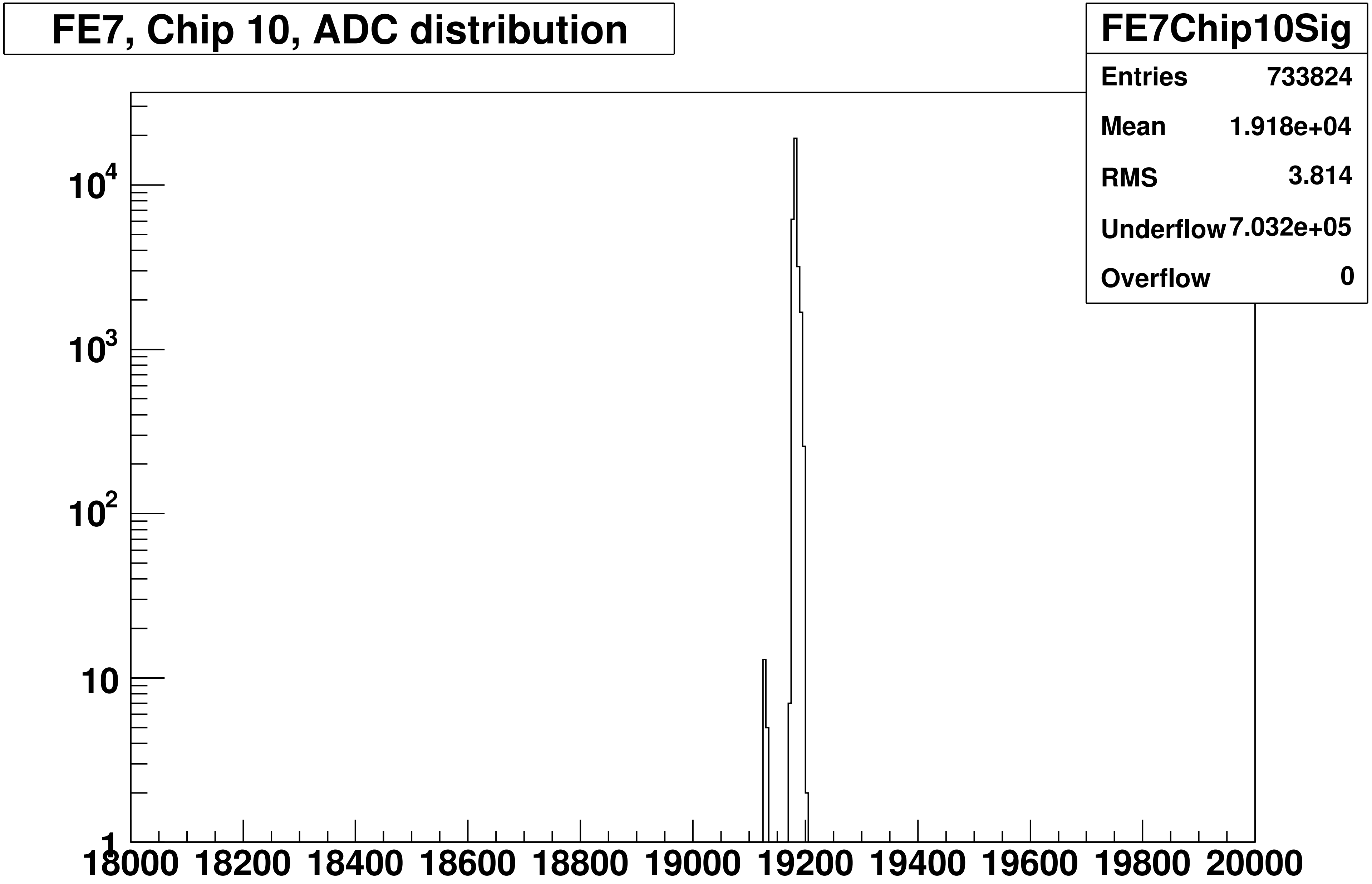


FE7, Chip 9, ADC distribution
FE7Chip09Sig
Entries 733824
Mean 1.923e+04
RMS 5.477
Underflow 7.028e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000

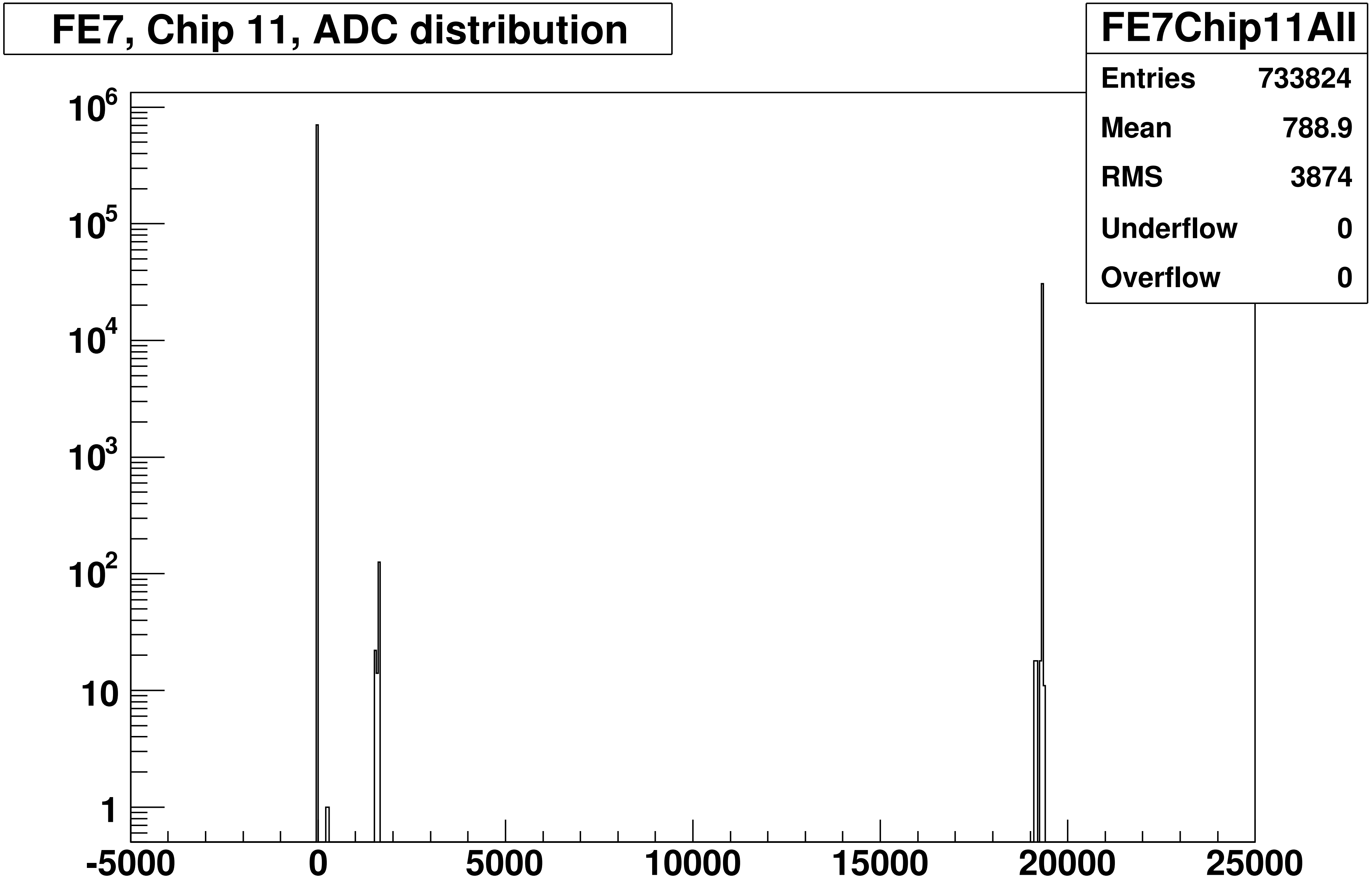

FE7, Chip 10, ADC distribution
FE7Chip10All
Entries 733824
Mean 815.7
RMS 3831
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000

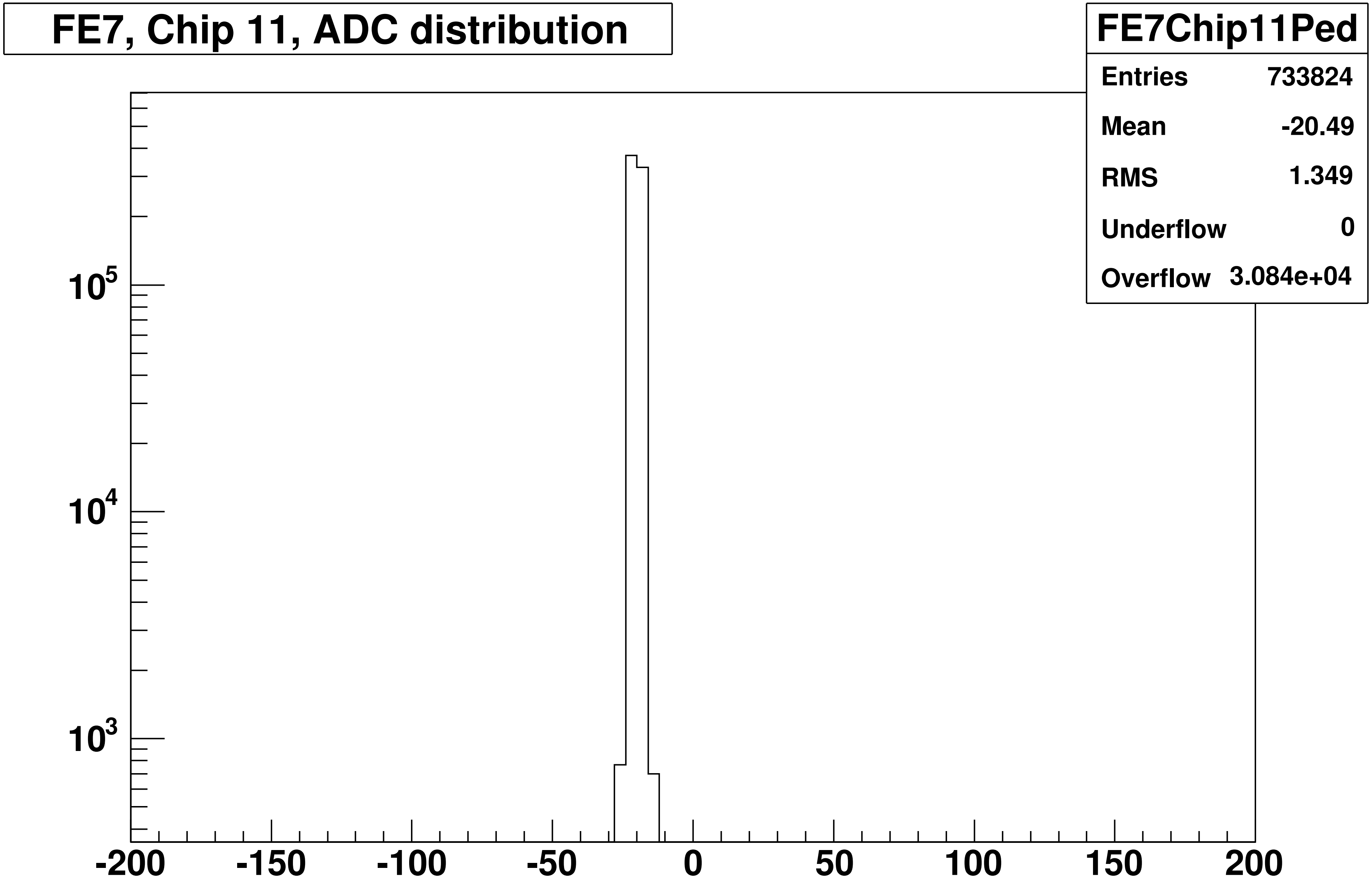


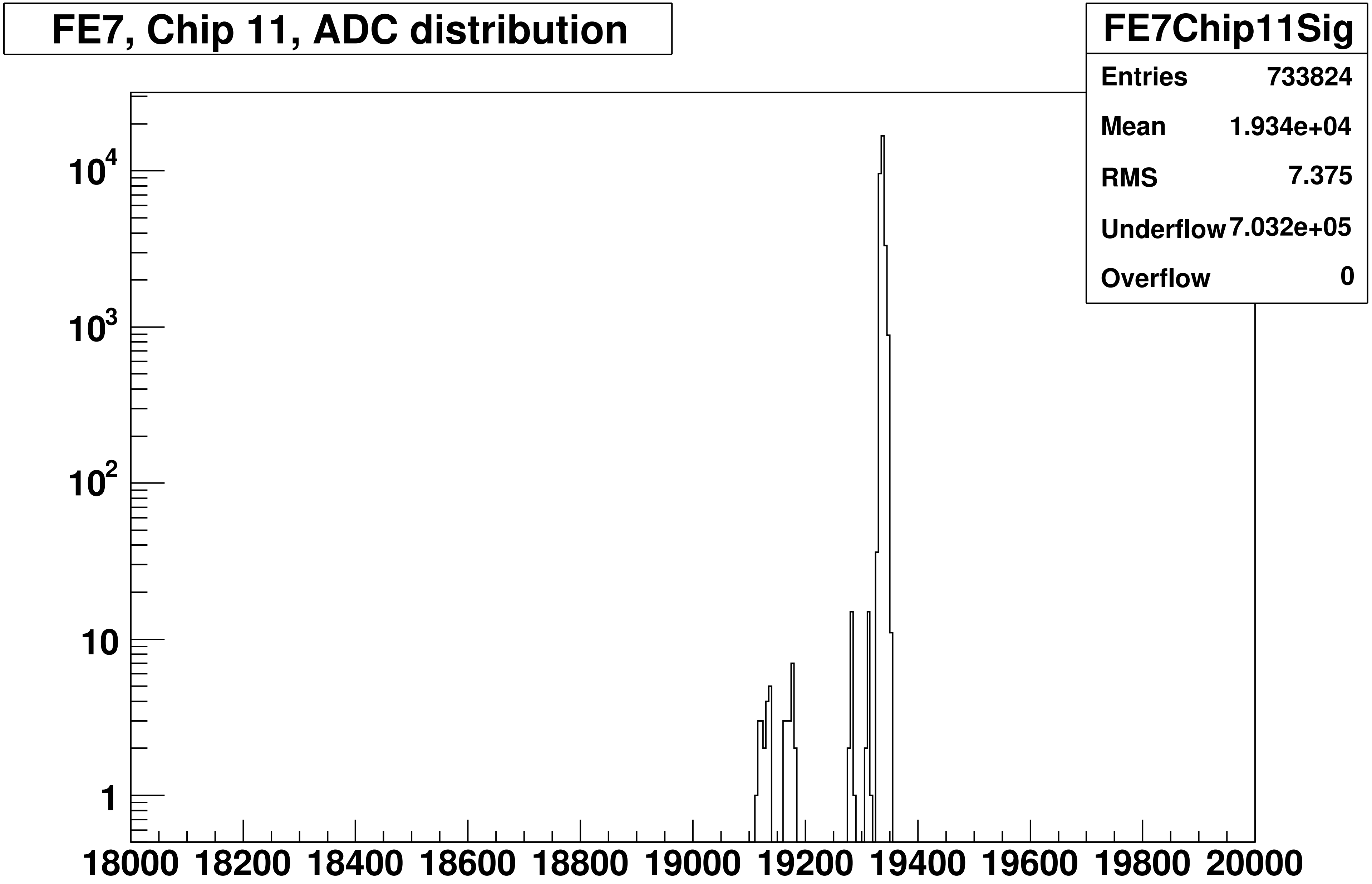
FE7, Chip 10, ADC distribution
FE7Chip10Ped
Entries 733824
Mean 16.53
RMS 1.473
Underflow 0
Overflow 3.06e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
200



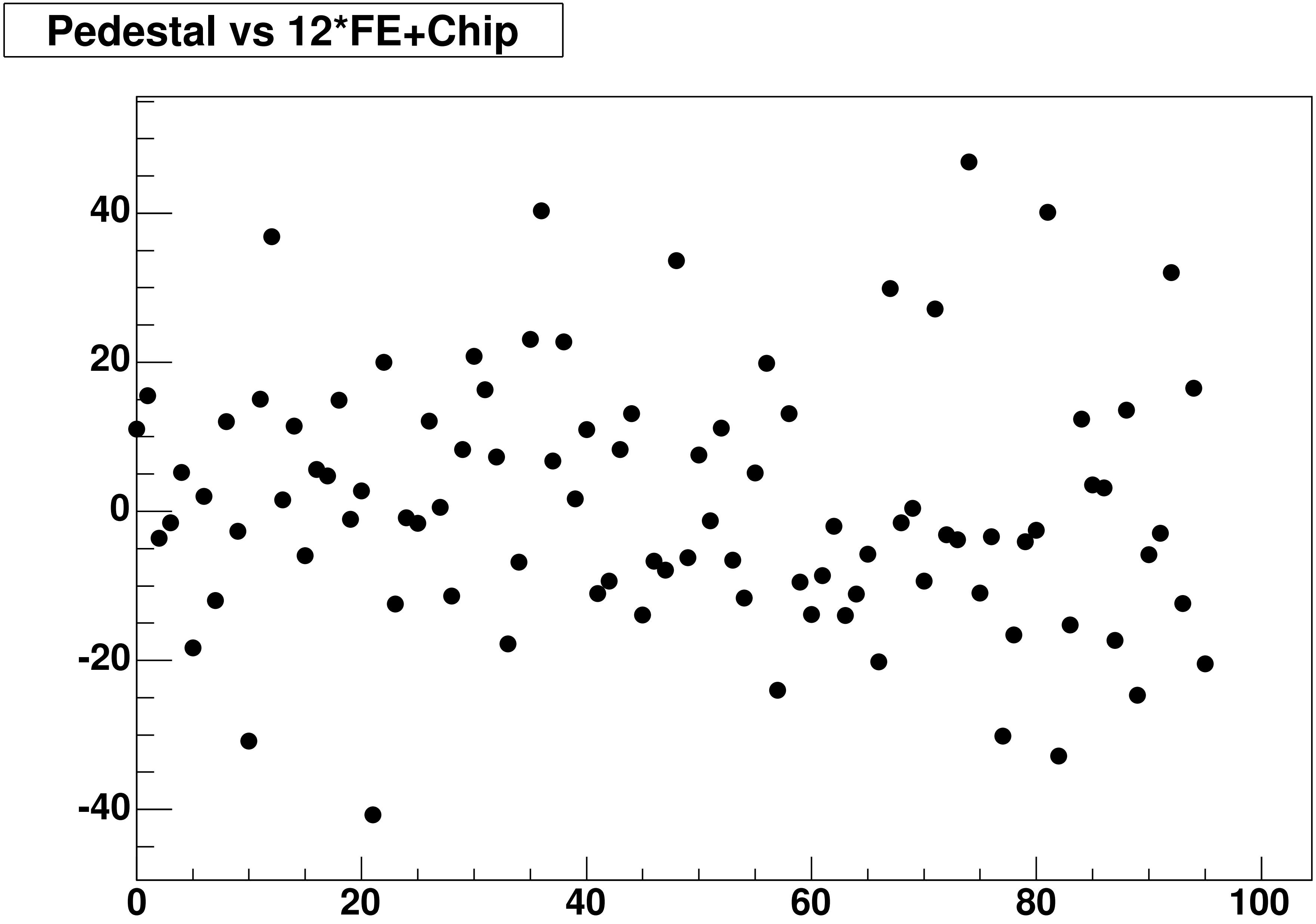
FE7, Chip 10, ADC distribution
FE7Chip10Sig
Entries 733824
Mean 1.918e+04
RMS 3.814
Underflow 7.032e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000

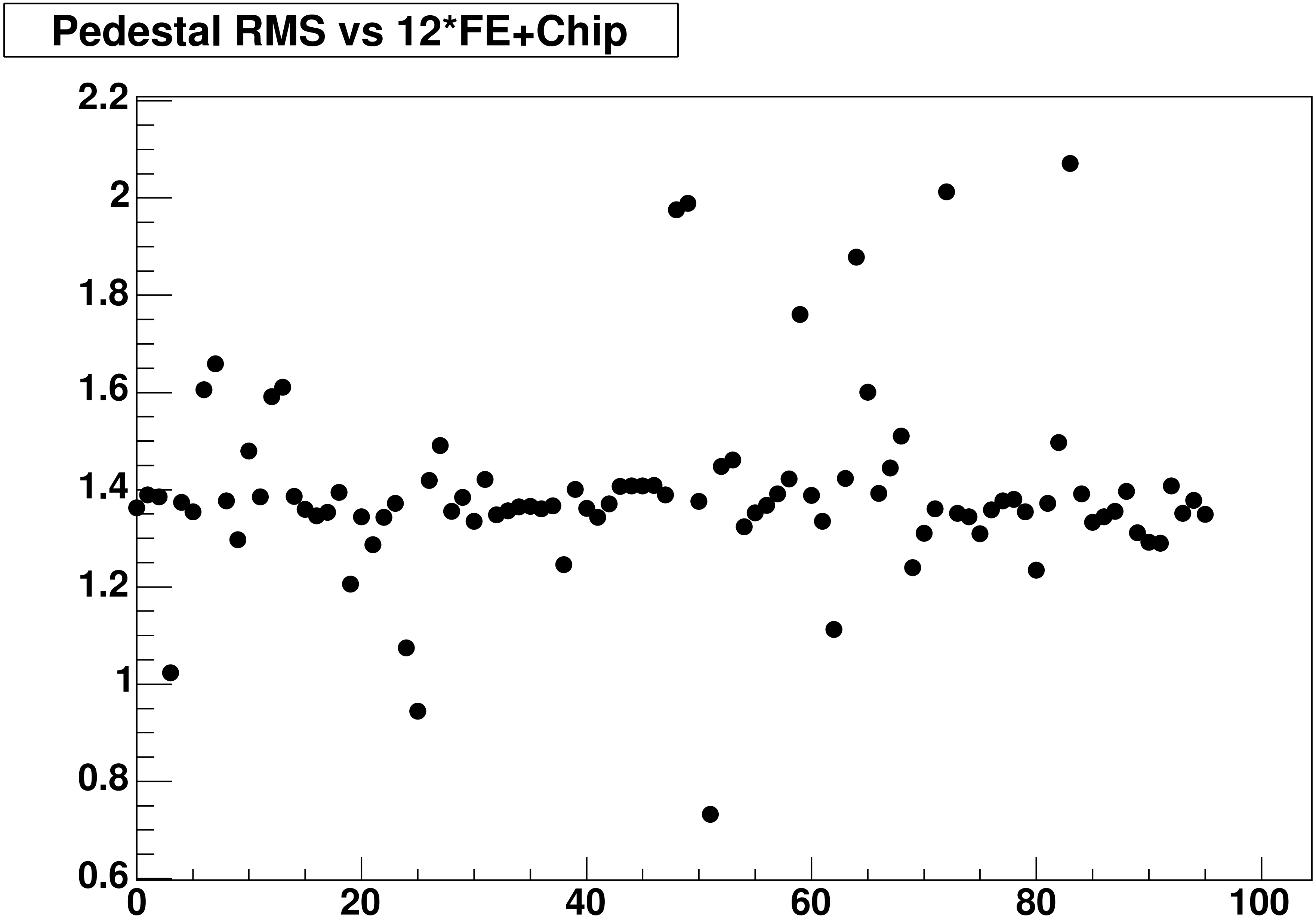

FE7, Chip 11, ADC distribution
FE7Chip11All
Entries 733824
Mean 788.9
RMS 3874
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE7, Chip 11, ADC distribution
FE7Chip11Ped
Entries 733824
Mean -20.49
RMS 1.349
Underflow 0
Overflow 3.084e+04
10^5
10^4
10^3
-200
-150
-100
-50
0
50
100
150
200

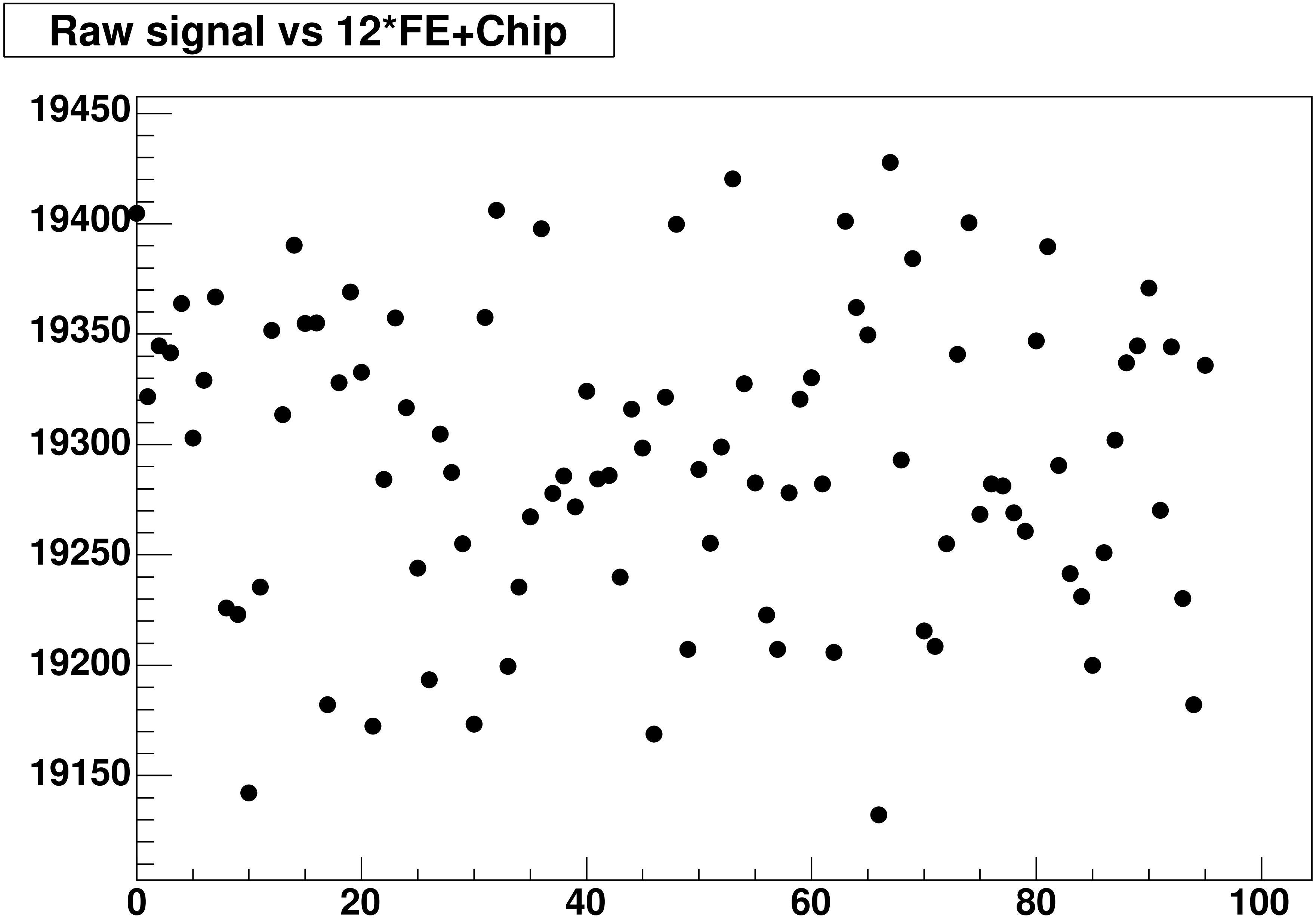


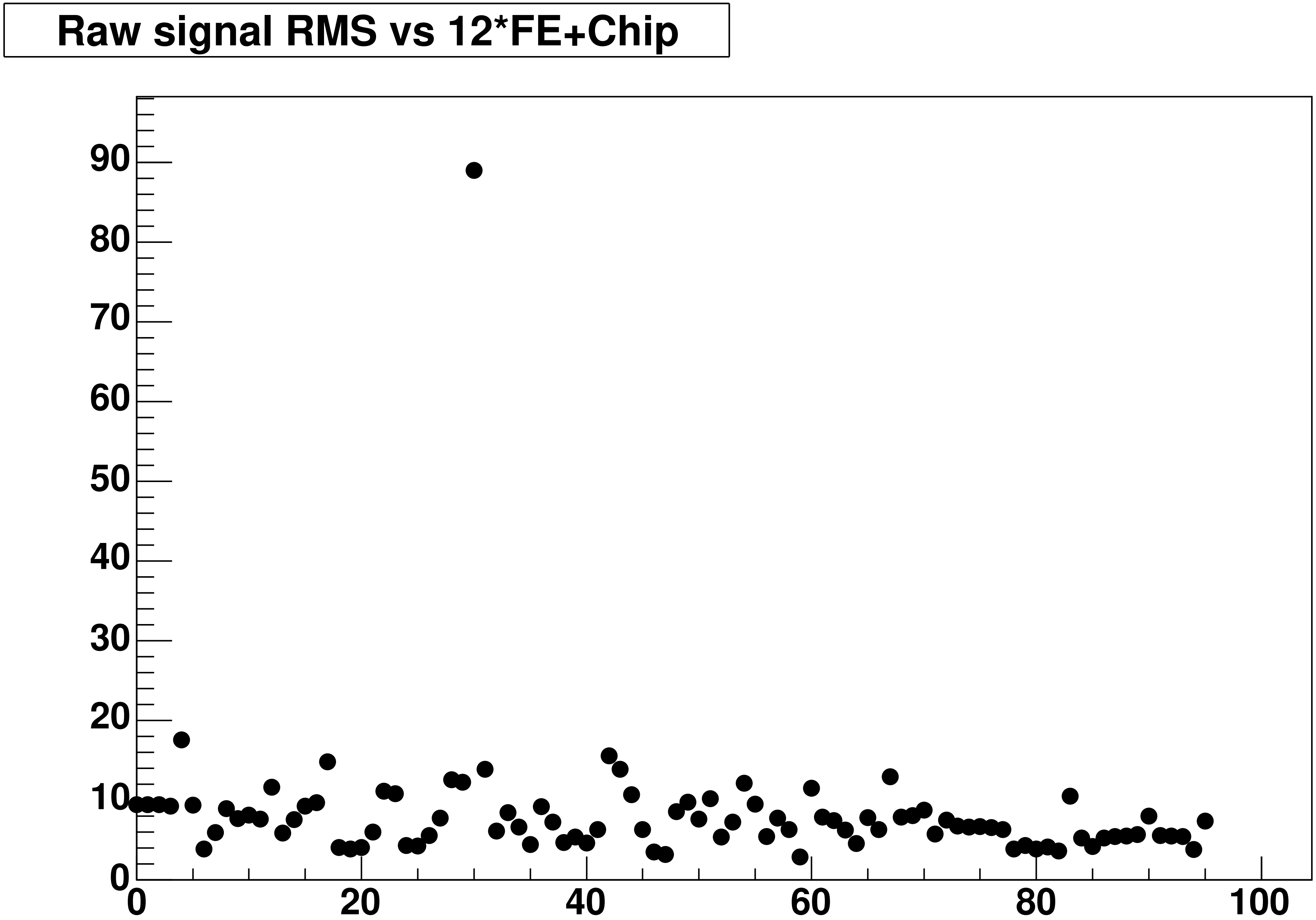
FE7, Chip 11, ADC distribution
FE7Chip11Sig
Entries 733824
Mean 1.934e+04
RMS 7.375
Underflow 7.032e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000

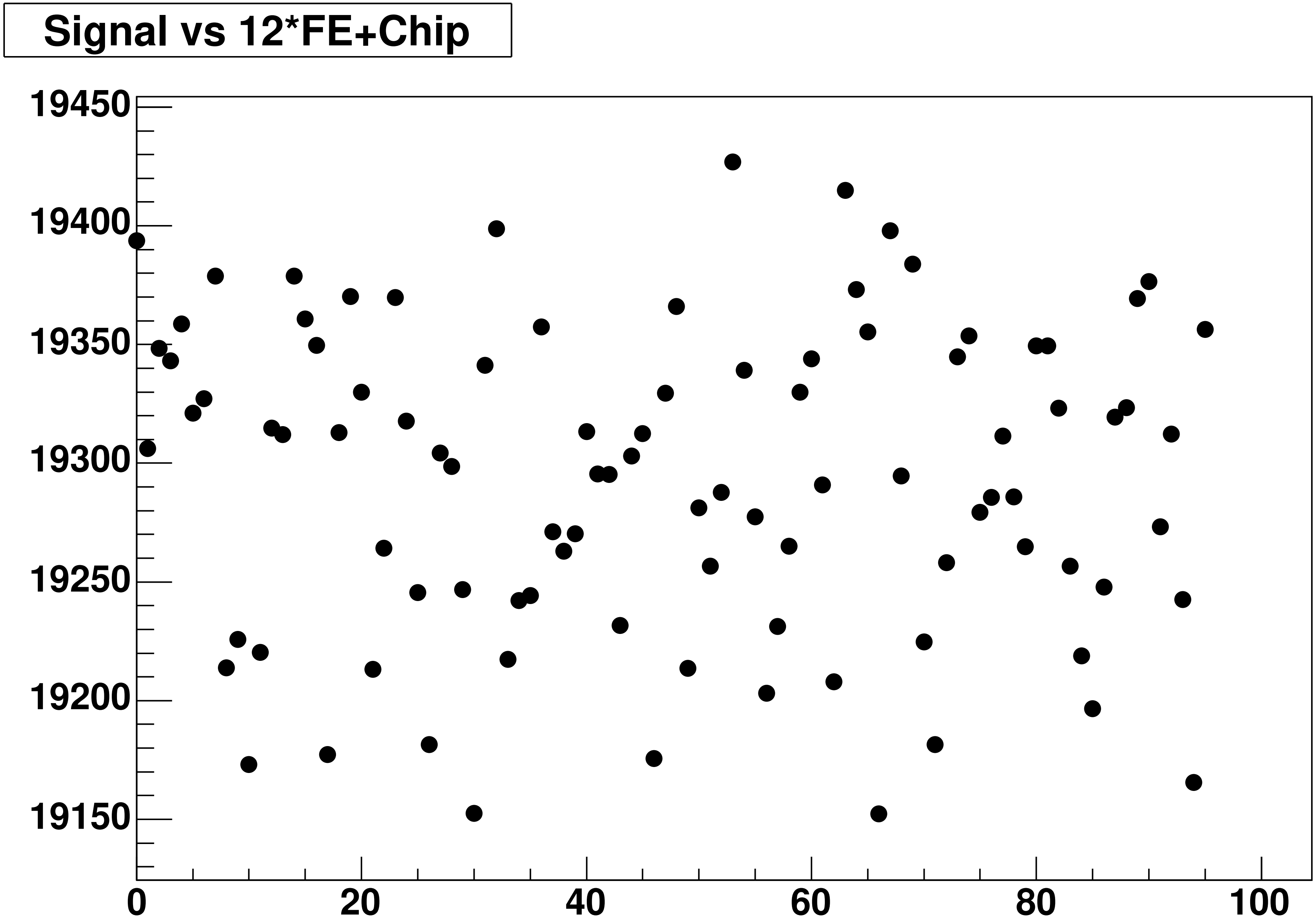

Pedestal vs 12*FE+Chip
40
20
0
-20
-40
0
20
40
60
80
100

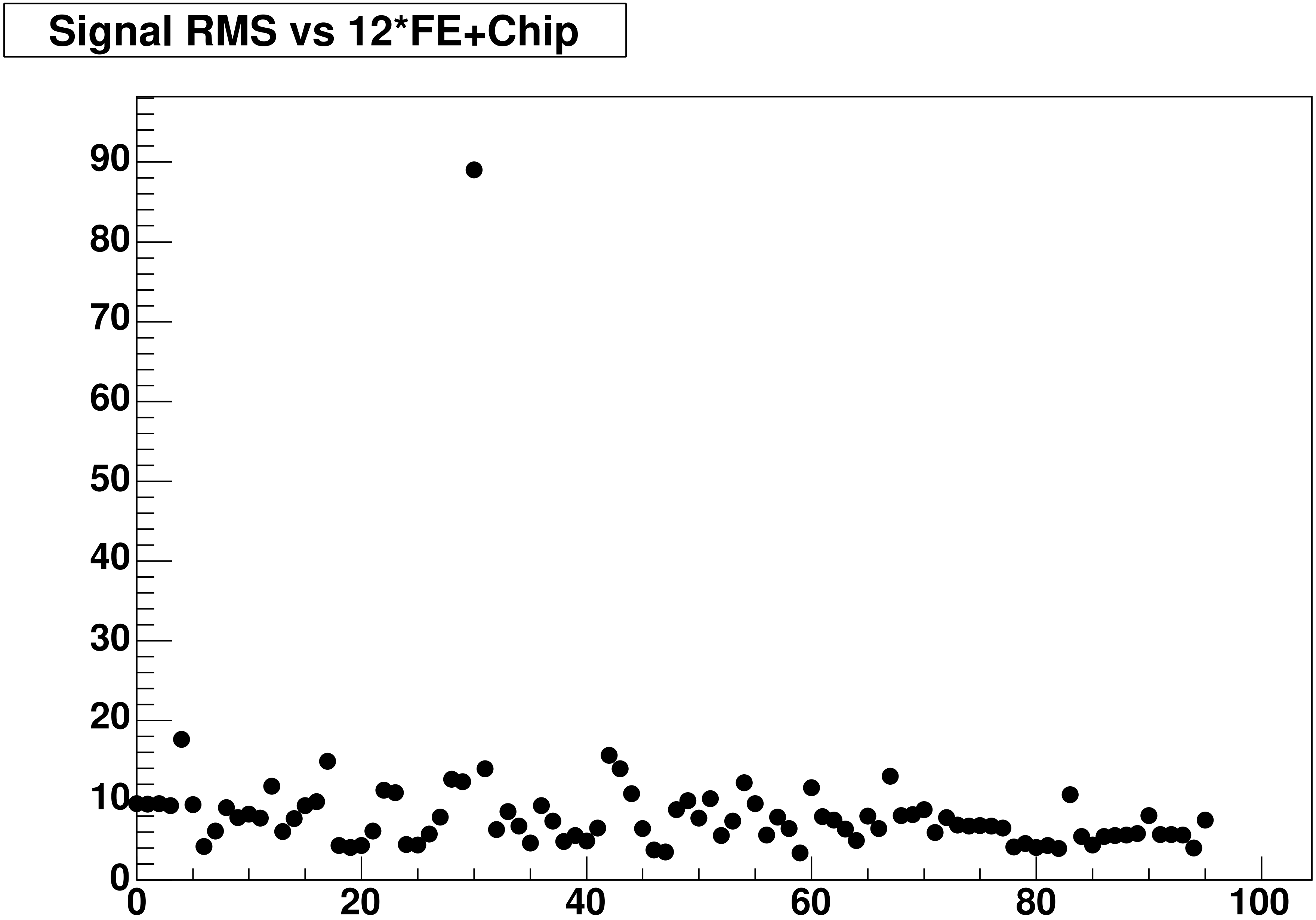


Pedestal RMS vs 12*FE+Chip
2.2
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0
20
40
60
80
100


Raw signal vs 12*FE+Chip
19450
19400
19350
19300
19250
19200
19150
0
20
40
60
80
100


Raw signal RMS vs 12*FE+Chip
0
10
20
30
40
50
60
70
80
90
0
20
40
60
80
100


Signal vs 12*FE+Chip
19450
19400
19350
19300
19250
19200
19150
0
20
40
60
80
100



Signal RMS vs 12*FE+Chip
90
80
70
60
50
40
30
20
10
0
0
20
40
60
80
100