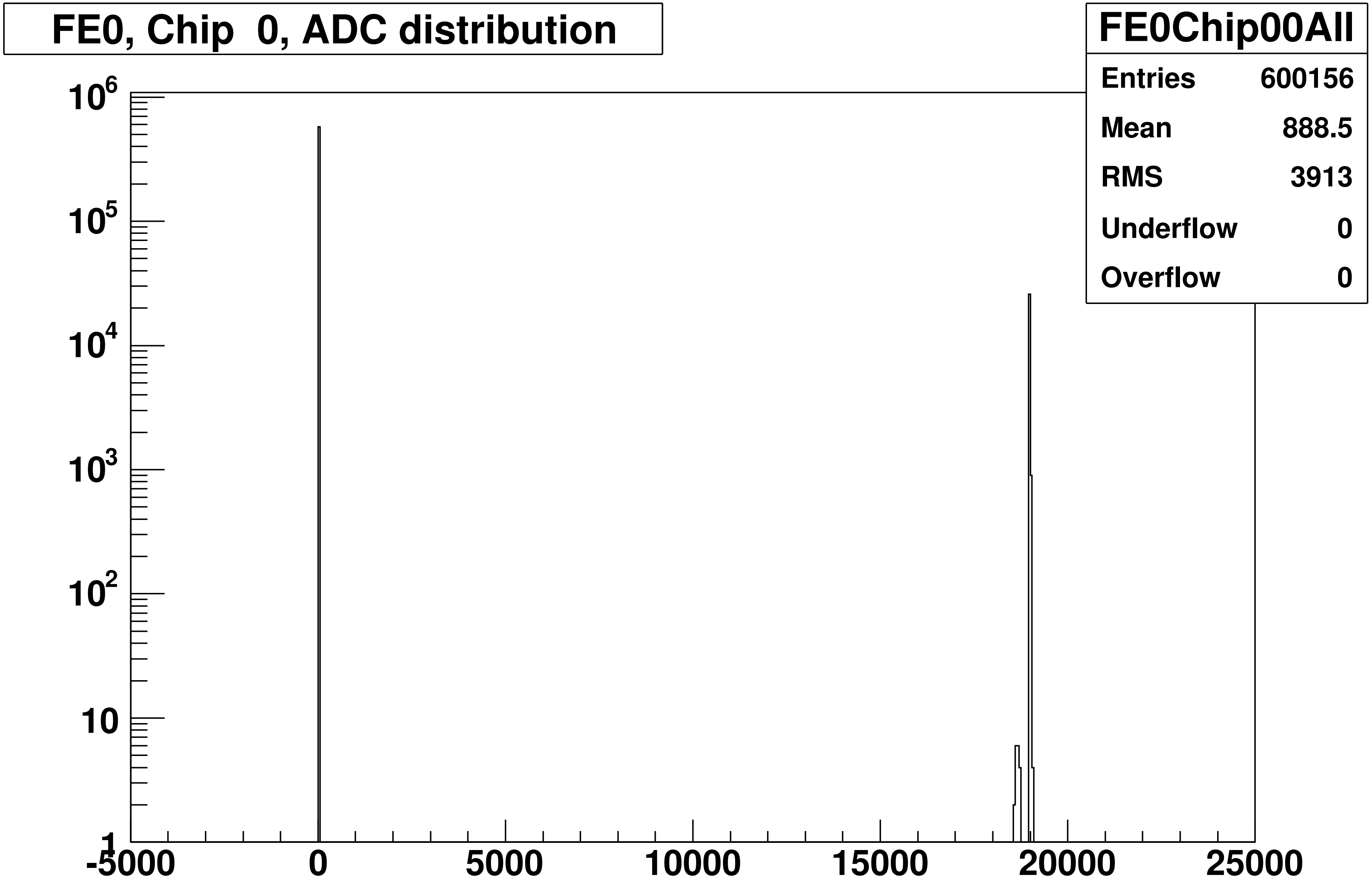
FE0, Chip 0, ADC distribution
FE0Chip00All
Entries 600156
Mean 888.5
RMS 3913
Underflow 0
Overflow 0
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10^4
10^3
10^2
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0
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20000
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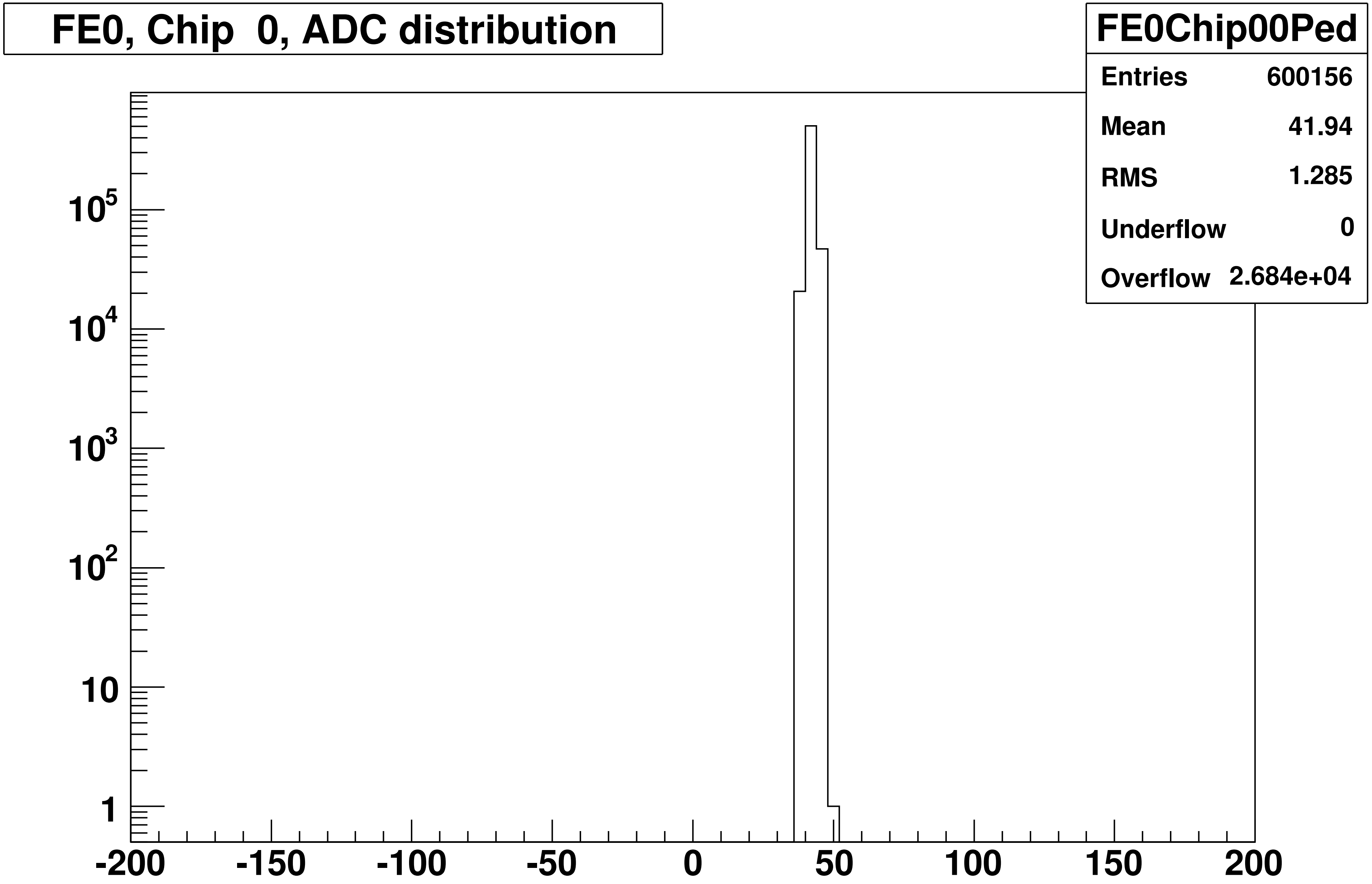

FE0, Chip 0, ADC distribution
FE0Chip00Ped
Entries 600156
Mean 41.94
RMS 1.285
Underflow 0
Overflow 2.684e+04
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10^3
10^2
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100
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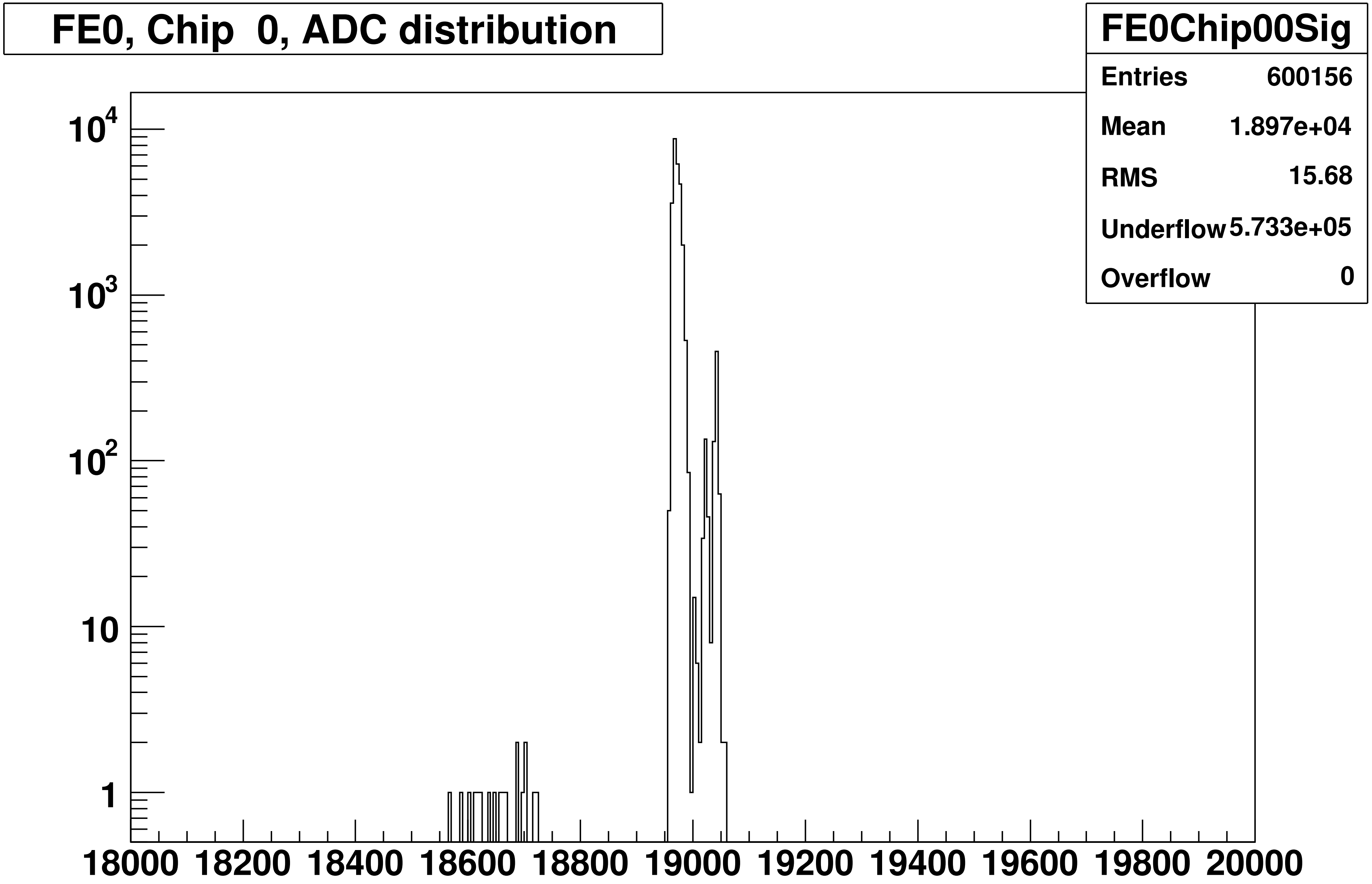
FE0, Chip 0, ADC distribution
FE0Chip00Sig
Entries 600156
Mean 1.897e+04
RMS 15.68
Underflow 5.733e+05
Overflow 0
10^4
10^3
10^2
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1
18000
18200
18400
18600
18800
19000
19200
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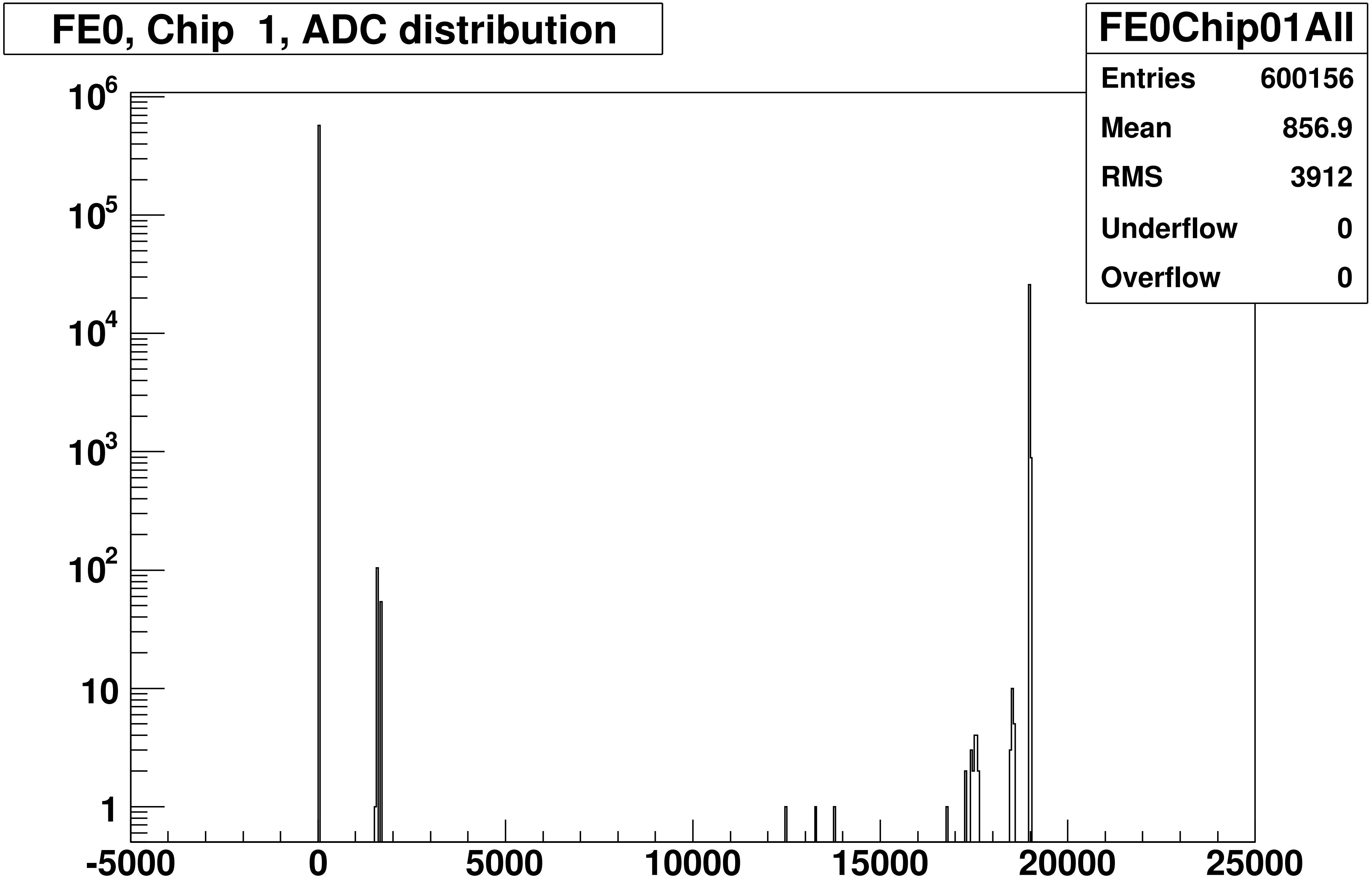
19600
19800
20000


FE0, Chip 1, ADC distribution
FE0Chip01All
Entries 600156
Mean 856.9
RMS 3912
Underflow 0
Overflow 0
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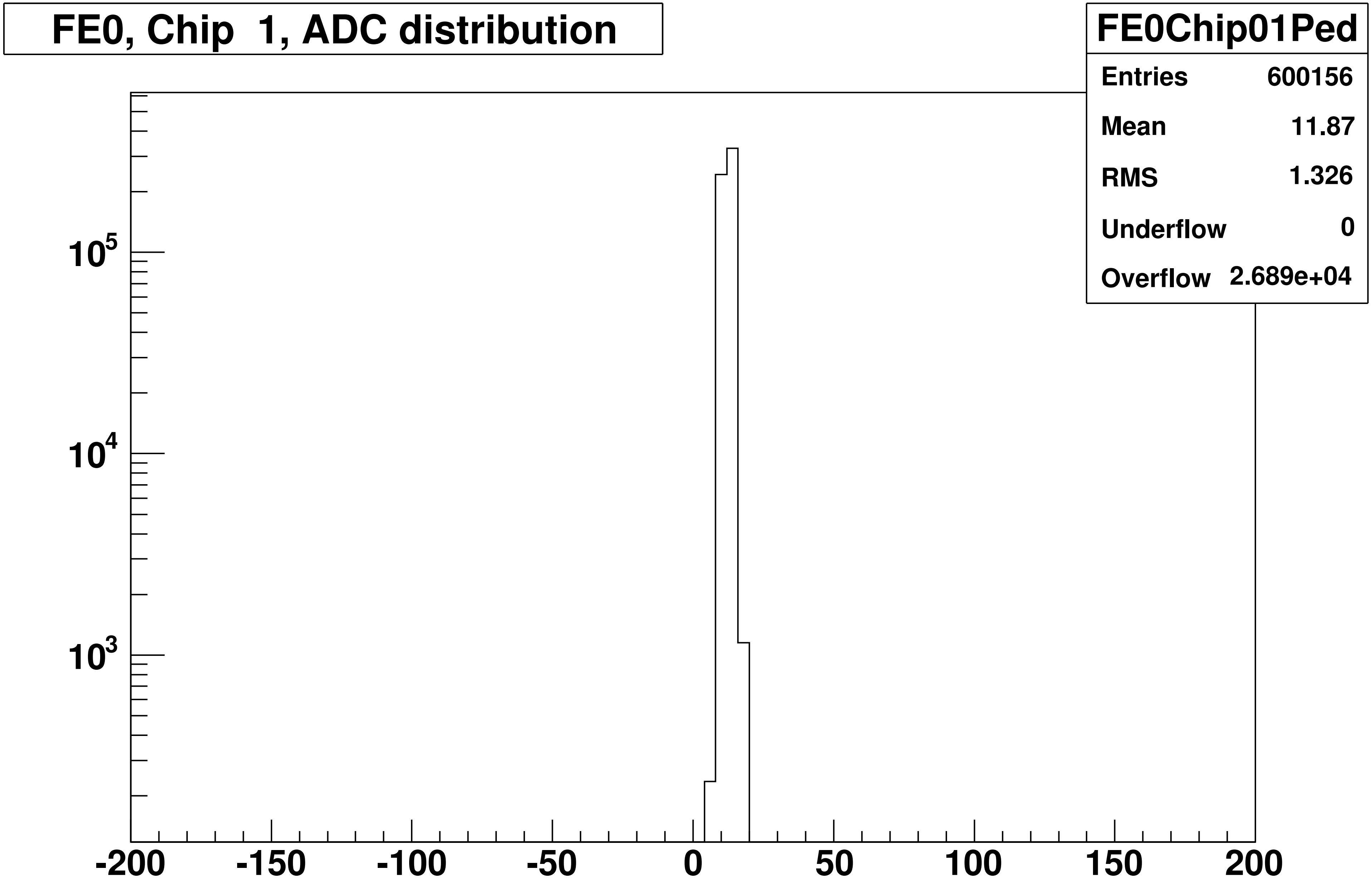
FE0, Chip 1, ADC distribution
FE0Chip01Ped
Entries 600156
Mean 11.87
RMS 1.326
Underflow 0
Overflow 2.689e+04
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10^4
10^3
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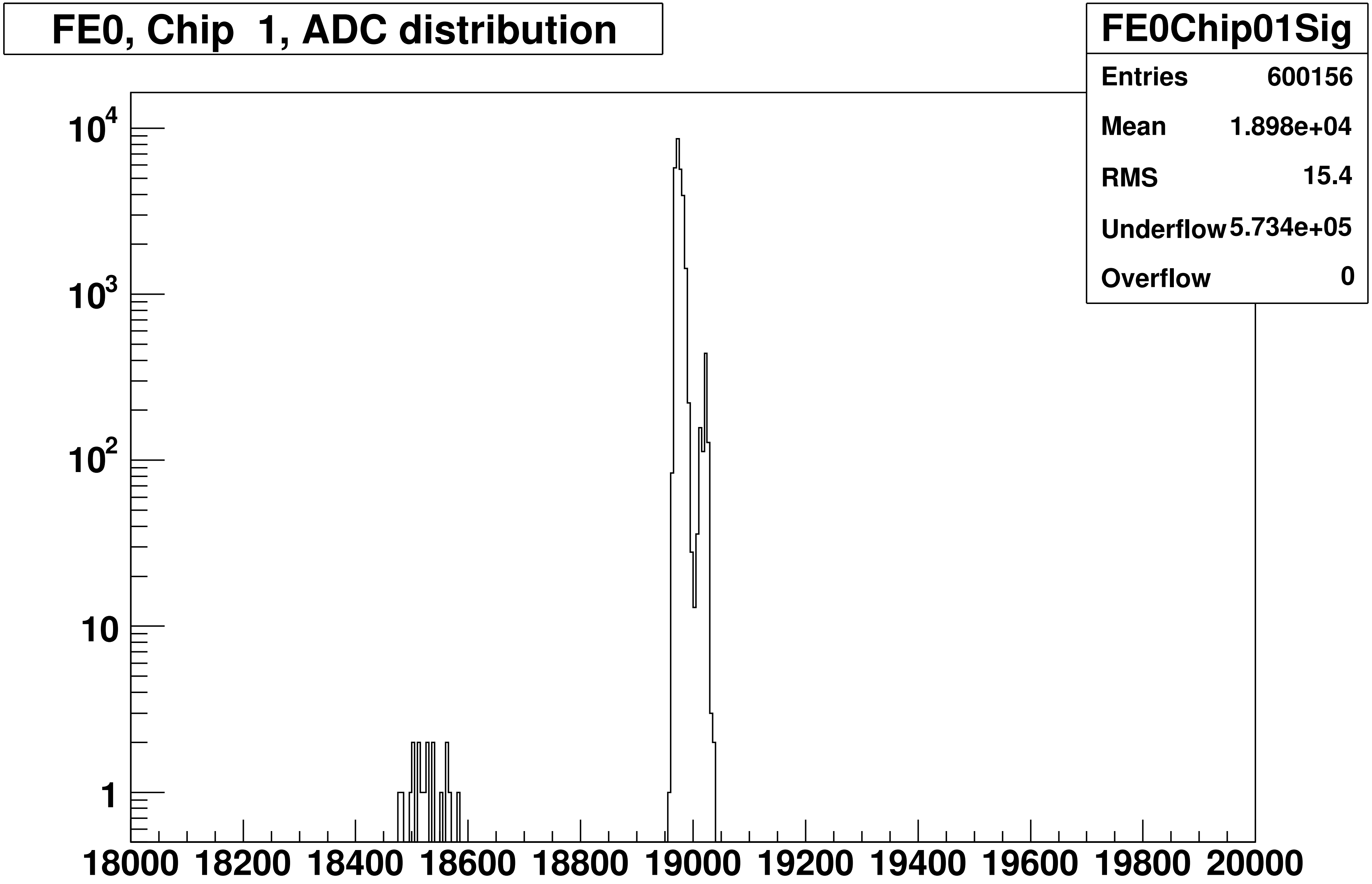

FE0, Chip 1, ADC distribution
FE0Chip01Sig
Entries 600156
Mean 1.898e+04
RMS 15.4
Underflow 5.734e+05
Overflow 0
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10^3
10^2
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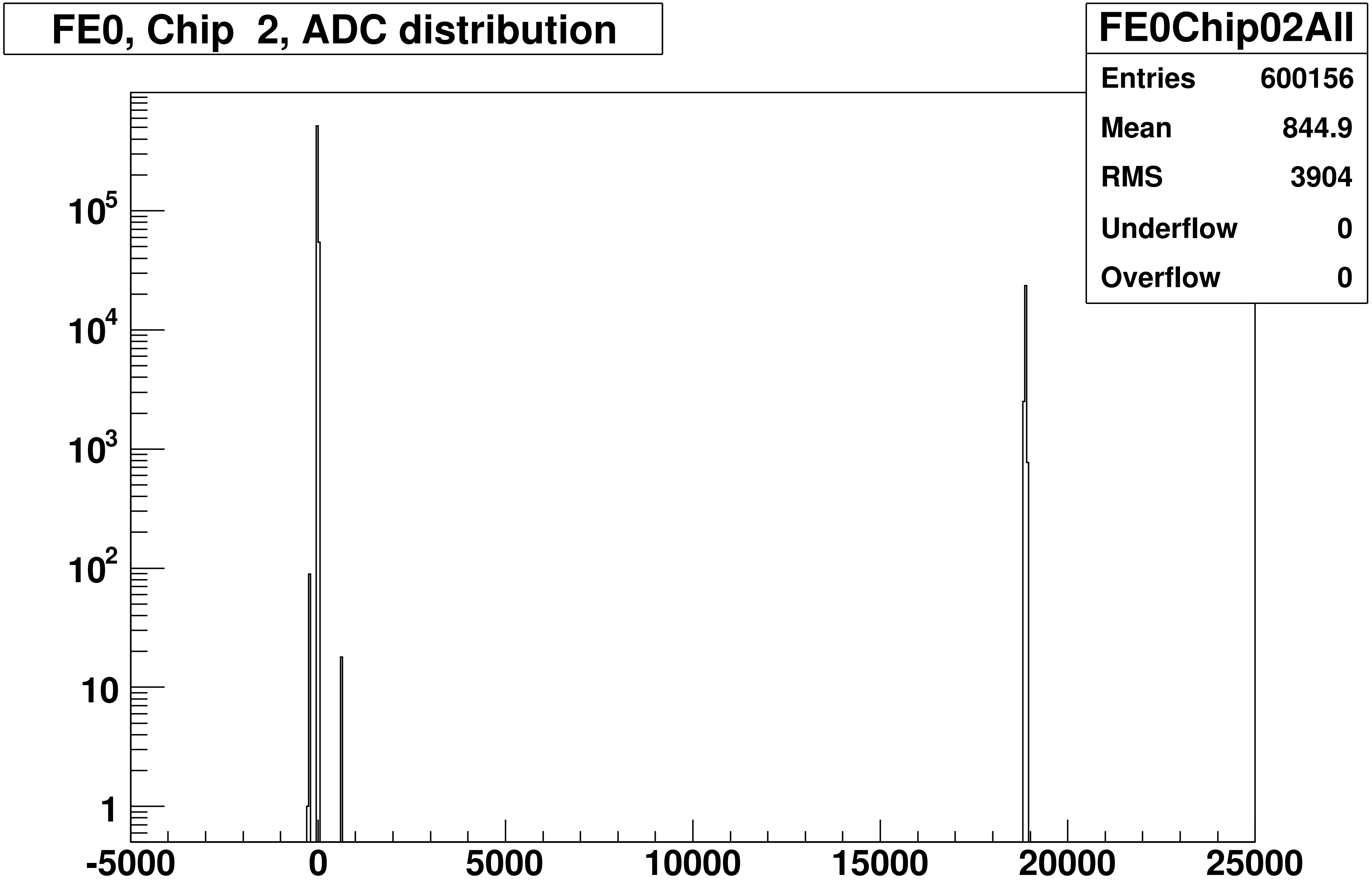
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE0, Chip 2, ADC distribution
FE0Chip02All
Entries 600156
Mean 844.9
RMS 3904
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
1
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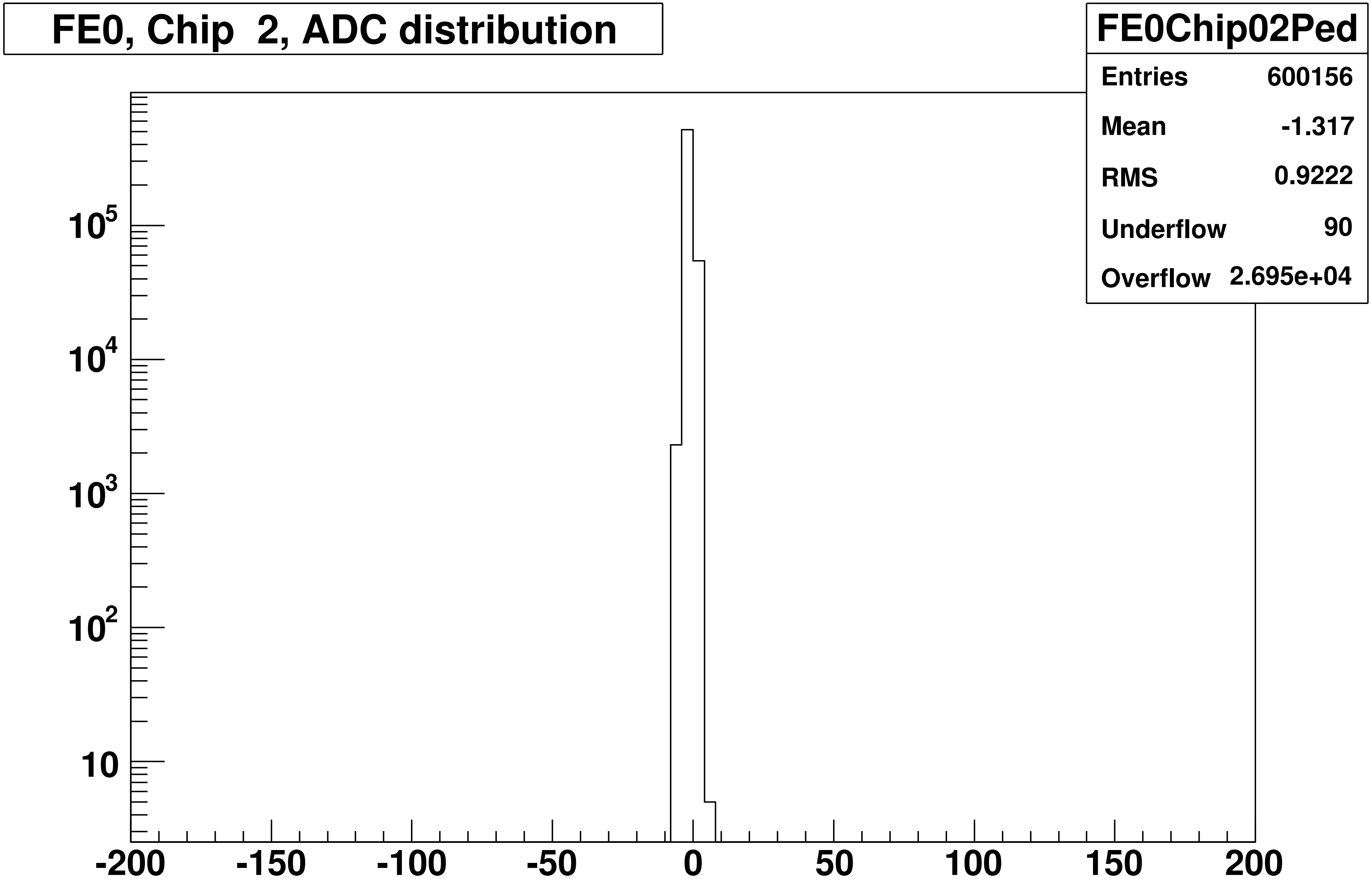
FE0, Chip 2, ADC distribution
FE0Chip02Ped
Entries 600156
Mean -1.317
RMS 0.9222
Underflow 90
Overflow 2.695e+04
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10^4
10^3
10^2
10
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150
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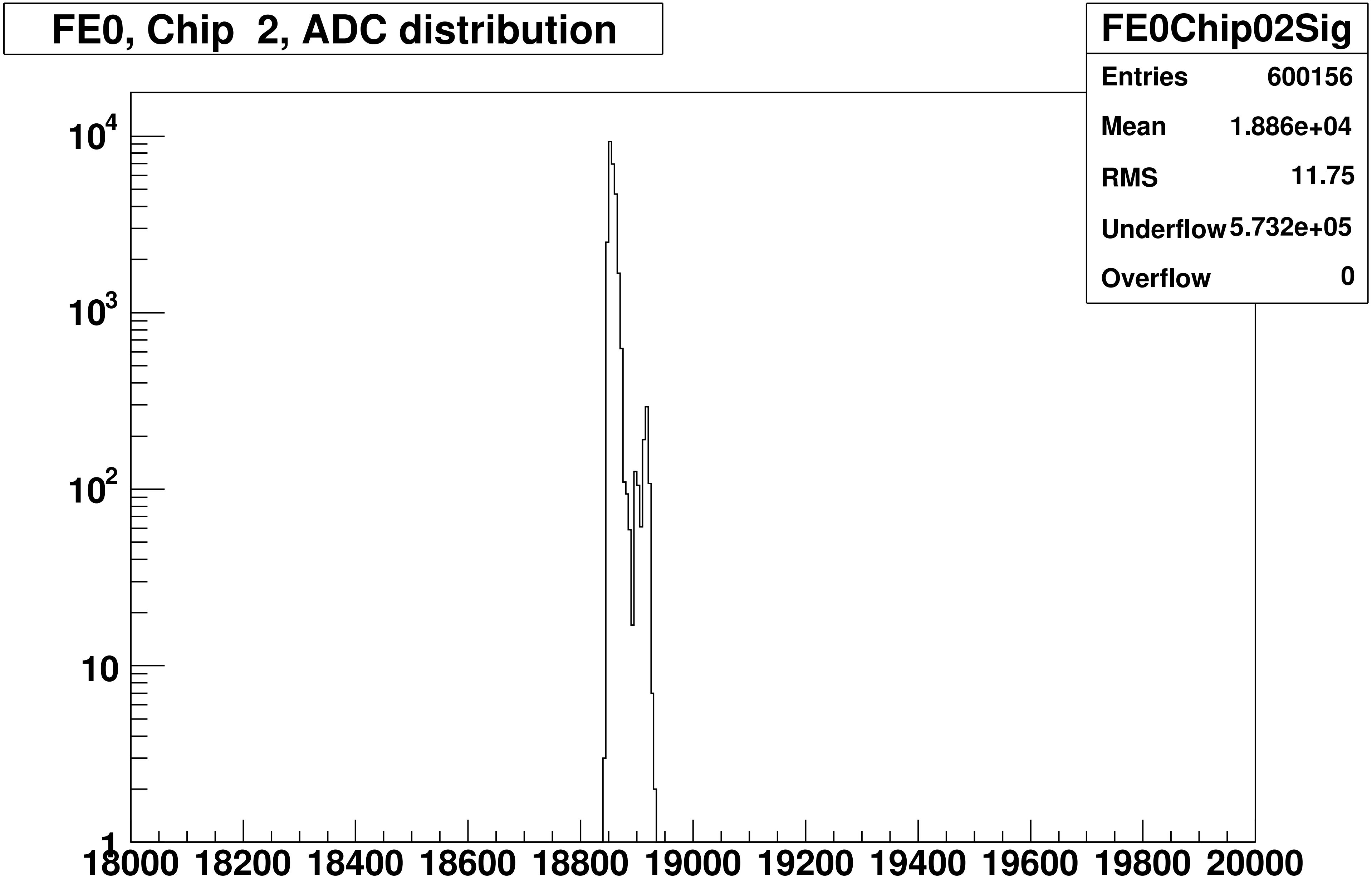
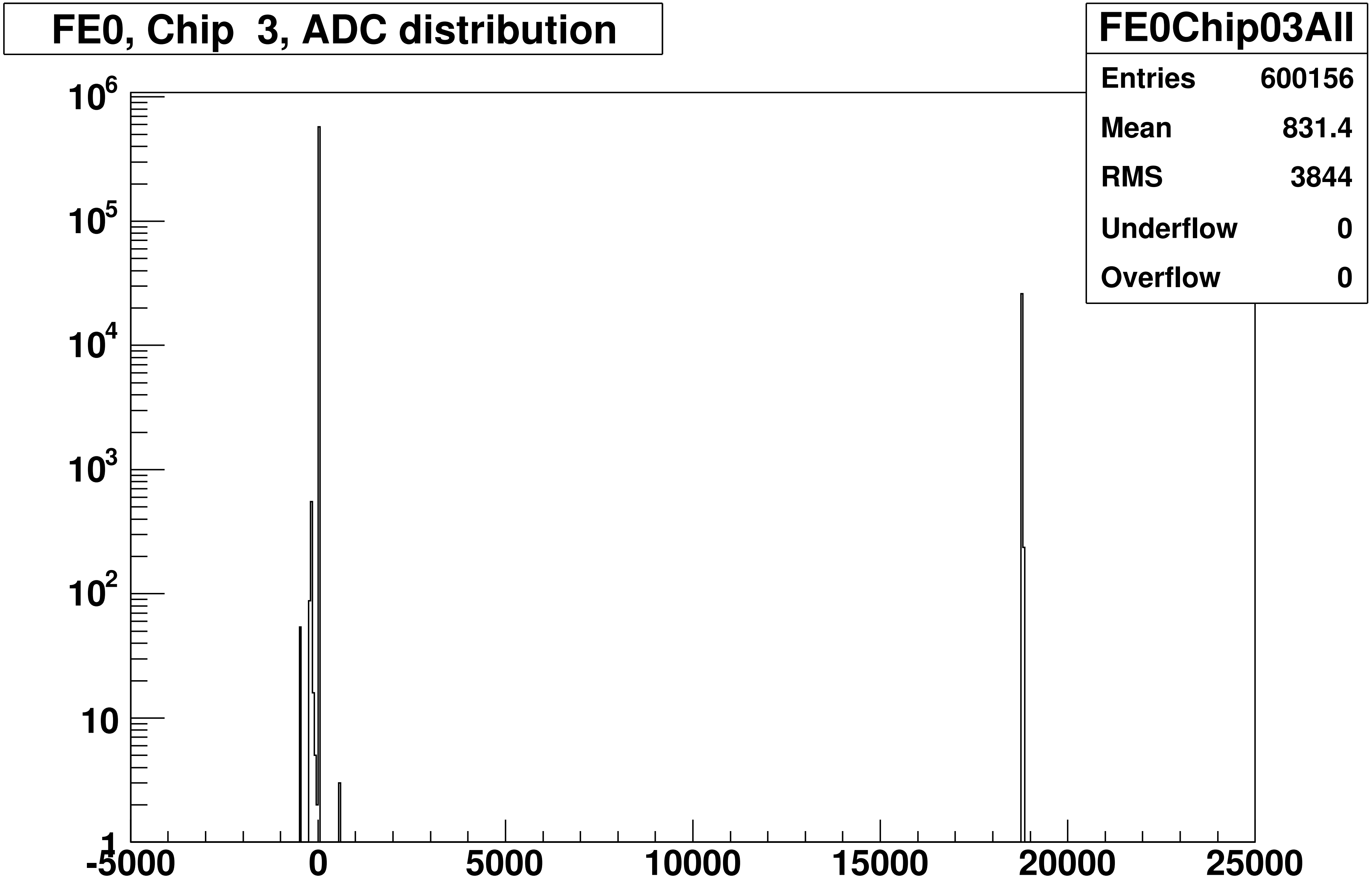


FE0, Chip 2, ADC distribution
FE0Chip02Sig
Entries 600156
Mean 1.886e+04
RMS 11.75
Underflow 5.732e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE0, Chip 3, ADC distribution
FE0Chip03All
Entries 600156
Mean 831.4
RMS 3844
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
1
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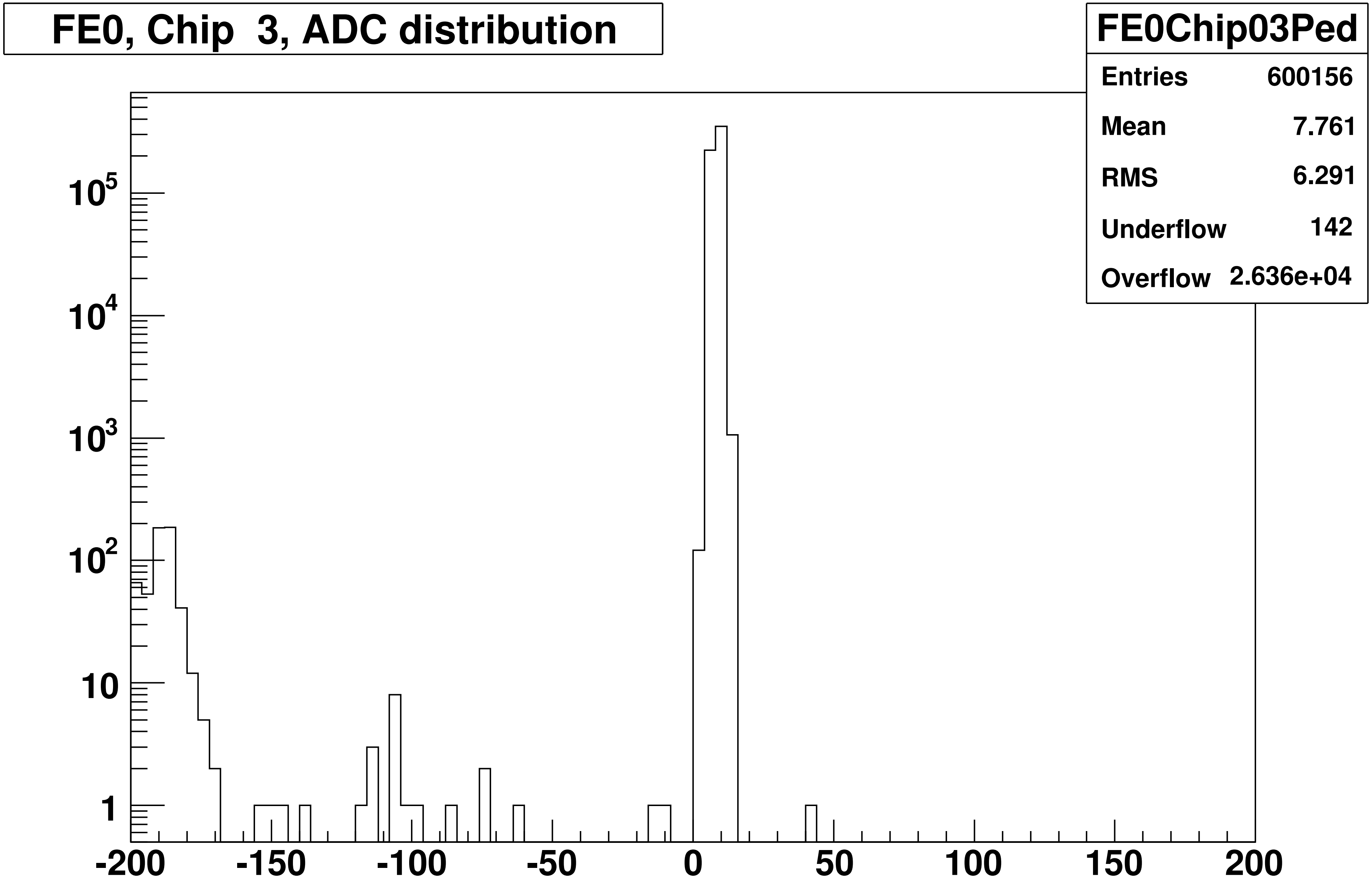
5000
10000
15000
20000
25000



FE0, Chip 3, ADC distribution
FE0Chip03Ped
Entries 600156
Mean 7.761
RMS 6.291
Underflow 142
Overflow 2.636e+04
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10^4
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10^2
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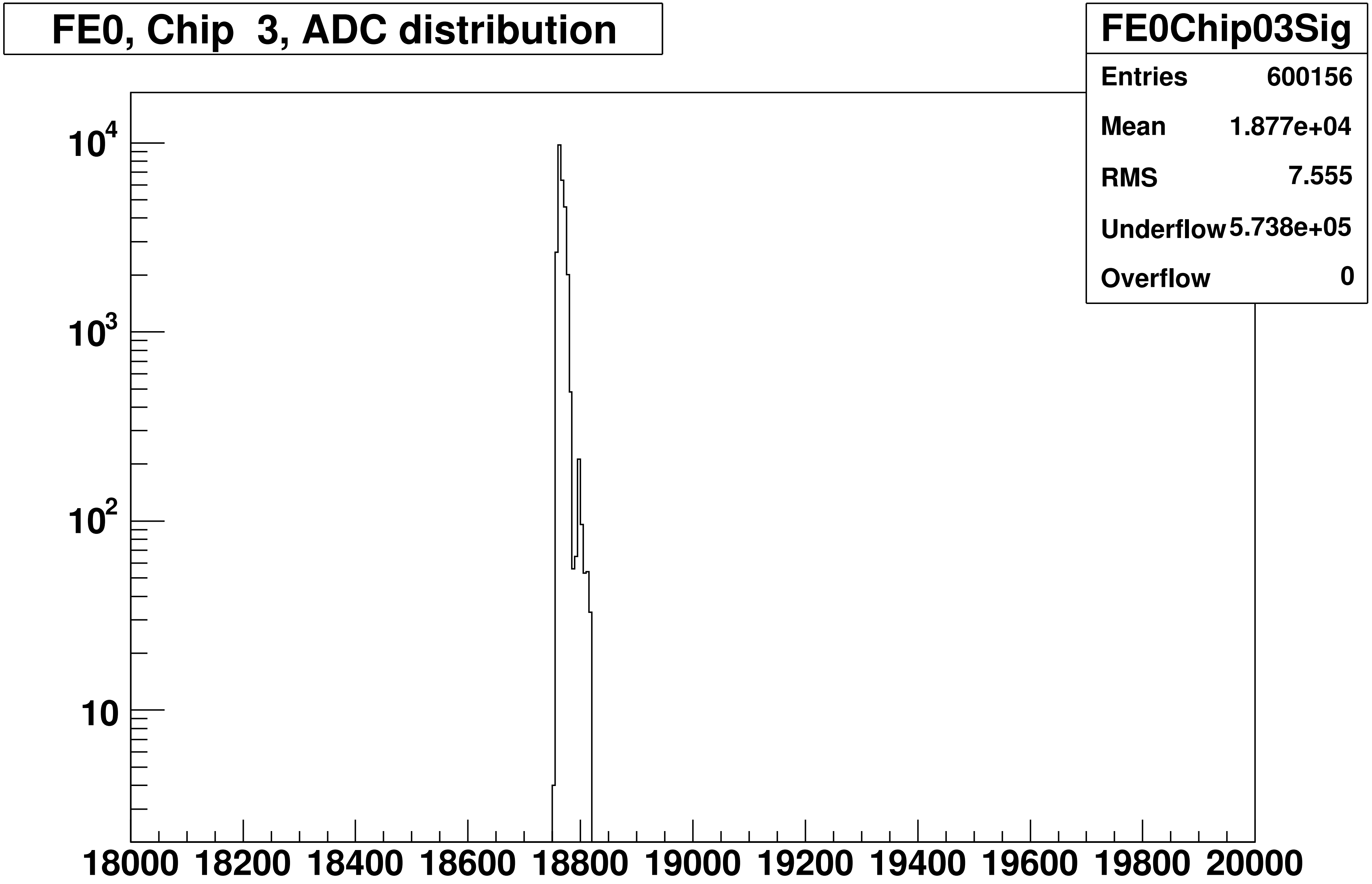
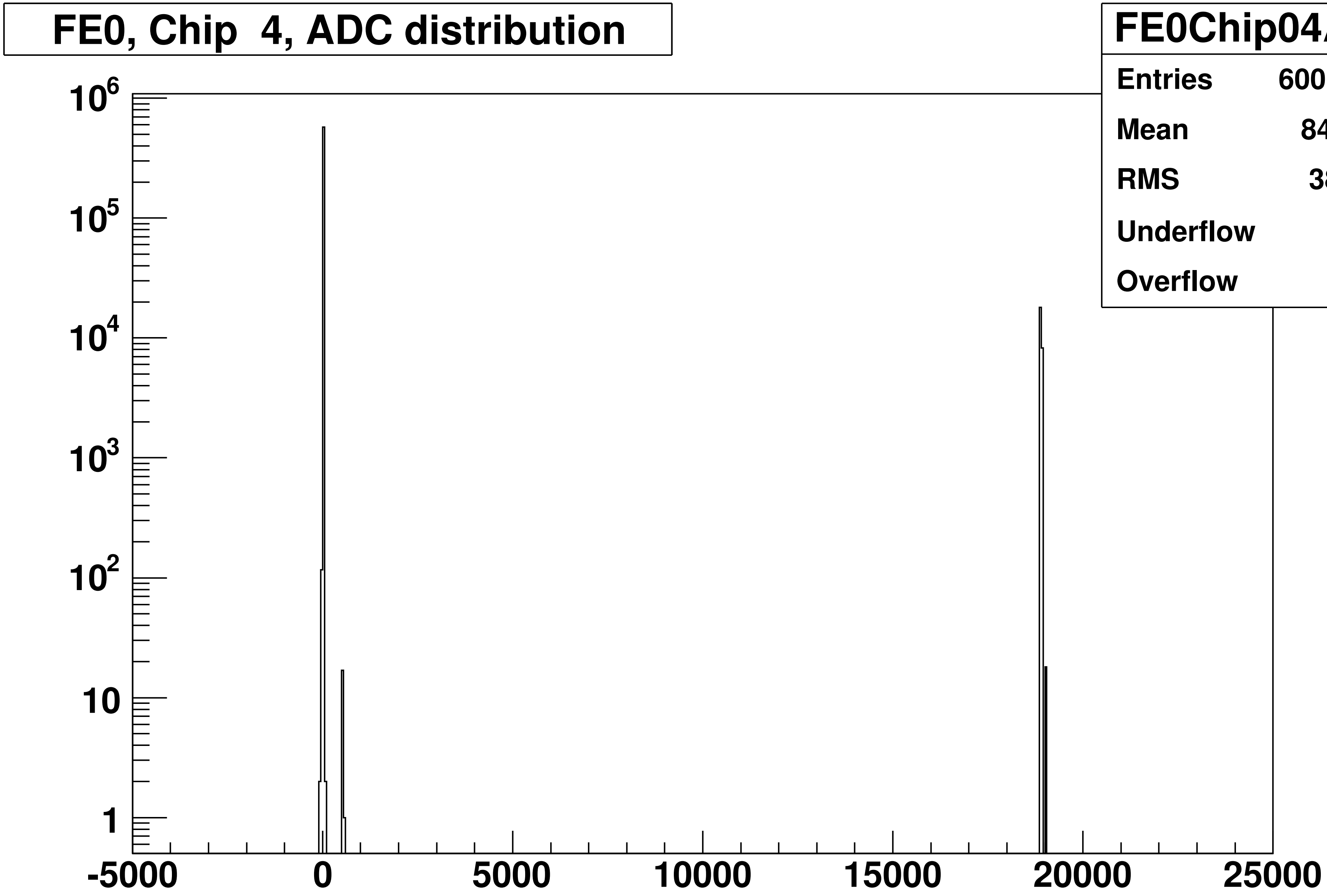
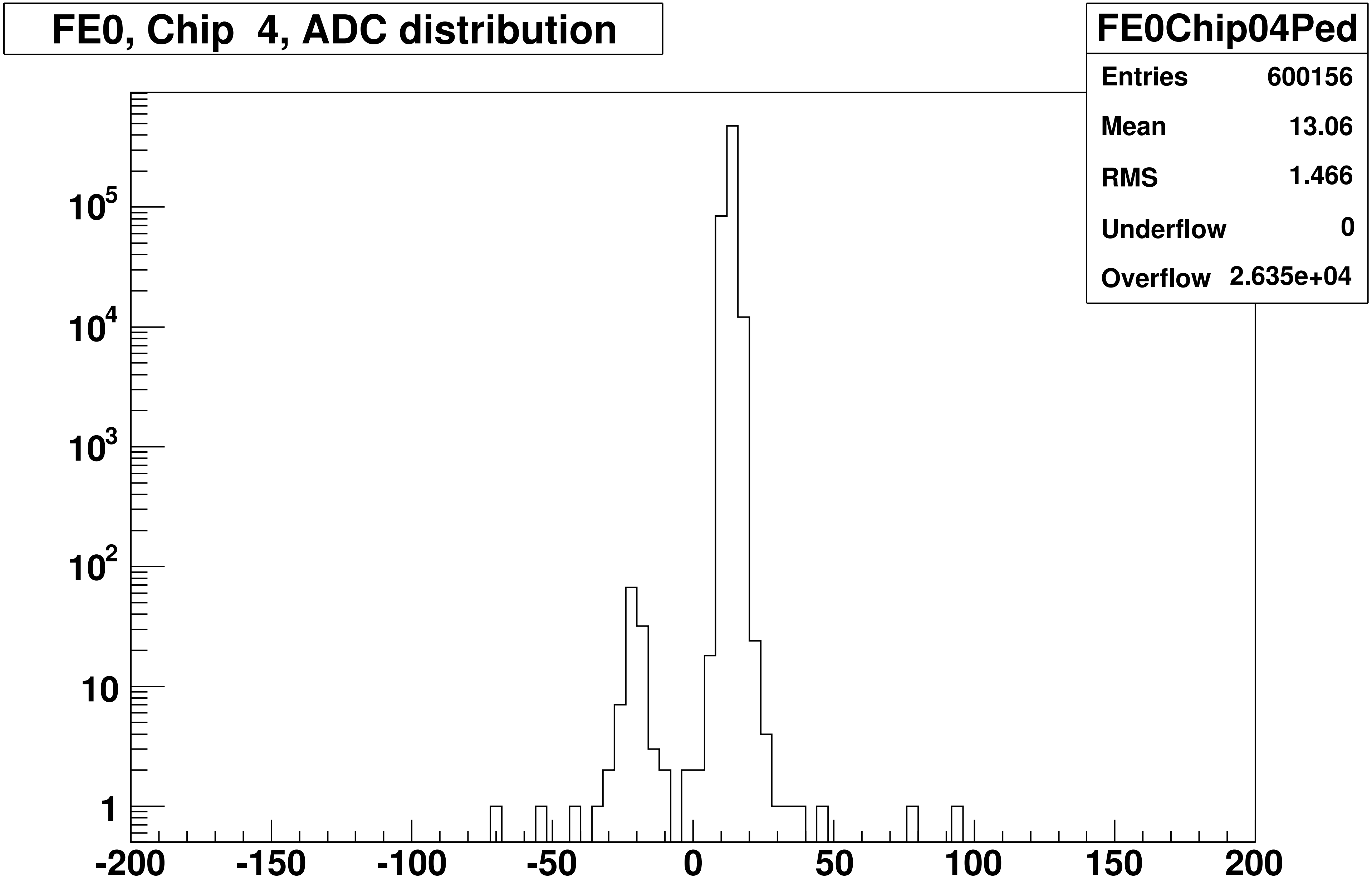
0
50
100
150
200



FE0, Chip 3, ADC distribution
FE0Chip03Sig
Entries 600156
Mean 1.877e+04
RMS 7.555
Underflow 5.738e+05
Overflow 0
10^4
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE0, Chip 4, ADC distribution
FE0Chip04All
Entries 600156
Mean 841.7
RMS 3868
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE0, Chip 4, ADC distribution
FE0Chip04Ped
Entries 600156
Mean 13.06
RMS 1.466
Underflow 0
Overflow 2.635e+04
10^5
10^4
10^3
10^2
10
1
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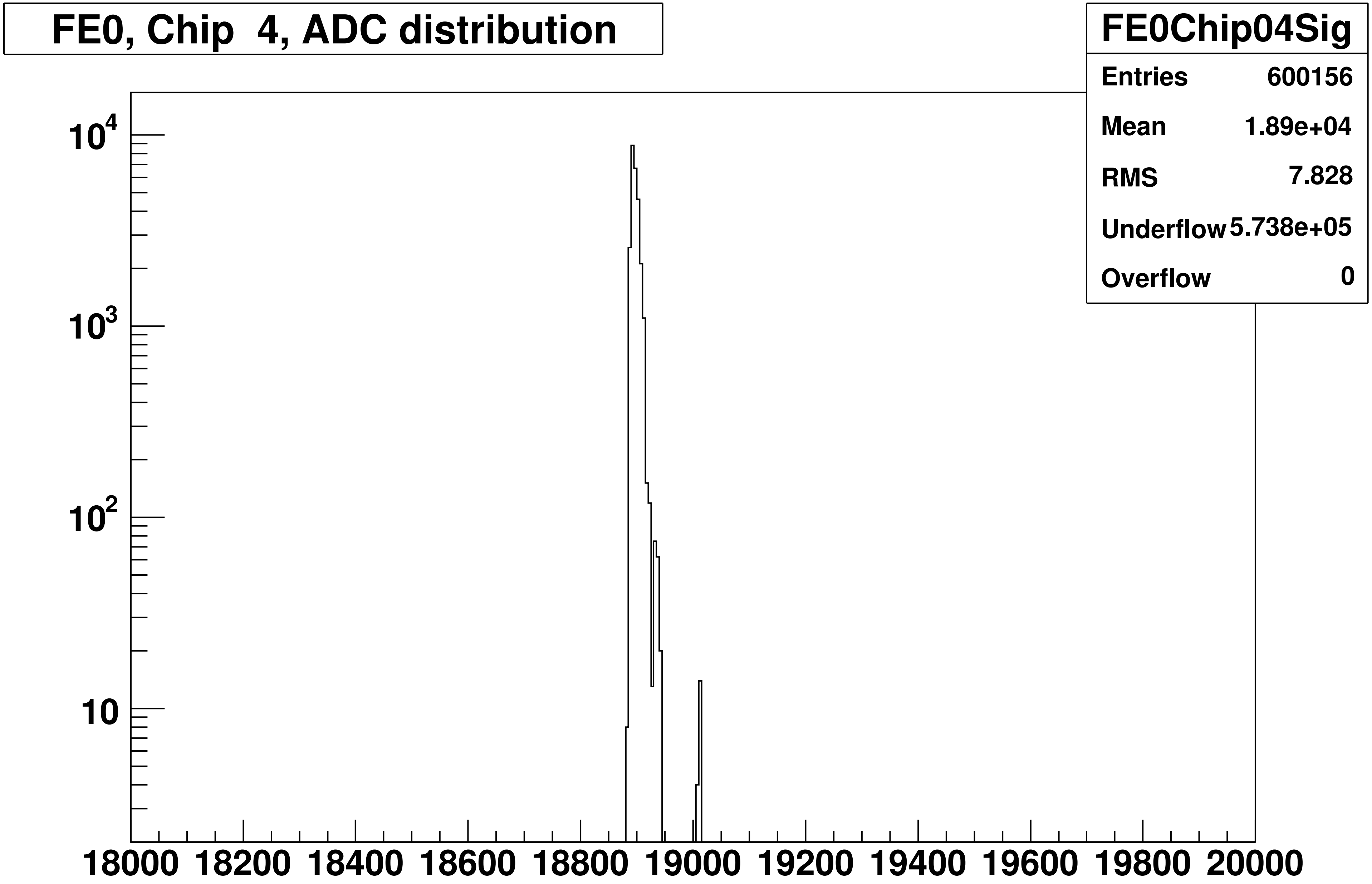
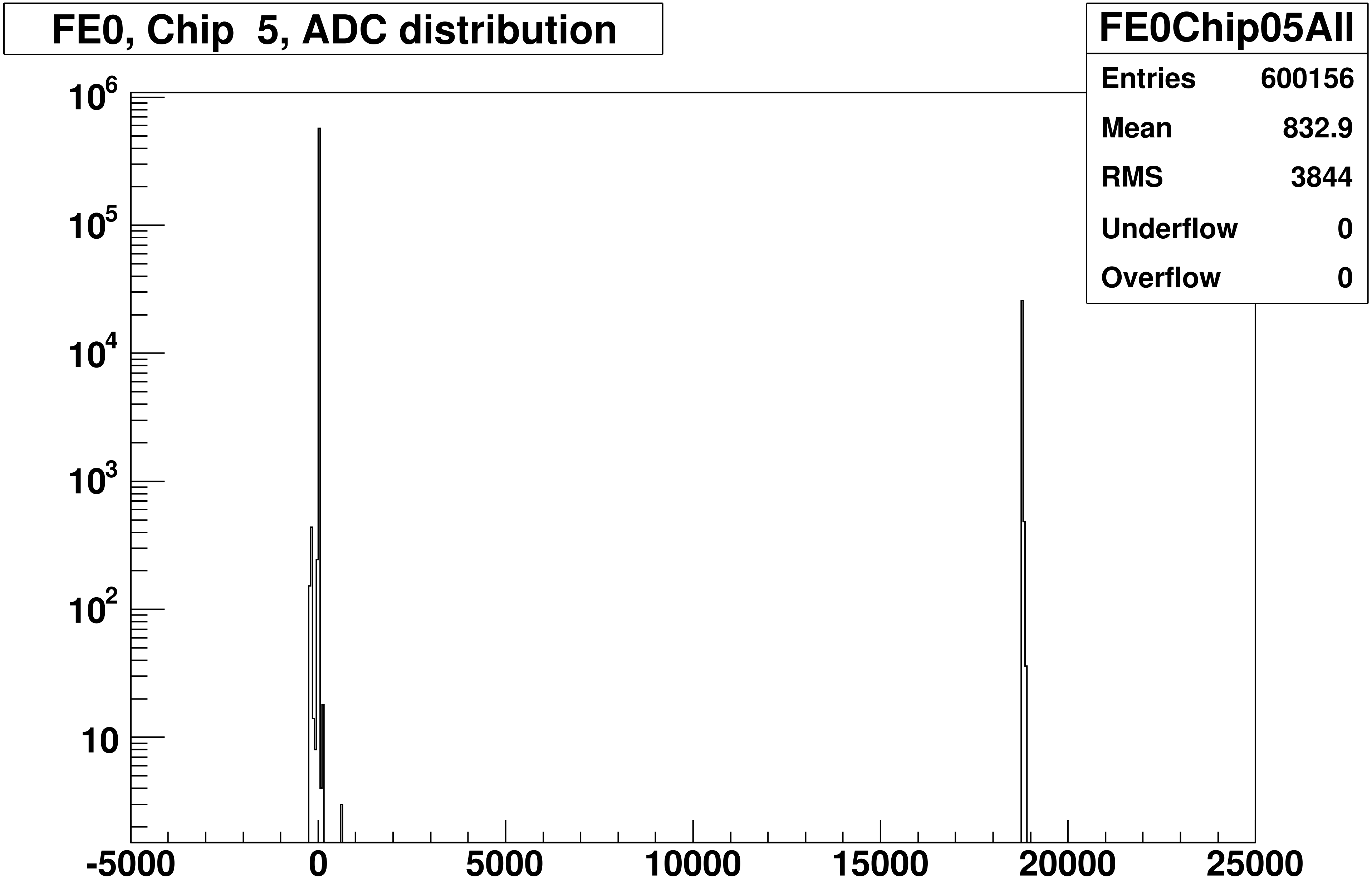
50
100
150
200



FE0, Chip 4, ADC distribution
FE0Chip04Sig
Entries 600156
Mean 1.89e+04
RMS 7.828
Underflow 5.738e+05
Overflow 0
10^4
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE0, Chip 5, ADC distribution
FE0Chip05All
Entries 600156
Mean 832.9
RMS 3844
Underflow 0
Overflow 0
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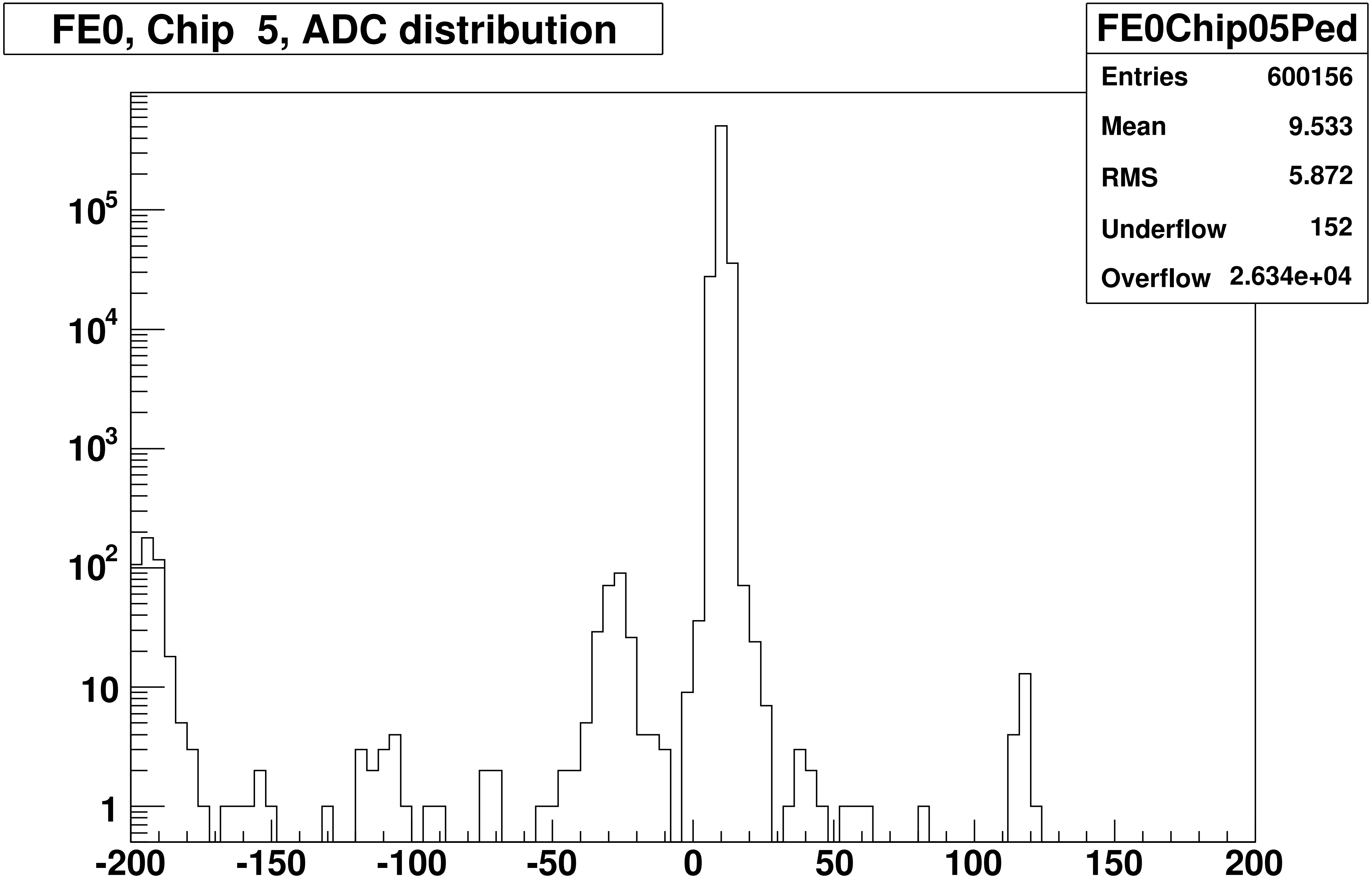
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000



FE0, Chip 5, ADC distribution
FE0Chip05Ped
Entries 600156
Mean 9.533
RMS 5.872
Underflow 152
Overflow 2.634e+04
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10^4
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10^2
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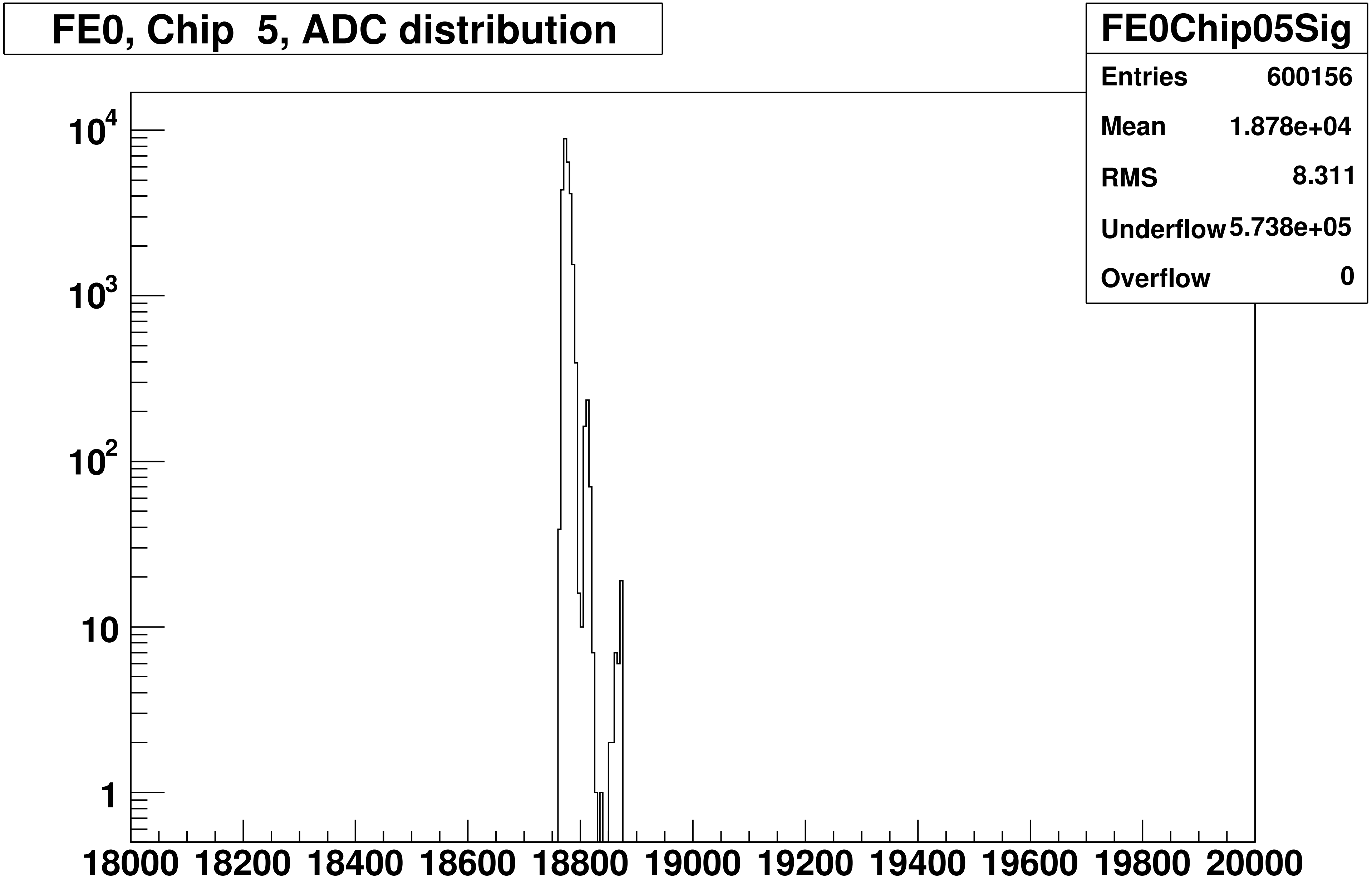
0
50
100
150
200


FE0, Chip 5, ADC distribution
FE0Chip05Sig
Entries 600156
Mean 1.878e+04
RMS 8.311
Underflow 5.738e+05
Overflow 0
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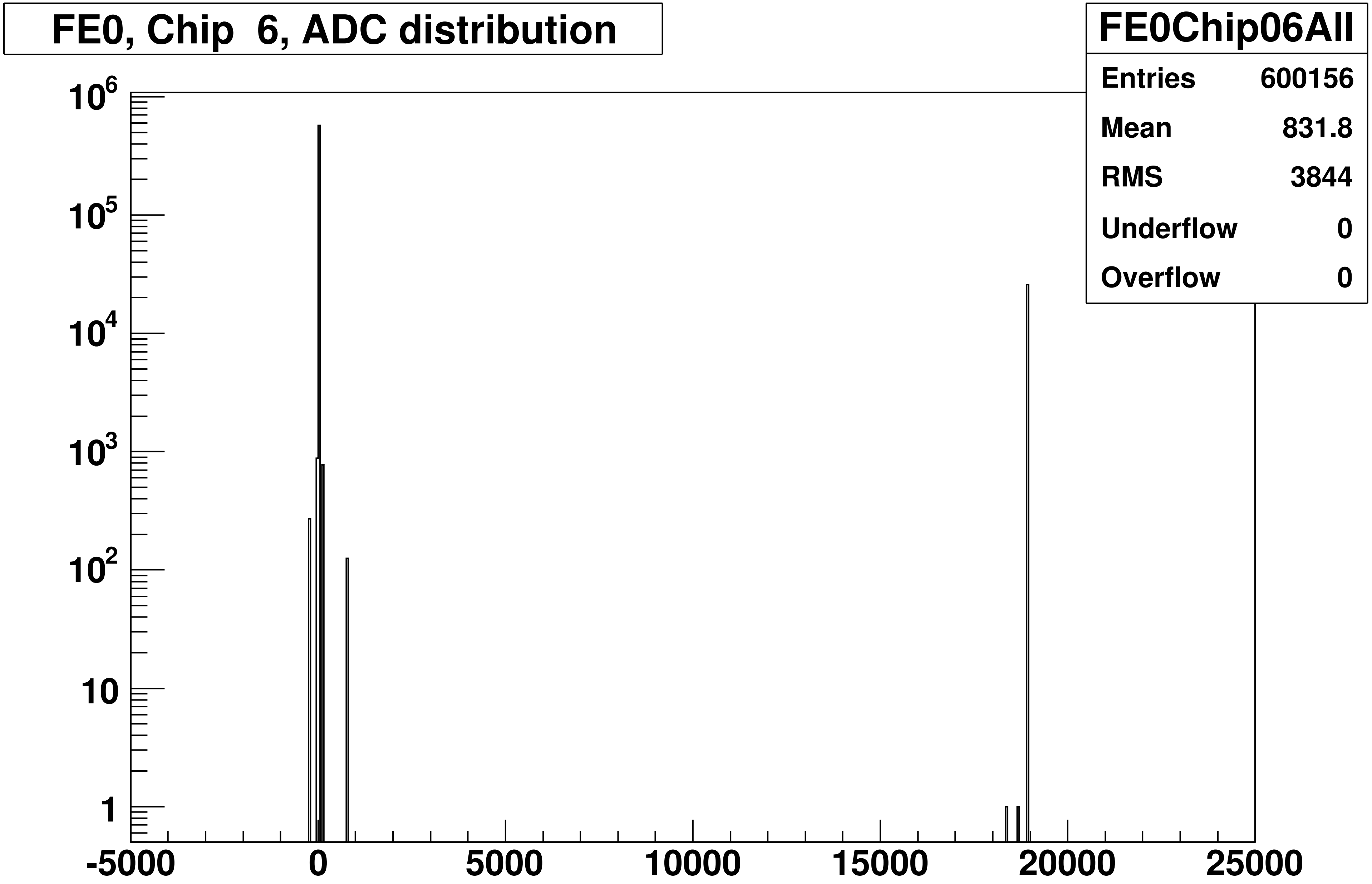
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE0, Chip 6, ADC distribution
FE0Chip06All
Entries 600156
Mean 831.8
RMS 3844
Underflow 0
Overflow 0
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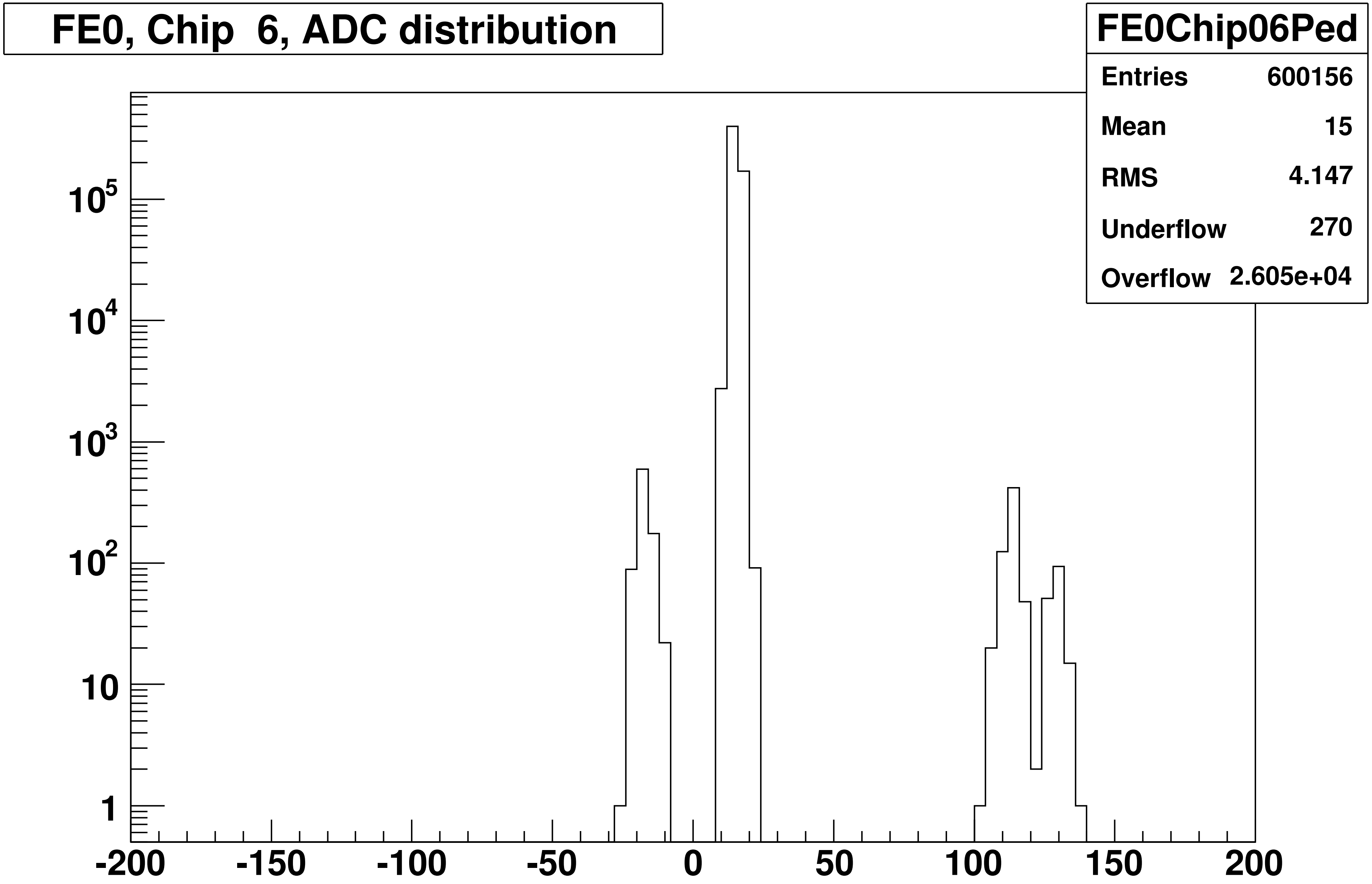
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE0, Chip 6, ADC distribution
FE0Chip06Ped
Entries 600156
Mean 15
RMS 4.147
Underflow 270
Overflow 2.605e+04
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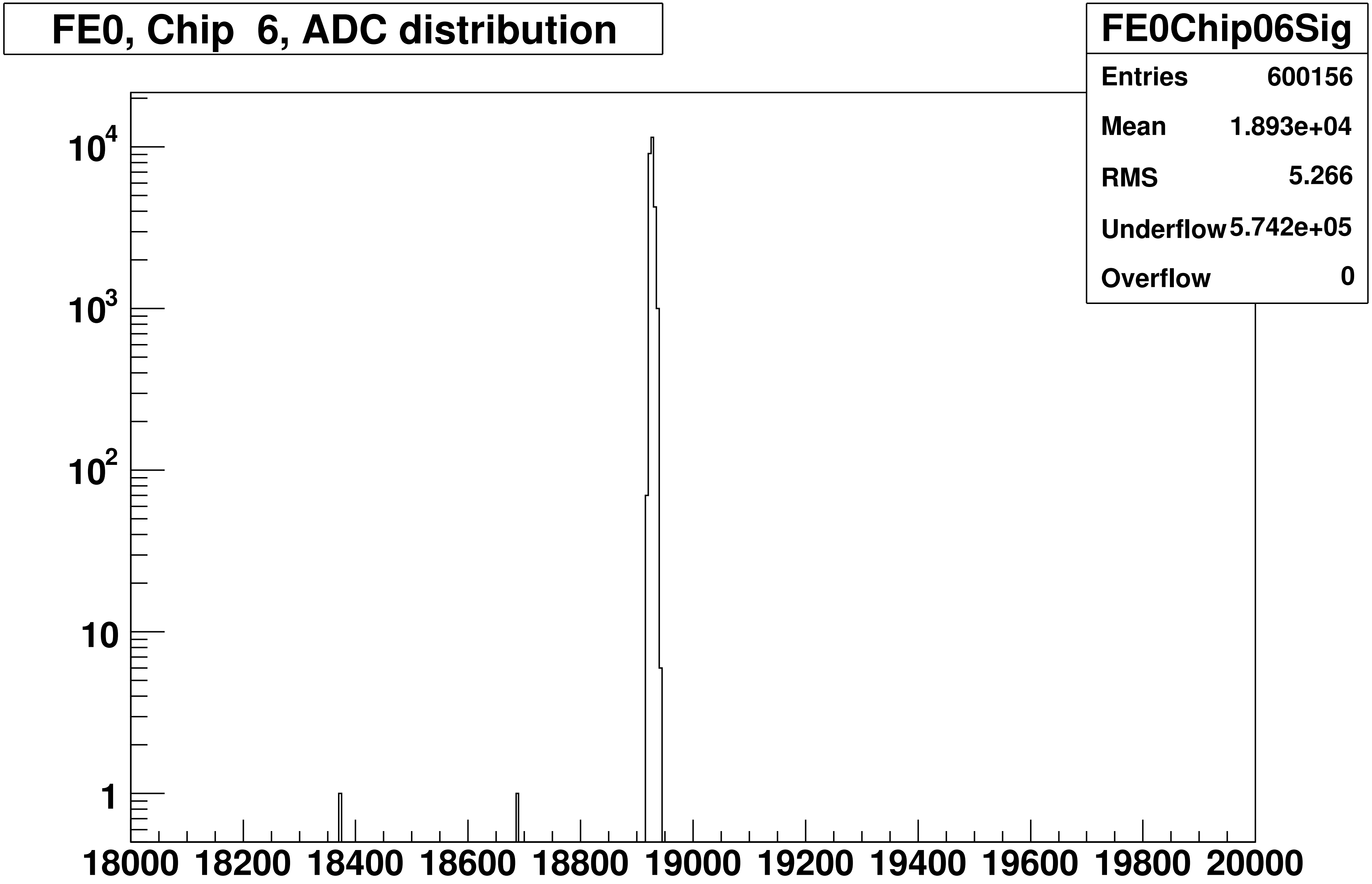
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
200


FE0, Chip 6, ADC distribution
FE0Chip06Sig
Entries 600156
Mean 1.893e+04
RMS 5.266
Underflow 5.742e+05
Overflow 0
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10^3
10^2
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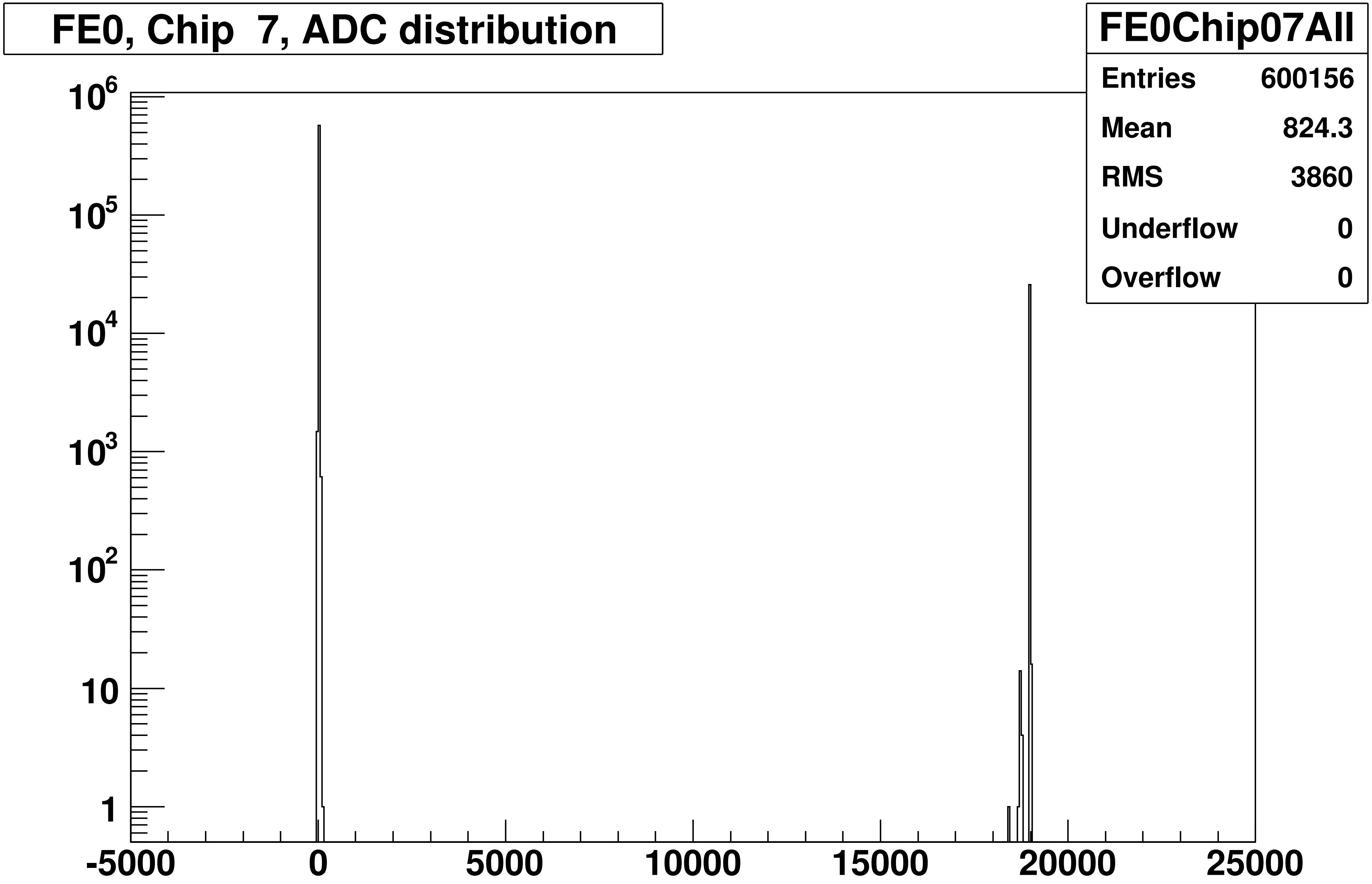
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE0, Chip 7, ADC distribution
FE0Chip07All
Entries 600156
Mean 824.3
RMS 3860
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
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0
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10000
15000
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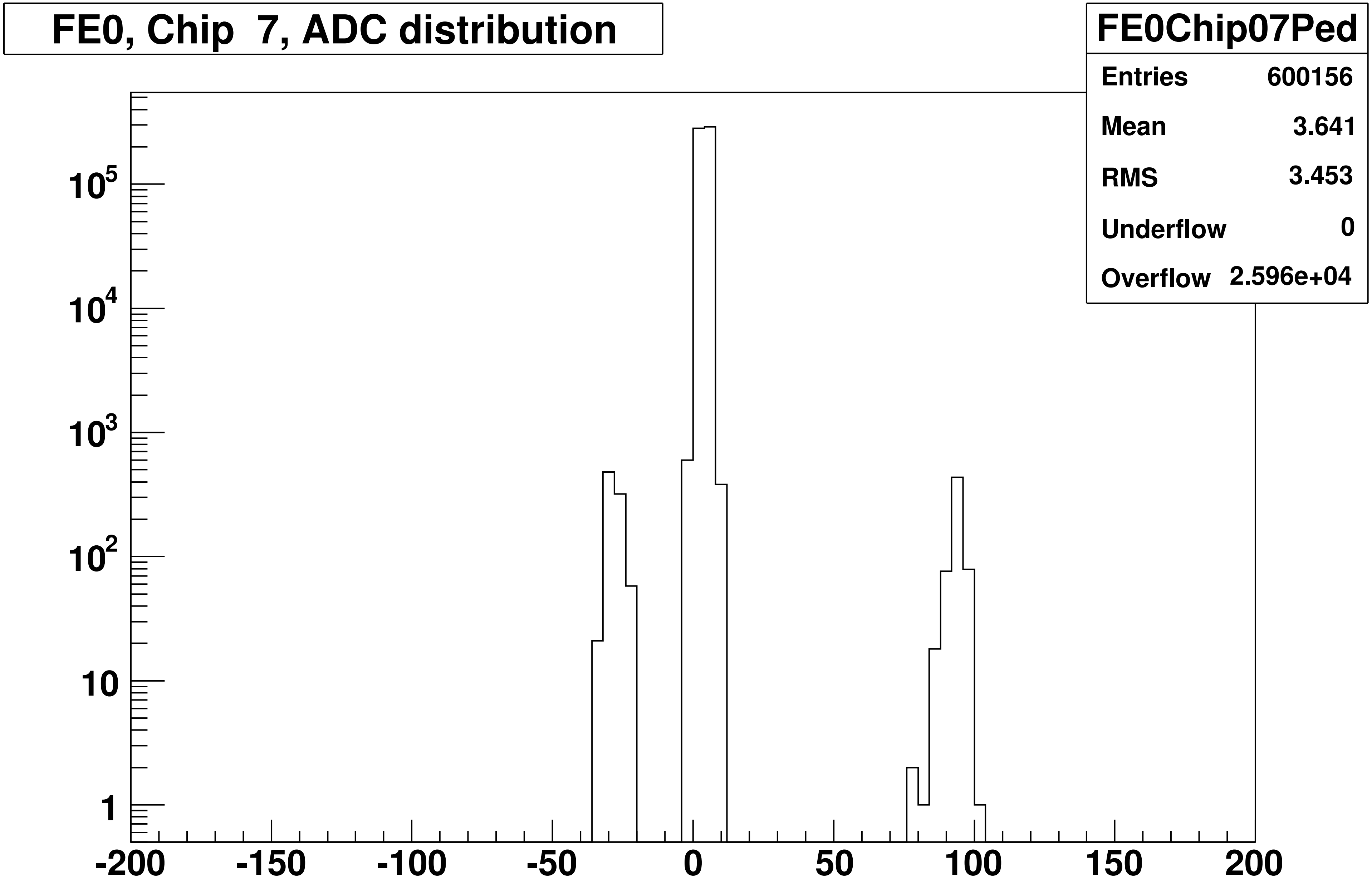
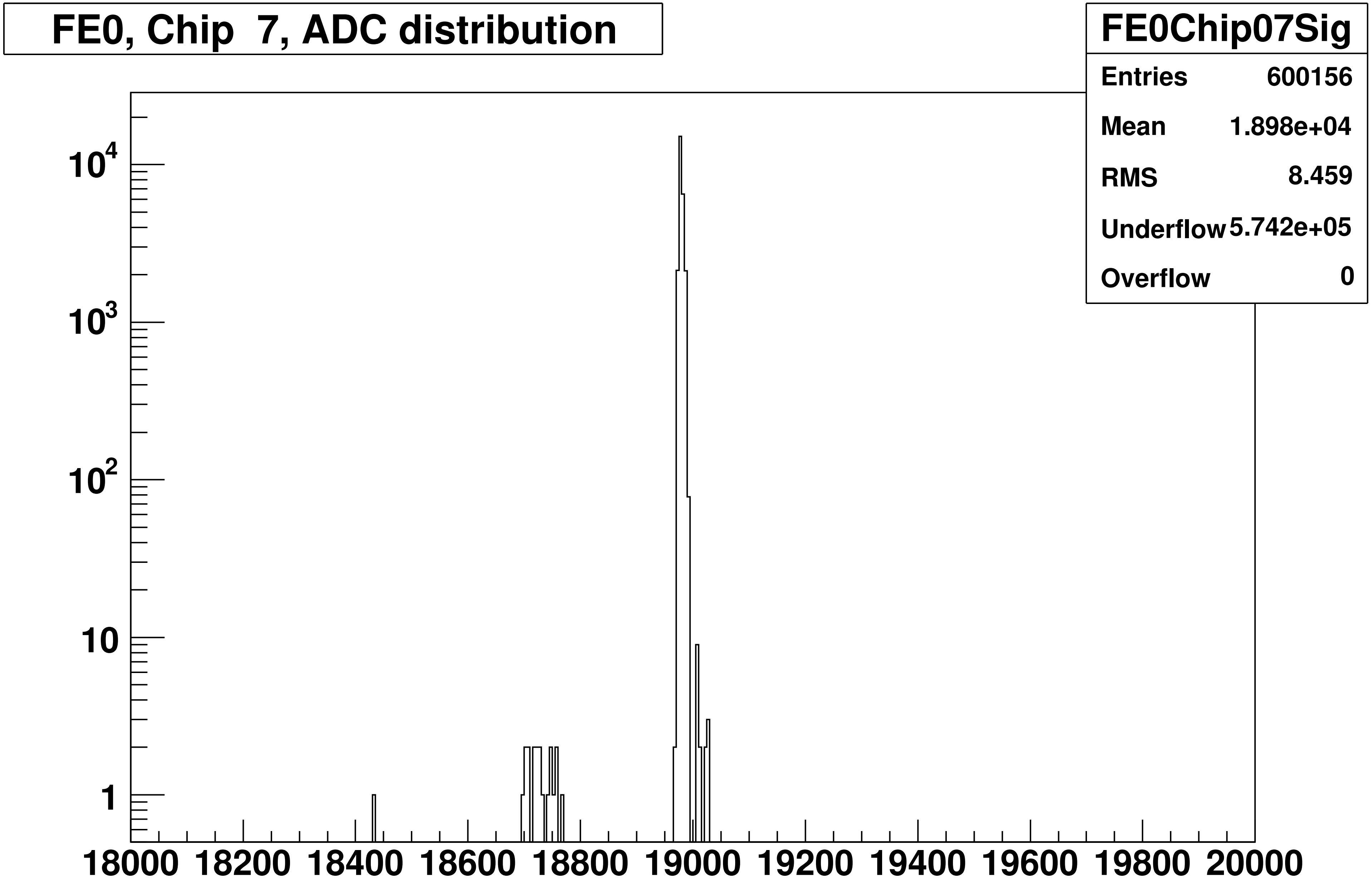
25000


FE0, Chip 7, ADC distribution
FE0Chip07Ped
Entries 600156
Mean 3.641
RMS 3.453
Underflow 0
Overflow 2.596e+04
10^5
10^4
10^3
10^2
10
1
-200 -150 -100 -50 0 50 100 150 200



FE0, Chip 7, ADC distribution
FE0Chip07Sig
Entries 600156
Mean 1.898e+04
RMS 8.459
Underflow 5.742e+05
Overflow 0
10^4
10^3
10^2
10
1
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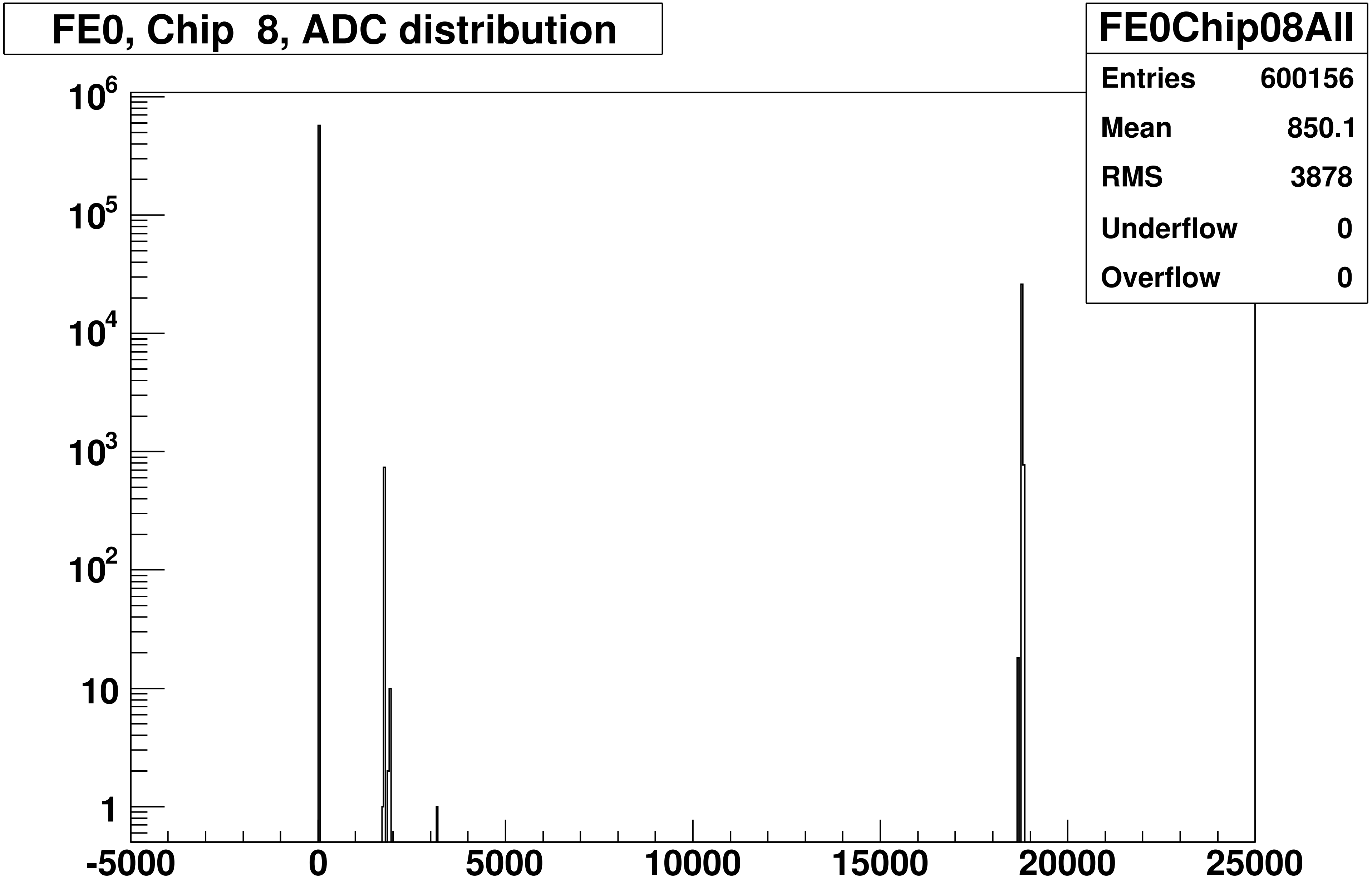

FE0, Chip 8, ADC distribution
FE0Chip08All
Entries 600156
Mean 850.1
RMS 3878
Underflow 0
Overflow 0
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10^4
10^3
10^2
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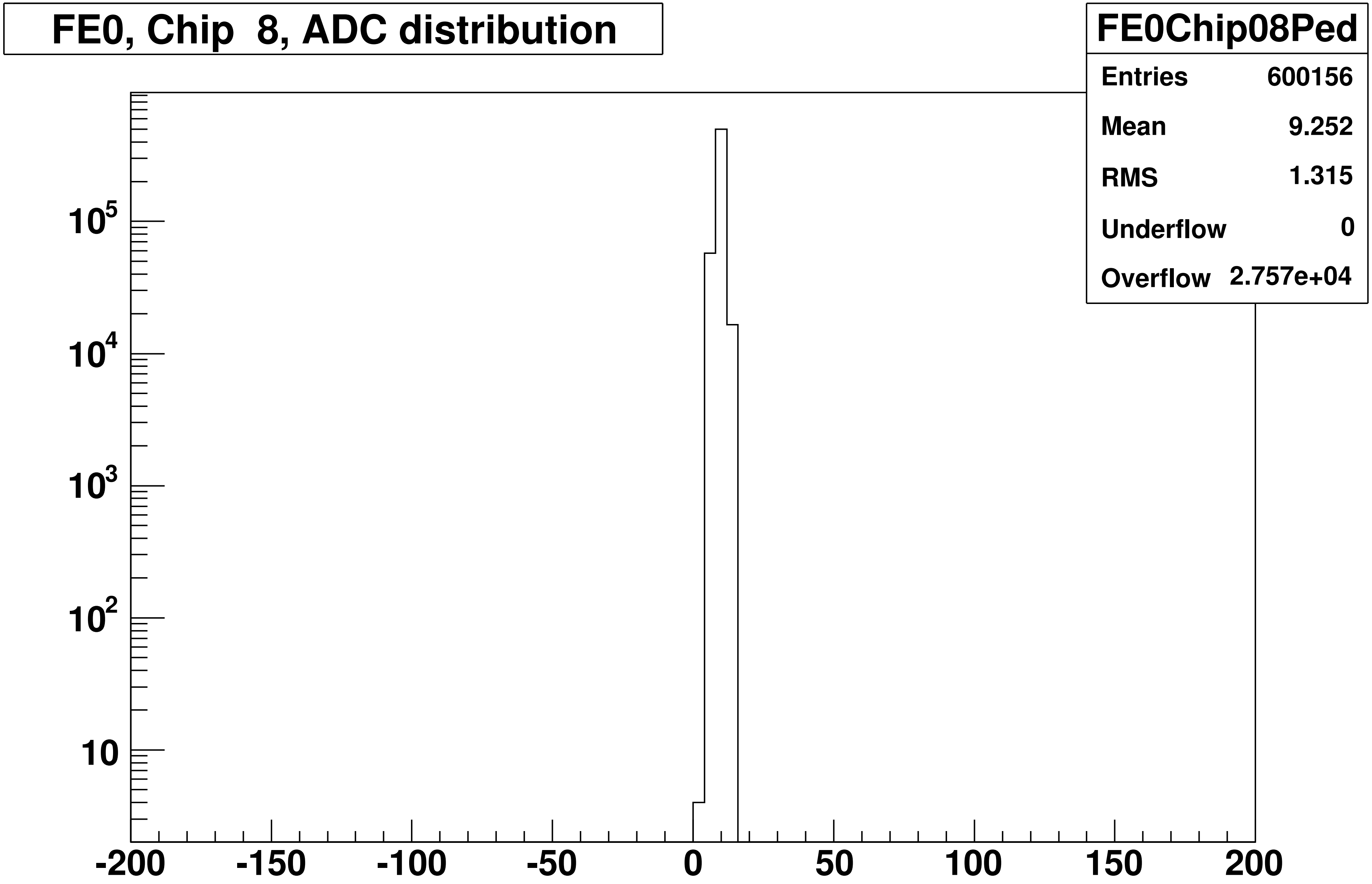

FE0, Chip 8, ADC distribution
FE0Chip08Ped
Entries 600156
Mean 9.252
RMS 1.315
Underflow 0
Overflow 2.757e+04
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10^3
10^2
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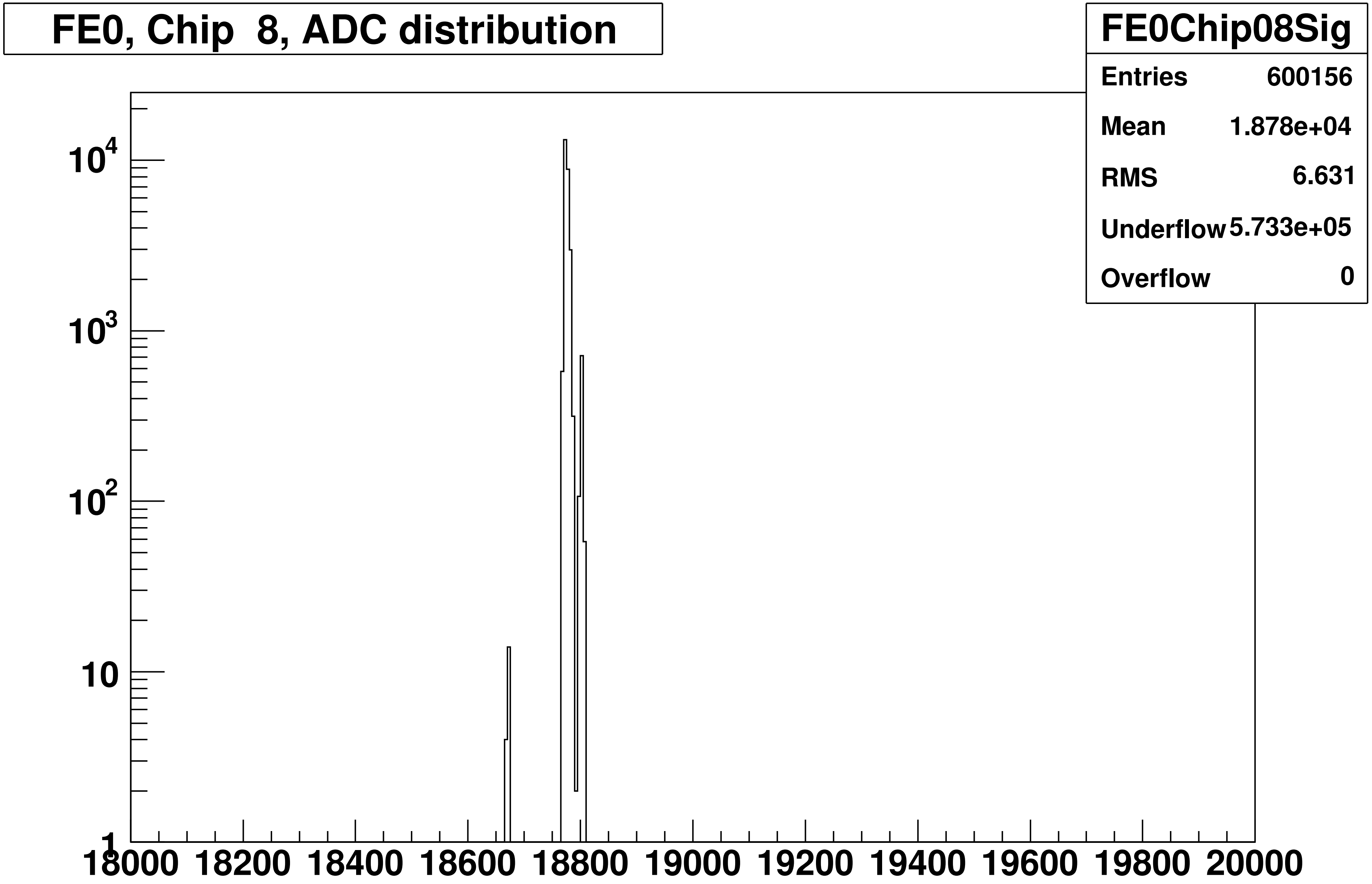

FE0, Chip 8, ADC distribution
FE0Chip08Sig
Entries 600156
Mean 1.878e+04
RMS 6.631
Underflow 5.733e+05
Overflow 0
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10^3
10^2
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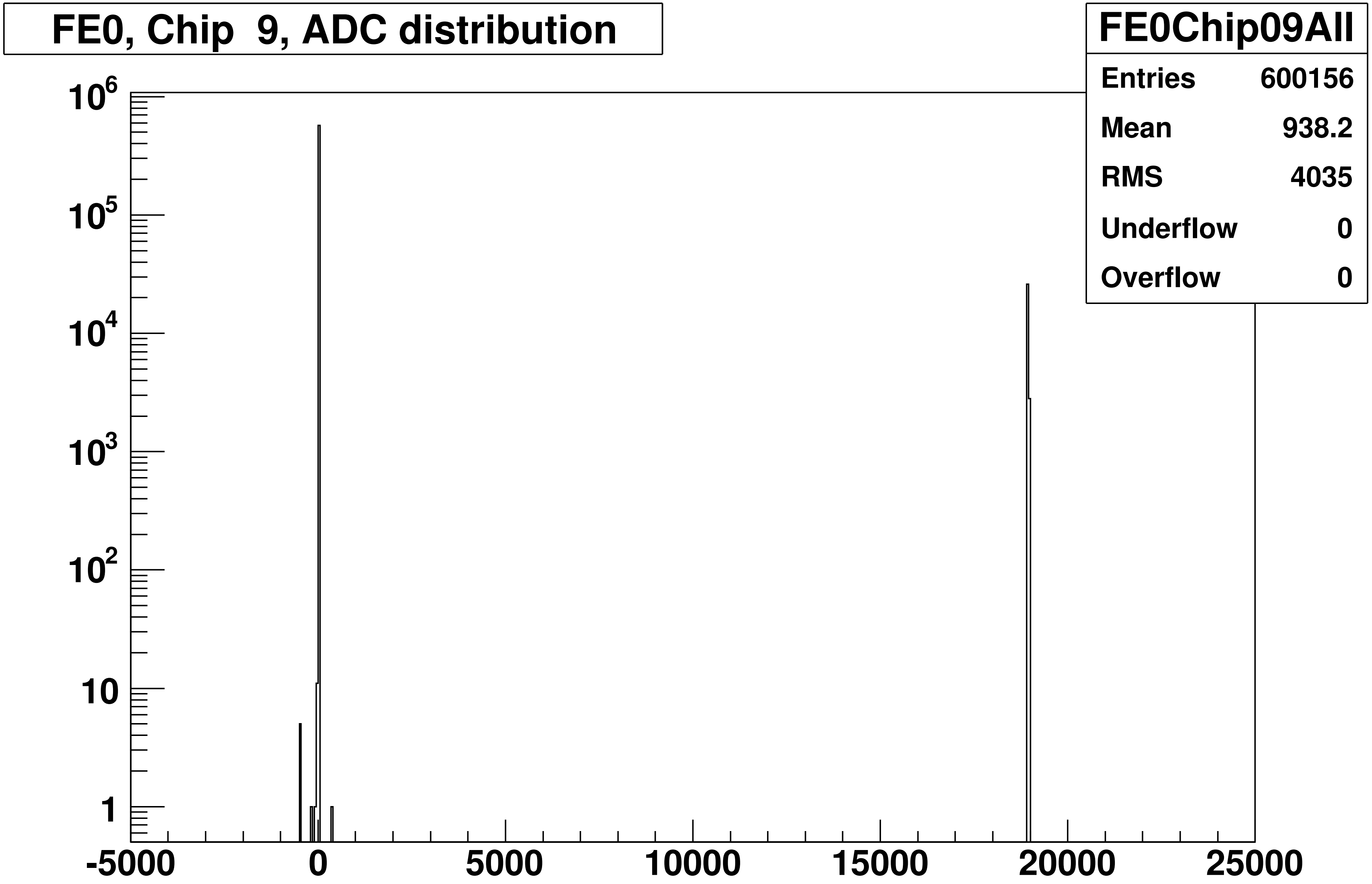
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE0, Chip 9, ADC distribution
FE0Chip09All
Entries 600156
Mean 938.2
RMS 4035
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
1
-5000
0
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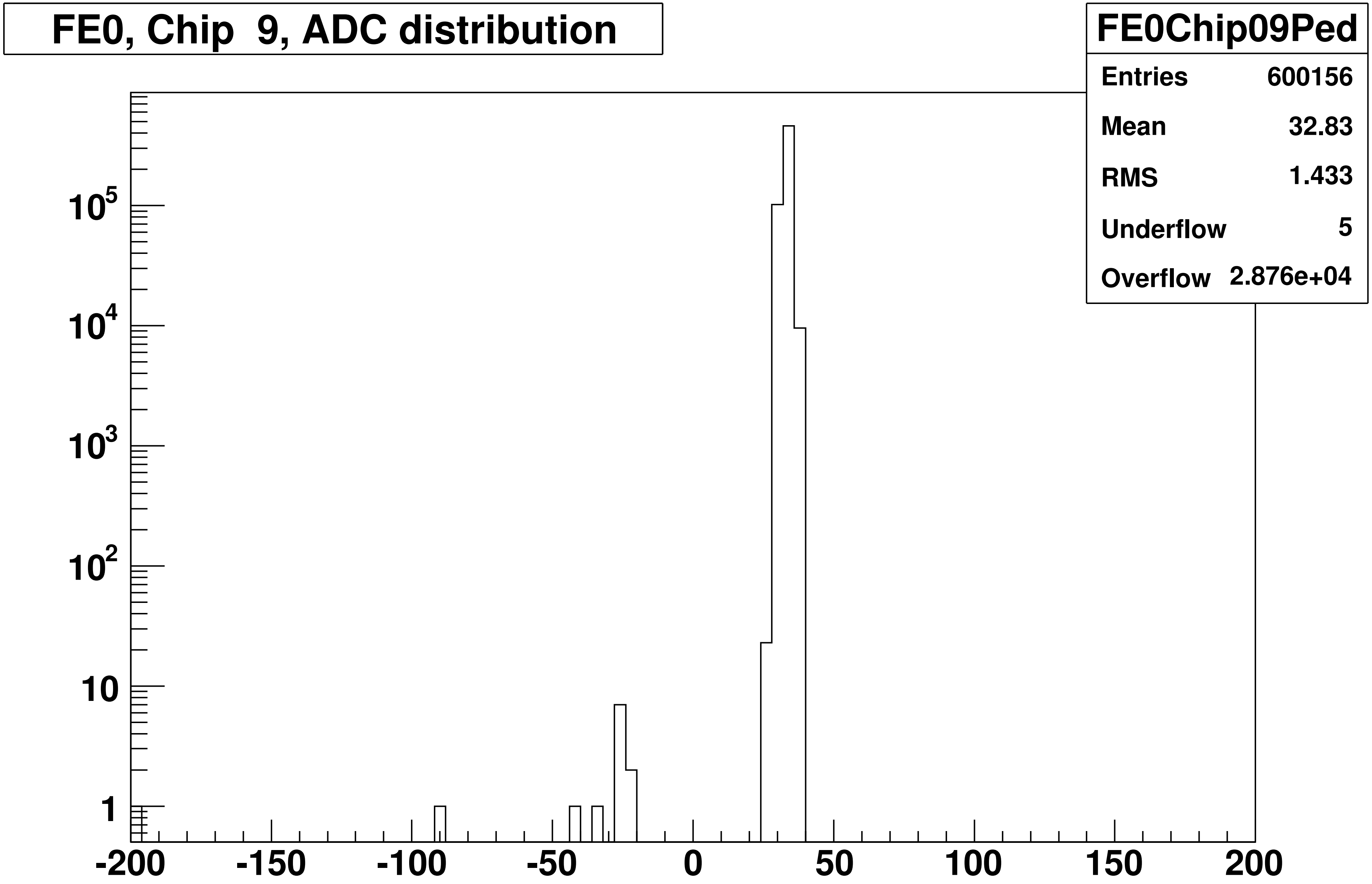
20000
25000


FE0, Chip 9, ADC distribution
FE0Chip09Ped
Entries 600156
Mean 32.83
RMS 1.433
Underflow 5
Overflow 2.876e+04
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10^4
10^3
10^2
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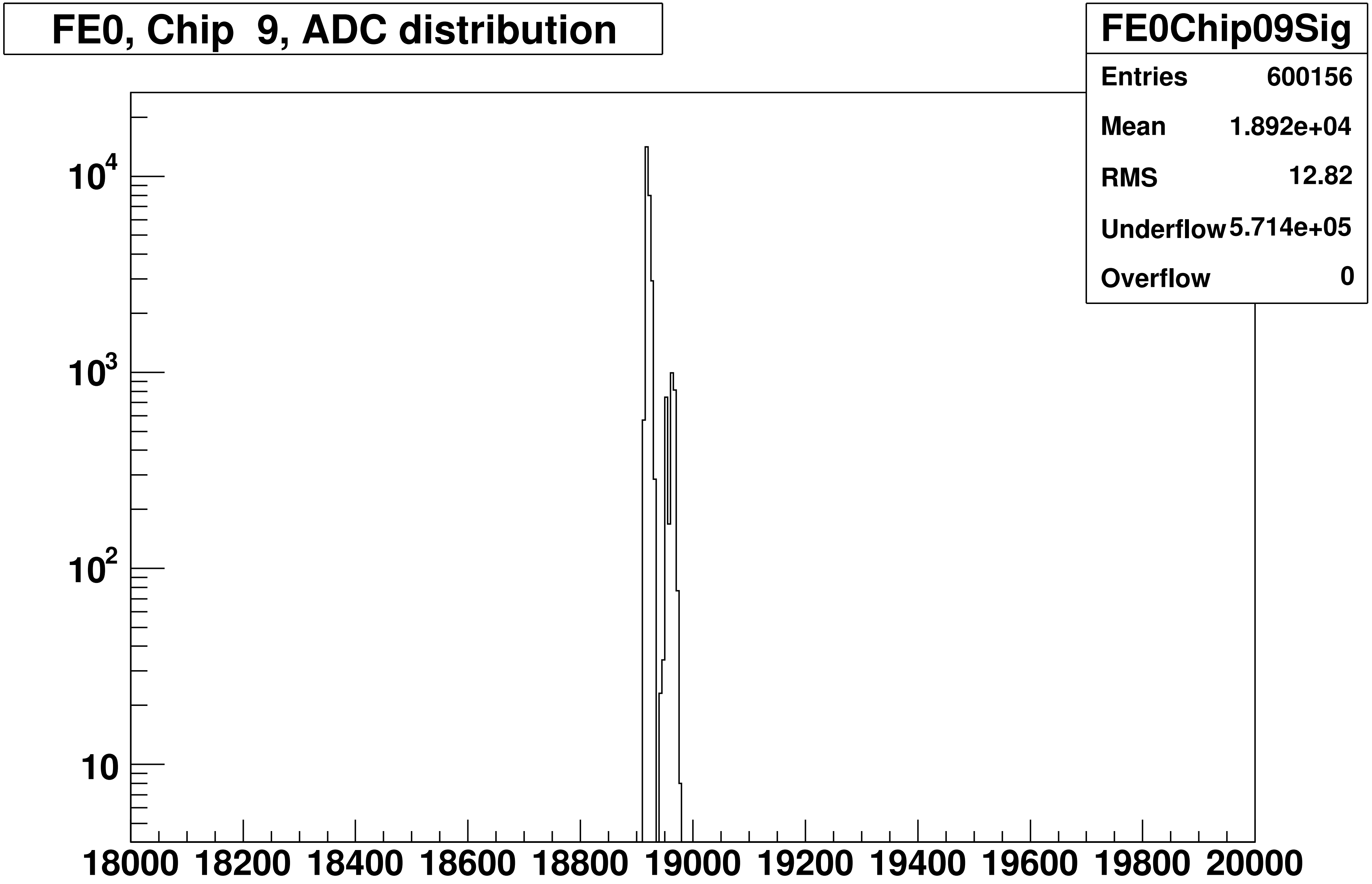
200



FE0, Chip 9, ADC distribution
FE0Chip09Sig
Entries 600156
Mean 1.892e+04
RMS 12.82
Underflow 5.714e+05
Overflow 0
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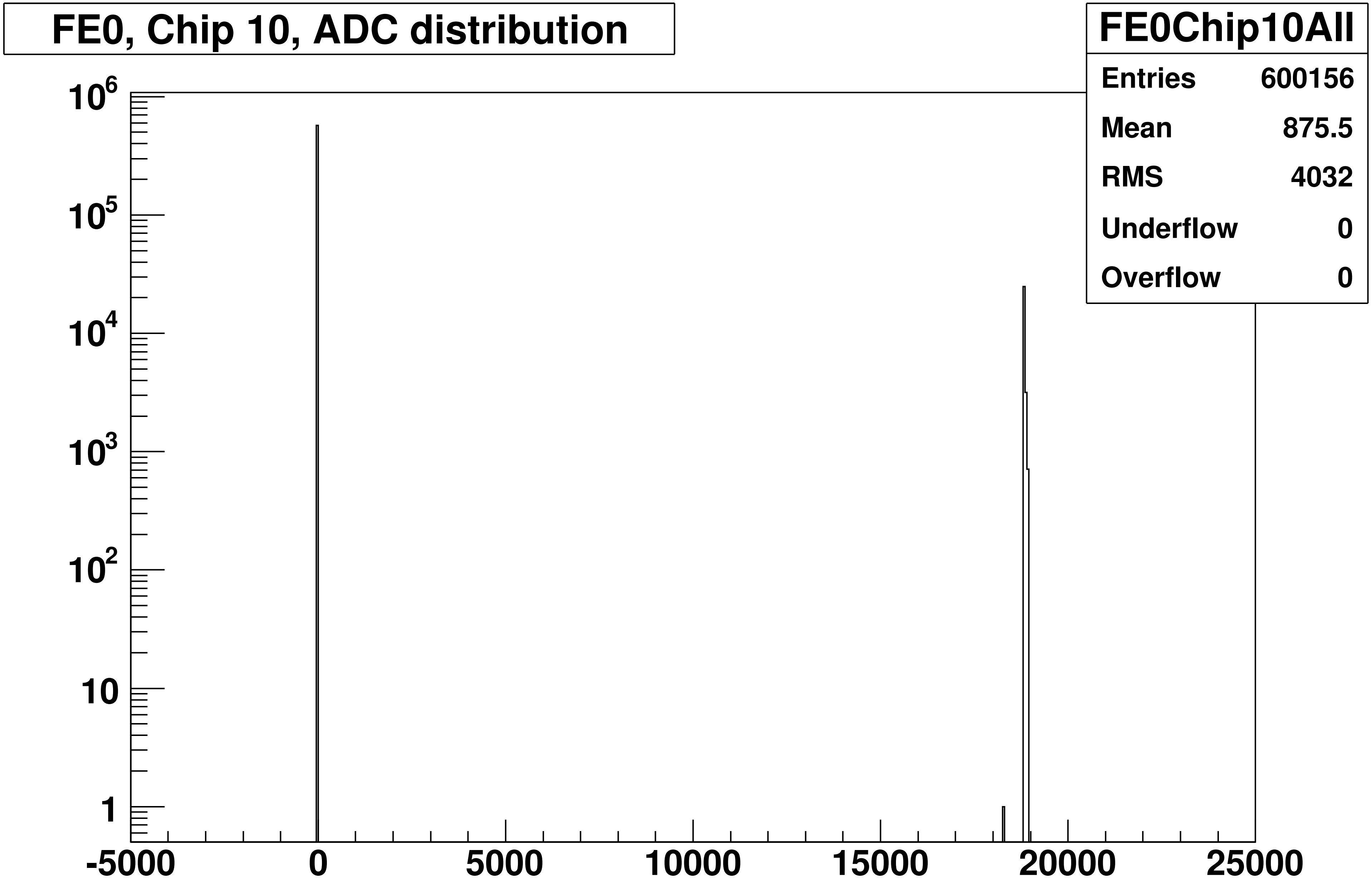
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE0, Chip 10, ADC distribution
FE0Chip10All
Entries 600156
Mean 875.5
RMS 4032
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
1
-5000
0
5000
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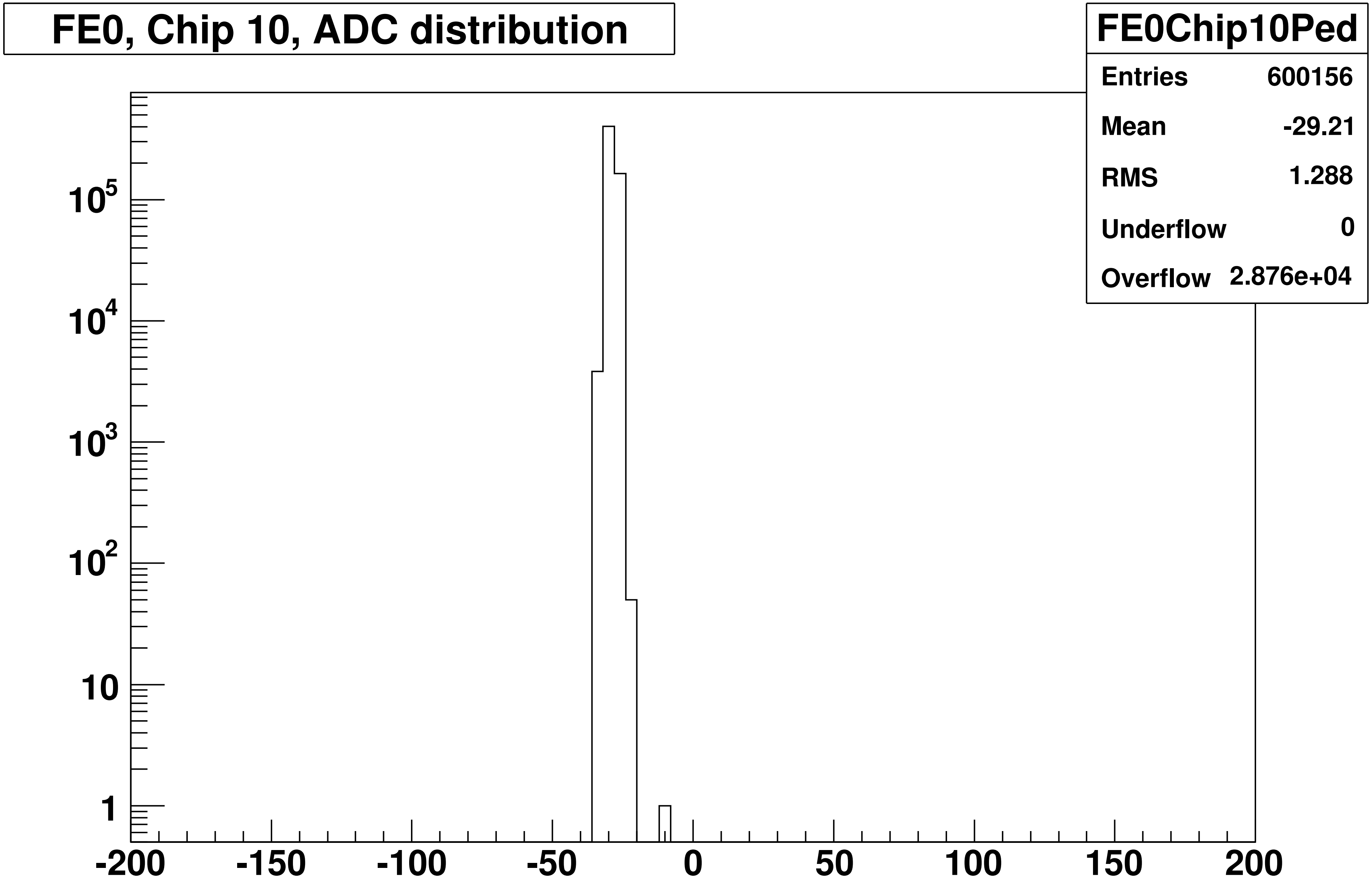
20000
25000


FE0, Chip 10, ADC distribution
FE0Chip10Ped
Entries 600156
Mean -29.21
RMS 1.288
Underflow 0
Overflow 2.876e+04
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10^3
10^2
10
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0
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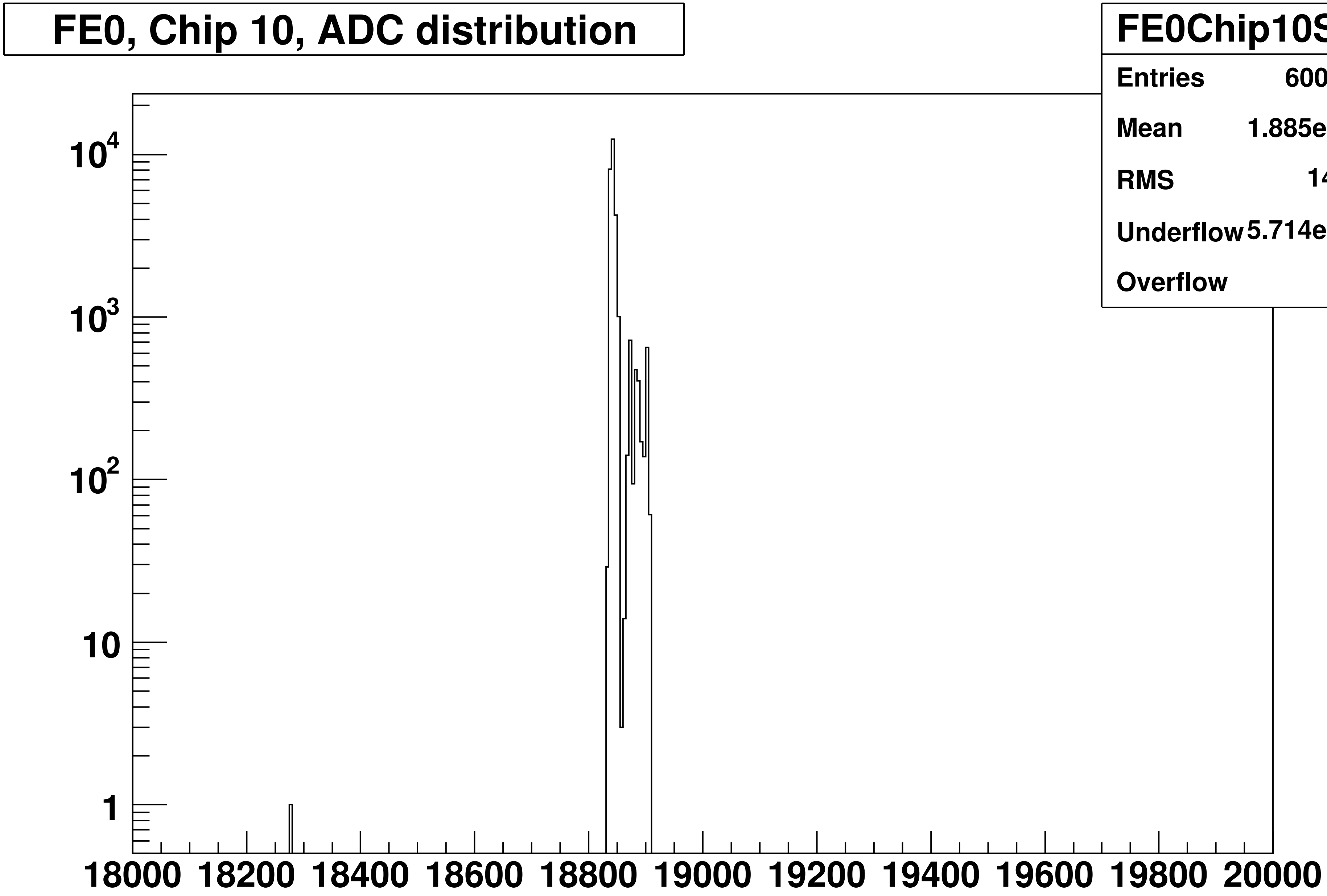
150
200



FE0, Chip 10, ADC distribution
FE0Chip10Sig
Entries 600156
Mean 1.885e+04
RMS 14.52
Underflow 5.714e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
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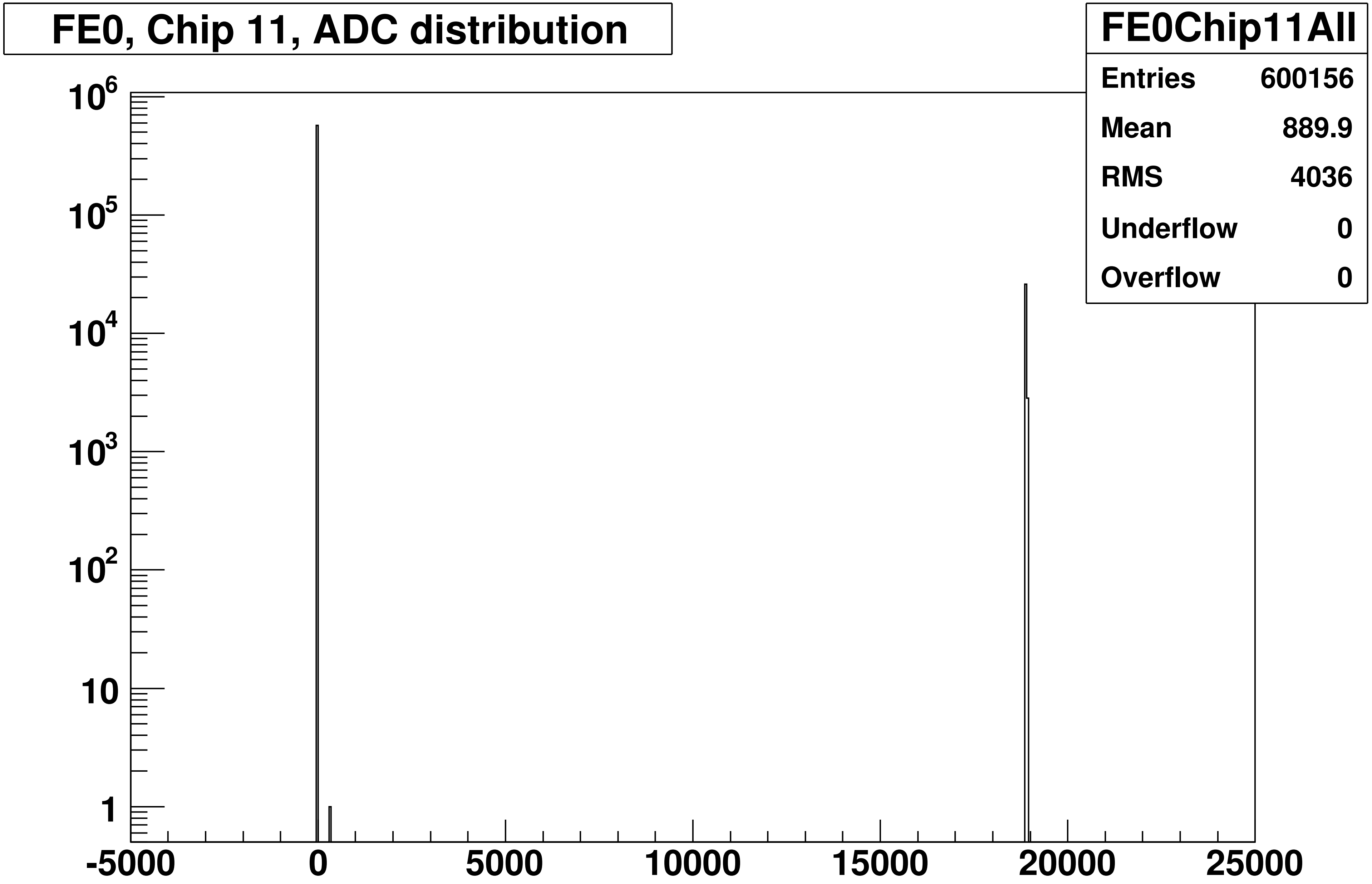
19800
20000



FE0, Chip 11, ADC distribution
FE0Chip11All
Entries 600156
Mean 889.9
RMS 4036
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
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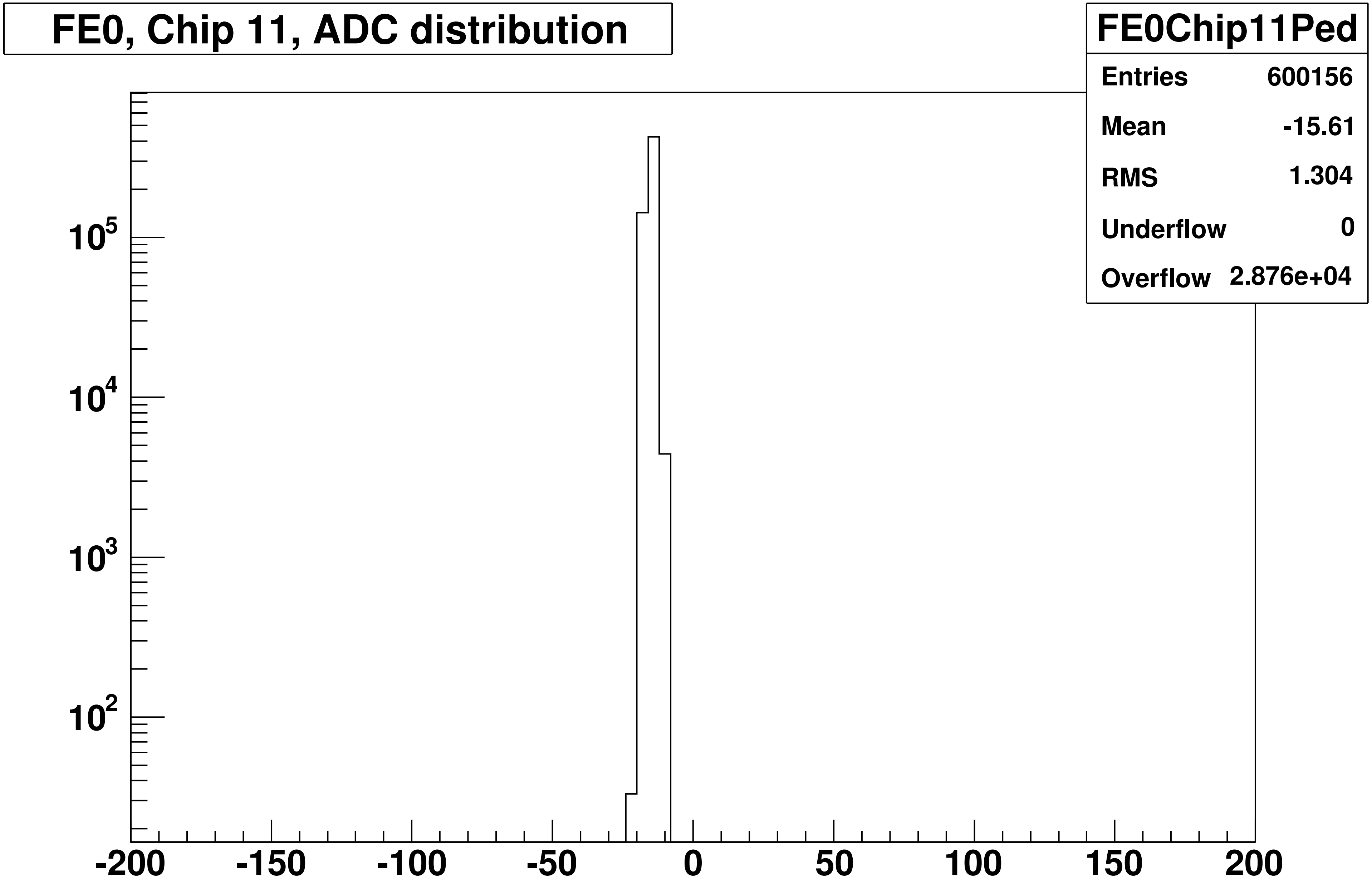

FE0, Chip 11, ADC distribution
FE0Chip11Ped
Entries 600156
Mean -15.61
RMS 1.304
Underflow 0
Overflow 2.876e+04
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10^4
10^3
10^2
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-100
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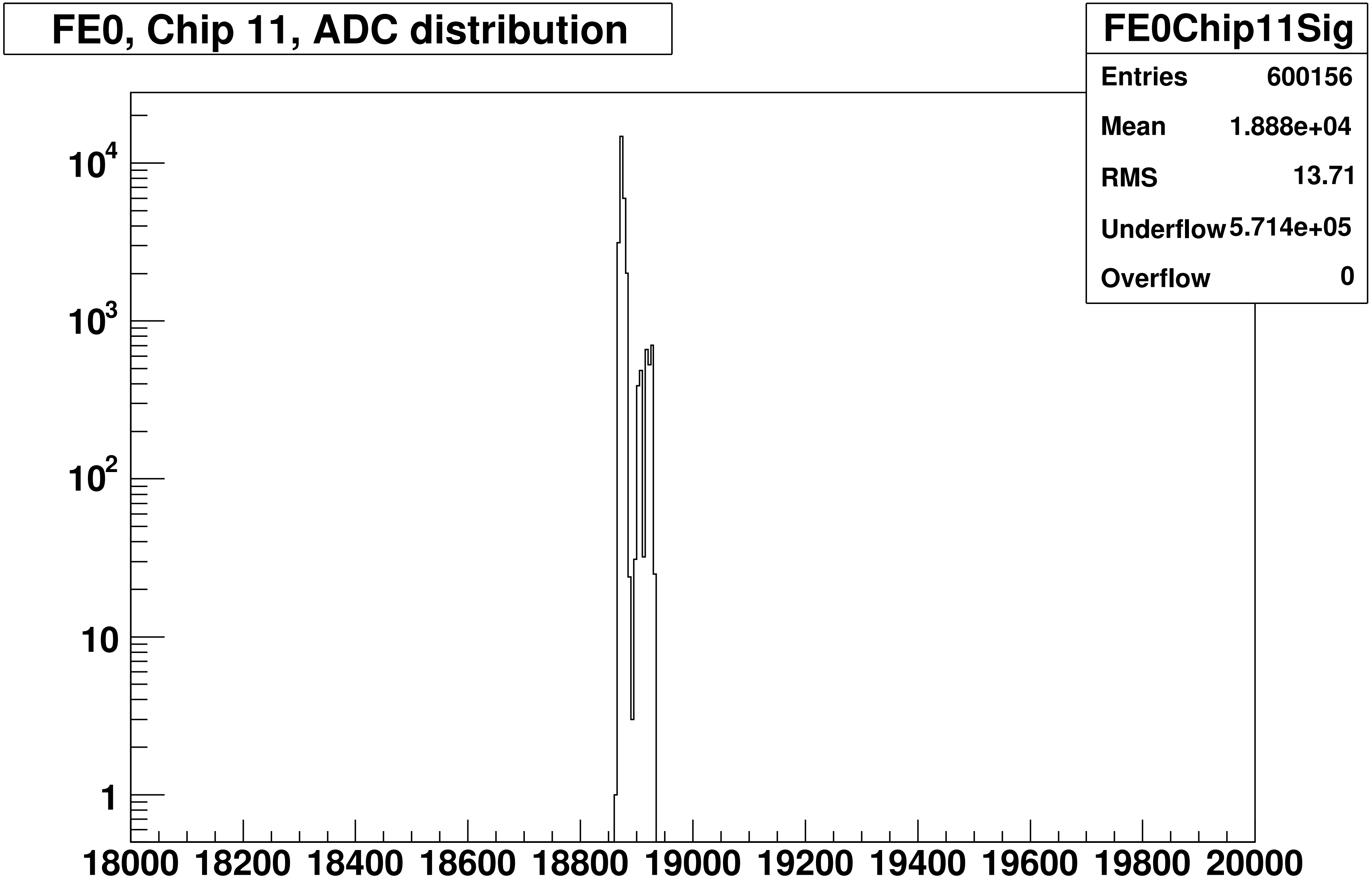
50
100
150
200



FE0, Chip 11, ADC distribution
FE0Chip11Sig
Entries 600156
Mean 1.888e+04
RMS 13.71
Underflow 5.714e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
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19000
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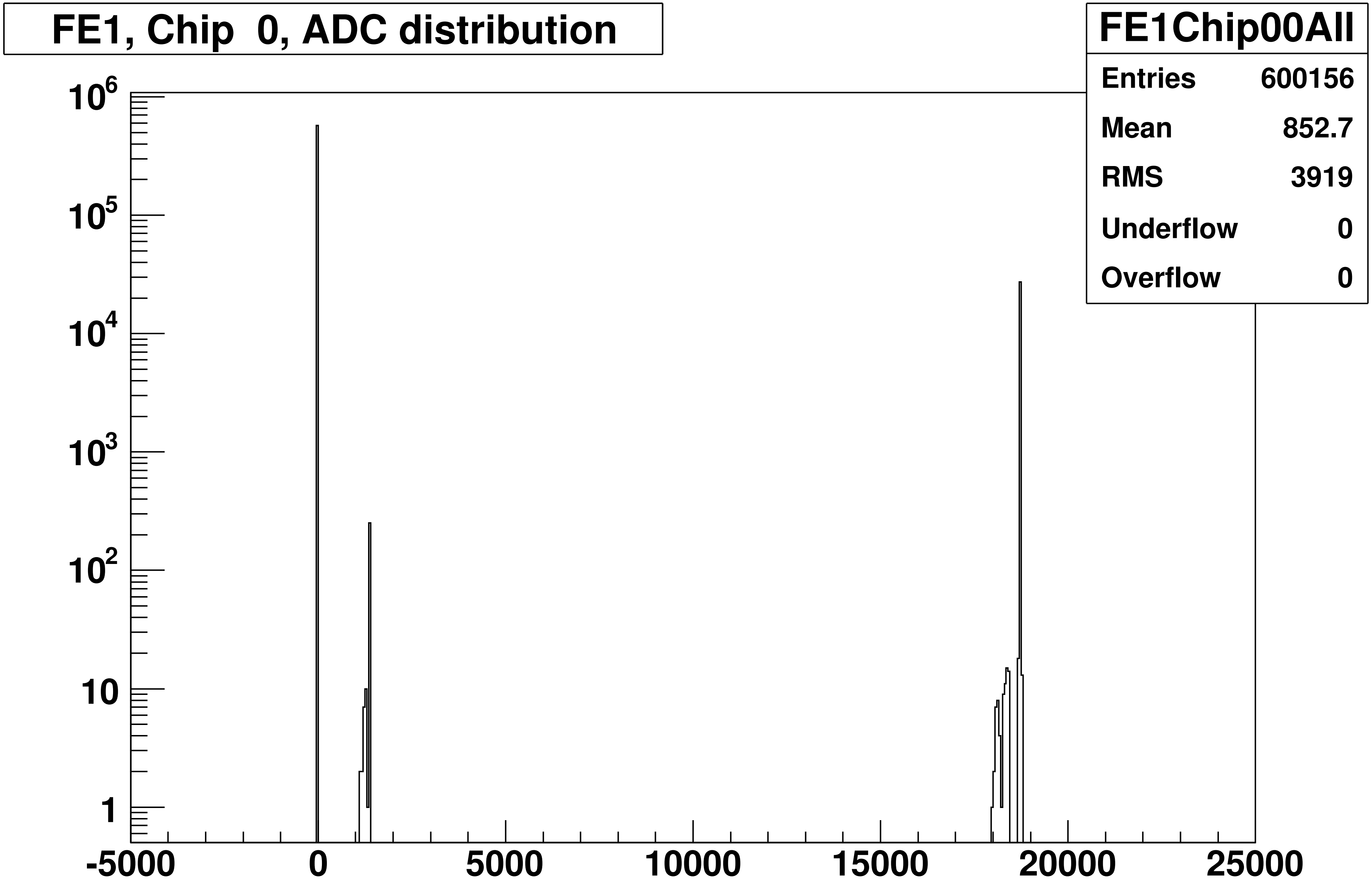
19600
19800
20000


FE1, Chip 0, ADC distribution
FE1Chip00All
Entries 600156
Mean 852.7
RMS 3919
Underflow 0
Overflow 0
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10
10^2
10^3
10^4
10^5
10^6
-5000
0
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10000
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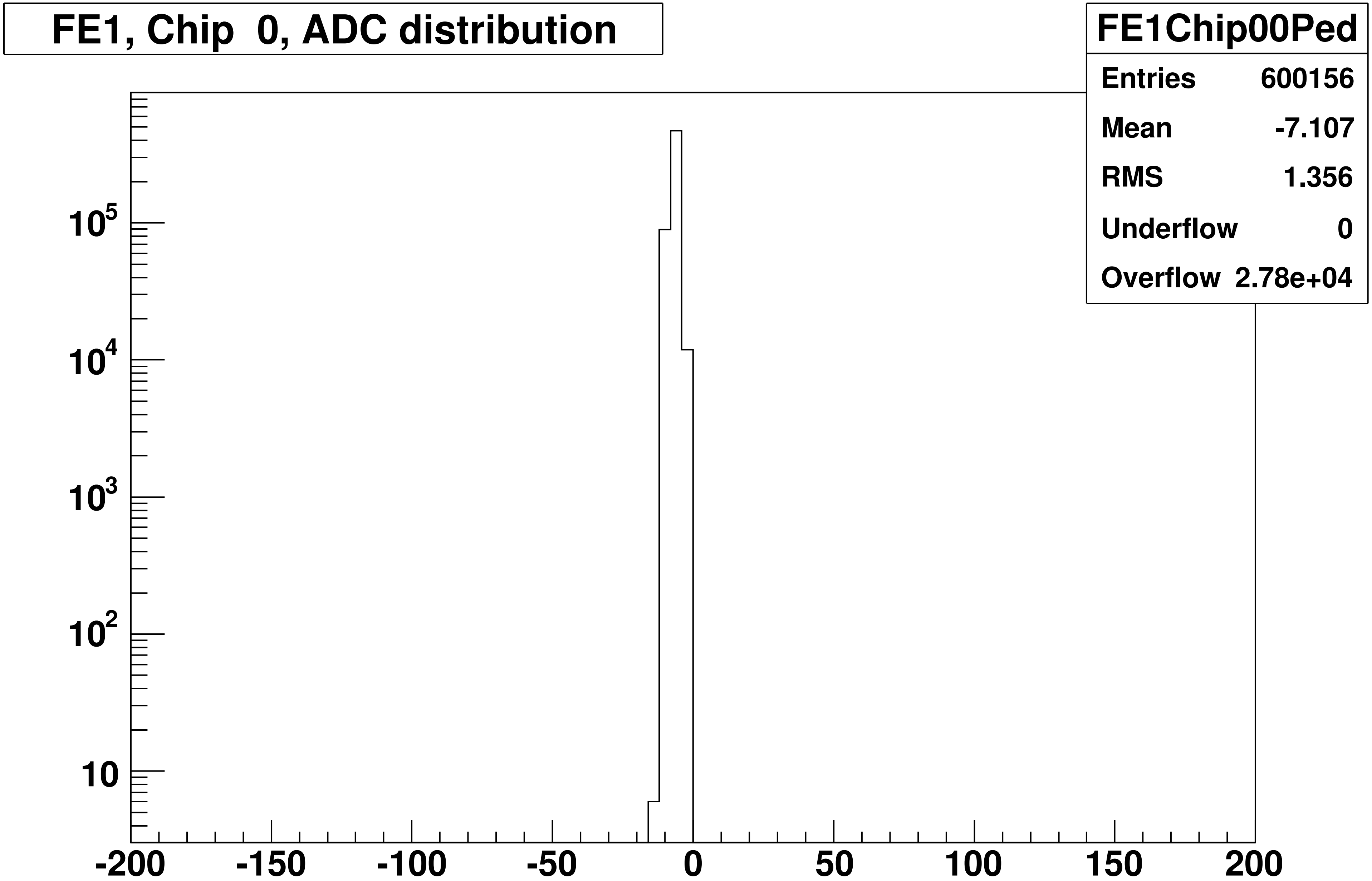
20000
25000


FE1, Chip 0, ADC distribution
FE1Chip00Ped
Entries 600156
Mean -7.107
RMS 1.356
Underflow 0
Overflow 2.78e+04
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10^4
10^3
10^2
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-100
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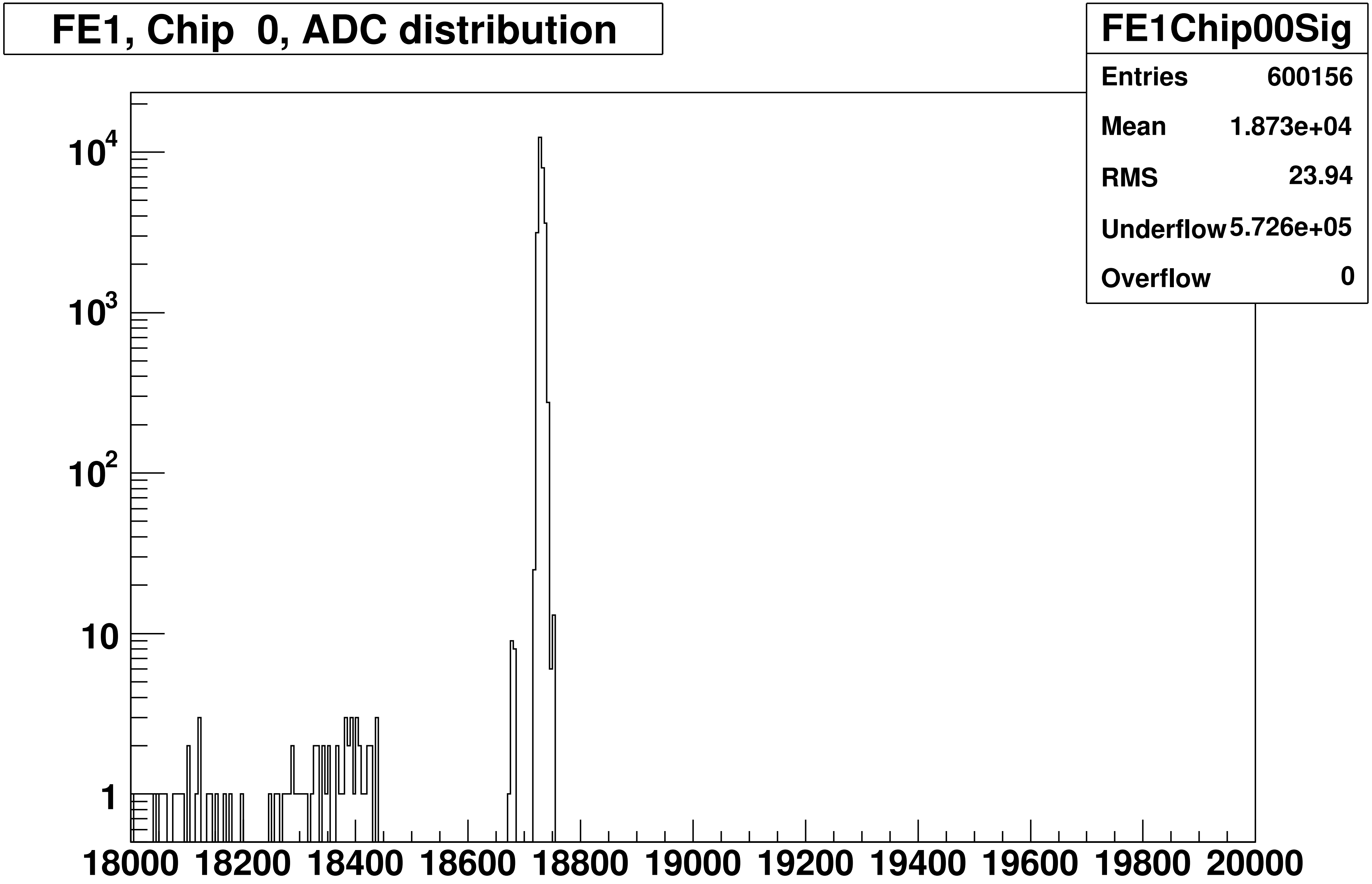
50
100
150
200



FE1, Chip 0, ADC distribution
FE1Chip00Sig
Entries 600156
Mean 1.873e+04
RMS 23.94
Underflow 5.726e+05
Overflow 0
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10^3
10^2
10
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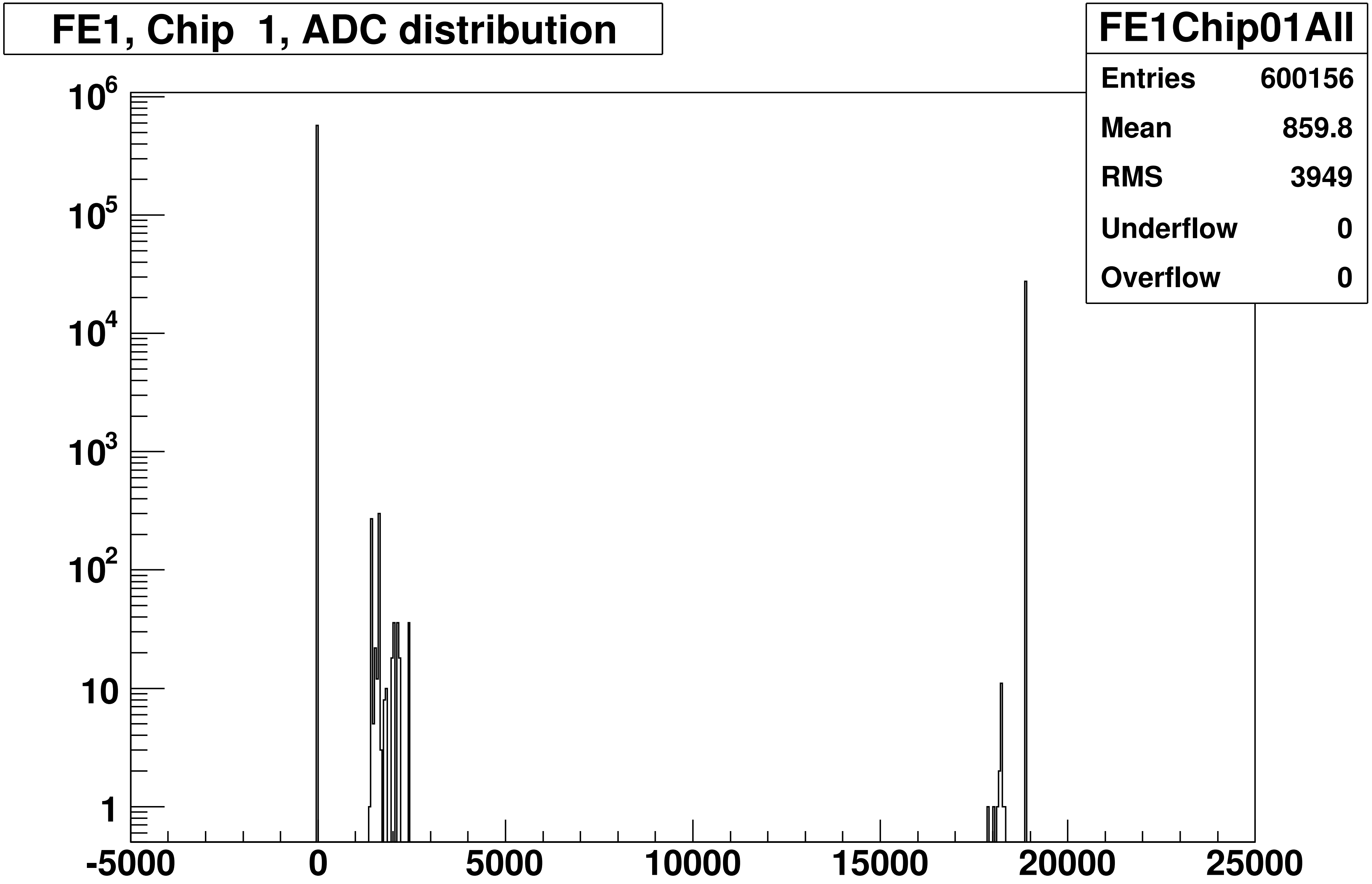
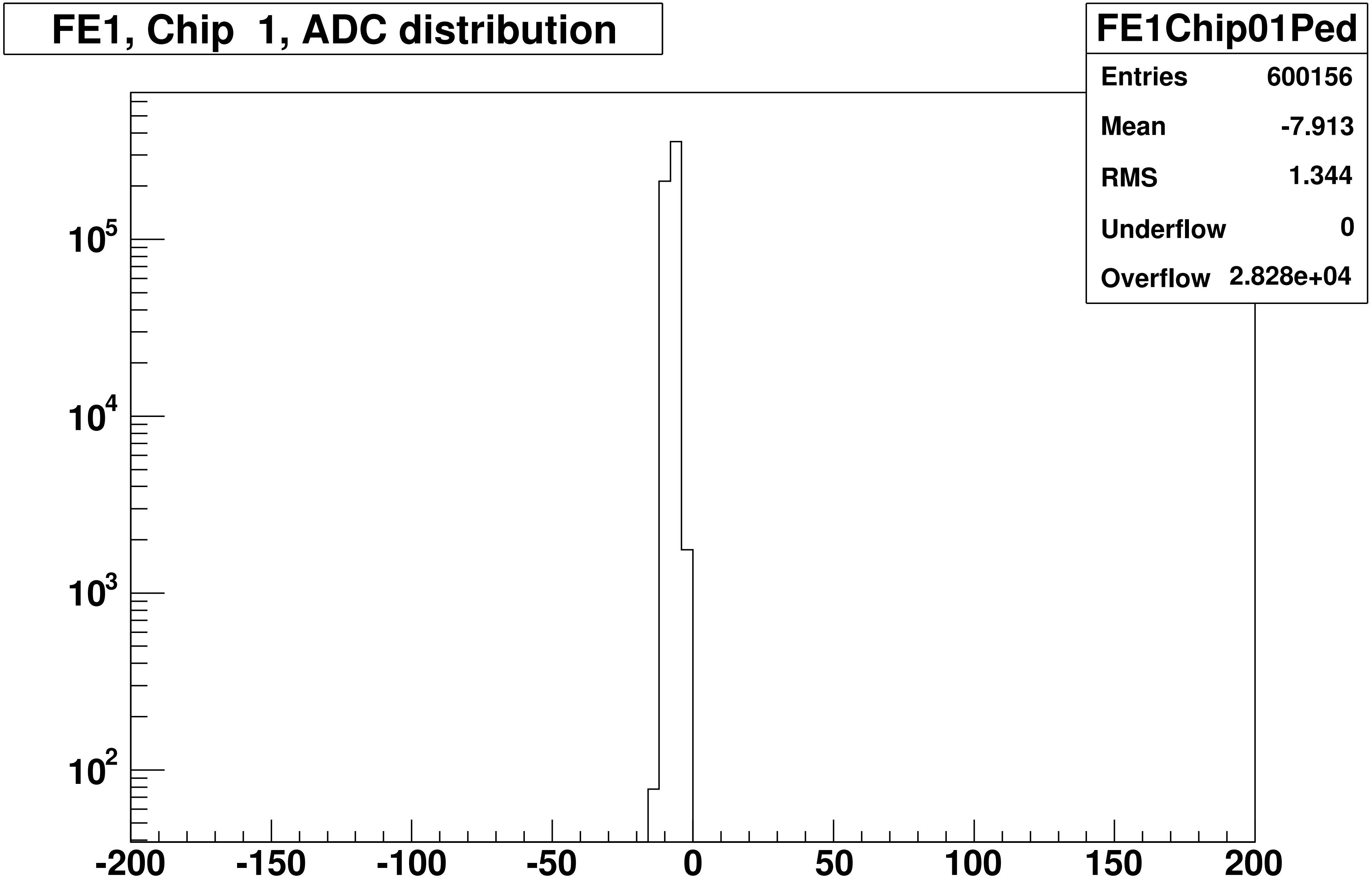
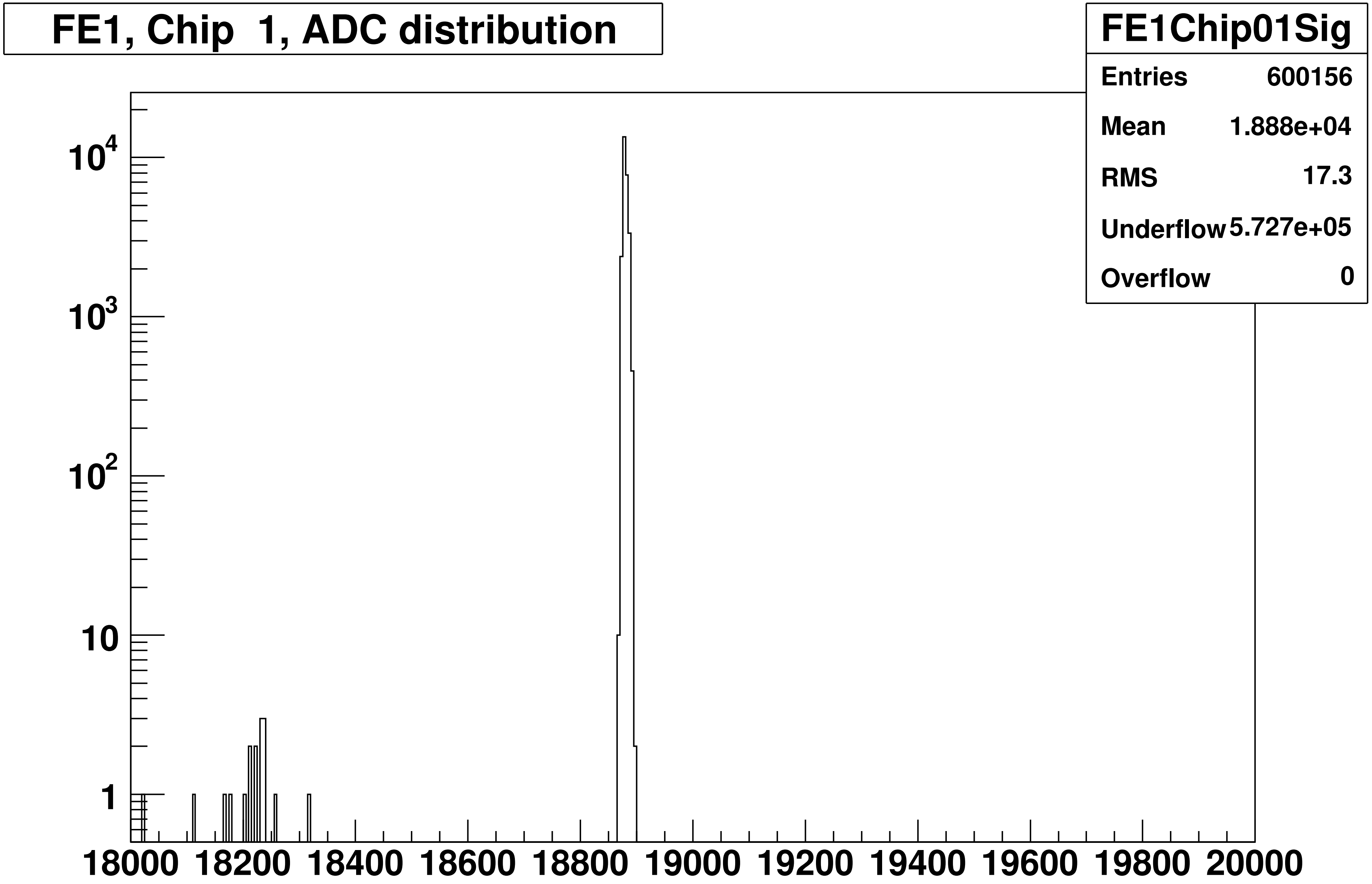
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



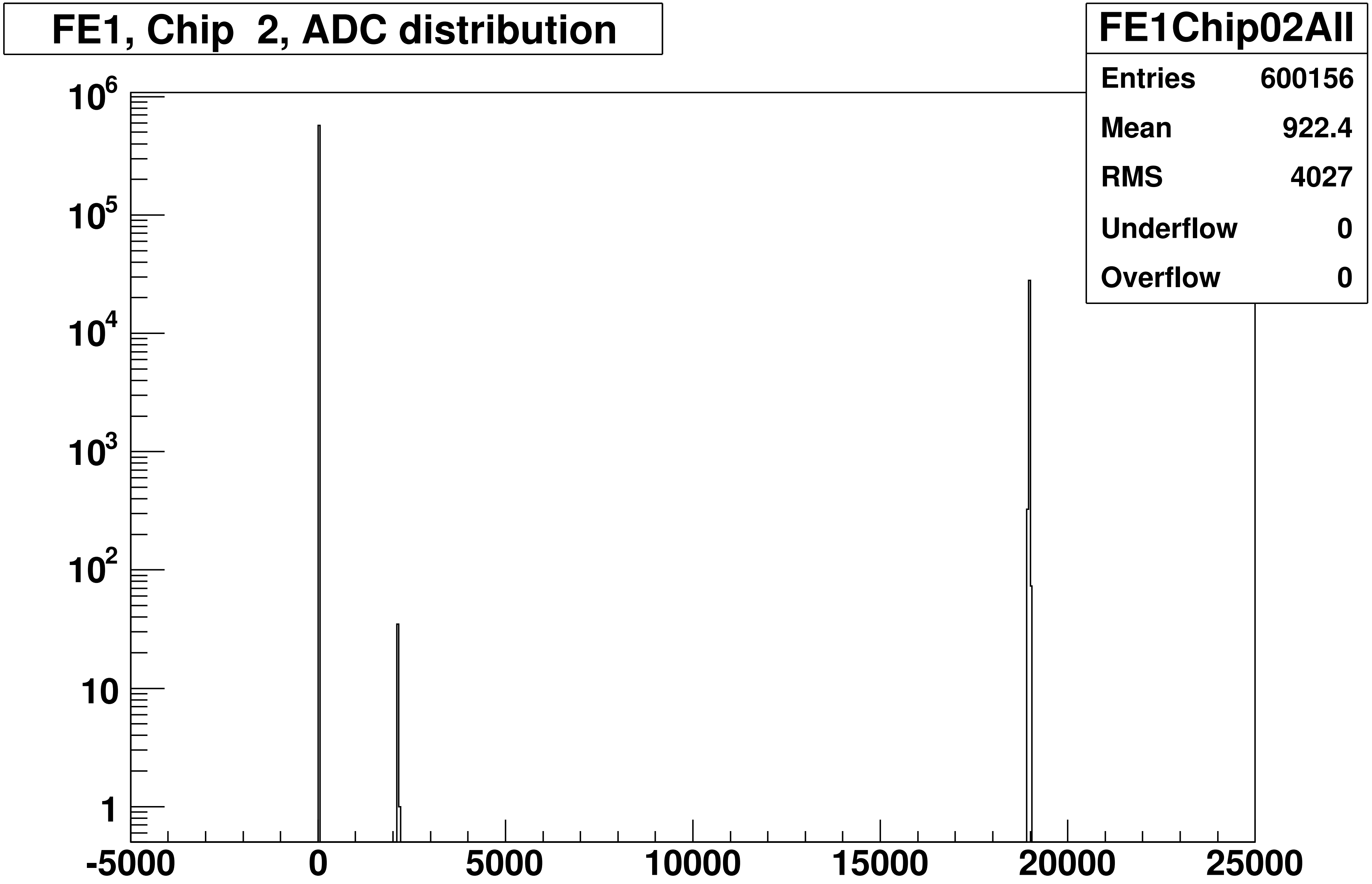
FE1, Chip 1, ADC distribution
FE1Chip01All
Entries 600156
Mean 859.8
RMS 3949
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000

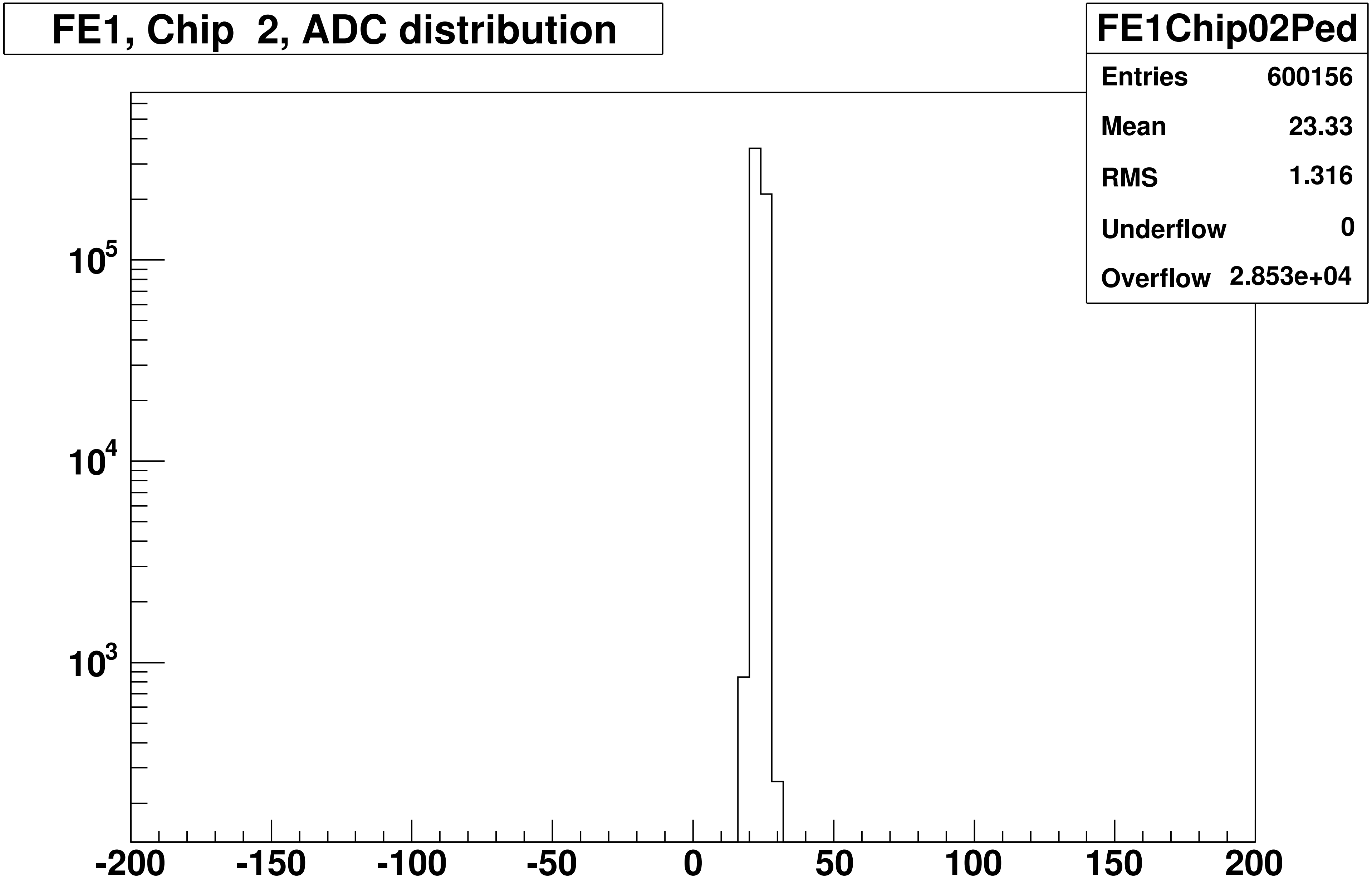


FE1, Chip 1, ADC distribution
FE1Chip01Ped
Entries 600156
Mean -7.913
RMS 1.344
Underflow 0
Overflow 2.828e+04
10^5
10^4
10^3
10^2
-200
-150
-100
-50
0
50
100
150
200



FE1, Chip 1, ADC distribution
FE1Chip01Sig
Entries 600156
Mean 1.888e+04
RMS 17.3
Underflow 5.727e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE1, Chip 2, ADC distribution
FE1Chip02All
Entries 600156
Mean 922.4
RMS 4027
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE1, Chip 2, ADC distribution
FE1Chip02Ped
Entries 600156
Mean 23.33
RMS 1.316
Underflow 0
Overflow 2.853e+04
10^5
10^4
10^3
-200
-150
-100
-50
0
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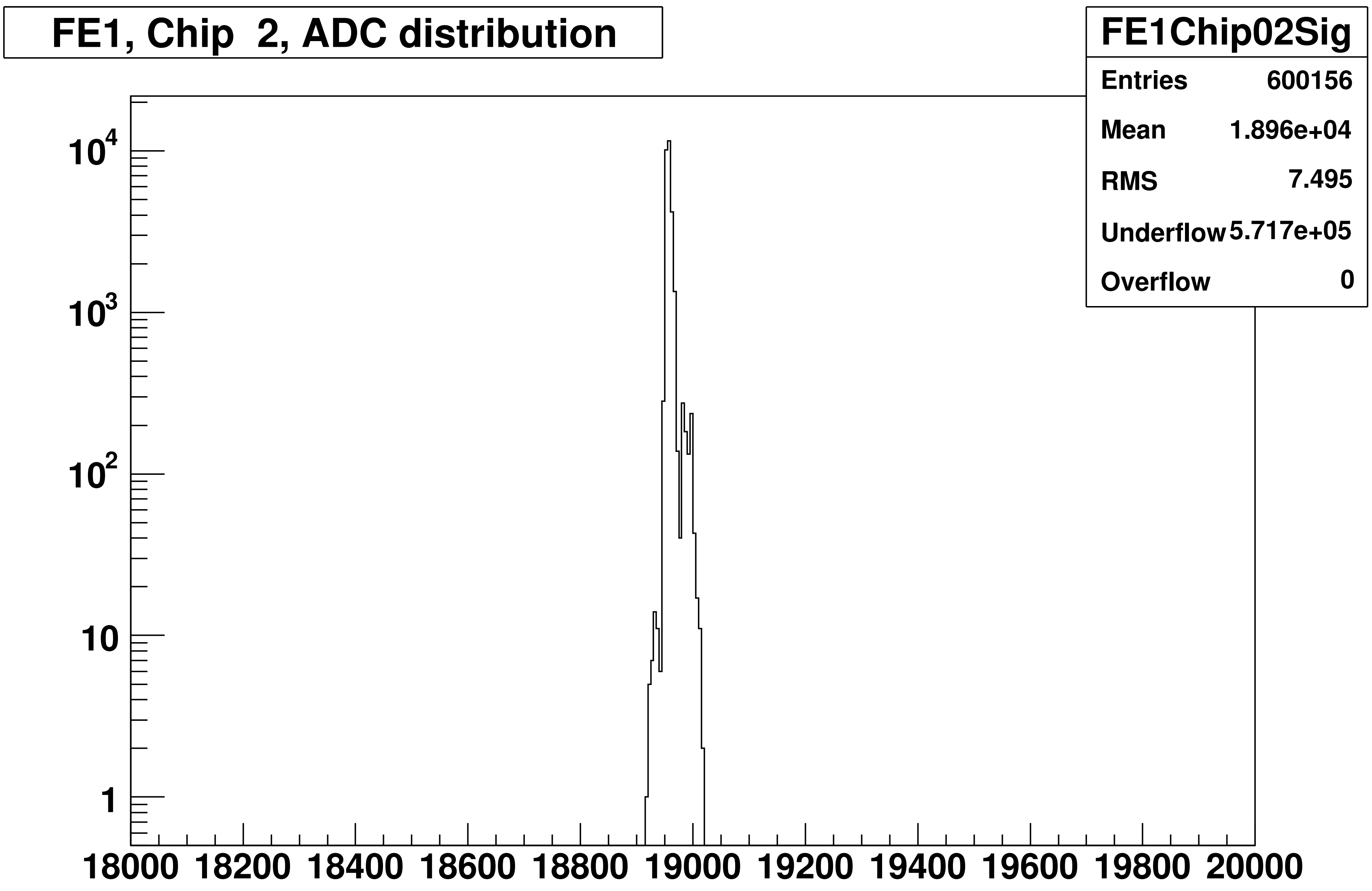
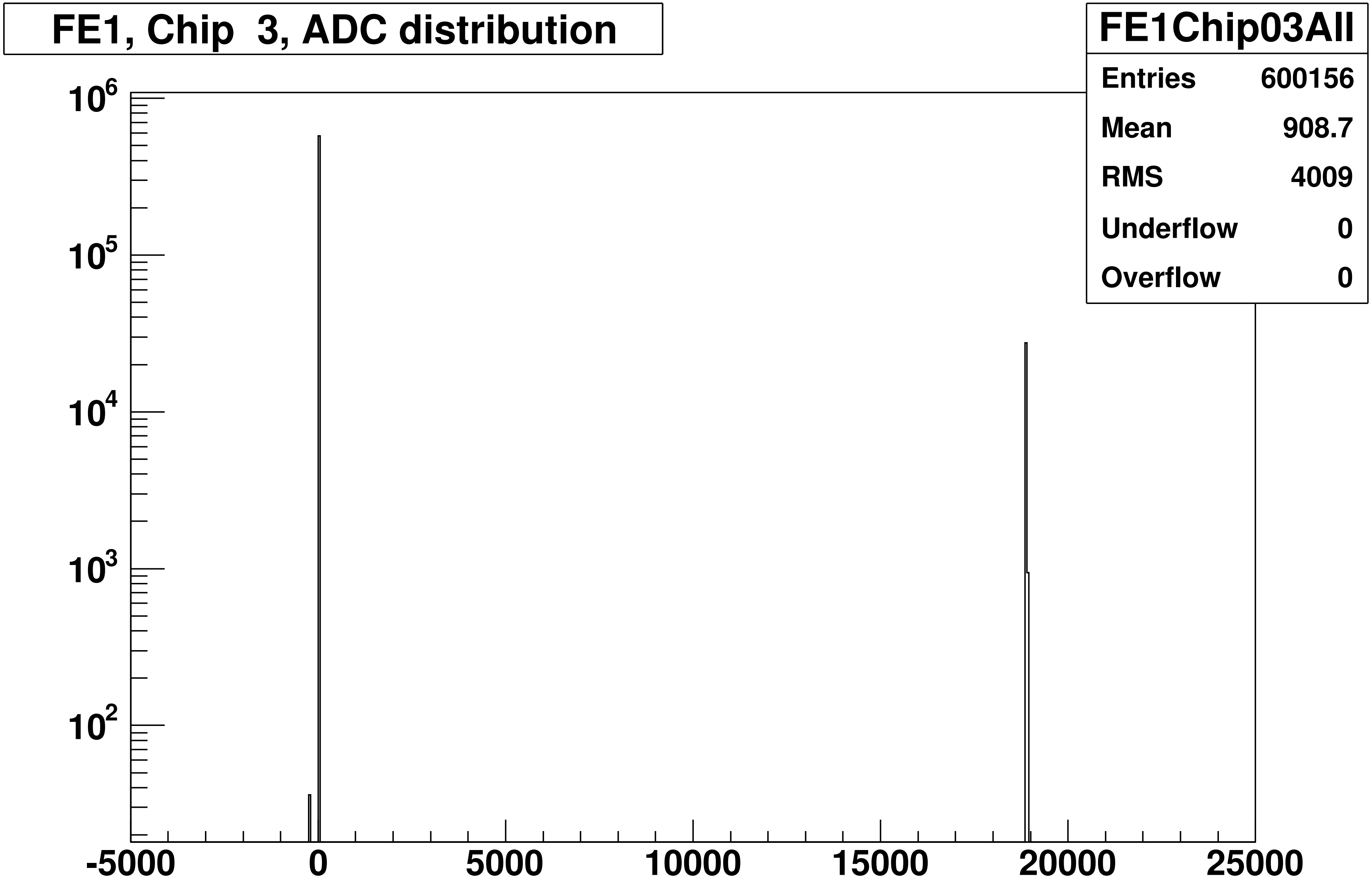
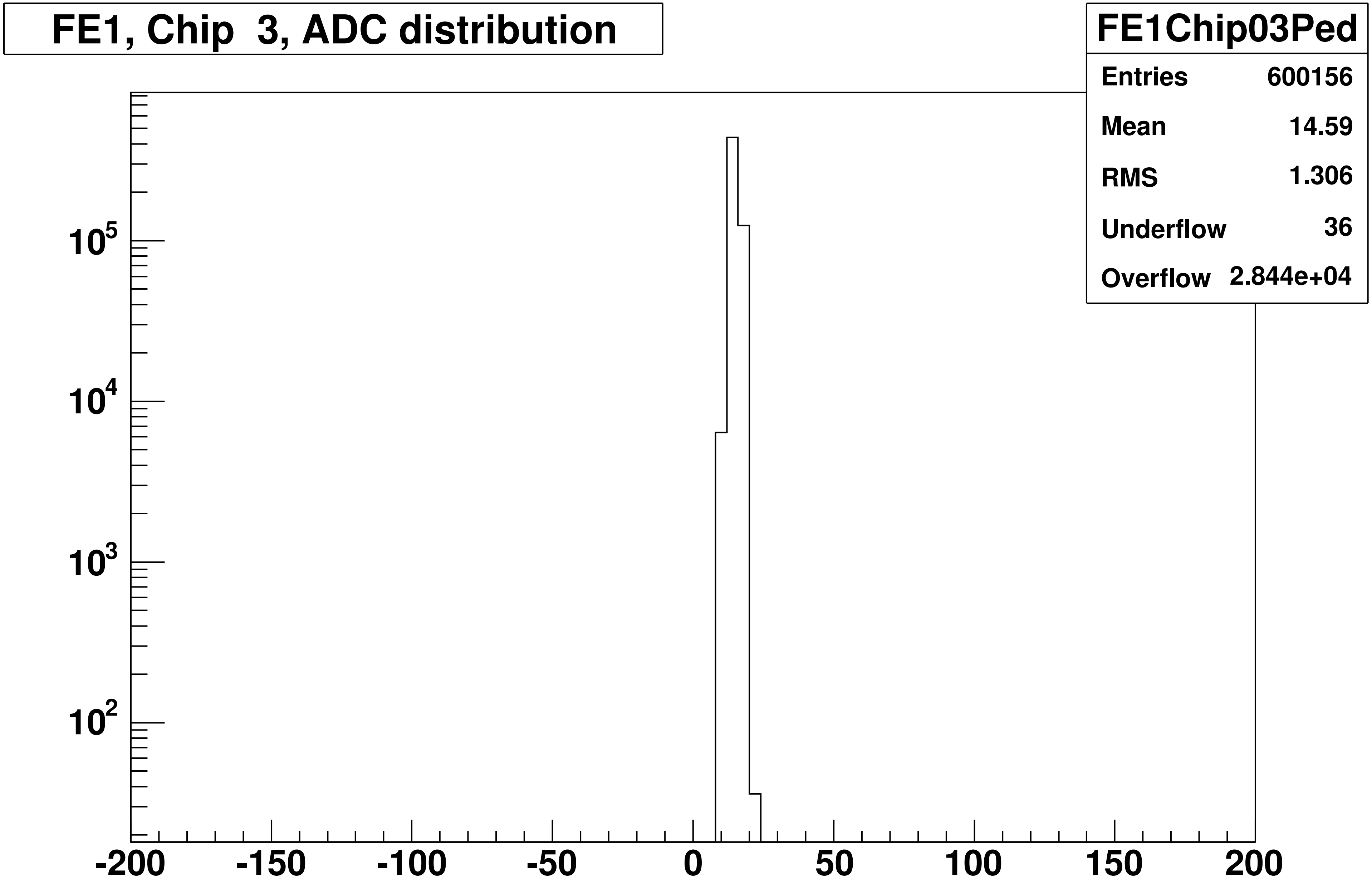
100
150
200



FE1, Chip 2, ADC distribution
FE1Chip02Sig
Entries 600156
Mean 1.896e+04
RMS 7.495
Underflow 5.717e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE1, Chip 3, ADC distribution
FE1Chip03All
Entries 600156
Mean 908.7
RMS 4009
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000



FE1, Chip 3, ADC distribution
FE1Chip03Ped
Entries 600156
Mean 14.59
RMS 1.306
Underflow 36
Overflow 2.844e+04
10^5
10^4
10^3
10^2
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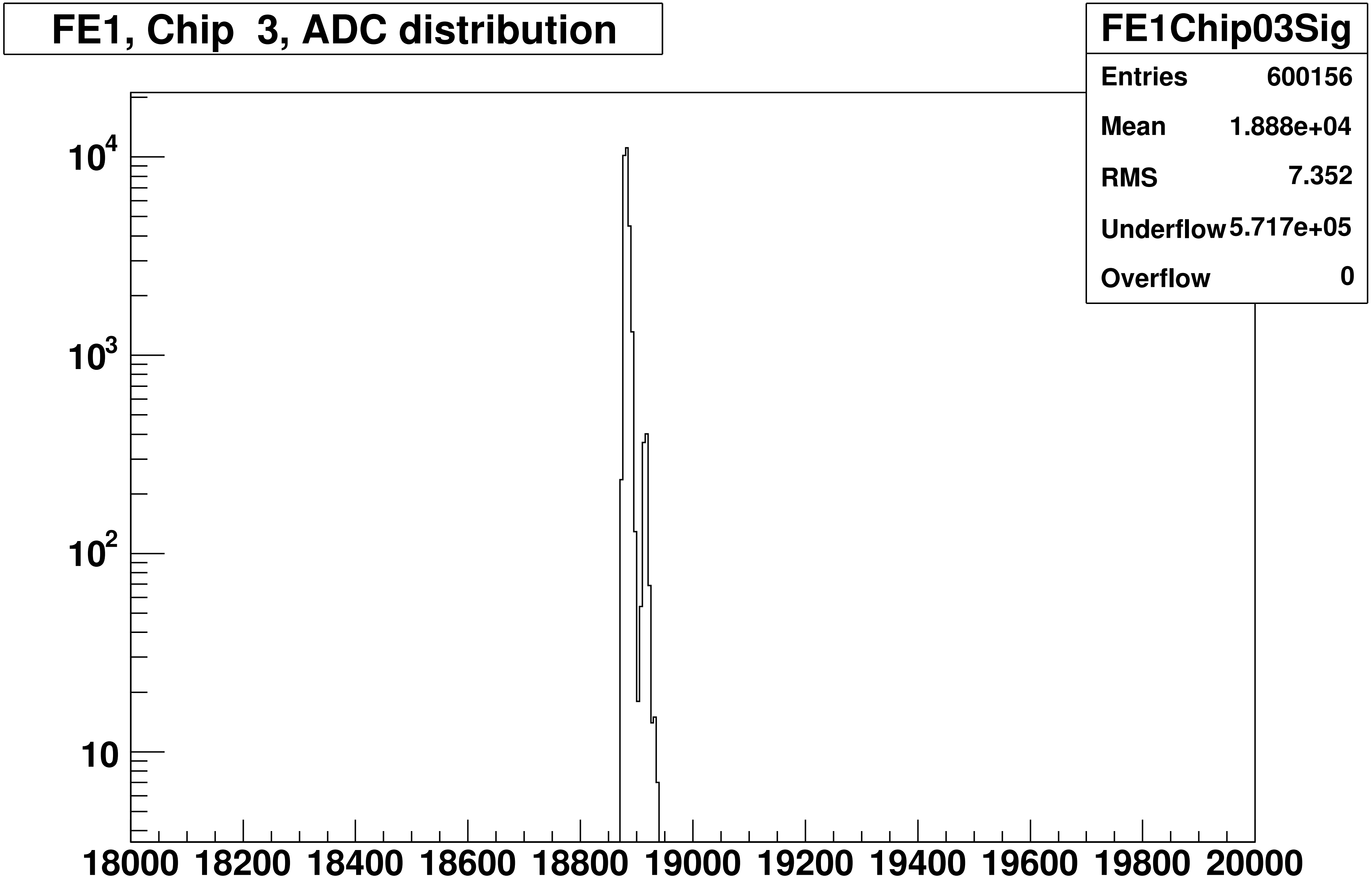
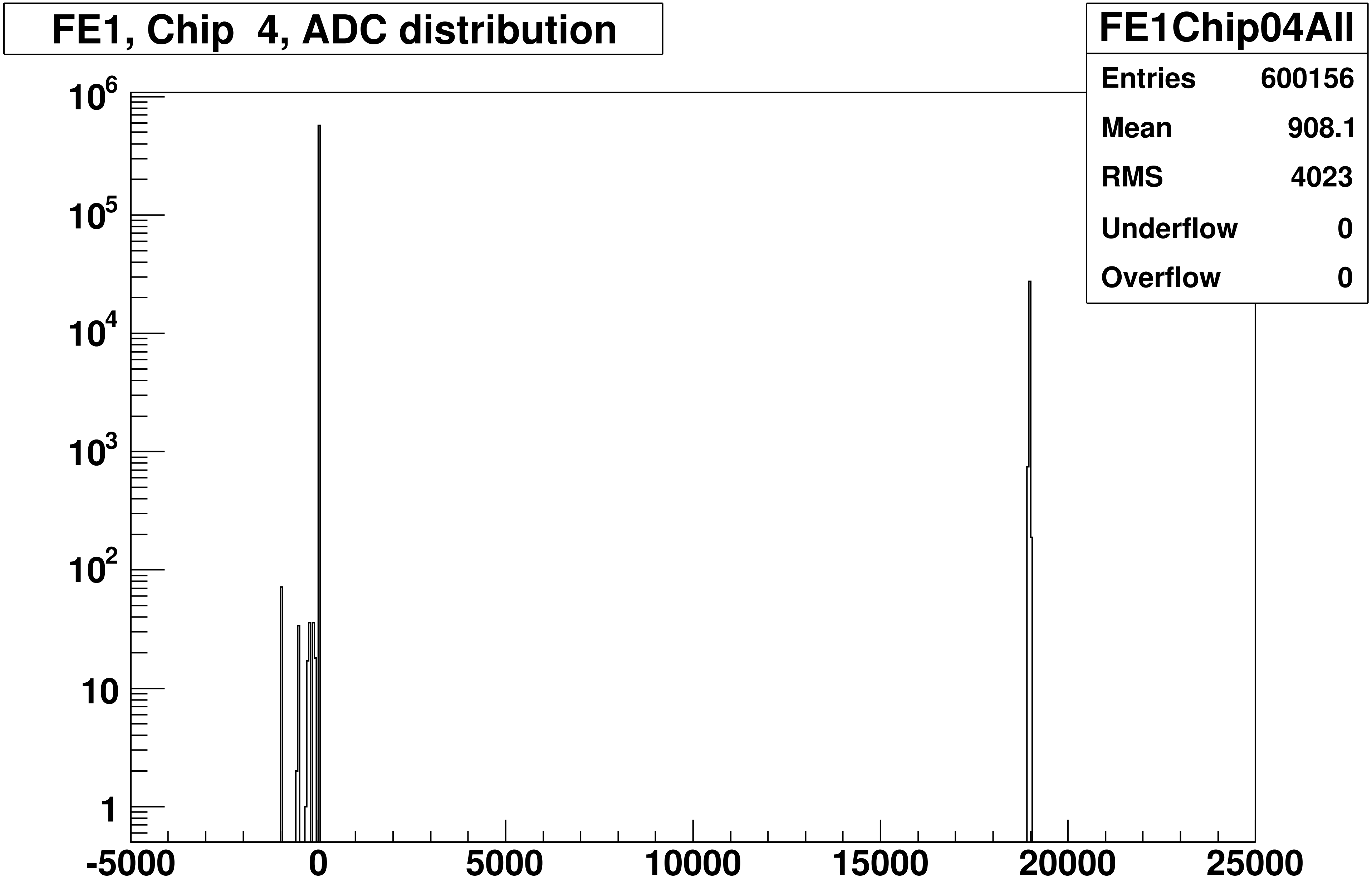
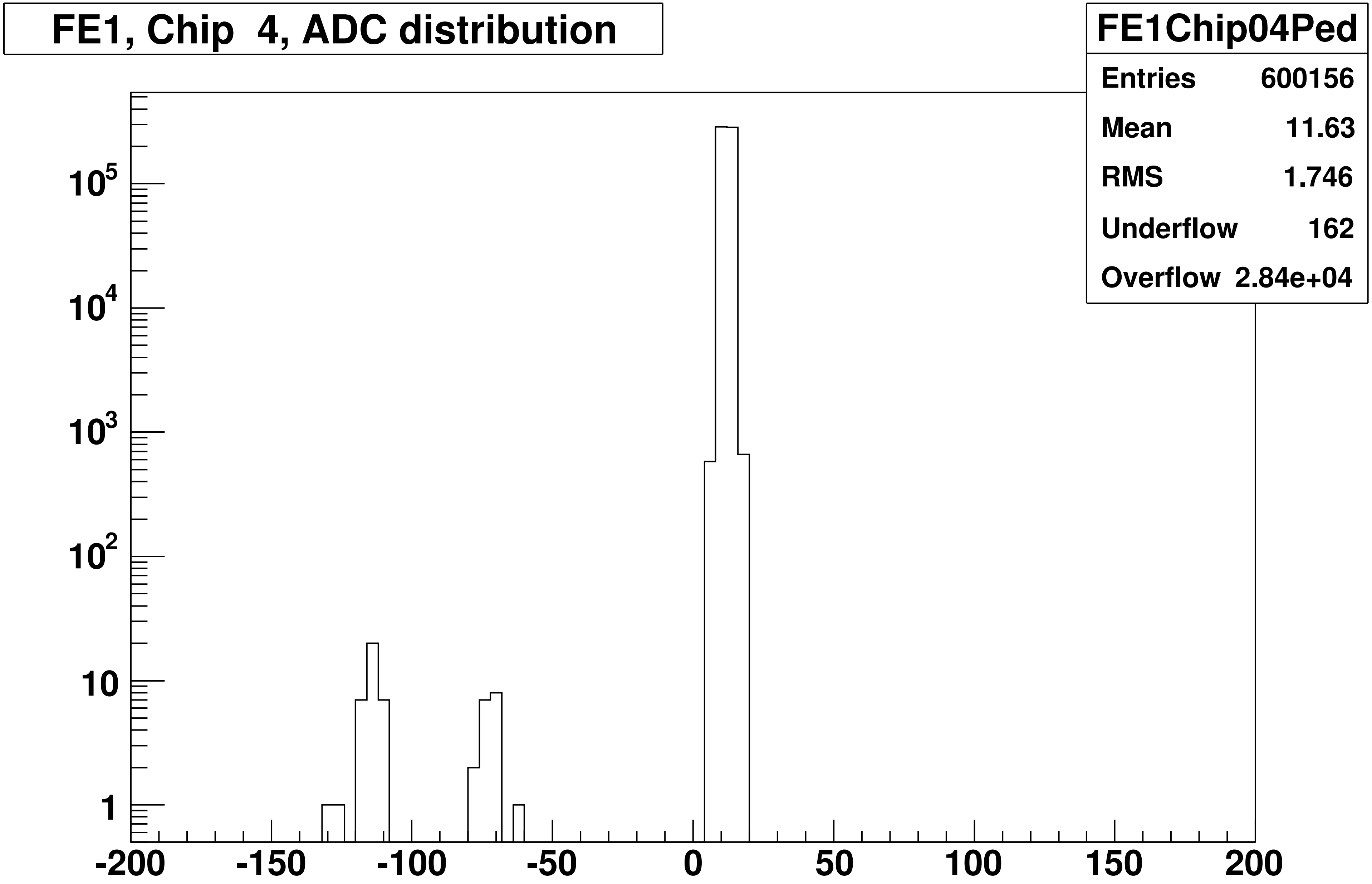
0
50
100
150
200

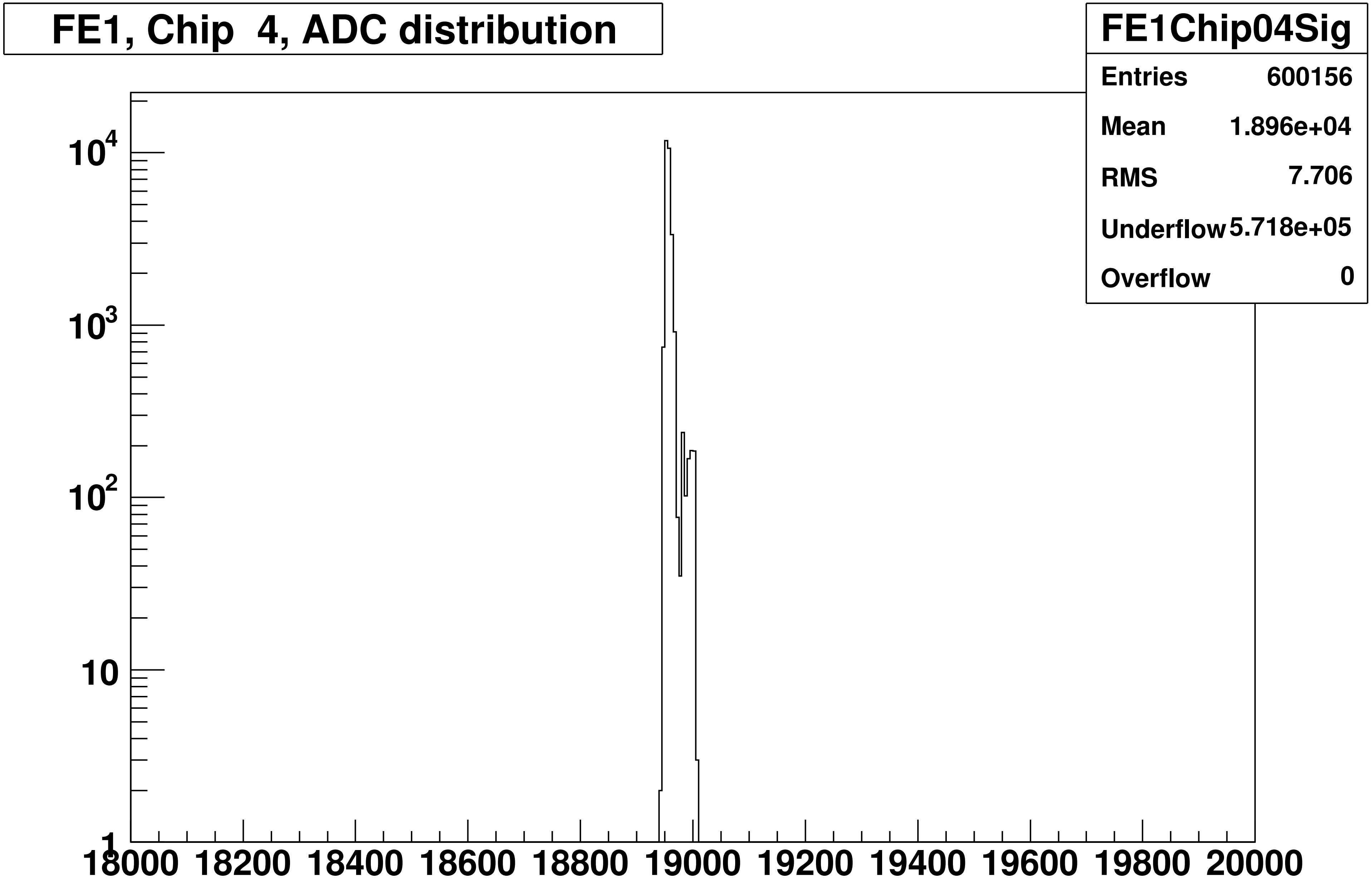


FE1, Chip 3, ADC distribution
FE1Chip03Sig
Entries 600156
Mean 1.888e+04
RMS 7.352
Underflow 5.717e+05
Overflow 0
10^4
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000

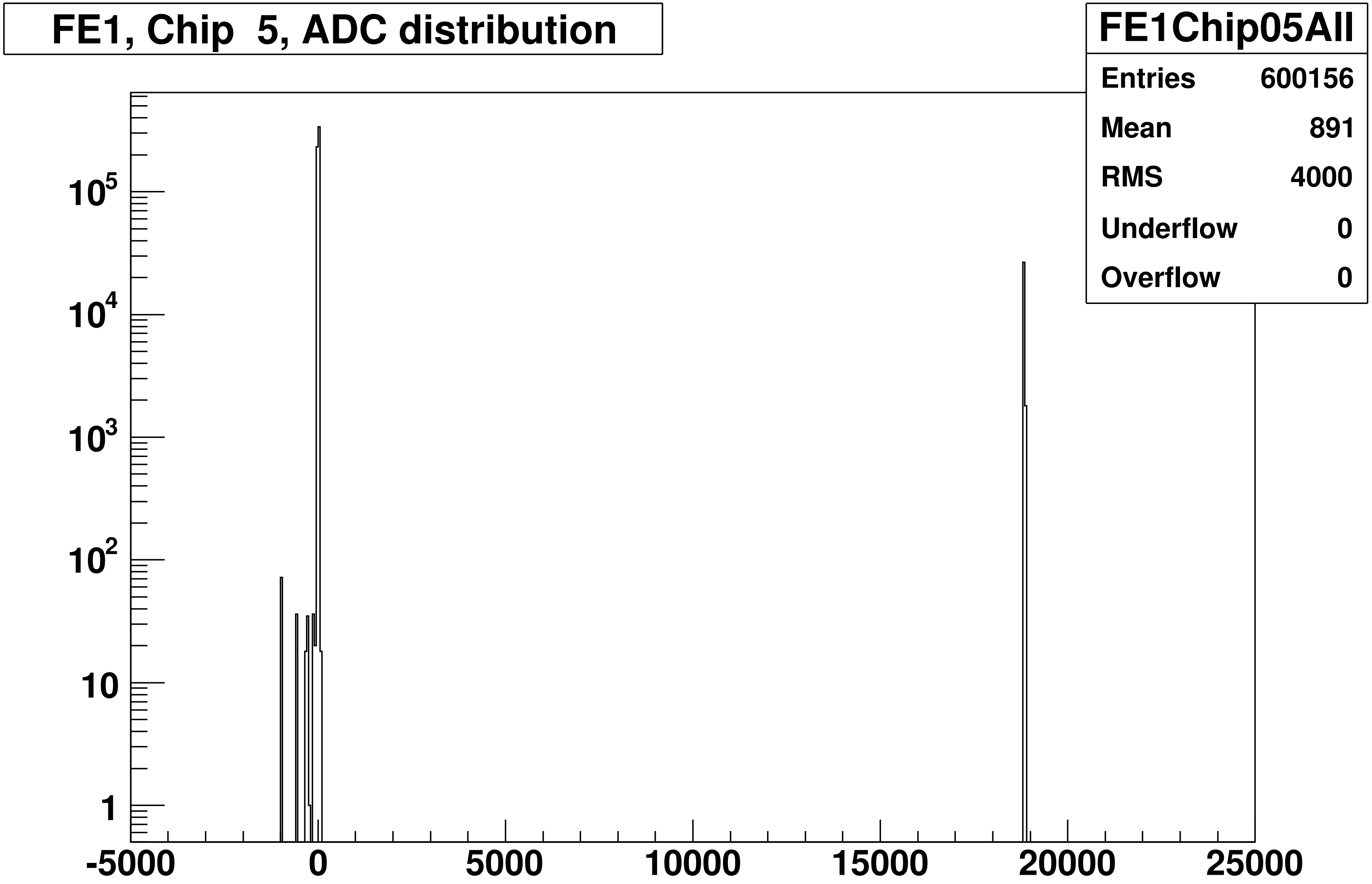

FE1, Chip 4, ADC distribution
FE1Chip04All
Entries 600156
Mean 908.1
RMS 4023
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



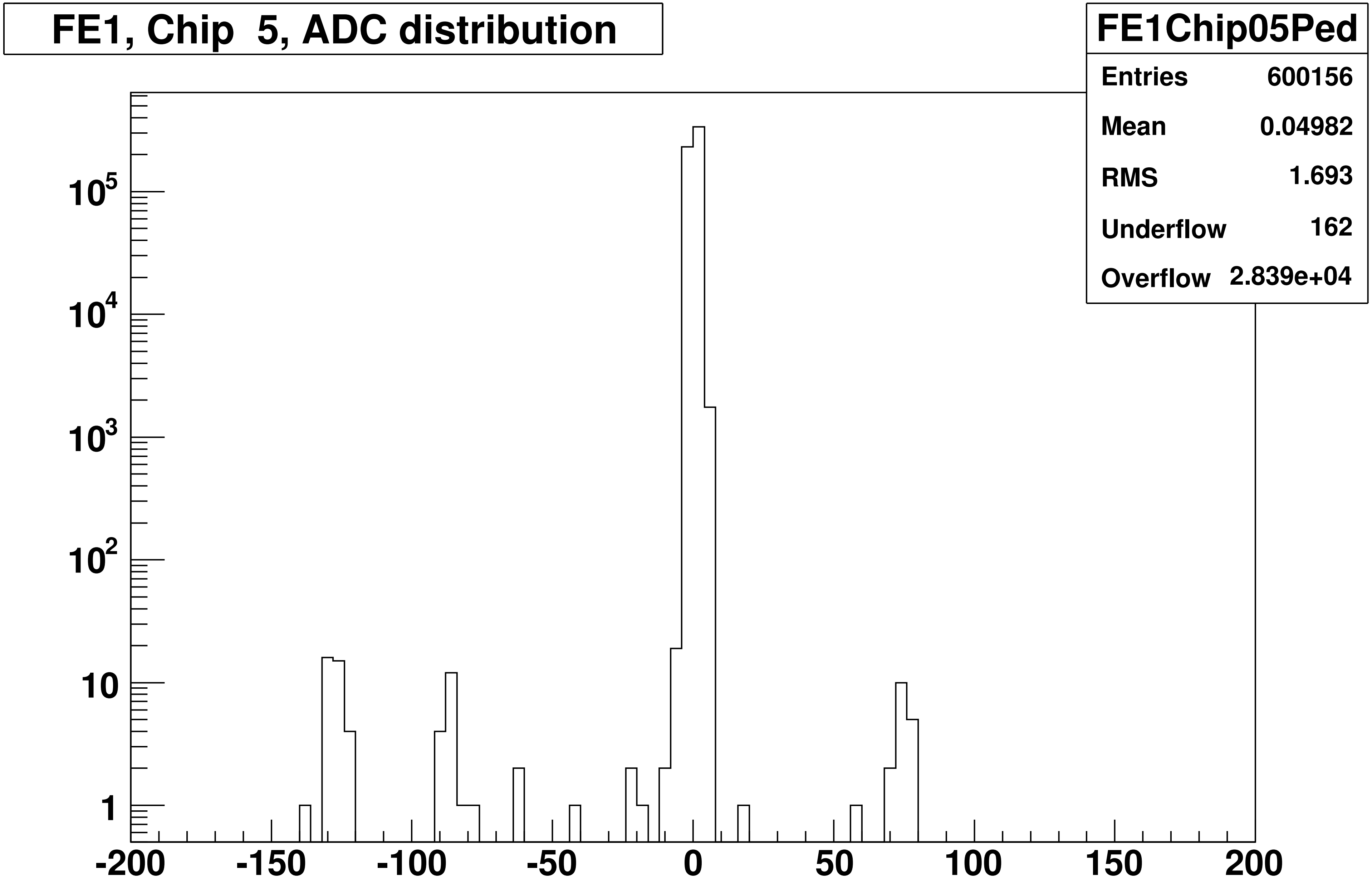
FE1, Chip 4, ADC distribution
FE1Chip04Ped
Entries 600156
Mean 11.63
RMS 1.746
Underflow 162
Overflow 2.84e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
200

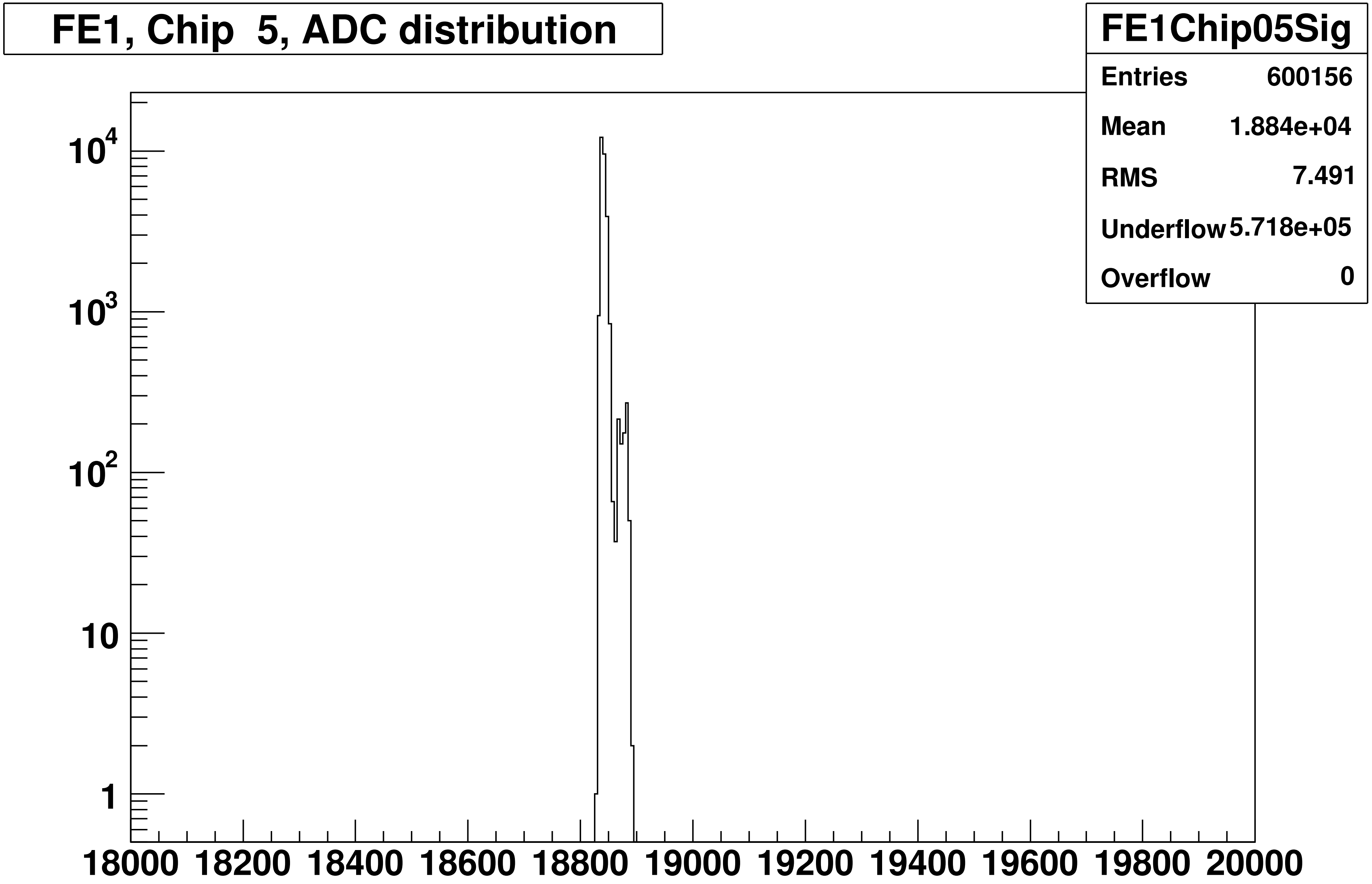


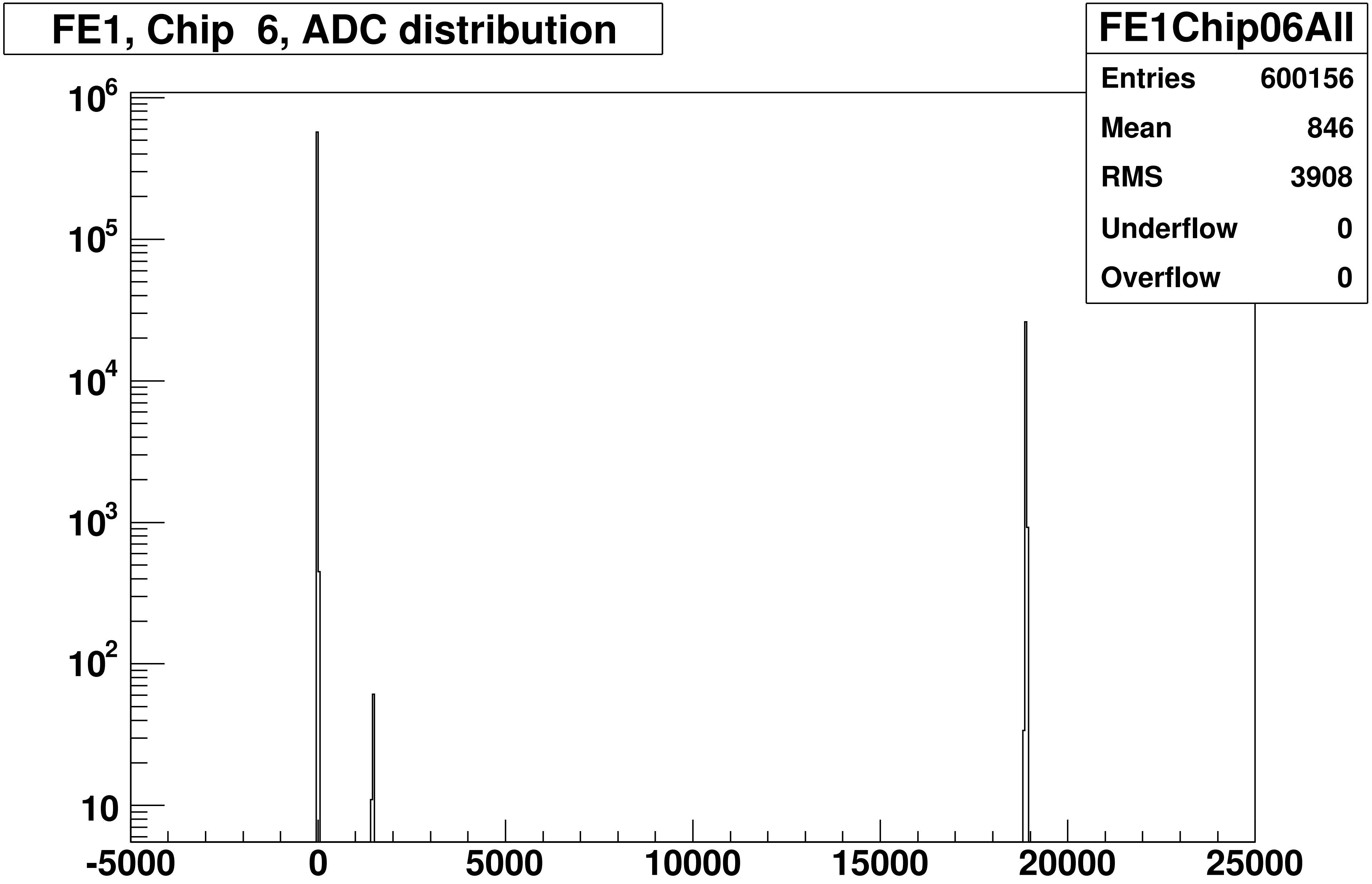
FE1, Chip 4, ADC distribution
FE1Chip04Sig
Entries 600156
Mean 1.896e+04
RMS 7.706
Underflow 5.718e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000



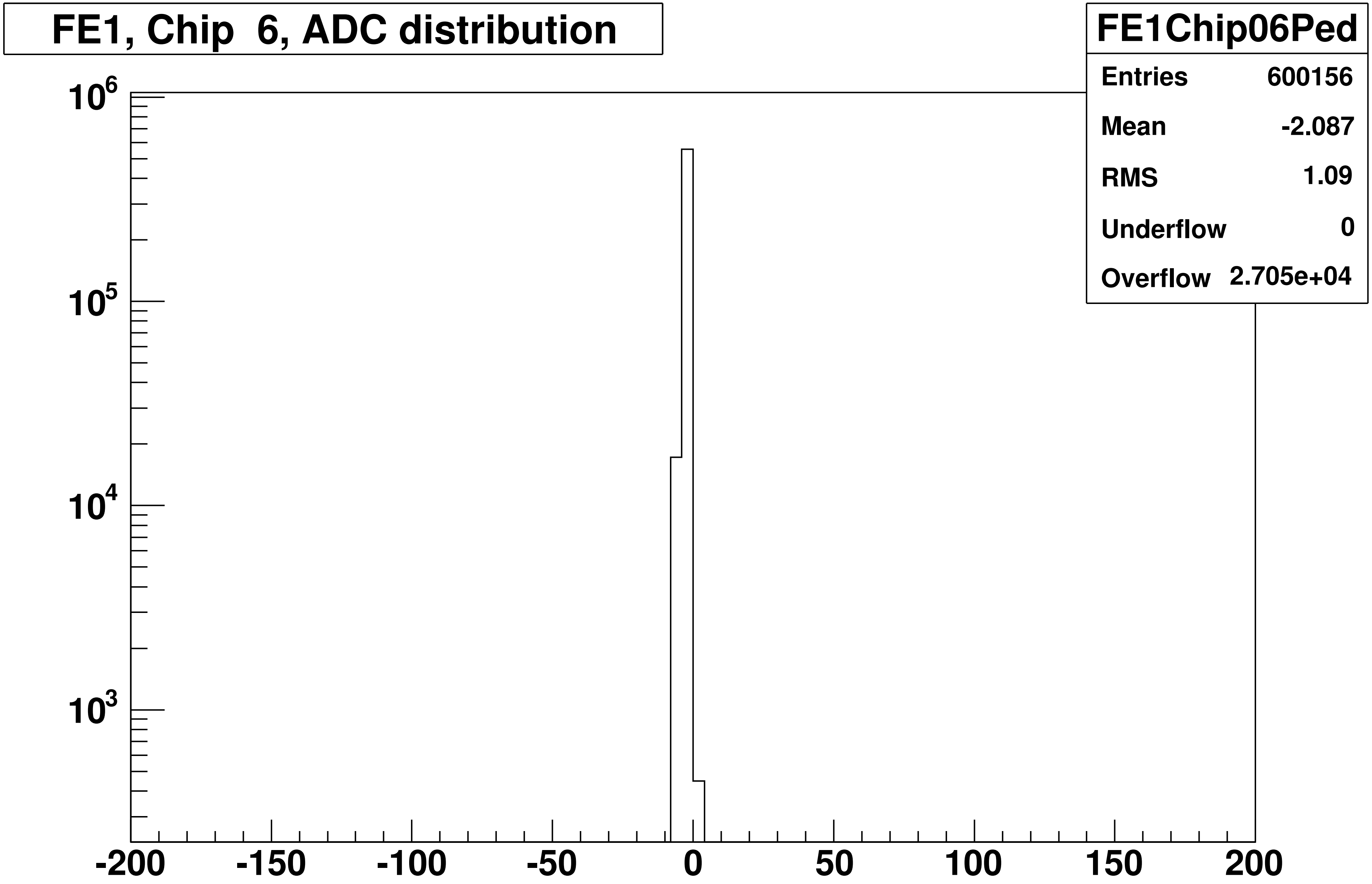
FE1, Chip 5, ADC distribution
FE1Chip05All
Entries 600156
Mean 891
RMS 4000
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000

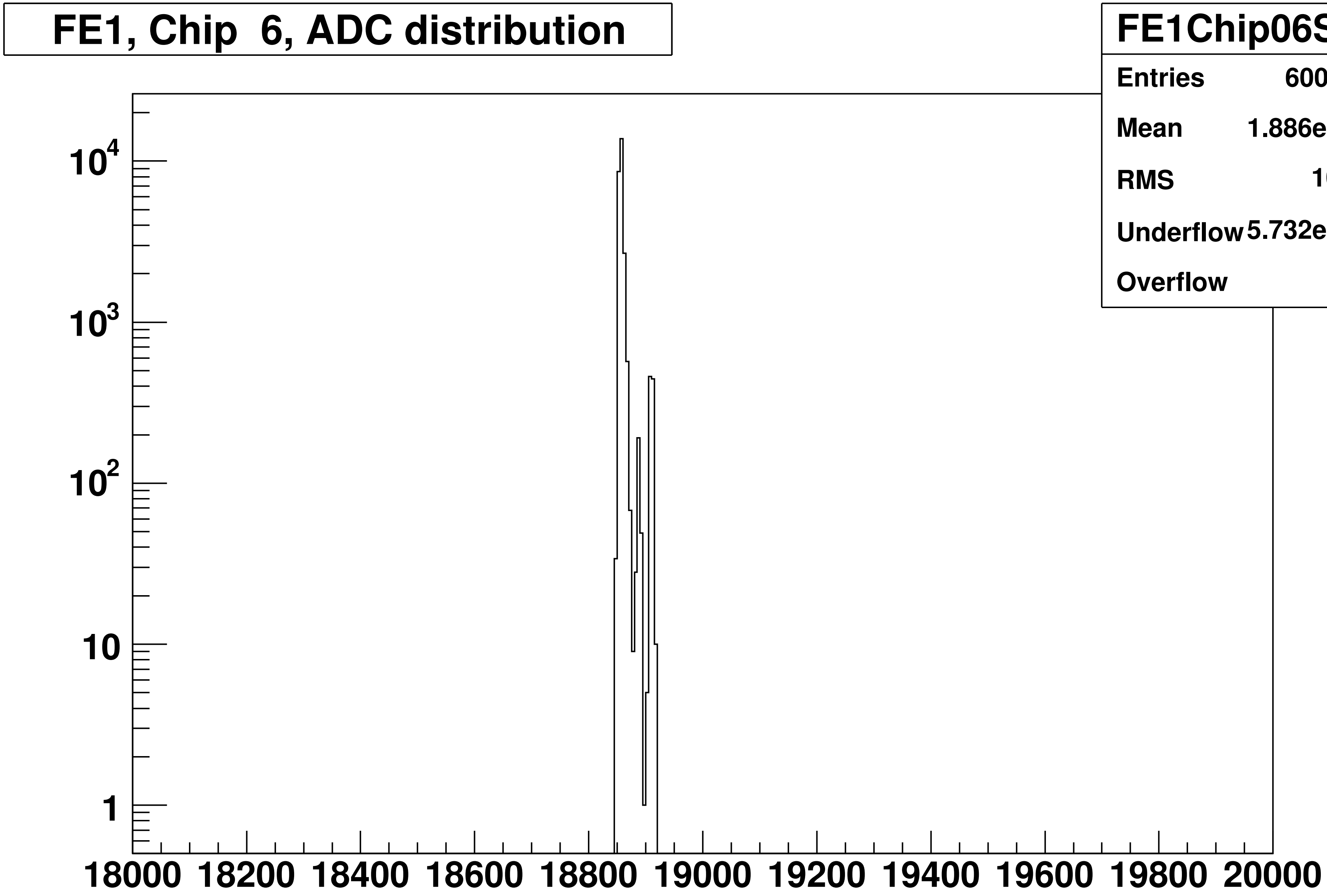

FE1, Chip 5, ADC distribution
FE1Chip05Ped
Entries 600156
Mean 0.04982
RMS 1.693
Underflow 162
Overflow 2.839e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
200

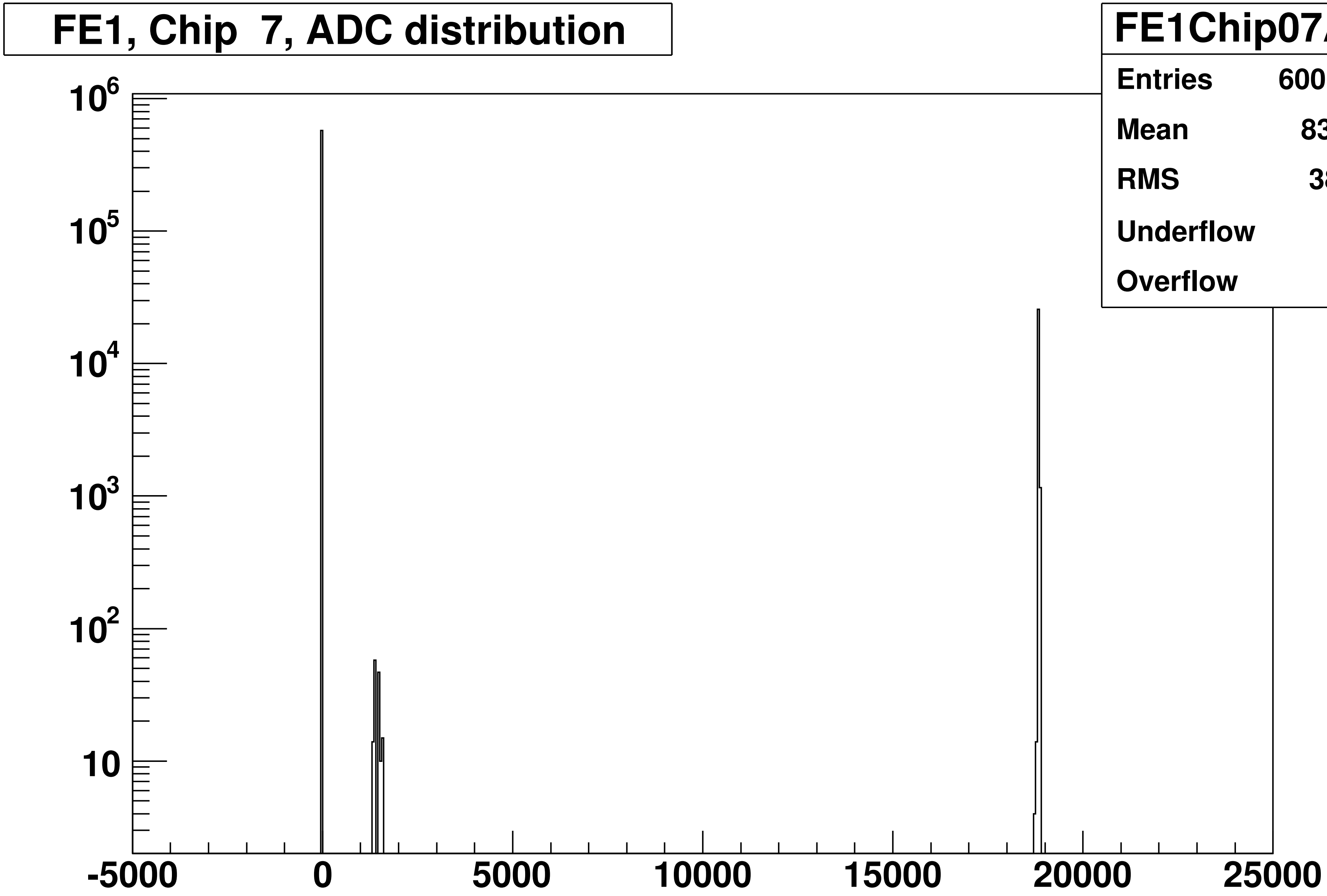

FE1, Chip 5, ADC distribution
FE1Chip05Sig
Entries 600156
Mean 1.884e+04
RMS 7.491
Underflow 5.718e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



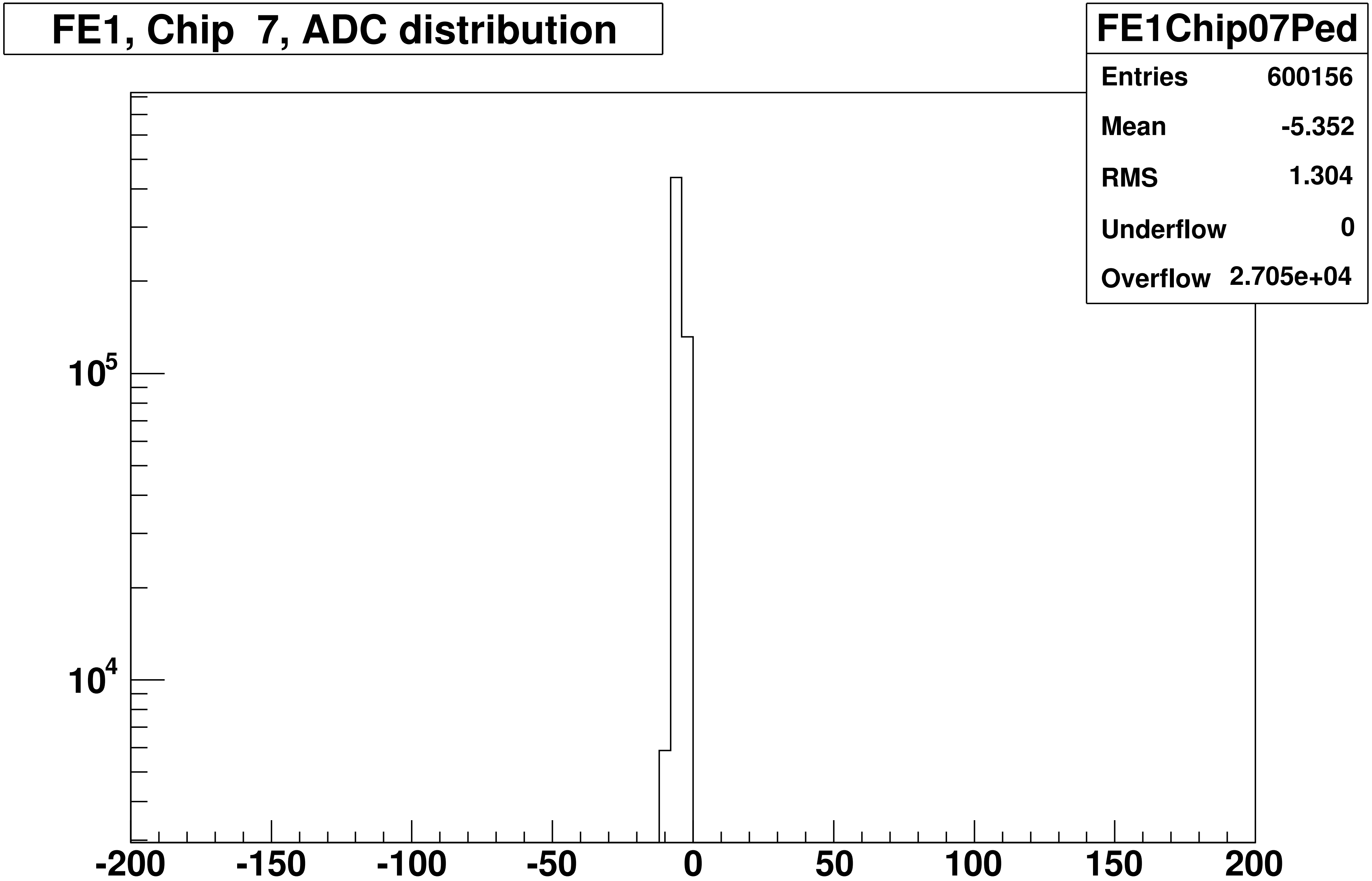
FE1, Chip 6, ADC distribution
FE1Chip06All
Entries 600156
Mean 846
RMS 3908
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000

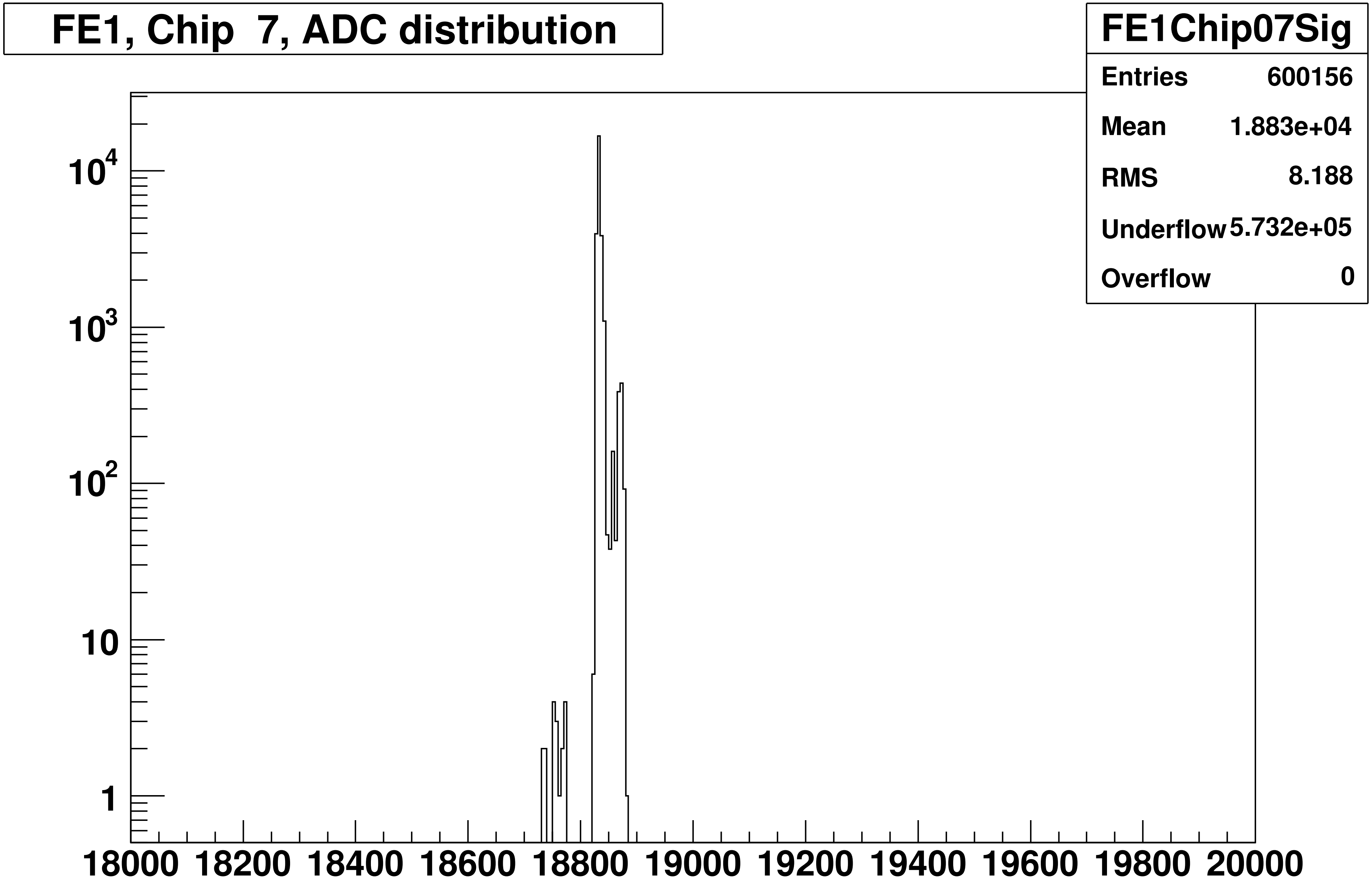

FE1, Chip 6, ADC distribution
FE1Chip06Ped
Entries 600156
Mean -2.087
RMS 1.09
Underflow 0
Overflow 2.705e+04
10^6
10^5
10^4
10^3
-200 -150 -100 -50 0 50 100 150 200


FE1, Chip 6, ADC distribution
FE1Chip06Sig
Entries 600156
Mean 1.886e+04
RMS 10.61
Underflow 5.732e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000

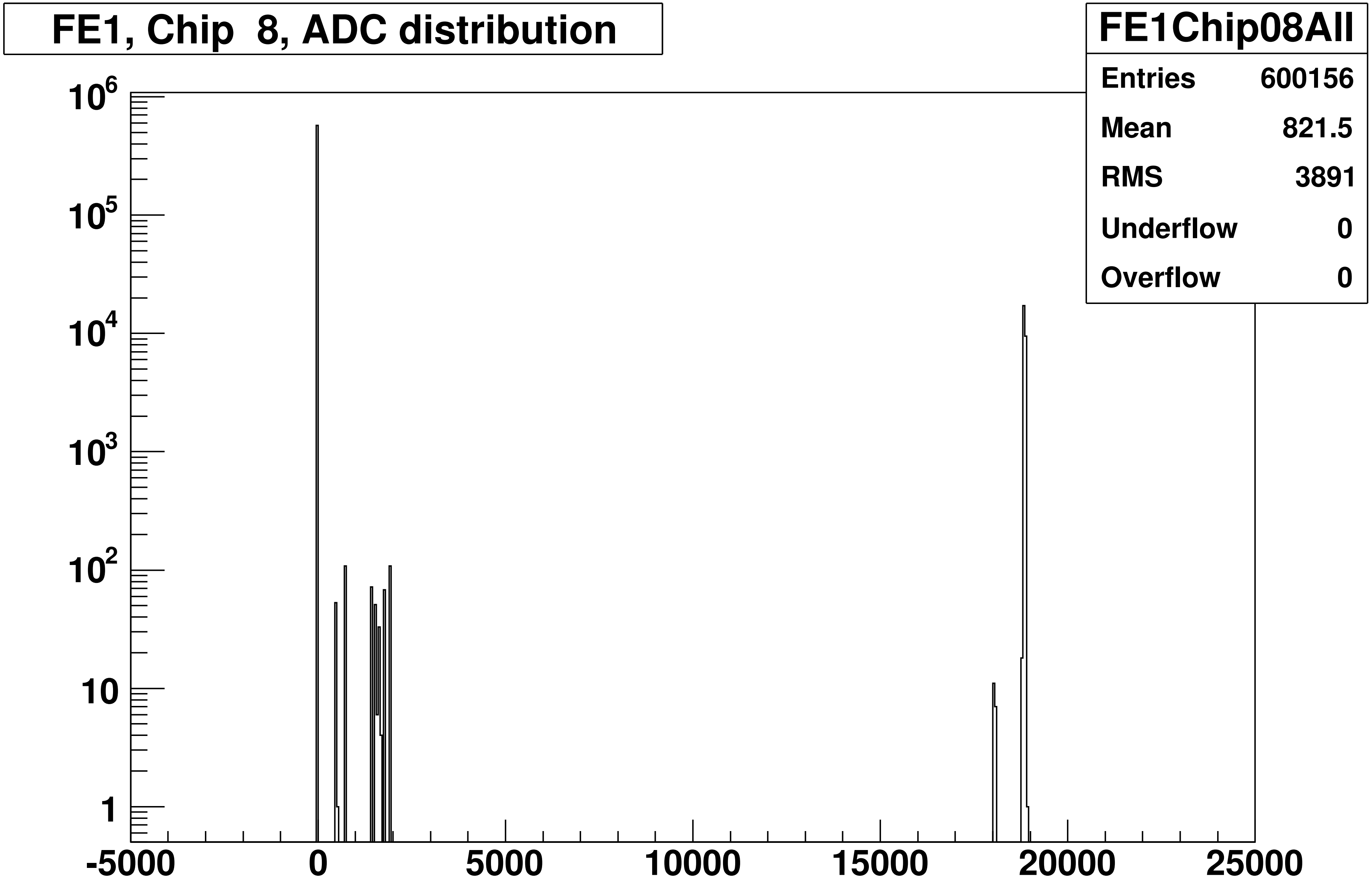


FE1, Chip 7, ADC distribution
FE1Chip07All
Entries 600156
Mean 839.7
RMS 3899
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000

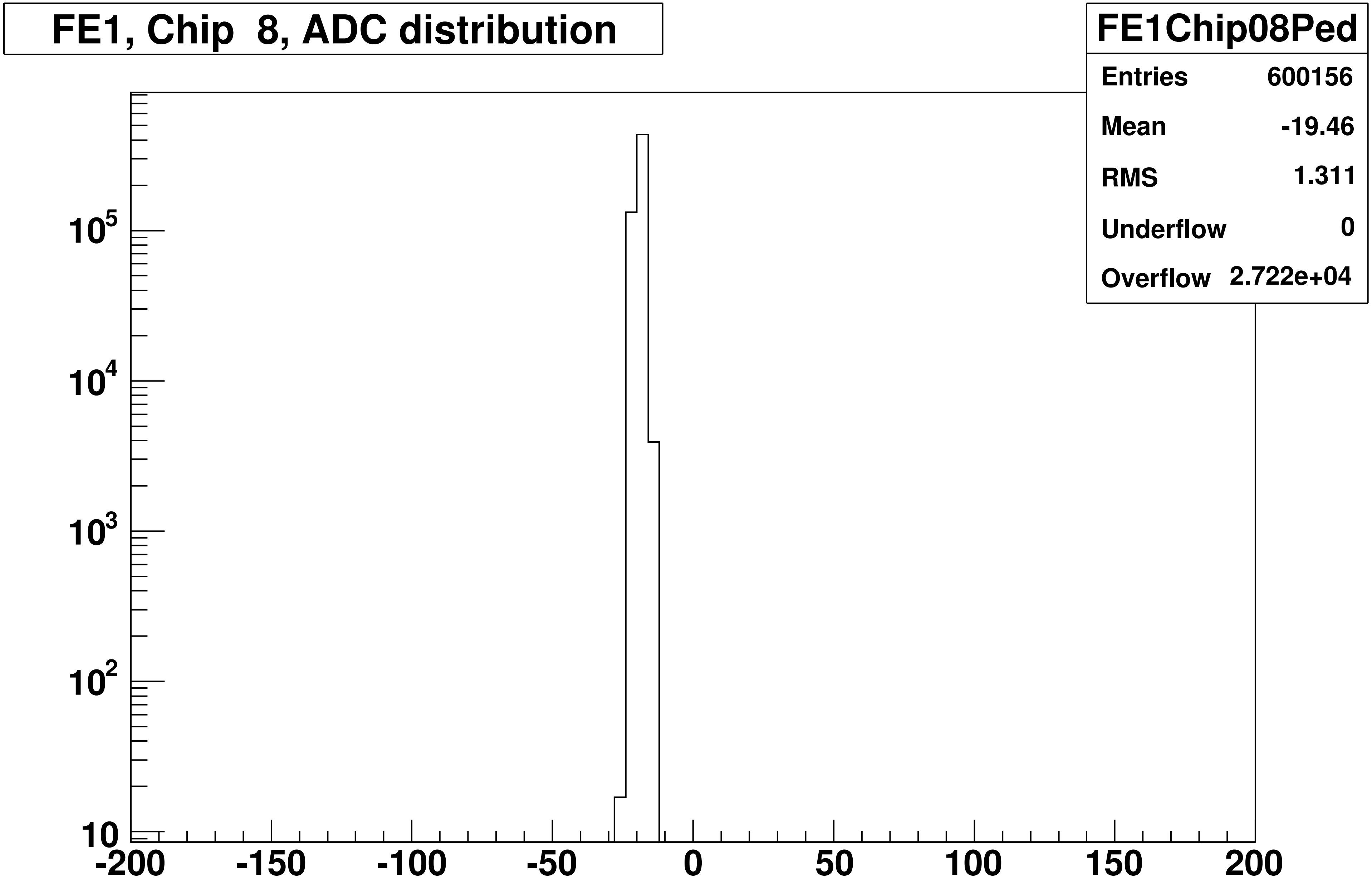

FE1, Chip 7, ADC distribution
FE1Chip07Ped
Entries 600156
Mean -5.352
RMS 1.304
Underflow 0
Overflow 2.705e+04
10^5
10^4
-200
-150
-100
-50
0
50
100
150
200

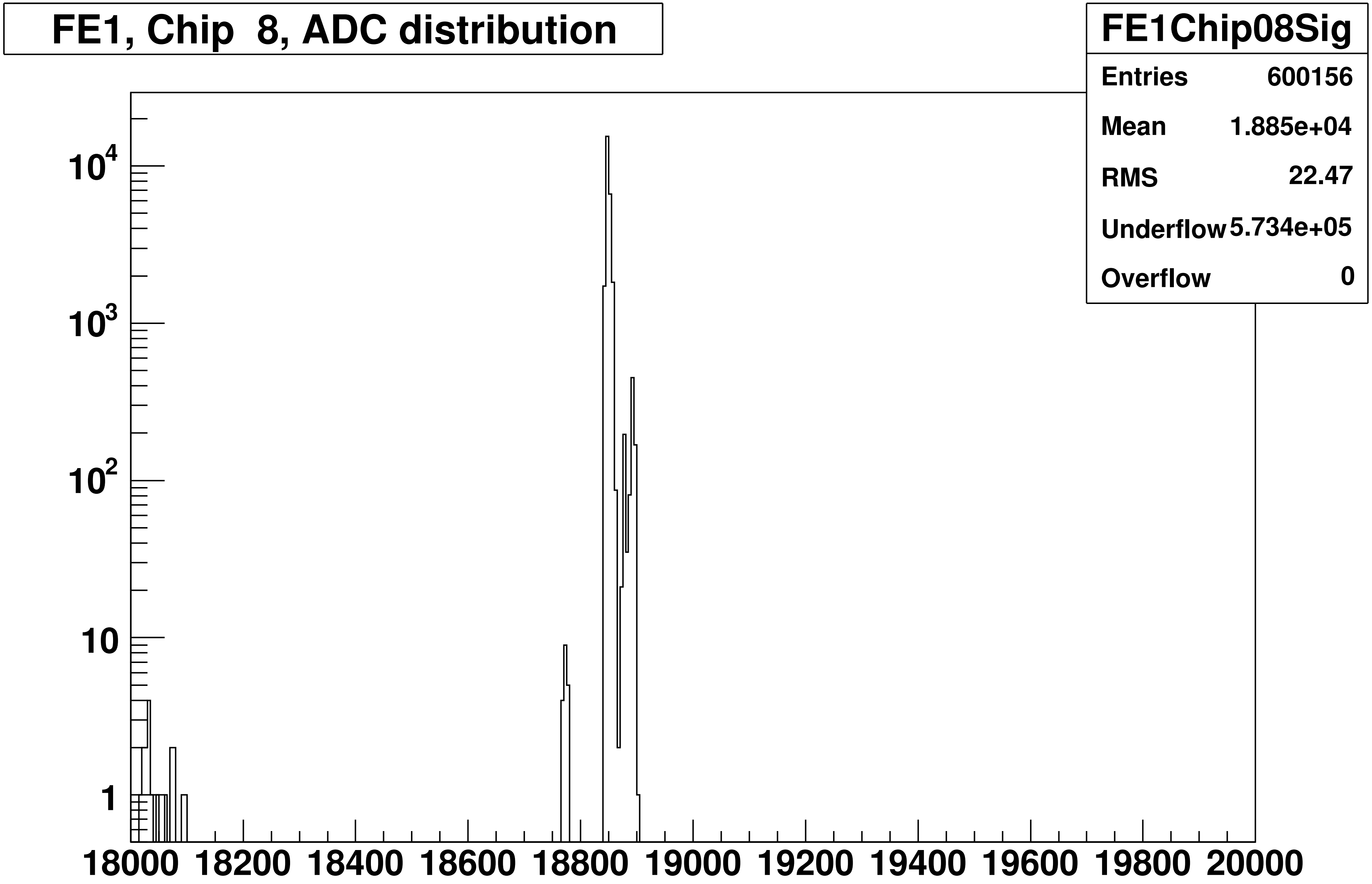


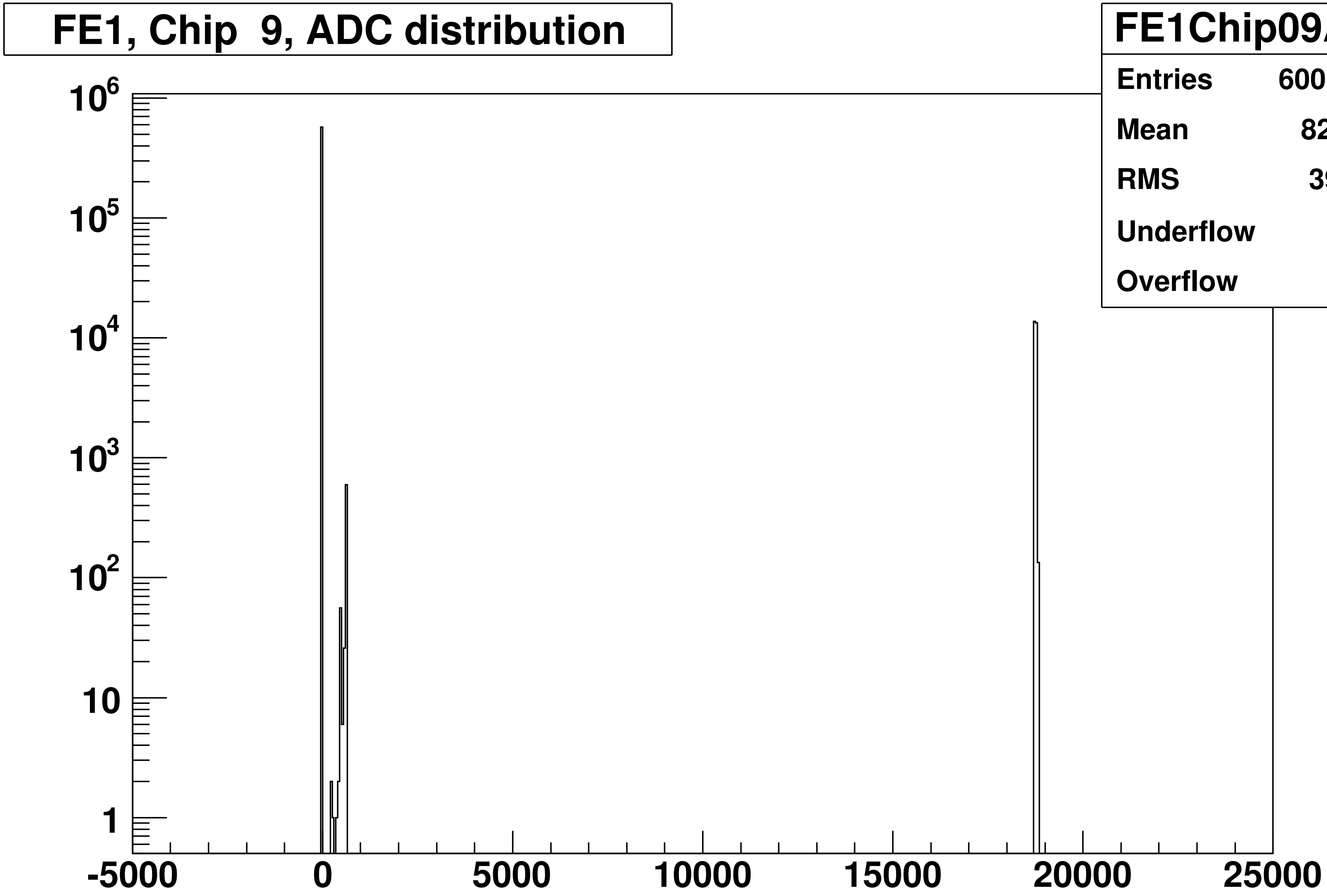
FE1, Chip 7, ADC distribution
FE1Chip07Sig
Entries 600156
Mean 1.883e+04
RMS 8.188
Underflow 5.732e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000

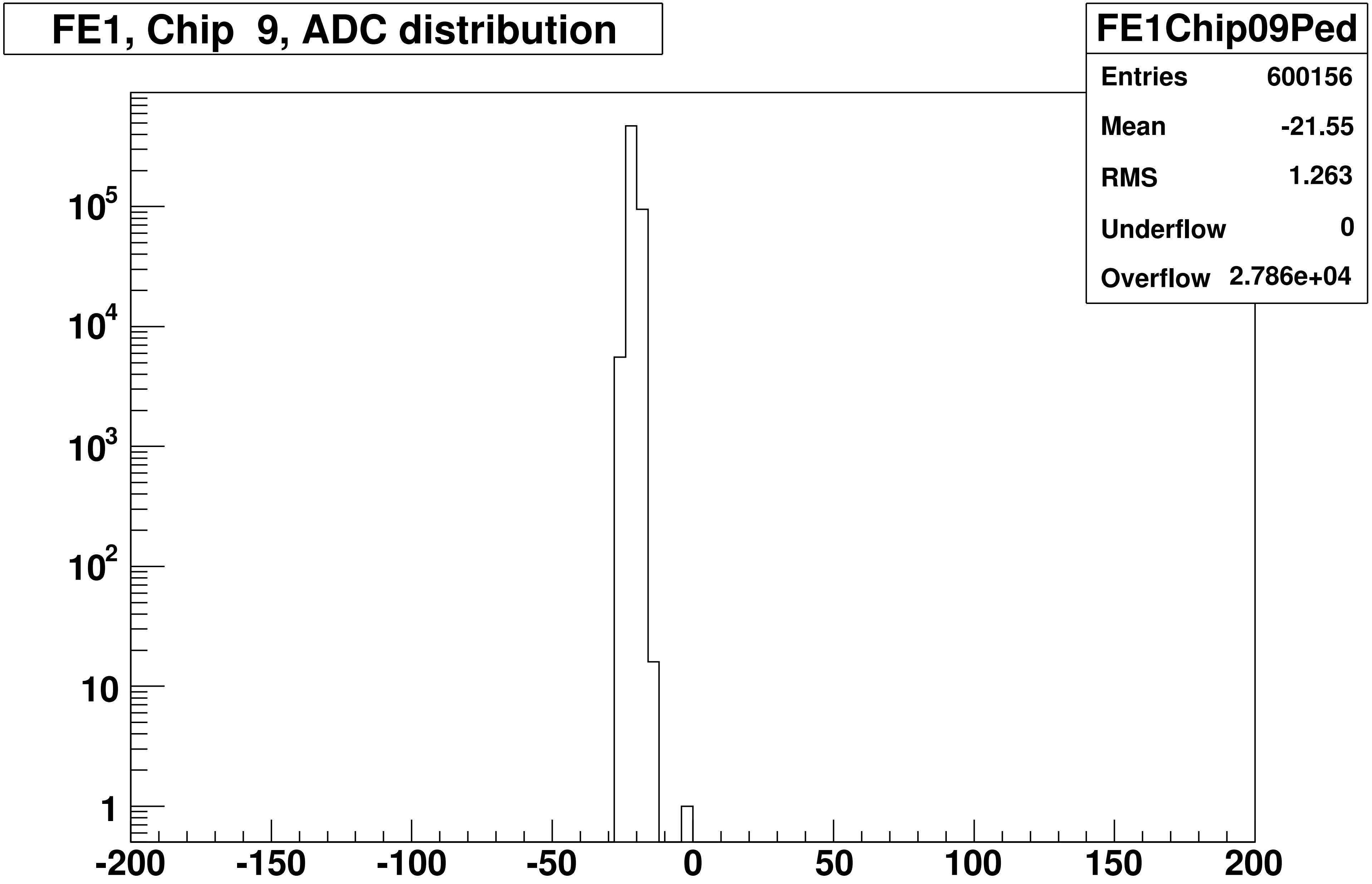


FE1, Chip 8, ADC distribution
FE1Chip08All
Entries 600156
Mean 821.5
RMS 3891
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000

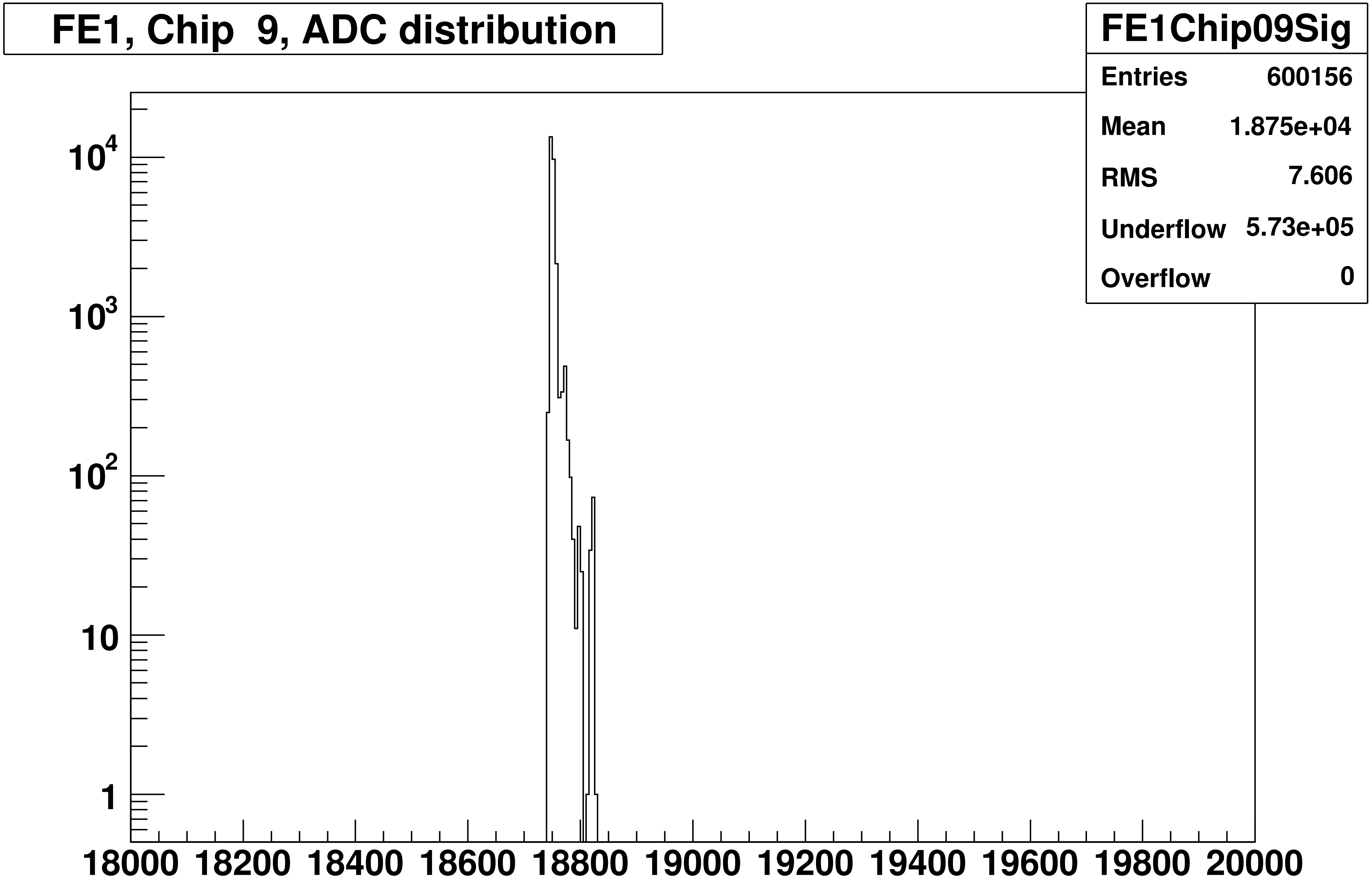

FE1, Chip 8, ADC distribution
FE1Chip08Ped
Entries 600156
Mean -19.46
RMS 1.311
Underflow 0
Overflow 2.722e+04
10
10^2
10^3
10^4
10^5
-200
-150
-100
-50
0
50
100
150
200

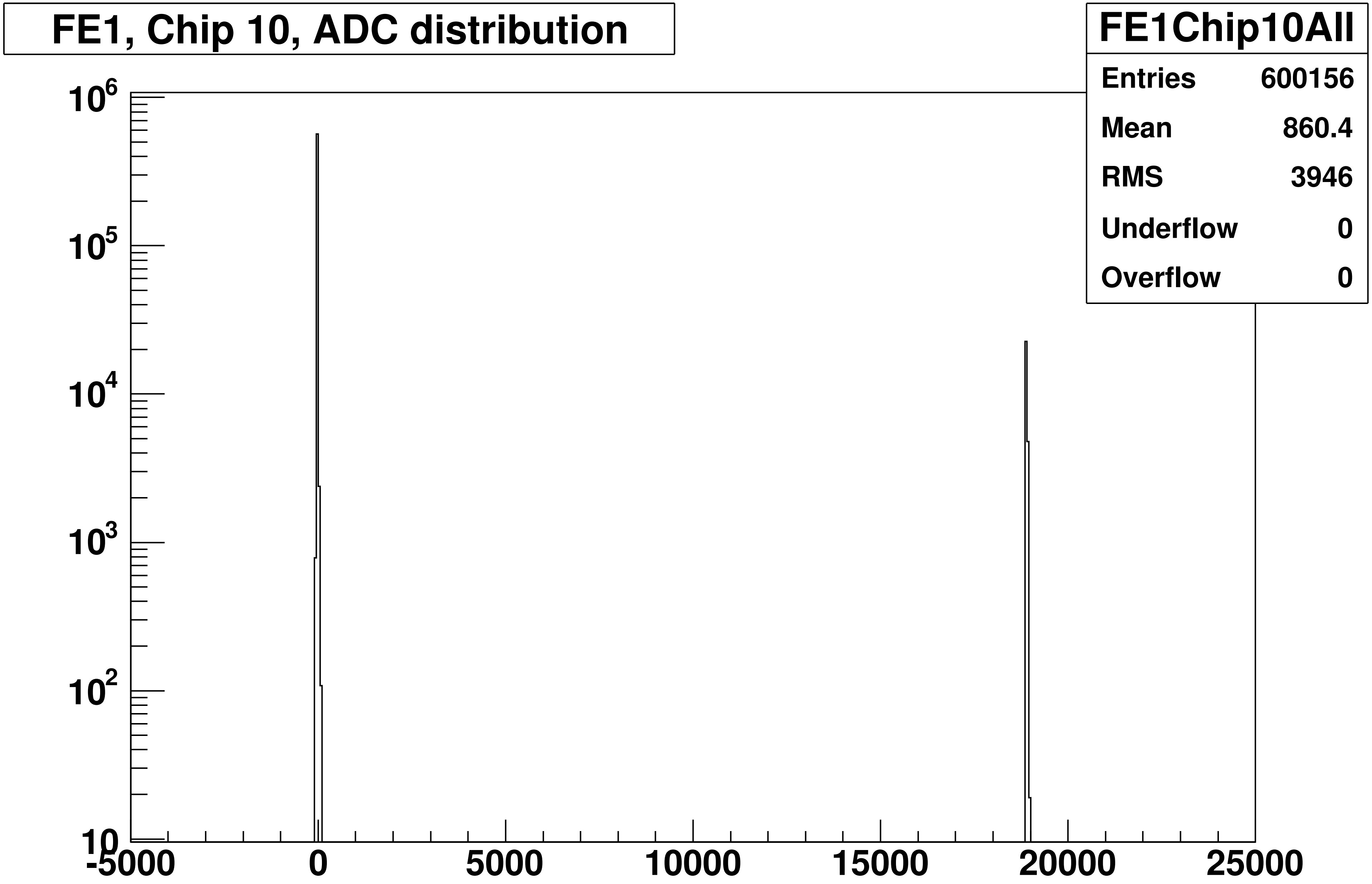

FE1, Chip 8, ADC distribution
FE1Chip08Sig
Entries 600156
Mean 1.885e+04
RMS 22.47
Underflow 5.734e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE1, Chip 9, ADC distribution
FE1Chip09All
Entries 600156
Mean 828.8
RMS 3902
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE1, Chip 9, ADC distribution
FE1Chip09Ped
Entries 600156
Mean -21.55
RMS 1.263
Underflow 0
Overflow 2.786e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
200


FE1, Chip 9, ADC distribution
FE1Chip09Sig
Entries 600156
Mean 1.875e+04
RMS 7.606
Underflow 5.73e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE1, Chip 10, ADC distribution
FE1Chip10All
Entries 600156
Mean 860.4
RMS 3946
Underflow 0
Overflow 0
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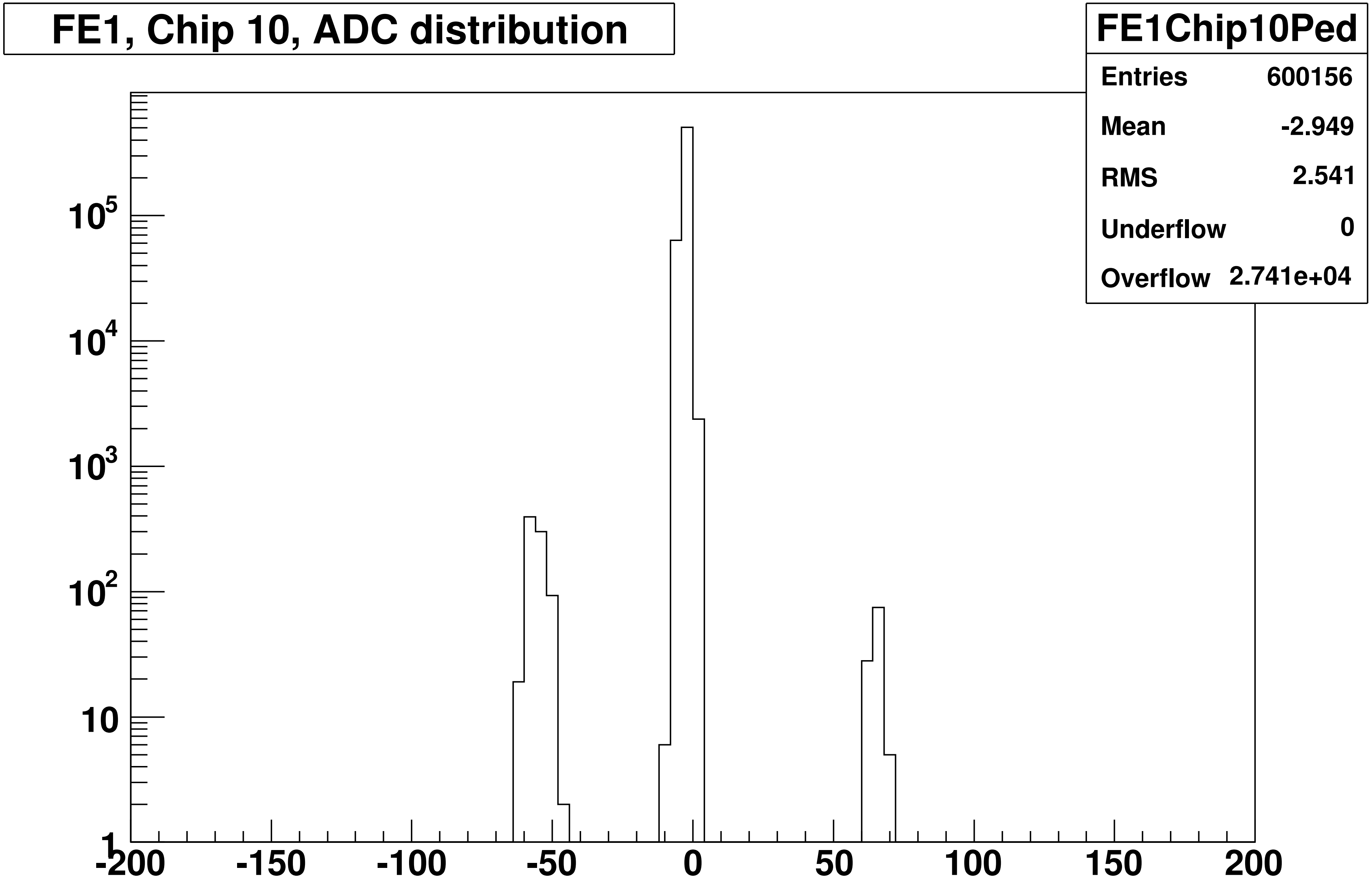
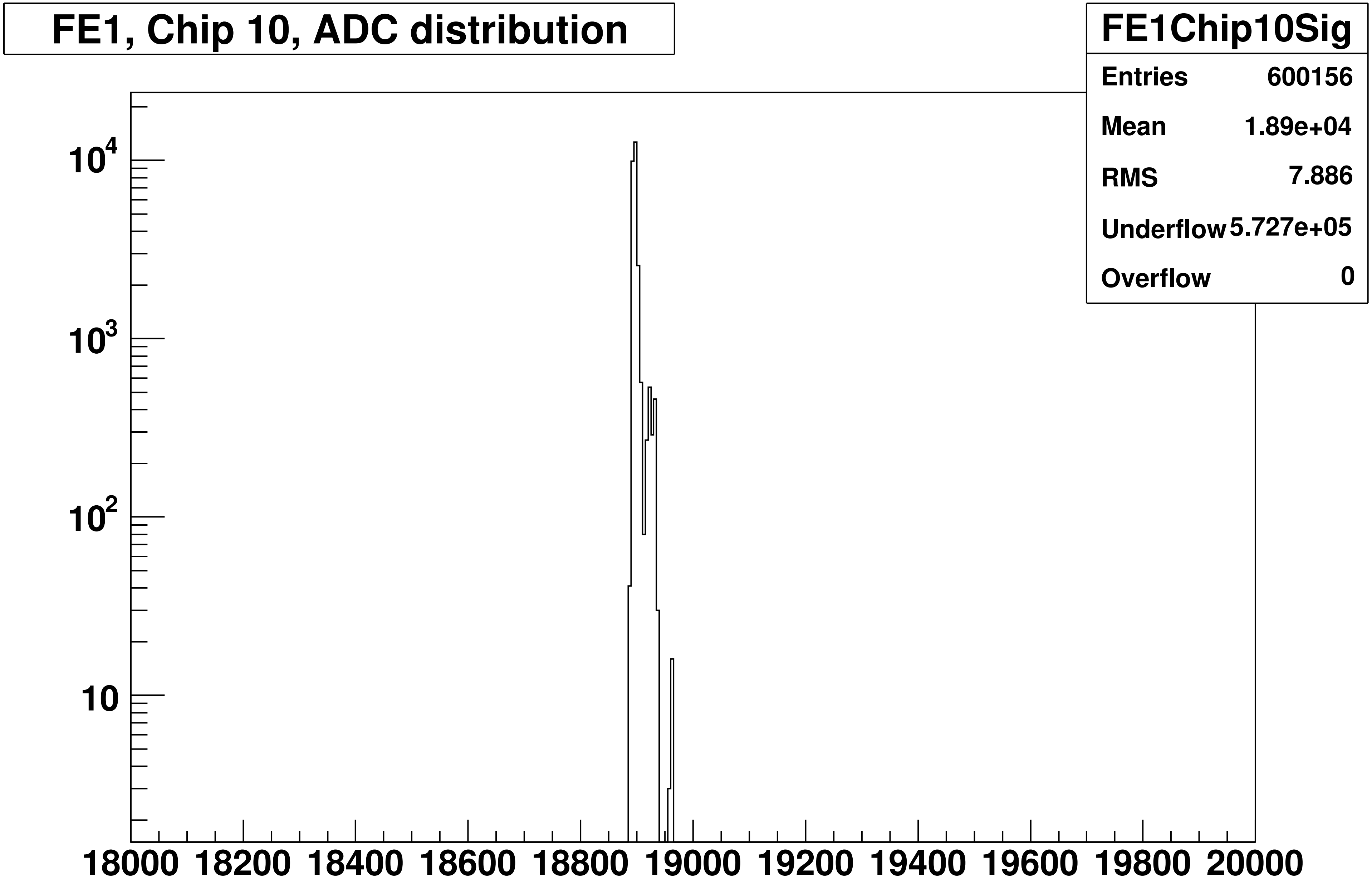
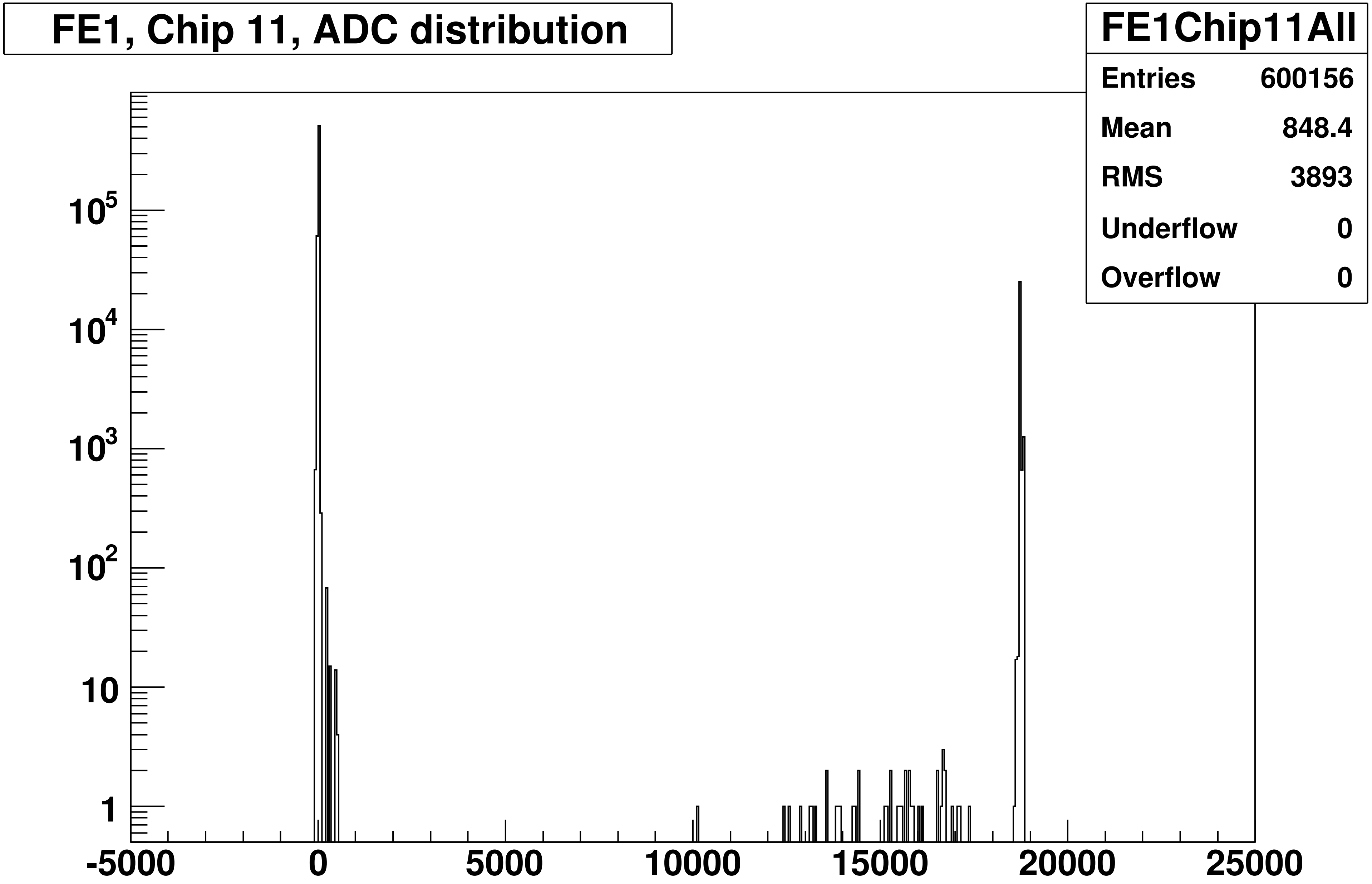
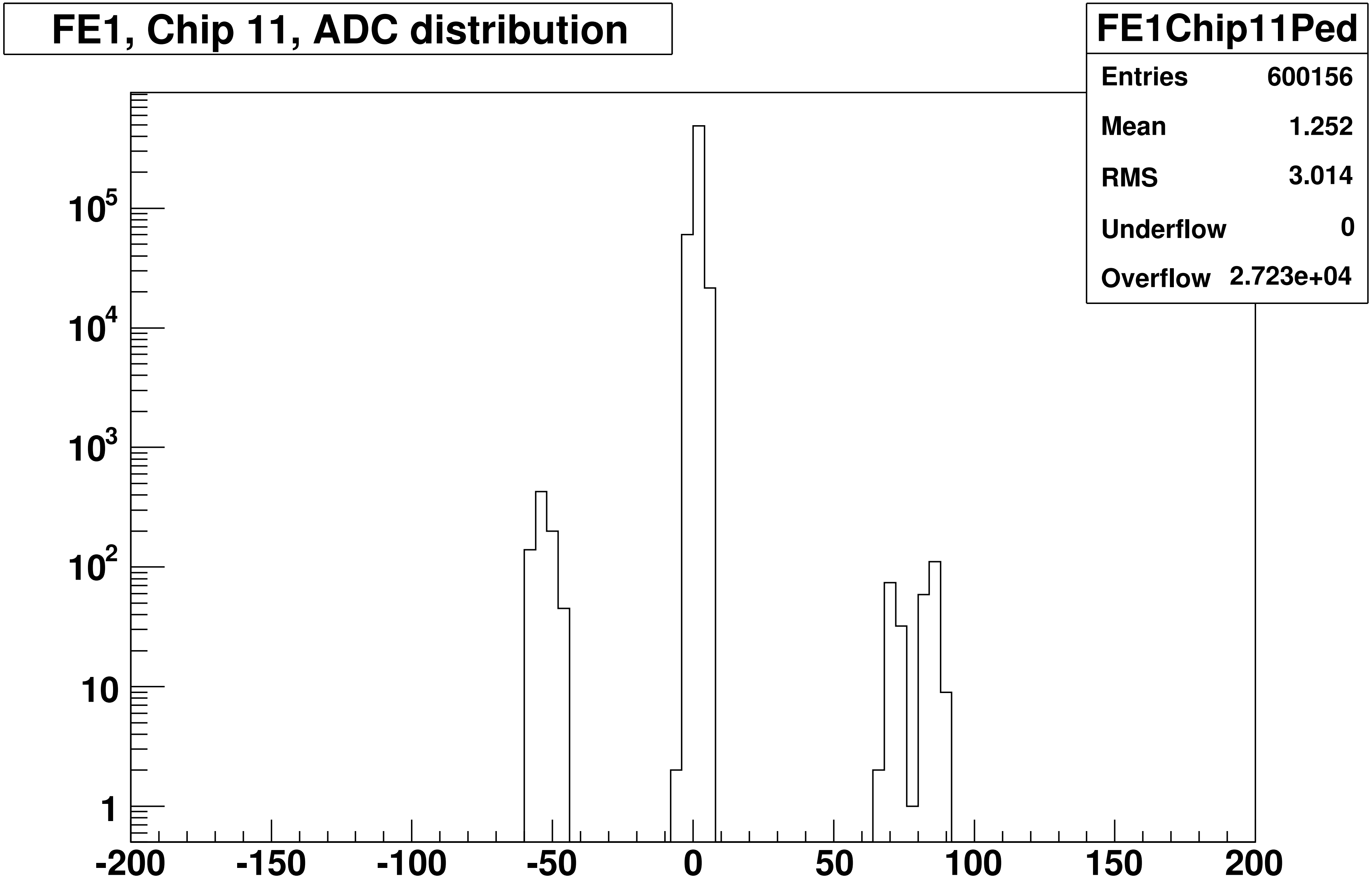
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE1, Chip 10, ADC distribution
FE1Chip10Ped
Entries 600156
Mean -2.949
RMS 2.541
Underflow 0
Overflow 2.741e+04
1
10
10^2
10^3
10^4
10^5
-200
-150
-100
-50
0
50
100
150
200

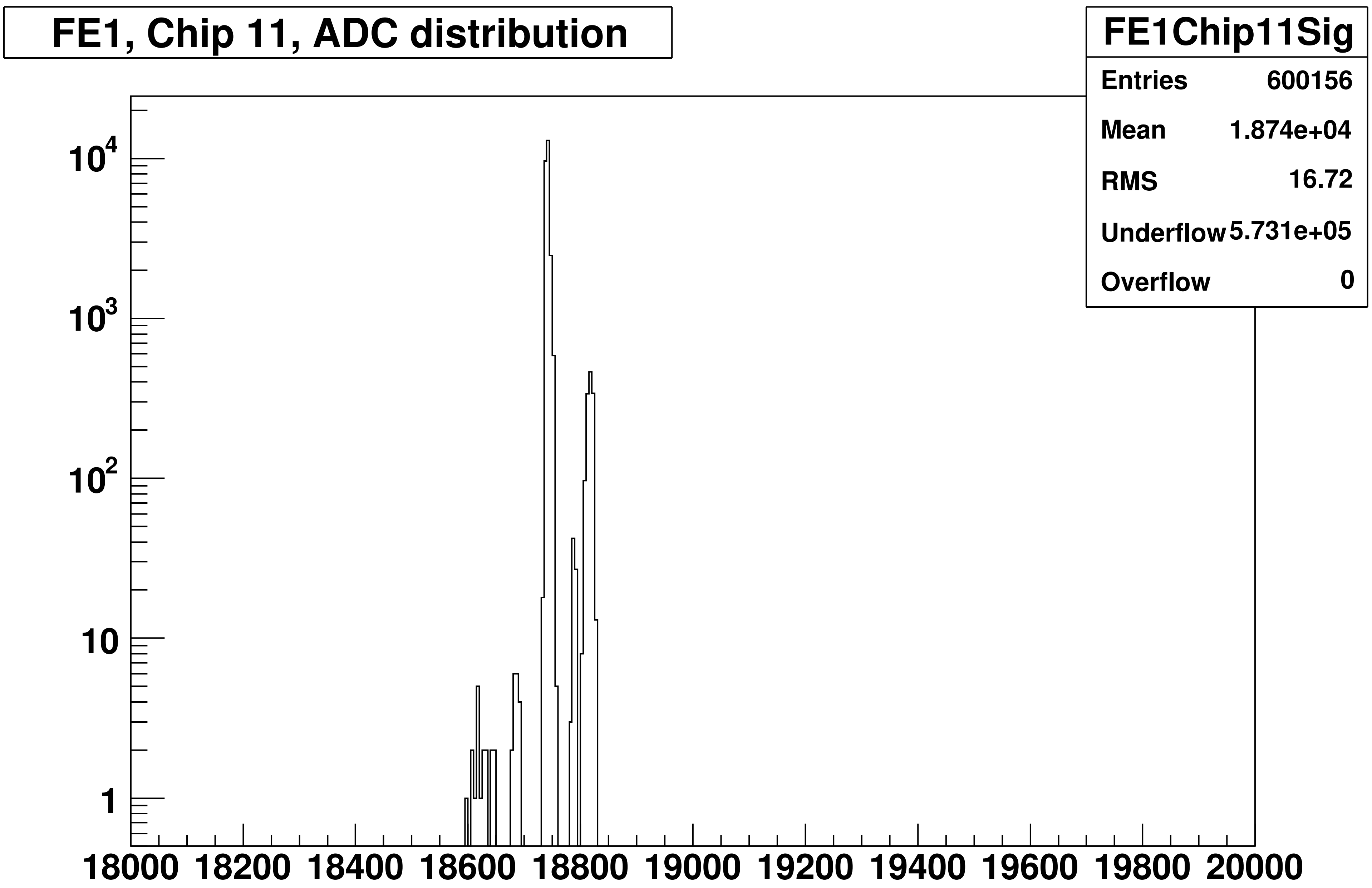


FE1, Chip 10, ADC distribution
FE1Chip10Sig
Entries 600156
Mean 1.89e+04
RMS 7.886
Underflow 5.727e+05
Overflow 0
10^4
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE1, Chip 11, ADC distribution
FE1Chip11All
Entries 600156
Mean 848.4
RMS 3893
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE1, Chip 11, ADC distribution
FE1Chip11Ped
Entries 600156
Mean 1.252
RMS 3.014
Underflow 0
Overflow 2.723e+04
1
10
10^2
10^3
10^4
10^5
-200
-150
-100
-50
0
50
100
150
200


FE1, Chip 11, ADC distribution
FE1Chip11Sig
Entries 600156
Mean 1.874e+04
RMS 16.72
Underflow 5.731e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
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19000
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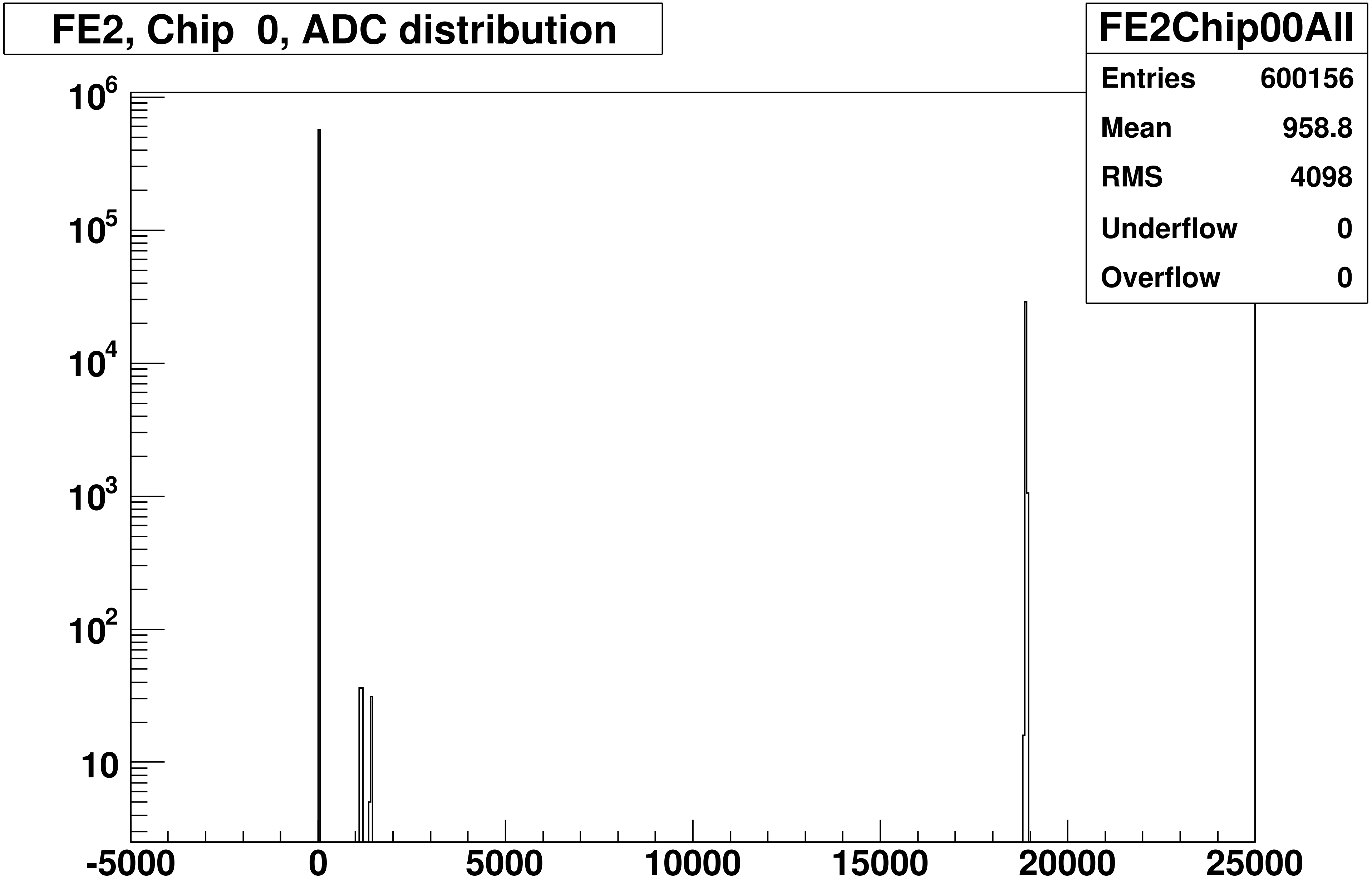
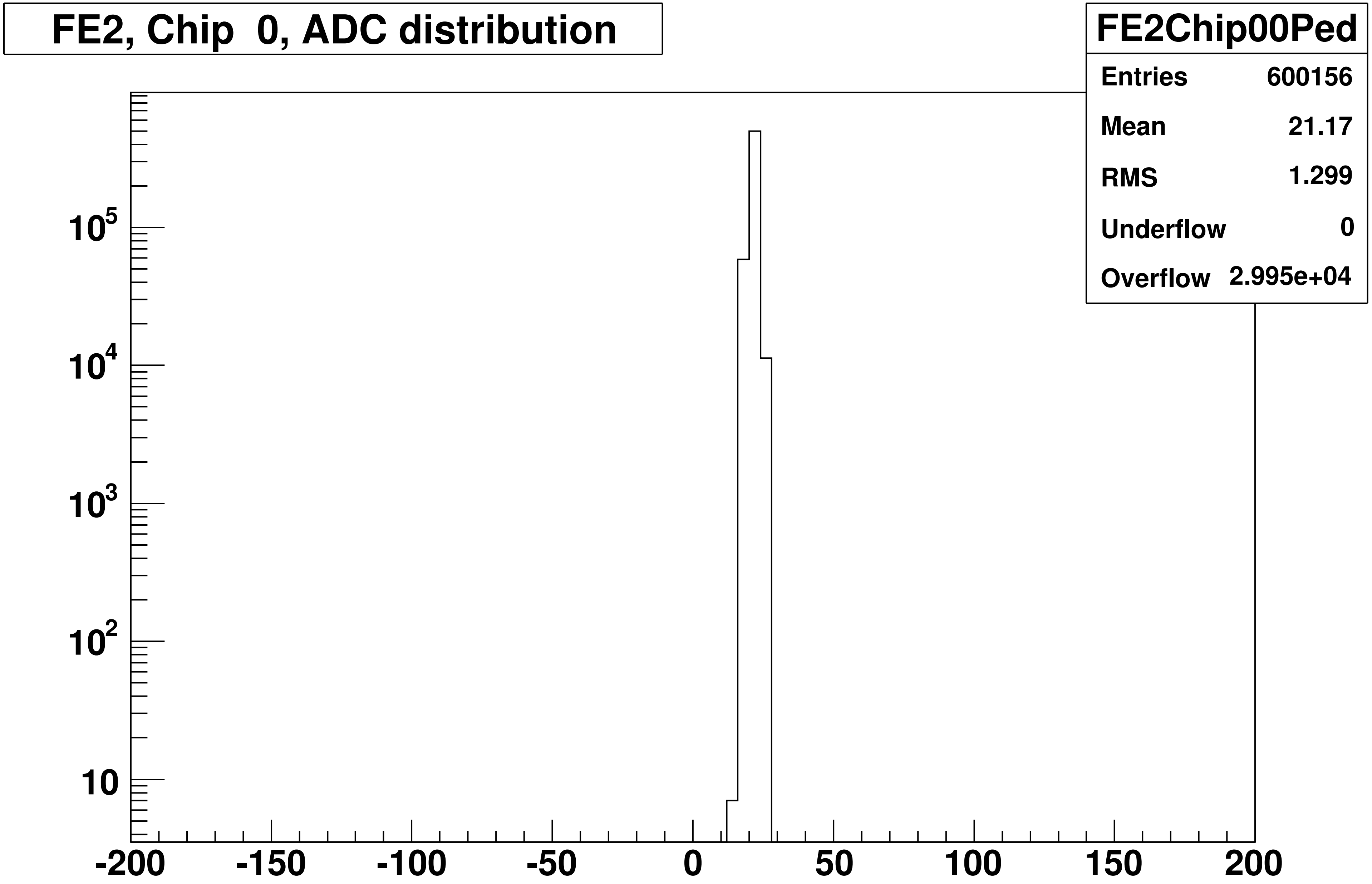
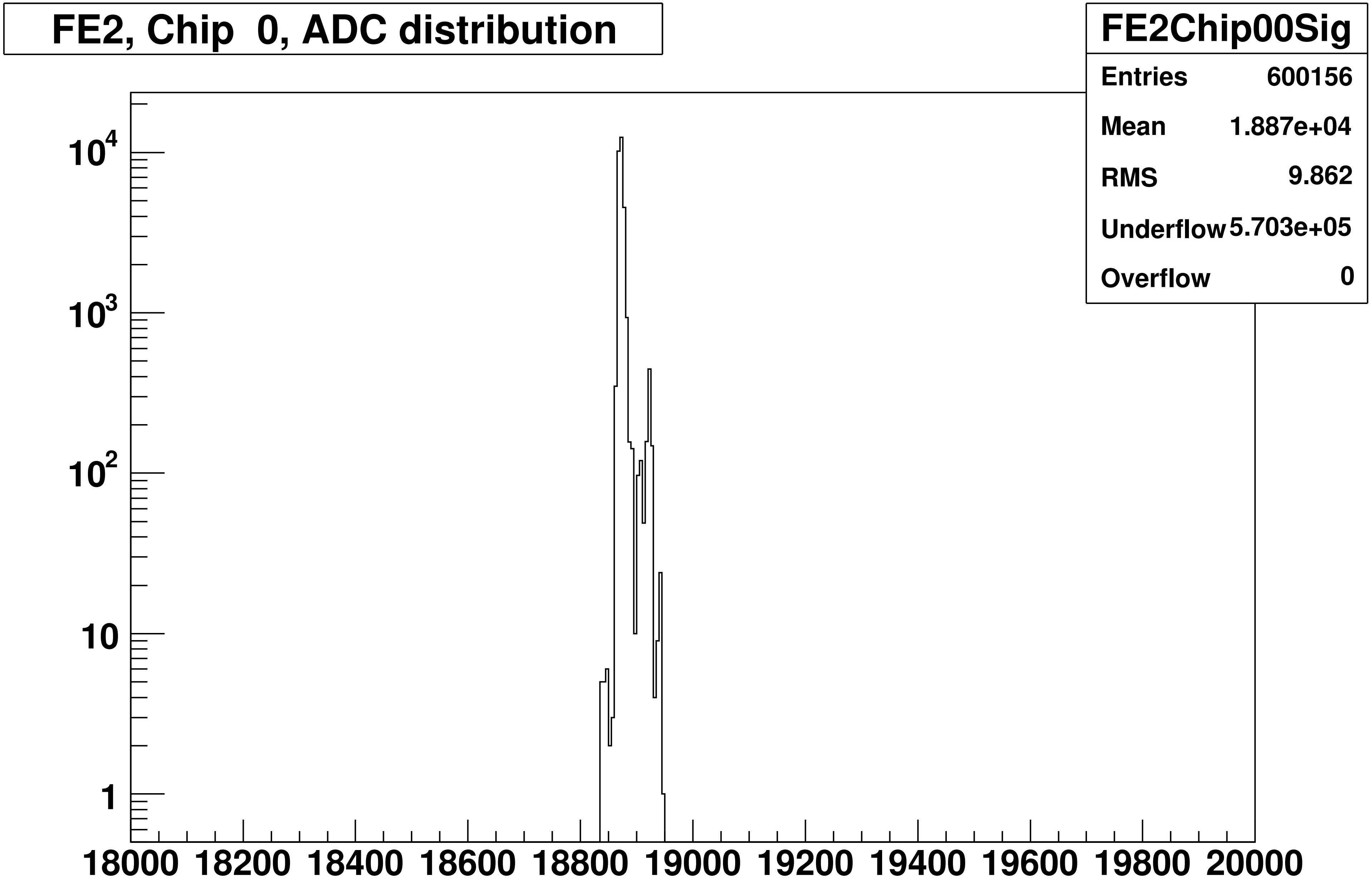
19400
19600
19800
20000

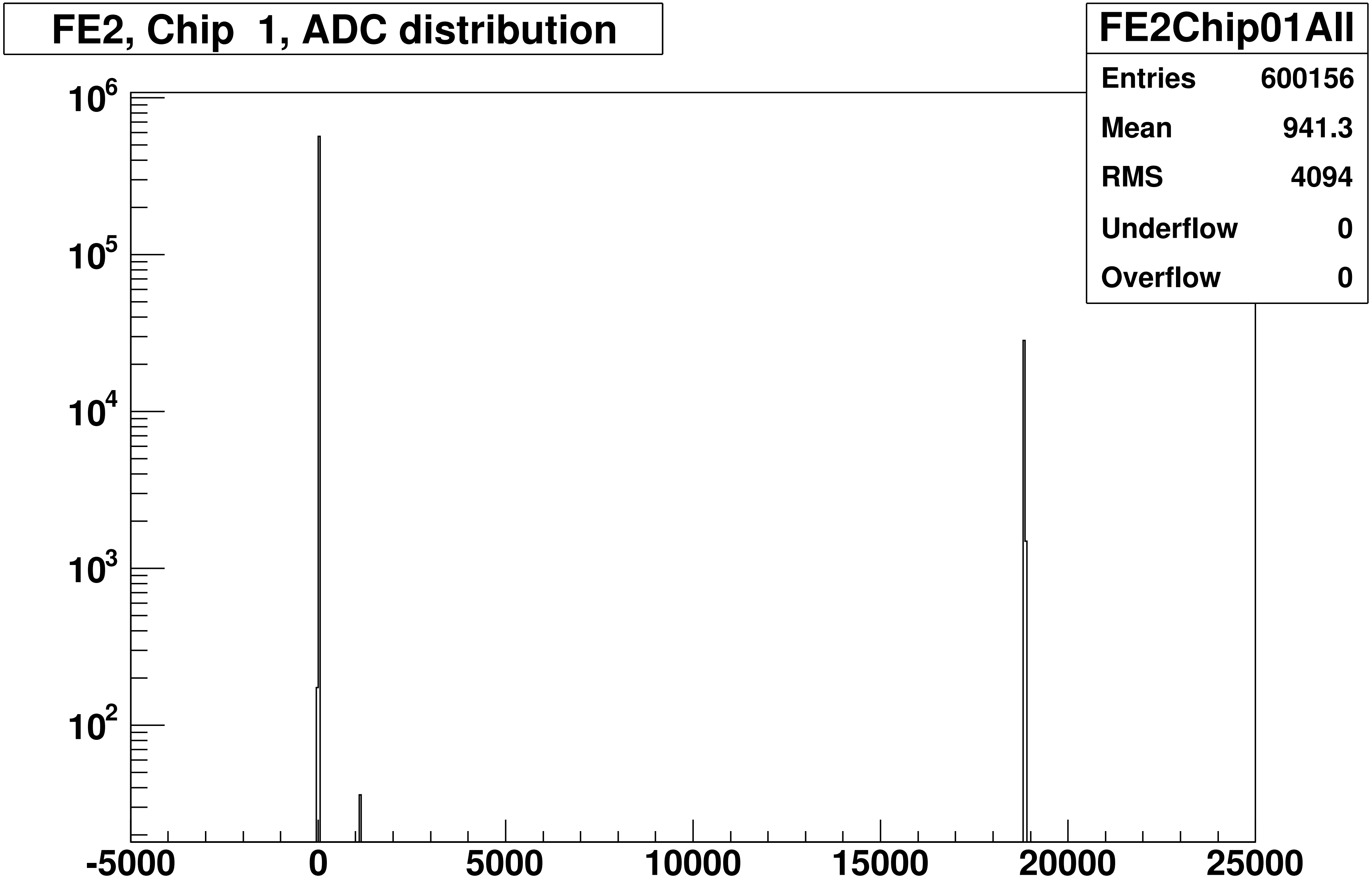


FE2, Chip 0, ADC distribution
FE2Chip00All
Entries 600156
Mean 958.8
RMS 4098
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000

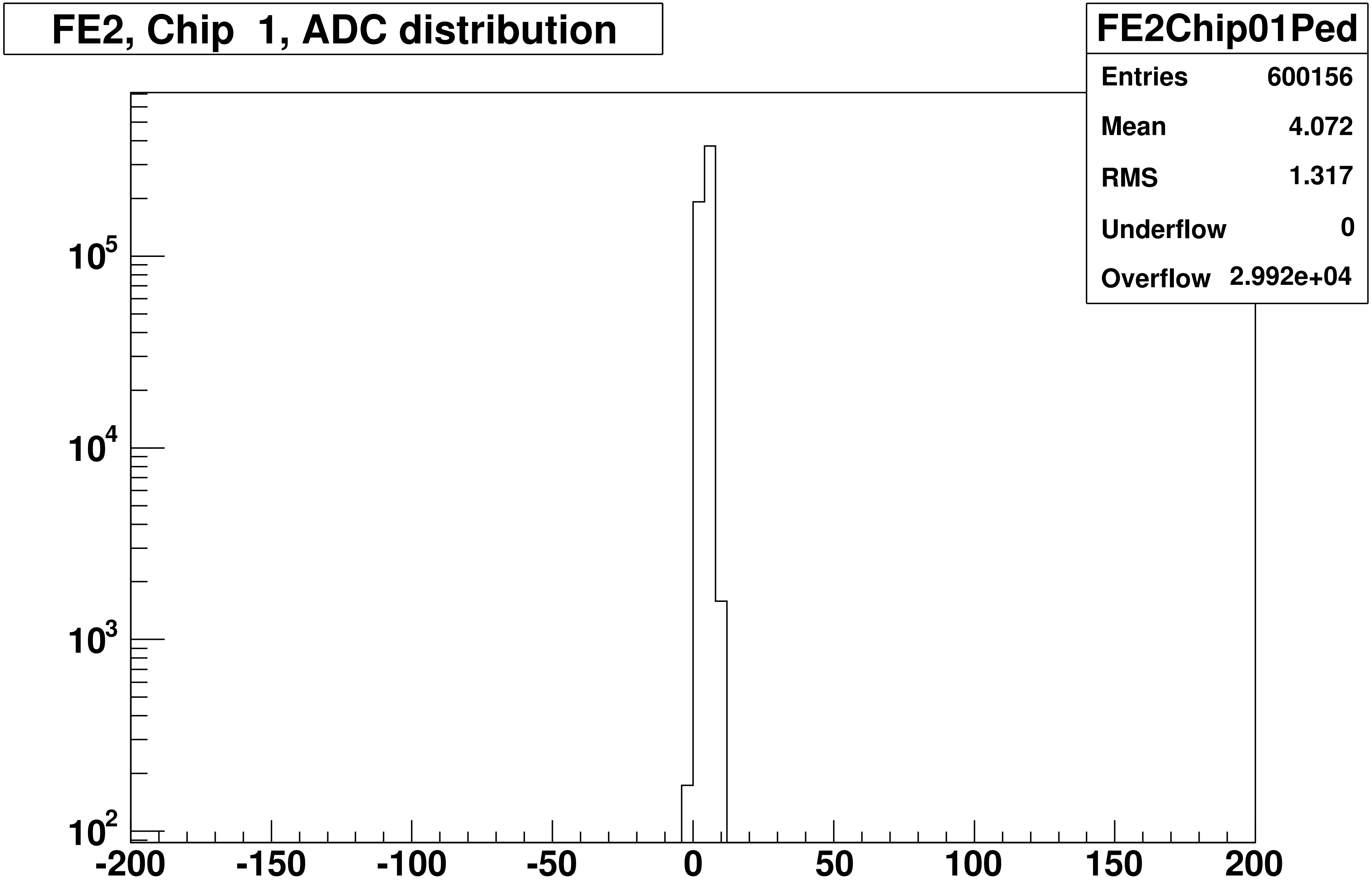


FE2, Chip 0, ADC distribution
FE2Chip00Ped
Entries 600156
Mean 21.17
RMS 1.299
Underflow 0
Overflow 2.995e+04
10^5
10^4
10^3
10^2
10
-200
-150
-100
-50
0
50
100
150
200

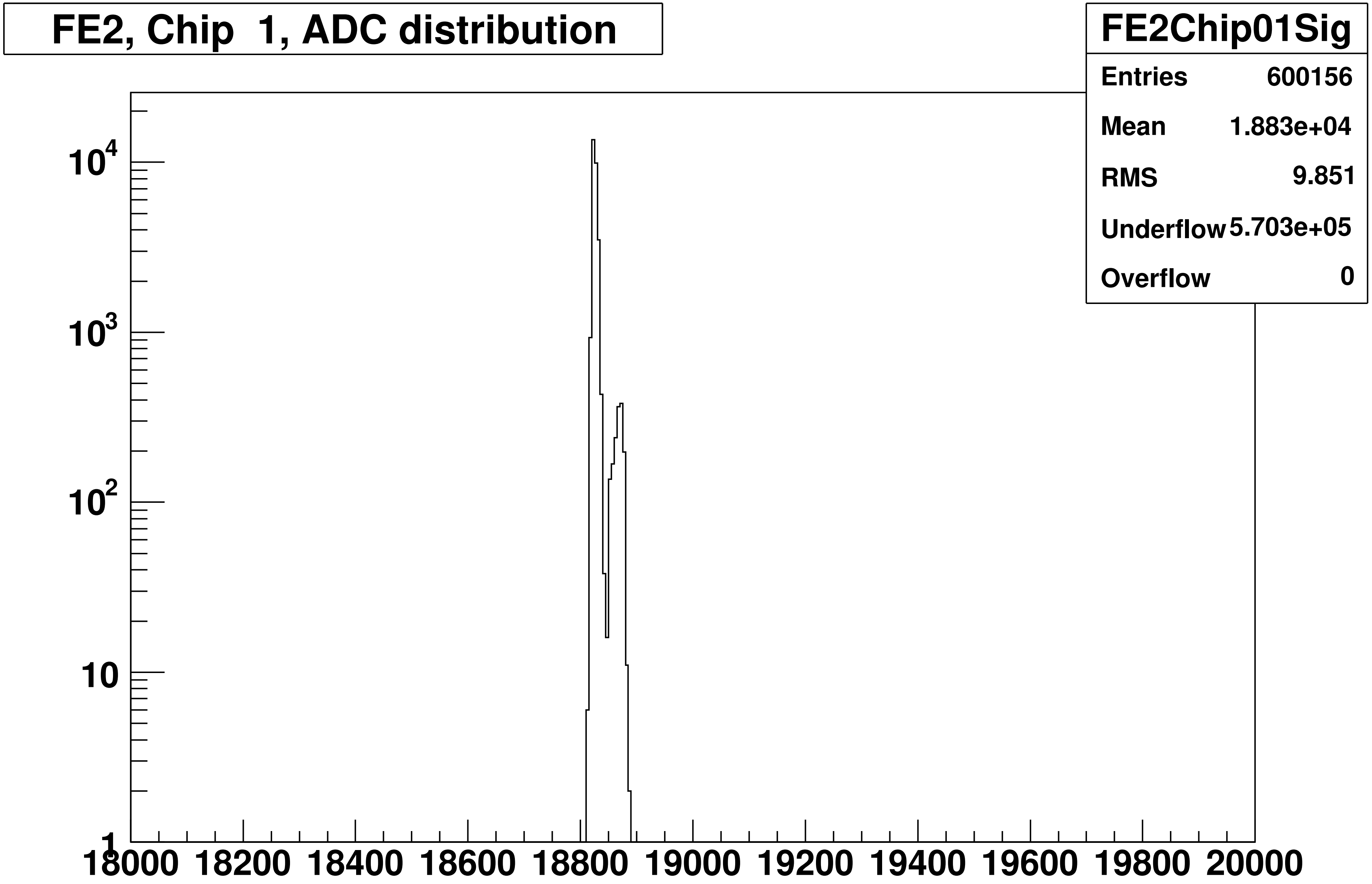

FE2, Chip 0, ADC distribution
FE2Chip00Sig
Entries 600156
Mean 1.887e+04
RMS 9.862
Underflow 5.703e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



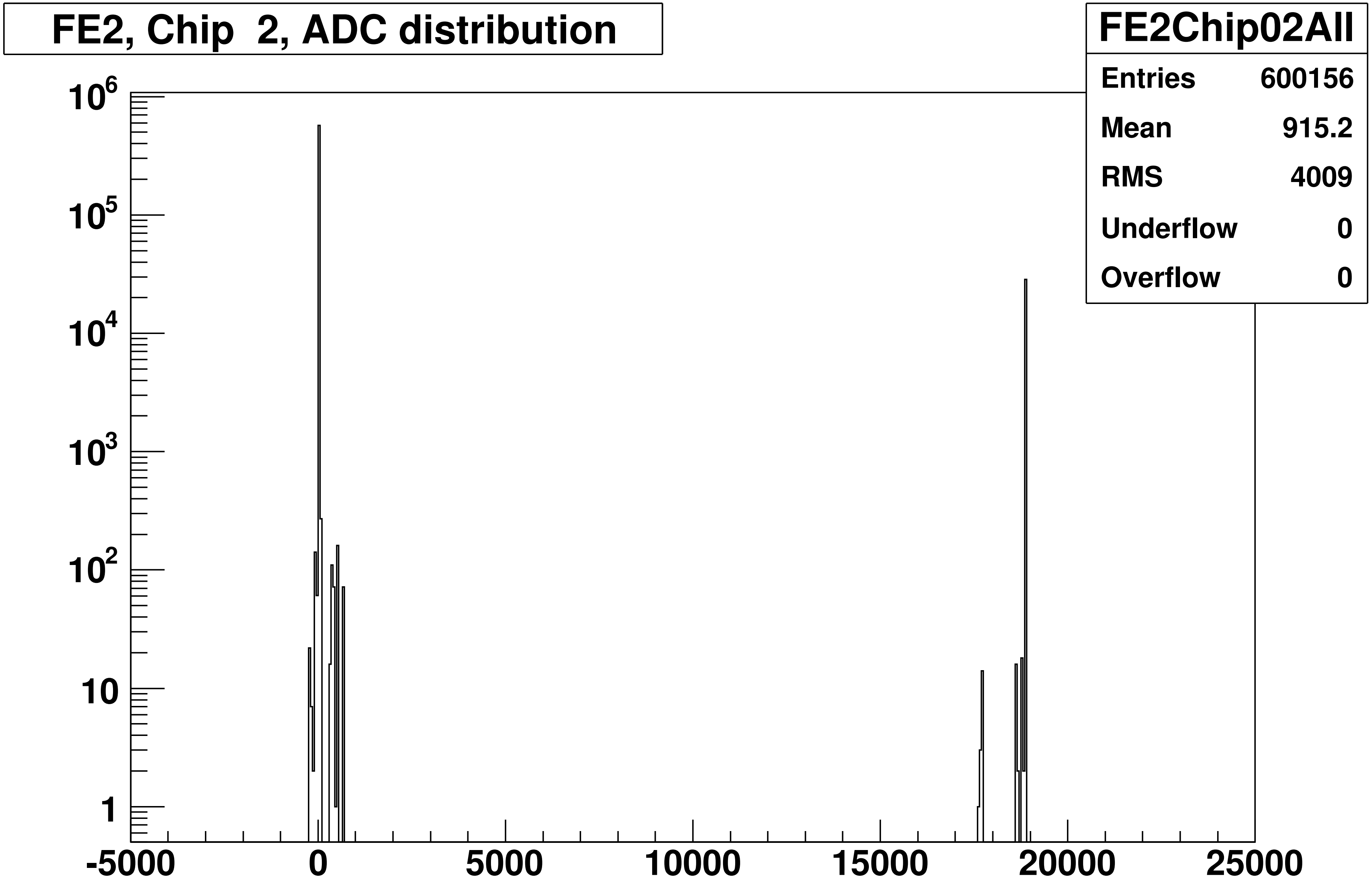
FE2, Chip 1, ADC distribution
FE2Chip01All
Entries 600156
Mean 941.3
RMS 4094
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000

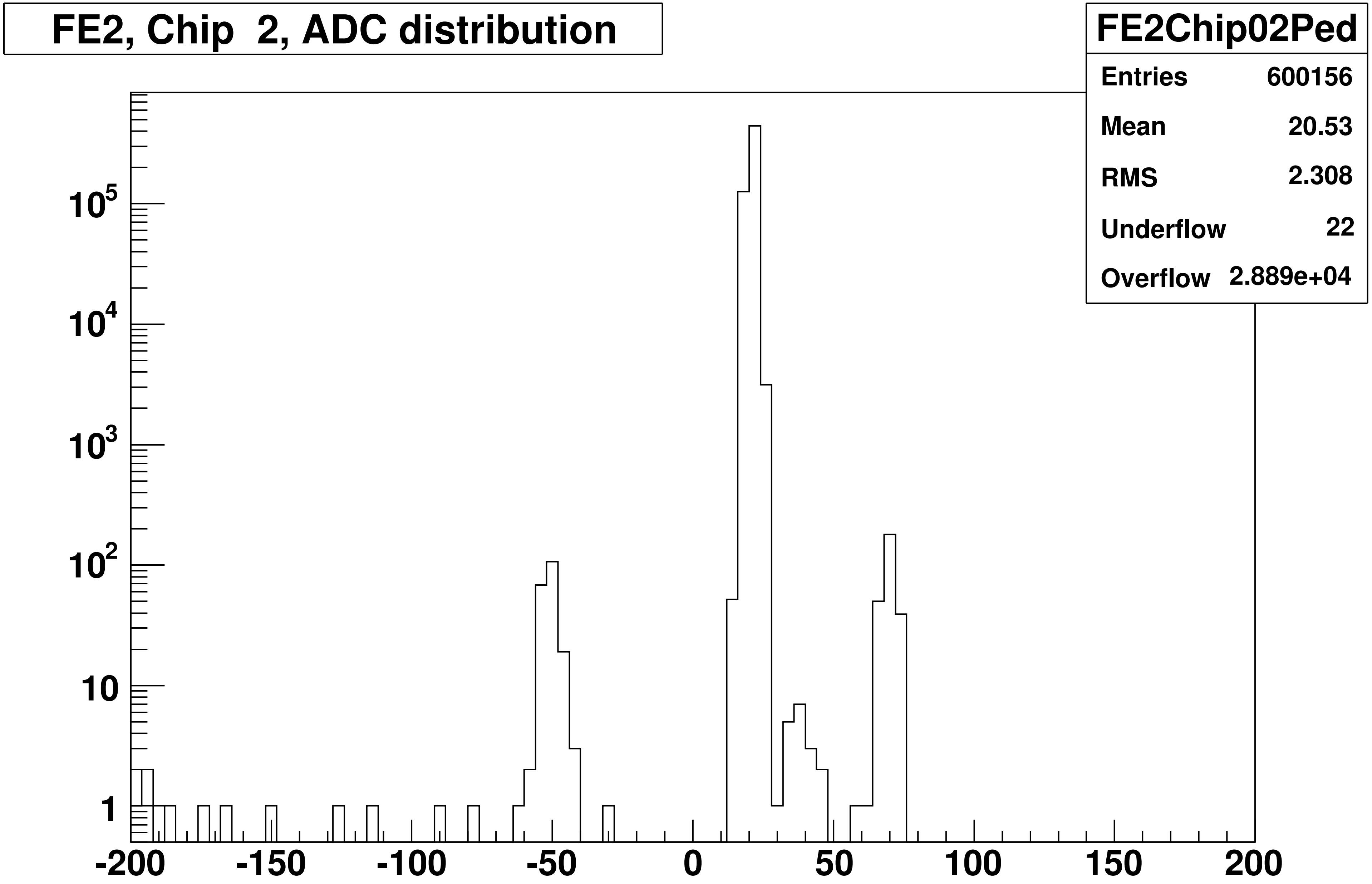


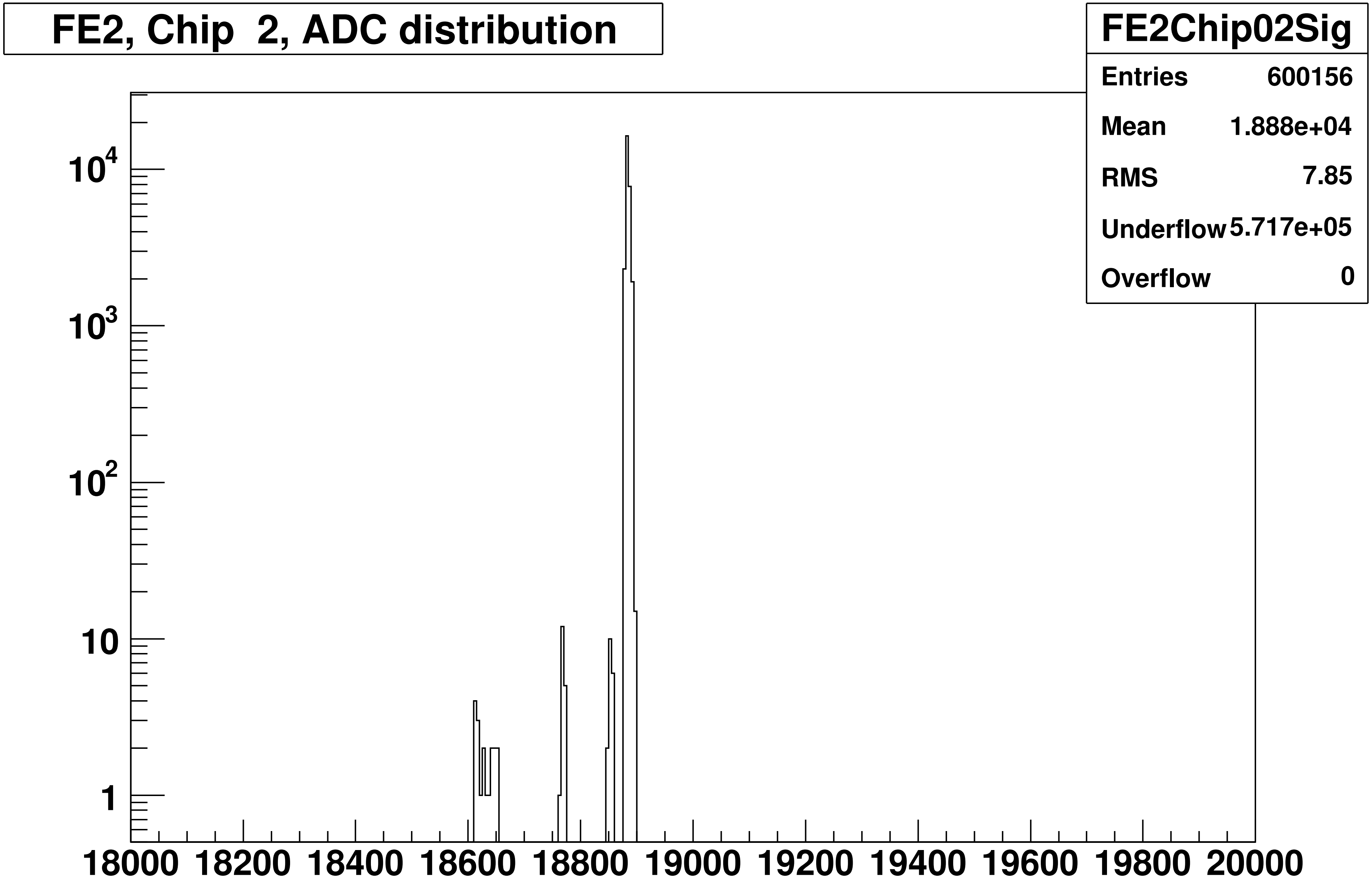
FE2, Chip 1, ADC distribution
FE2Chip01Ped
Entries 600156
Mean 4.072
RMS 1.317
Underflow 0
Overflow 2.992e+04
10^5
10^4
10^3
10^2
-200
-150
-100
-50
0
50
100
150
200



FE2, Chip 1, ADC distribution
FE2Chip01Sig
Entries 600156
Mean 1.883e+04
RMS 9.851
Underflow 5.703e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE2, Chip 2, ADC distribution
FE2Chip02All
Entries 600156
Mean 915.2
RMS 4009
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE2, Chip 2, ADC distribution
FE2Chip02Ped
Entries 600156
Mean 20.53
RMS 2.308
Underflow 22
Overflow 2.889e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
200


FE2, Chip 2, ADC distribution
FE2Chip02Sig
Entries 600156
Mean 1.888e+04
RMS 7.85
Underflow 5.717e+05
Overflow 0
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10^3
10^2
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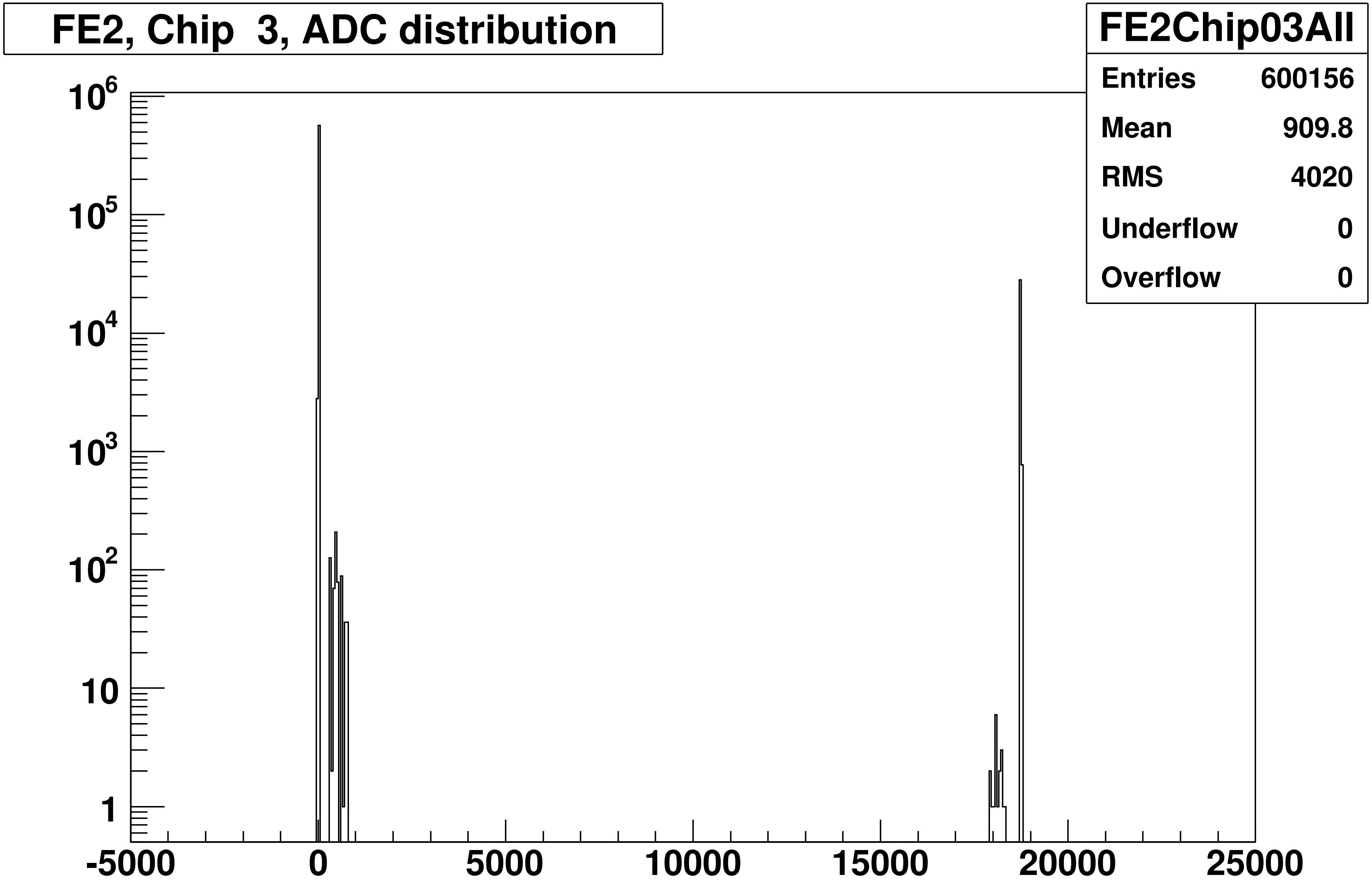
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE2, Chip 3, ADC distribution
FE2Chip03All
Entries 600156
Mean 909.8
RMS 4020
Underflow 0
Overflow 0
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10^3
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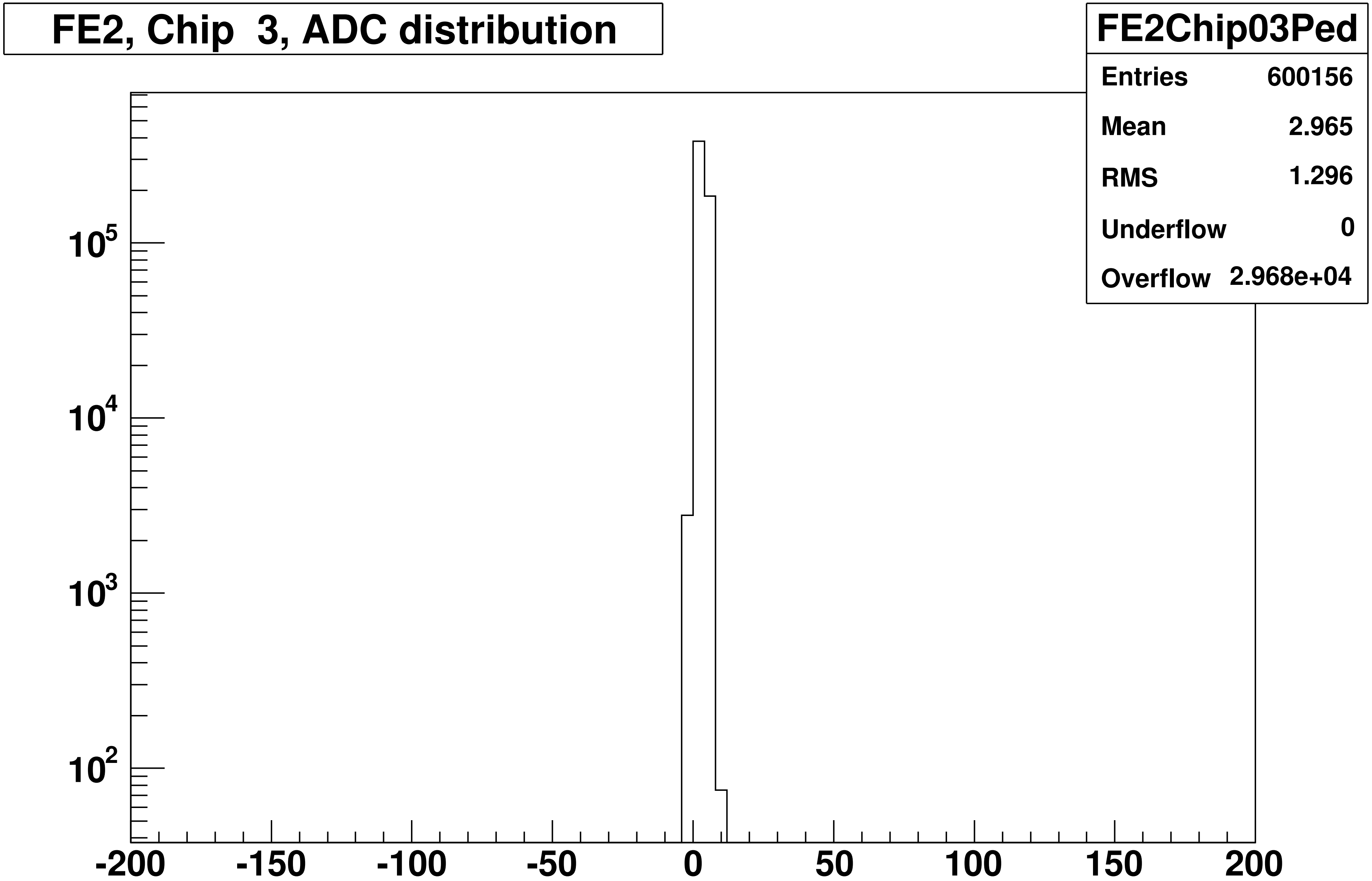

FE2, Chip 3, ADC distribution
FE2Chip03Ped
Entries 600156
Mean 2.965
RMS 1.296
Underflow 0
Overflow 2.968e+04
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10^3
10^2
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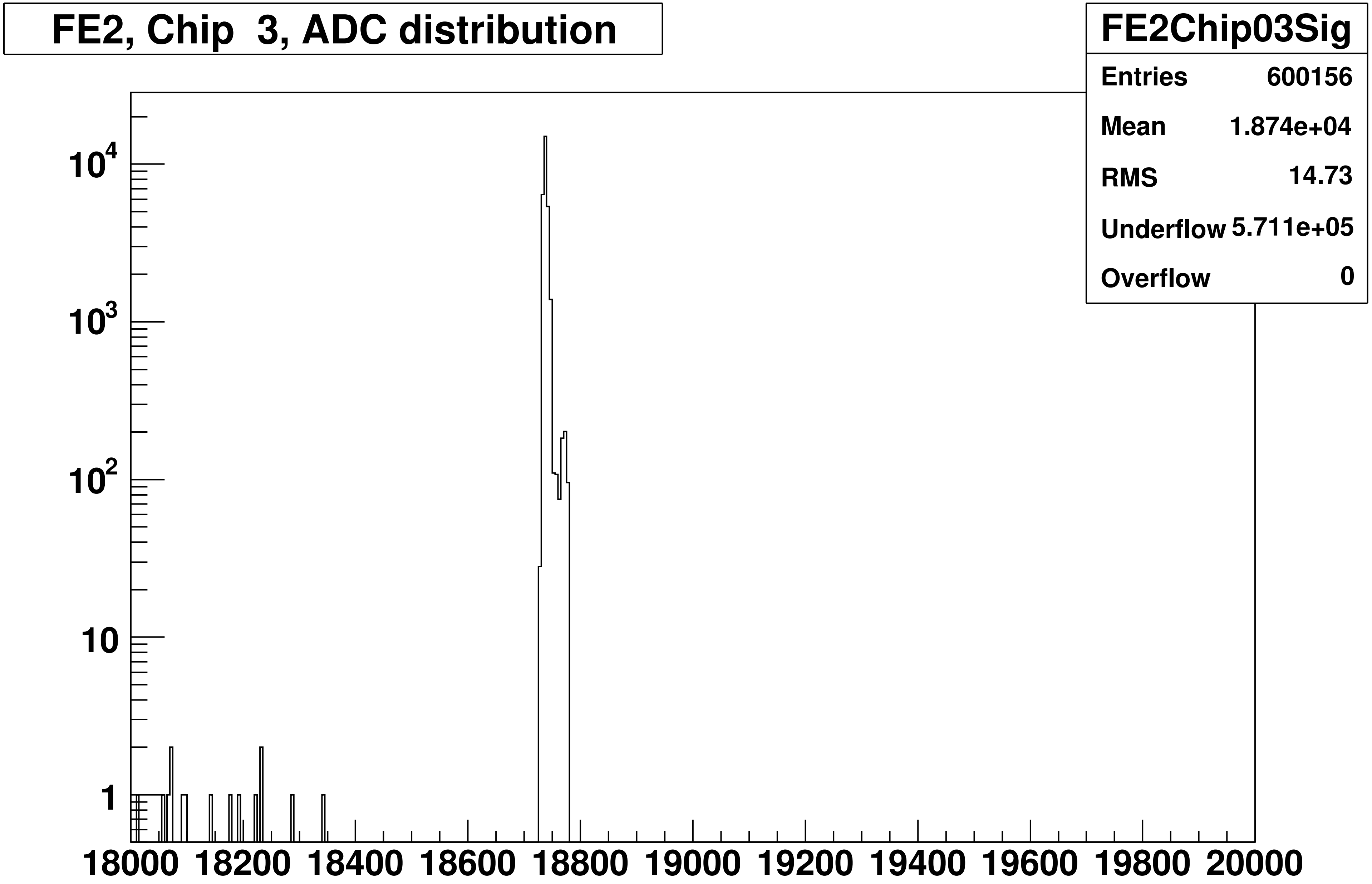
200



FE2, Chip 3, ADC distribution
FE2Chip03Sig
Entries 600156
Mean 1.874e+04
RMS 14.73
Underflow 5.711e+05
Overflow 0
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10^3
10^2
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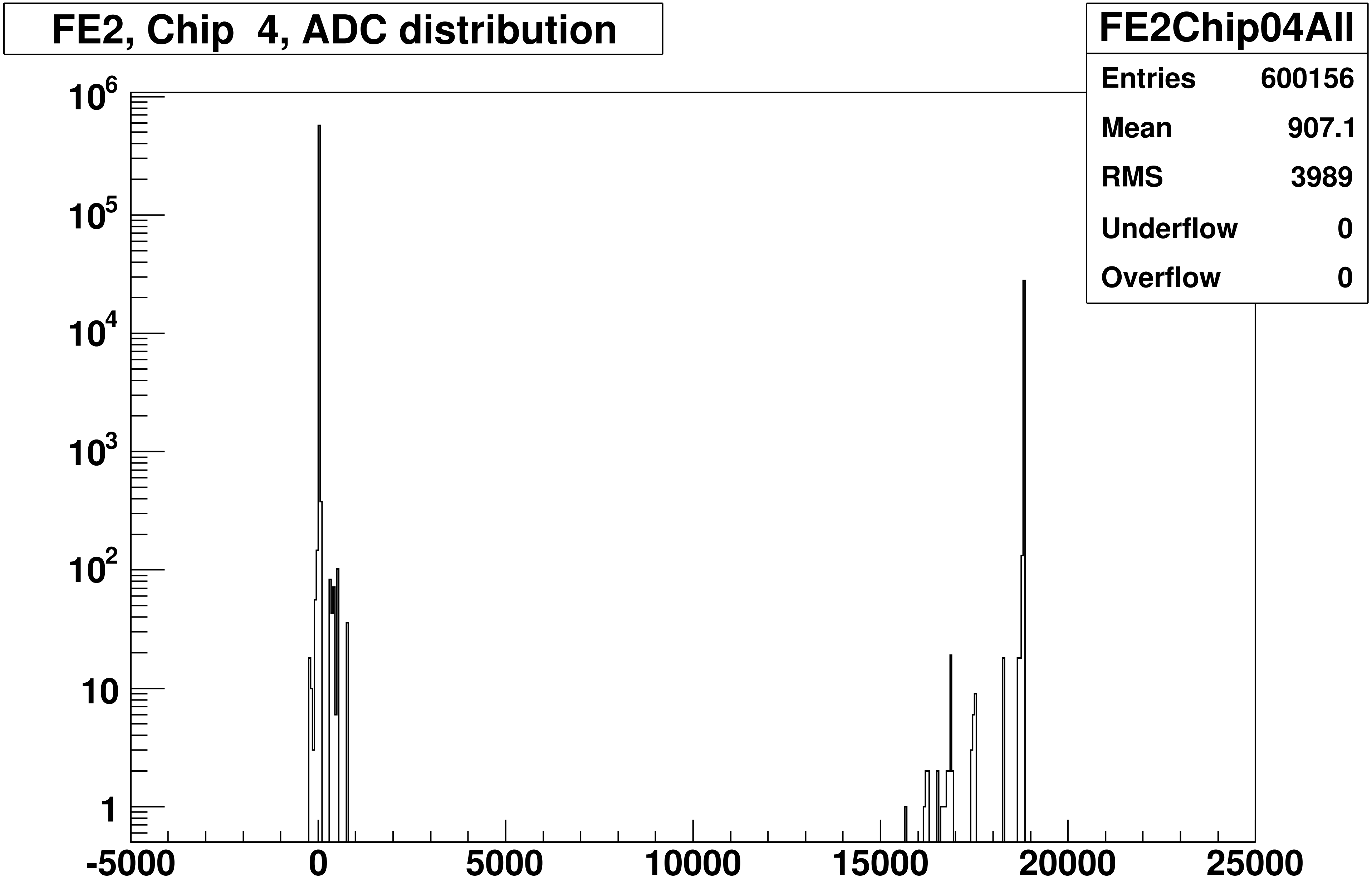

FE2, Chip 4, ADC distribution
FE2Chip04All
Entries 600156
Mean 907.1
RMS 3989
Underflow 0
Overflow 0
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10^4
10^3
10^2
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5000
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20000
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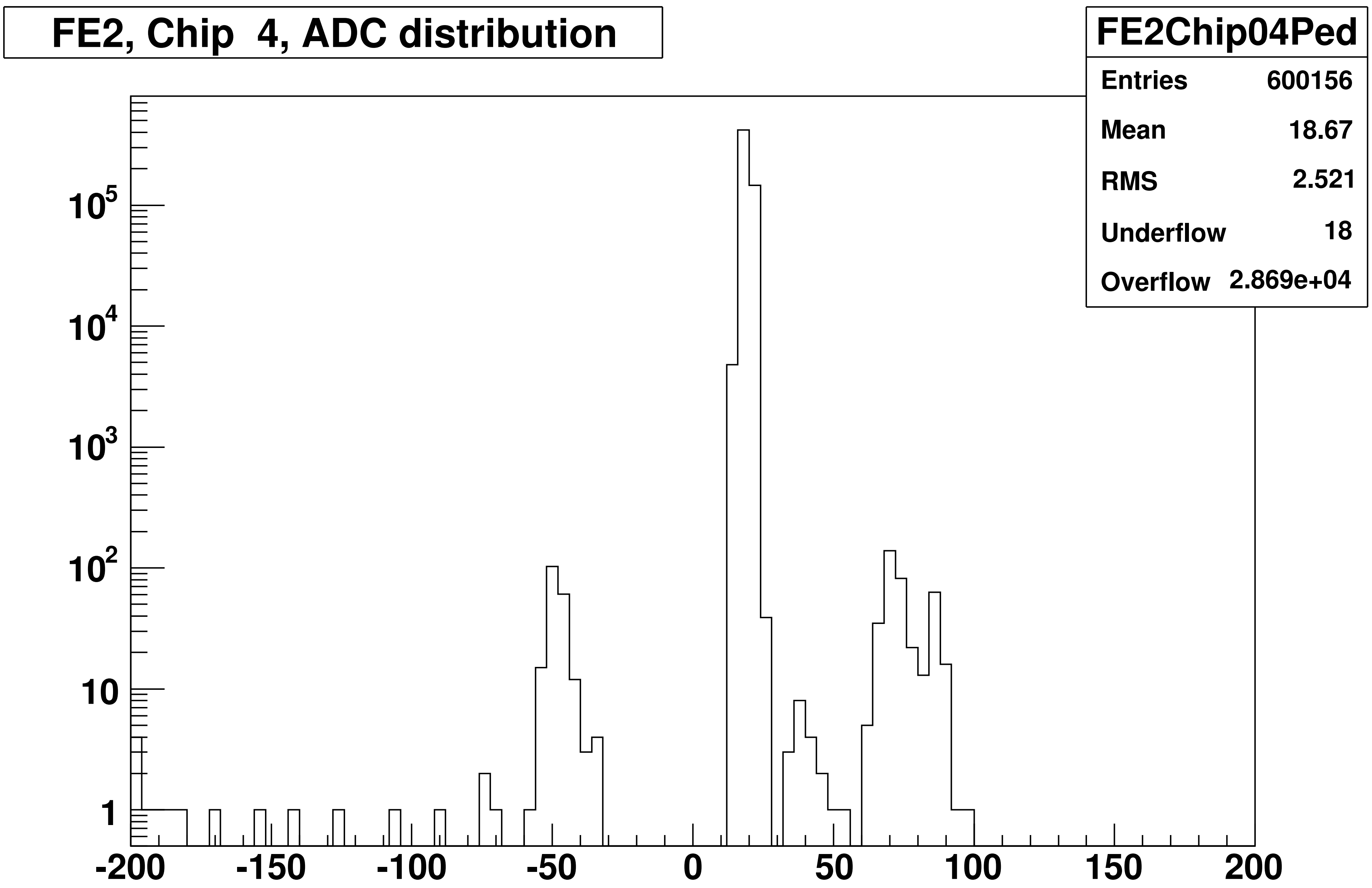

FE2, Chip 4, ADC distribution
FE2Chip04Ped
Entries 600156
Mean 18.67
RMS 2.521
Underflow 18
Overflow 2.869e+04
10^5
10^4
10^3
10^2
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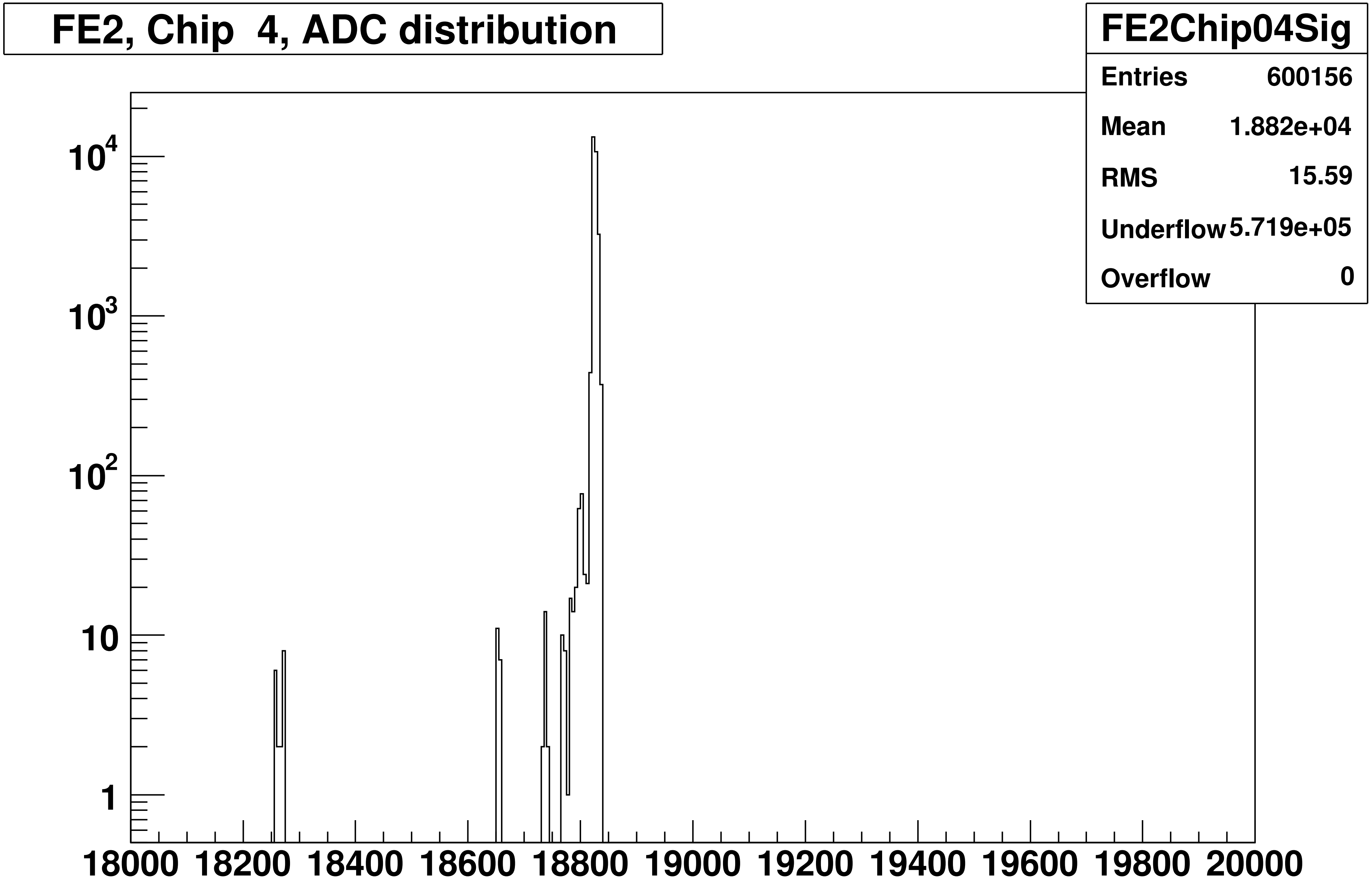

FE2, Chip 4, ADC distribution
FE2Chip04Sig
Entries 600156
Mean 1.882e+04
RMS 15.59
Underflow 5.719e+05
Overflow 0
10^4
10^3
10^2
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18000
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18400
18600
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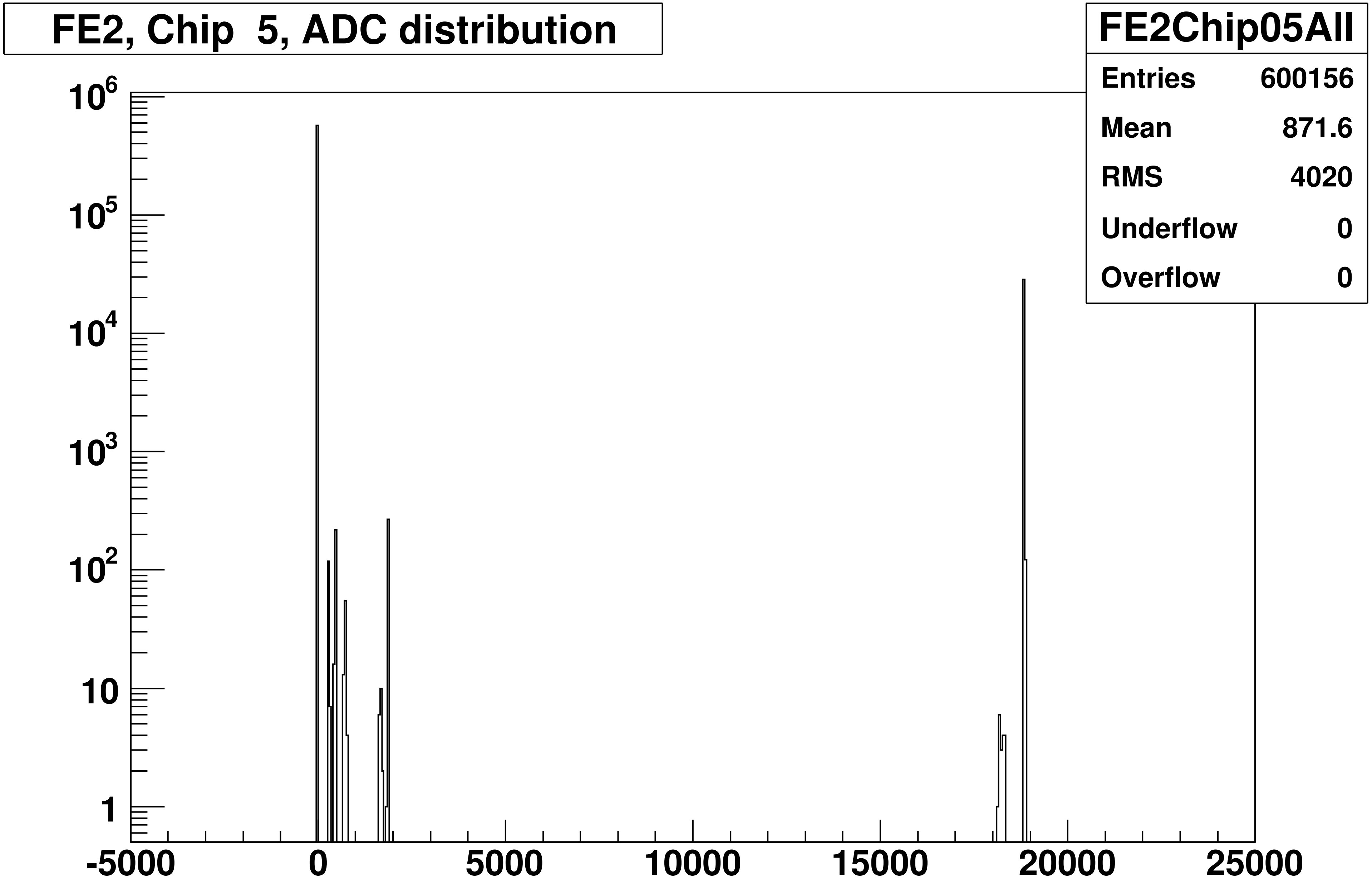
19400
19600
19800
20000


FE2, Chip 5, ADC distribution
FE2Chip05All
Entries 600156
Mean 871.6
RMS 4020
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
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-5000
0
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10000
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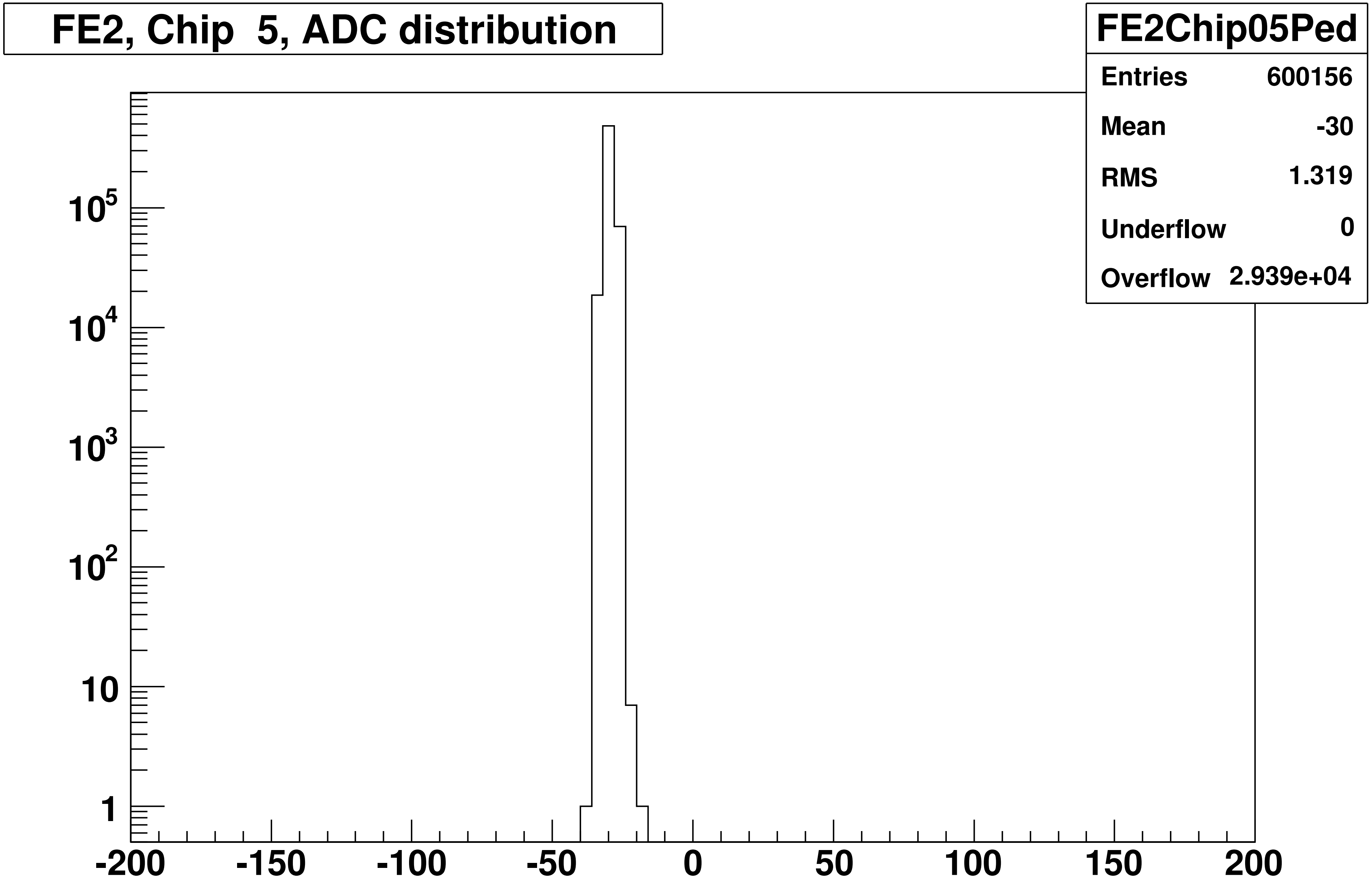
20000
25000



FE2, Chip 5, ADC distribution
FE2Chip05Ped
Entries 600156
Mean -30
RMS 1.319
Underflow 0
Overflow 2.939e+04
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10^3
10^2
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150
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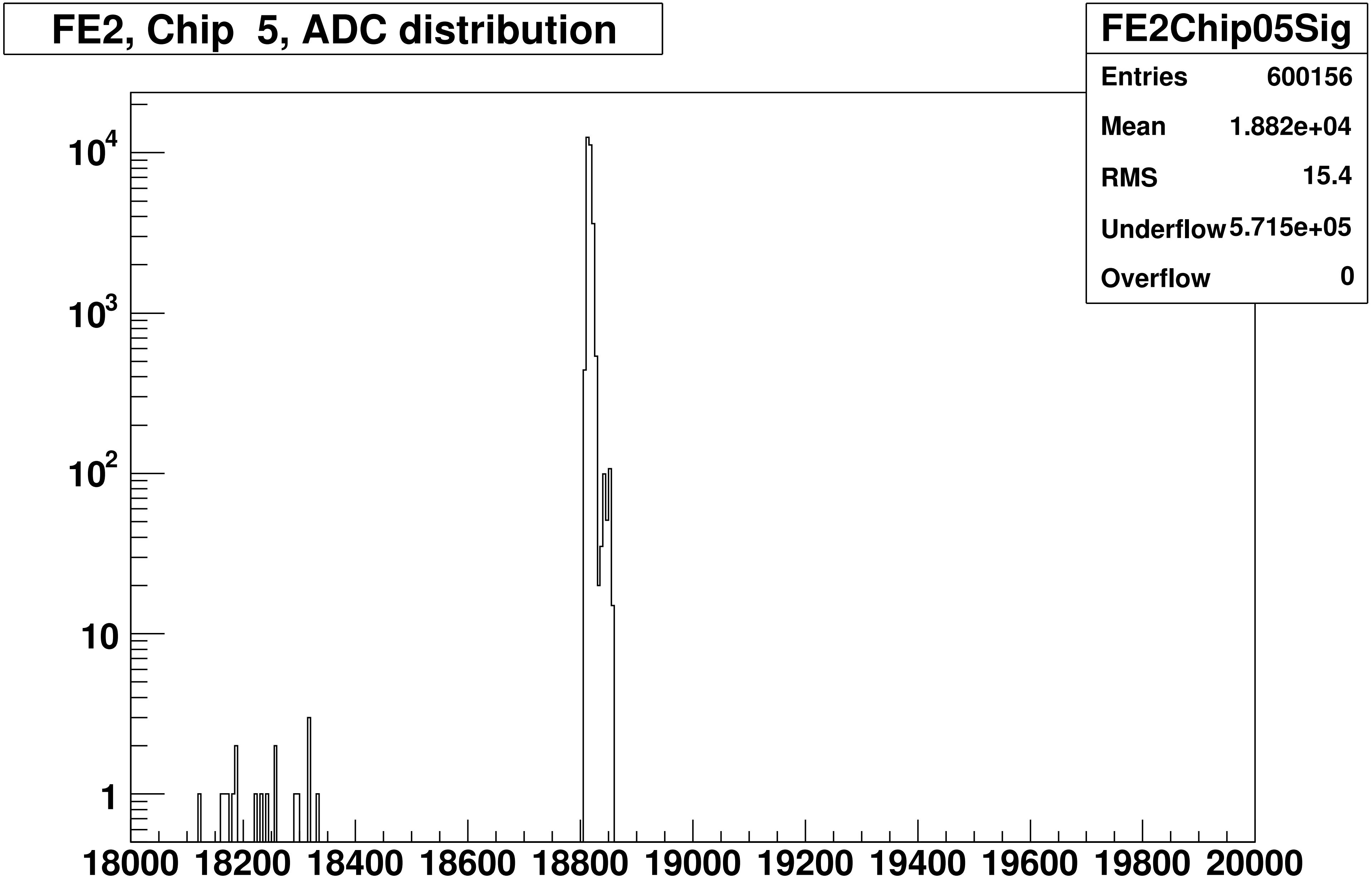
FE2, Chip 5, ADC distribution
FE2Chip05Sig
Entries 600156
Mean 1.882e+04
RMS 15.4
Underflow 5.715e+05
Overflow 0
10^4
10^3
10^2
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18000
18200
18400
18600
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19000
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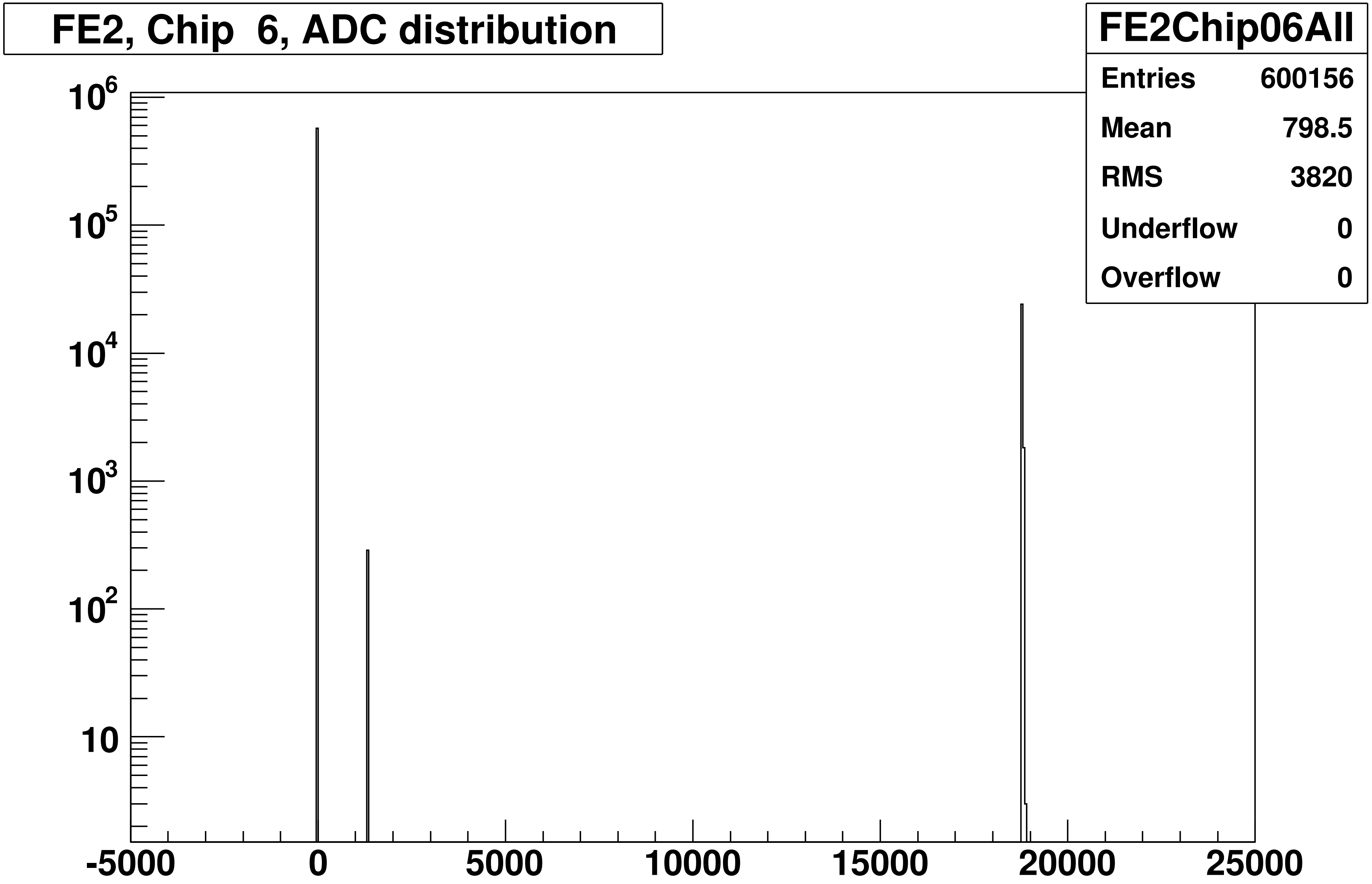
19800
20000


FE2, Chip 6, ADC distribution
FE2Chip06All
Entries 600156
Mean 798.5
RMS 3820
Underflow 0
Overflow 0
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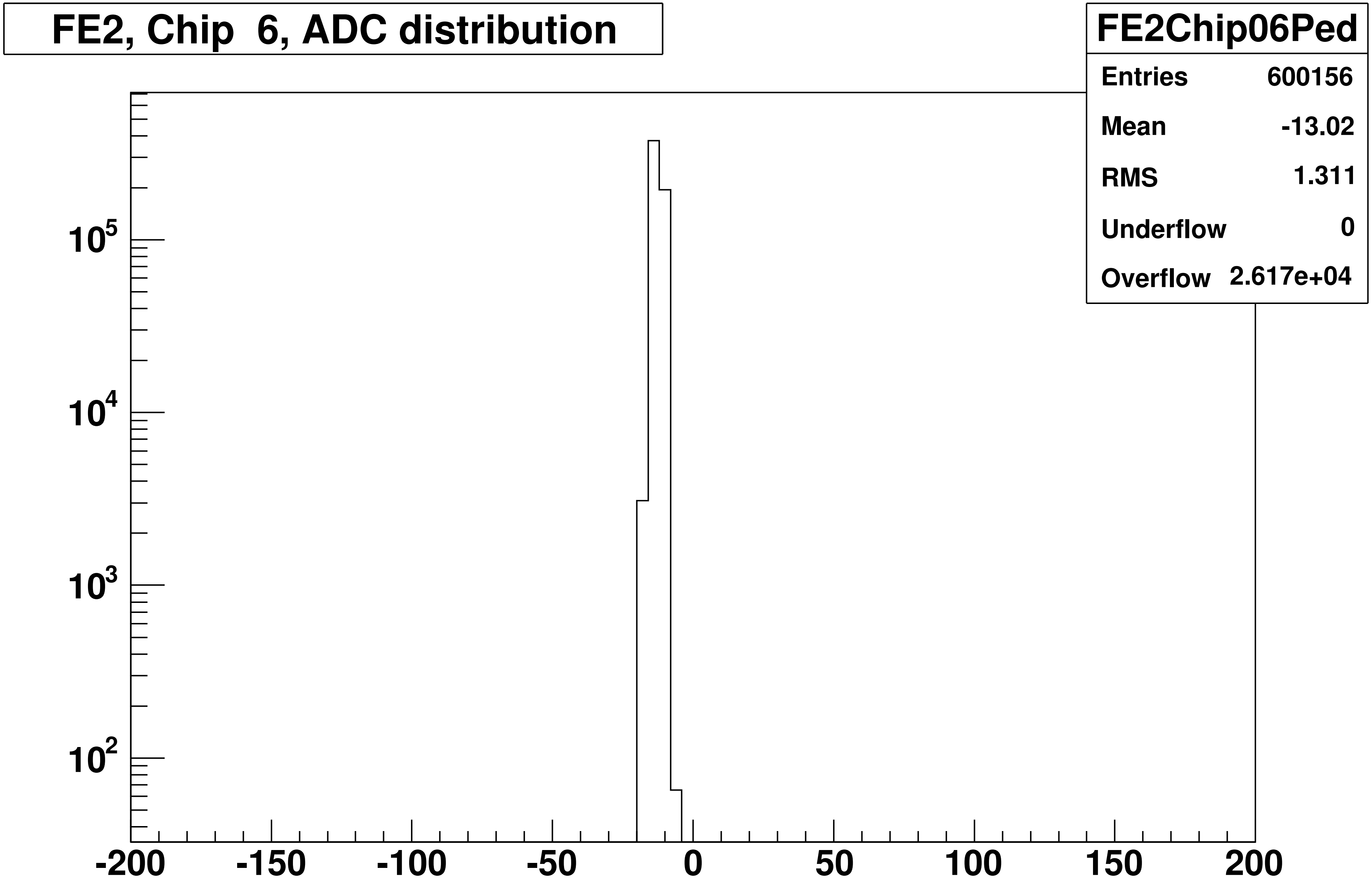
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000



FE2, Chip 6, ADC distribution
FE2Chip06Ped
Entries 600156
Mean -13.02
RMS 1.311
Underflow 0
Overflow 2.617e+04
10^5
10^4
10^3
10^2
-200
-150
-100
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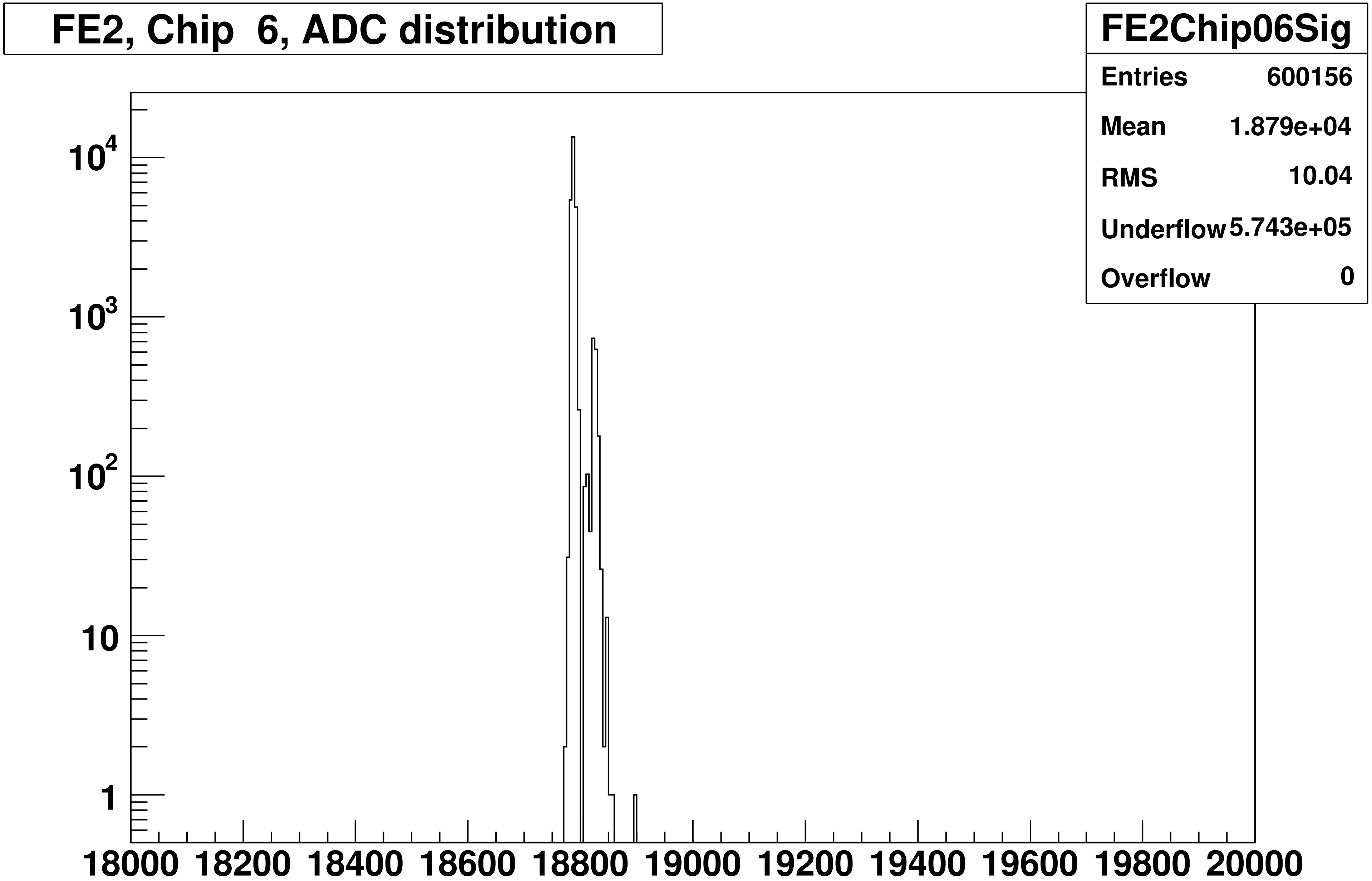
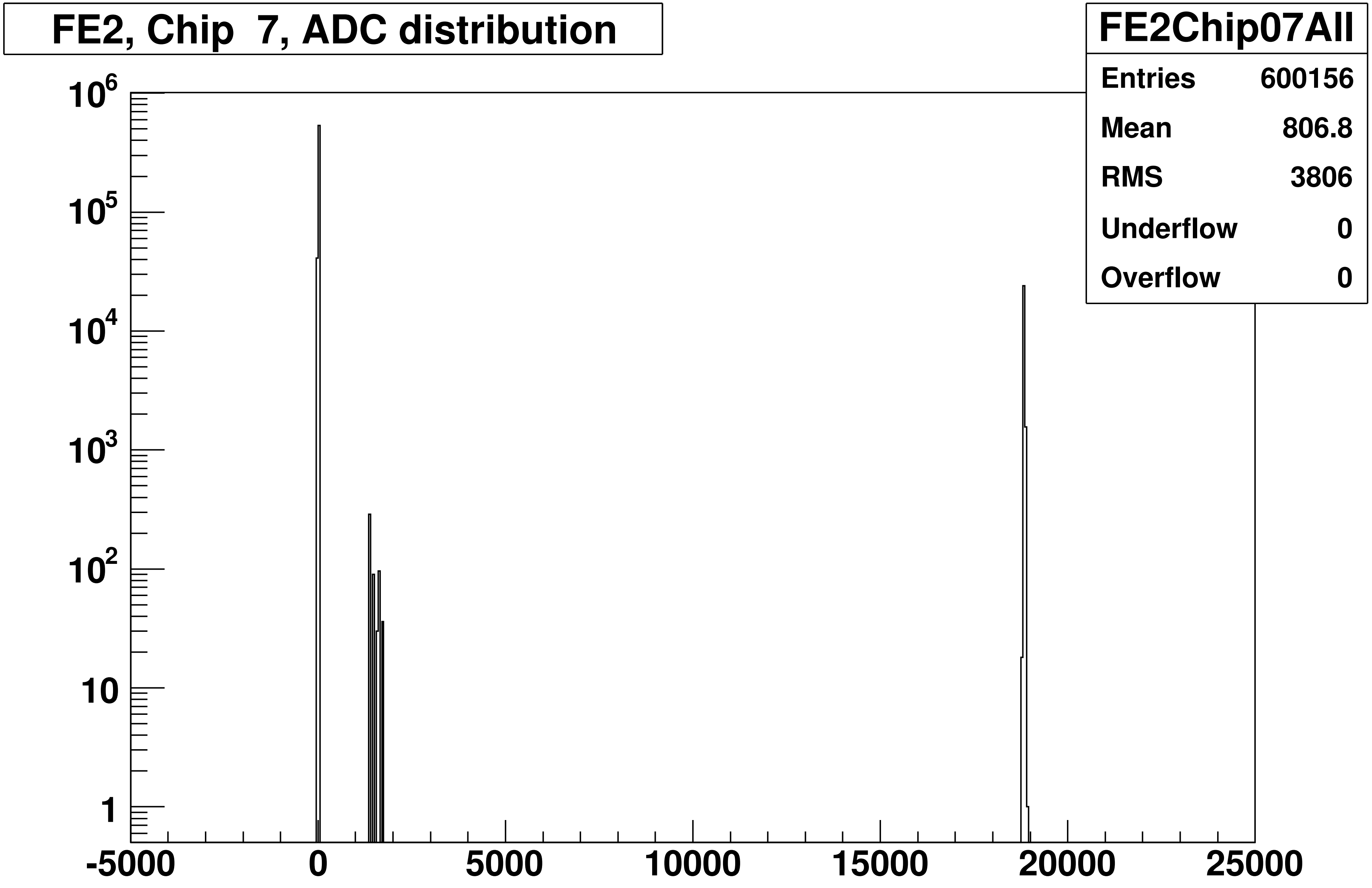
0
50
100
150
200



FE2, Chip 6, ADC distribution
FE2Chip06Sig
Entries 600156
Mean 1.879e+04
RMS 10.04
Underflow 5.743e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000


FE2, Chip 7, ADC distribution
FE2Chip07All
Entries 600156
Mean 806.8
RMS 3806
Underflow 0
Overflow 0
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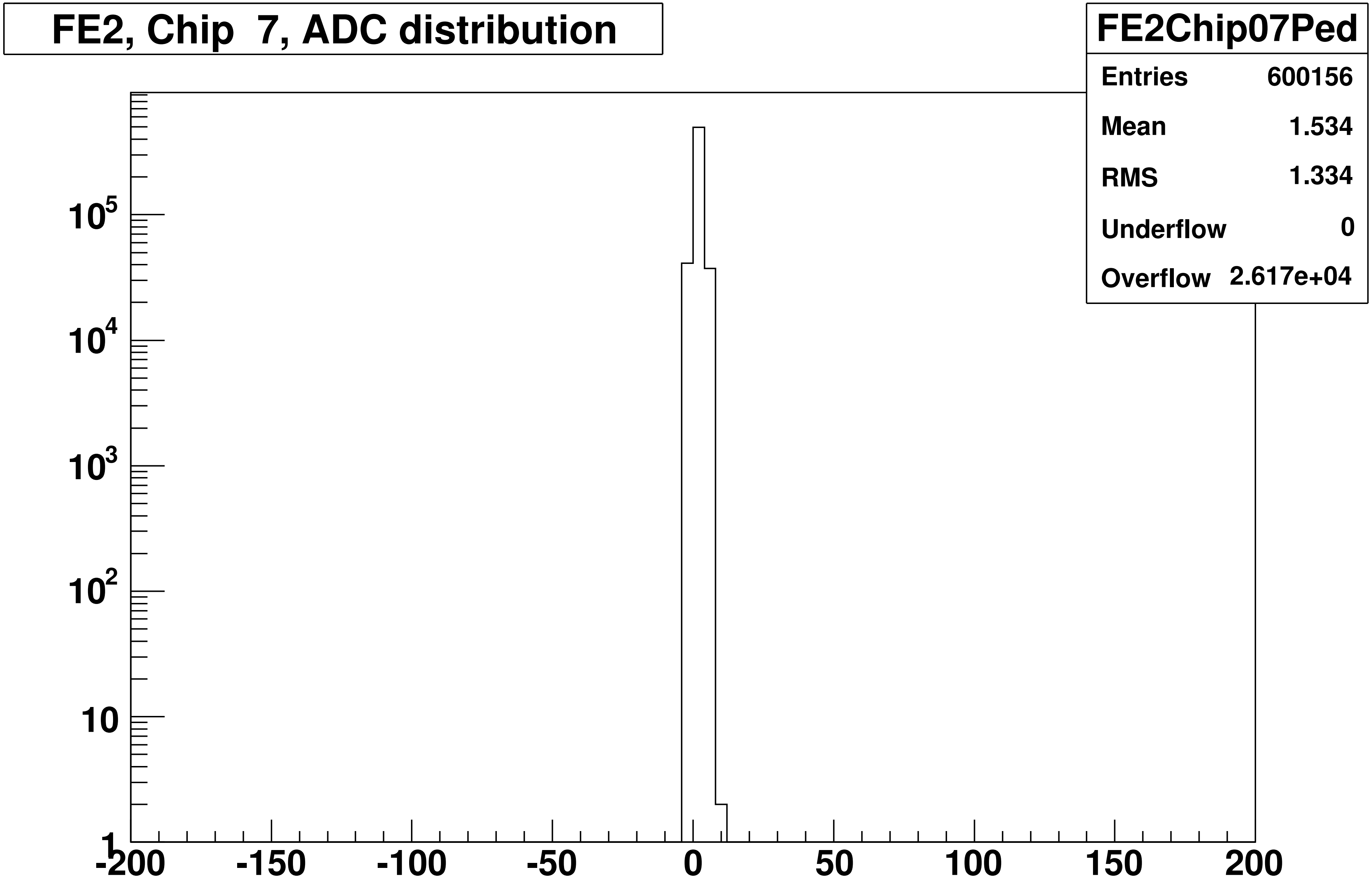
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE2, Chip 7, ADC distribution
FE2Chip07Ped
Entries 600156
Mean 1.534
RMS 1.334
Underflow 0
Overflow 2.617e+04
1
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10^2
10^3
10^4
10^5
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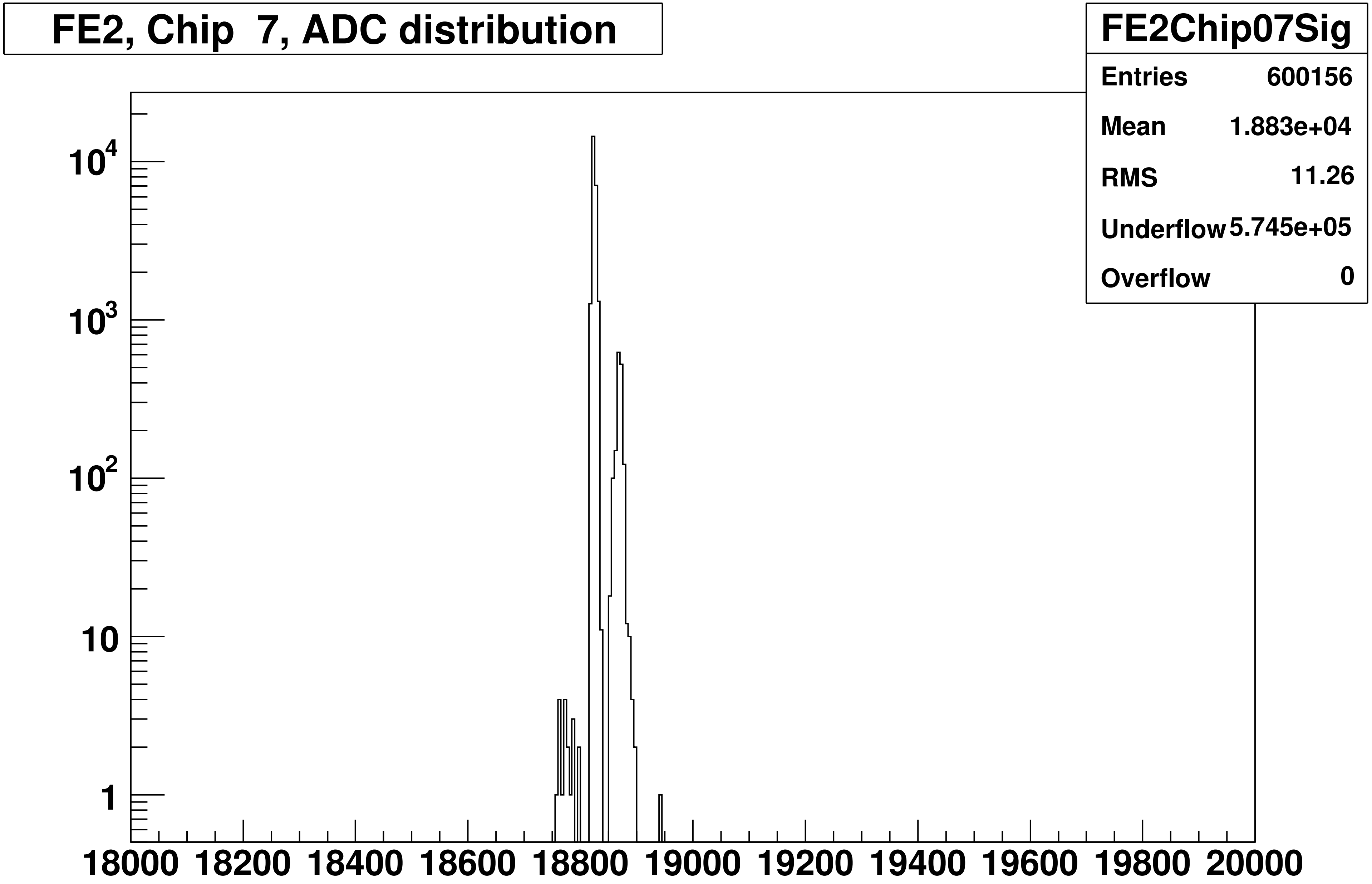
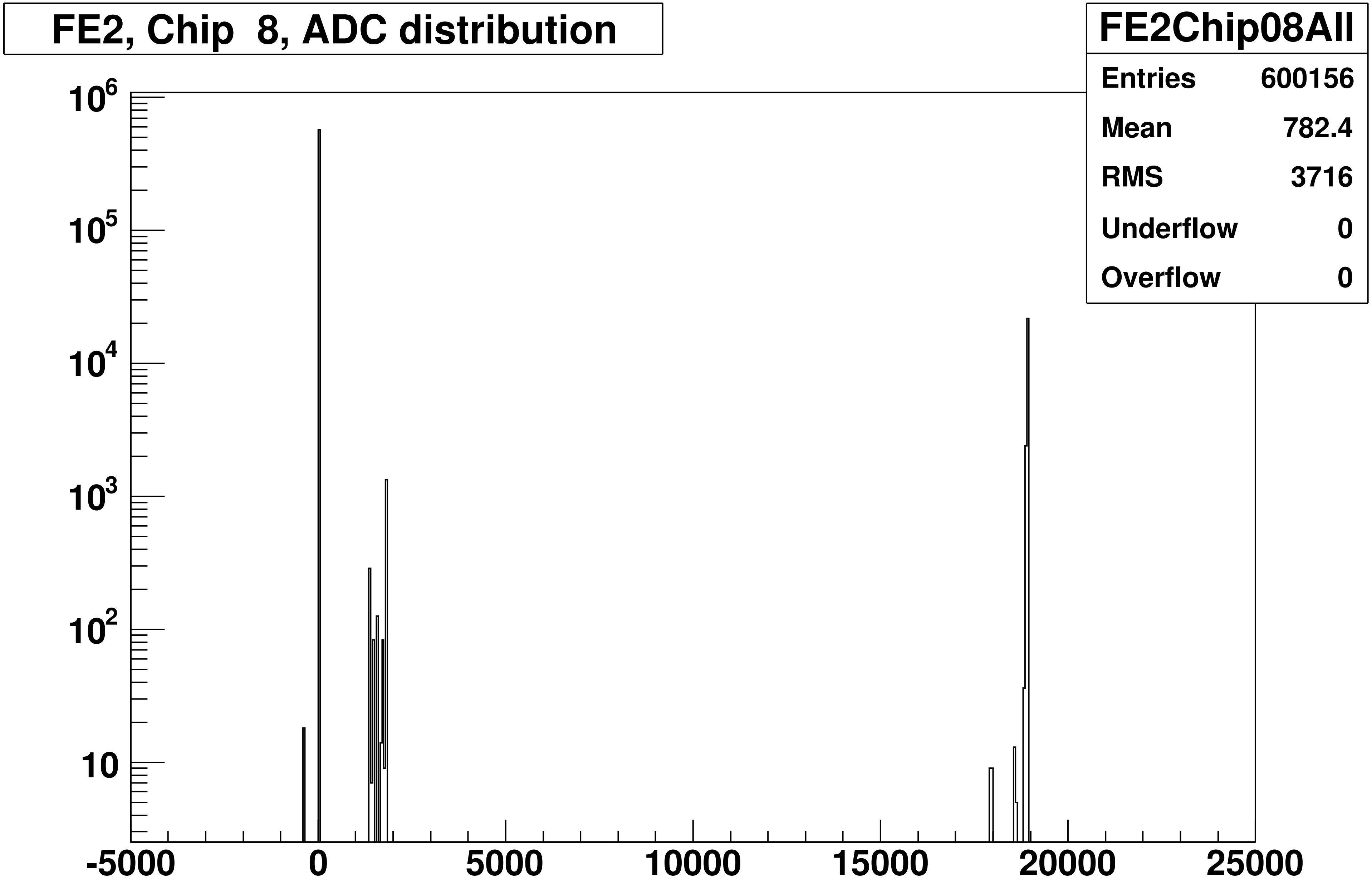
0
50
100
150
200



FE2, Chip 7, ADC distribution
FE2Chip07Sig
Entries 600156
Mean 1.883e+04
RMS 11.26
Underflow 5.745e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE2, Chip 8, ADC distribution
FE2Chip08All
Entries 600156
Mean 782.4
RMS 3716
Underflow 0
Overflow 0
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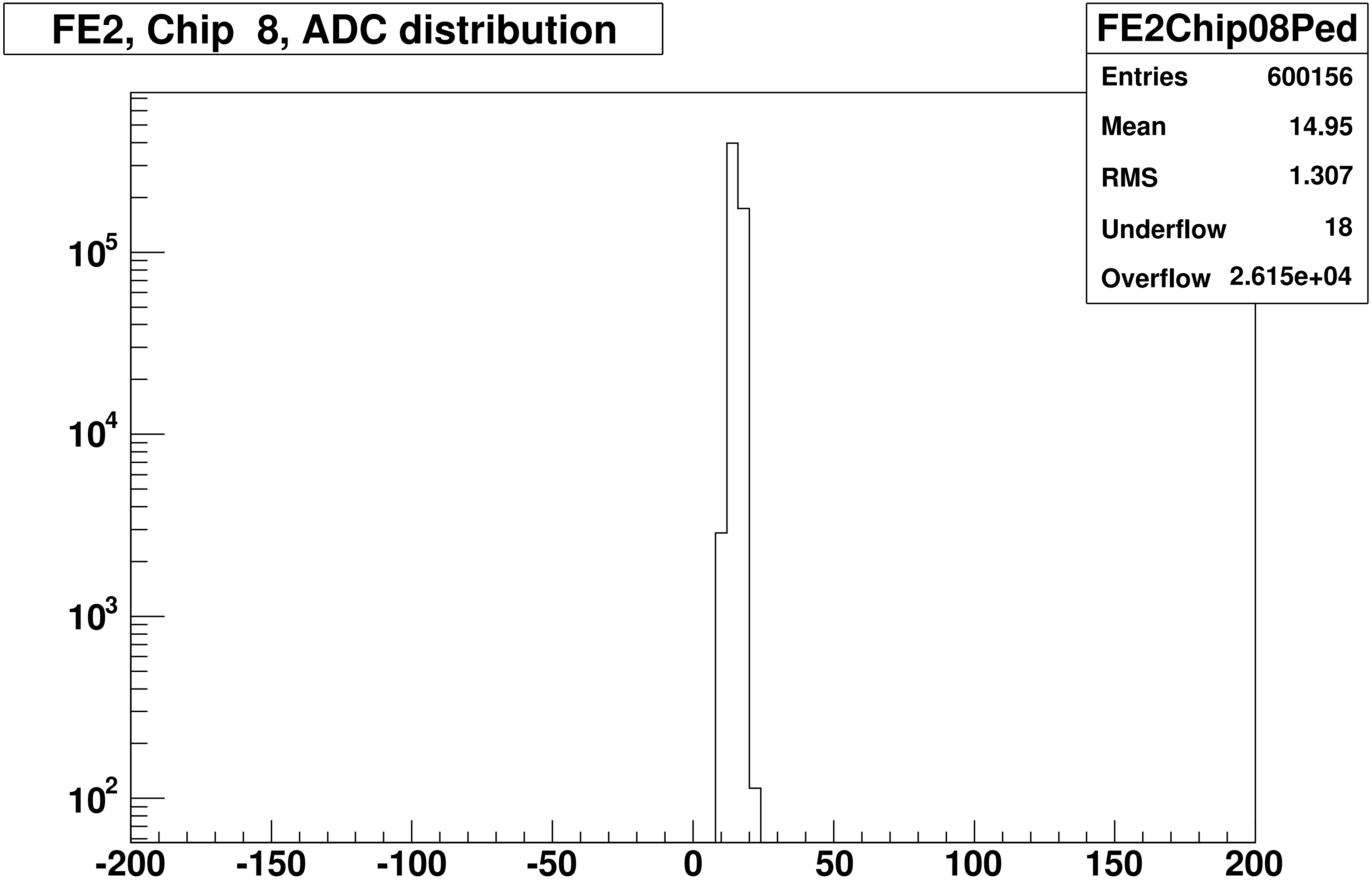
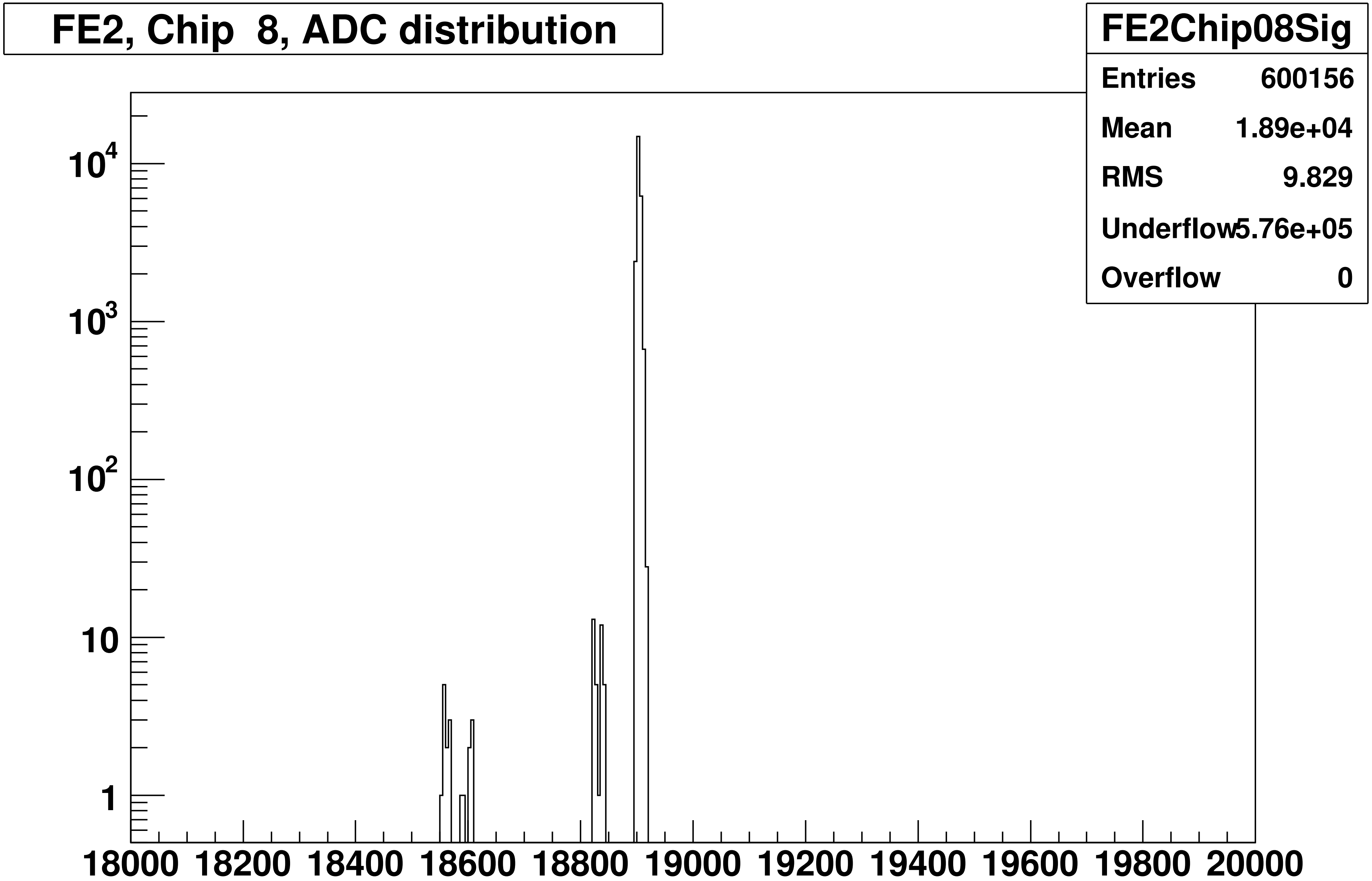
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE2, Chip 8, ADC distribution
FE2Chip08Ped
Entries 600156
Mean 14.95
RMS 1.307
Underflow 18
Overflow 2.615e+04
10^5
10^4
10^3
10^2
-200
-150
-100
-50
0
50
100
150
200


FE2, Chip 8, ADC distribution
FE2Chip08Sig
Entries 600156
Mean 1.89e+04
RMS 9.829
Underflow 5.76e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
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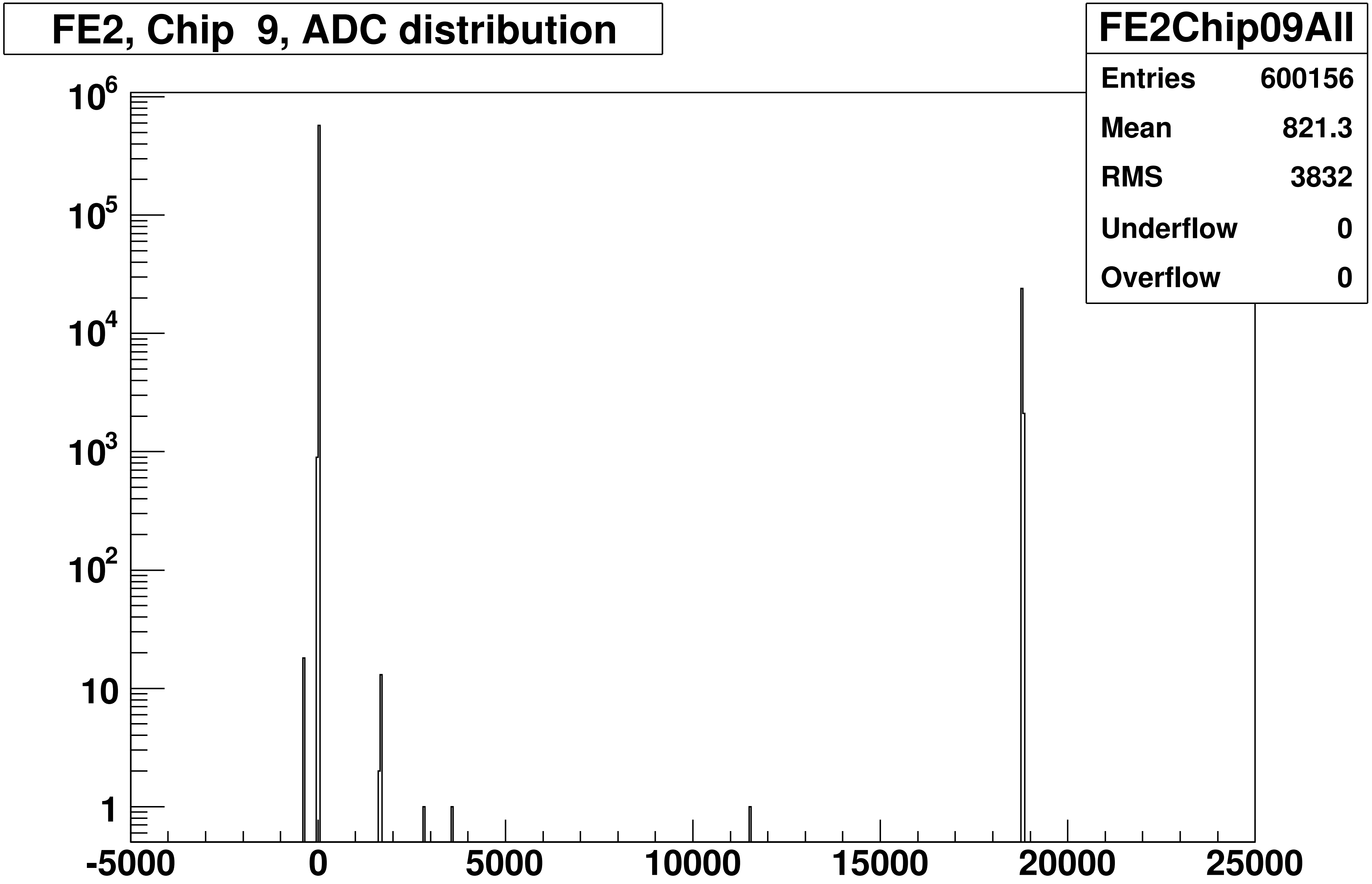

FE2, Chip 9, ADC distribution
FE2Chip09All
Entries 600156
Mean 821.3
RMS 3832
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
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-5000
0
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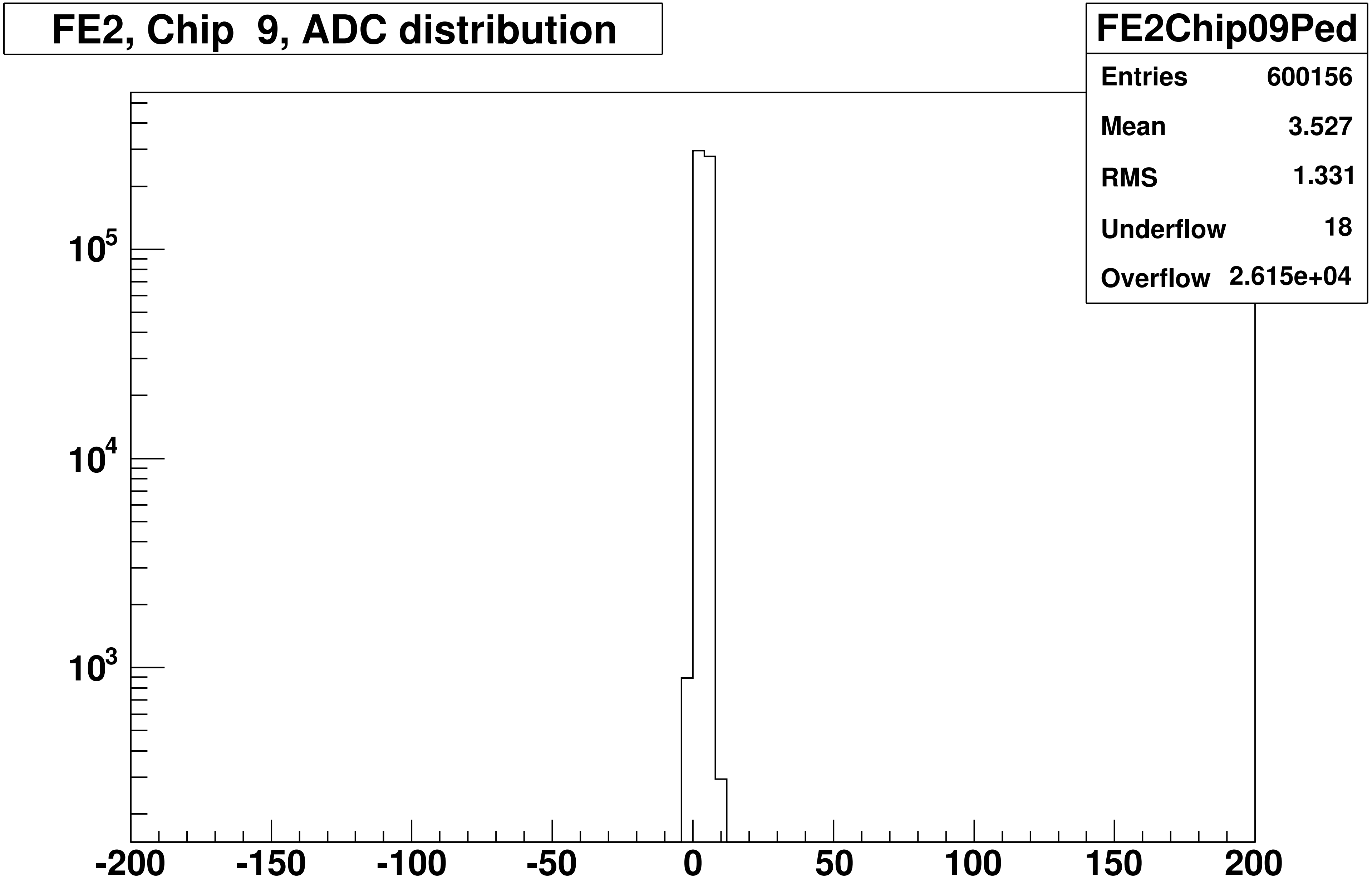
10000
15000
20000
25000


FE2, Chip 9, ADC distribution
FE2Chip09Ped
Entries 600156
Mean 3.527
RMS 1.331
Underflow 18
Overflow 2.615e+04
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10^4
10^3
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-150
-100
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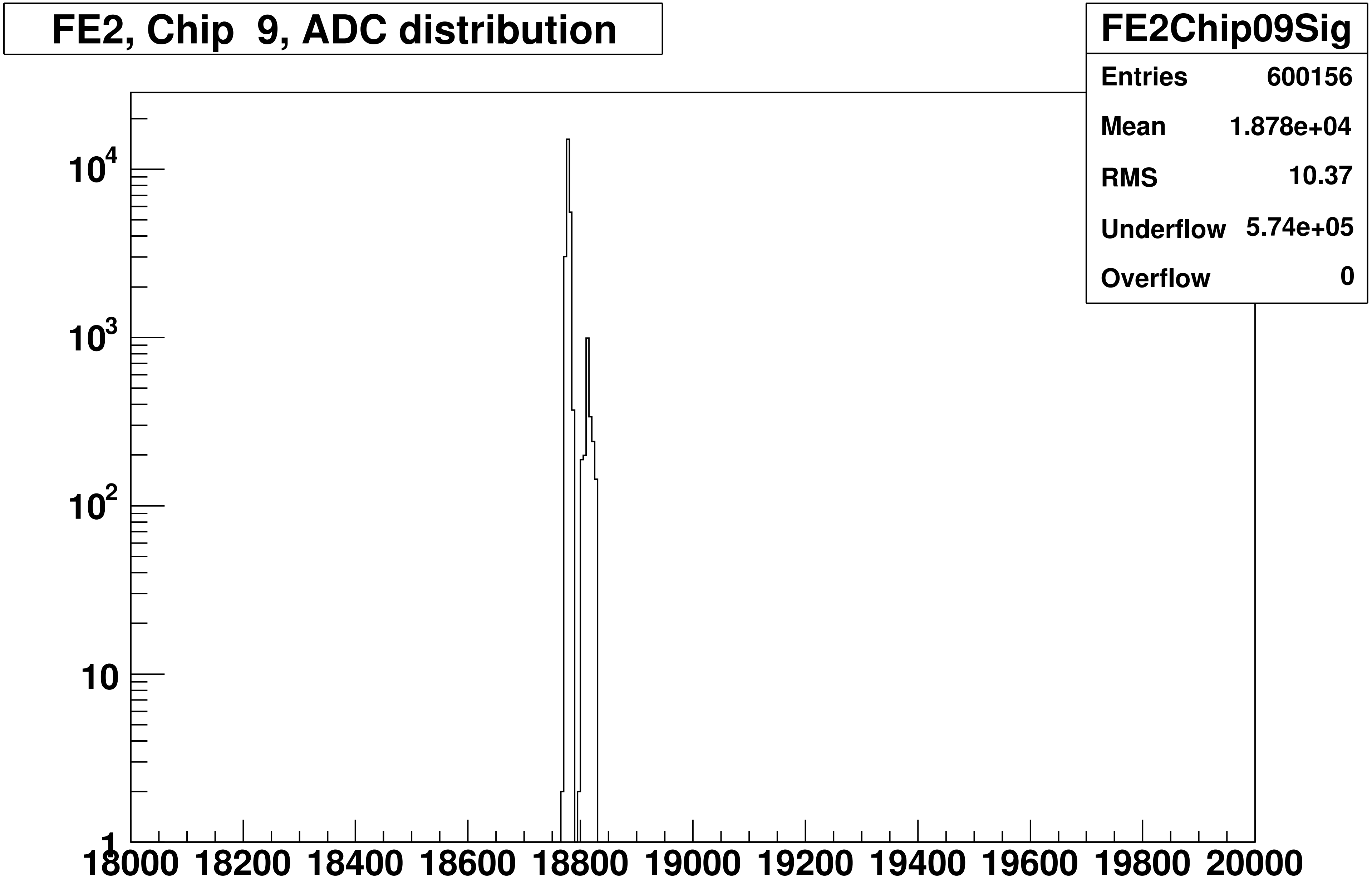
100
150
200



FE2, Chip 9, ADC distribution
FE2Chip09Sig
Entries 600156
Mean 1.878e+04
RMS 10.37
Underflow 5.74e+05
Overflow 0
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10^3
10^2
10
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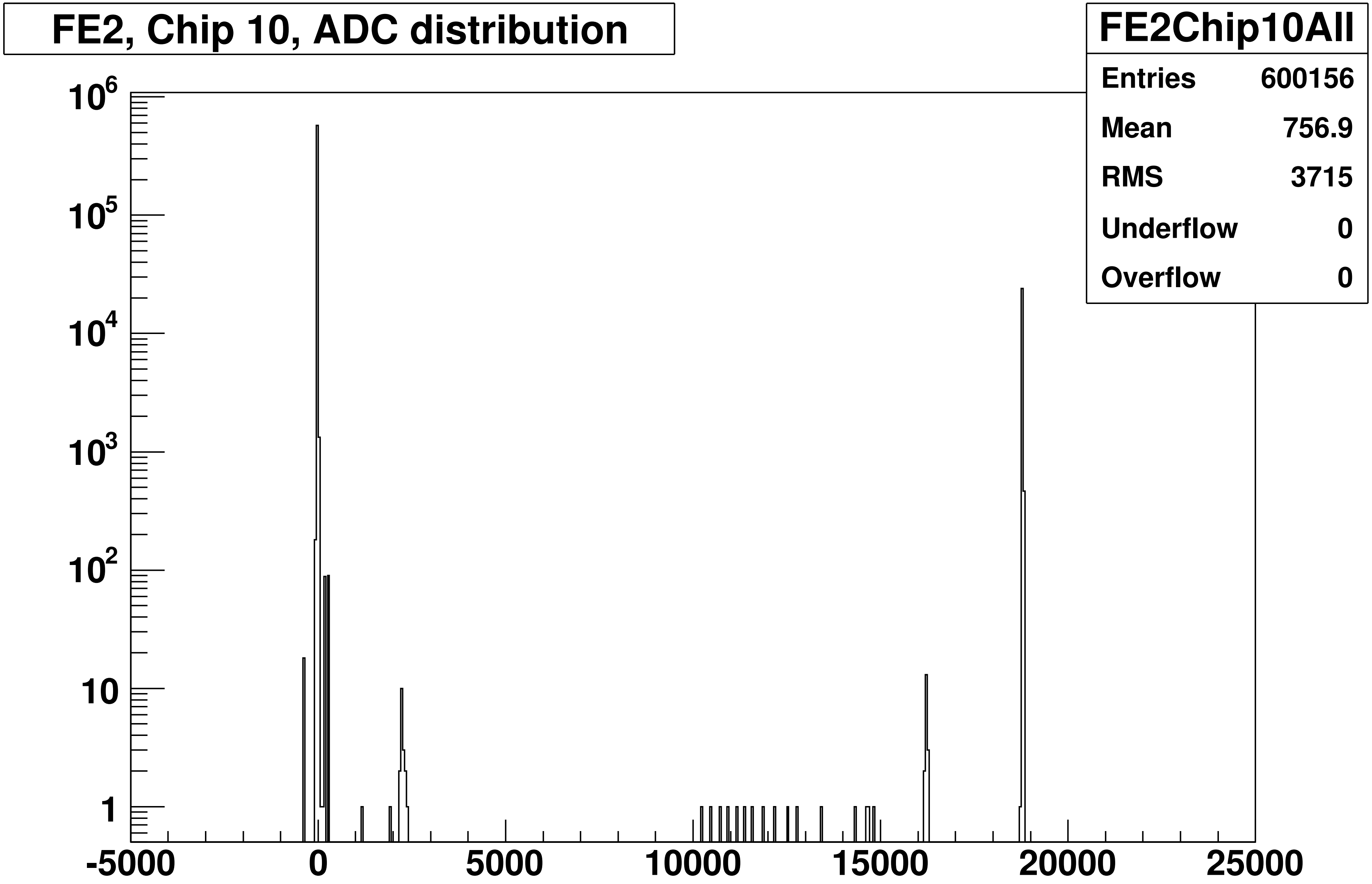
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE2, Chip 10, ADC distribution
FE2Chip10All
Entries 600156
Mean 756.9
RMS 3715
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
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10000
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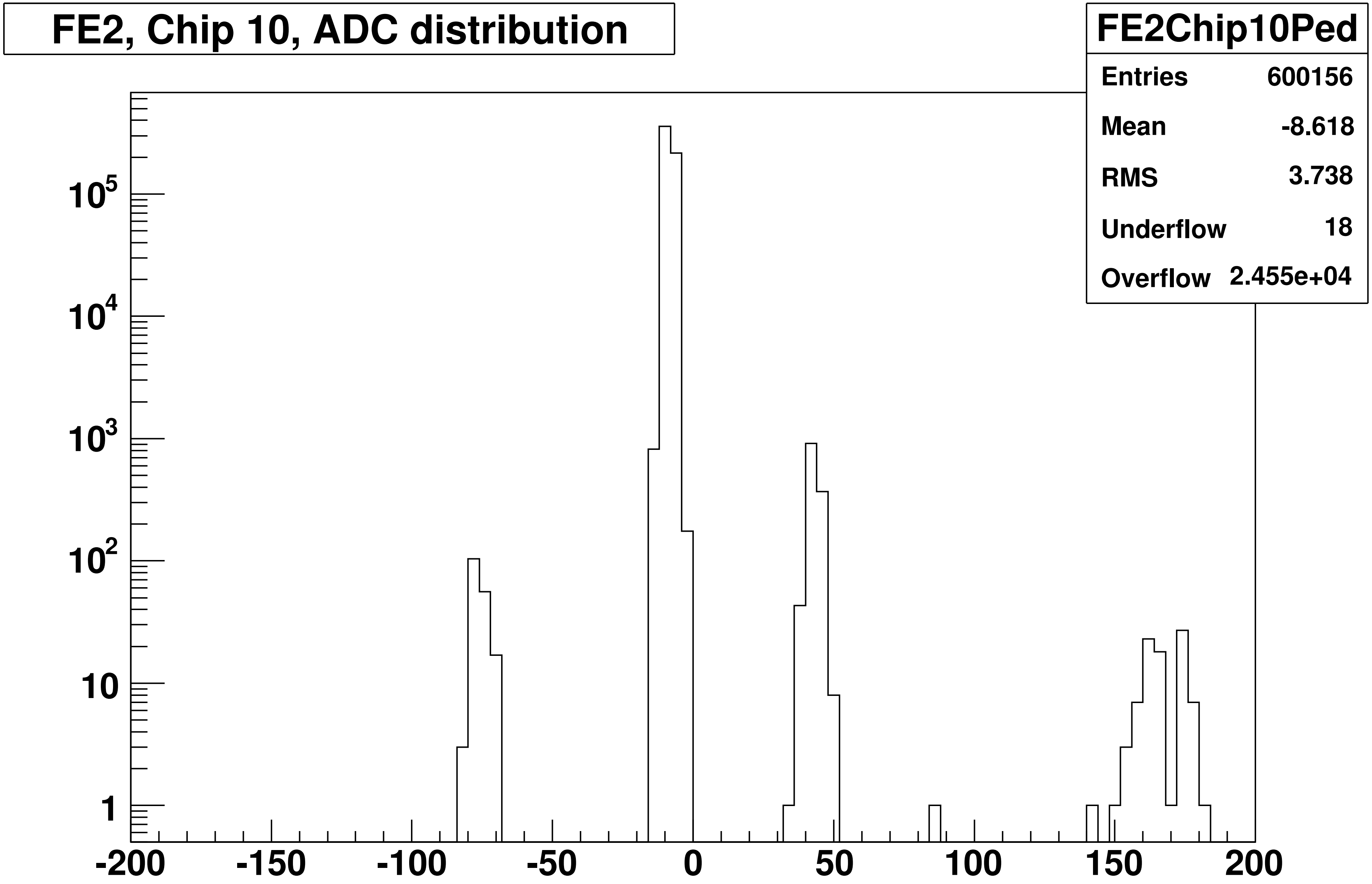
20000
25000


FE2, Chip 10, ADC distribution
FE2Chip10Ped
Entries 600156
Mean -8.618
RMS 3.738
Underflow 18
Overflow 2.455e+04
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10^4
10^3
10^2
10
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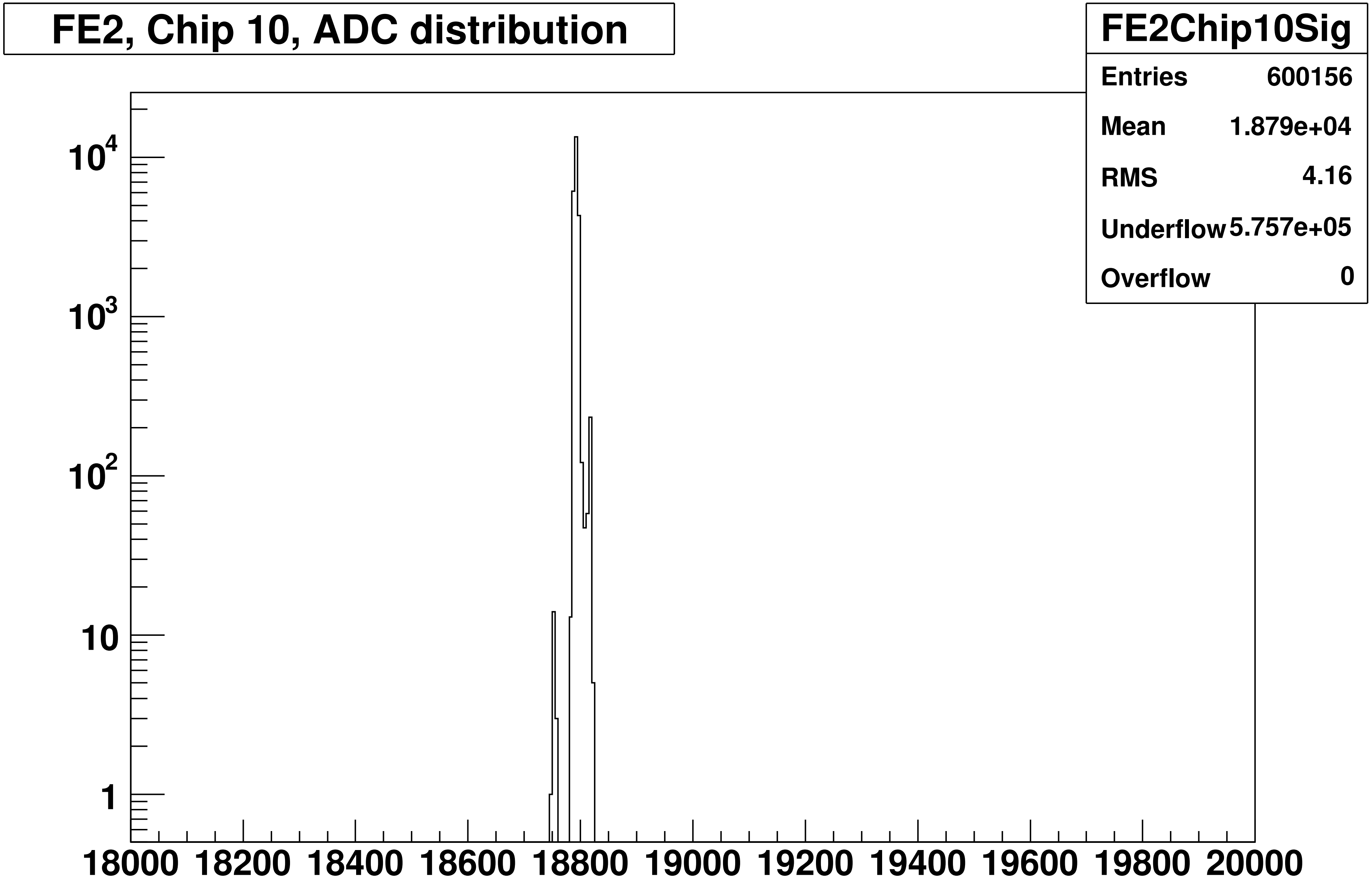
FE2, Chip 10, ADC distribution
FE2Chip10Sig
Entries 600156
Mean 1.879e+04
RMS 4.16
Underflow 5.757e+05
Overflow 0
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10^3
10^2
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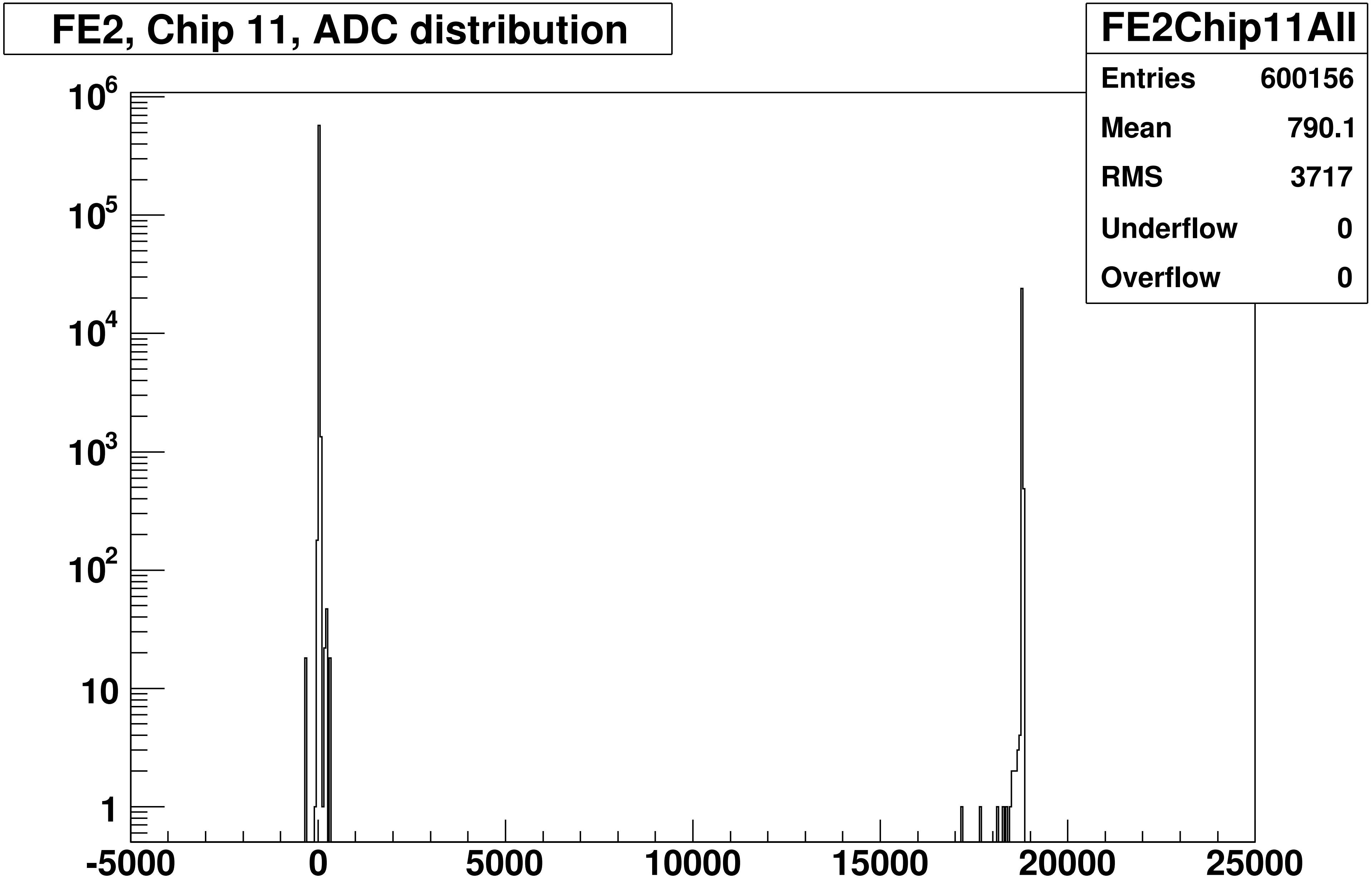

FE2, Chip 11, ADC distribution
FE2Chip11All
Entries 600156
Mean 790.1
RMS 3717
Underflow 0
Overflow 0
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10^3
10^2
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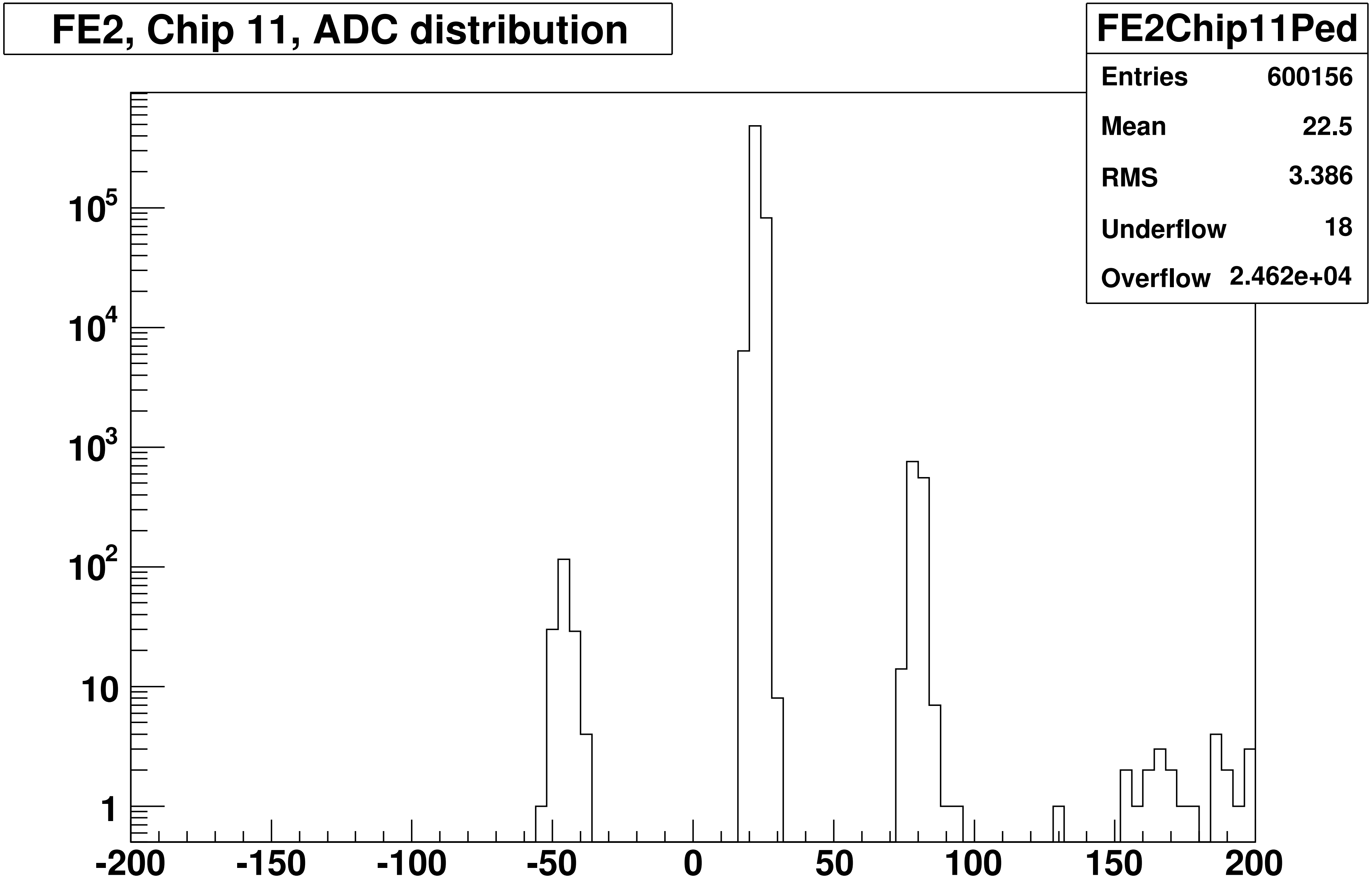
FE2, Chip 11, ADC distribution
FE2Chip11Ped
Entries 600156
Mean 22.5
RMS 3.386
Underflow 18
Overflow 2.462e+04
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10^3
10^2
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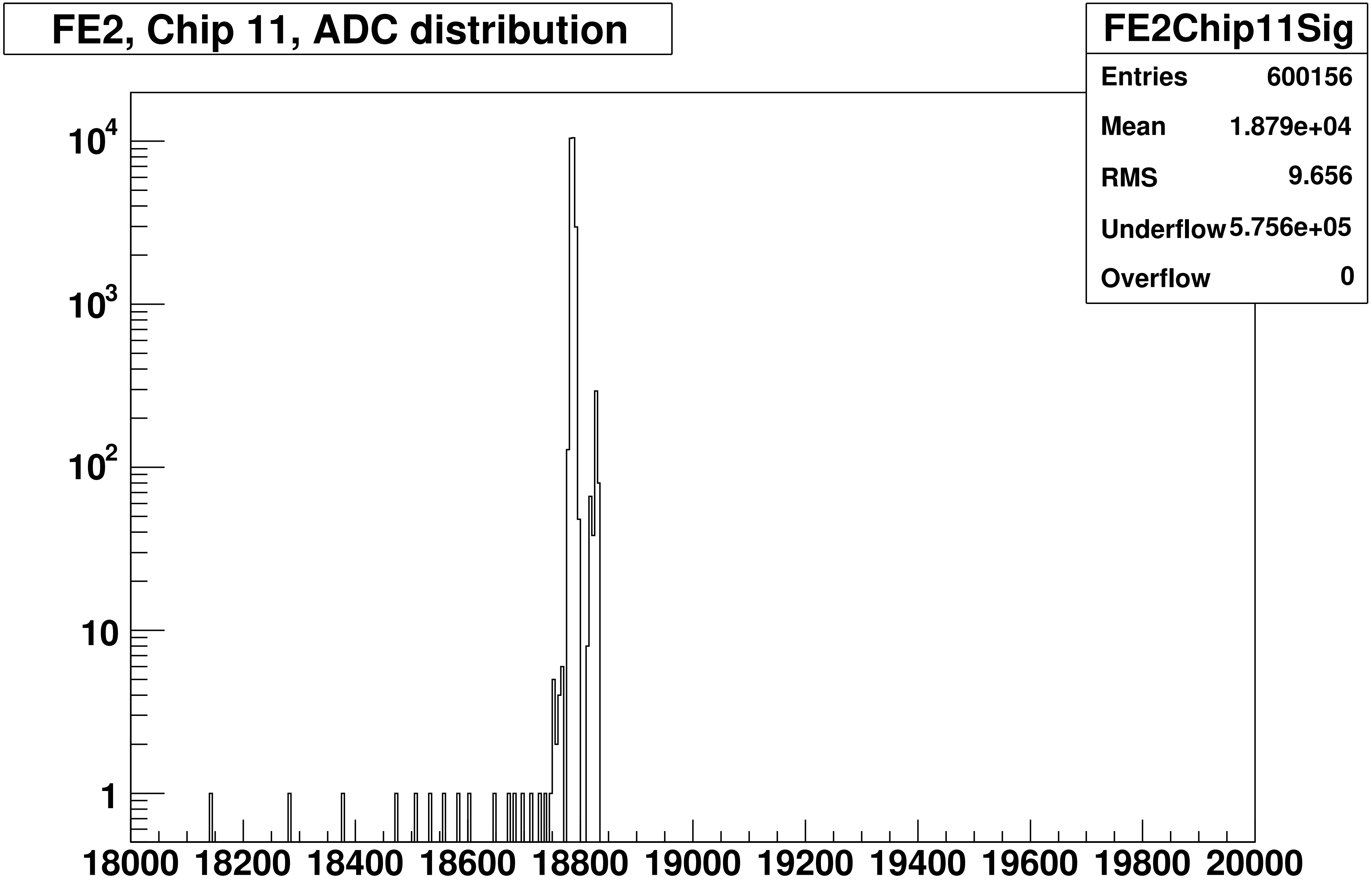
FE2, Chip 11, ADC distribution
FE2Chip11Sig
Entries 600156
Mean 1.879e+04
RMS 9.656
Underflow 5.756e+05
Overflow 0
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10^3
10^2
10
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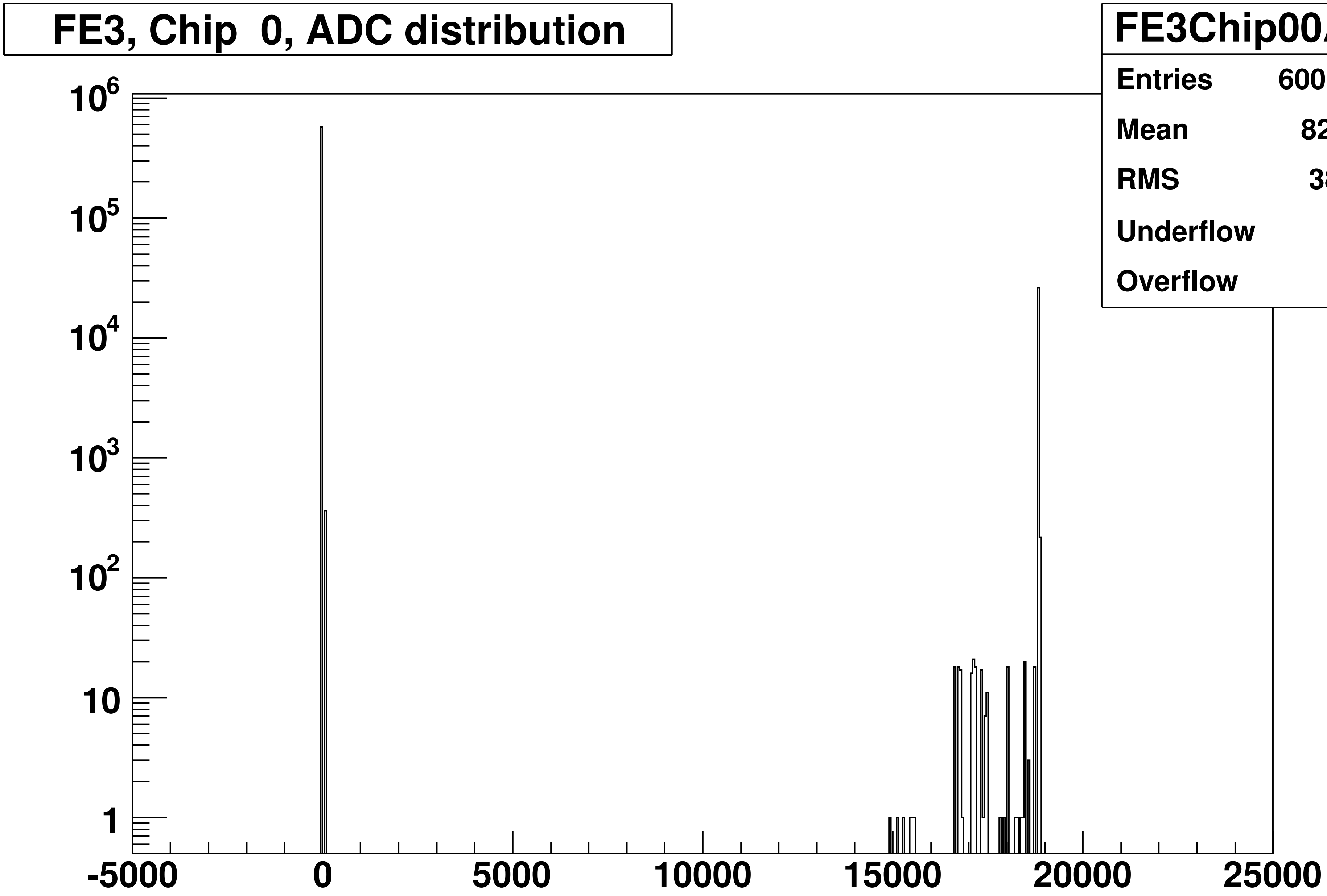
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE3, Chip 0, ADC distribution
FE3Chip00All
Entries 600156
Mean 820.3
RMS 3893
Underflow 0
Overflow 0
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10^3
10^2
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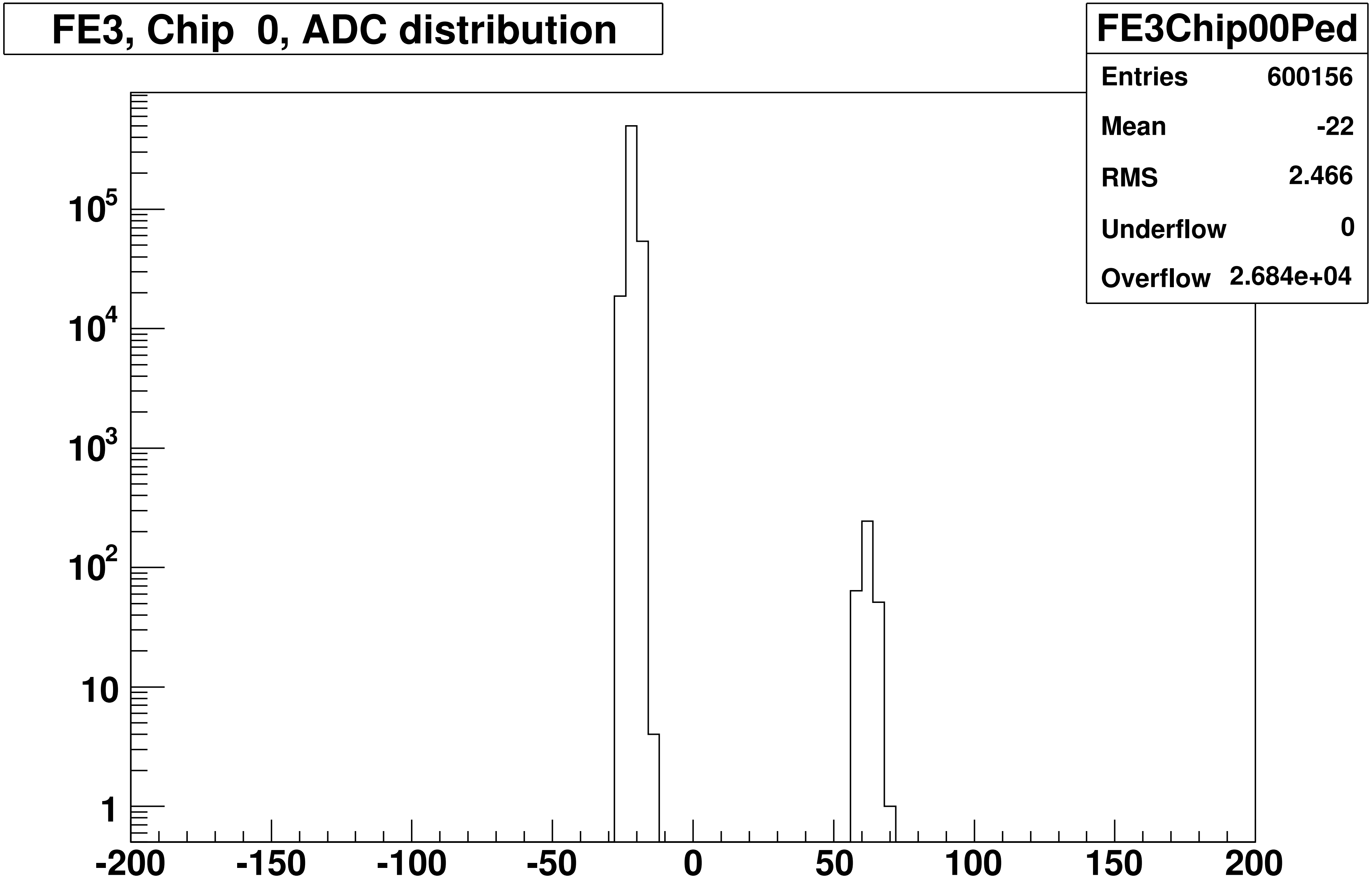
25000


FE3, Chip 0, ADC distribution
FE3Chip00Ped
Entries 600156
Mean -22
RMS 2.466
Underflow 0
Overflow 2.684e+04
10^5
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10^3
10^2
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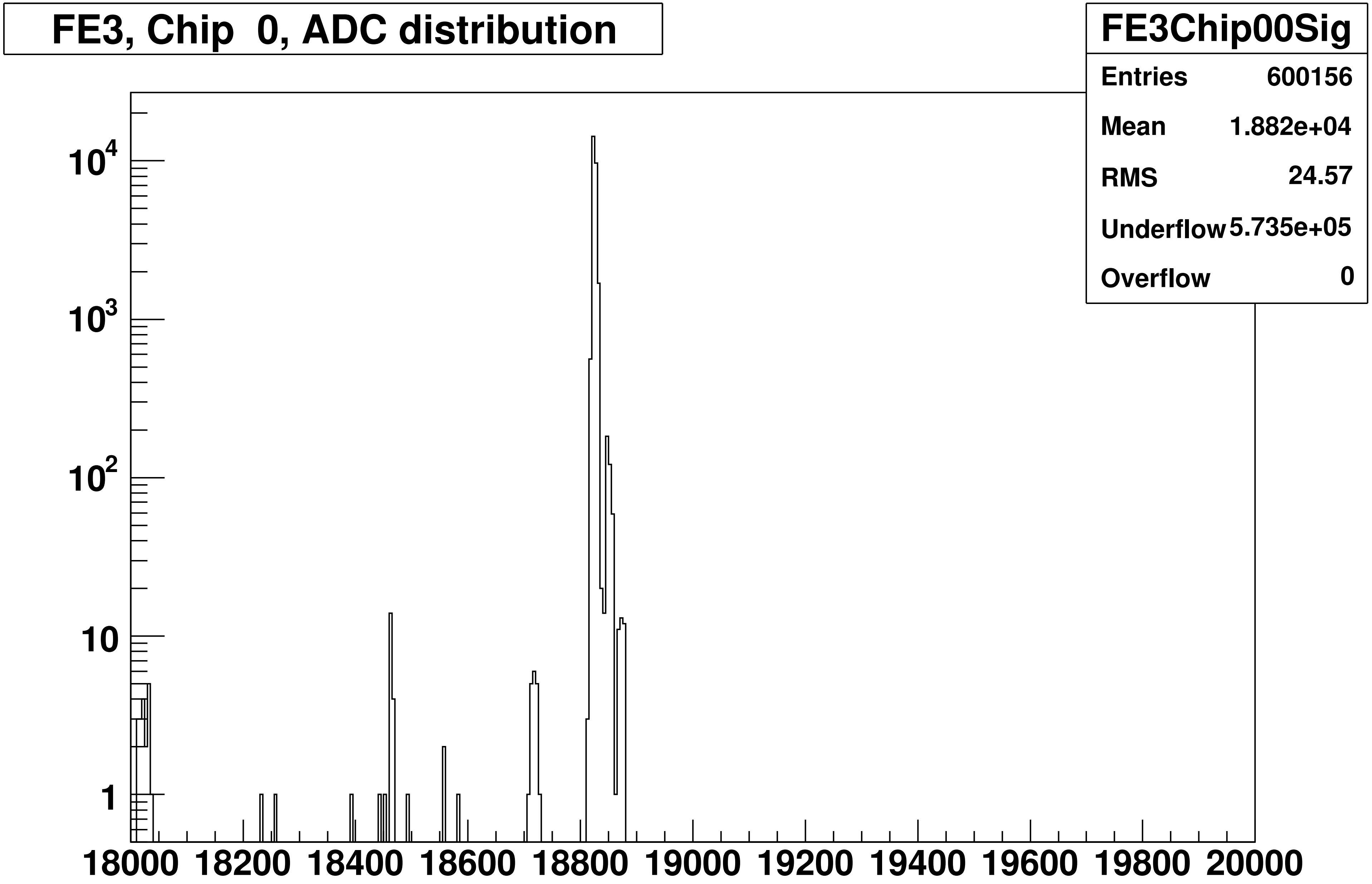
150
200



FE3, Chip 0, ADC distribution
FE3Chip00Sig
Entries 600156
Mean 1.882e+04
RMS 24.57
Underflow 5.735e+05
Overflow 0
10^4
10^3
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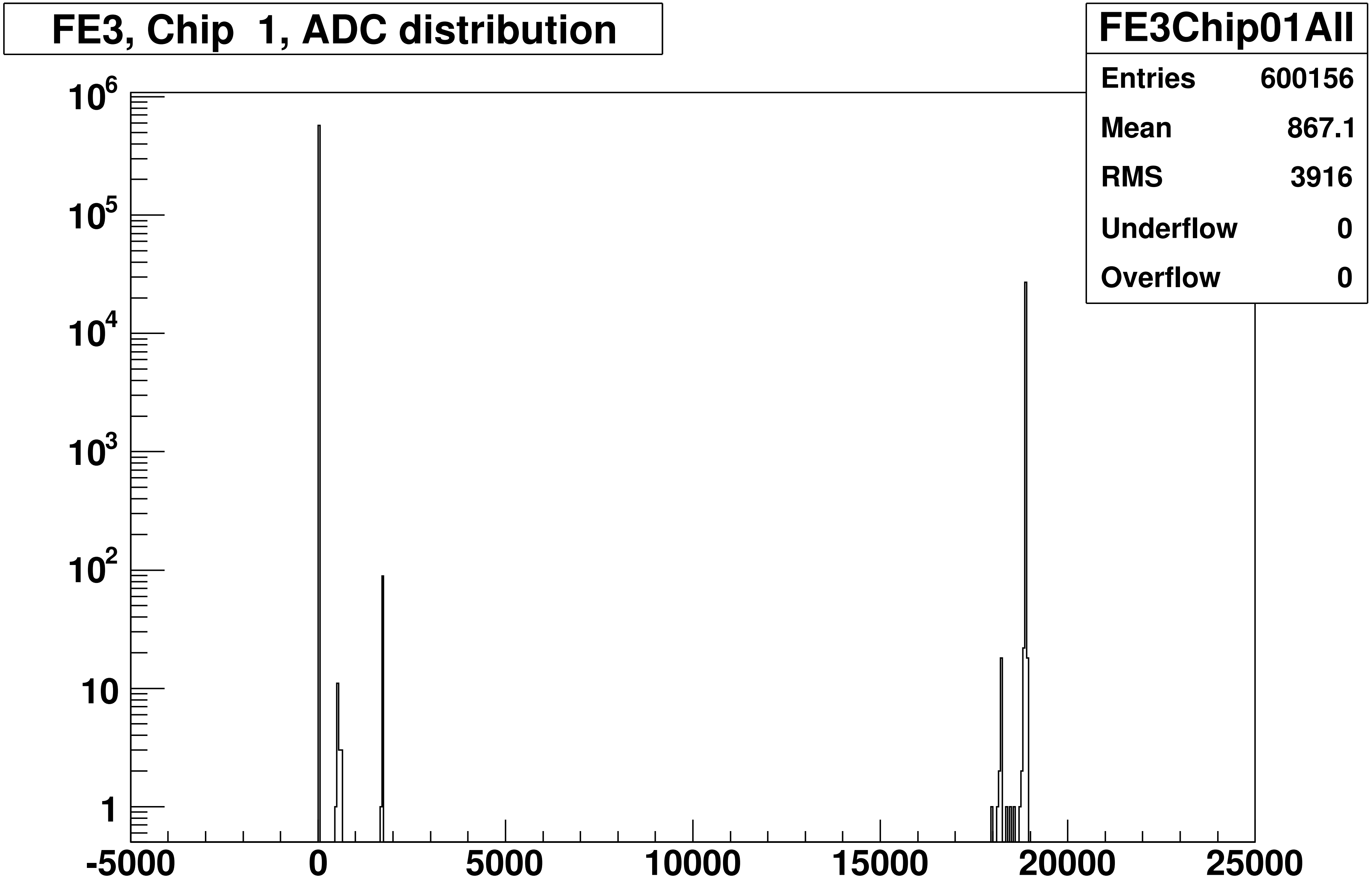
20000


FE3, Chip 1, ADC distribution
FE3Chip01All
Entries 600156
Mean 867.1
RMS 3916
Underflow 0
Overflow 0
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10^4
10^3
10^2
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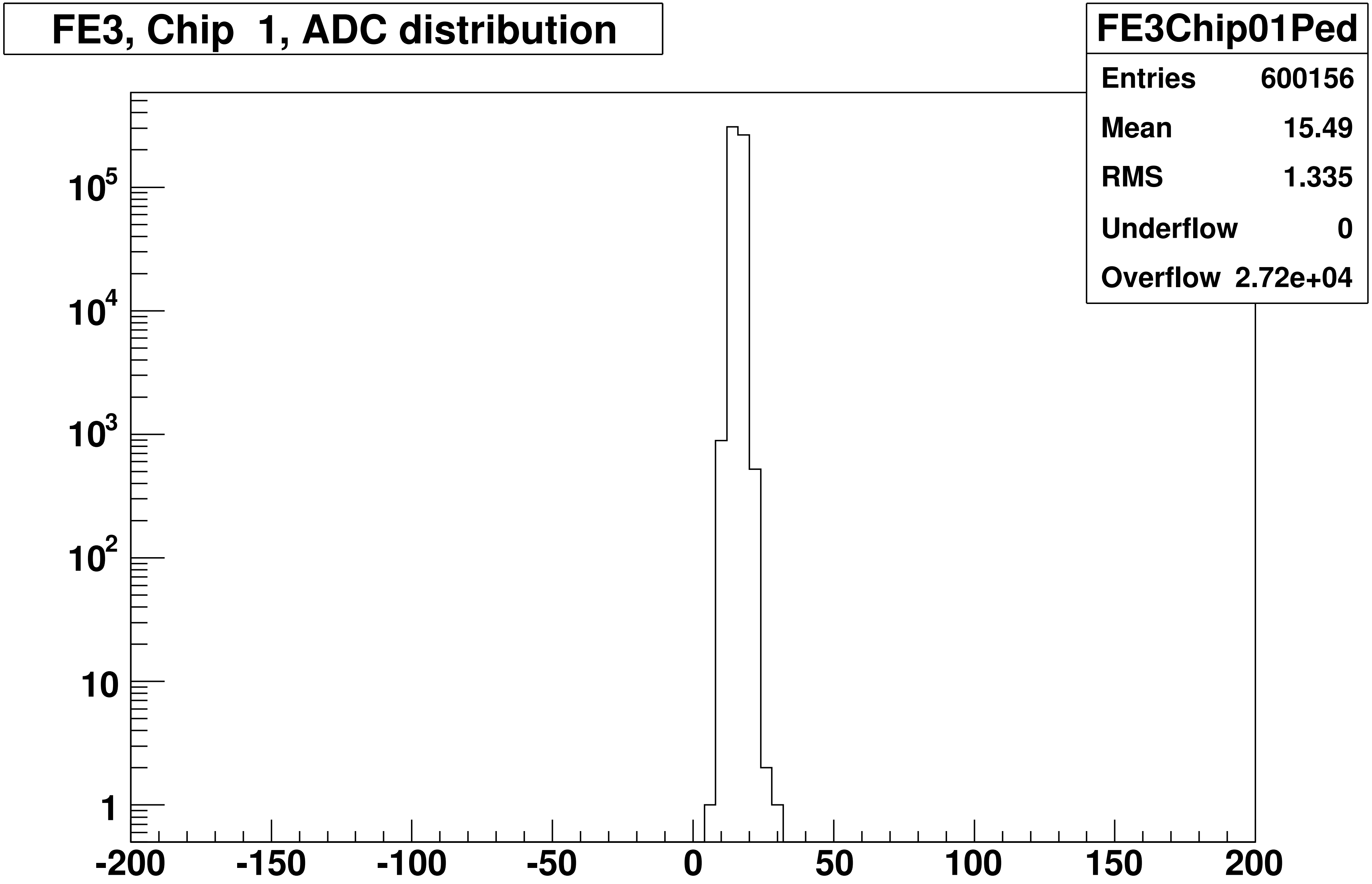
25000



FE3, Chip 1, ADC distribution
FE3Chip01Ped
Entries 600156
Mean 15.49
RMS 1.335
Underflow 0
Overflow 2.72e+04
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10^3
10^2
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-100
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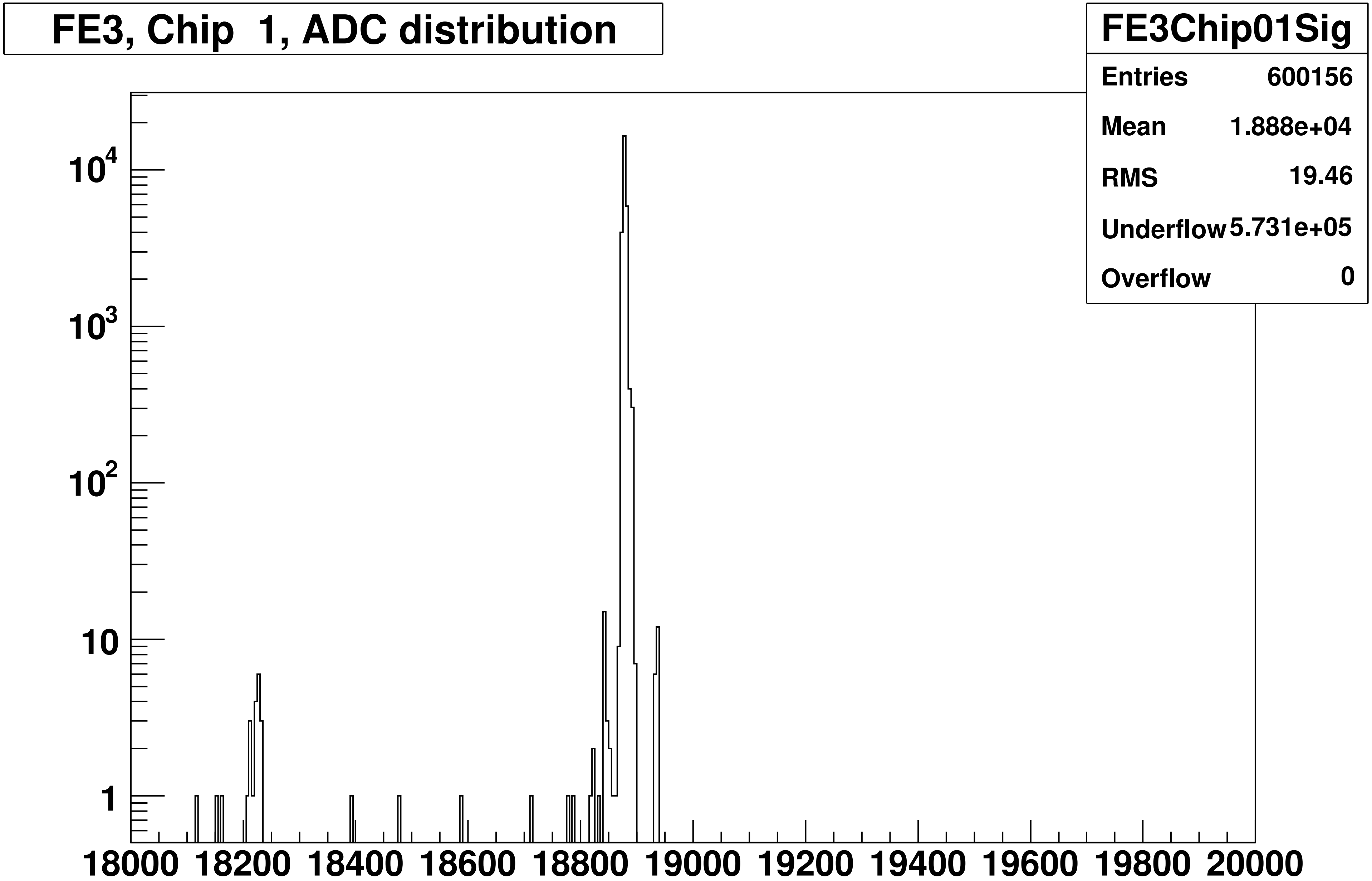
100
150
200


FE3, Chip 1, ADC distribution
FE3Chip01Sig
Entries 600156
Mean 1.888e+04
RMS 19.46
Underflow 5.731e+05
Overflow 0
10^4
10^3
10^2
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19000
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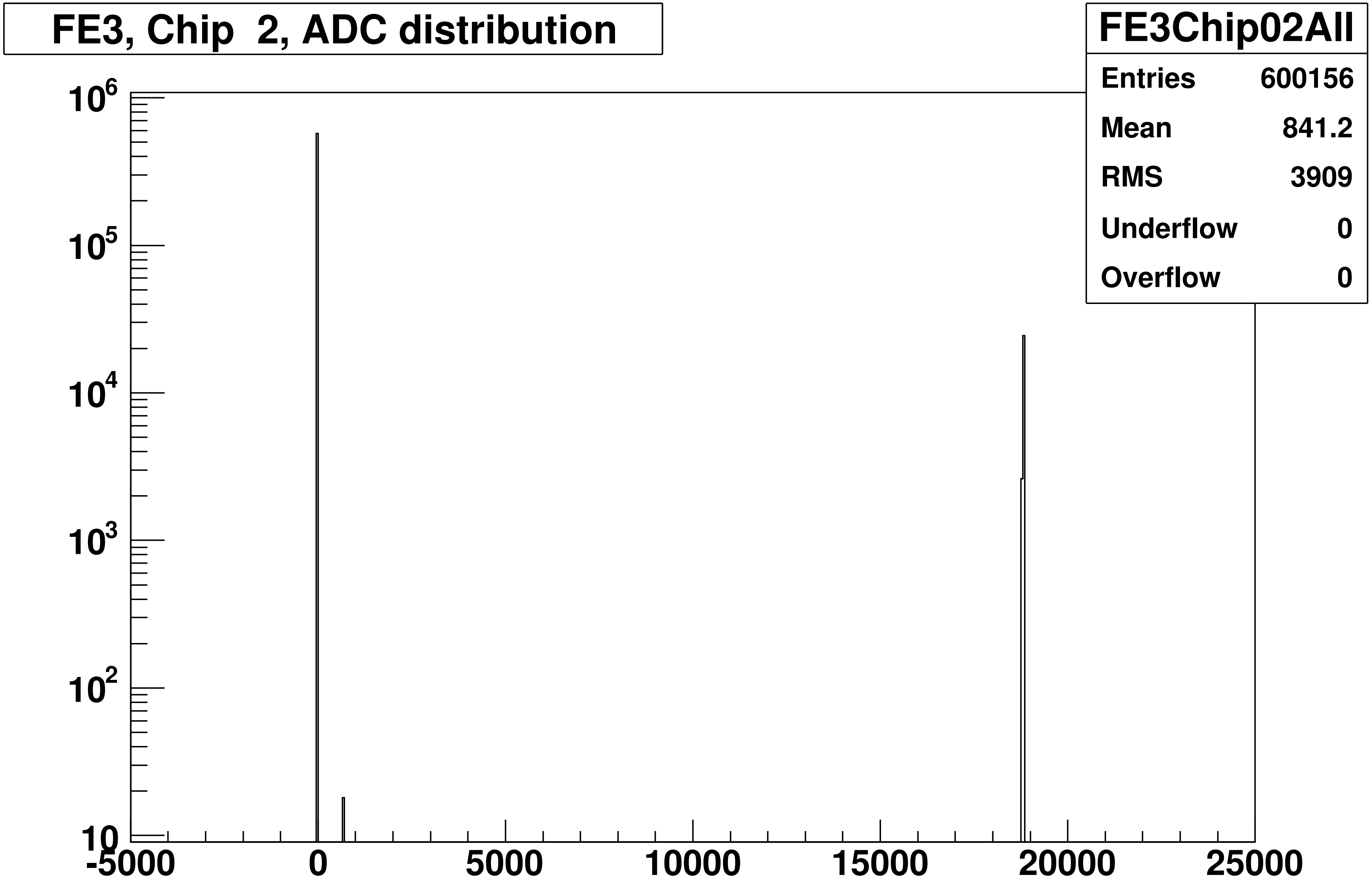

FE3, Chip 2, ADC distribution
FE3Chip02All
Entries 600156
Mean 841.2
RMS 3909
Underflow 0
Overflow 0
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10^5
10^4
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10^2
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0
5000
10000
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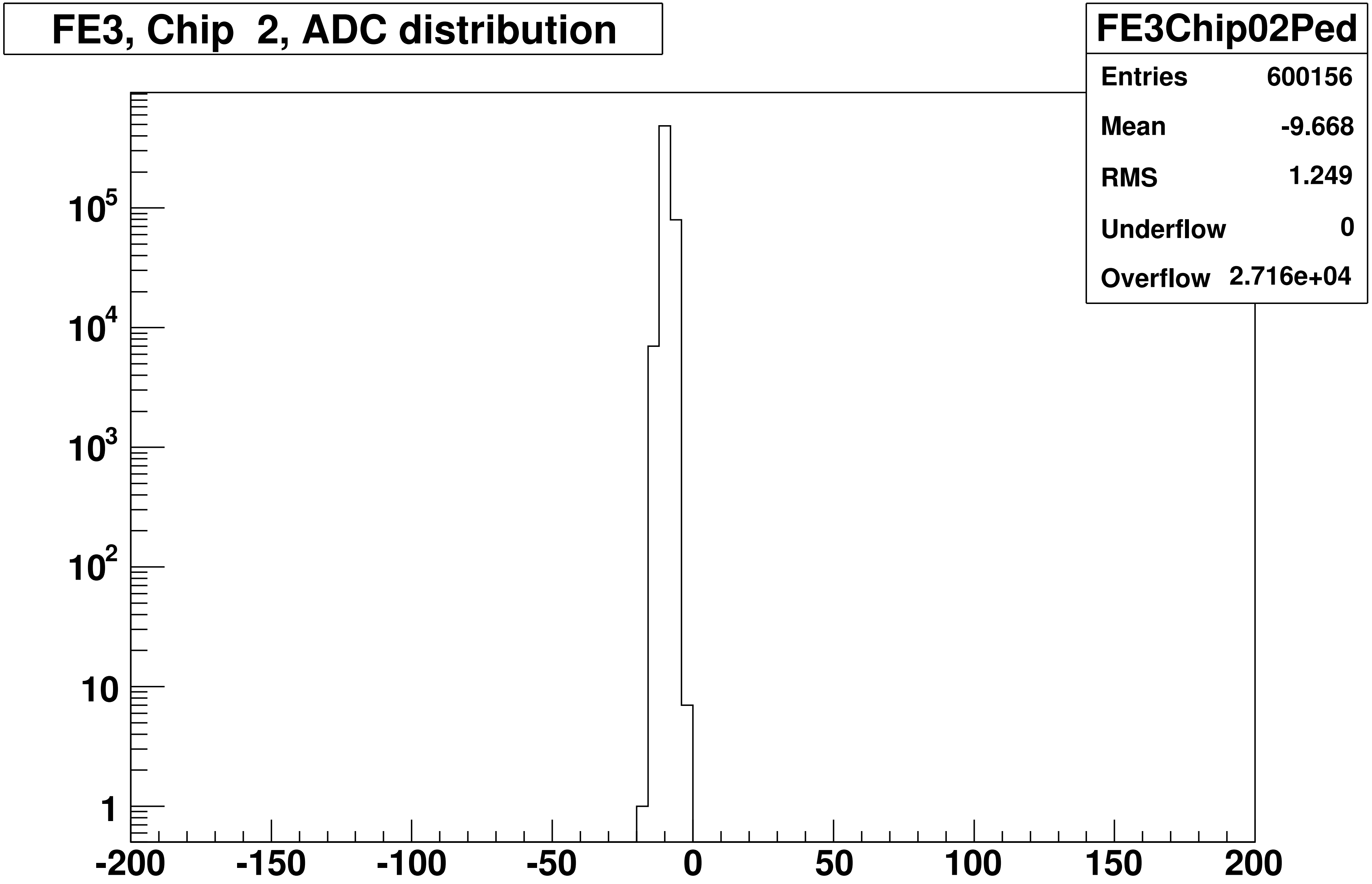
FE3, Chip 2, ADC distribution
FE3Chip02Ped
Entries 600156
Mean -9.668
RMS 1.249
Underflow 0
Overflow 2.716e+04
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10^2
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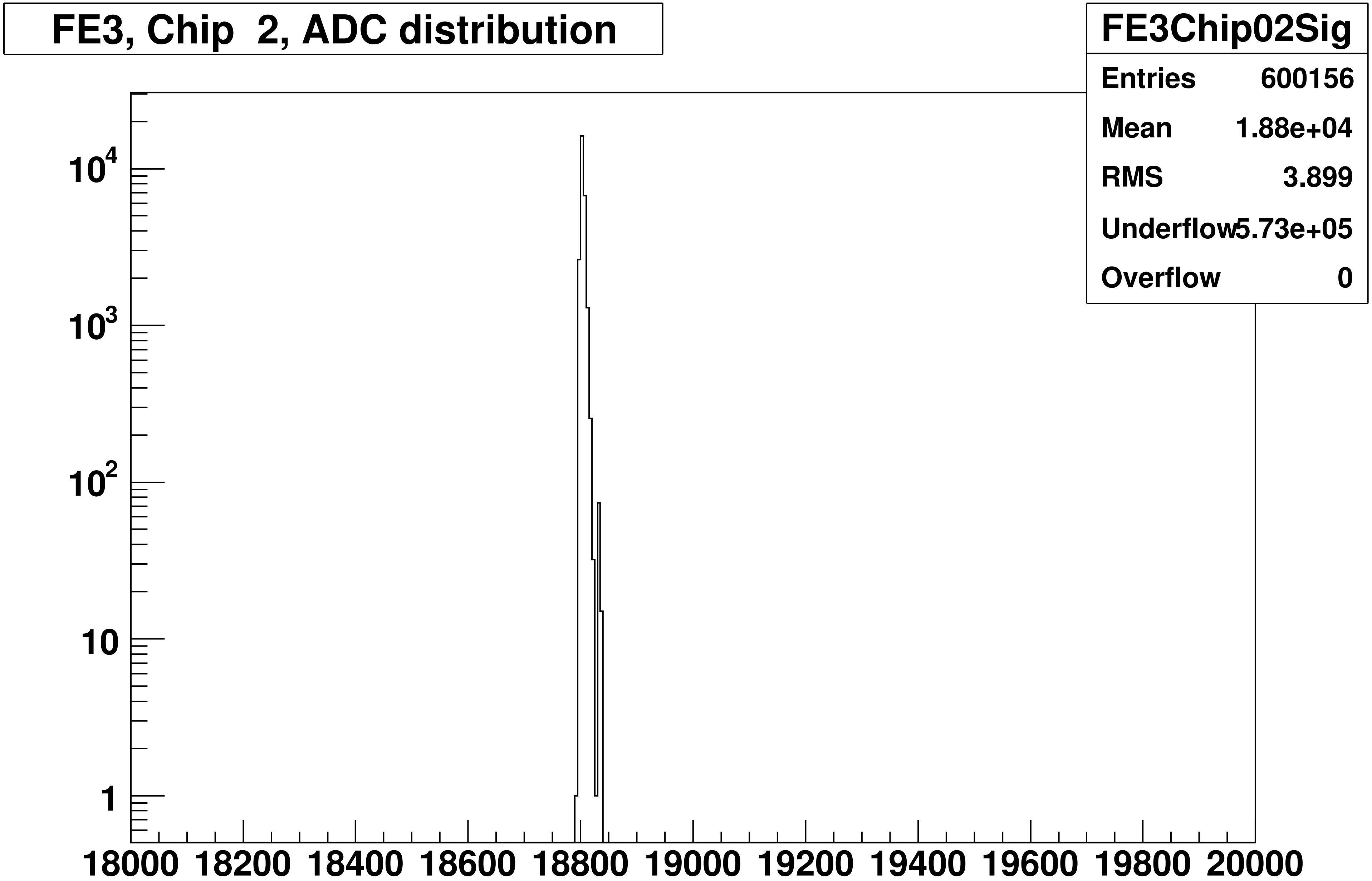
FE3, Chip 2, ADC distribution
FE3Chip02Sig
Entries 600156
Mean 1.88e+04
RMS 3.899
Underflow 5.73e+05
Overflow 0
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10^3
10^2
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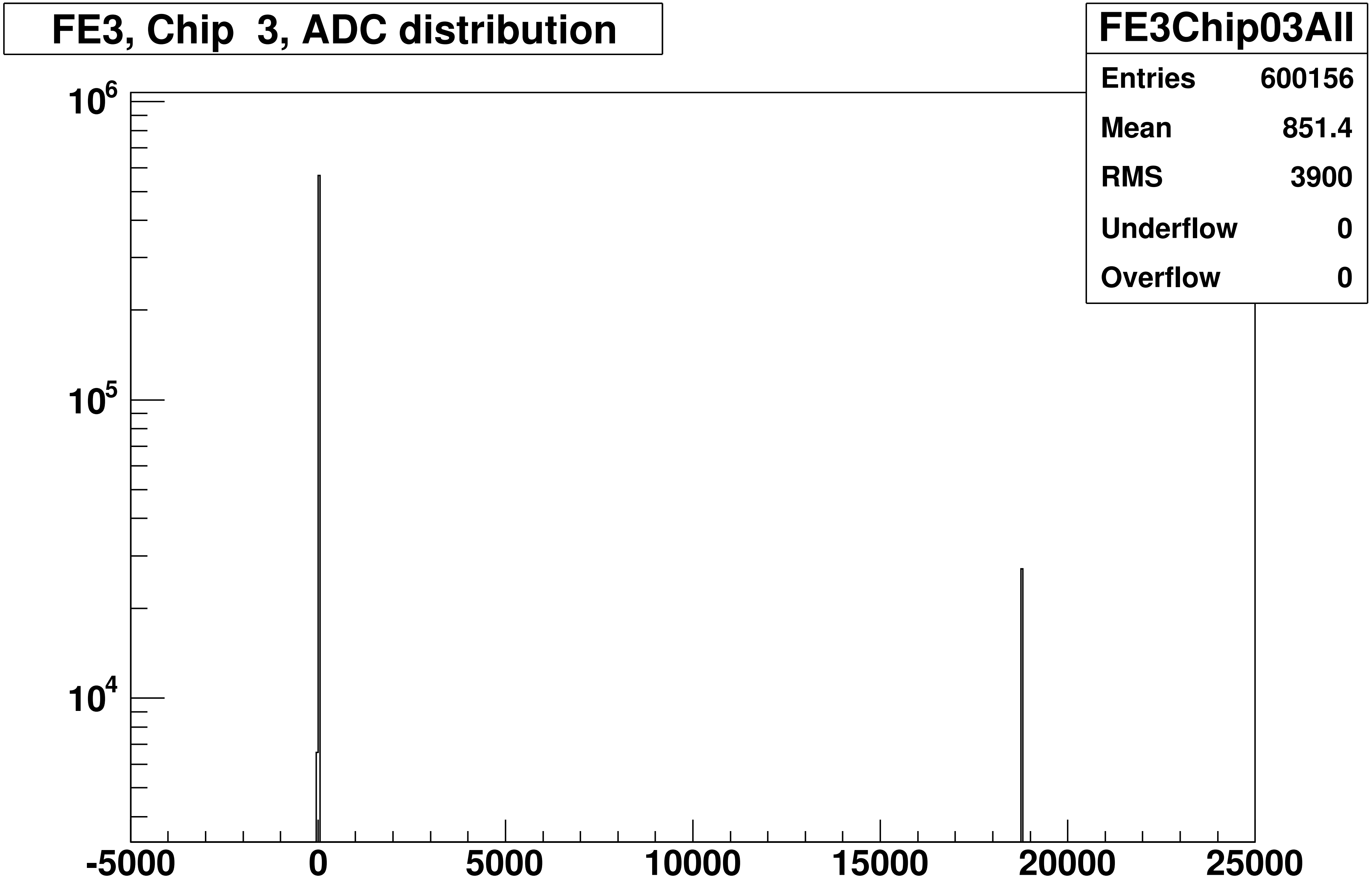
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE3, Chip 3, ADC distribution
FE3Chip03All
Entries 600156
Mean 851.4
RMS 3900
Underflow 0
Overflow 0
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10^4
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0
5000
10000
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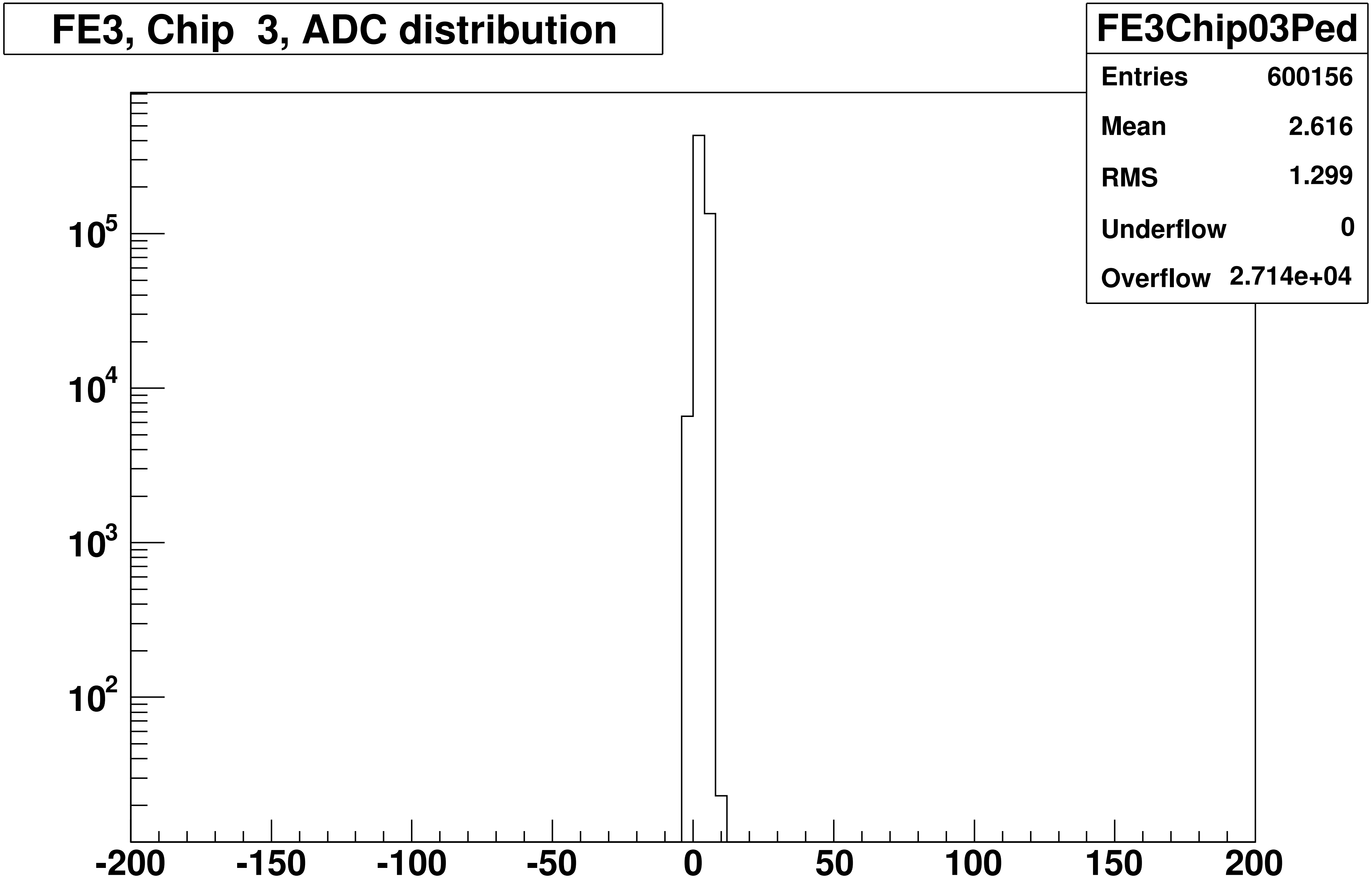
20000
25000



FE3, Chip 3, ADC distribution
FE3Chip03Ped
Entries 600156
Mean 2.616
RMS 1.299
Underflow 0
Overflow 2.714e+04
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10^4
10^3
10^2
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-100
-50
0
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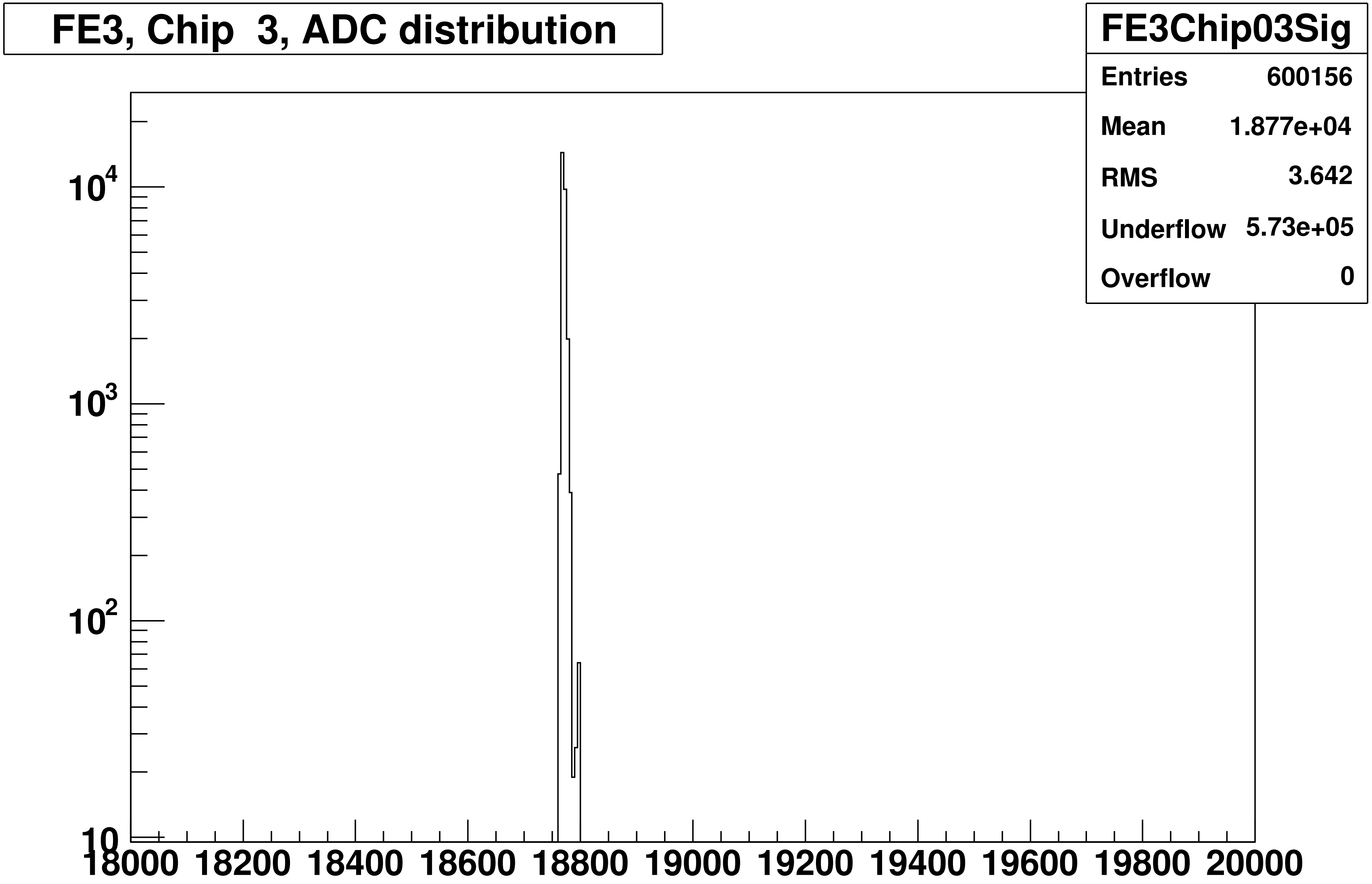
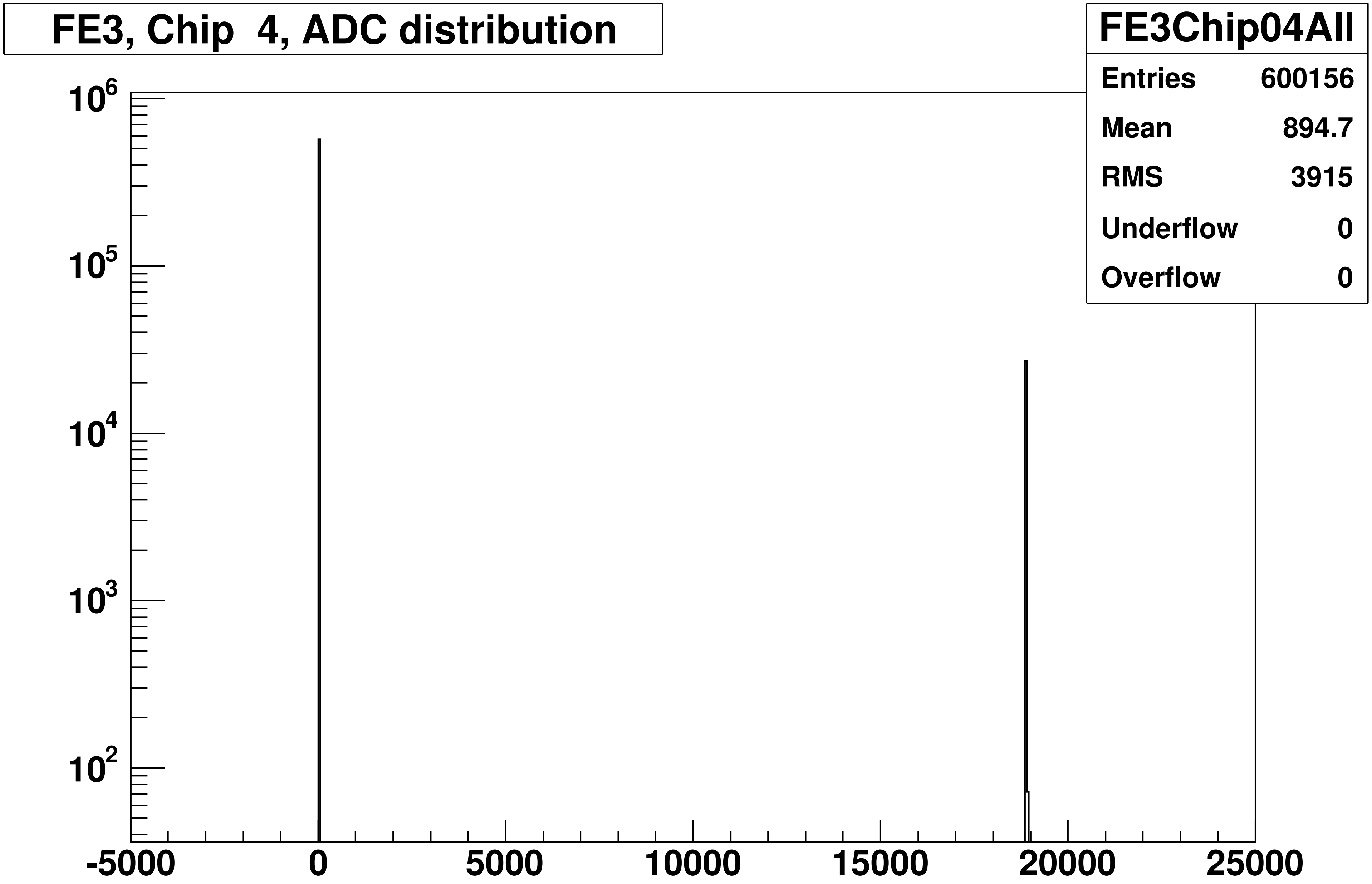
100
150
200


FE3, Chip 3, ADC distribution
FE3Chip03Sig
Entries 600156
Mean 1.877e+04
RMS 3.642
Underflow 5.73e+05
Overflow 0
10
10^2
10^3
10^4
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE3, Chip 4, ADC distribution
FE3Chip04All
Entries 600156
Mean 894.7
RMS 3915
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
-5000
0
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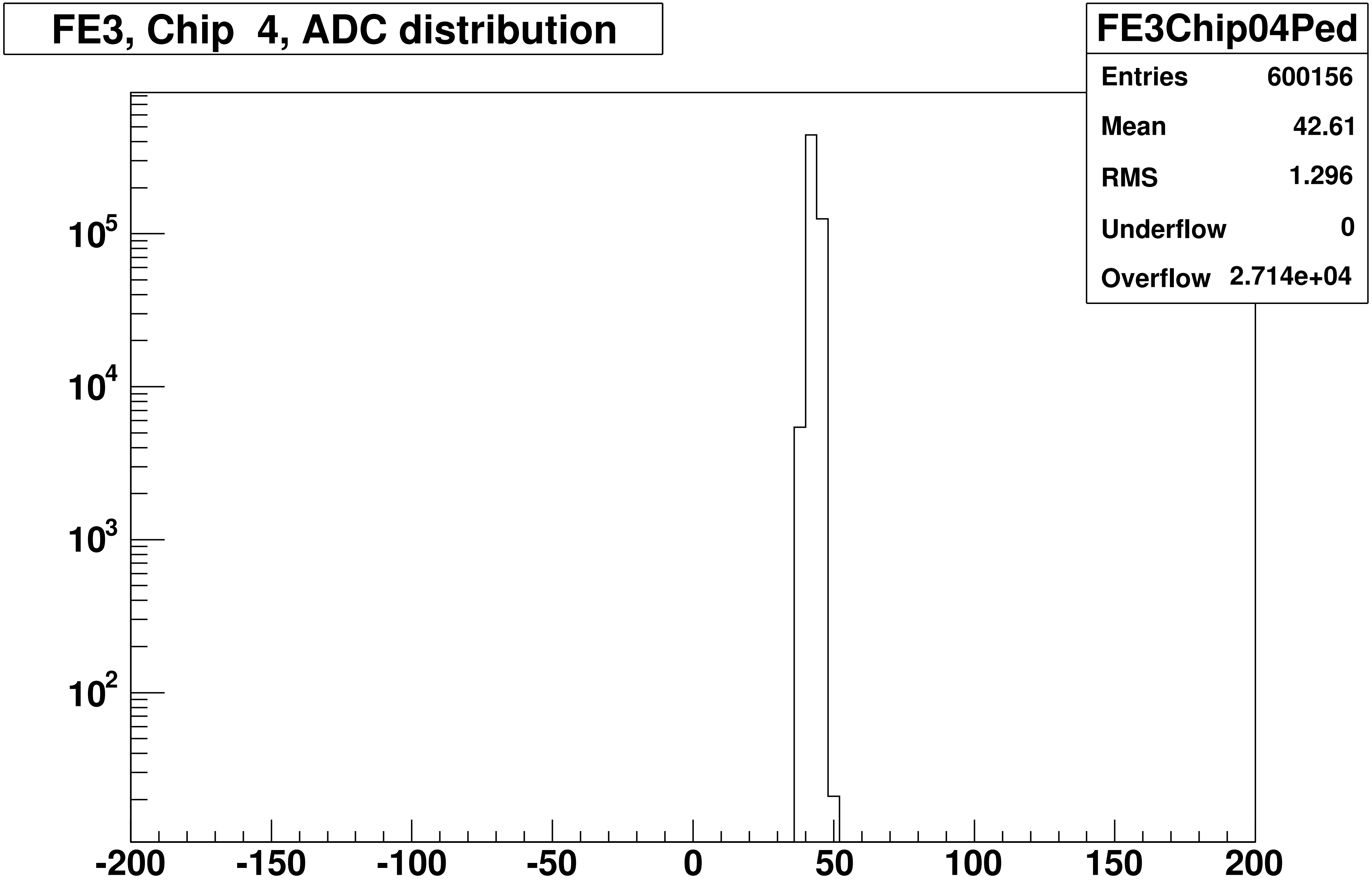
10000
15000
20000
25000


FE3, Chip 4, ADC distribution
FE3Chip04Ped
Entries 600156
Mean 42.61
RMS 1.296
Underflow 0
Overflow 2.714e+04
10^5
10^4
10^3
10^2
-200
-150
-100
-50
0
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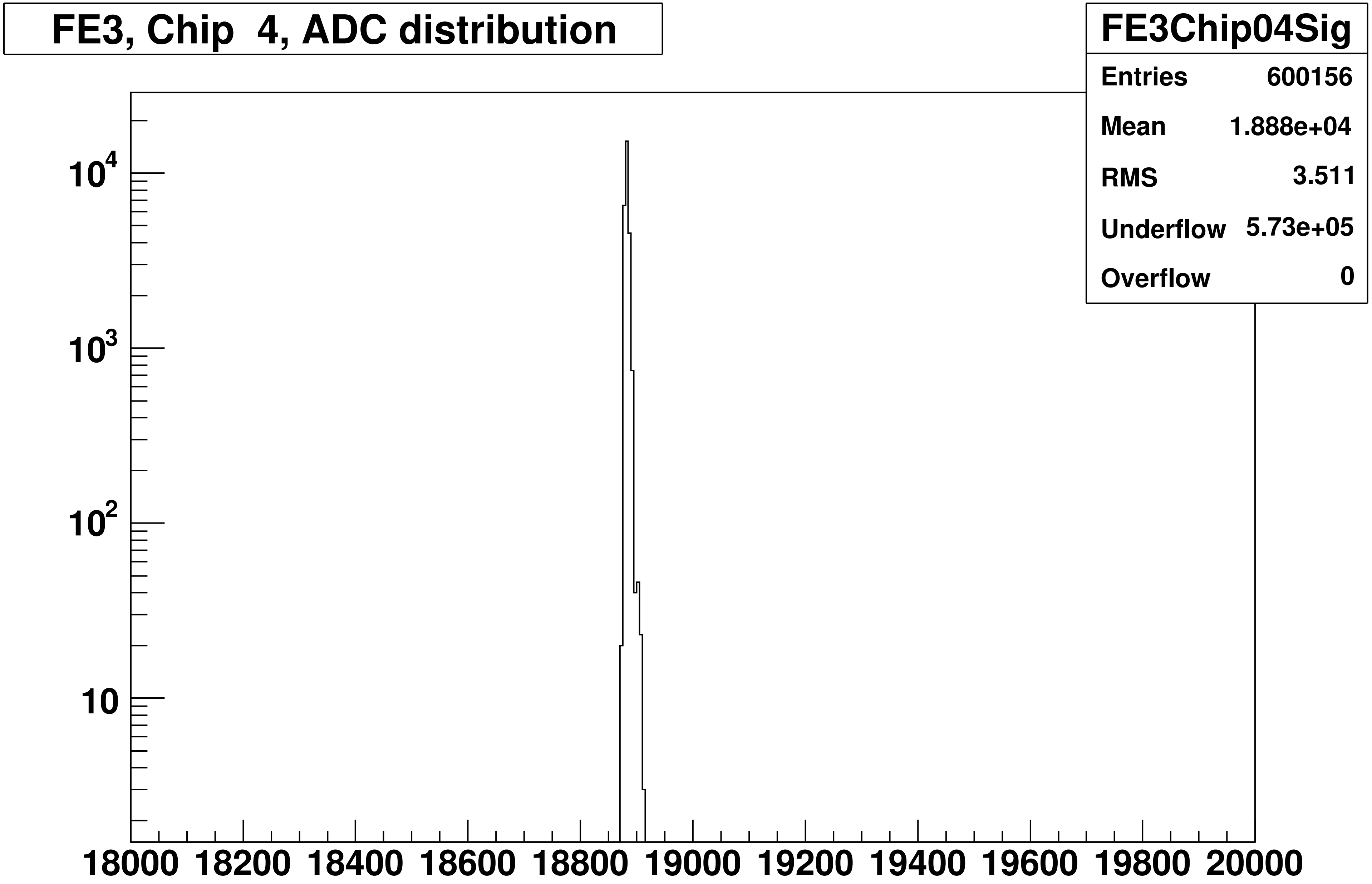
100
150
200



FE3, Chip 4, ADC distribution
FE3Chip04Sig
Entries 600156
Mean 1.888e+04
RMS 3.511
Underflow 5.73e+05
Overflow 0
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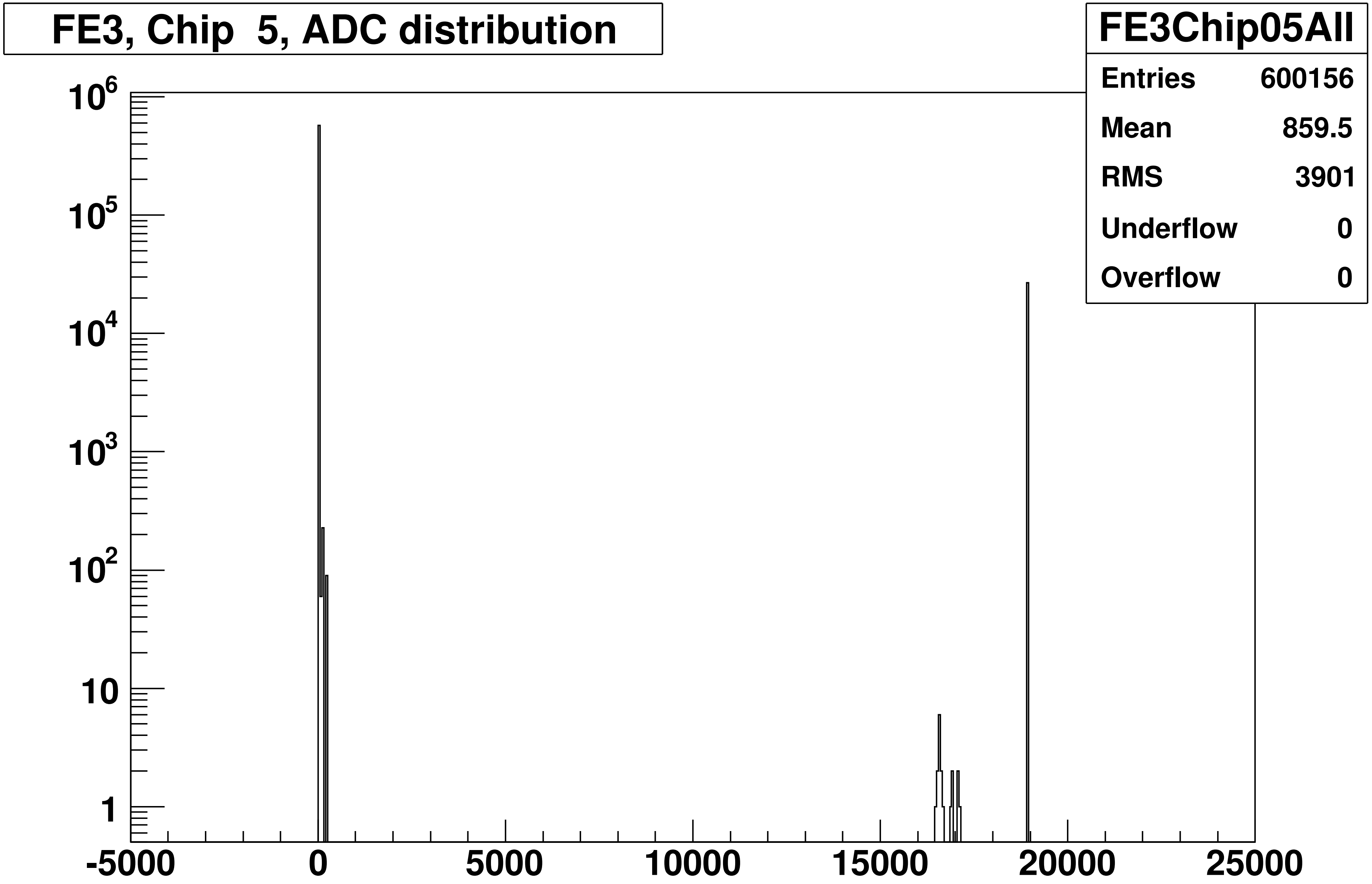
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE3, Chip 5, ADC distribution
FE3Chip05All
Entries 600156
Mean 859.5
RMS 3901
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
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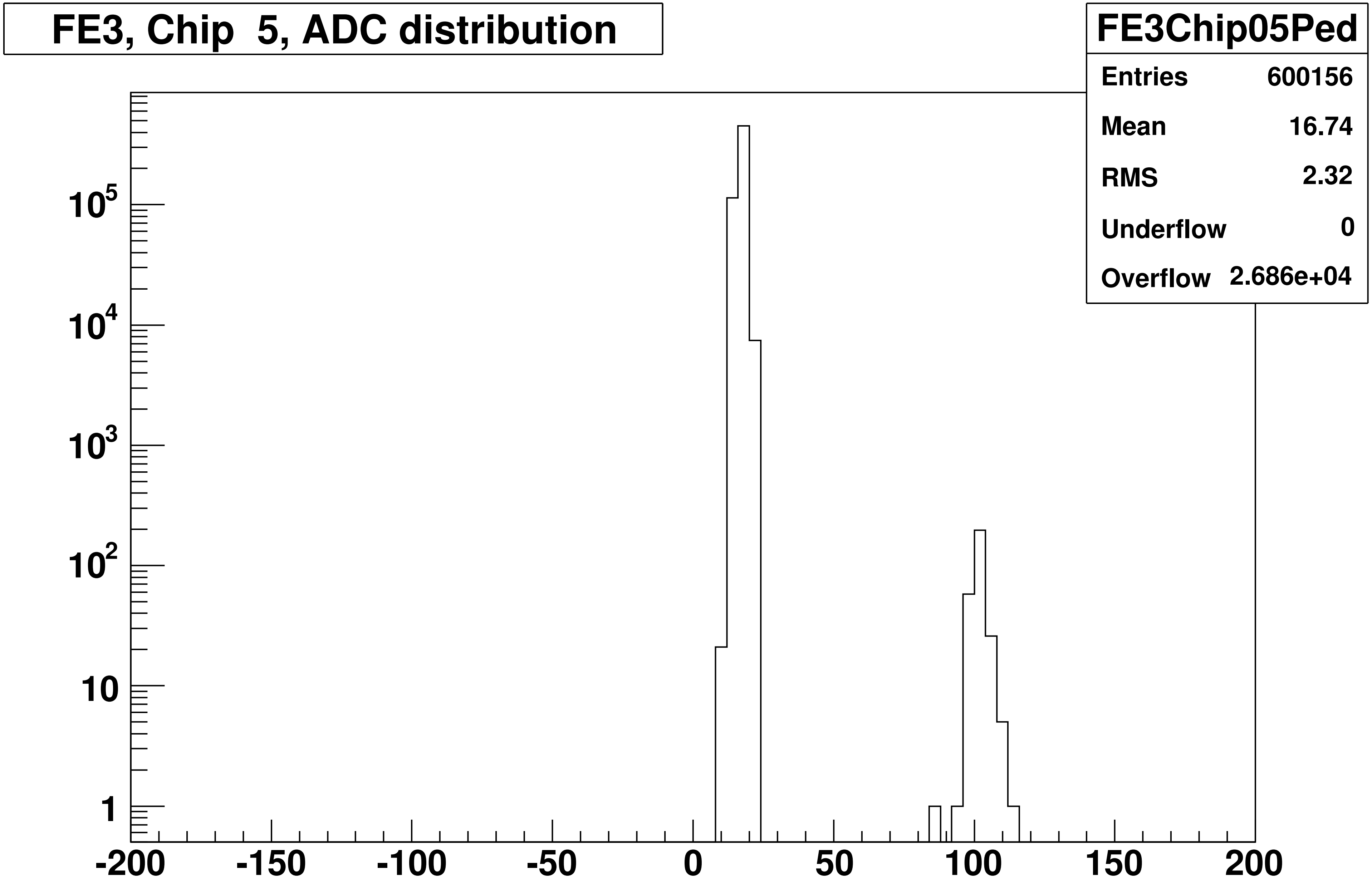

FE3, Chip 5, ADC distribution
FE3Chip05Ped
Entries 600156
Mean 16.74
RMS 2.32
Underflow 0
Overflow 2.686e+04
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10^3
10^2
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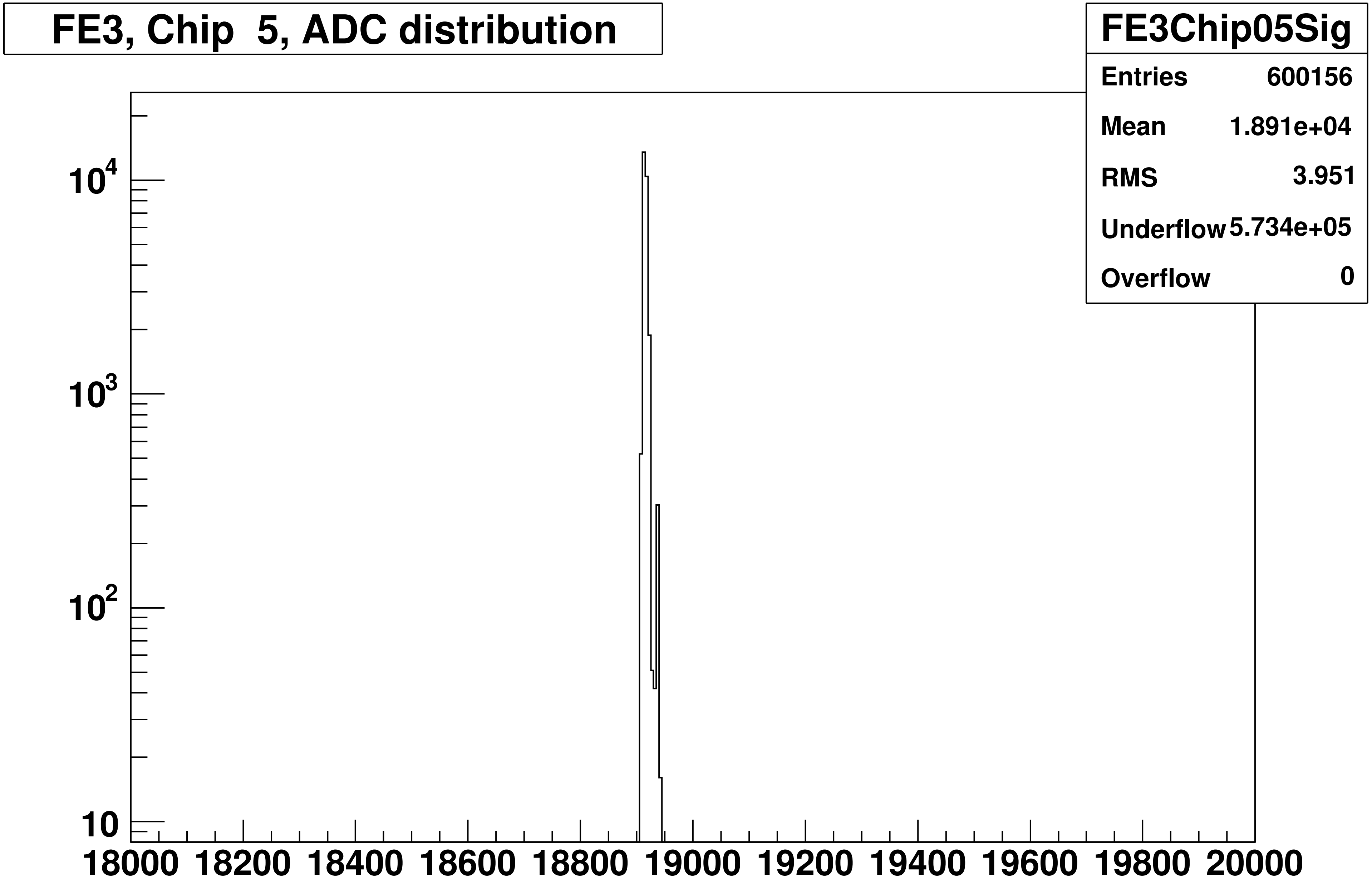
100
150
200


FE3, Chip 5, ADC distribution
FE3Chip05Sig
Entries 600156
Mean 1.891e+04
RMS 3.951
Underflow 5.734e+05
Overflow 0
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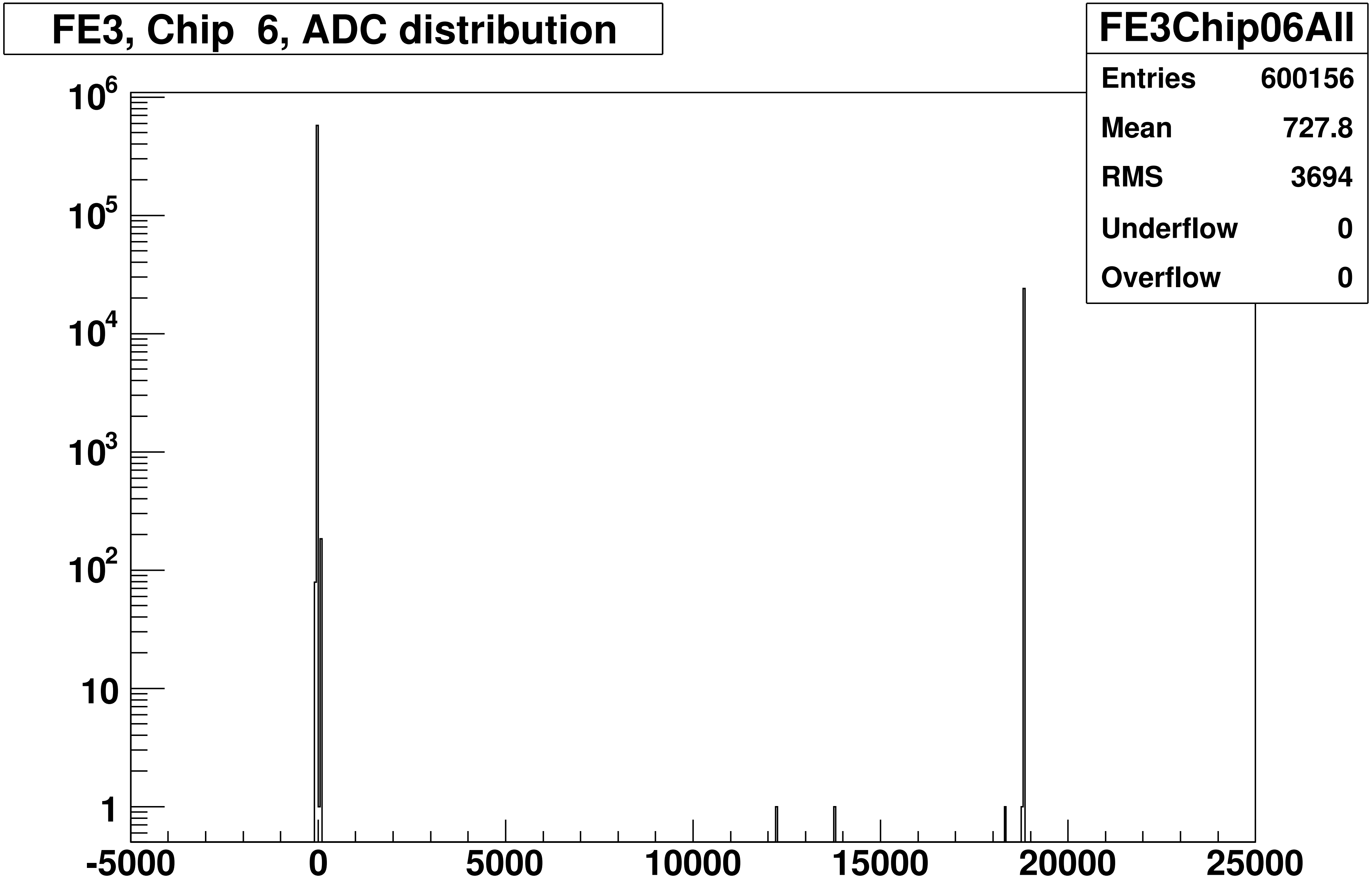
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE3, Chip 6, ADC distribution
FE3Chip06All
Entries 600156
Mean 727.8
RMS 3694
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
1
-5000
0
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10000
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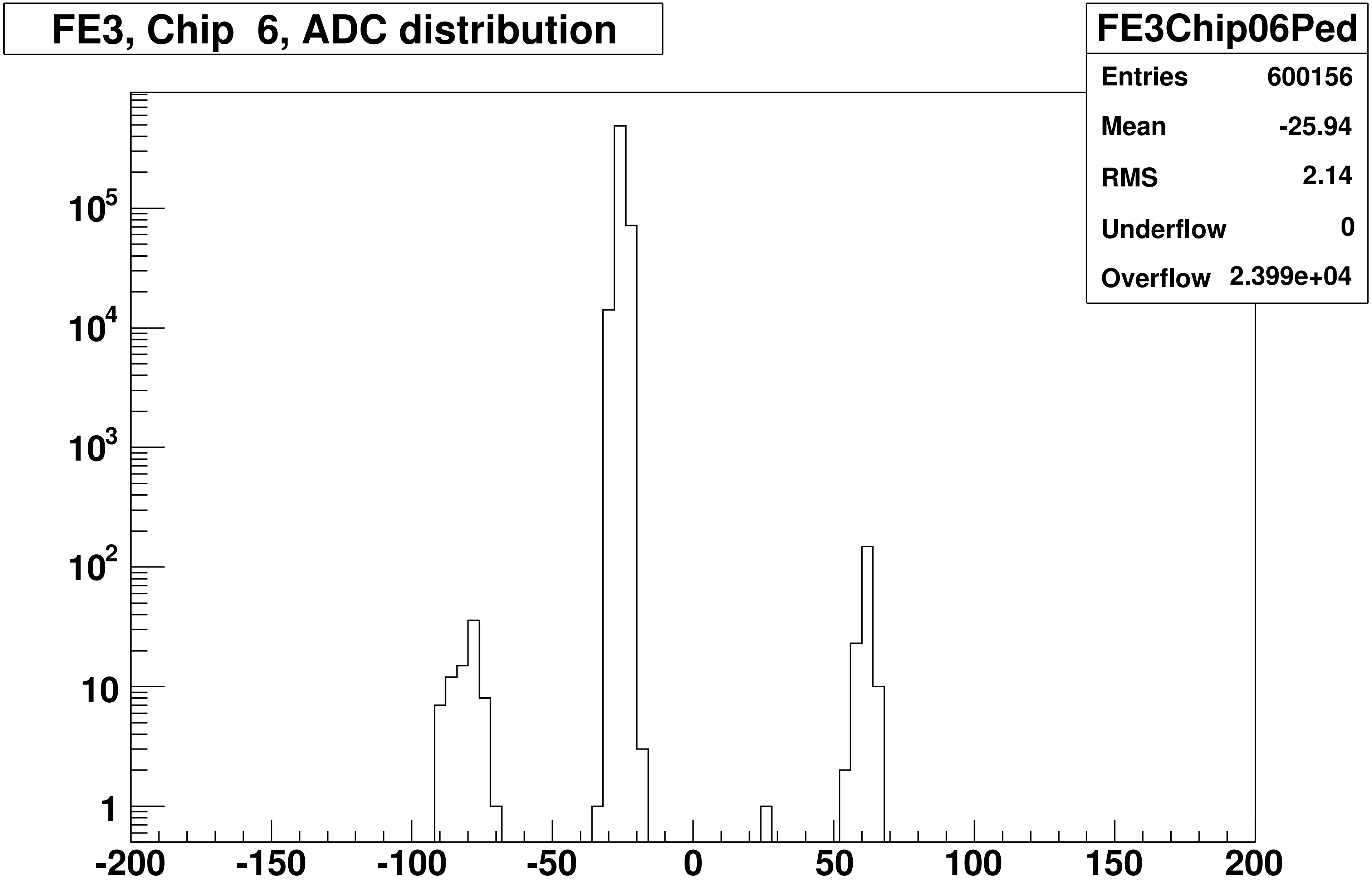
20000
25000



FE3, Chip 6, ADC distribution
FE3Chip06Ped
Entries 600156
Mean -25.94
RMS 2.14
Underflow 0
Overflow 2.399e+04
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10^4
10^3
10^2
10
1
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-100
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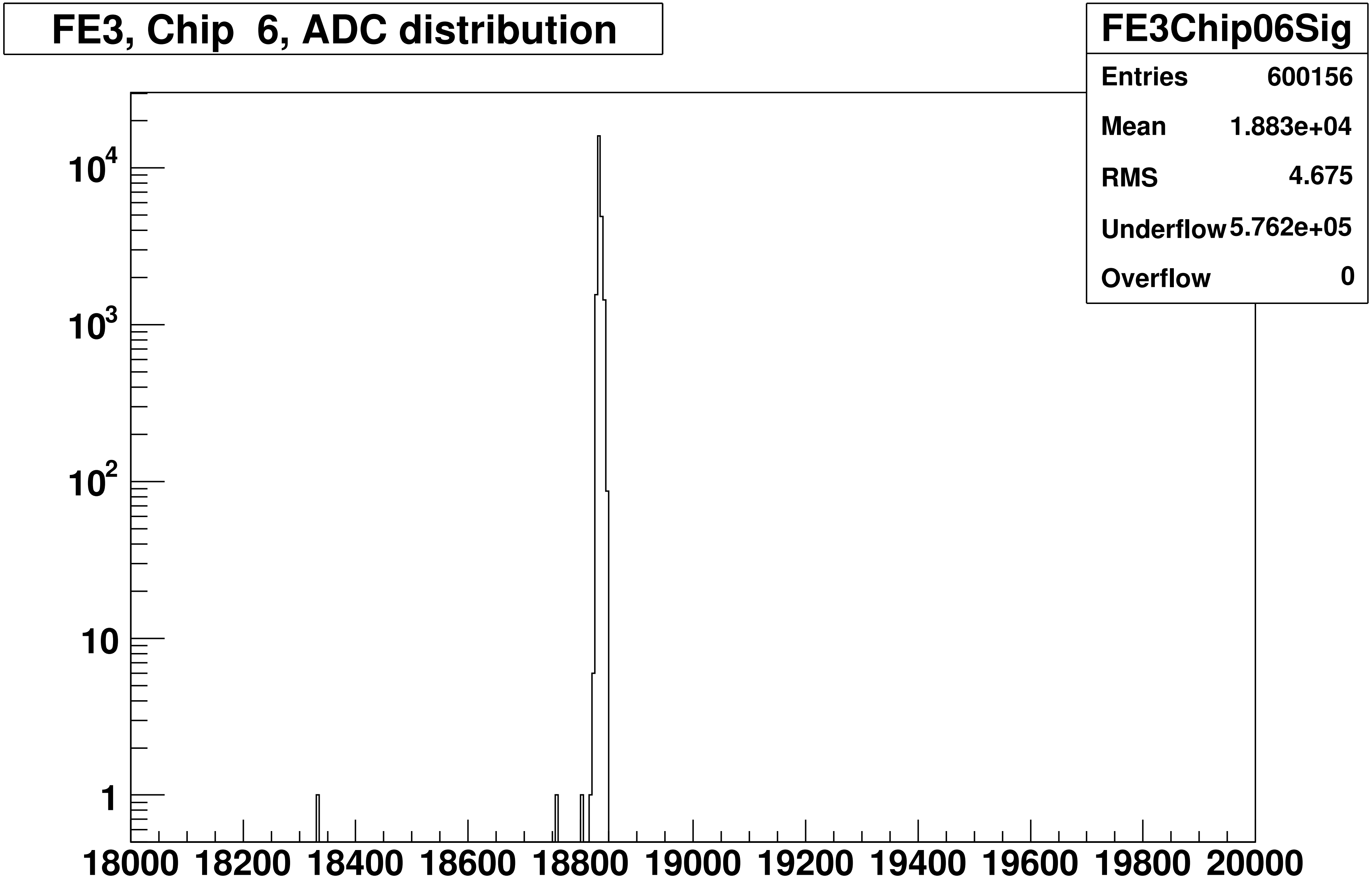
0
50
100
150
200


FE3, Chip 6, ADC distribution
FE3Chip06Sig
Entries 600156
Mean 1.883e+04
RMS 4.675
Underflow 5.762e+05
Overflow 0
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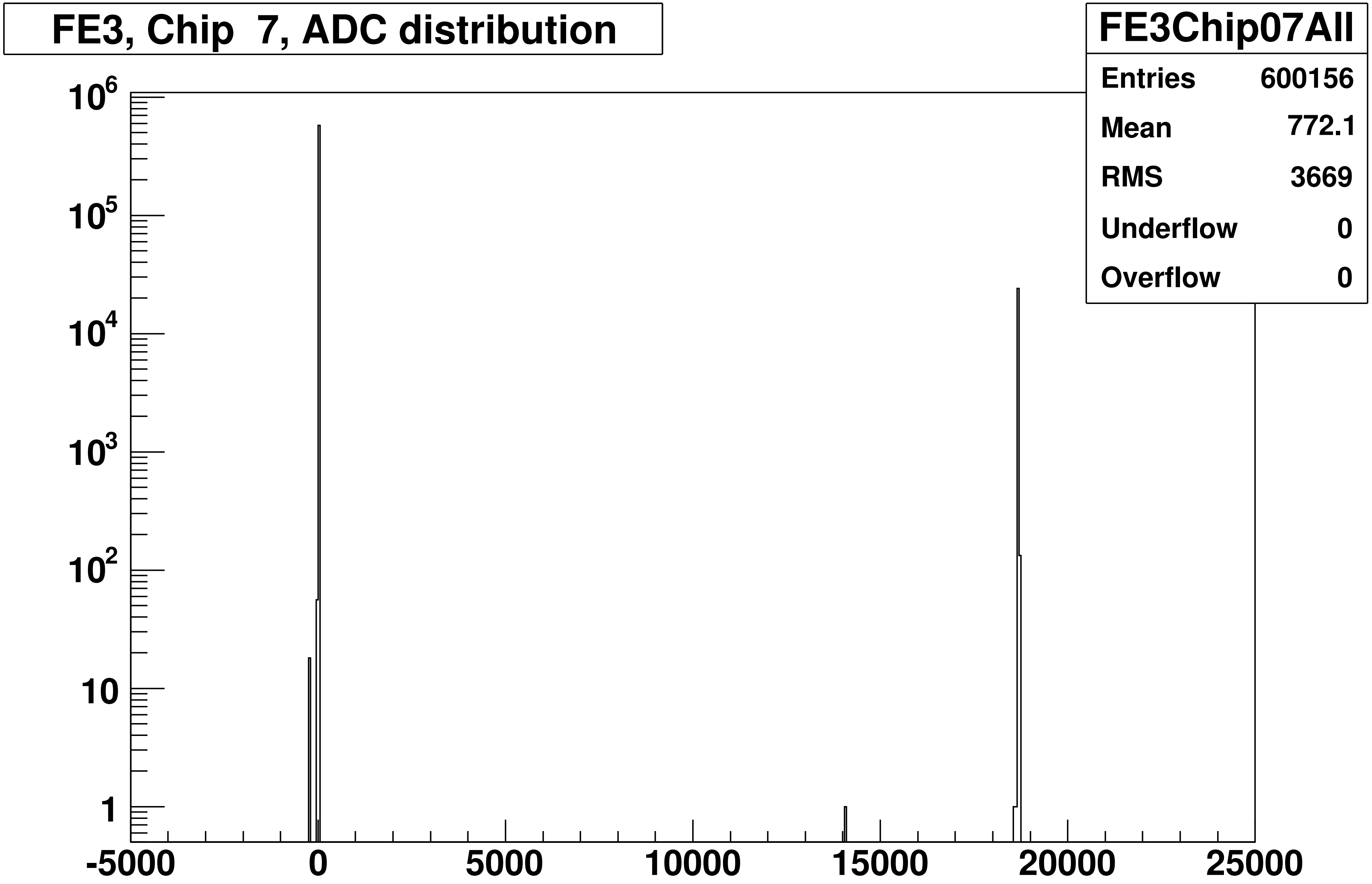
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE3, Chip 7, ADC distribution
FE3Chip07All
Entries 600156
Mean 772.1
RMS 3669
Underflow 0
Overflow 0
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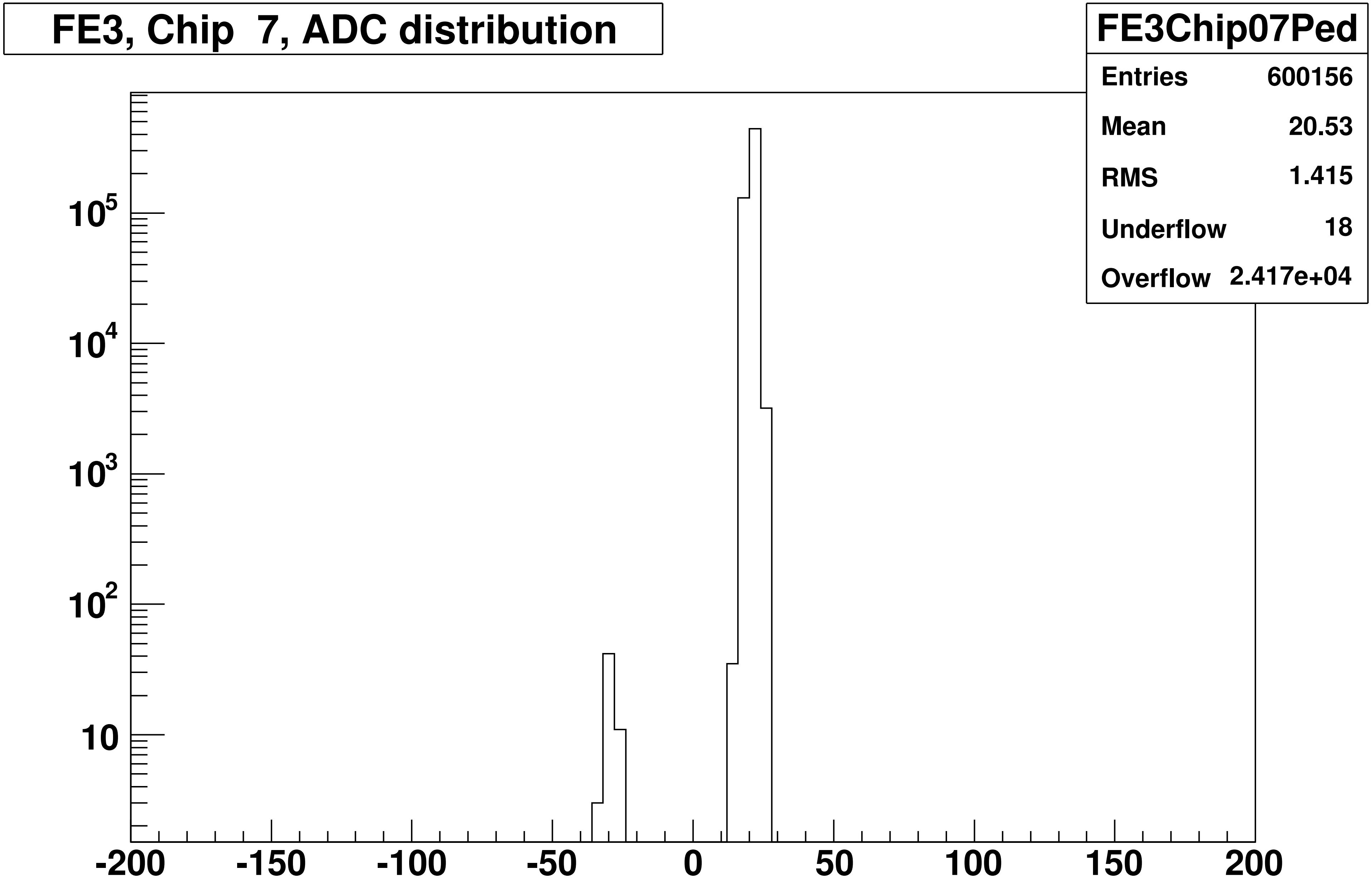
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE3, Chip 7, ADC distribution
FE3Chip07Ped
Entries 600156
Mean 20.53
RMS 1.415
Underflow 18
Overflow 2.417e+04
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10^2
10^3
10^4
10^5
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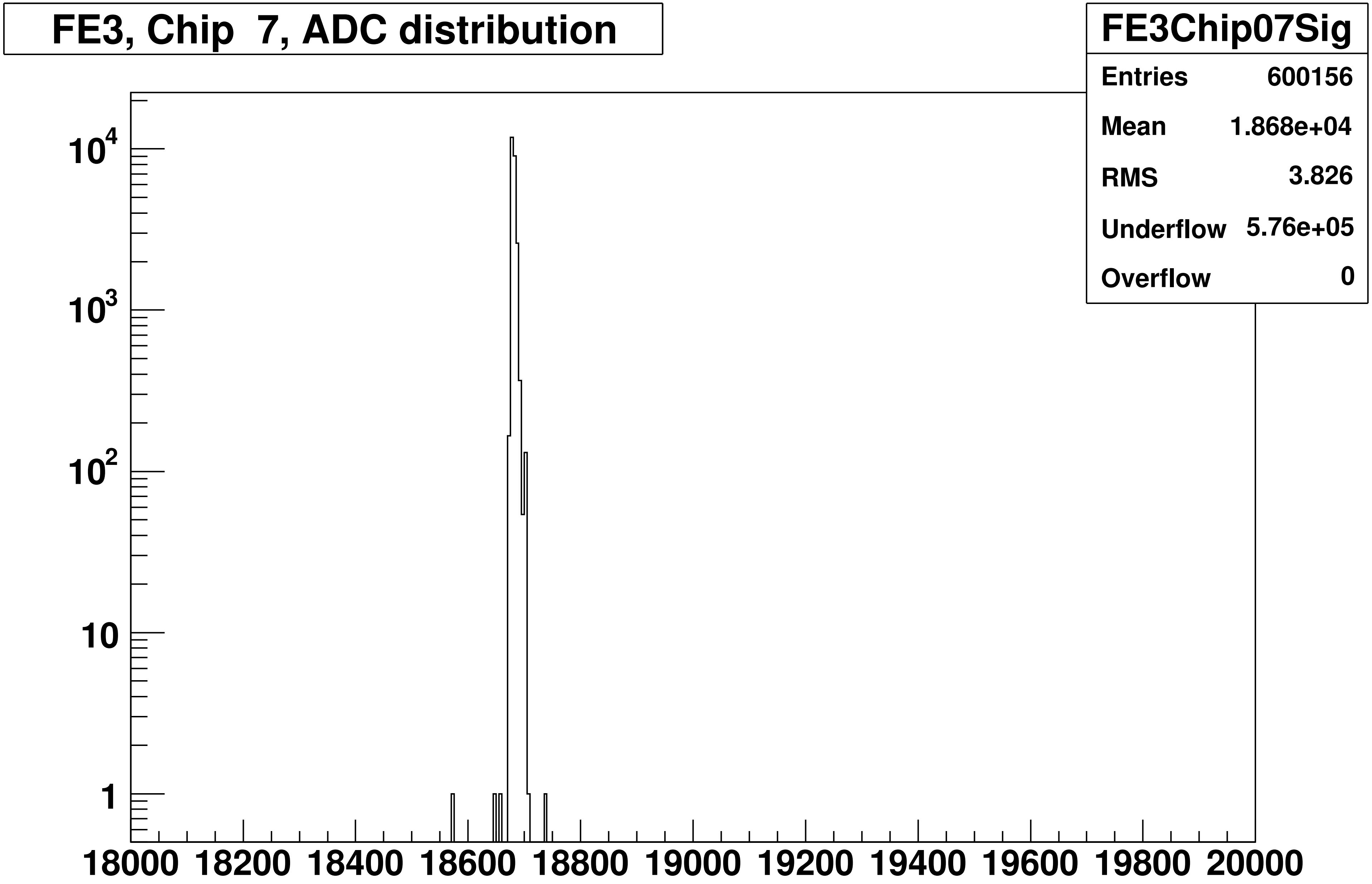
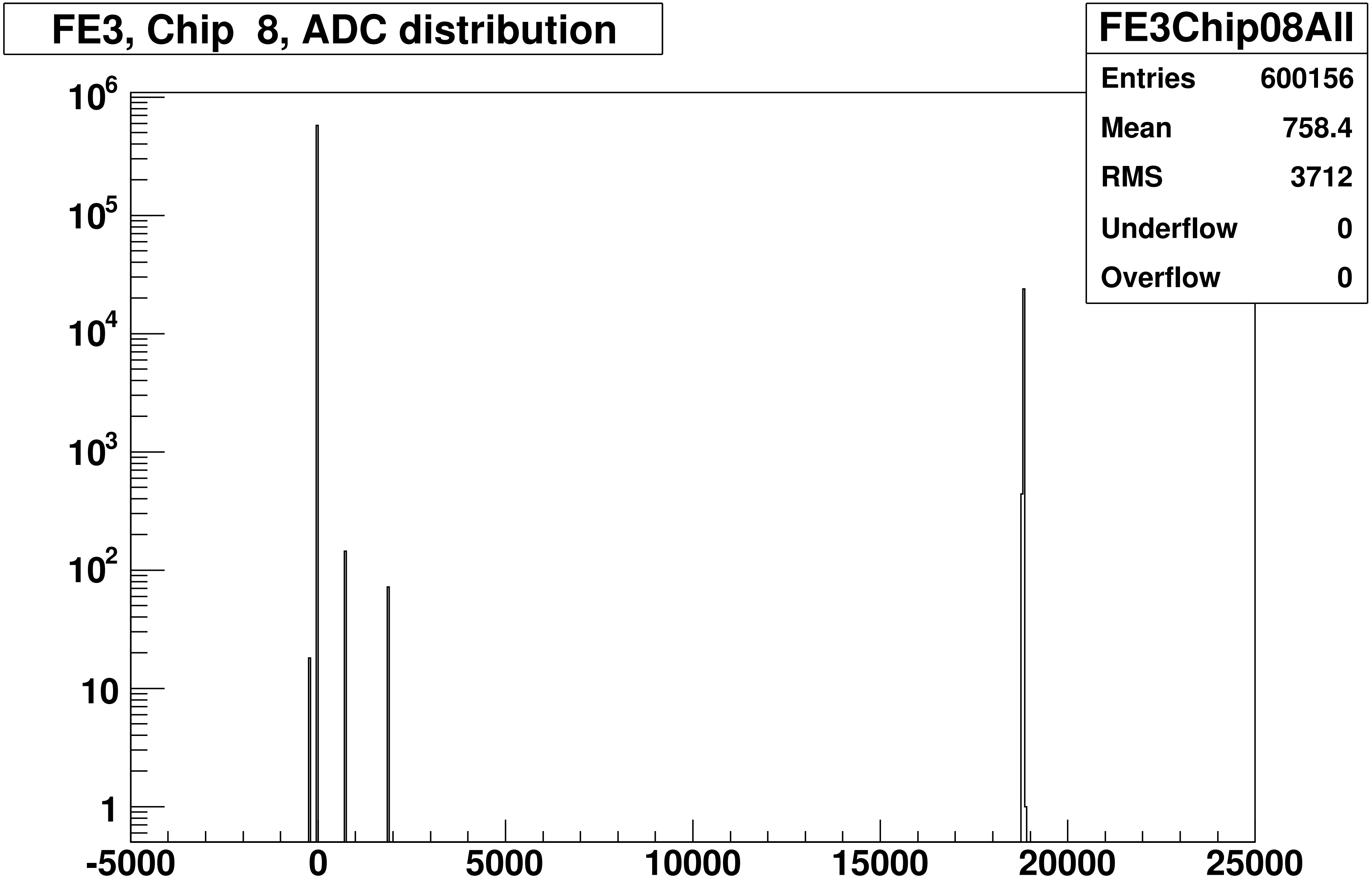
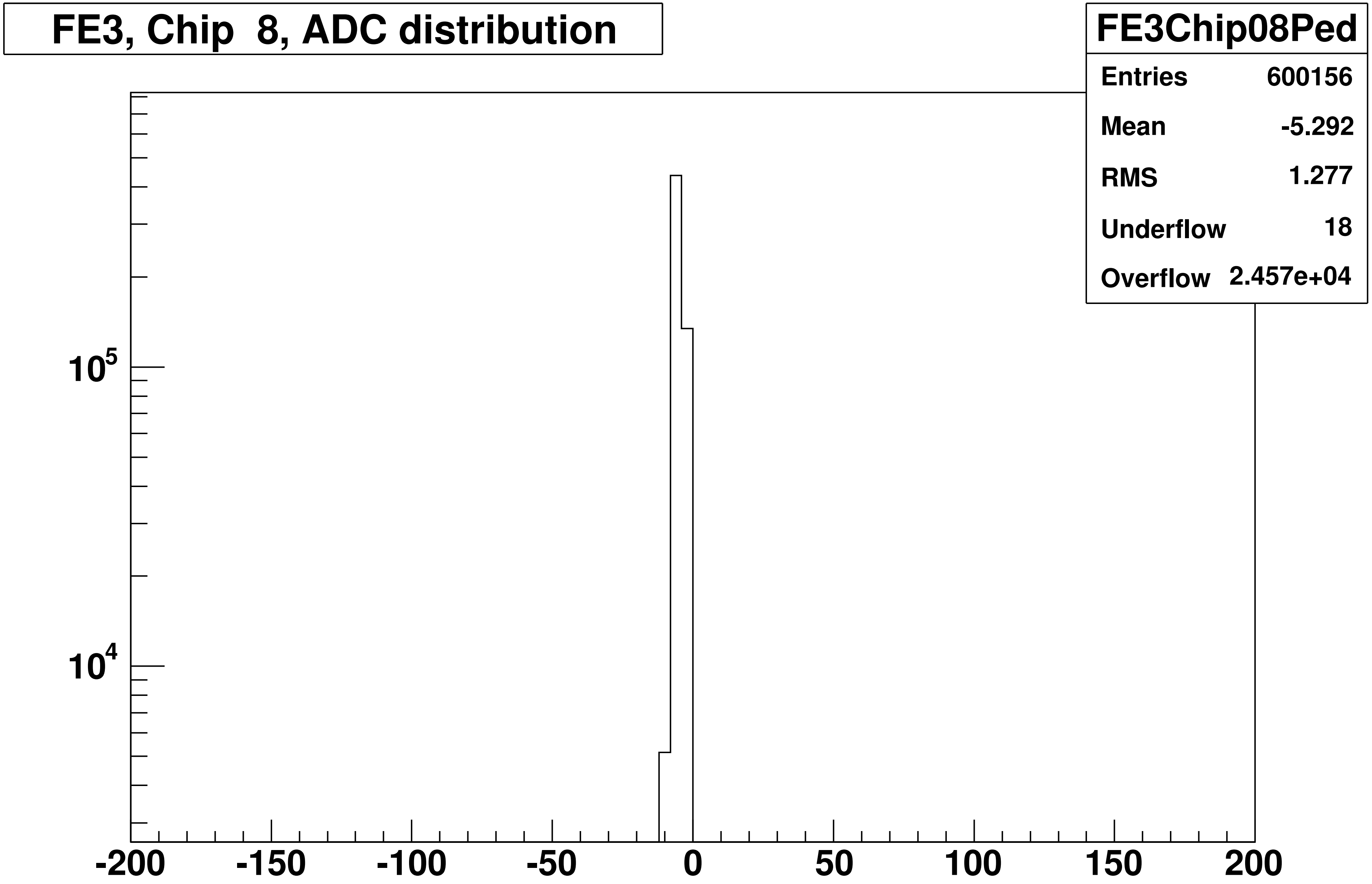
-150
-100
-50
0
50
100
150
200

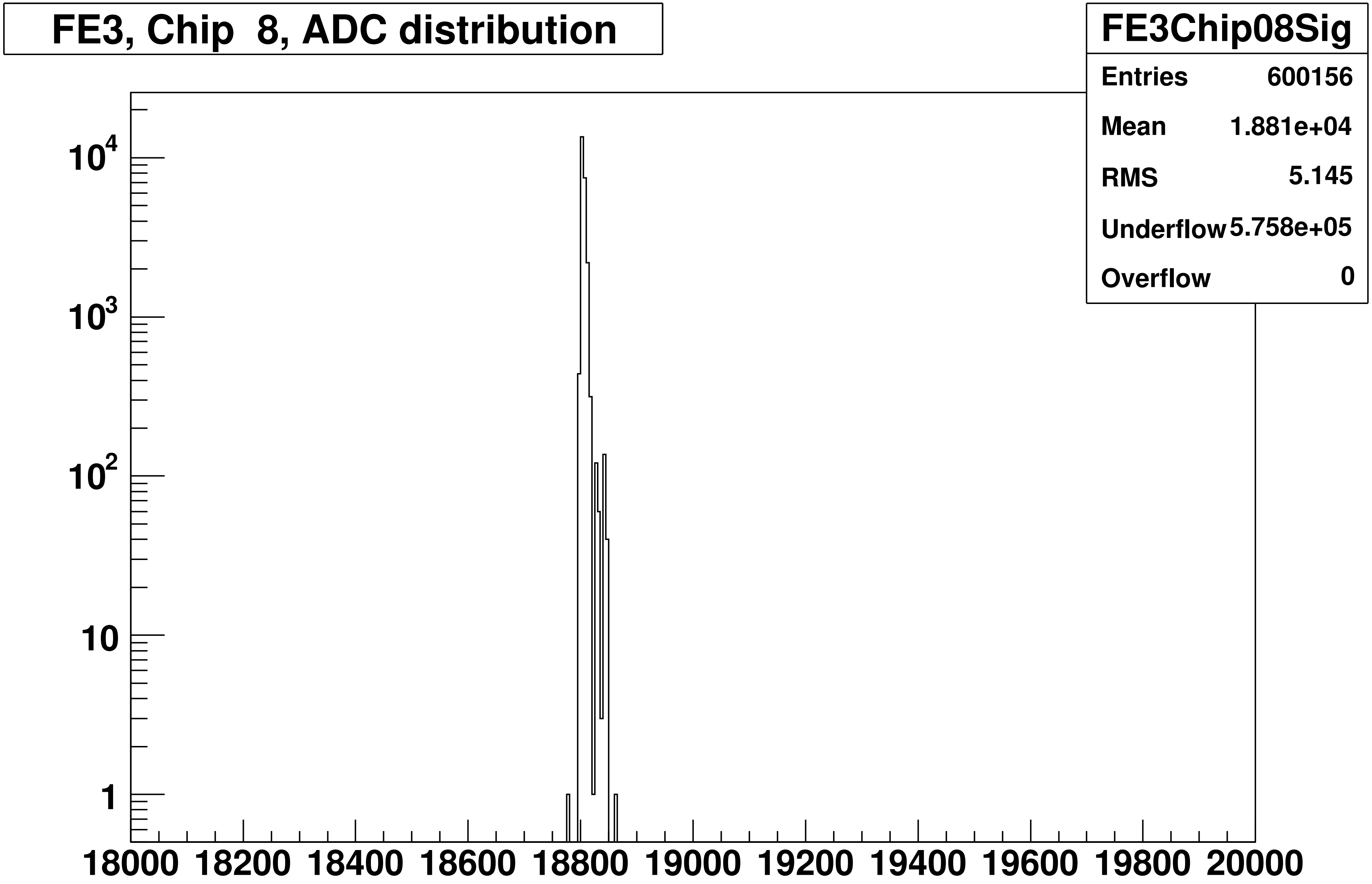


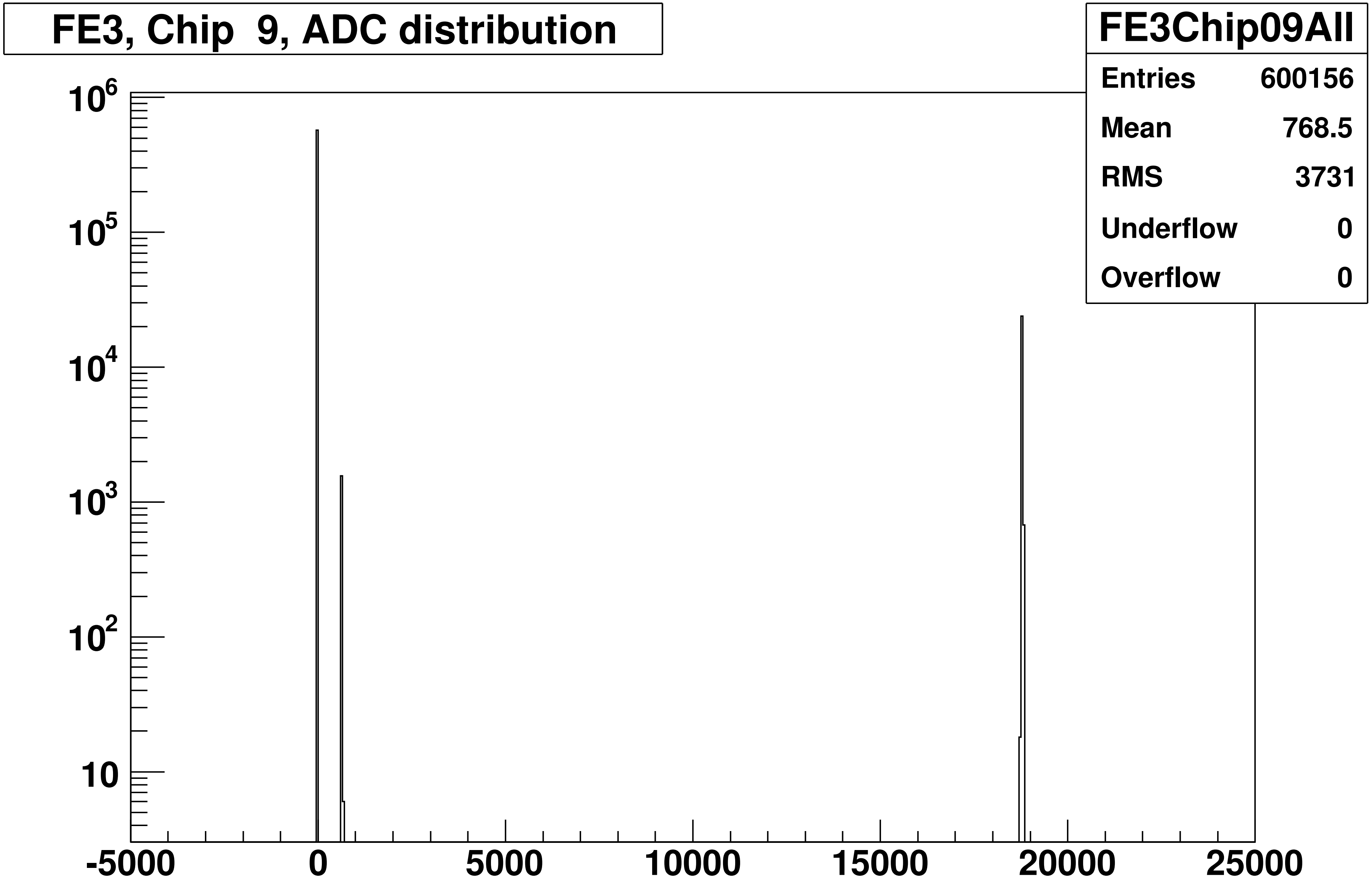
FE3, Chip 7, ADC distribution
FE3Chip07Sig
Entries 600156
Mean 1.868e+04
RMS 3.826
Underflow 5.76e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE3, Chip 8, ADC distribution
FE3Chip08All
Entries 600156
Mean 758.4
RMS 3712
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE3, Chip 8, ADC distribution
FE3Chip08Ped
Entries 600156
Mean -5.292
RMS 1.277
Underflow 18
Overflow 2.457e+04
10^5
10^4
-200 -150 -100 -50 0 50 100 150 200


FE3, Chip 8, ADC distribution
FE3Chip08Sig
Entries 600156
Mean 1.881e+04
RMS 5.145
Underflow 5.758e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000


FE3, Chip 9, ADC distribution
FE3Chip09All
Entries 600156
Mean 768.5
RMS 3731
Underflow 0
Overflow 0
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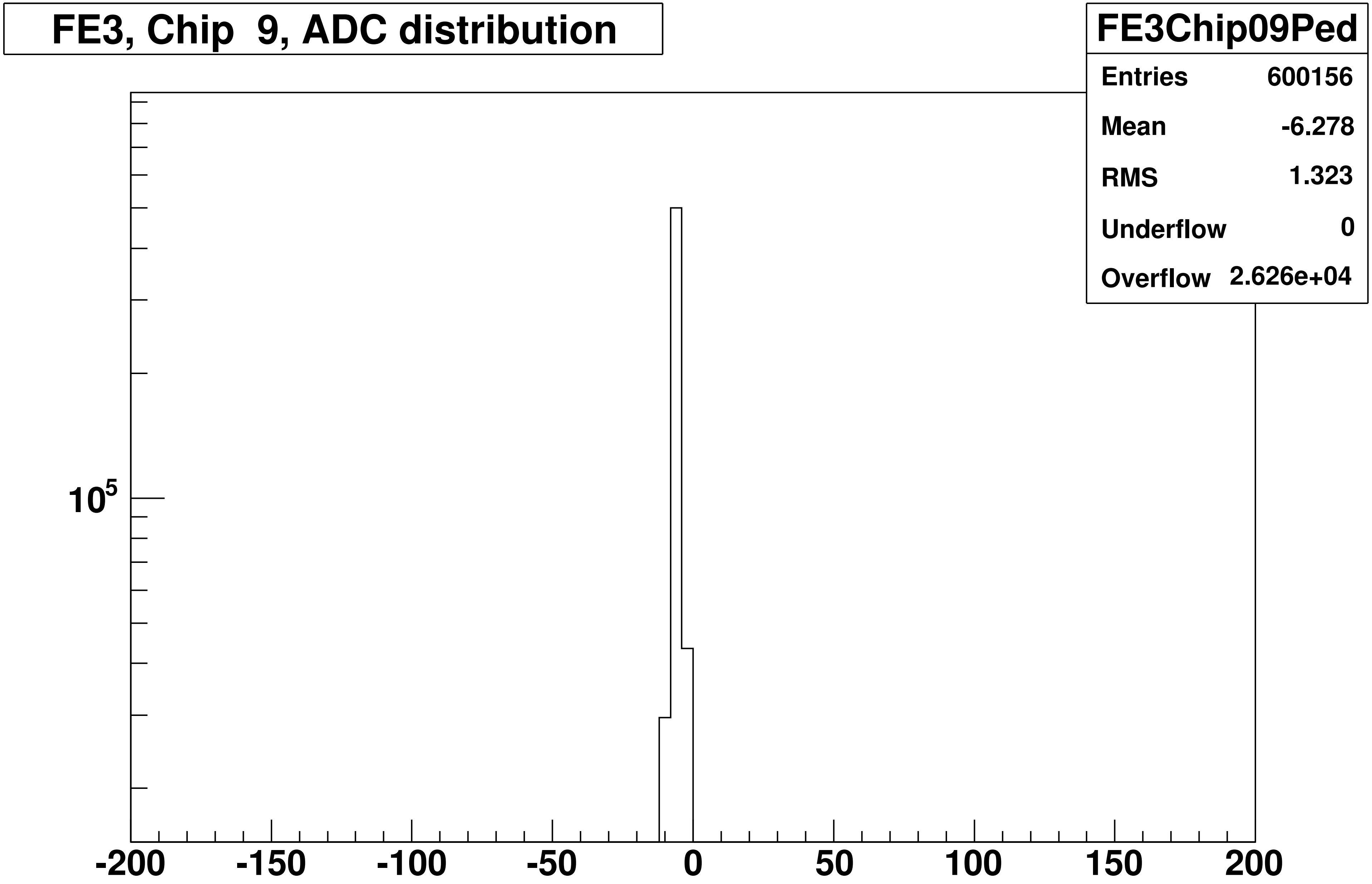
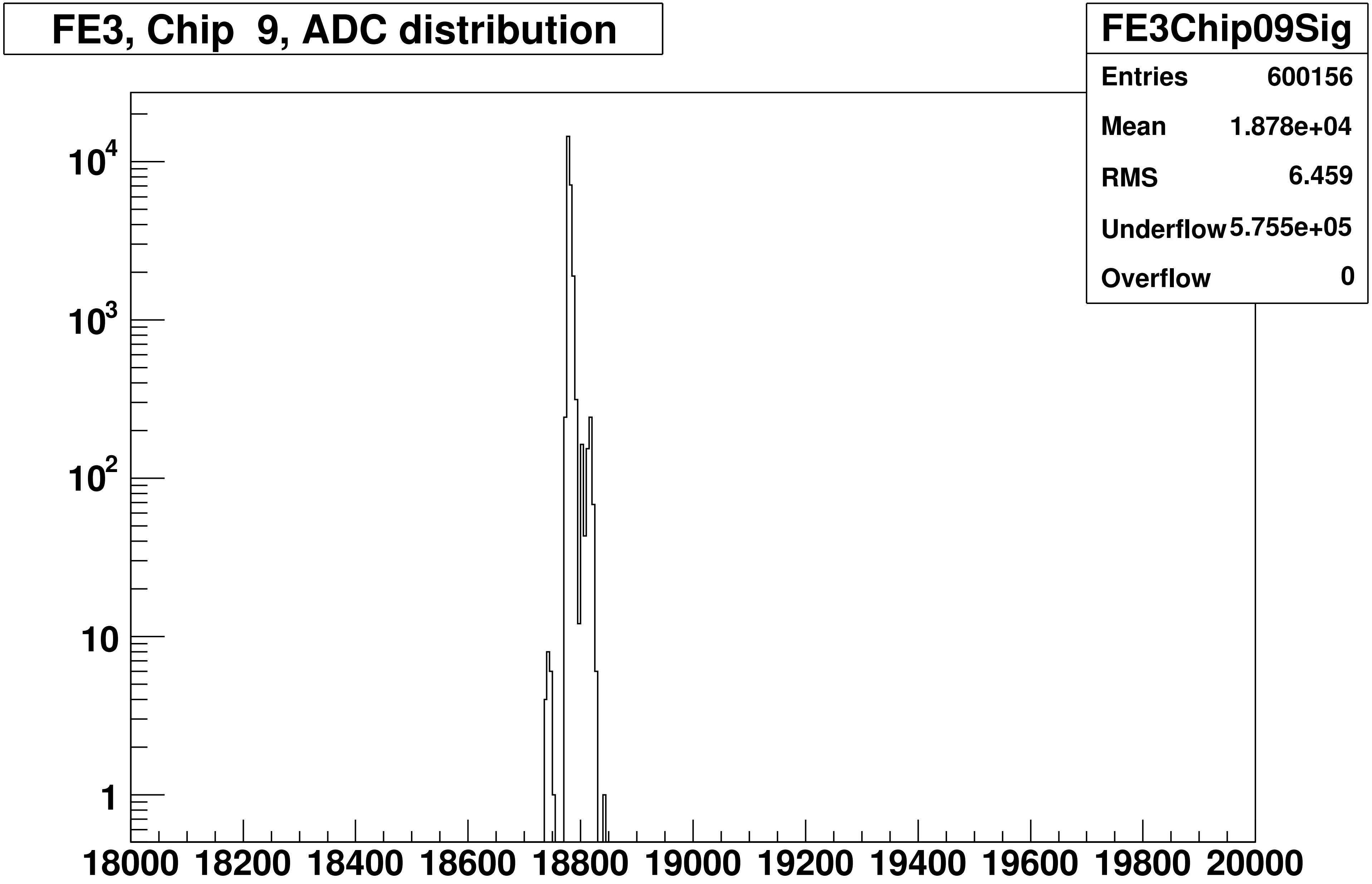
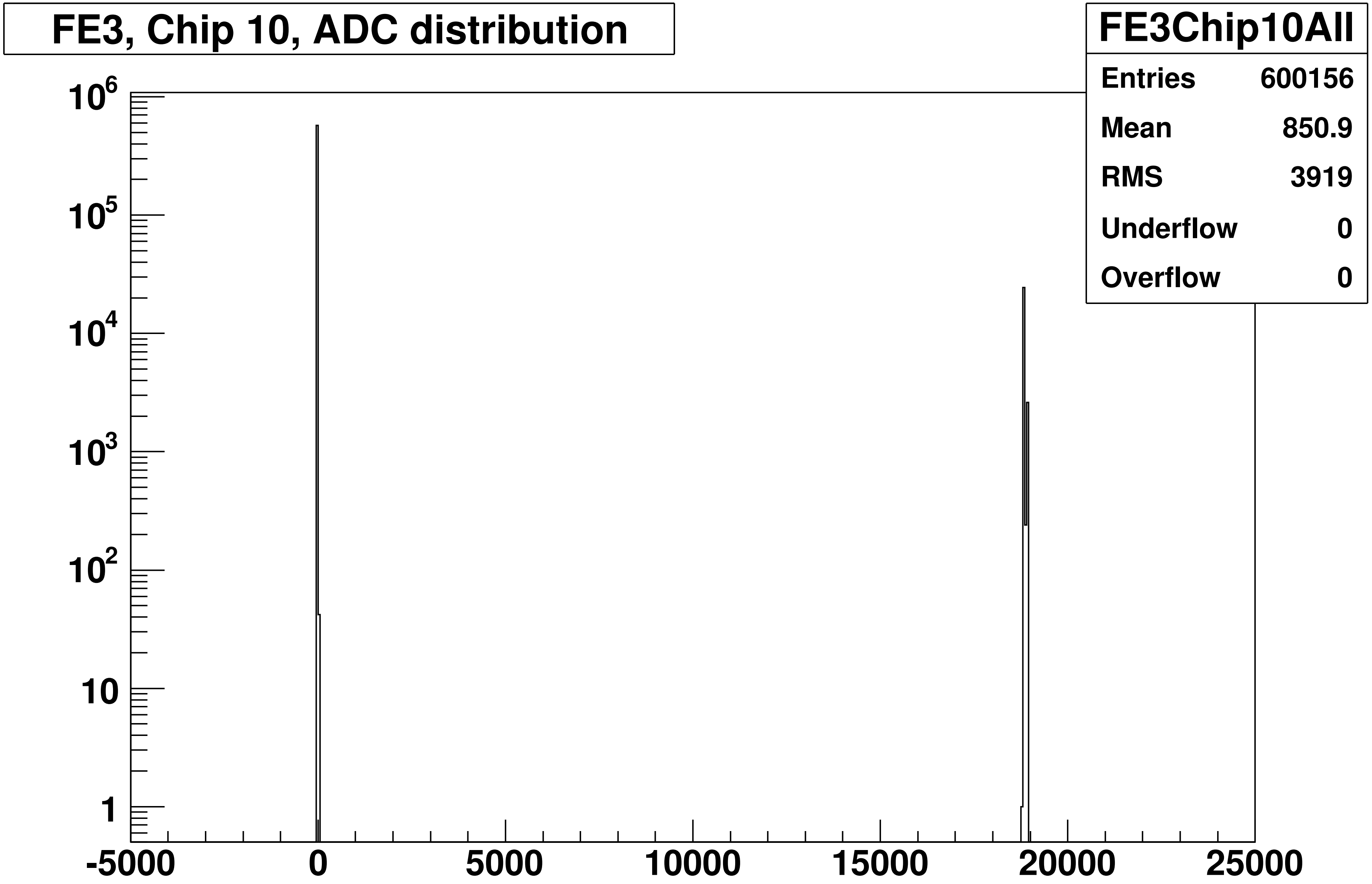
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000



FE3, Chip 9, ADC distribution
FE3Chip09Ped
Entries 600156
Mean -6.278
RMS 1.323
Underflow 0
Overflow 2.626e+04
10^5
-200
-150
-100
-50
0
50
100
150
200


FE3, Chip 9, ADC distribution
FE3Chip09Sig
Entries 600156
Mean 1.878e+04
RMS 6.459
Underflow 5.755e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000



FE3, Chip 10, ADC distribution
FE3Chip10All
Entries 600156
Mean 850.9
RMS 3919
Underflow 0
Overflow 0
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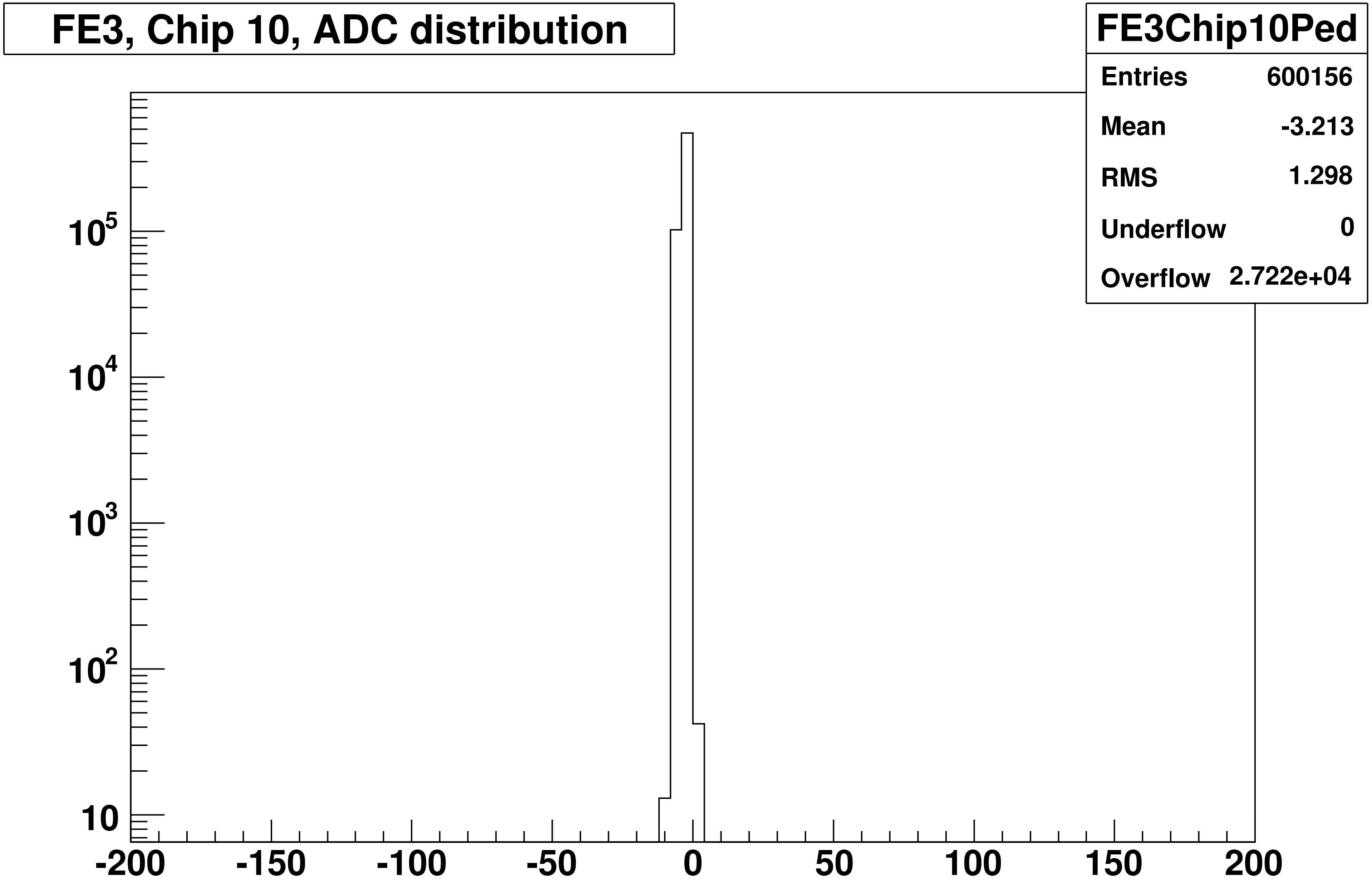
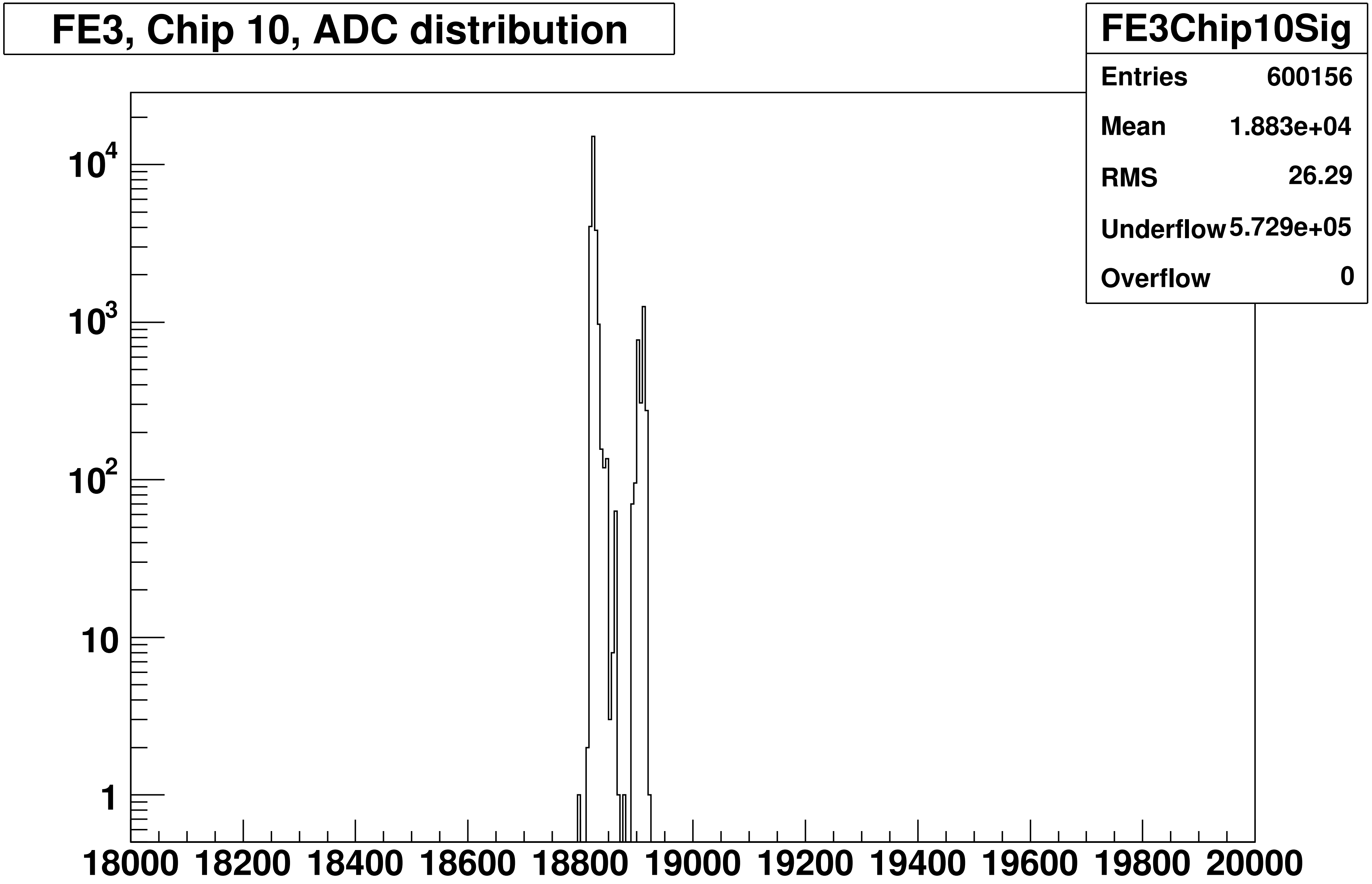
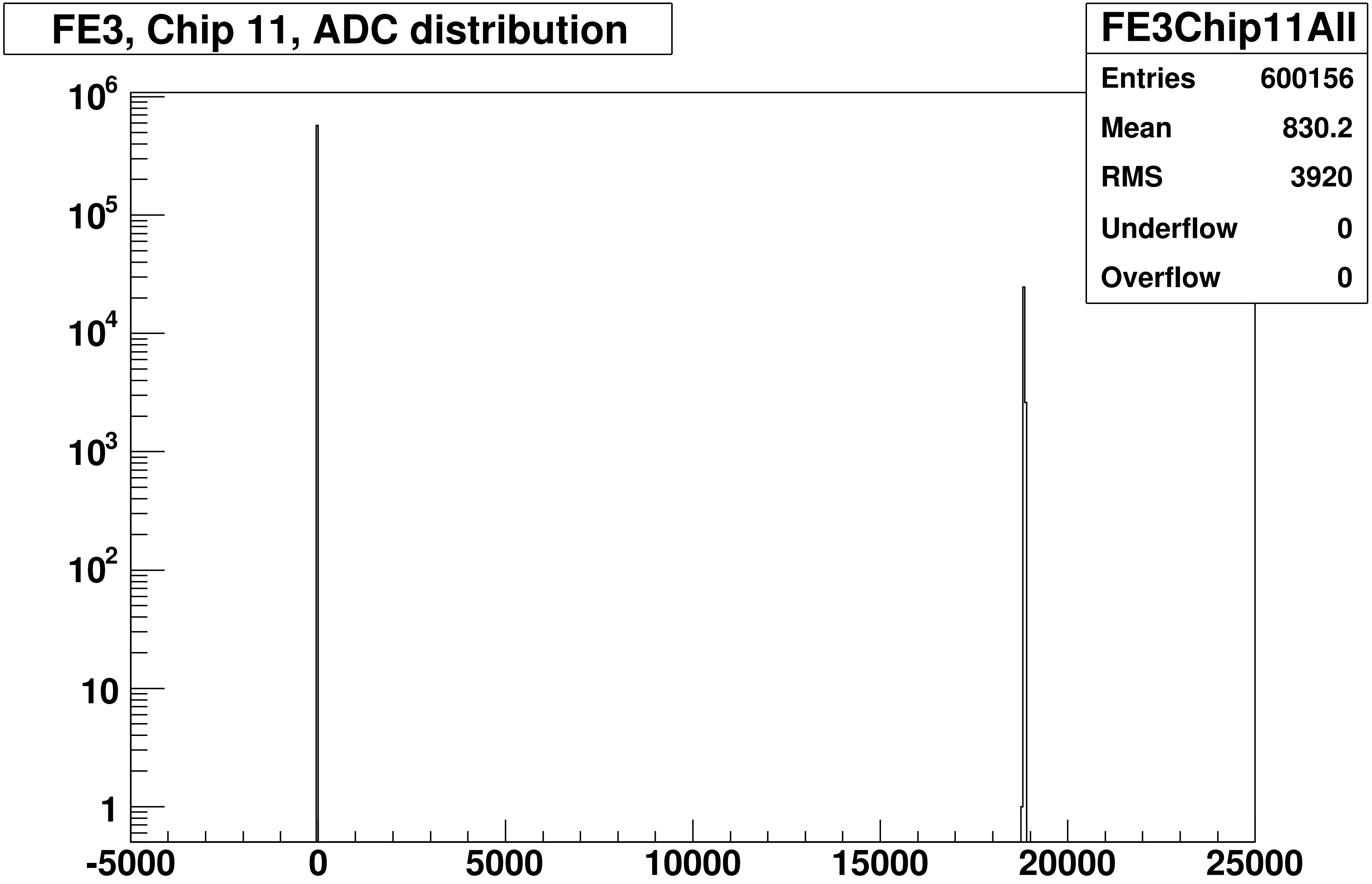
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE3, Chip 10, ADC distribution
FE3Chip10Ped
Entries 600156
Mean -3.213
RMS 1.298
Underflow 0
Overflow 2.722e+04
10
10^2
10^3
10^4
10^5
-200
-150
-100
-50
0
50
100
150
200


FE3, Chip 10, ADC distribution
FE3Chip10Sig
Entries 600156
Mean 1.883e+04
RMS 26.29
Underflow 5.729e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000


FE3, Chip 11, ADC distribution
FE3Chip11All
Entries 600156
Mean 830.2
RMS 3920
Underflow 0
Overflow 0
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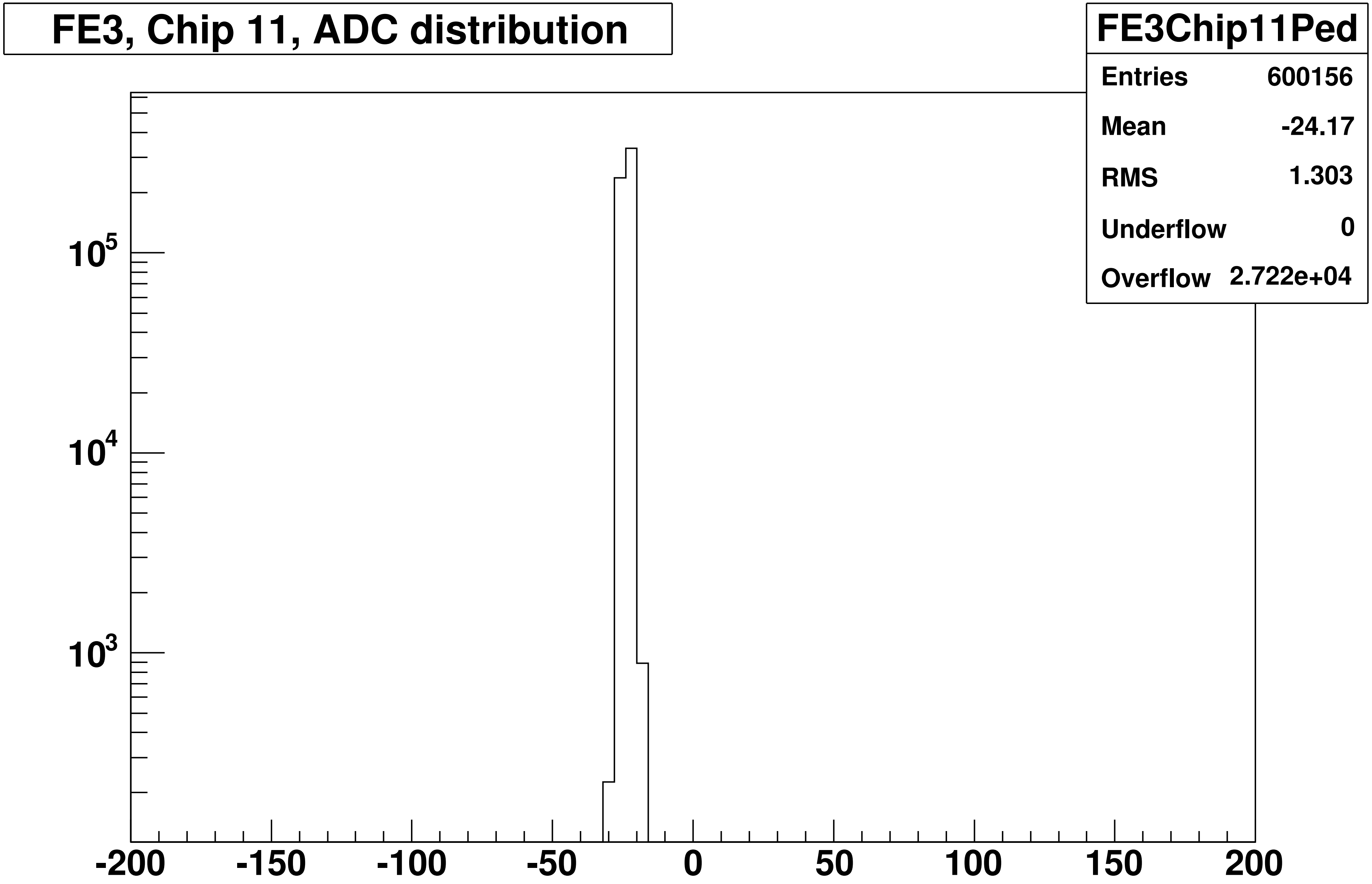
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE3, Chip 11, ADC distribution
FE3Chip11Ped
Entries 600156
Mean -24.17
RMS 1.303
Underflow 0
Overflow 2.722e+04
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10^4
10^3
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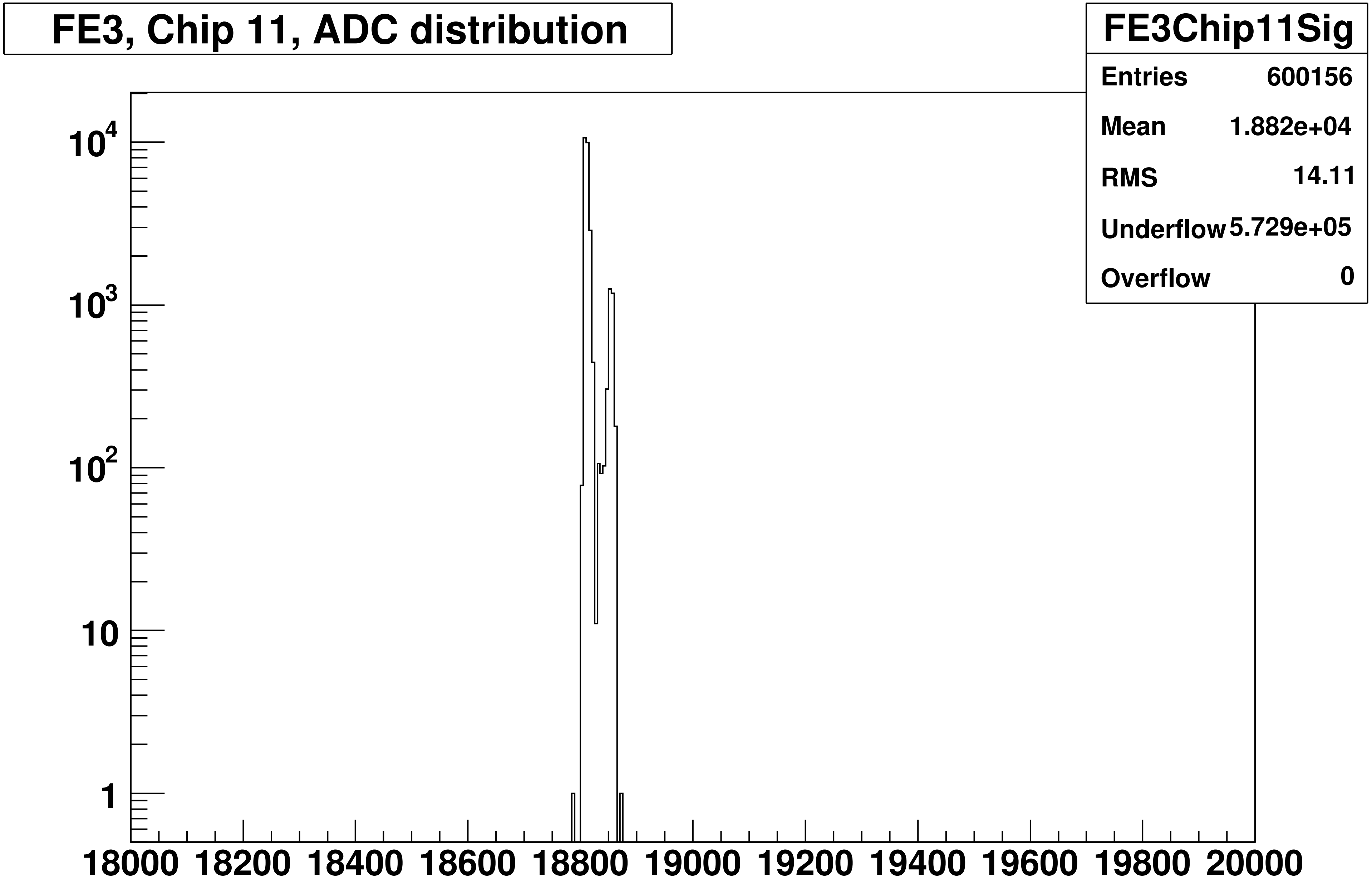
-100
-50
0
50
100
150
200



FE3, Chip 11, ADC distribution
FE3Chip11Sig
Entries 600156
Mean 1.882e+04
RMS 14.11
Underflow 5.729e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
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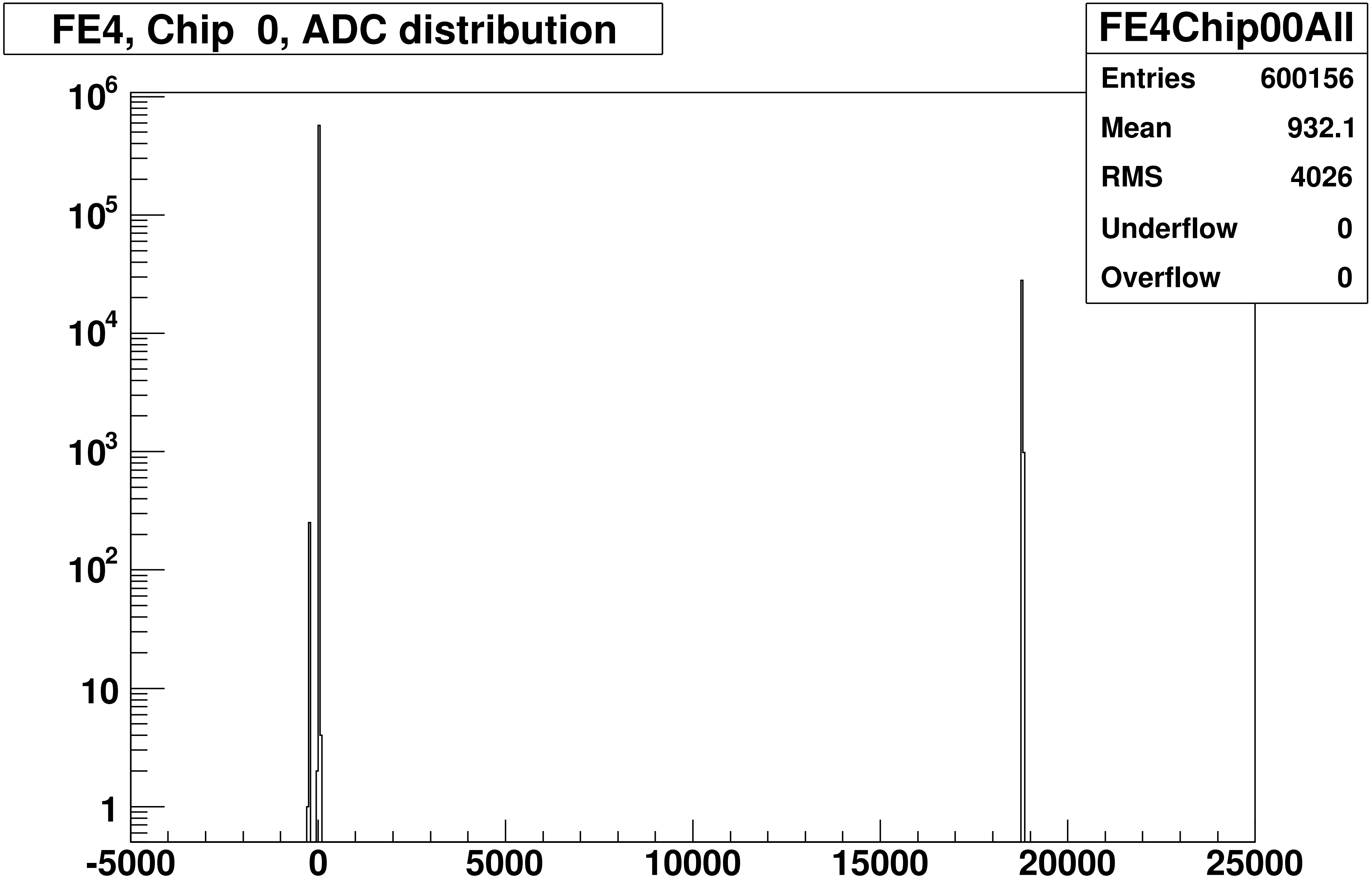
19400
19600
19800
20000



FE4, Chip 0, ADC distribution
FE4Chip00All
Entries 600156
Mean 932.1
RMS 4026
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
1
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0
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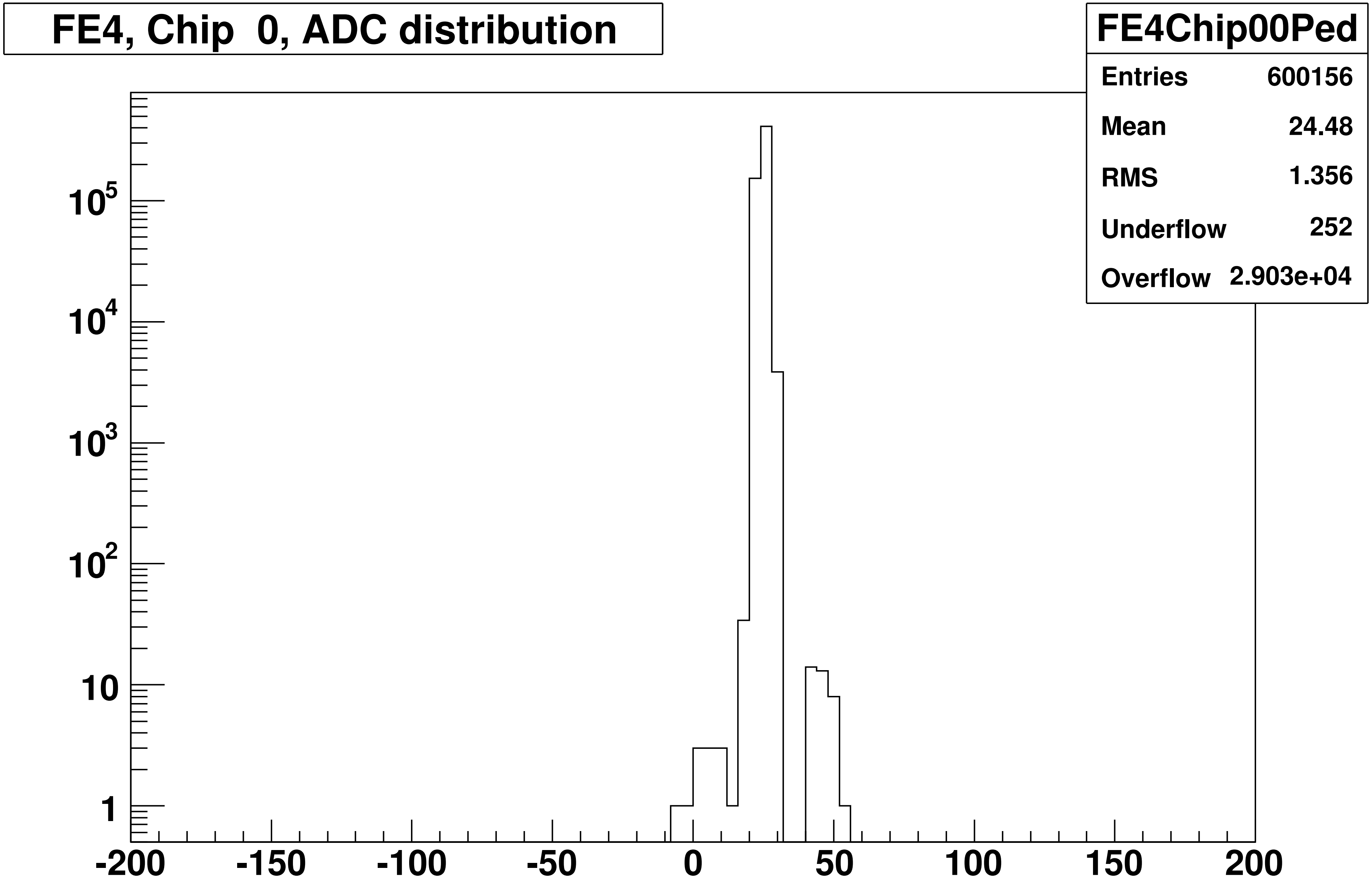
10000
15000
20000
25000


FE4, Chip 0, ADC distribution
FE4Chip00Ped
Entries 600156
Mean 24.48
RMS 1.356
Underflow 252
Overflow 2.903e+04
10^5
10^4
10^3
10^2
10
1
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-100
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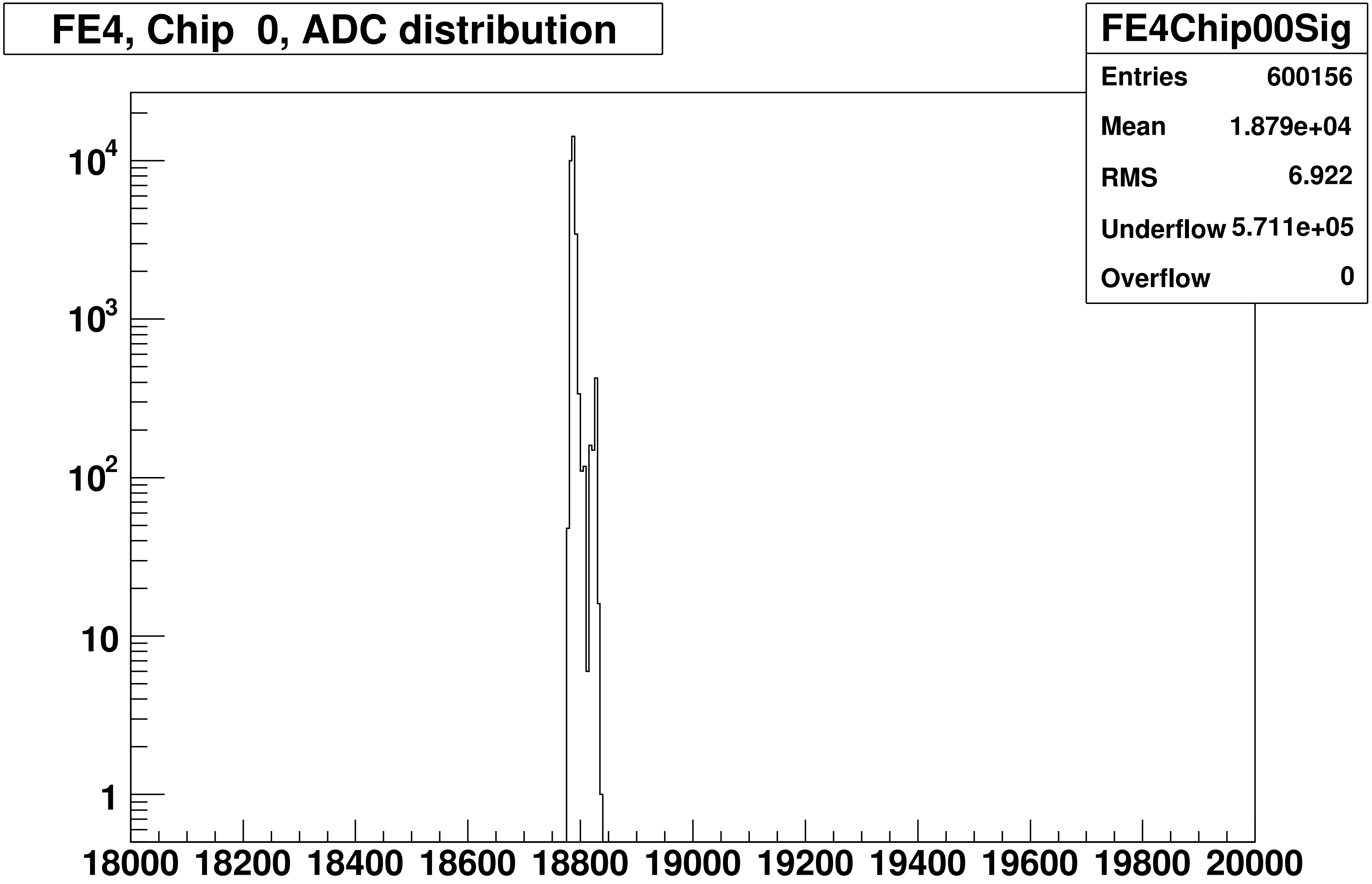
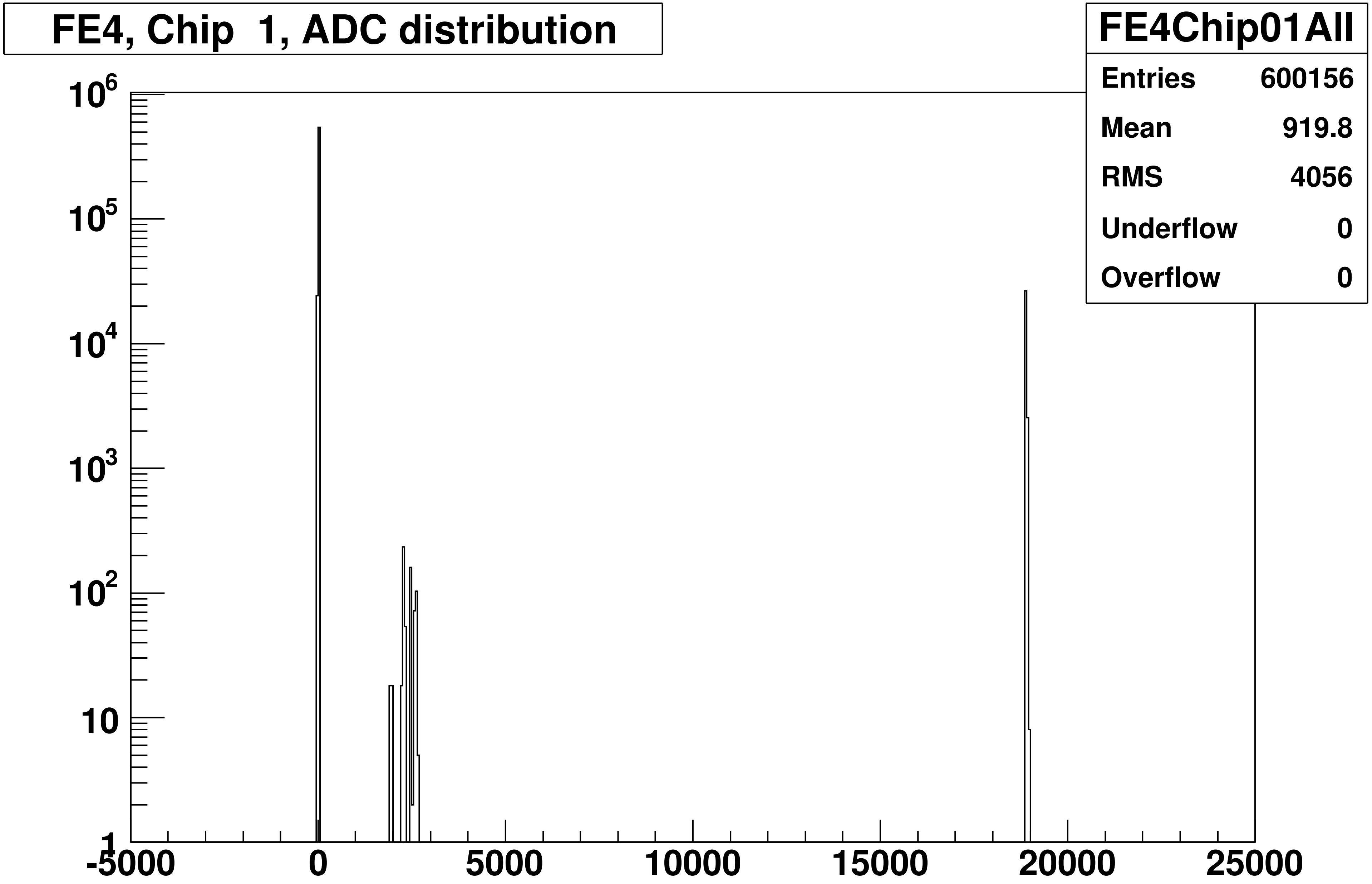
150
200



FE4, Chip 0, ADC distribution
FE4Chip00Sig
Entries 600156
Mean 1.879e+04
RMS 6.922
Underflow 5.711e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE4, Chip 1, ADC distribution
FE4Chip01All
Entries 600156
Mean 919.8
RMS 4056
Underflow 0
Overflow 0
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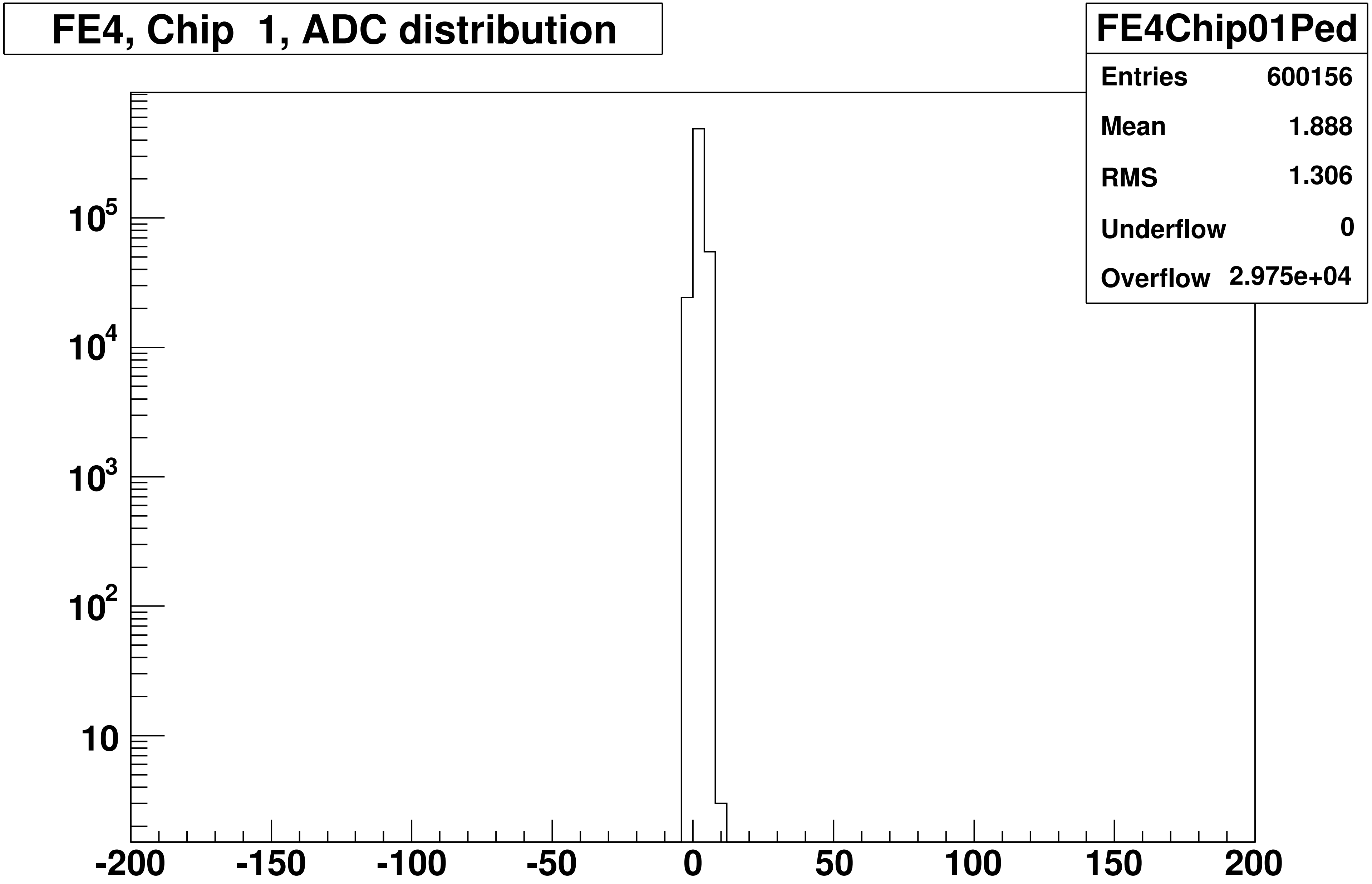
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE4, Chip 1, ADC distribution
FE4Chip01Ped
Entries 600156
Mean 1.888
RMS 1.306
Underflow 0
Overflow 2.975e+04
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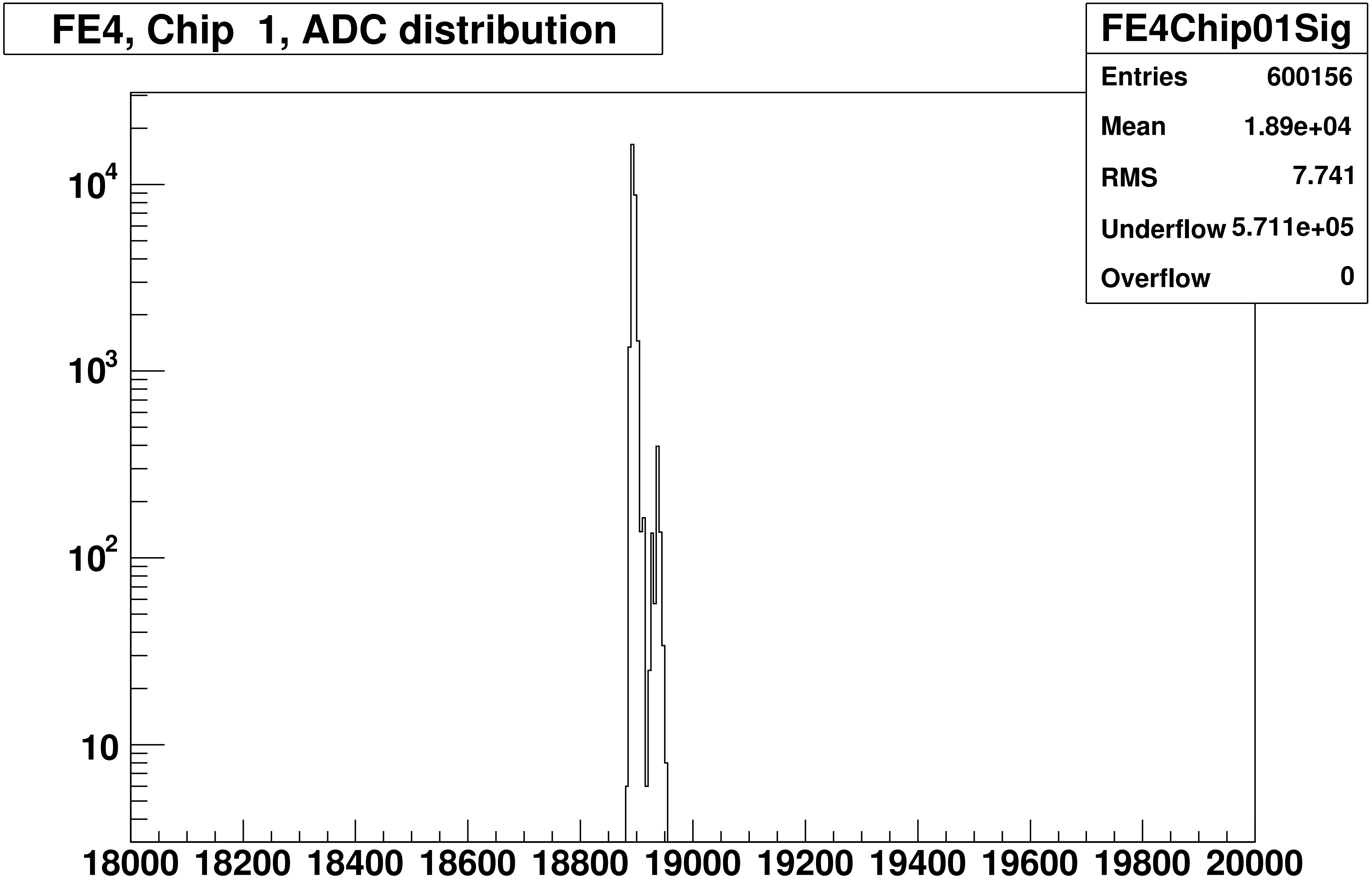
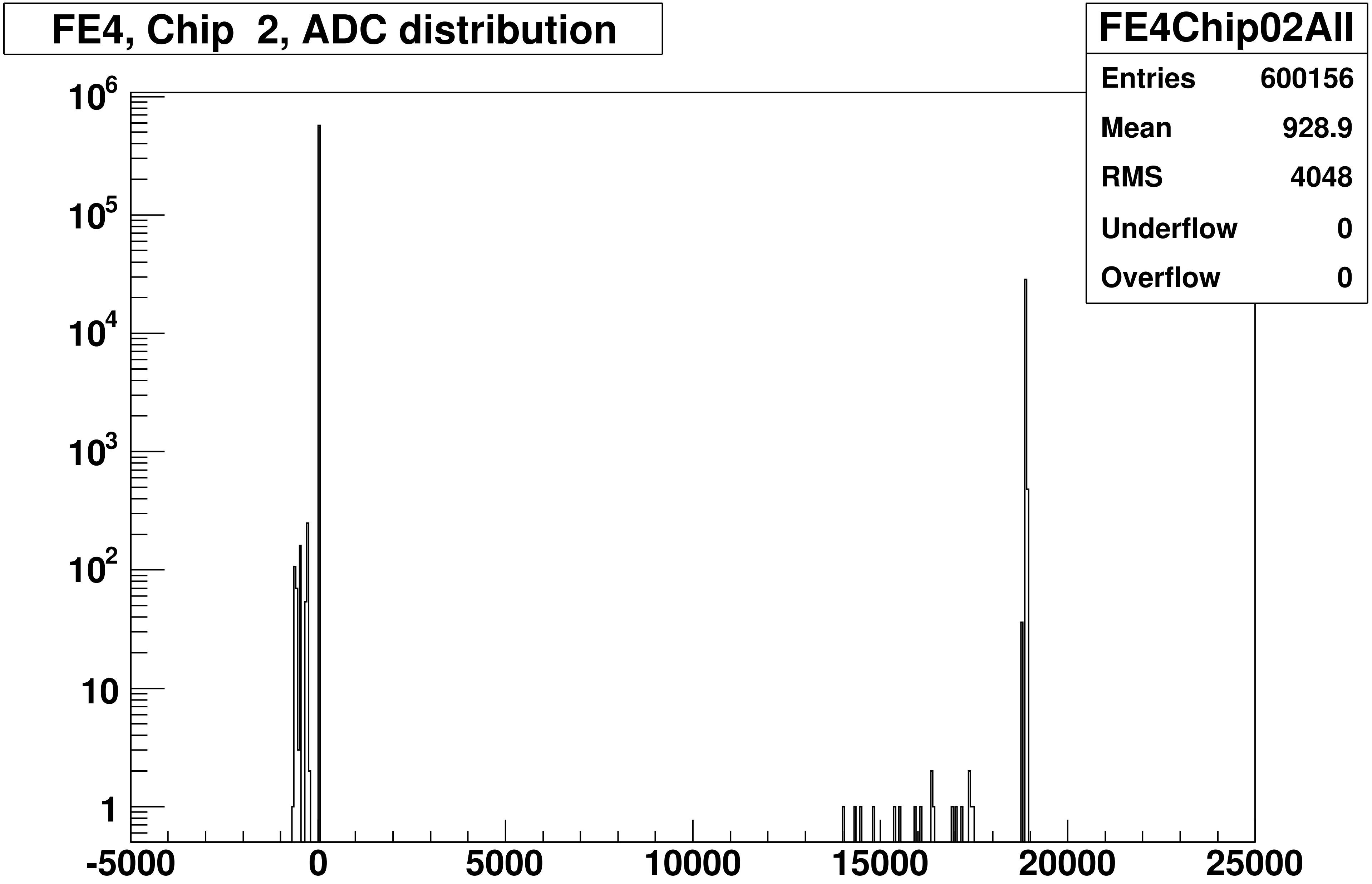
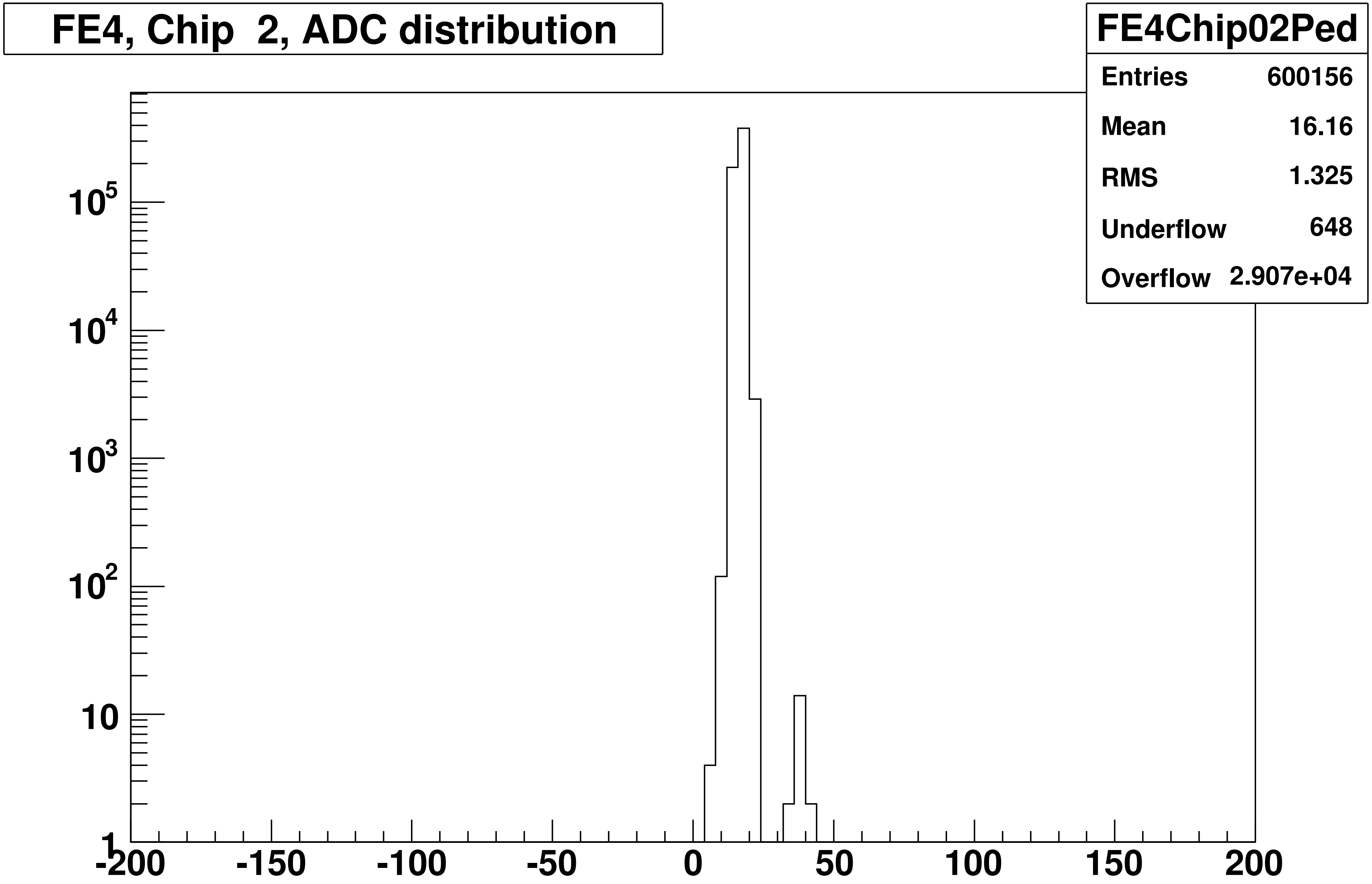
10^2
10^3
10^4
10^5
-200
-150
-100
-50
0
50
100
150
200



FE4, Chip 1, ADC distribution
FE4Chip01Sig
Entries 600156
Mean 1.89e+04
RMS 7.741
Underflow 5.711e+05
Overflow 0
10^4
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE4, Chip 2, ADC distribution
FE4Chip02All
Entries 600156
Mean 928.9
RMS 4048
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE4, Chip 2, ADC distribution
FE4Chip02Ped
Entries 600156
Mean 16.16
RMS 1.325
Underflow 648
Overflow 2.907e+04
10^5
10^4
10^3
10^2
10
1
-200
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-100
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0
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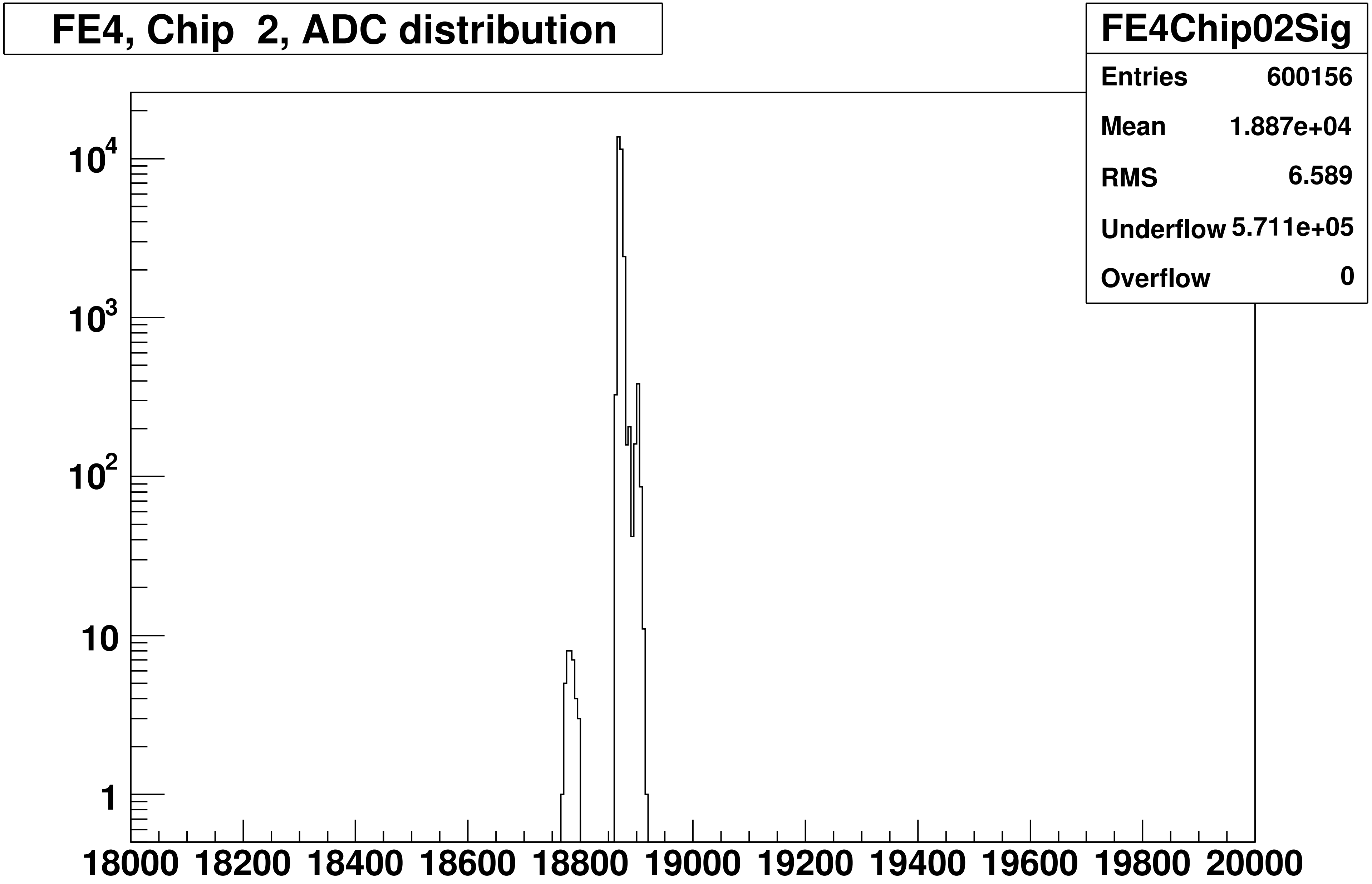
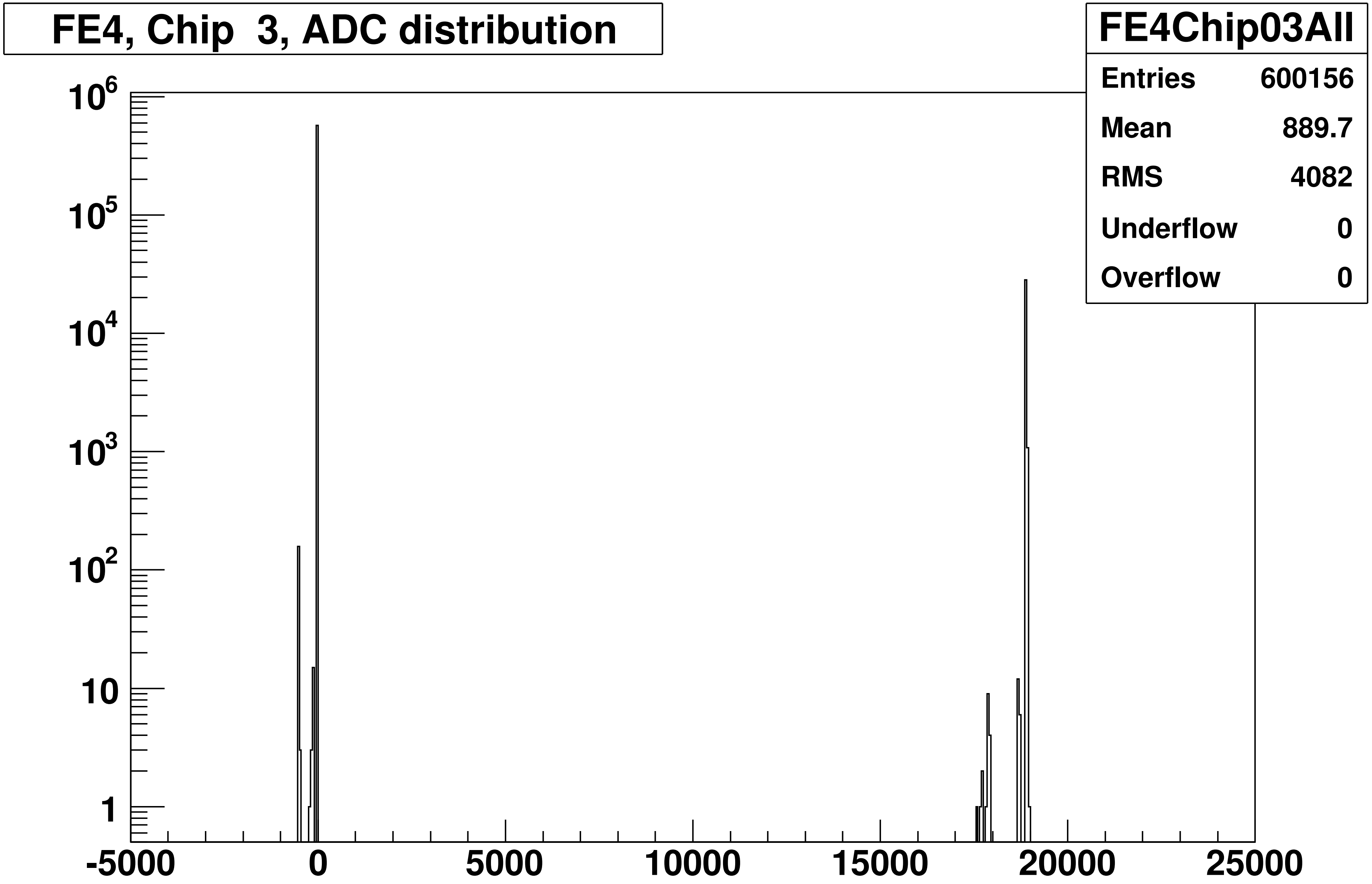
100
150
200



FE4, Chip 2, ADC distribution
FE4Chip02Sig
Entries 600156
Mean 1.887e+04
RMS 6.589
Underflow 5.711e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE4, Chip 3, ADC distribution
FE4Chip03All
Entries 600156
Mean 889.7
RMS 4082
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
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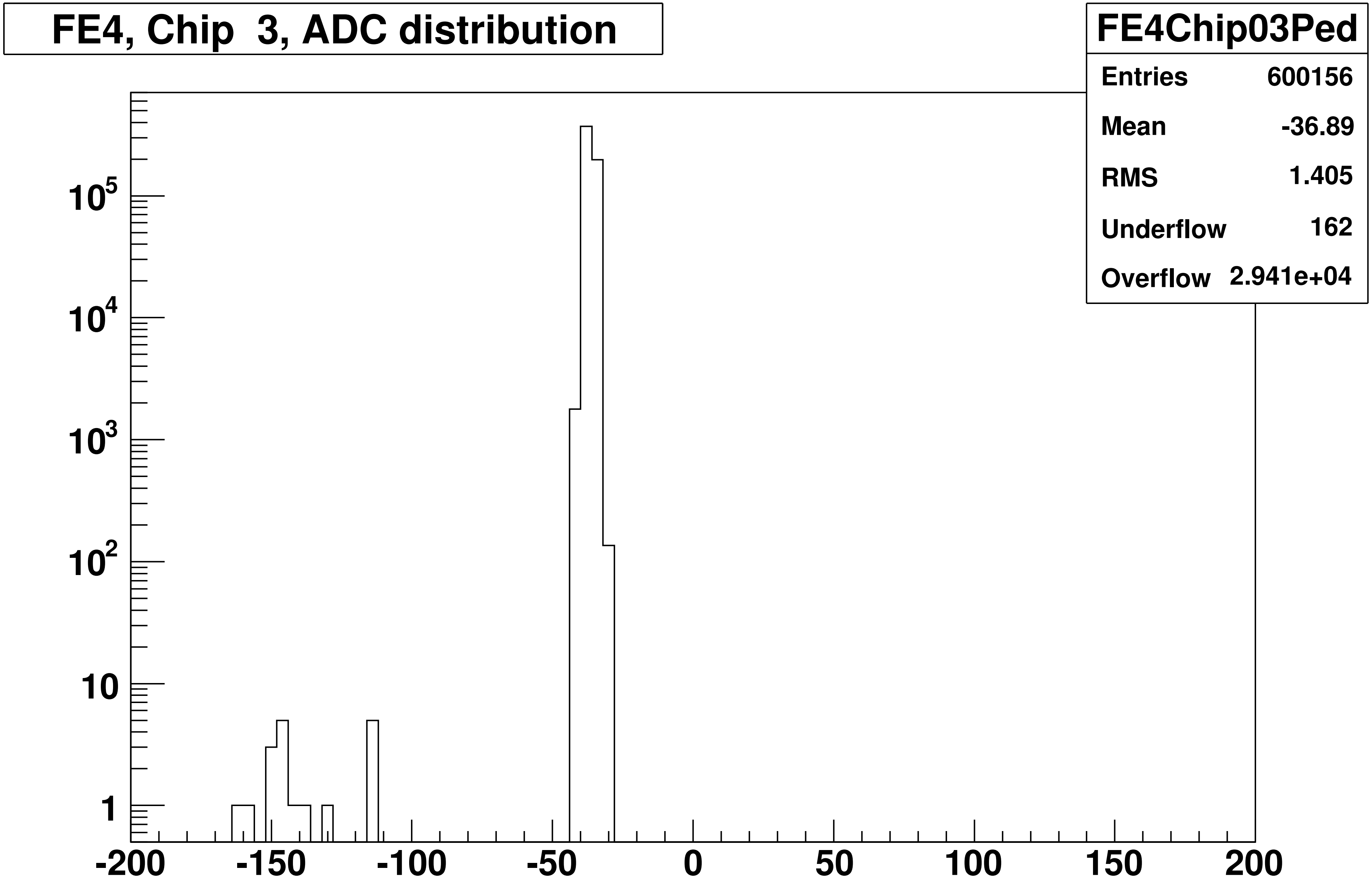
25000



FE4, Chip 3, ADC distribution
FE4Chip03Ped
Entries 600156
Mean -36.89
RMS 1.405
Underflow 162
Overflow 2.941e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
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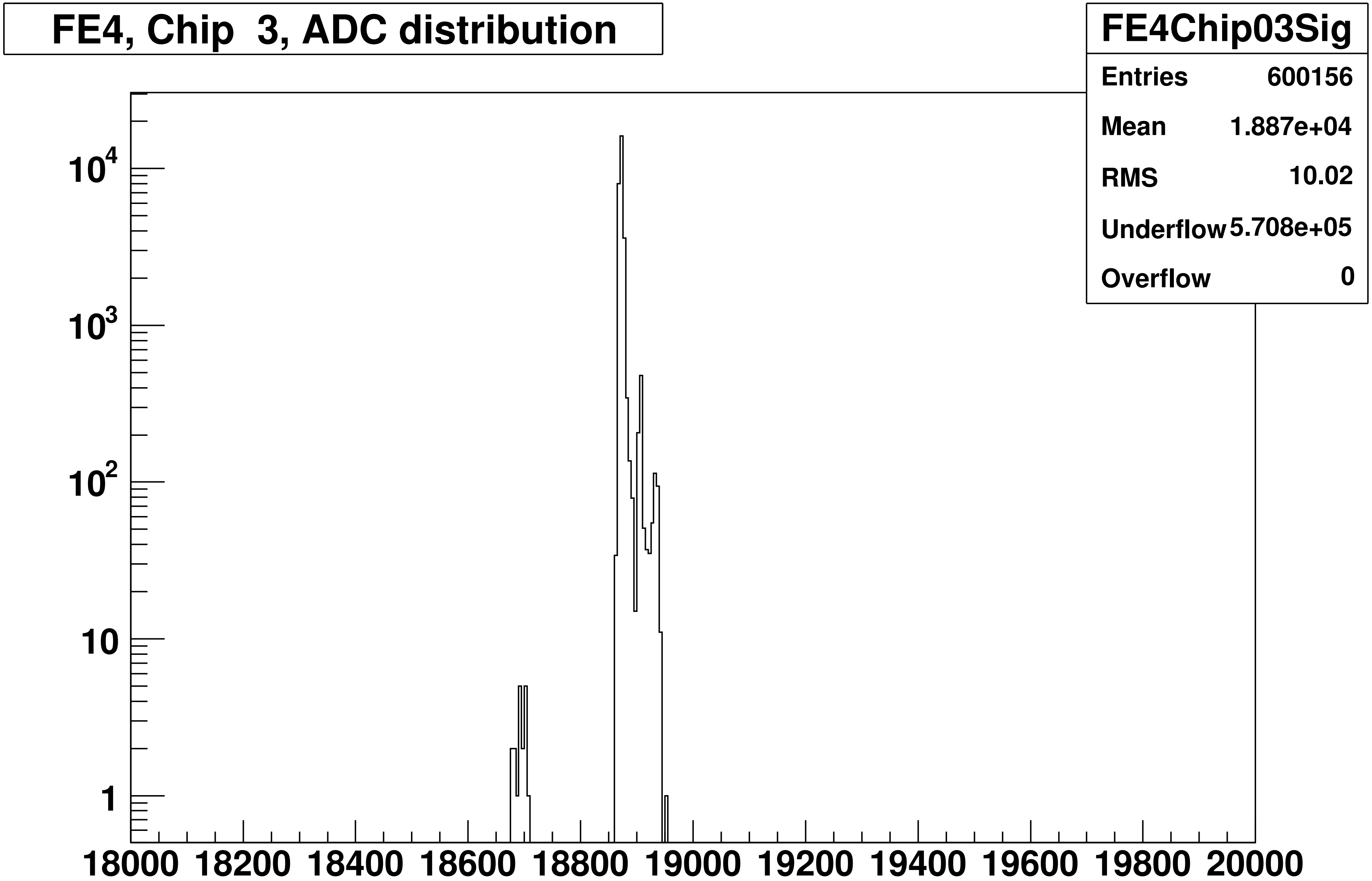
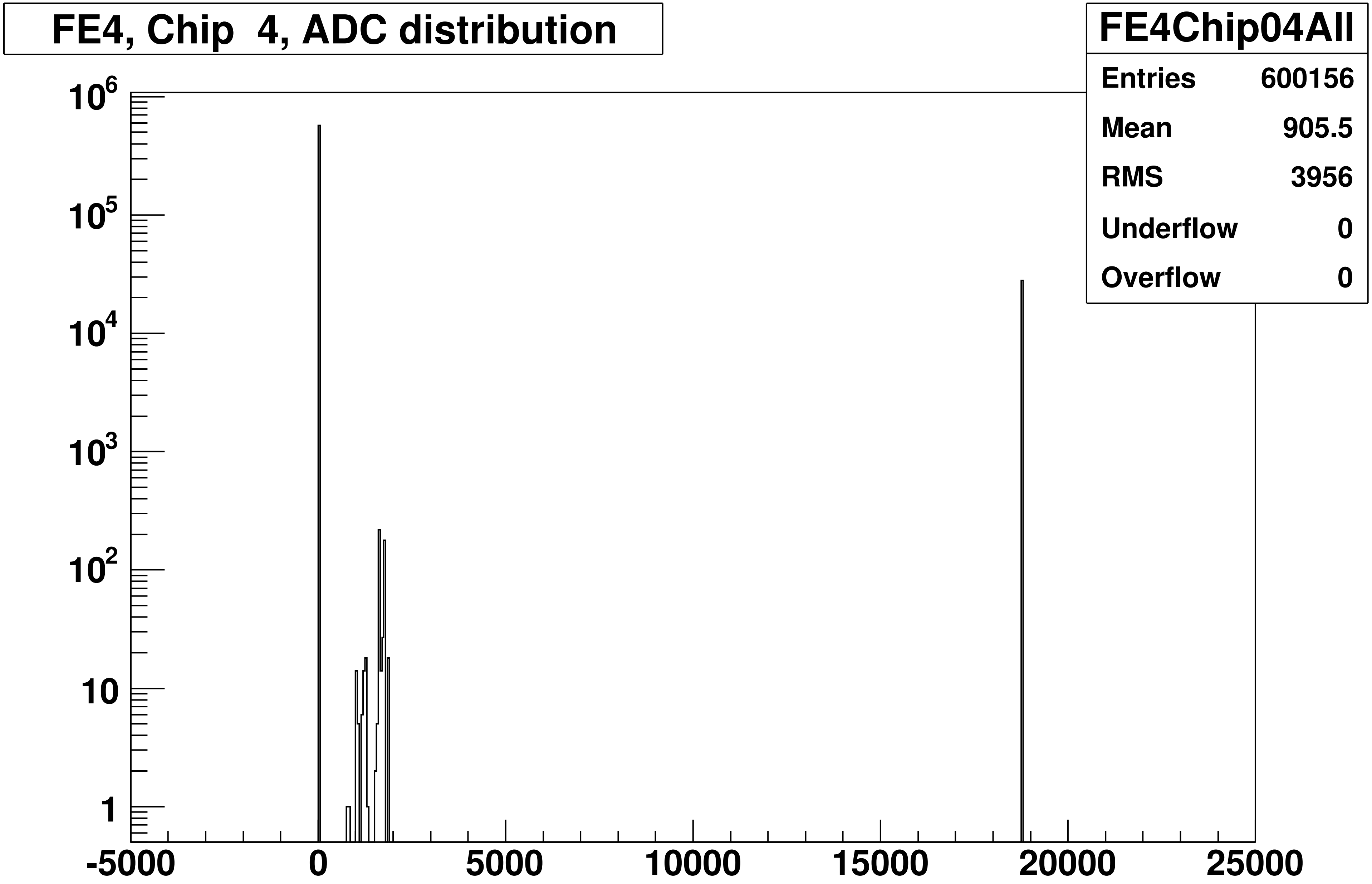
0
50
100
150
200



FE4, Chip 3, ADC distribution
FE4Chip03Sig
Entries 600156
Mean 1.887e+04
RMS 10.02
Underflow 5.708e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE4, Chip 4, ADC distribution
FE4Chip04All
Entries 600156
Mean 905.5
RMS 3956
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
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-5000
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5000
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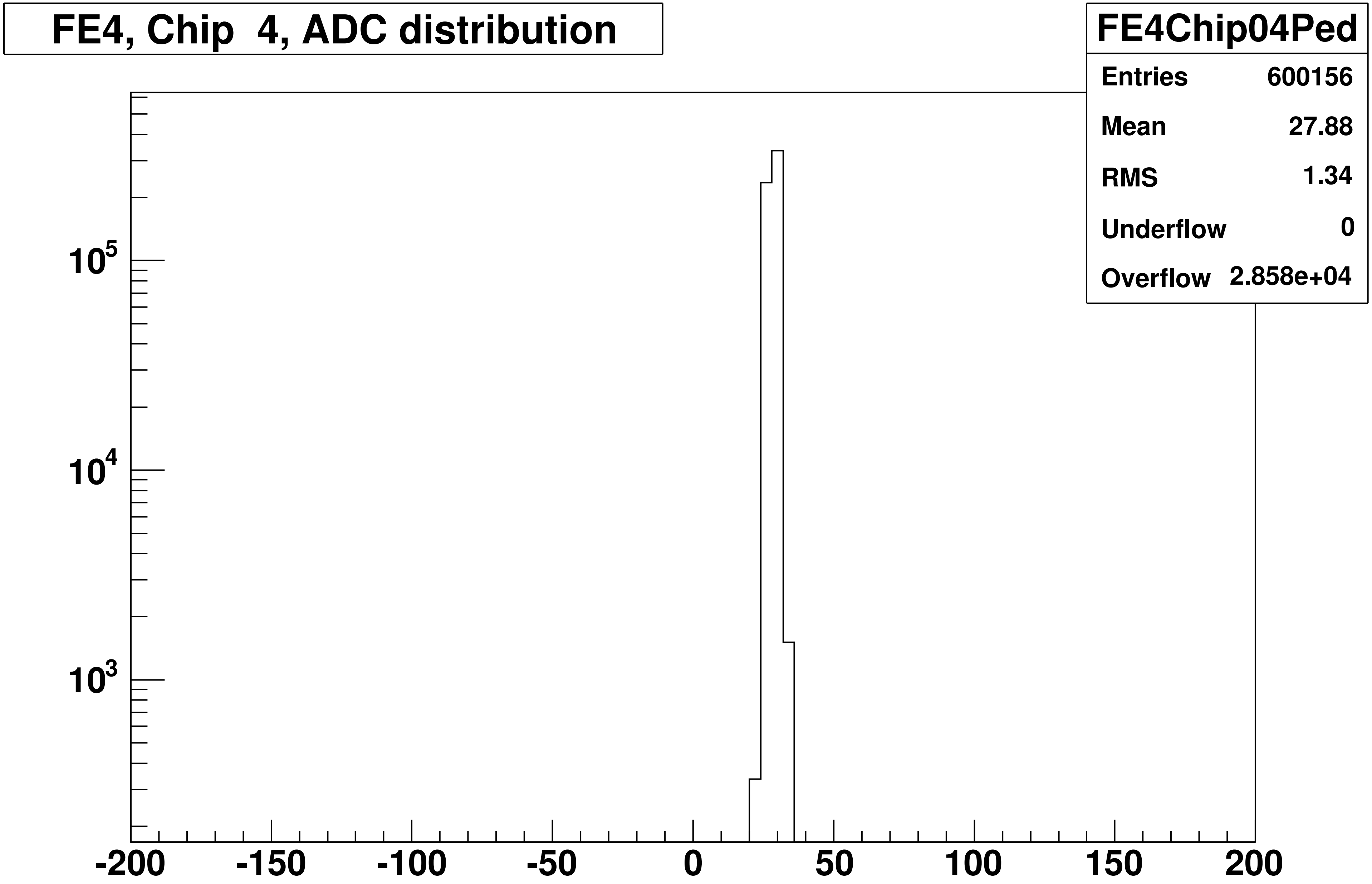

FE4, Chip 4, ADC distribution
FE4Chip04Ped
Entries 600156
Mean 27.88
RMS 1.34
Underflow 0
Overflow 2.858e+04
10^5
10^4
10^3
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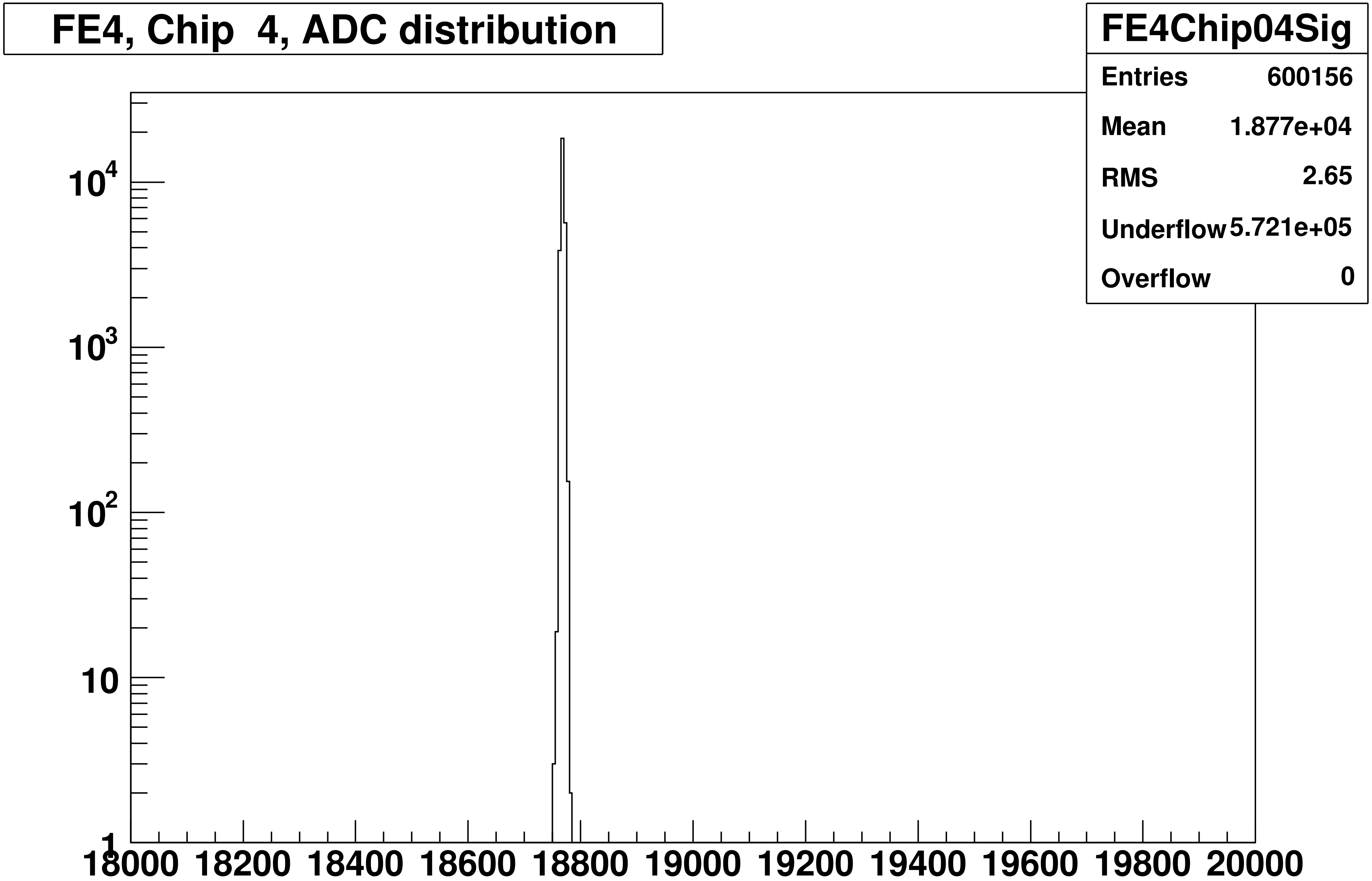
-100
-50
0
50
100
150
200



FE4, Chip 4, ADC distribution
FE4Chip04Sig
Entries 600156
Mean 1.877e+04
RMS 2.65
Underflow 5.721e+05
Overflow 0
10^4
10^3
10^2
10
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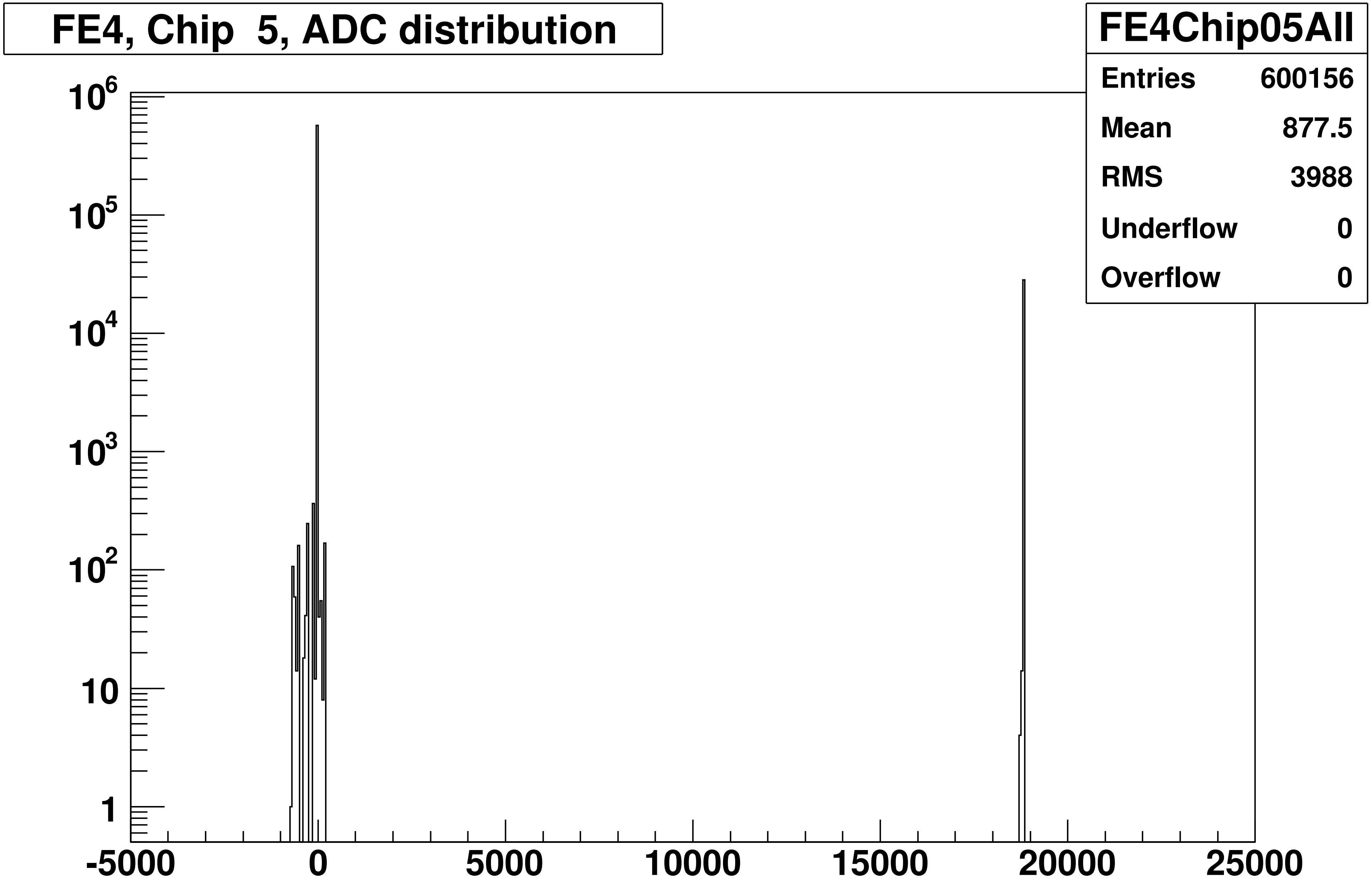
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE4, Chip 5, ADC distribution
FE4Chip05All
Entries 600156
Mean 877.5
RMS 3988
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
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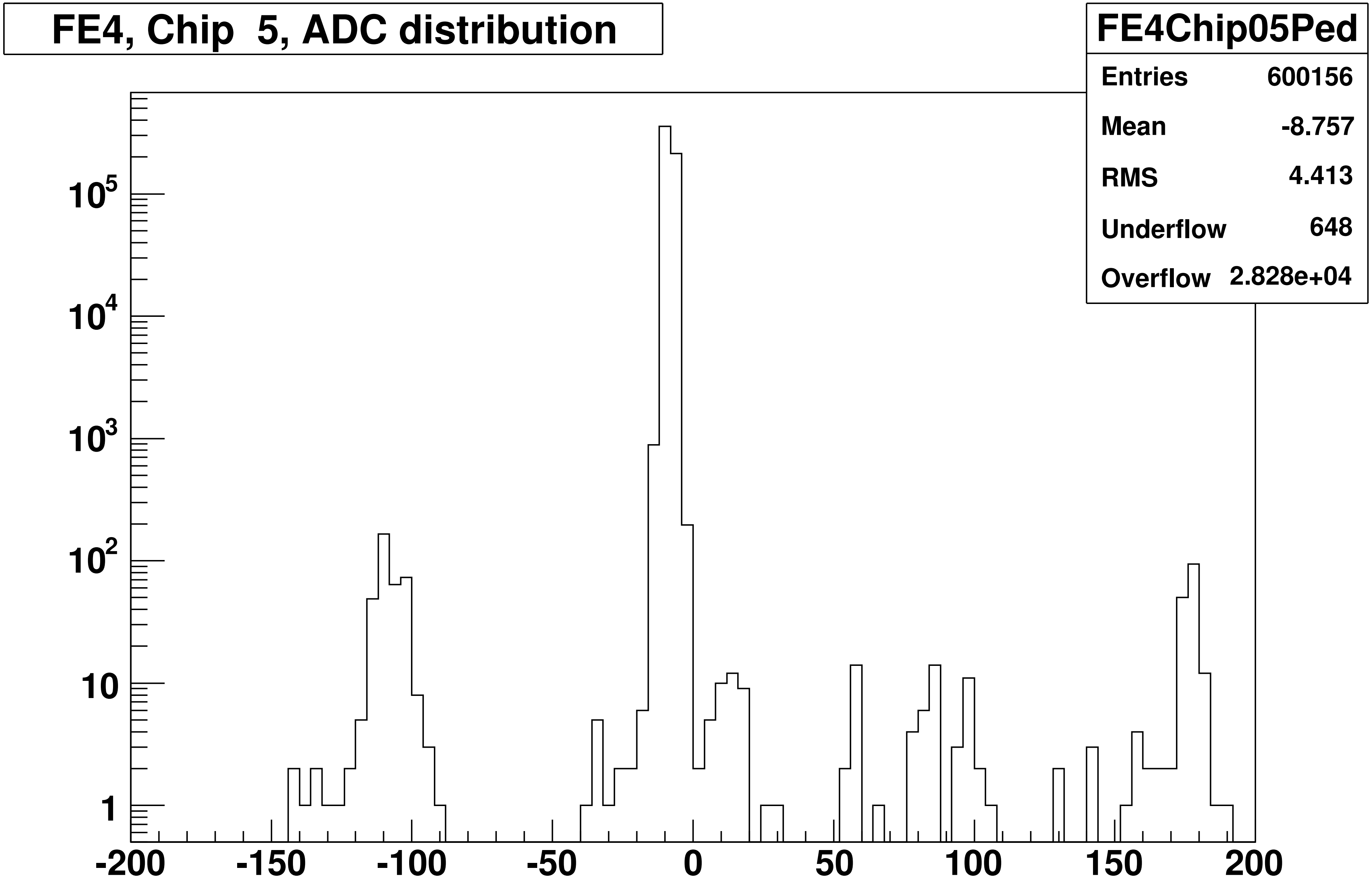
20000
25000



FE4, Chip 5, ADC distribution
FE4Chip05Ped
Entries 600156
Mean -8.757
RMS 4.413
Underflow 648
Overflow 2.828e+04
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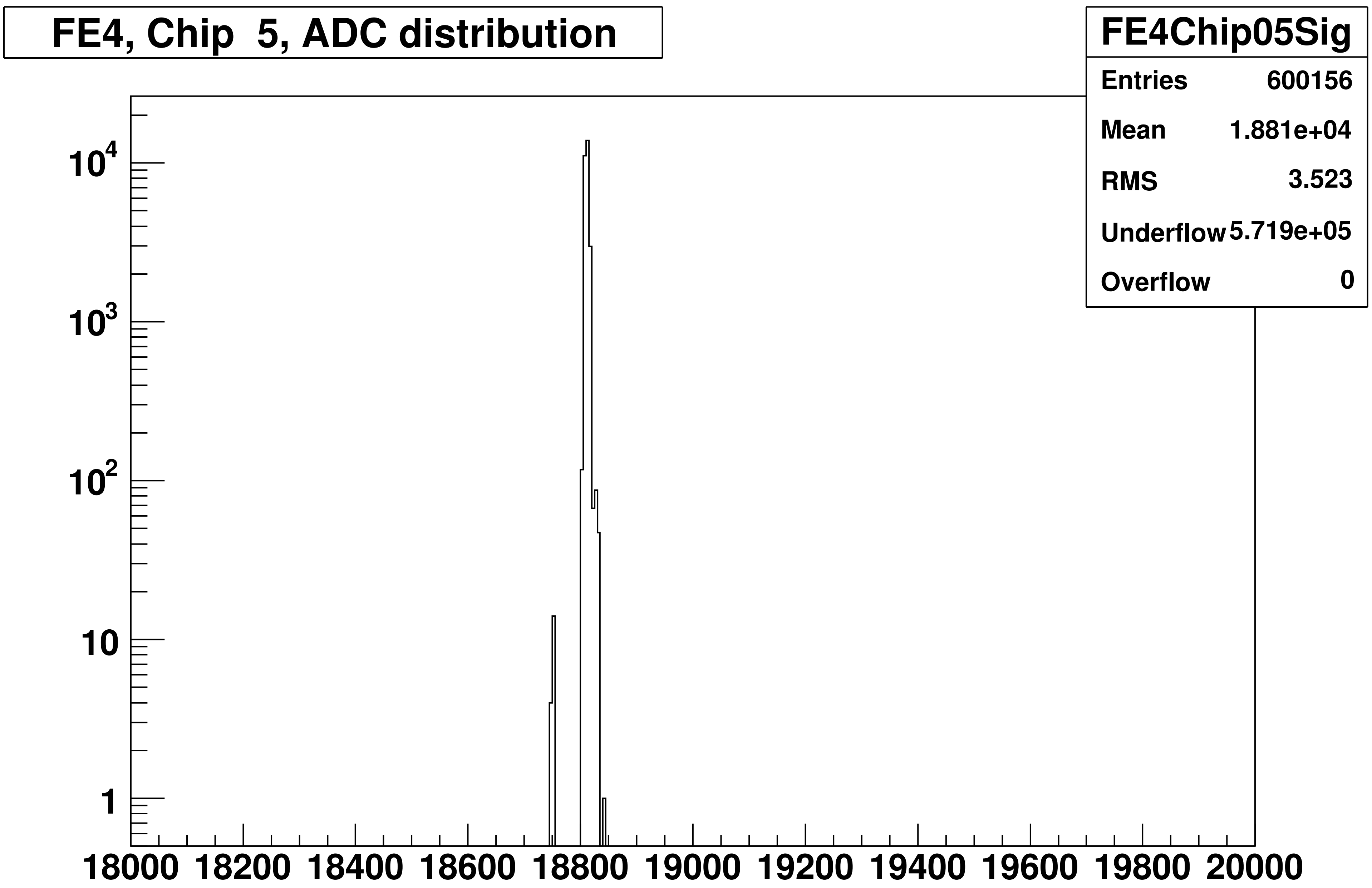
FE4, Chip 5, ADC distribution
FE4Chip05Sig
Entries 600156
Mean 1.881e+04
RMS 3.523
Underflow 5.719e+05
Overflow 0
10^4
10^3
10^2
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18000
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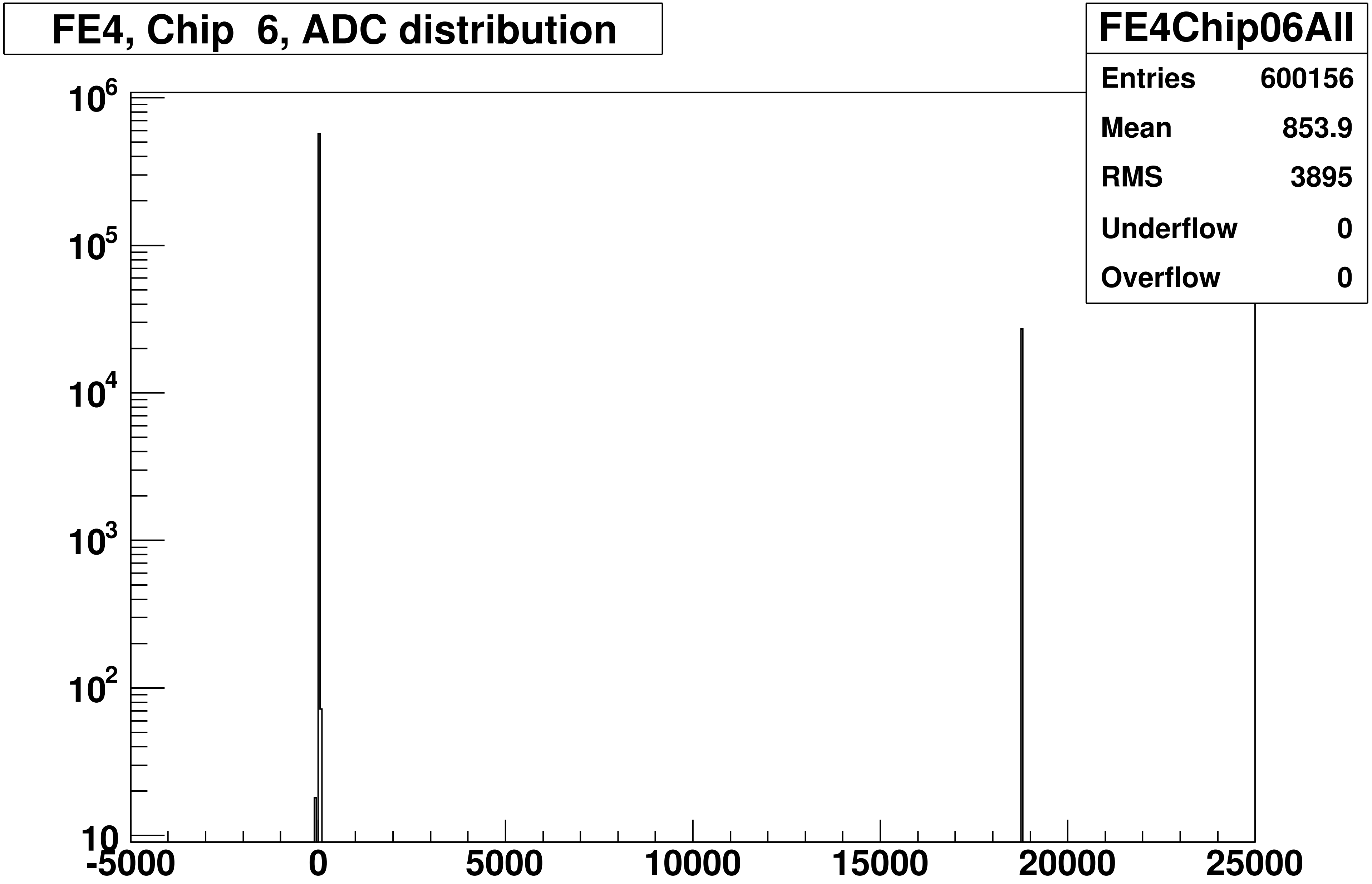
FE4, Chip 6, ADC distribution
FE4Chip06All
Entries 600156
Mean 853.9
RMS 3895
Underflow 0
Overflow 0
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10^3
10^4
10^5
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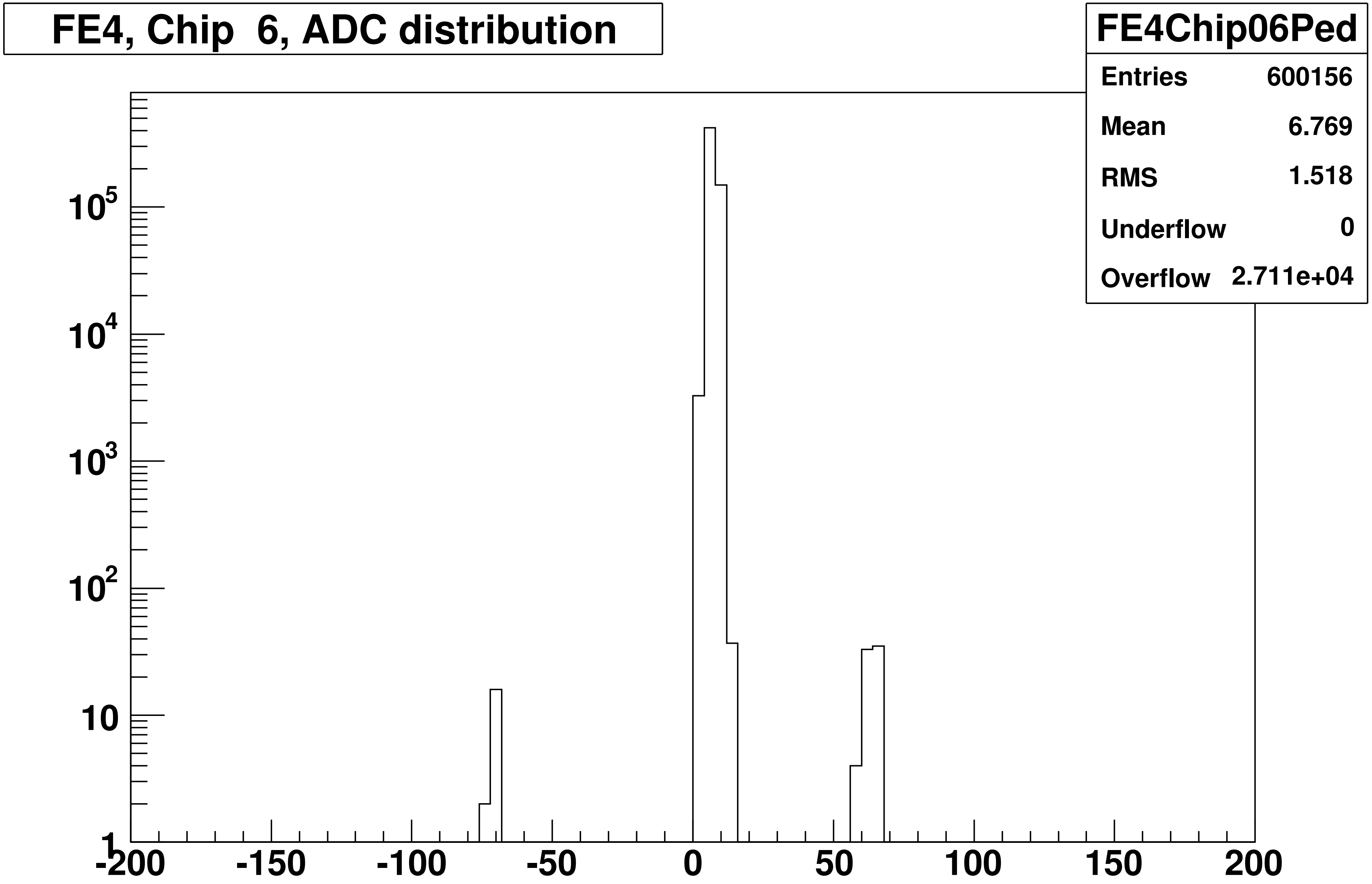

FE4, Chip 6, ADC distribution
FE4Chip06Ped
Entries 600156
Mean 6.769
RMS 1.518
Underflow 0
Overflow 2.711e+04
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10^3
10^2
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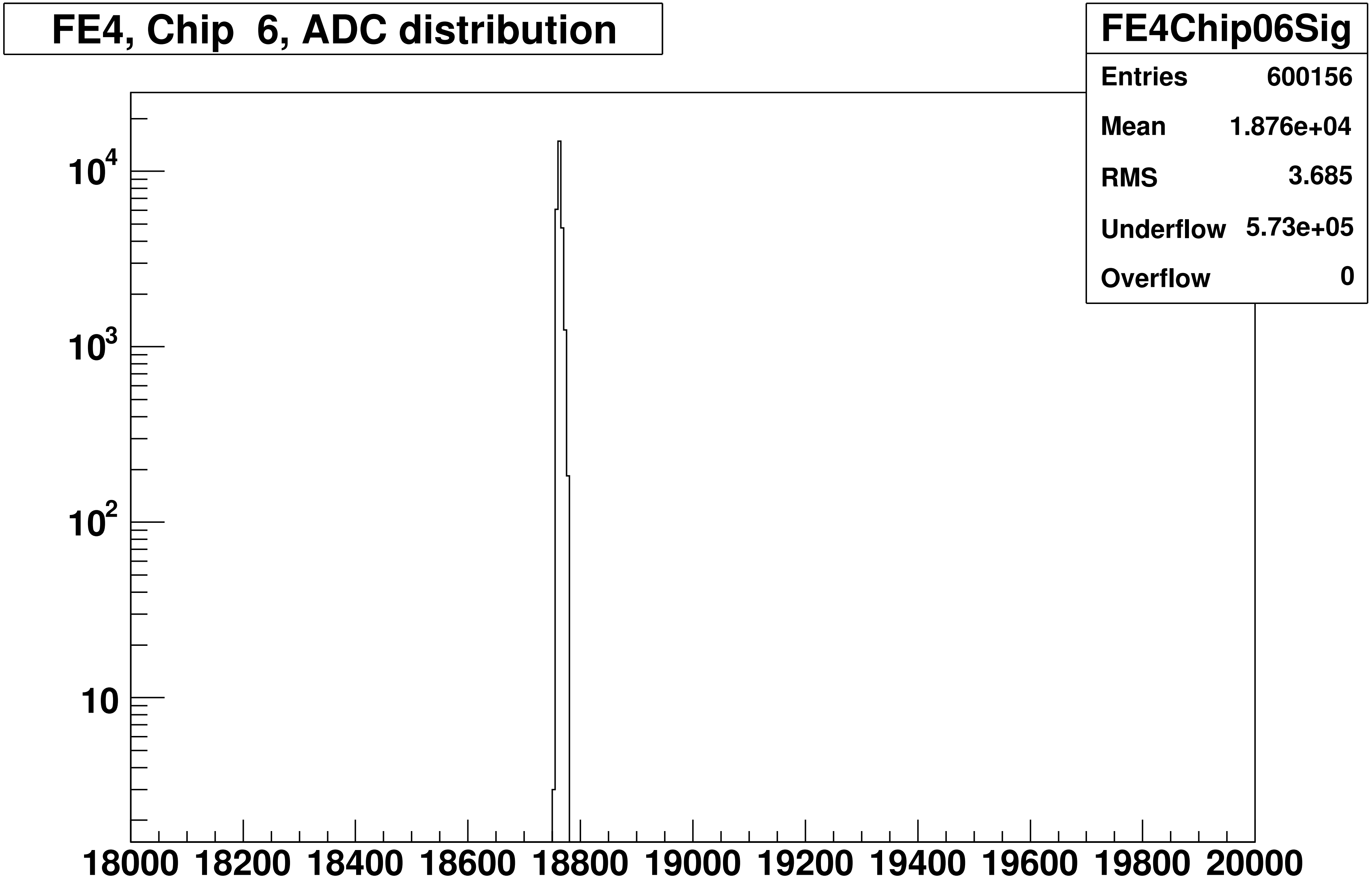
FE4, Chip 6, ADC distribution
FE4Chip06Sig
Entries 600156
Mean 1.876e+04
RMS 3.685
Underflow 5.73e+05
Overflow 0
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10^2
10^3
10^4
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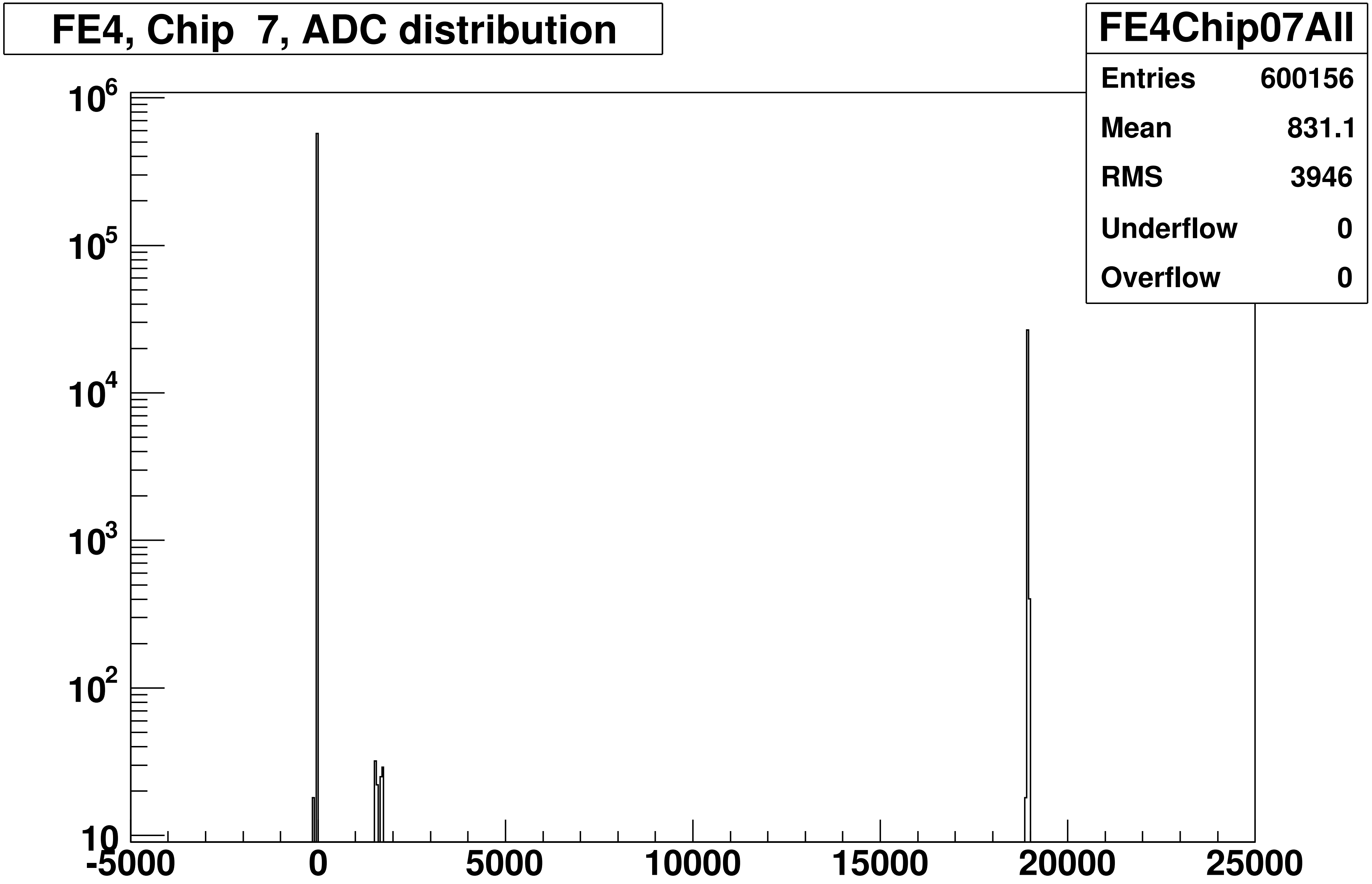
FE4, Chip 7, ADC distribution
FE4Chip07All
Entries 600156
Mean 831.1
RMS 3946
Underflow 0
Overflow 0
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10^3
10^4
10^5
10^6
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10000
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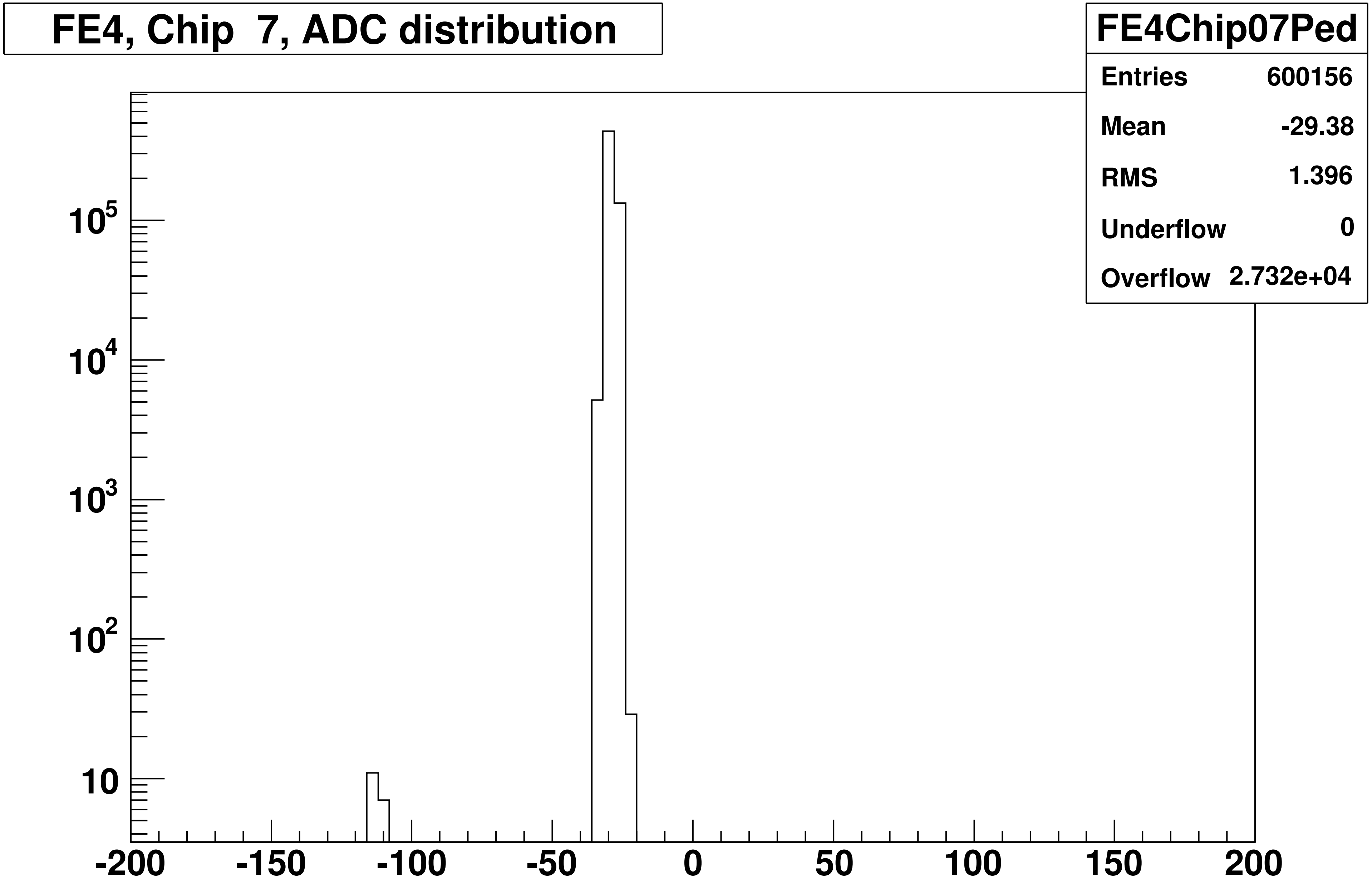
FE4, Chip 7, ADC distribution
FE4Chip07Ped
Entries 600156
Mean -29.38
RMS 1.396
Underflow 0
Overflow 2.732e+04
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10^3
10^4
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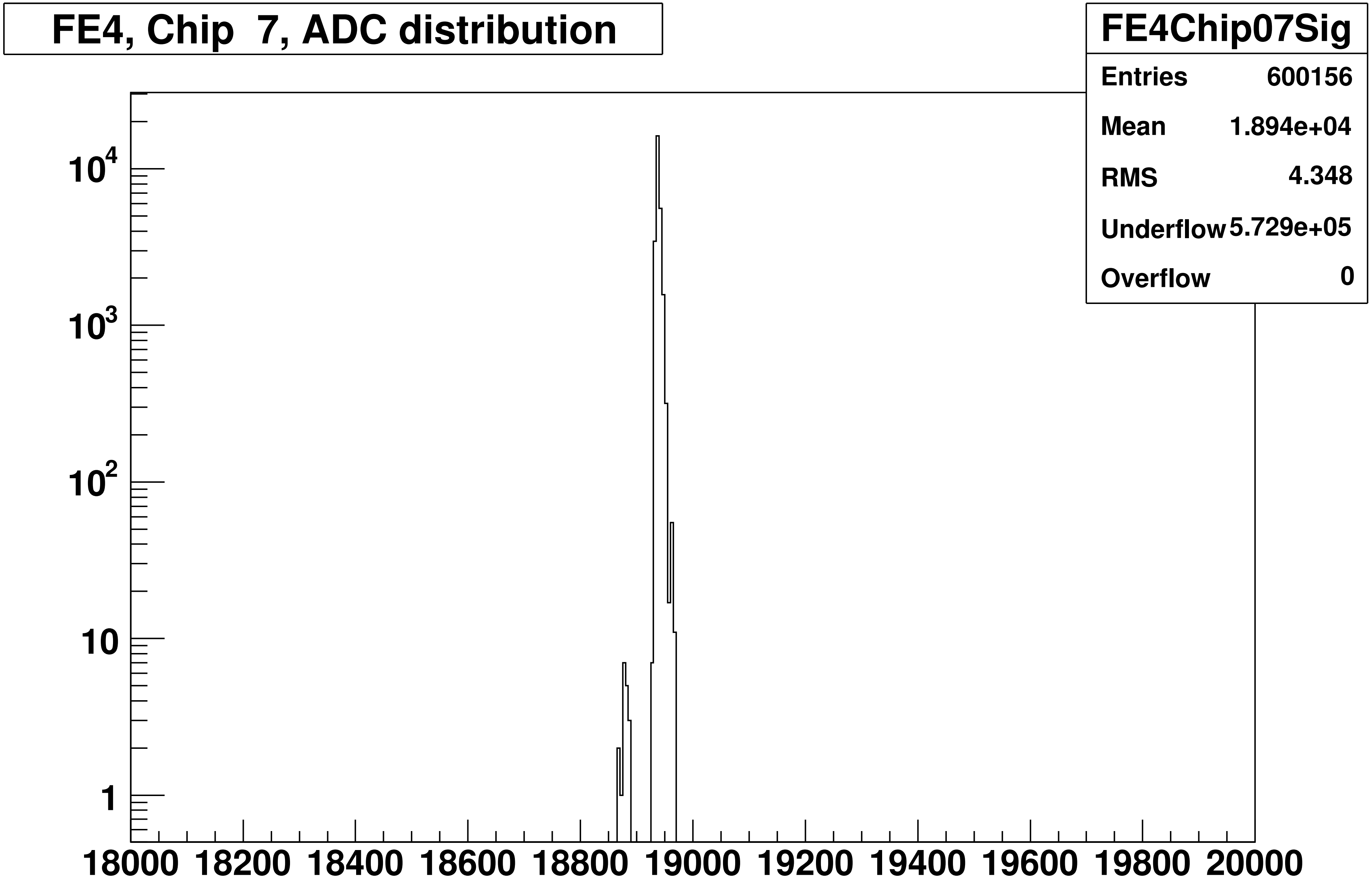
FE4, Chip 7, ADC distribution
FE4Chip07Sig
Entries 600156
Mean 1.894e+04
RMS 4.348
Underflow 5.729e+05
Overflow 0
10^4
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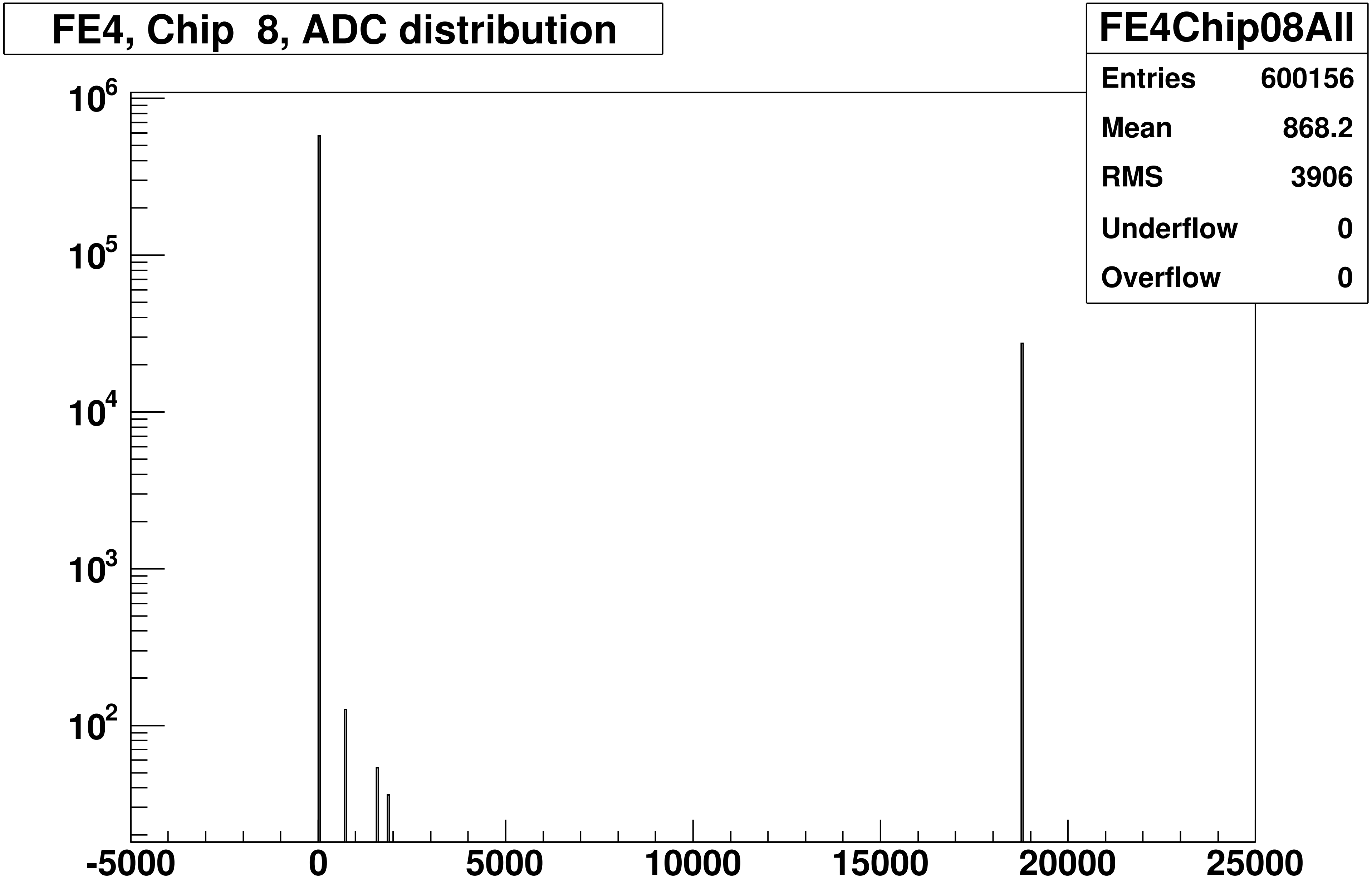

FE4, Chip 8, ADC distribution
FE4Chip08All
Entries 600156
Mean 868.2
RMS 3906
Underflow 0
Overflow 0
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10^5
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10^3
10^2
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20000
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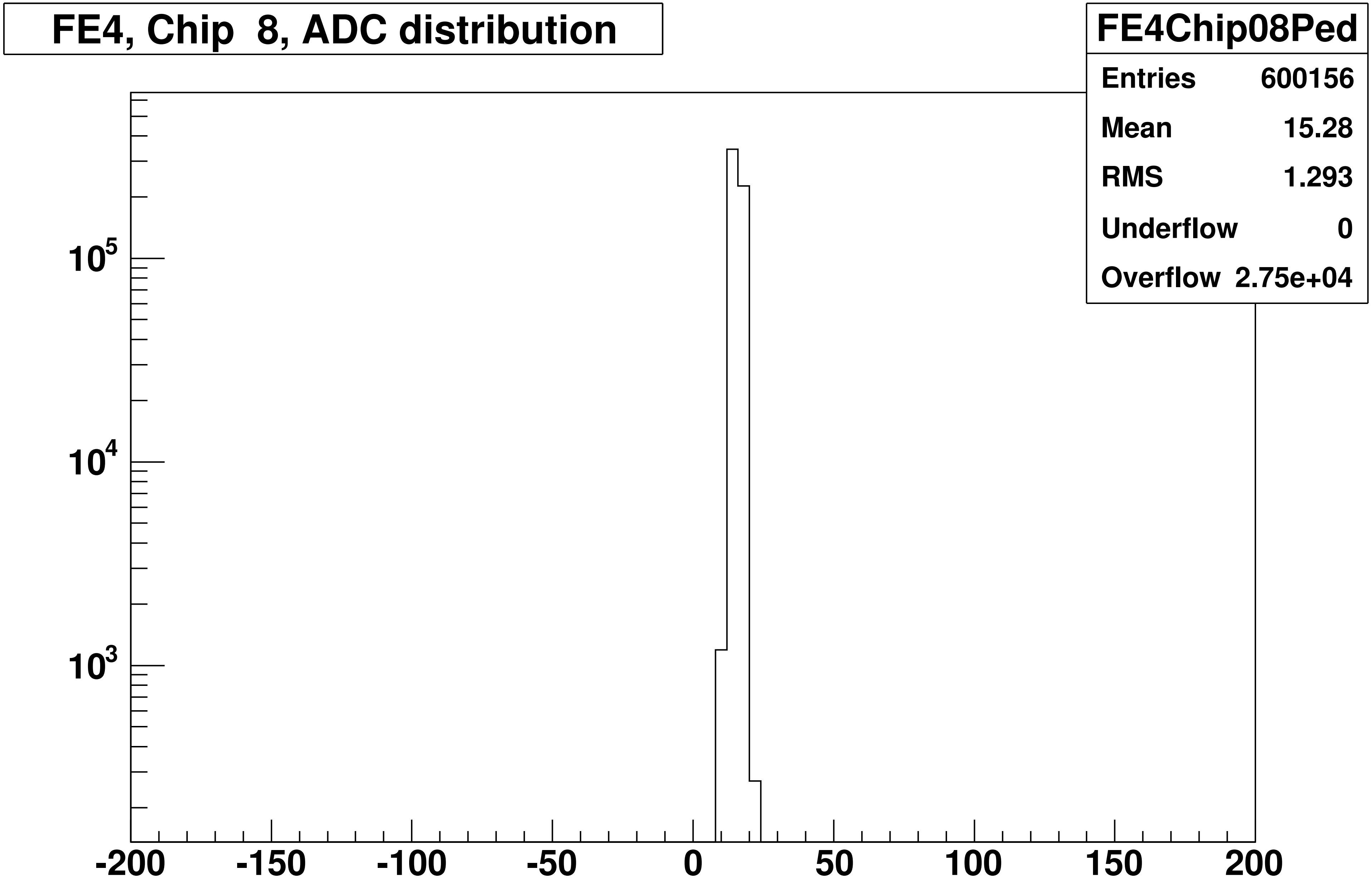
FE4, Chip 8, ADC distribution
FE4Chip08Ped
Entries 600156
Mean 15.28
RMS 1.293
Underflow 0
Overflow 2.75e+04
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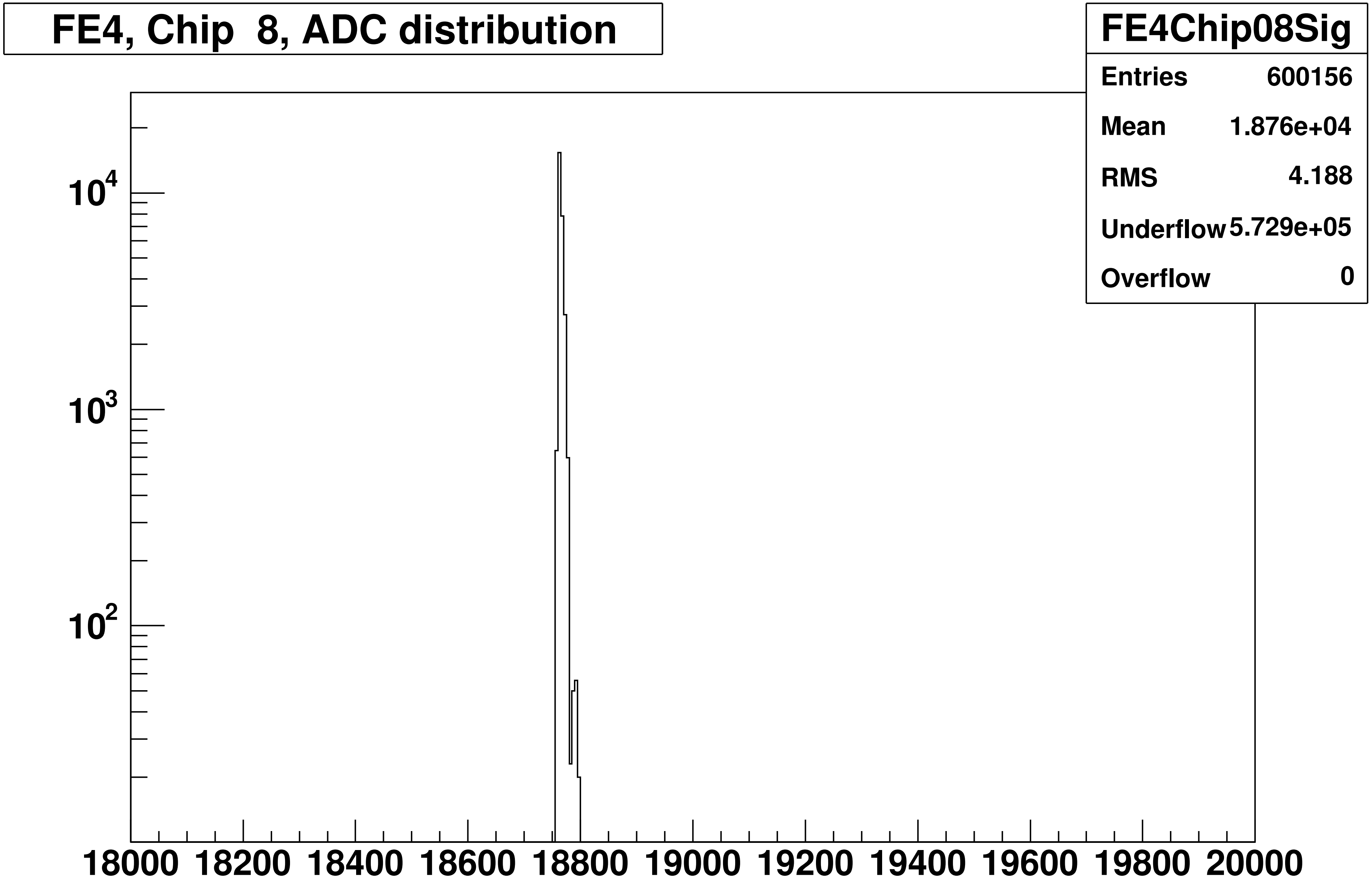

FE4, Chip 8, ADC distribution
FE4Chip08Sig
Entries 600156
Mean 1.876e+04
RMS 4.188
Underflow 5.729e+05
Overflow 0
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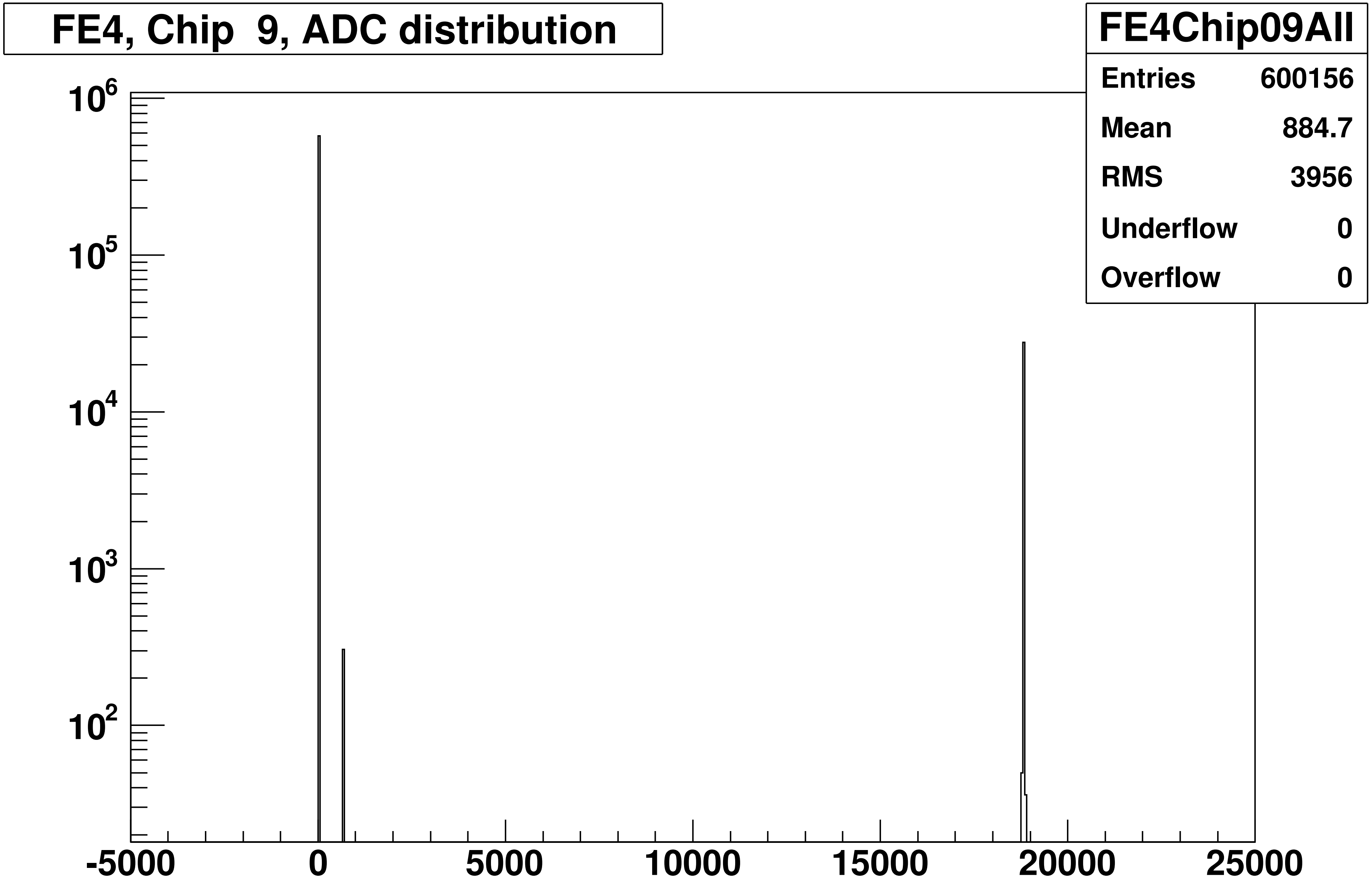
10^3
10^2
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE4, Chip 9, ADC distribution
FE4Chip09All
Entries 600156
Mean 884.7
RMS 3956
Underflow 0
Overflow 0
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10^5
10^4
10^3
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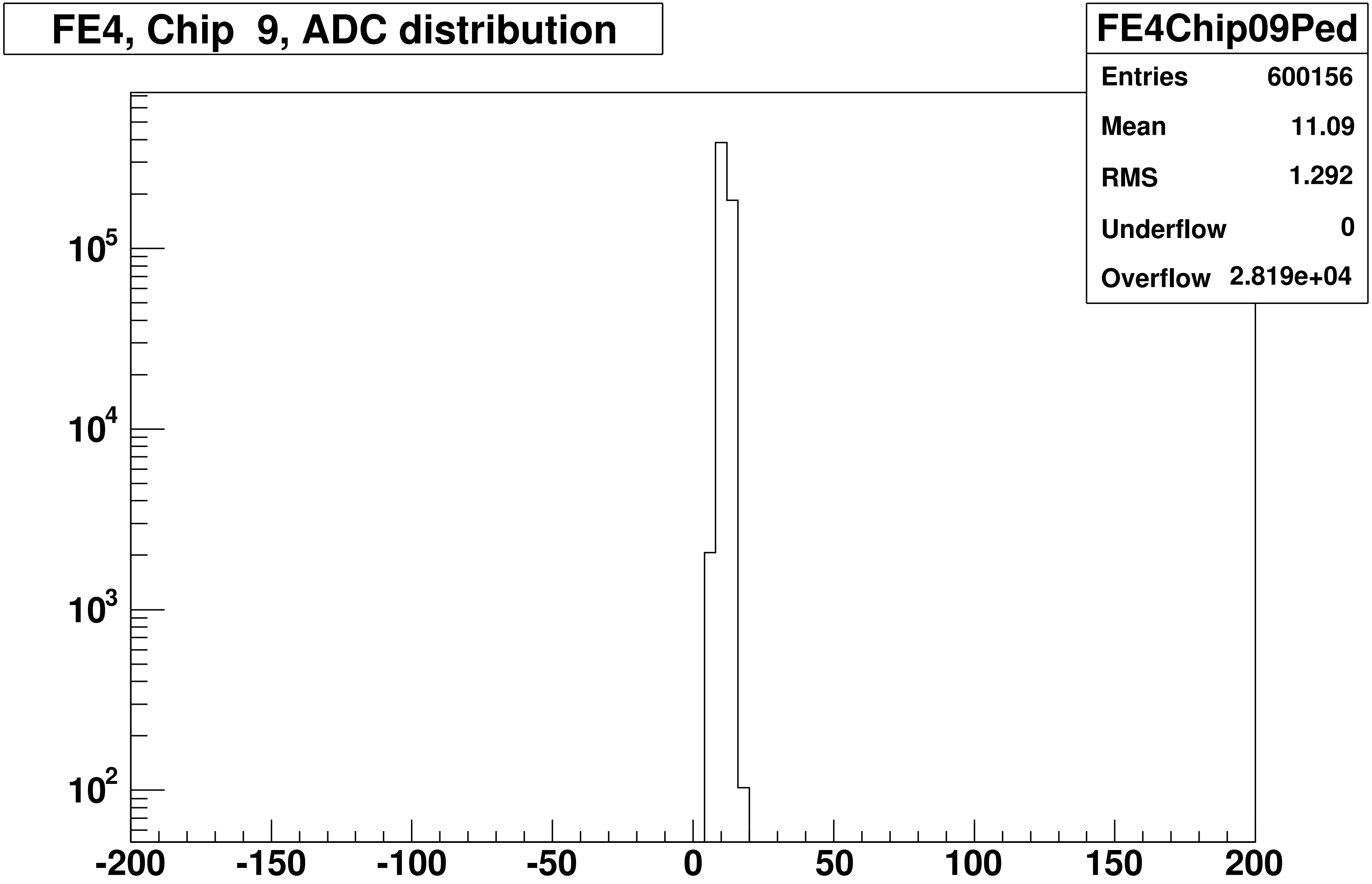
FE4, Chip 9, ADC distribution
FE4Chip09Ped
Entries 600156
Mean 11.09
RMS 1.292
Underflow 0
Overflow 2.819e+04
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10^3
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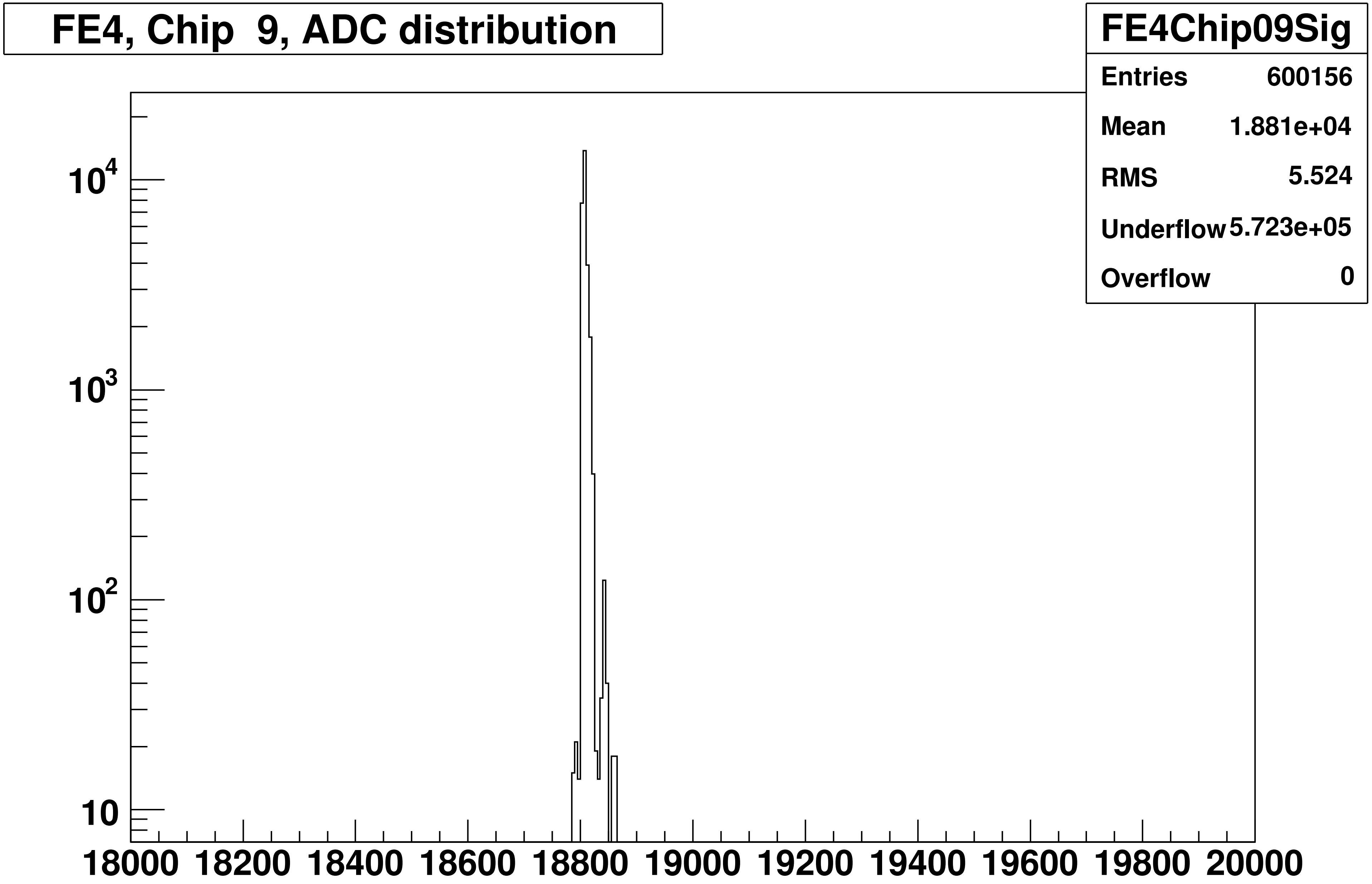
FE4, Chip 9, ADC distribution
FE4Chip09Sig
Entries 600156
Mean 1.881e+04
RMS 5.524
Underflow 5.723e+05
Overflow 0
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10^2
10^3
10^4
18000
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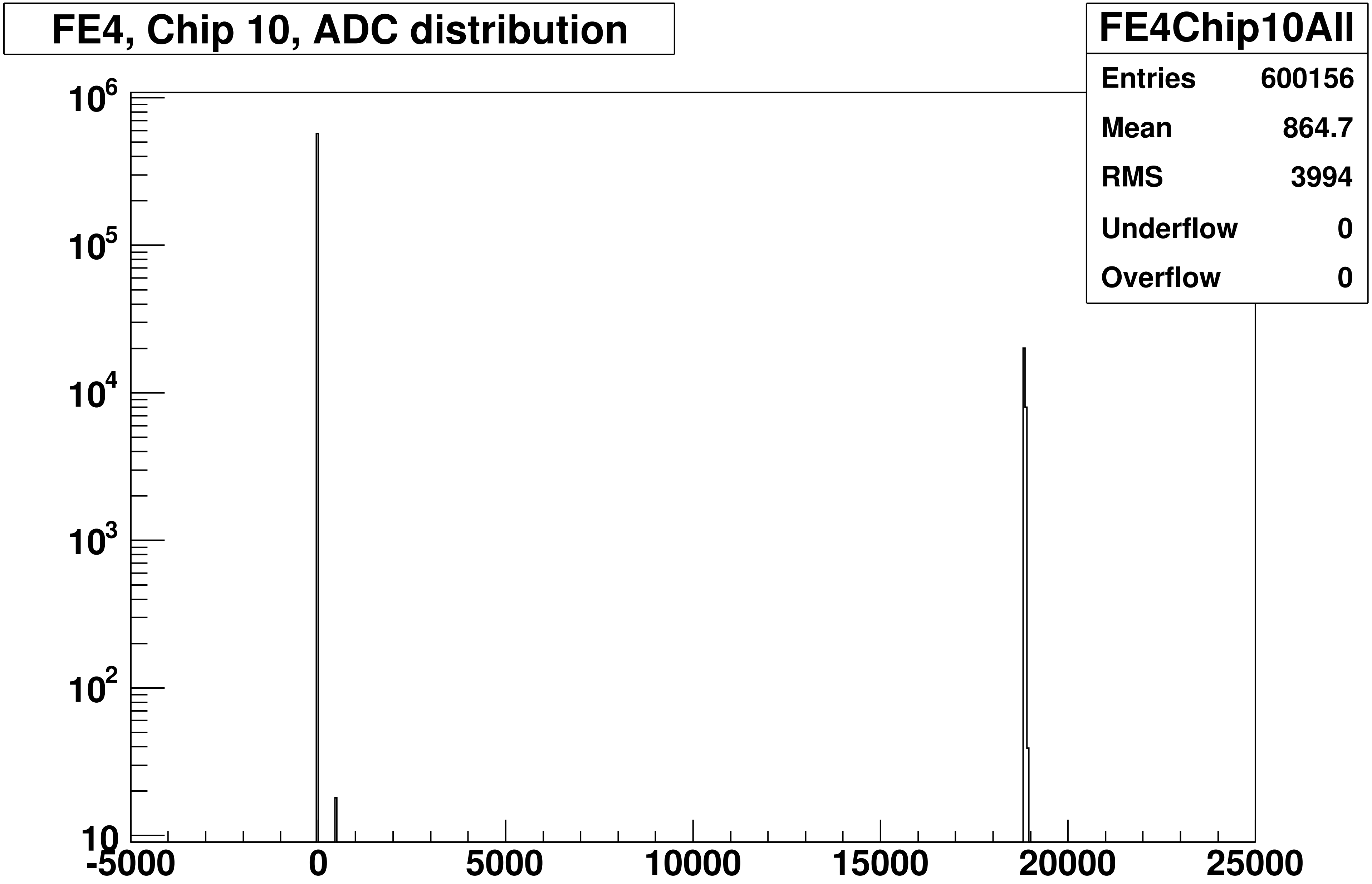
FE4, Chip 10, ADC distribution
FE4Chip10All
Entries 600156
Mean 864.7
RMS 3994
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
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10000
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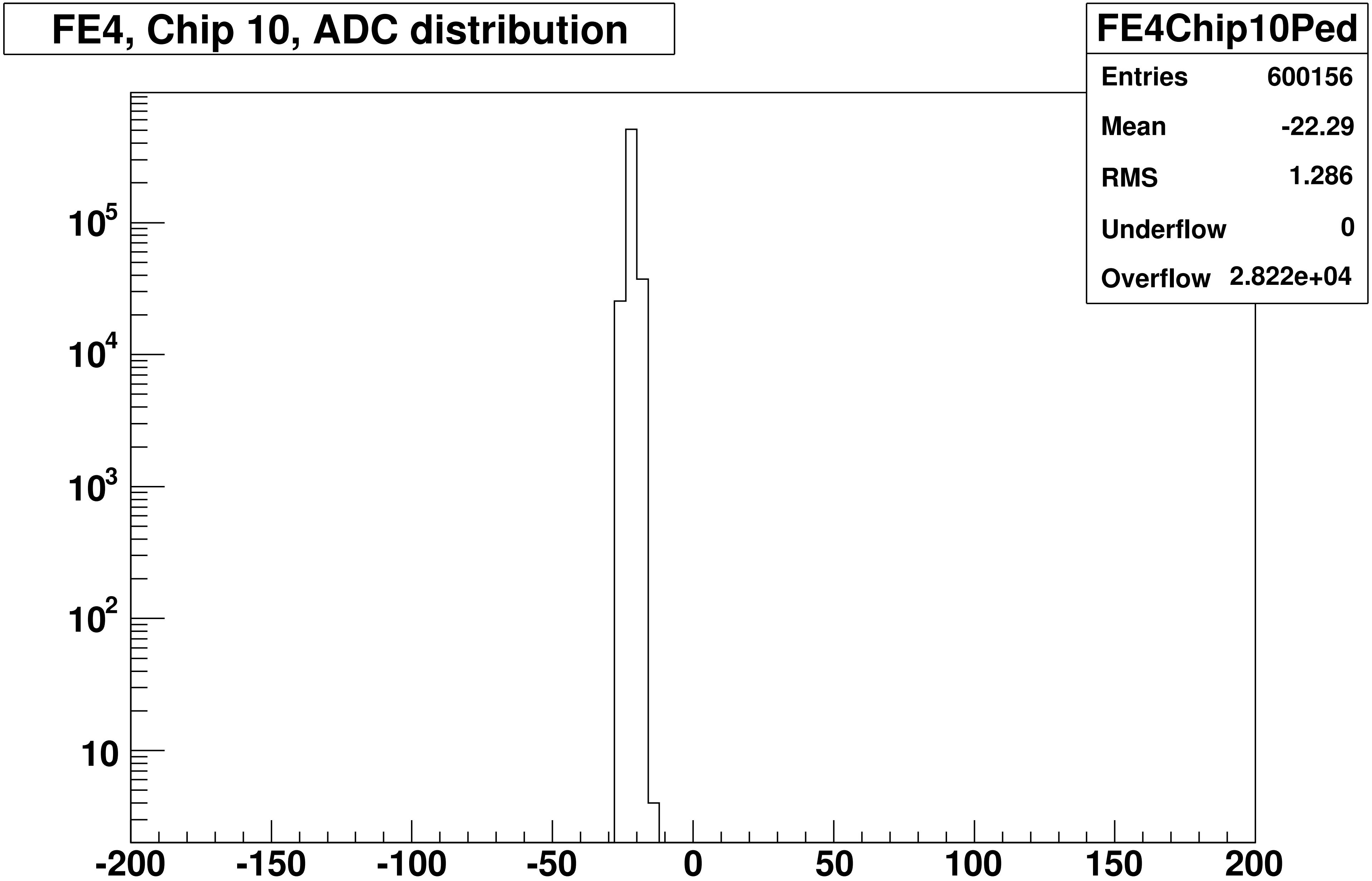
20000
25000


FE4, Chip 10, ADC distribution
FE4Chip10Ped
Entries 600156
Mean -22.29
RMS 1.286
Underflow 0
Overflow 2.822e+04
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10^4
10^3
10^2
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150
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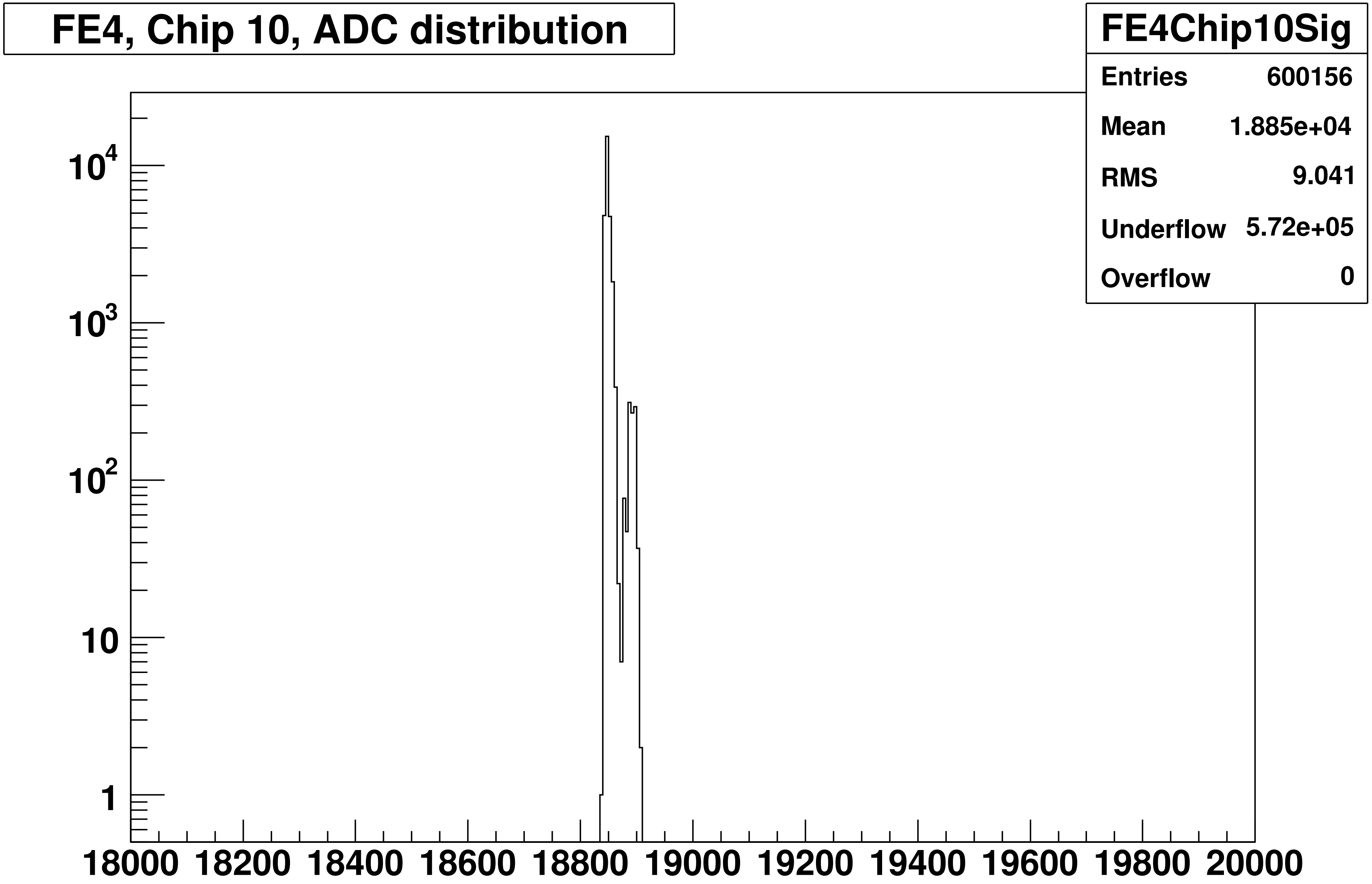

FE4, Chip 10, ADC distribution
FE4Chip10Sig
Entries 600156
Mean 1.885e+04
RMS 9.041
Underflow 5.72e+05
Overflow 0
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10^3
10^2
10
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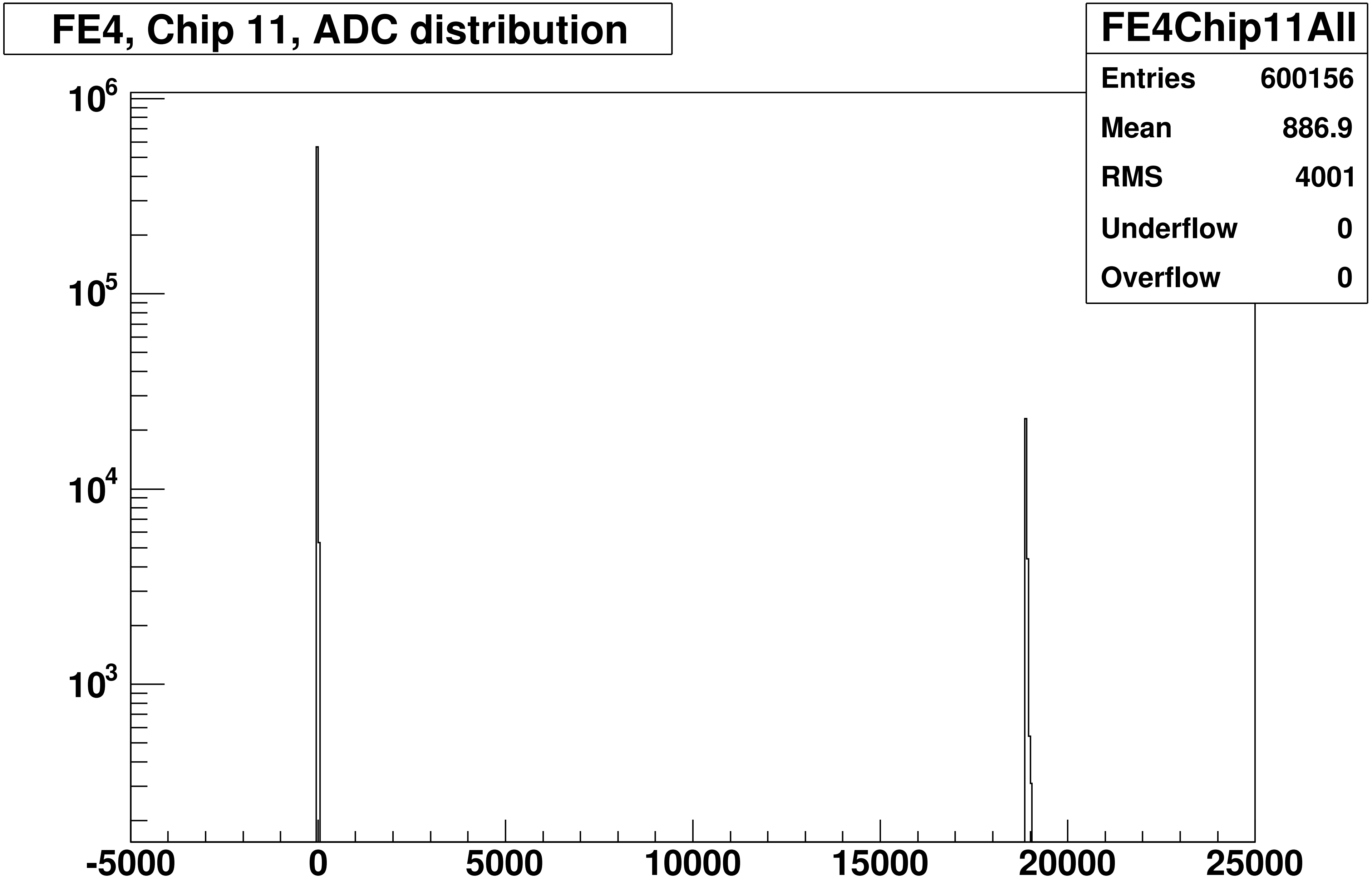
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE4, Chip 11, ADC distribution
FE4Chip11All
Entries 600156
Mean 886.9
RMS 4001
Underflow 0
Overflow 0
10^6
10^5
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10^3
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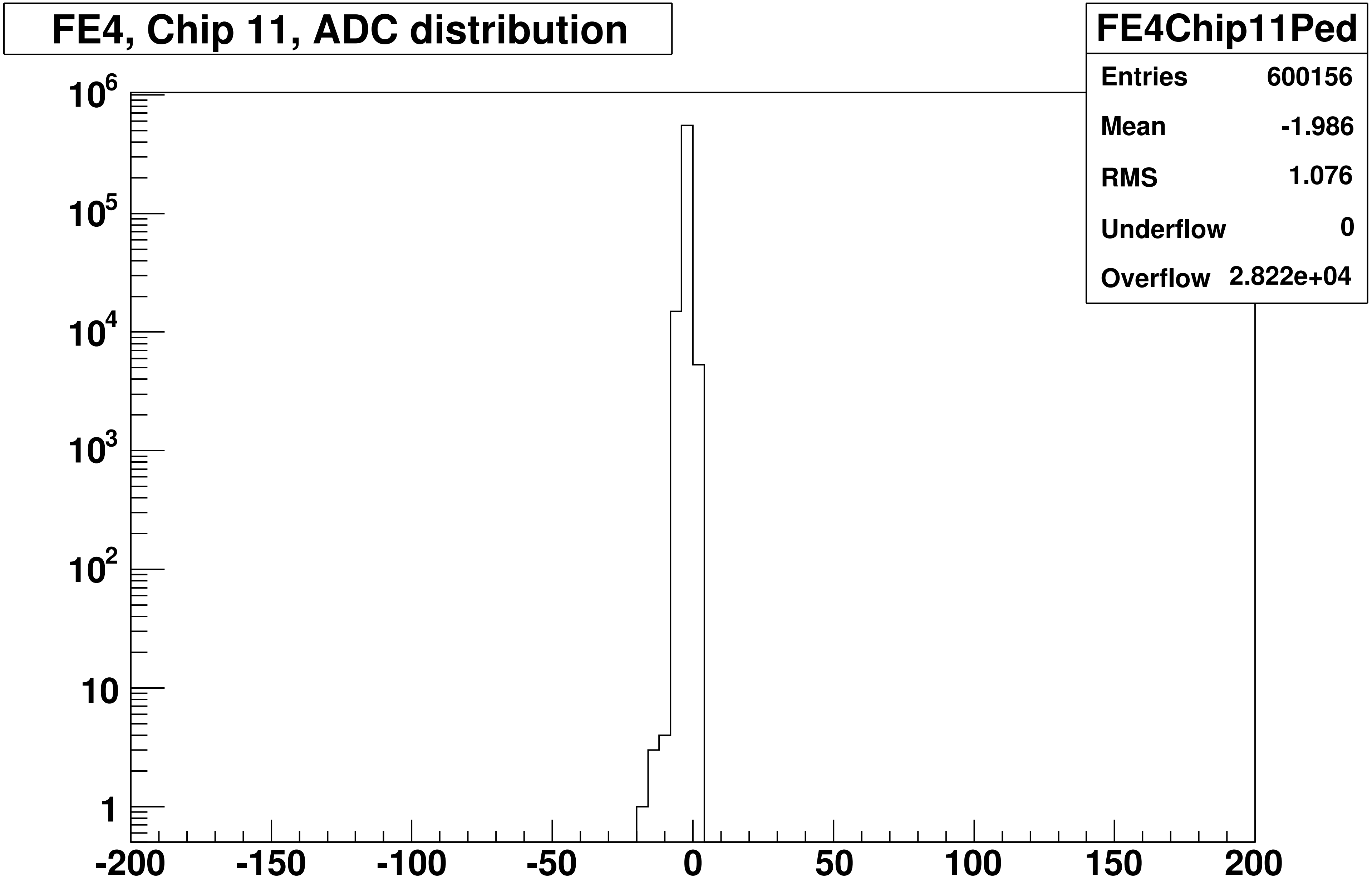
20000
25000


FE4, Chip 11, ADC distribution
FE4Chip11Ped
Entries 600156
Mean -1.986
RMS 1.076
Underflow 0
Overflow 2.822e+04
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10^3
10^2
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100
150
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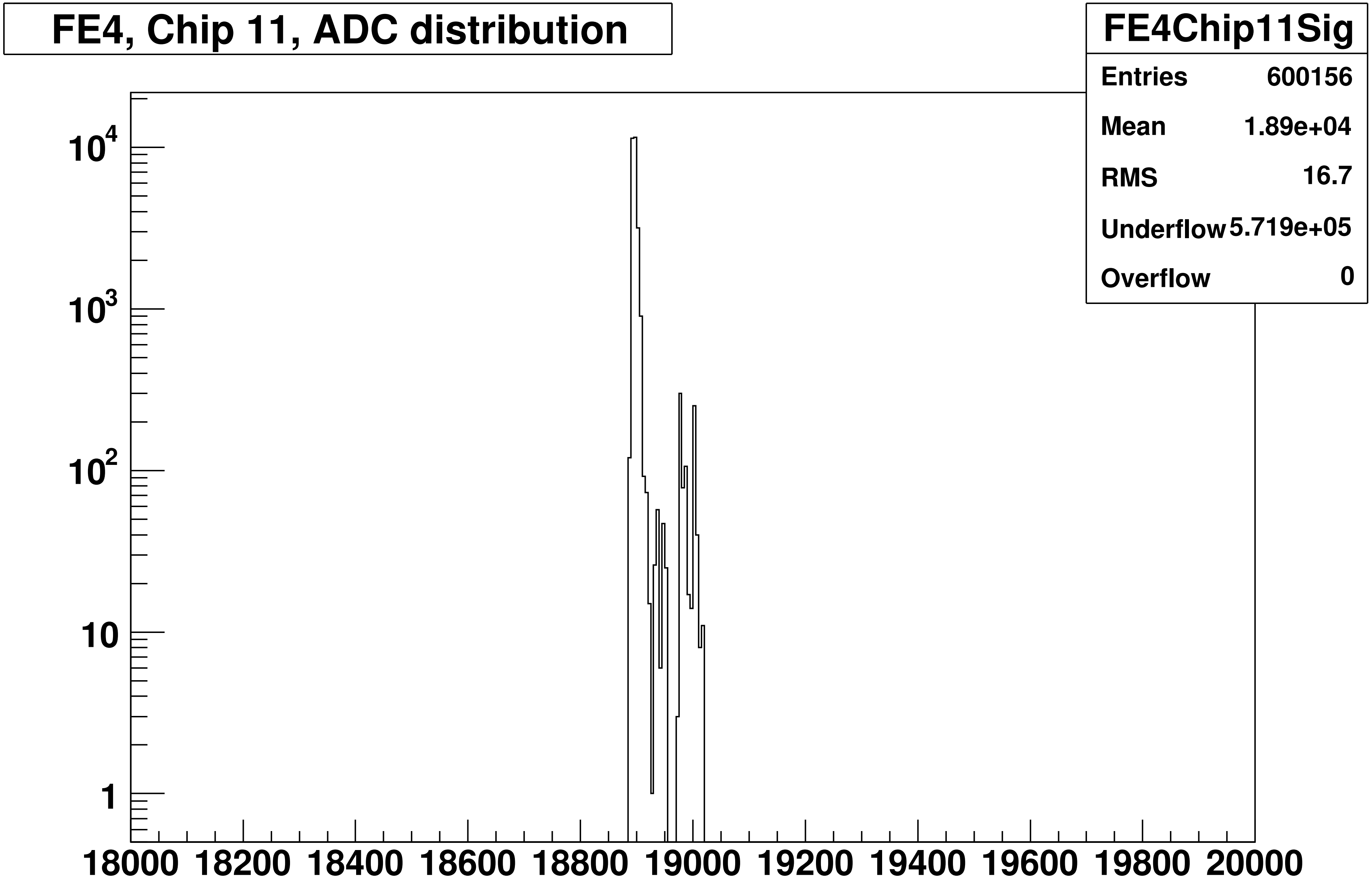
FE4, Chip 11, ADC distribution
FE4Chip11Sig
Entries 600156
Mean 1.89e+04
RMS 16.7
Underflow 5.719e+05
Overflow 0
10^4
10^3
10^2
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18000
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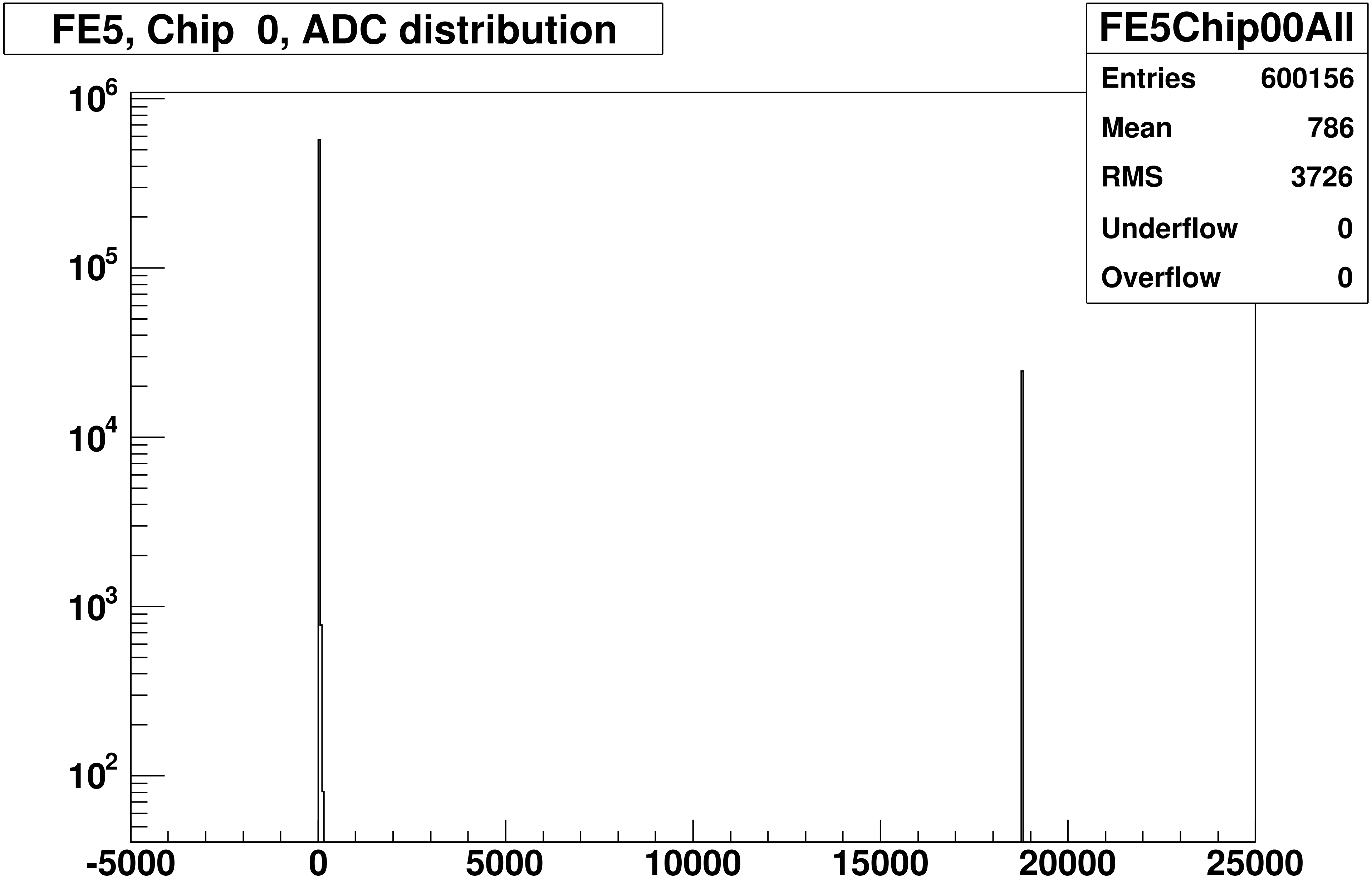

FE5, Chip 0, ADC distribution
FE5Chip00All
Entries 600156
Mean 786
RMS 3726
Underflow 0
Overflow 0
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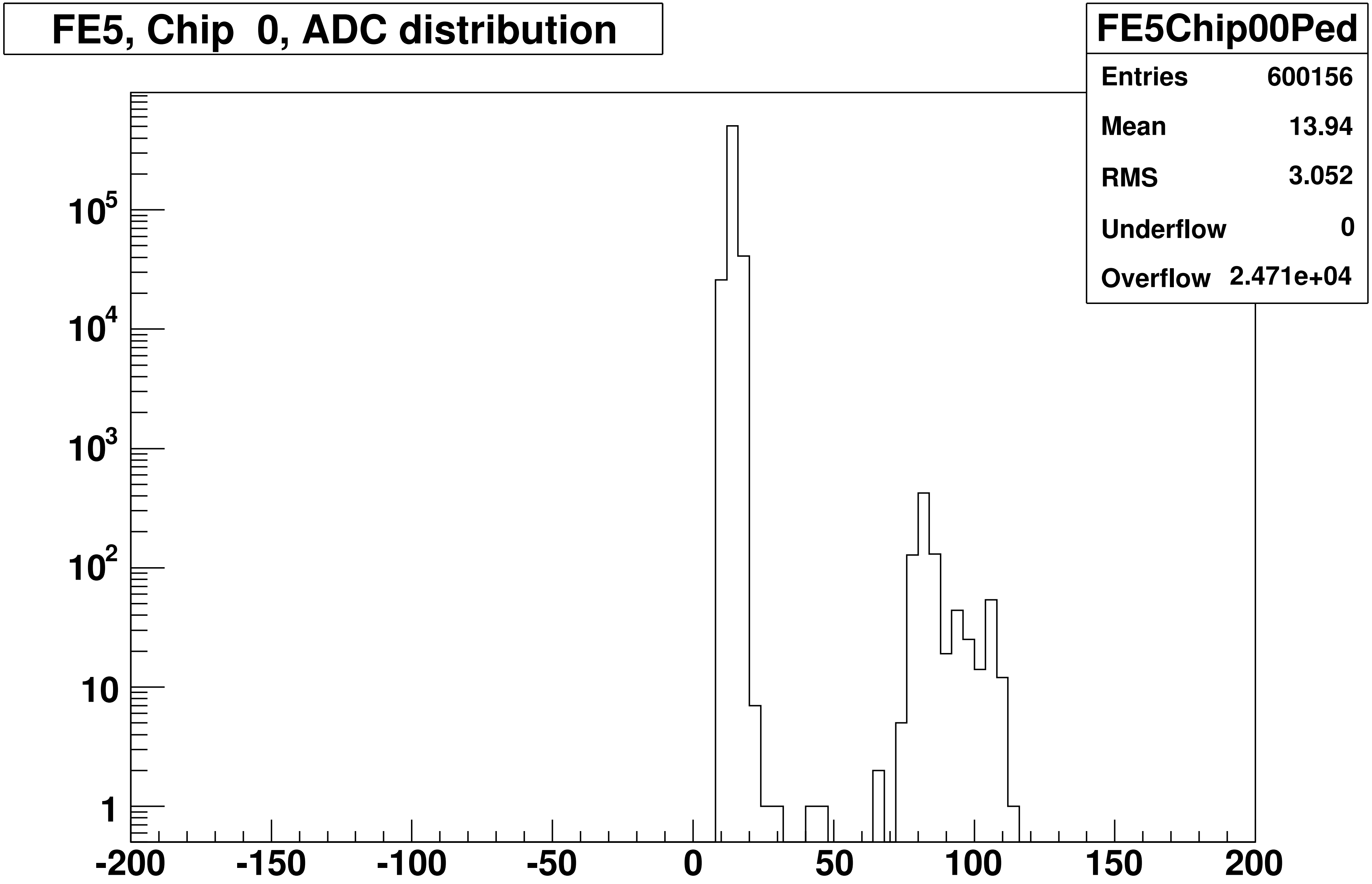

FE5, Chip 0, ADC distribution
FE5Chip00Ped
Entries 600156
Mean 13.94
RMS 3.052
Underflow 0
Overflow 2.471e+04
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10^3
10^2
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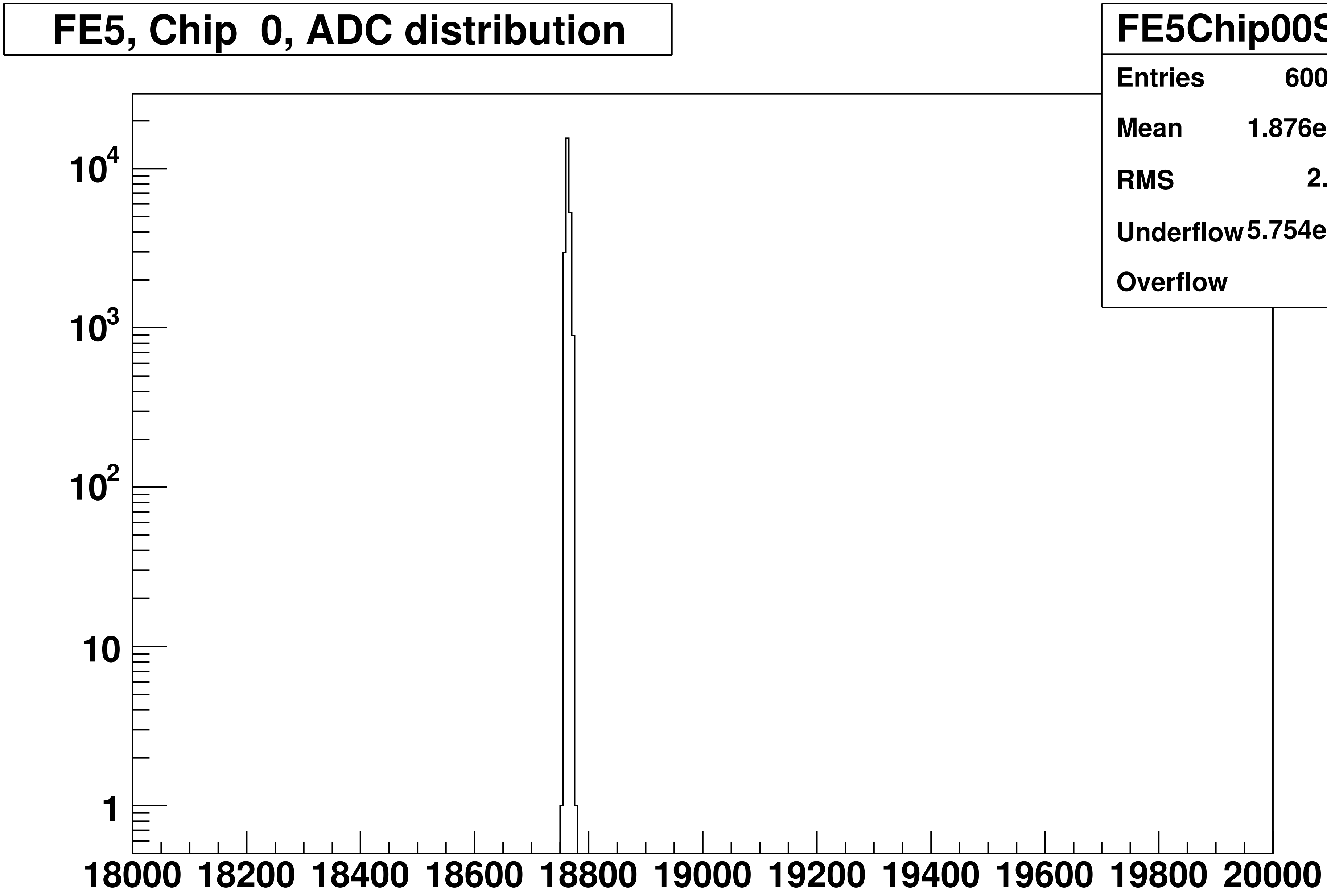

FE5, Chip 0, ADC distribution
FE5Chip00Sig
Entries 600156
Mean 1.876e+04
RMS 2.985
Underflow 5.754e+05
Overflow 0
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10^3
10^2
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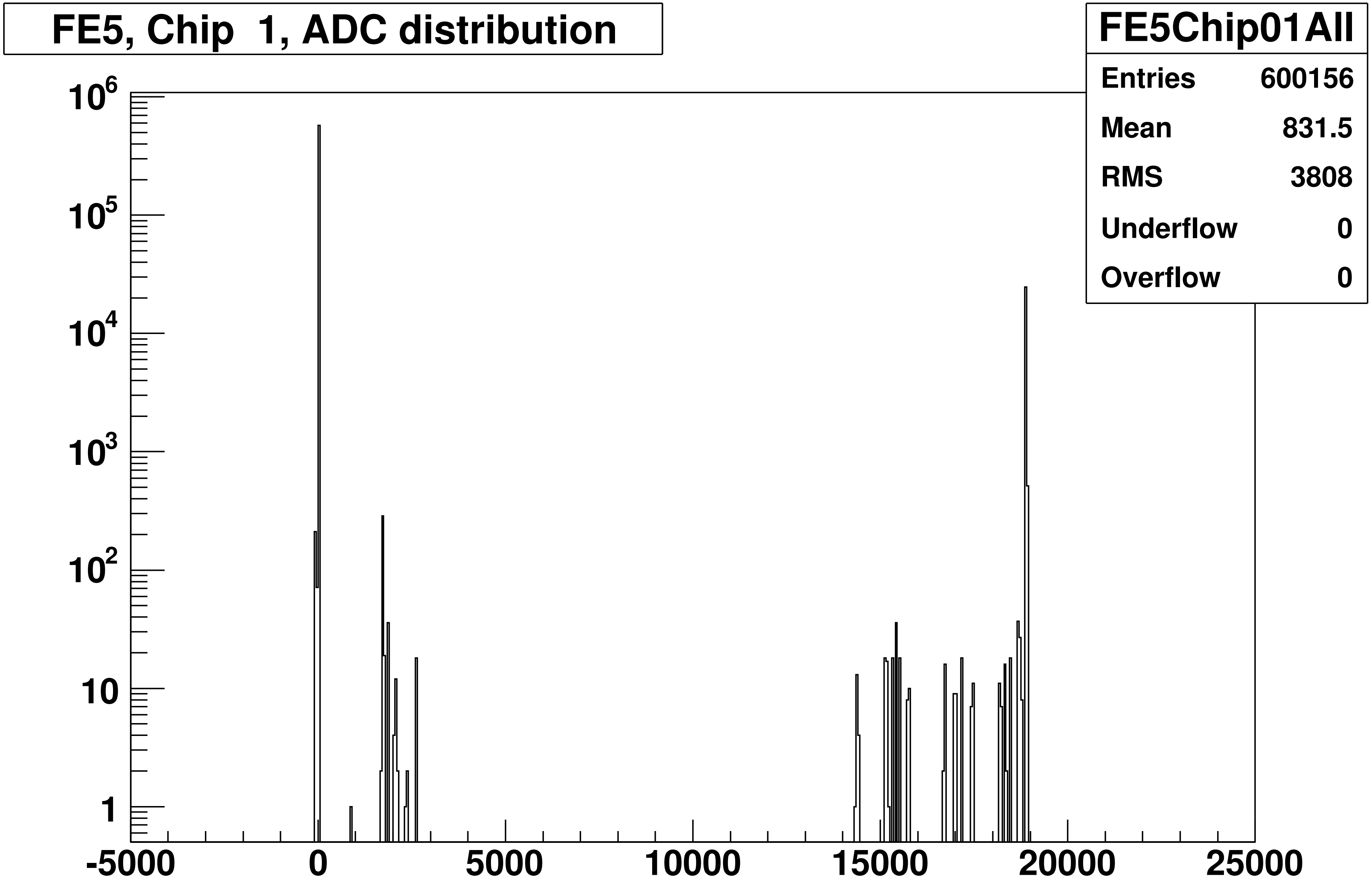
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE5, Chip 1, ADC distribution
FE5Chip01All
Entries 600156
Mean 831.5
RMS 3808
Underflow 0
Overflow 0
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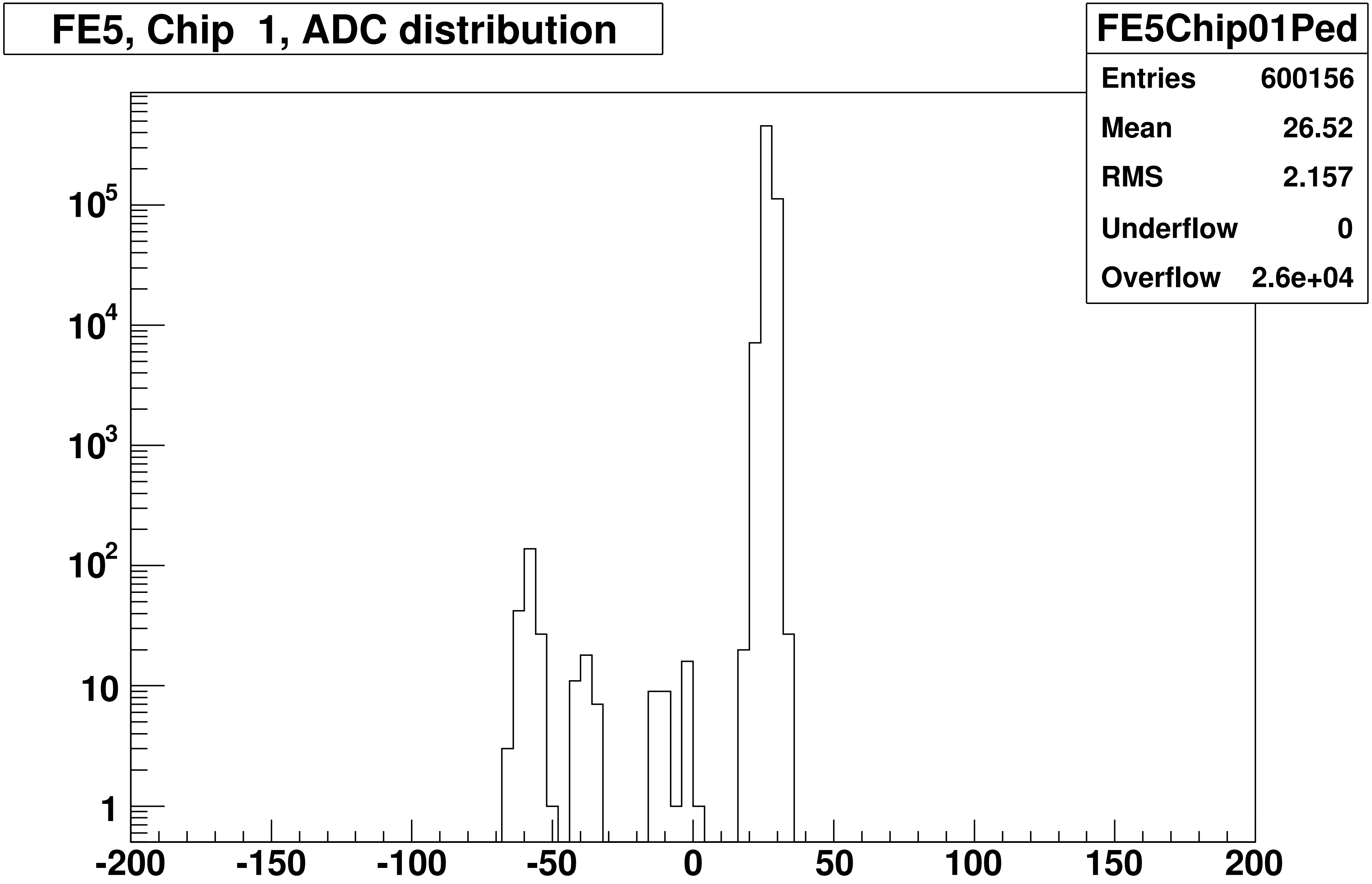
FE5, Chip 1, ADC distribution
FE5Chip01Ped
Entries 600156
Mean 26.52
RMS 2.157
Underflow 0
Overflow 2.6e+04
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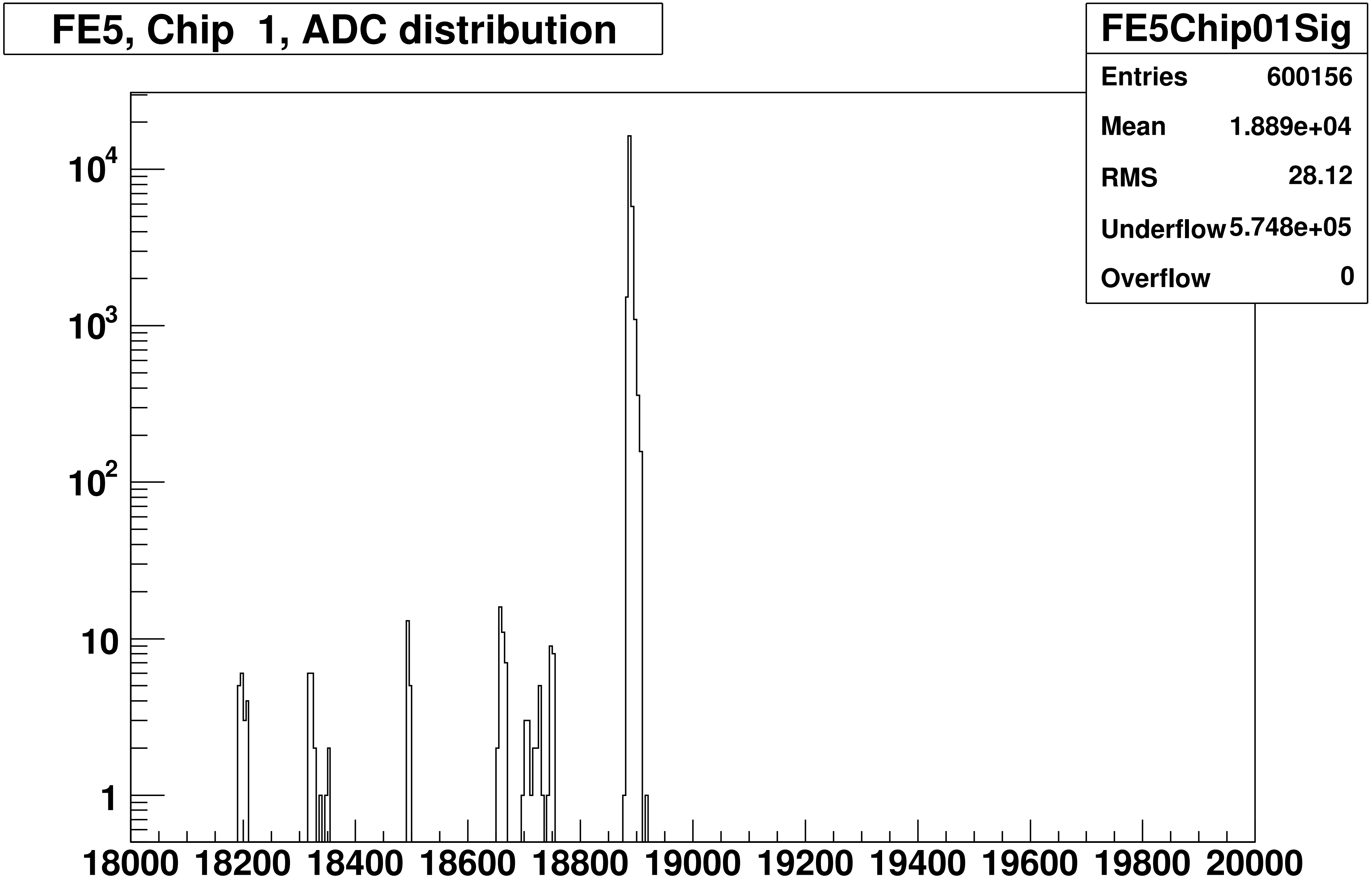
FE5, Chip 1, ADC distribution
FE5Chip01Sig
Entries 600156
Mean 1.889e+04
RMS 28.12
Underflow 5.748e+05
Overflow 0
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10^3
10^2
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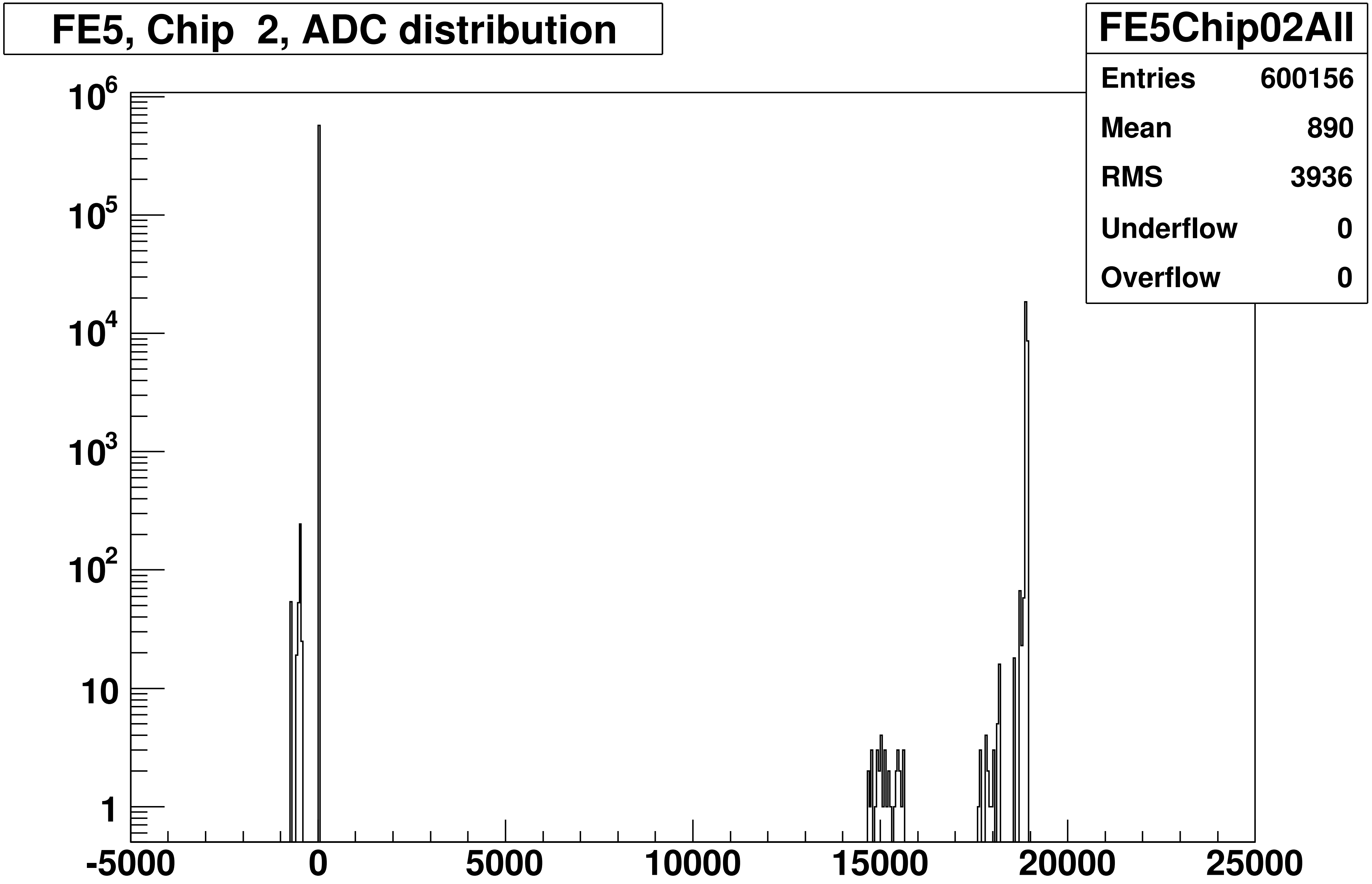
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE5, Chip 2, ADC distribution
FE5Chip02All
Entries 600156
Mean 890
RMS 3936
Underflow 0
Overflow 0
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10^3
10^2
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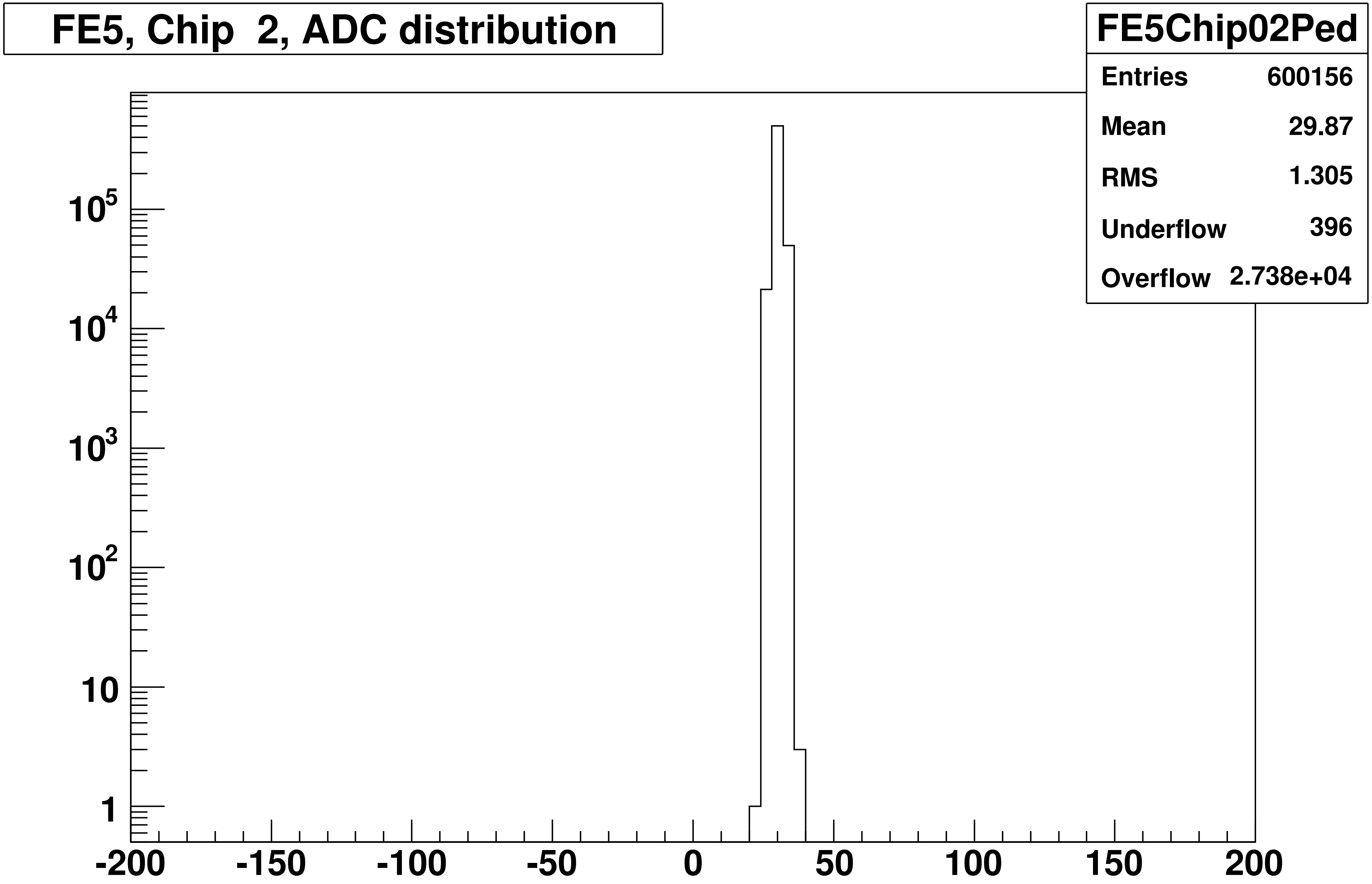
FE5, Chip 2, ADC distribution
FE5Chip02Ped
Entries 600156
Mean 29.87
RMS 1.305
Underflow 396
Overflow 2.738e+04
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10^3
10^2
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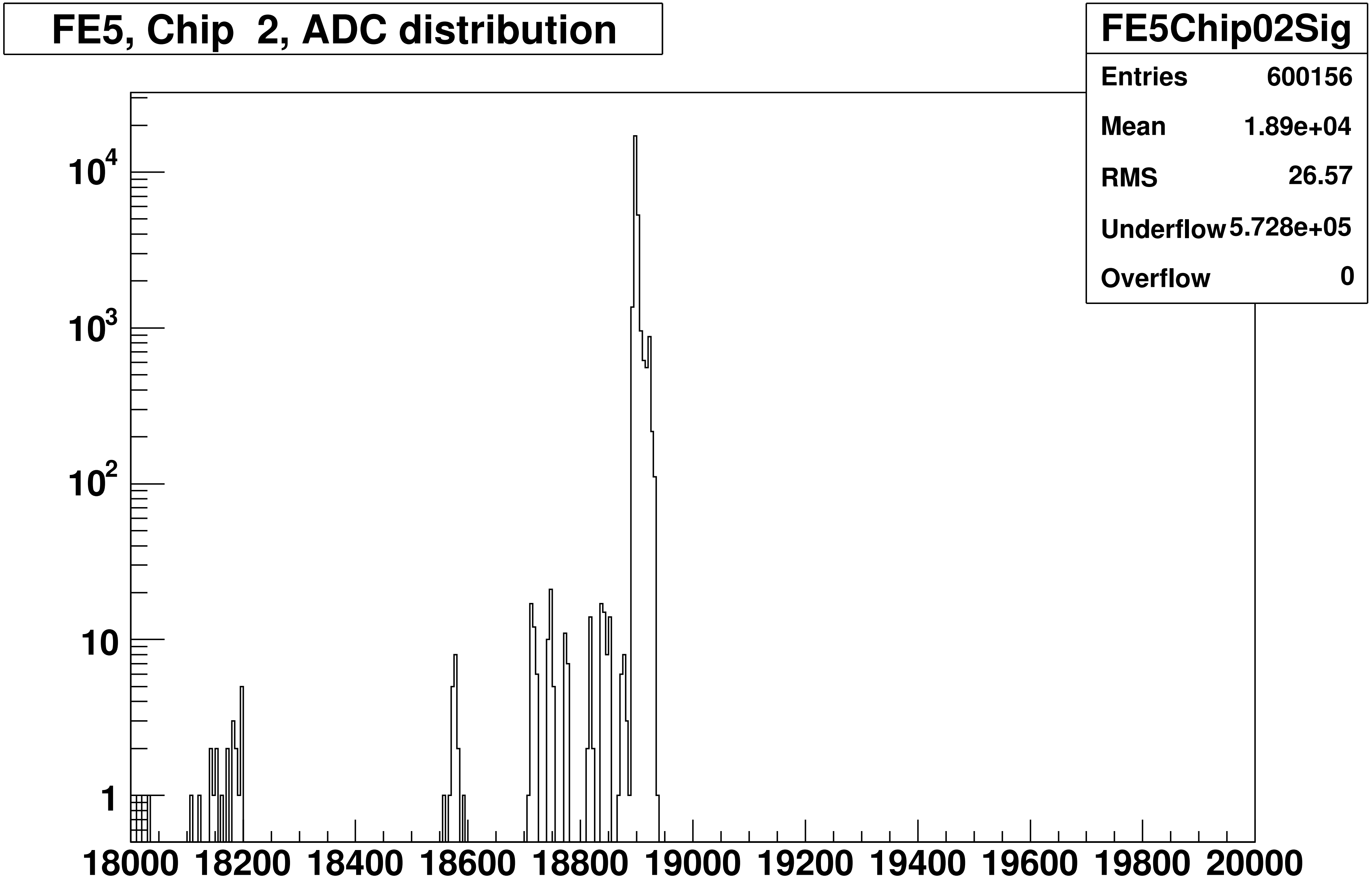

FE5, Chip 2, ADC distribution
FE5Chip02Sig
Entries 600156
Mean 1.89e+04
RMS 26.57
Underflow 5.728e+05
Overflow 0
10^4
10^3
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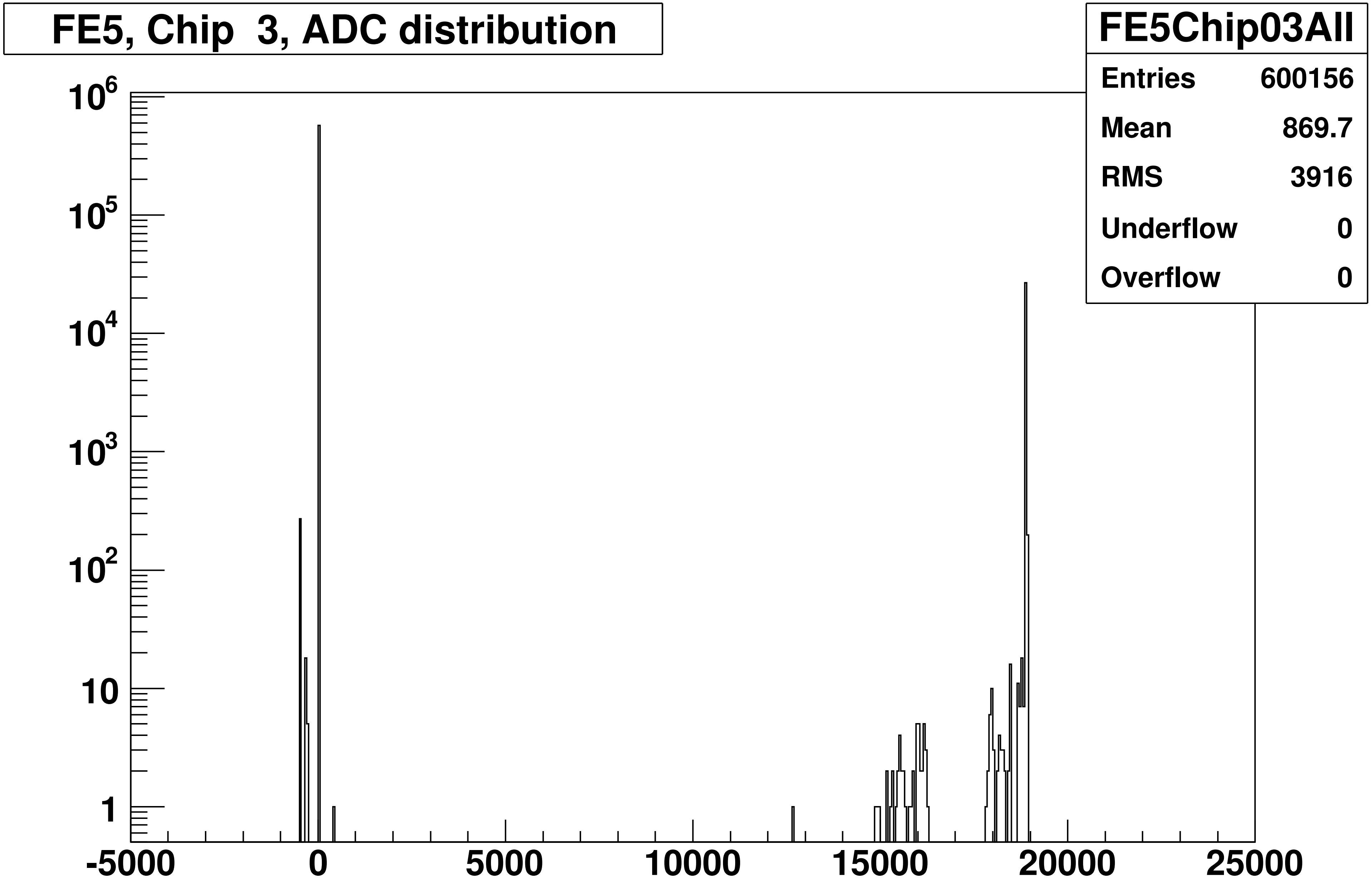
20000



FE5, Chip 3, ADC distribution
FE5Chip03All
Entries 600156
Mean 869.7
RMS 3916
Underflow 0
Overflow 0
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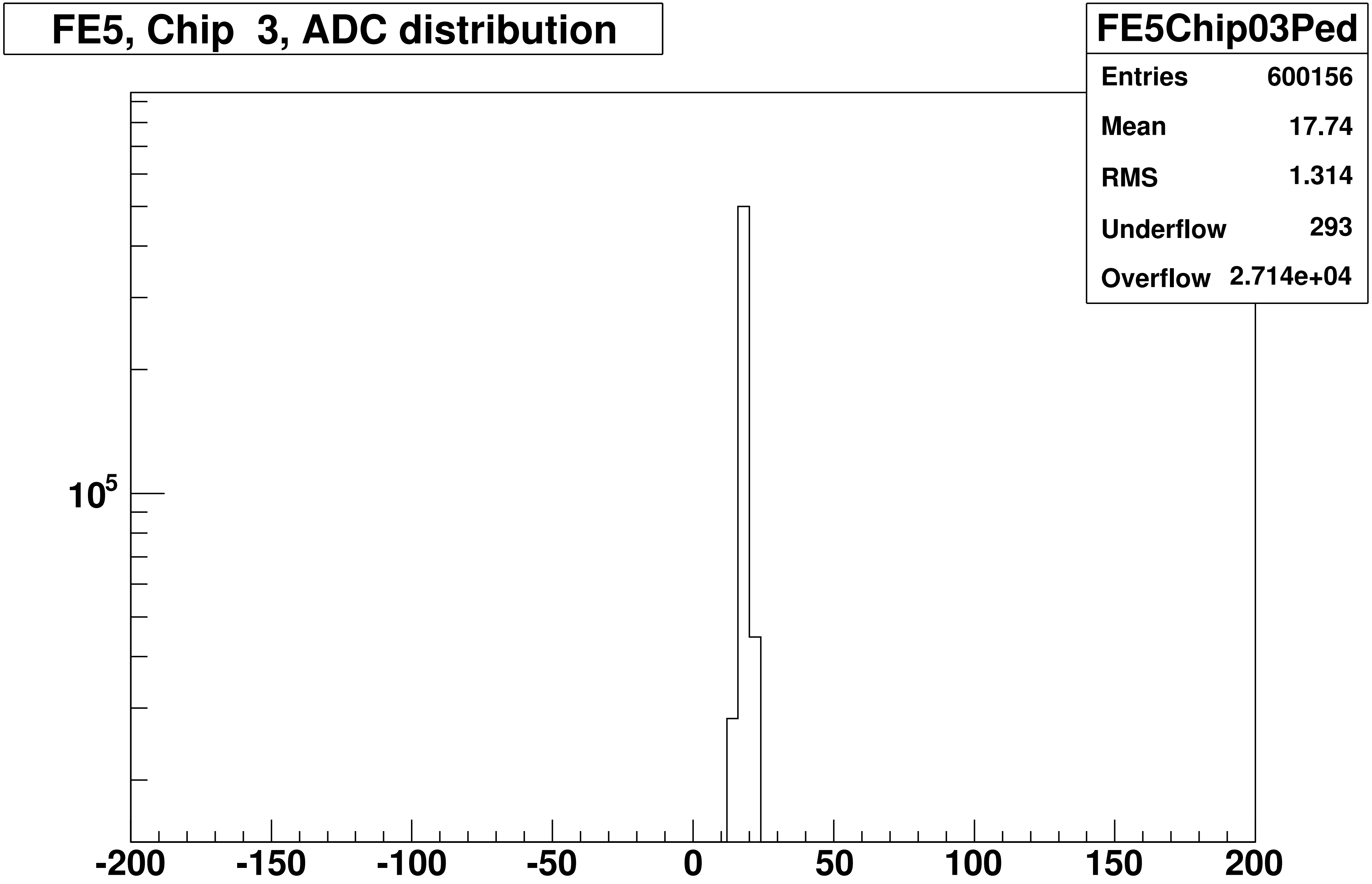
FE5, Chip 3, ADC distribution
FE5Chip03Ped
Entries 600156
Mean 17.74
RMS 1.314
Underflow 293
Overflow 2.714e+04
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150
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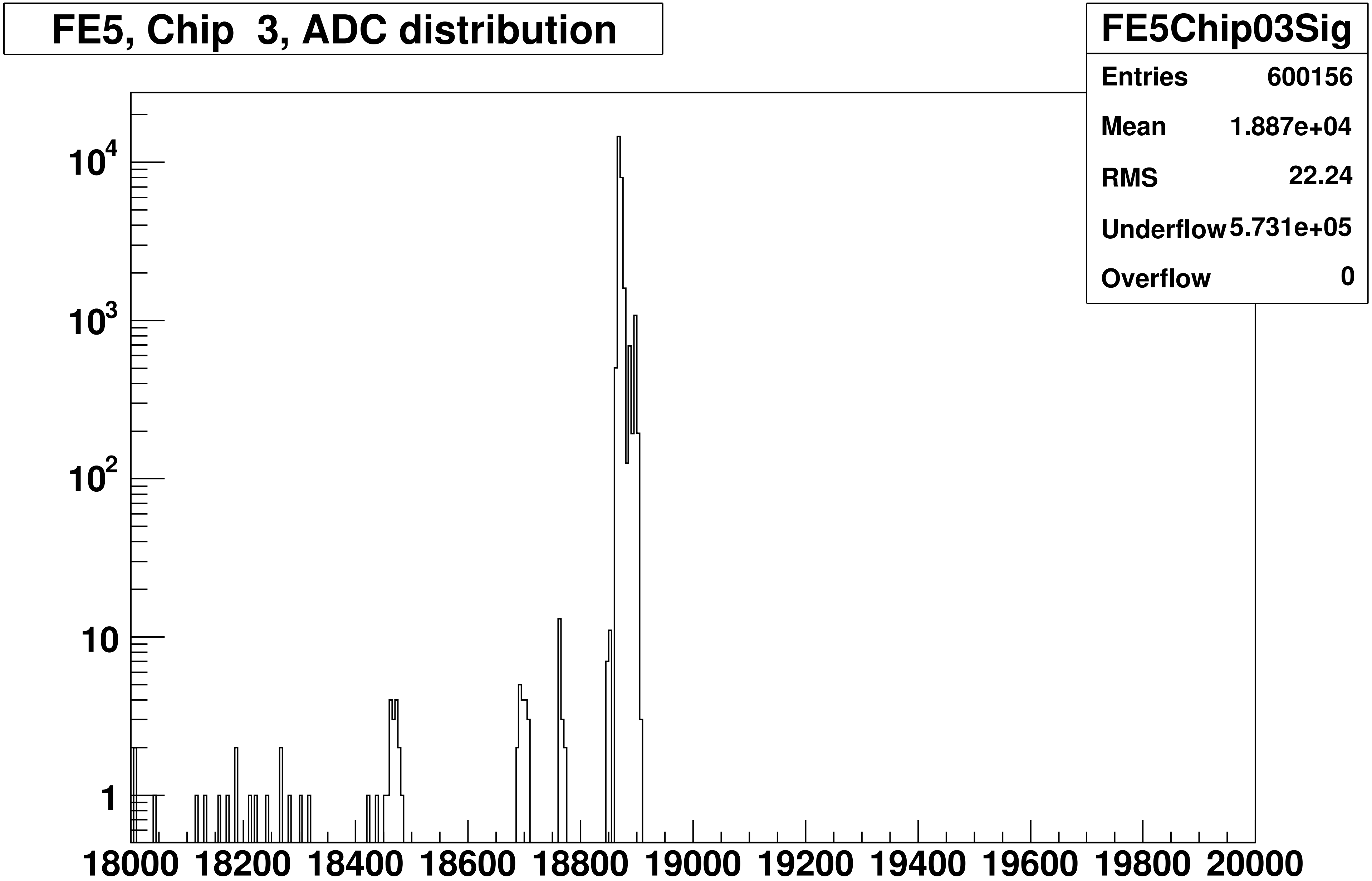

FE5, Chip 3, ADC distribution
FE5Chip03Sig
Entries 600156
Mean 1.887e+04
RMS 22.24
Underflow 5.731e+05
Overflow 0
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10^3
10^2
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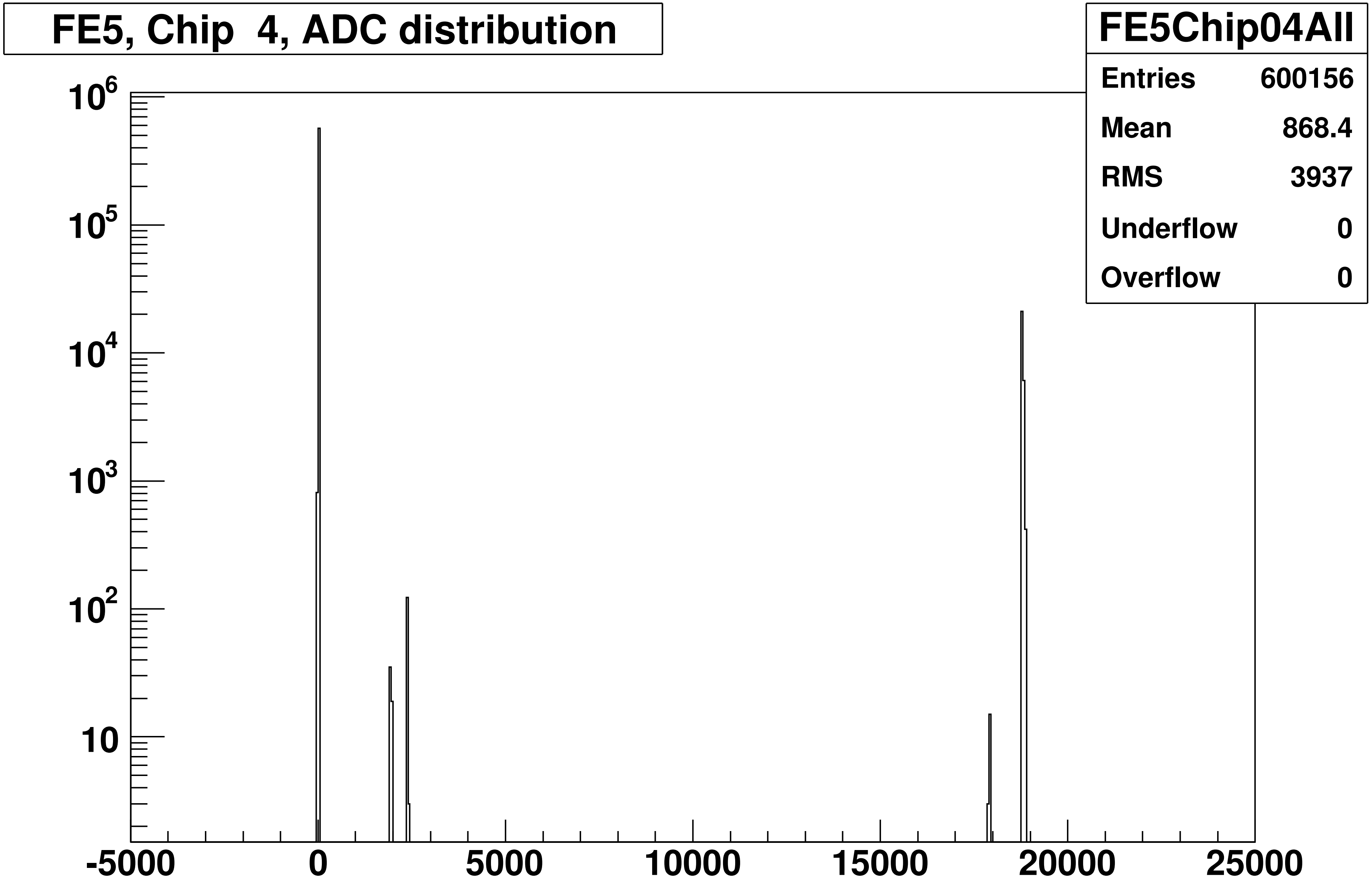
FE5, Chip 4, ADC distribution
FE5Chip04All
Entries 600156
Mean 868.4
RMS 3937
Underflow 0
Overflow 0
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10^4
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10^2
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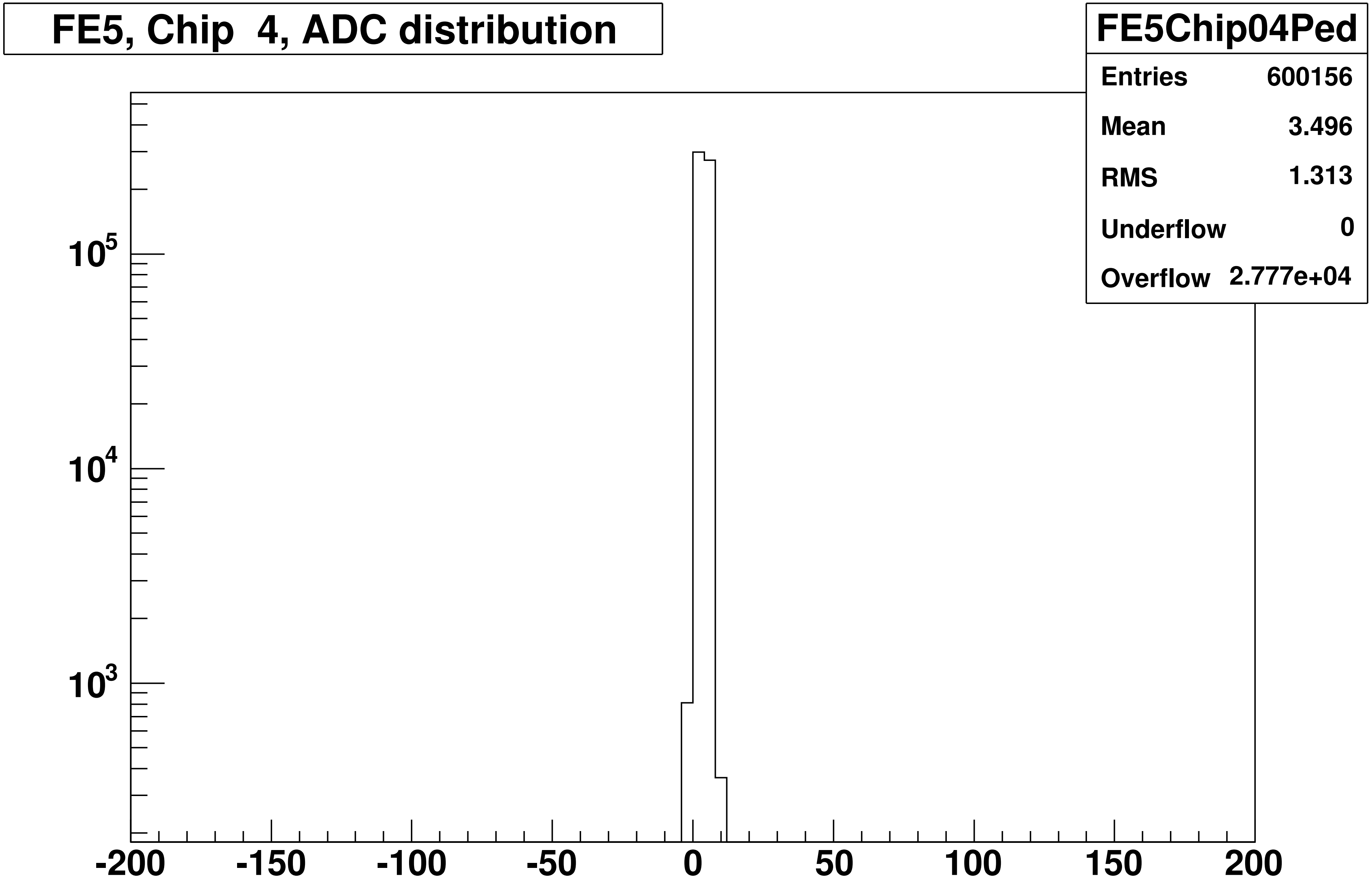

FE5, Chip 4, ADC distribution
FE5Chip04Ped
Entries 600156
Mean 3.496
RMS 1.313
Underflow 0
Overflow 2.777e+04
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10^3
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150
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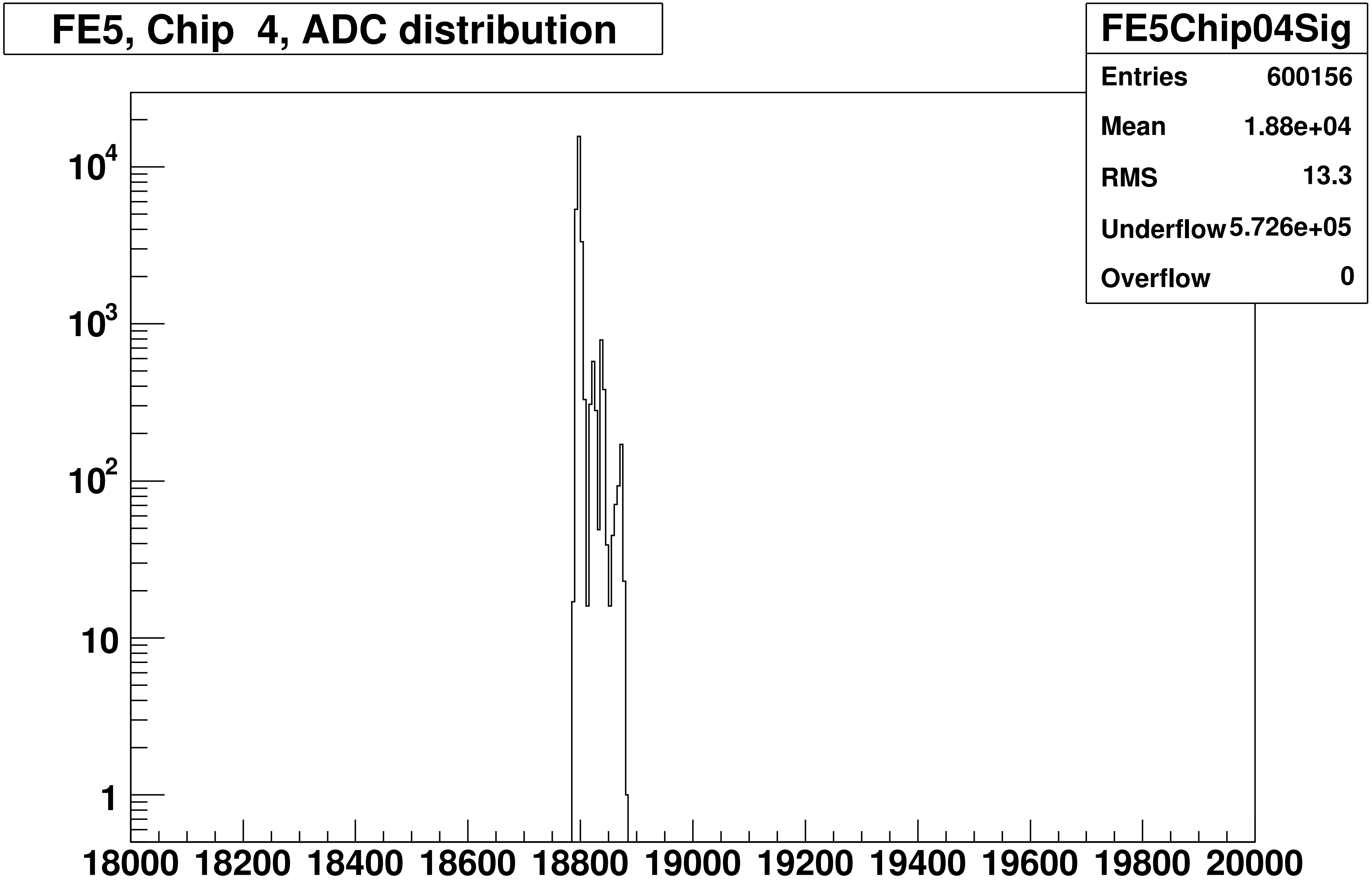

FE5, Chip 4, ADC distribution
FE5Chip04Sig
Entries 600156
Mean 1.88e+04
RMS 13.3
Underflow 5.726e+05
Overflow 0
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10^3
10^2
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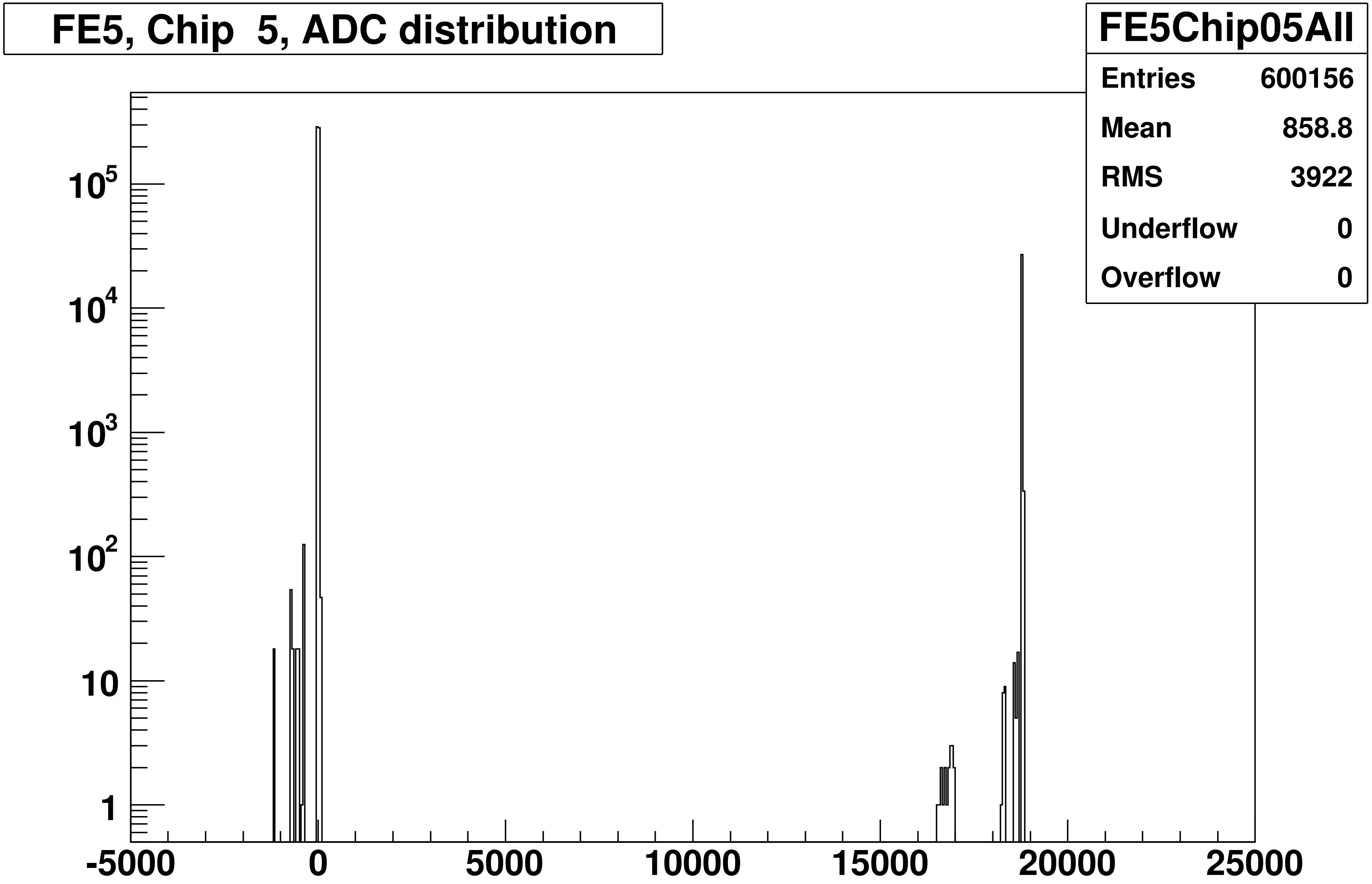

FE5, Chip 5, ADC distribution
FE5Chip05All
Entries 600156
Mean 858.8
RMS 3922
Underflow 0
Overflow 0
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10^3
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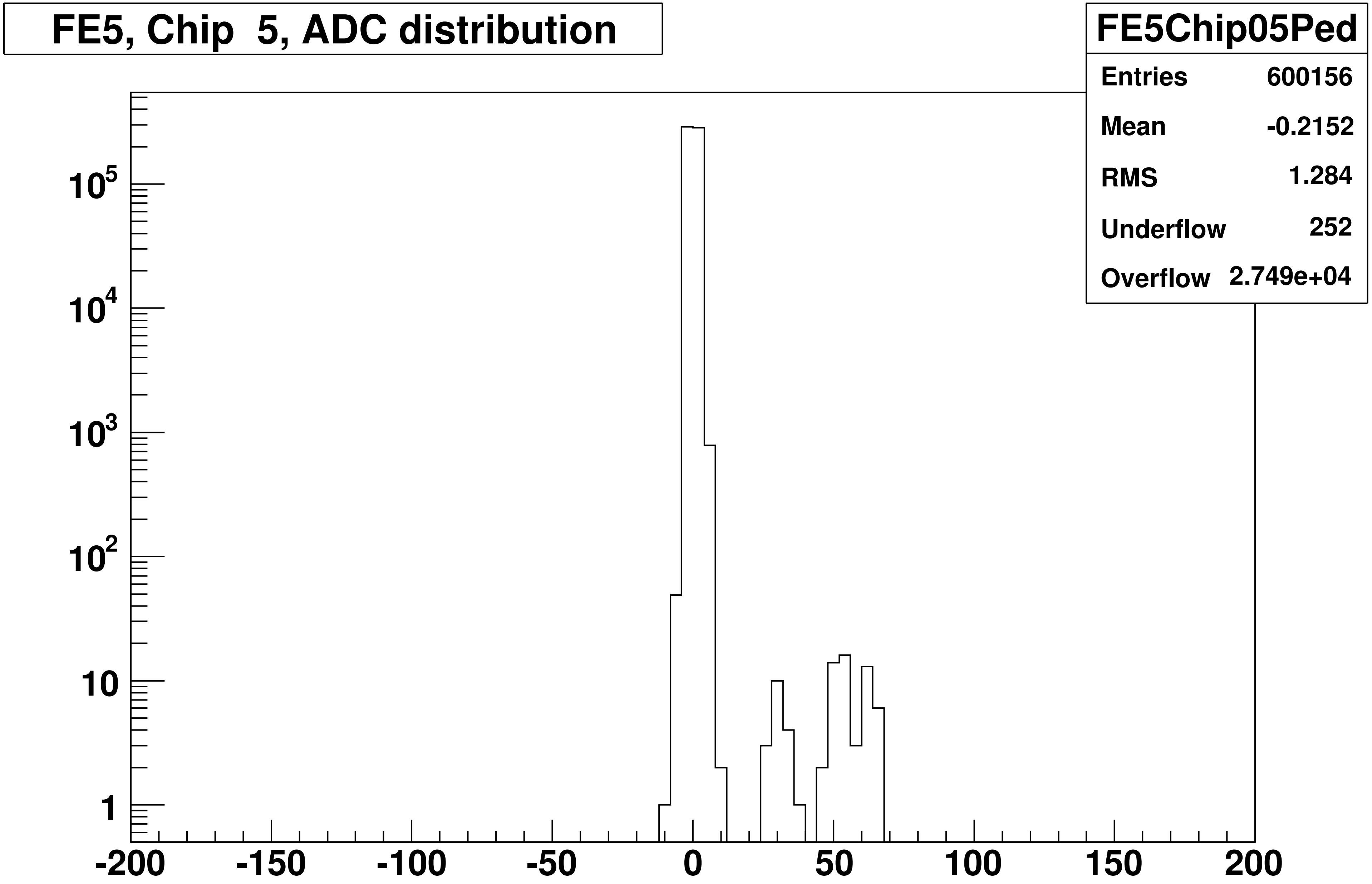

FE5, Chip 5, ADC distribution
FE5Chip05Ped
Entries 600156
Mean -0.2152
RMS 1.284
Underflow 252
Overflow 2.749e+04
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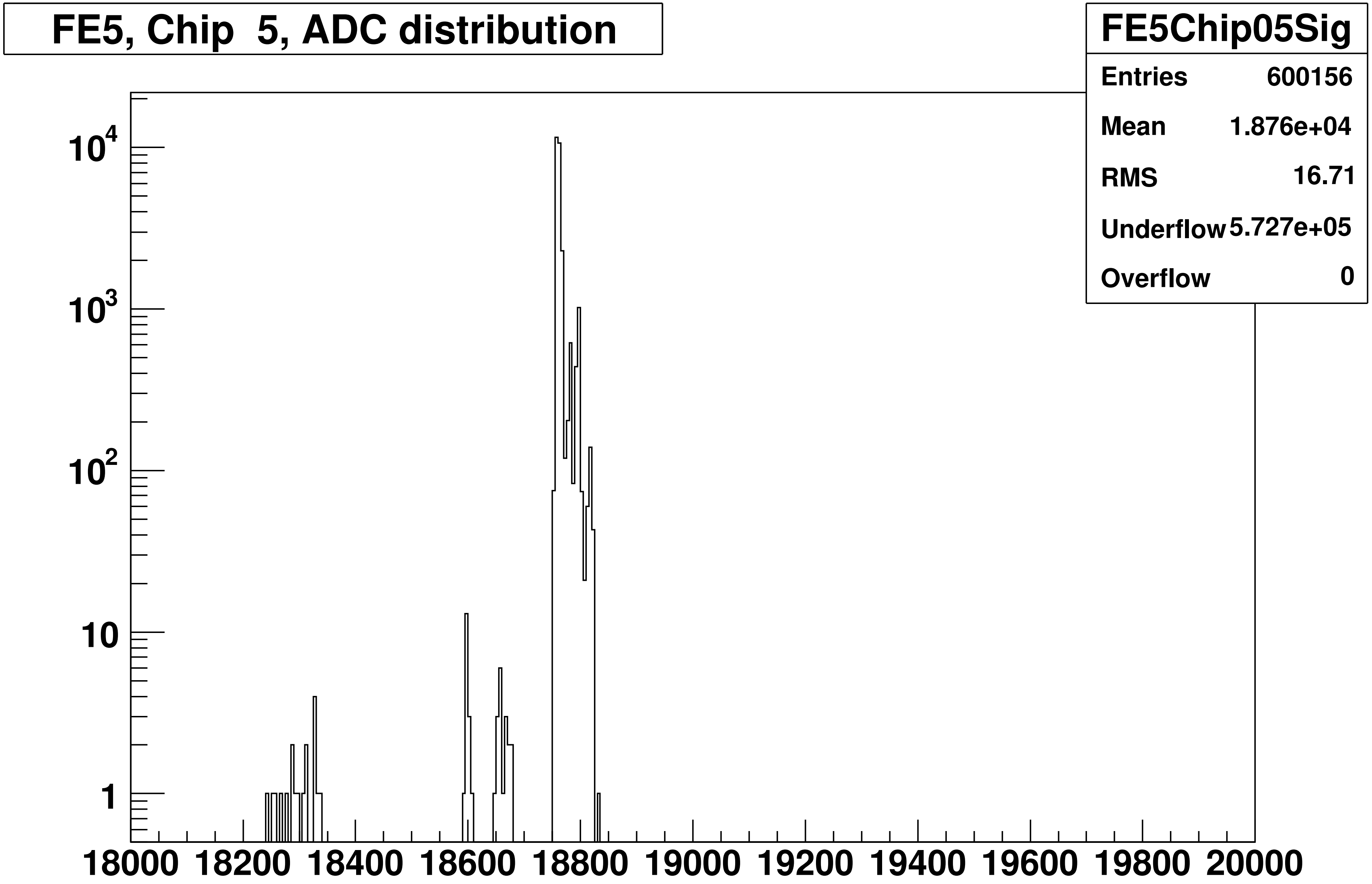
FE5, Chip 5, ADC distribution
FE5Chip05Sig
Entries 600156
Mean 1.876e+04
RMS 16.71
Underflow 5.727e+05
Overflow 0
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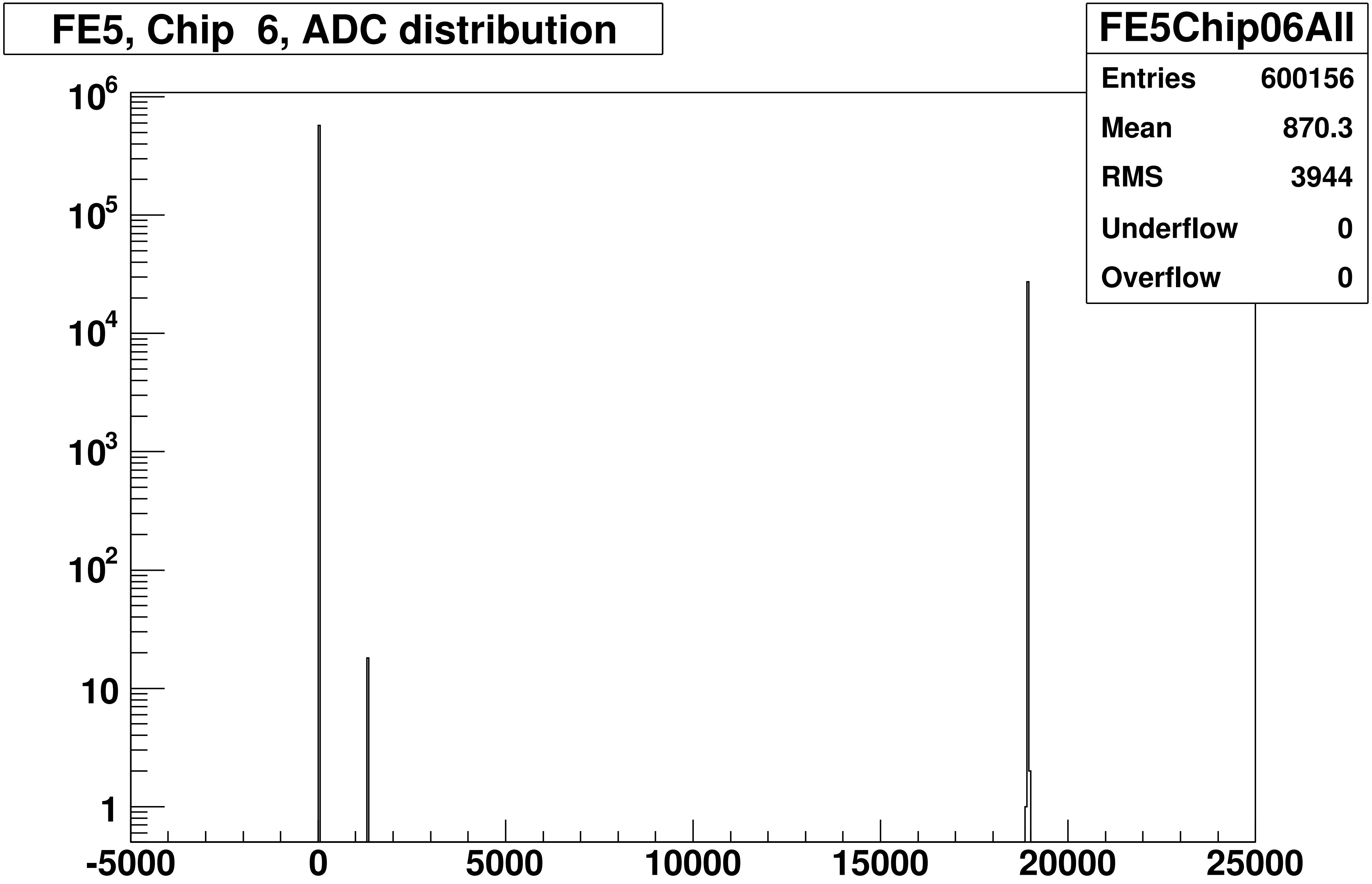

FE5, Chip 6, ADC distribution
FE5Chip06All
Entries 600156
Mean 870.3
RMS 3944
Underflow 0
Overflow 0
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10^4
10^3
10^2
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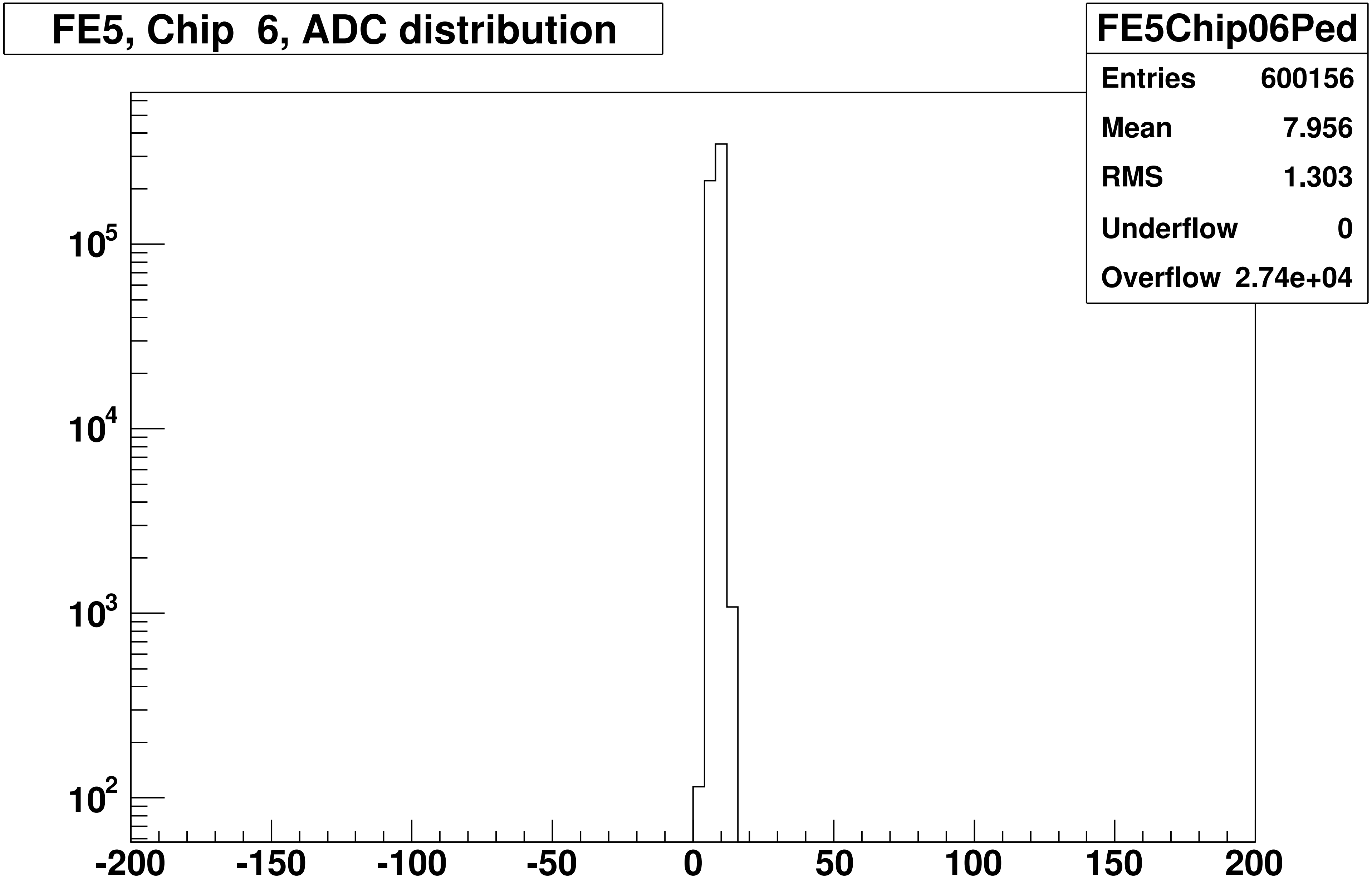
FE5, Chip 6, ADC distribution
FE5Chip06Ped
Entries 600156
Mean 7.956
RMS 1.303
Underflow 0
Overflow 2.74e+04
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10^4
10^3
10^2
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-100
-50
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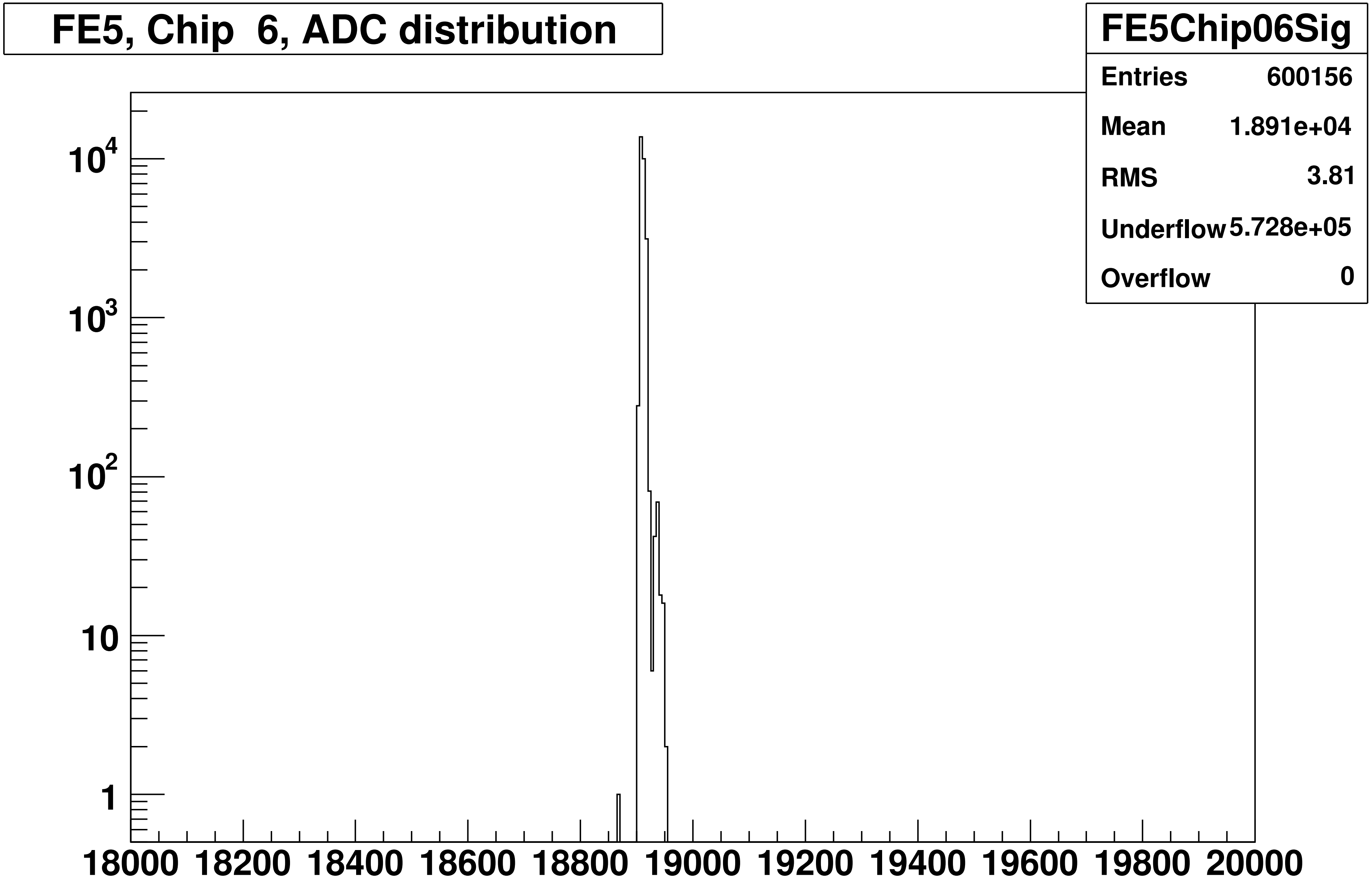
100
150
200


FE5, Chip 6, ADC distribution
FE5Chip06Sig
Entries 600156
Mean 1.891e+04
RMS 3.81
Underflow 5.728e+05
Overflow 0
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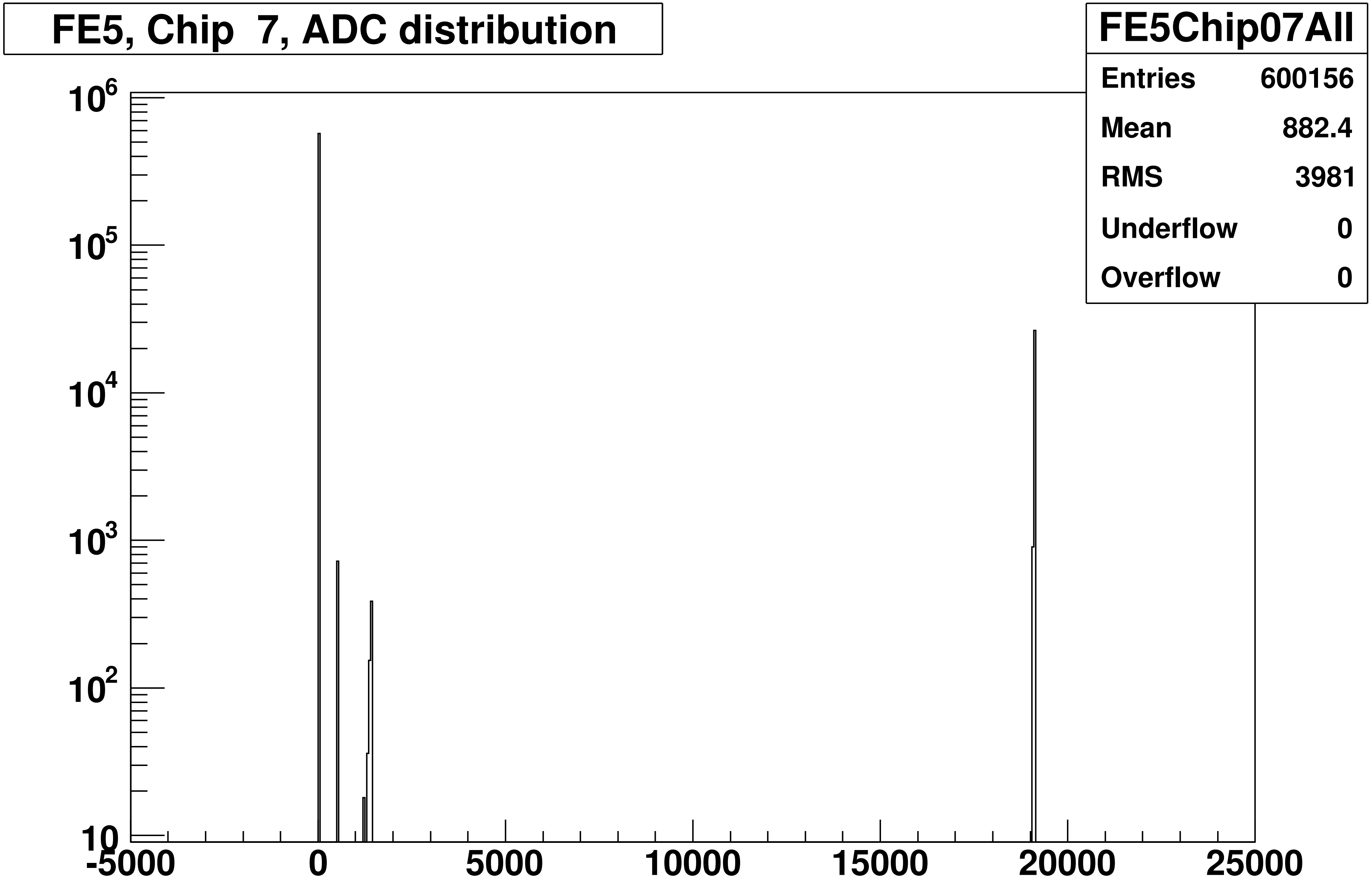
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE5, Chip 7, ADC distribution
FE5Chip07All
Entries 600156
Mean 882.4
RMS 3981
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
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10000
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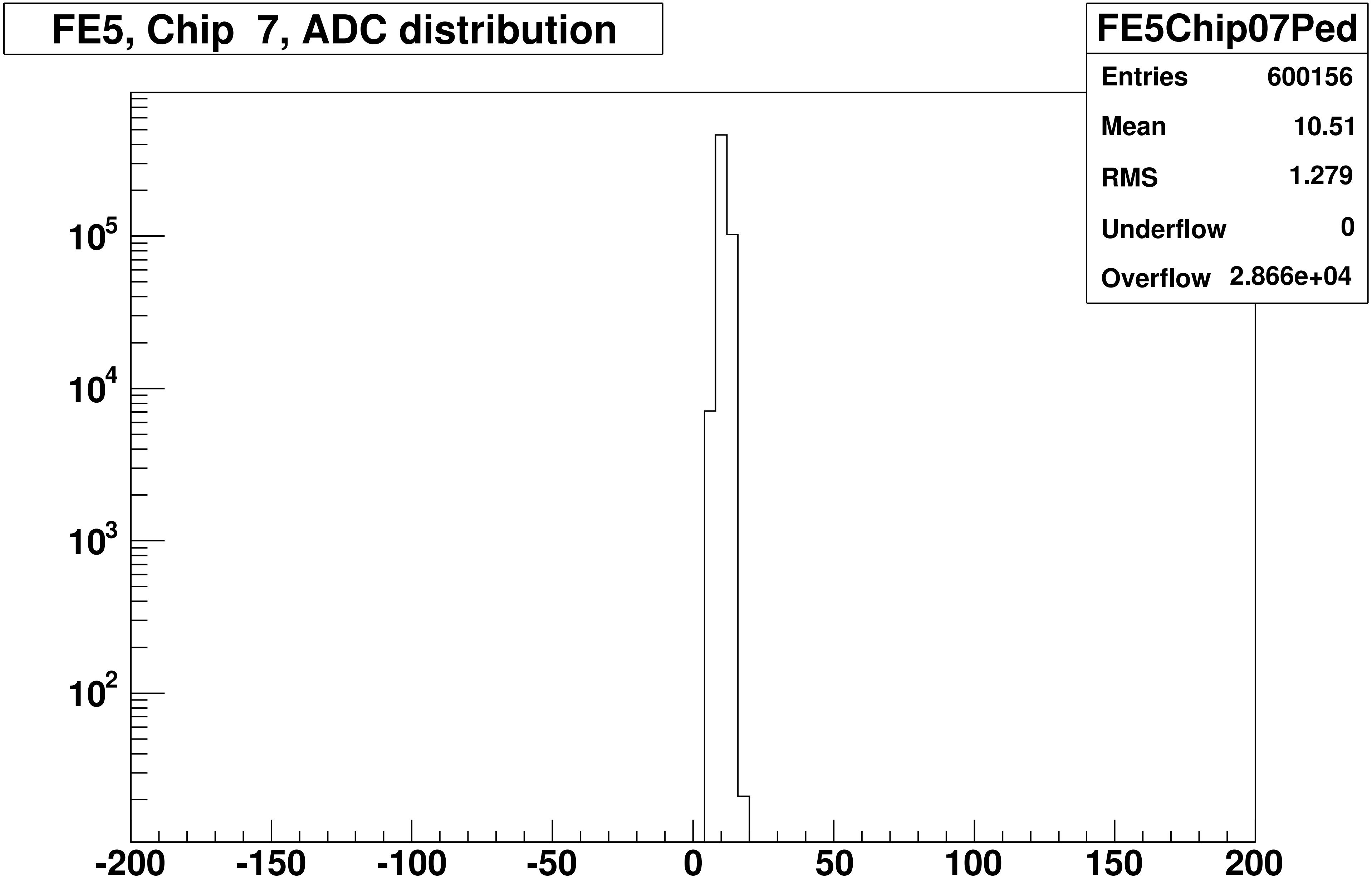
25000


FE5, Chip 7, ADC distribution
FE5Chip07Ped
Entries 600156
Mean 10.51
RMS 1.279
Underflow 0
Overflow 2.866e+04
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10^4
10^3
10^2
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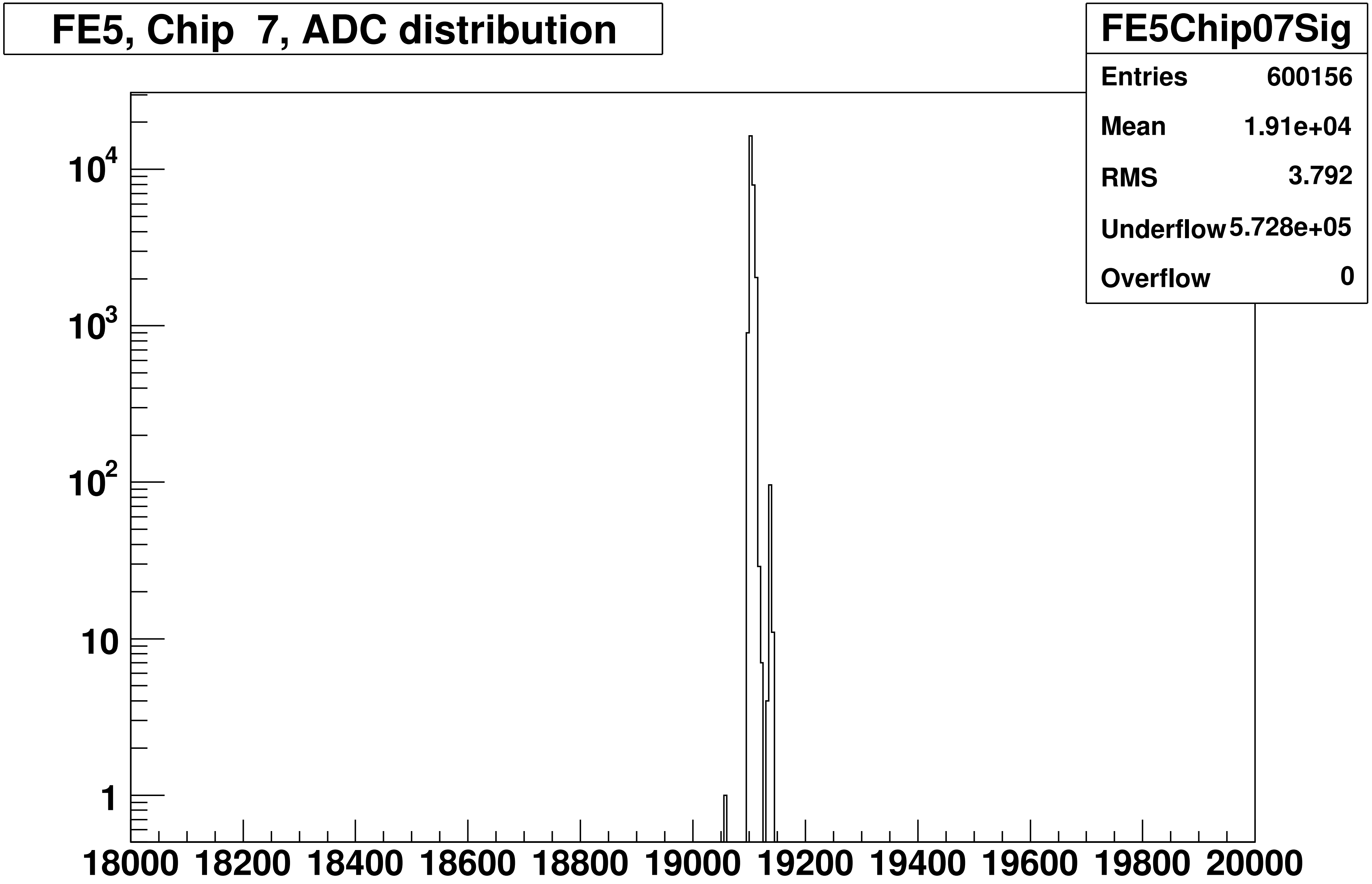

FE5, Chip 7, ADC distribution
FE5Chip07Sig
Entries 600156
Mean 1.91e+04
RMS 3.792
Underflow 5.728e+05
Overflow 0
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10^3
10^2
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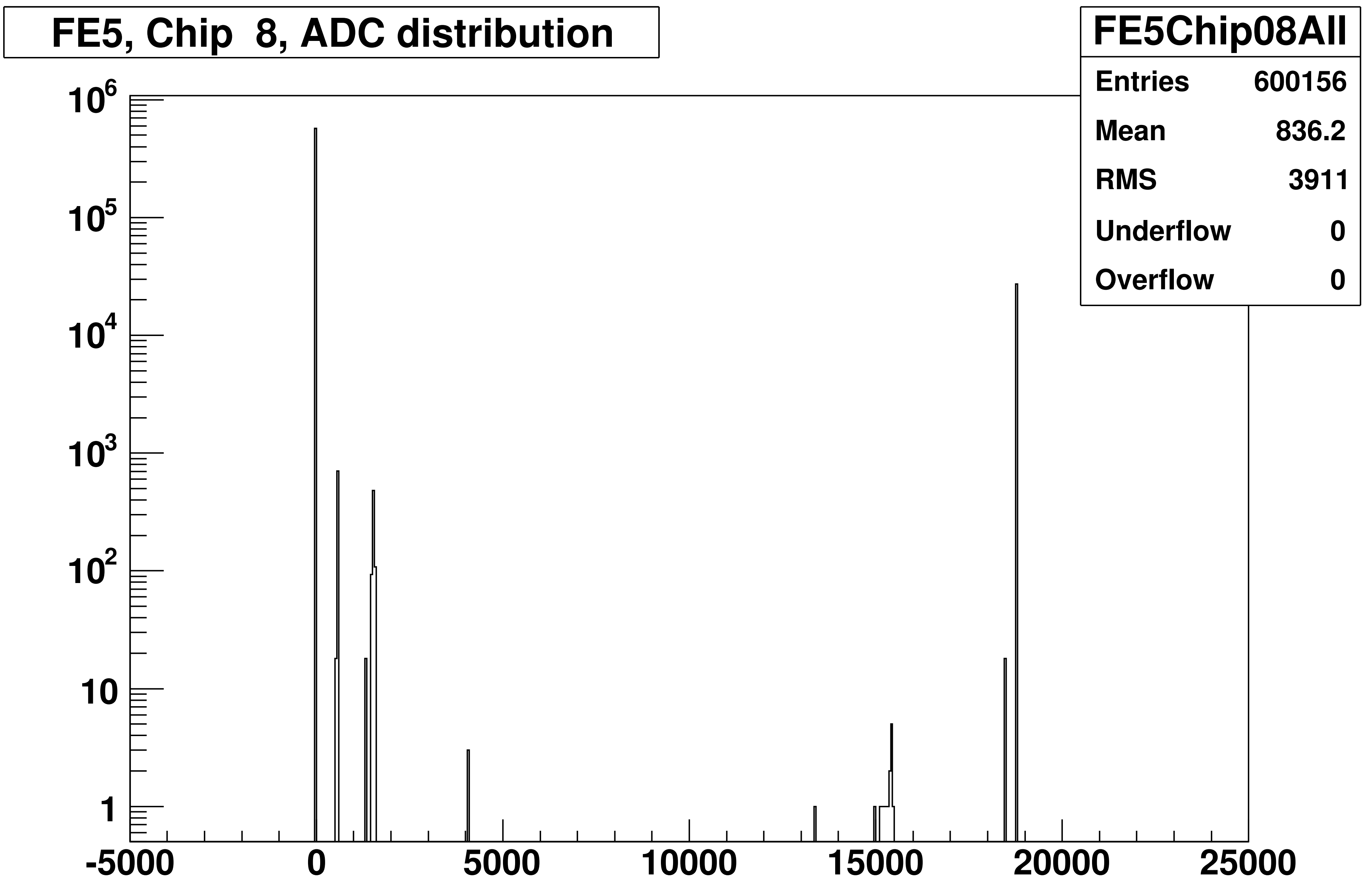
FE5, Chip 8, ADC distribution
FE5Chip08All
Entries 600156
Mean 836.2
RMS 3911
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
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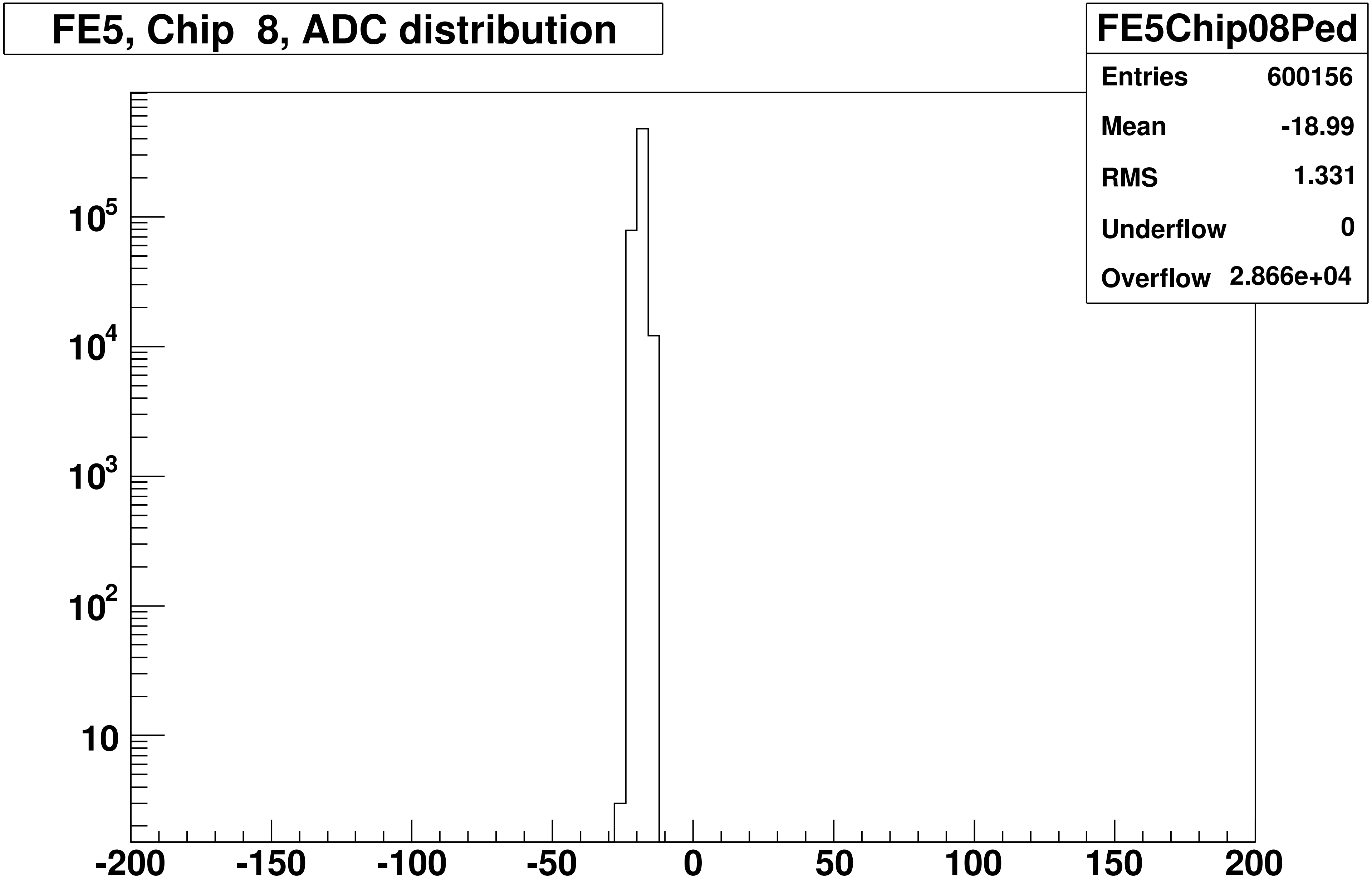

FE5, Chip 8, ADC distribution
FE5Chip08Ped
Entries 600156
Mean -18.99
RMS 1.331
Underflow 0
Overflow 2.866e+04
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10^4
10^3
10^2
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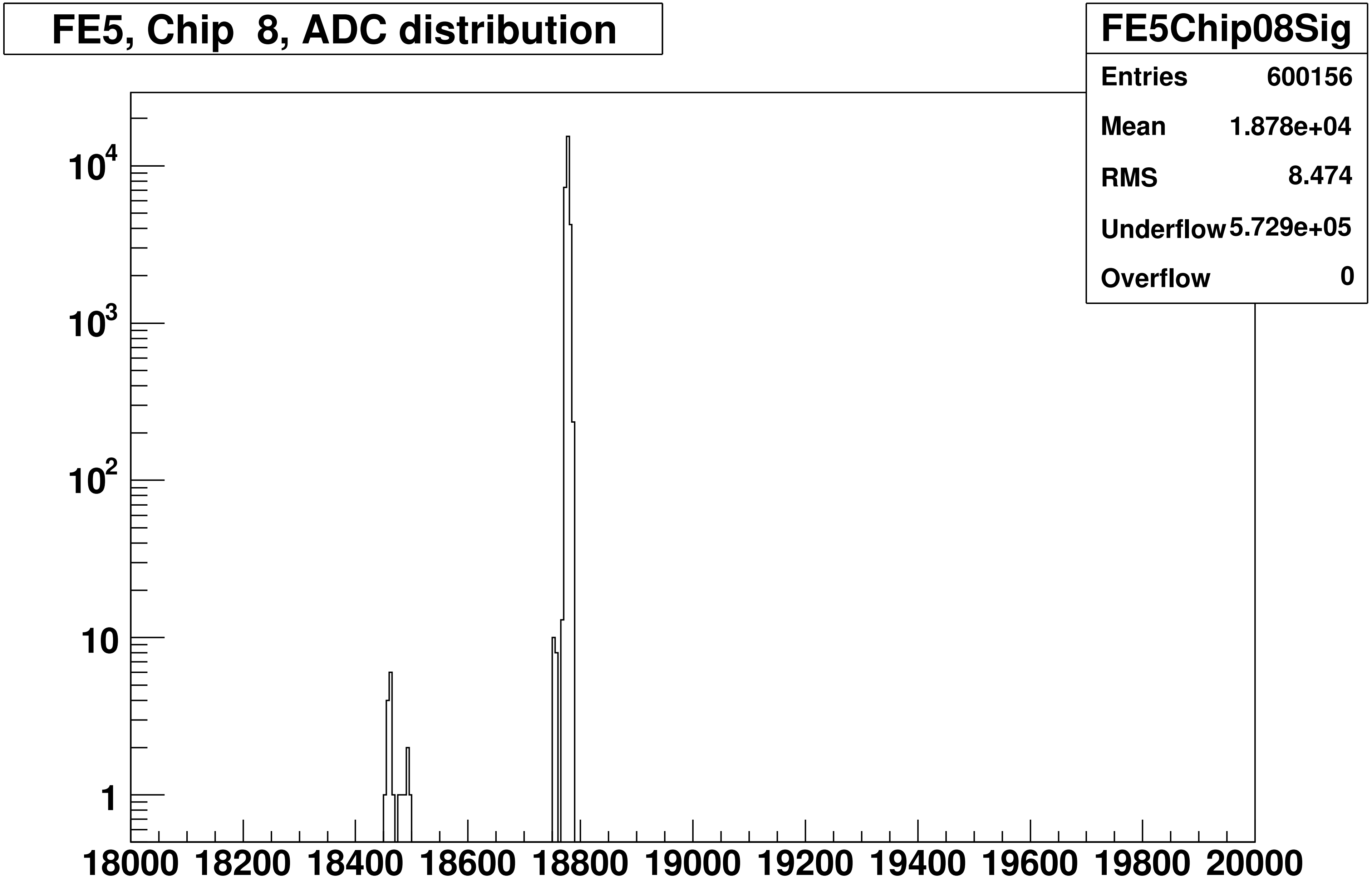
FE5, Chip 8, ADC distribution
FE5Chip08Sig
Entries 600156
Mean 1.878e+04
RMS 8.474
Underflow 5.729e+05
Overflow 0
10^4
10^3
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1
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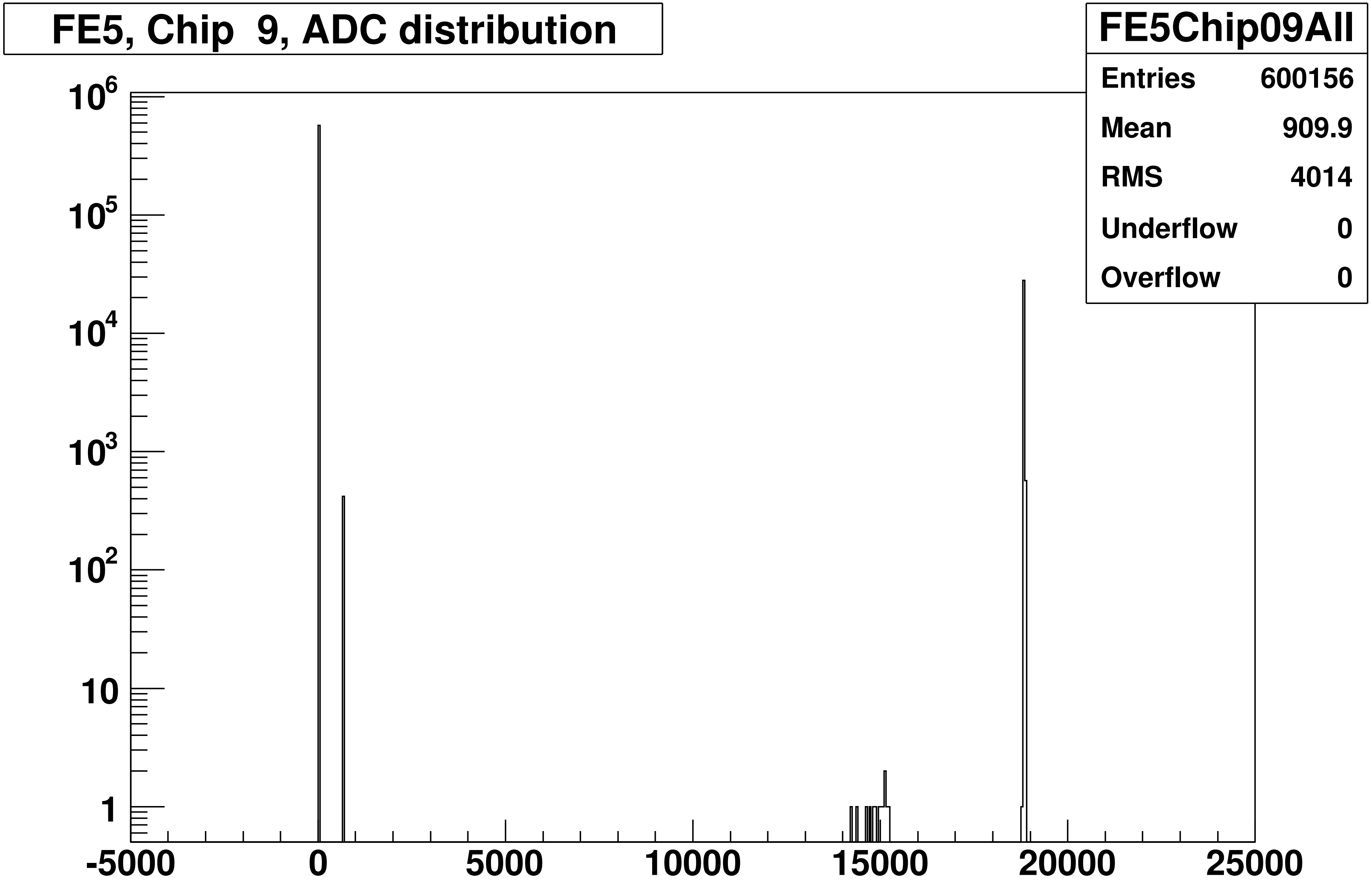
FE5, Chip 9, ADC distribution
FE5Chip09All
Entries 600156
Mean 909.9
RMS 4014
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
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1
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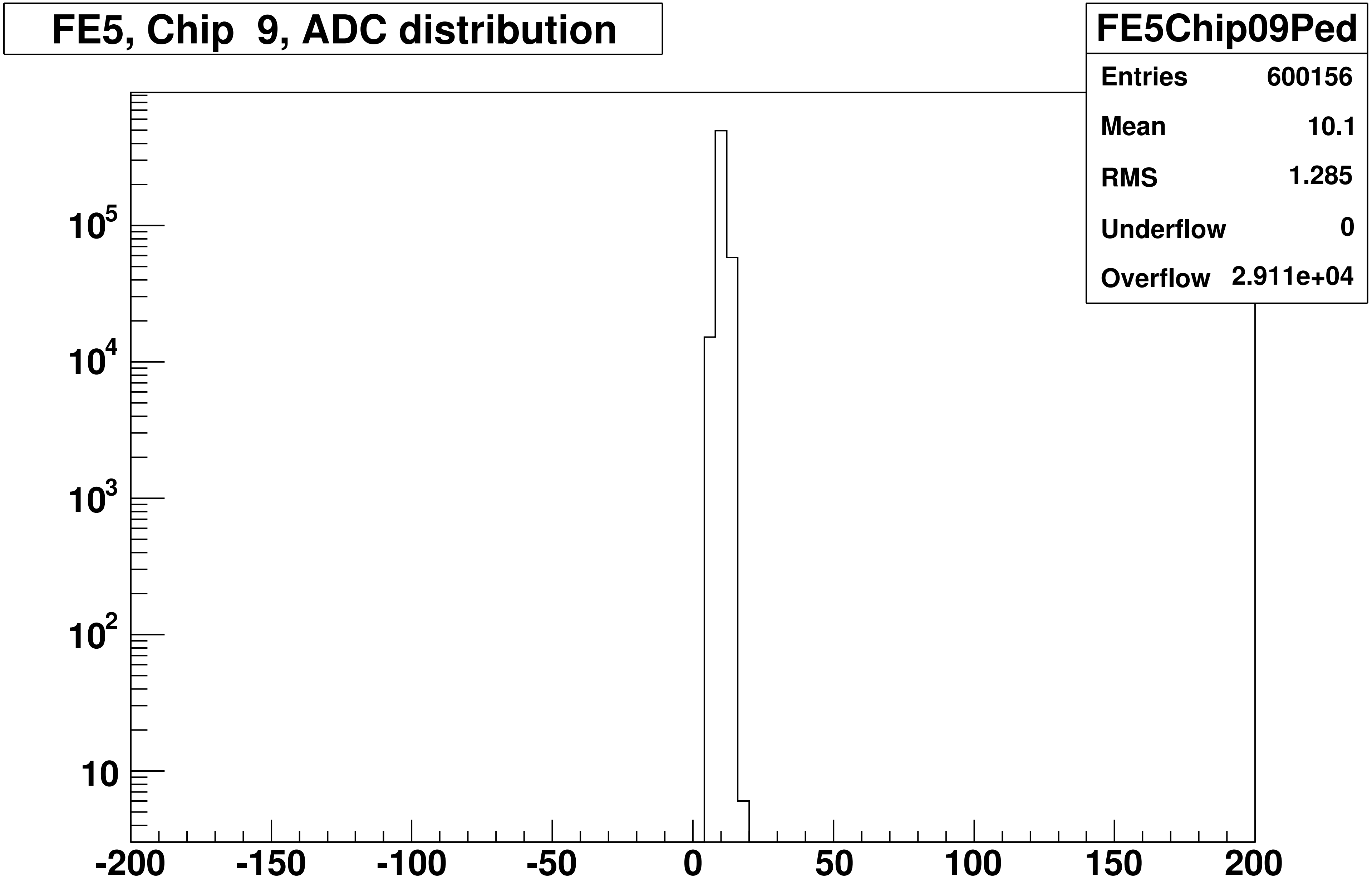
FE5, Chip 9, ADC distribution
FE5Chip09Ped
Entries 600156
Mean 10.1
RMS 1.285
Underflow 0
Overflow 2.911e+04
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10^2
10^3
10^4
10^5
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150
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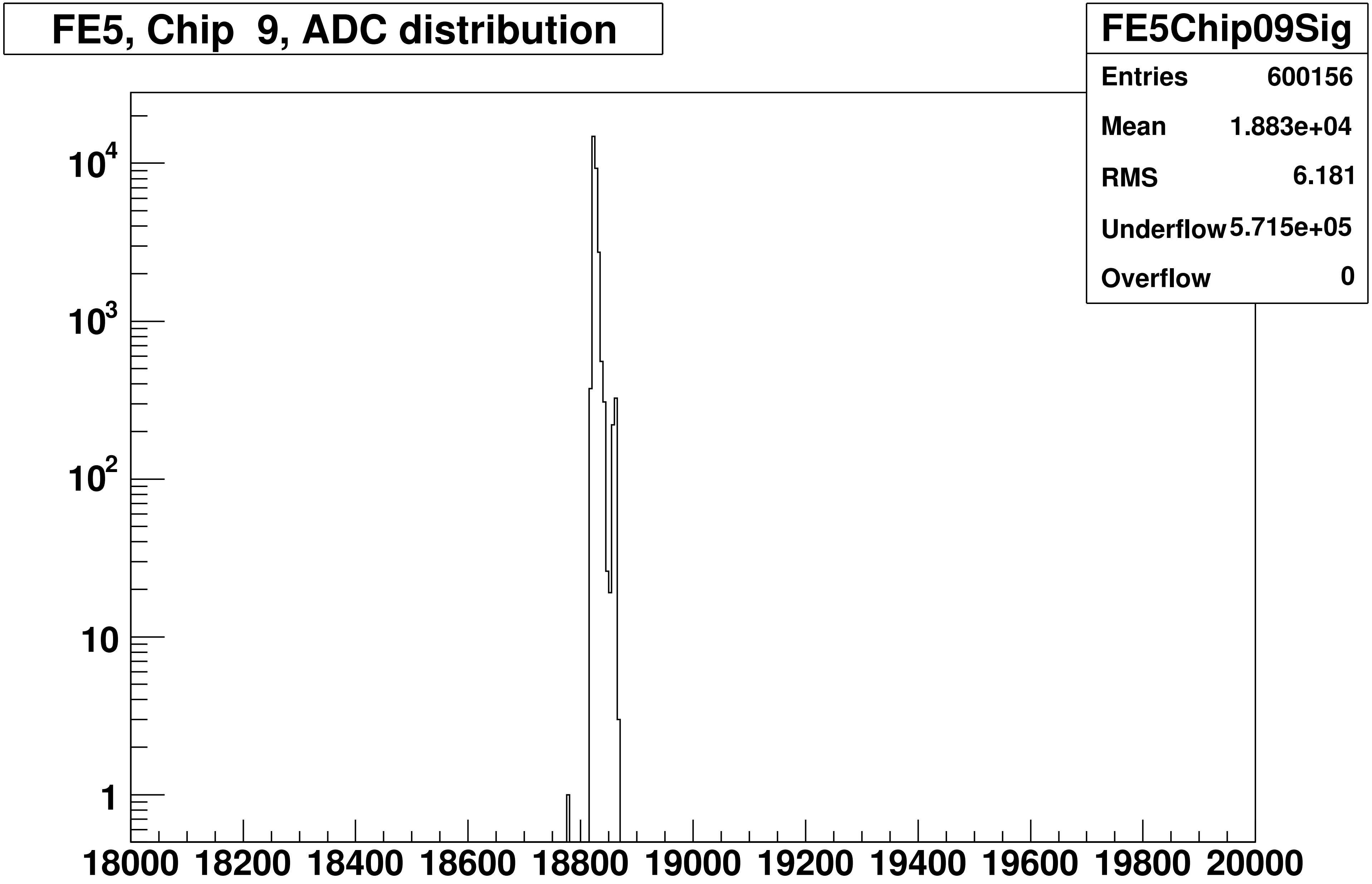
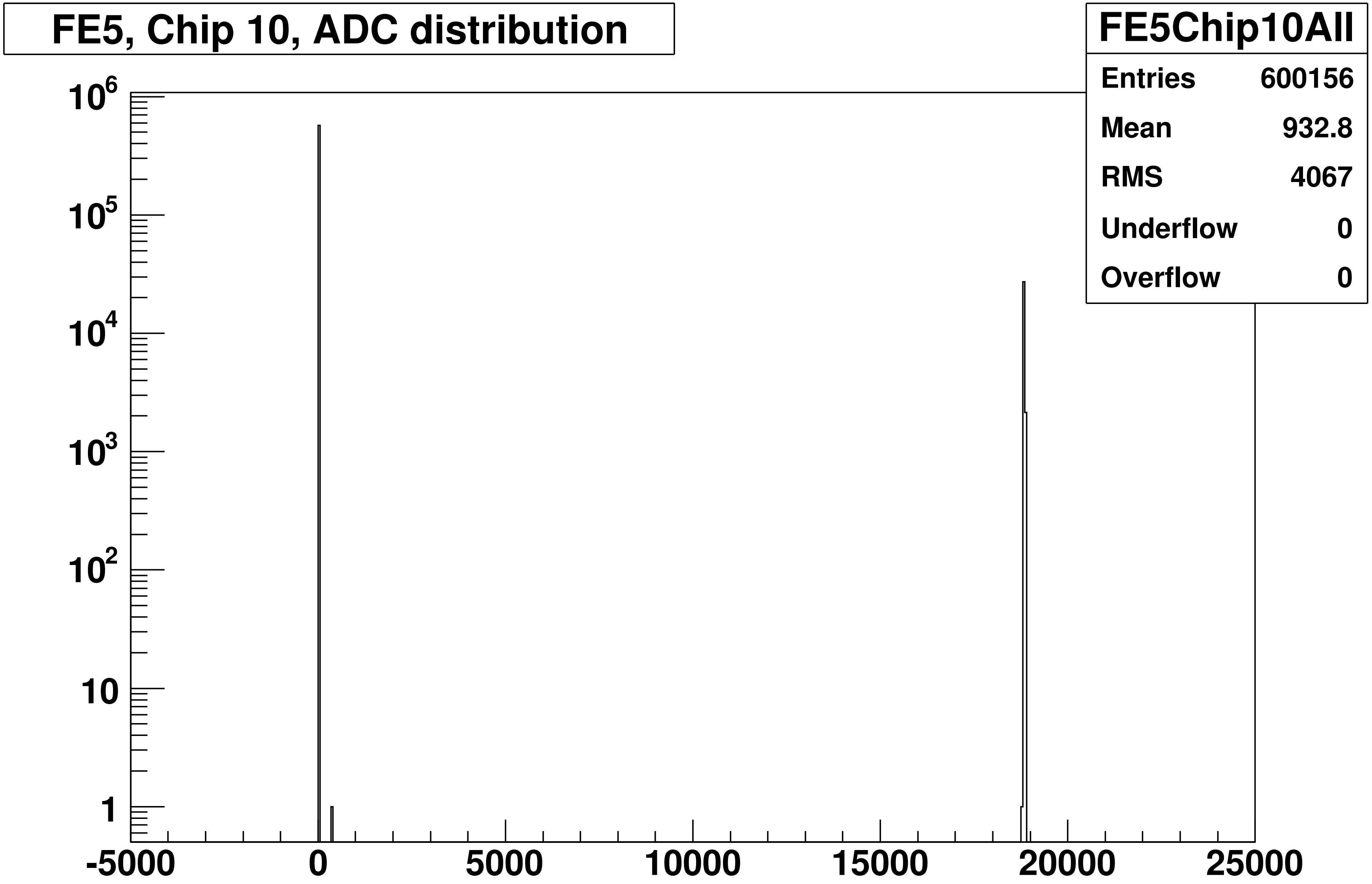


FE5, Chip 9, ADC distribution
FE5Chip09Sig
Entries 600156
Mean 1.883e+04
RMS 6.181
Underflow 5.715e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE5, Chip 10, ADC distribution
FE5Chip10All
Entries 600156
Mean 932.8
RMS 4067
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
1
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0
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10000
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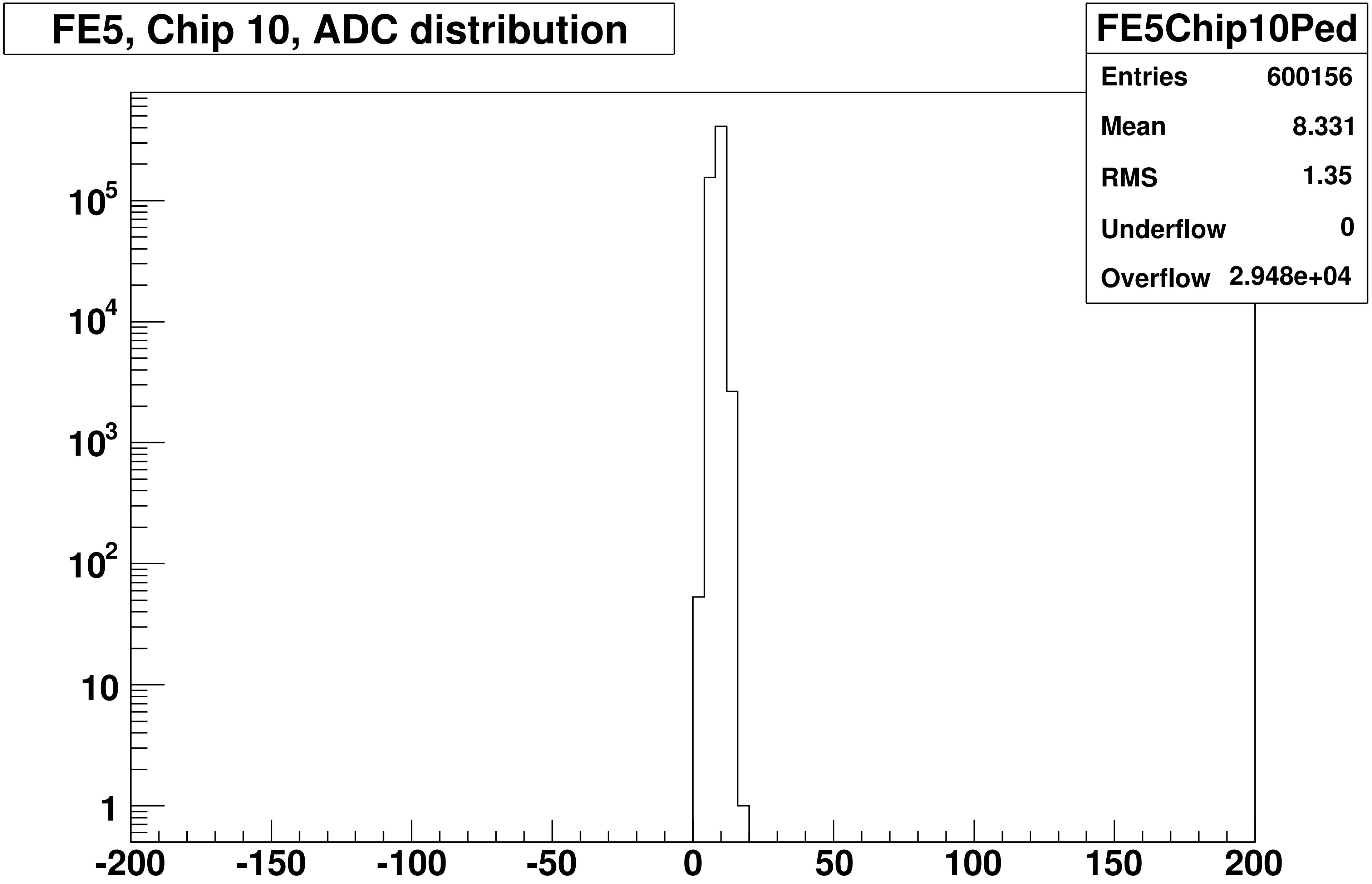
20000
25000


FE5, Chip 10, ADC distribution
FE5Chip10Ped
Entries 600156
Mean 8.331
RMS 1.35
Underflow 0
Overflow 2.948e+04
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10^3
10^2
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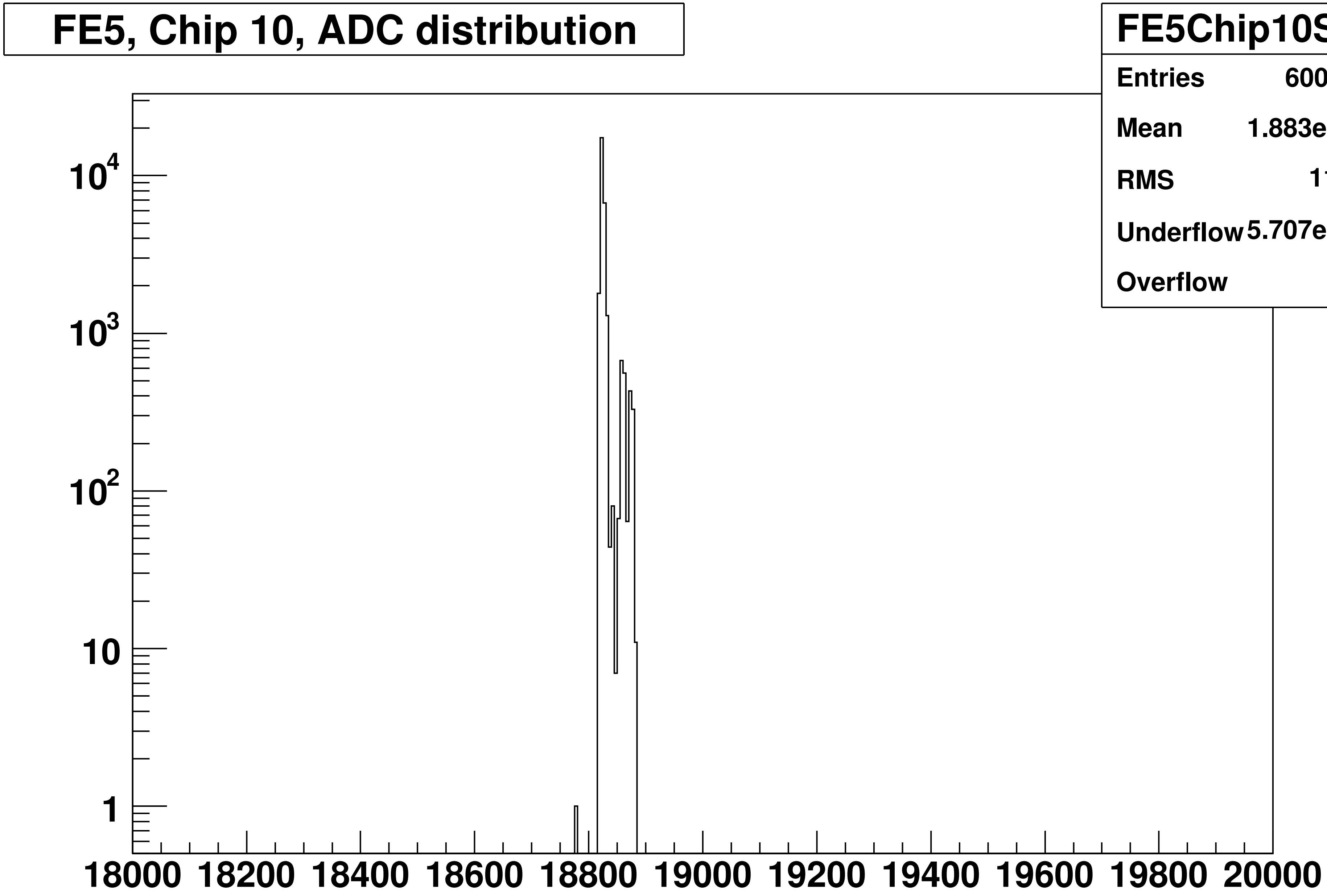
FE5, Chip 10, ADC distribution
FE5Chip10Sig
Entries 600156
Mean 1.883e+04
RMS 11.32
Underflow 5.707e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
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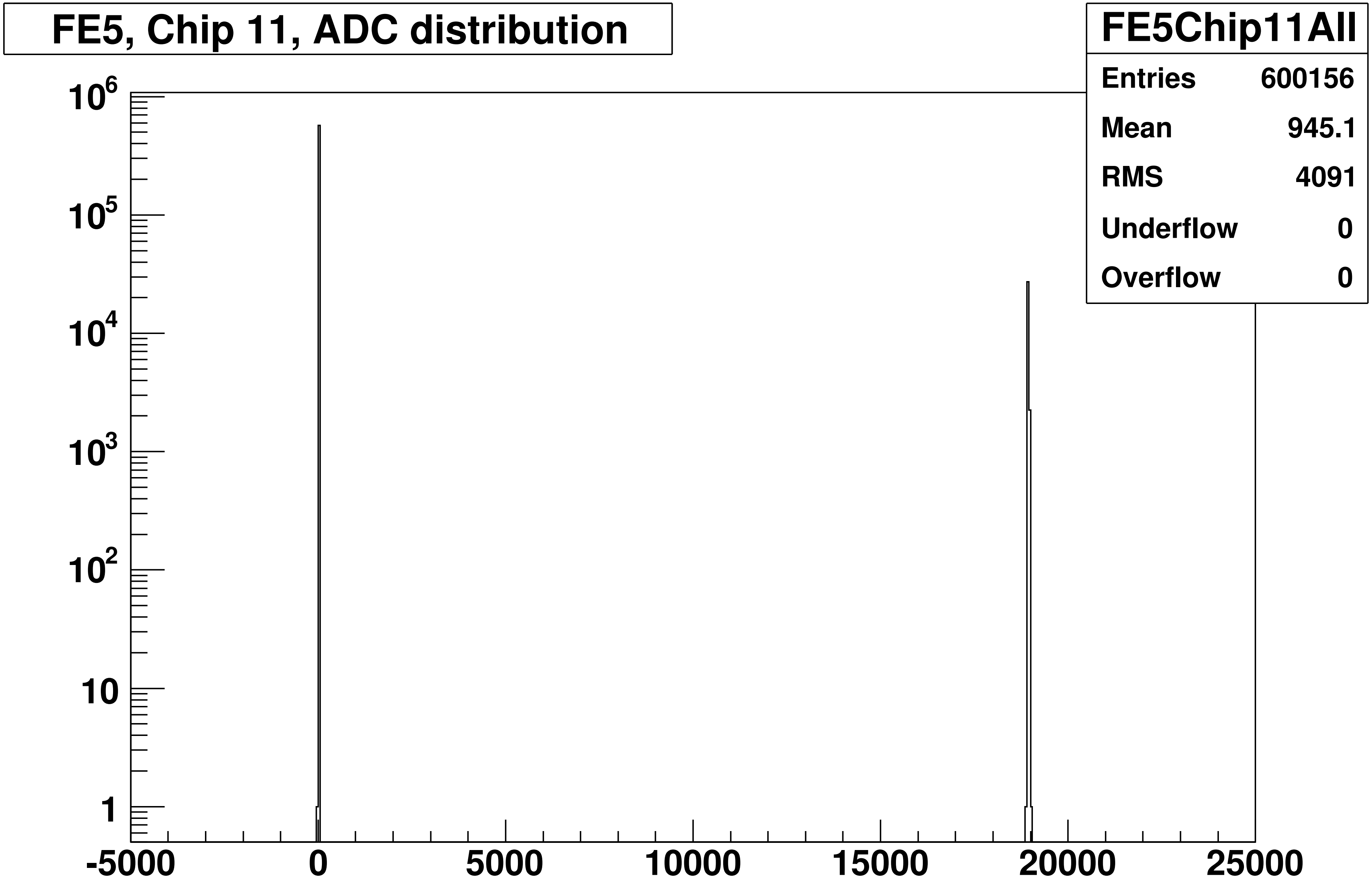
20000



FE5, Chip 11, ADC distribution
FE5Chip11All
Entries 600156
Mean 945.1
RMS 4091
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
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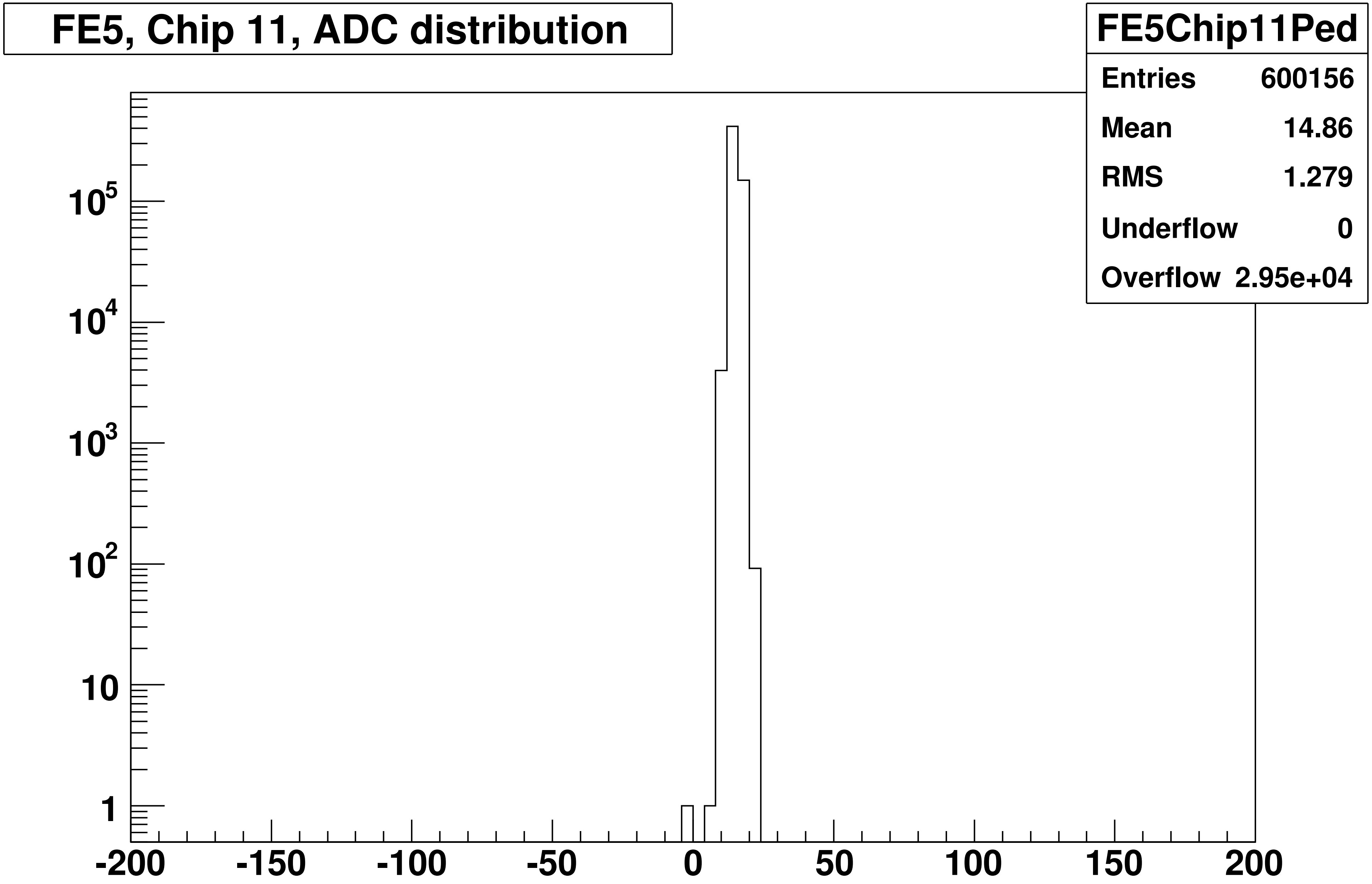
FE5, Chip 11, ADC distribution
FE5Chip11Ped
Entries 600156
Mean 14.86
RMS 1.279
Underflow 0
Overflow 2.95e+04
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10^4
10^3
10^2
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1
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100
150
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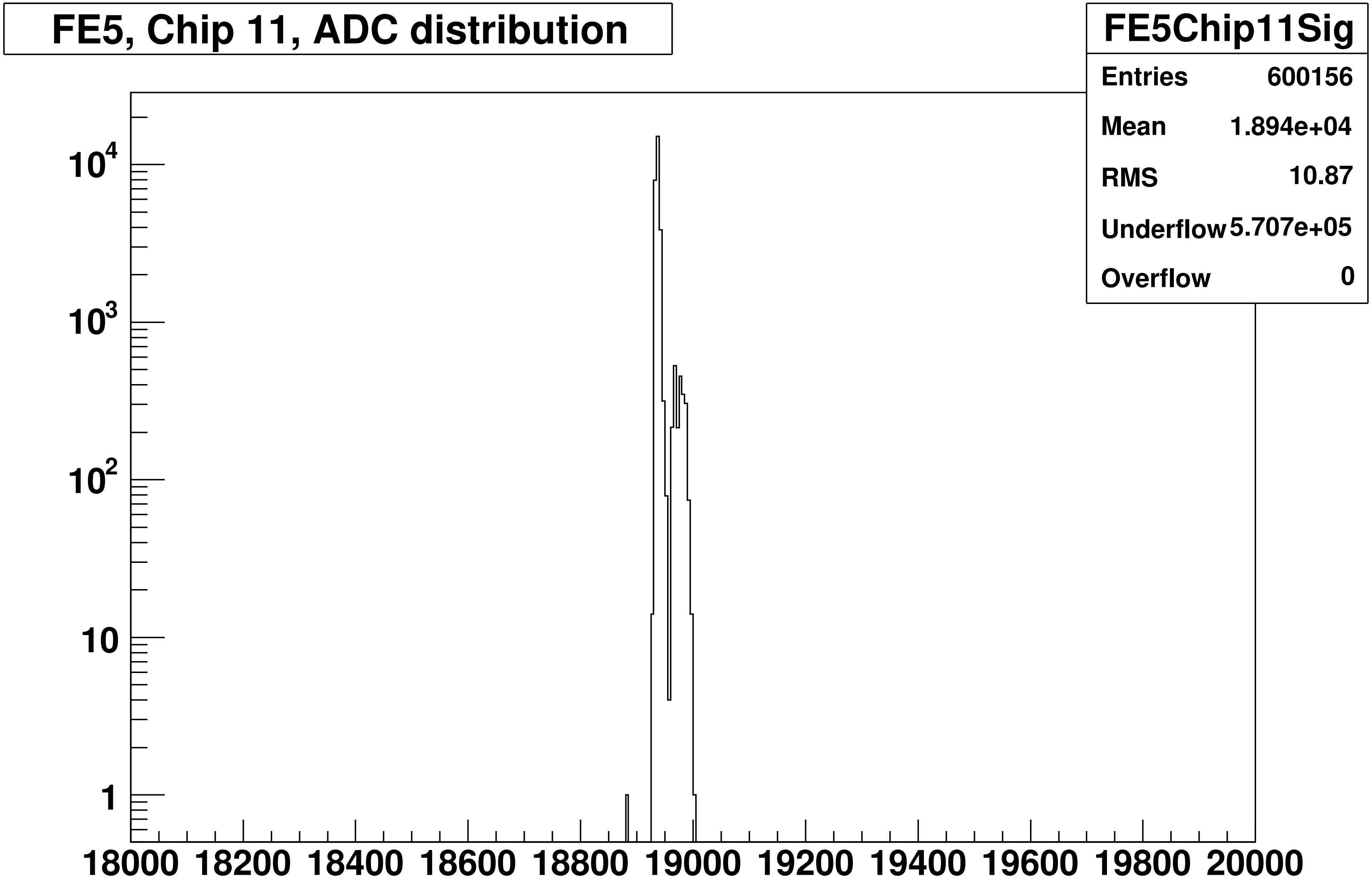
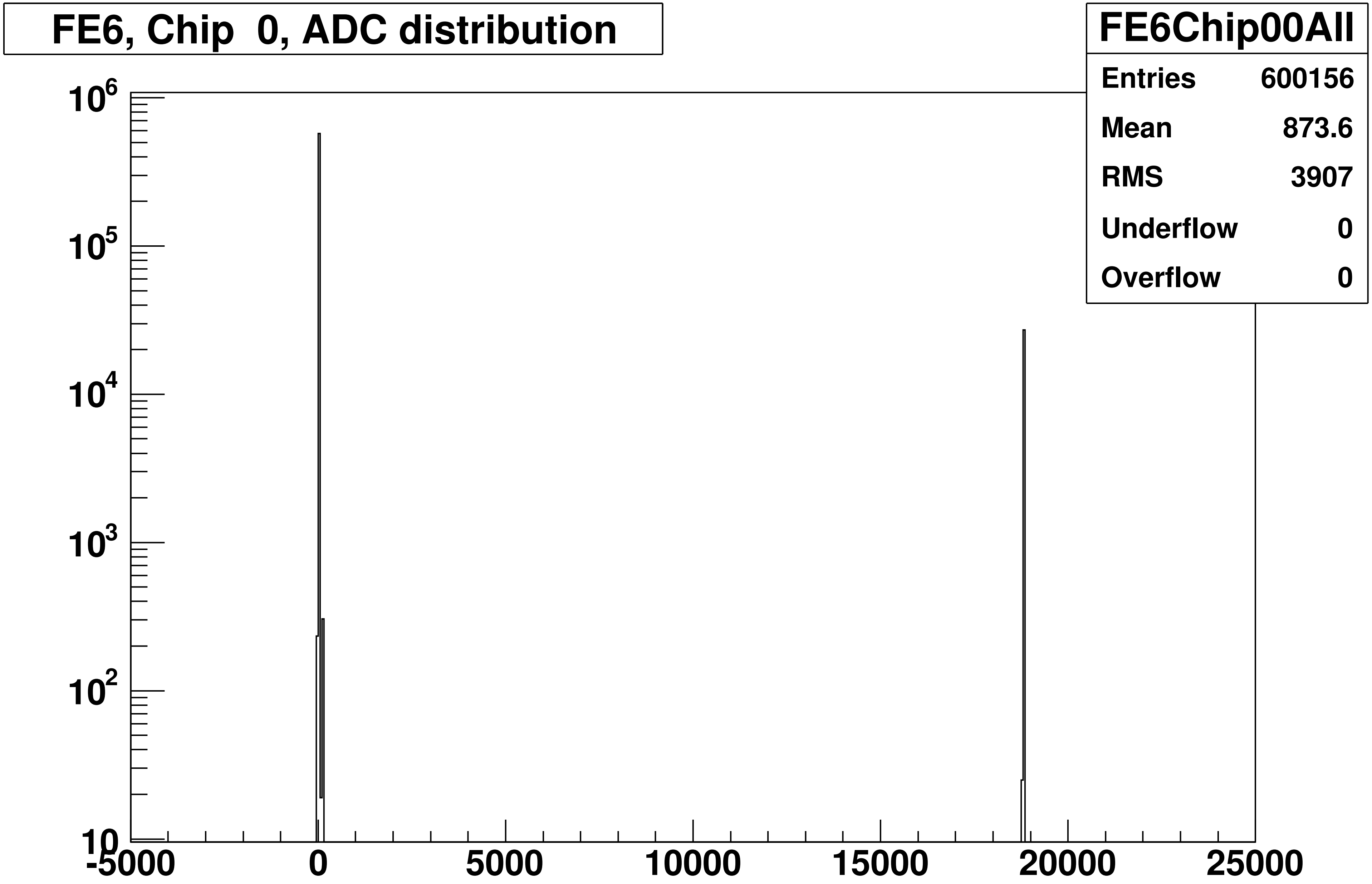
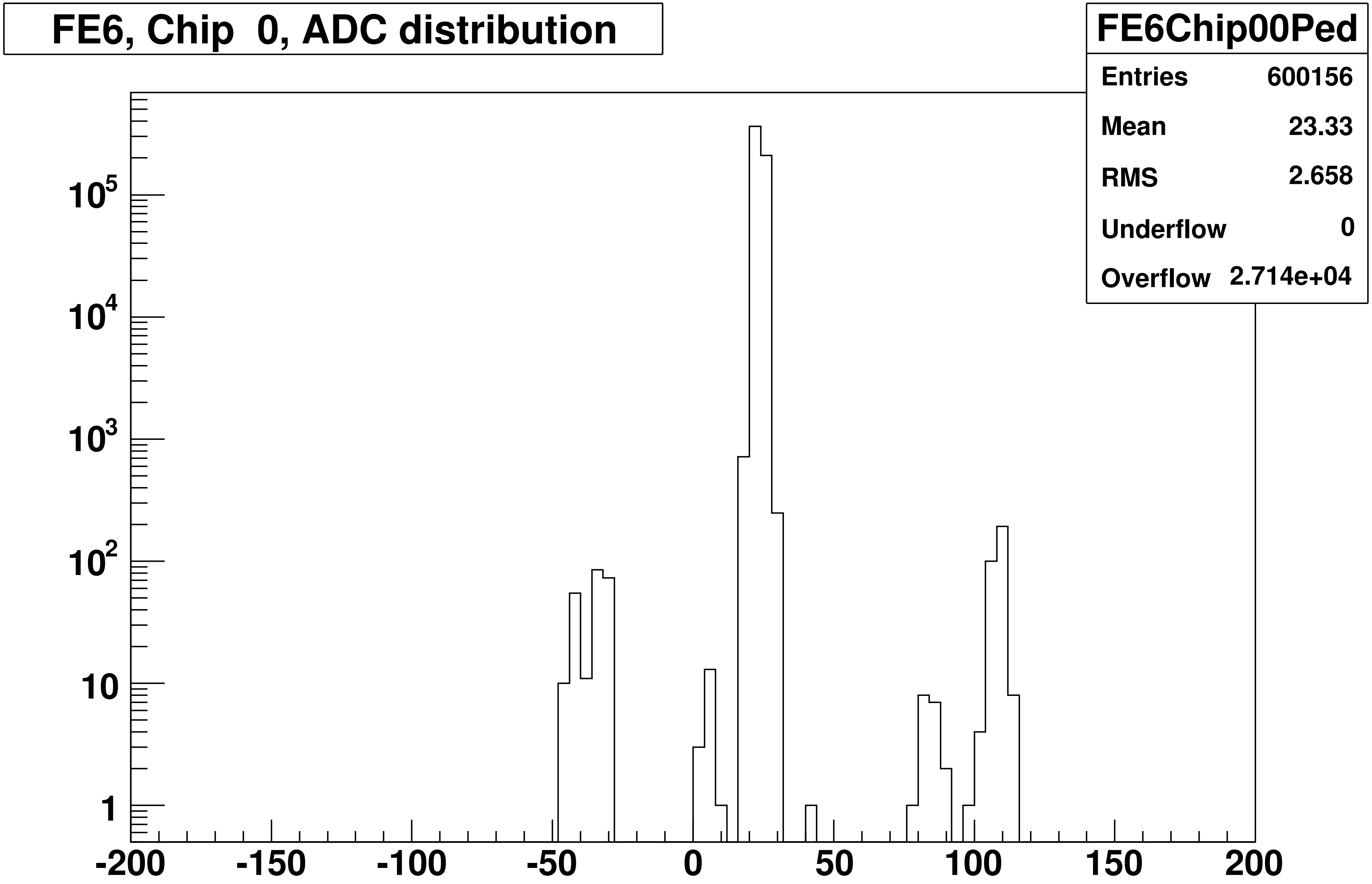

FE5, Chip 11, ADC distribution
FE5Chip11Sig
Entries 600156
Mean 1.894e+04
RMS 10.87
Underflow 5.707e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE6, Chip 0, ADC distribution
FE6Chip00All
Entries 600156
Mean 873.6
RMS 3907
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE6, Chip 0, ADC distribution
FE6Chip00Ped
Entries 600156
Mean 23.33
RMS 2.658
Underflow 0
Overflow 2.714e+04
10^5
10^4
10^3
10^2
10
1
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-150
-100
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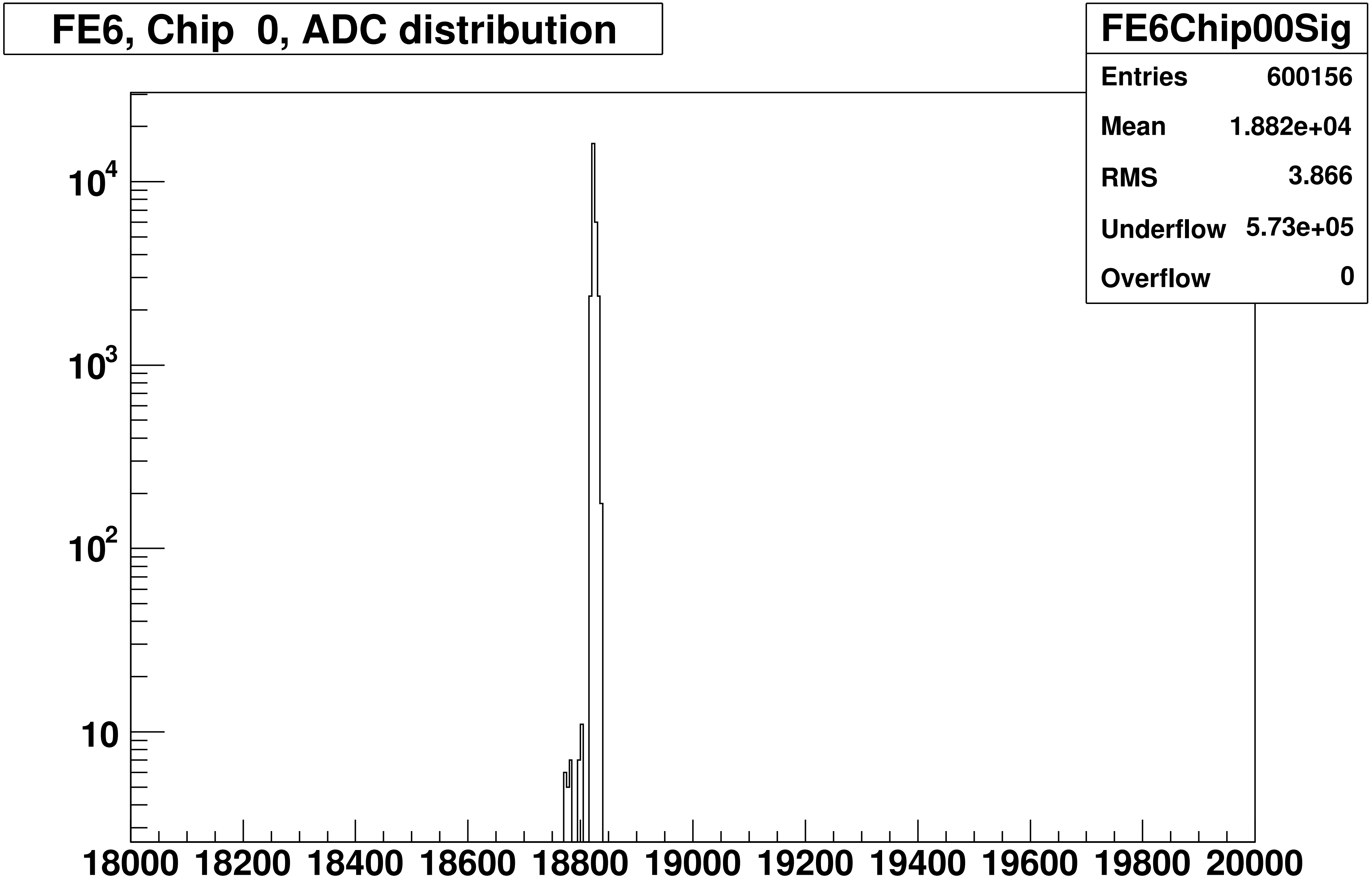
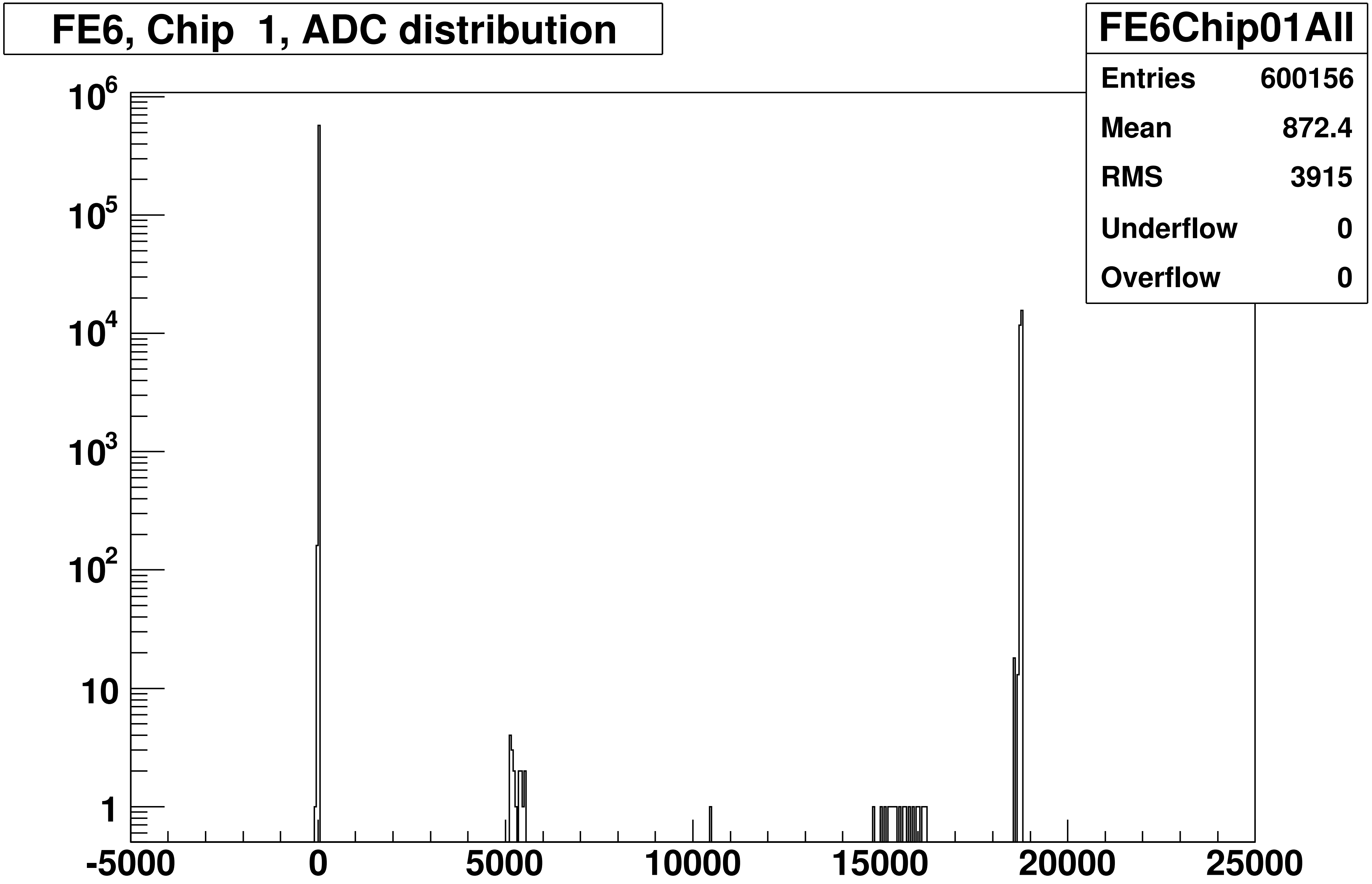
0
50
100
150
200



FE6, Chip 0, ADC distribution
FE6Chip00Sig
Entries 600156
Mean 1.882e+04
RMS 3.866
Underflow 5.73e+05
Overflow 0
10^4
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE6, Chip 1, ADC distribution
FE6Chip01All
Entries 600156
Mean 872.4
RMS 3915
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
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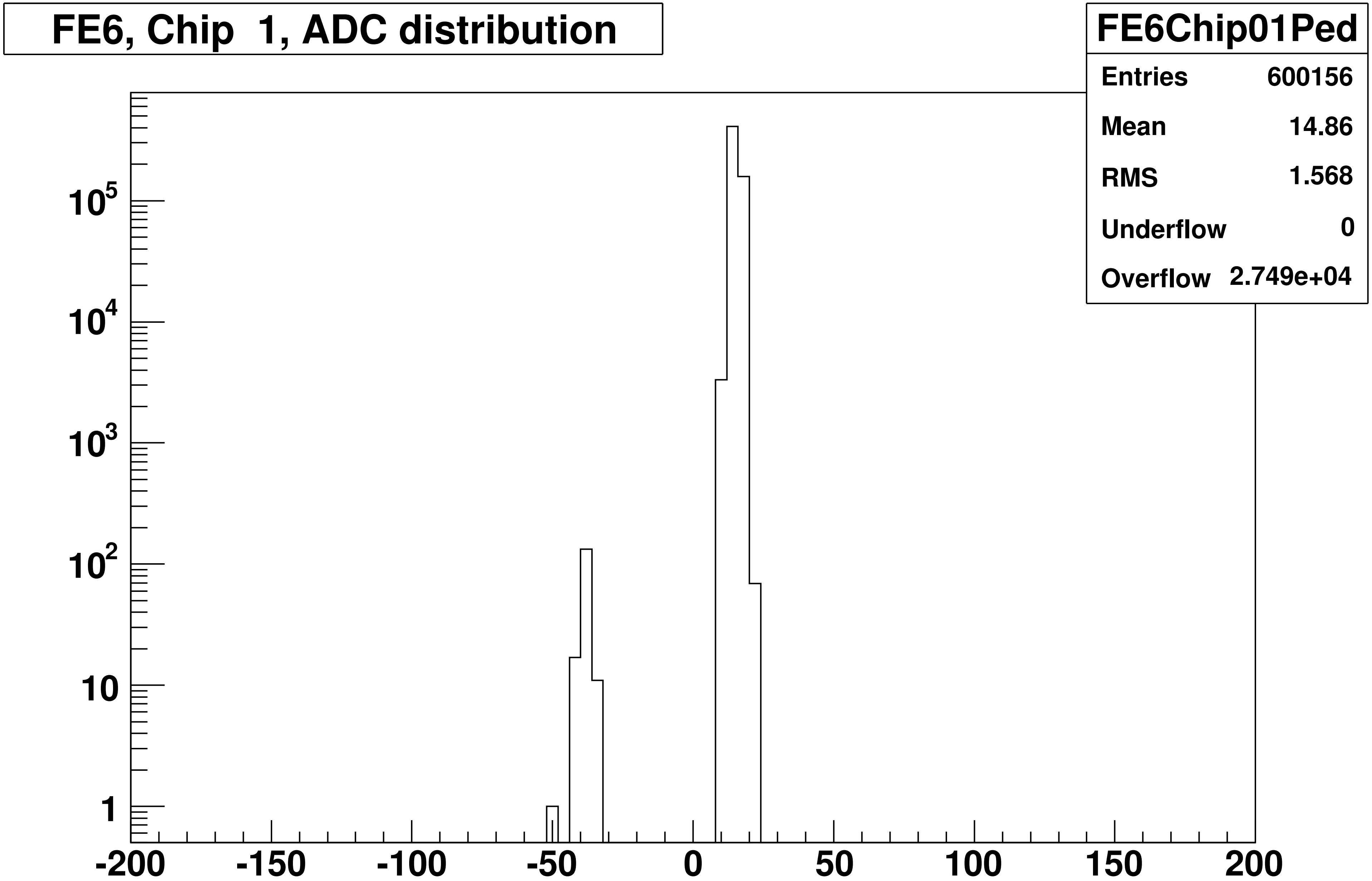
20000
25000


FE6, Chip 1, ADC distribution
FE6Chip01Ped
Entries 600156
Mean 14.86
RMS 1.568
Underflow 0
Overflow 2.749e+04
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10^3
10^4
10^5
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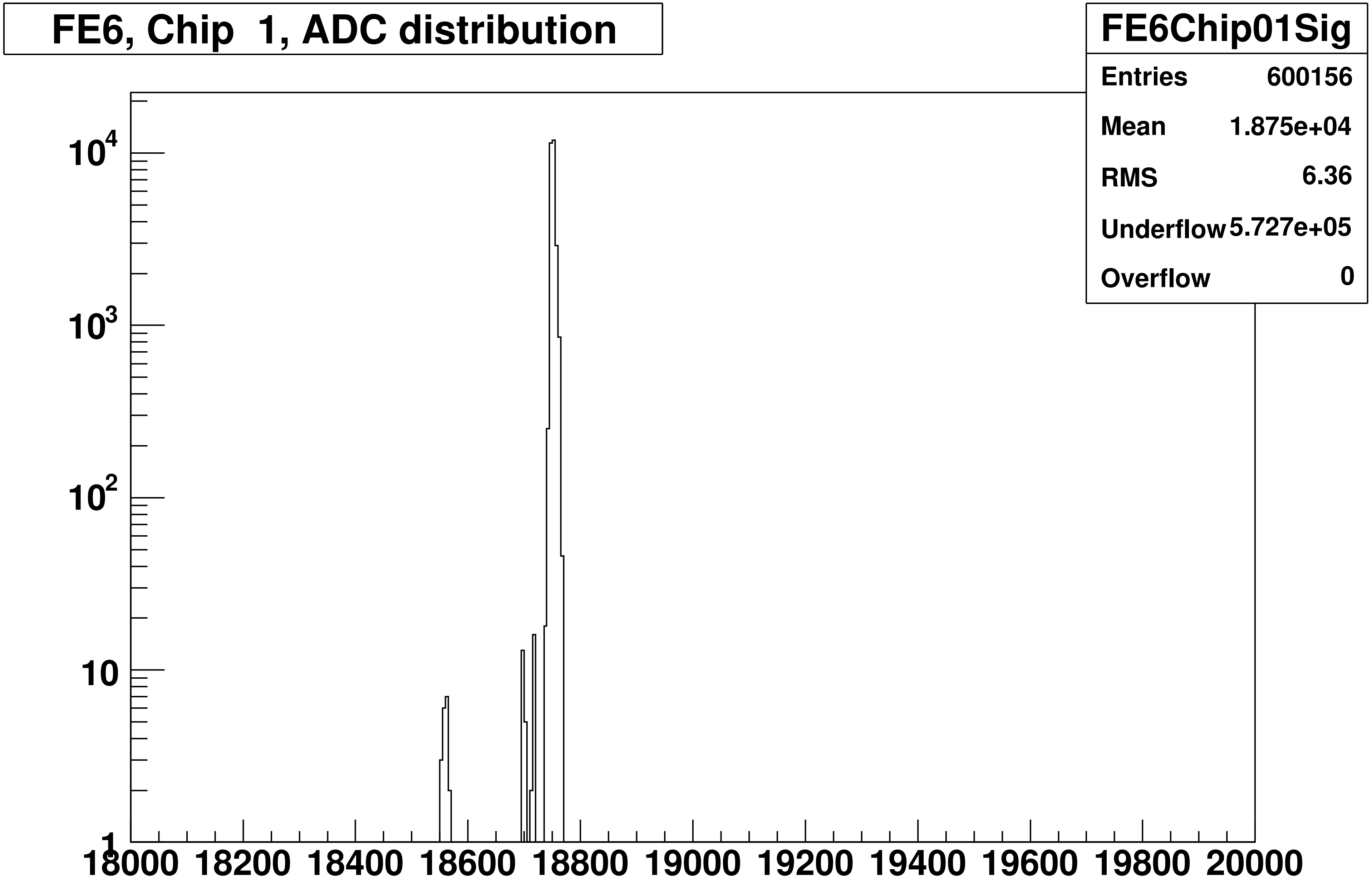
-100
-50
0
50
100
150
200



FE6, Chip 1, ADC distribution
FE6Chip01Sig
Entries 600156
Mean 1.875e+04
RMS 6.36
Underflow 5.727e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
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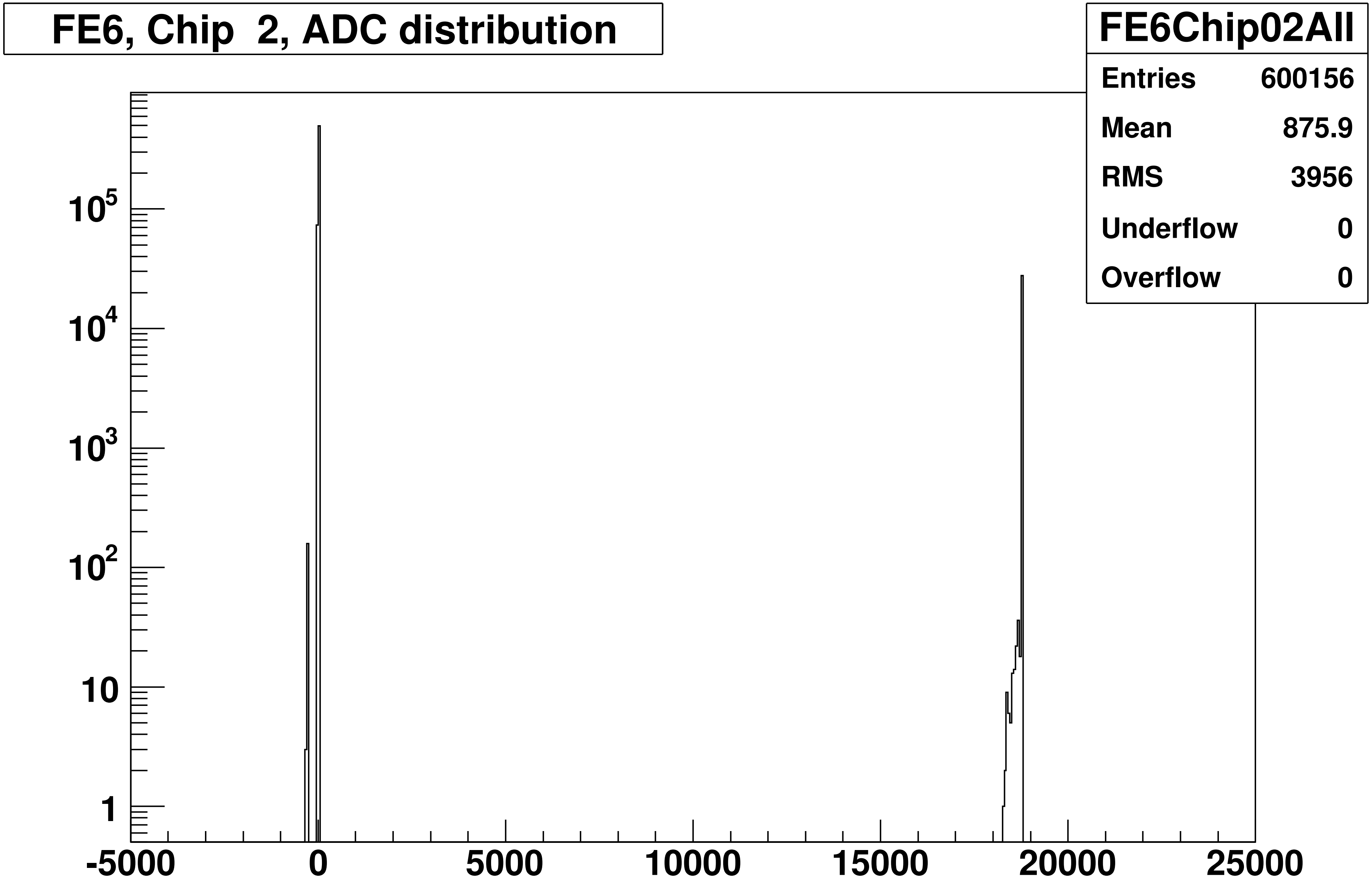

FE6, Chip 2, ADC distribution
FE6Chip02All
Entries 600156
Mean 875.9
RMS 3956
Underflow 0
Overflow 0
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10^4
10^3
10^2
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0
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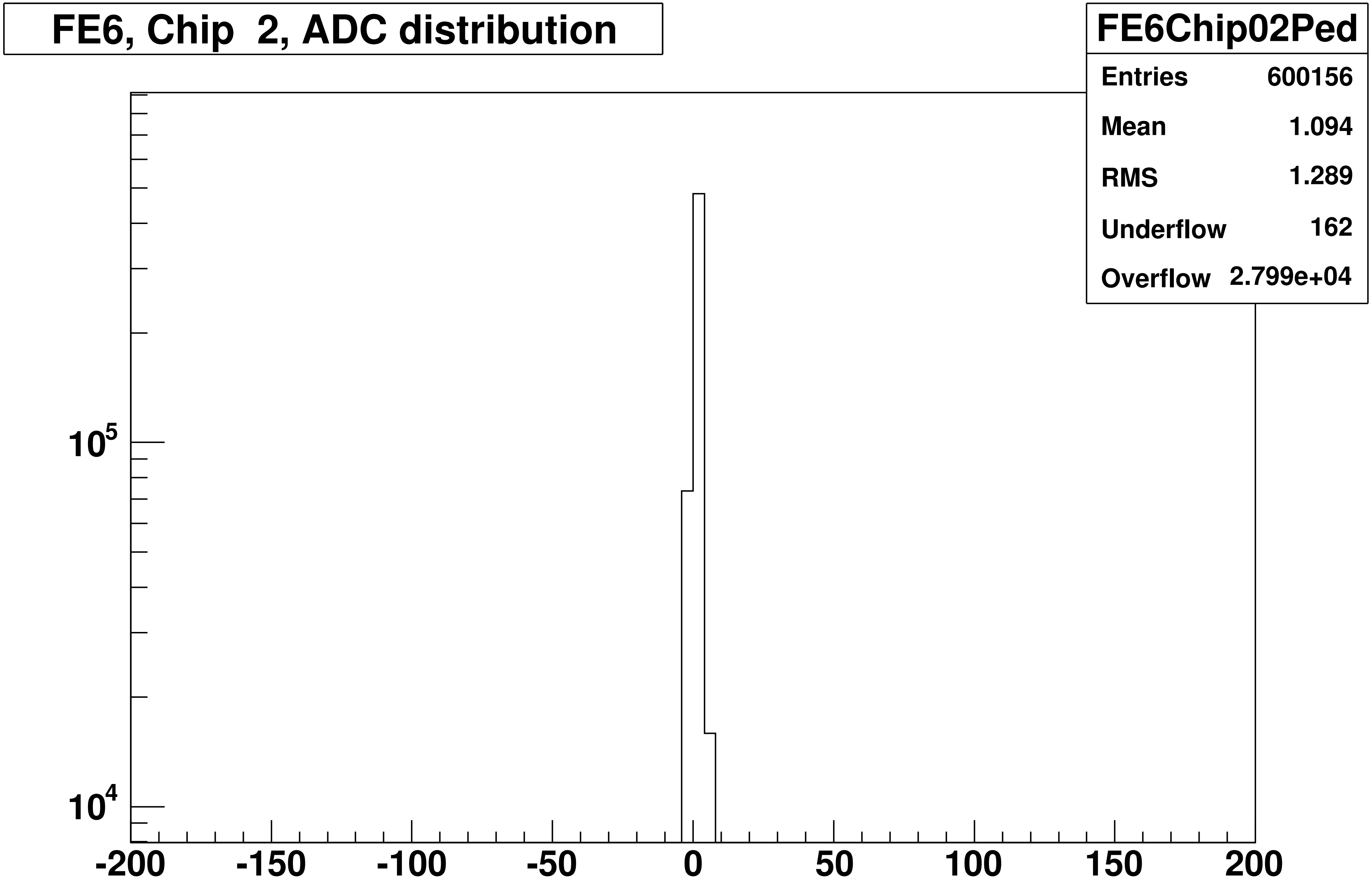

FE6, Chip 2, ADC distribution
FE6Chip02Ped
Entries 600156
Mean 1.094
RMS 1.289
Underflow 162
Overflow 2.799e+04
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10^4
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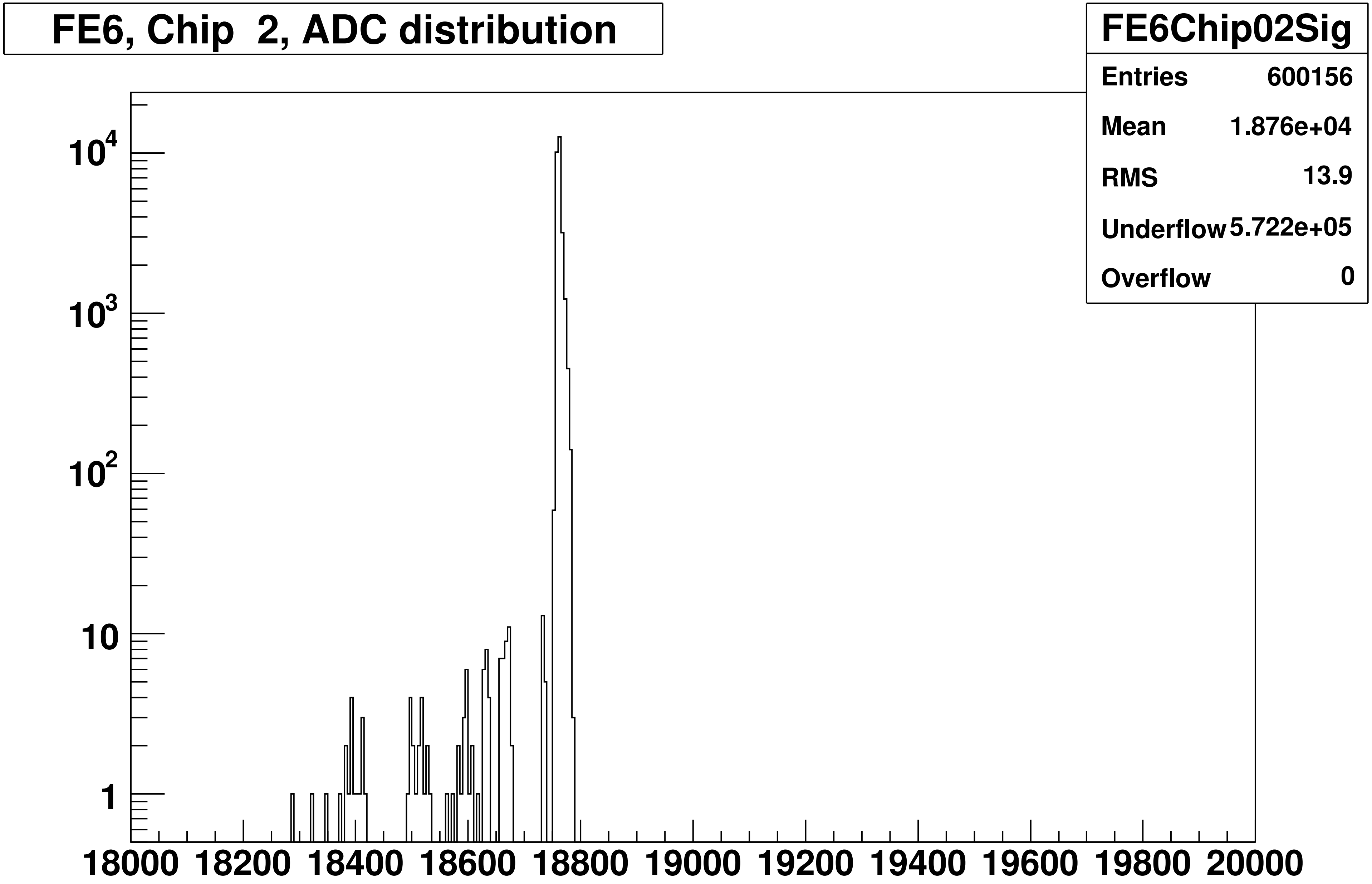
100
150
200


FE6, Chip 2, ADC distribution
FE6Chip02Sig
Entries 600156
Mean 1.876e+04
RMS 13.9
Underflow 5.722e+05
Overflow 0
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10^3
10^2
10
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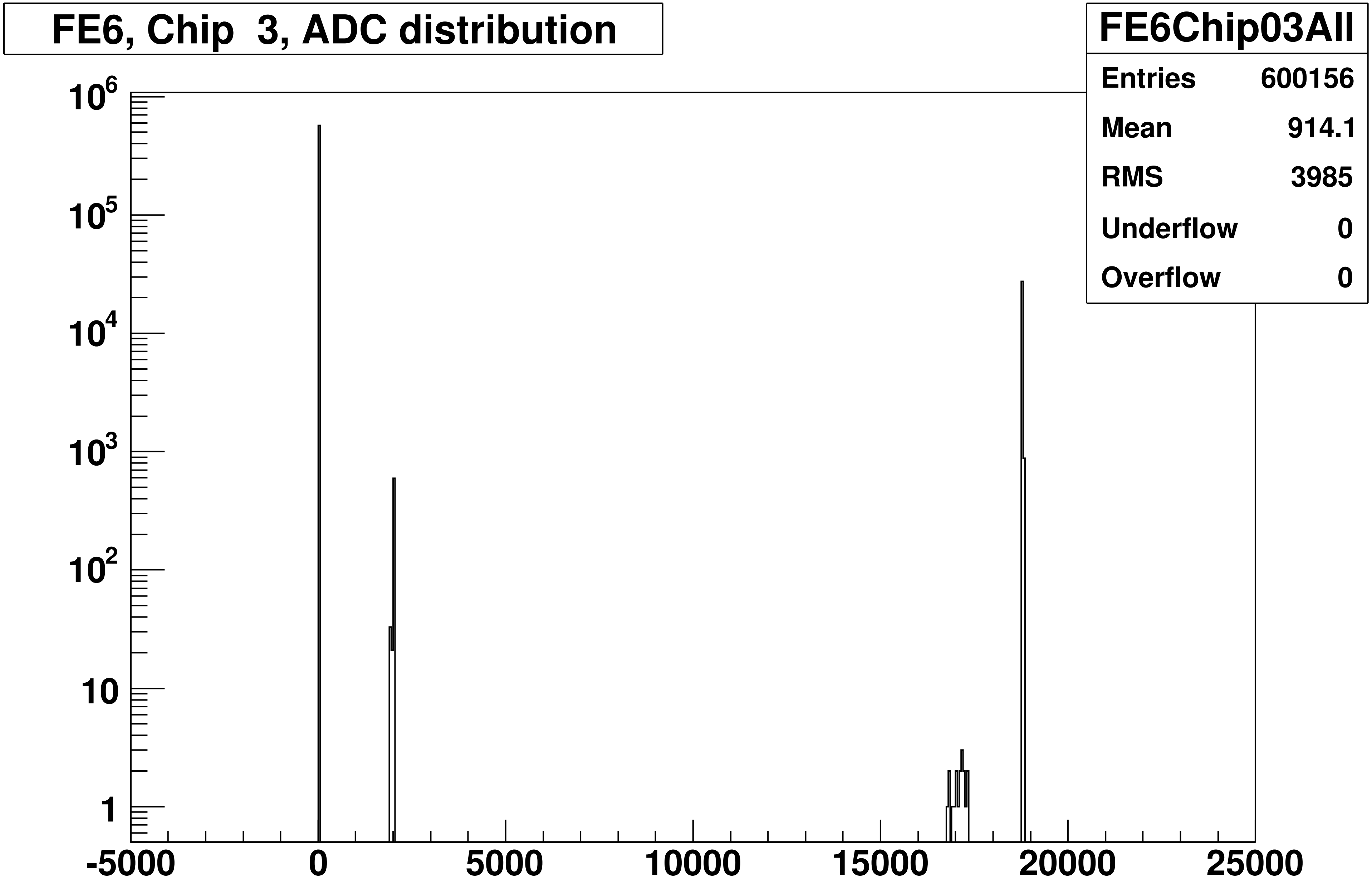
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE6, Chip 3, ADC distribution
FE6Chip03All
Entries 600156
Mean 914.1
RMS 3985
Underflow 0
Overflow 0
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10^2
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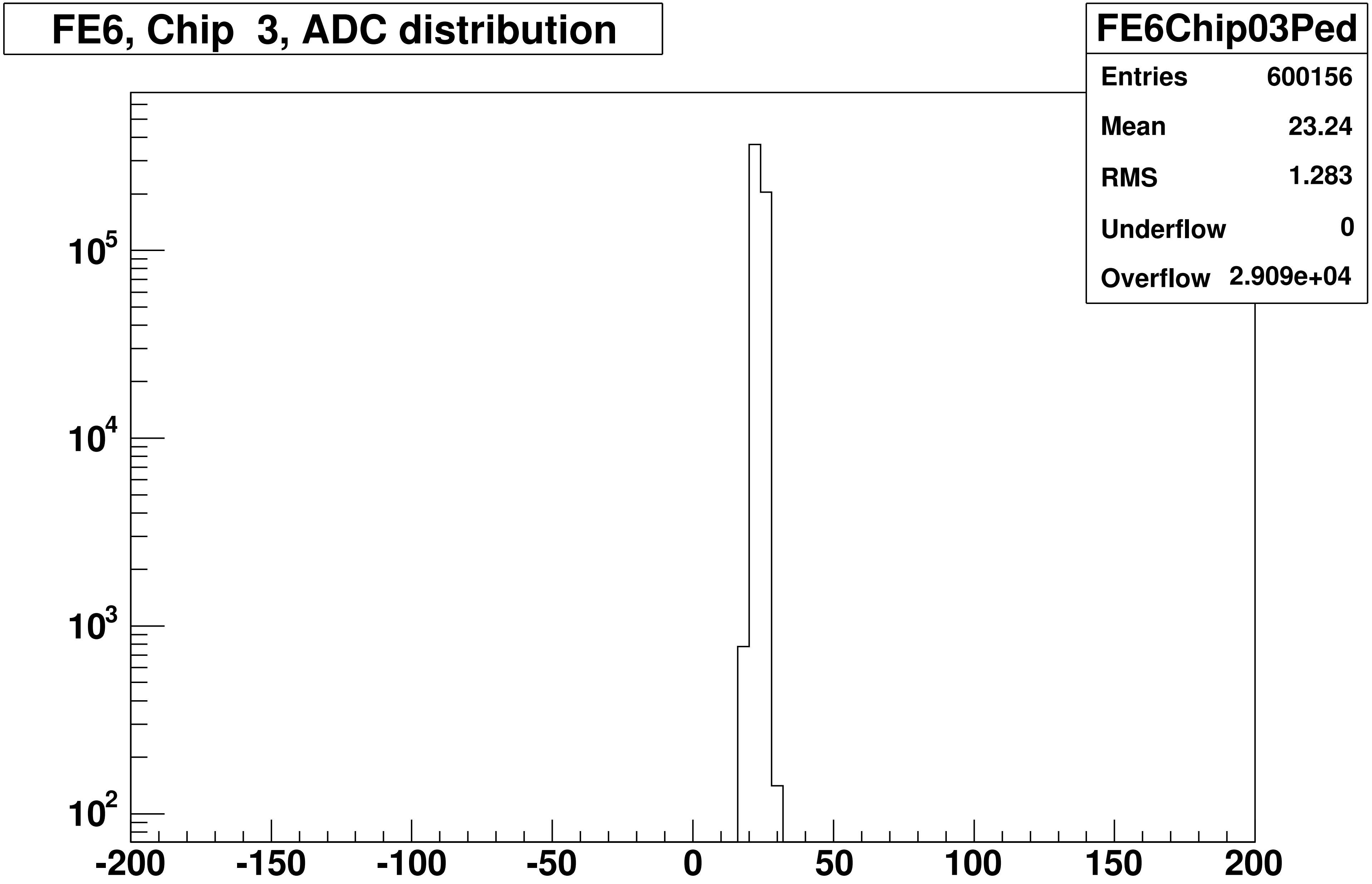
FE6, Chip 3, ADC distribution
FE6Chip03Ped
Entries 600156
Mean 23.24
RMS 1.283
Underflow 0
Overflow 2.909e+04
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10^3
10^2
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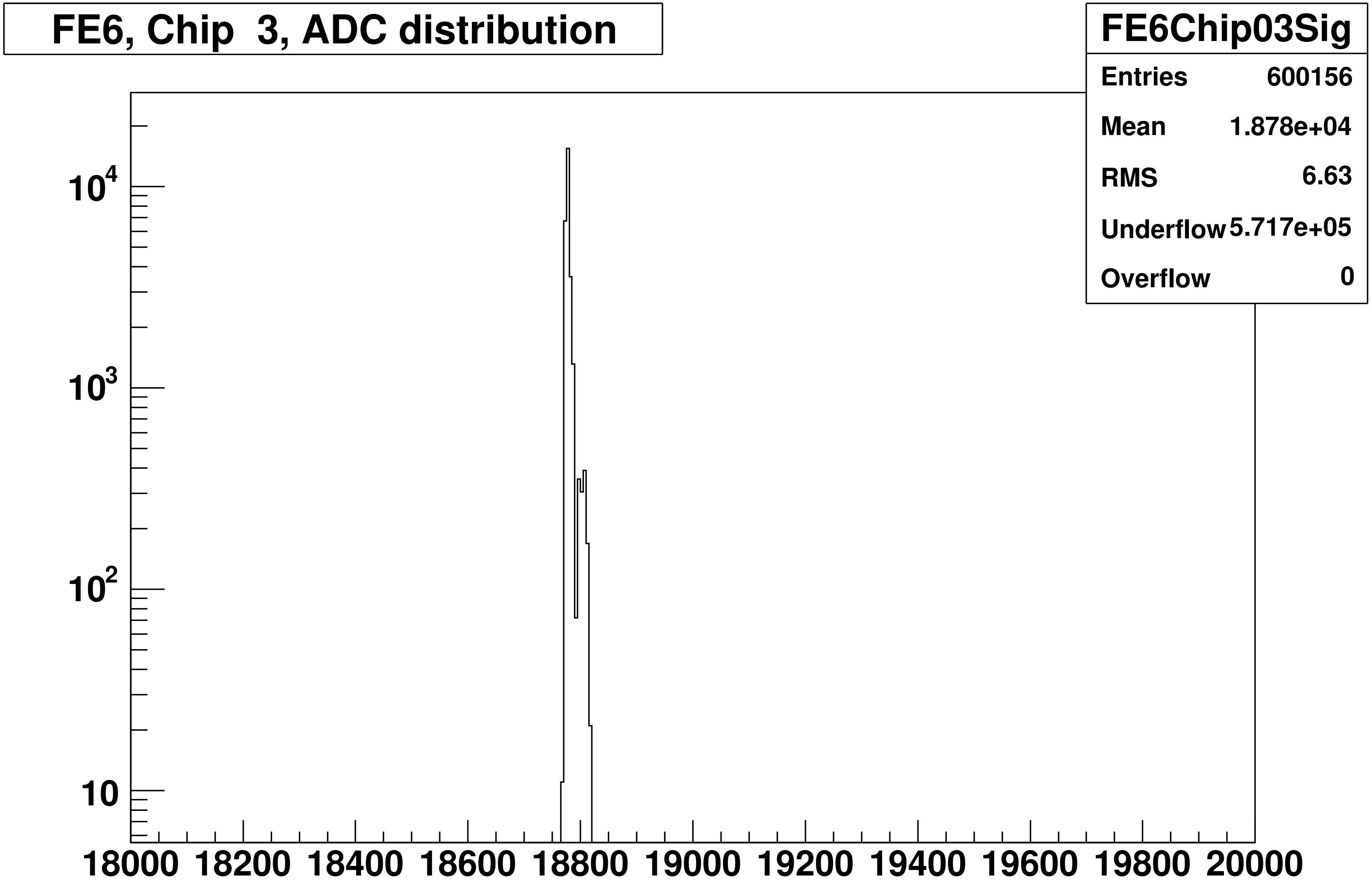
200



FE6, Chip 3, ADC distribution
FE6Chip03Sig
Entries 600156
Mean 1.878e+04
RMS 6.63
Underflow 5.717e+05
Overflow 0
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10^3
10^2
10
18000
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18400
18600
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19000
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19600
19800
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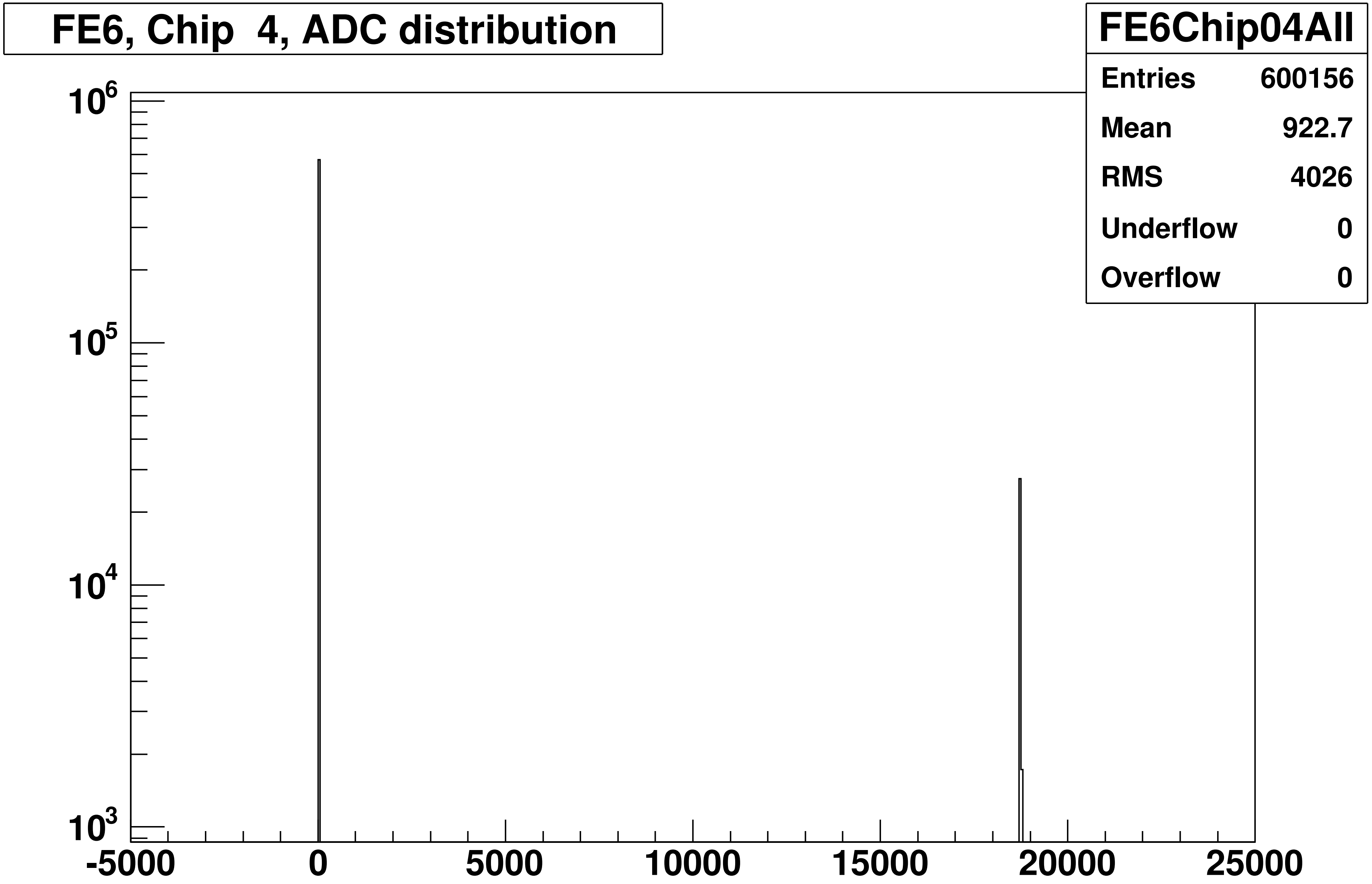

FE6, Chip 4, ADC distribution
FE6Chip04All
Entries 600156
Mean 922.7
RMS 4026
Underflow 0
Overflow 0
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10^4
10^3
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5000
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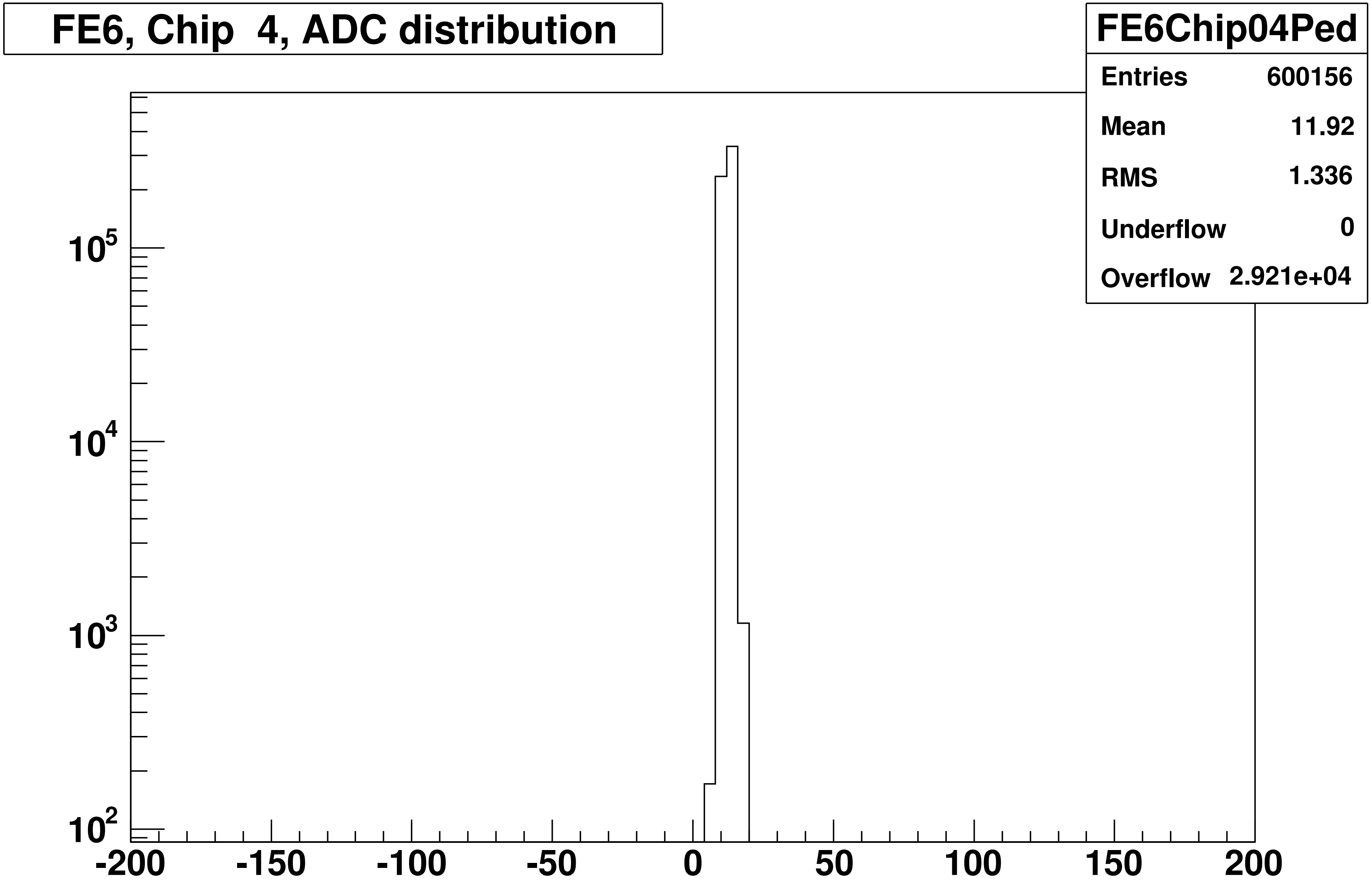
20000
25000



FE6, Chip 4, ADC distribution
FE6Chip04Ped
Entries 600156
Mean 11.92
RMS 1.336
Underflow 0
Overflow 2.921e+04
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10^4
10^3
10^2
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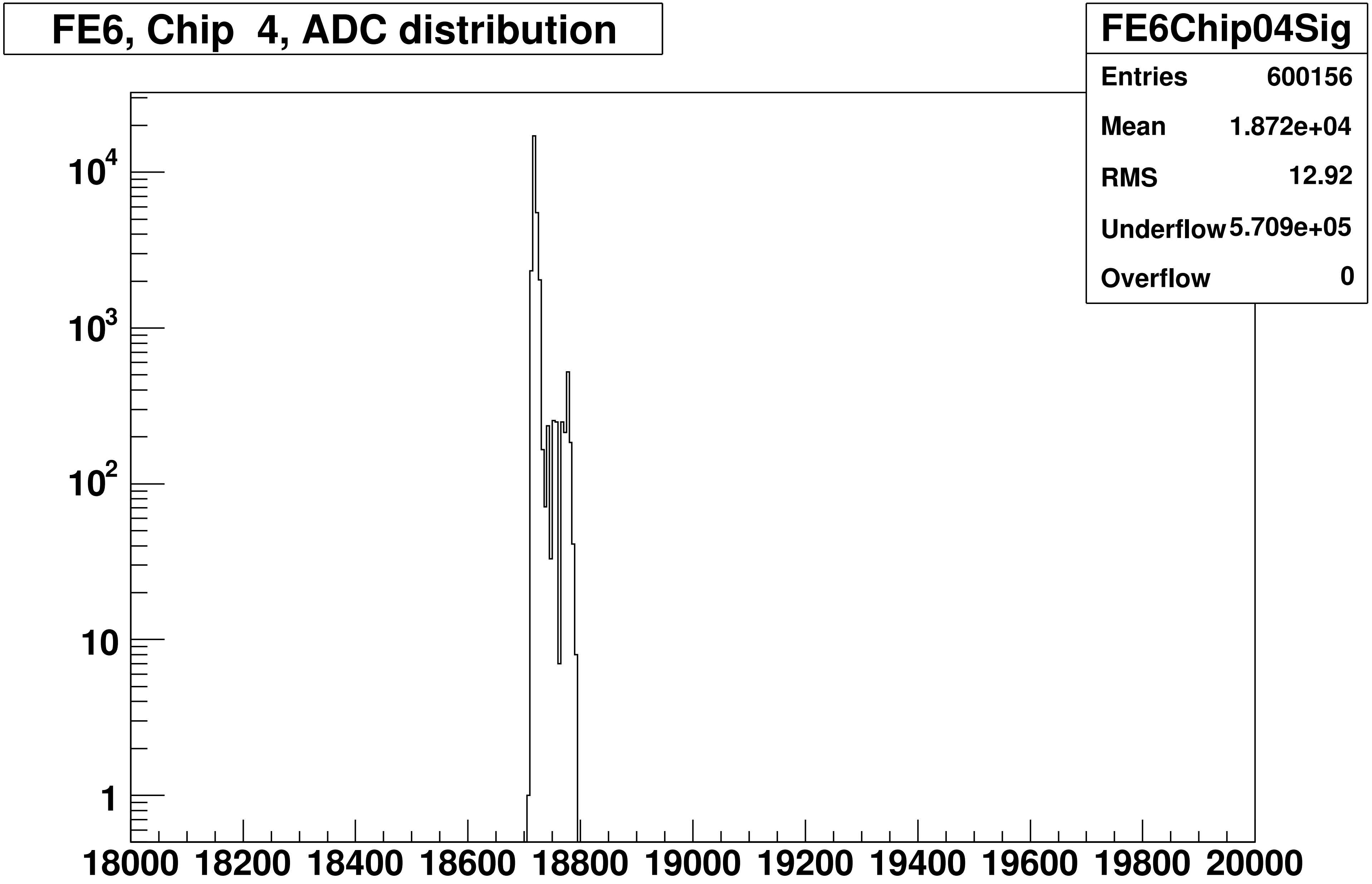
200



FE6, Chip 4, ADC distribution
FE6Chip04Sig
Entries 600156
Mean 1.872e+04
RMS 12.92
Underflow 5.709e+05
Overflow 0
10^4
10^3
10^2
10
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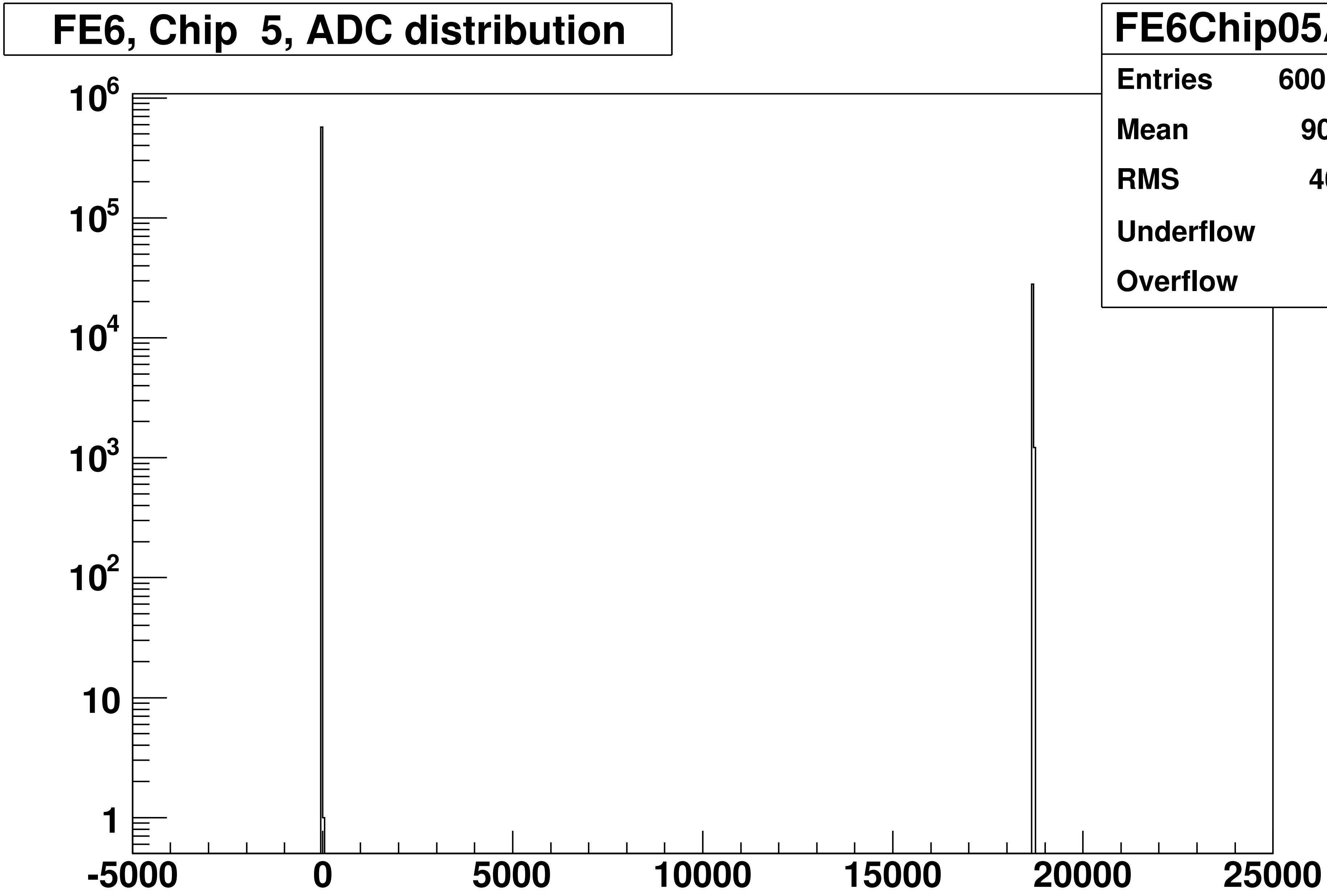
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE6, Chip 5, ADC distribution
FE6Chip05All
Entries 600156
Mean 902.2
RMS 4018
Underflow 0
Overflow 0
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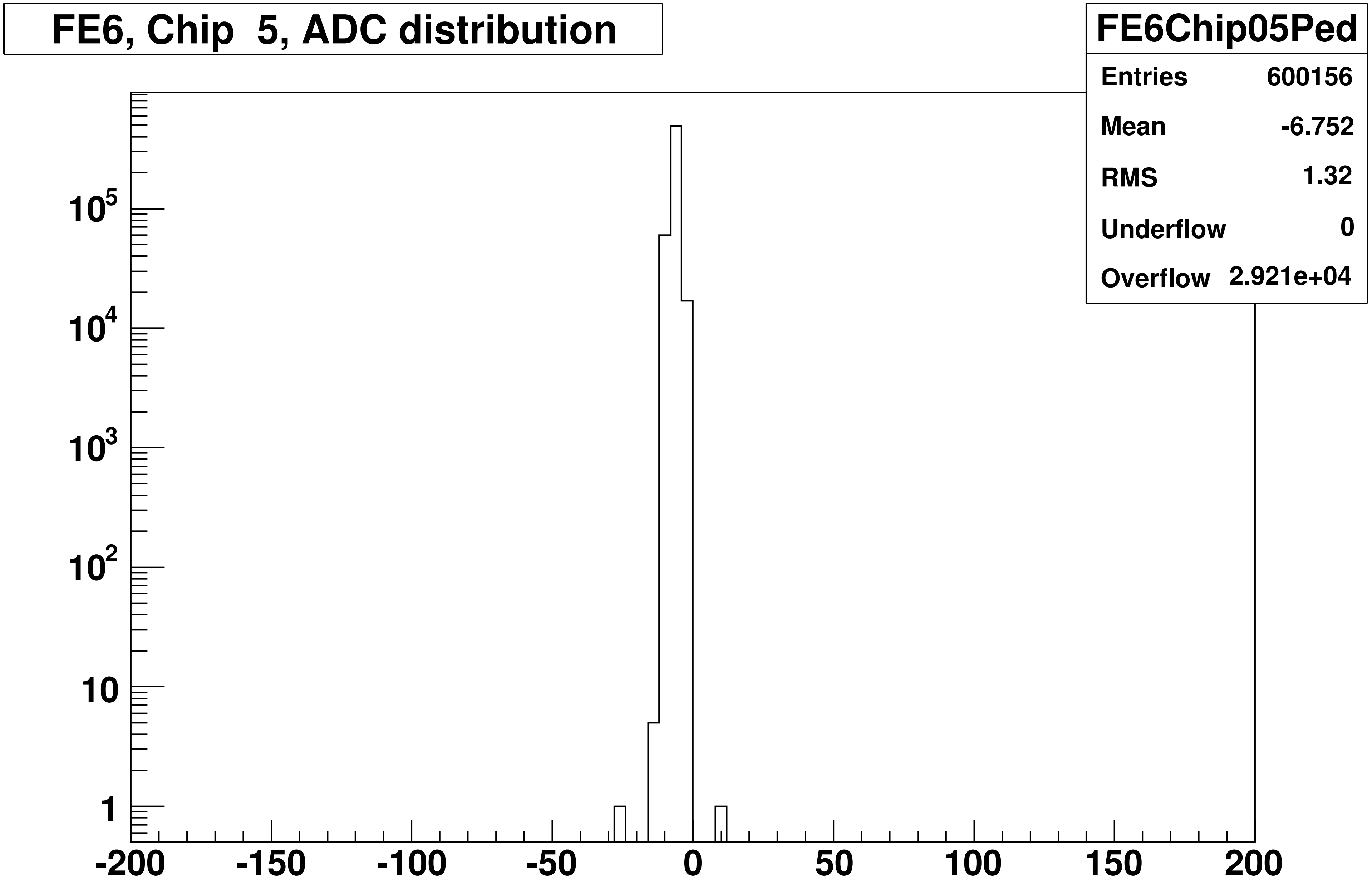

FE6, Chip 5, ADC distribution
FE6Chip05Ped
Entries 600156
Mean -6.752
RMS 1.32
Underflow 0
Overflow 2.921e+04
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10^3
10^2
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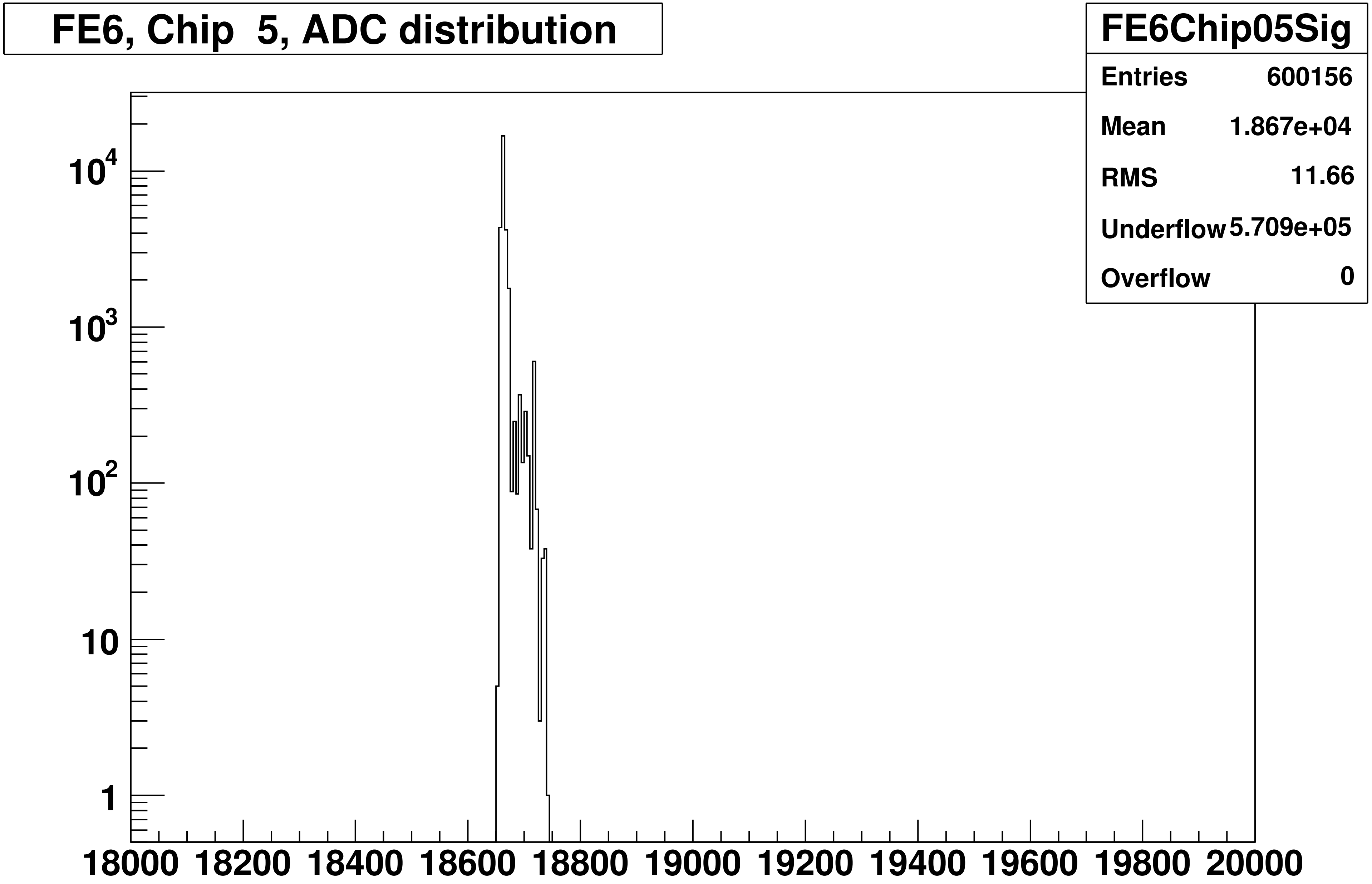
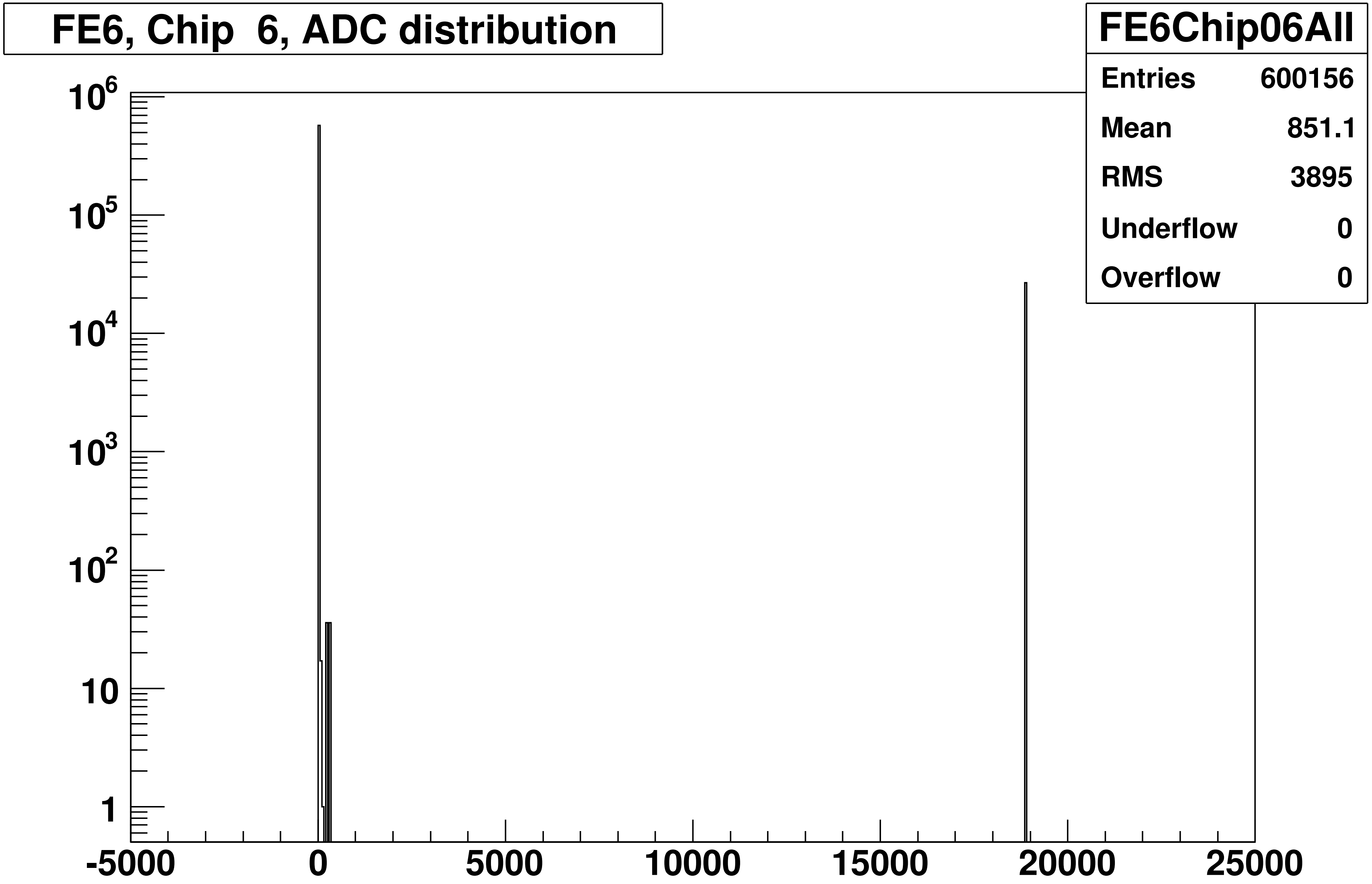
150
200


FE6, Chip 5, ADC distribution
FE6Chip05Sig
Entries 600156
Mean 1.867e+04
RMS 11.66
Underflow 5.709e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE6, Chip 6, ADC distribution
FE6Chip06All
Entries 600156
Mean 851.1
RMS 3895
Underflow 0
Overflow 0
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10^4
10^3
10^2
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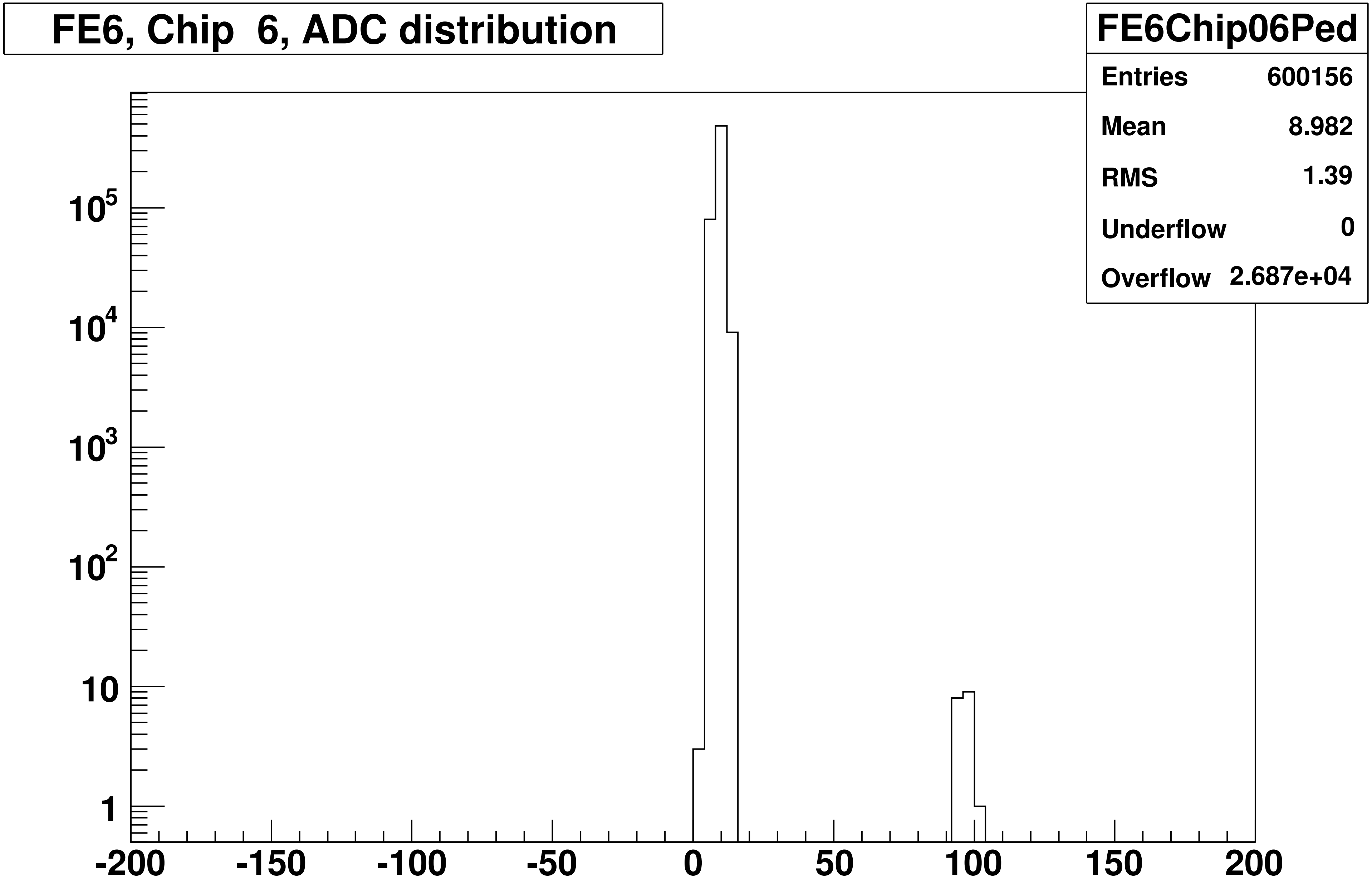

FE6, Chip 6, ADC distribution
FE6Chip06Ped
Entries 600156
Mean 8.982
RMS 1.39
Underflow 0
Overflow 2.687e+04
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10^4
10^3
10^2
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1
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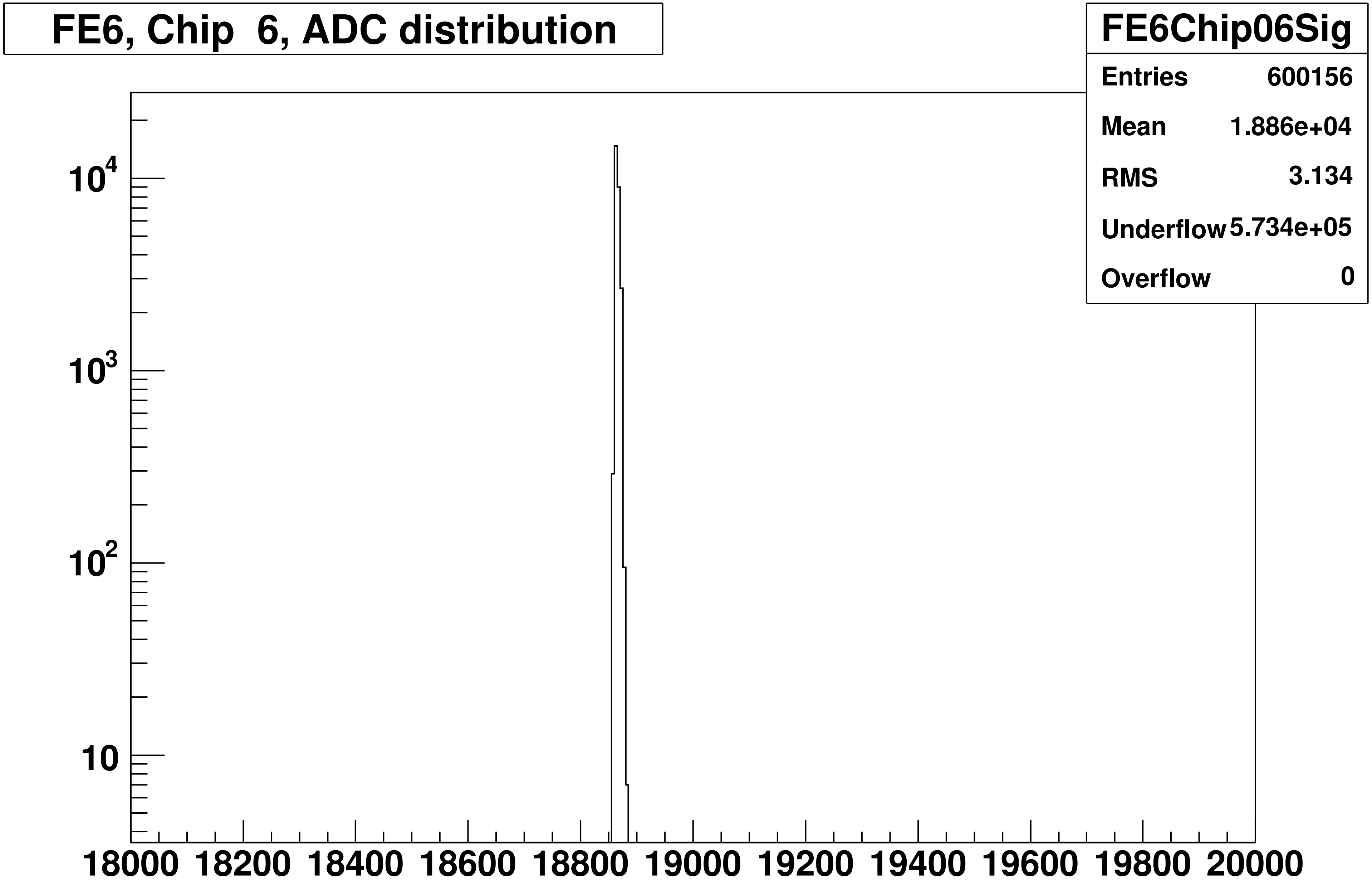
150
200


FE6, Chip 6, ADC distribution
FE6Chip06Sig
Entries 600156
Mean 1.886e+04
RMS 3.134
Underflow 5.734e+05
Overflow 0
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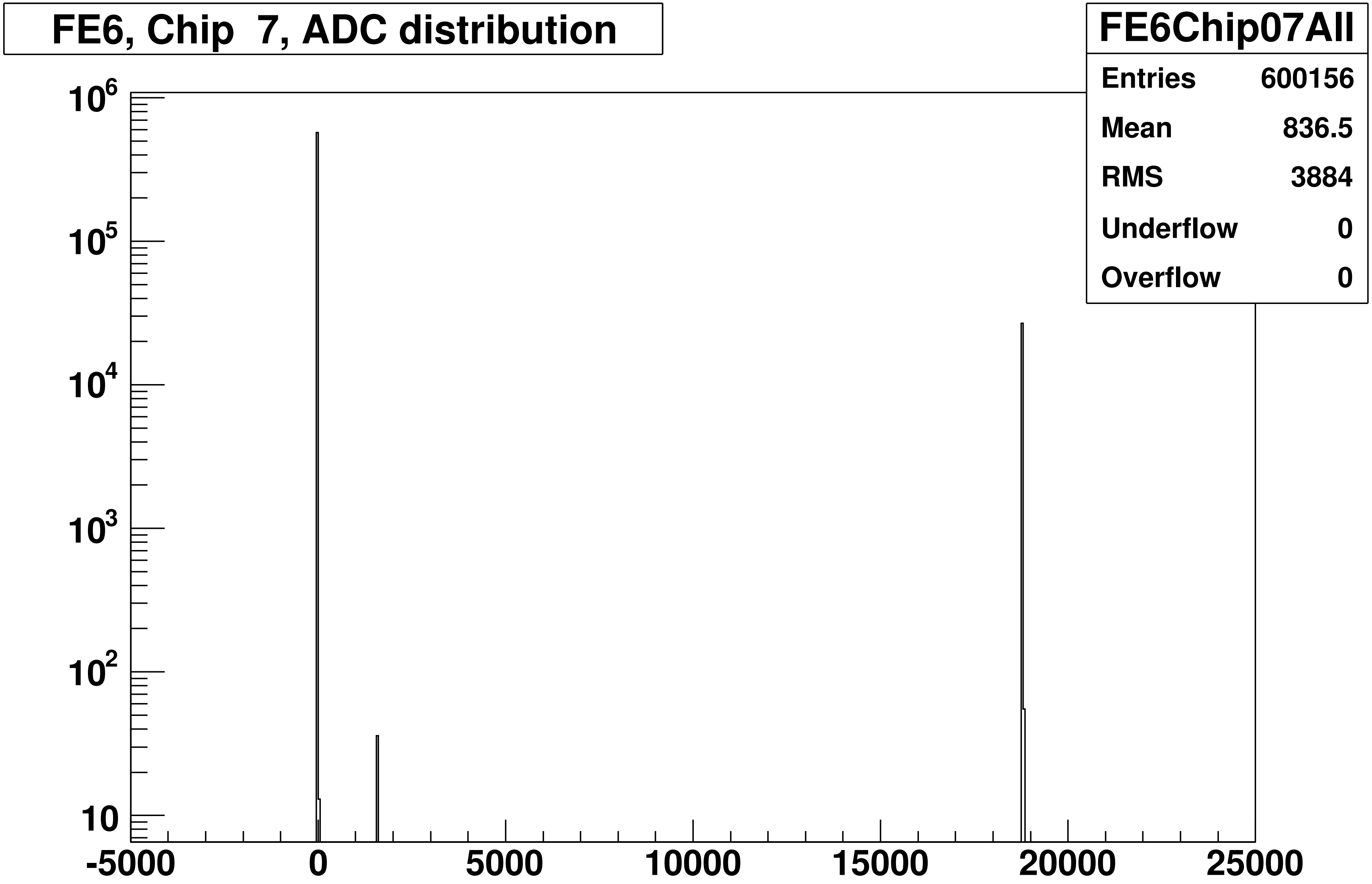
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE6, Chip 7, ADC distribution
FE6Chip07All
Entries 600156
Mean 836.5
RMS 3884
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
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0
5000
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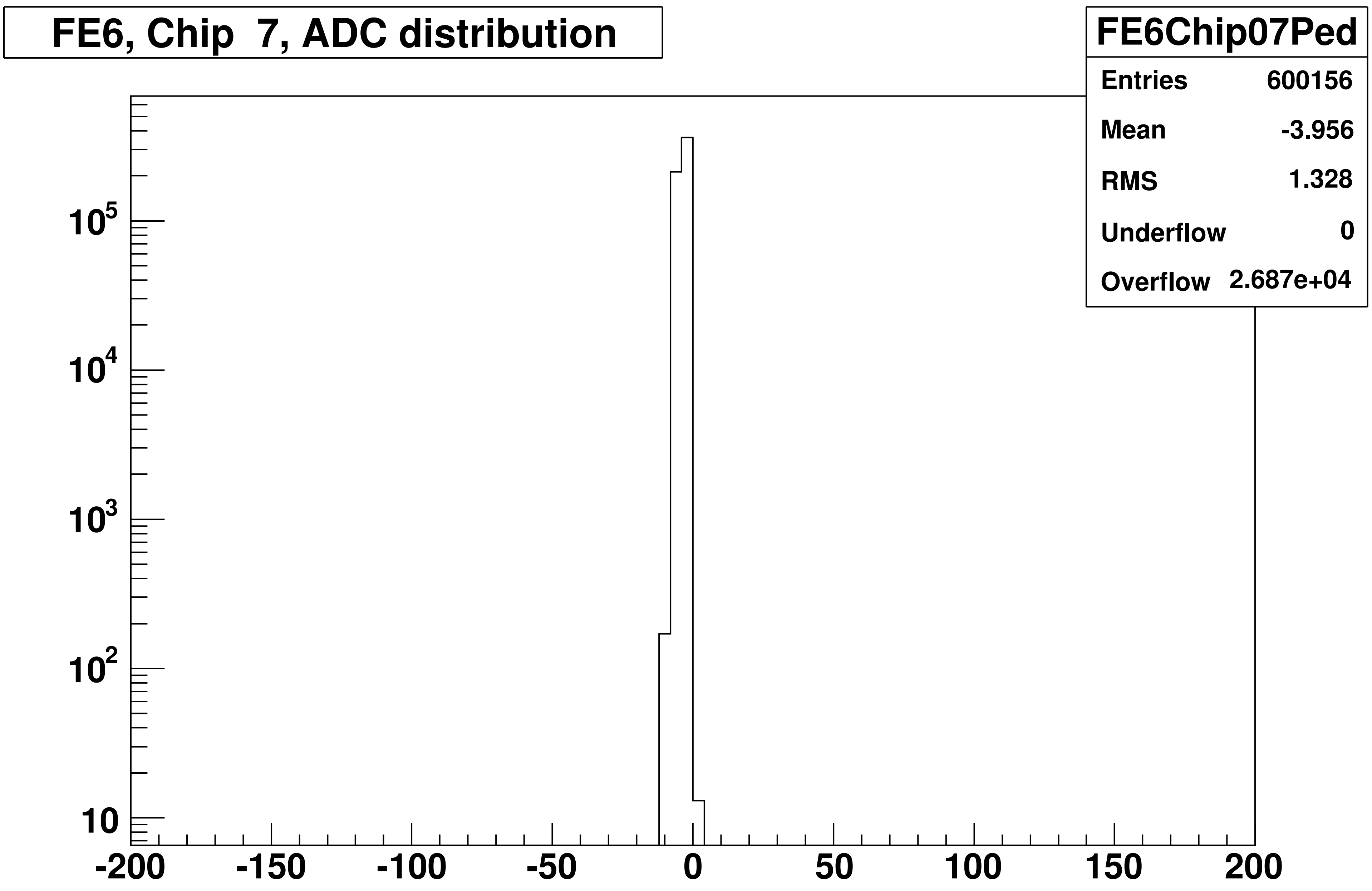
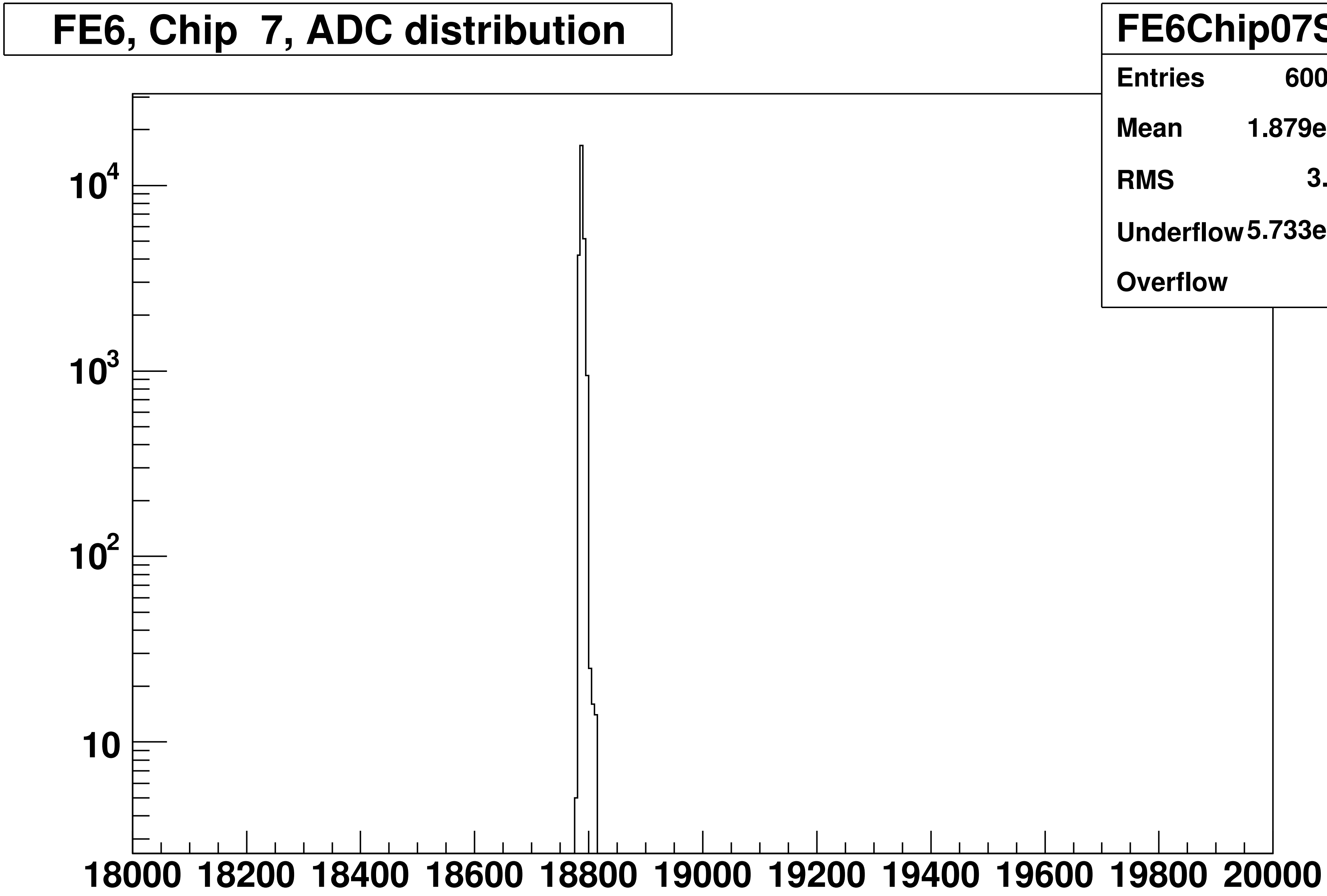
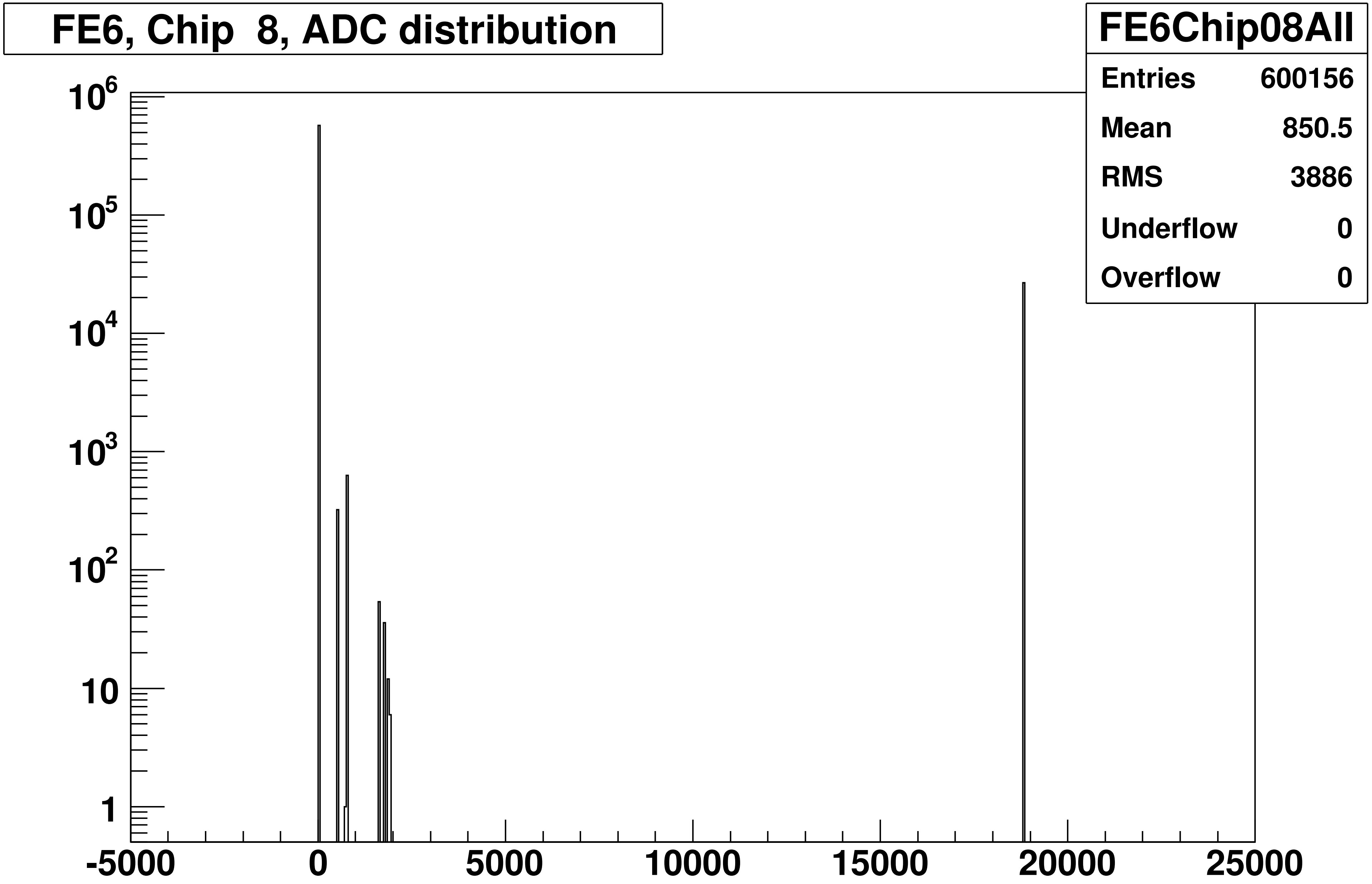
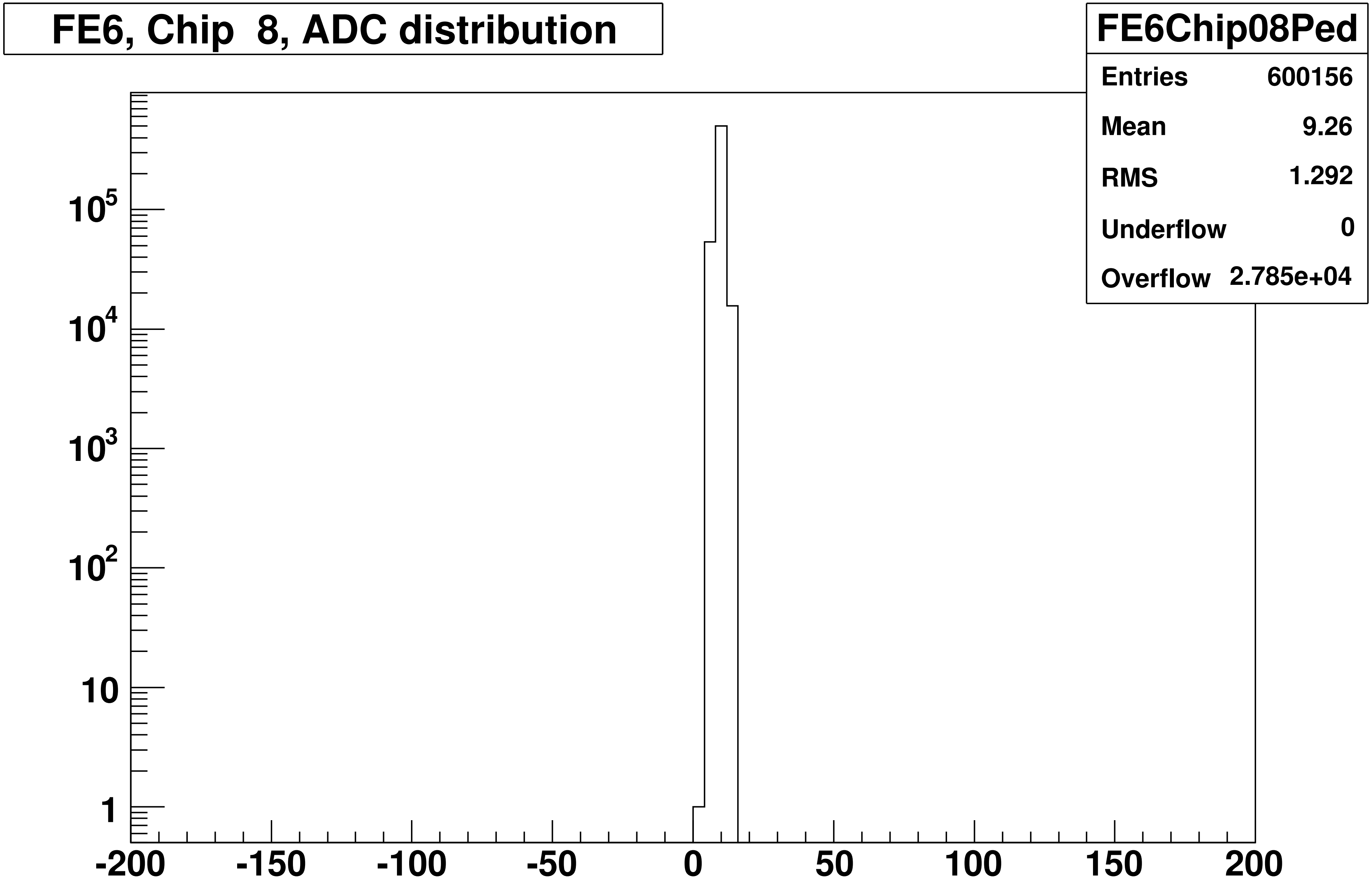
25000


FE6, Chip 7, ADC distribution
FE6Chip07Ped
Entries 600156
Mean -3.956
RMS 1.328
Underflow 0
Overflow 2.687e+04
10^5
10^4
10^3
10^2
10
-200
-150
-100
-50
0
50
100
150
200


FE6, Chip 7, ADC distribution
FE6Chip07Sig
Entries 600156
Mean 1.879e+04
RMS 3.234
Underflow 5.733e+05
Overflow 0
10^4
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE6, Chip 8, ADC distribution
FE6Chip08All
Entries 600156
Mean 850.5
RMS 3886
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE6, Chip 8, ADC distribution
FE6Chip08Ped
Entries 600156
Mean 9.26
RMS 1.292
Underflow 0
Overflow 2.785e+04
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10^4
10^3
10^2
10
1
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-150
-100
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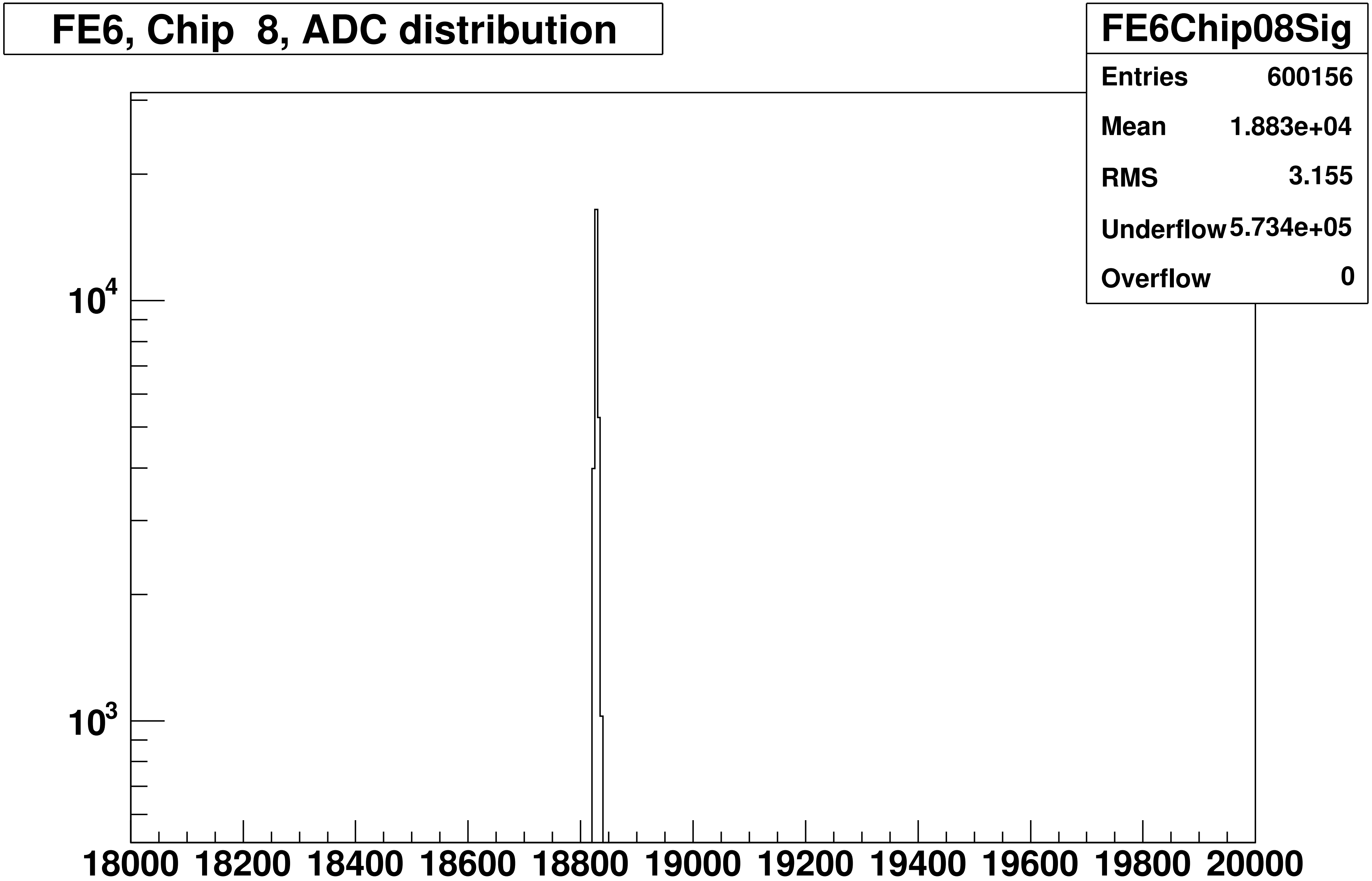
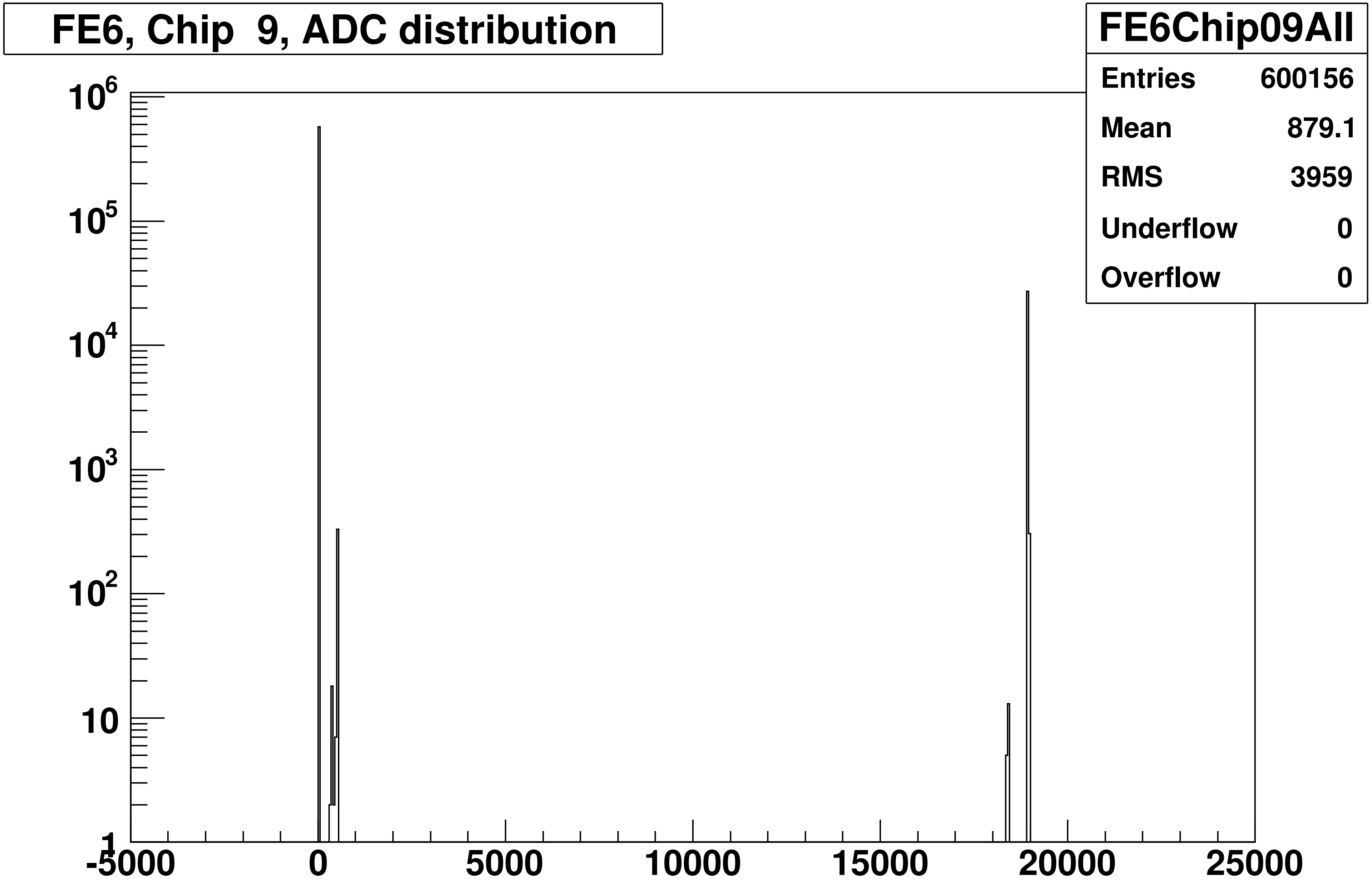
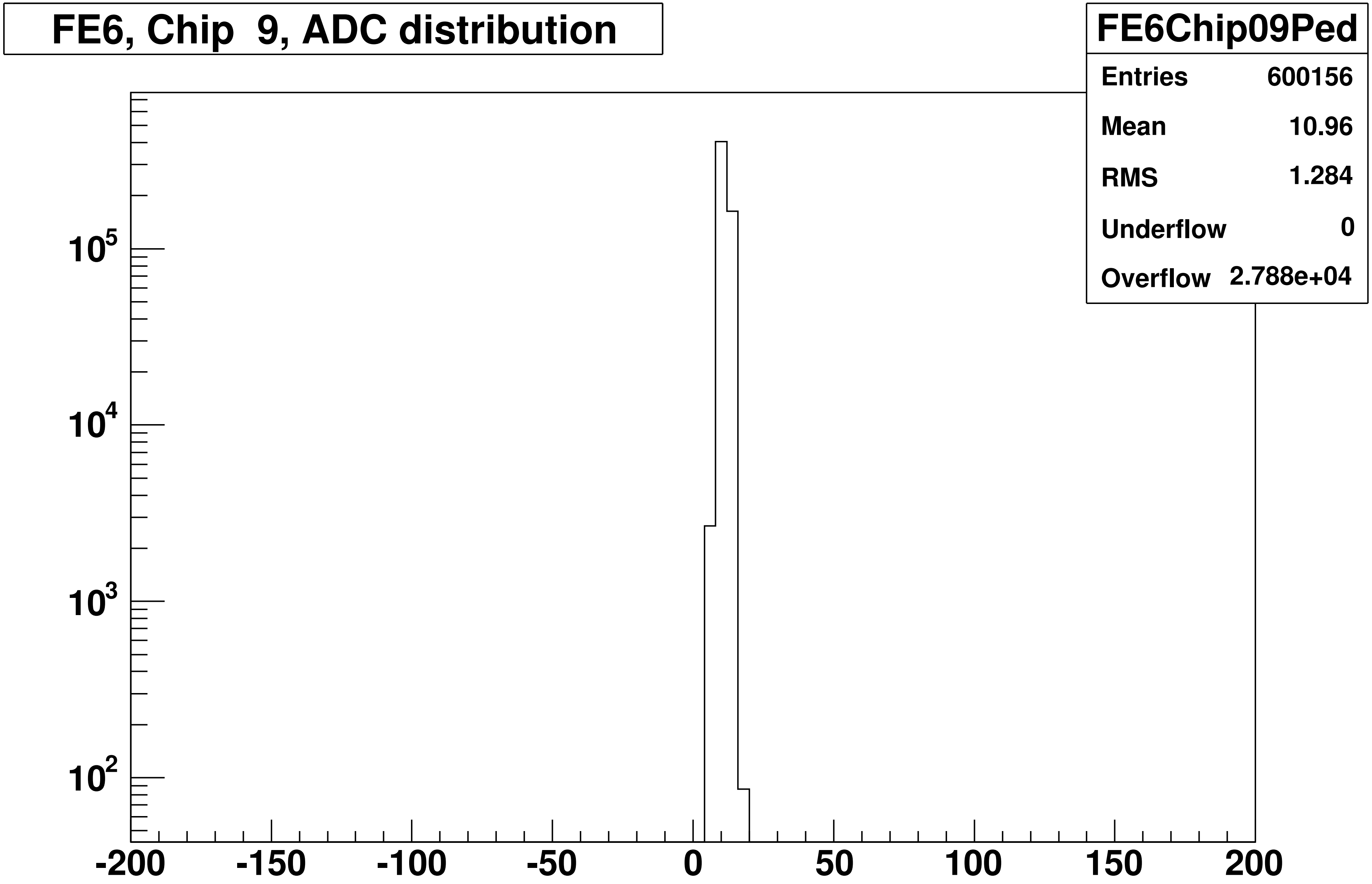
0
50
100
150
200


FE6, Chip 8, ADC distribution
FE6Chip08Sig
Entries 600156
Mean 1.883e+04
RMS 3.155
Underflow 5.734e+05
Overflow 0
10^4
10^3
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE6, Chip 9, ADC distribution
FE6Chip09All
Entries 600156
Mean 879.1
RMS 3959
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE6, Chip 9, ADC distribution
FE6Chip09Ped
Entries 600156
Mean 10.96
RMS 1.284
Underflow 0
Overflow 2.788e+04
10^5
10^4
10^3
10^2
-200
-150
-100
-50
0
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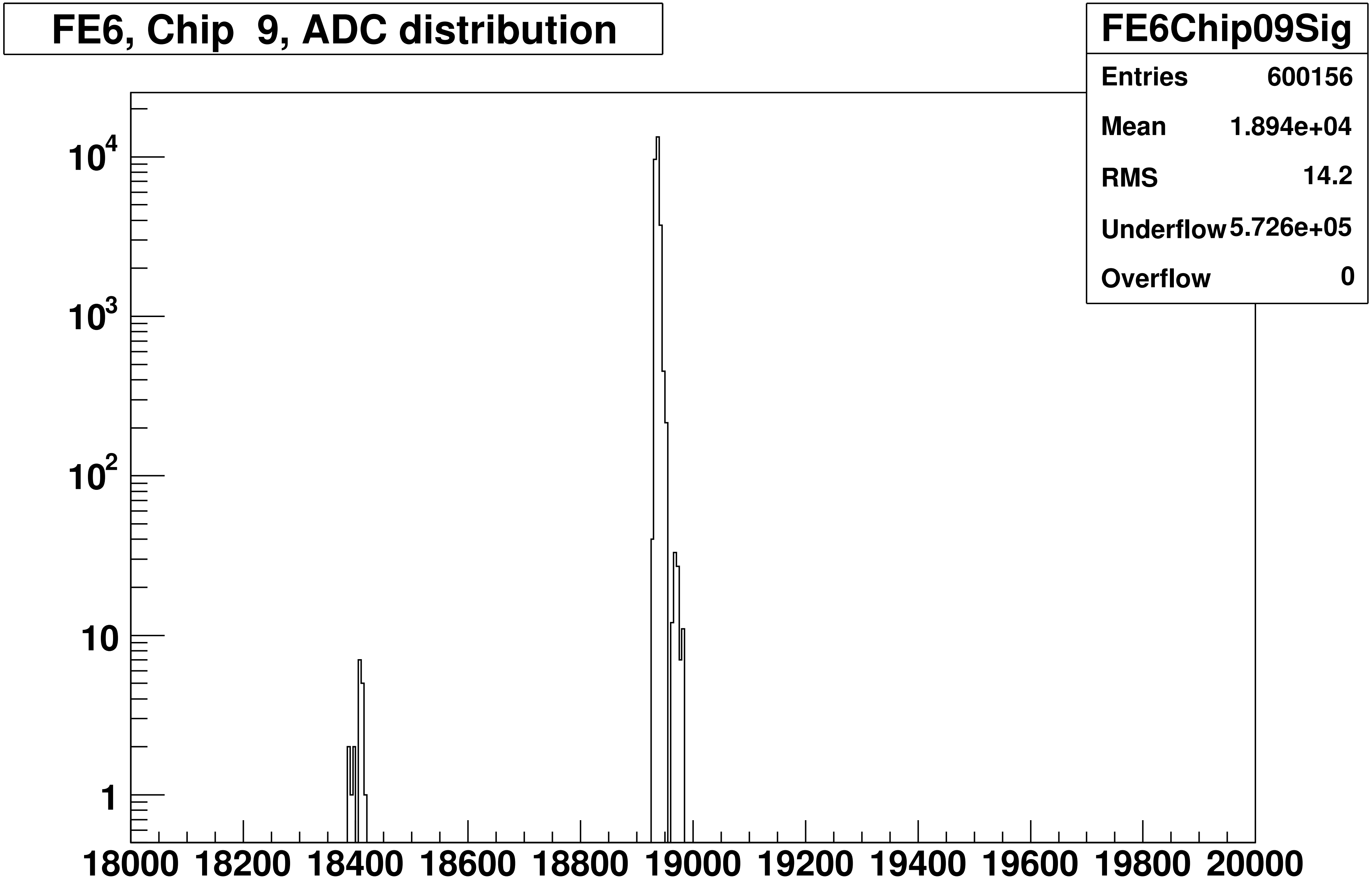
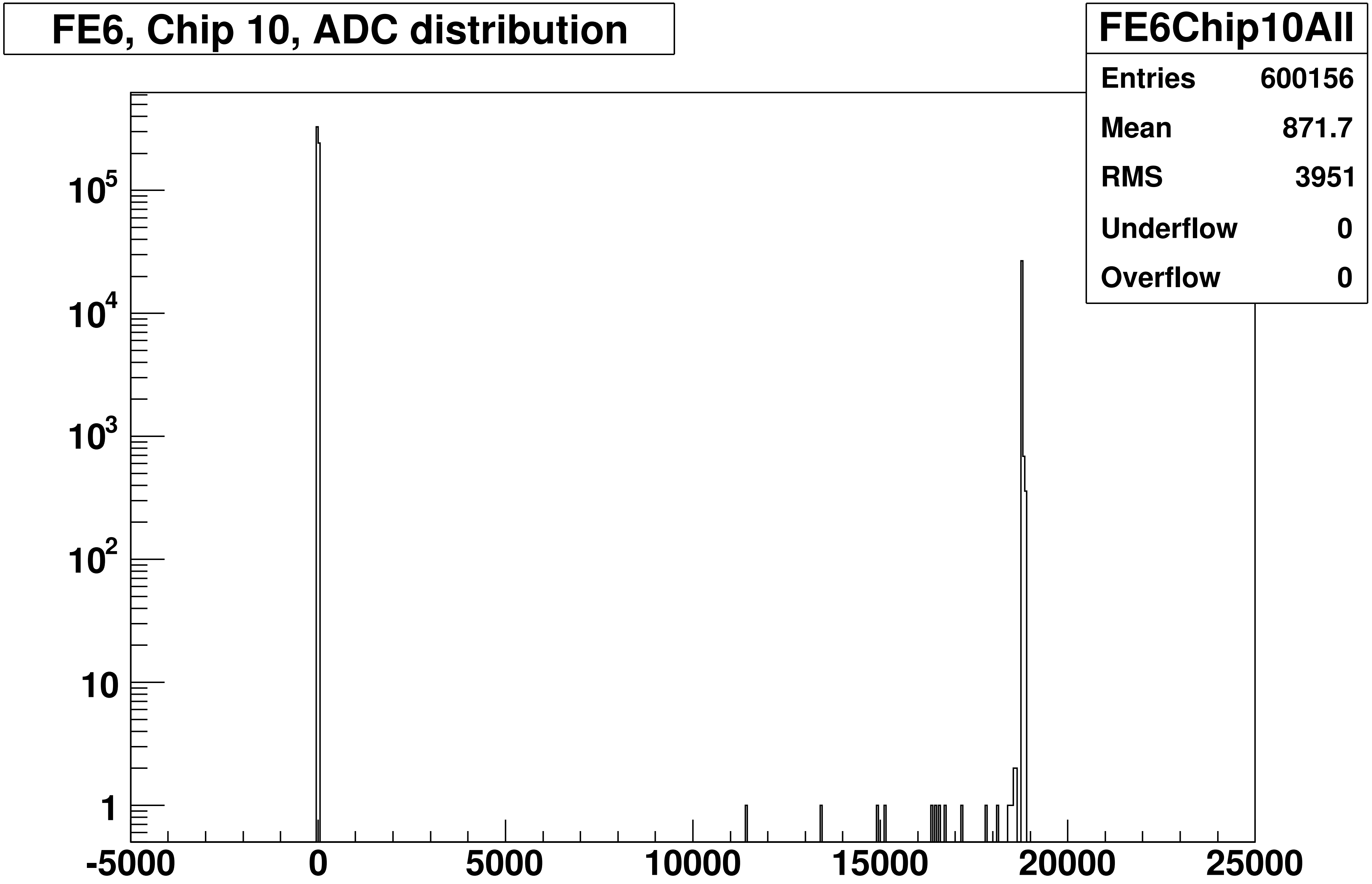
100
150
200


FE6, Chip 9, ADC distribution
FE6Chip09Sig
Entries 600156
Mean 1.894e+04
RMS 14.2
Underflow 5.726e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE6, Chip 10, ADC distribution
FE6Chip10All
Entries 600156
Mean 871.7
RMS 3951
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
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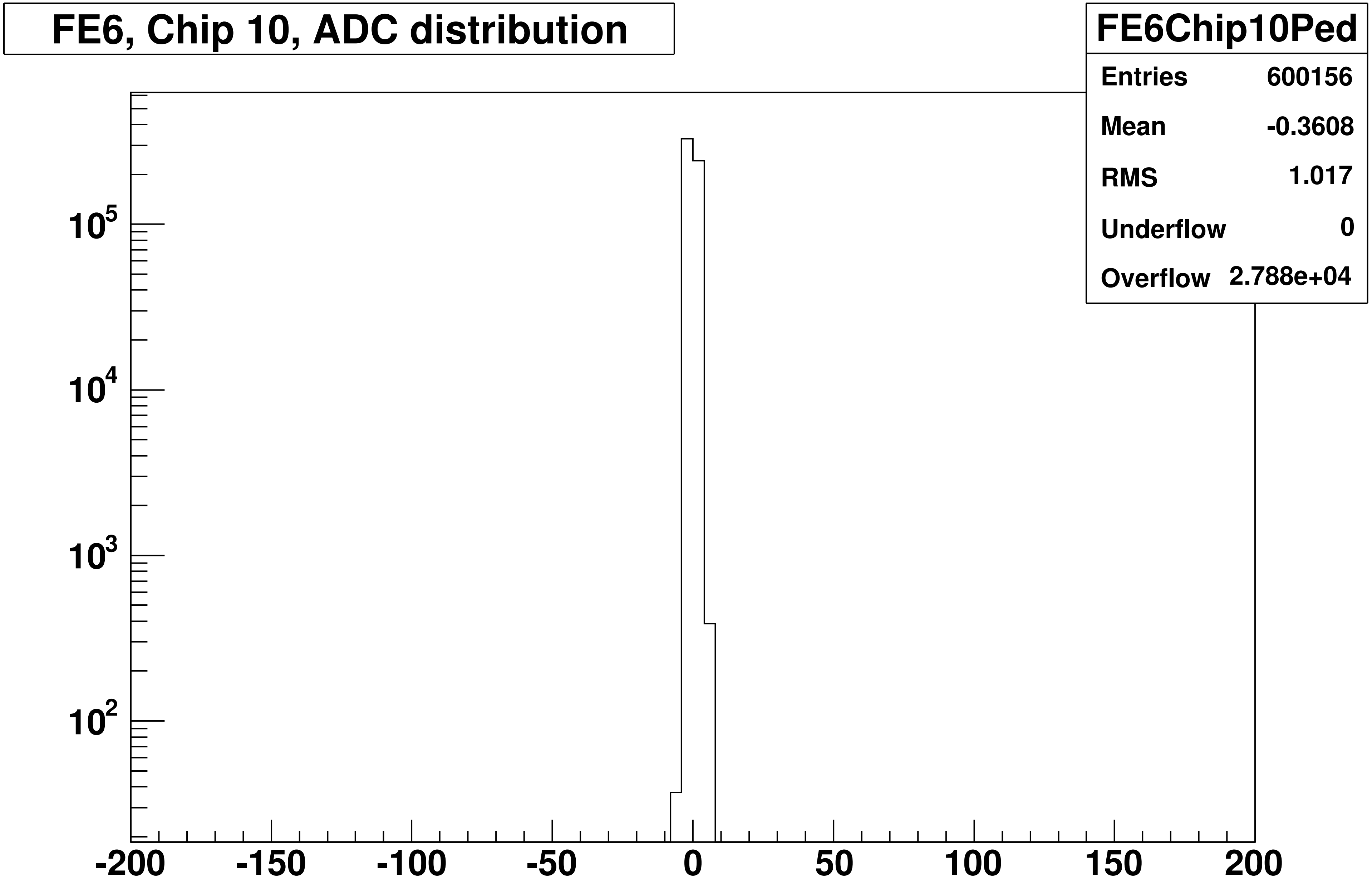
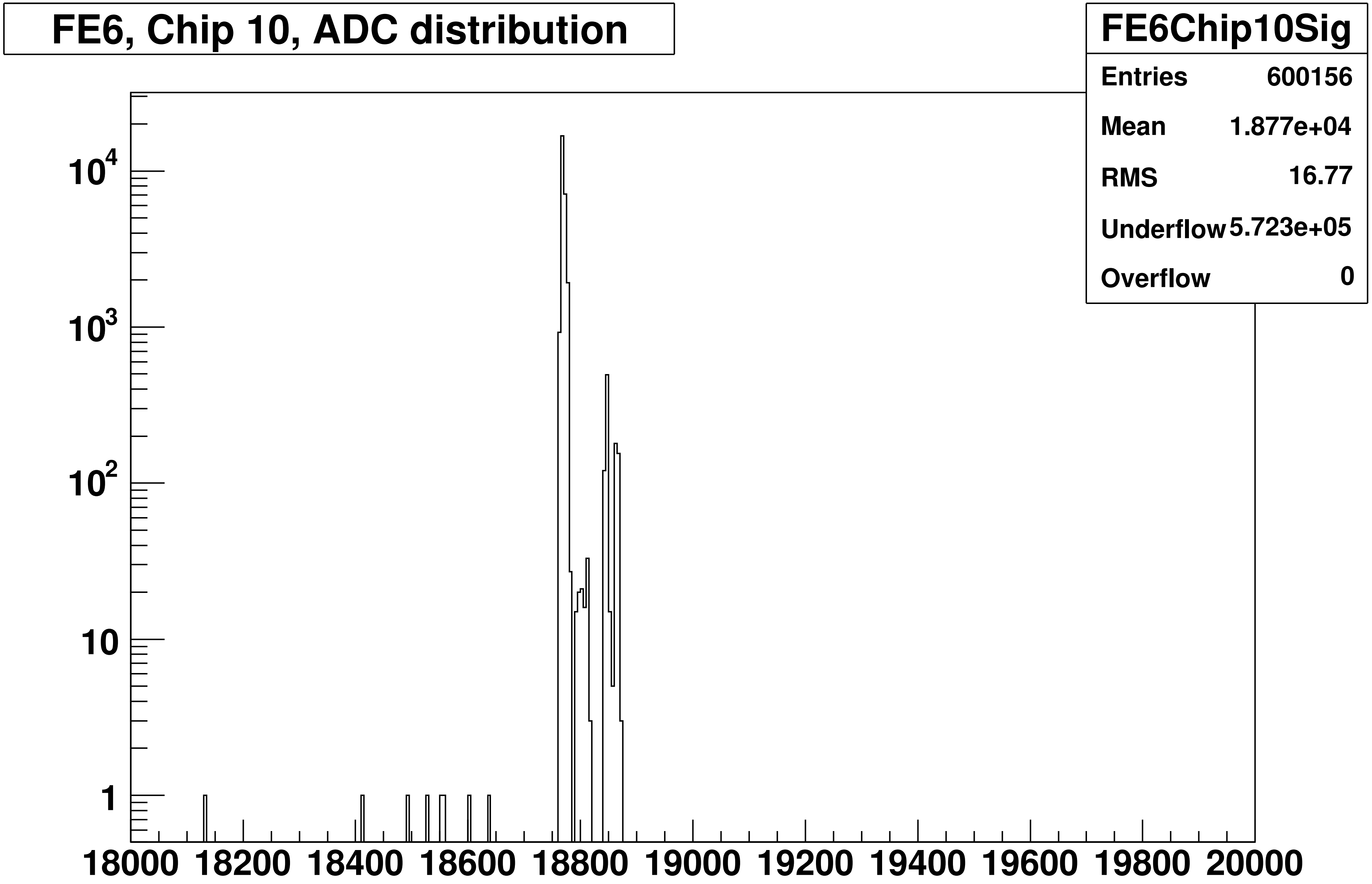
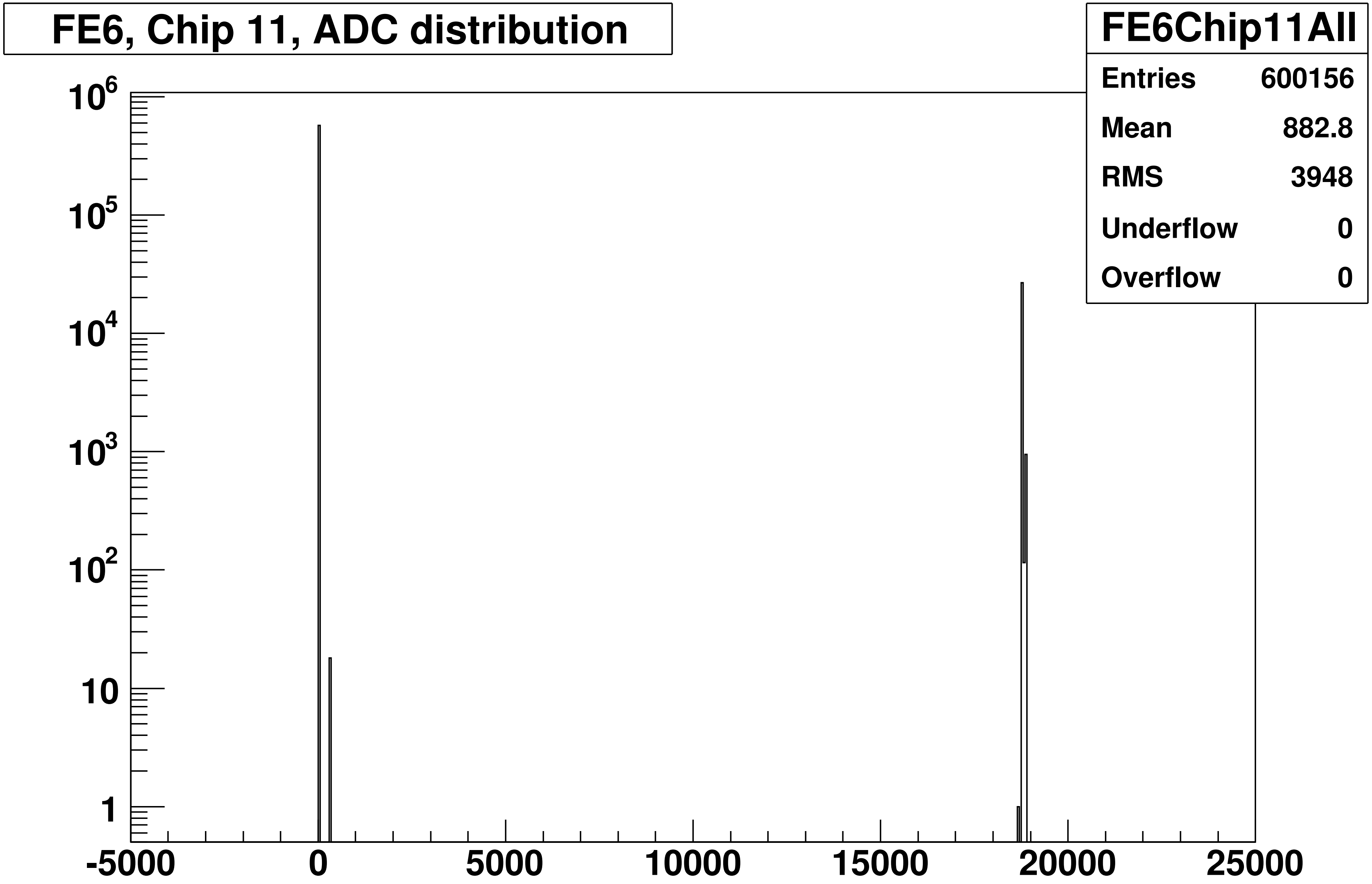
10000
15000
20000
25000



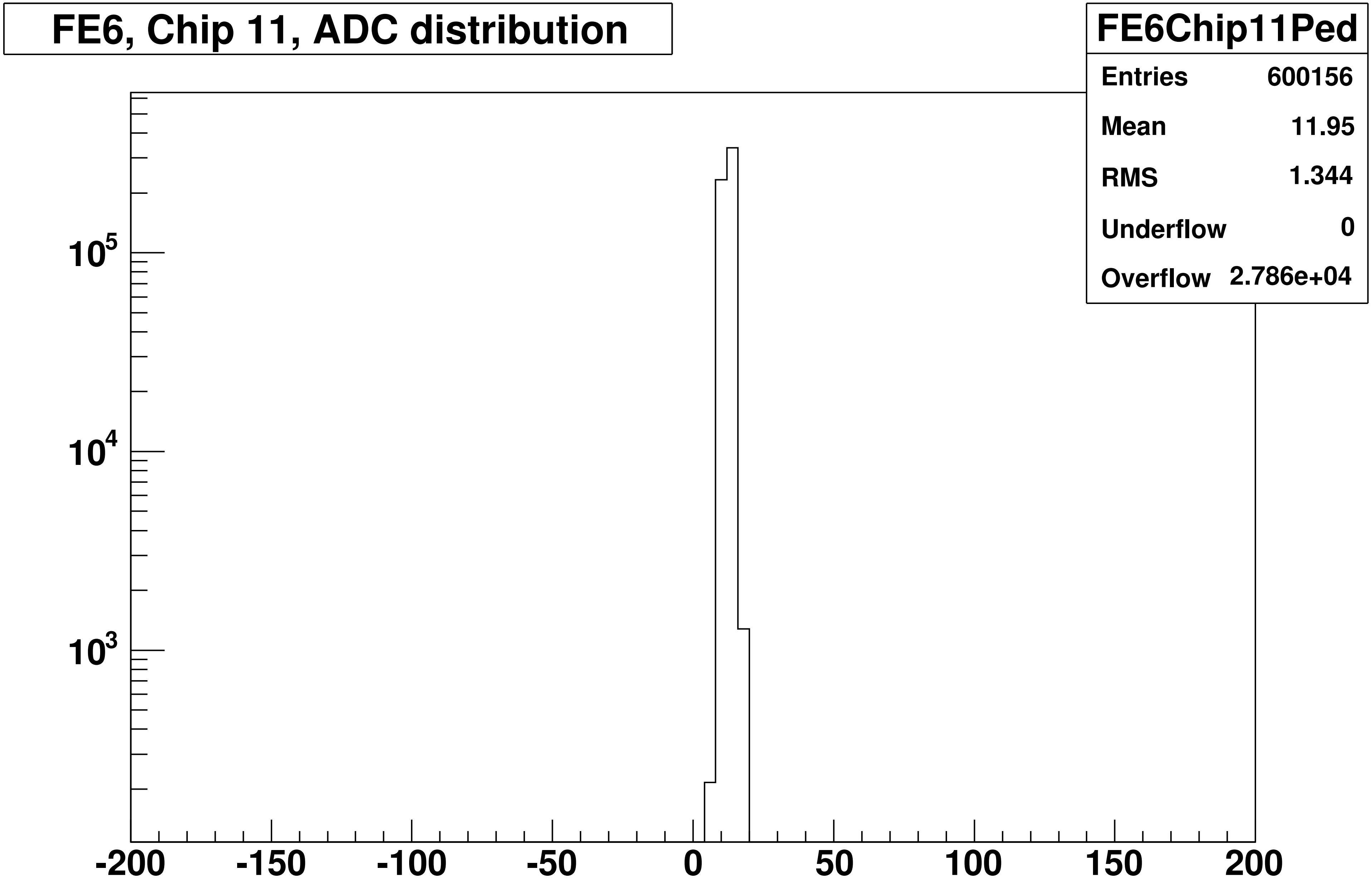
FE6, Chip 10, ADC distribution
FE6Chip10Ped
Entries 600156
Mean -0.3608
RMS 1.017
Underflow 0
Overflow 2.788e+04
10^5
10^4
10^3
10^2
-200 -150 -100 -50 0 50 100 150 200



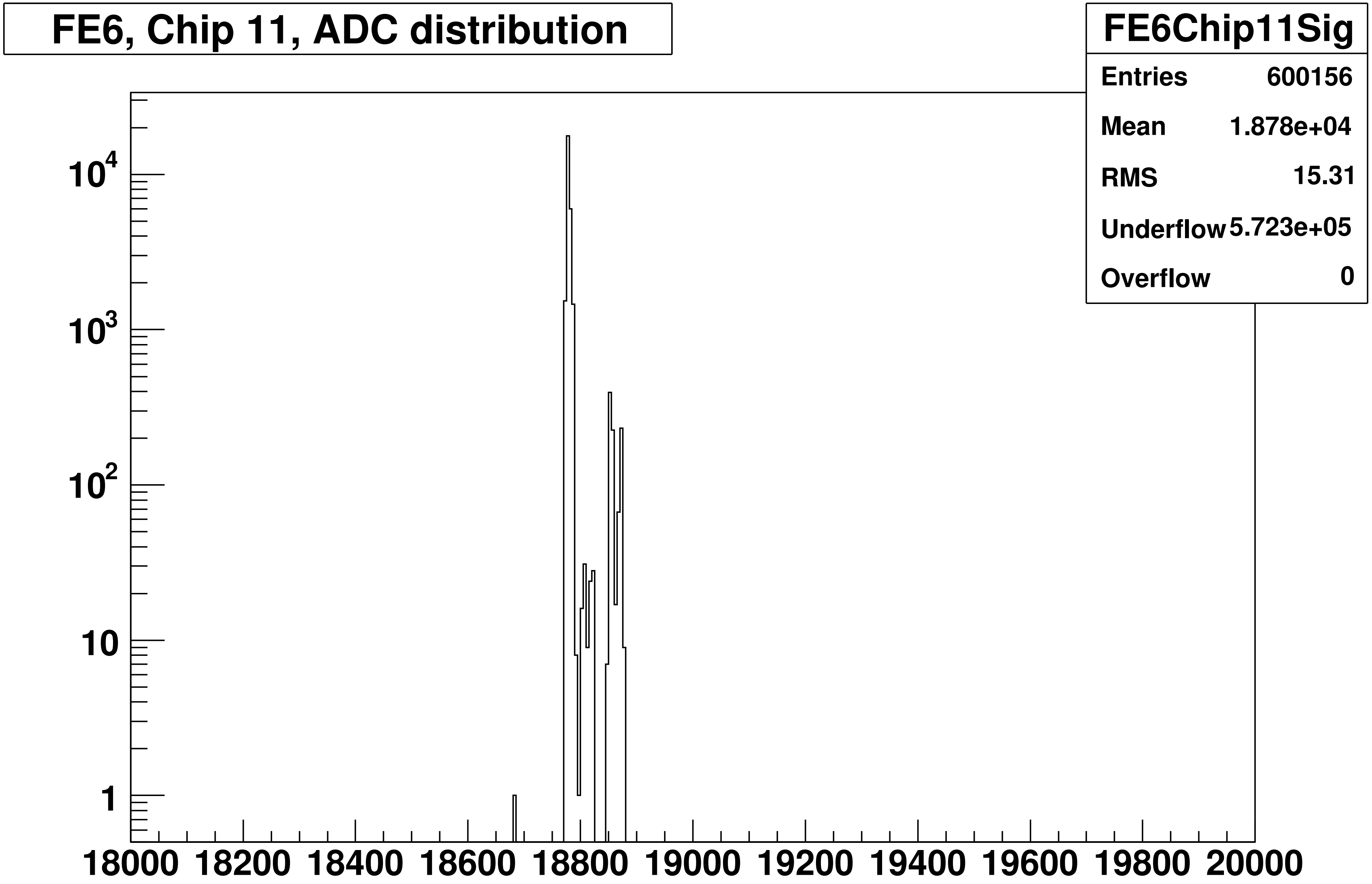
FE6, Chip 10, ADC distribution
FE6Chip10Sig
Entries 600156
Mean 1.877e+04
RMS 16.77
Underflow 5.723e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



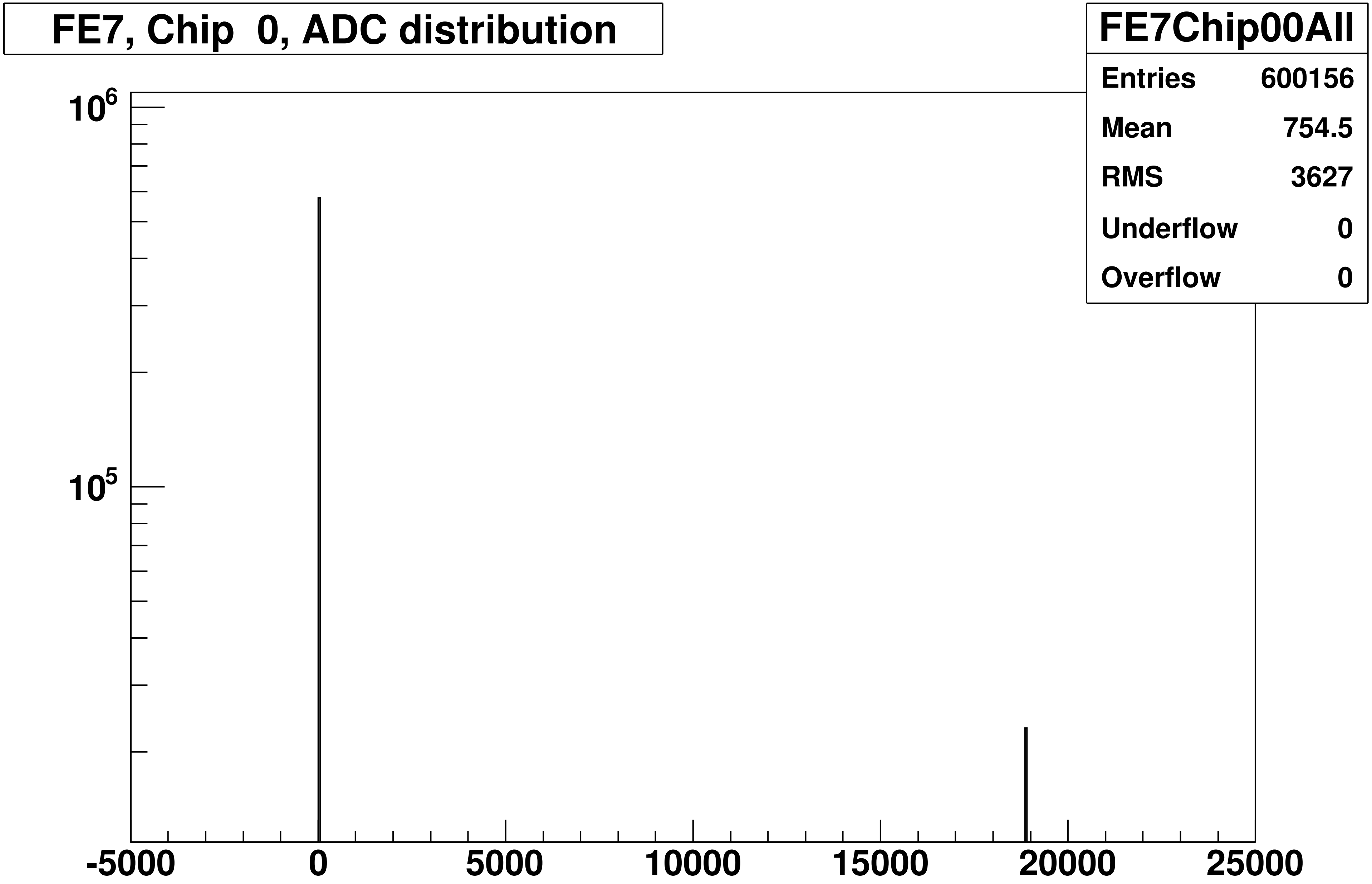
FE6, Chip 11, ADC distribution
FE6Chip11All
Entries 600156
Mean 882.8
RMS 3948
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



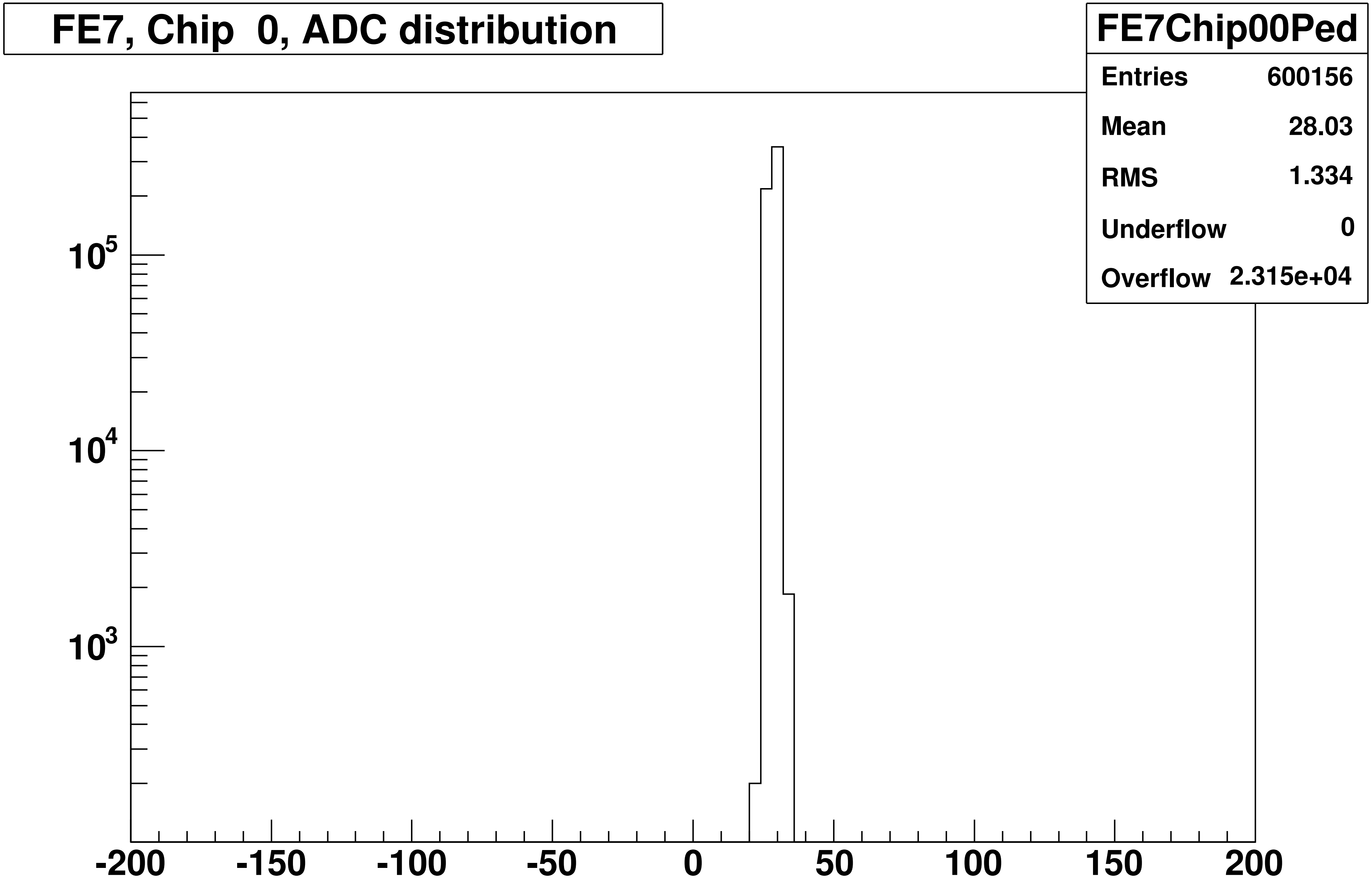
FE6, Chip 11, ADC distribution
FE6Chip11Ped
Entries 600156
Mean 11.95
RMS 1.344
Underflow 0
Overflow 2.786e+04
10^5
10^4
10^3
-200
-150
-100
-50
0
50
100
150
200

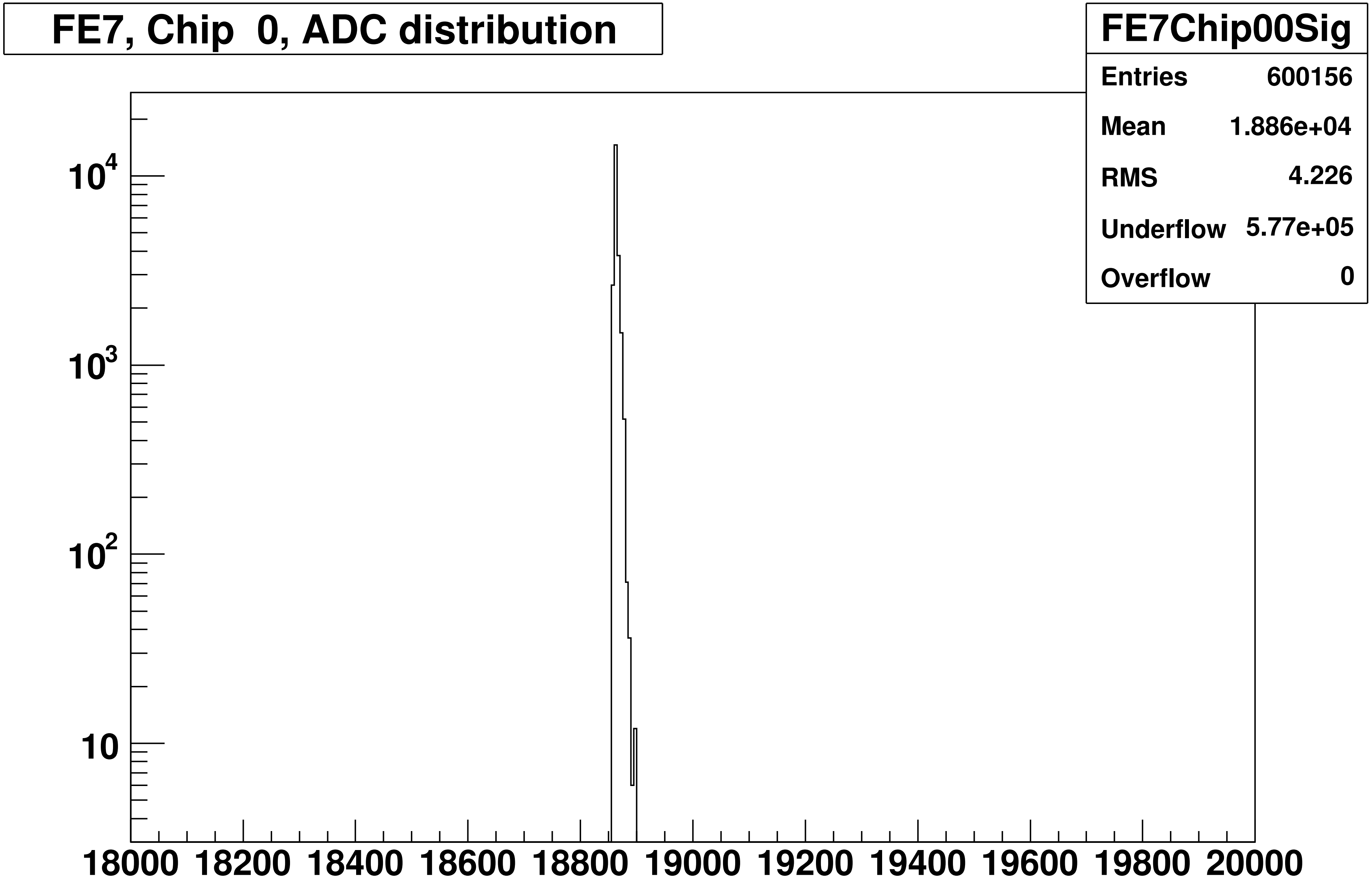


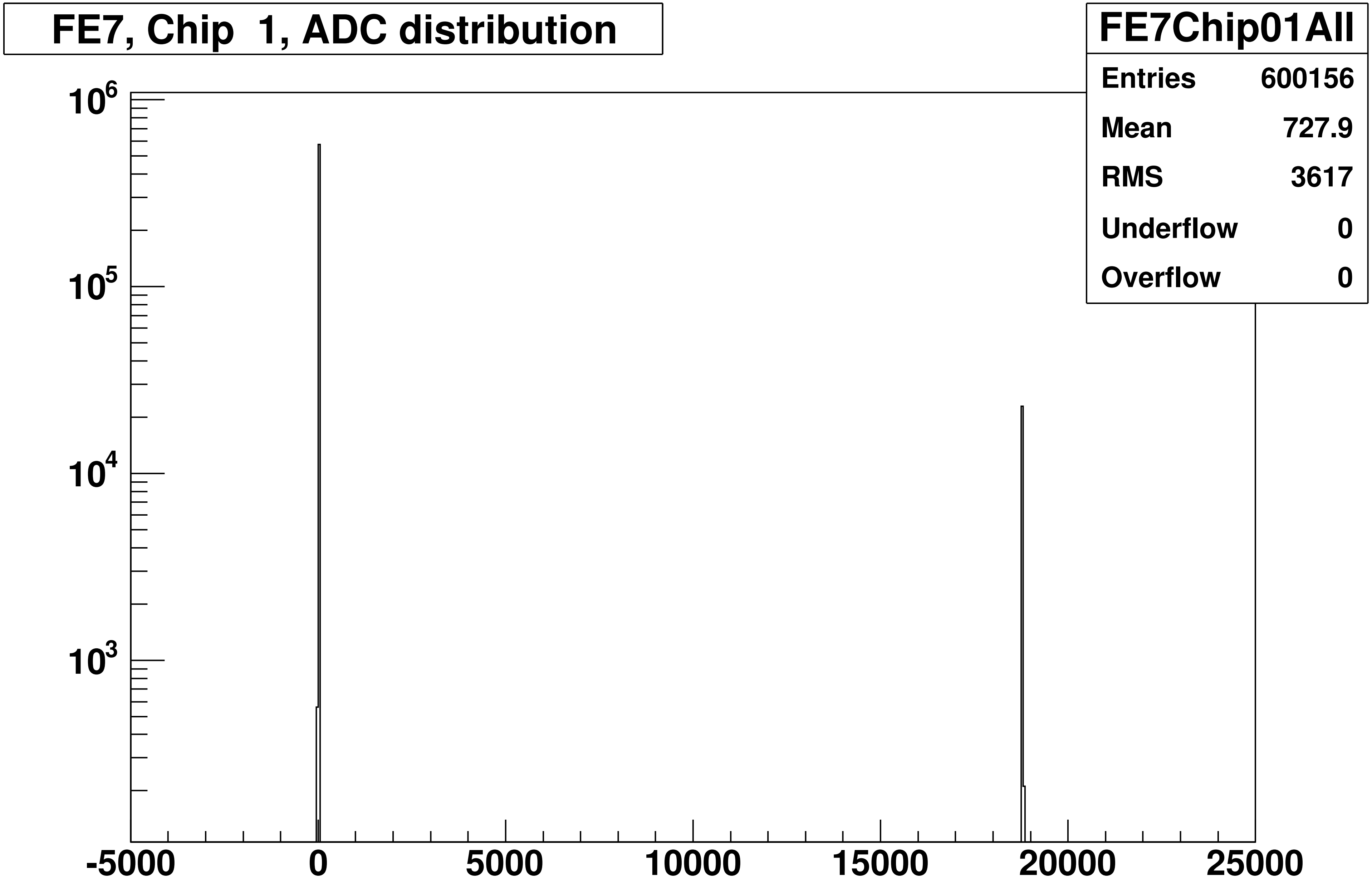
FE6, Chip 11, ADC distribution
FE6Chip11Sig
Entries 600156
Mean 1.878e+04
RMS 15.31
Underflow 5.723e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000

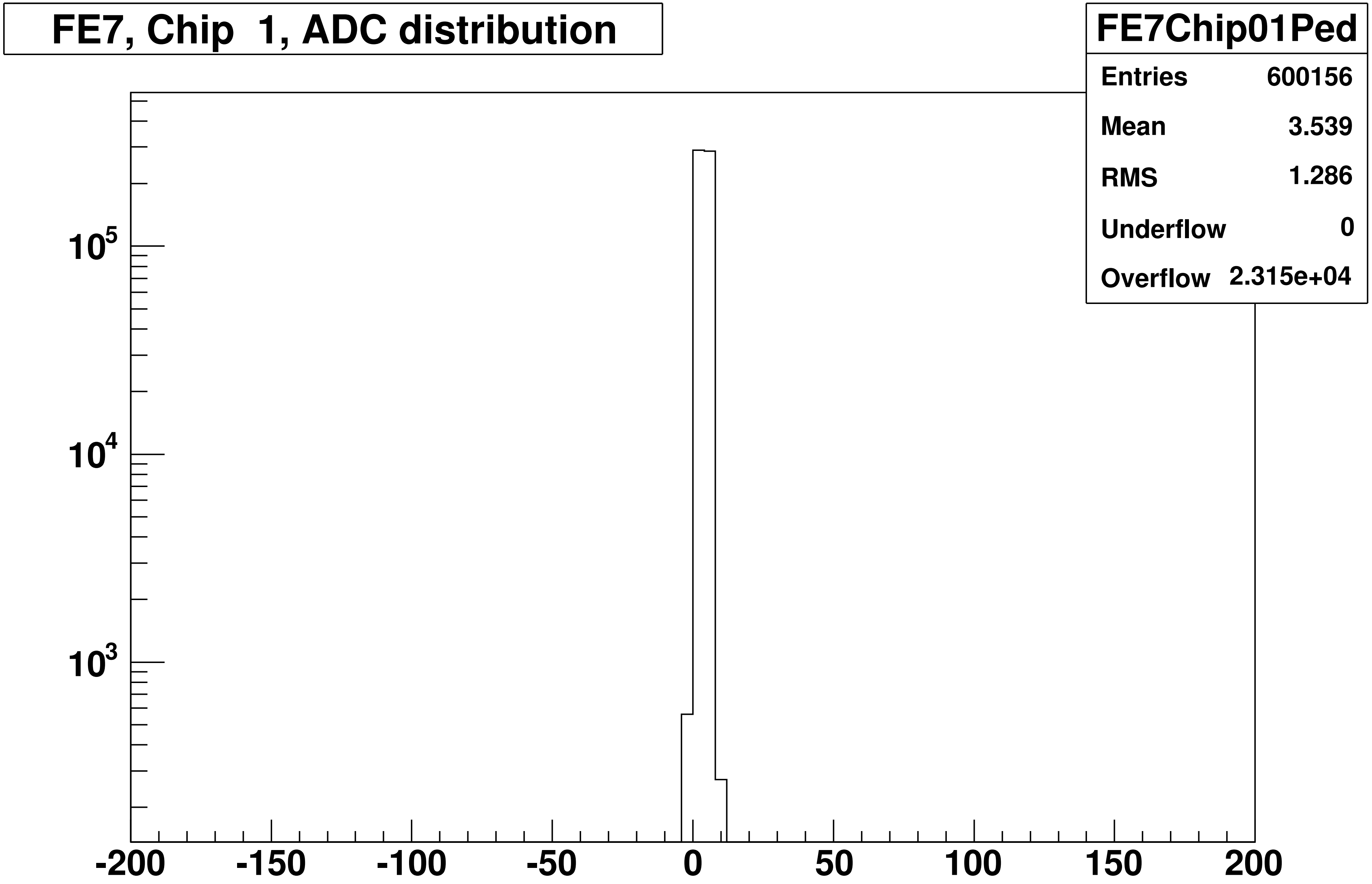


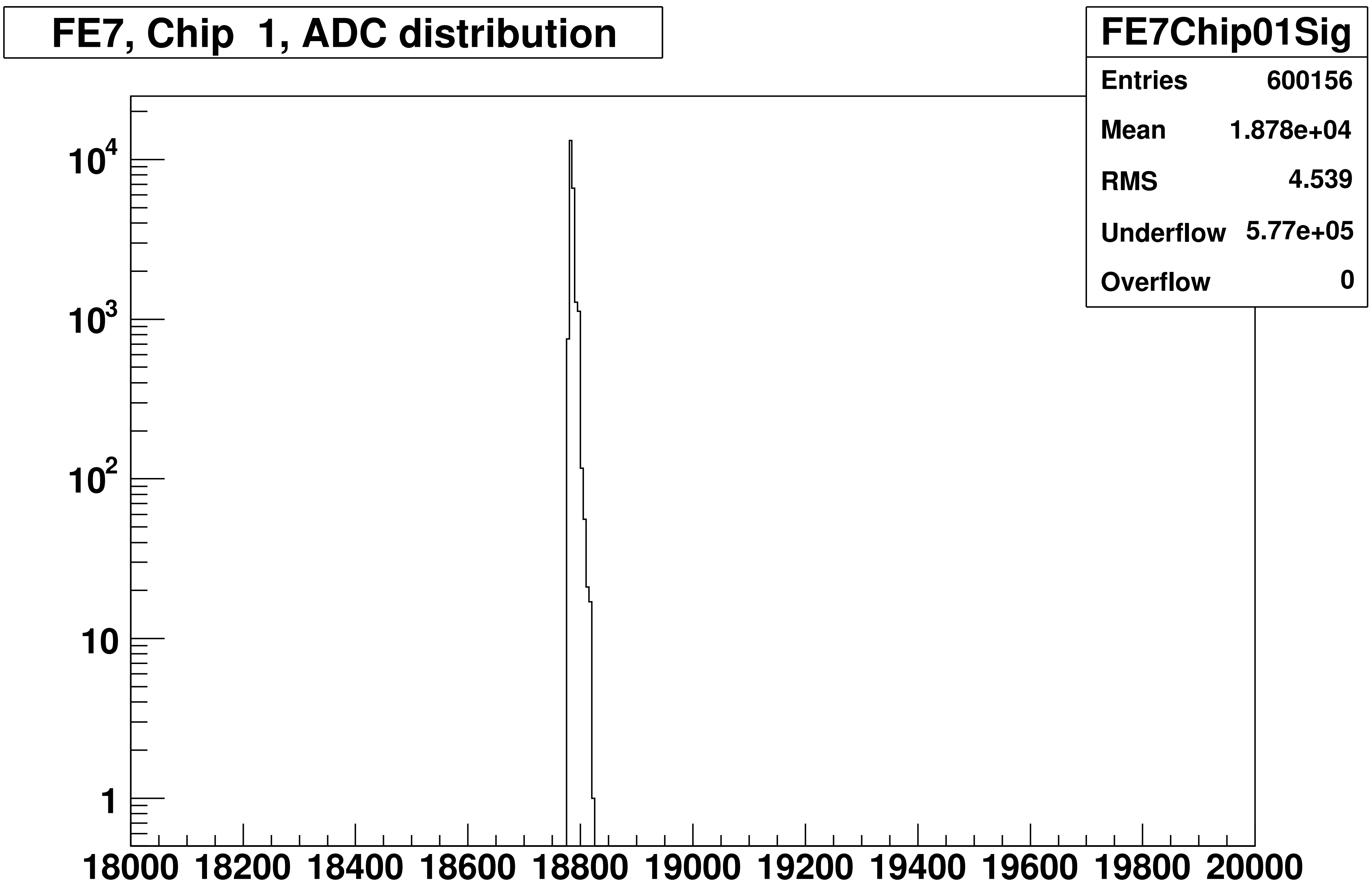
FE7, Chip 0, ADC distribution
FE7Chip00All
Entries 600156
Mean 754.5
RMS 3627
Underflow 0
Overflow 0
10^6
10^5
-5000
0
5000
10000
15000
20000
25000

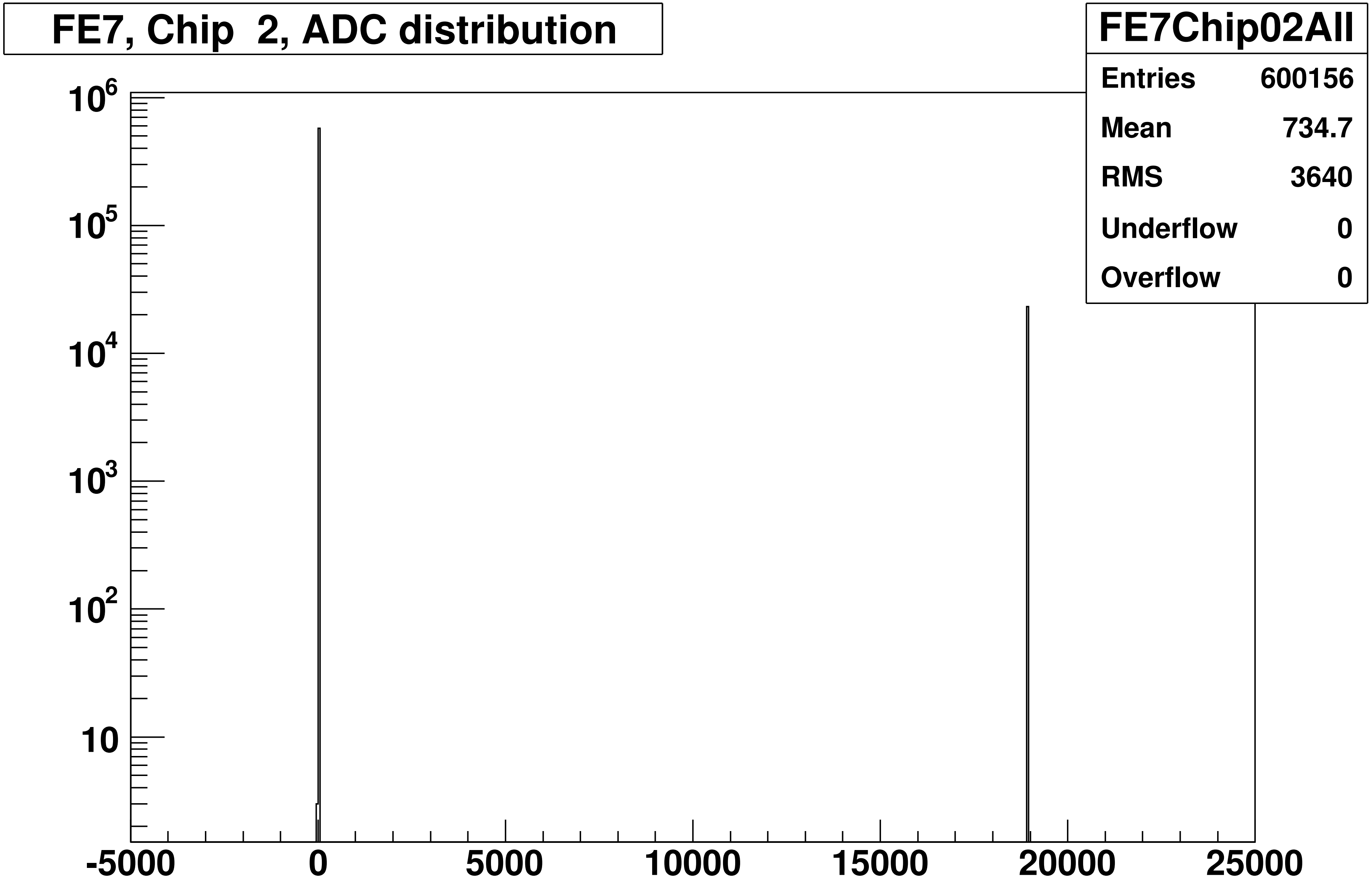

FE7, Chip 0, ADC distribution
FE7Chip00Ped
Entries 600156
Mean 28.03
RMS 1.334
Underflow 0
Overflow 2.315e+04
10^5
10^4
10^3
-200
-150
-100
-50
0
50
100
150
200

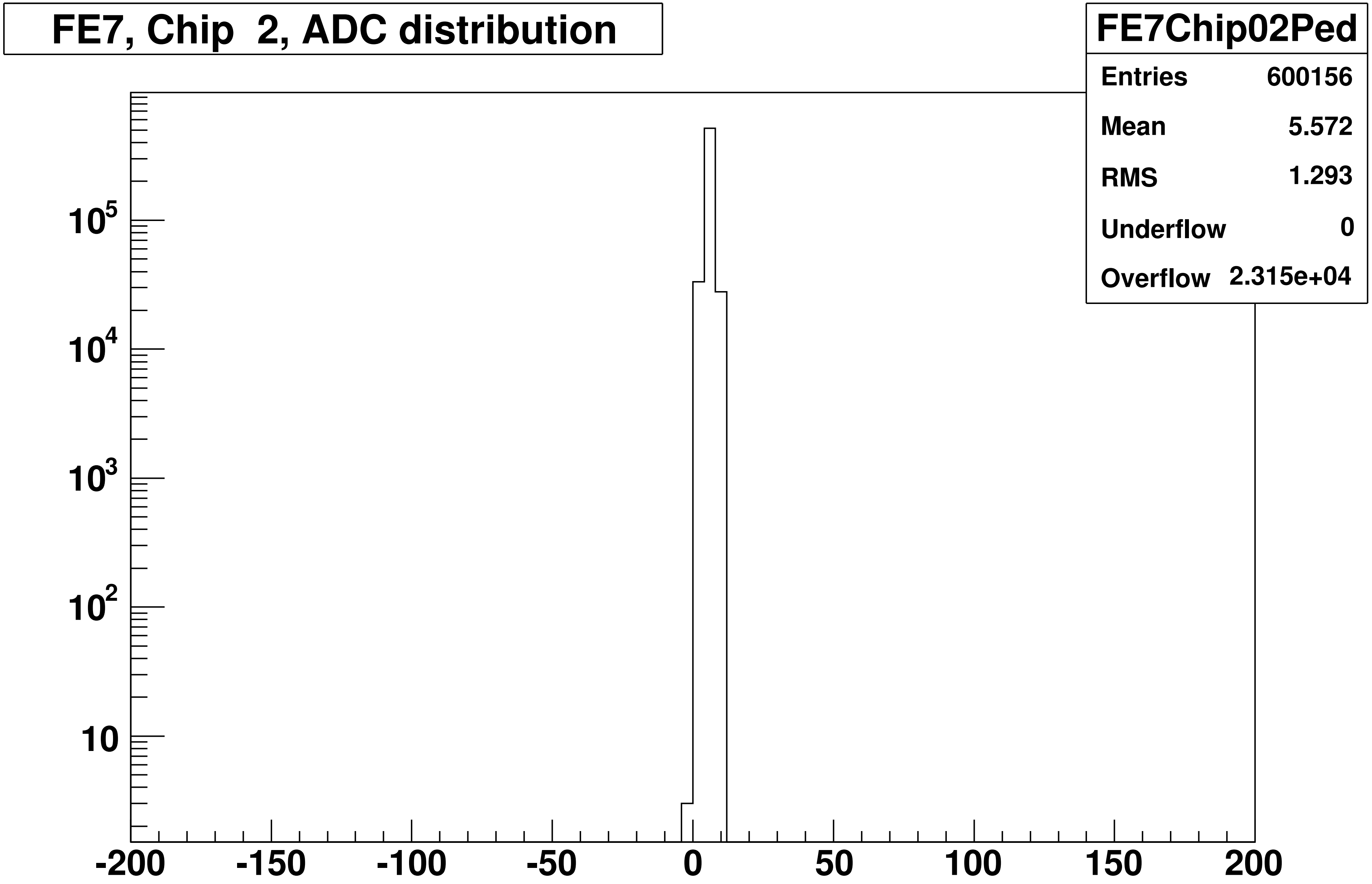

FE7, Chip 0, ADC distribution
FE7Chip00Sig
Entries 600156
Mean 1.886e+04
RMS 4.226
Underflow 5.77e+05
Overflow 0
10
10^2
10^3
10^4
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000


FE7, Chip 1, ADC distribution
FE7Chip01All
Entries 600156
Mean 727.9
RMS 3617
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
-5000
0
5000
10000
15000
20000
25000

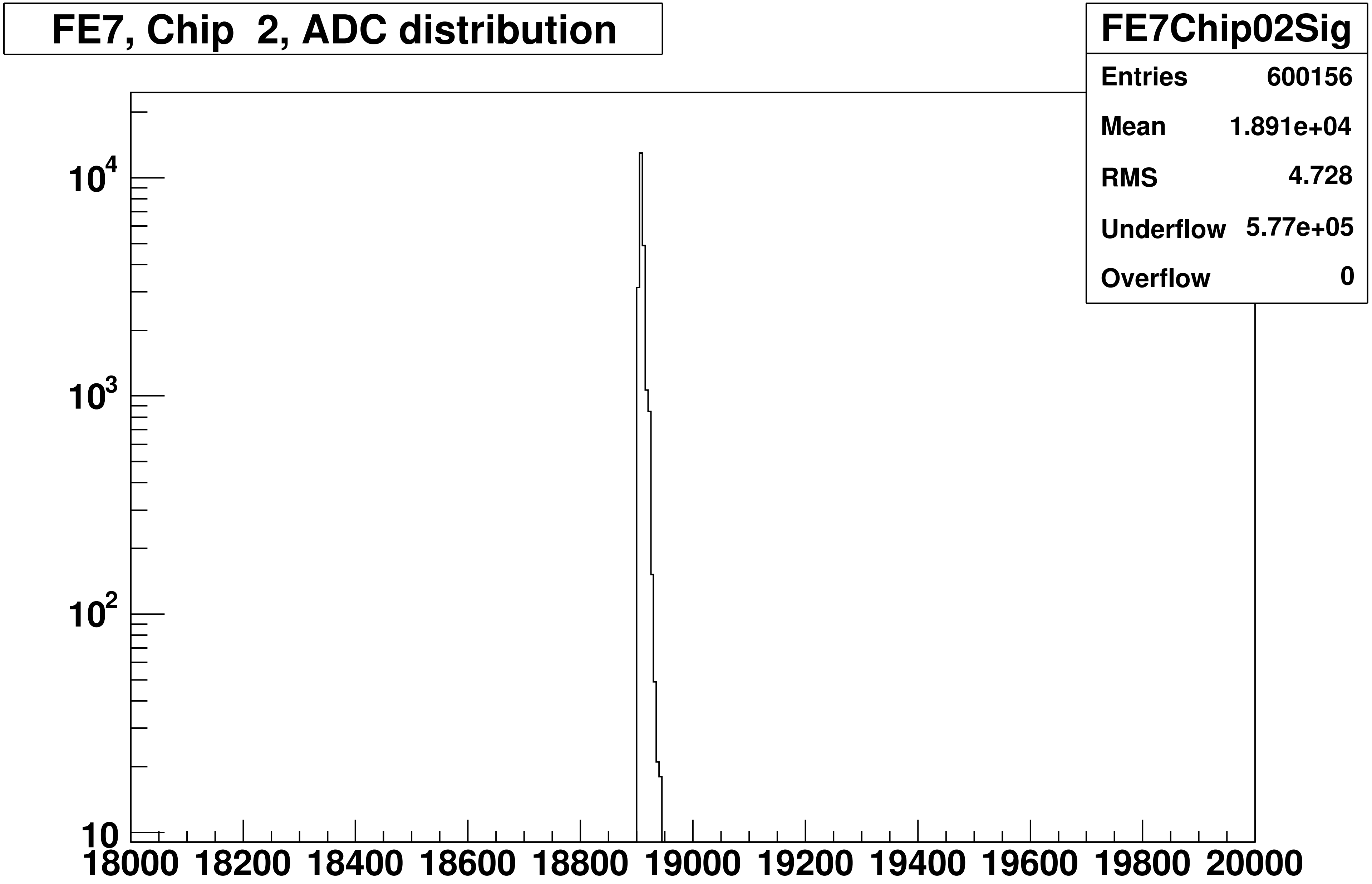

FE7, Chip 1, ADC distribution
FE7Chip01Ped
Entries 600156
Mean 3.539
RMS 1.286
Underflow 0
Overflow 2.315e+04
10^5
10^4
10^3
-200
-150
-100
-50
0
50
100
150
200


FE7, Chip 1, ADC distribution
FE7Chip01Sig
Entries 600156
Mean 1.878e+04
RMS 4.539
Underflow 5.77e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000

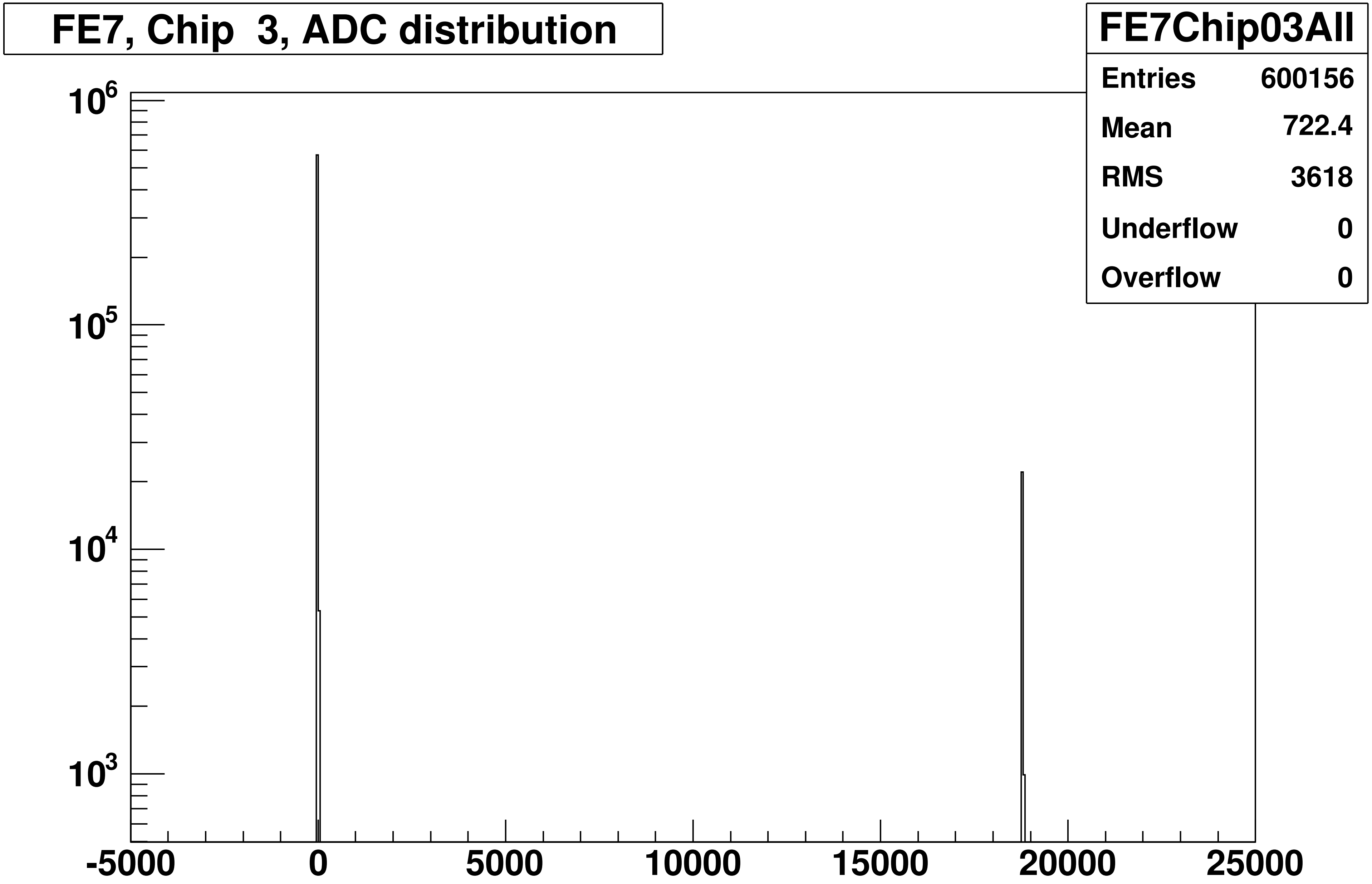

FE7, Chip 2, ADC distribution
FE7Chip02All
Entries 600156
Mean 734.7
RMS 3640
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000



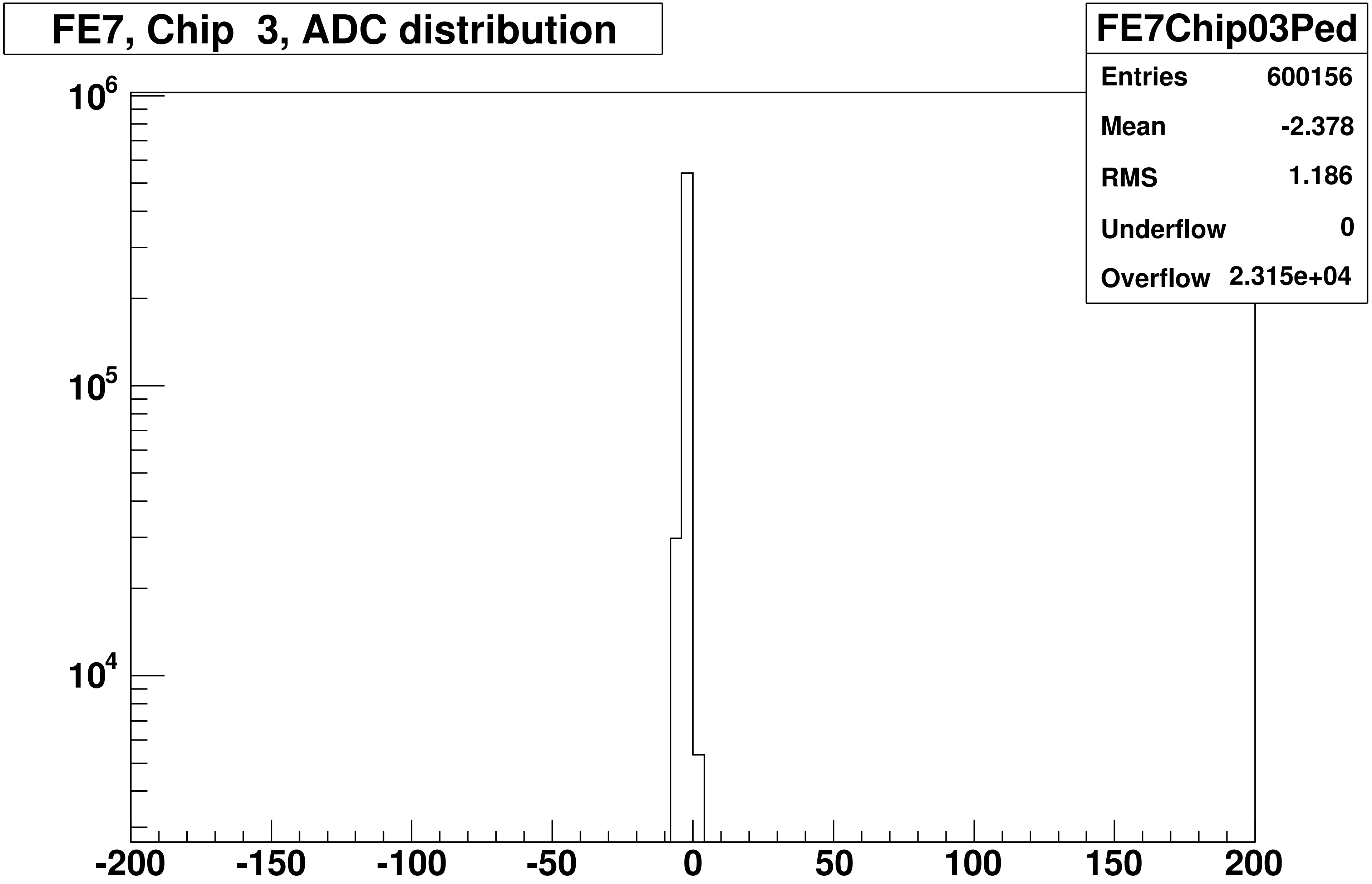
FE7, Chip 2, ADC distribution
FE7Chip02Ped
Entries 600156
Mean 5.572
RMS 1.293
Underflow 0
Overflow 2.315e+04
10
10^2
10^3
10^4
10^5
-200
-150
-100
-50
0
50
100
150
200



FE7, Chip 2, ADC distribution
FE7Chip02Sig
Entries 600156
Mean 1.891e+04
RMS 4.728
Underflow 5.77e+05
Overflow 0
10^4
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE7, Chip 3, ADC distribution
FE7Chip03All
Entries 600156
Mean 722.4
RMS 3618
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
-5000
0
5000
10000
15000
20000
25000



FE7, Chip 3, ADC distribution
FE7Chip03Ped
Entries 600156
Mean -2.378
RMS 1.186
Underflow 0
Overflow 2.315e+04
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10^5
10^4
-200
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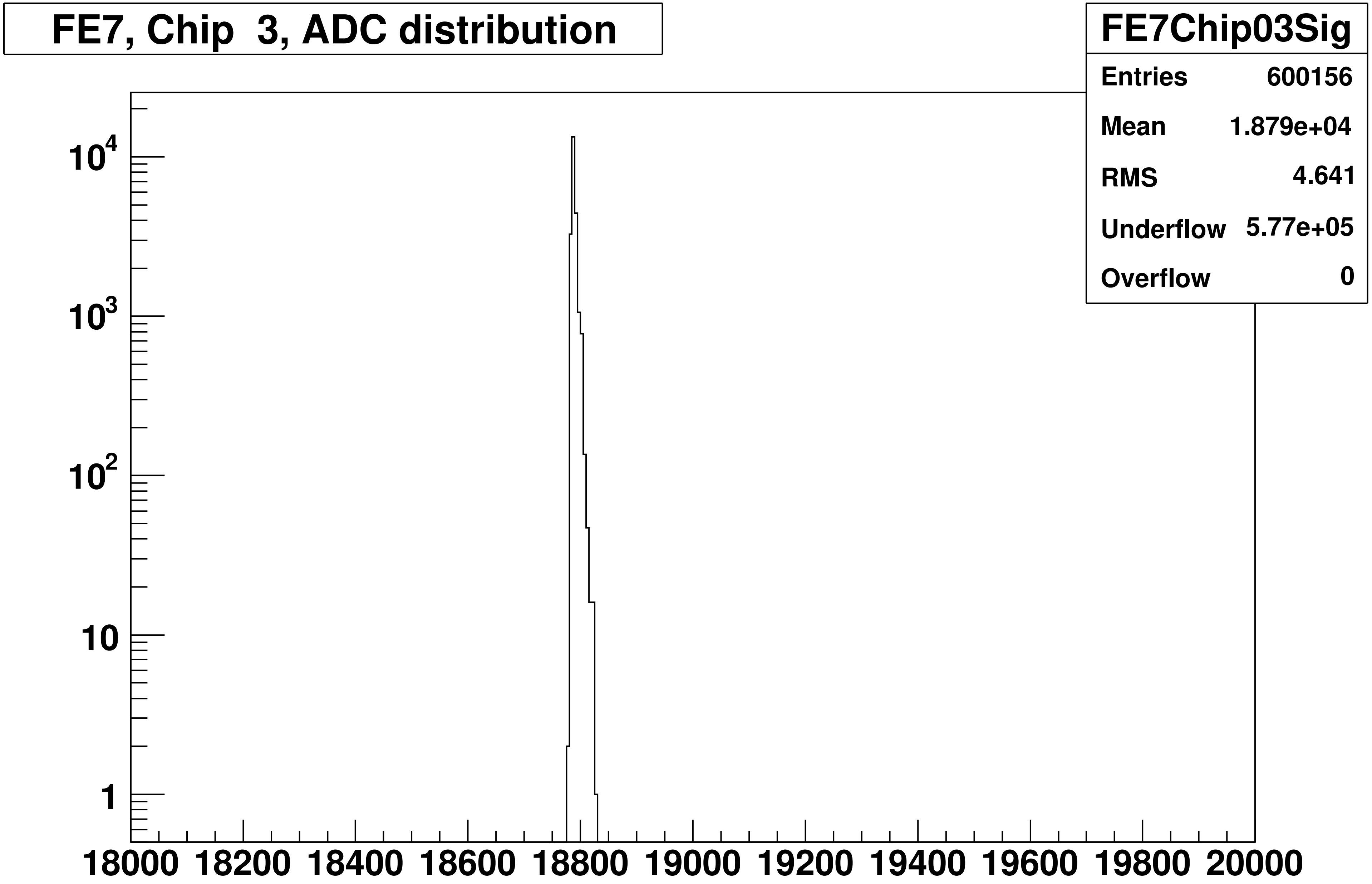
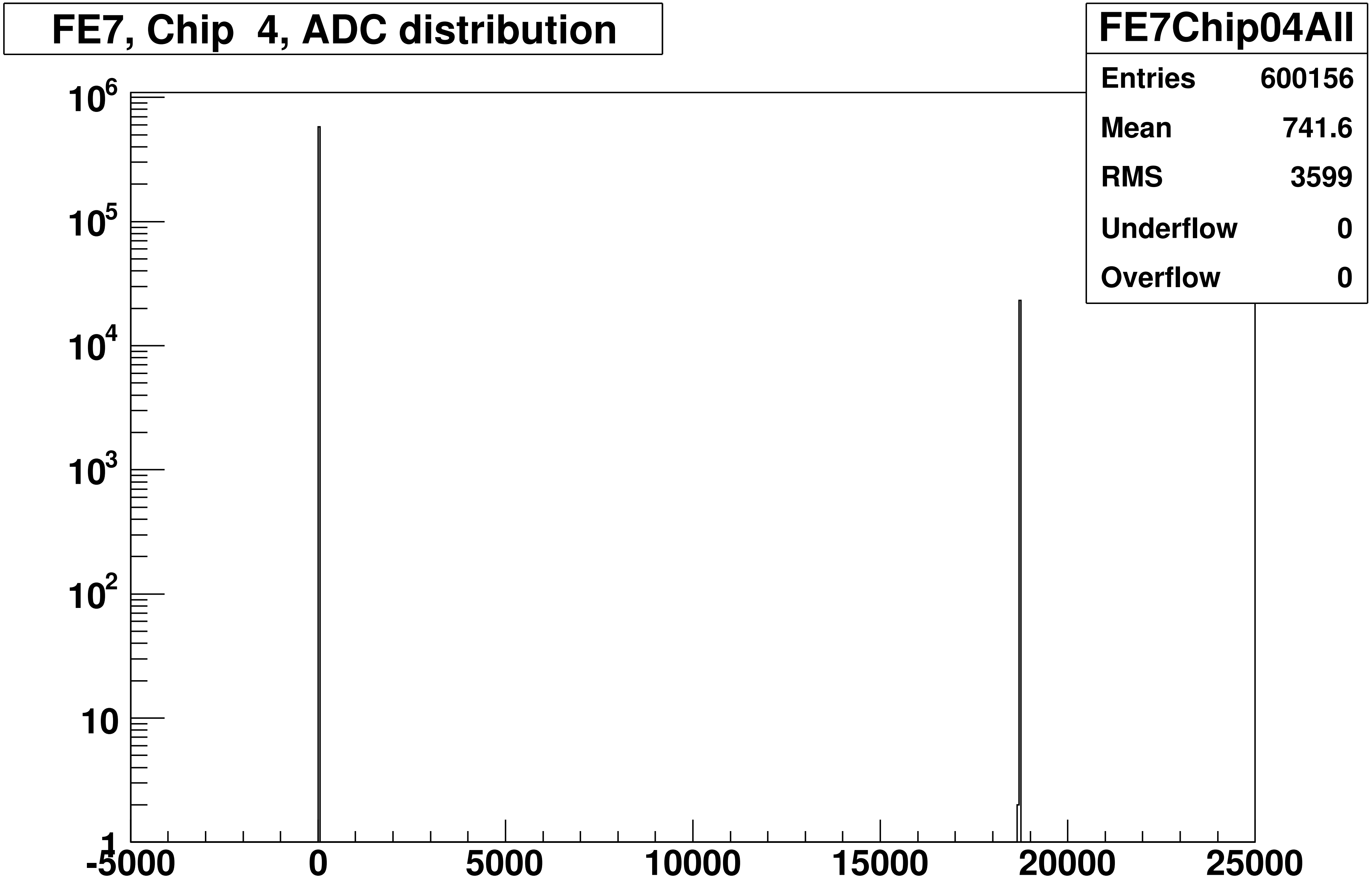
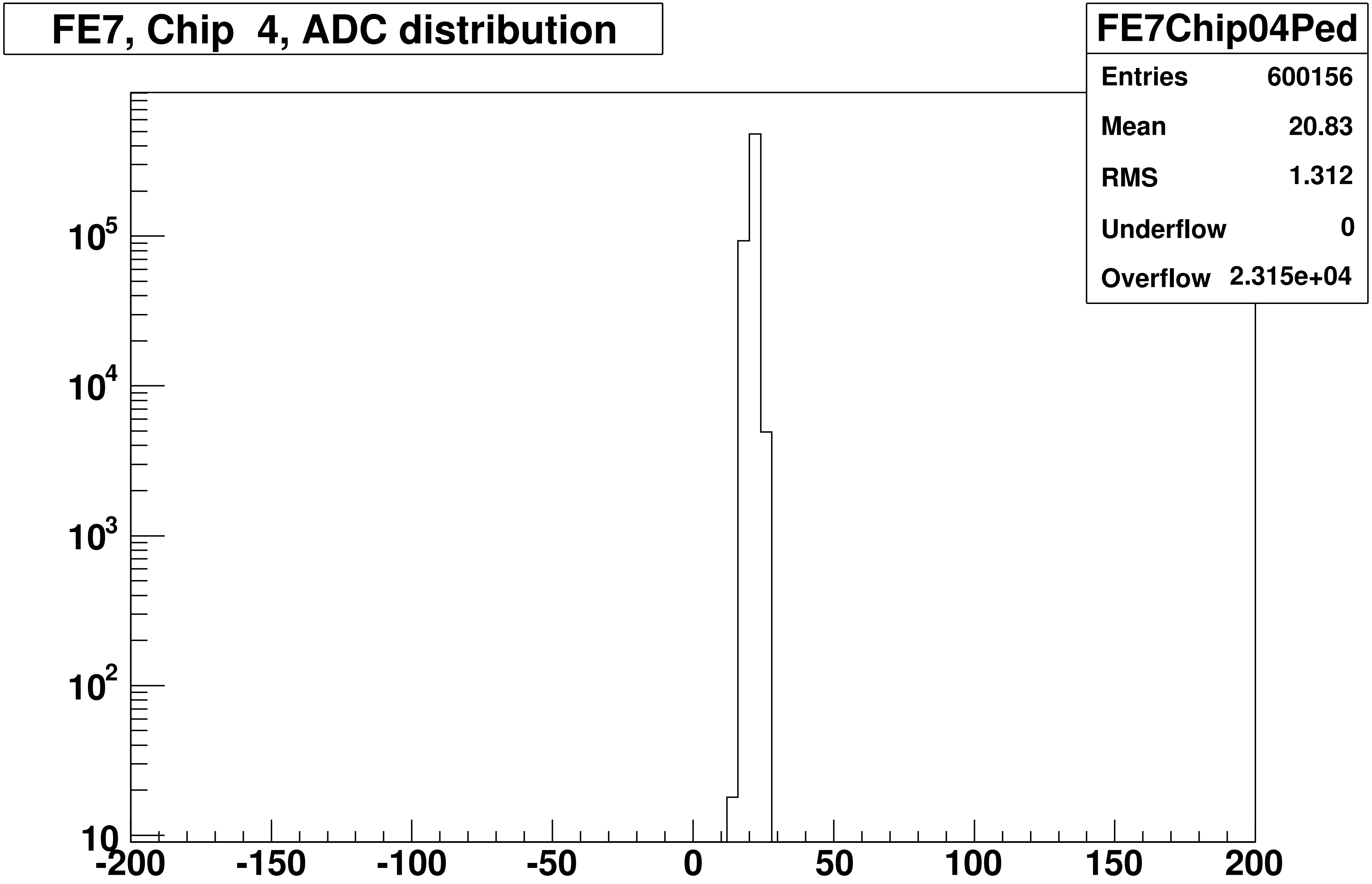
-100
-50
0
50
100
150
200

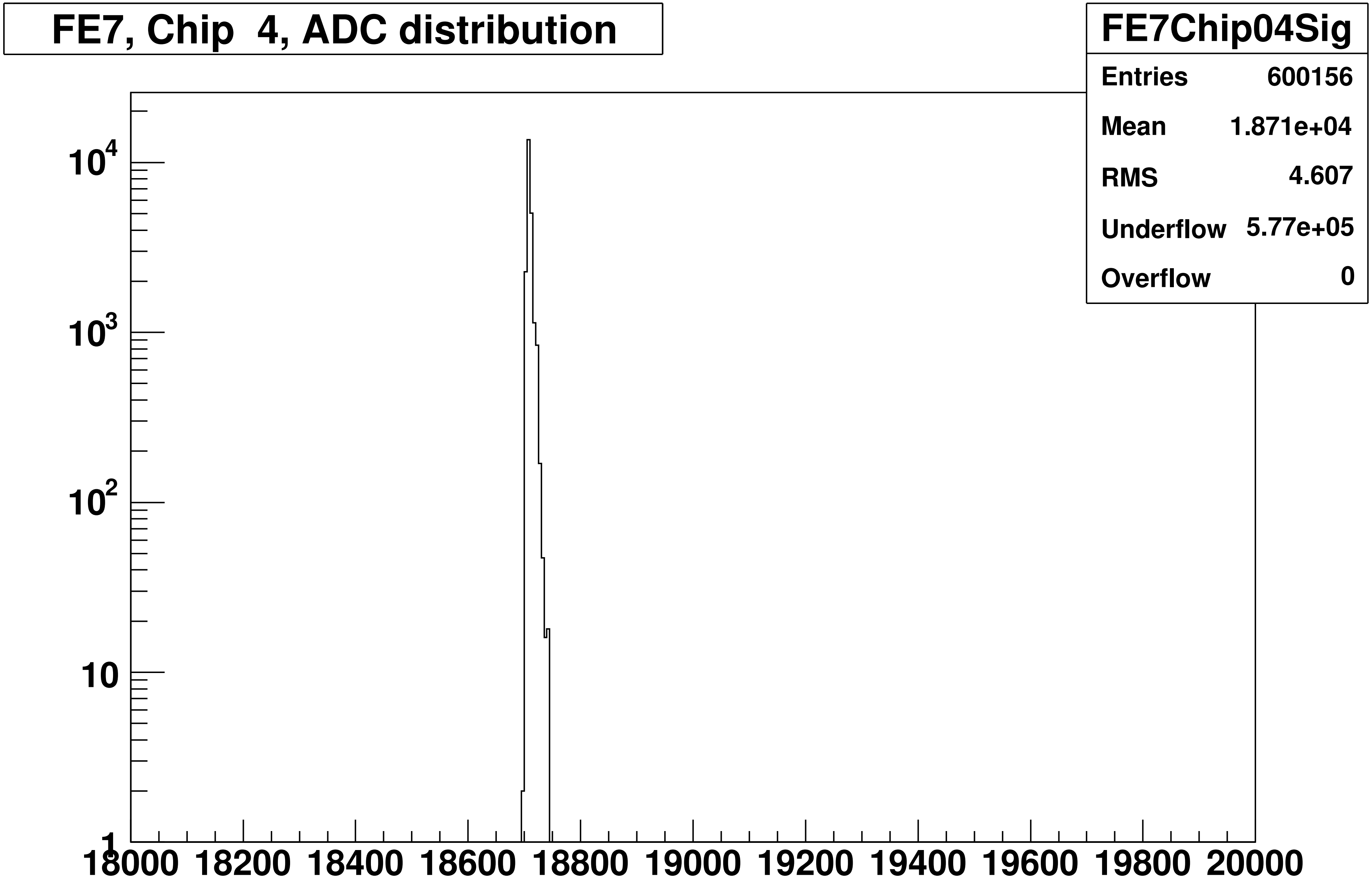


FE7, Chip 3, ADC distribution
FE7Chip03Sig
Entries 600156
Mean 1.879e+04
RMS 4.641
Underflow 5.77e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000

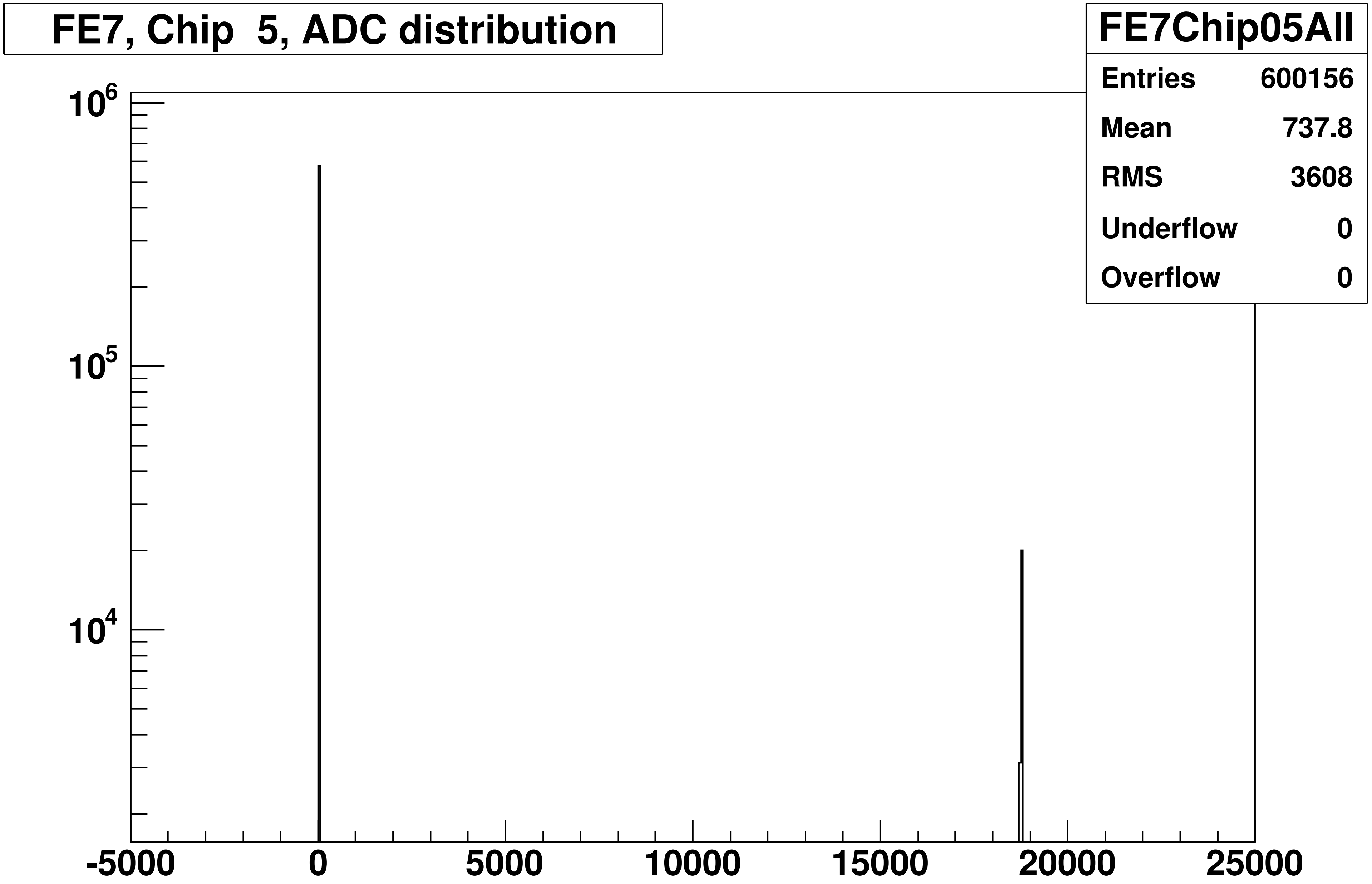


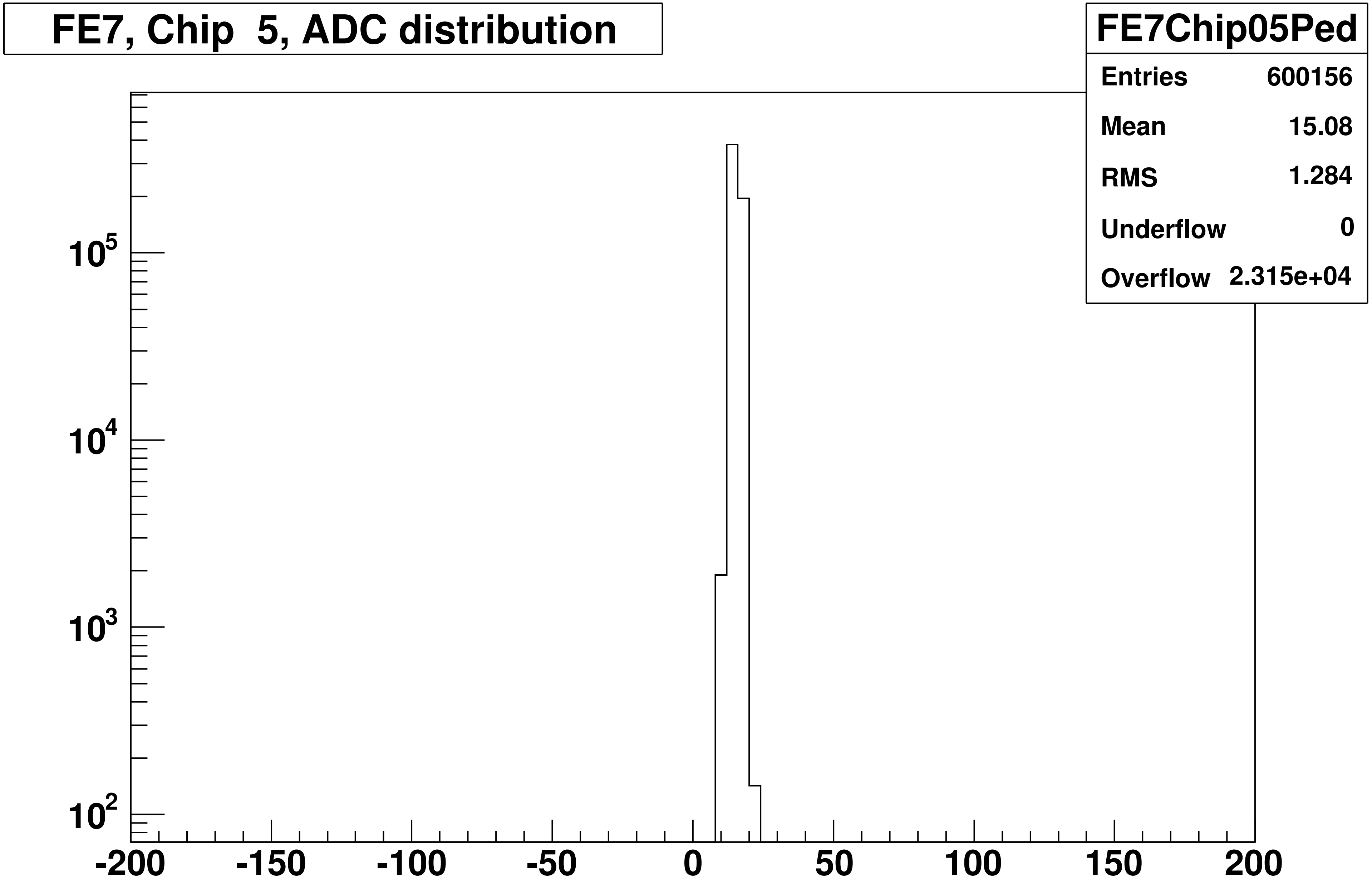
FE7, Chip 4, ADC distribution
FE7Chip04All
Entries 600156
Mean 741.6
RMS 3599
Underflow 0
Overflow 0
1
10
10^2
10^3
10^4
10^5
10^6
-5000
0
5000
10000
15000
20000
25000

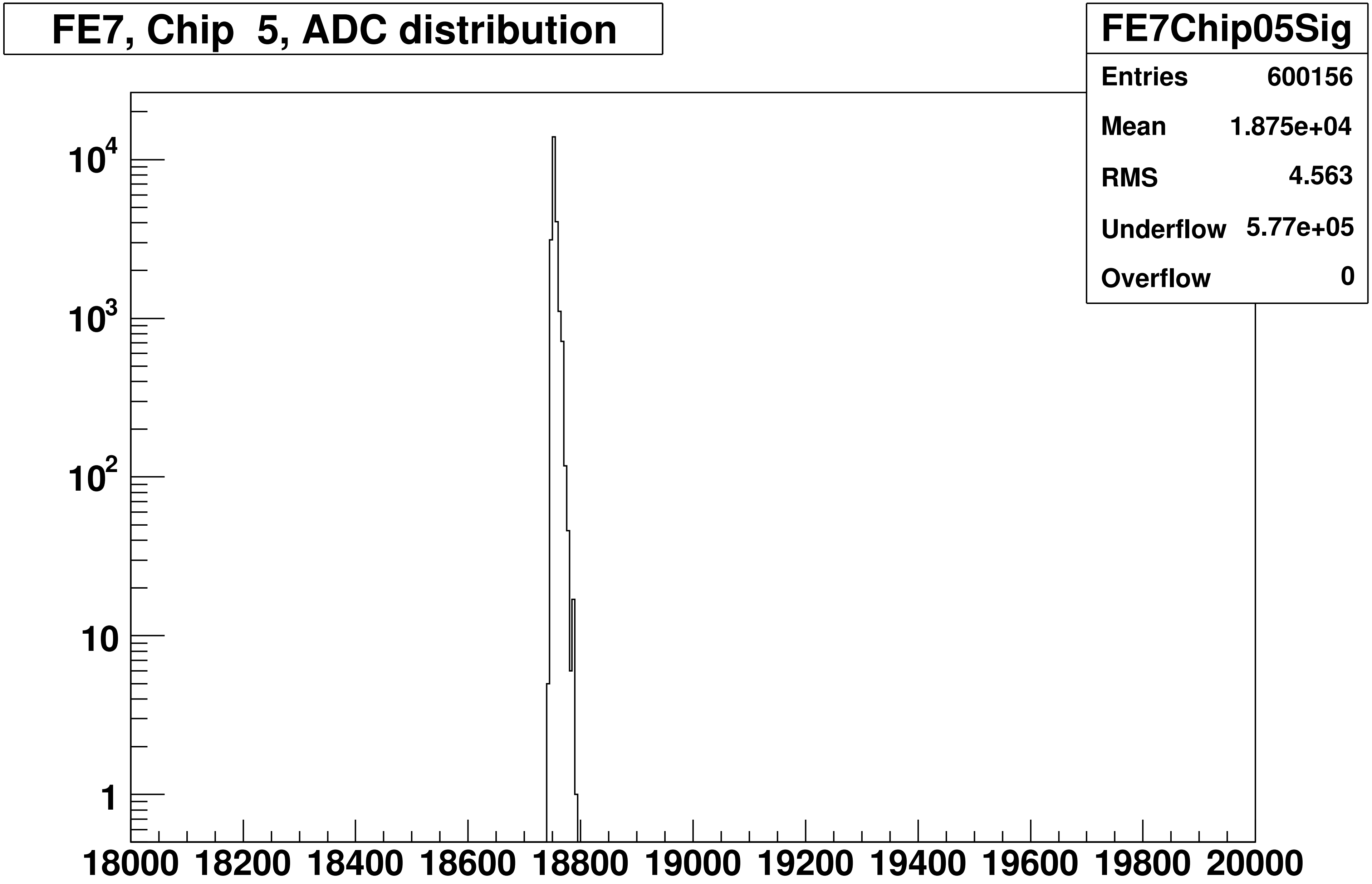

FE7, Chip 4, ADC distribution
FE7Chip04Ped
Entries 600156
Mean 20.83
RMS 1.312
Underflow 0
Overflow 2.315e+04
10
10^2
10^3
10^4
10^5
-200
-150
-100
-50
0
50
100
150
200

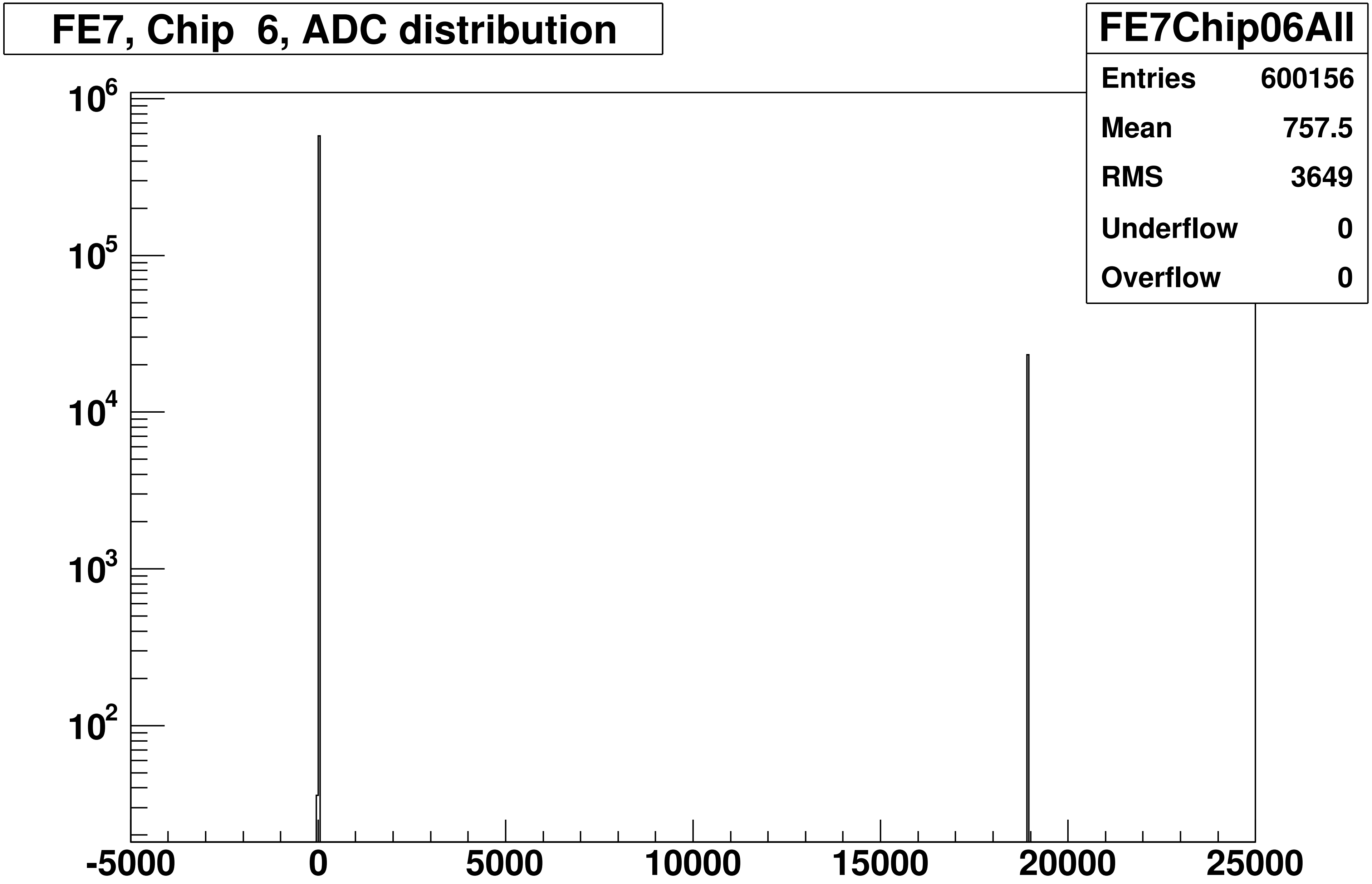


FE7, Chip 4, ADC distribution
FE7Chip04Sig
Entries 600156
Mean 1.871e+04
RMS 4.607
Underflow 5.77e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000

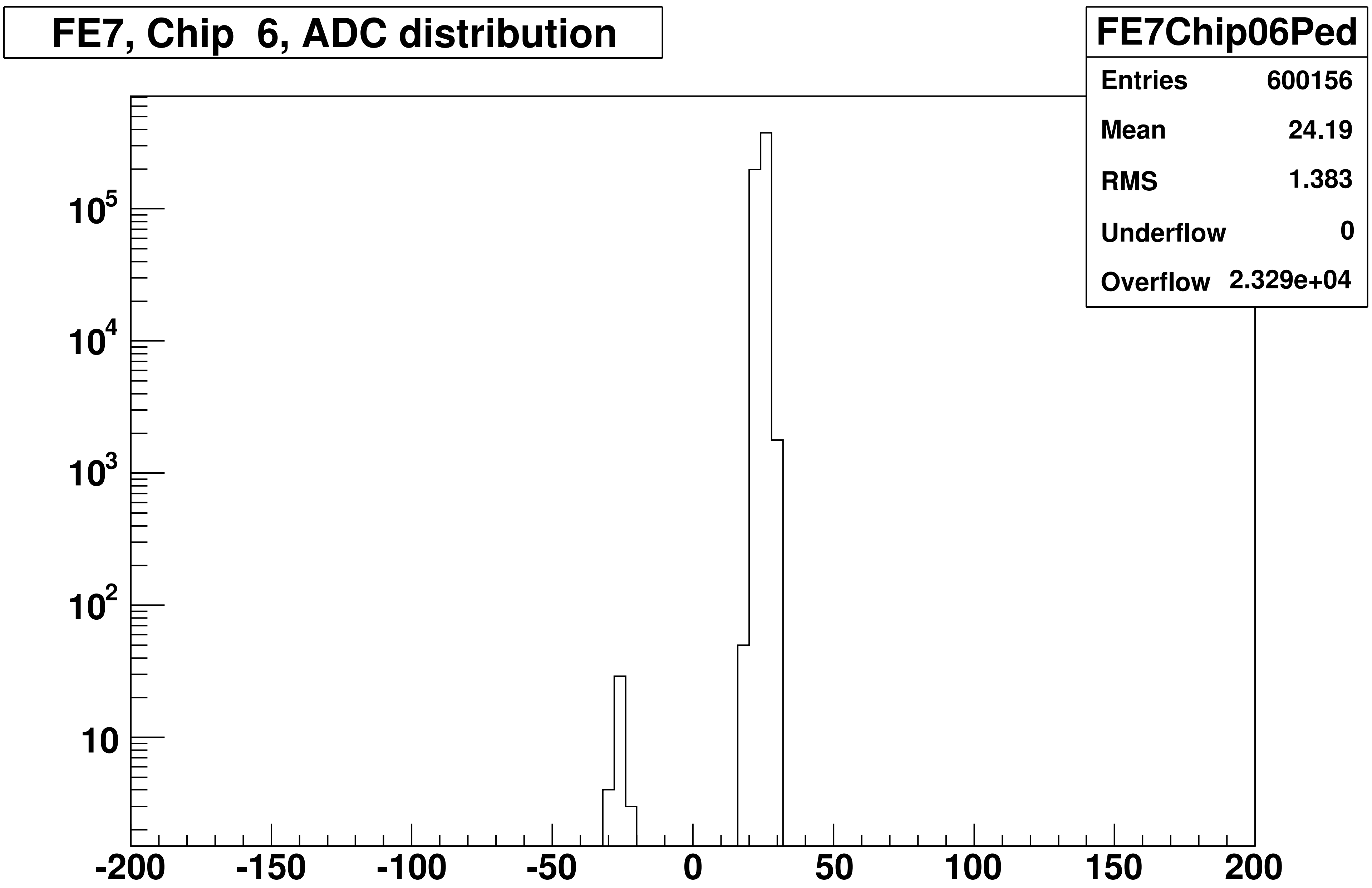

FE7, Chip 5, ADC distribution
FE7Chip05All
Entries 600156
Mean 737.8
RMS 3608
Underflow 0
Overflow 0
10^6
10^5
10^4
-5000
0
5000
10000
15000
20000
25000


FE7, Chip 5, ADC distribution
FE7Chip05Ped
Entries 600156
Mean 15.08
RMS 1.284
Underflow 0
Overflow 2.315e+04
10^5
10^4
10^3
10^2
-200
-150
-100
-50
0
50
100
150
200


FE7, Chip 5, ADC distribution
FE7Chip05Sig
Entries 600156
Mean 1.875e+04
RMS 4.563
Underflow 5.77e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE7, Chip 6, ADC distribution
FE7Chip06All
Entries 600156
Mean 757.5
RMS 3649
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000



FE7, Chip 6, ADC distribution
FE7Chip06Ped
Entries 600156
Mean 24.19
RMS 1.383
Underflow 0
Overflow 2.329e+04
10^5
10^4
10^3
10^2
10
-200
-150
-100
-50
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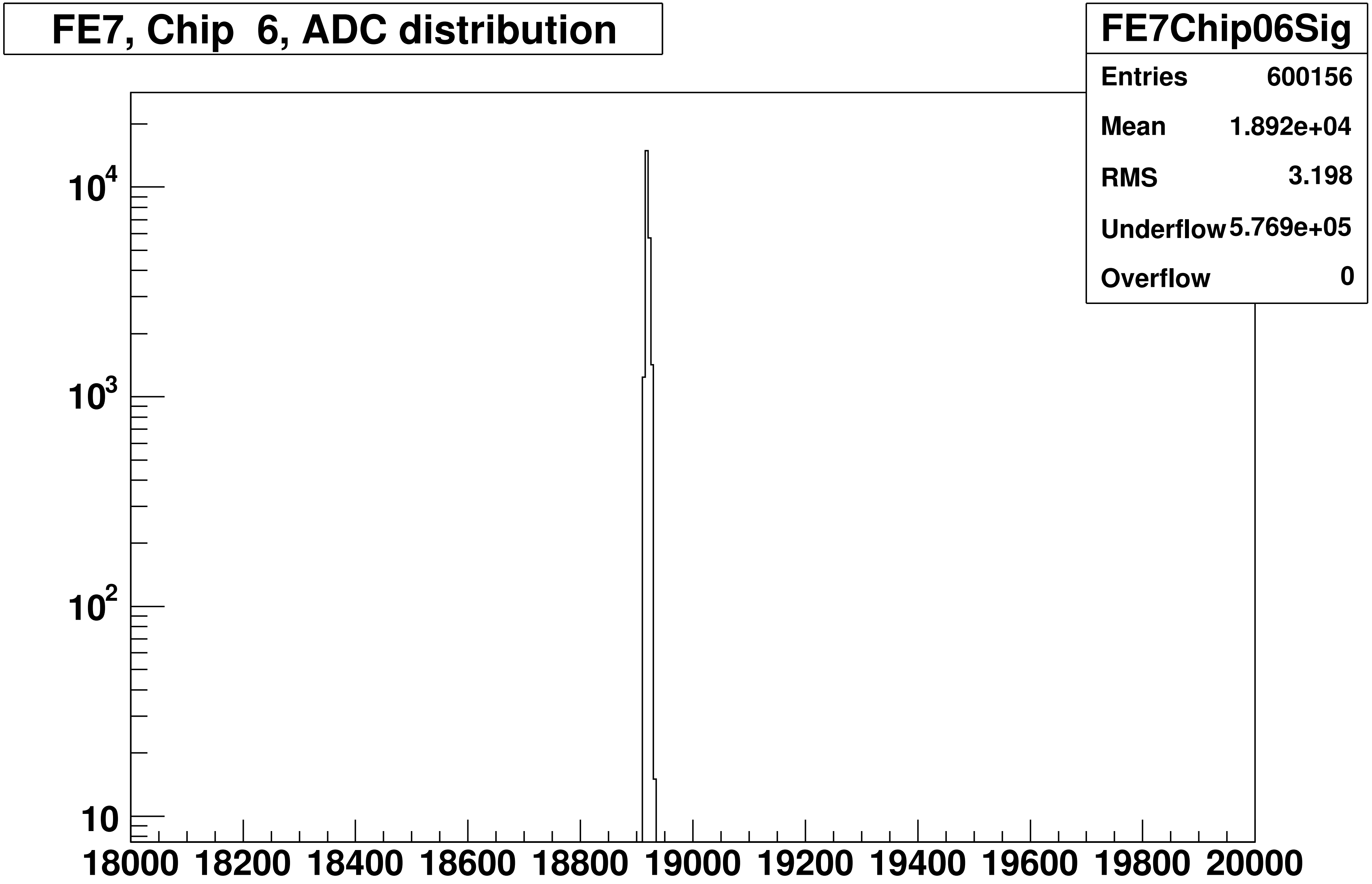
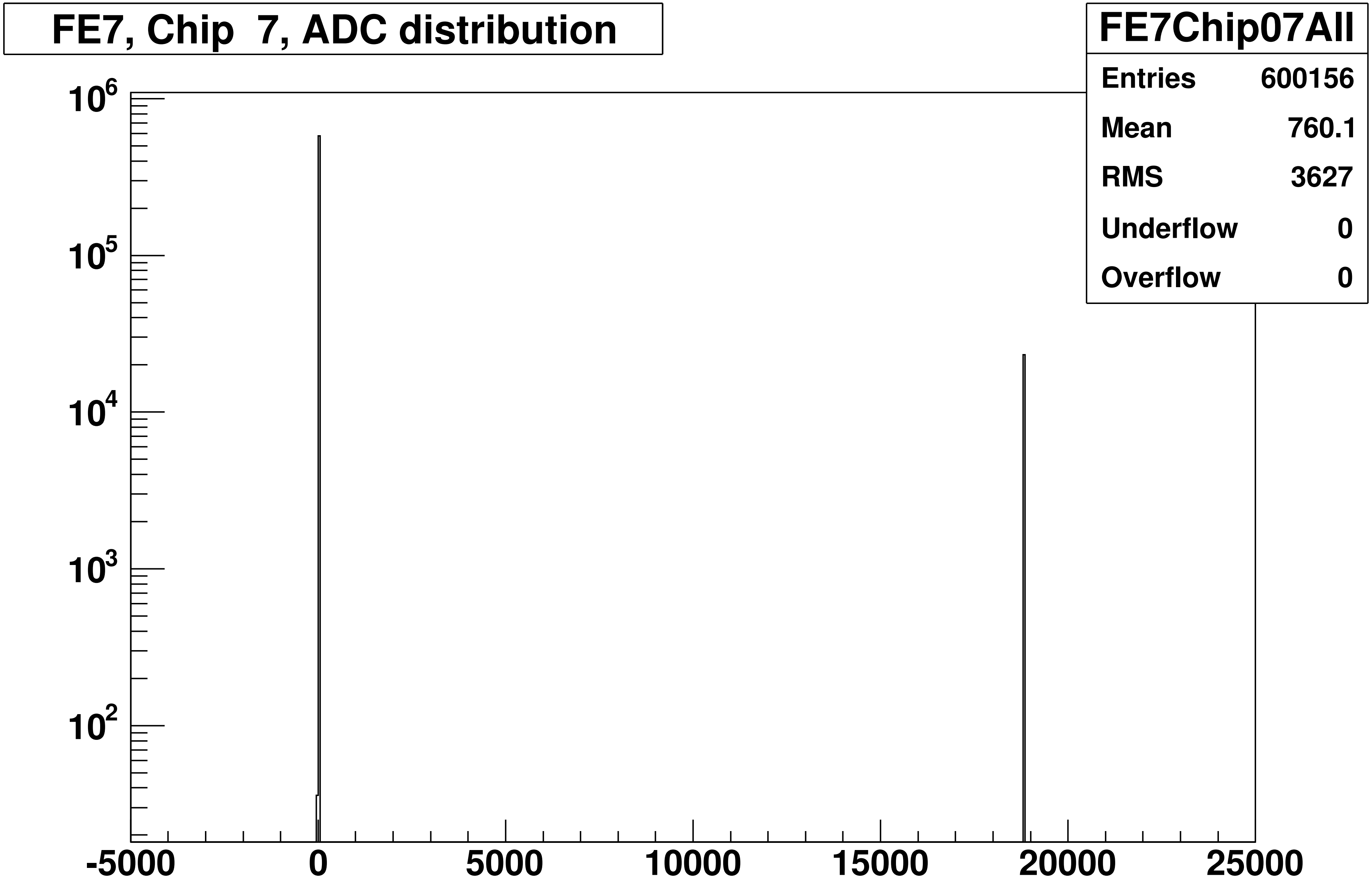
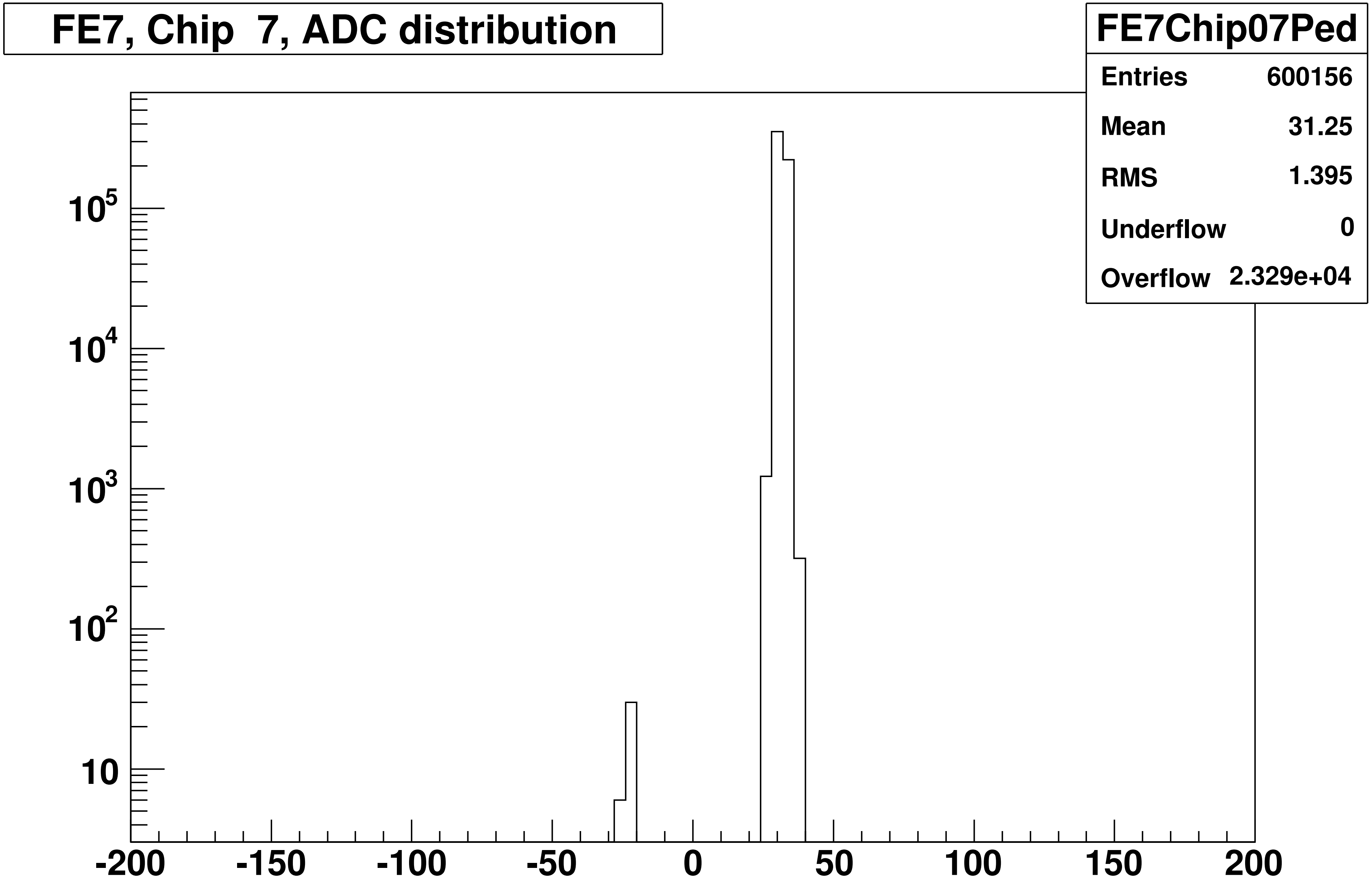
50
100
150
200

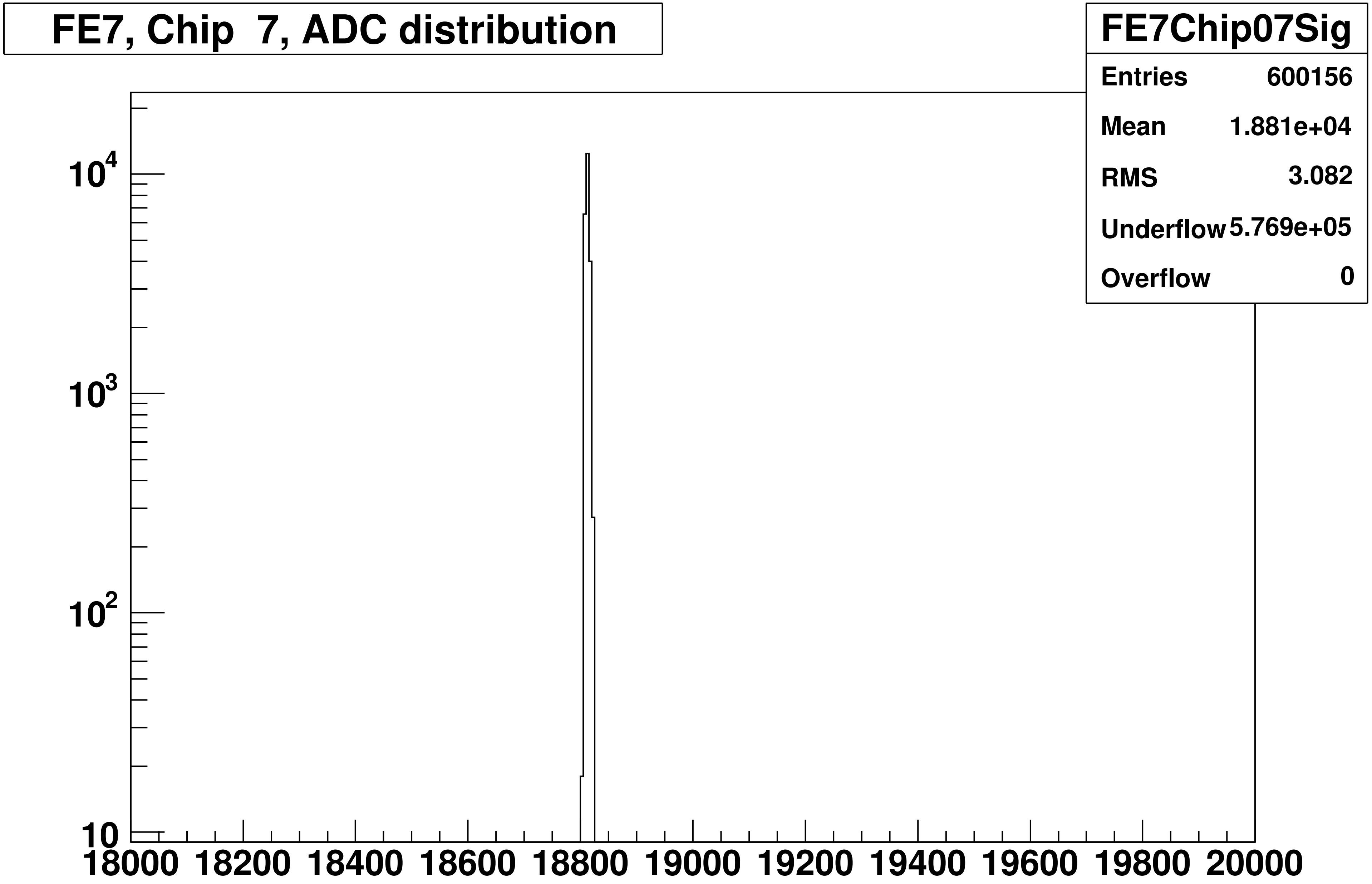

FE7, Chip 6, ADC distribution
FE7Chip06Sig
Entries 600156
Mean 1.892e+04
RMS 3.198
Underflow 5.769e+05
Overflow 0
10^4
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



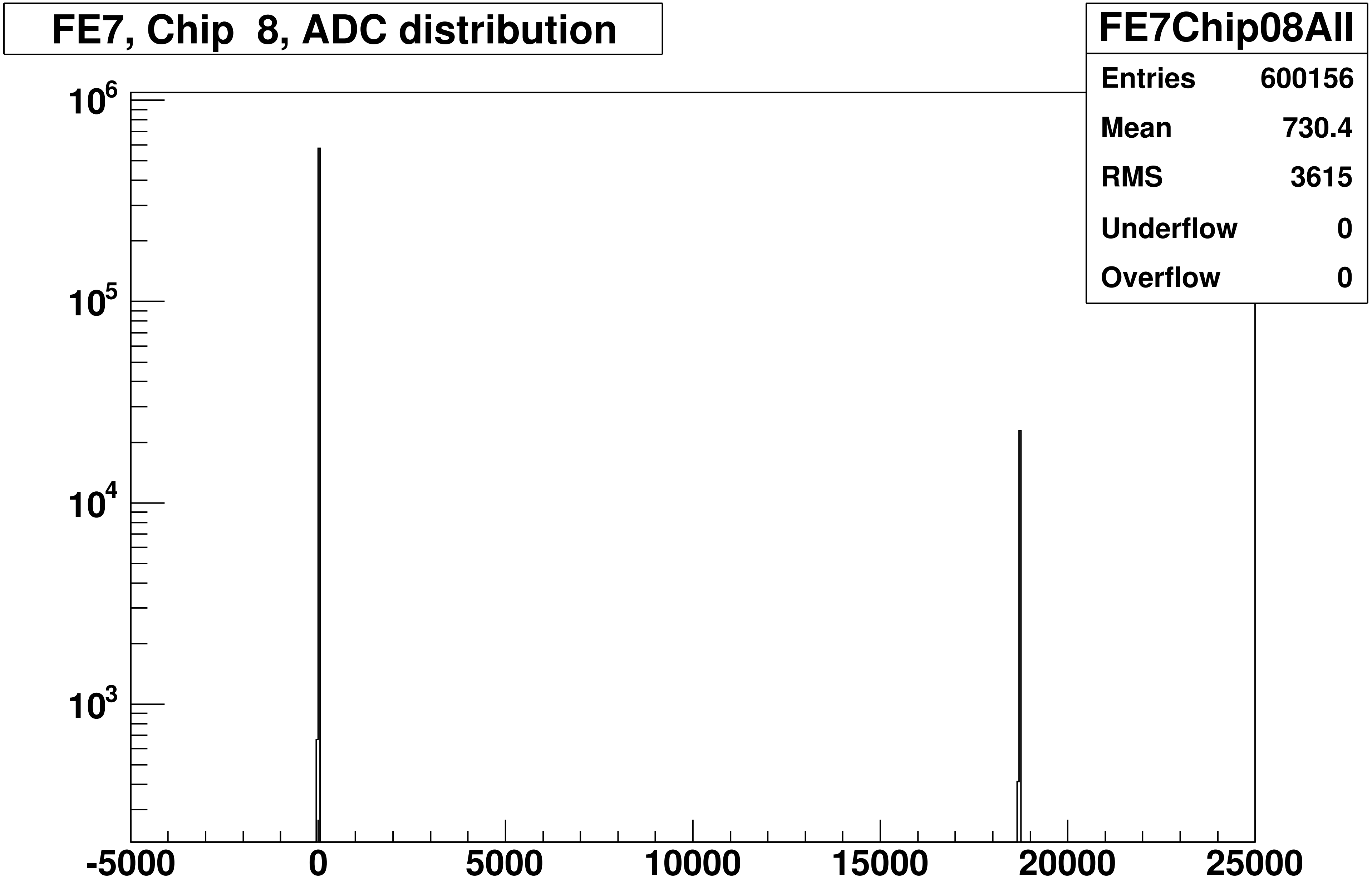
FE7, Chip 7, ADC distribution
FE7Chip07All
Entries 600156
Mean 760.1
RMS 3627
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000



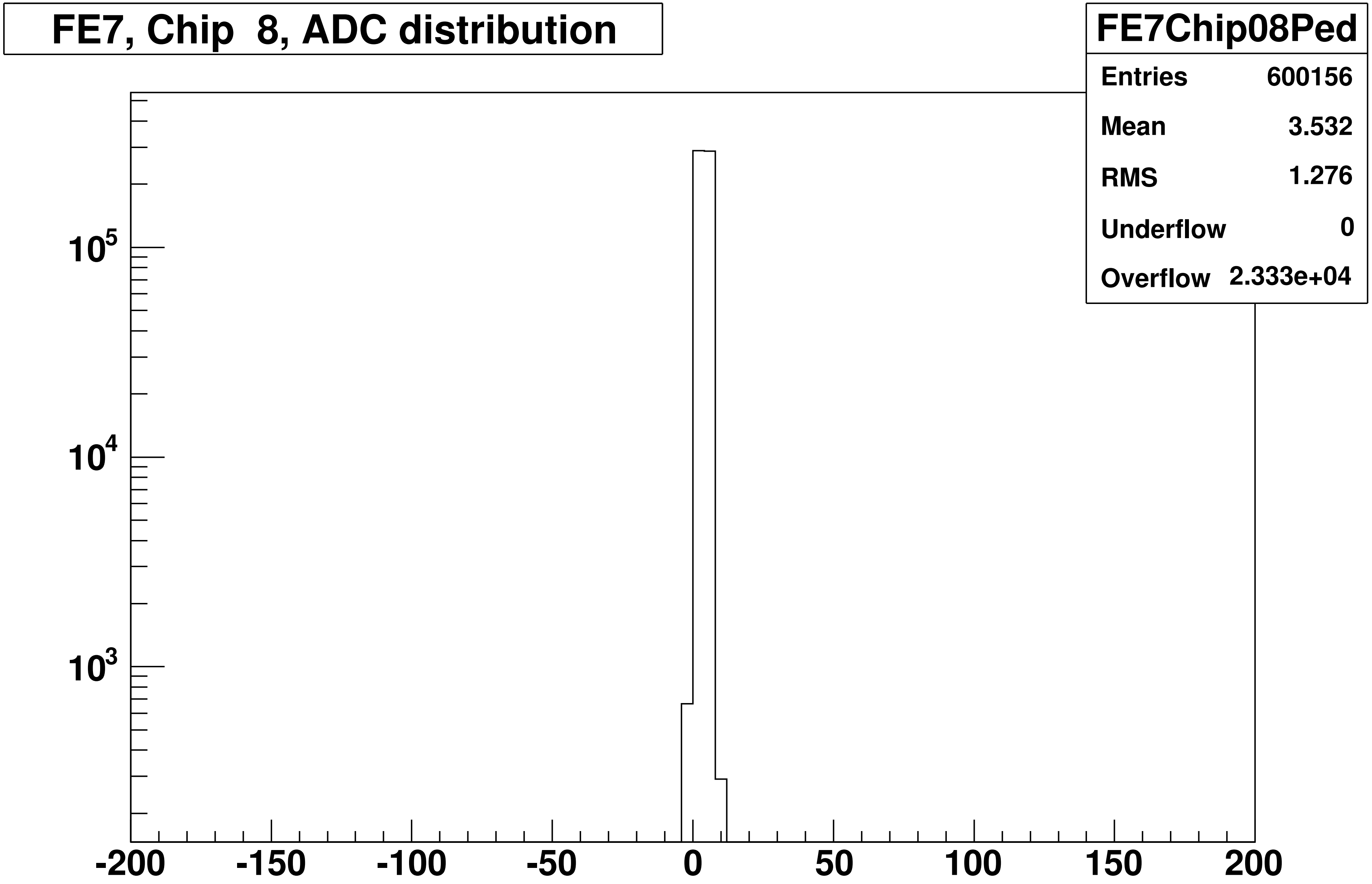
FE7, Chip 7, ADC distribution
FE7Chip07Ped
Entries 600156
Mean 31.25
RMS 1.395
Underflow 0
Overflow 2.329e+04
10^5
10^4
10^3
10^2
10
-200
-150
-100
-50
0
50
100
150
200



FE7, Chip 7, ADC distribution
FE7Chip07Sig
Entries 600156
Mean 1.881e+04
RMS 3.082
Underflow 5.769e+05
Overflow 0
10^4
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE7, Chip 8, ADC distribution
FE7Chip08All
Entries 600156
Mean 730.4
RMS 3615
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
-5000
0
5000
10000
15000
20000
25000



FE7, Chip 8, ADC distribution
FE7Chip08Ped
Entries 600156
Mean 3.532
RMS 1.276
Underflow 0
Overflow 2.333e+04
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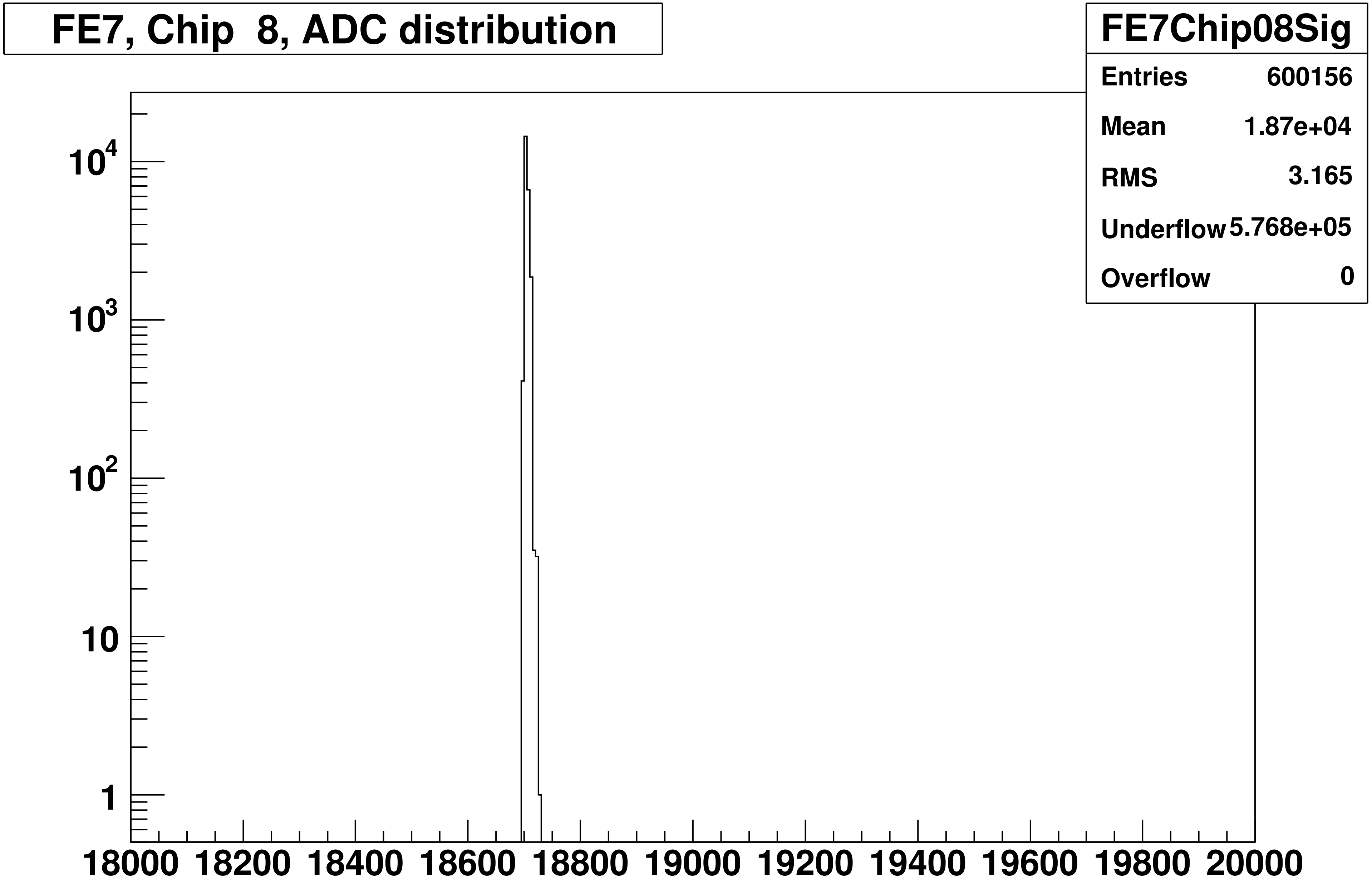
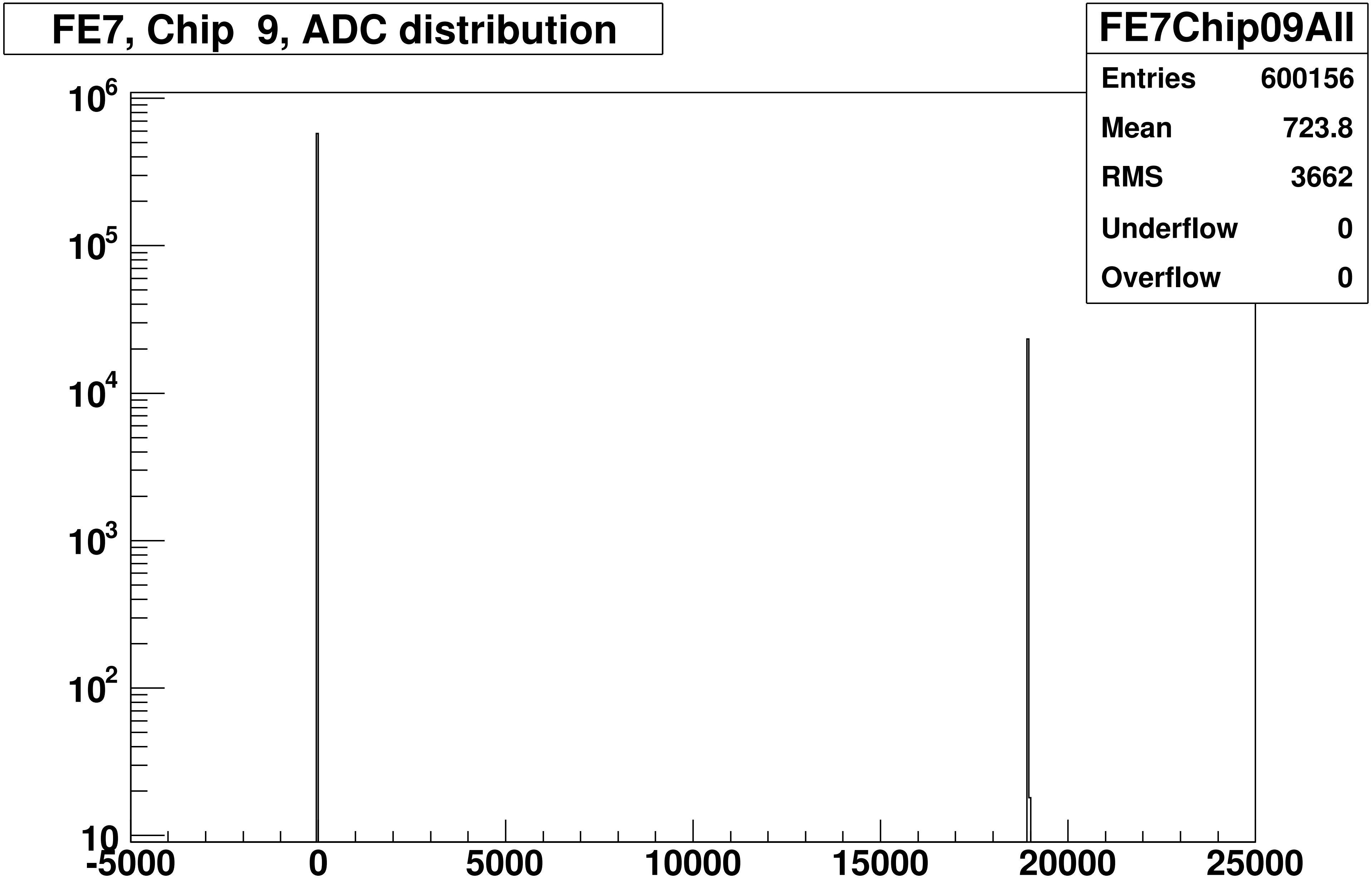
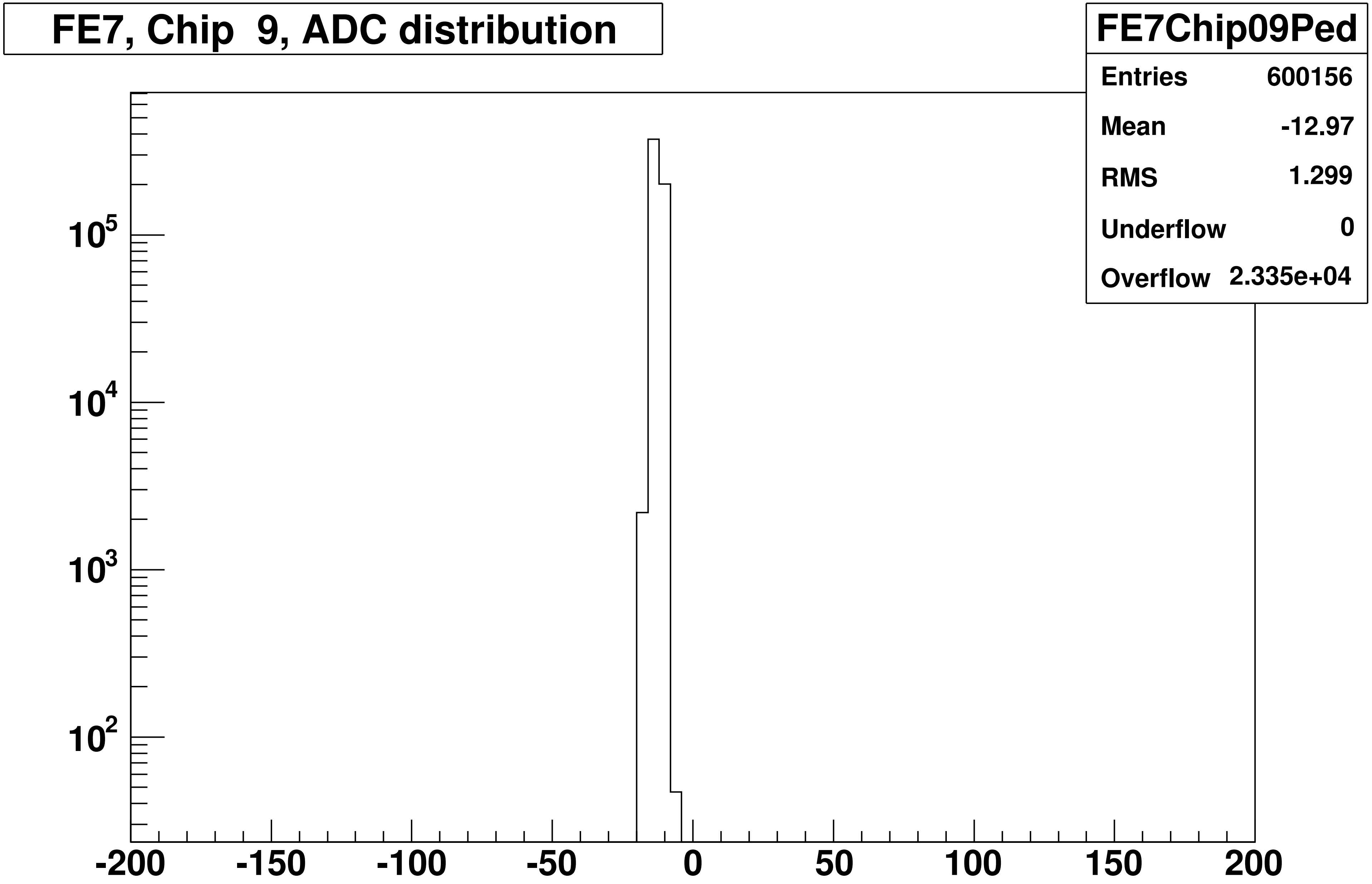
10^4
10^3
-200
-150
-100
-50
0
50
100
150
200

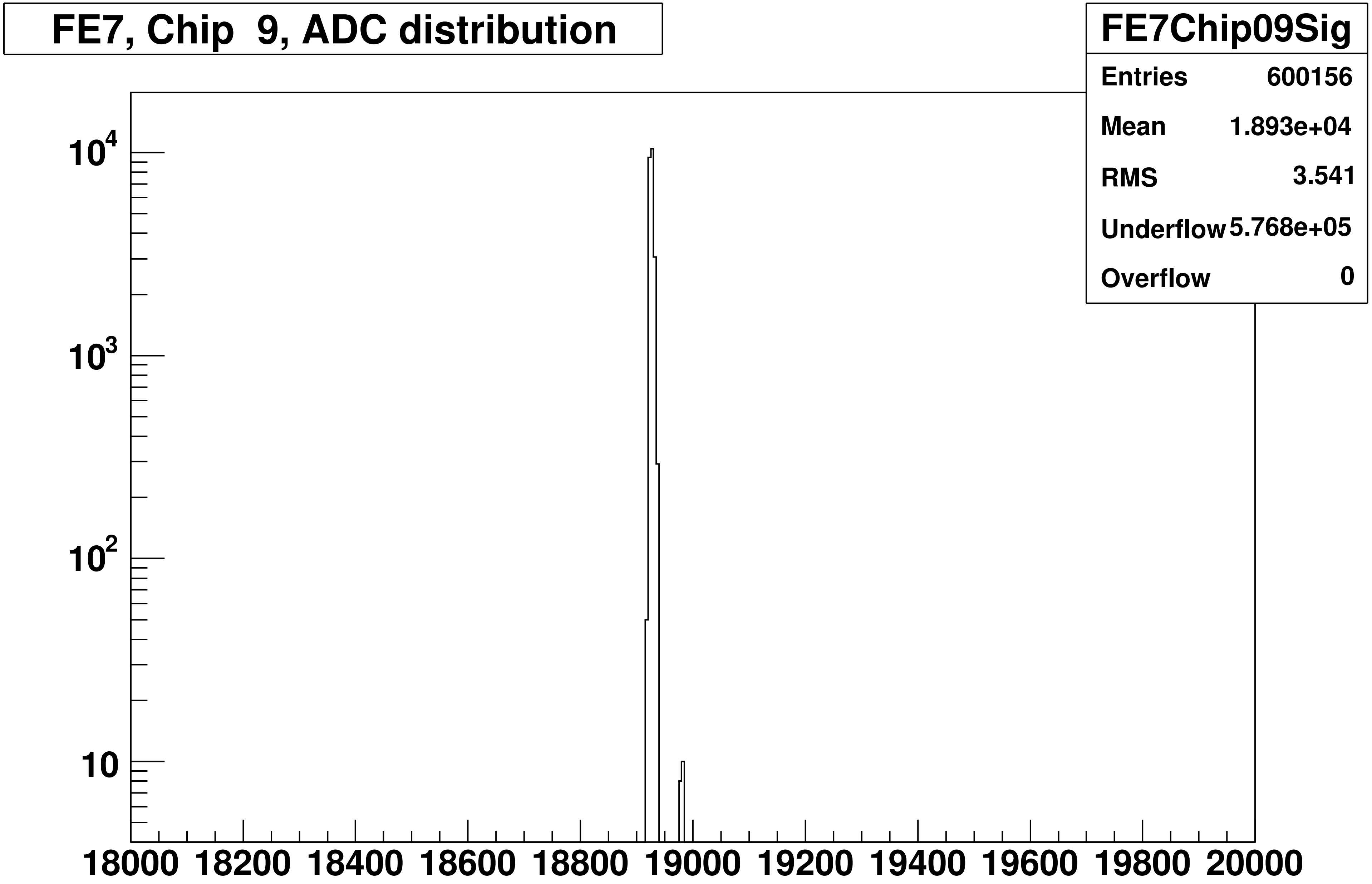


FE7, Chip 8, ADC distribution
FE7Chip08Sig
Entries 600156
Mean 1.87e+04
RMS 3.165
Underflow 5.768e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000

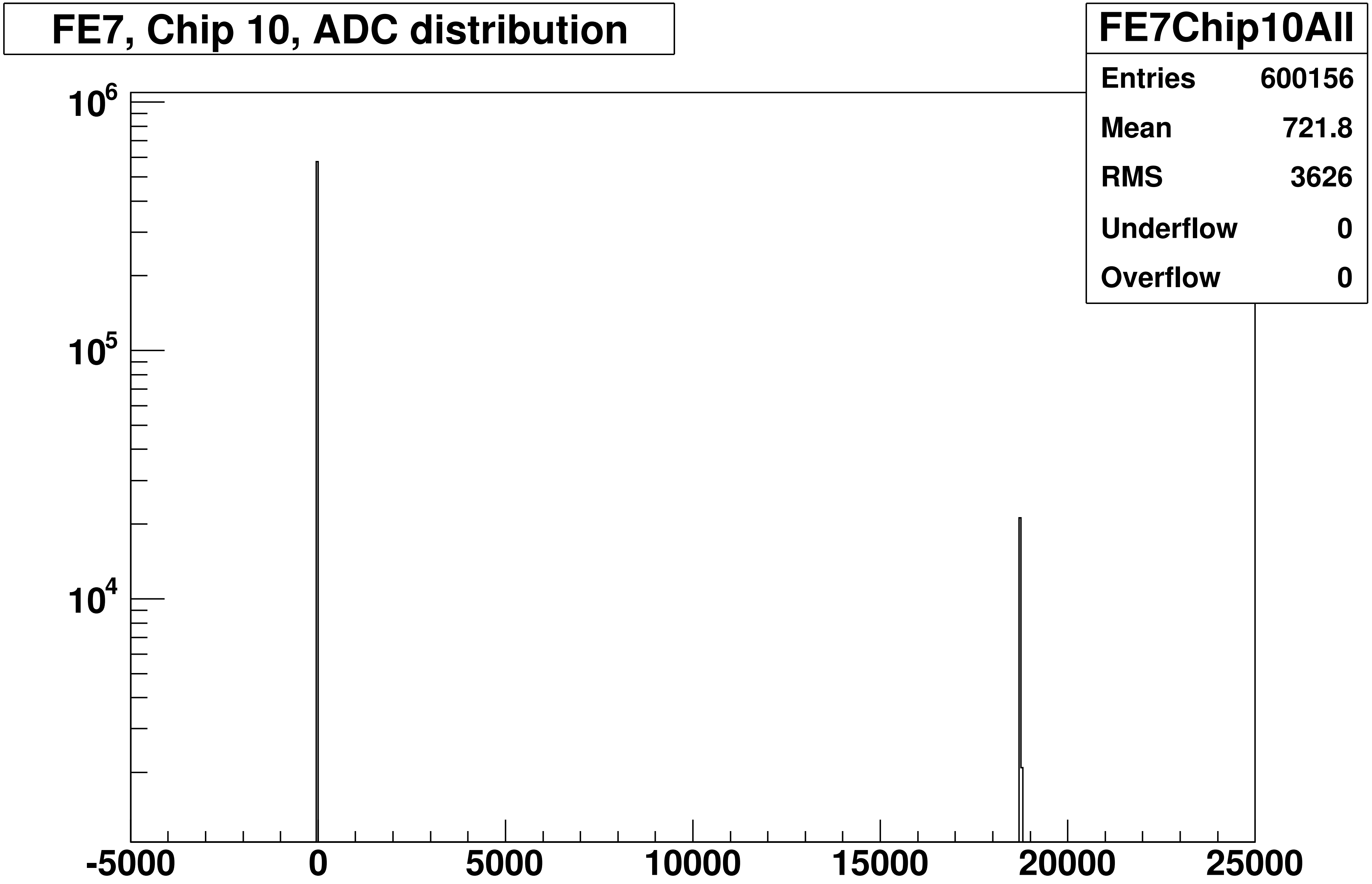

FE7, Chip 9, ADC distribution
FE7Chip09All
Entries 600156
Mean 723.8
RMS 3662
Underflow 0
Overflow 0
10
10^2
10^3
10^4
10^5
10^6
-5000
0
5000
10000
15000
20000
25000

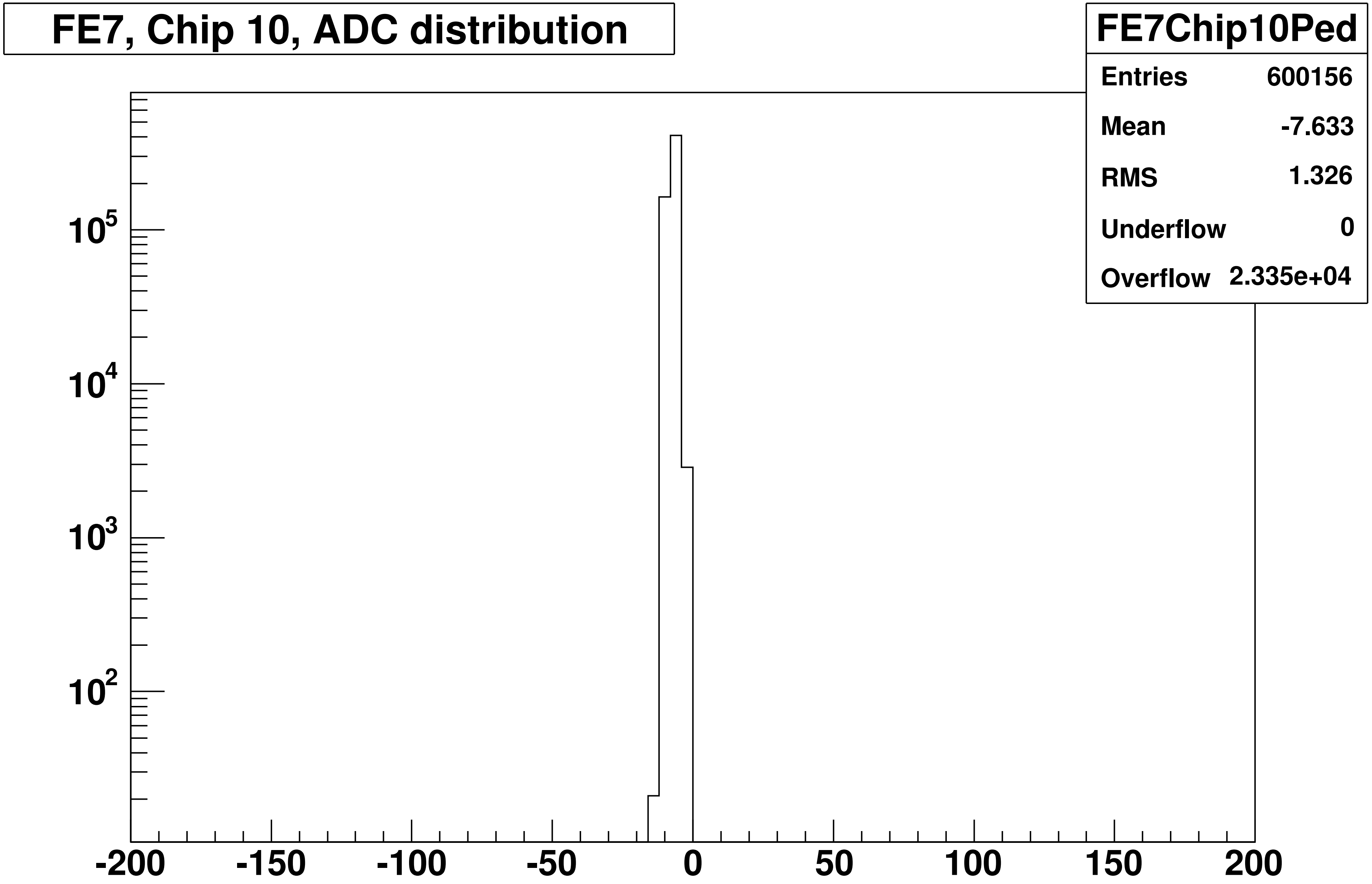


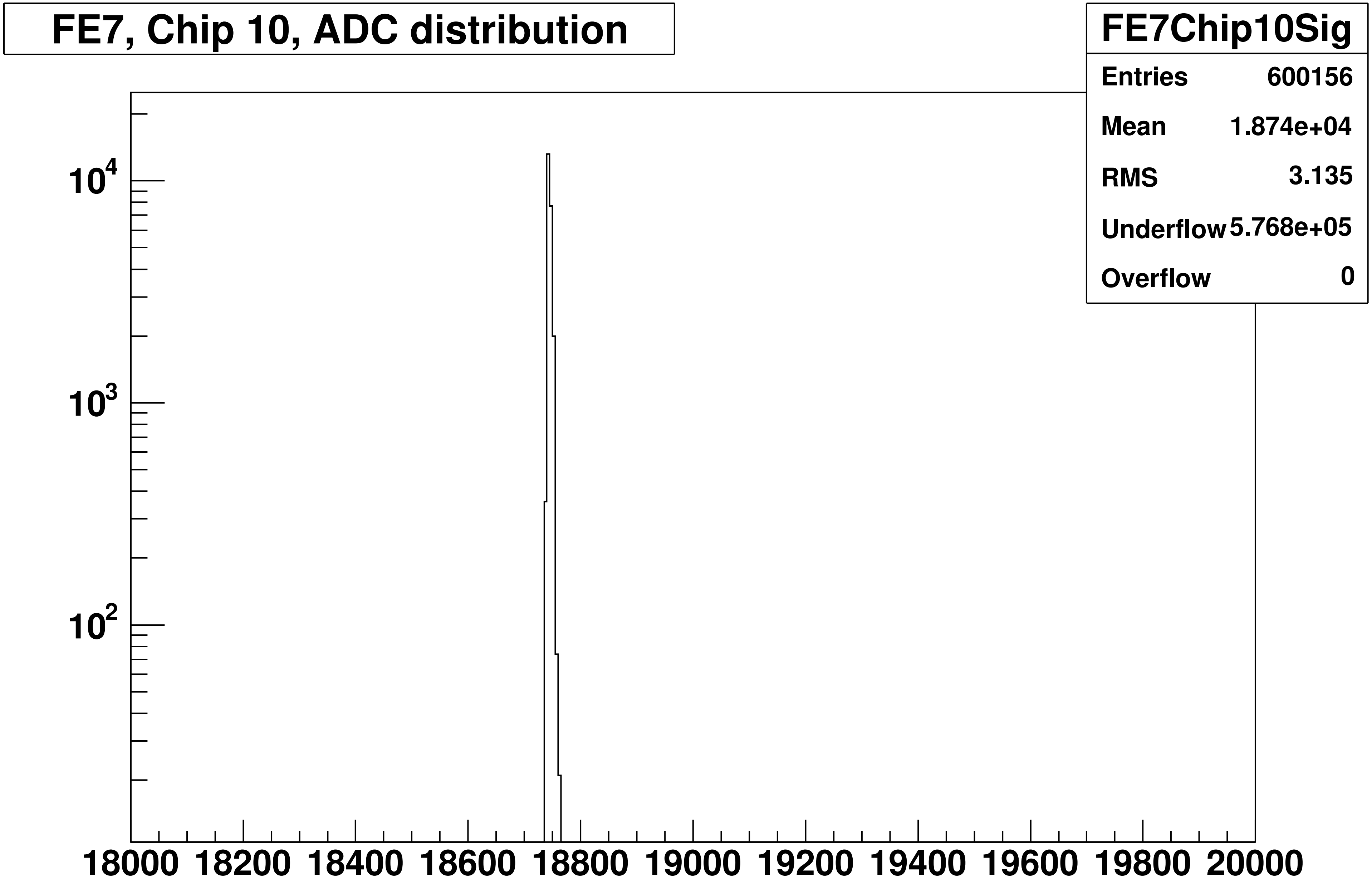
FE7, Chip 9, ADC distribution
FE7Chip09Ped
Entries 600156
Mean -12.97
RMS 1.299
Underflow 0
Overflow 2.335e+04
10^5
10^4
10^3
10^2
-200 -150 -100 -50 0 50 100 150 200

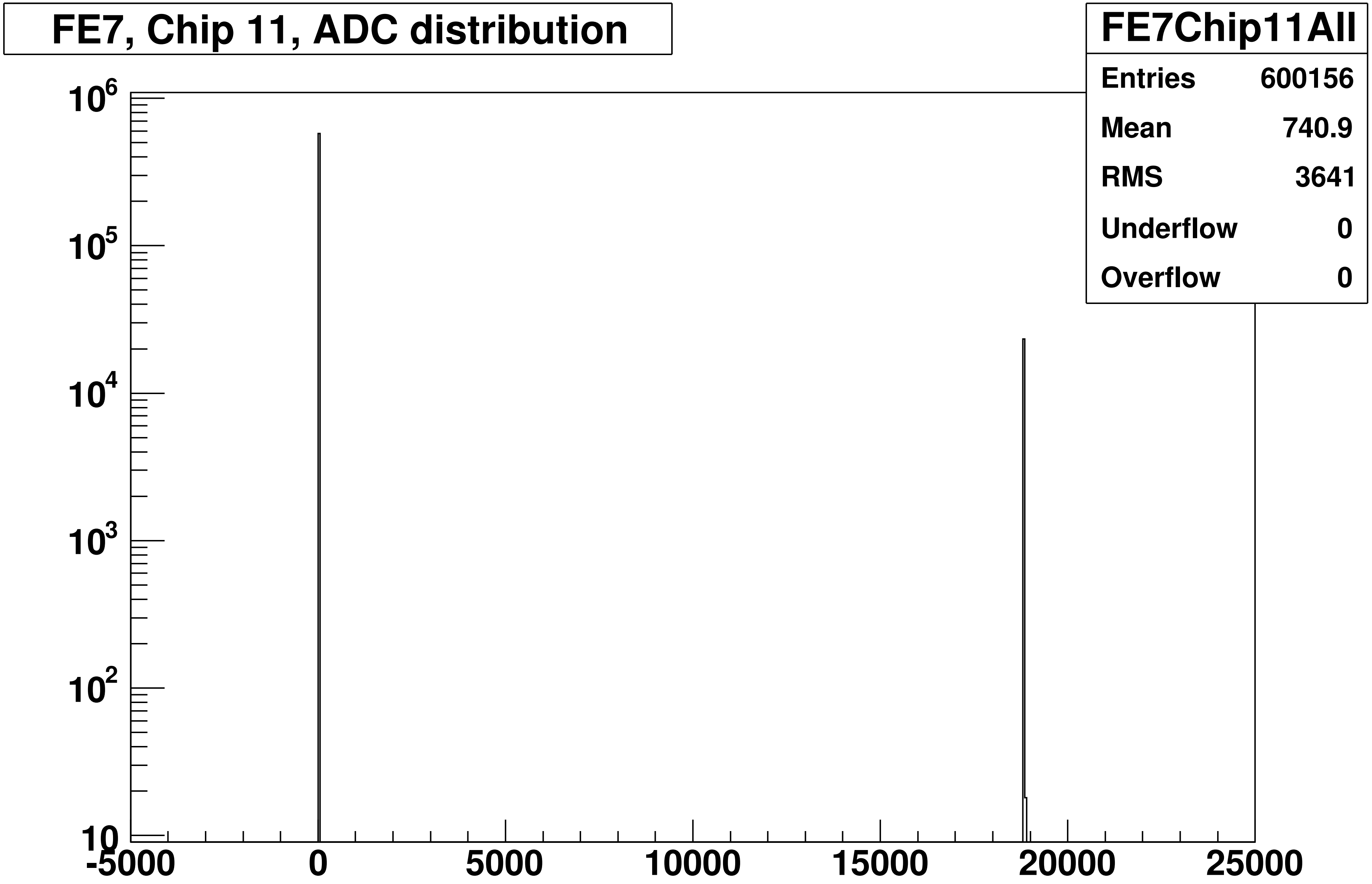


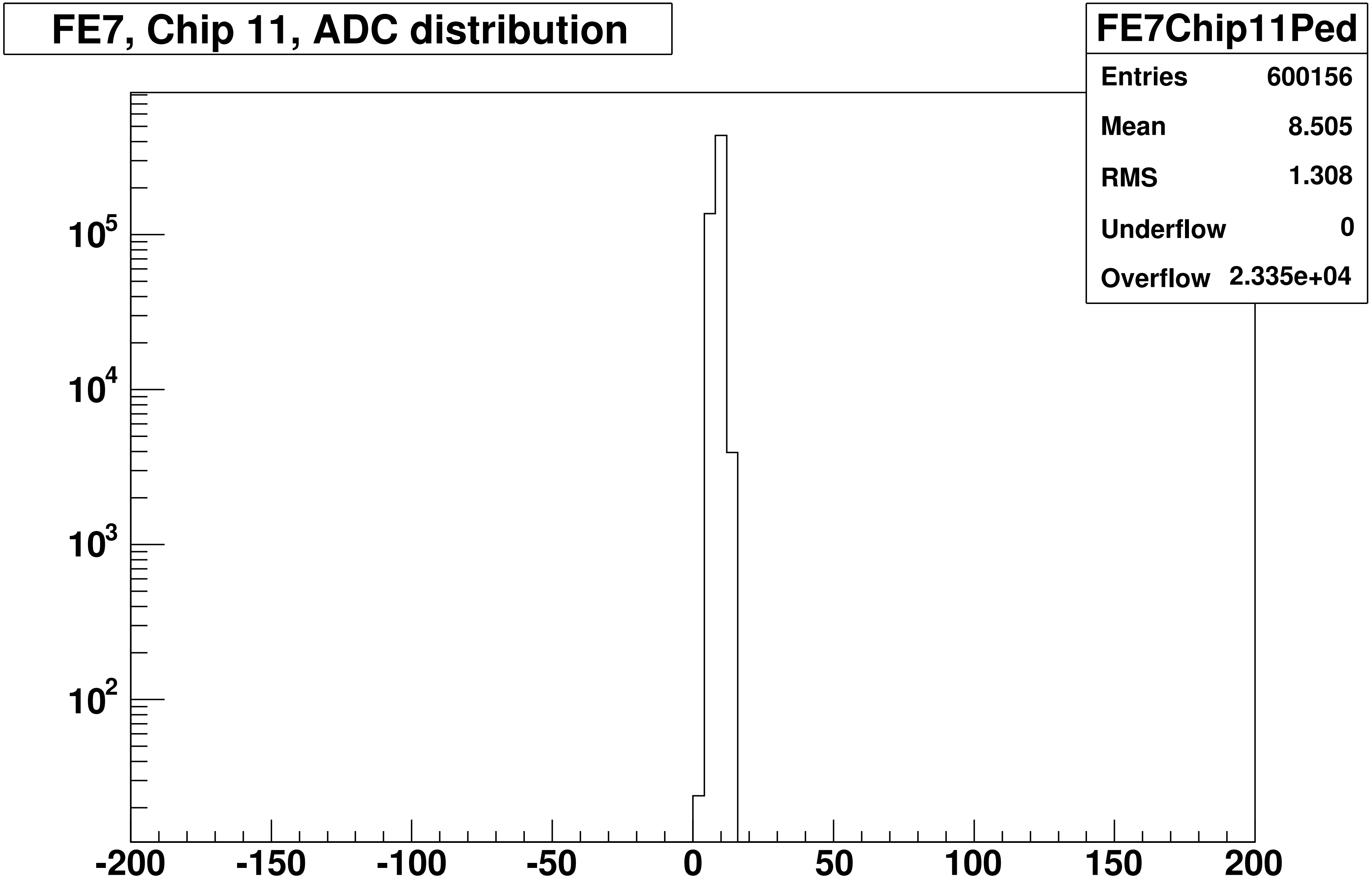
FE7, Chip 9, ADC distribution
FE7Chip09Sig
Entries 600156
Mean 1.893e+04
RMS 3.541
Underflow 5.768e+05
Overflow 0
10^4
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000

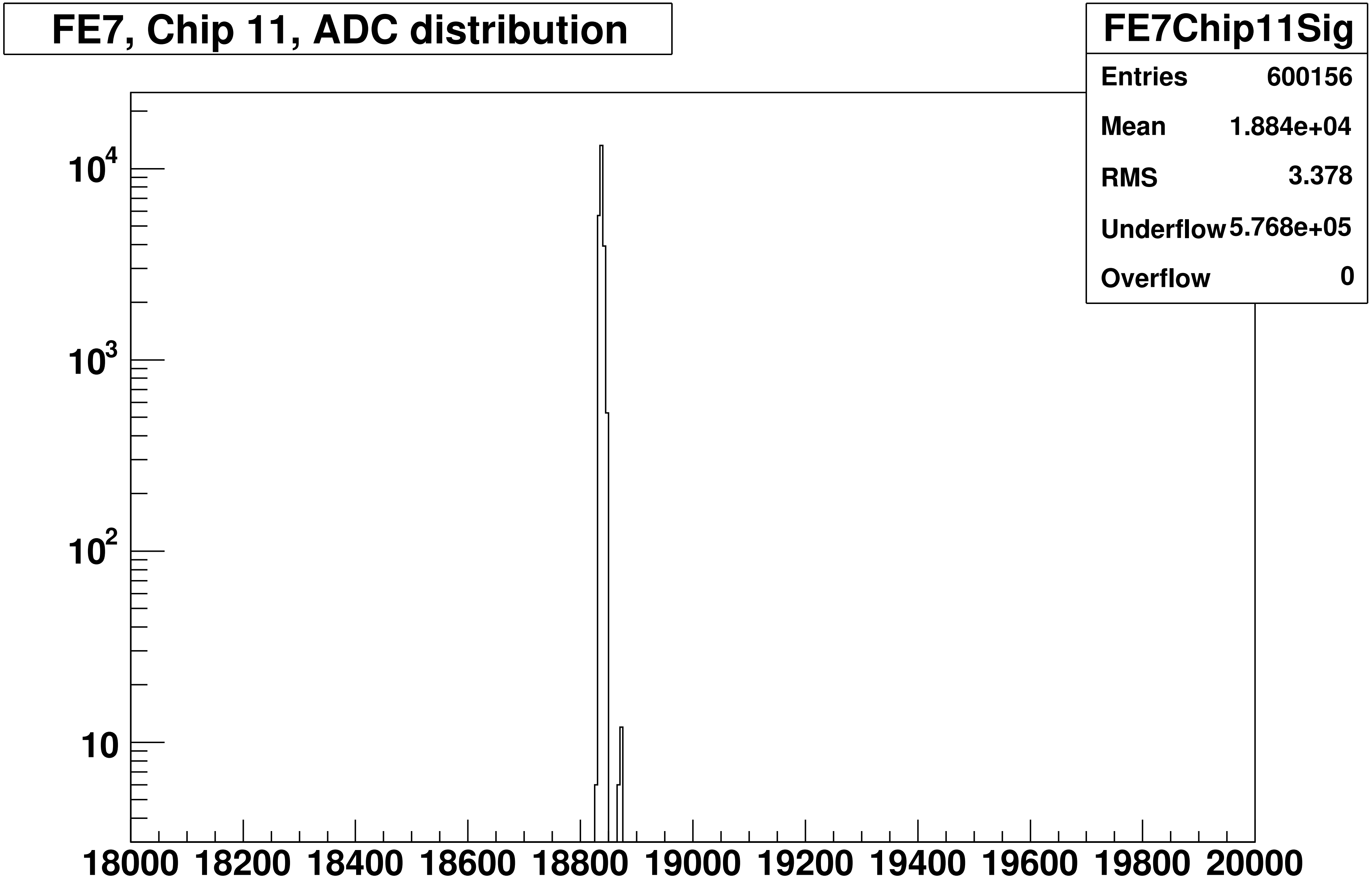

FE7, Chip 10, ADC distribution
FE7Chip10All
Entries 600156
Mean 721.8
RMS 3626
Underflow 0
Overflow 0
10^6
10^5
10^4
-5000
0
5000
10000
15000
20000
25000


FE7, Chip 10, ADC distribution
FE7Chip10Ped
Entries 600156
Mean -7.633
RMS 1.326
Underflow 0
Overflow 2.335e+04
10^5
10^4
10^3
10^2
-200
-150
-100
-50
0
50
100
150
200

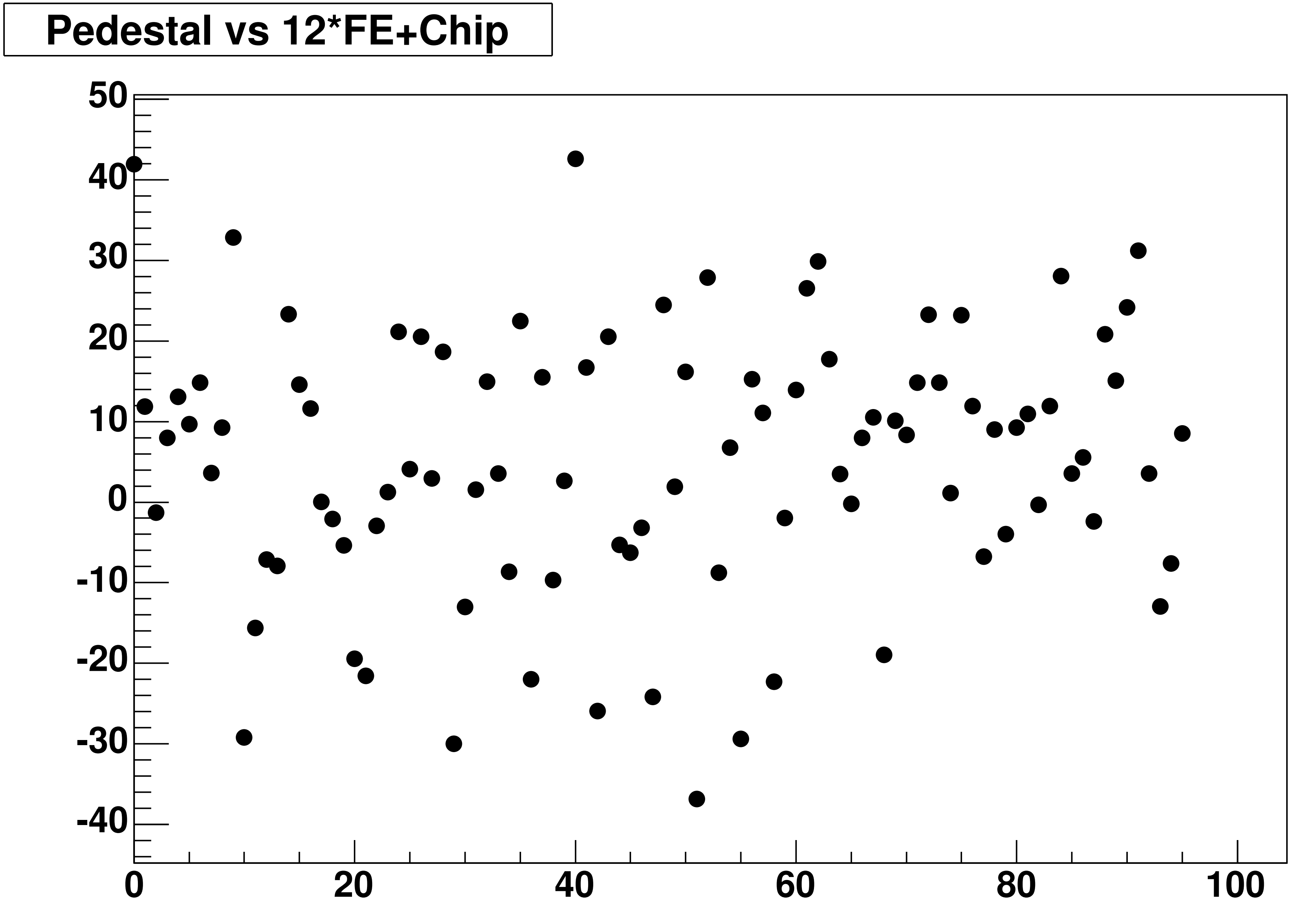

FE7, Chip 10, ADC distribution
FE7Chip10Sig
Entries 600156
Mean 1.874e+04
RMS 3.135
Underflow 5.768e+05
Overflow 0
10^4
10^3
10^2
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000

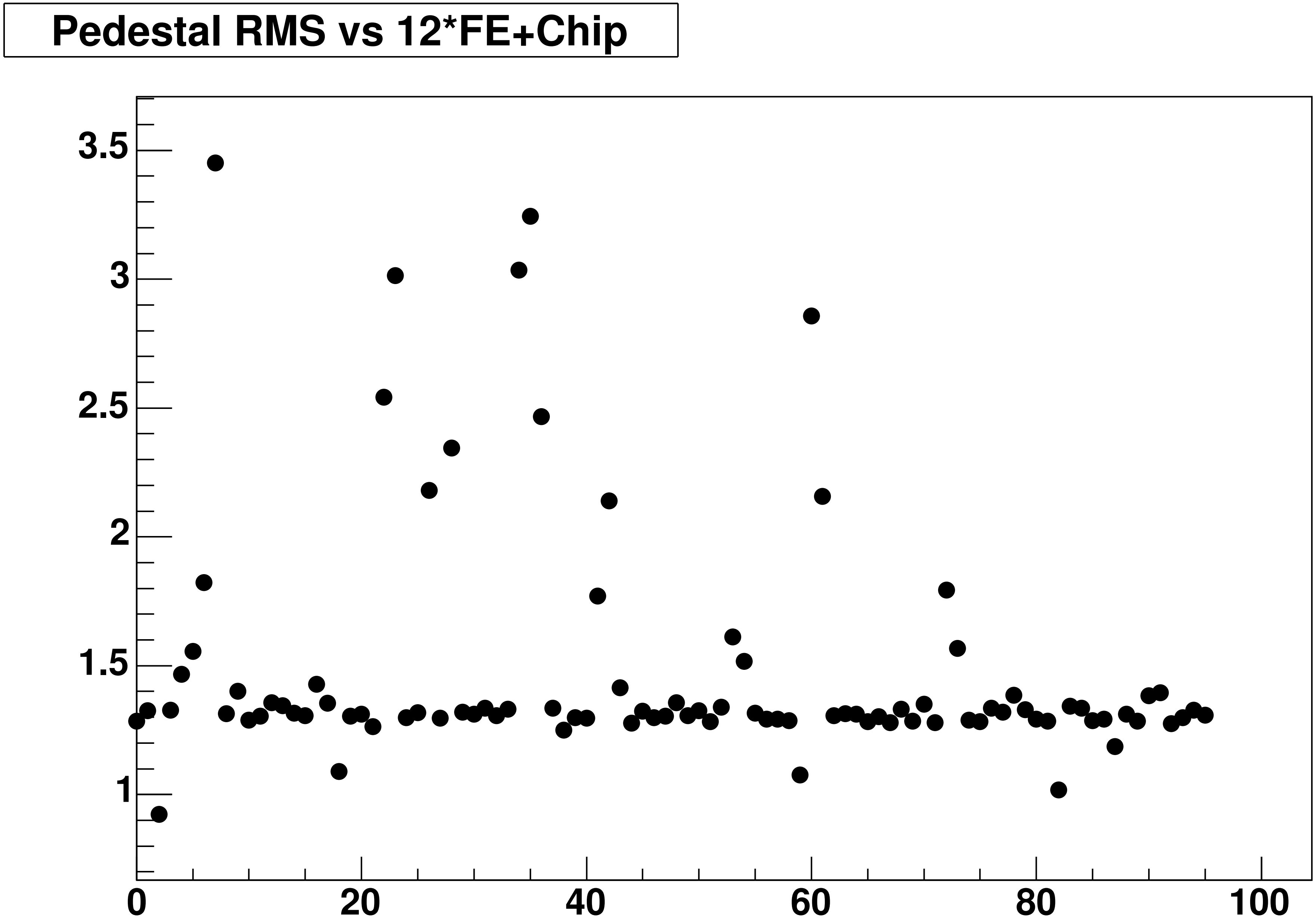

FE7, Chip 11, ADC distribution
FE7Chip11All
Entries 600156
Mean 740.9
RMS 3641
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE7, Chip 11, ADC distribution
FE7Chip11Ped
Entries 600156
Mean 8.505
RMS 1.308
Underflow 0
Overflow 2.335e+04
10^5
10^4
10^3
10^2
-200
-150
-100
-50
0
50
100
150
200

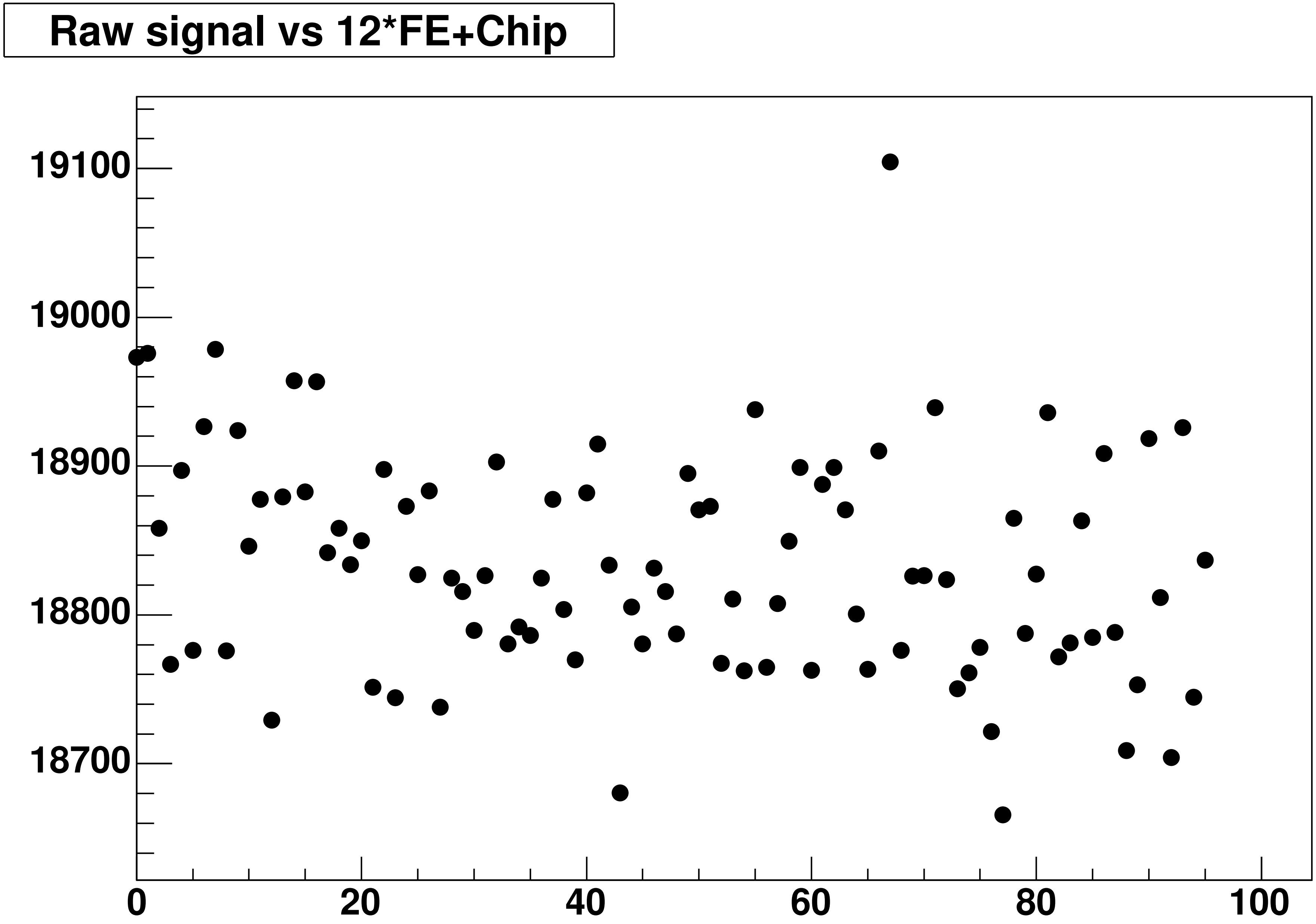


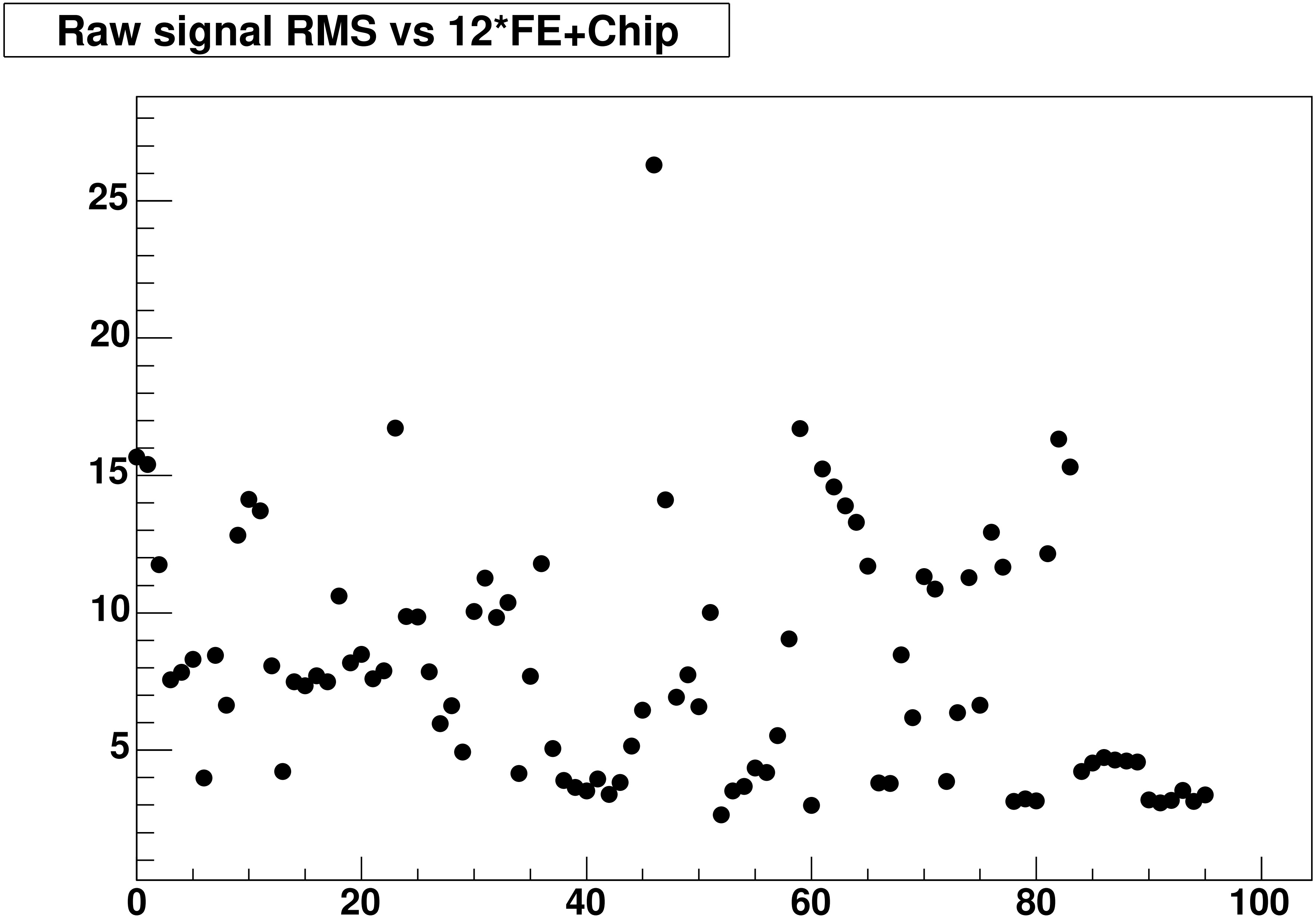
FE7, Chip 11, ADC distribution
FE7Chip11Sig
Entries 600156
Mean 1.884e+04
RMS 3.378
Underflow 5.768e+05
Overflow 0
10^4
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000

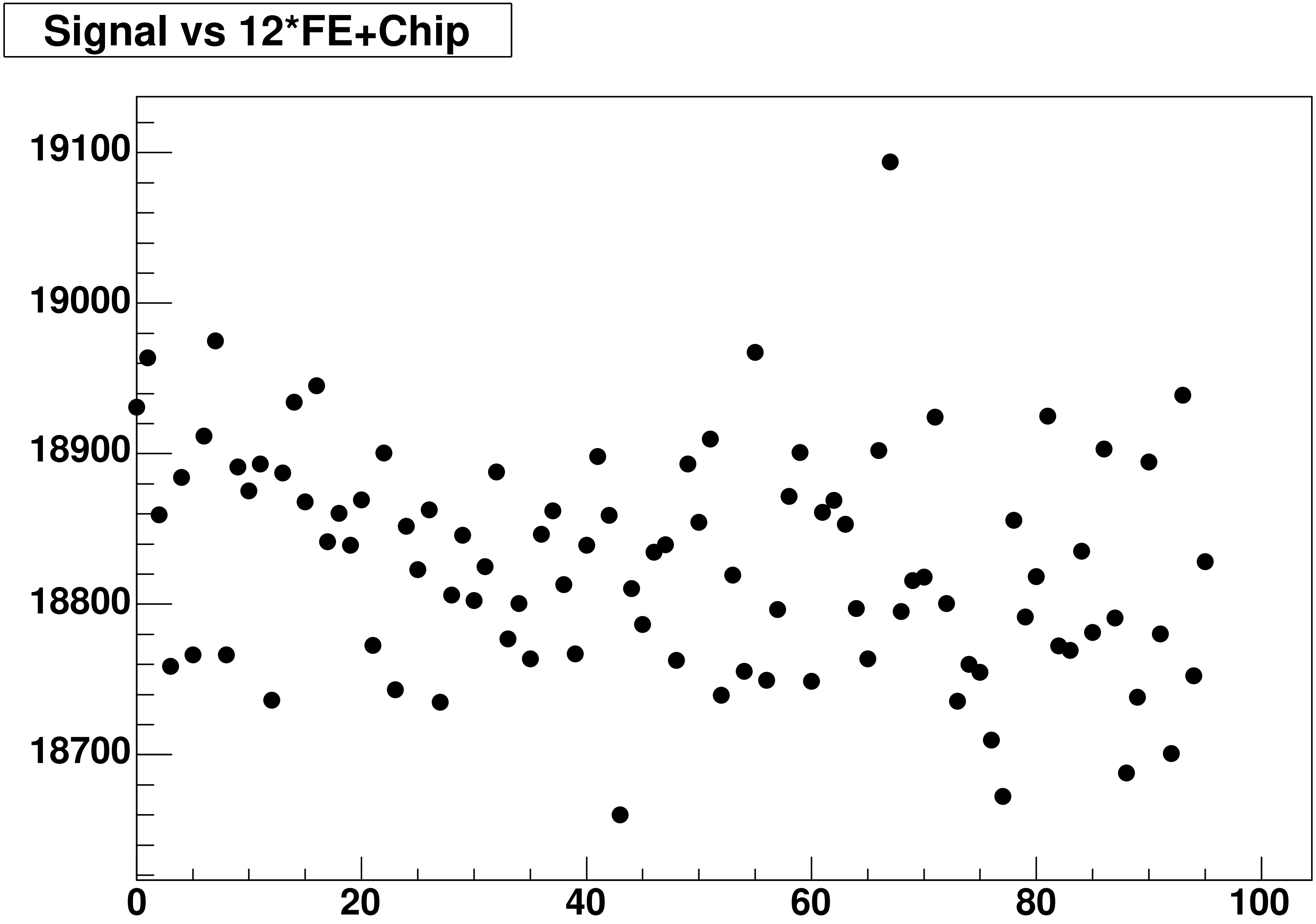

Pedestal vs 12*FE+Chip
50
40
30
20
10
0
-10
-20
-30
-40
0
20
40
60
80
100



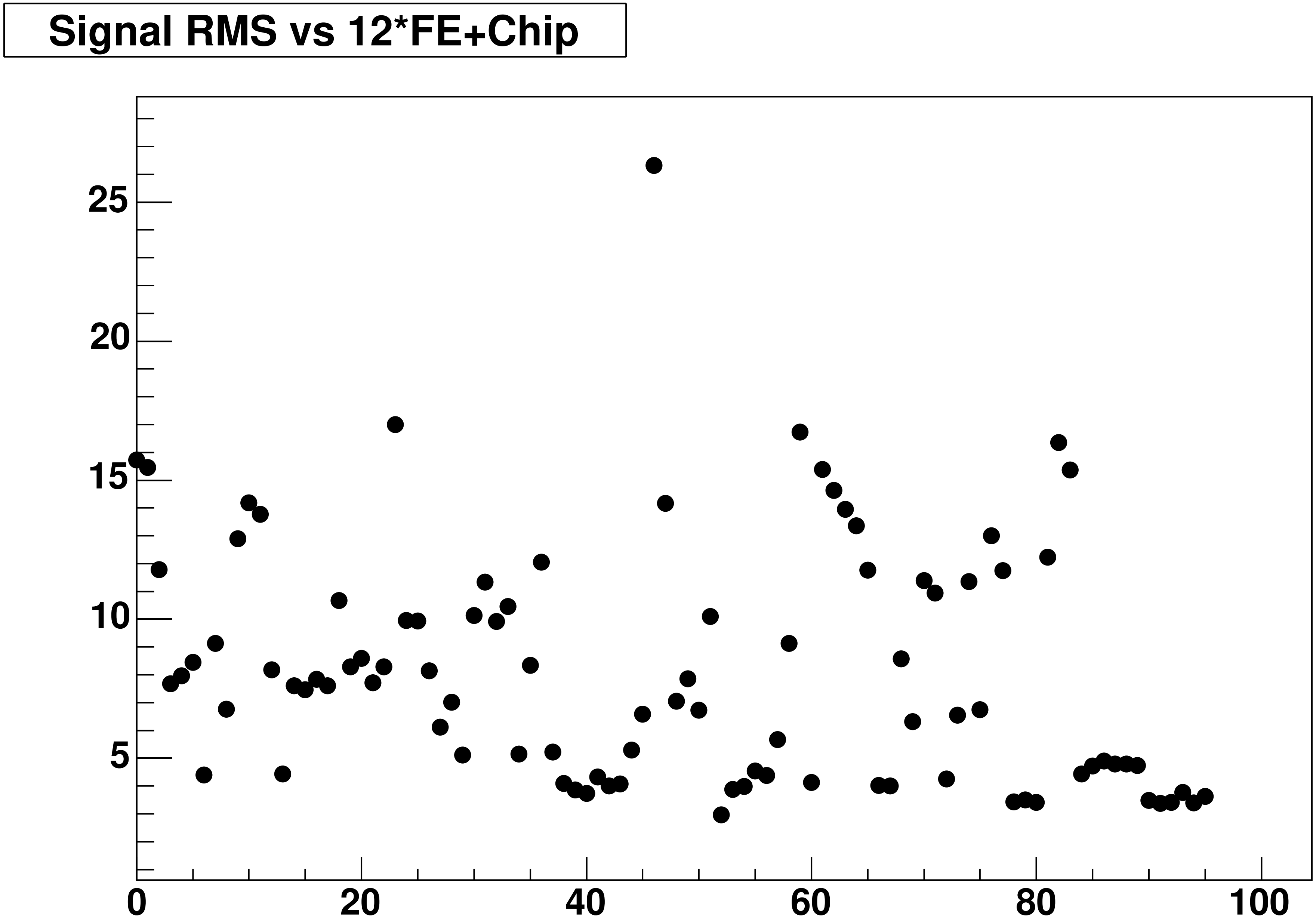
Pedestal RMS vs 12*FE+Chip
3.5
3
2.5
2
1.5
1
0
20
40
60
80
100


Raw signal vs 12*FE+Chip
19100
19000
18900
18800
18700
0
20
40
60
80
100


Raw signal RMS vs 12*FE+Chip
25
20
15
10
5
0
20
40
60
80
100



Signal vs 12*FE+Chip
19100
19000
18900
18800
18700
0
20
40
60
80
100



Signal RMS vs 12*FE+Chip
25
20
15
10
5
0
20
40
60
80
100