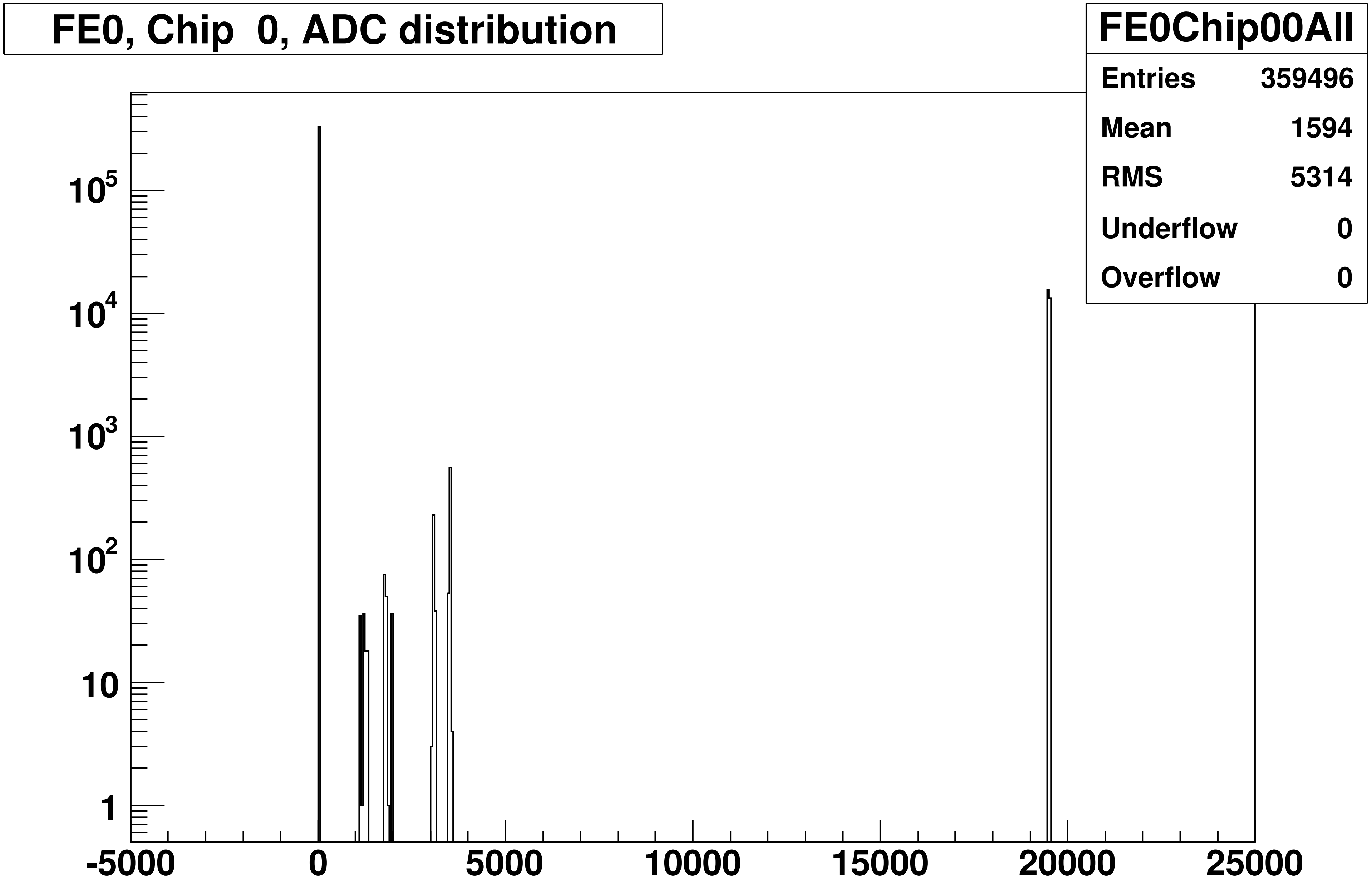
FE0, Chip 0, ADC distribution
FE0Chip00All
Entries 359496
Mean 1594
RMS 5314
Underflow 0
Overflow 0
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10^3
10^2
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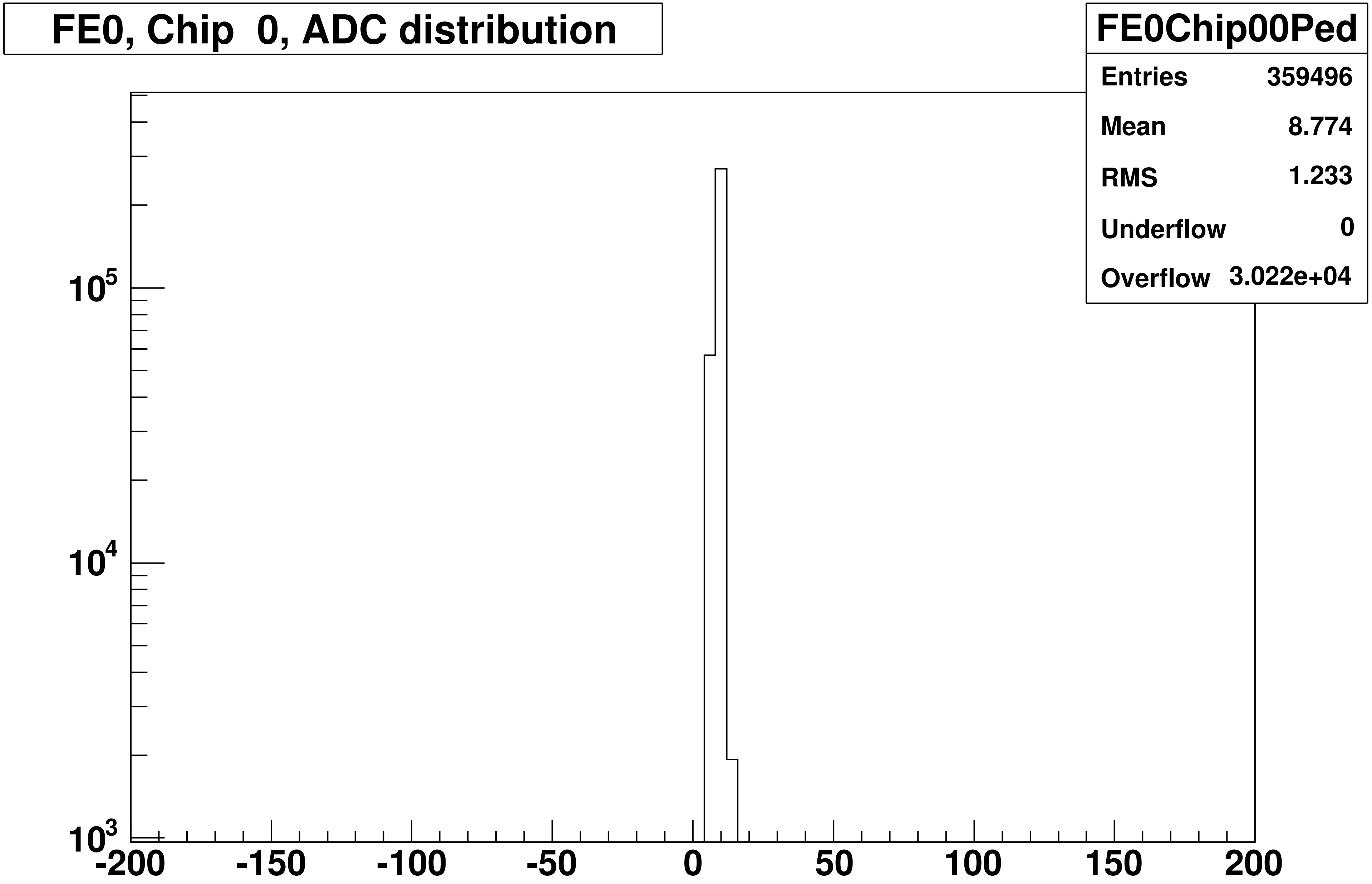
FE0, Chip 0, ADC distribution
FE0Chip00Ped
Entries 359496
Mean 8.774
RMS 1.233
Underflow 0
Overflow 3.022e+04
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10^4
10^3
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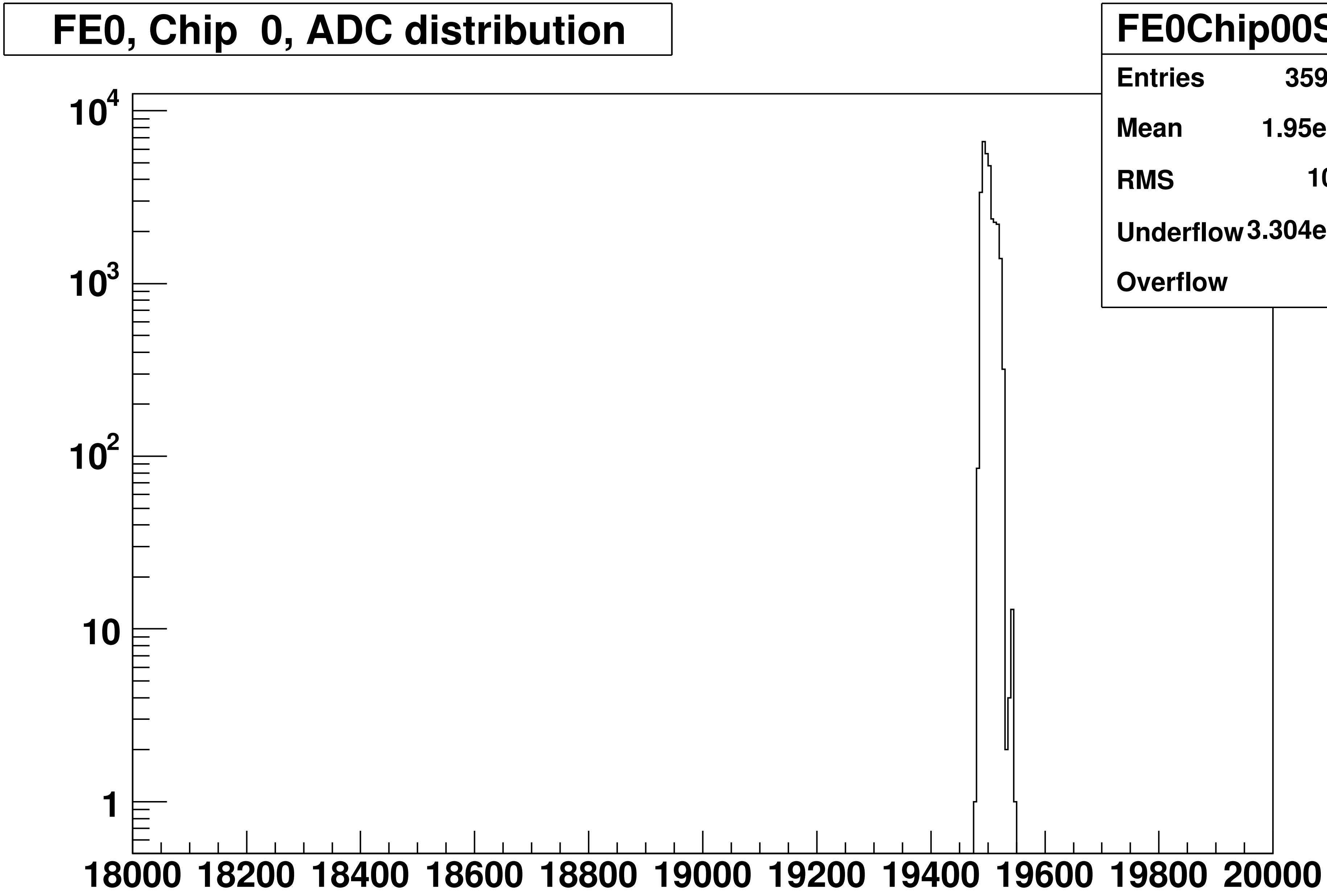
FE0, Chip 0, ADC distribution
FE0Chip00Sig
Entries 359496
Mean 1.95e+04
RMS 10.25
Underflow 3.304e+05
Overflow 0
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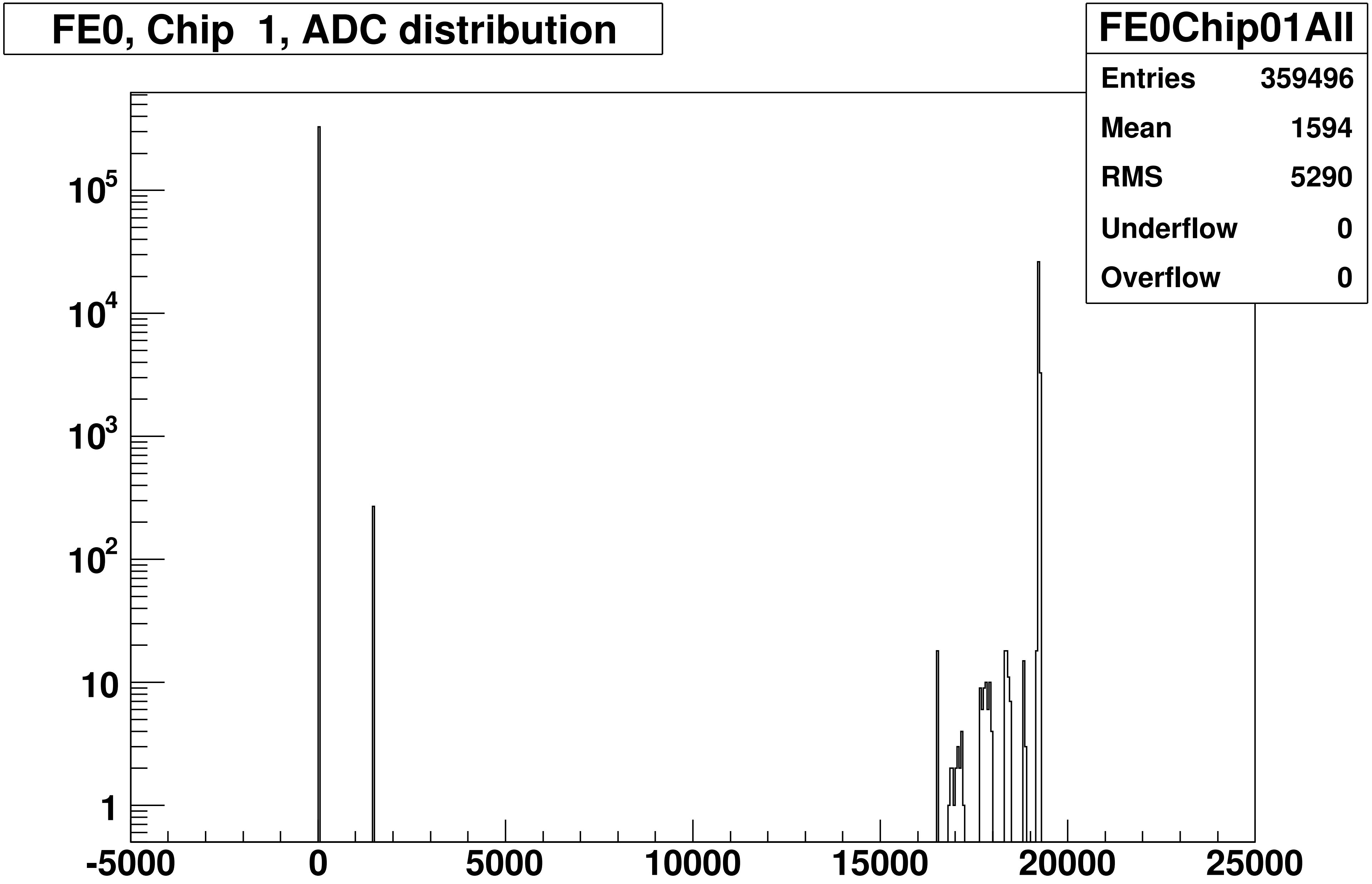

FE0, Chip 1, ADC distribution
FE0Chip01All
Entries 359496
Mean 1594
RMS 5290
Underflow 0
Overflow 0
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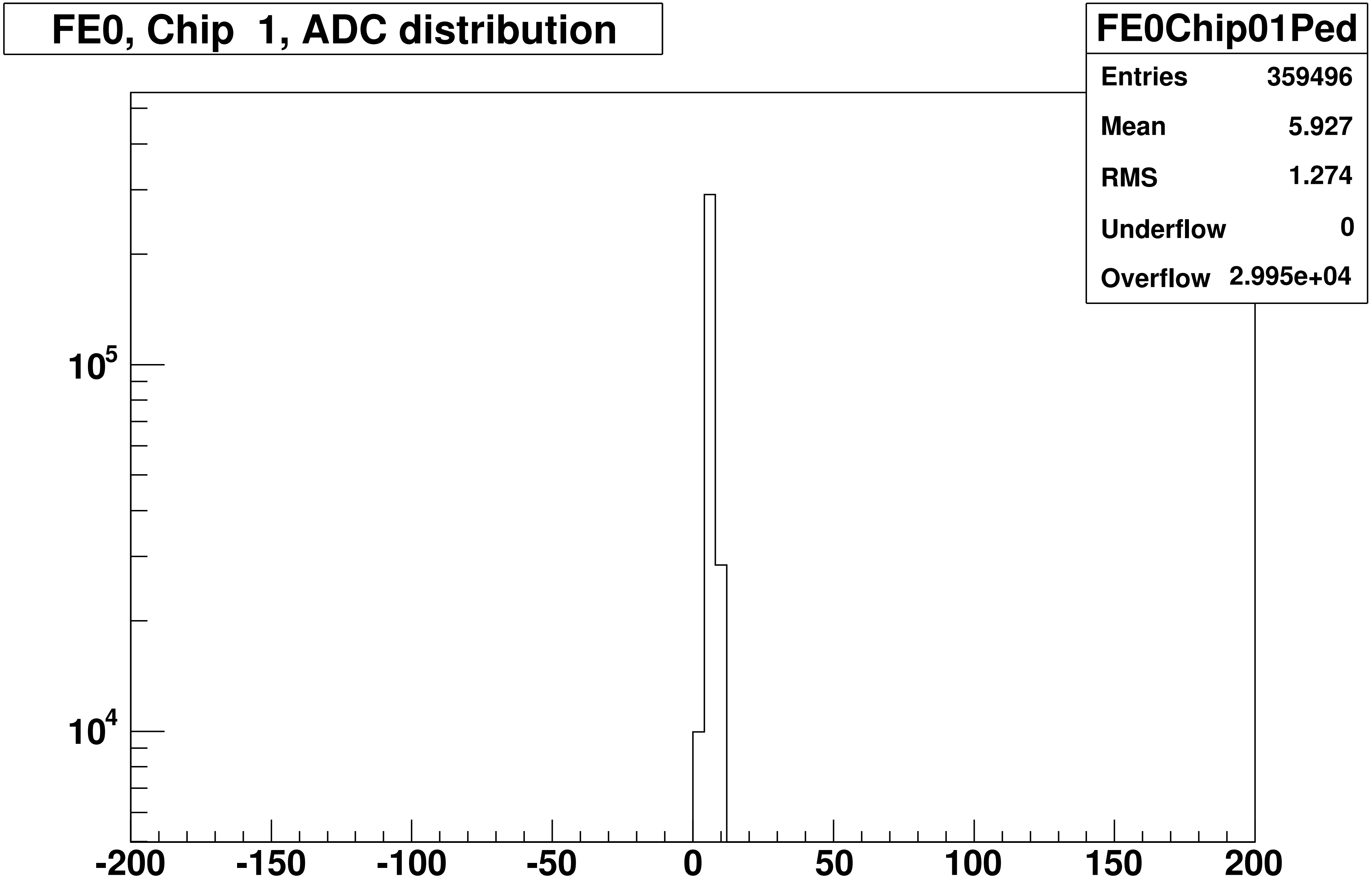
FE0, Chip 1, ADC distribution
FE0Chip01Ped
Entries 359496
Mean 5.927
RMS 1.274
Underflow 0
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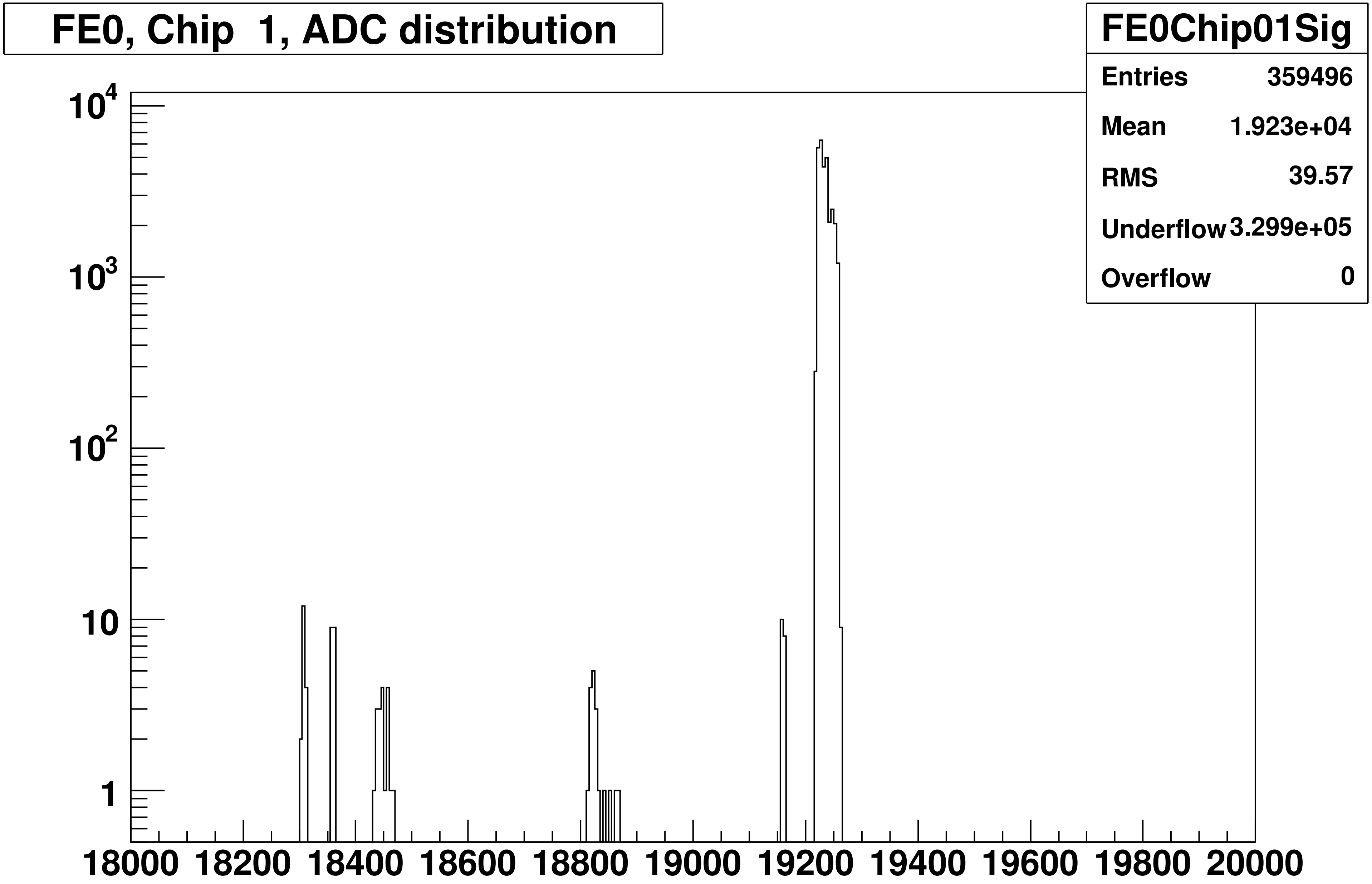
100
150
200


FE0, Chip 1, ADC distribution
FE0Chip01Sig
Entries 359496
Mean 1.923e+04
RMS 39.57
Underflow 3.299e+05
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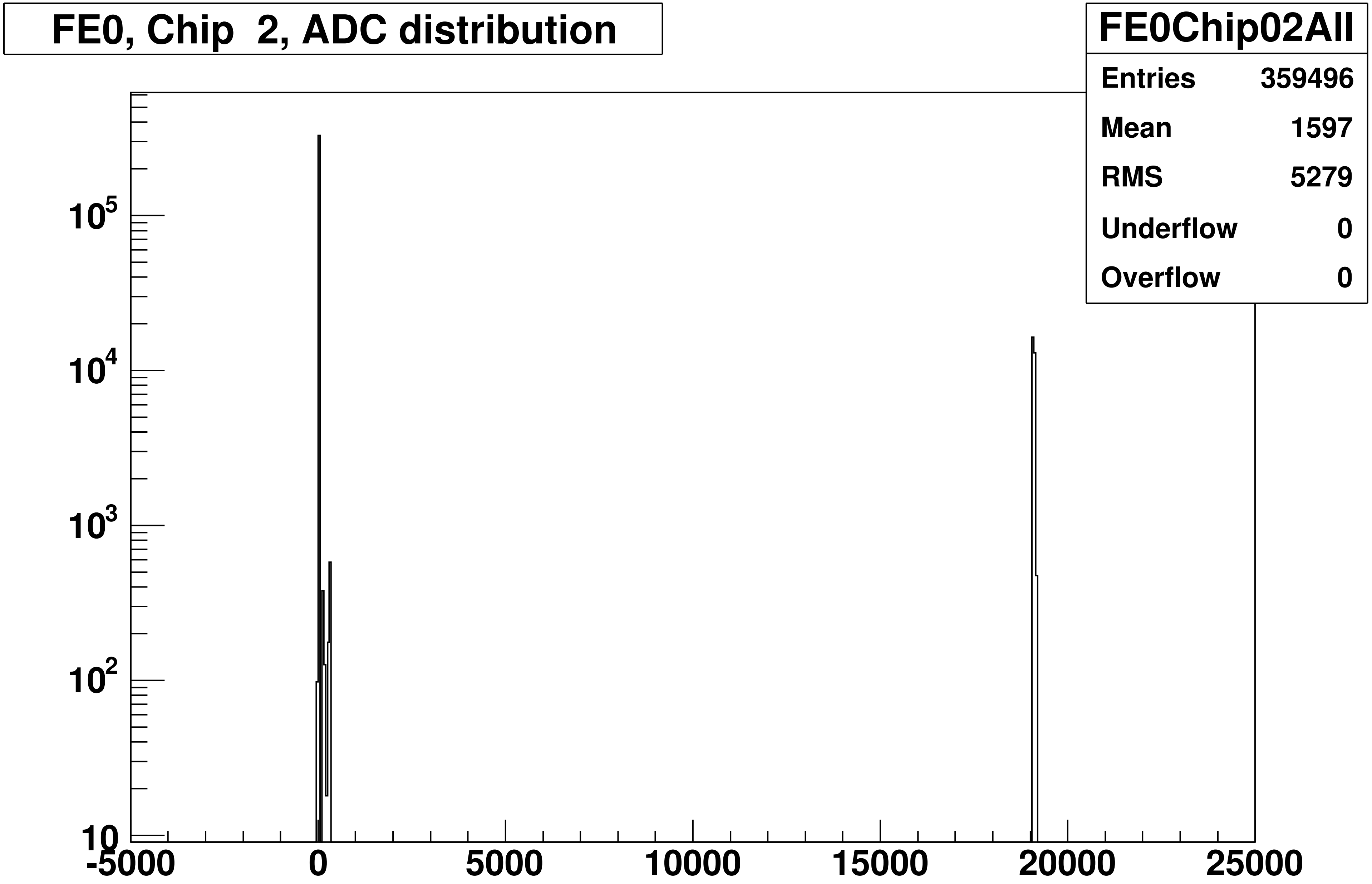
FE0, Chip 2, ADC distribution
FE0Chip02All
Entries 359496
Mean 1597
RMS 5279
Underflow 0
Overflow 0
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10^4
10^3
10^2
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15000
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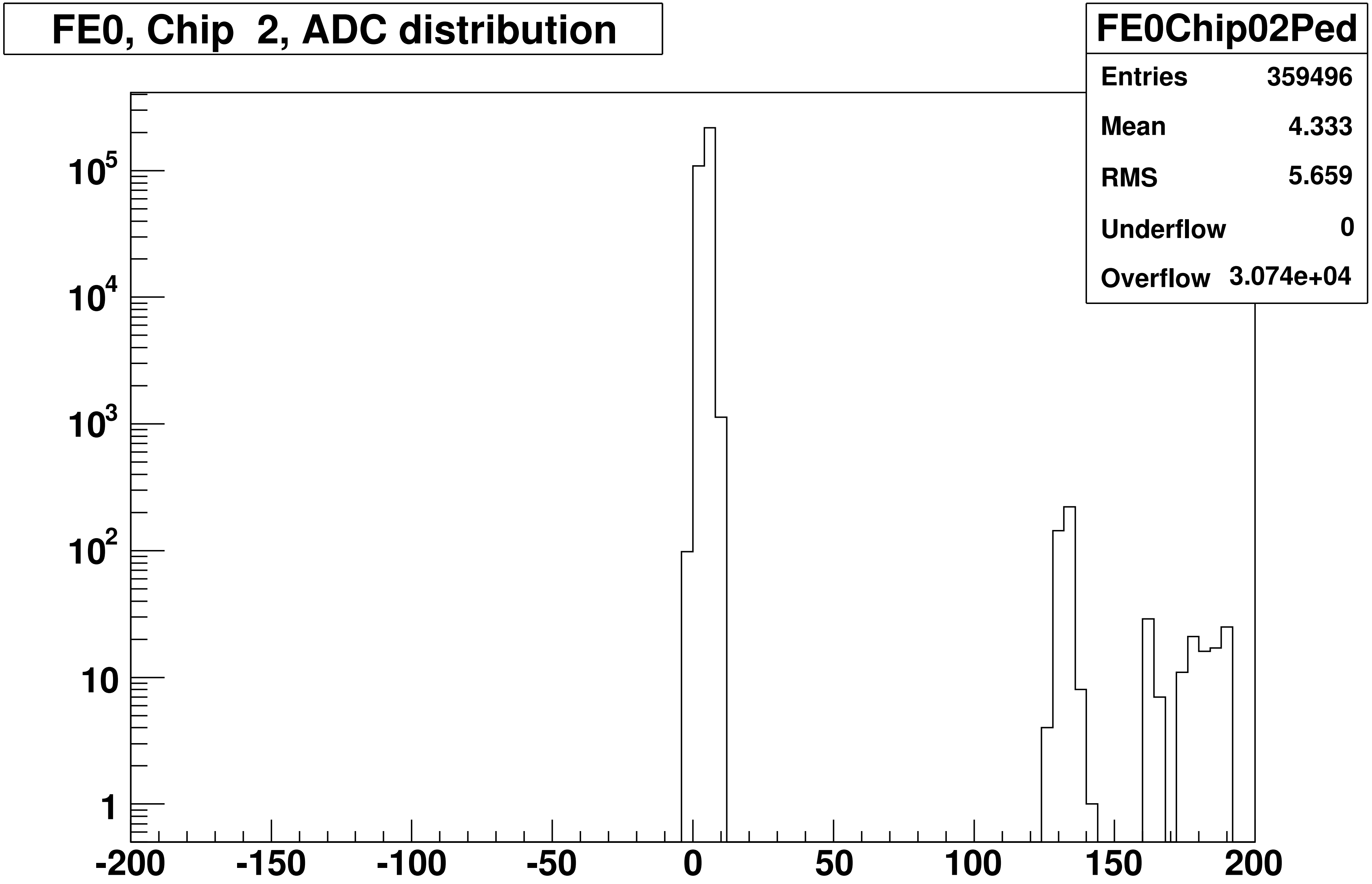
FE0, Chip 2, ADC distribution
FE0Chip02Ped
Entries 359496
Mean 4.333
RMS 5.659
Underflow 0
Overflow 3.074e+04
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10^3
10^2
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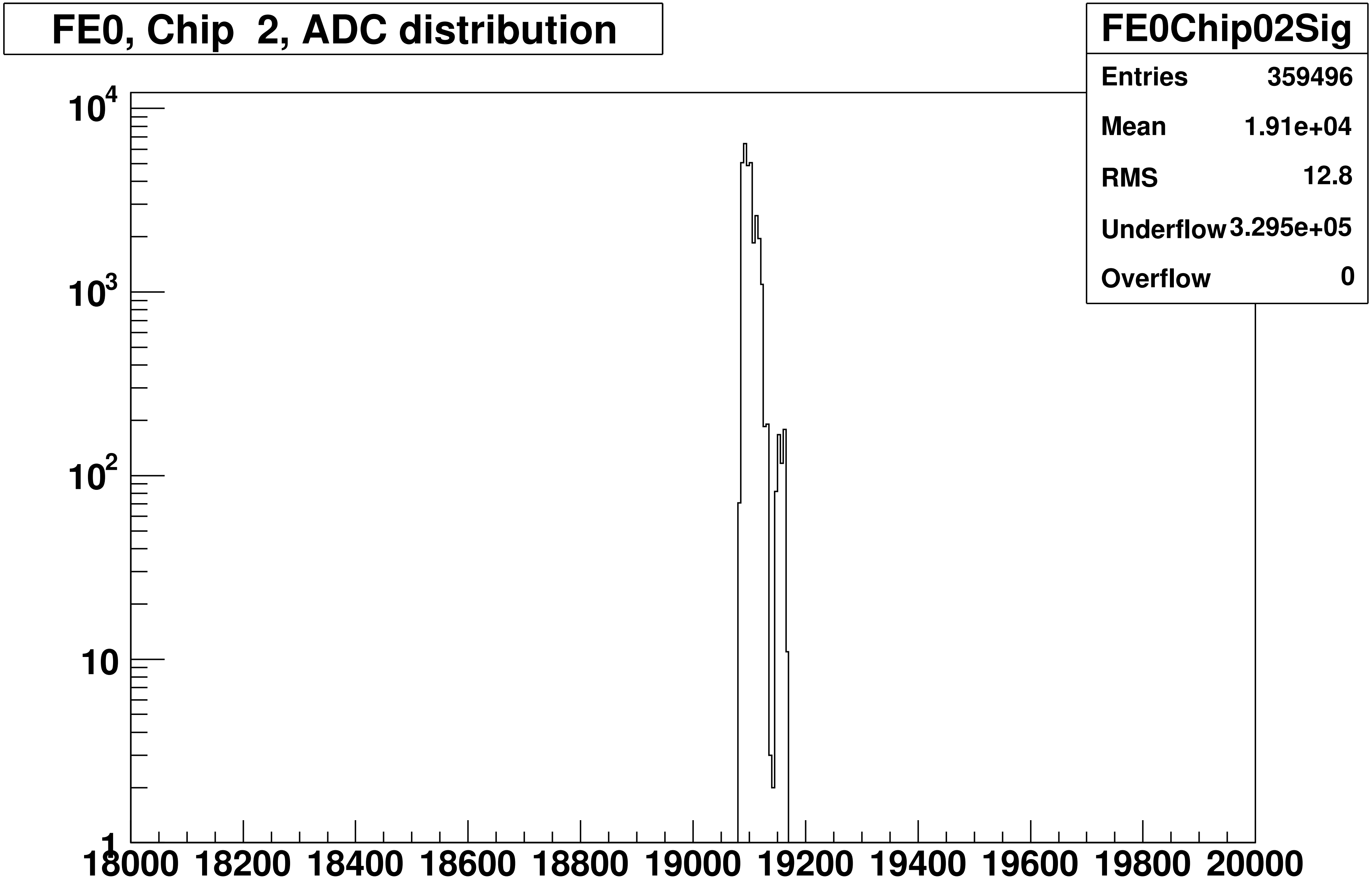
FE0, Chip 2, ADC distribution
FE0Chip02Sig
Entries 359496
Mean 1.91e+04
RMS 12.8
Underflow 3.295e+05
Overflow 0
10^4
10^3
10^2
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1
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18400
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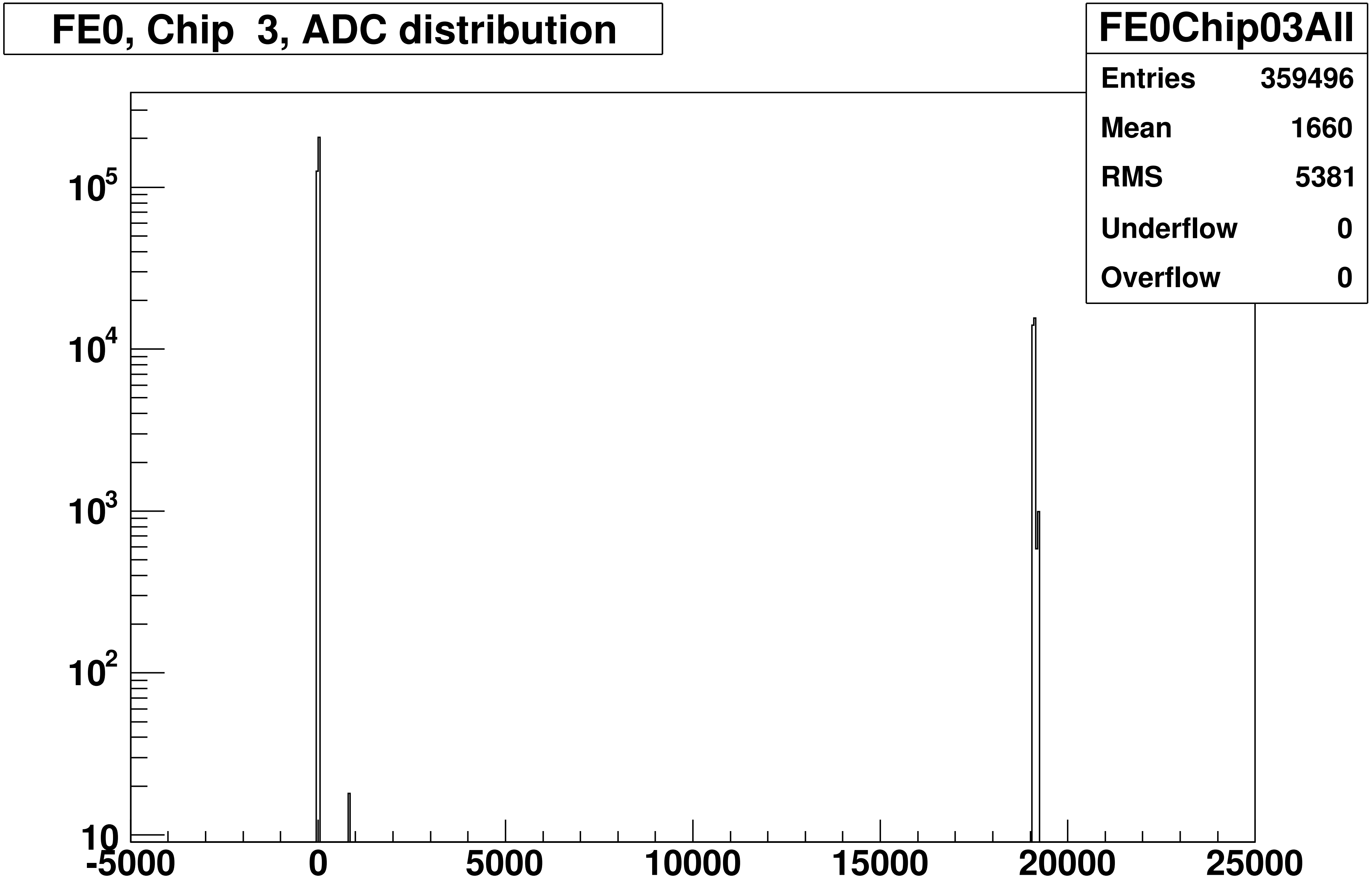
FE0, Chip 3, ADC distribution
FE0Chip03All
Entries 359496
Mean 1660
RMS 5381
Underflow 0
Overflow 0
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10^2
10^3
10^4
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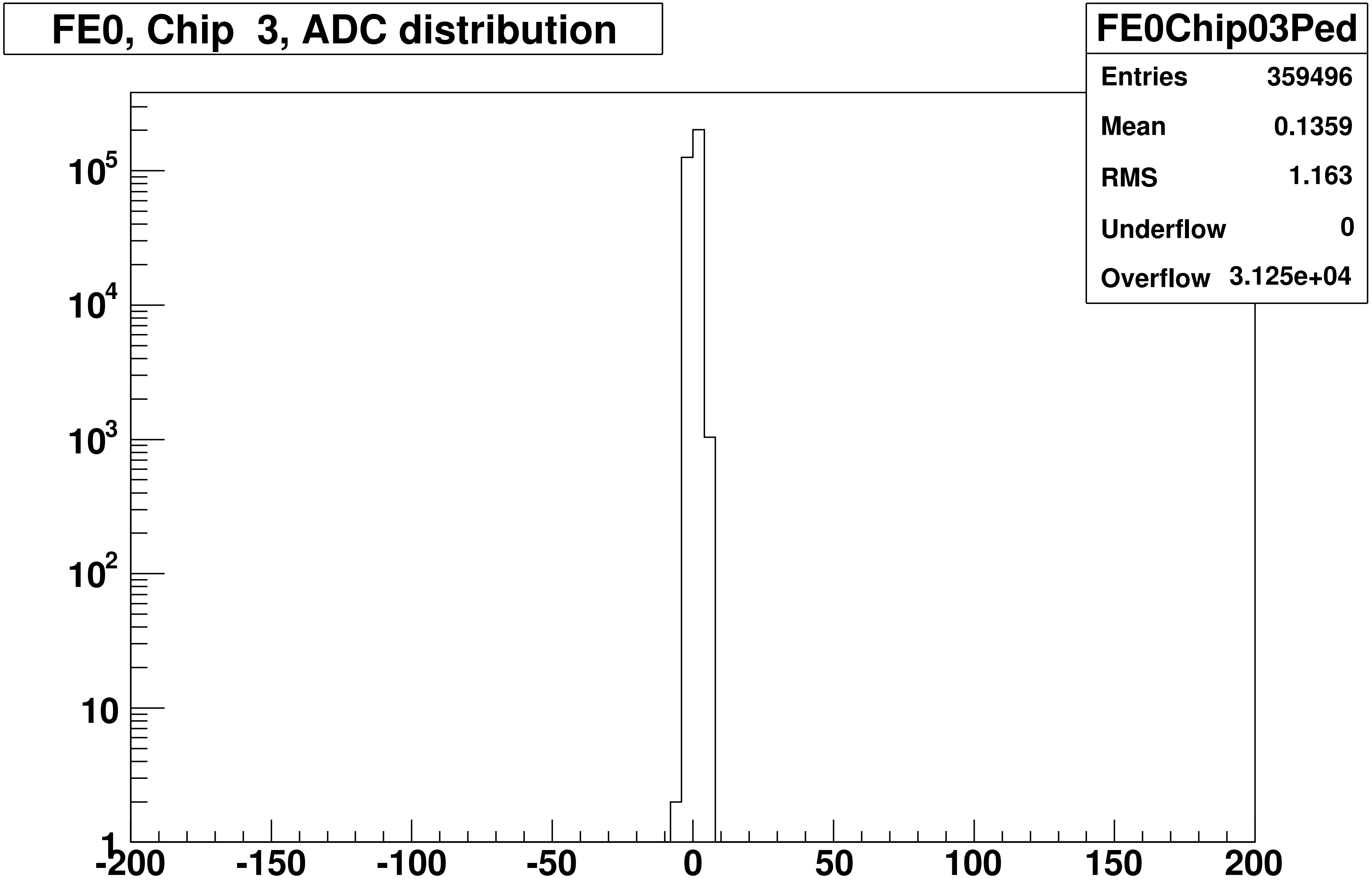
FE0, Chip 3, ADC distribution
FE0Chip03Ped
Entries 359496
Mean 0.1359
RMS 1.163
Underflow 0
Overflow 3.125e+04
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150
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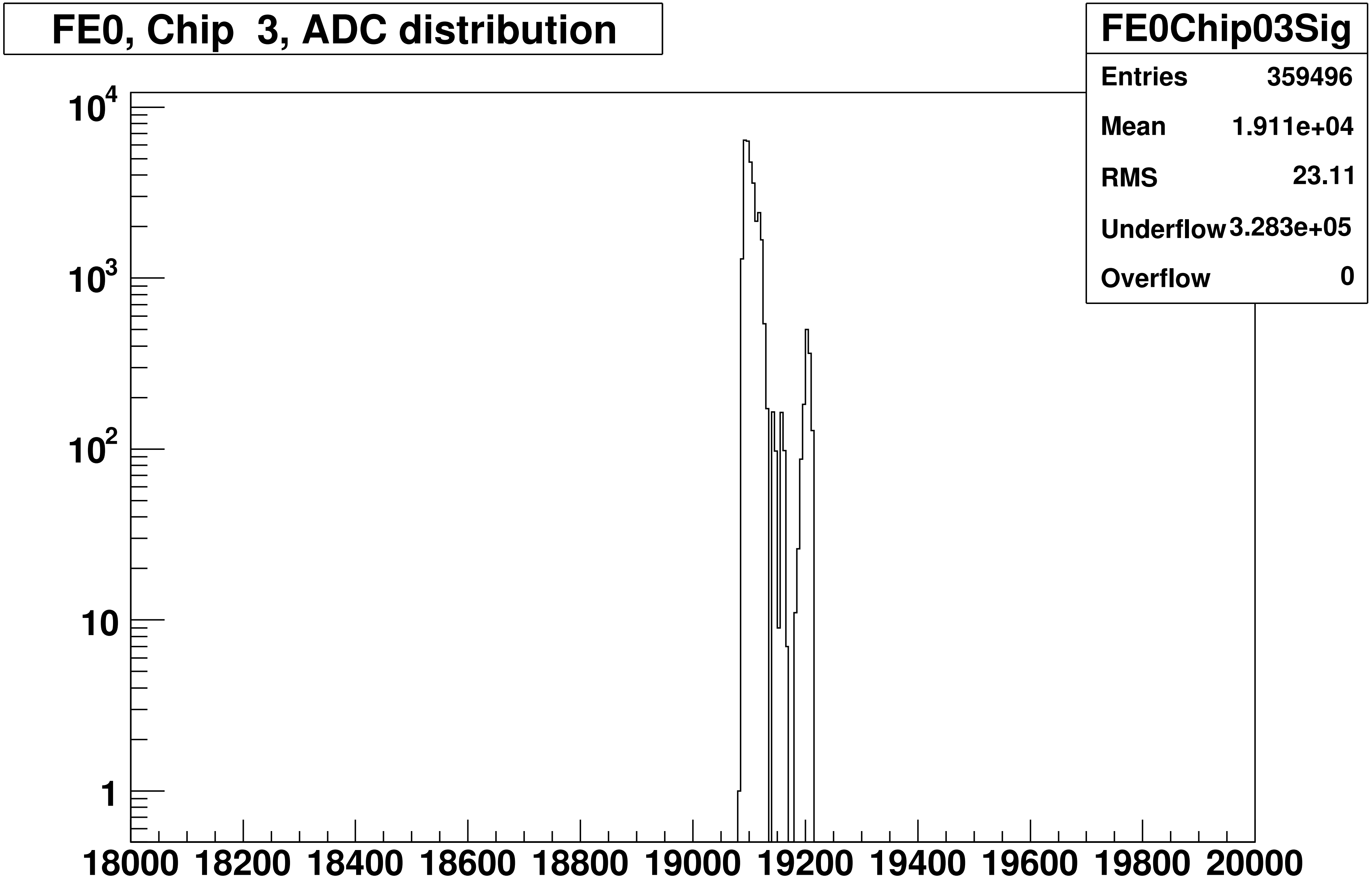
FE0, Chip 3, ADC distribution
FE0Chip03Sig
Entries 359496
Mean 1.911e+04
RMS 23.11
Underflow 3.283e+05
Overflow 0
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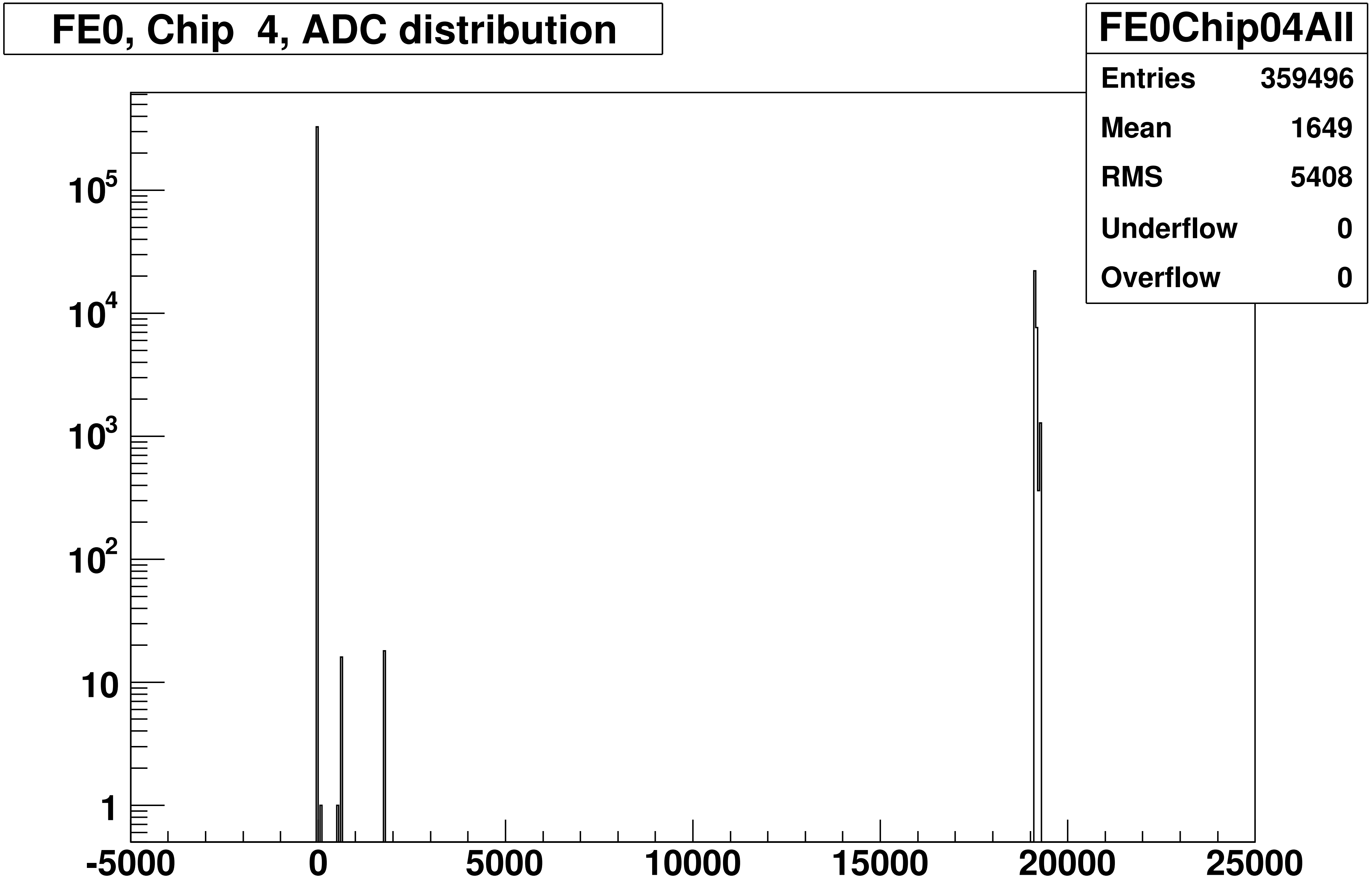
FE0, Chip 4, ADC distribution
FE0Chip04All
Entries 359496
Mean 1649
RMS 5408
Underflow 0
Overflow 0
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10^3
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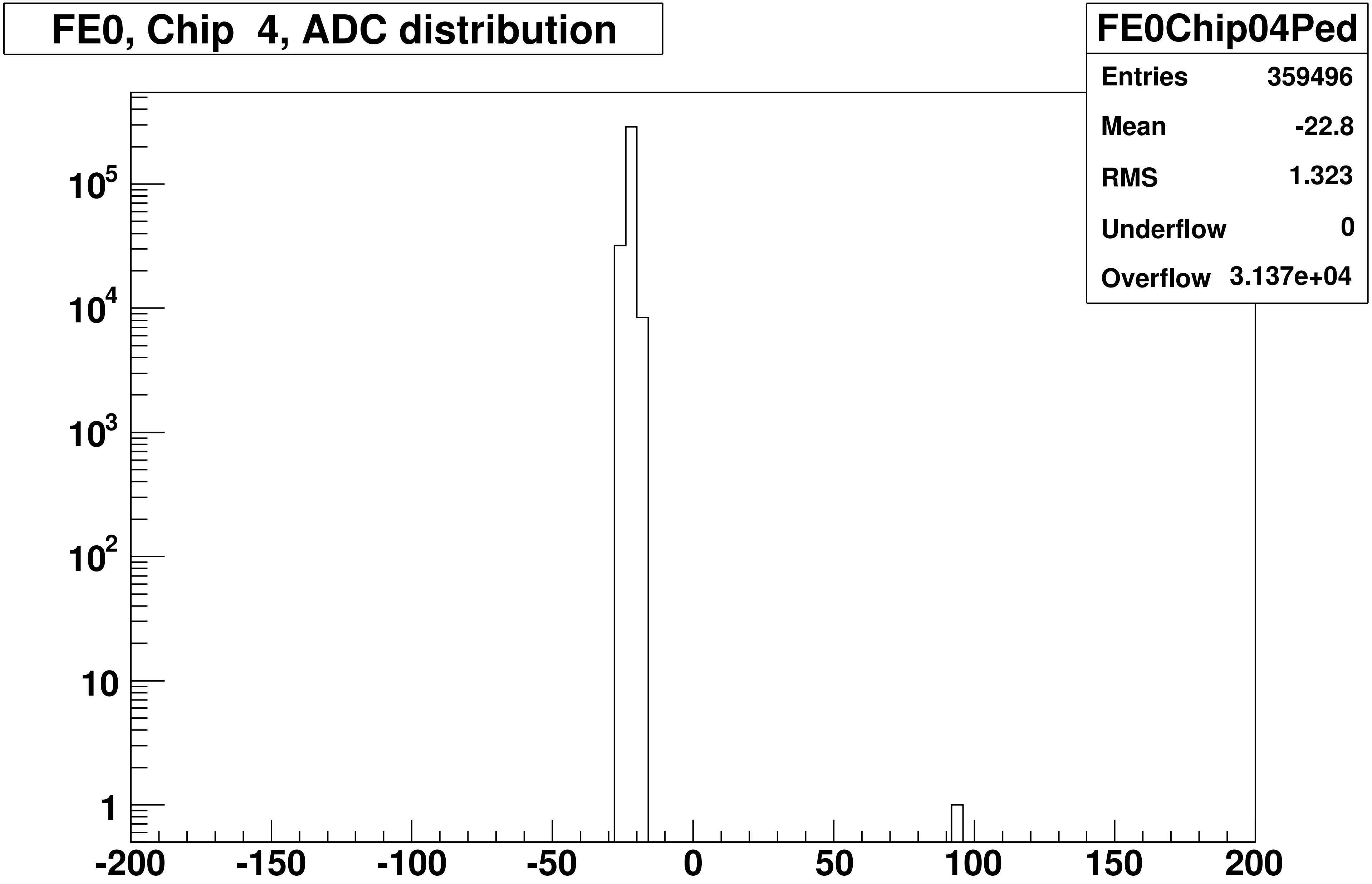
FE0, Chip 4, ADC distribution
FE0Chip04Ped
Entries 359496
Mean -22.8
RMS 1.323
Underflow 0
Overflow 3.137e+04
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150
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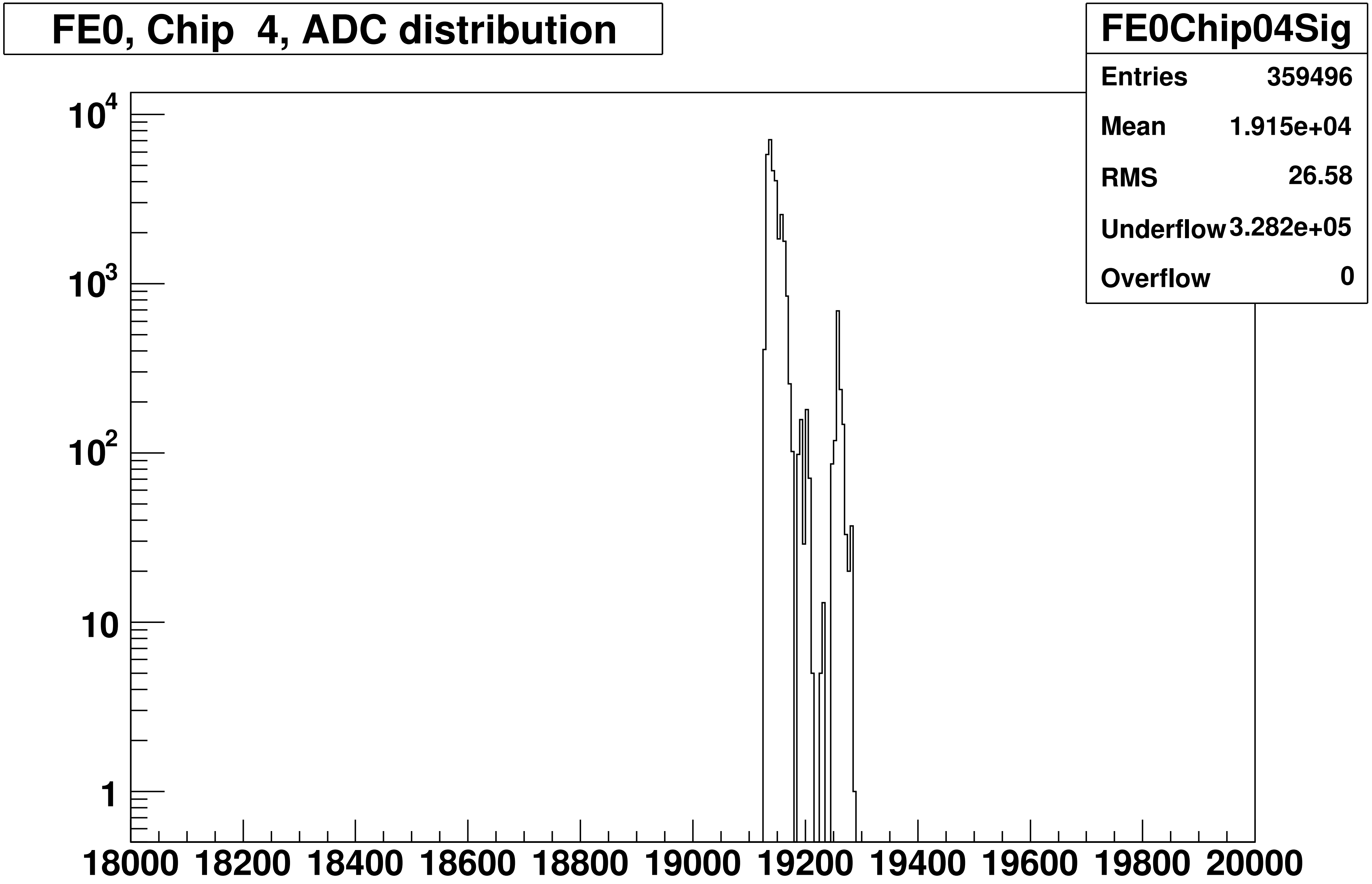
FE0, Chip 4, ADC distribution
FE0Chip04Sig
Entries 359496
Mean 1.915e+04
RMS 26.58
Underflow 3.282e+05
Overflow 0
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10^3
10^2
10
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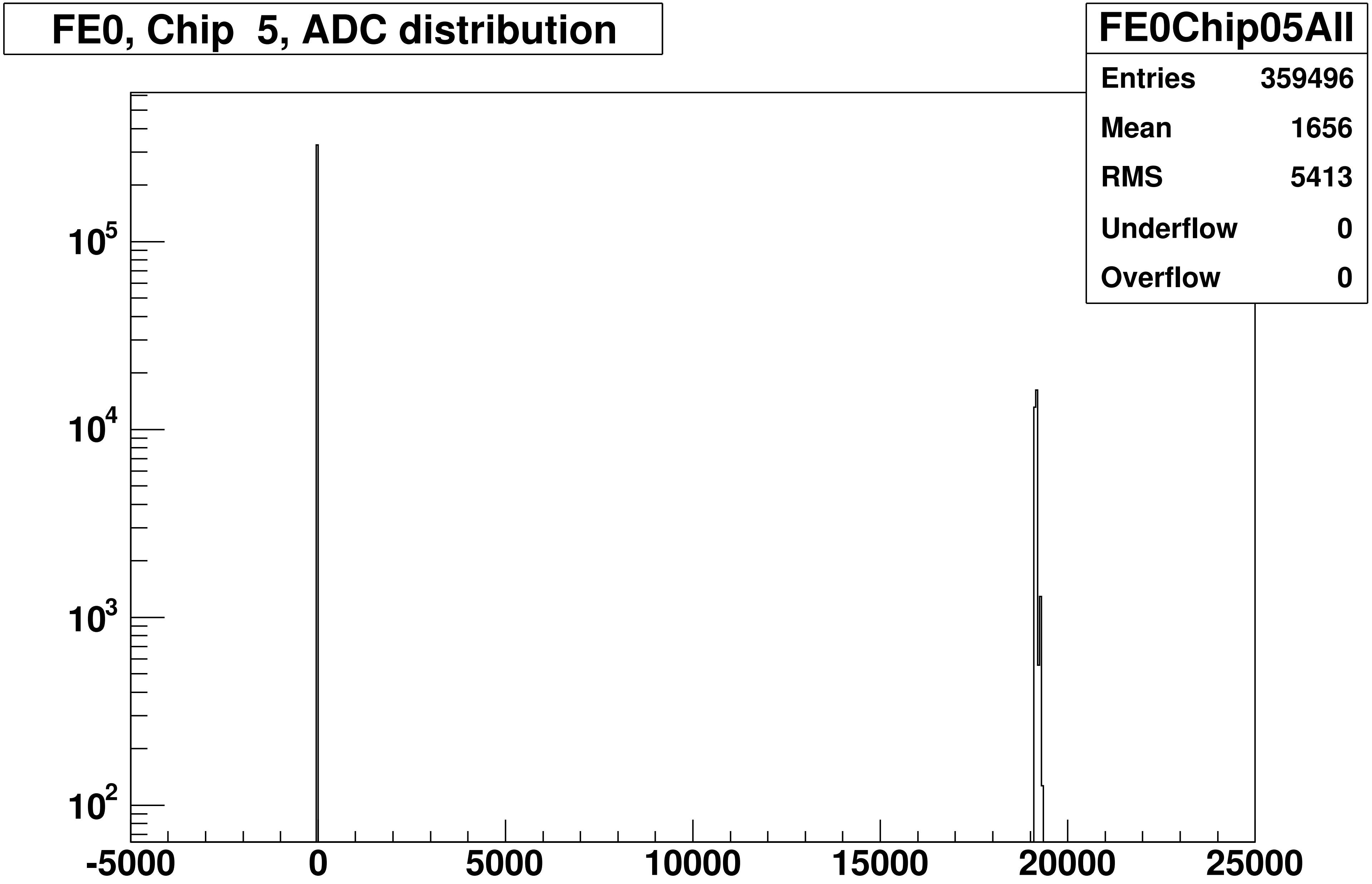
FE0, Chip 5, ADC distribution
FE0Chip05All
Entries 359496
Mean 1656
RMS 5413
Underflow 0
Overflow 0
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10^3
10^2
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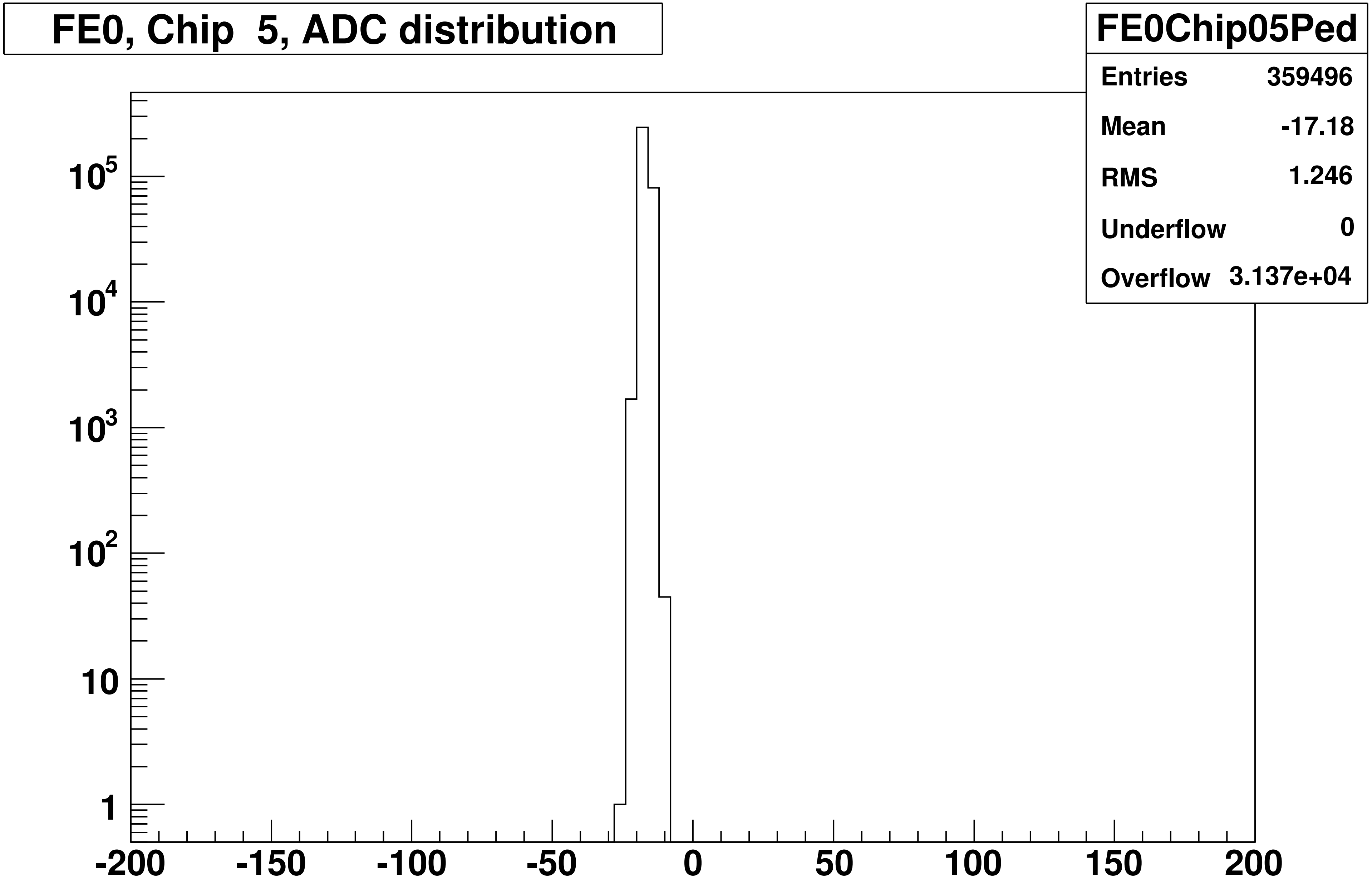
15000
20000
25000


FE0, Chip 5, ADC distribution
FE0Chip05Ped
Entries 359496
Mean -17.18
RMS 1.246
Underflow 0
Overflow 3.137e+04
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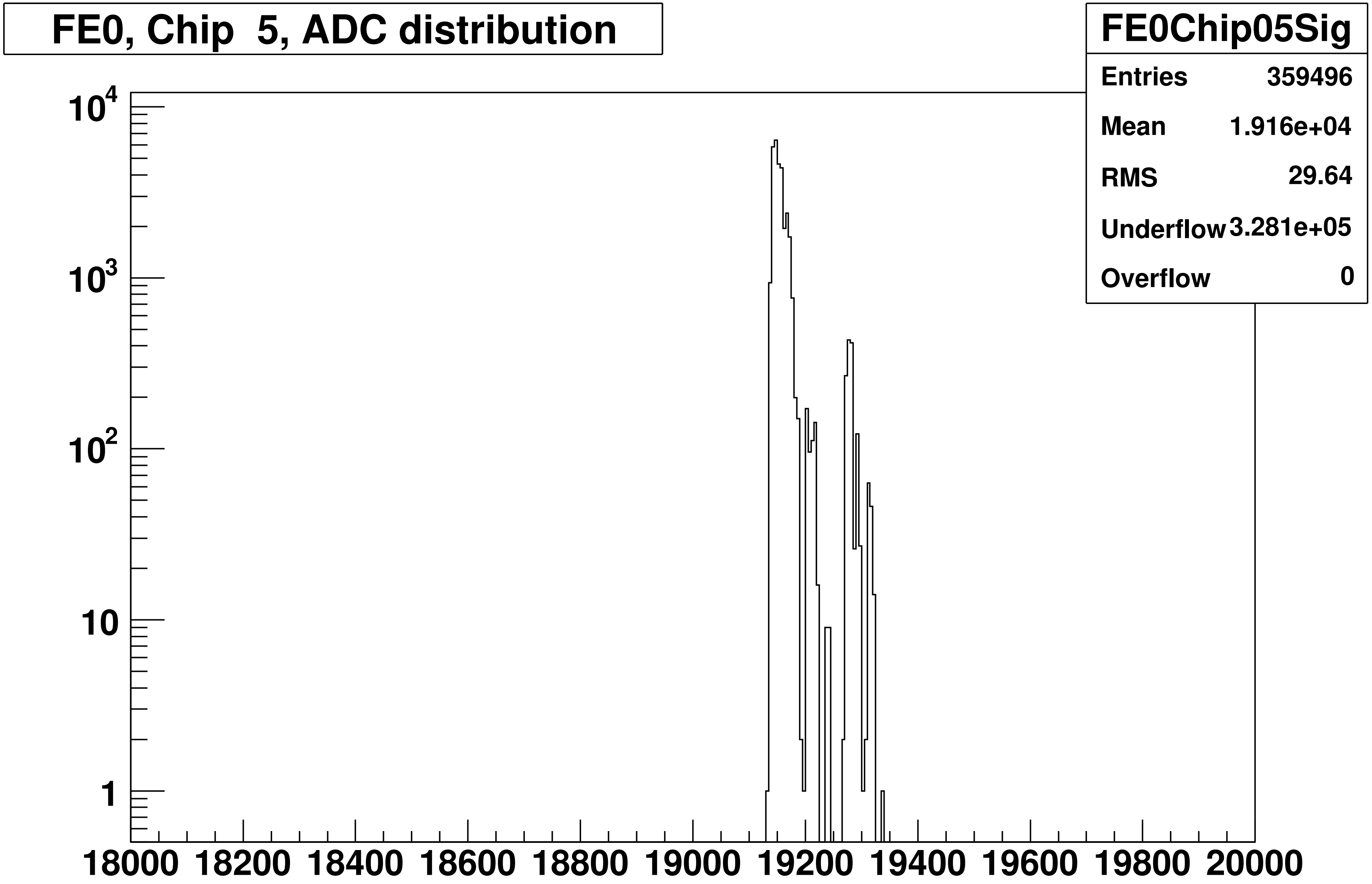
FE0, Chip 5, ADC distribution
FE0Chip05Sig
Entries 359496
Mean 1.916e+04
RMS 29.64
Underflow 3.281e+05
Overflow 0
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10^3
10^2
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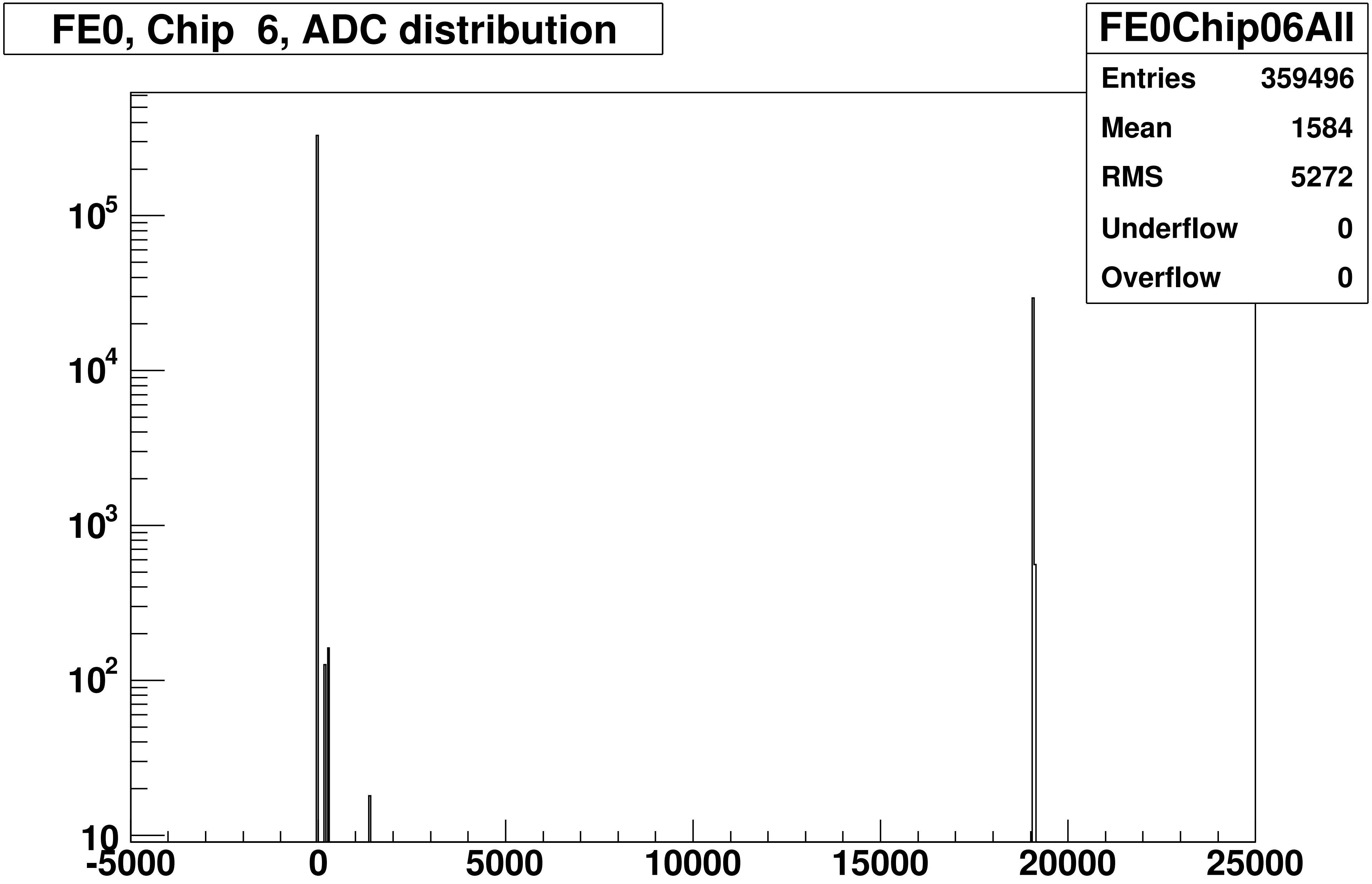
FE0, Chip 6, ADC distribution
FE0Chip06All
Entries 359496
Mean 1584
RMS 5272
Underflow 0
Overflow 0
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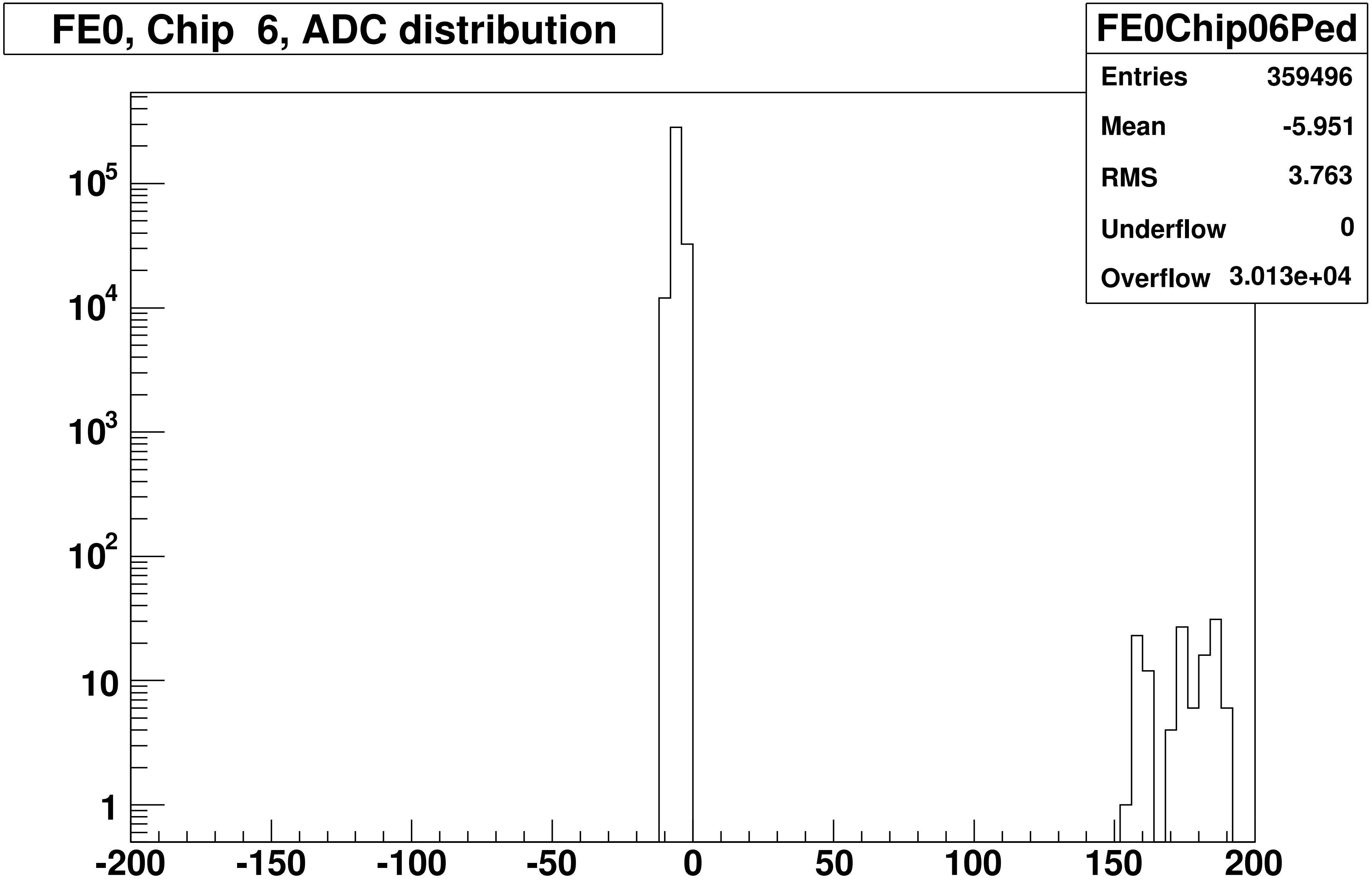
20000
25000


FE0, Chip 6, ADC distribution
FE0Chip06Ped
Entries 359496
Mean -5.951
RMS 3.763
Underflow 0
Overflow 3.013e+04
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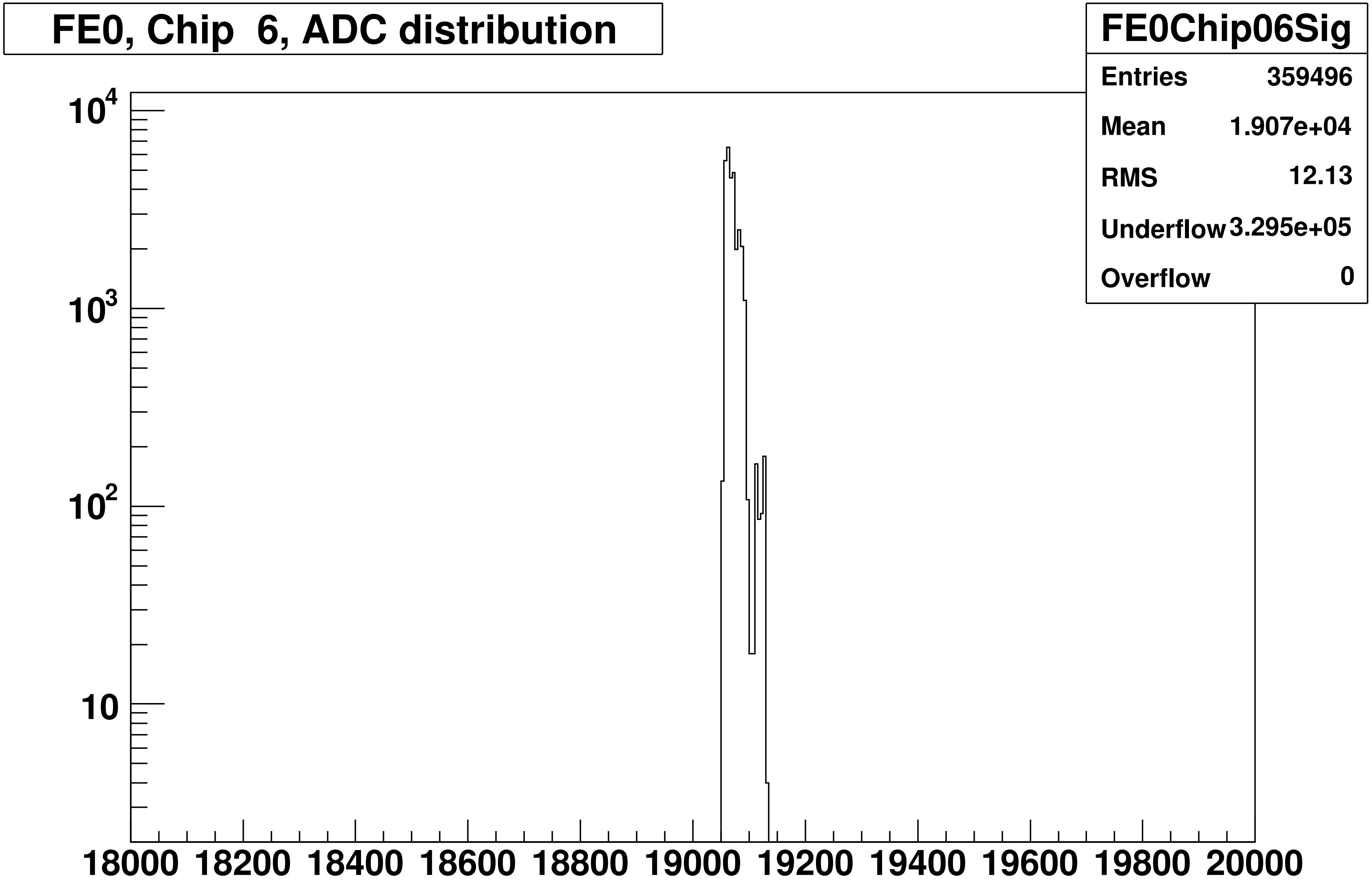
FE0, Chip 6, ADC distribution
FE0Chip06Sig
Entries 359496
Mean 1.907e+04
RMS 12.13
Underflow 3.295e+05
Overflow 0
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10^3
10^2
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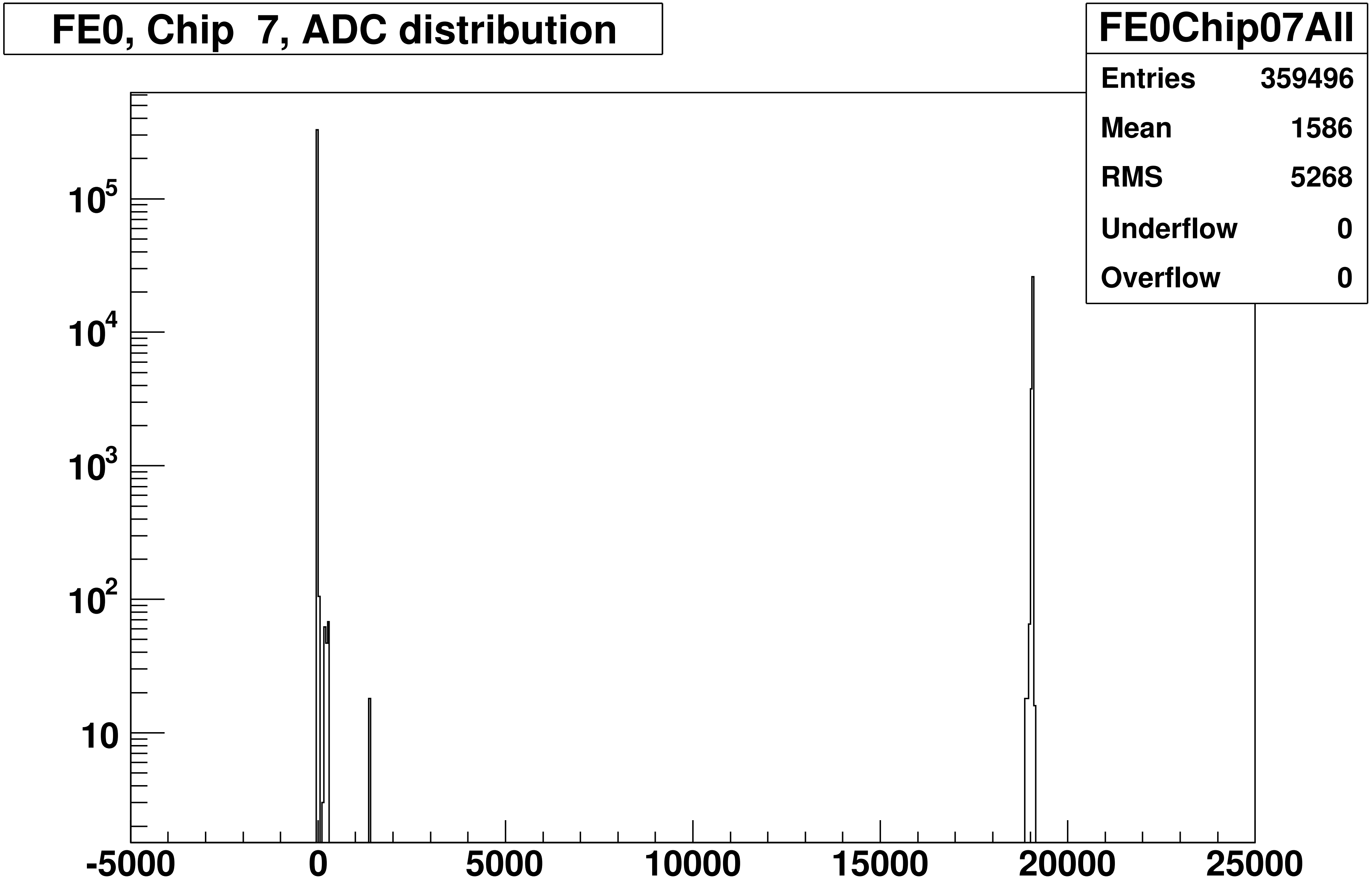
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE0, Chip 7, ADC distribution
FE0Chip07All
Entries 359496
Mean 1586
RMS 5268
Underflow 0
Overflow 0
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10^2
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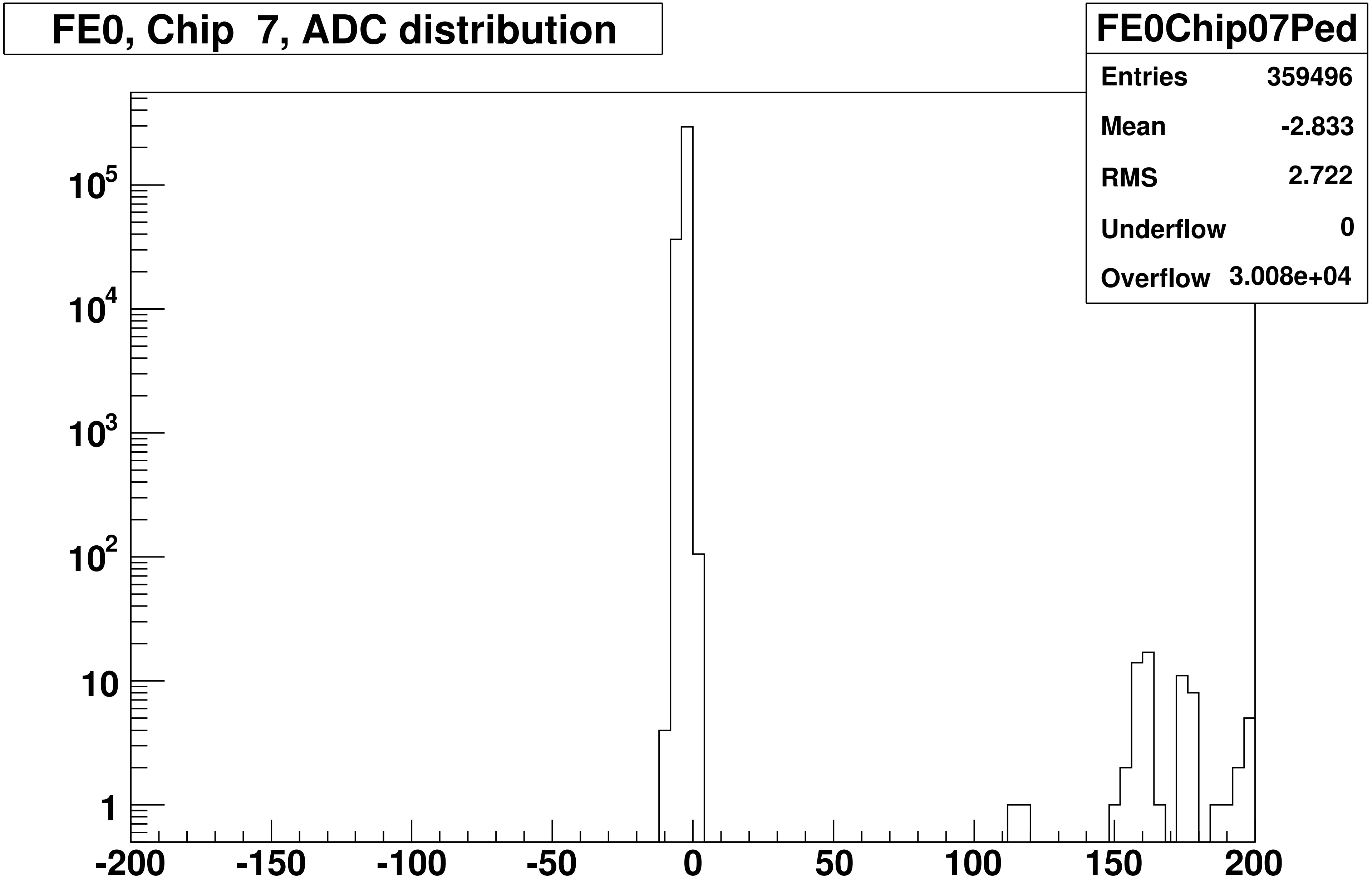
20000
25000


FE0, Chip 7, ADC distribution
FE0Chip07Ped
Entries 359496
Mean -2.833
RMS 2.722
Underflow 0
Overflow 3.008e+04
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10^3
10^2
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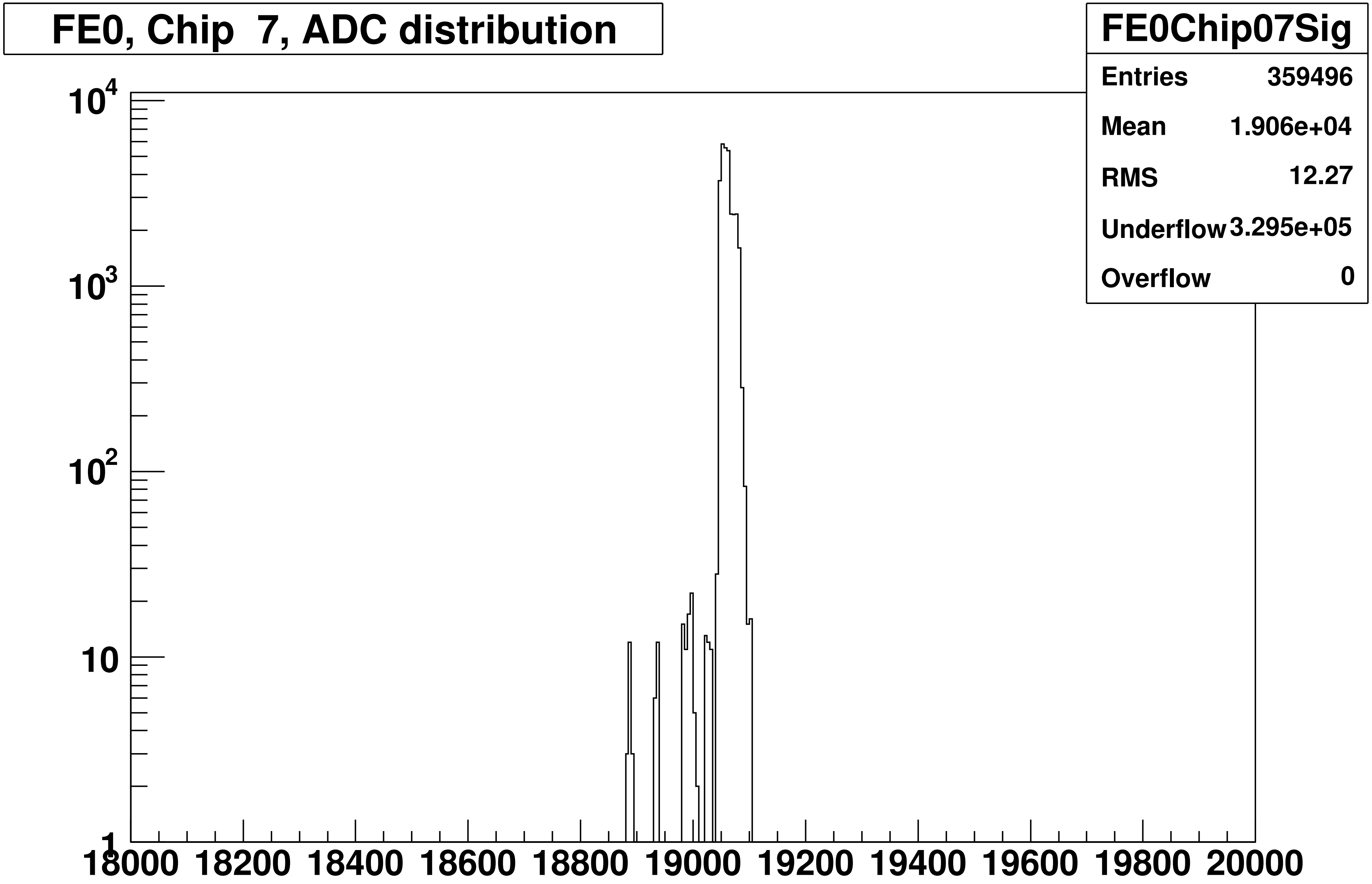
FE0, Chip 7, ADC distribution
FE0Chip07Sig
Entries 359496
Mean 1.906e+04
RMS 12.27
Underflow 3.295e+05
Overflow 0
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10^3
10^2
10
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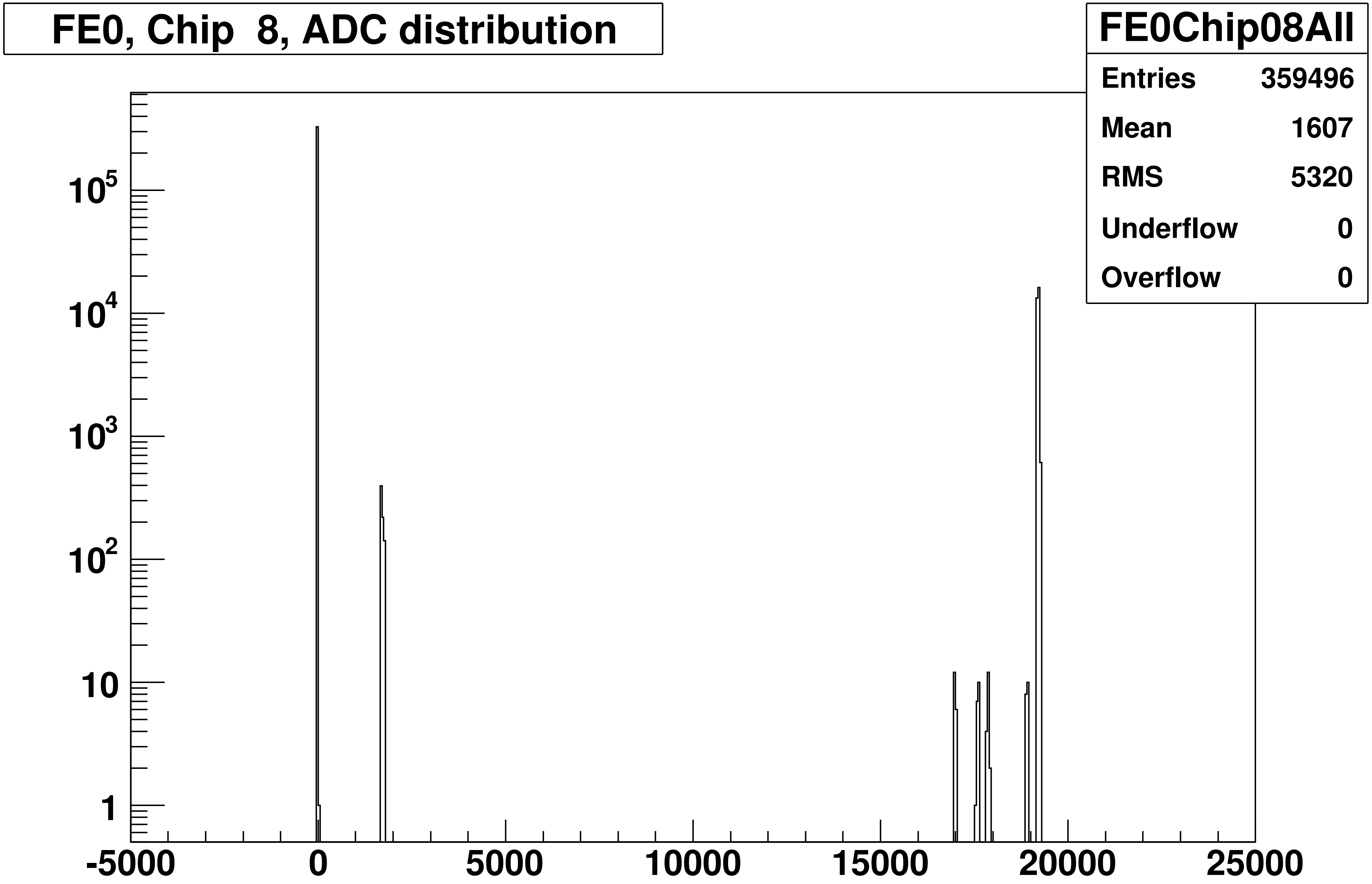
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE0, Chip 8, ADC distribution
FE0Chip08All
Entries 359496
Mean 1607
RMS 5320
Underflow 0
Overflow 0
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10^3
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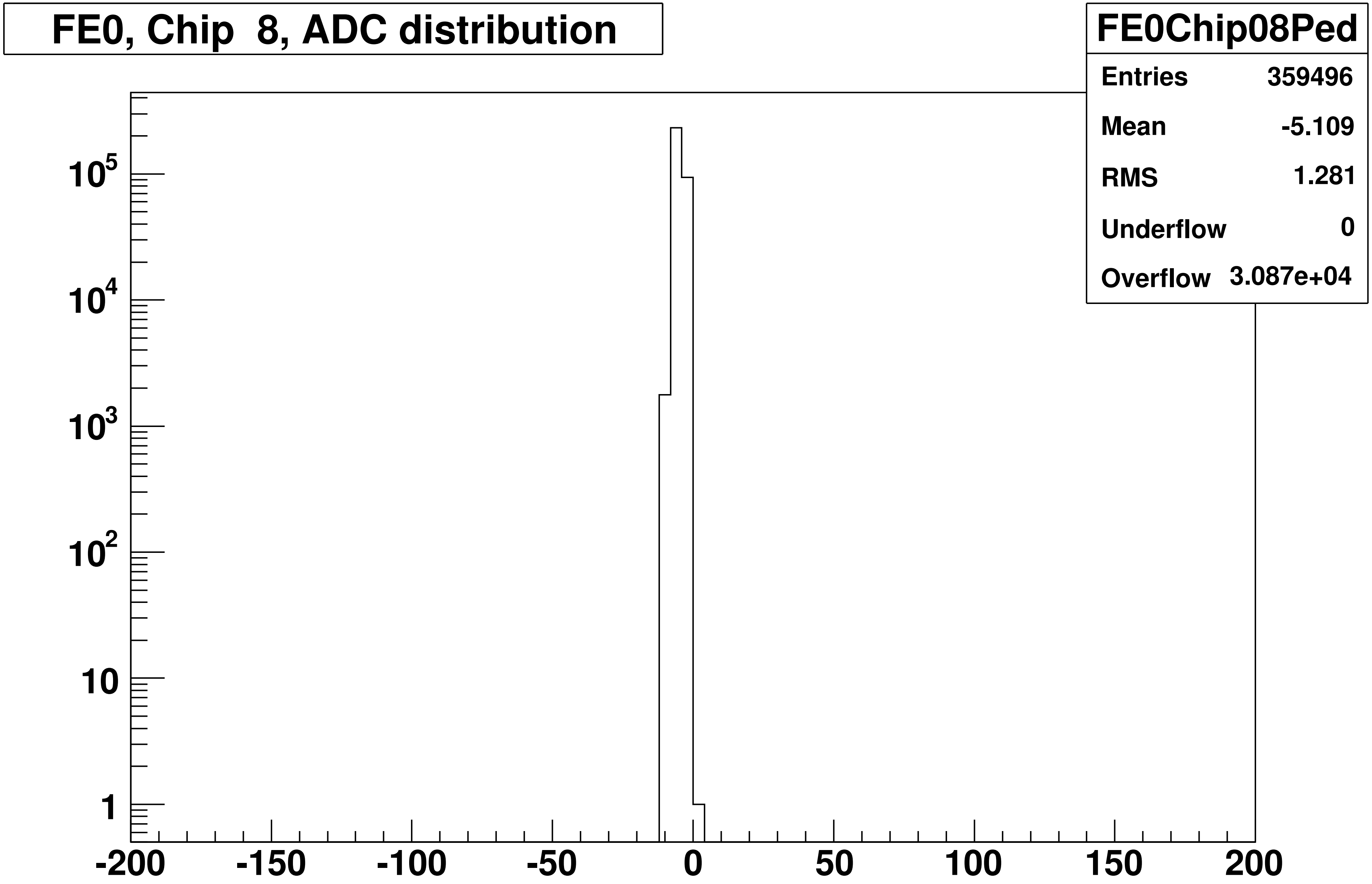
FE0, Chip 8, ADC distribution
FE0Chip08Ped
Entries 359496
Mean -5.109
RMS 1.281
Underflow 0
Overflow 3.087e+04
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10^2
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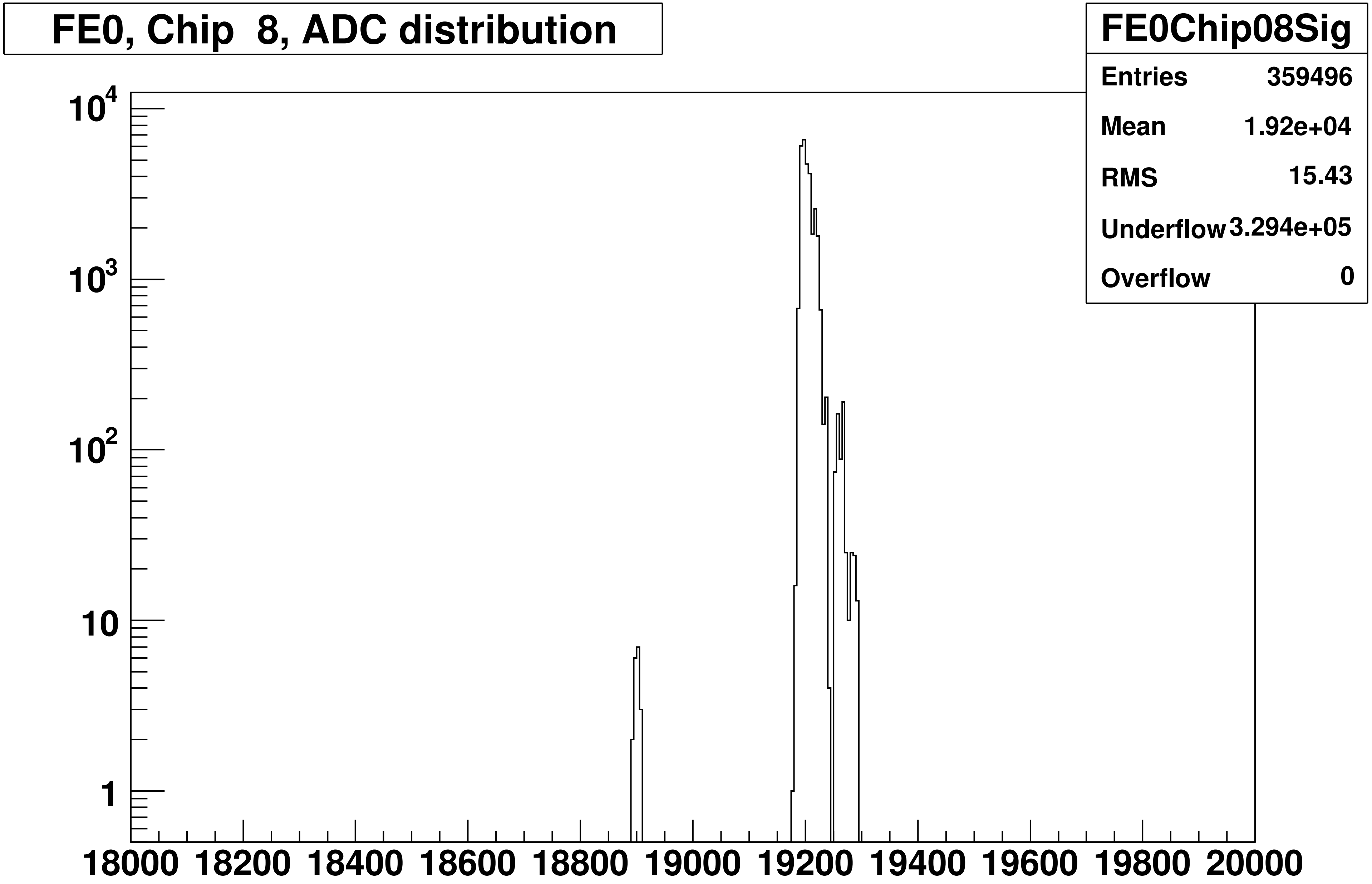
FE0, Chip 8, ADC distribution
FE0Chip08Sig
Entries 359496
Mean 1.92e+04
RMS 15.43
Underflow 3.294e+05
Overflow 0
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1
18000
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19000
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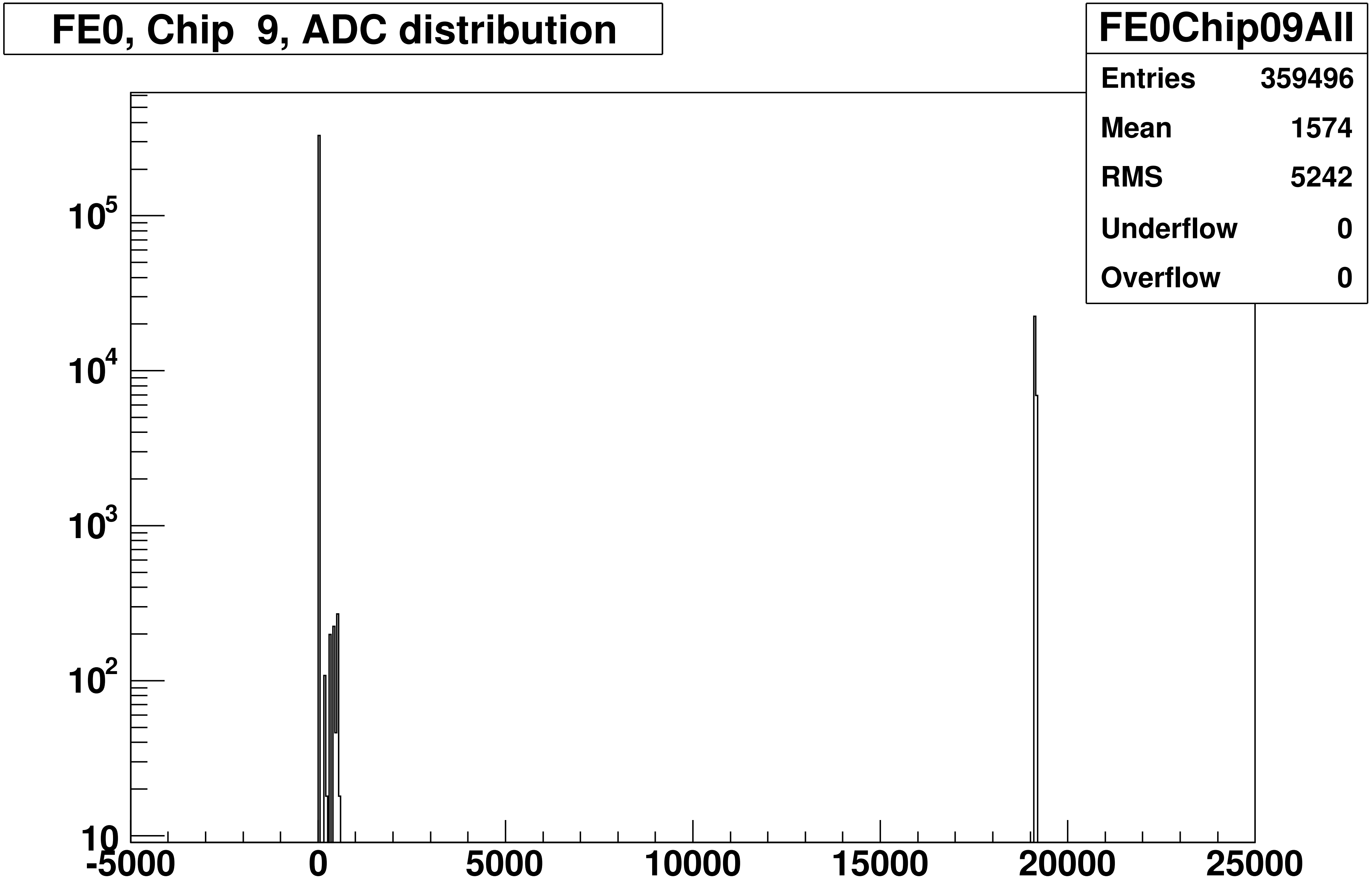
19800
20000


FE0, Chip 9, ADC distribution
FE0Chip09All
Entries 359496
Mean 1574
RMS 5242
Underflow 0
Overflow 0
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10^4
10^3
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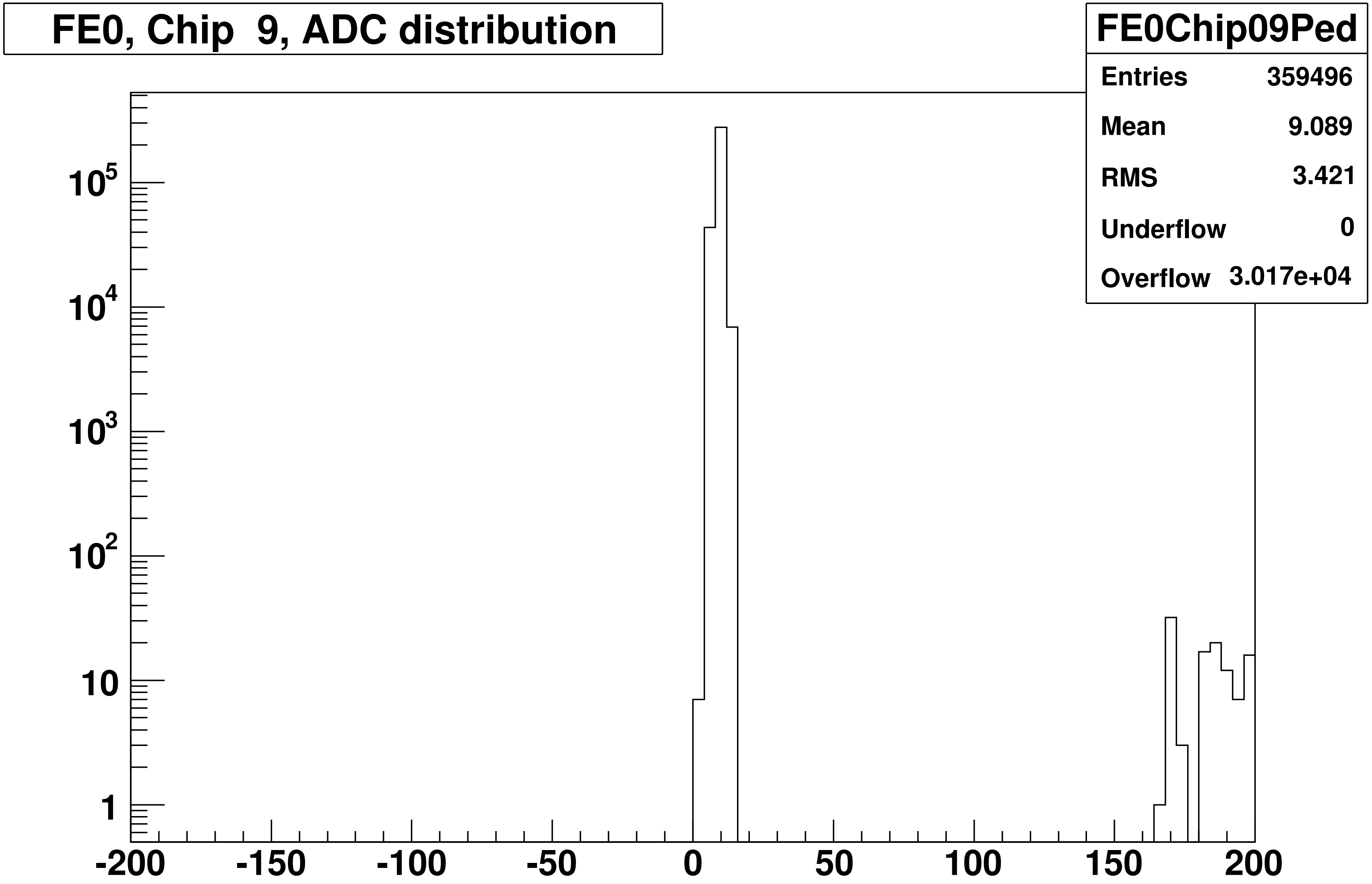
20000
25000


FE0, Chip 9, ADC distribution
FE0Chip09Ped
Entries 359496
Mean 9.089
RMS 3.421
Underflow 0
Overflow 3.017e+04
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10^3
10^2
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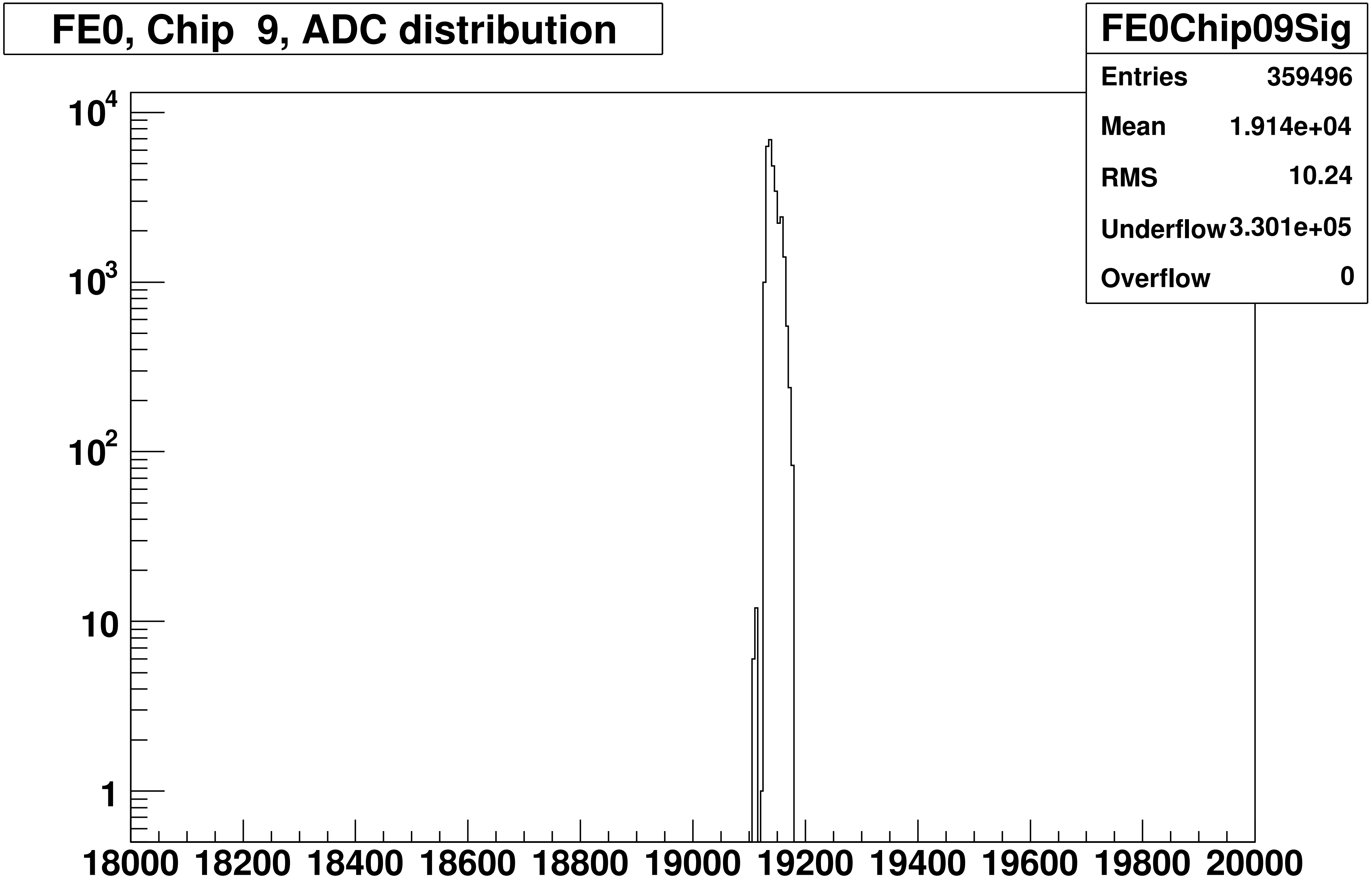
FE0, Chip 9, ADC distribution
FE0Chip09Sig
Entries 359496
Mean 1.914e+04
RMS 10.24
Underflow 3.301e+05
Overflow 0
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10^3
10^2
10
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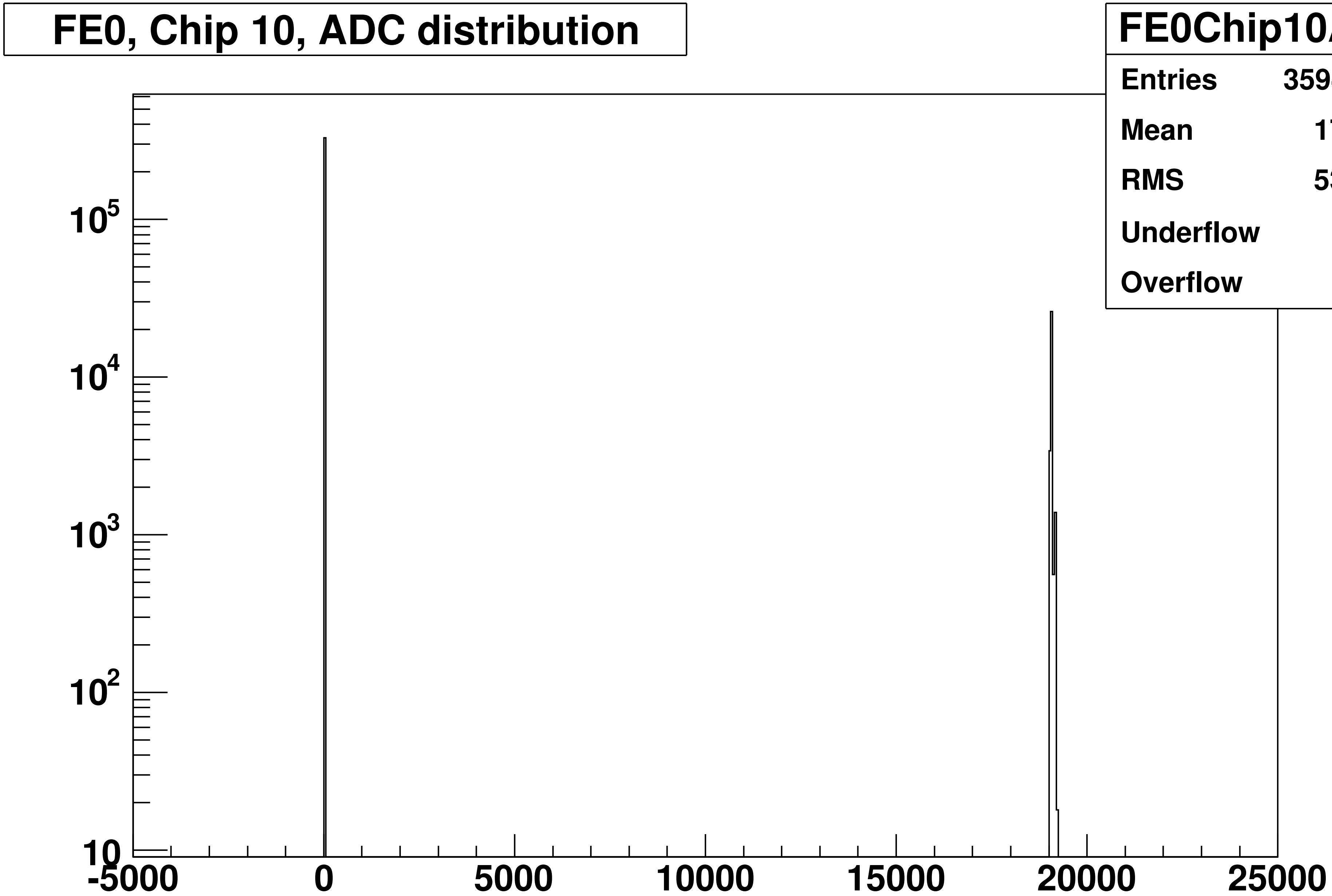
FE0, Chip 10, ADC distribution
FE0Chip10All
Entries 359496
Mean 1700
RMS 5369
Underflow 0
Overflow 0
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10^4
10^3
10^2
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0
5000
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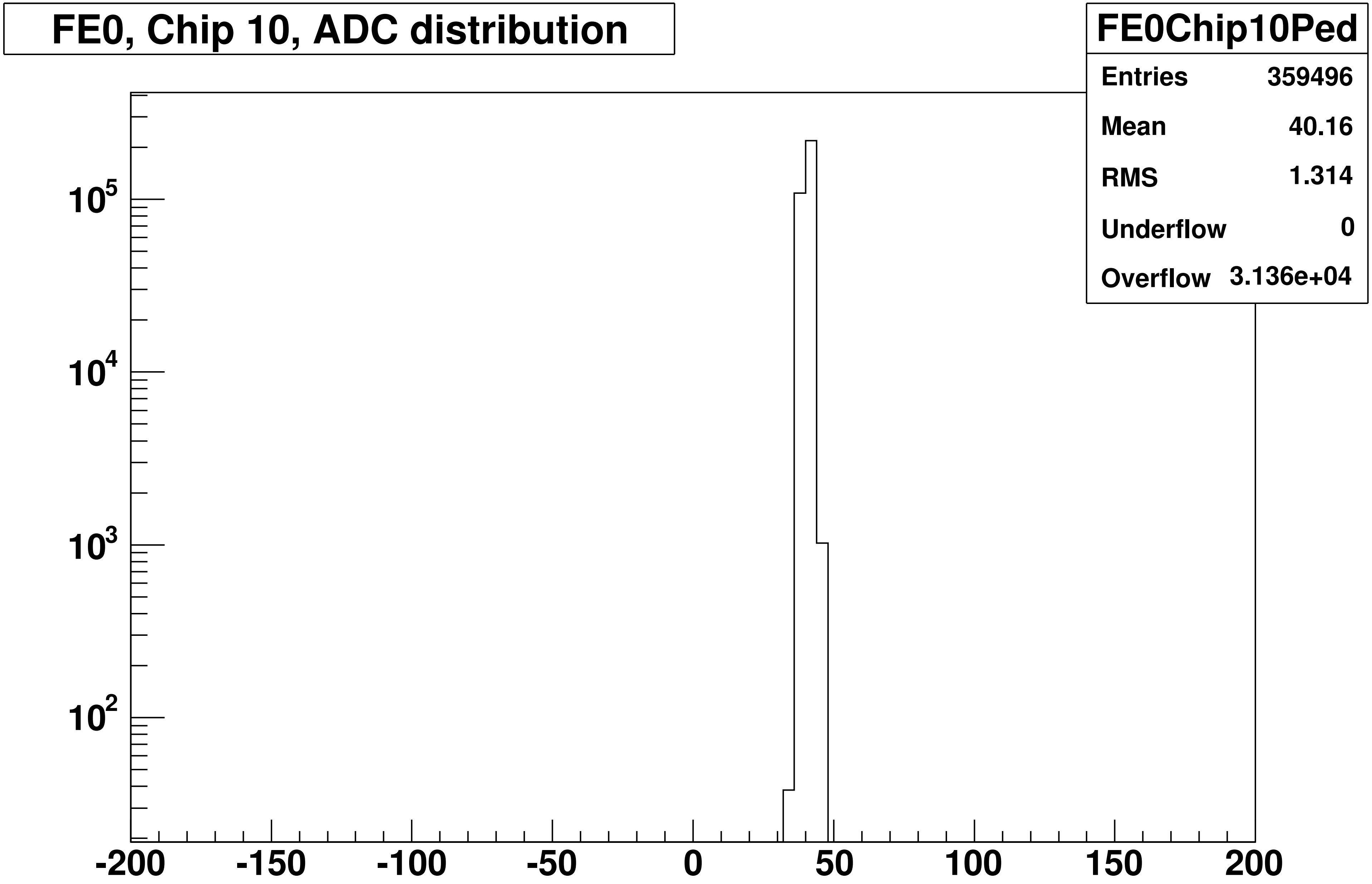
20000
25000


FE0, Chip 10, ADC distribution
FE0Chip10Ped
Entries 359496
Mean 40.16
RMS 1.314
Underflow 0
Overflow 3.136e+04
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10^3
10^2
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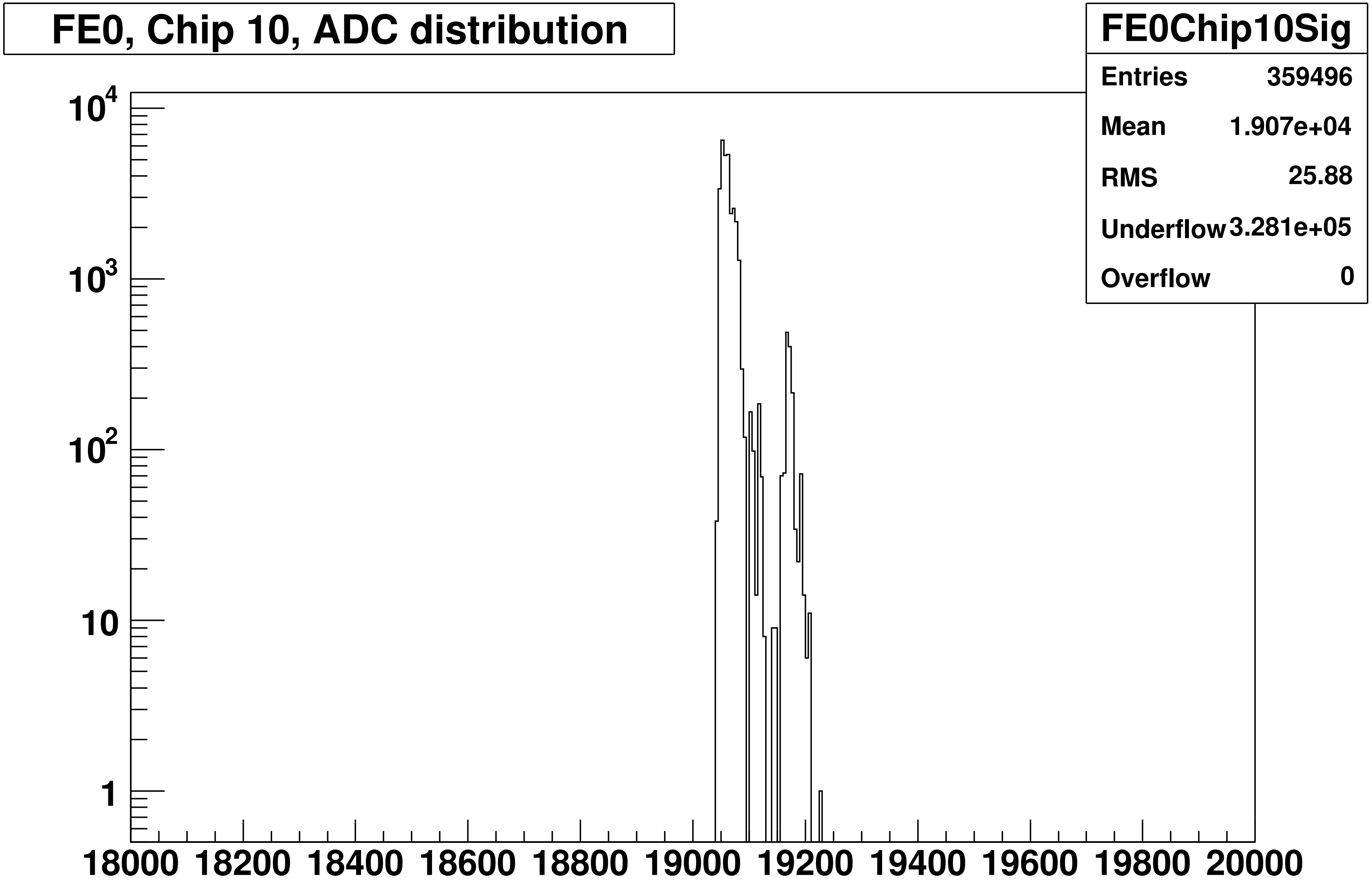
150
200



FE0, Chip 10, ADC distribution
FE0Chip10Sig
Entries 359496
Mean 1.907e+04
RMS 25.88
Underflow 3.281e+05
Overflow 0
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10^3
10^2
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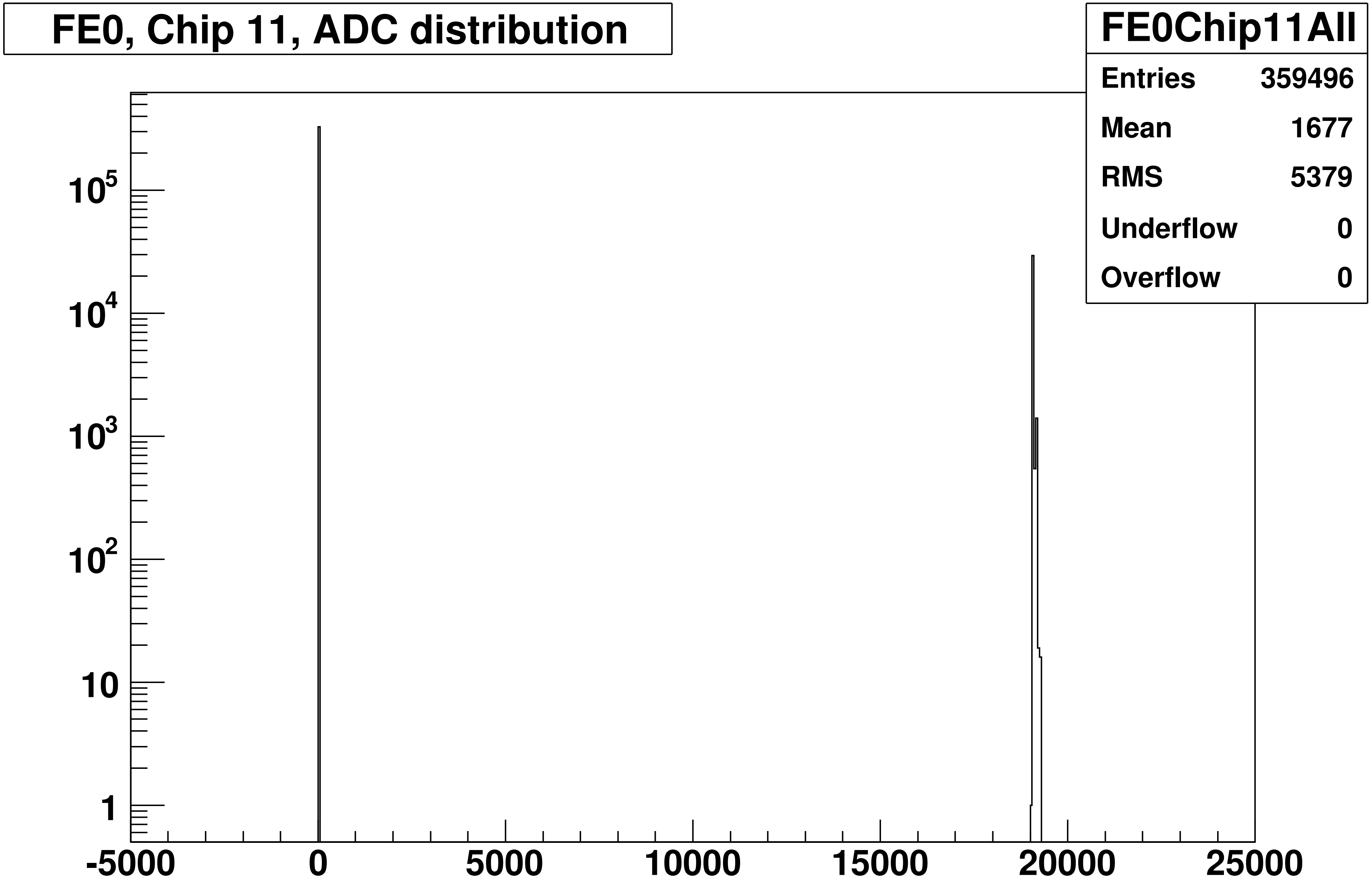
FE0, Chip 11, ADC distribution
FE0Chip11All
Entries 359496
Mean 1677
RMS 5379
Underflow 0
Overflow 0
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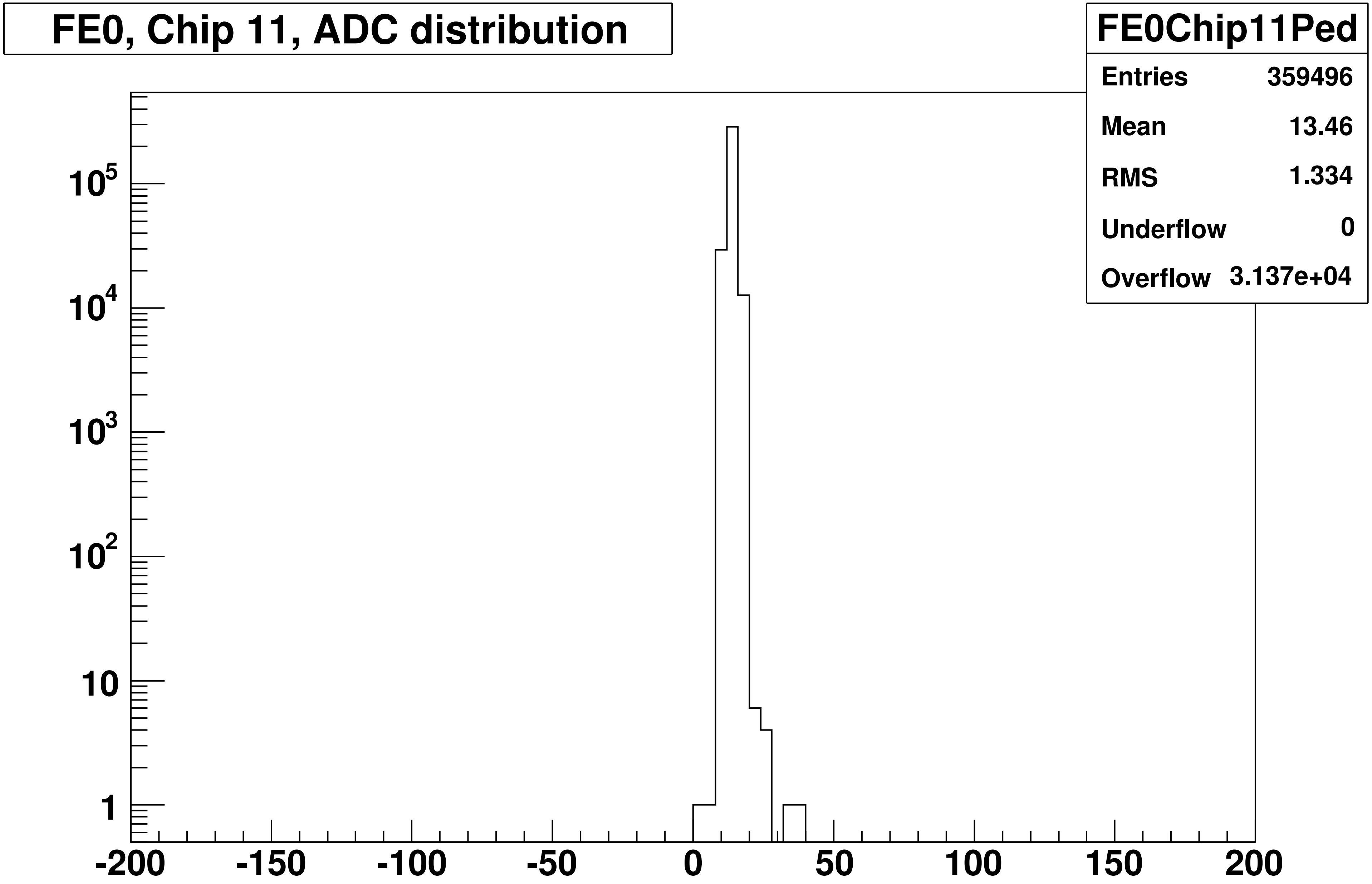
FE0, Chip 11, ADC distribution
FE0Chip11Ped
Entries 359496
Mean 13.46
RMS 1.334
Underflow 0
Overflow 3.137e+04
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150
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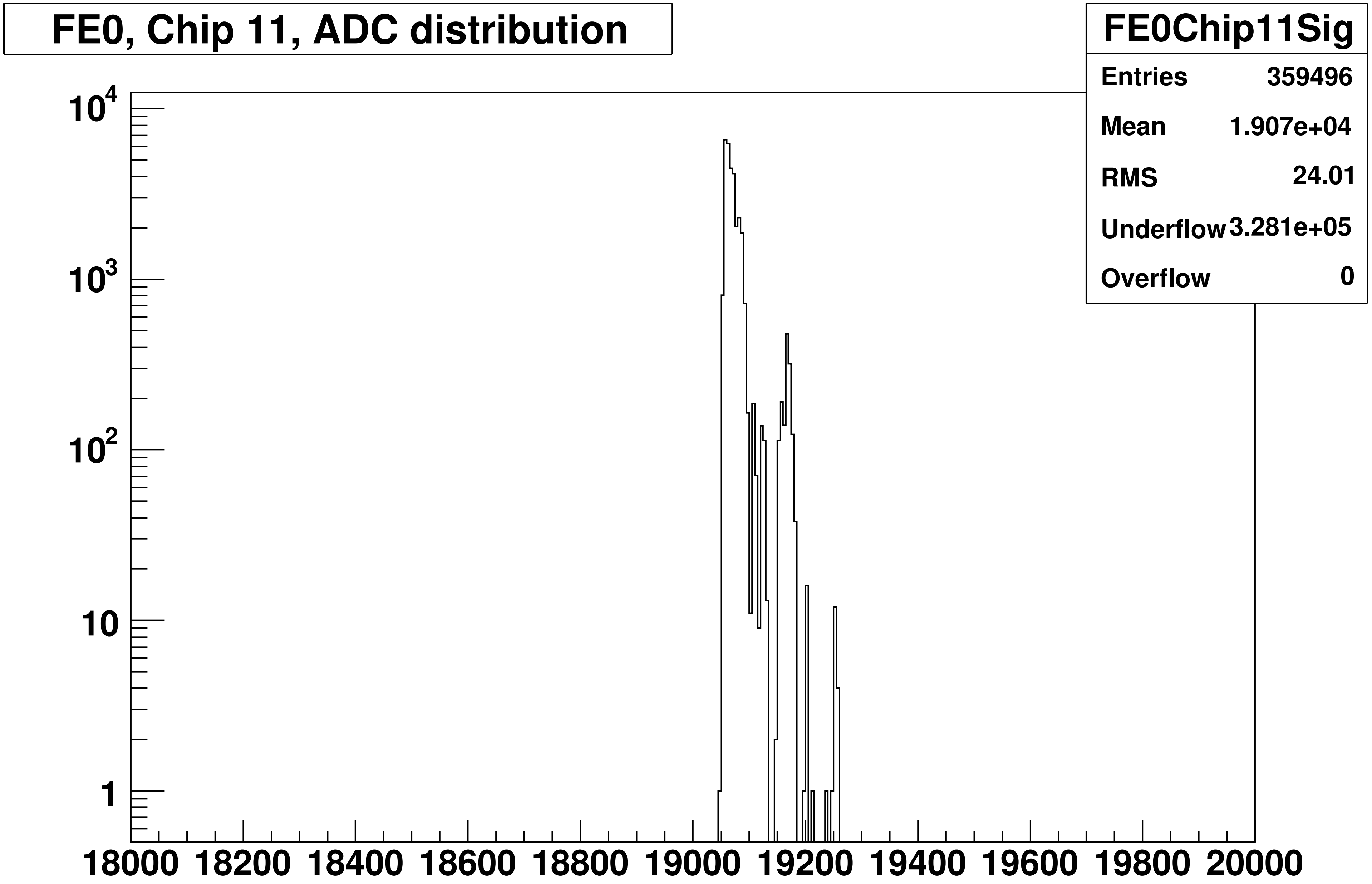

FE0, Chip 11, ADC distribution
FE0Chip11Sig
Entries 359496
Mean 1.907e+04
RMS 24.01
Underflow 3.281e+05
Overflow 0
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10^3
10^2
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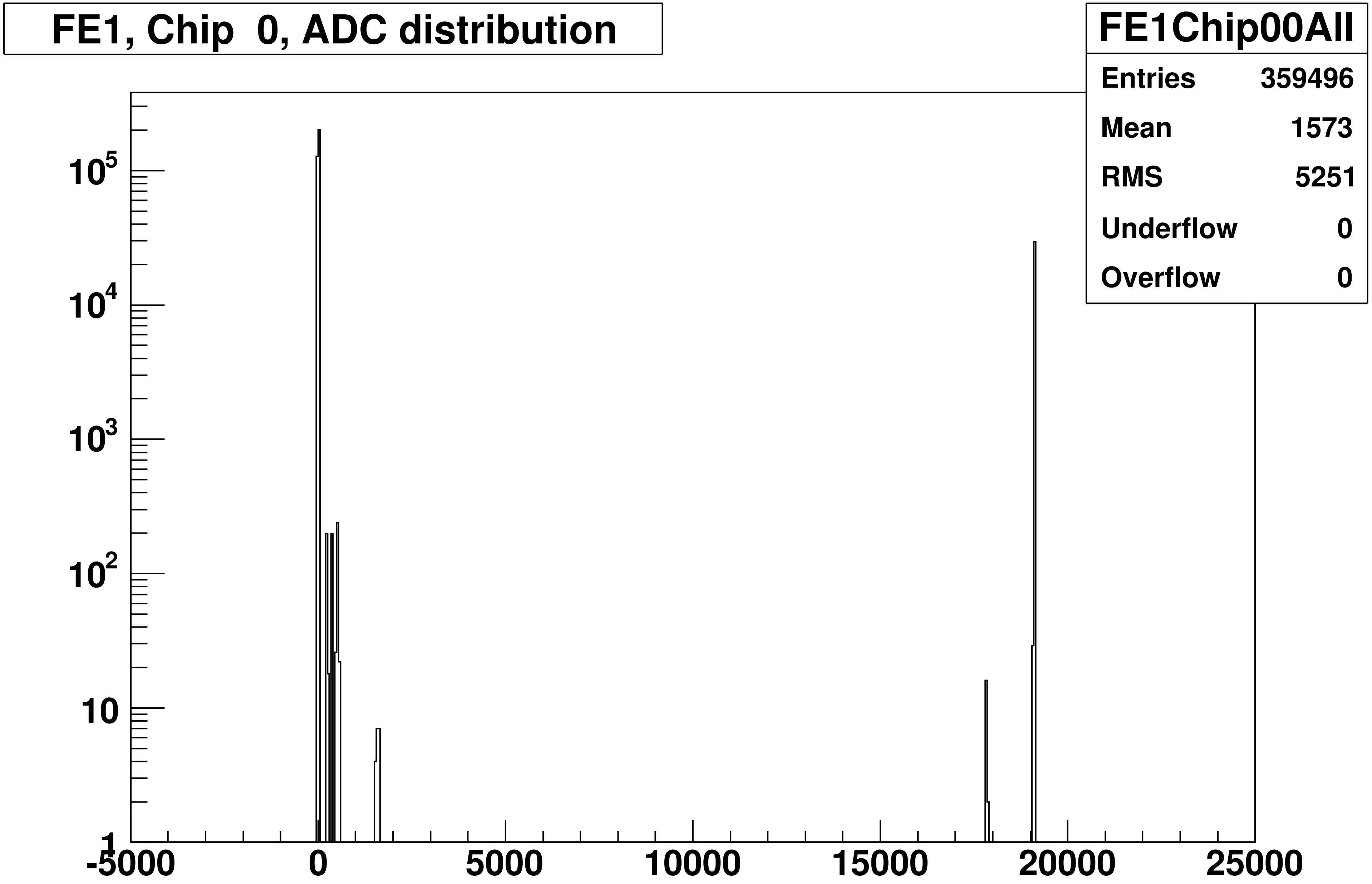
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE1, Chip 0, ADC distribution
FE1Chip00All
Entries 359496
Mean 1573
RMS 5251
Underflow 0
Overflow 0
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10^2
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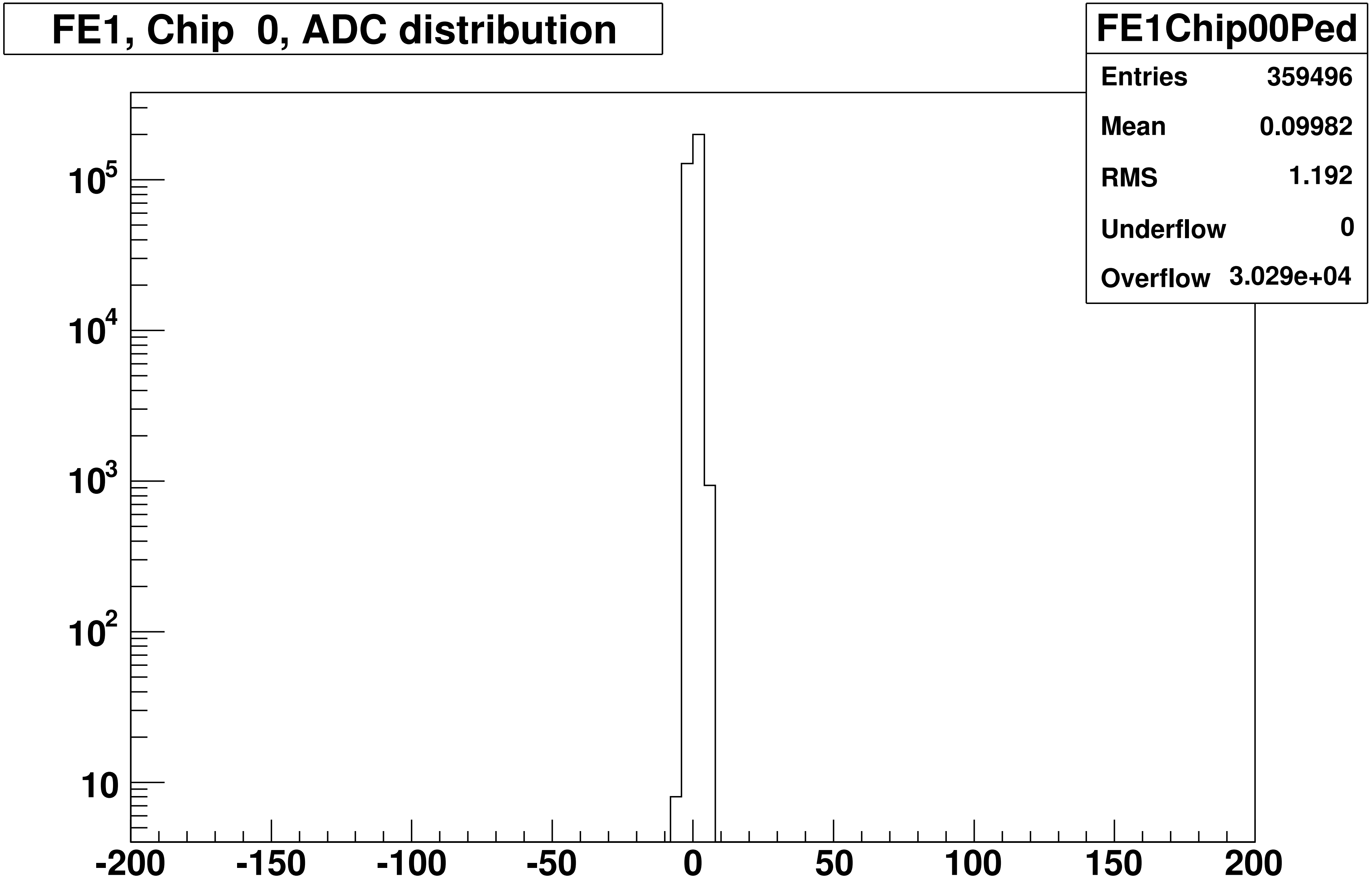
FE1, Chip 0, ADC distribution
FE1Chip00Ped
Entries 359496
Mean 0.09982
RMS 1.192
Underflow 0
Overflow 3.029e+04
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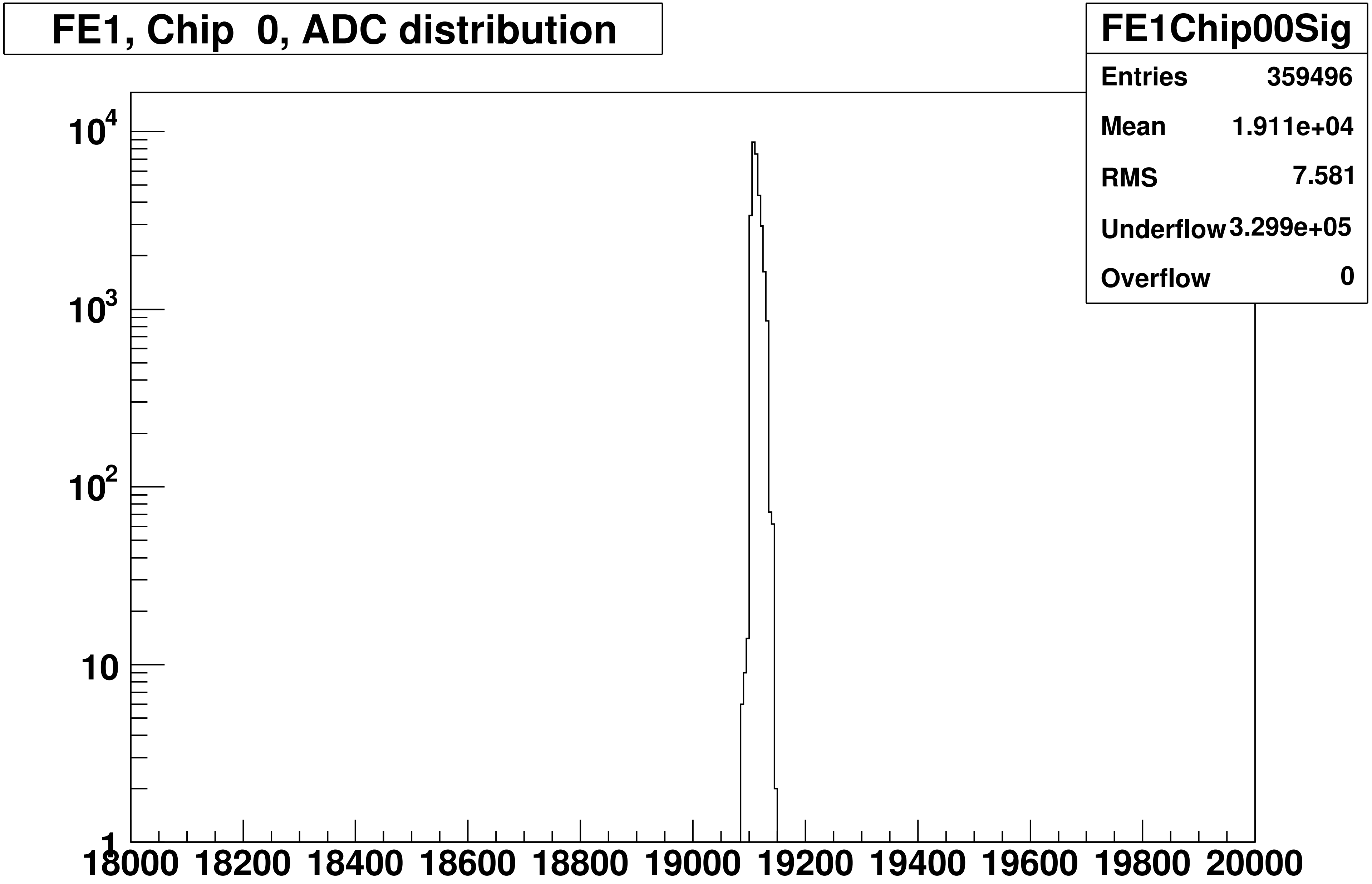
FE1, Chip 0, ADC distribution
FE1Chip00Sig
Entries 359496
Mean 1.911e+04
RMS 7.581
Underflow 3.299e+05
Overflow 0
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10^3
10^2
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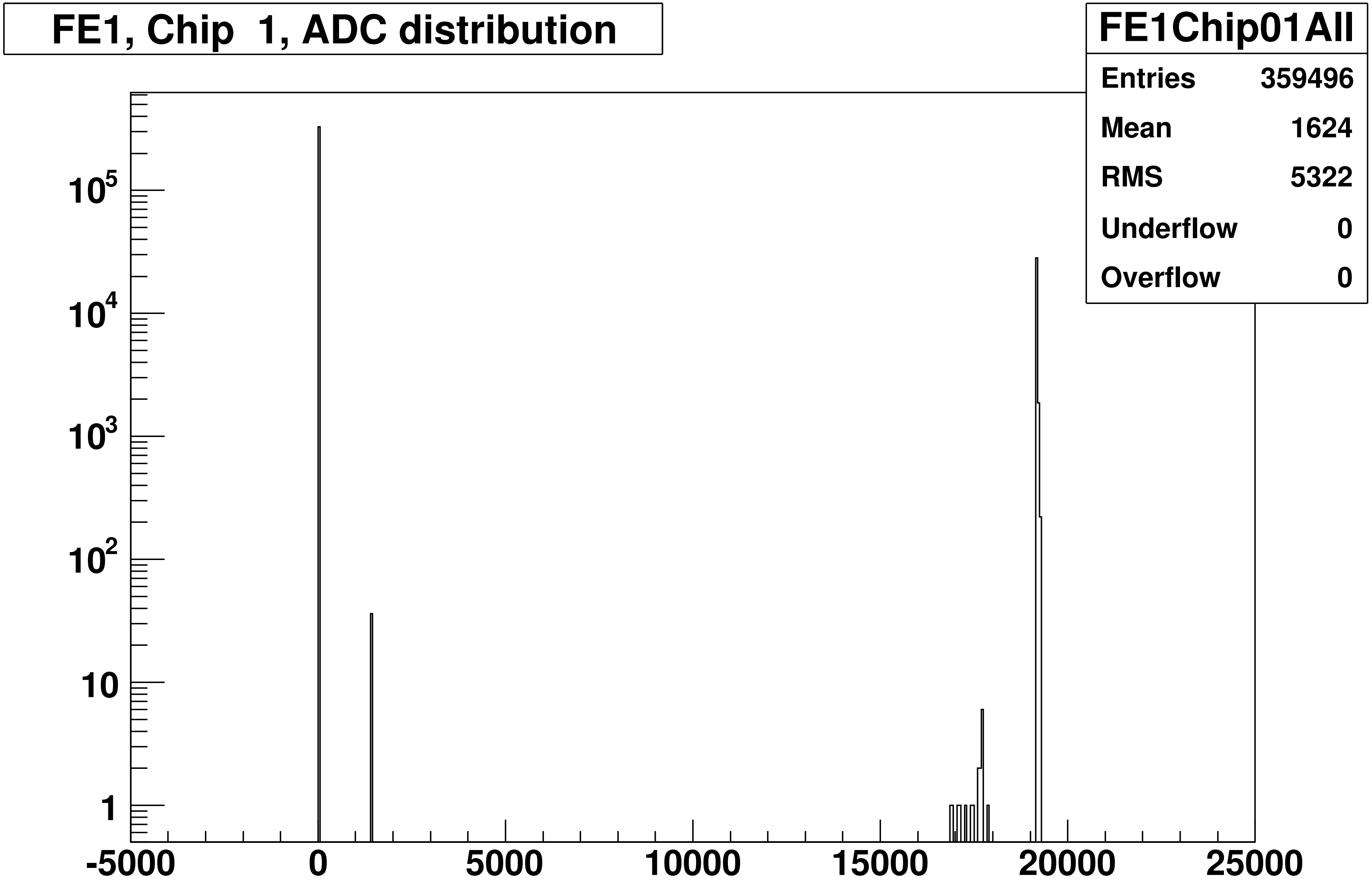
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE1, Chip 1, ADC distribution
FE1Chip01All
Entries 359496
Mean 1624
RMS 5322
Underflow 0
Overflow 0
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10^4
10^3
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10
1
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15000
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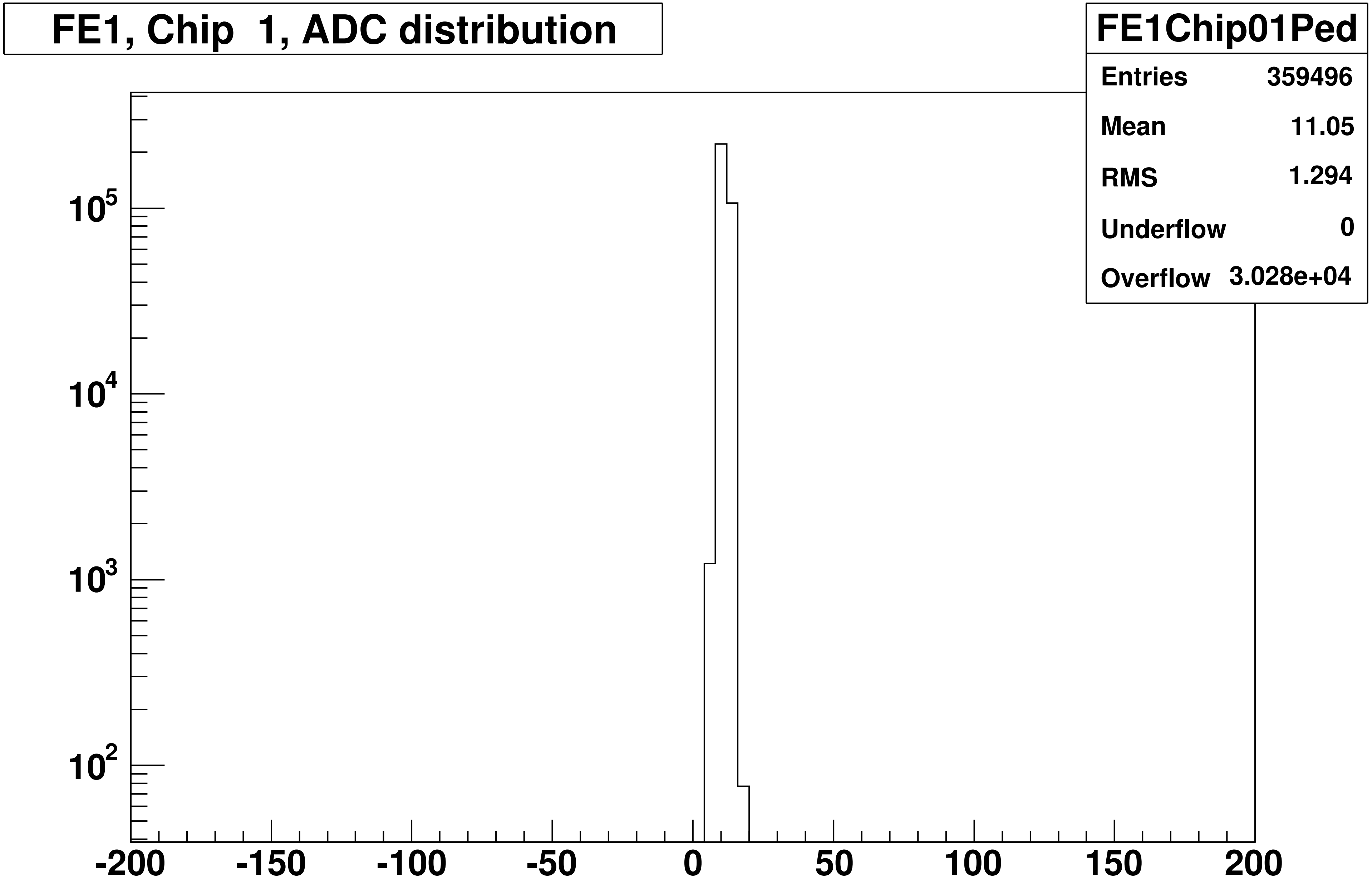
25000


FE1, Chip 1, ADC distribution
FE1Chip01Ped
Entries 359496
Mean 11.05
RMS 1.294
Underflow 0
Overflow 3.028e+04
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10^4
10^3
10^2
-200
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-50
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150
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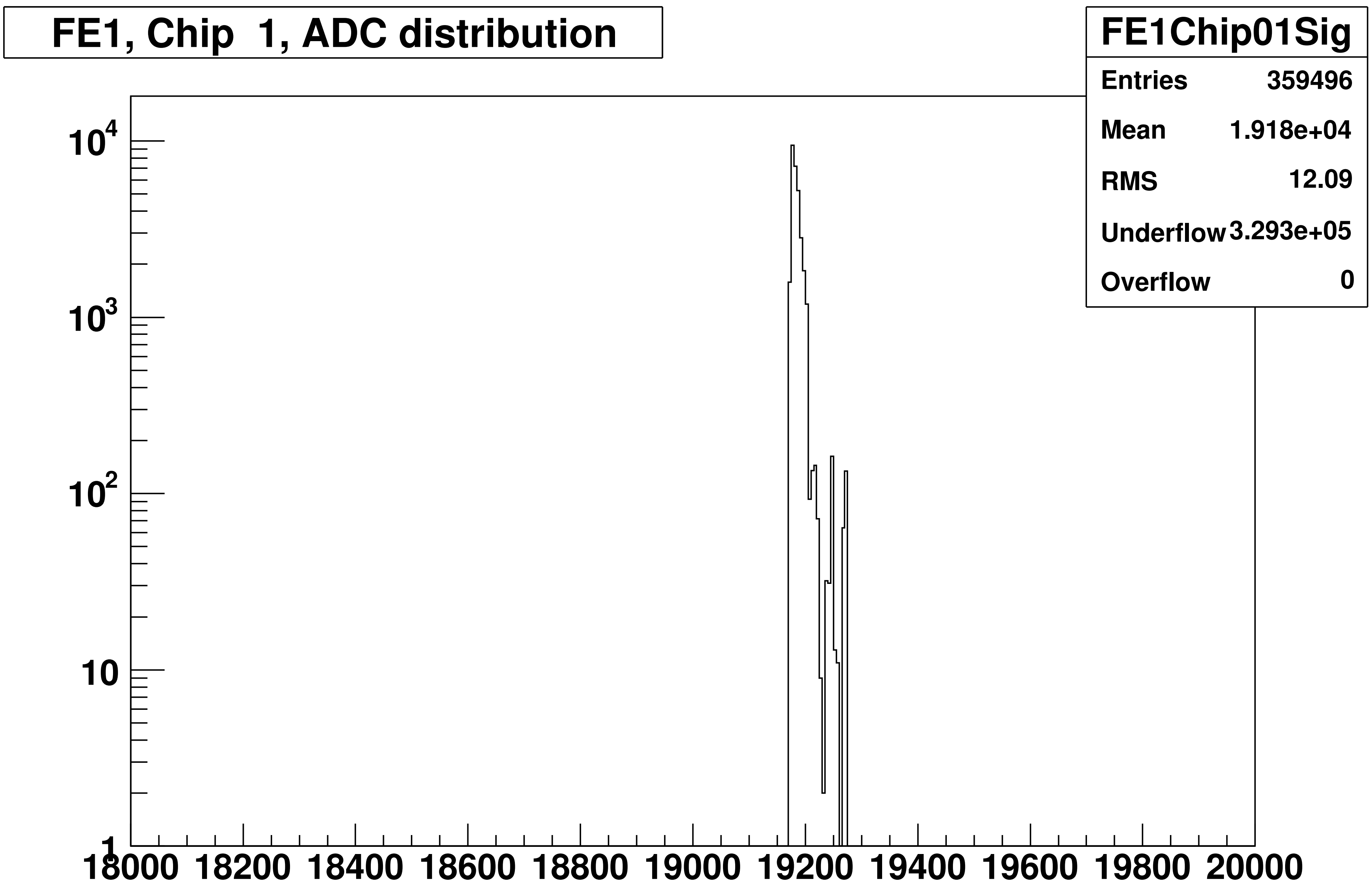
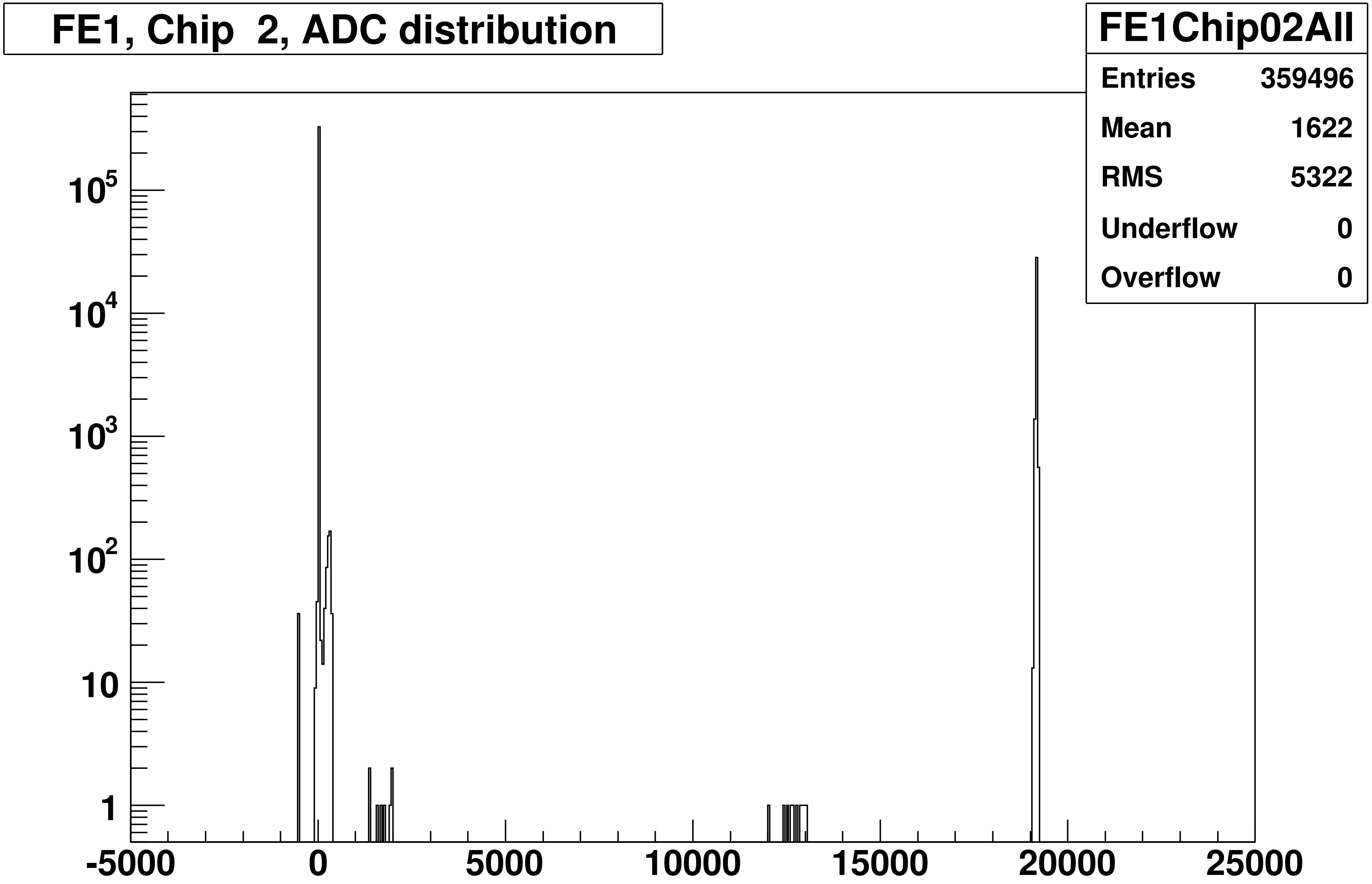

FE1, Chip 1, ADC distribution
FE1Chip01Sig
Entries 359496
Mean 1.918e+04
RMS 12.09
Underflow 3.293e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE1, Chip 2, ADC distribution
FE1Chip02All
Entries 359496
Mean 1622
RMS 5322
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
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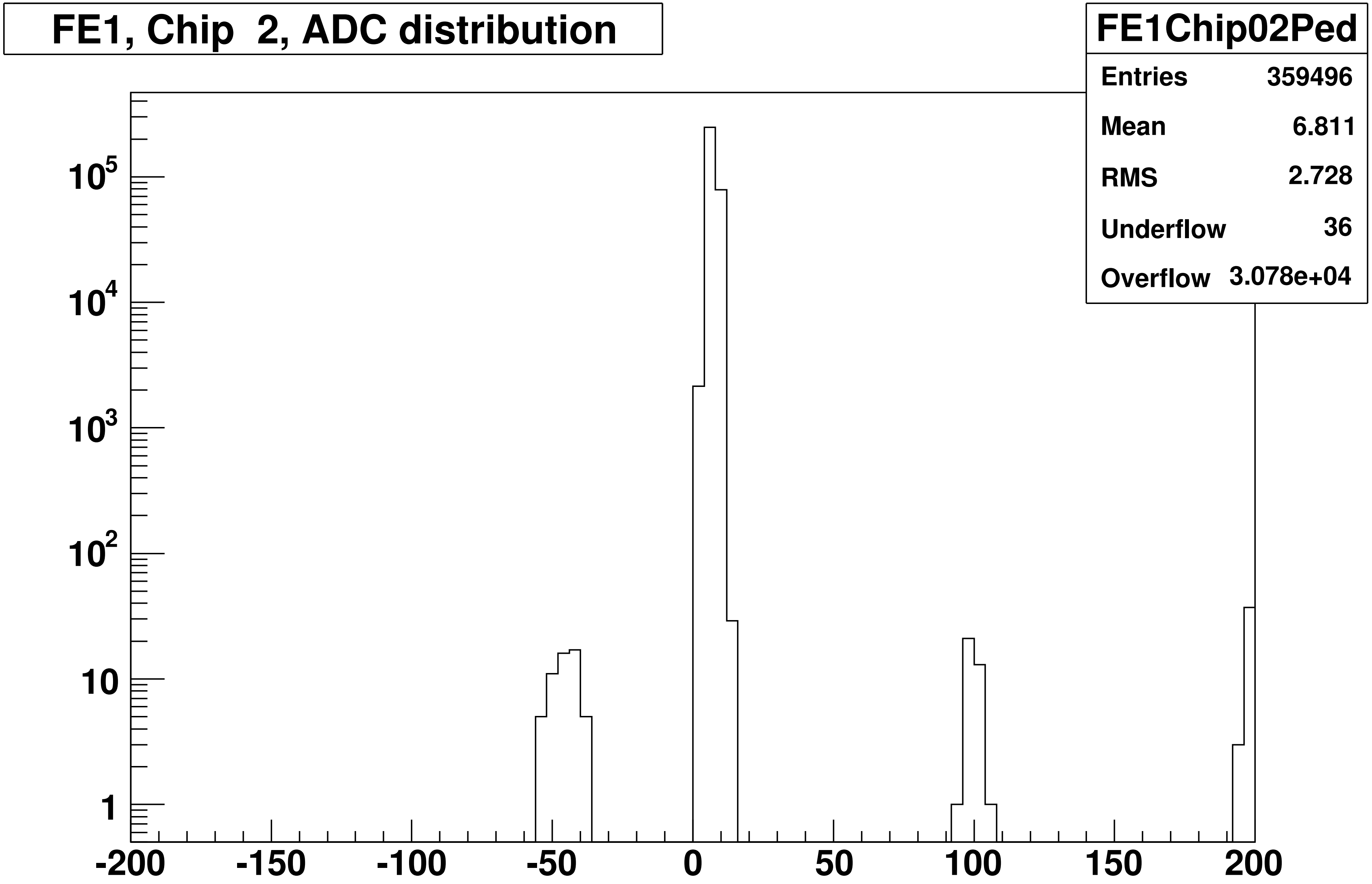
FE1, Chip 2, ADC distribution
FE1Chip02Ped
Entries 359496
Mean 6.811
RMS 2.728
Underflow 36
Overflow 3.078e+04
10^5
10^4
10^3
10^2
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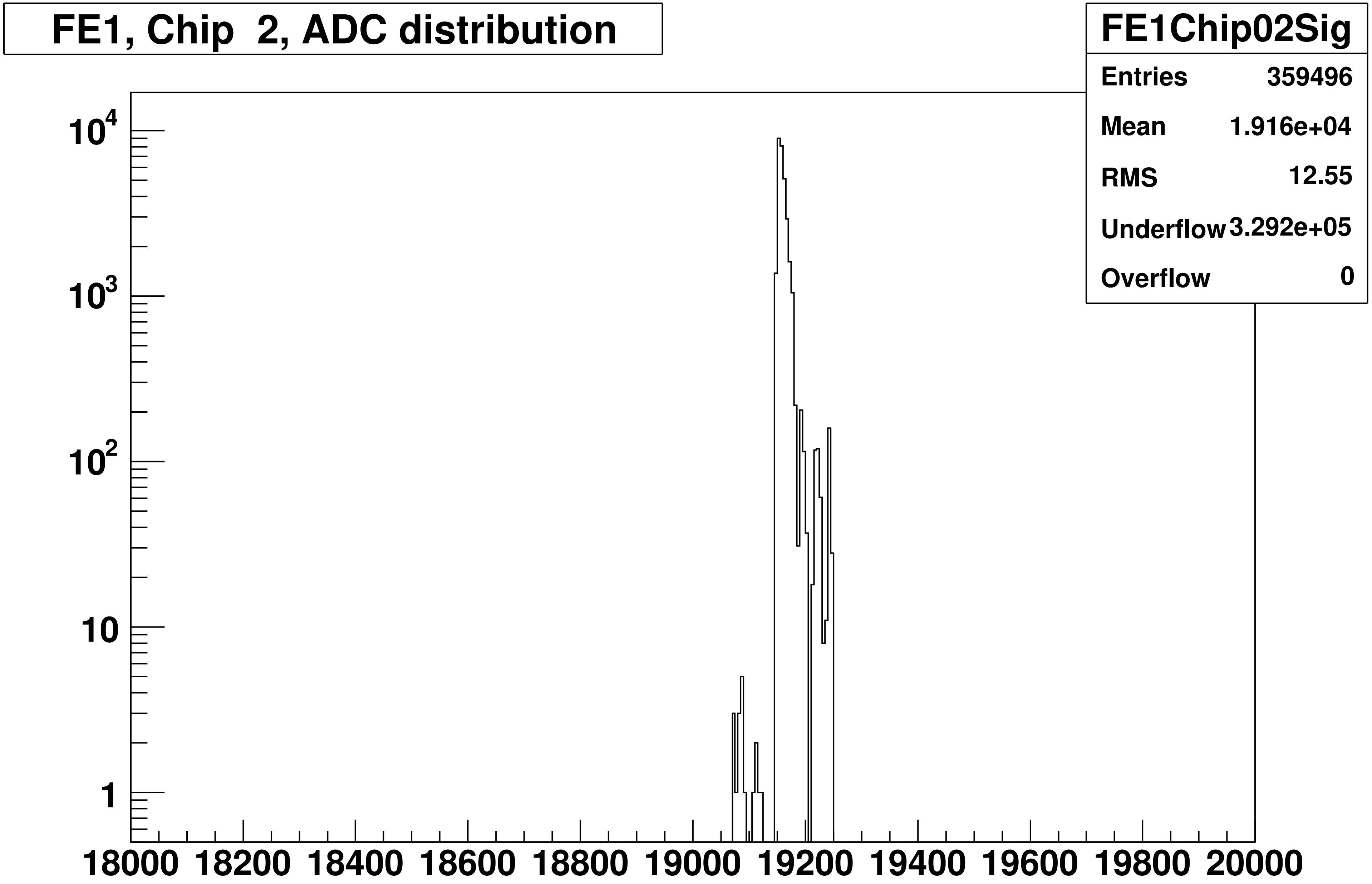

FE1, Chip 2, ADC distribution
FE1Chip02Sig
Entries 359496
Mean 1.916e+04
RMS 12.55
Underflow 3.292e+05
Overflow 0
10^4
10^3
10^2
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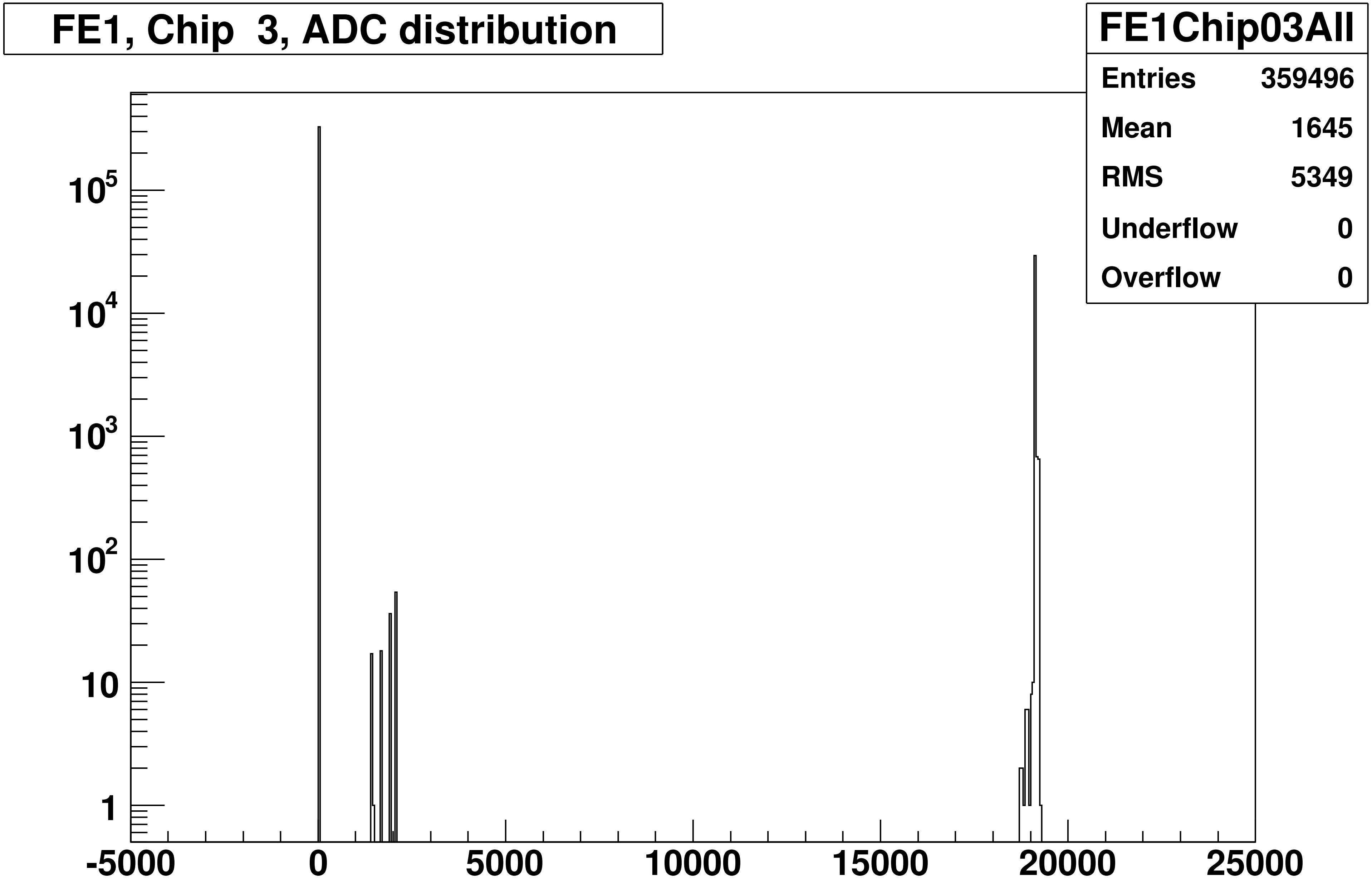
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE1, Chip 3, ADC distribution
FE1Chip03All
Entries 359496
Mean 1645
RMS 5349
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
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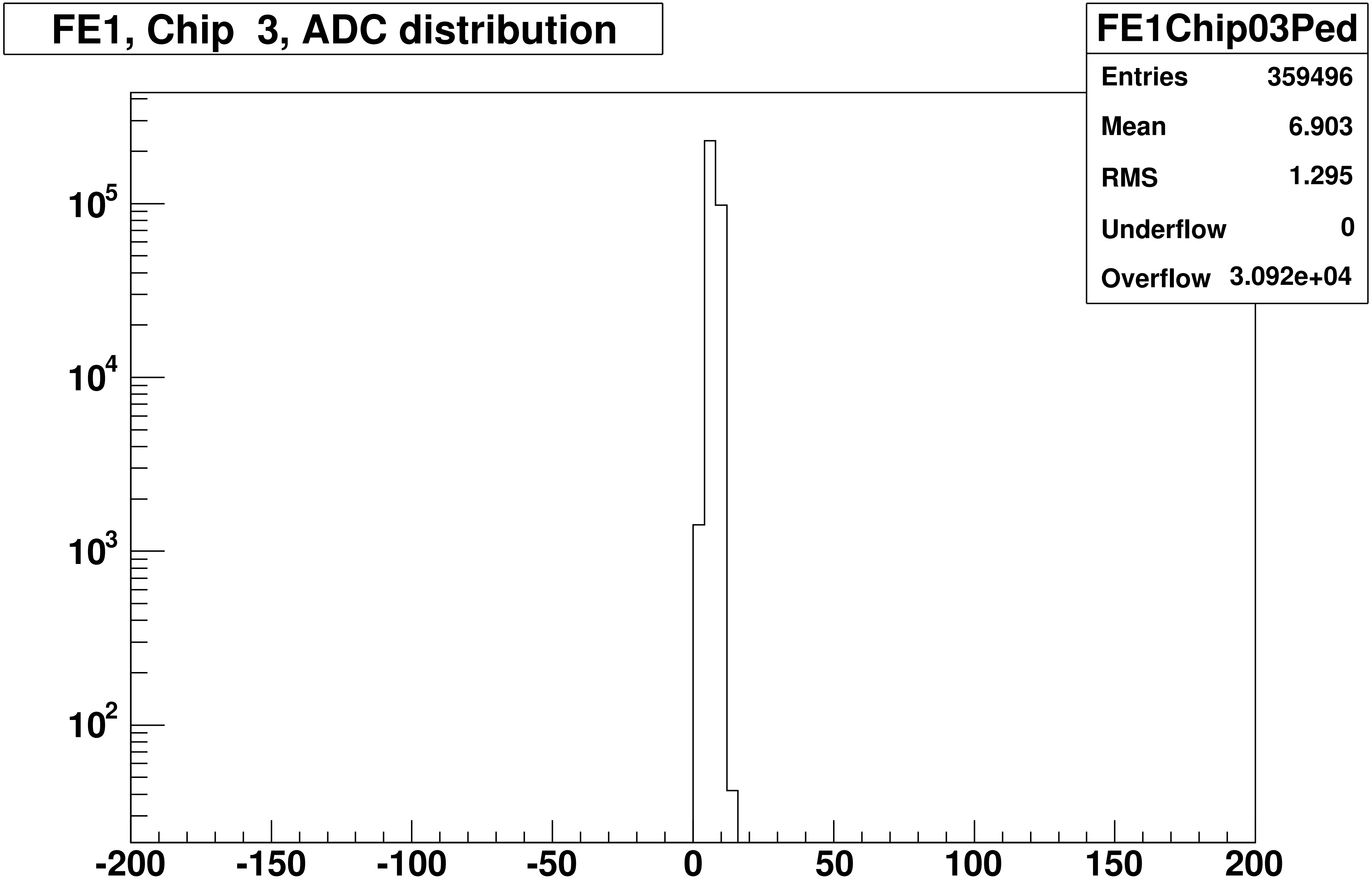
10000
15000
20000
25000


FE1, Chip 3, ADC distribution
FE1Chip03Ped
Entries 359496
Mean 6.903
RMS 1.295
Underflow 0
Overflow 3.092e+04
10^5
10^4
10^3
10^2
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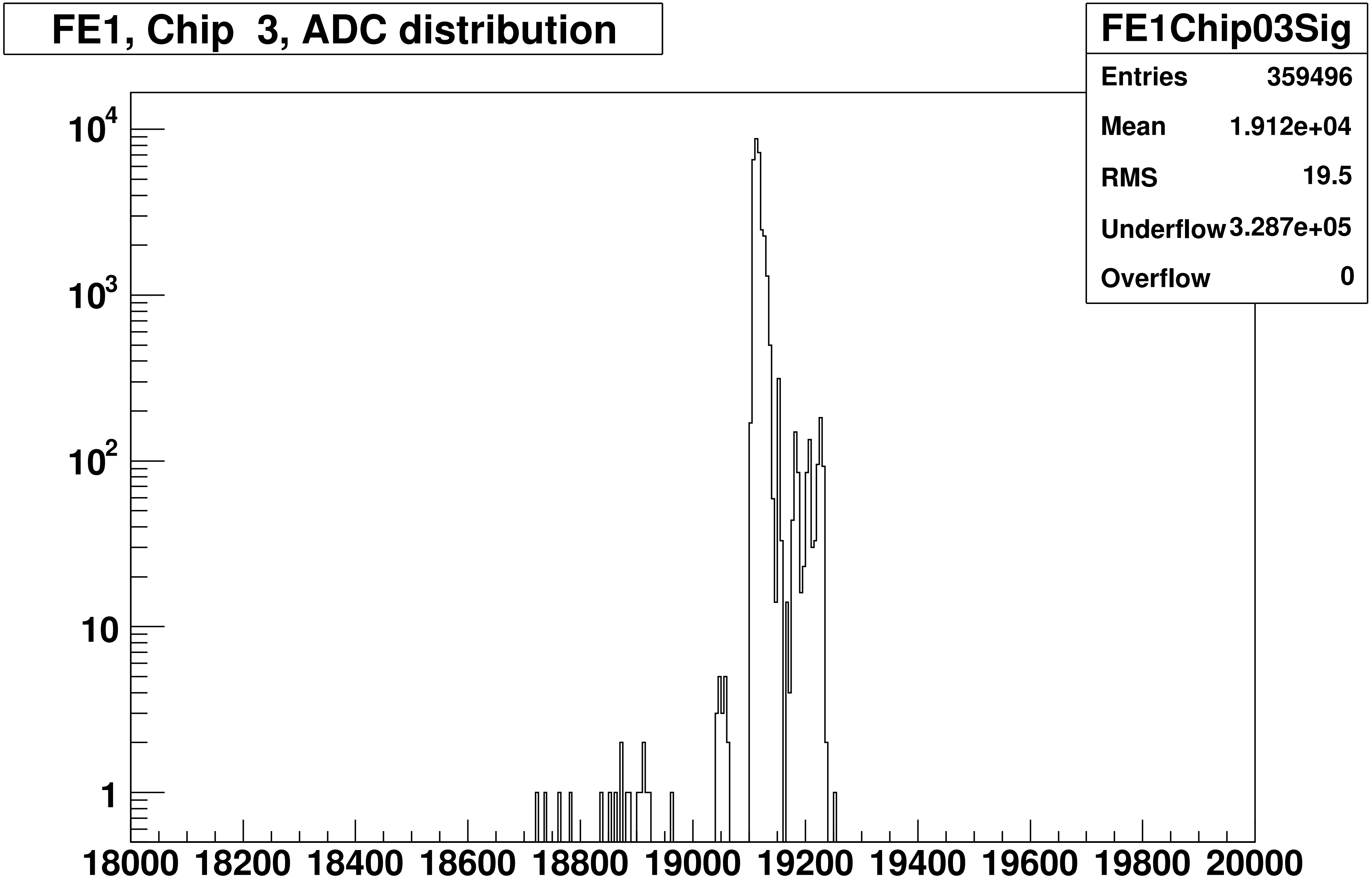
-100
-50
0
50
100
150
200


FE1, Chip 3, ADC distribution
FE1Chip03Sig
Entries 359496
Mean 1.912e+04
RMS 19.5
Underflow 3.287e+05
Overflow 0
10^4
10^3
10^2
10
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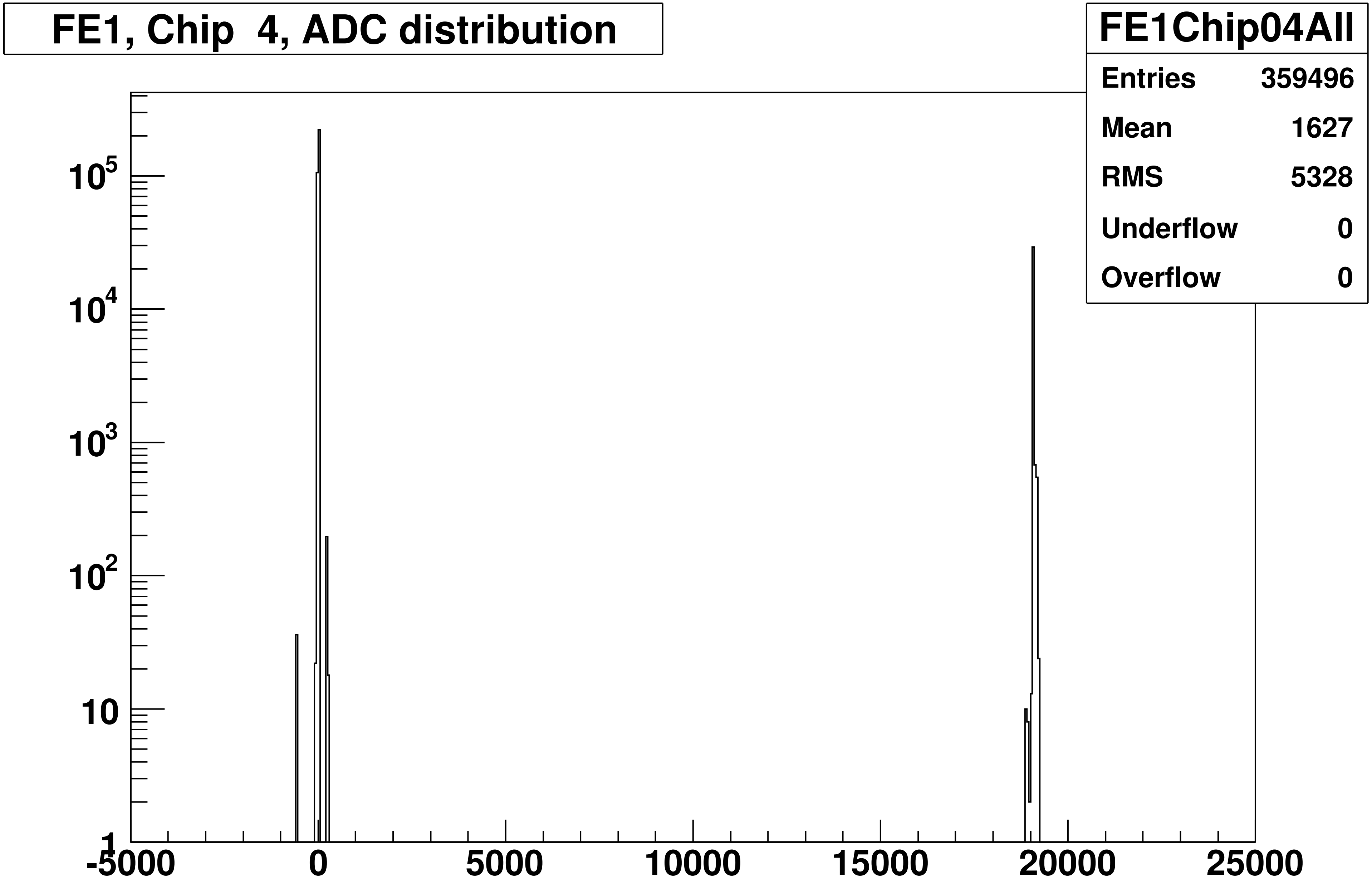
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE1, Chip 4, ADC distribution
FE1Chip04All
Entries 359496
Mean 1627
RMS 5328
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
1
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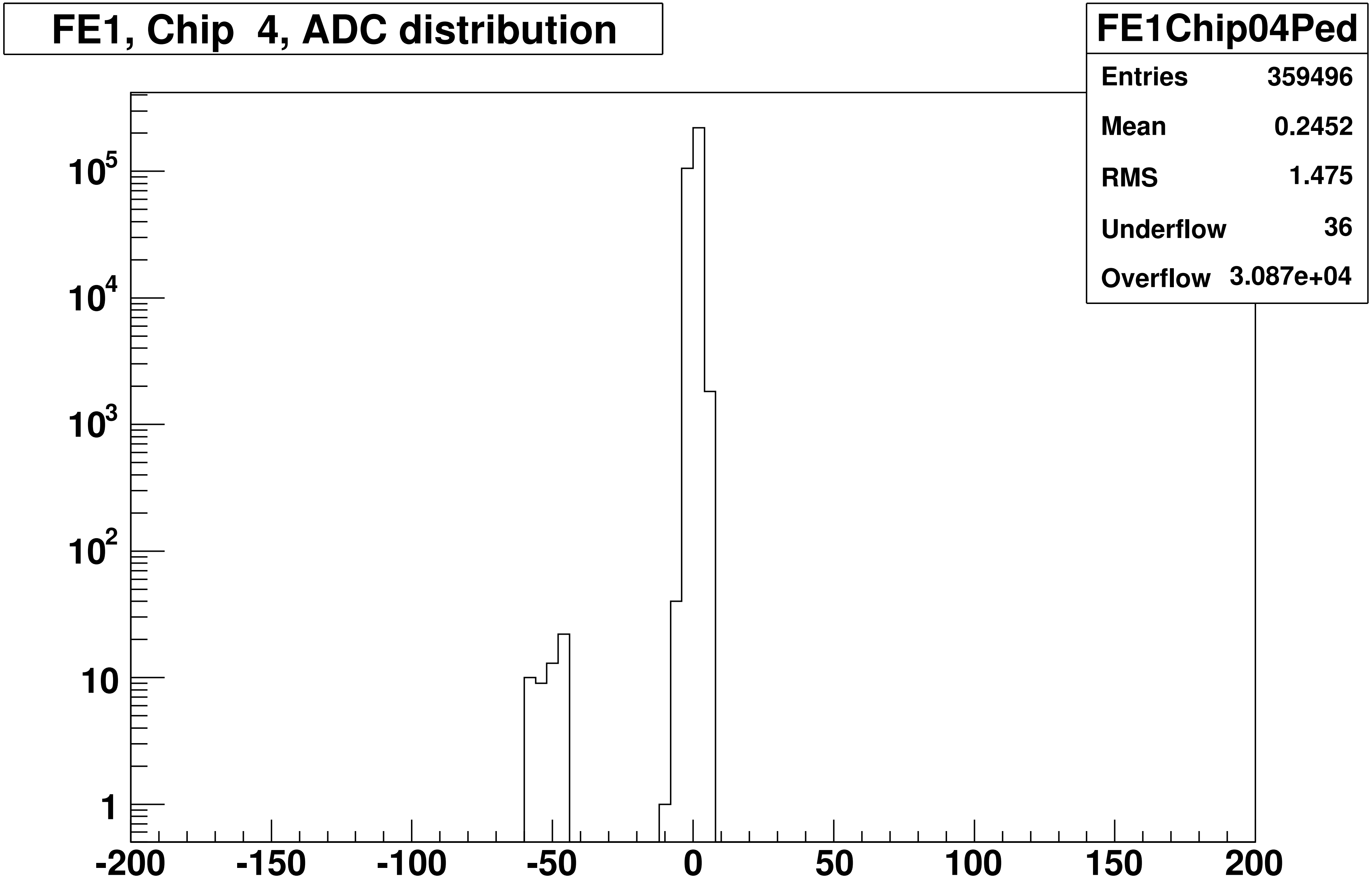
10000
15000
20000
25000



FE1, Chip 4, ADC distribution
FE1Chip04Ped
Entries 359496
Mean 0.2452
RMS 1.475
Underflow 36
Overflow 3.087e+04
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10^4
10^3
10^2
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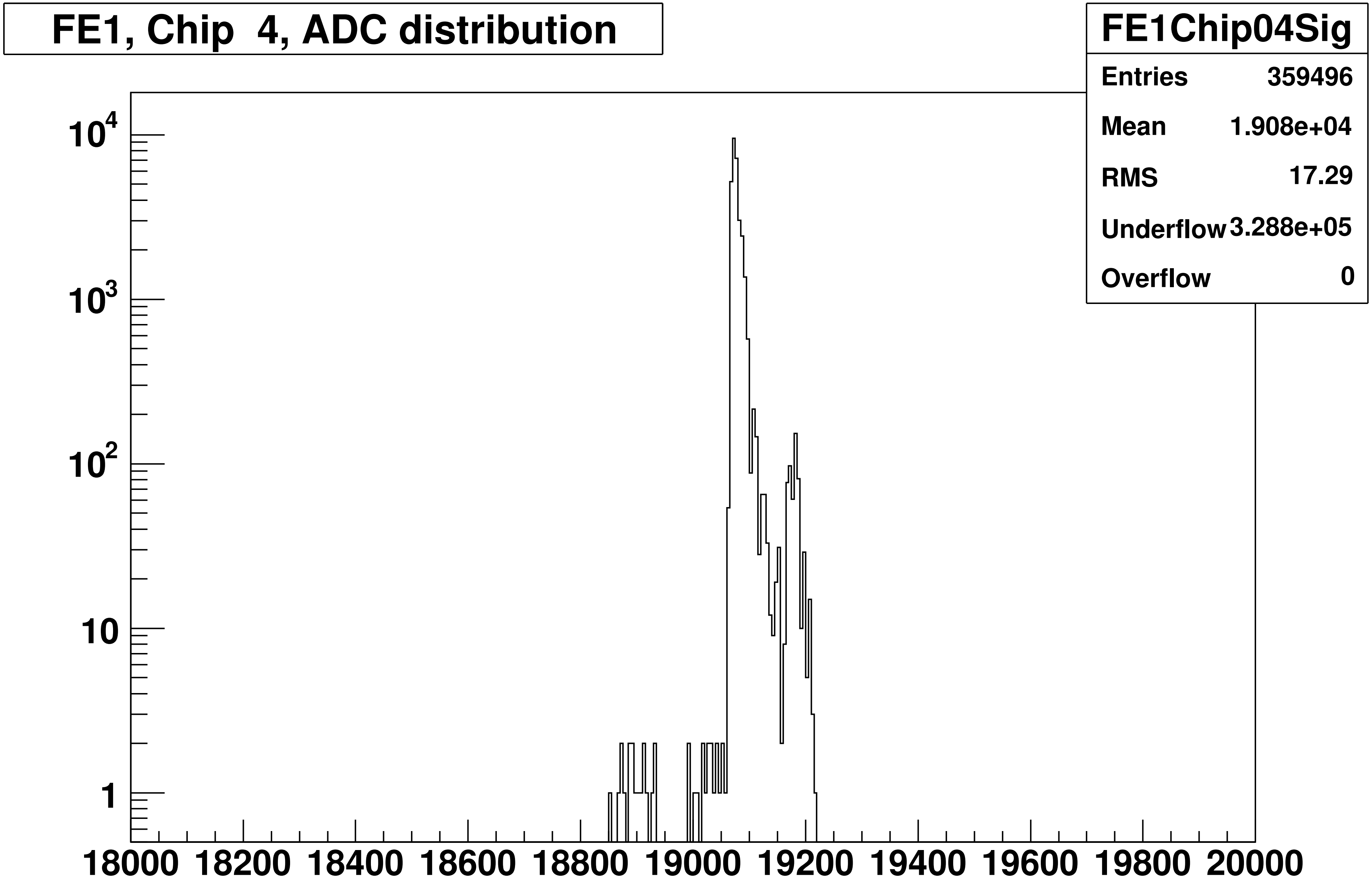
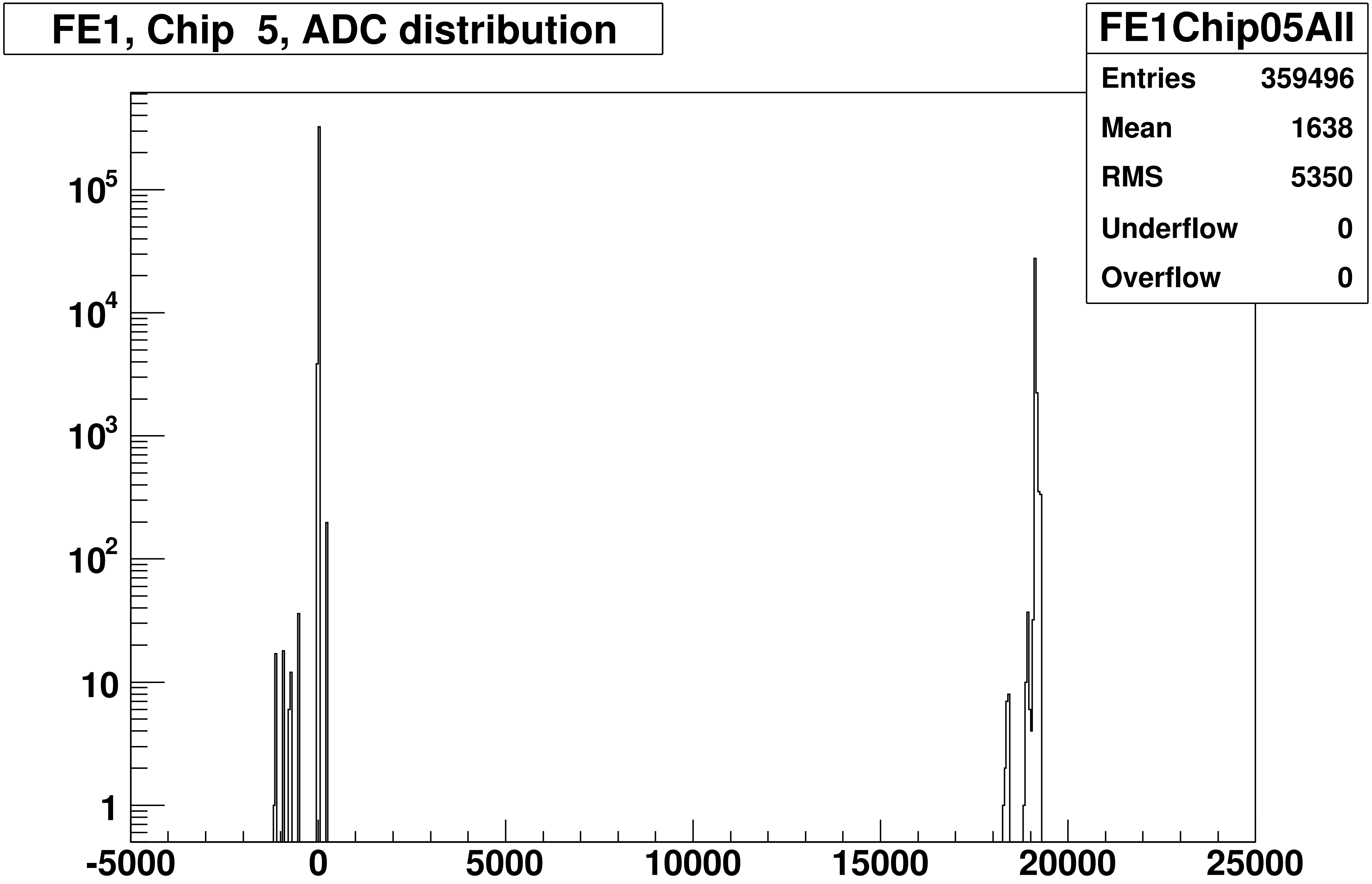
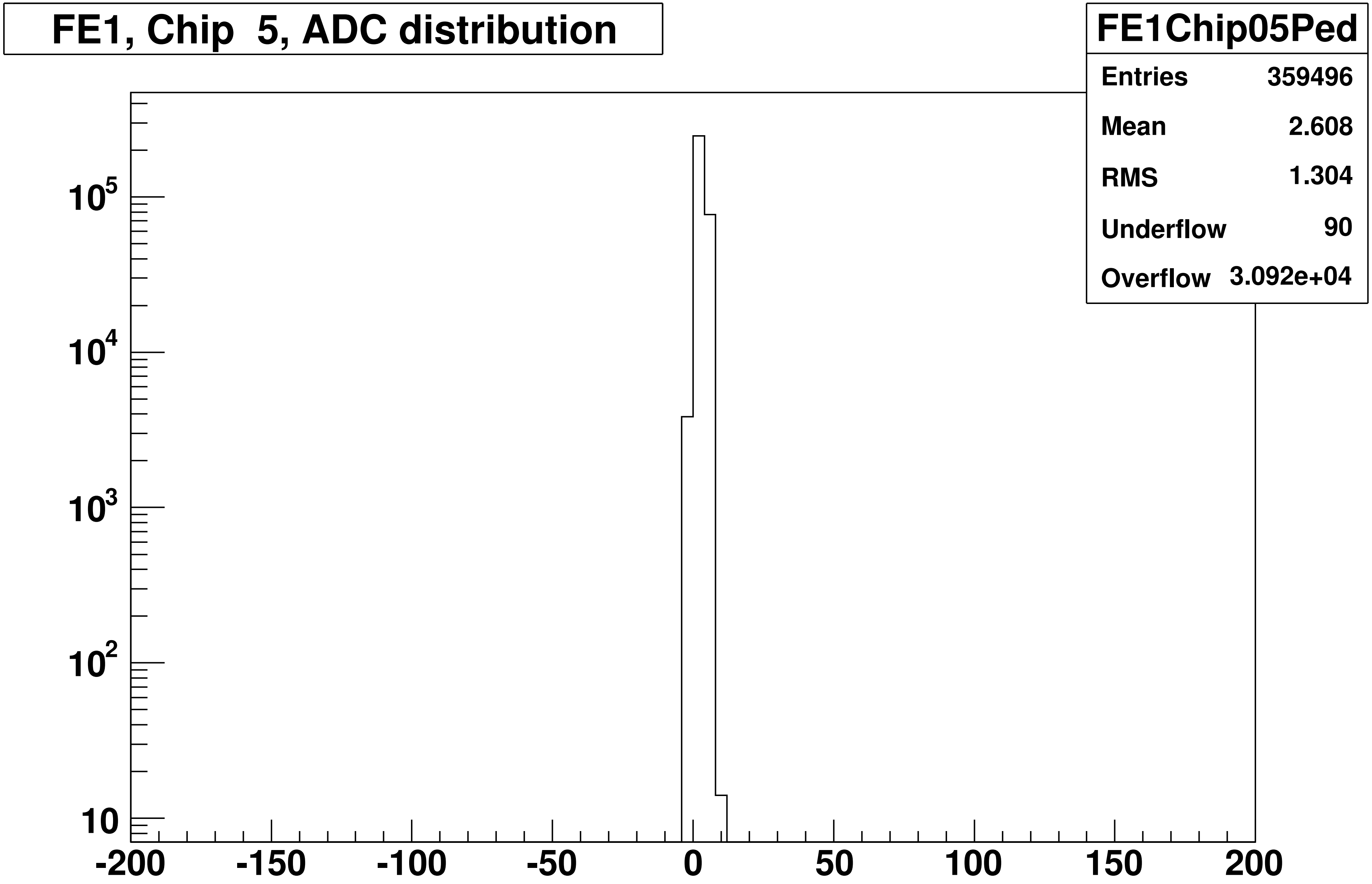
100
150
200


FE1, Chip 4, ADC distribution
FE1Chip04Sig
Entries 359496
Mean 1.908e+04
RMS 17.29
Underflow 3.288e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000


FE1, Chip 5, ADC distribution
FE1Chip05All
Entries 359496
Mean 1638
RMS 5350
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE1, Chip 5, ADC distribution
FE1Chip05Ped
Entries 359496
Mean 2.608
RMS 1.304
Underflow 90
Overflow 3.092e+04
10
10^2
10^3
10^4
10^5
-200
-150
-100
-50
0
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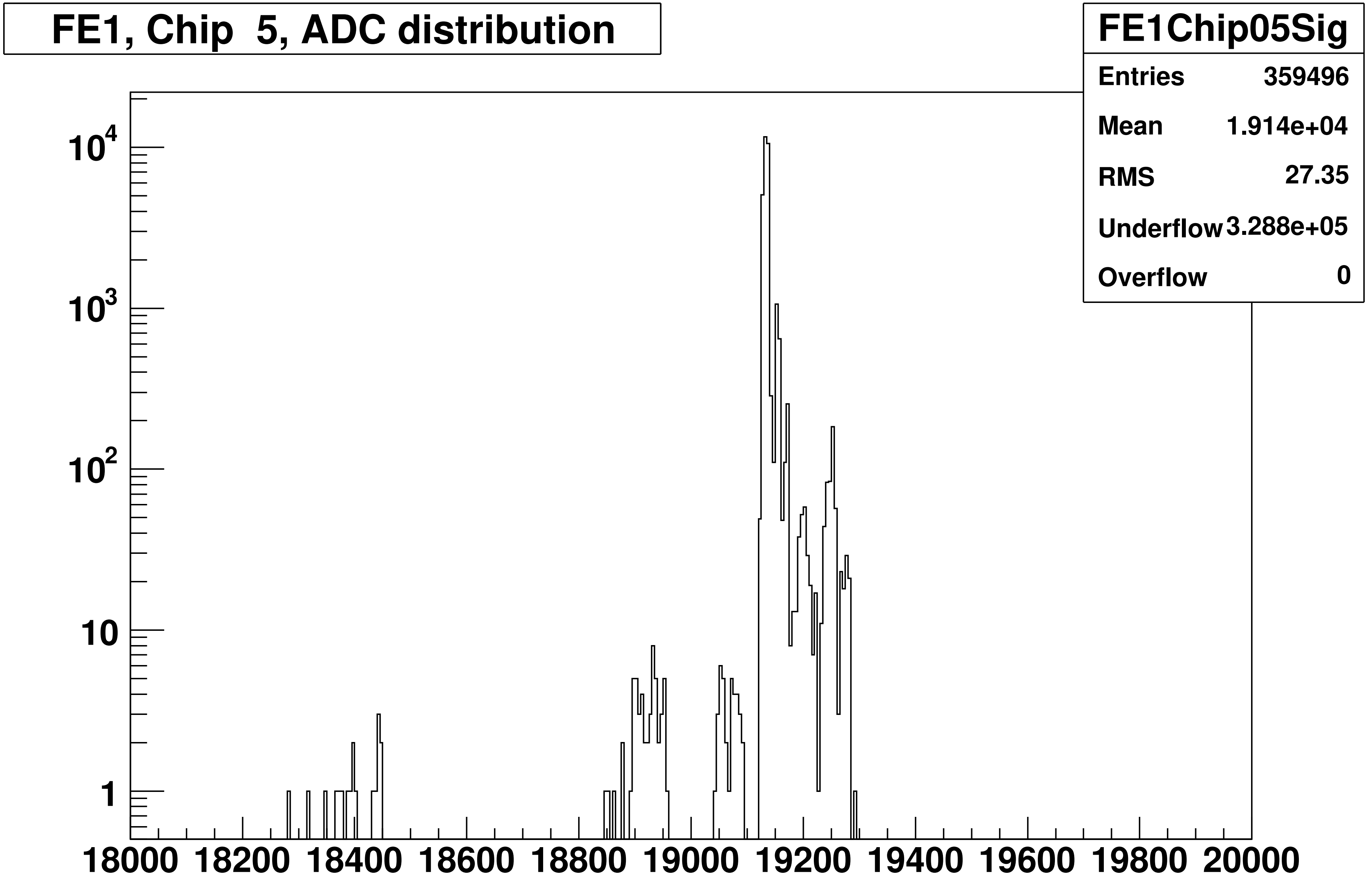
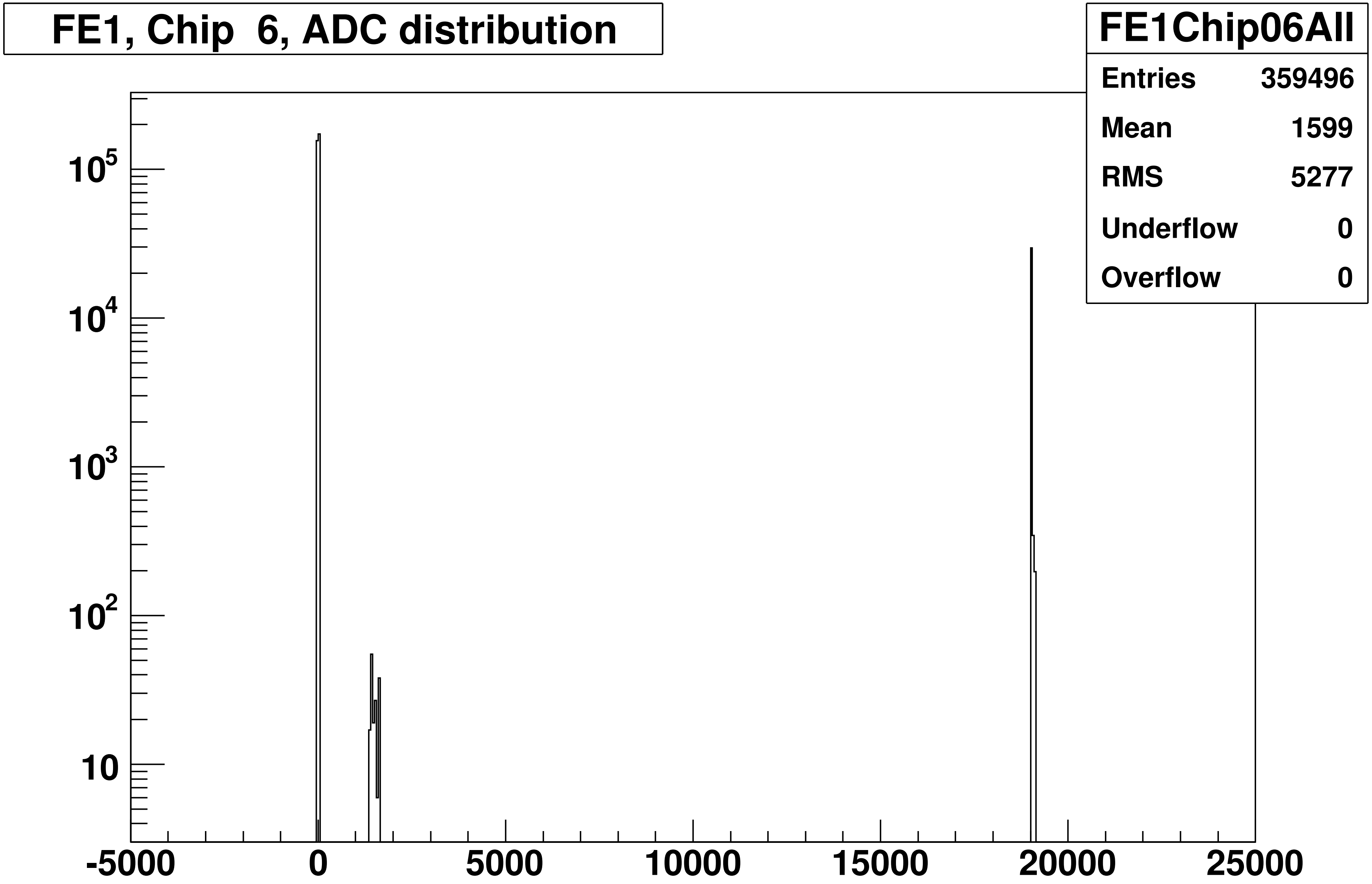
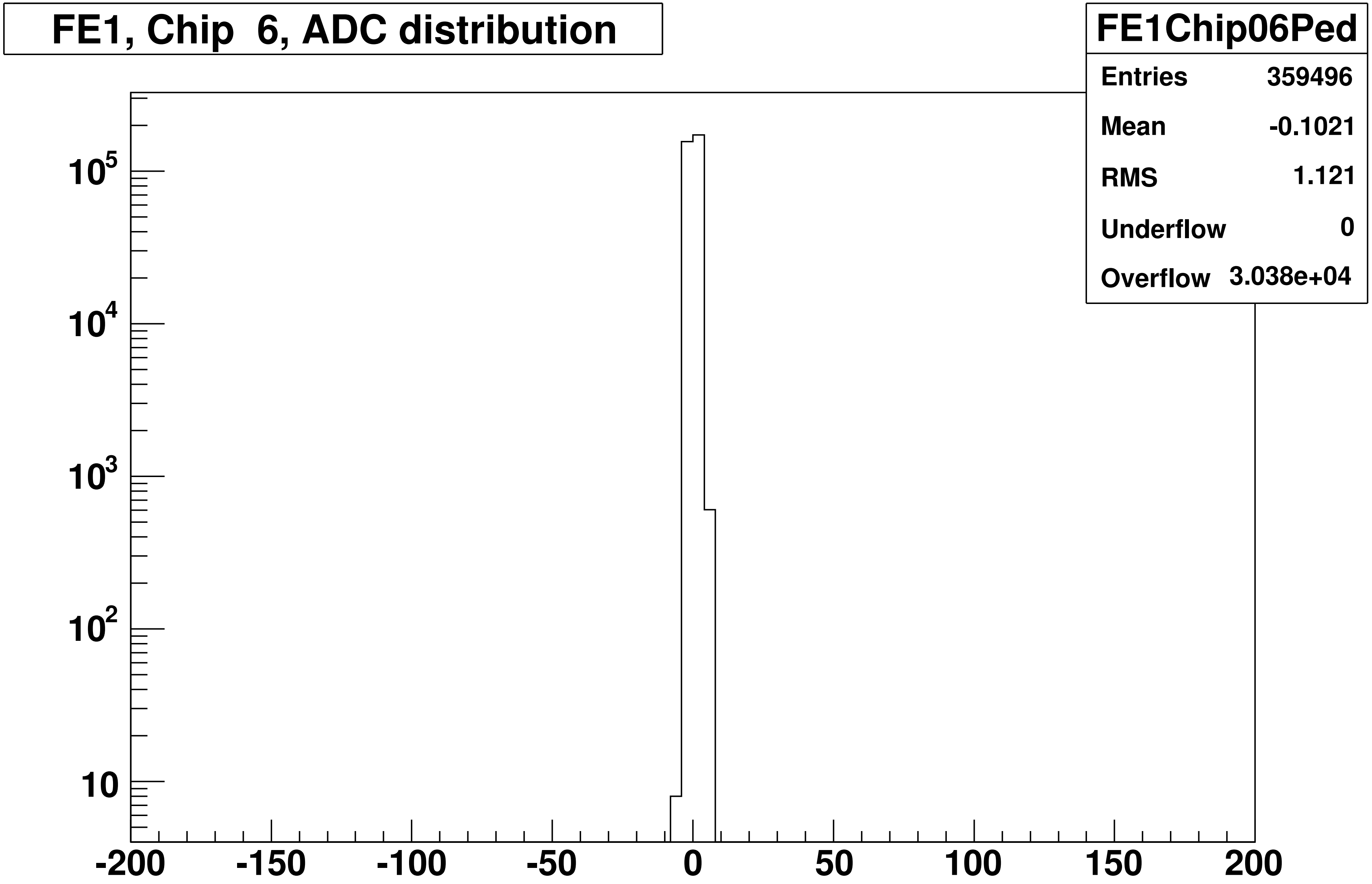
100
150
200



FE1, Chip 5, ADC distribution
FE1Chip05Sig
Entries 359496
Mean 1.914e+04
RMS 27.35
Underflow 3.288e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE1, Chip 6, ADC distribution
FE1Chip06All
Entries 359496
Mean 1599
RMS 5277
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000



FE1, Chip 6, ADC distribution
FE1Chip06Ped
Entries 359496
Mean -0.1021
RMS 1.121
Underflow 0
Overflow 3.038e+04
10
10^2
10^3
10^4
10^5
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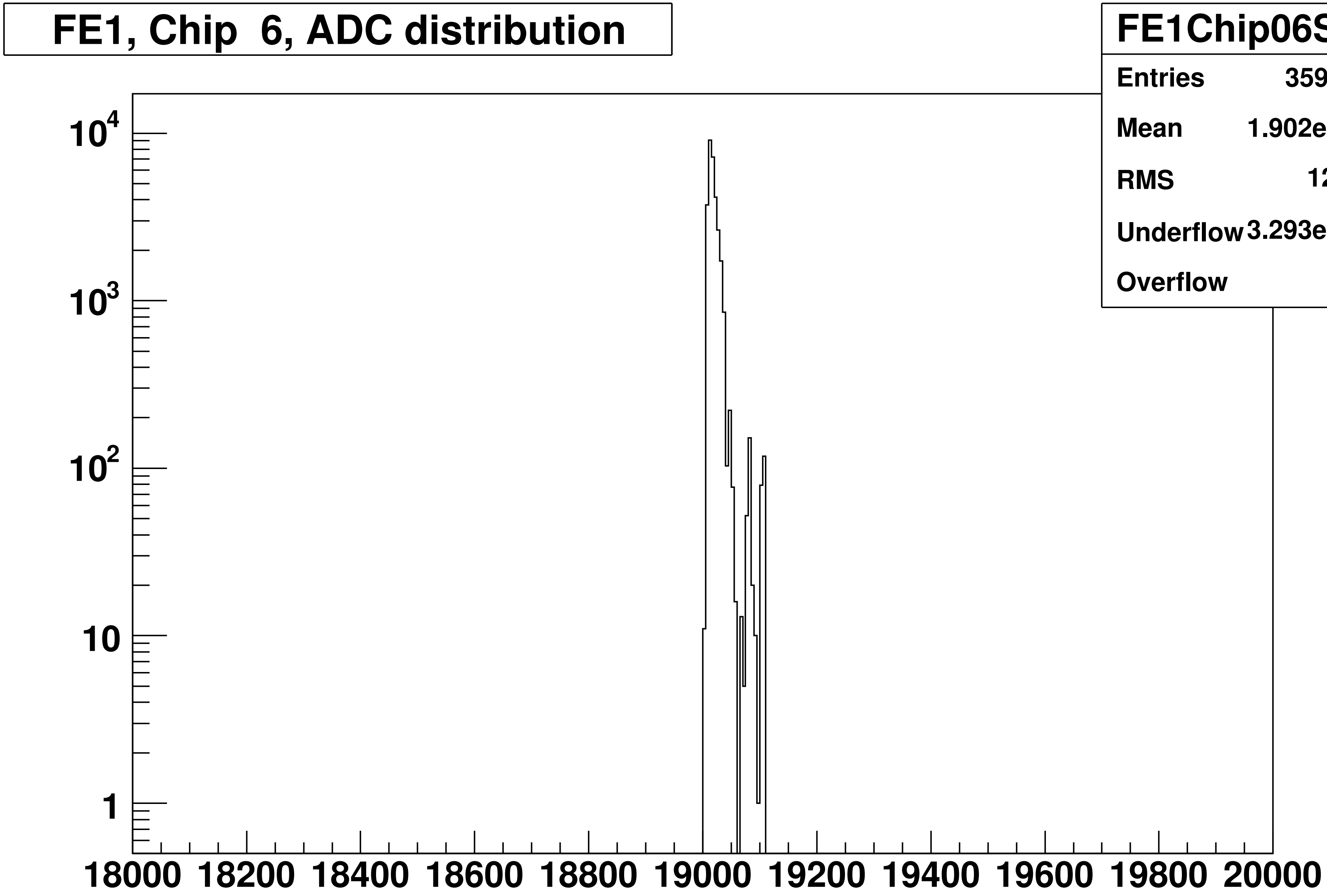
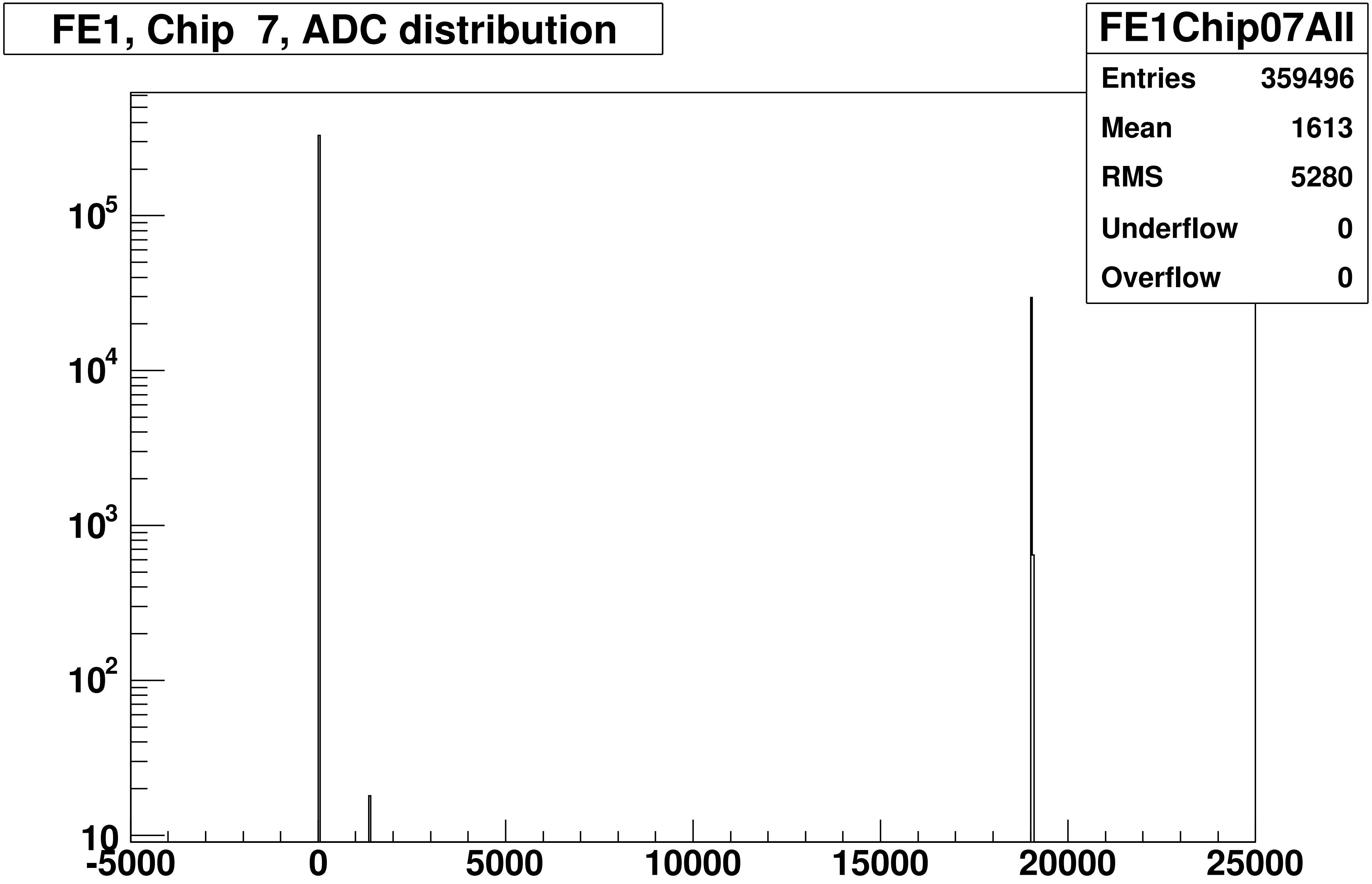
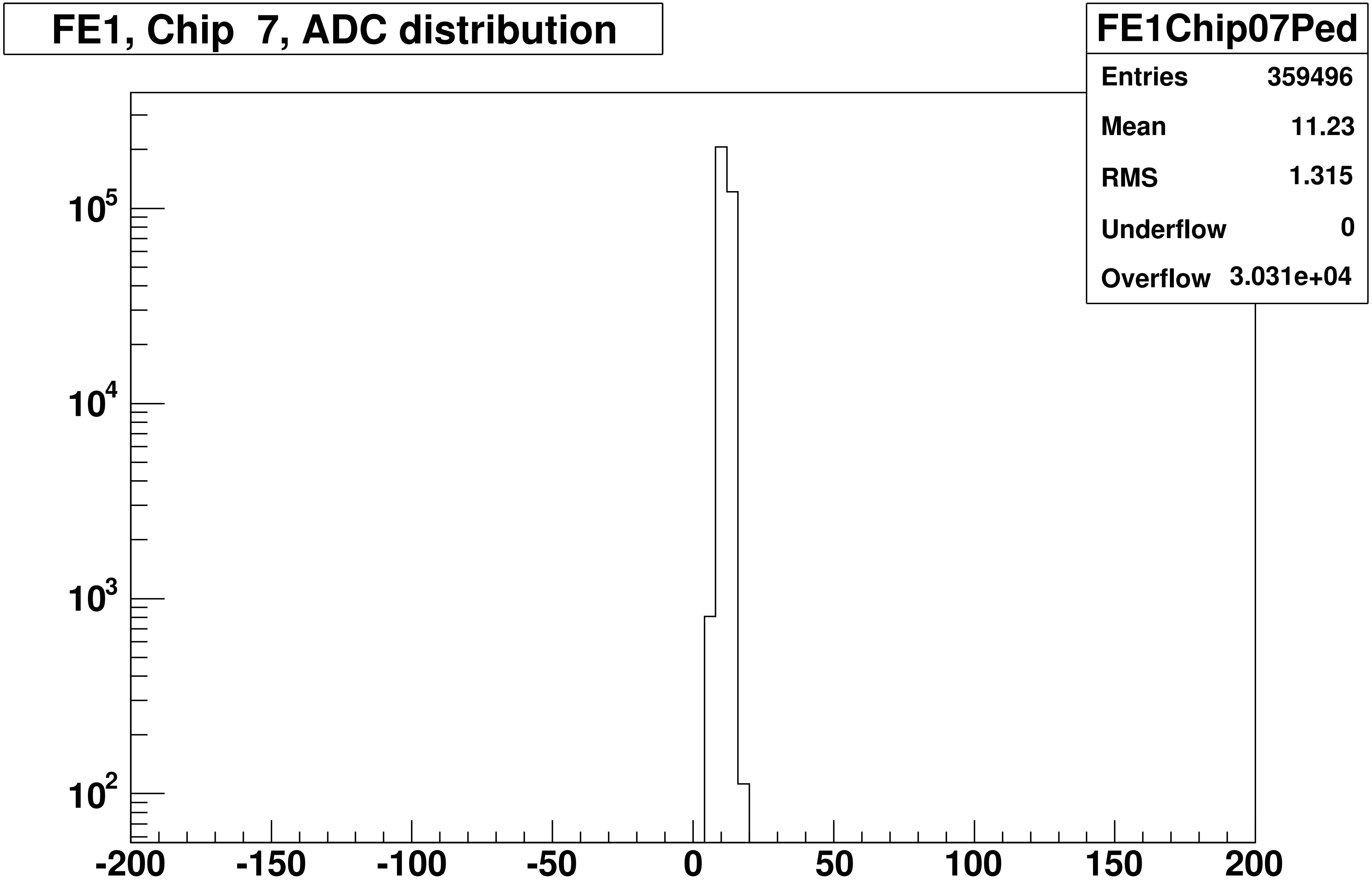
-150
-100
-50
0
50
100
150
200



FE1, Chip 6, ADC distribution
FE1Chip06Sig
Entries 359496
Mean 1.902e+04
RMS 12.19
Underflow 3.293e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000



FE1, Chip 7, ADC distribution
FE1Chip07All
Entries 359496
Mean 1613
RMS 5280
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000



FE1, Chip 7, ADC distribution
FE1Chip07Ped
Entries 359496
Mean 11.23
RMS 1.315
Underflow 0
Overflow 3.031e+04
10^5
10^4
10^3
10^2
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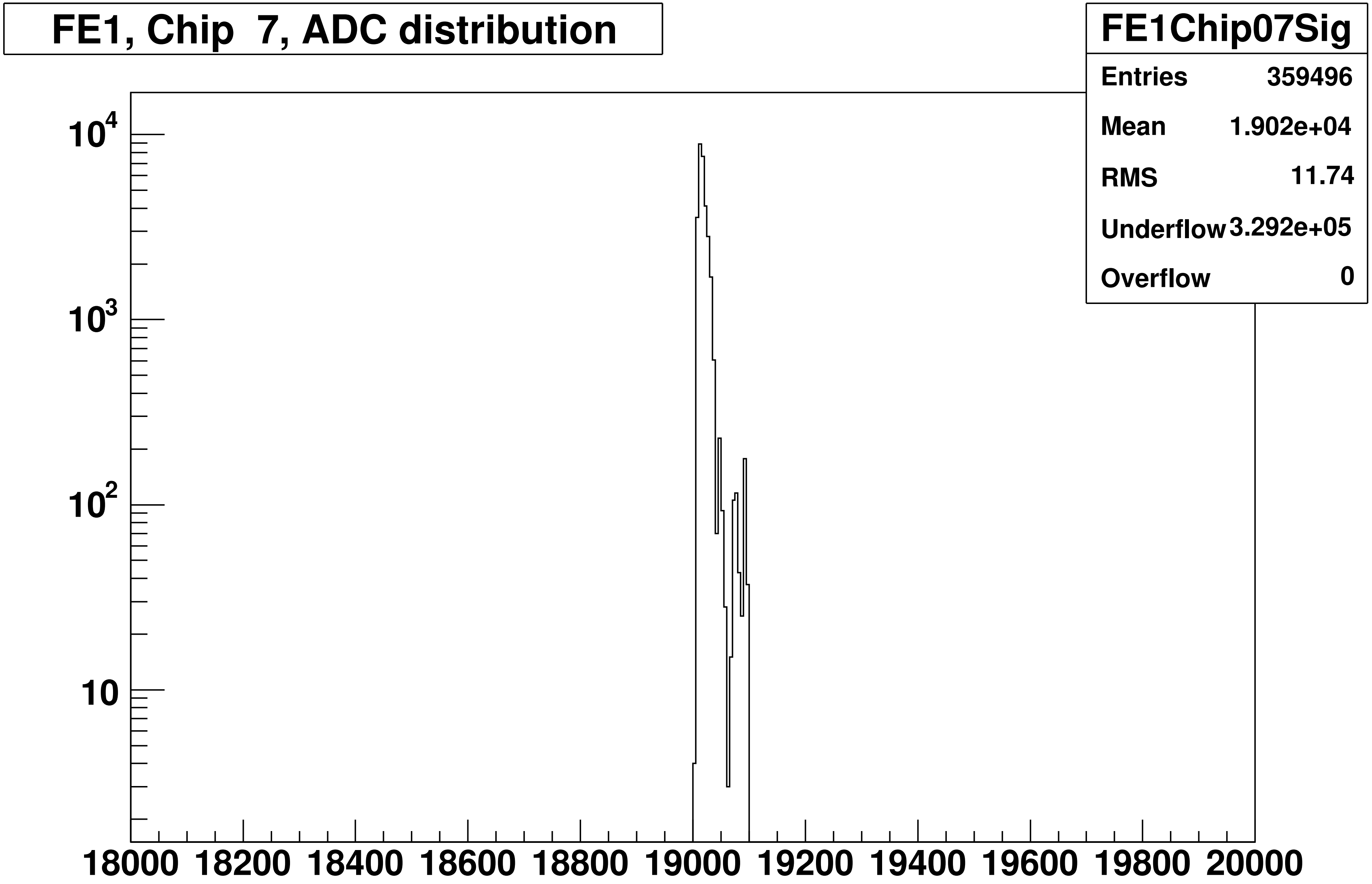
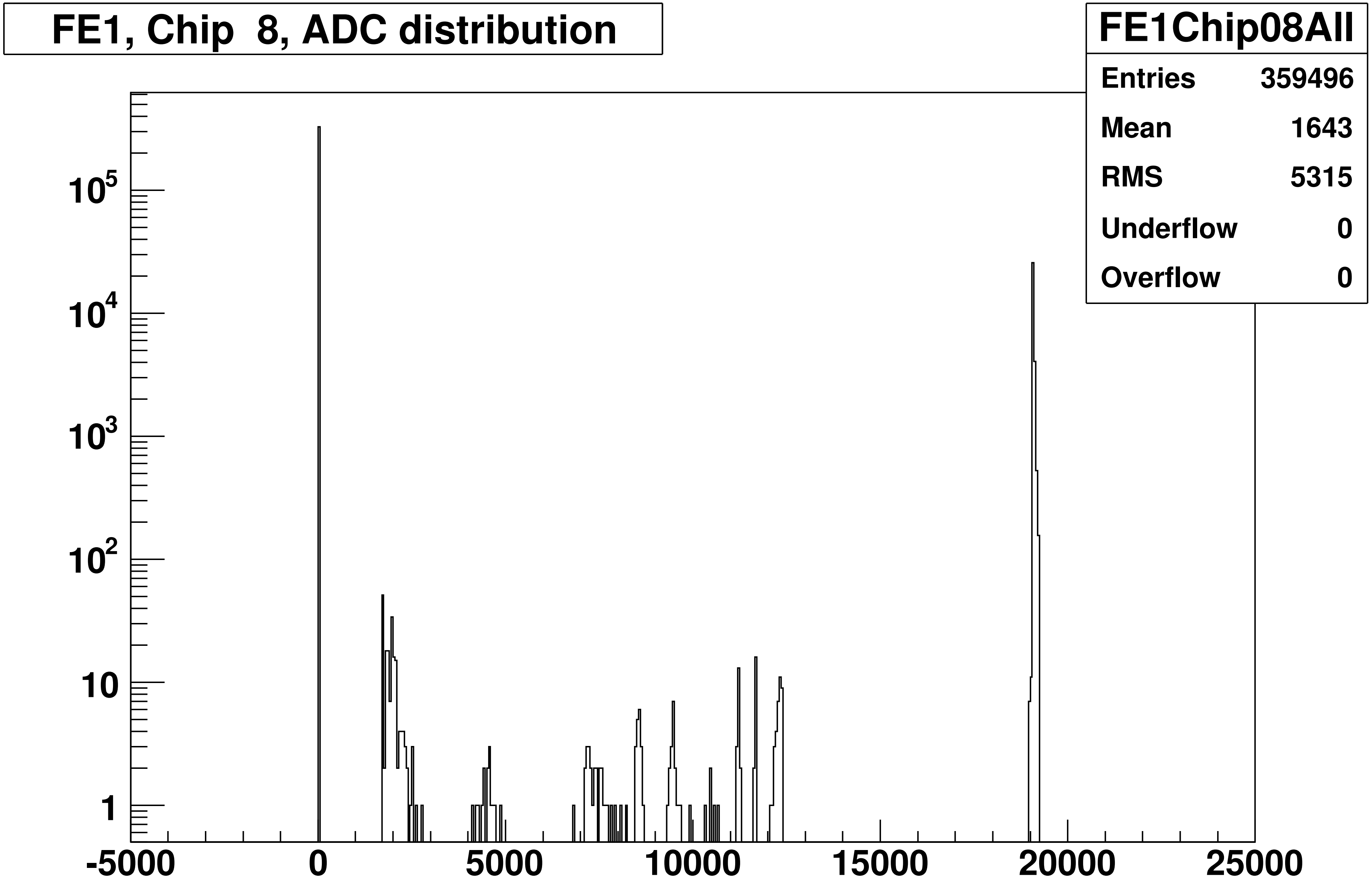
-100
-50
0
50
100
150
200



FE1, Chip 7, ADC distribution
FE1Chip07Sig
Entries 359496
Mean 1.902e+04
RMS 11.74
Underflow 3.292e+05
Overflow 0
10^4
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE1, Chip 8, ADC distribution
FE1Chip08All
Entries 359496
Mean 1643
RMS 5315
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
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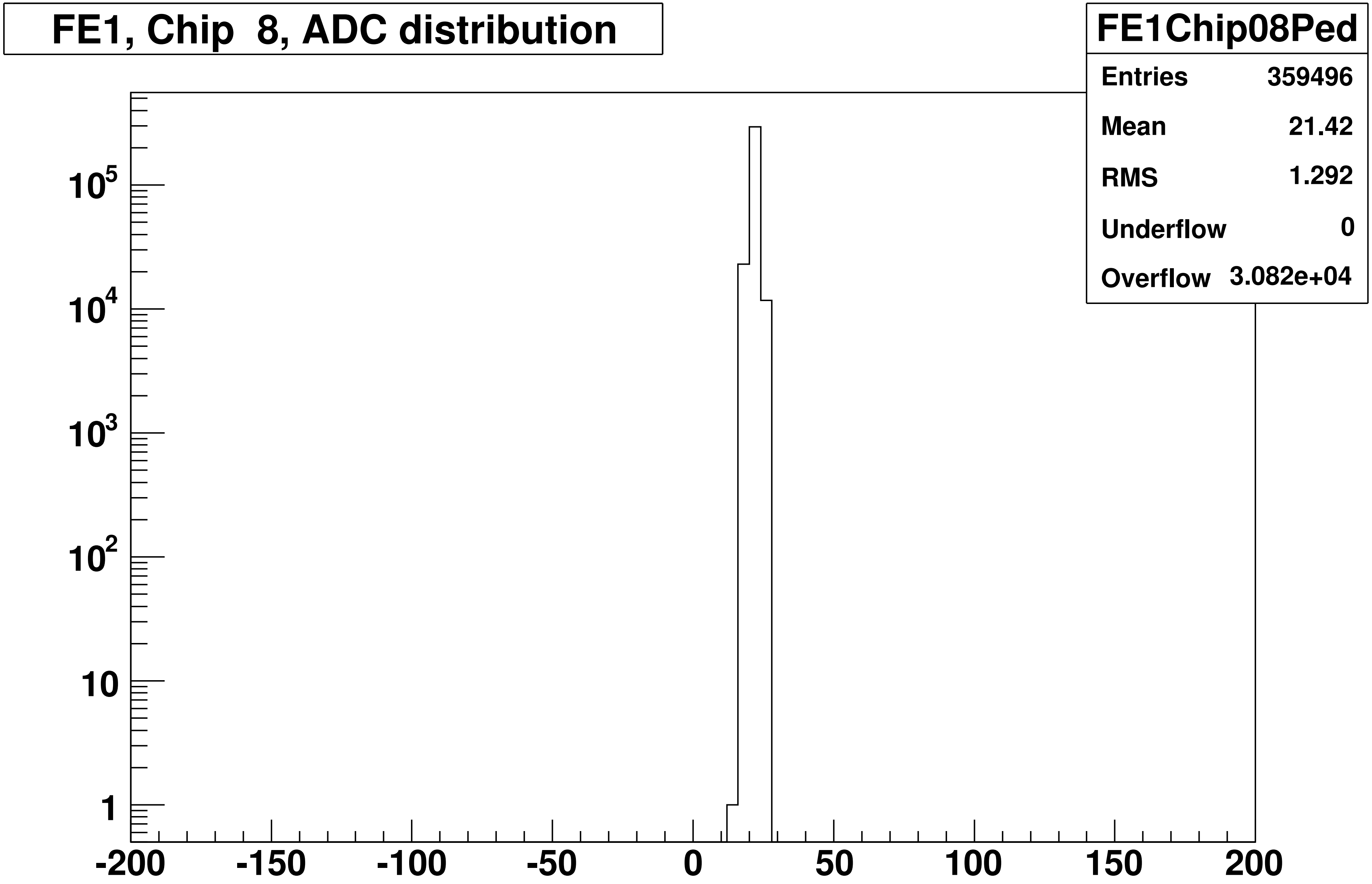
10000
15000
20000
25000


FE1, Chip 8, ADC distribution
FE1Chip08Ped
Entries 359496
Mean 21.42
RMS 1.292
Underflow 0
Overflow 3.082e+04
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10^3
10^2
10
1
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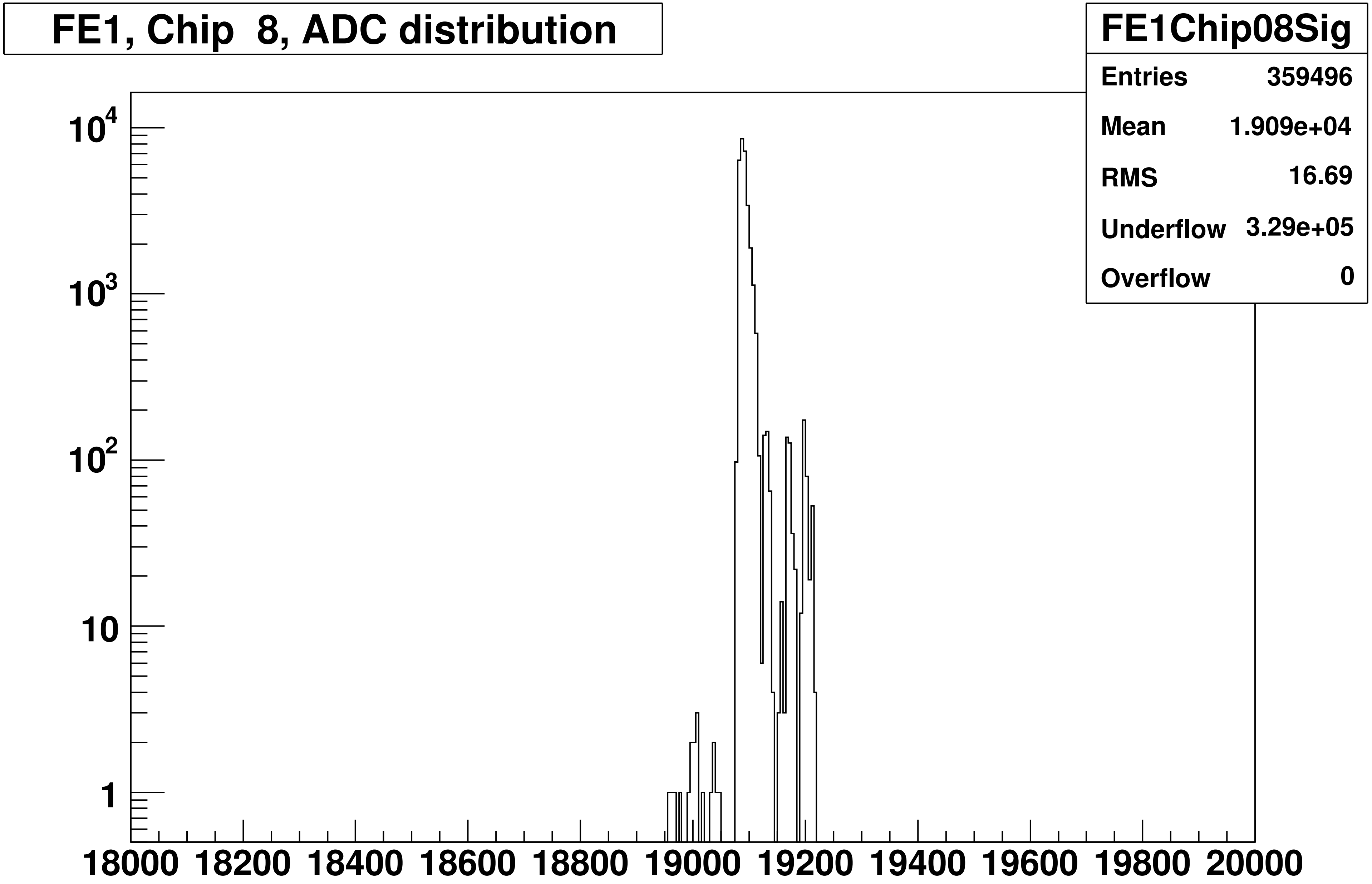
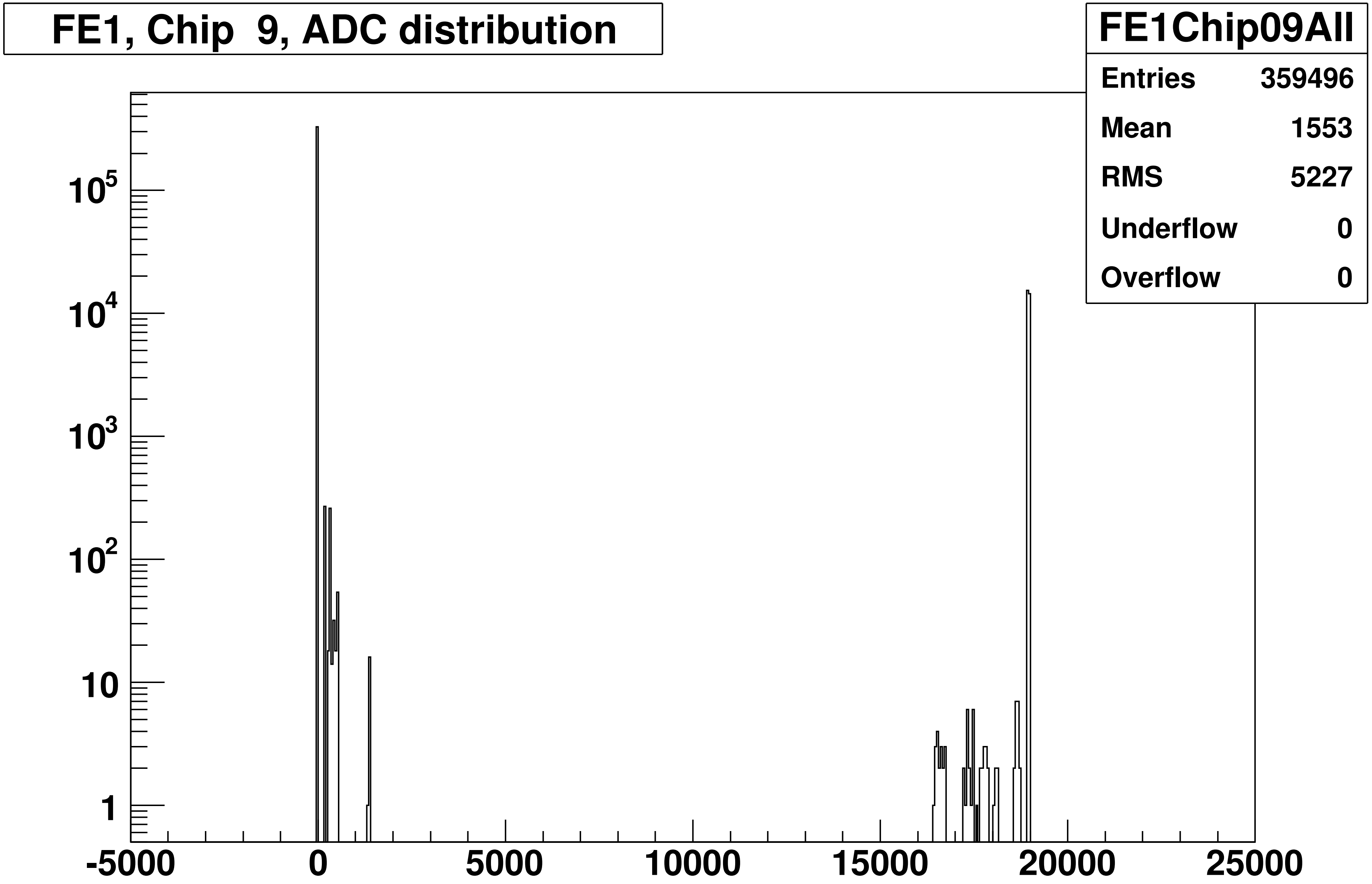
100
150
200



FE1, Chip 8, ADC distribution
FE1Chip08Sig
Entries 359496
Mean 1.909e+04
RMS 16.69
Underflow 3.29e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000


FE1, Chip 9, ADC distribution
FE1Chip09All
Entries 359496
Mean 1553
RMS 5227
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
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-5000
0
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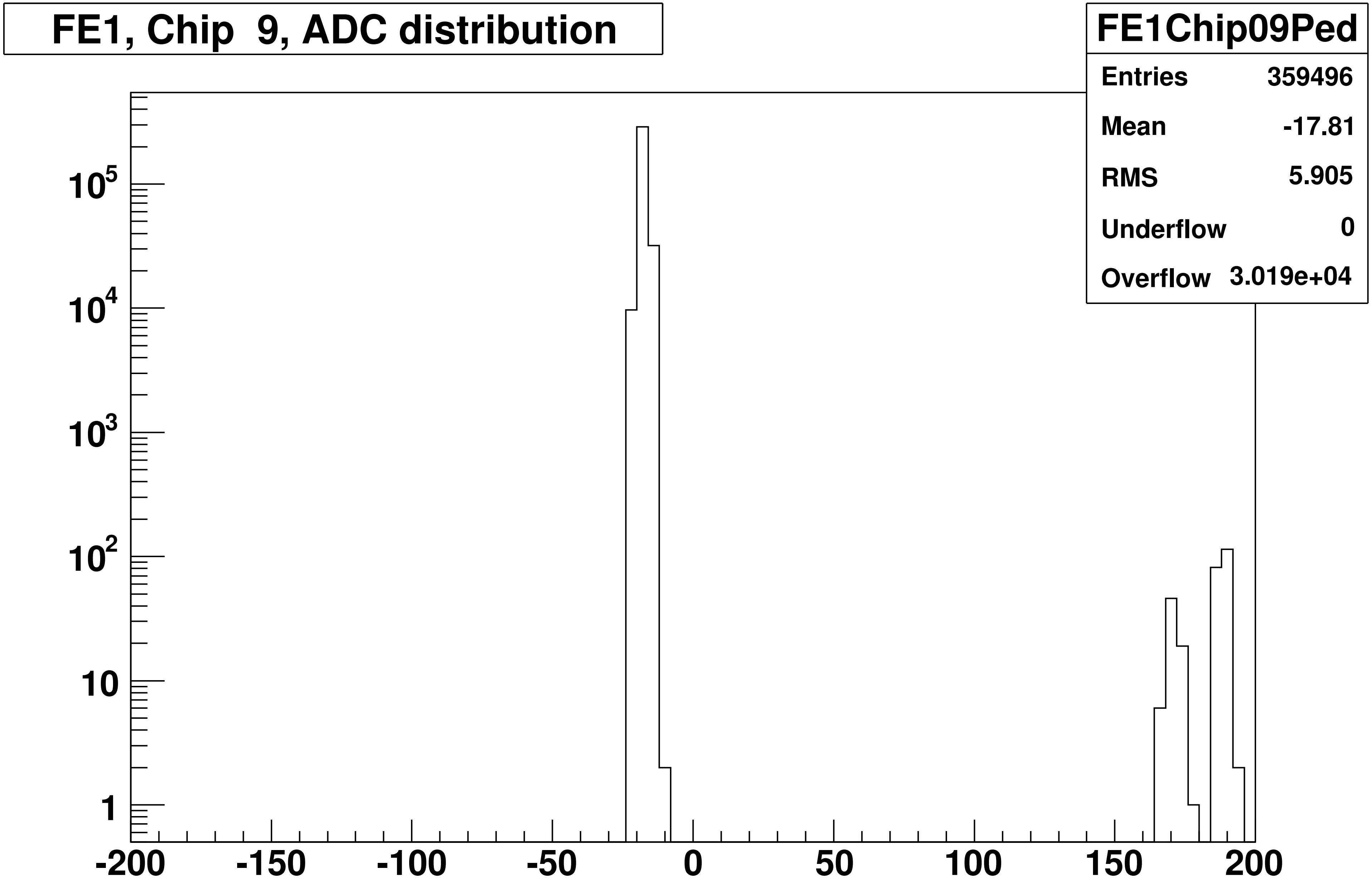
10000
15000
20000
25000



FE1, Chip 9, ADC distribution
FE1Chip09Ped
Entries 359496
Mean -17.81
RMS 5.905
Underflow 0
Overflow 3.019e+04
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10^4
10^3
10^2
10
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-100
-50
0
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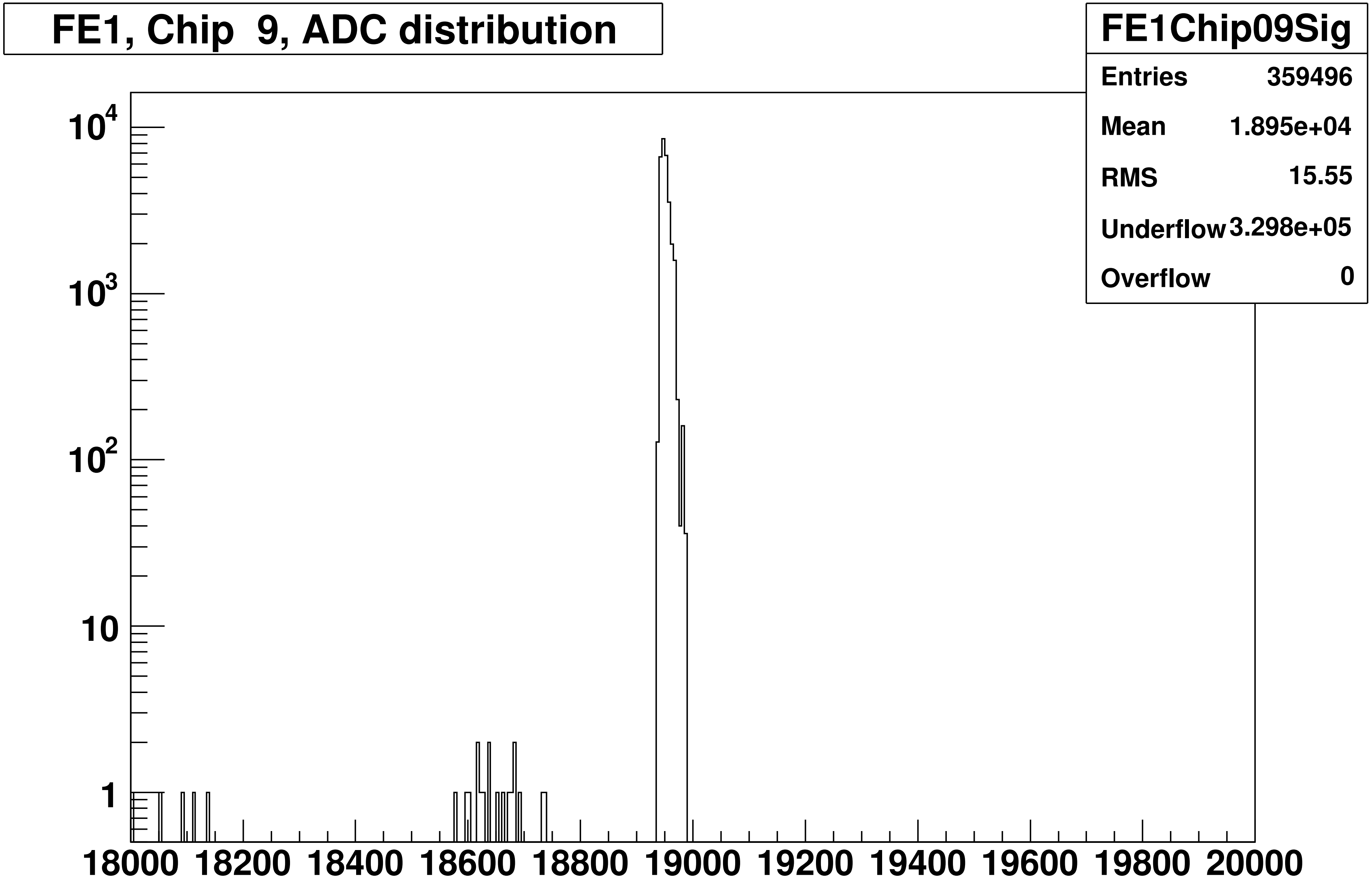
100
150
200


FE1, Chip 9, ADC distribution
FE1Chip09Sig
Entries 359496
Mean 1.895e+04
RMS 15.55
Underflow 3.298e+05
Overflow 0
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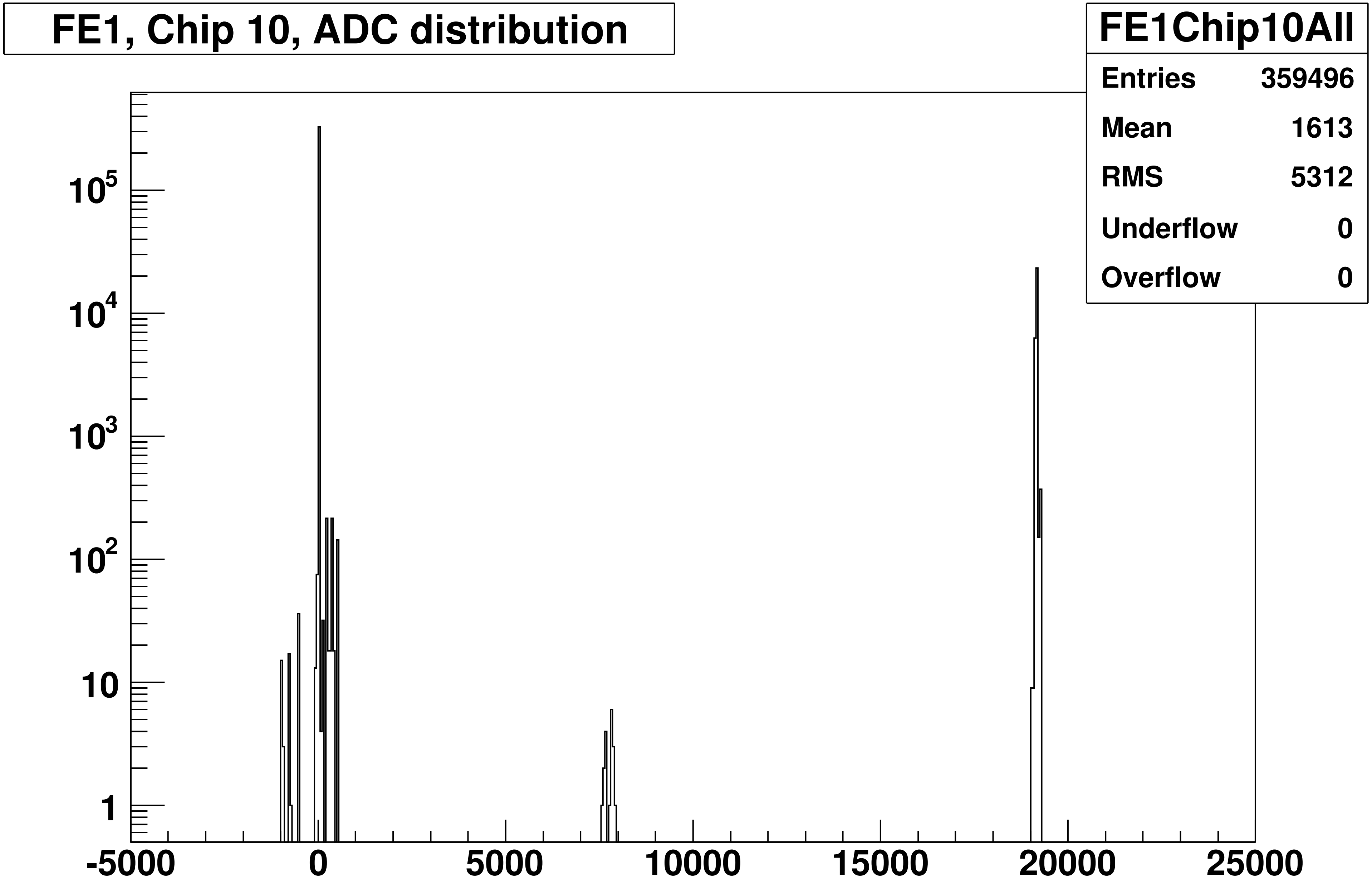
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE1, Chip 10, ADC distribution
FE1Chip10All
Entries 359496
Mean 1613
RMS 5312
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
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-5000
0
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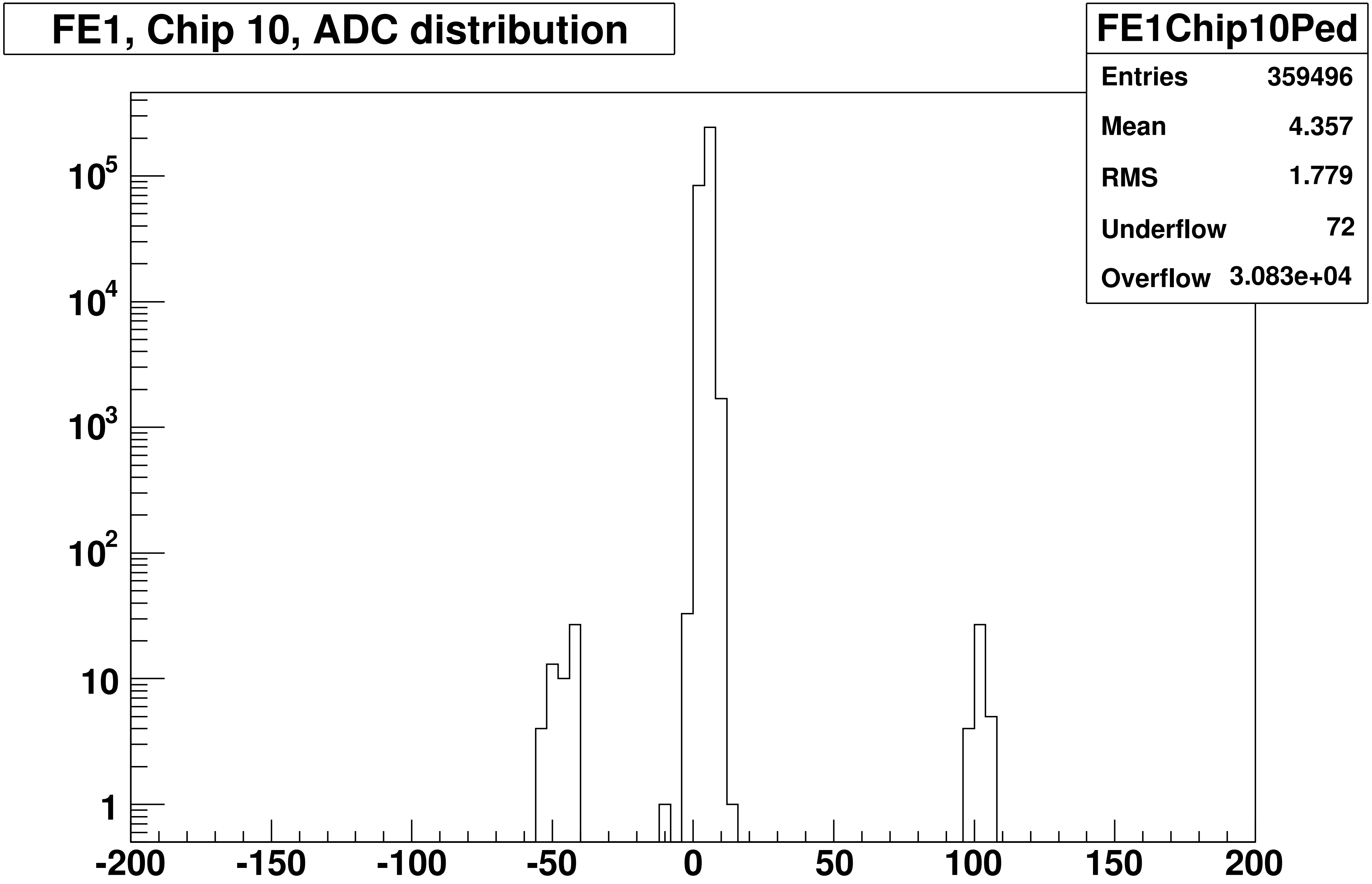
10000
15000
20000
25000


FE1, Chip 10, ADC distribution
FE1Chip10Ped
Entries 359496
Mean 4.357
RMS 1.779
Underflow 72
Overflow 3.083e+04
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10^4
10^3
10^2
10
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-100
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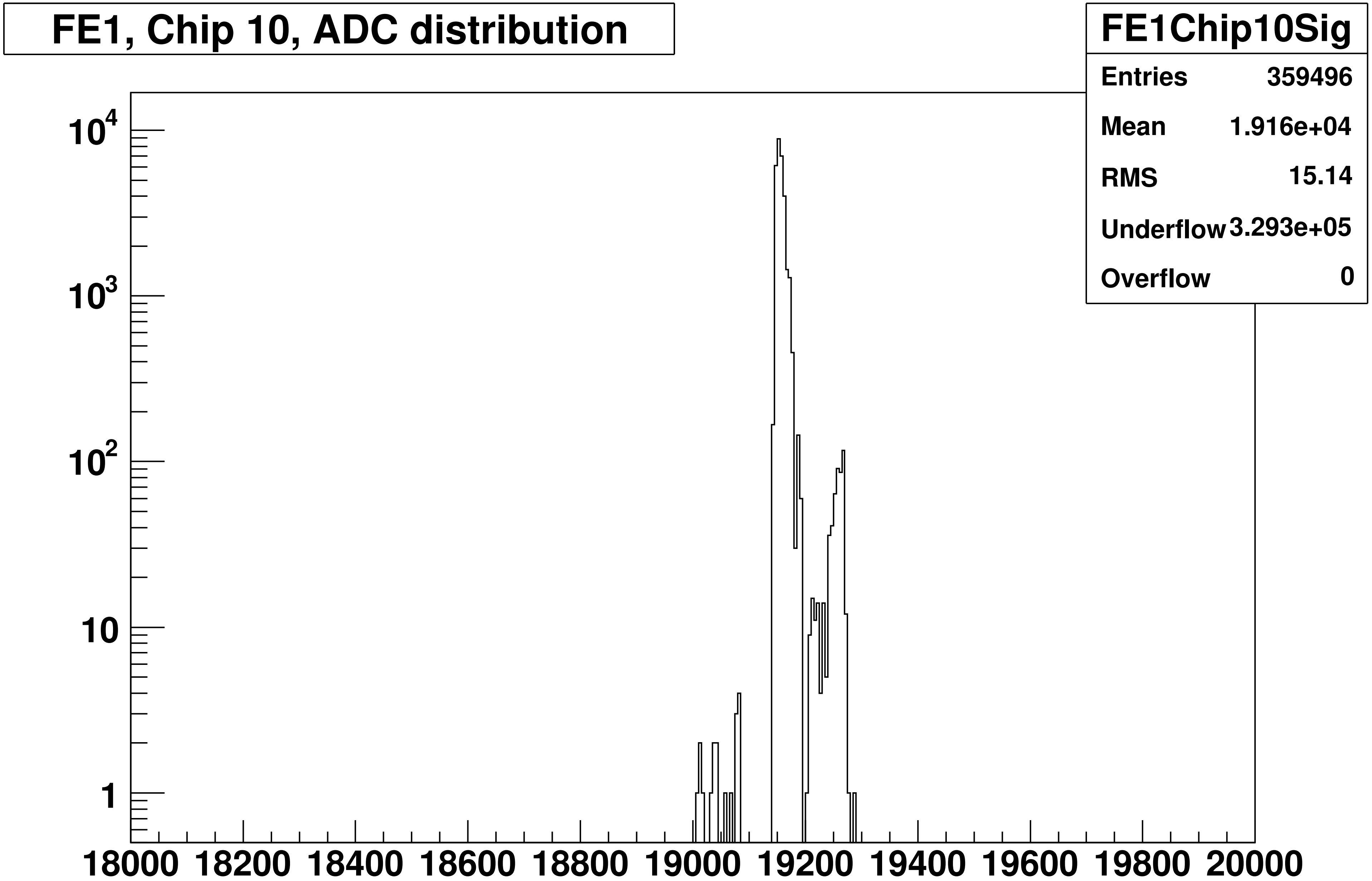
100
150
200


FE1, Chip 10, ADC distribution
FE1Chip10Sig
Entries 359496
Mean 1.916e+04
RMS 15.14
Underflow 3.293e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
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18400
18600
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19000
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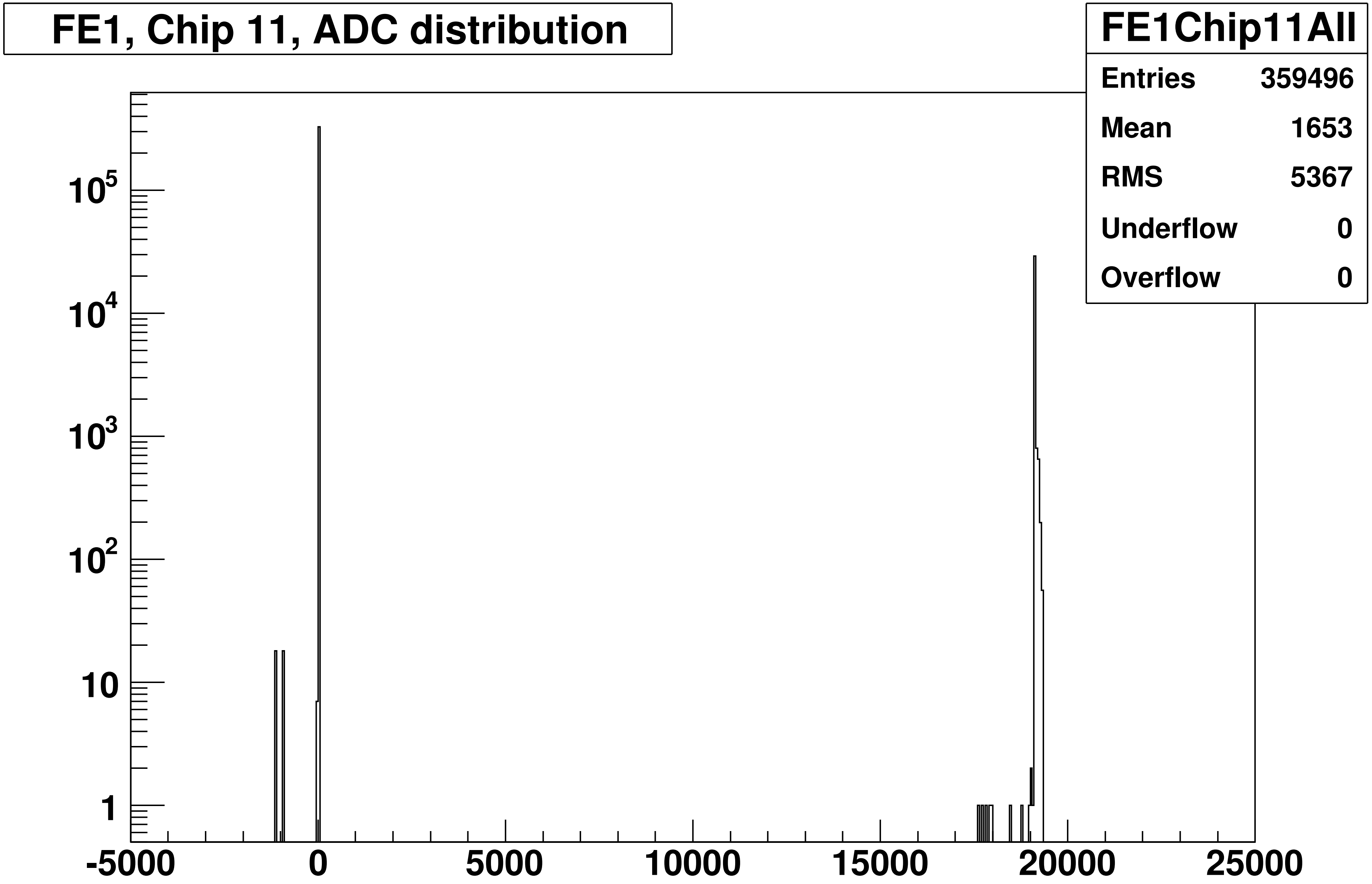
19600
19800
20000



FE1, Chip 11, ADC distribution
FE1Chip11All
Entries 359496
Mean 1653
RMS 5367
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
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0
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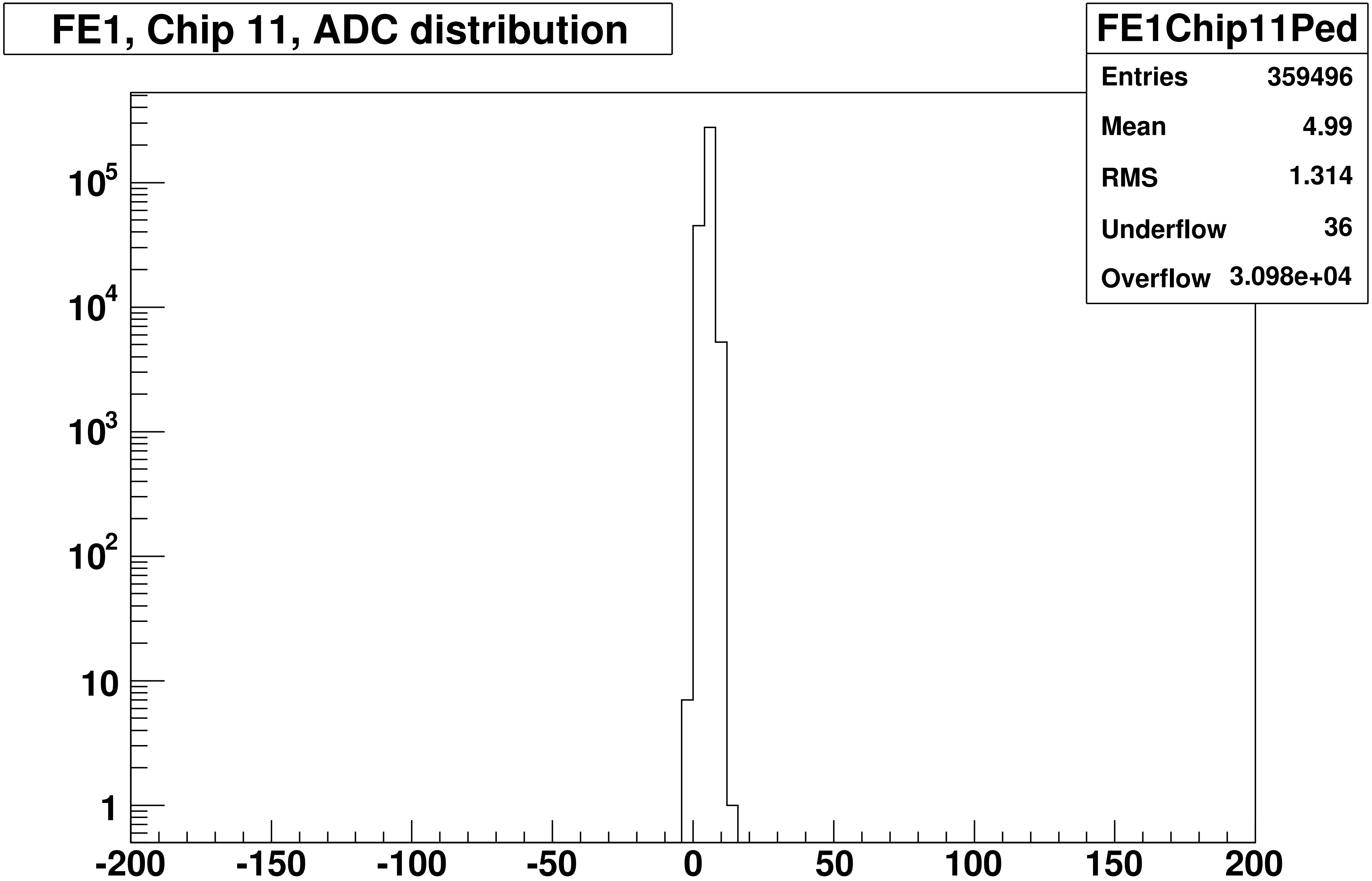
20000
25000


FE1, Chip 11, ADC distribution
FE1Chip11Ped
Entries 359496
Mean 4.99
RMS 1.314
Underflow 36
Overflow 3.098e+04
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10^3
10^2
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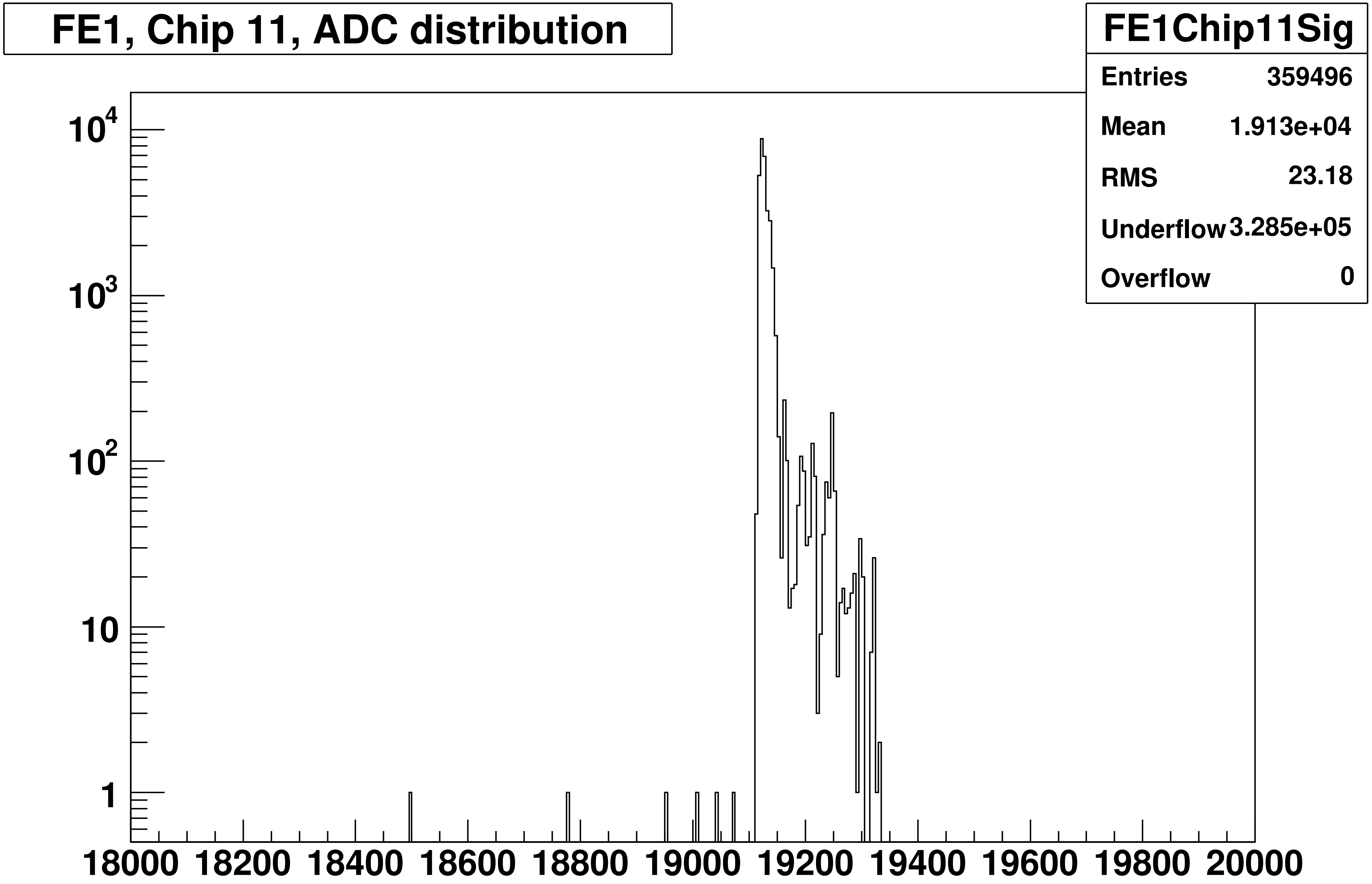
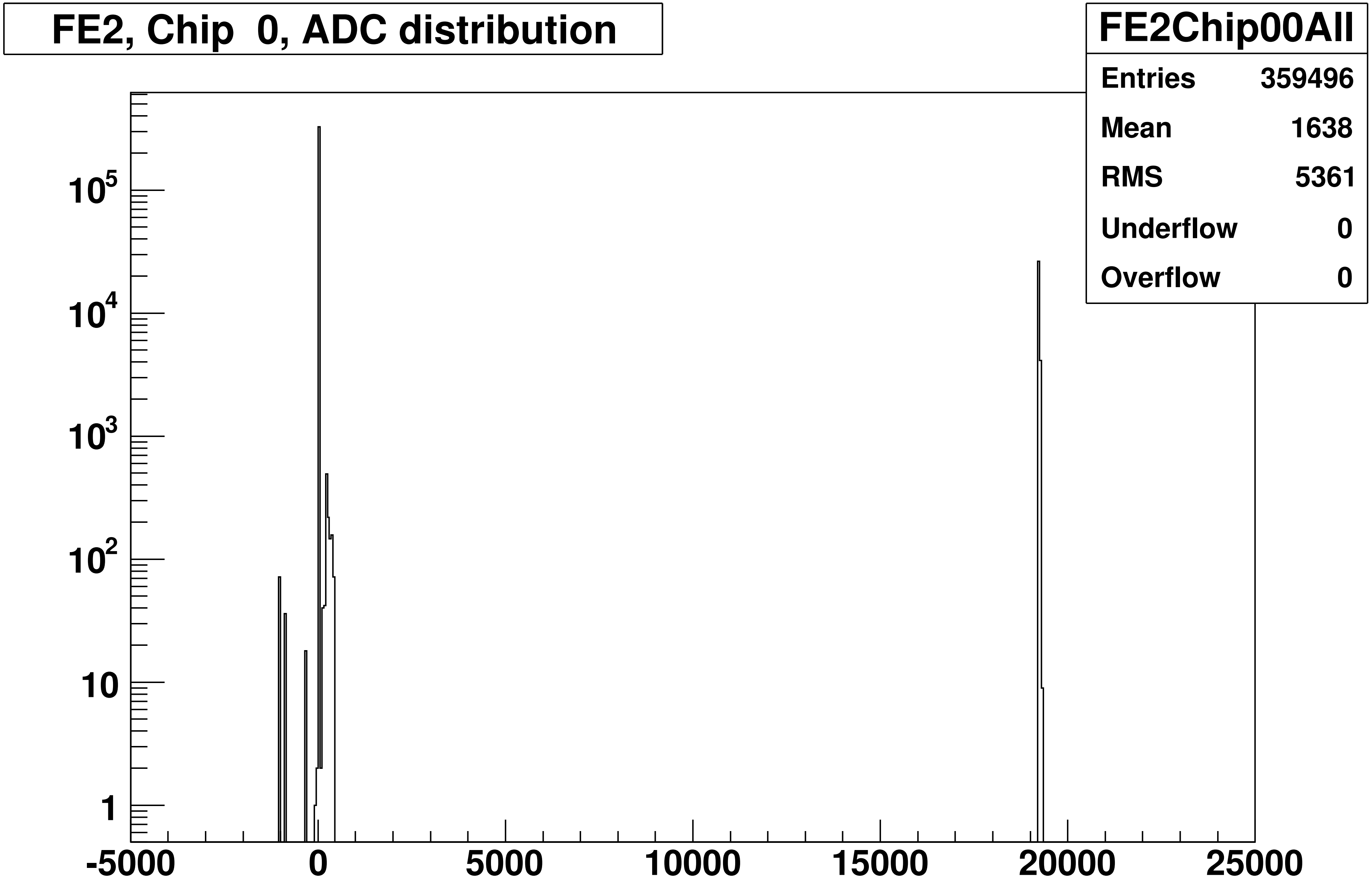
150
200


FE1, Chip 11, ADC distribution
FE1Chip11Sig
Entries 359496
Mean 1.913e+04
RMS 23.18
Underflow 3.285e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE2, Chip 0, ADC distribution
FE2Chip00All
Entries 359496
Mean 1638
RMS 5361
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
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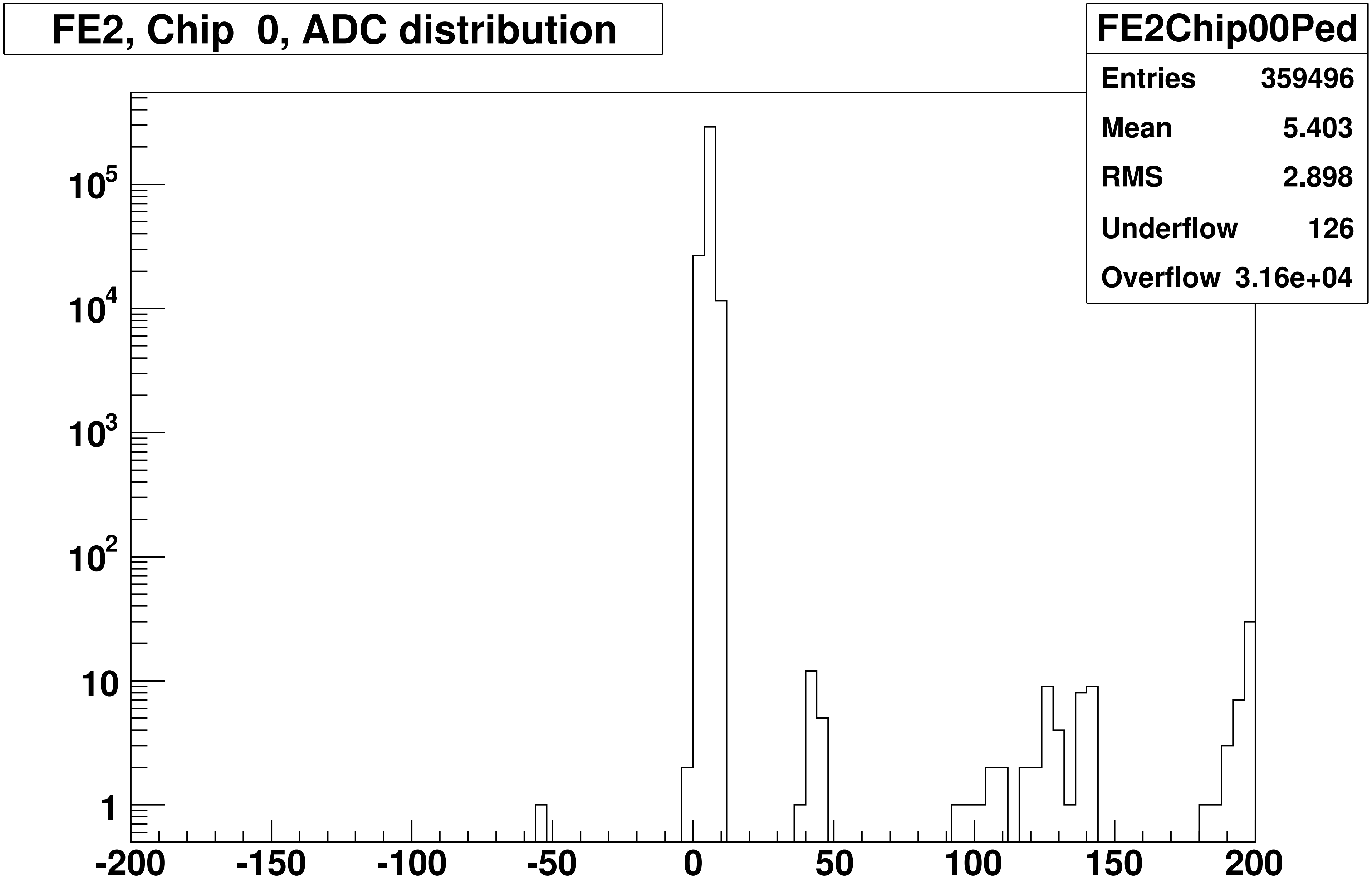
-5000
0
5000
10000
15000
20000
25000


FE2, Chip 0, ADC distribution
FE2Chip00Ped
Entries 359496
Mean 5.403
RMS 2.898
Underflow 126
Overflow 3.16e+04
10^5
10^4
10^3
10^2
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-100
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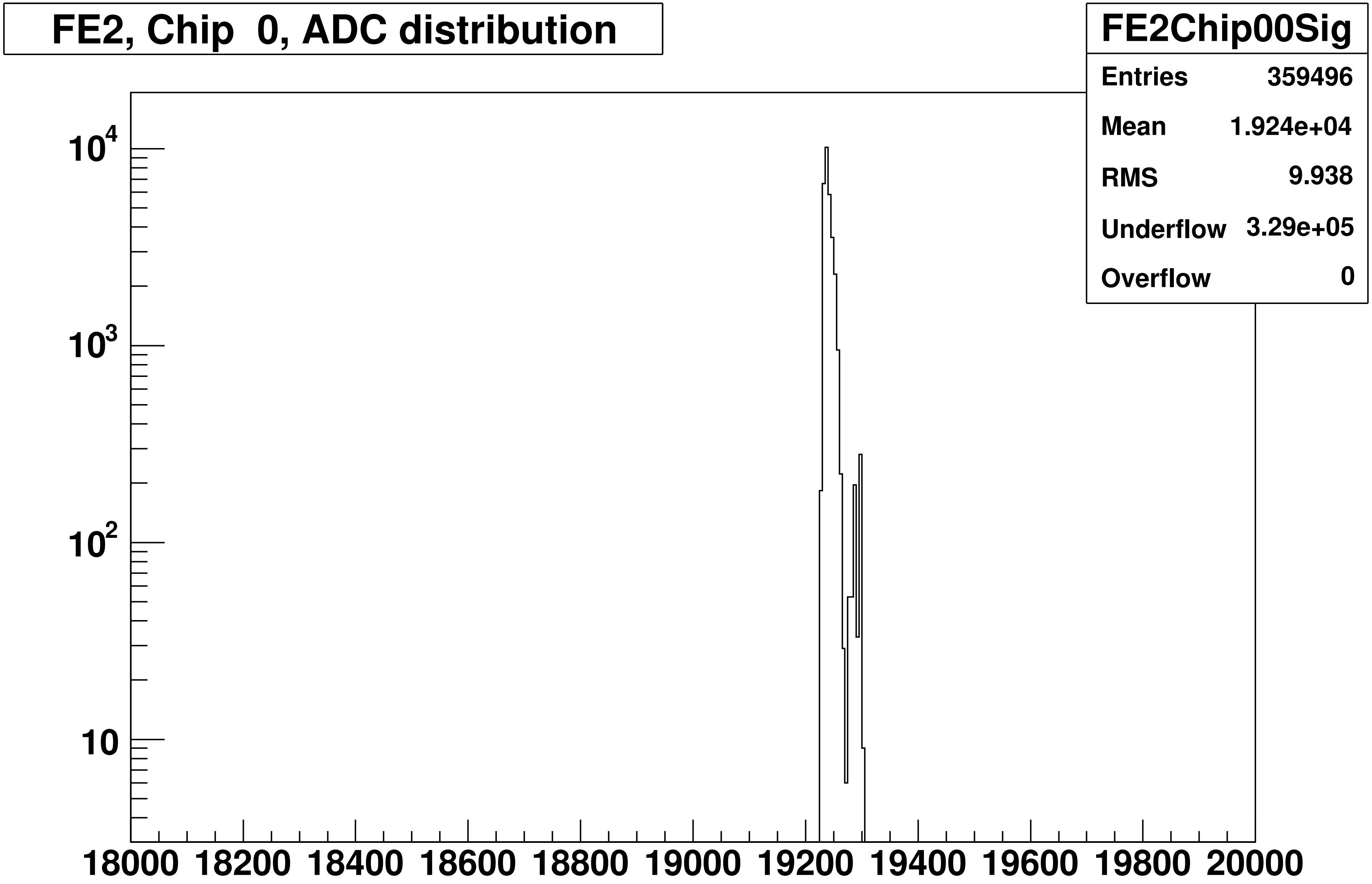
100
150
200



FE2, Chip 0, ADC distribution
FE2Chip00Sig
Entries 359496
Mean 1.924e+04
RMS 9.938
Underflow 3.29e+05
Overflow 0
10^4
10^3
10^2
10
18000
18200
18400
18600
18800
19000
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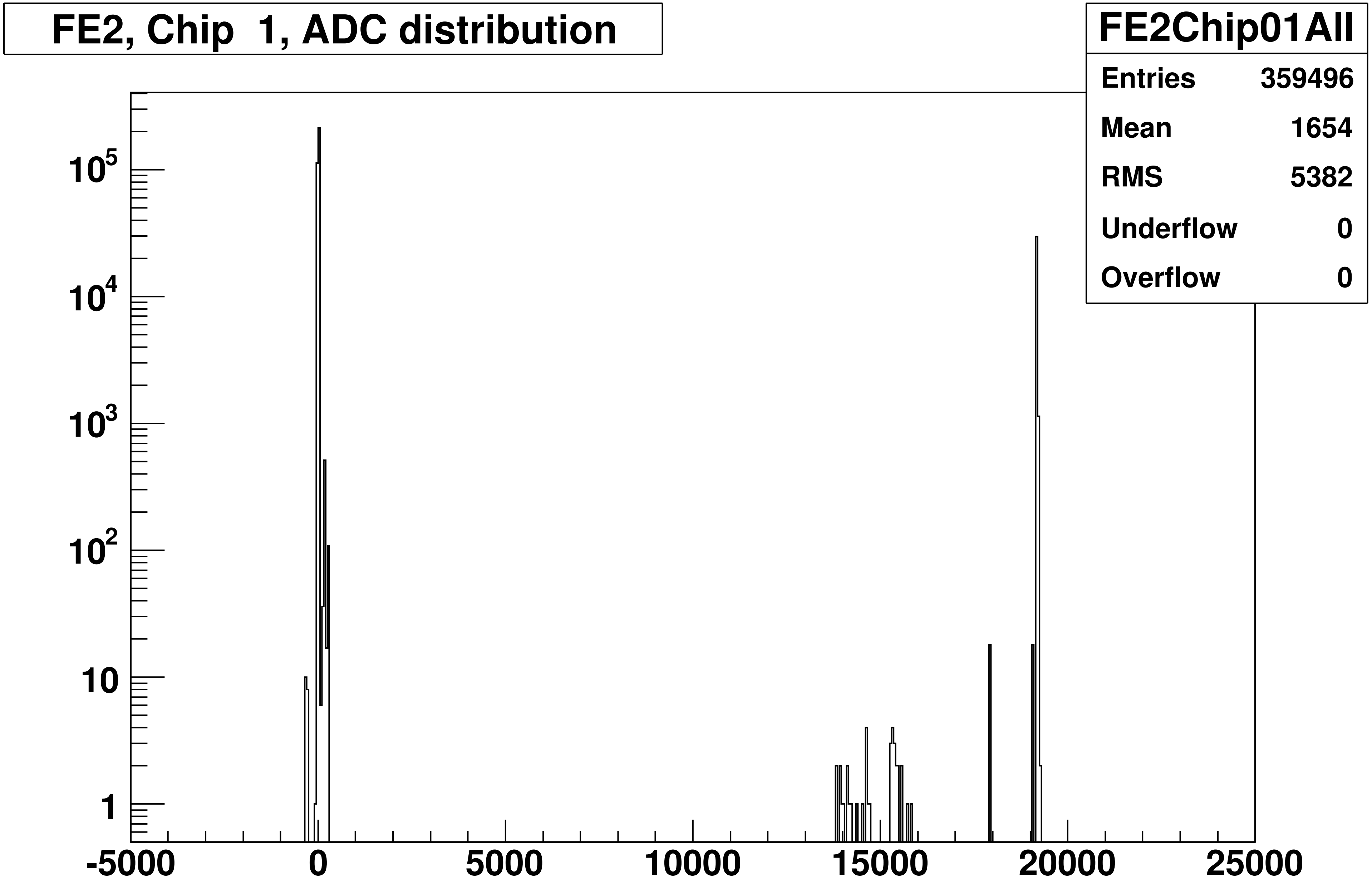
19400
19600
19800
20000


FE2, Chip 1, ADC distribution
FE2Chip01All
Entries 359496
Mean 1654
RMS 5382
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
1
-5000
0
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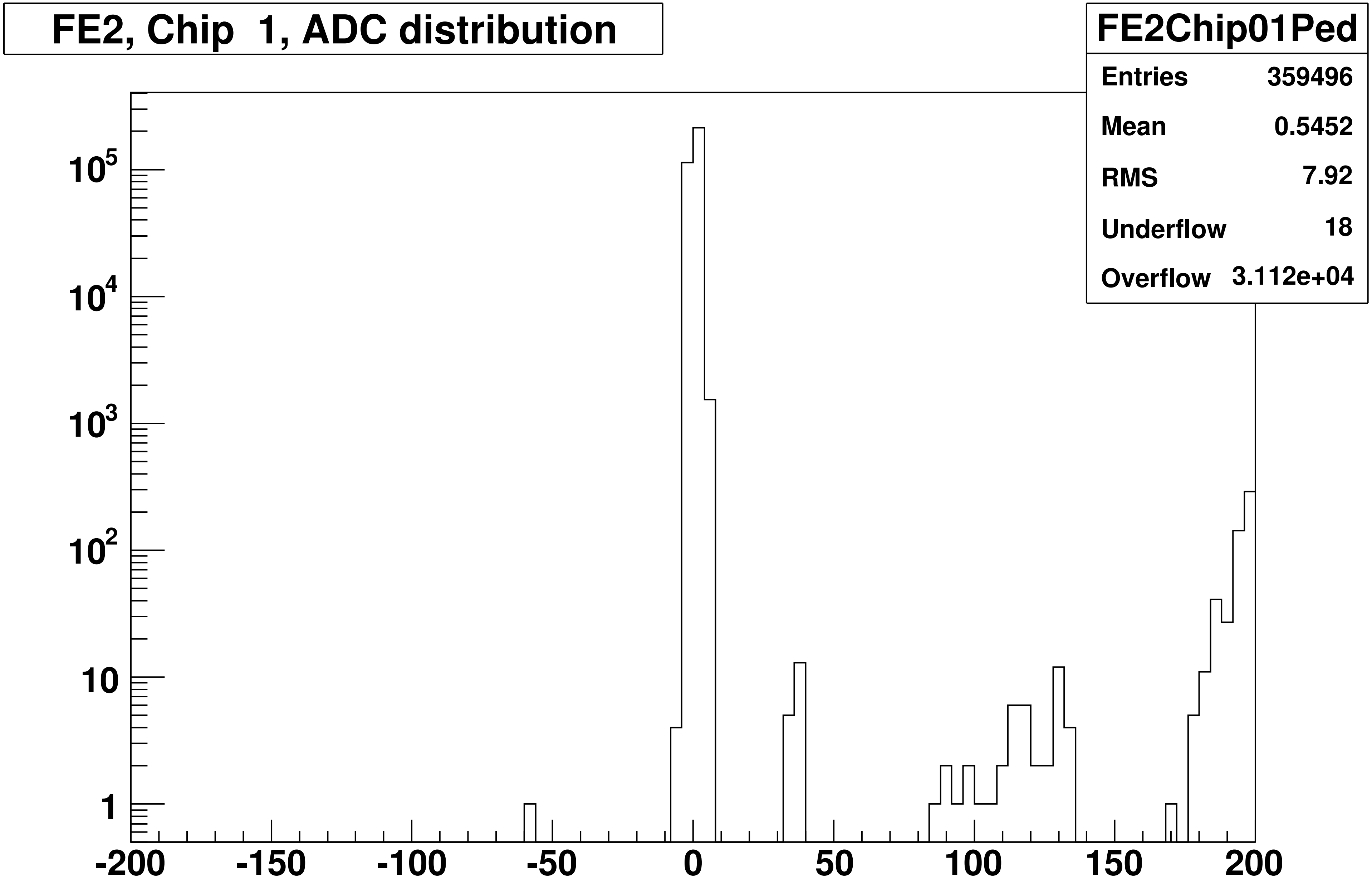
20000
25000


FE2, Chip 1, ADC distribution
FE2Chip01Ped
Entries 359496
Mean 0.5452
RMS 7.92
Underflow 18
Overflow 3.112e+04
10^5
10^4
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10^2
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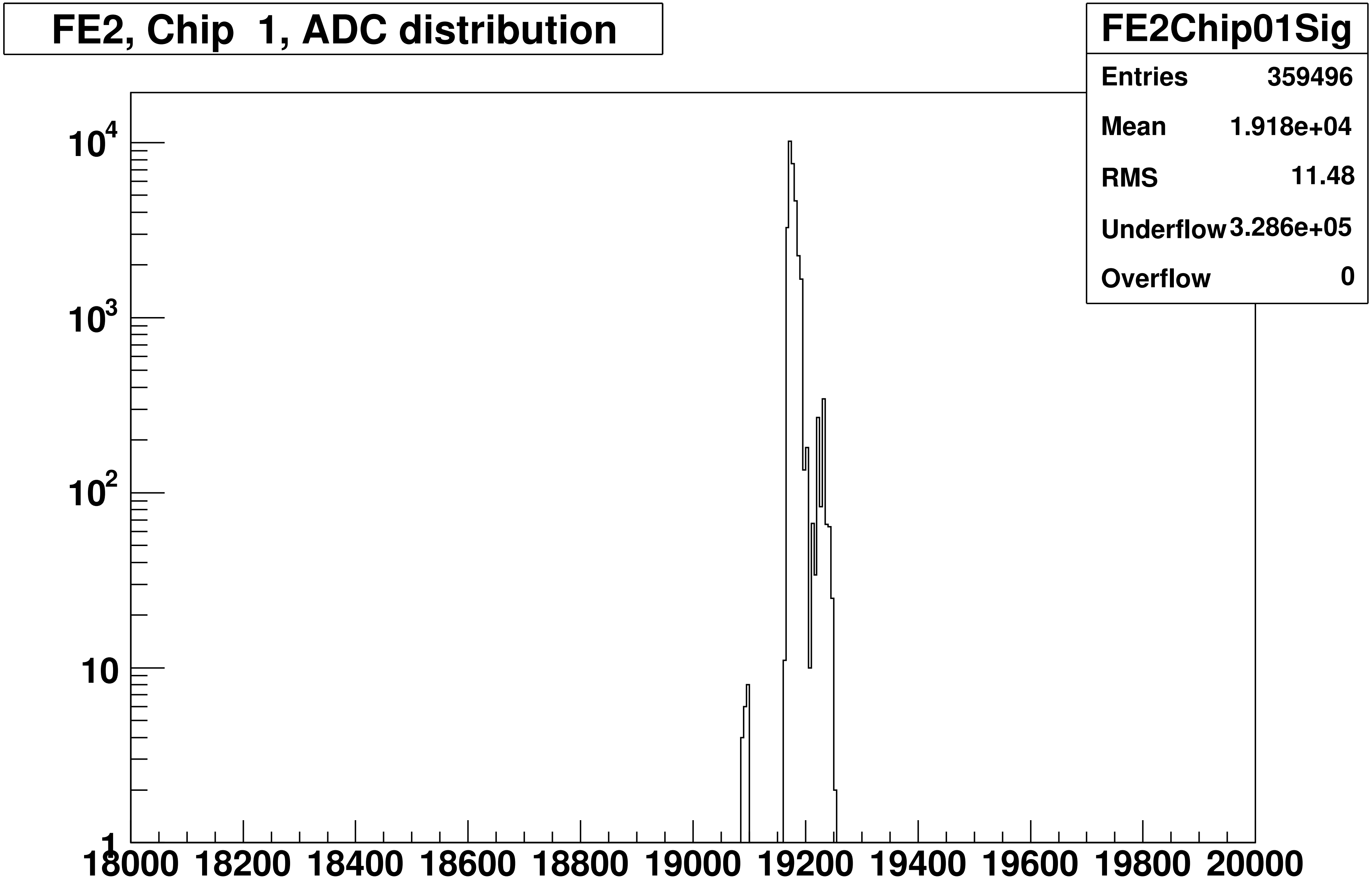
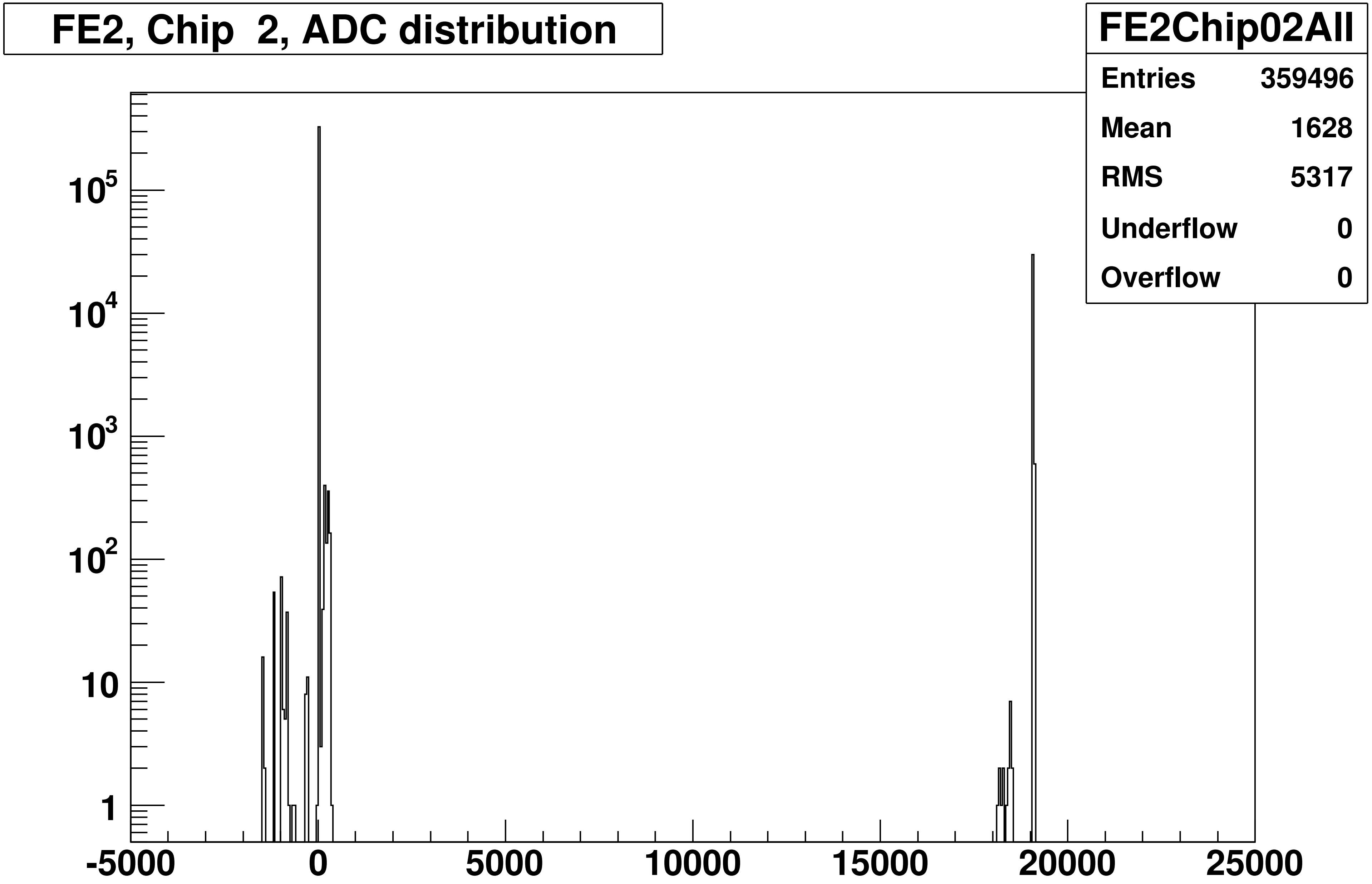
150
200


FE2, Chip 1, ADC distribution
FE2Chip01Sig
Entries 359496
Mean 1.918e+04
RMS 11.48
Underflow 3.286e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE2, Chip 2, ADC distribution
FE2Chip02All
Entries 359496
Mean 1628
RMS 5317
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
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-5000
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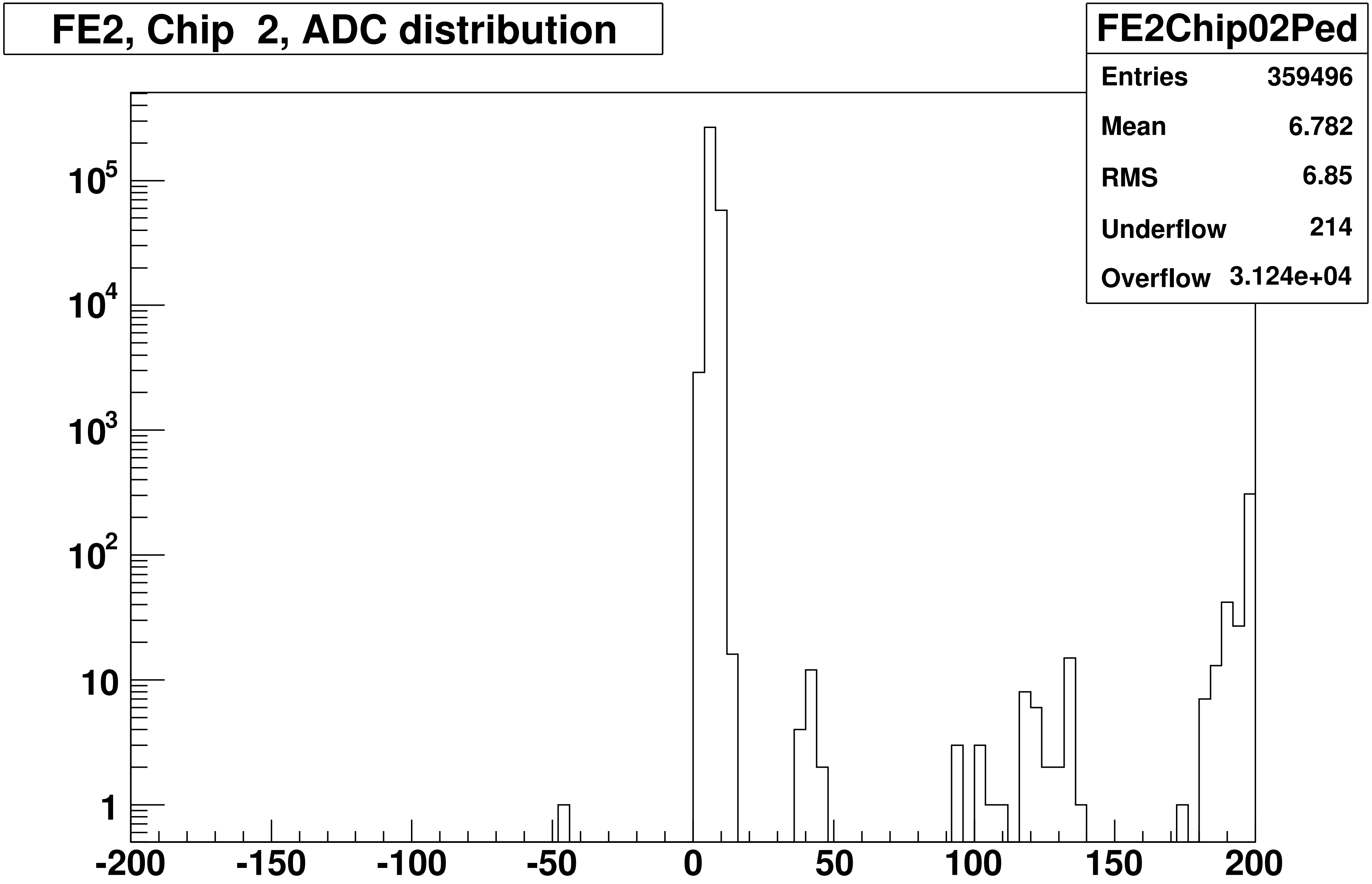
25000



FE2, Chip 2, ADC distribution
FE2Chip02Ped
Entries 359496
Mean 6.782
RMS 6.85
Underflow 214
Overflow 3.124e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
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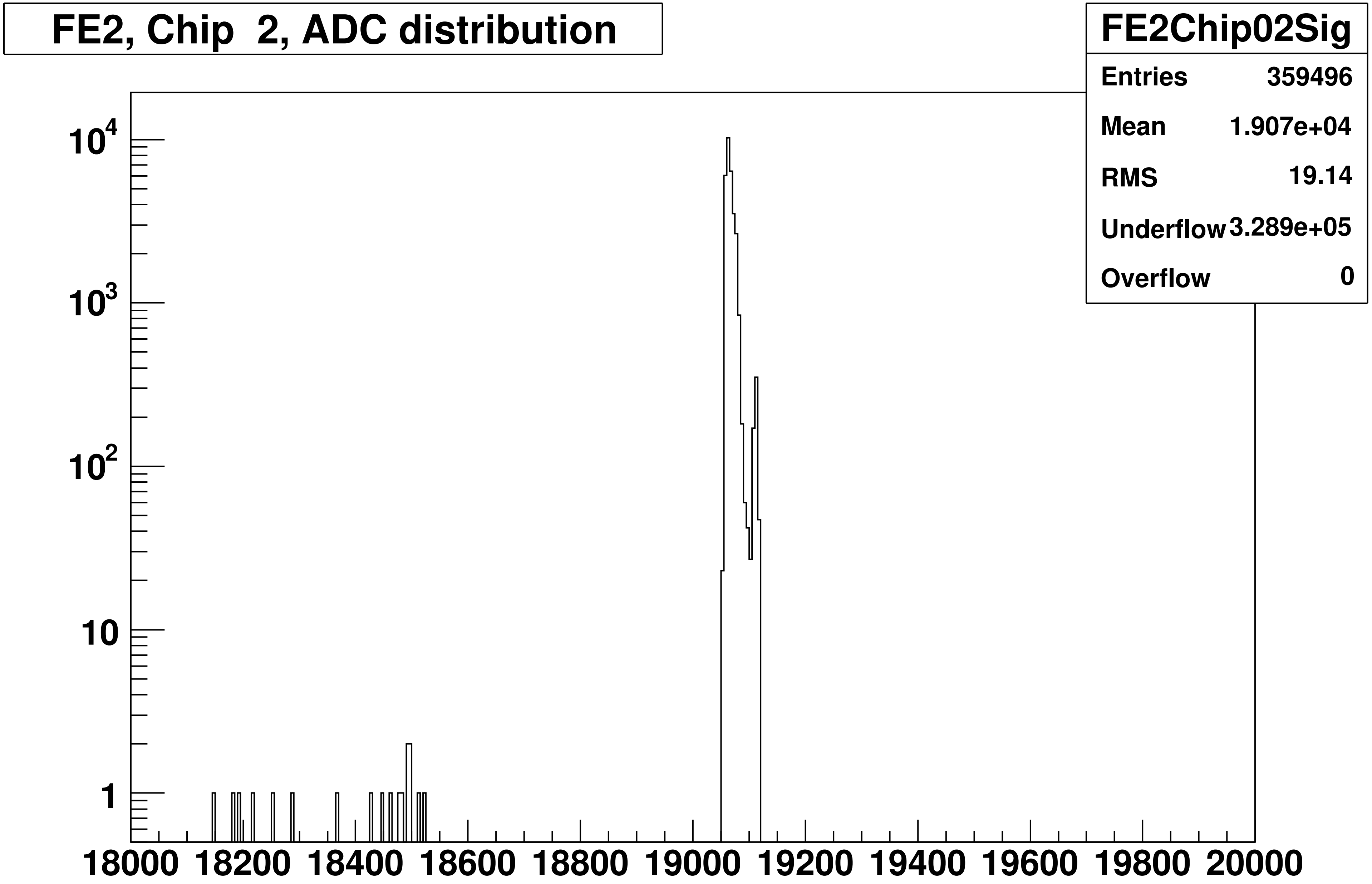
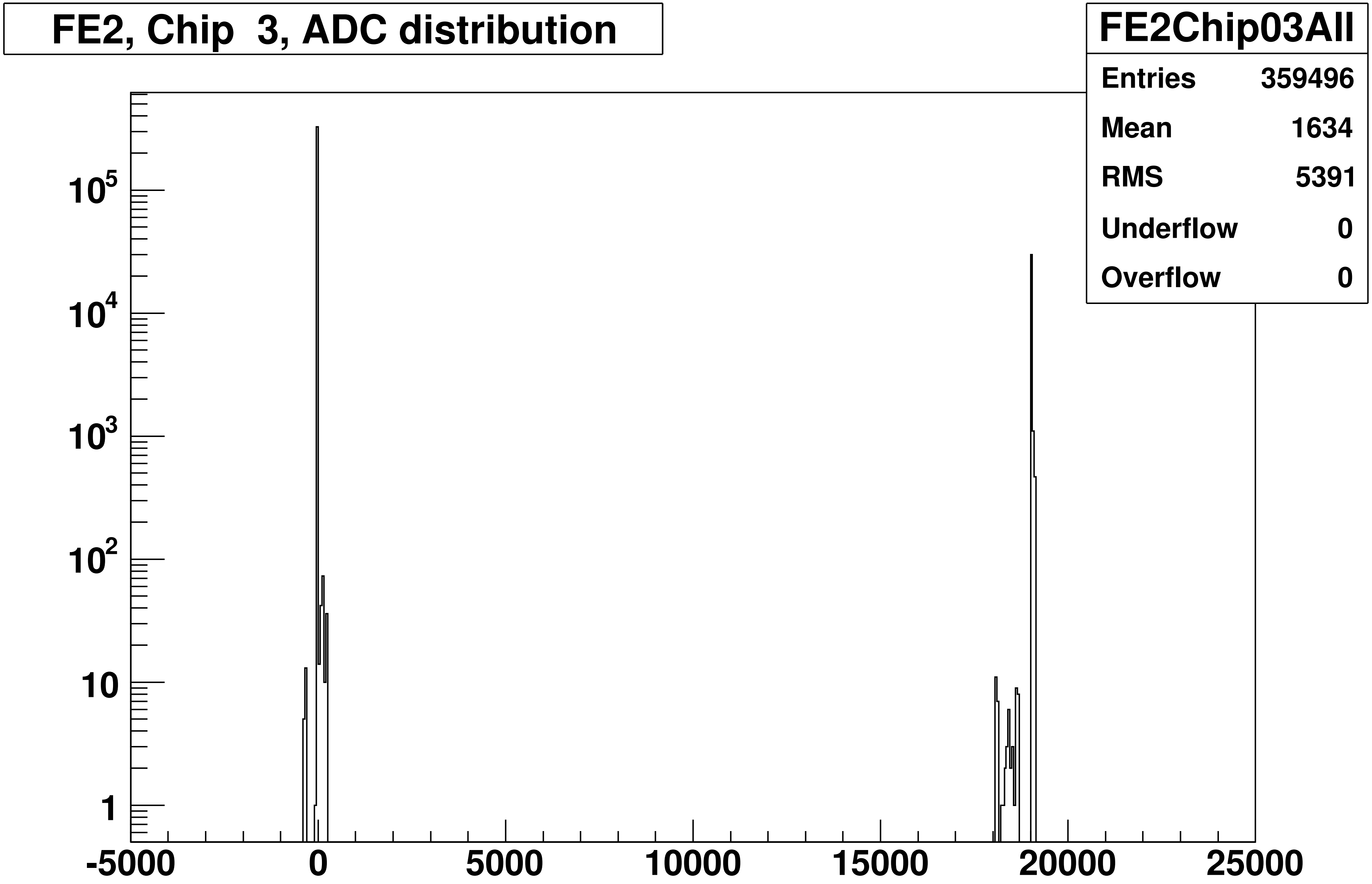


FE2, Chip 2, ADC distribution
FE2Chip02Sig
Entries 359496
Mean 1.907e+04
RMS 19.14
Underflow 3.289e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000


FE2, Chip 3, ADC distribution
FE2Chip03All
Entries 359496
Mean 1634
RMS 5391
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
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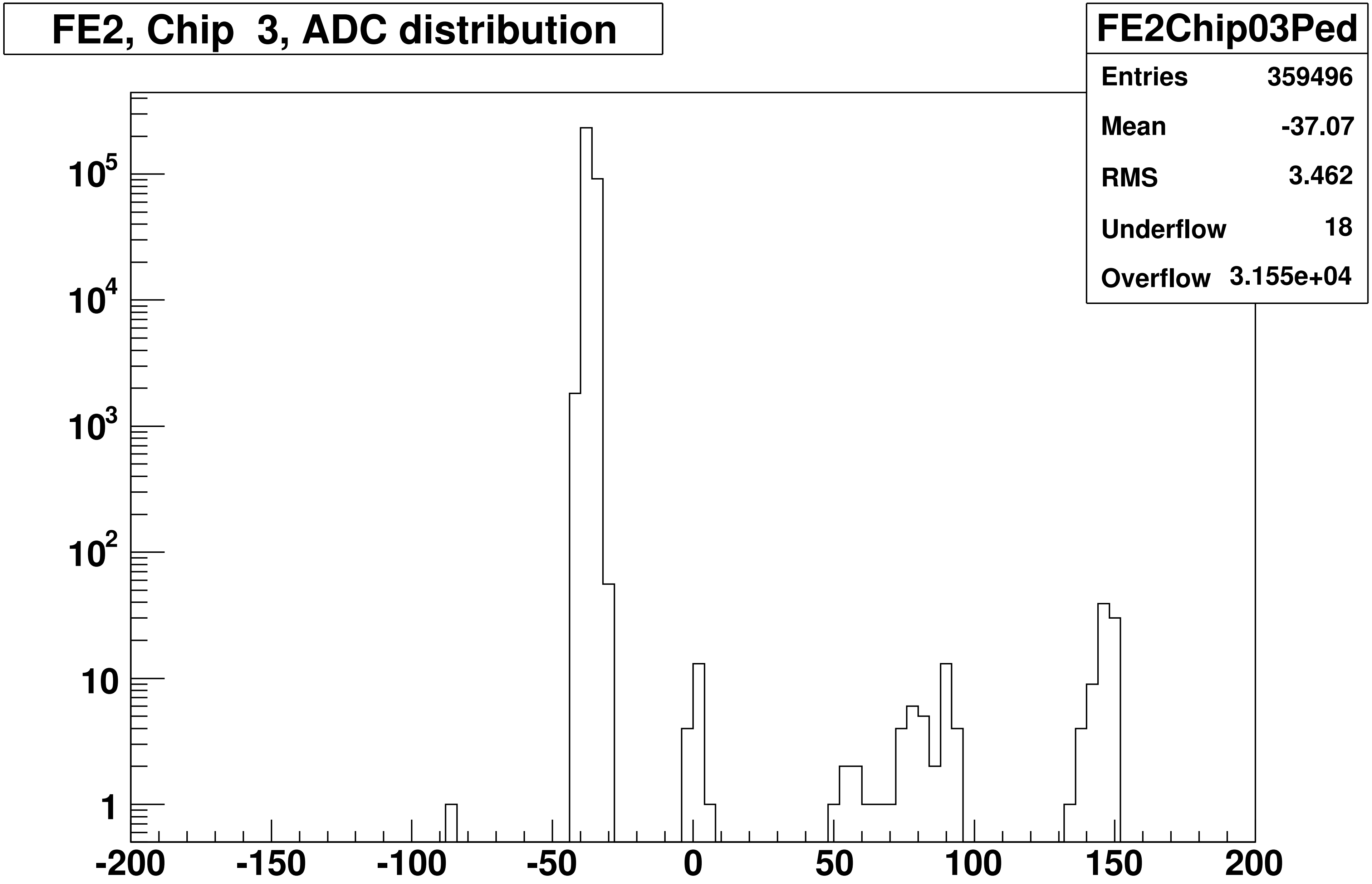
10000
15000
20000
25000



FE2, Chip 3, ADC distribution
FE2Chip03Ped
Entries 359496
Mean -37.07
RMS 3.462
Underflow 18
Overflow 3.155e+04
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10^4
10^3
10^2
10
1
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-100
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0
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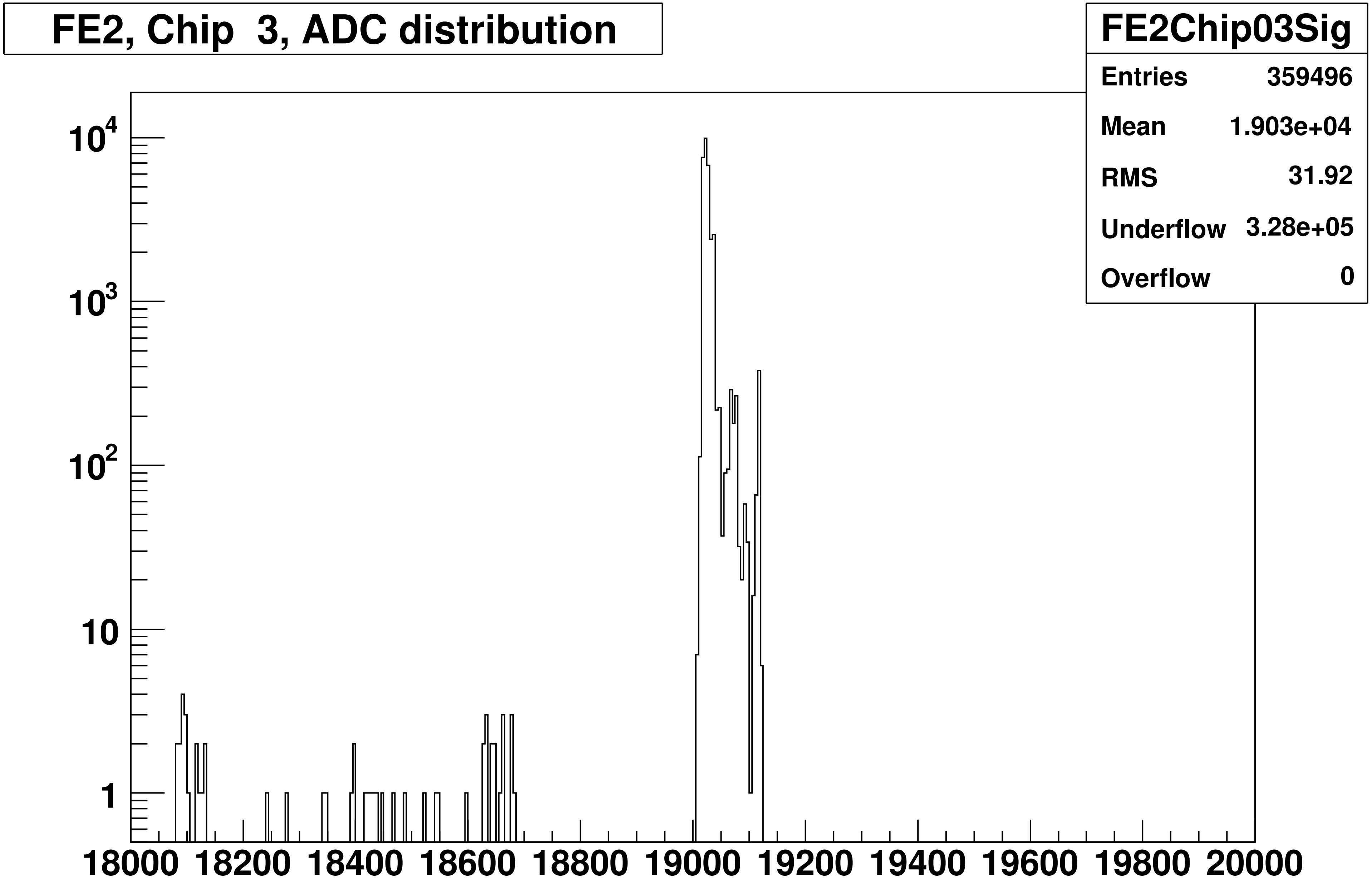
100
150
200


FE2, Chip 3, ADC distribution
FE2Chip03Sig
Entries 359496
Mean 1.903e+04
RMS 31.92
Underflow 3.28e+05
Overflow 0
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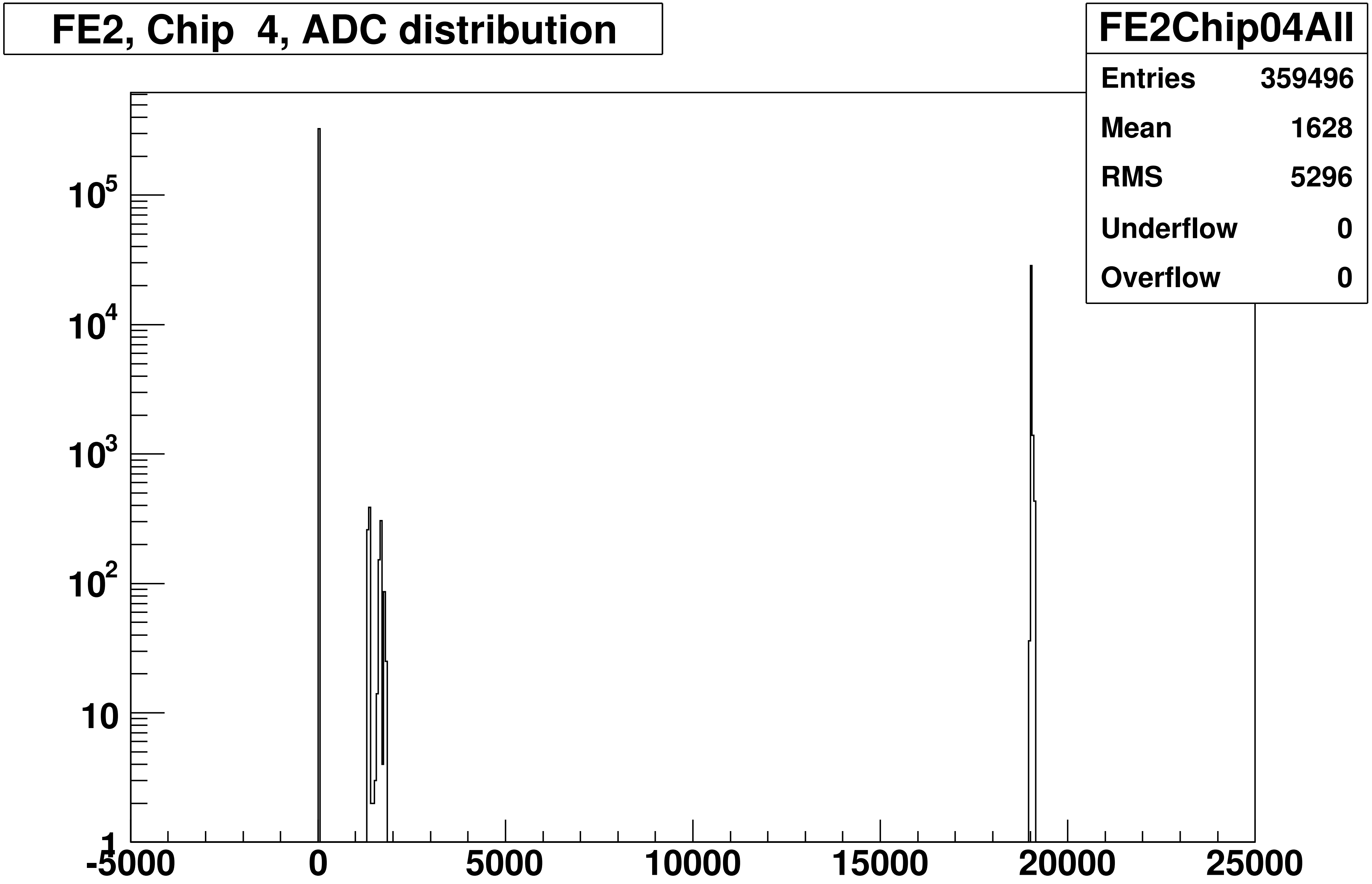
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE2, Chip 4, ADC distribution
FE2Chip04All
Entries 359496
Mean 1628
RMS 5296
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
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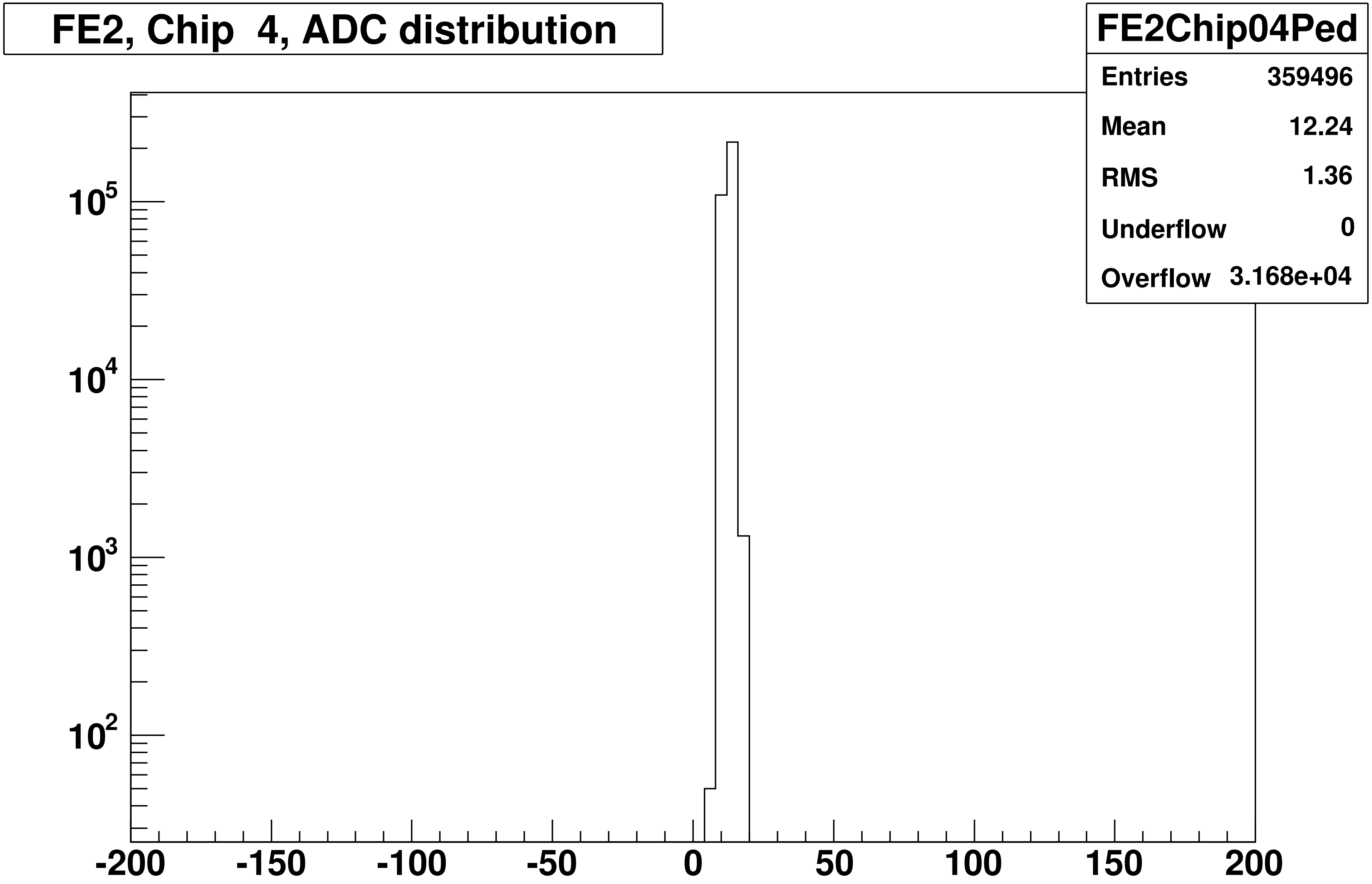
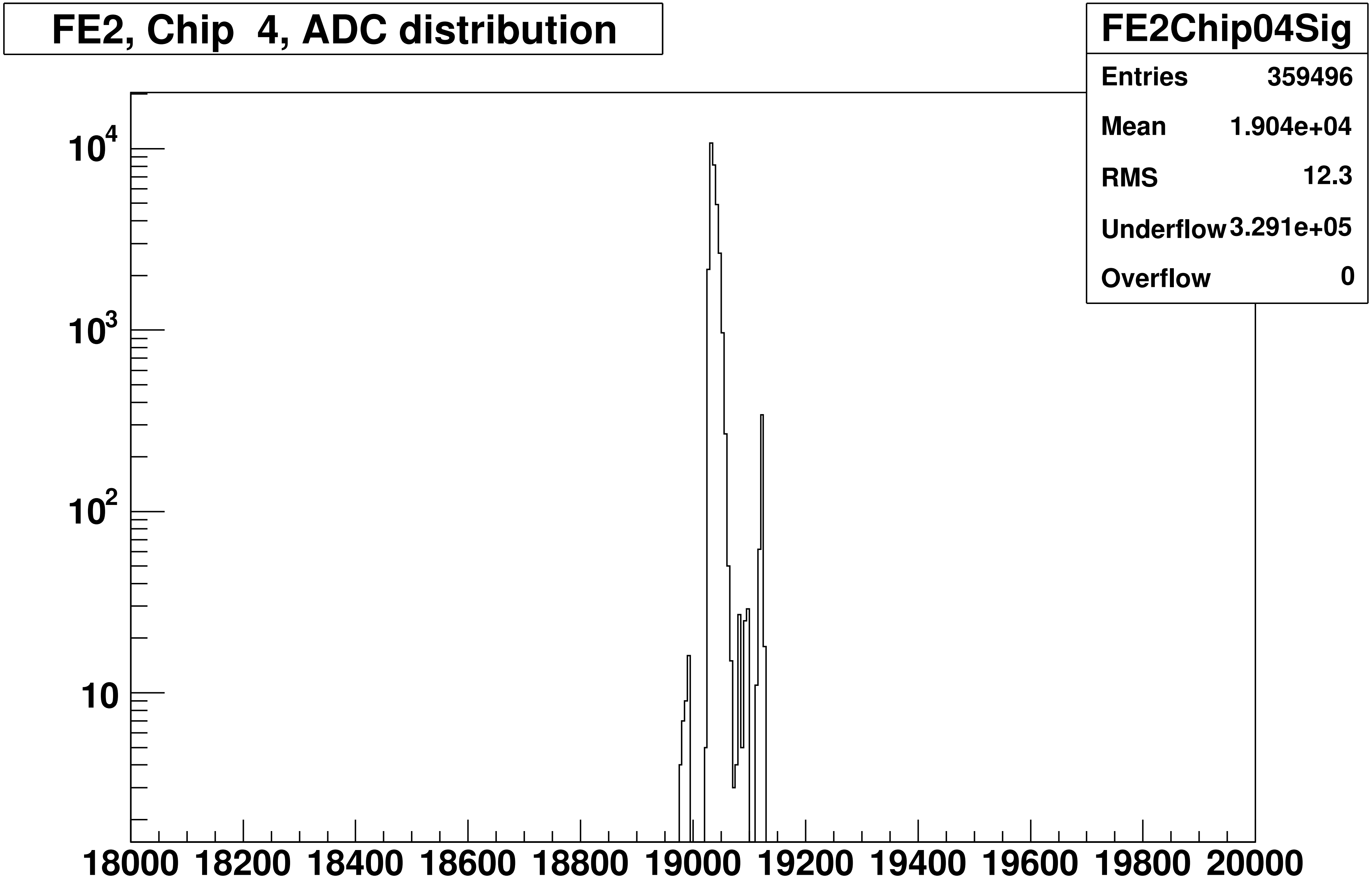
10000
15000
20000
25000


FE2, Chip 4, ADC distribution
FE2Chip04Ped
Entries 359496
Mean 12.24
RMS 1.36
Underflow 0
Overflow 3.168e+04
10^5
10^4
10^3
10^2
-200 -150 -100 -50 0 50 100 150 200


FE2, Chip 4, ADC distribution
FE2Chip04Sig
Entries 359496
Mean 1.904e+04
RMS 12.3
Underflow 3.291e+05
Overflow 0
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10^3
10^2
10
18000
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18400
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19000
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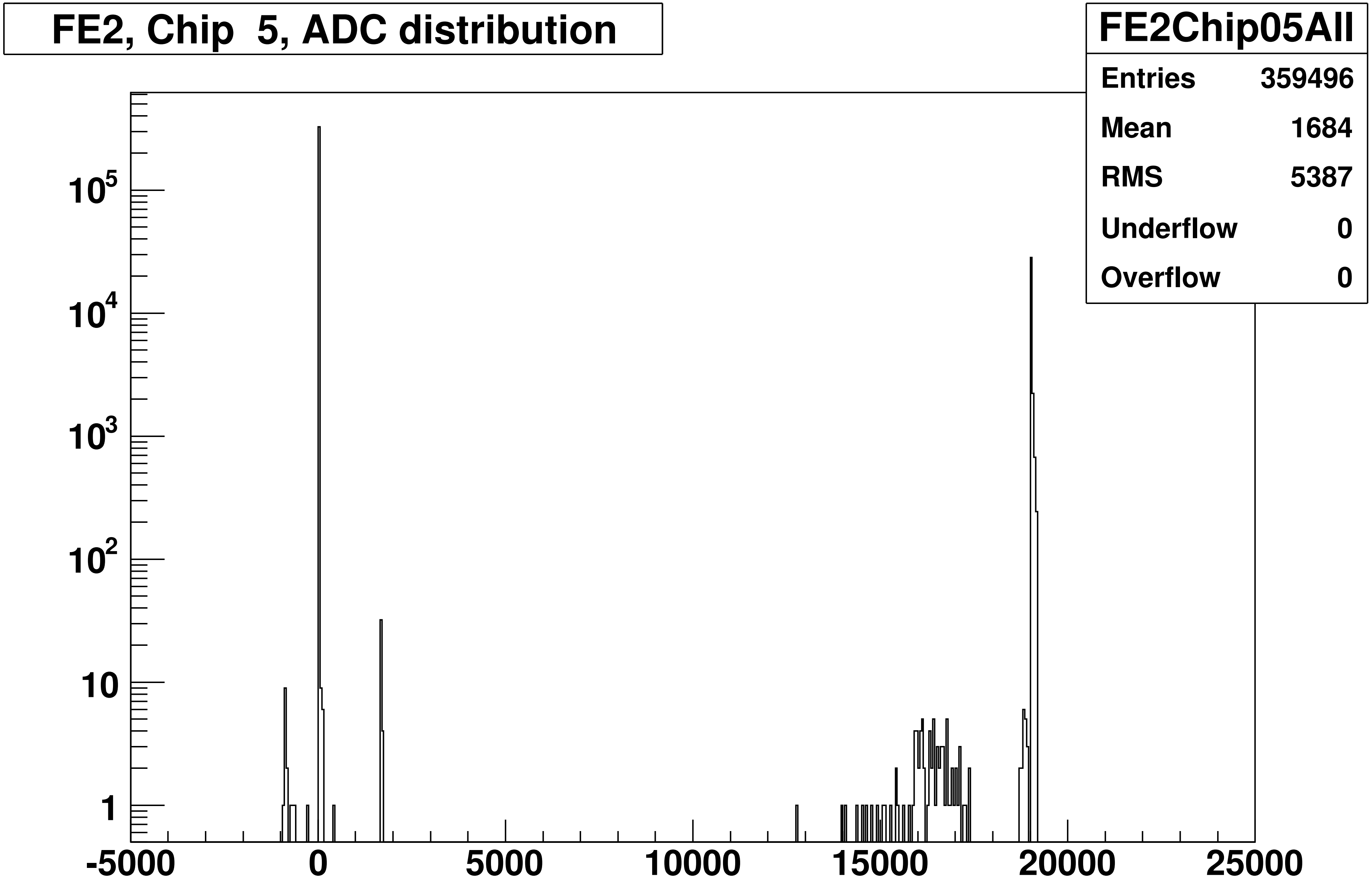
19400
19600
19800
20000


FE2, Chip 5, ADC distribution
FE2Chip05All
Entries 359496
Mean 1684
RMS 5387
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
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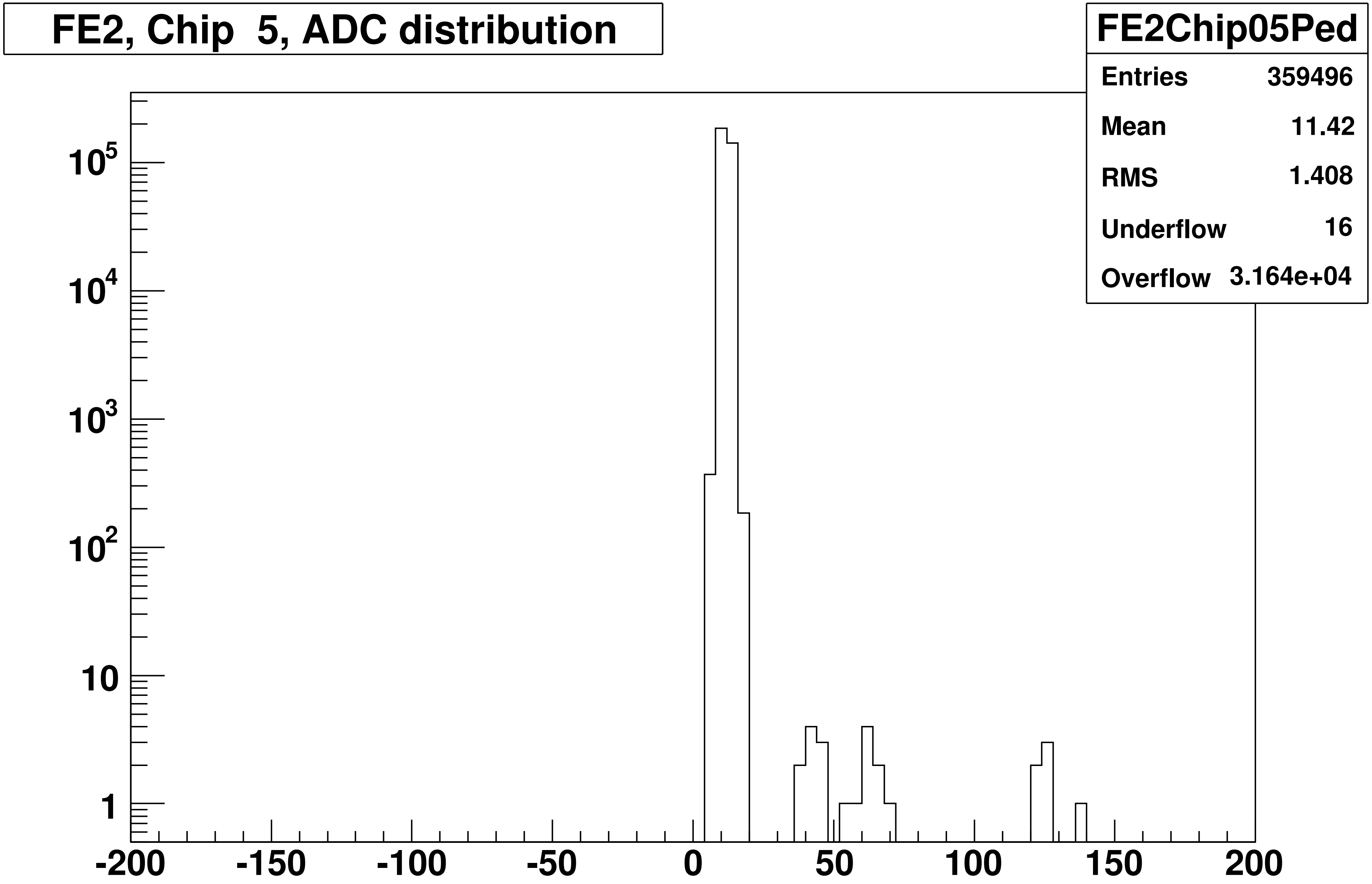
10000
15000
20000
25000


FE2, Chip 5, ADC distribution
FE2Chip05Ped
Entries 359496
Mean 11.42
RMS 1.408
Underflow 16
Overflow 3.164e+04
10^5
10^4
10^3
10^2
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1
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-100
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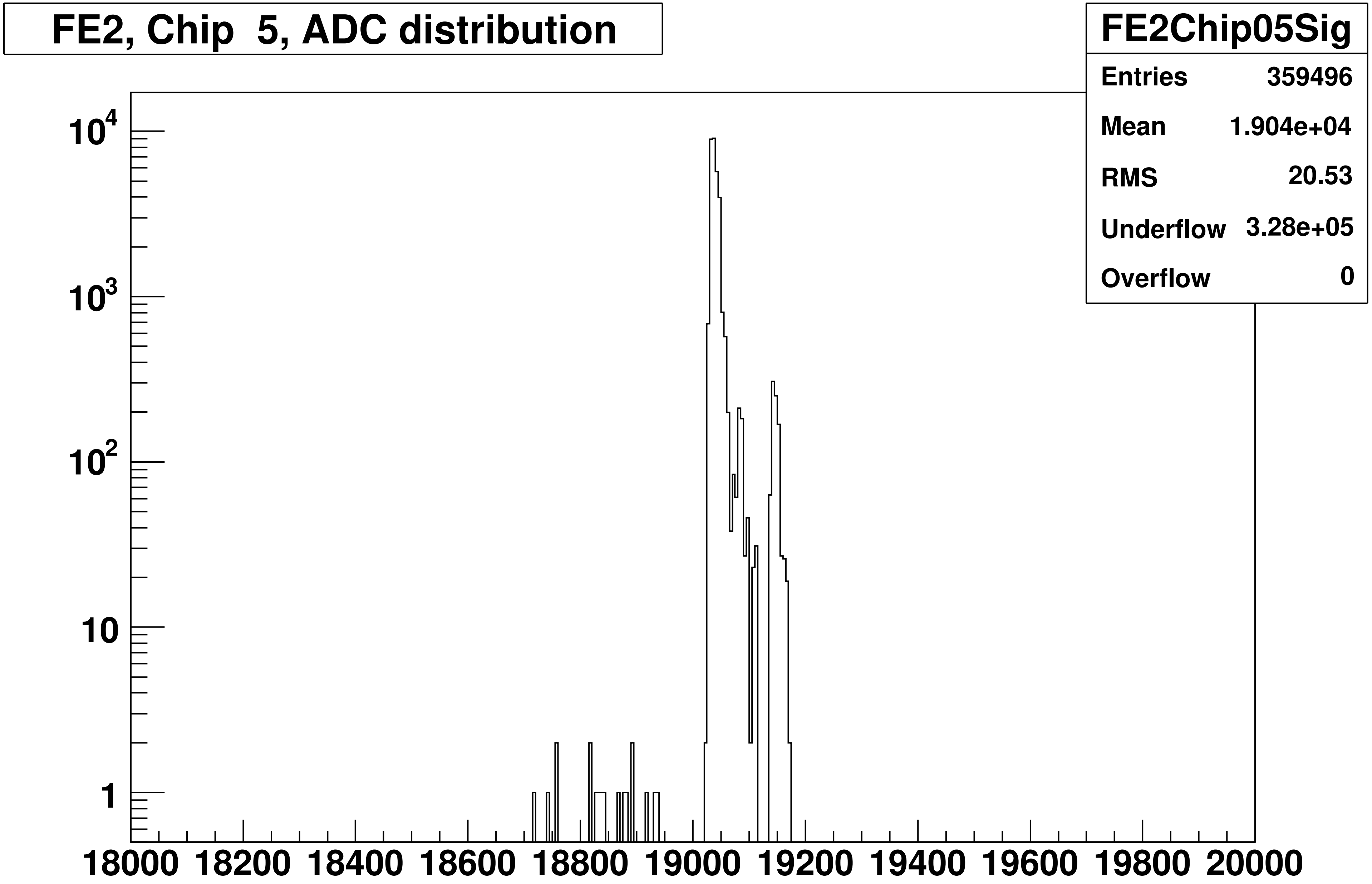
50
100
150
200


FE2, Chip 5, ADC distribution
FE2Chip05Sig
Entries 359496
Mean 1.904e+04
RMS 20.53
Underflow 3.28e+05
Overflow 0
10^4
10^3
10^2
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1
18000
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18600
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19000
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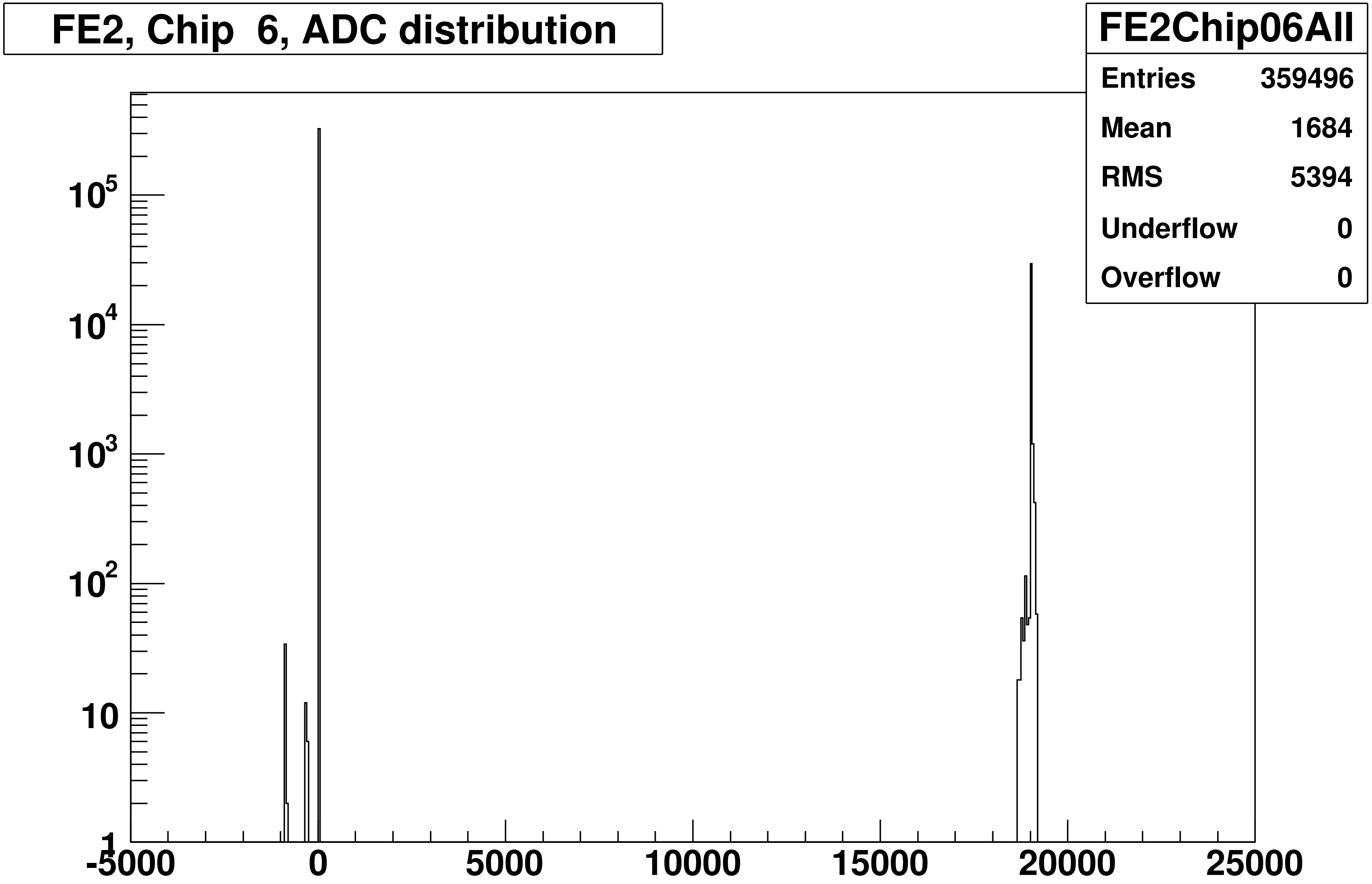
19800
20000



FE2, Chip 6, ADC distribution
FE2Chip06All
Entries 359496
Mean 1684
RMS 5394
Underflow 0
Overflow 0
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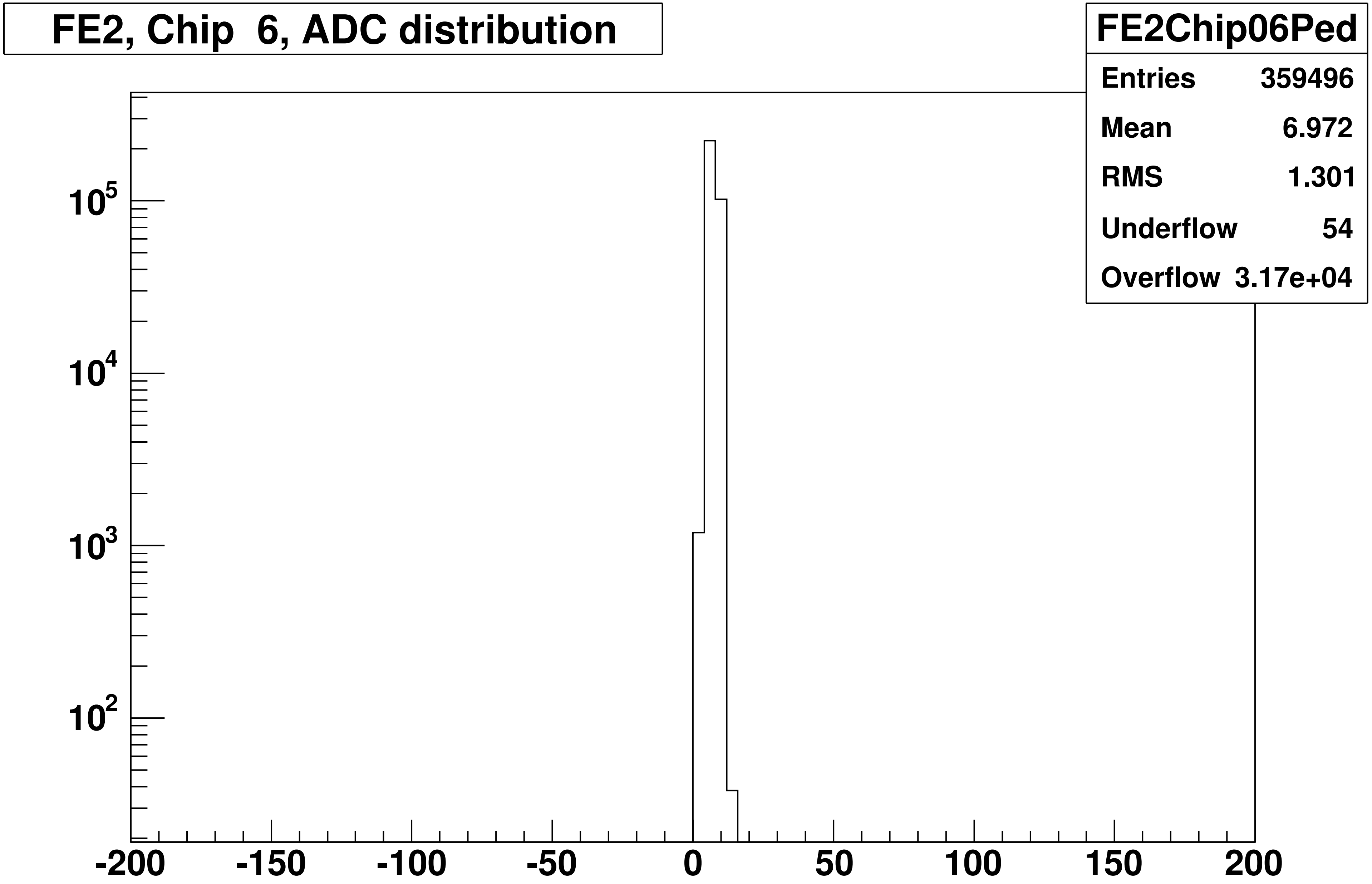
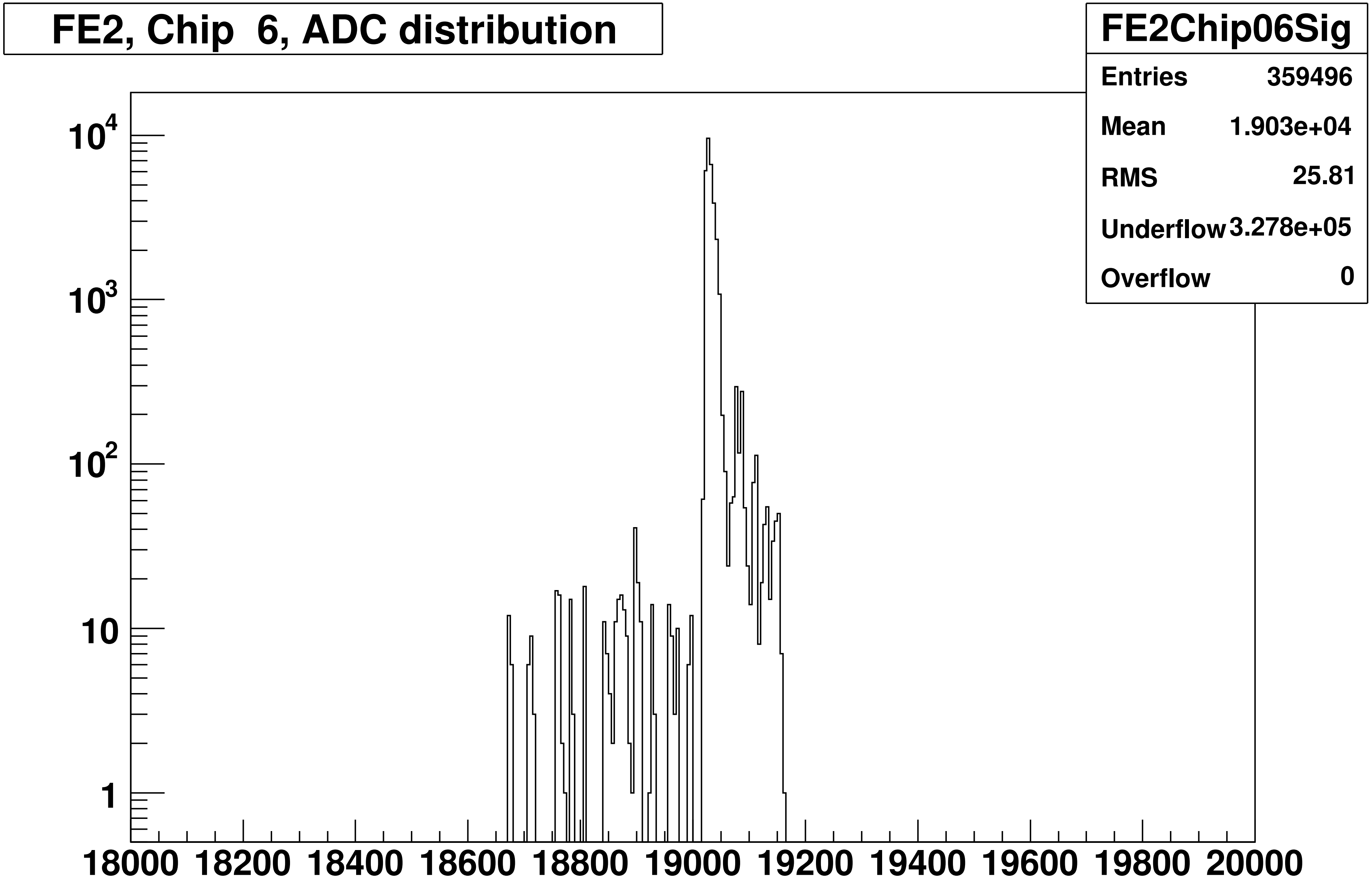
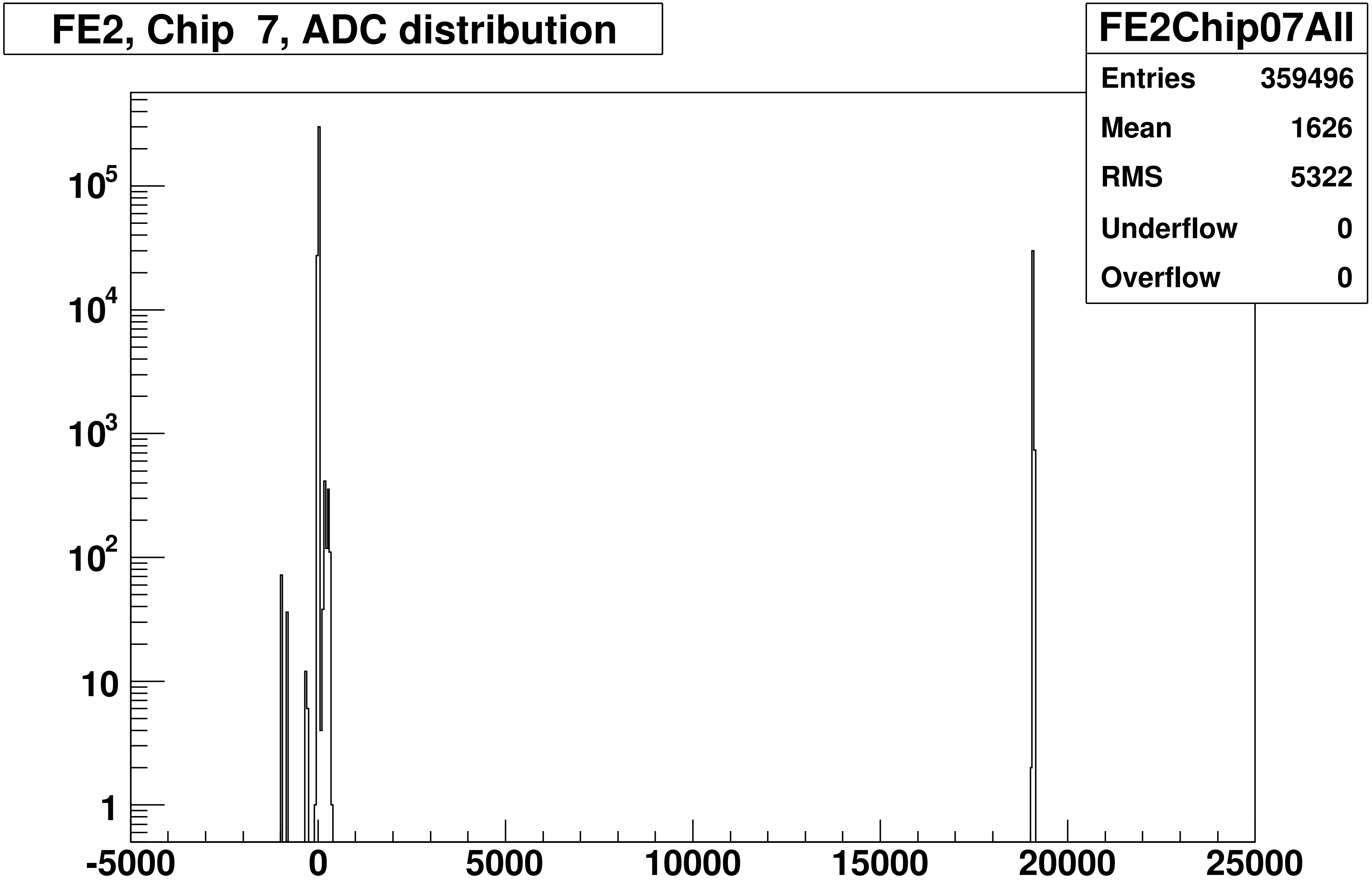
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE2, Chip 6, ADC distribution
FE2Chip06Ped
Entries 359496
Mean 6.972
RMS 1.301
Underflow 54
Overflow 3.17e+04
10^5
10^4
10^3
10^2
-200 -150 -100 -50 0 50 100 150 200


FE2, Chip 6, ADC distribution
FE2Chip06Sig
Entries 359496
Mean 1.903e+04
RMS 25.81
Underflow 3.278e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE2, Chip 7, ADC distribution
FE2Chip07All
Entries 359496
Mean 1626
RMS 5322
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
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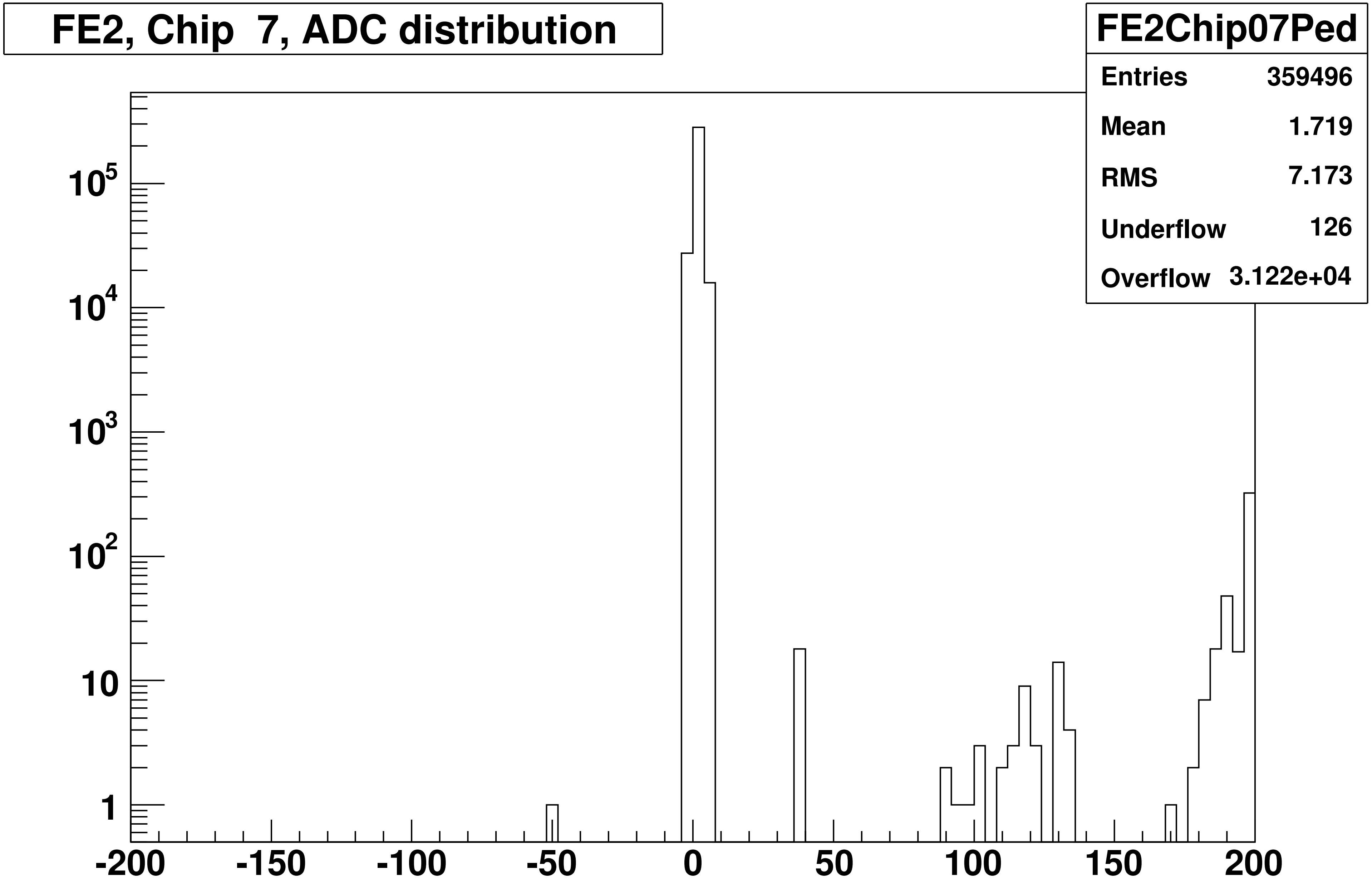
10000
15000
20000
25000


FE2, Chip 7, ADC distribution
FE2Chip07Ped
Entries 359496
Mean 1.719
RMS 7.173
Underflow 126
Overflow 3.122e+04
10^5
10^4
10^3
10^2
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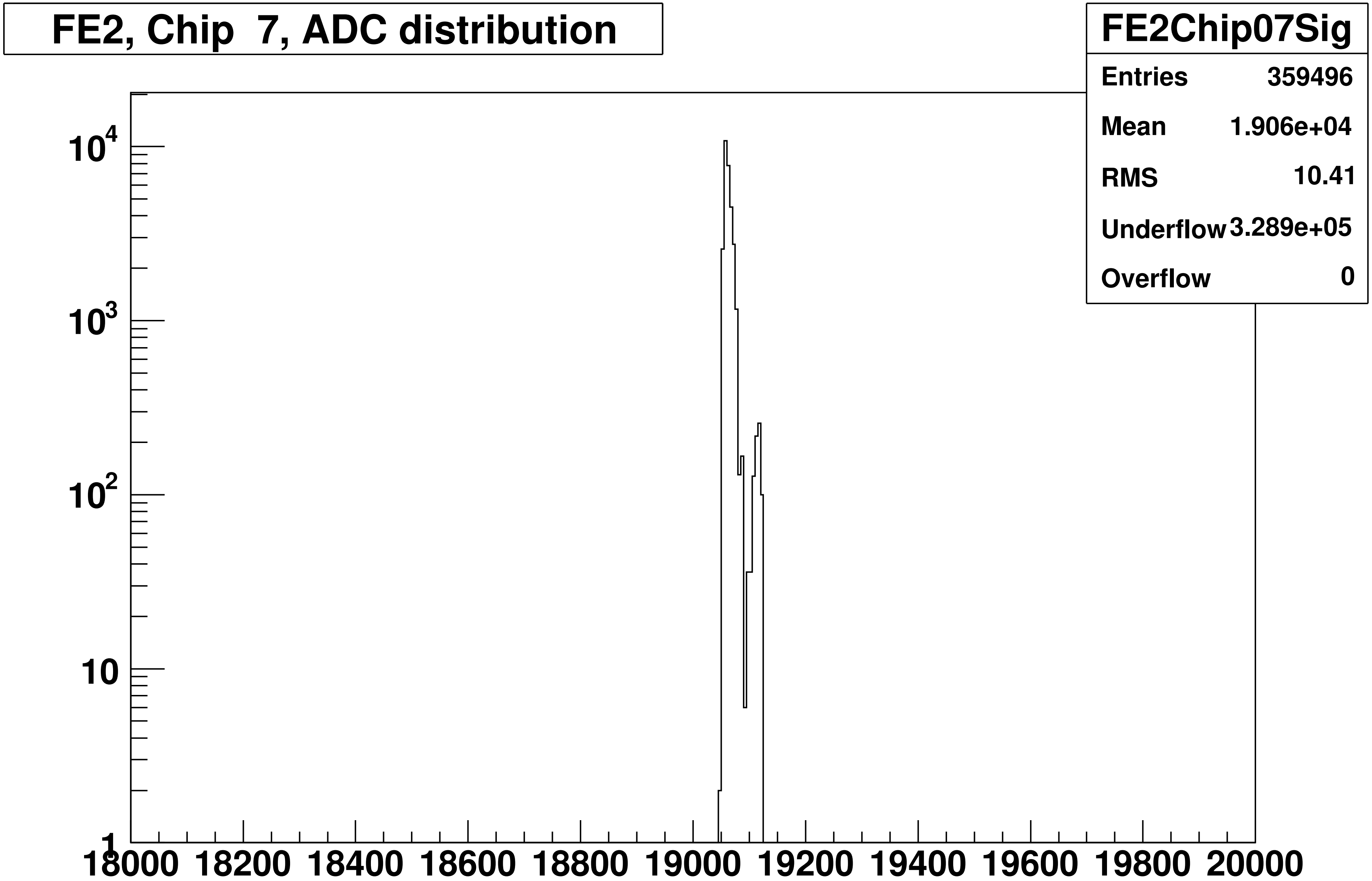
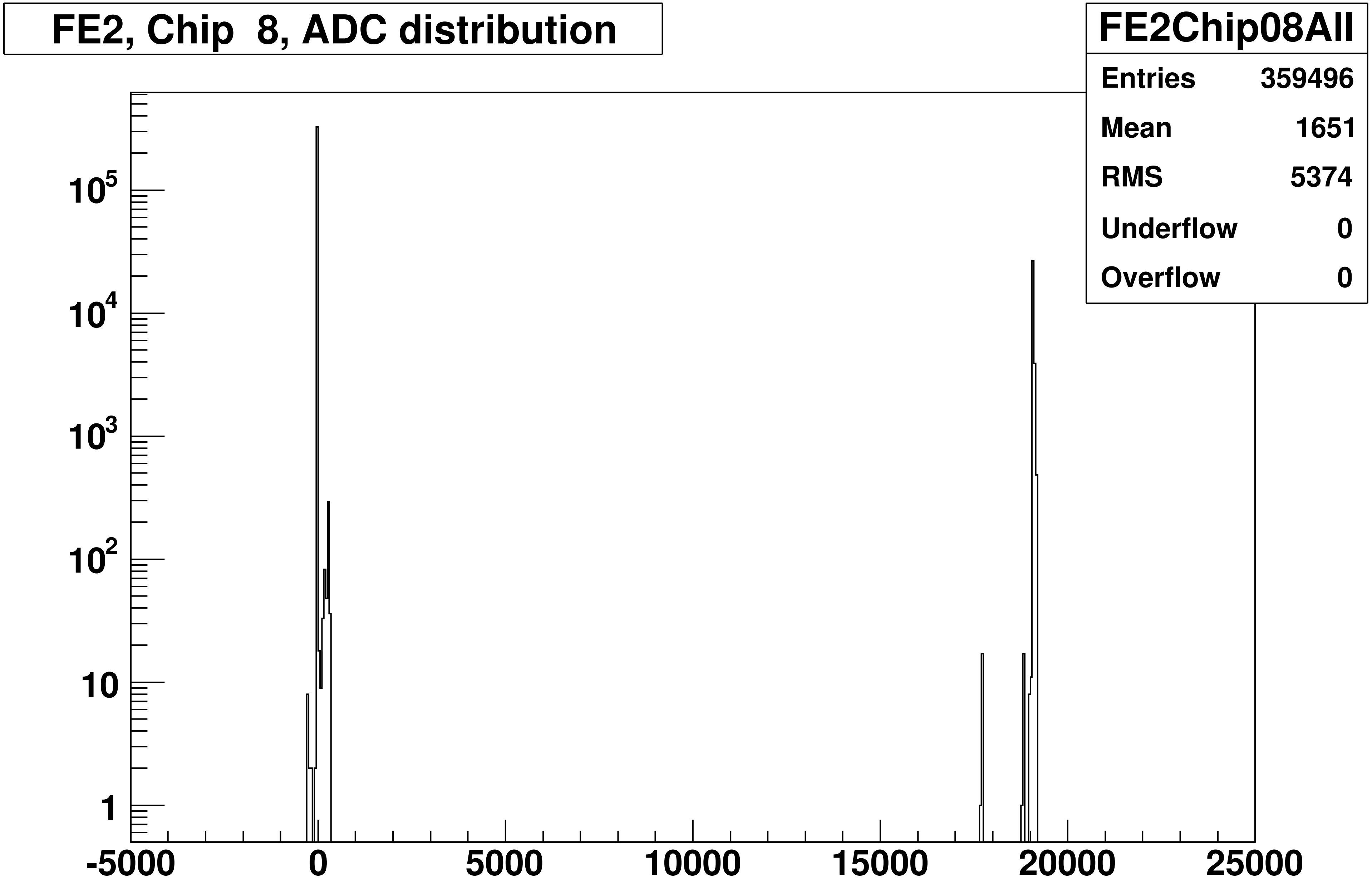
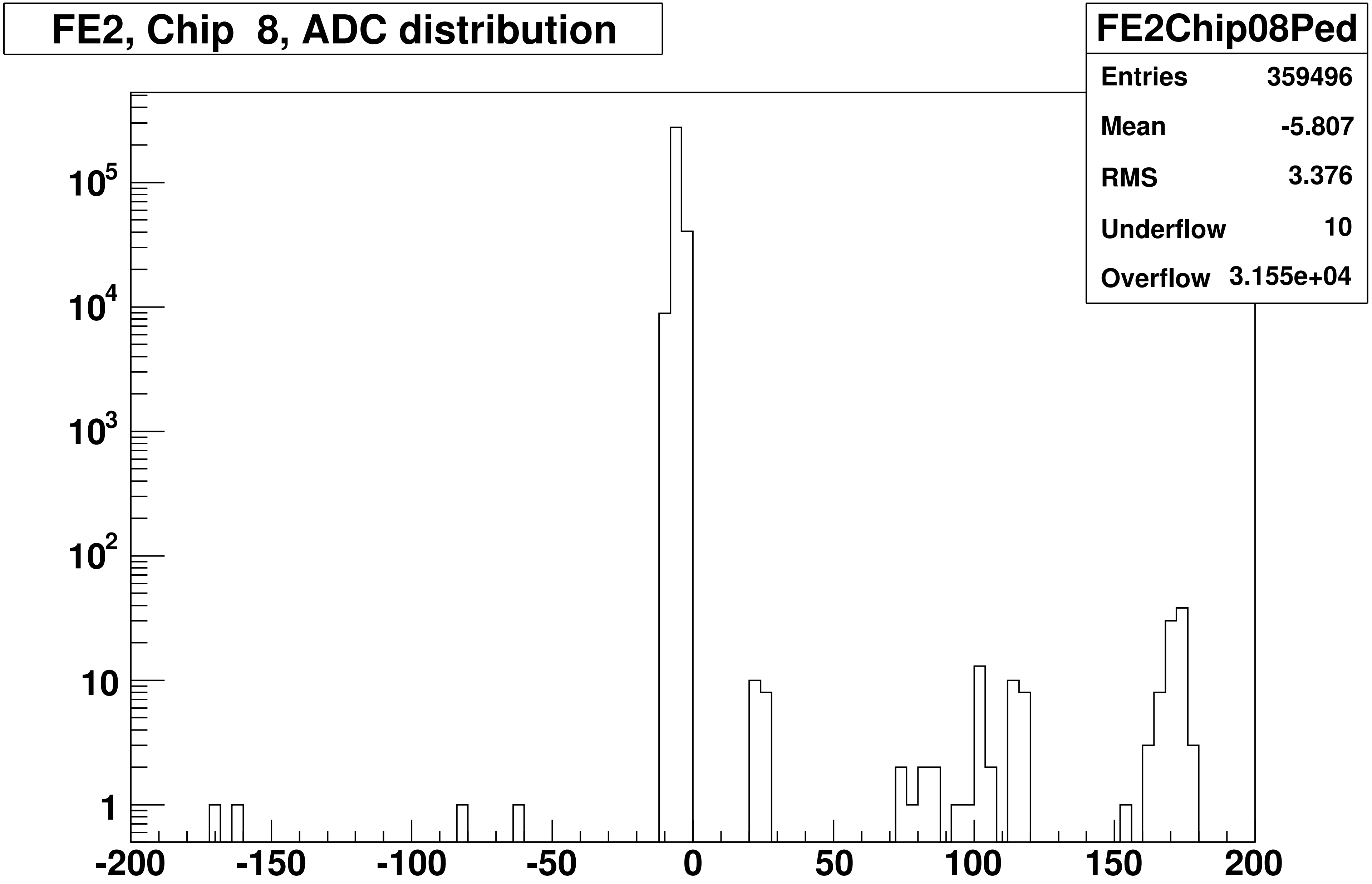
0
50
100
150
200



FE2, Chip 7, ADC distribution
FE2Chip07Sig
Entries 359496
Mean 1.906e+04
RMS 10.41
Underflow 3.289e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE2, Chip 8, ADC distribution
FE2Chip08All
Entries 359496
Mean 1651
RMS 5374
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE2, Chip 8, ADC distribution
FE2Chip08Ped
Entries 359496
Mean -5.807
RMS 3.376
Underflow 10
Overflow 3.155e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
-50
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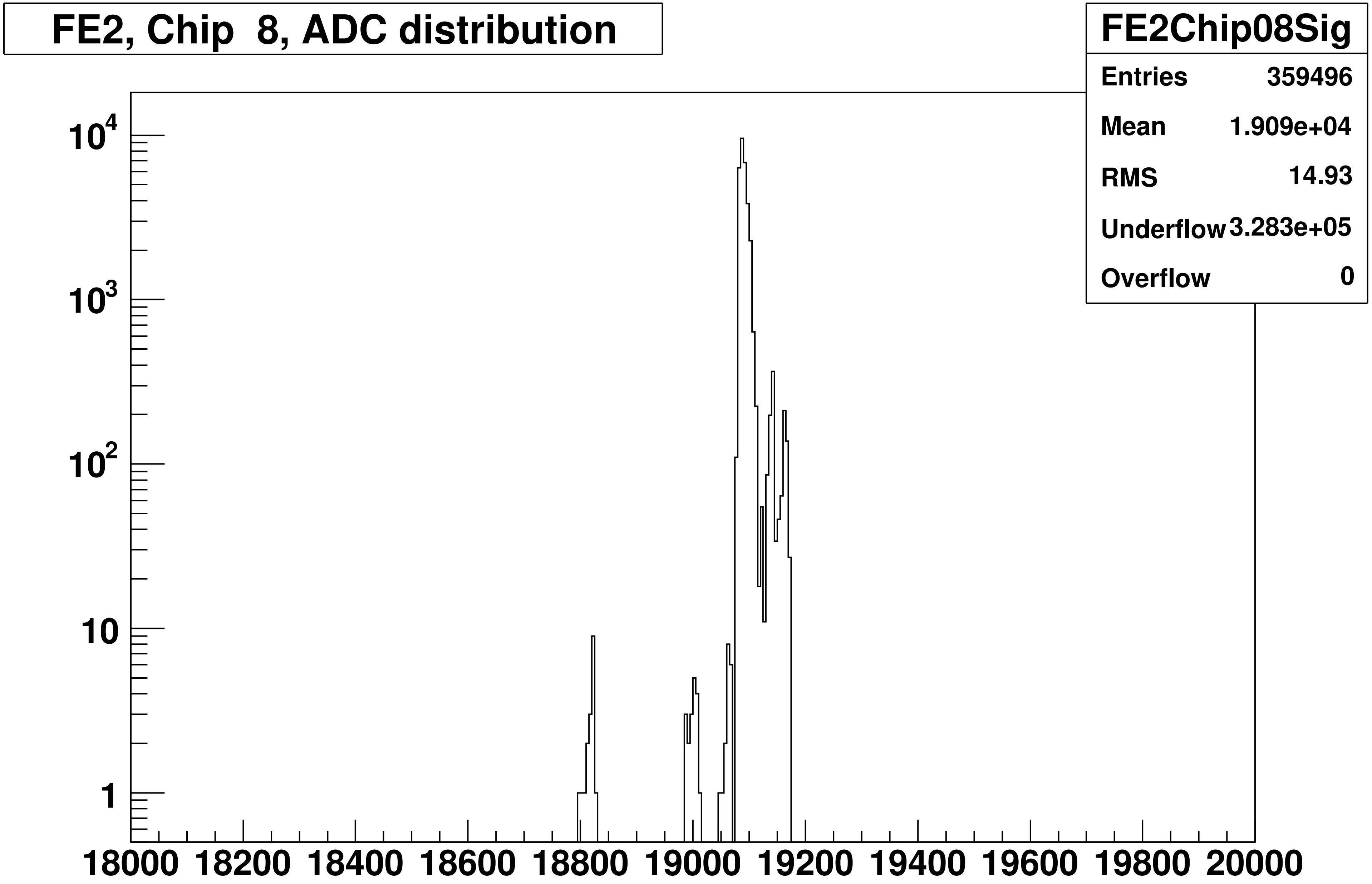
50
100
150
200


FE2, Chip 8, ADC distribution
FE2Chip08Sig
Entries 359496
Mean 1.909e+04
RMS 14.93
Underflow 3.283e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
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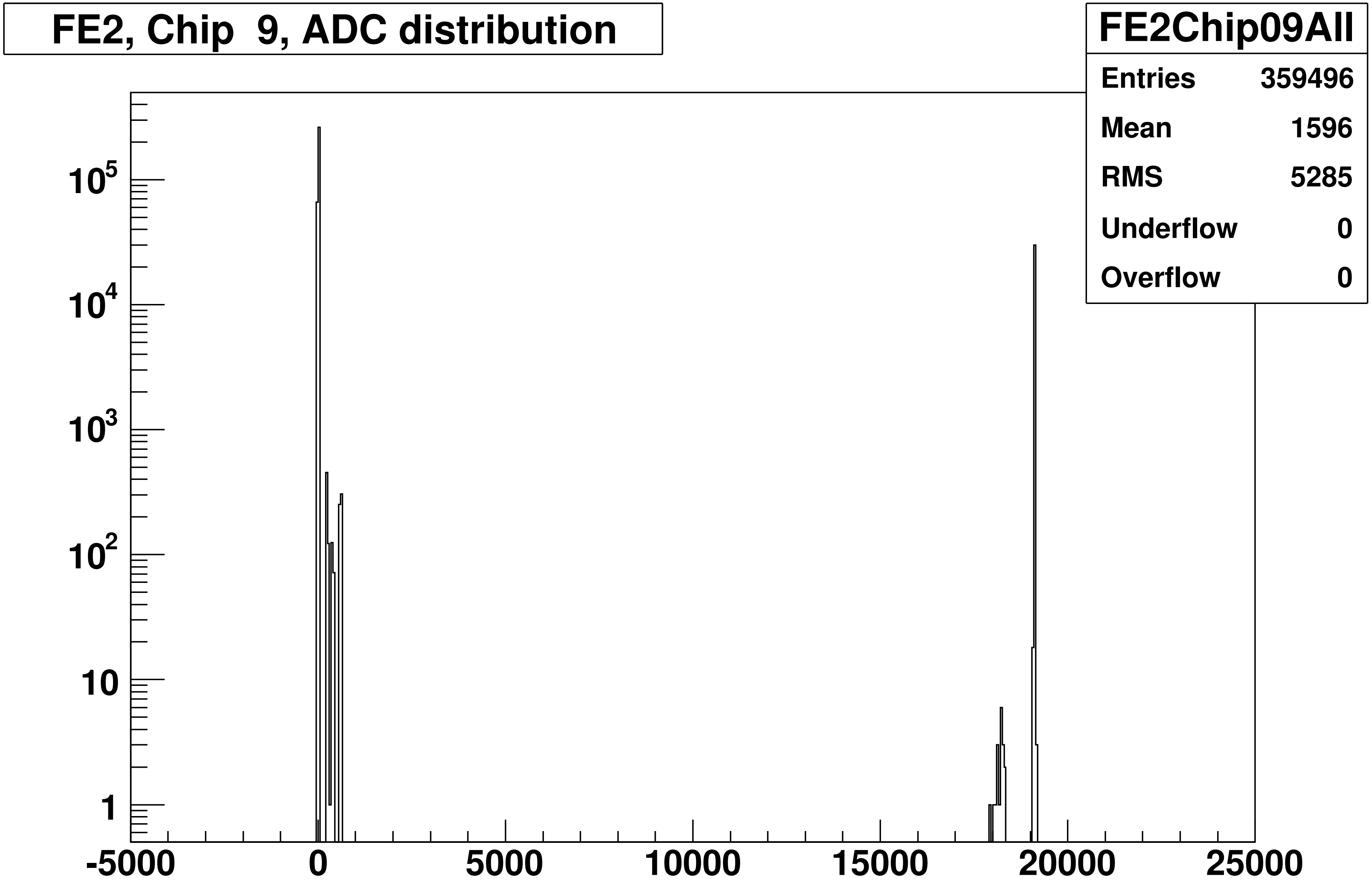
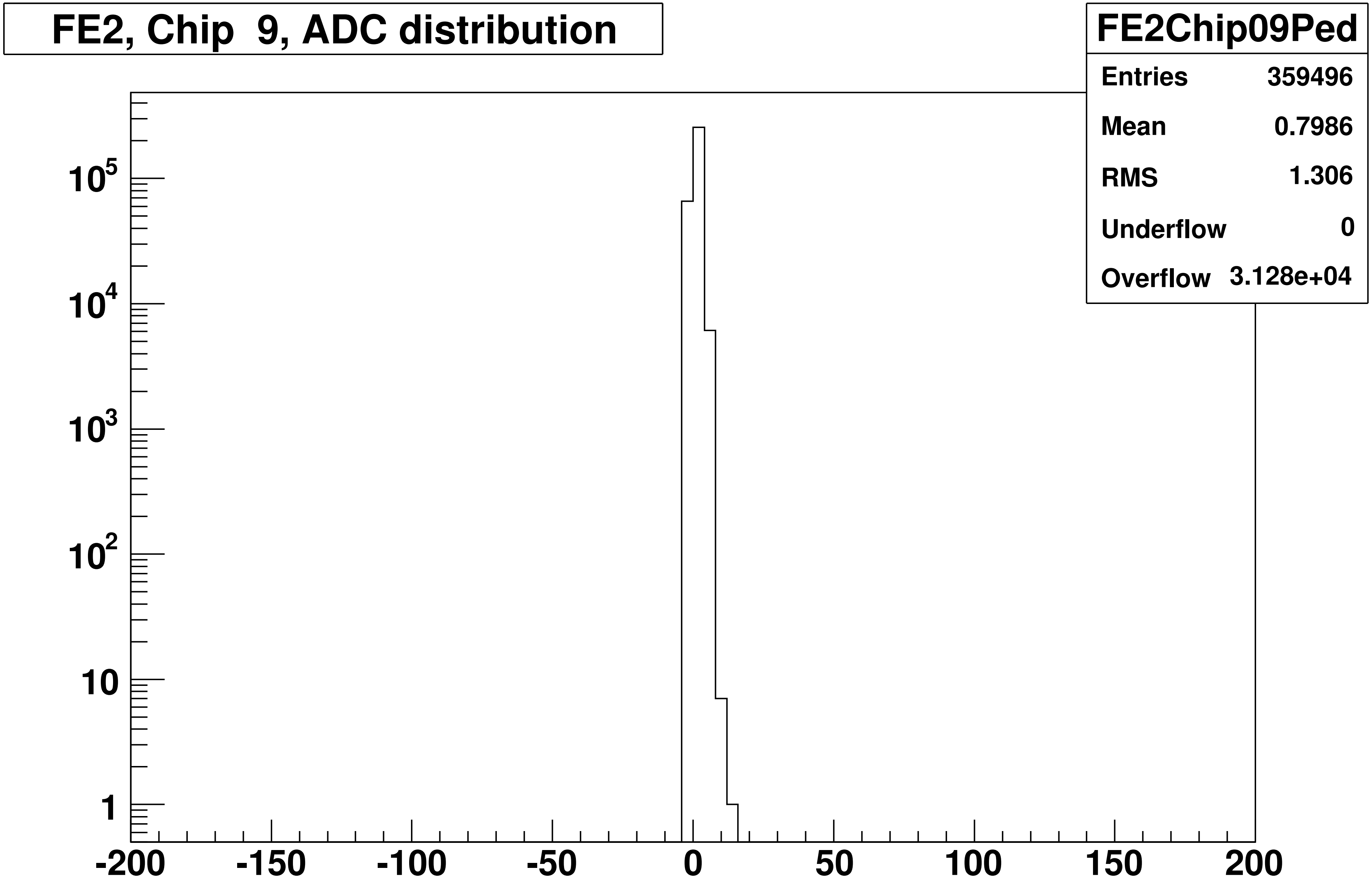
19600
19800
20000


FE2, Chip 9, ADC distribution
FE2Chip09All
Entries 359496
Mean 1596
RMS 5285
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE2, Chip 9, ADC distribution
FE2Chip09Ped
Entries 359496
Mean 0.7986
RMS 1.306
Underflow 0
Overflow 3.128e+04
10^5
10^4
10^3
10^2
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1
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-100
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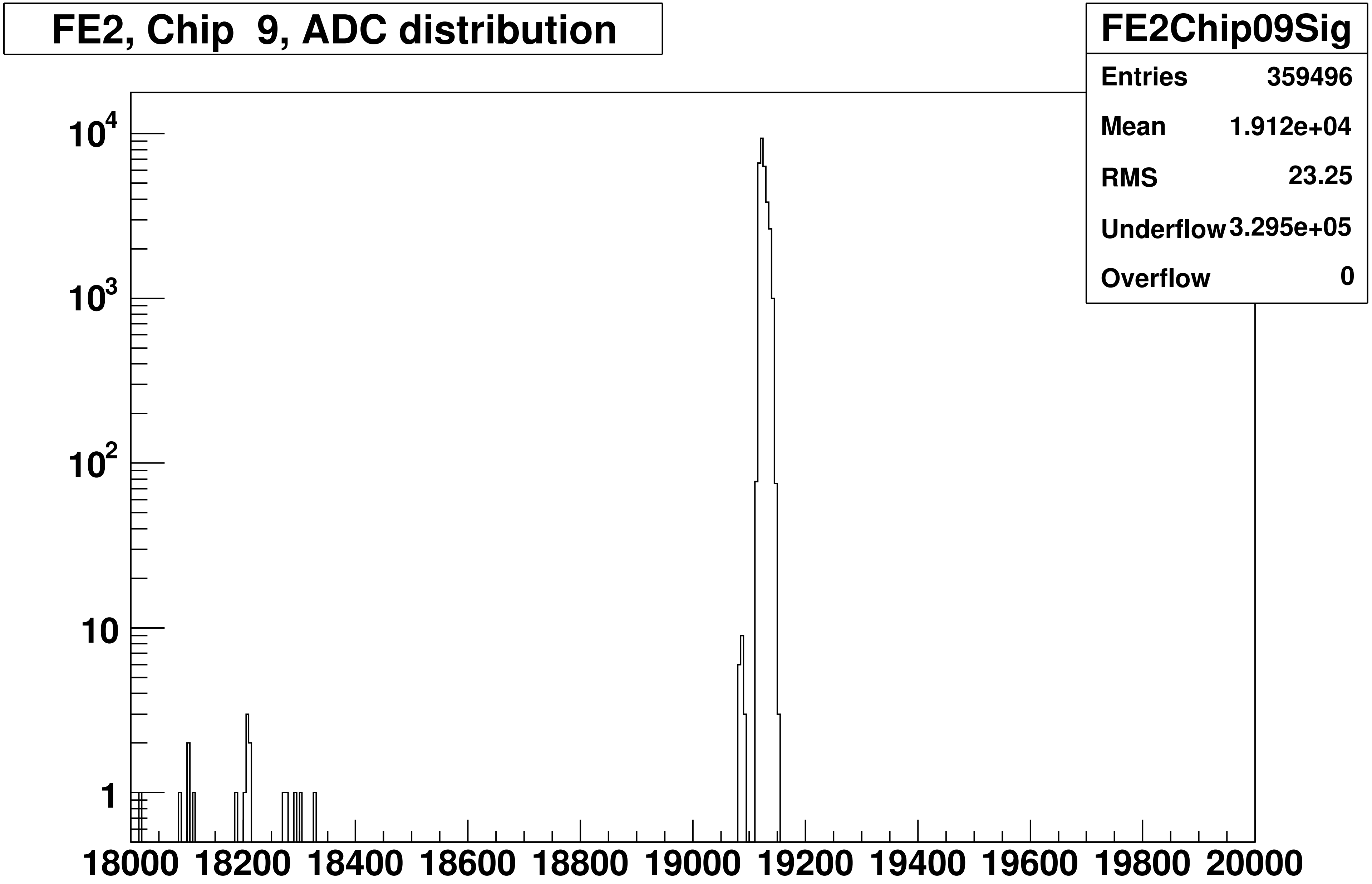
150
200


FE2, Chip 9, ADC distribution
FE2Chip09Sig
Entries 359496
Mean 1.912e+04
RMS 23.25
Underflow 3.295e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
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18400
18600
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19000
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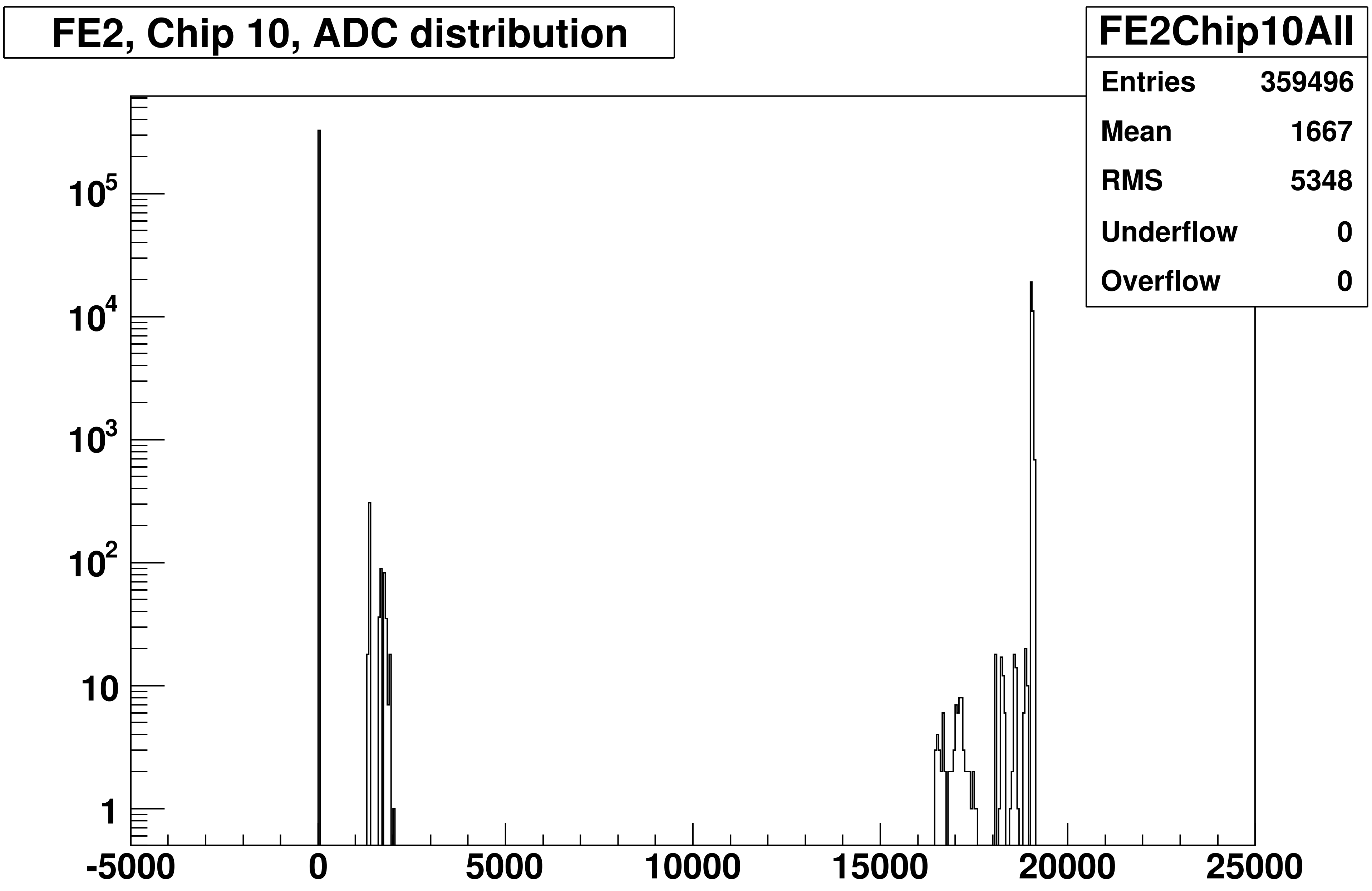
19400
19600
19800
20000


FE2, Chip 10, ADC distribution
FE2Chip10All
Entries 359496
Mean 1667
RMS 5348
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
1
-5000
0
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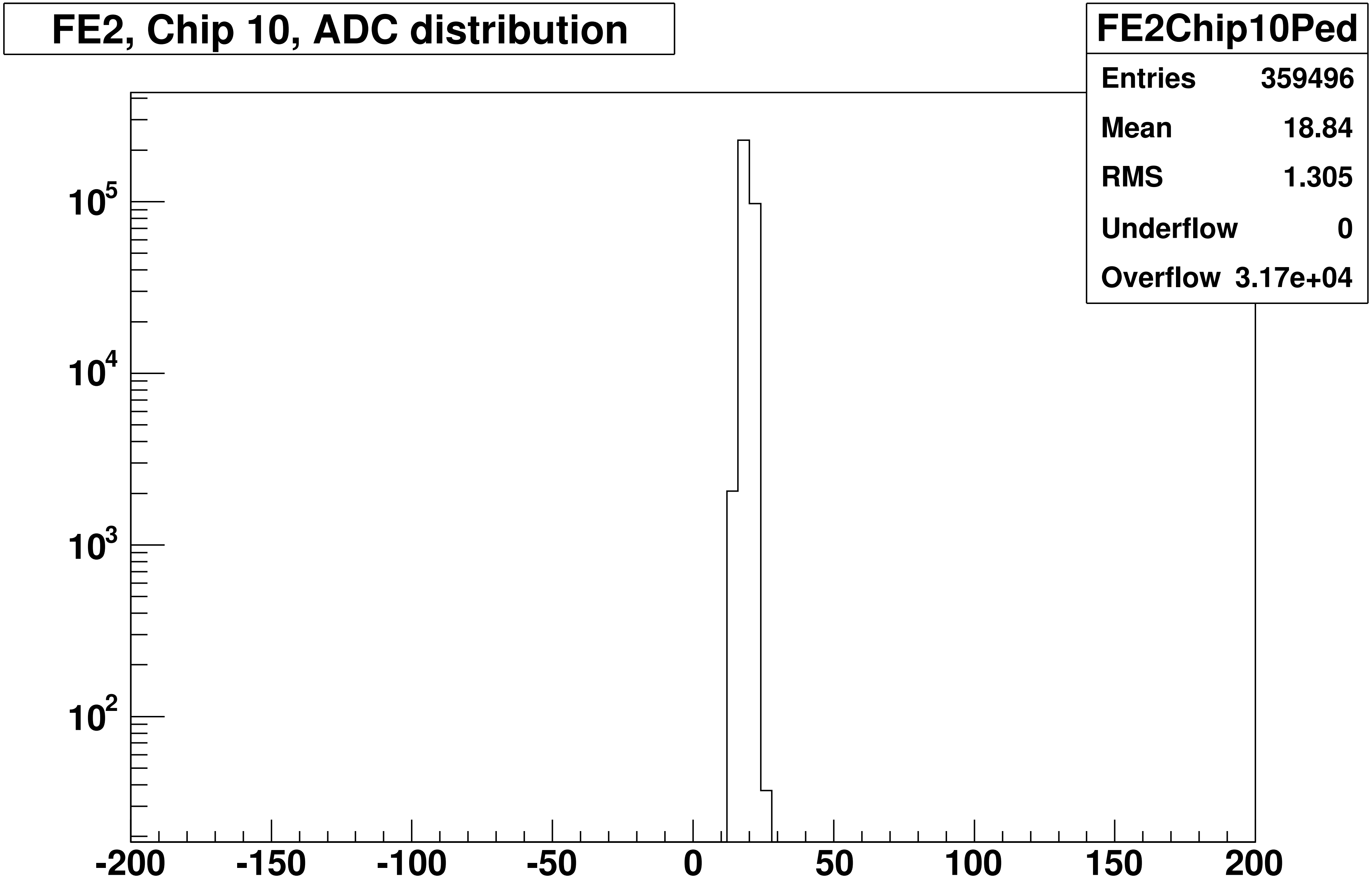
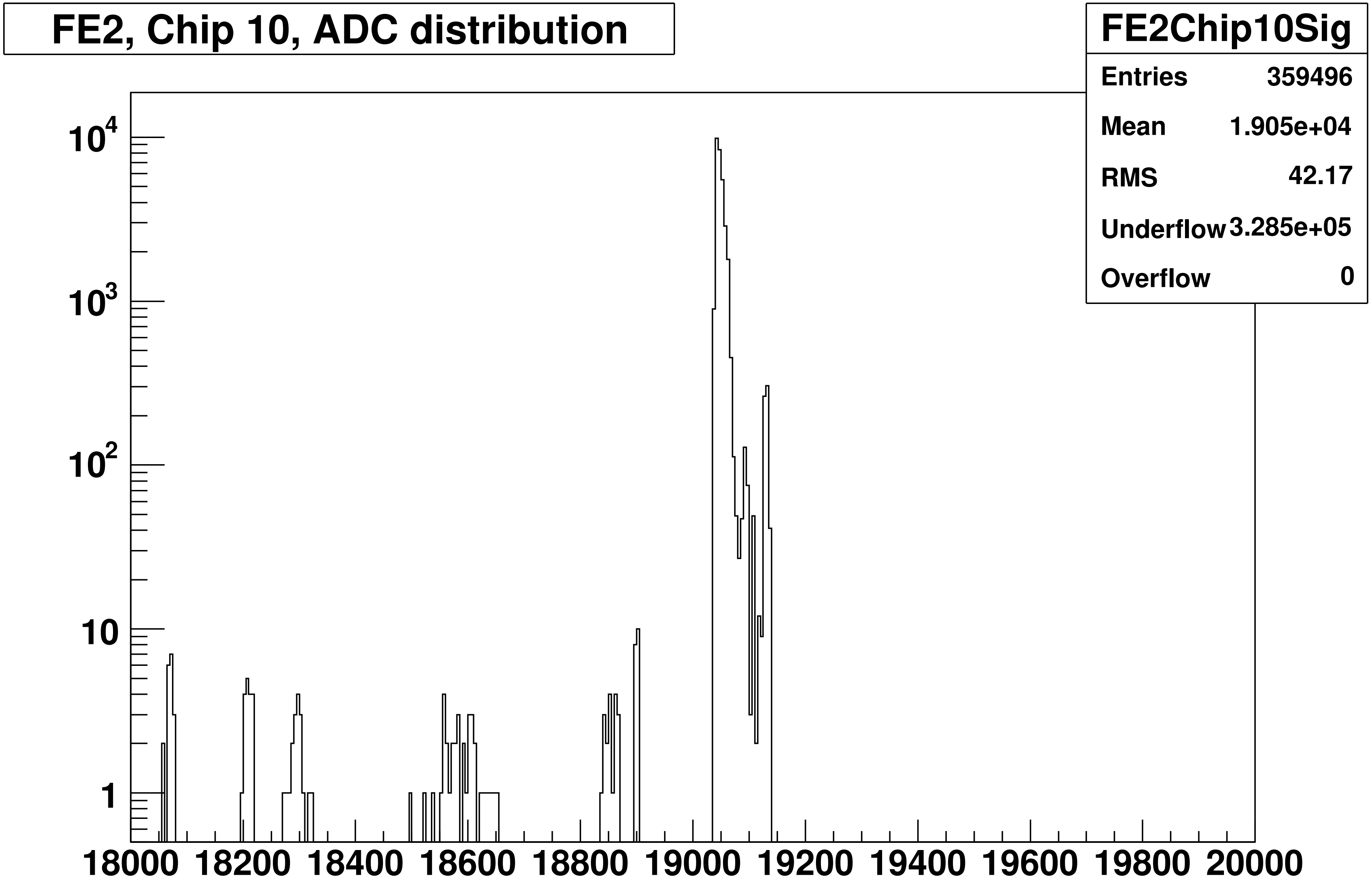
10000
15000
20000
25000



FE2, Chip 10, ADC distribution
FE2Chip10Ped
Entries 359496
Mean 18.84
RMS 1.305
Underflow 0
Overflow 3.17e+04
10^5
10^4
10^3
10^2
-200 -150 -100 -50 0 50 100 150 200



FE2, Chip 10, ADC distribution
FE2Chip10Sig
Entries 359496
Mean 1.905e+04
RMS 42.17
Underflow 3.285e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
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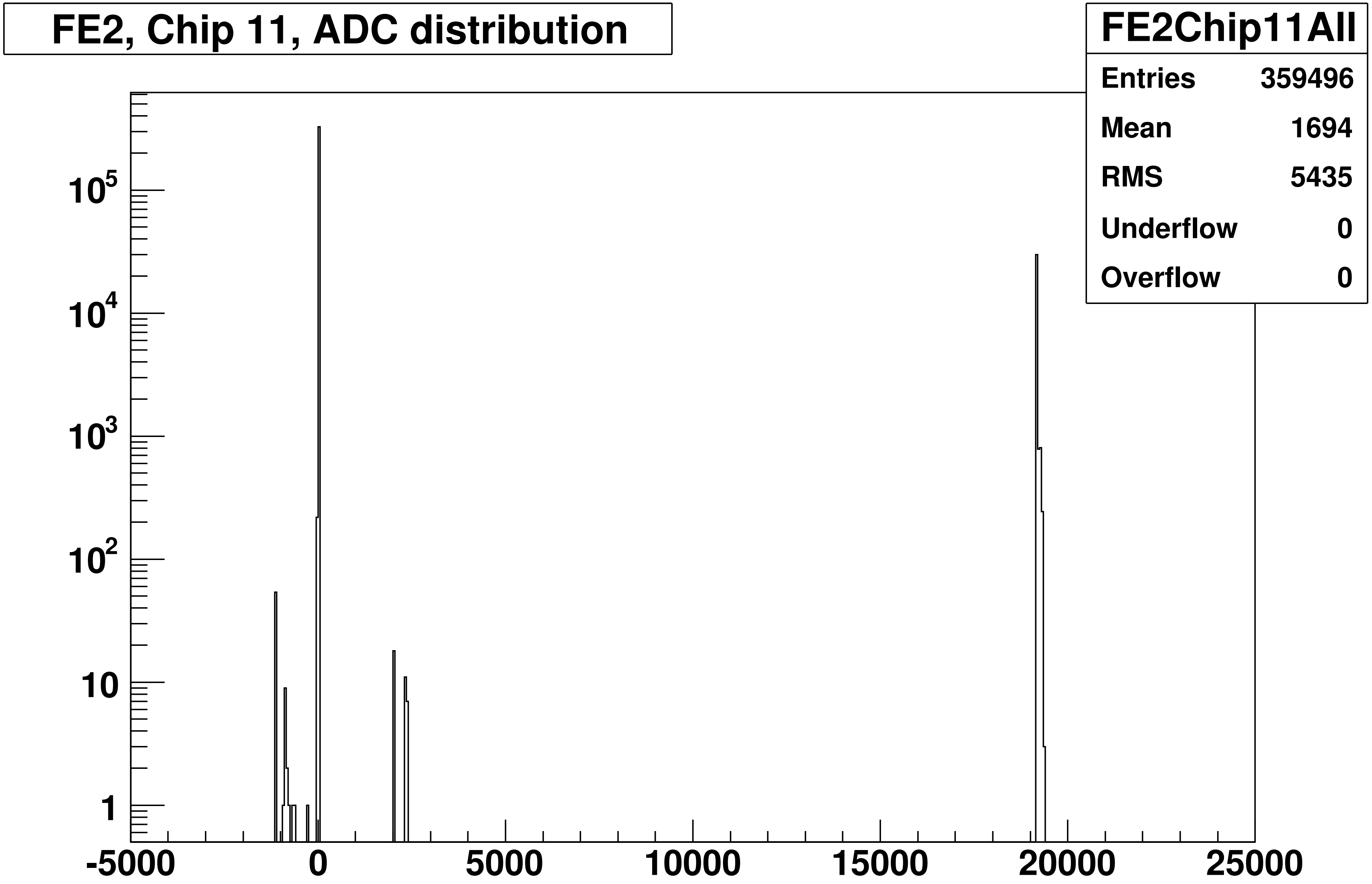
19000
19200
19400
19600
19800
20000


FE2, Chip 11, ADC distribution
FE2Chip11All
Entries 359496
Mean 1694
RMS 5435
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
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0
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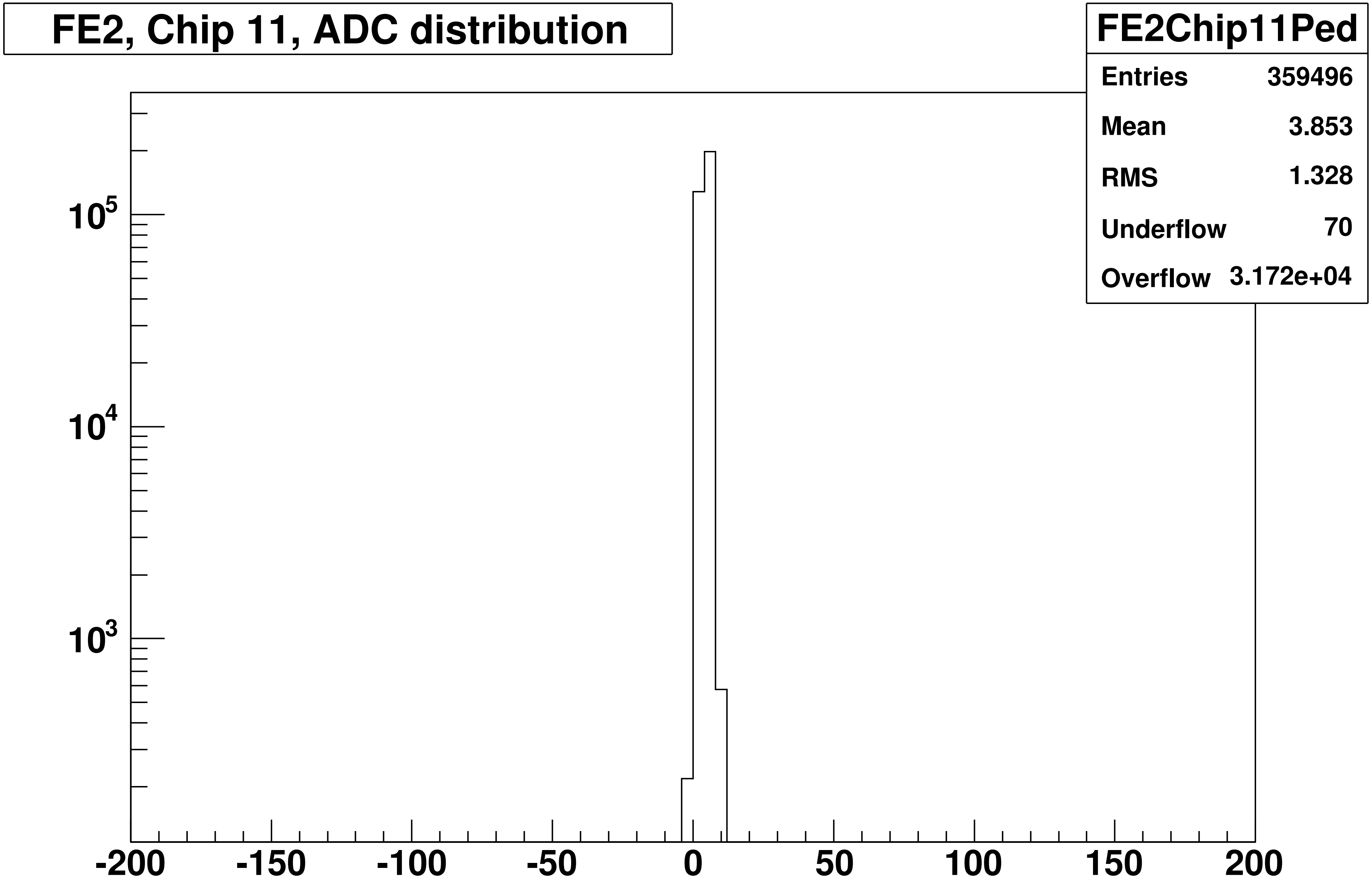
10000
15000
20000
25000


FE2, Chip 11, ADC distribution
FE2Chip11Ped
Entries 359496
Mean 3.853
RMS 1.328
Underflow 70
Overflow 3.172e+04
10^5
10^4
10^3
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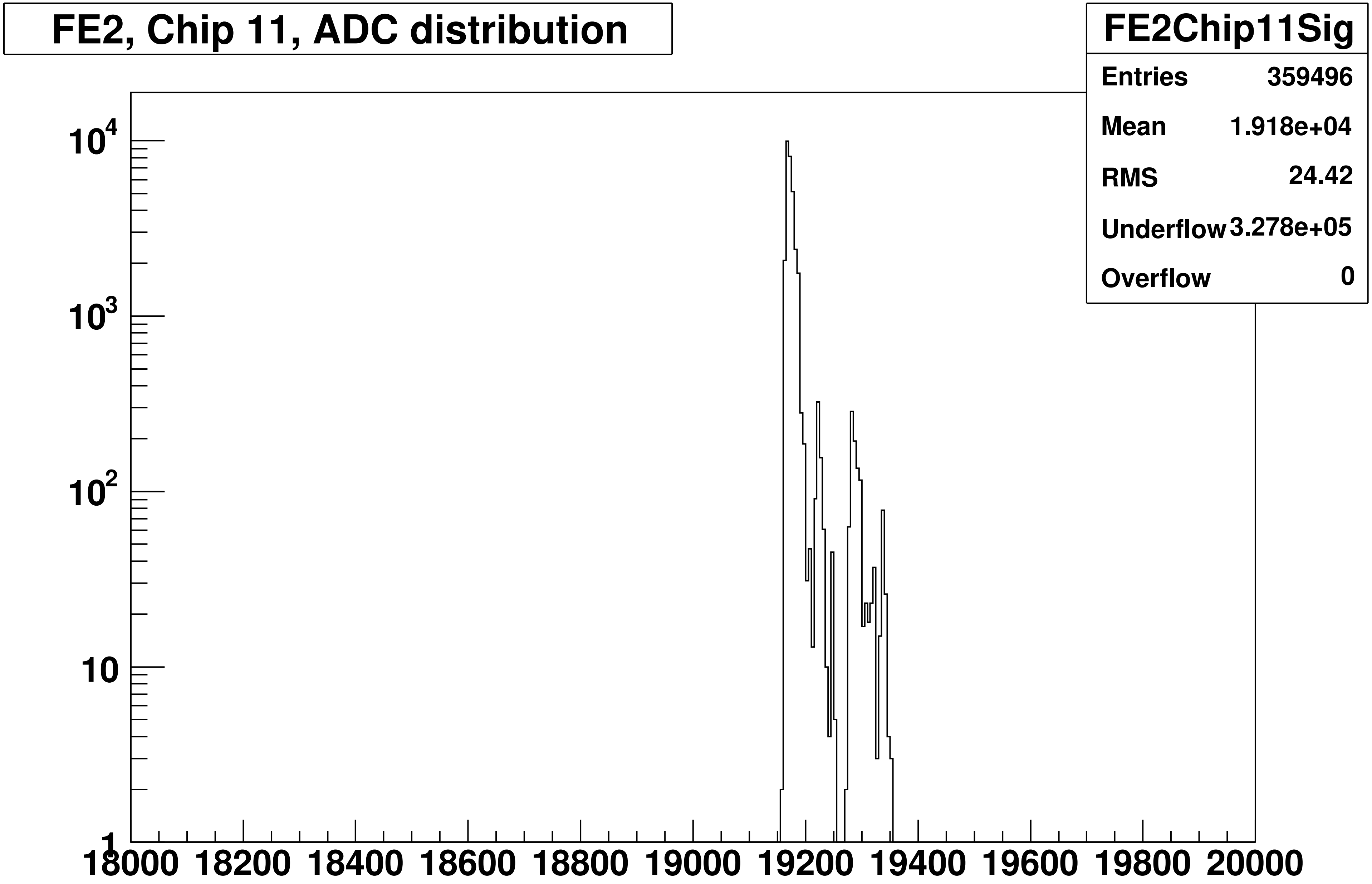
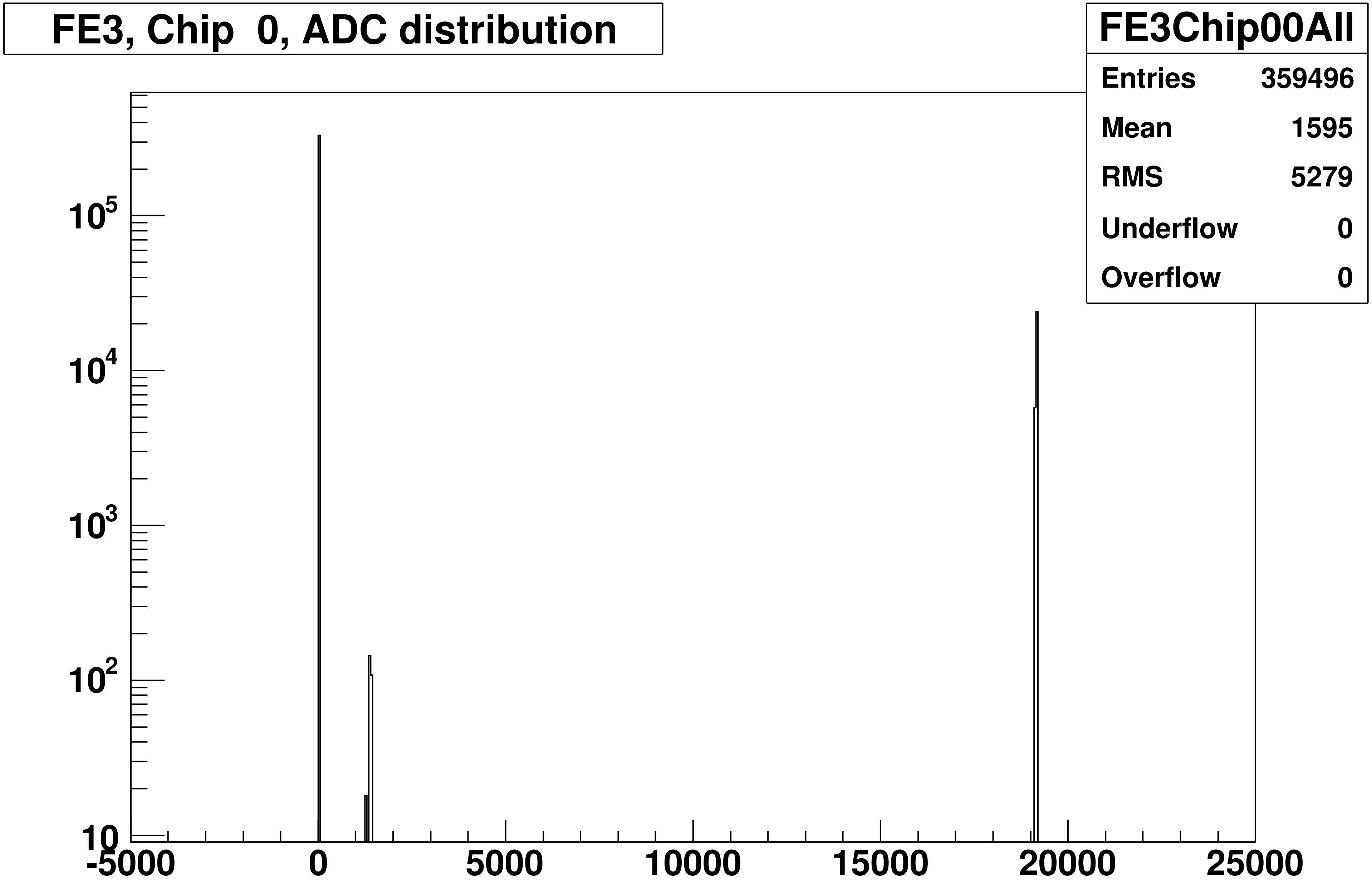
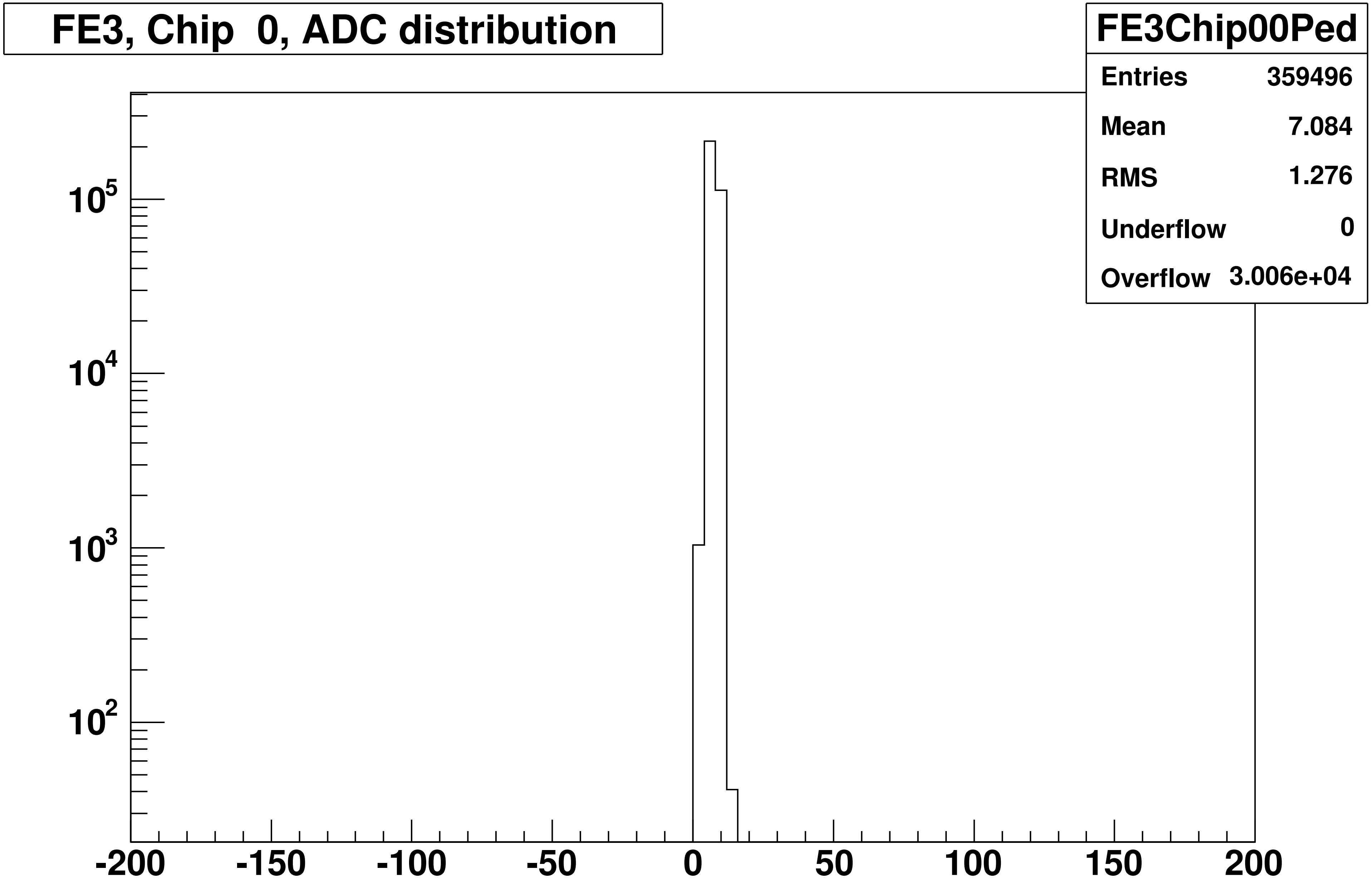
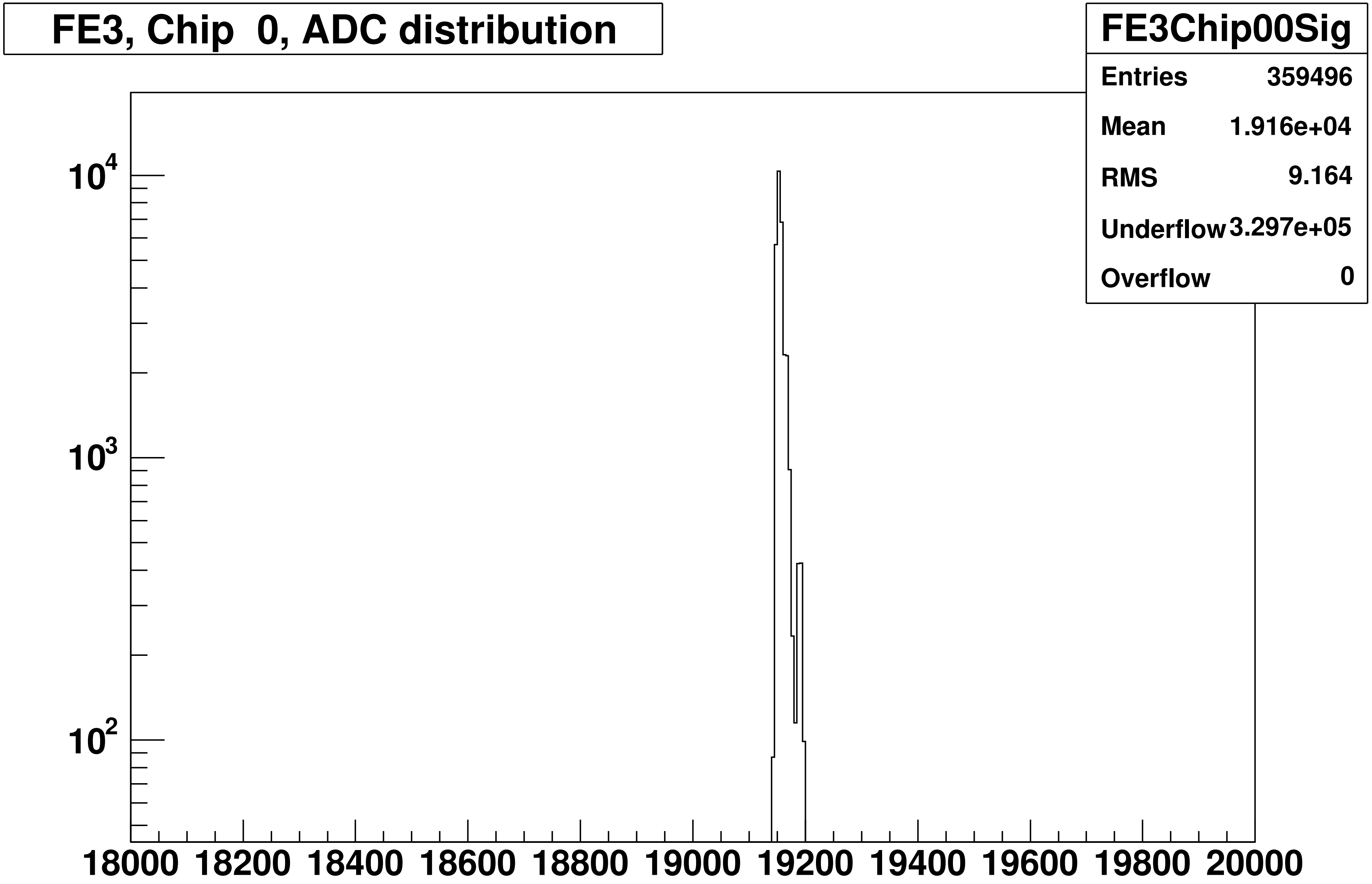
-100
-50
0
50
100
150
200


FE2, Chip 11, ADC distribution
FE2Chip11Sig
Entries 359496
Mean 1.918e+04
RMS 24.42
Underflow 3.278e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE3, Chip 0, ADC distribution
FE3Chip00All
Entries 359496
Mean 1595
RMS 5279
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE3, Chip 0, ADC distribution
FE3Chip00Ped
Entries 359496
Mean 7.084
RMS 1.276
Underflow 0
Overflow 3.006e+04
10^5
10^4
10^3
10^2
-200
-150
-100
-50
0
50
100
150
200


FE3, Chip 0, ADC distribution
FE3Chip00Sig
Entries 359496
Mean 1.916e+04
RMS 9.164
Underflow 3.297e+05
Overflow 0
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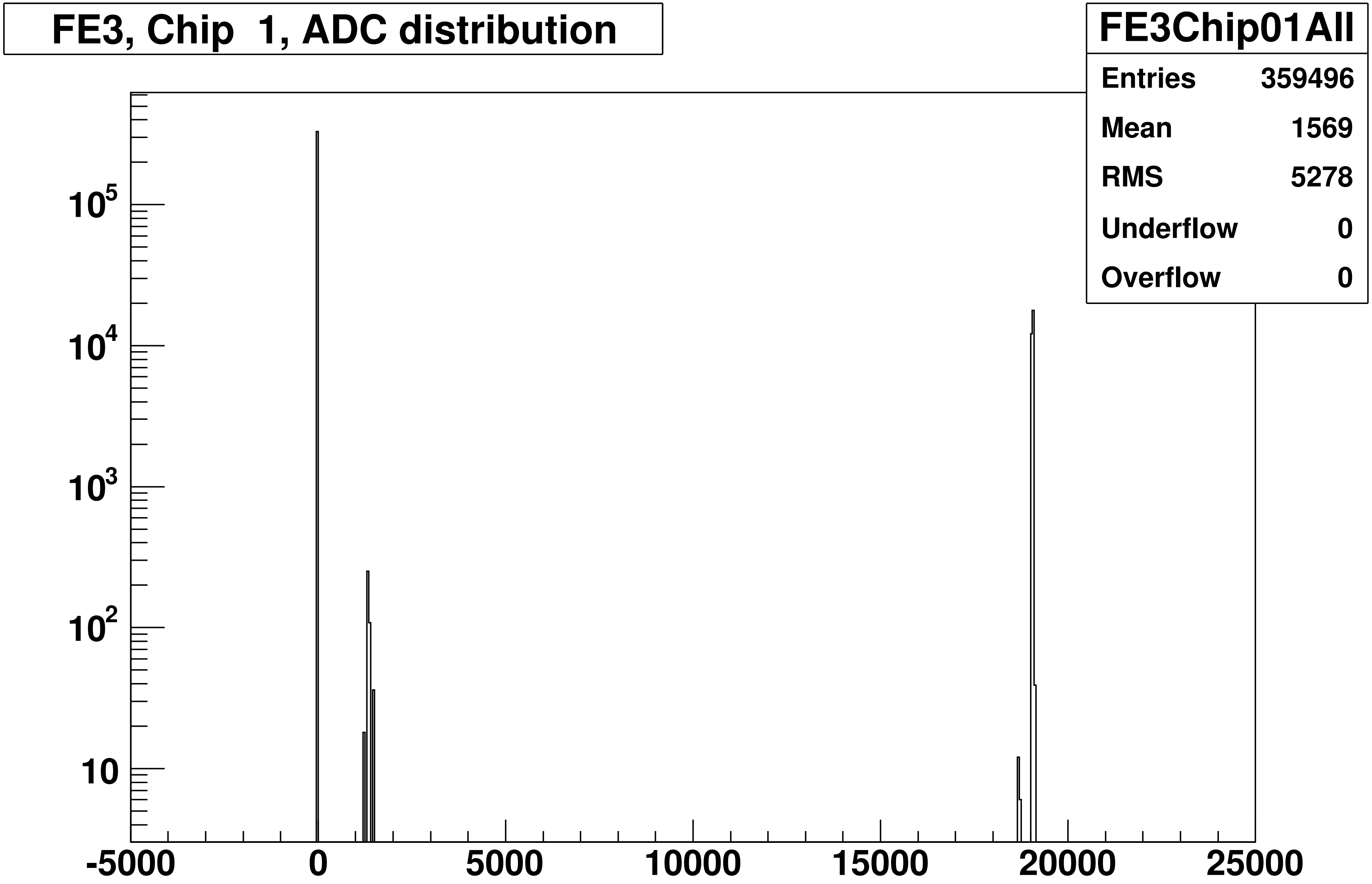
10^3
10^2
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE3, Chip 1, ADC distribution
FE3Chip01All
Entries 359496
Mean 1569
RMS 5278
Underflow 0
Overflow 0
10
10^2
10^3
10^4
10^5
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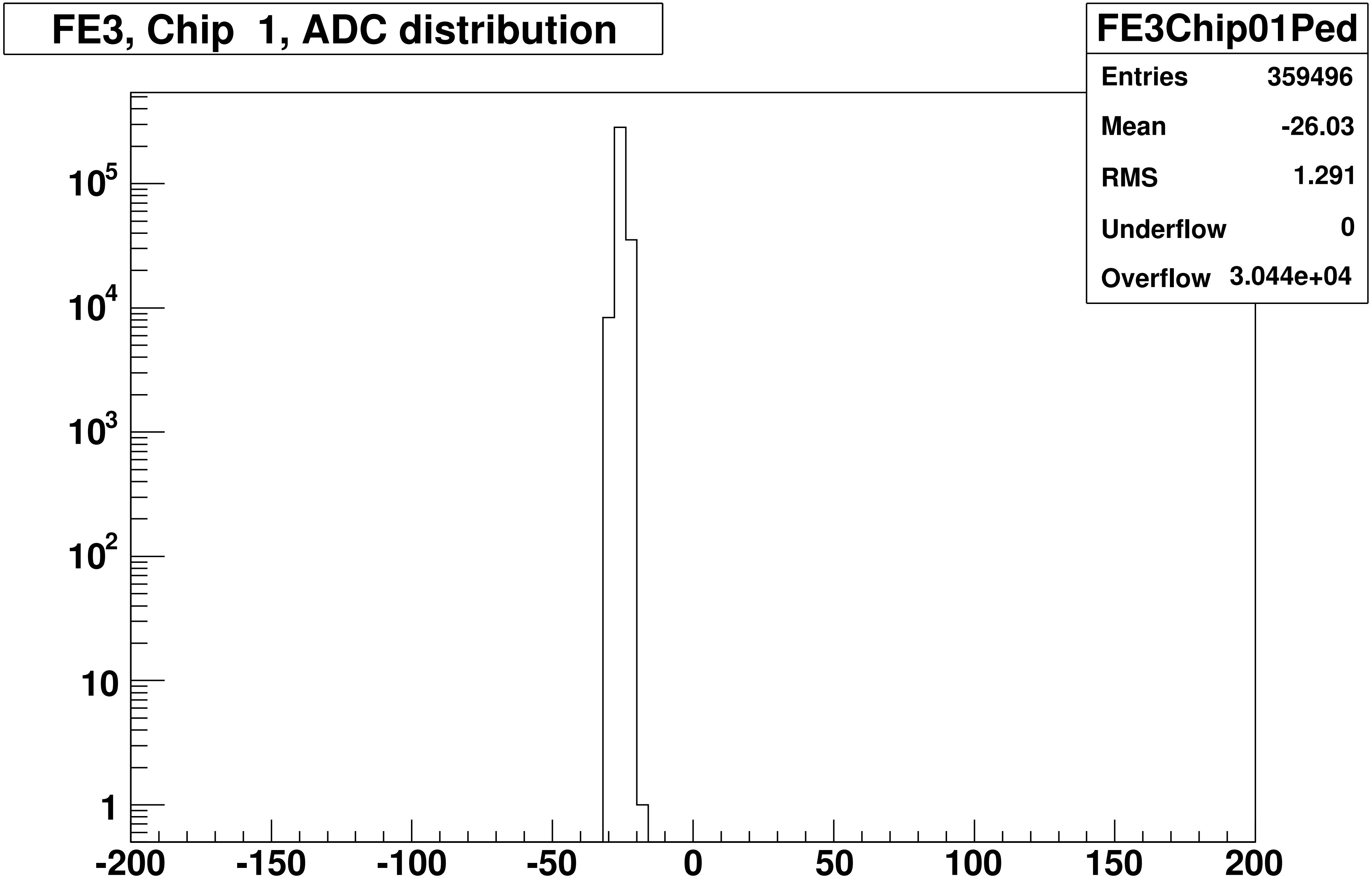
0
5000
10000
15000
20000
25000



FE3, Chip 1, ADC distribution
FE3Chip01Ped
Entries 359496
Mean -26.03
RMS 1.291
Underflow 0
Overflow 3.044e+04
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10^4
10^3
10^2
10
1
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-100
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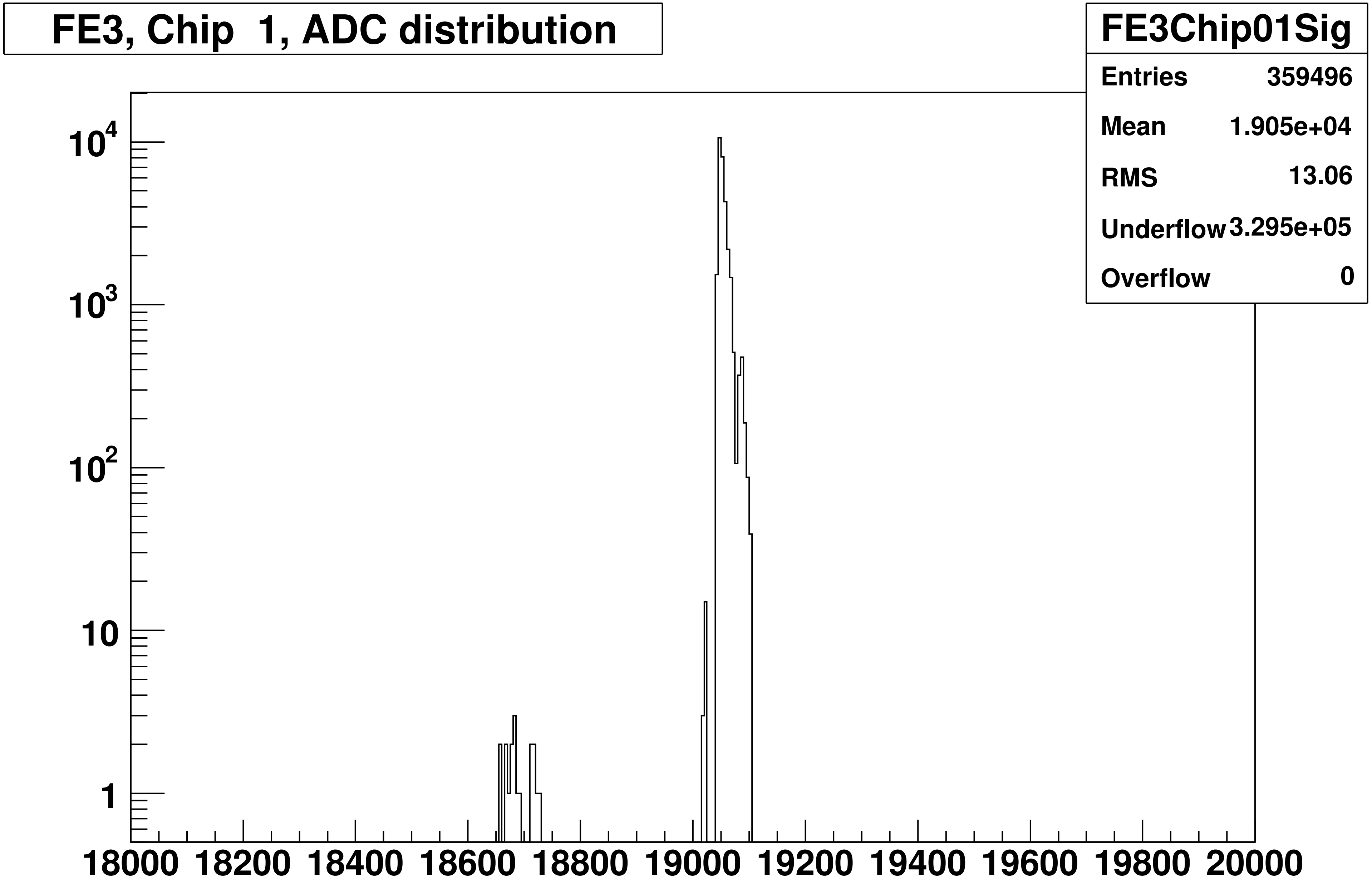
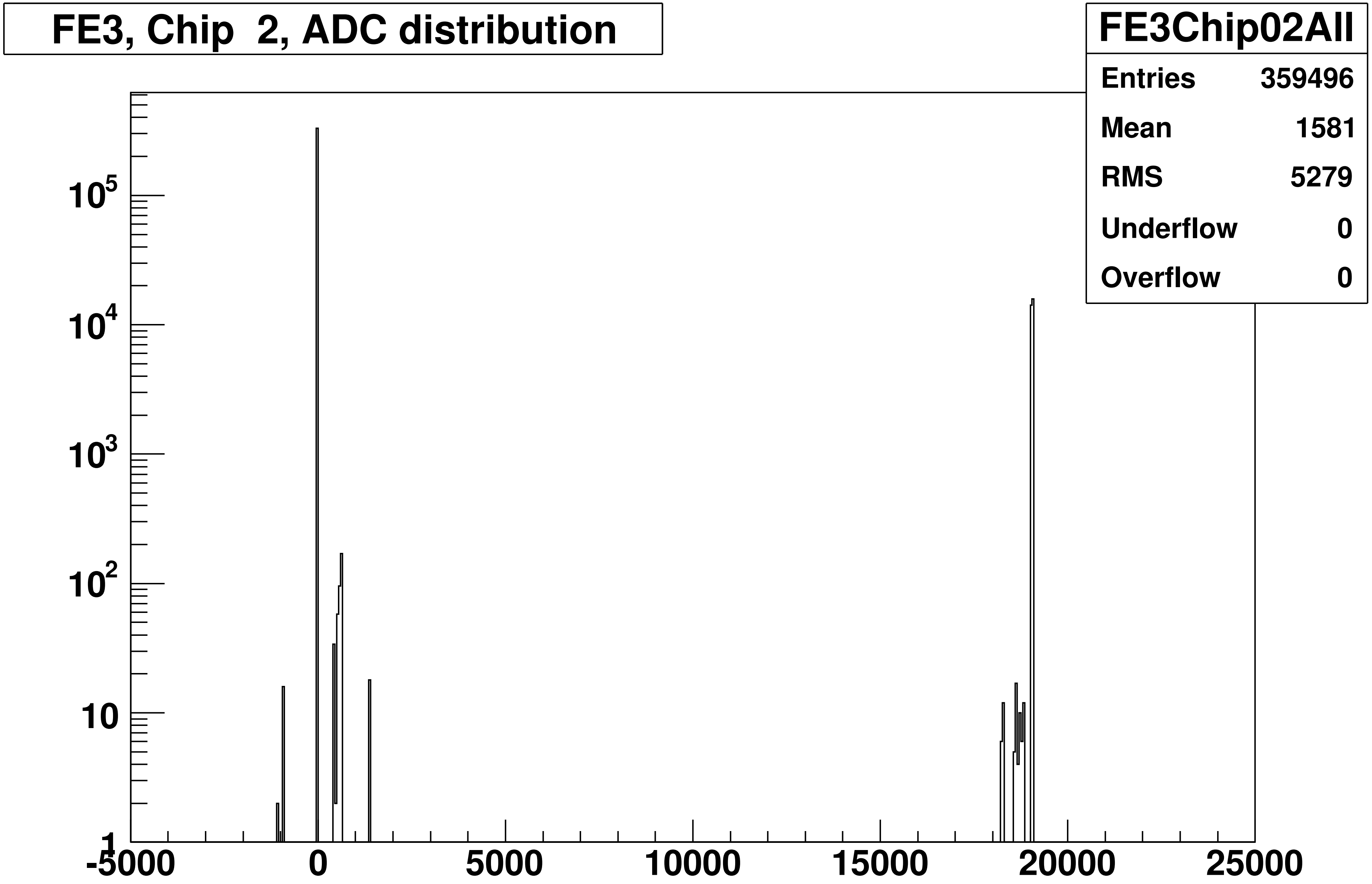
0
50
100
150
200



FE3, Chip 1, ADC distribution
FE3Chip01Sig
Entries 359496
Mean 1.905e+04
RMS 13.06
Underflow 3.295e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000



FE3, Chip 2, ADC distribution
FE3Chip02All
Entries 359496
Mean 1581
RMS 5279
Underflow 0
Overflow 0
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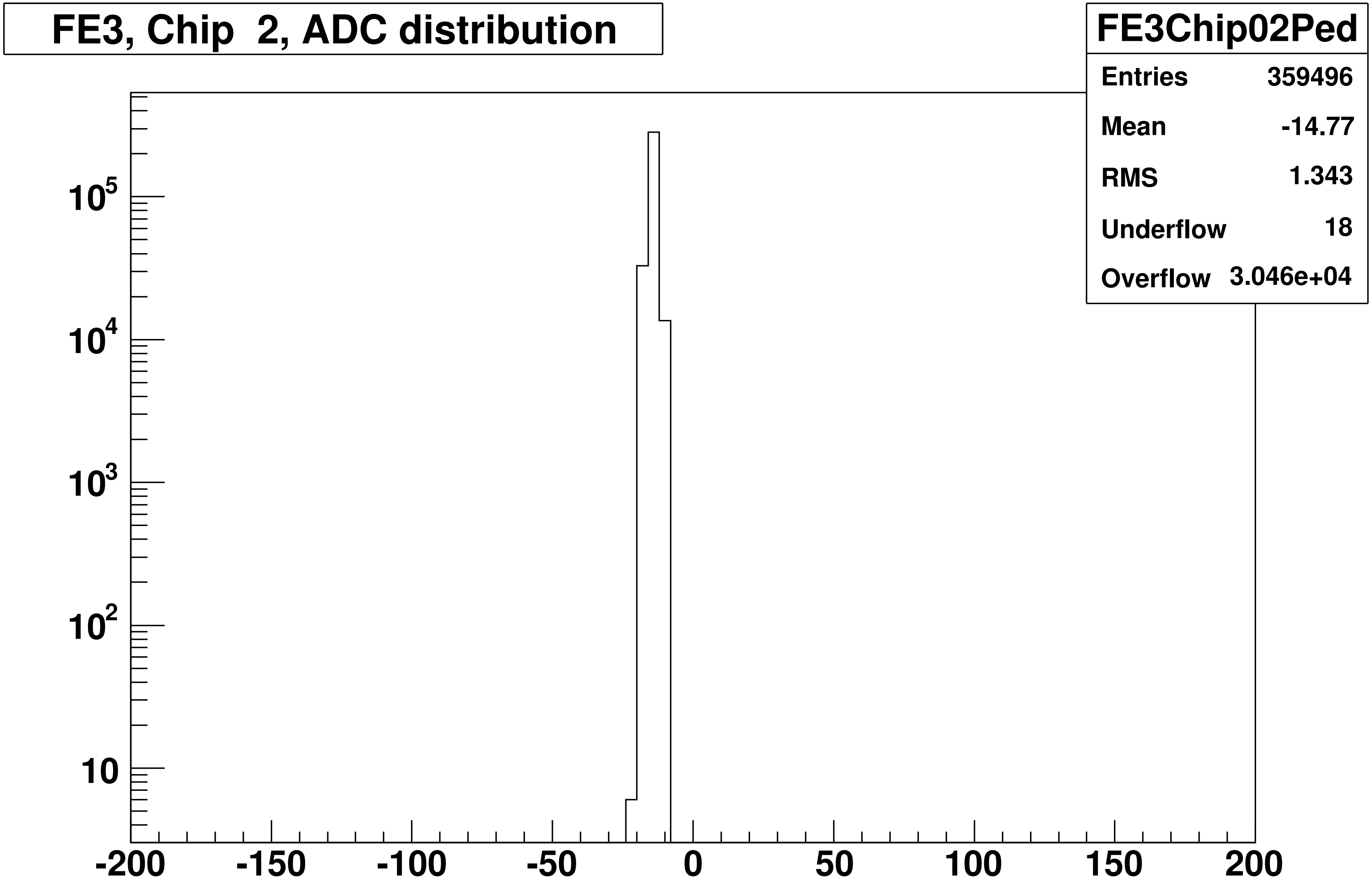
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE3, Chip 2, ADC distribution
FE3Chip02Ped
Entries 359496
Mean -14.77
RMS 1.343
Underflow 18
Overflow 3.046e+04
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10^4
10^3
10^2
10
-200
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-100
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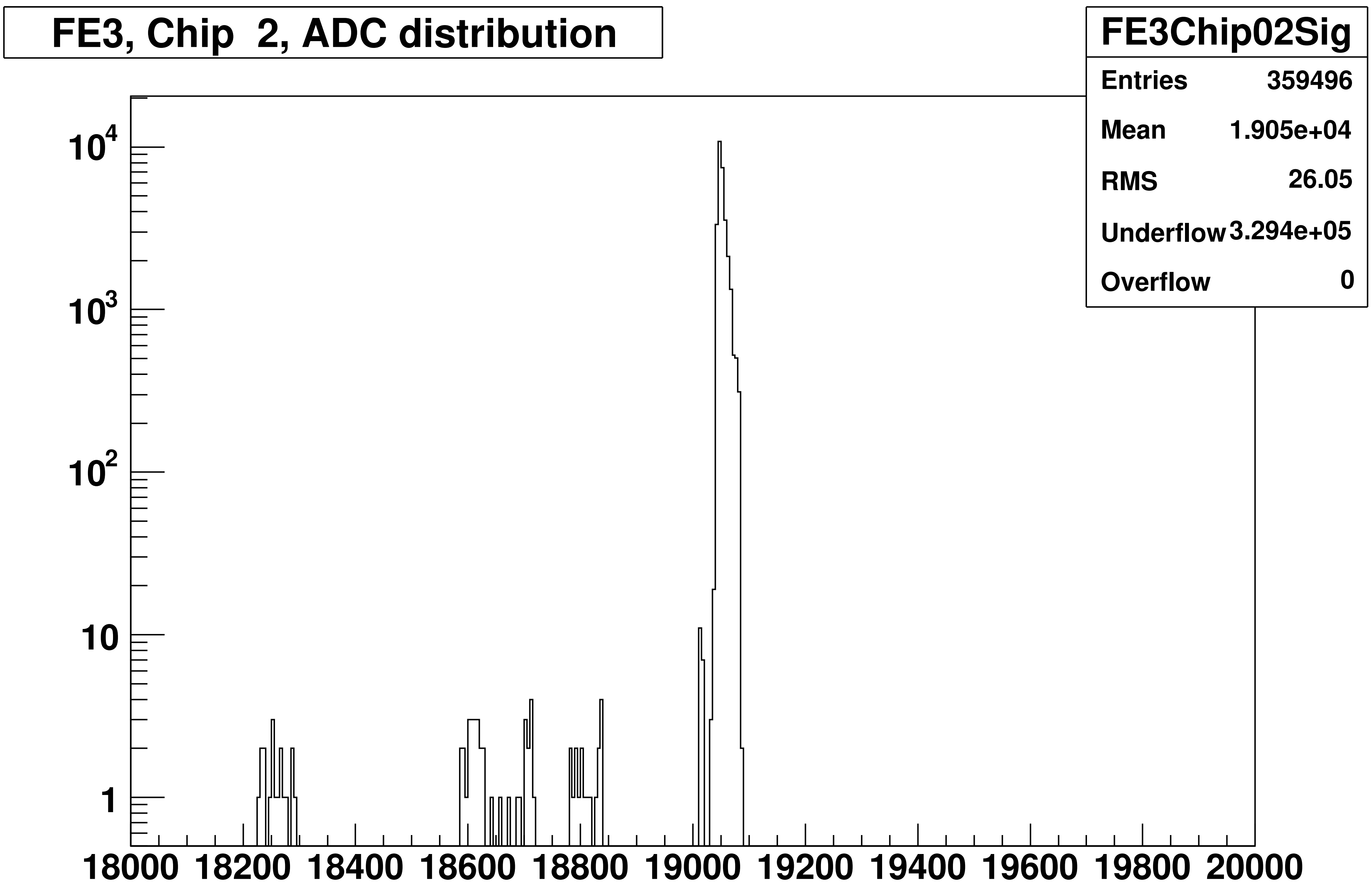
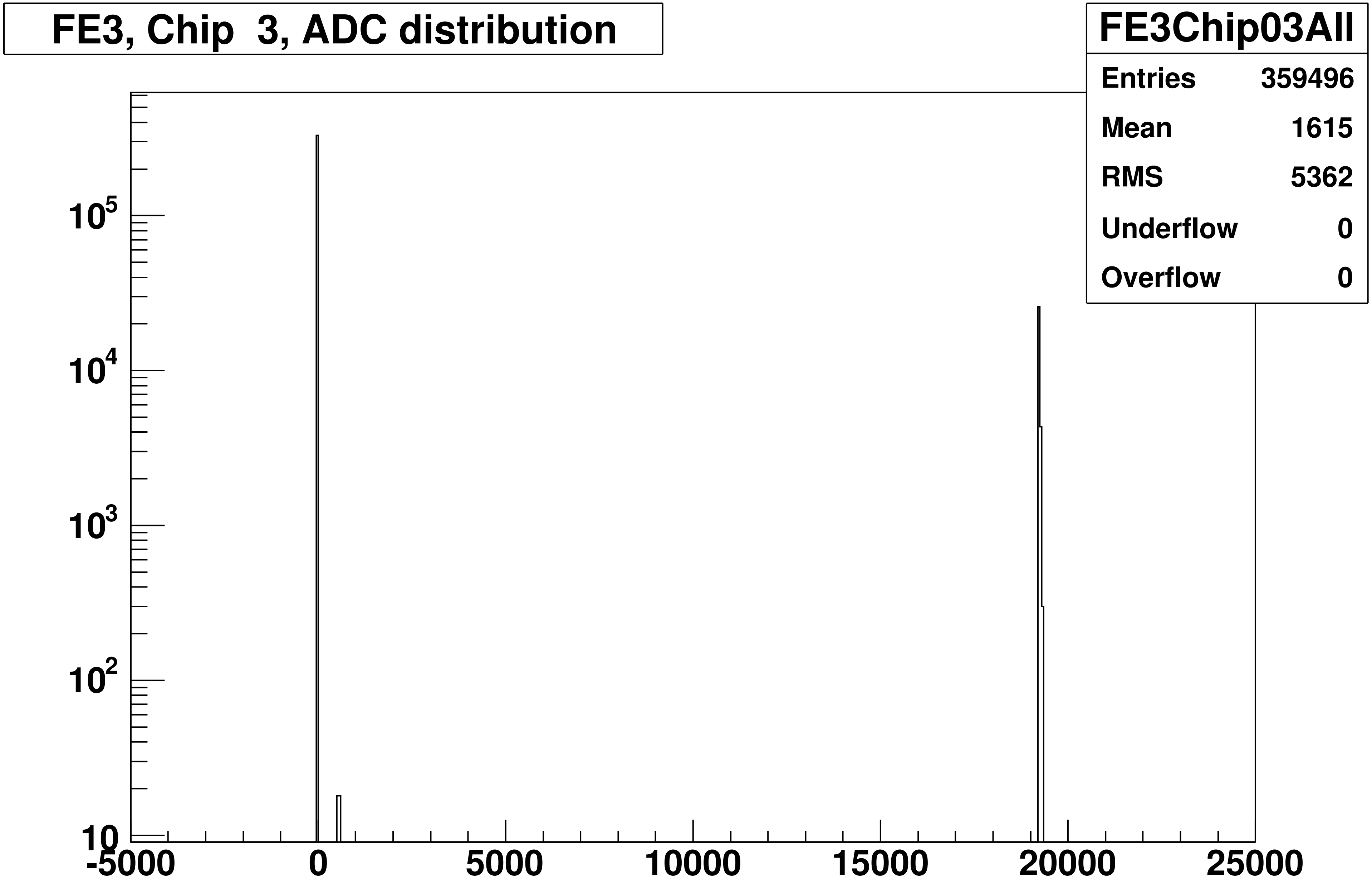
0
50
100
150
200


FE3, Chip 2, ADC distribution
FE3Chip02Sig
Entries 359496
Mean 1.905e+04
RMS 26.05
Underflow 3.294e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE3, Chip 3, ADC distribution
FE3Chip03All
Entries 359496
Mean 1615
RMS 5362
Underflow 0
Overflow 0
10
10^2
10^3
10^4
10^5
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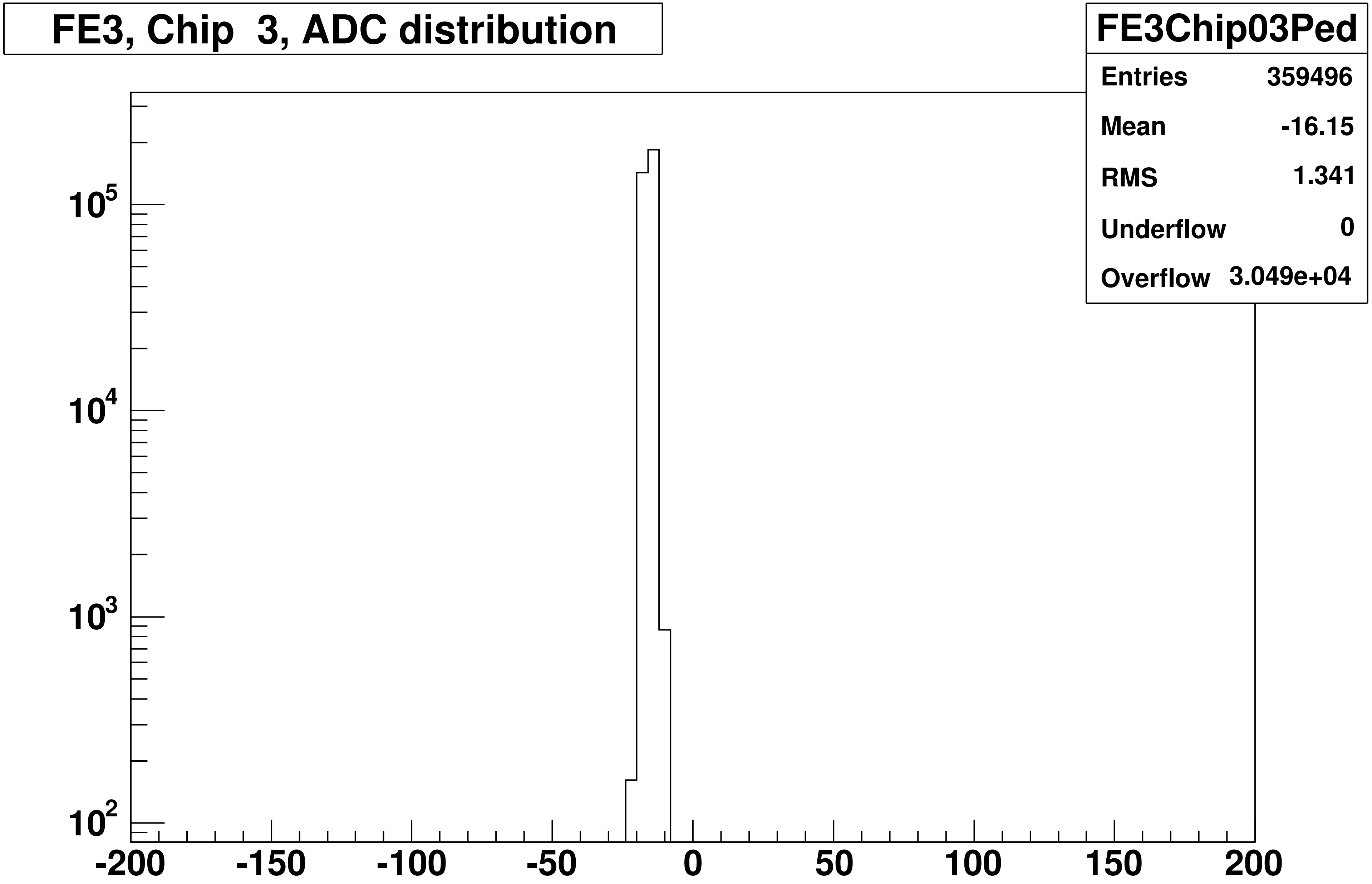
0
5000
10000
15000
20000
25000


FE3, Chip 3, ADC distribution
FE3Chip03Ped
Entries 359496
Mean -16.15
RMS 1.341
Underflow 0
Overflow 3.049e+04
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10^4
10^3
10^2
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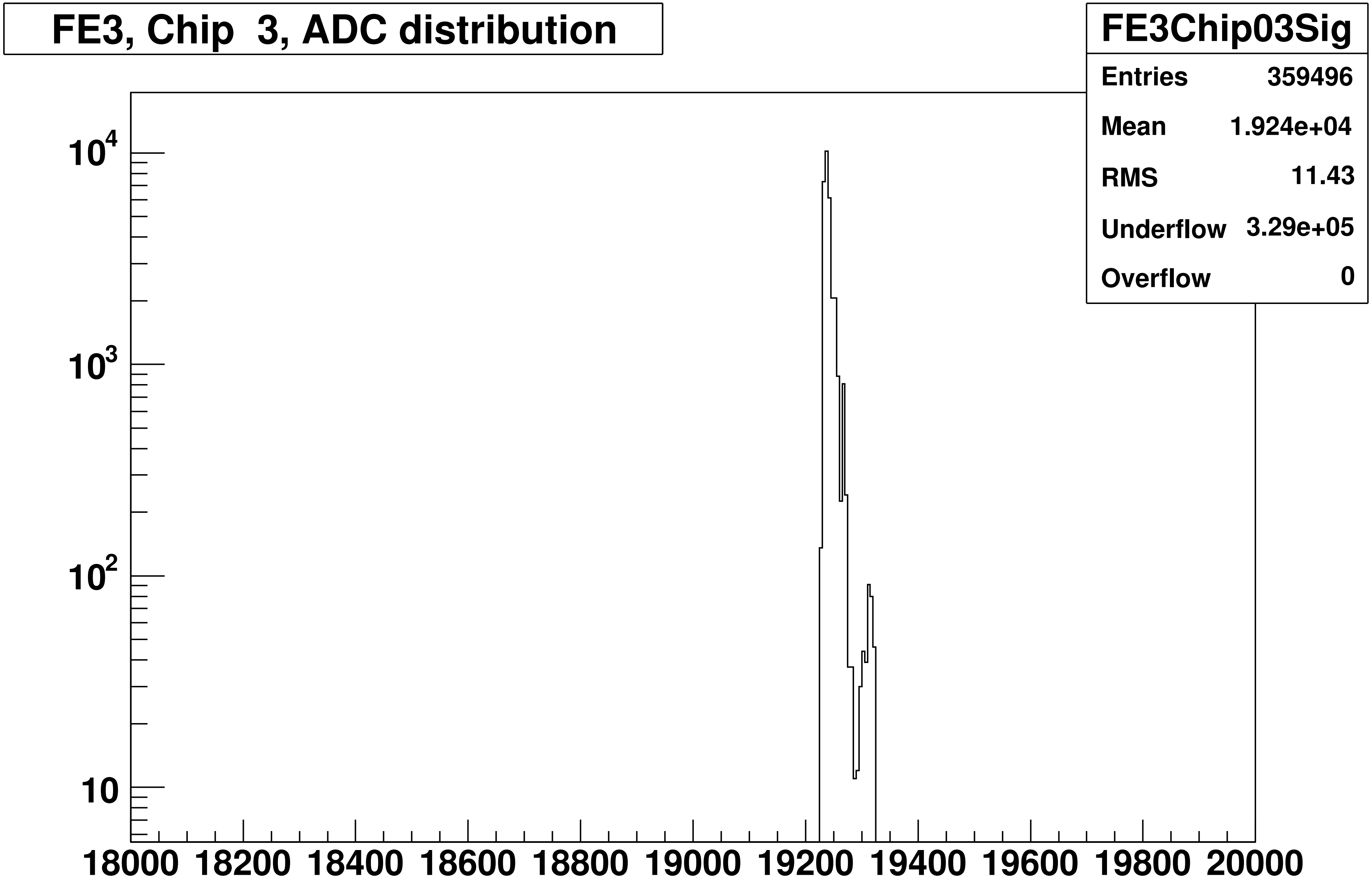
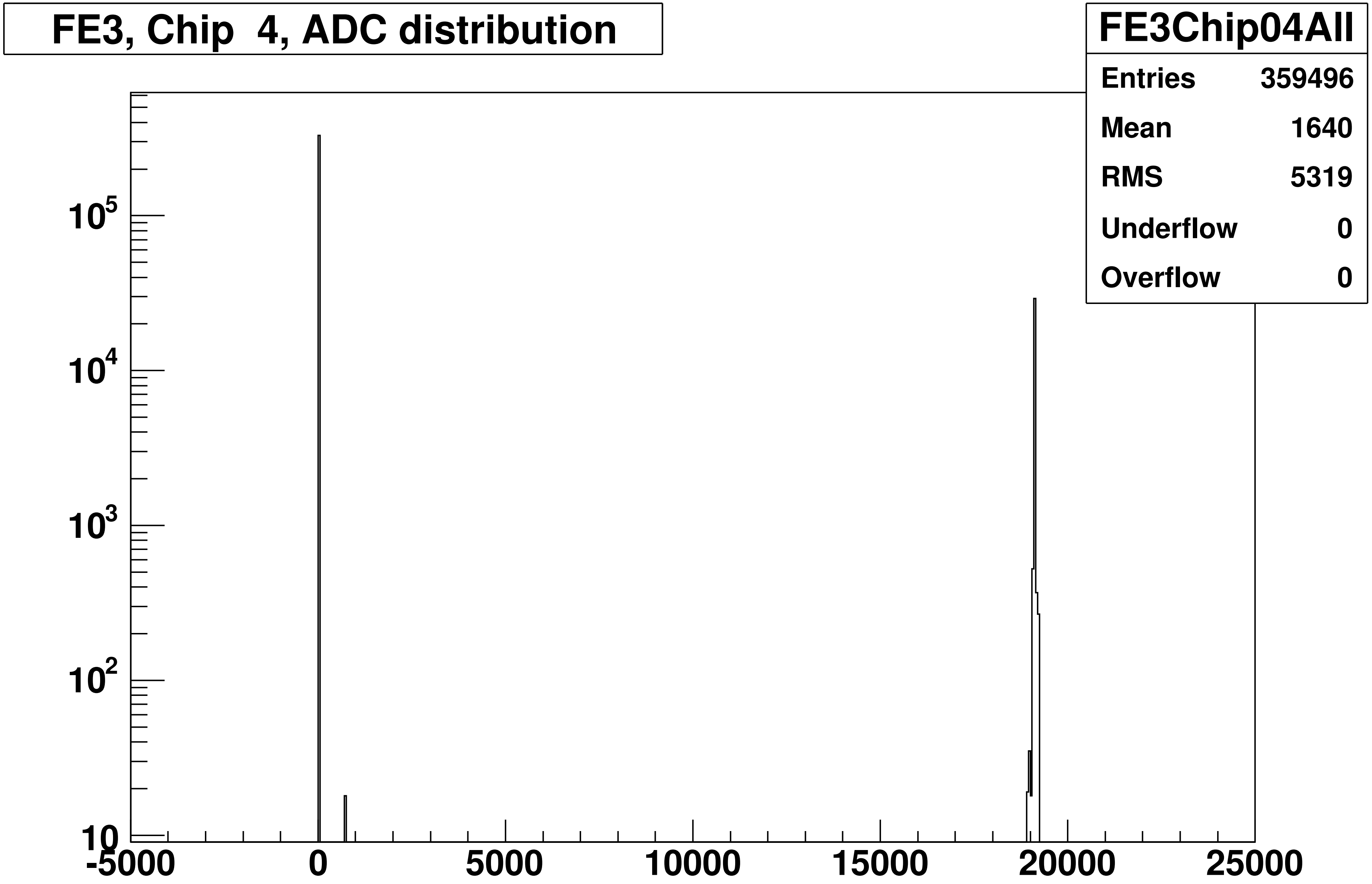
100
150
200


FE3, Chip 3, ADC distribution
FE3Chip03Sig
Entries 359496
Mean 1.924e+04
RMS 11.43
Underflow 3.29e+05
Overflow 0
10^4
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE3, Chip 4, ADC distribution
FE3Chip04All
Entries 359496
Mean 1640
RMS 5319
Underflow 0
Overflow 0
10
10^2
10^3
10^4
10^5
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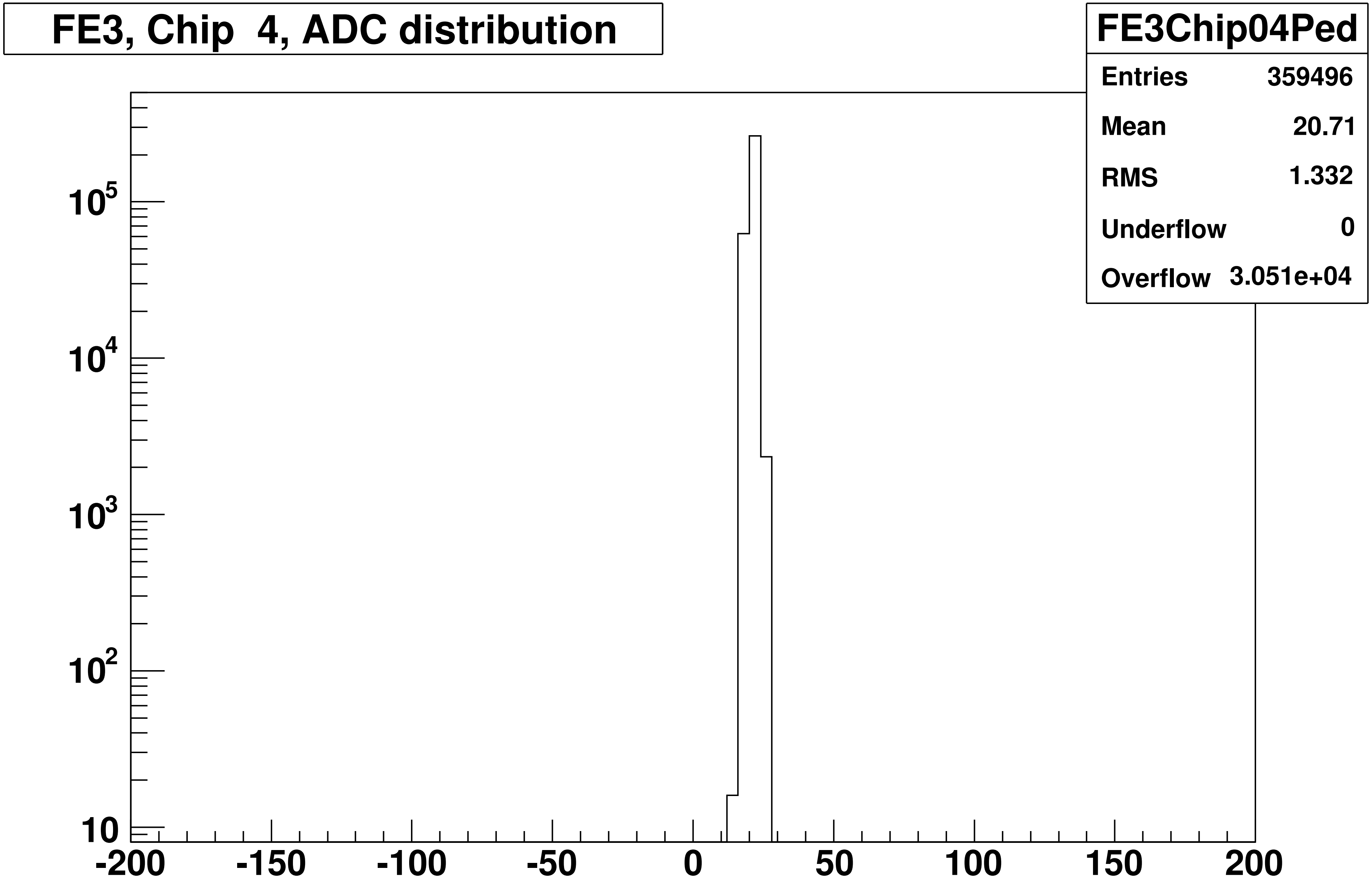
FE3, Chip 4, ADC distribution
FE3Chip04Ped
Entries 359496
Mean 20.71
RMS 1.332
Underflow 0
Overflow 3.051e+04
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10^4
10^3
10^2
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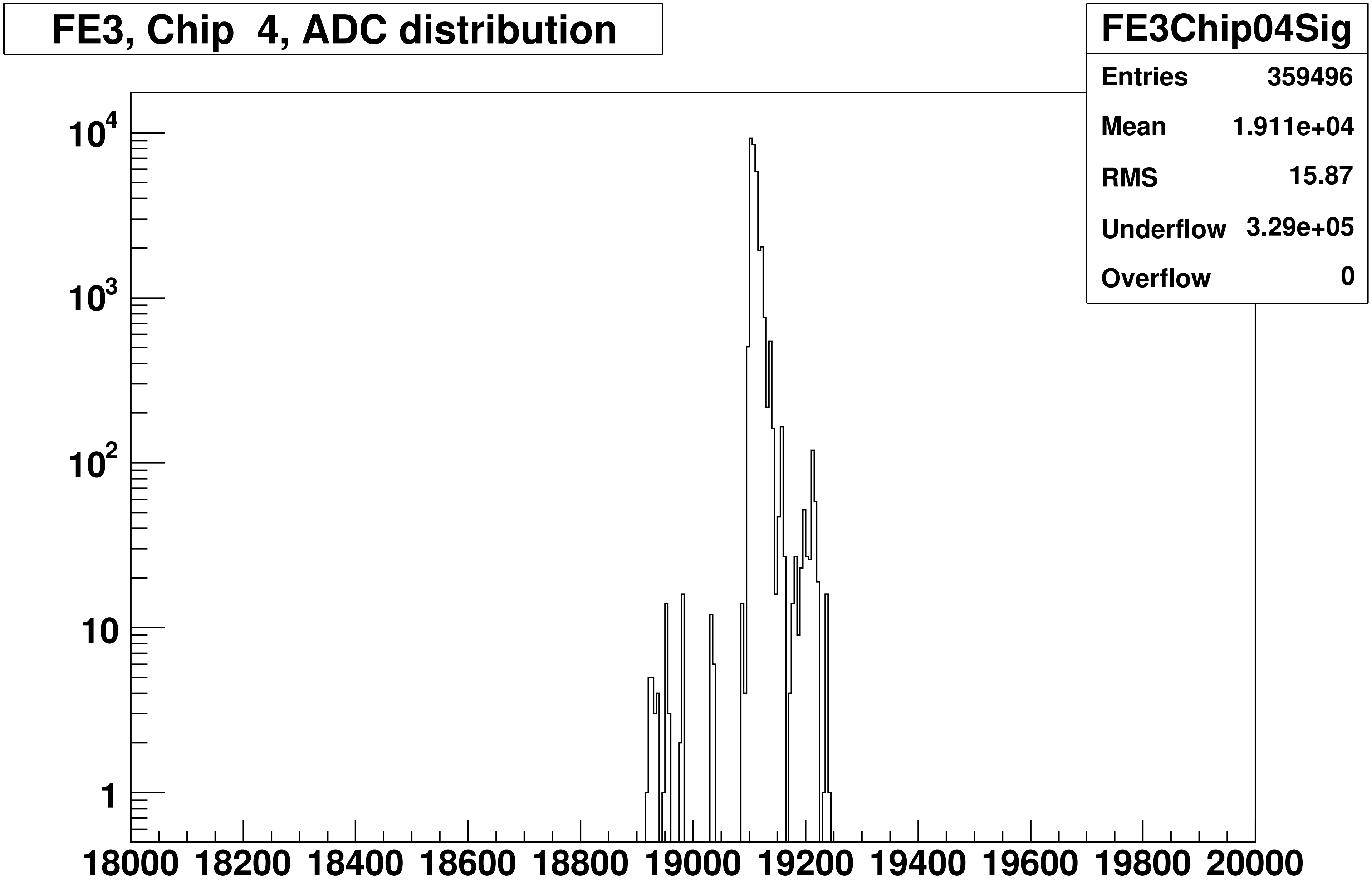
150
200


FE3, Chip 4, ADC distribution
FE3Chip04Sig
Entries 359496
Mean 1.911e+04
RMS 15.87
Underflow 3.29e+05
Overflow 0
10^4
10^3
10^2
10
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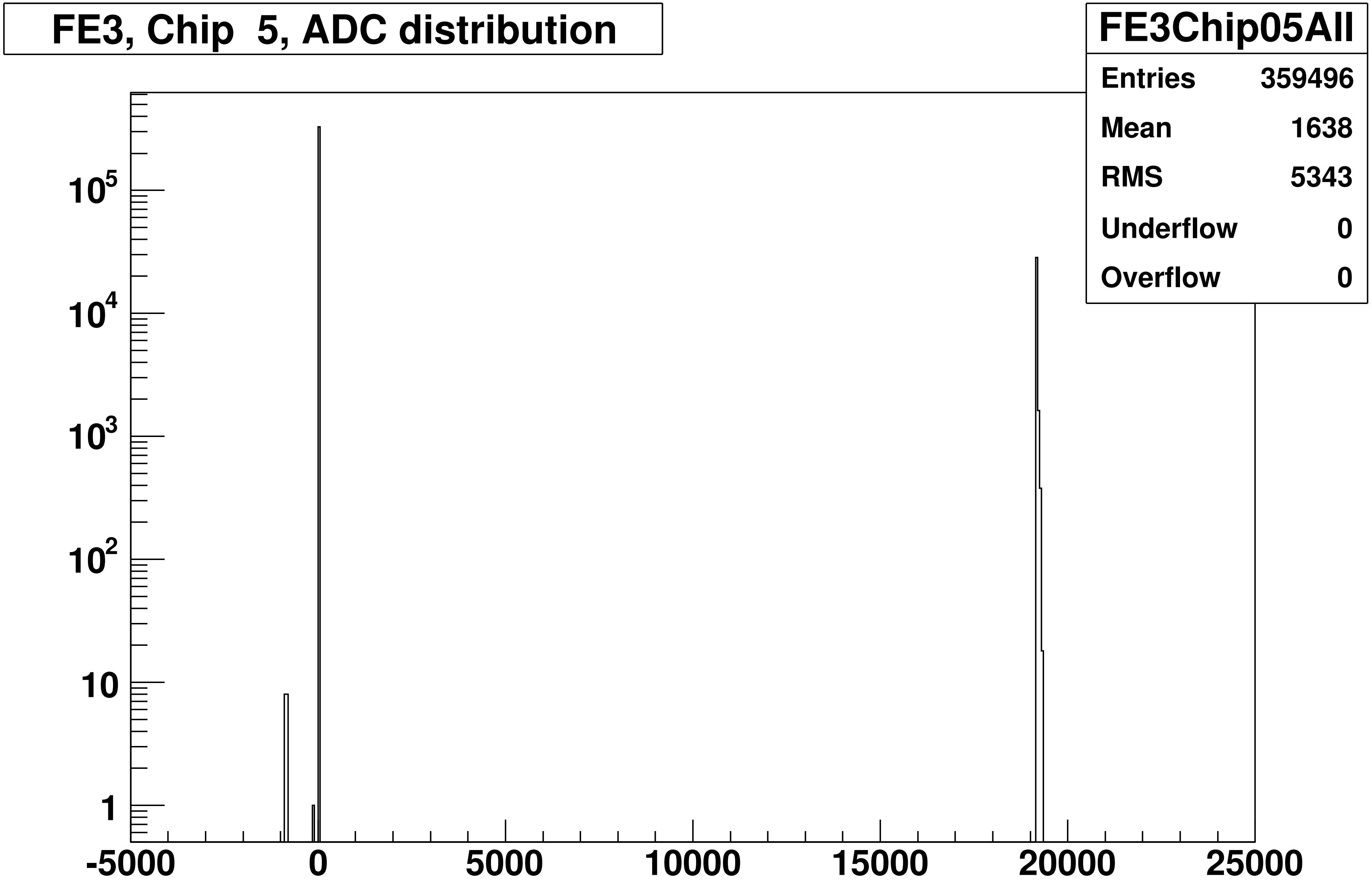

FE3, Chip 5, ADC distribution
FE3Chip05All
Entries 359496
Mean 1638
RMS 5343
Underflow 0
Overflow 0
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10
10^2
10^3
10^4
10^5
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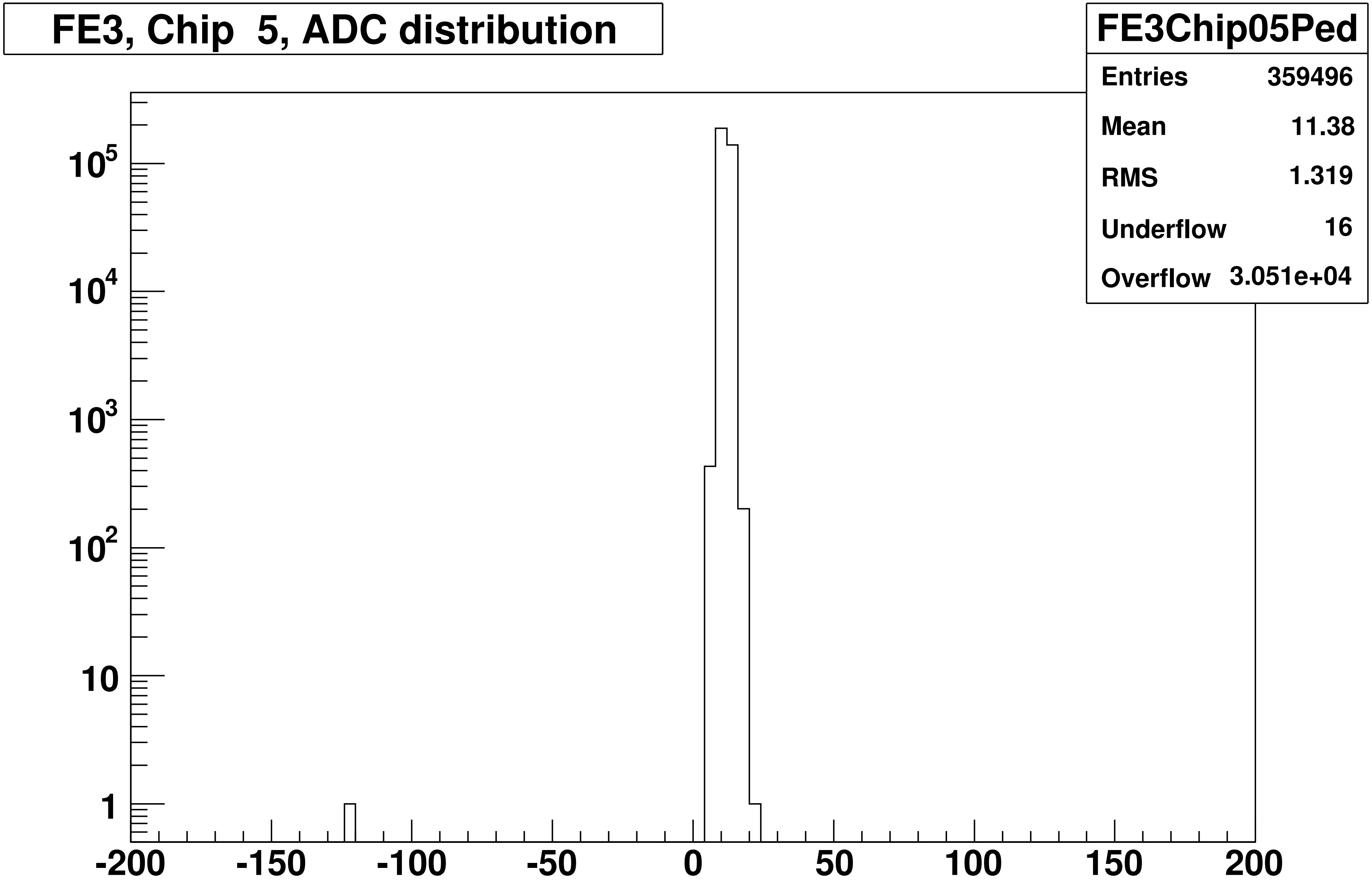
15000
20000
25000


FE3, Chip 5, ADC distribution
FE3Chip05Ped
Entries 359496
Mean 11.38
RMS 1.319
Underflow 16
Overflow 3.051e+04
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10^3
10^2
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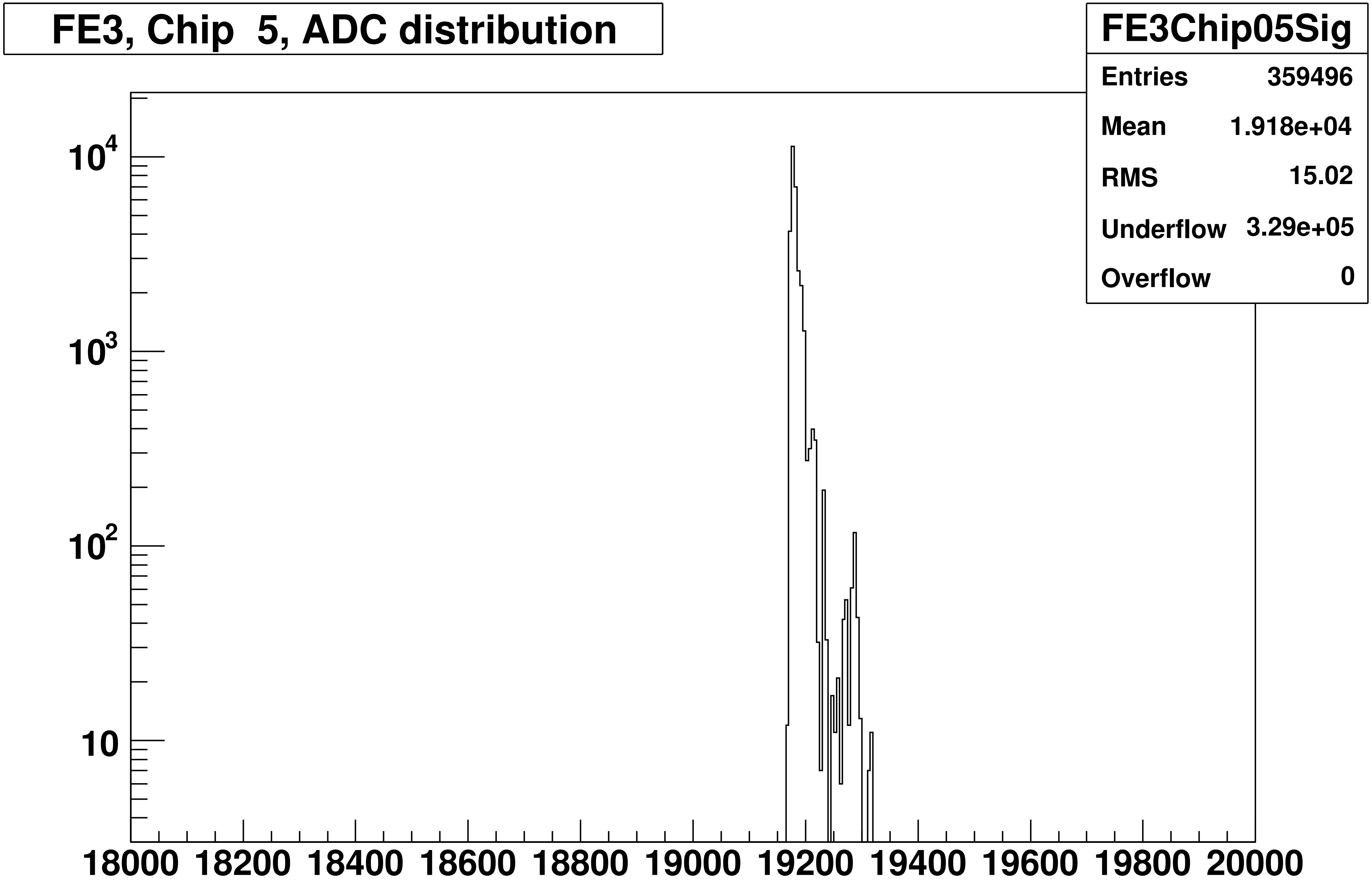
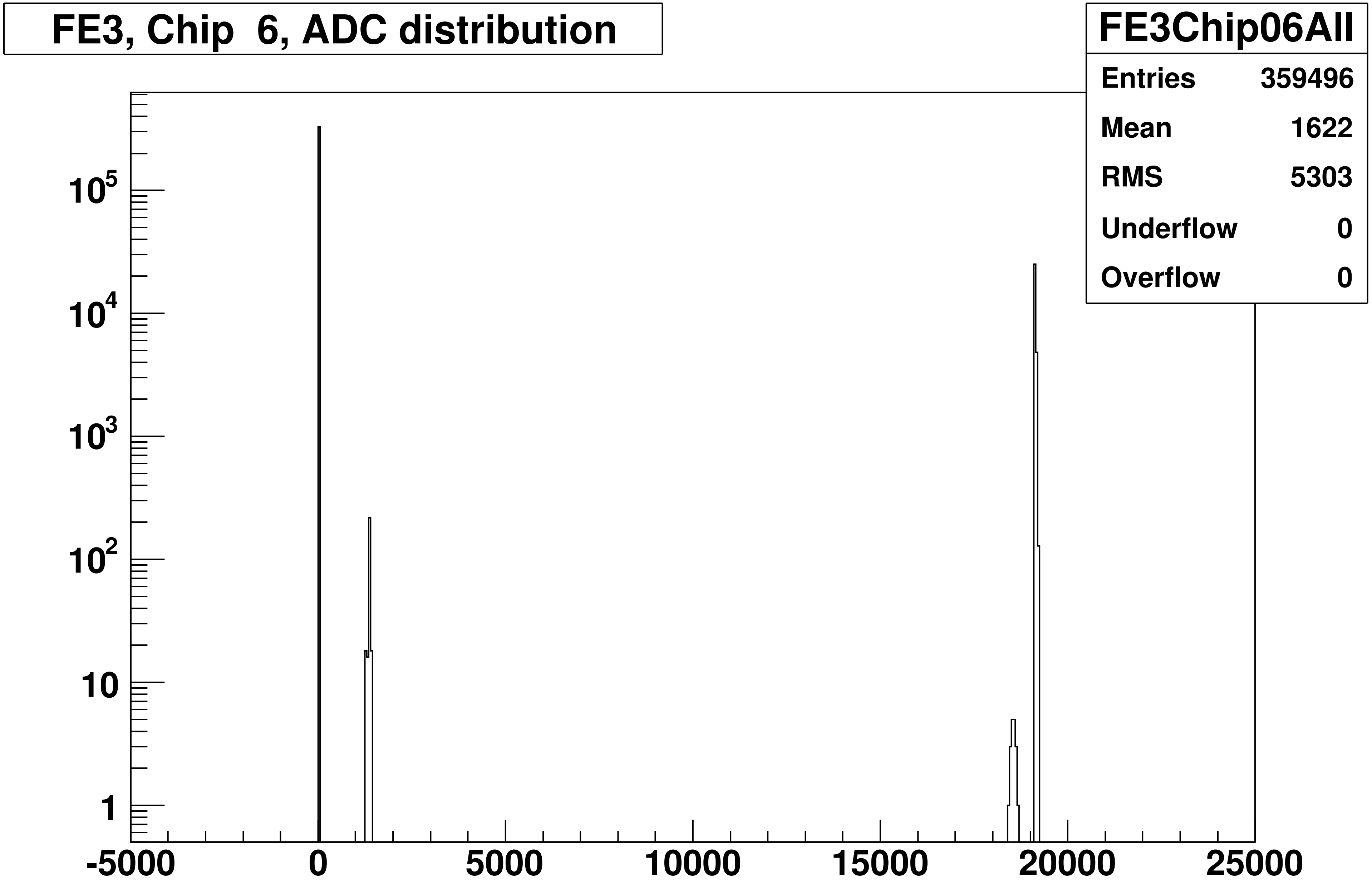

FE3, Chip 5, ADC distribution
FE3Chip05Sig
Entries 359496
Mean 1.918e+04
RMS 15.02
Underflow 3.29e+05
Overflow 0
10^4
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE3, Chip 6, ADC distribution
FE3Chip06All
Entries 359496
Mean 1622
RMS 5303
Underflow 0
Overflow 0
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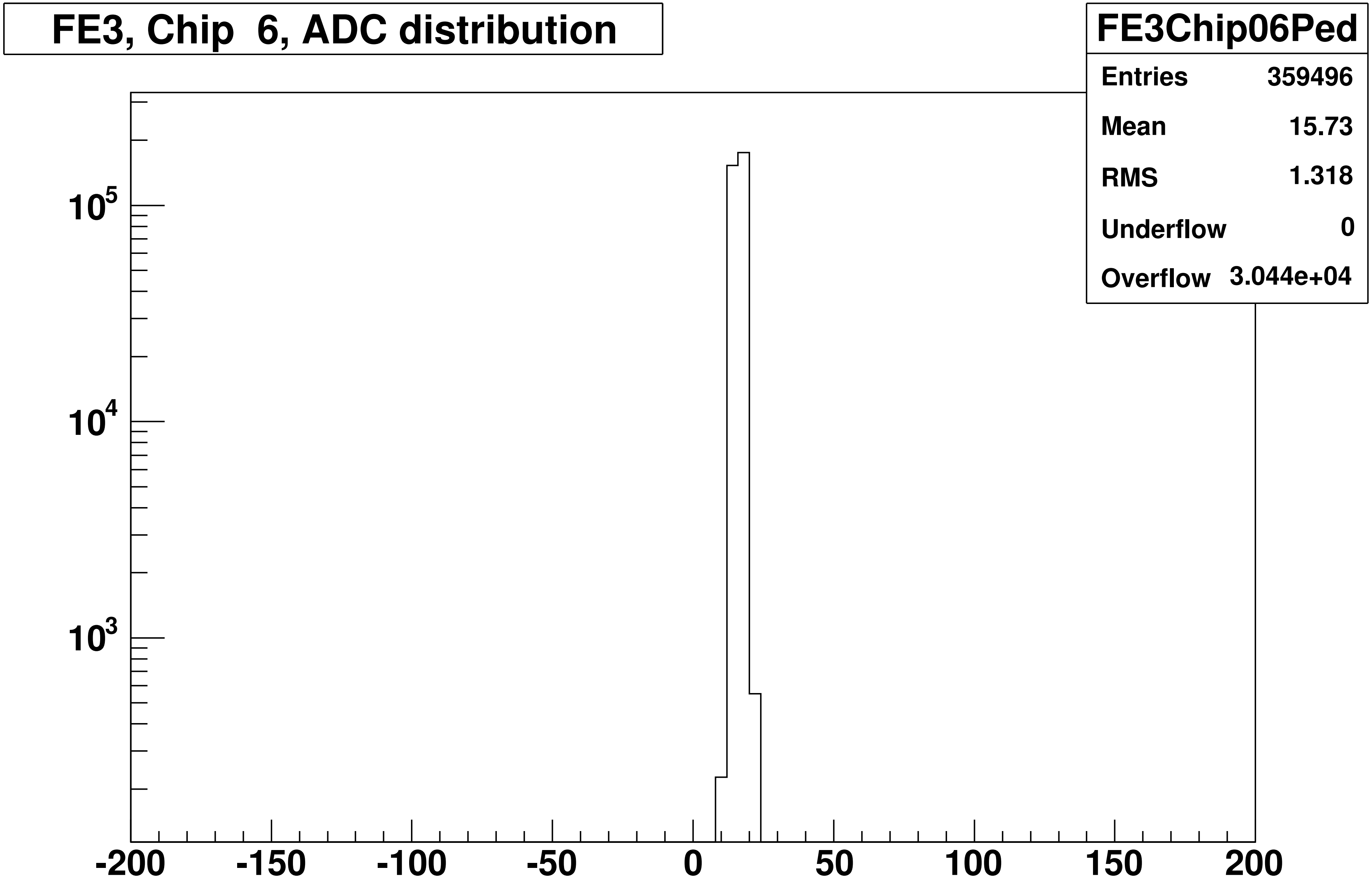
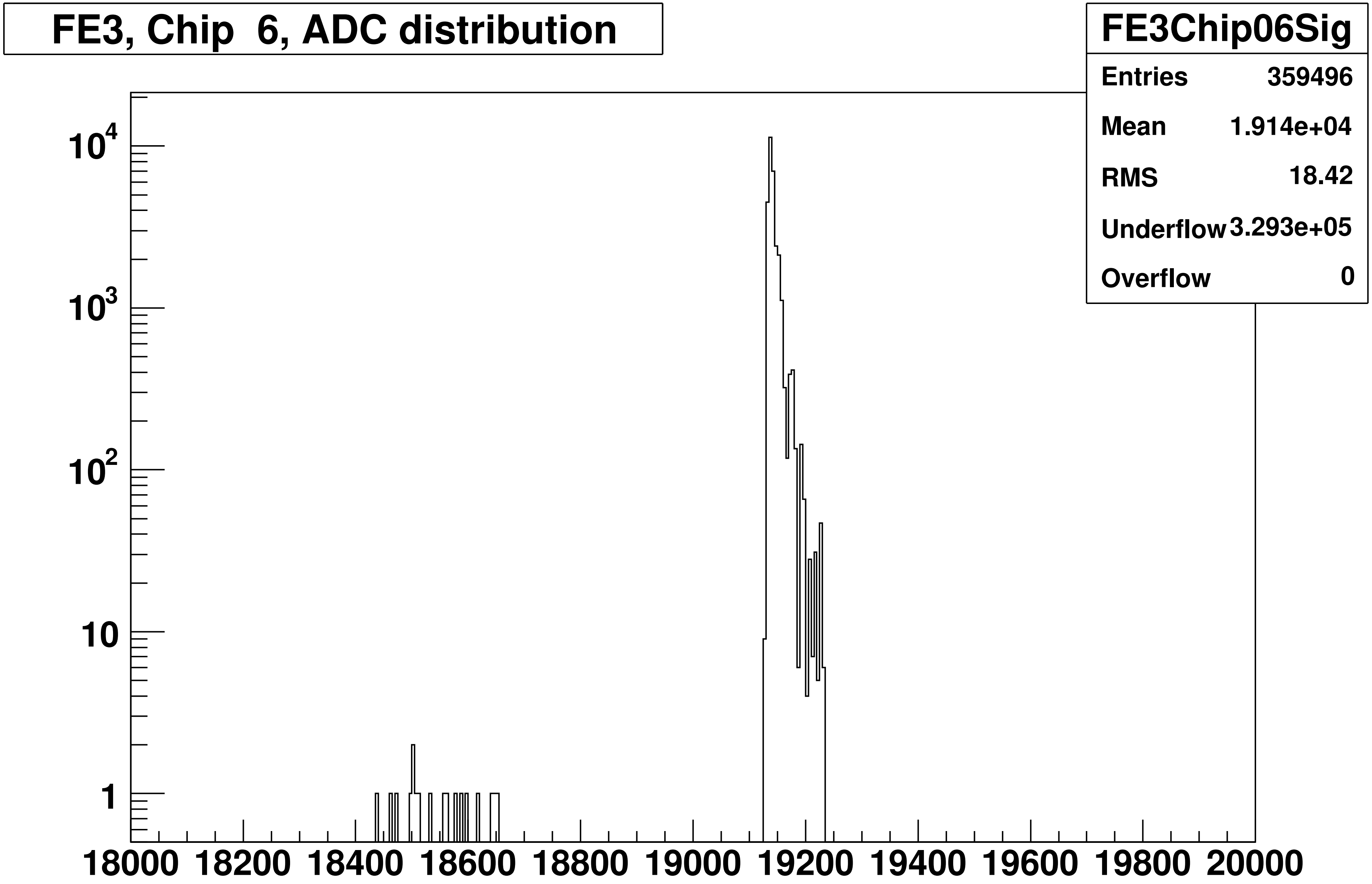
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE3, Chip 6, ADC distribution
FE3Chip06Ped
Entries 359496
Mean 15.73
RMS 1.318
Underflow 0
Overflow 3.044e+04
10^5
10^4
10^3
-200 -150 -100 -50 0 50 100 150 200


FE3, Chip 6, ADC distribution
FE3Chip06Sig
Entries 359496
Mean 1.914e+04
RMS 18.42
Underflow 3.293e+05
Overflow 0
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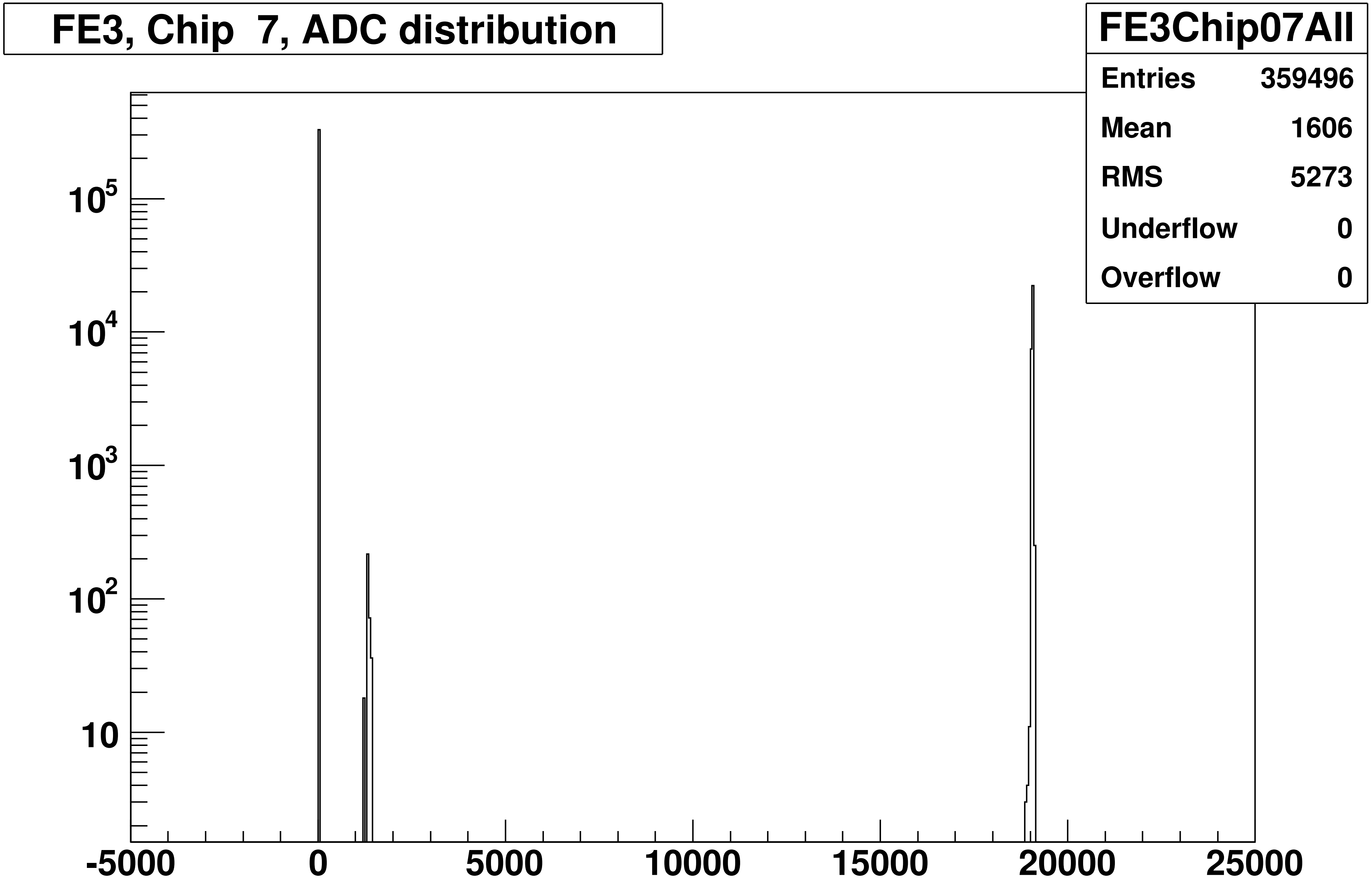
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE3, Chip 7, ADC distribution
FE3Chip07All
Entries 359496
Mean 1606
RMS 5273
Underflow 0
Overflow 0
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10^4
10^3
10^2
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-5000
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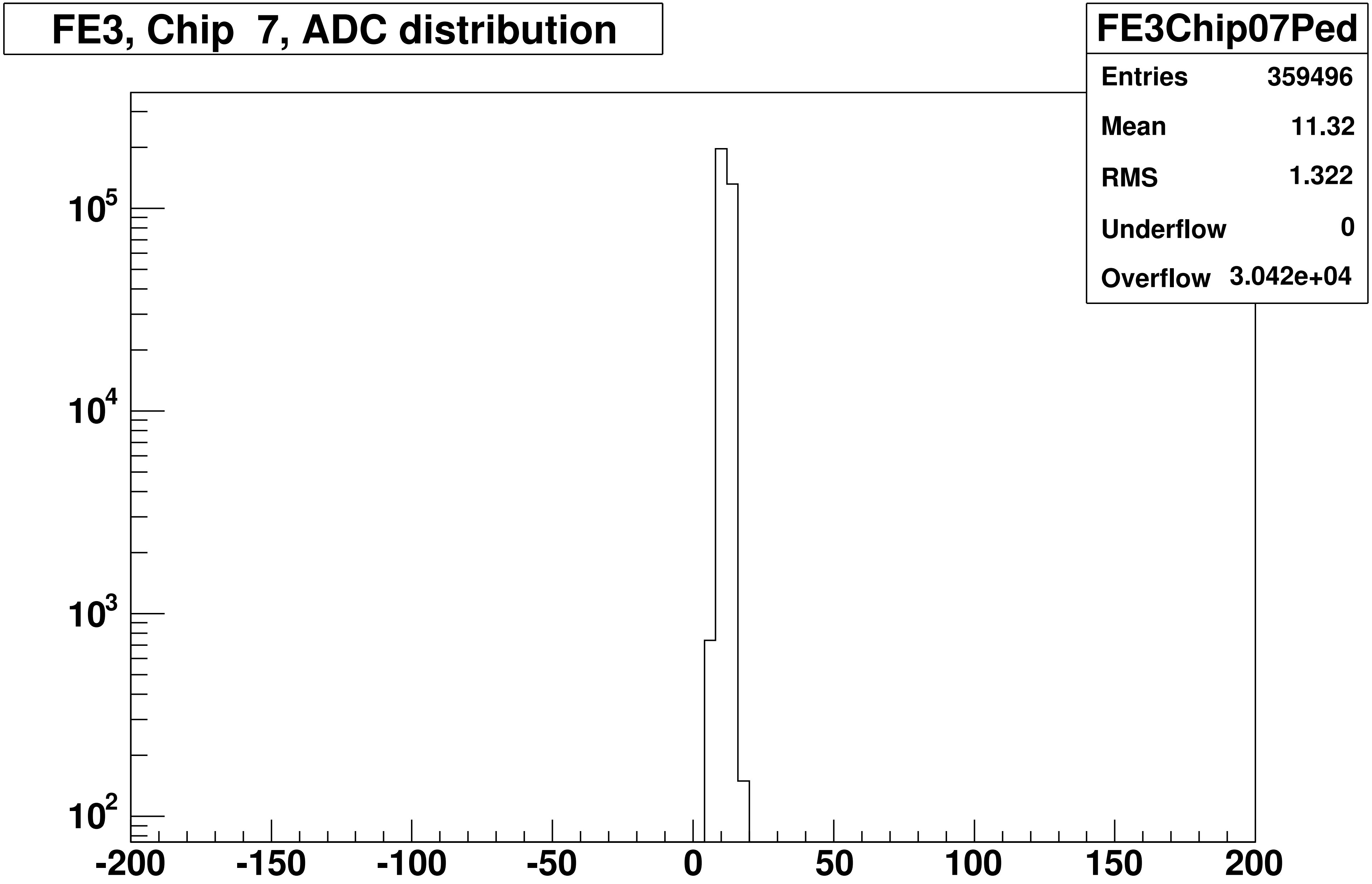
10000
15000
20000
25000


FE3, Chip 7, ADC distribution
FE3Chip07Ped
Entries 359496
Mean 11.32
RMS 1.322
Underflow 0
Overflow 3.042e+04
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10^4
10^3
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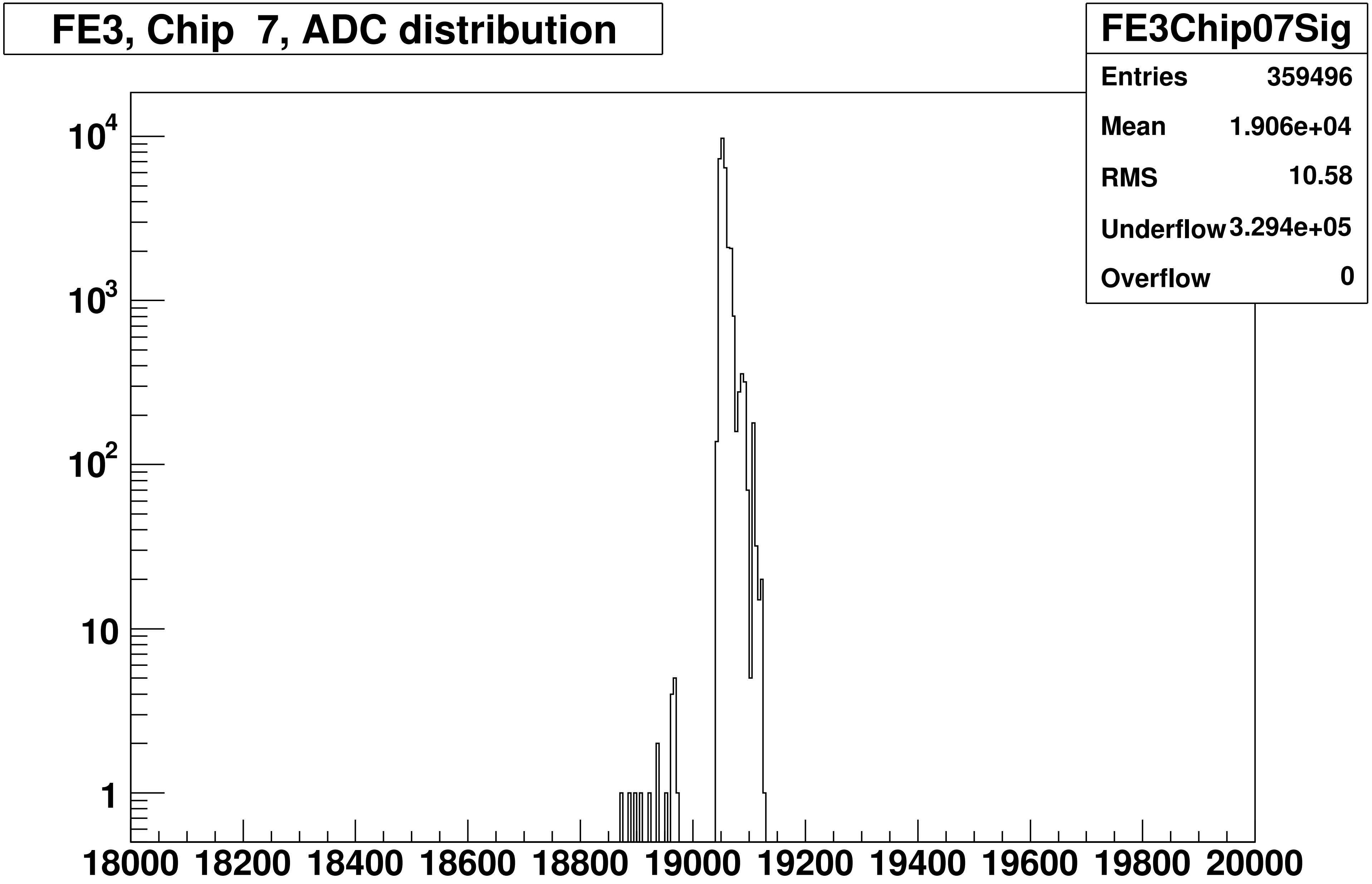

FE3, Chip 7, ADC distribution
FE3Chip07Sig
Entries 359496
Mean 1.906e+04
RMS 10.58
Underflow 3.294e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
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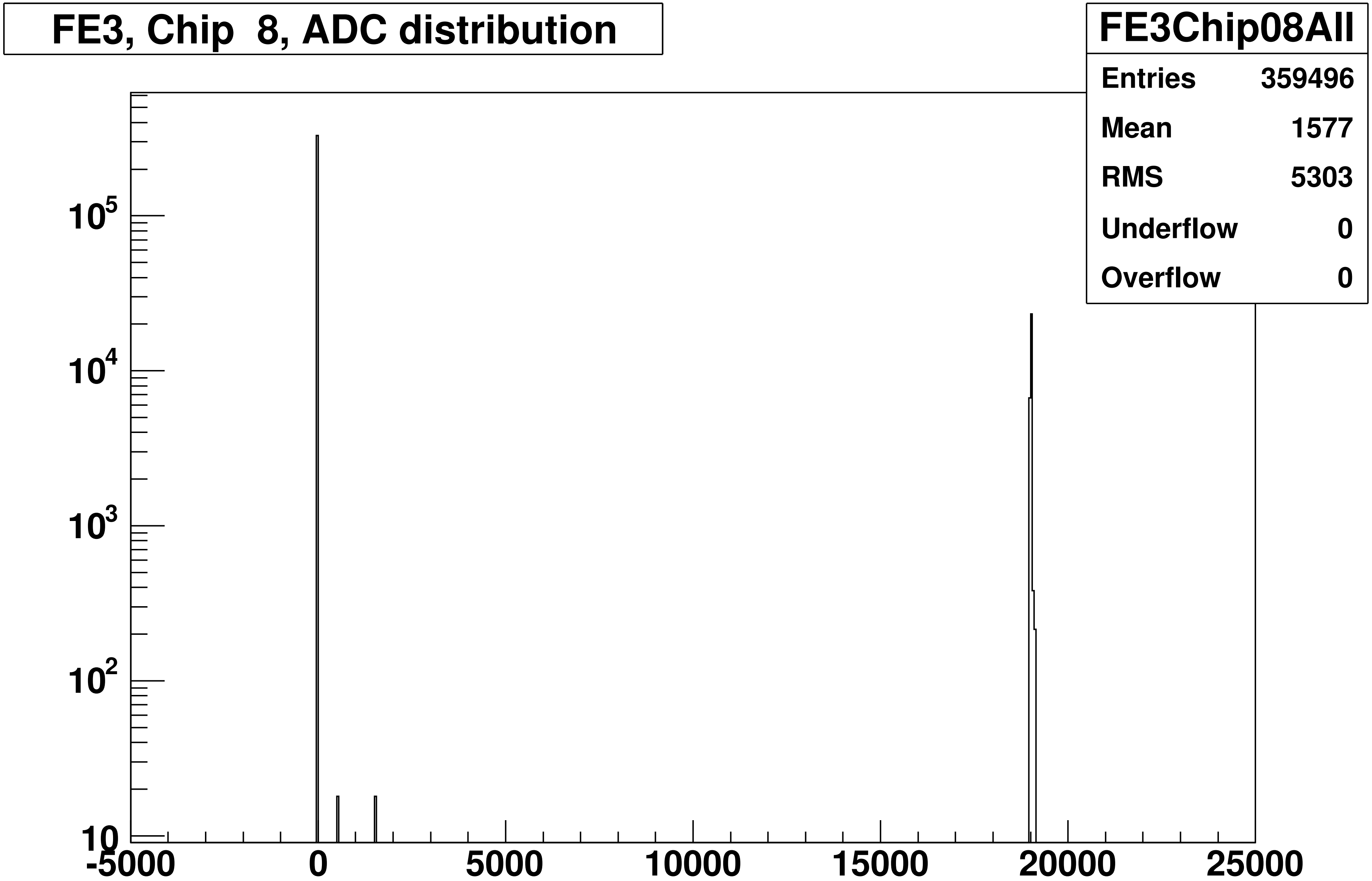
19400
19600
19800
20000


FE3, Chip 8, ADC distribution
FE3Chip08All
Entries 359496
Mean 1577
RMS 5303
Underflow 0
Overflow 0
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10^2
10^3
10^4
10^5
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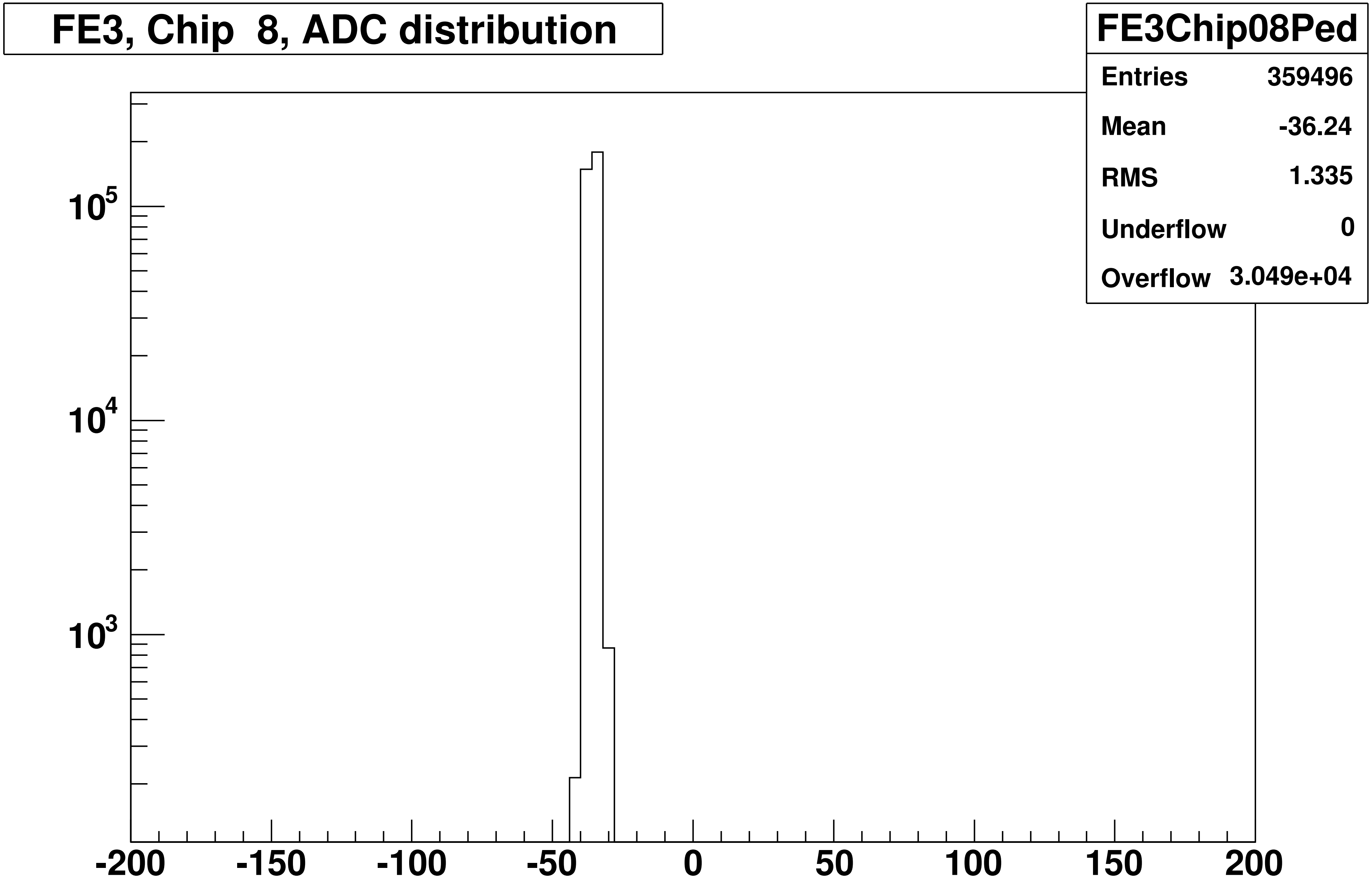
10000
15000
20000
25000


FE3, Chip 8, ADC distribution
FE3Chip08Ped
Entries 359496
Mean -36.24
RMS 1.335
Underflow 0
Overflow 3.049e+04
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10^4
10^3
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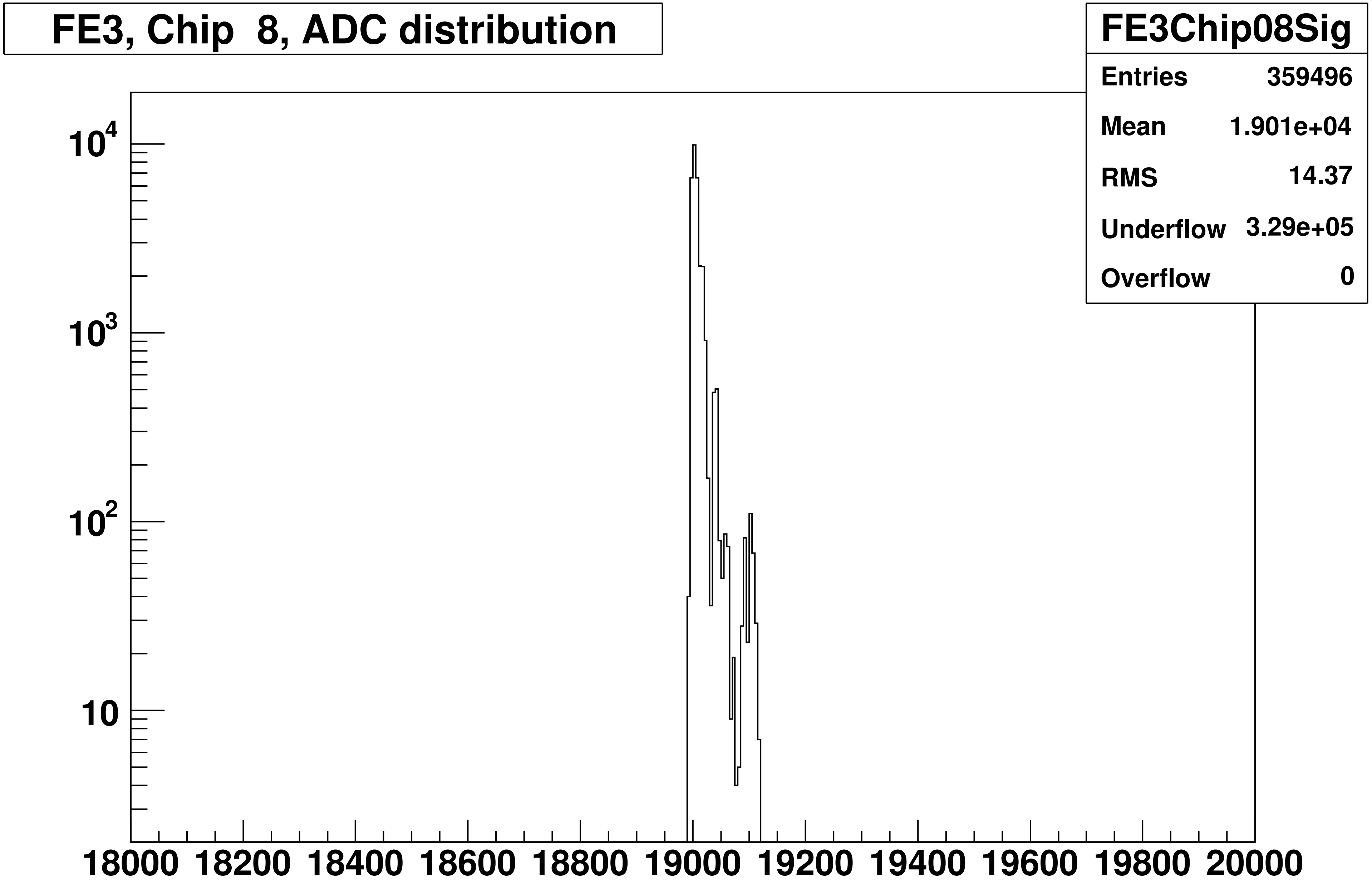
FE3, Chip 8, ADC distribution
FE3Chip08Sig
Entries 359496
Mean 1.901e+04
RMS 14.37
Underflow 3.29e+05
Overflow 0
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10^3
10^2
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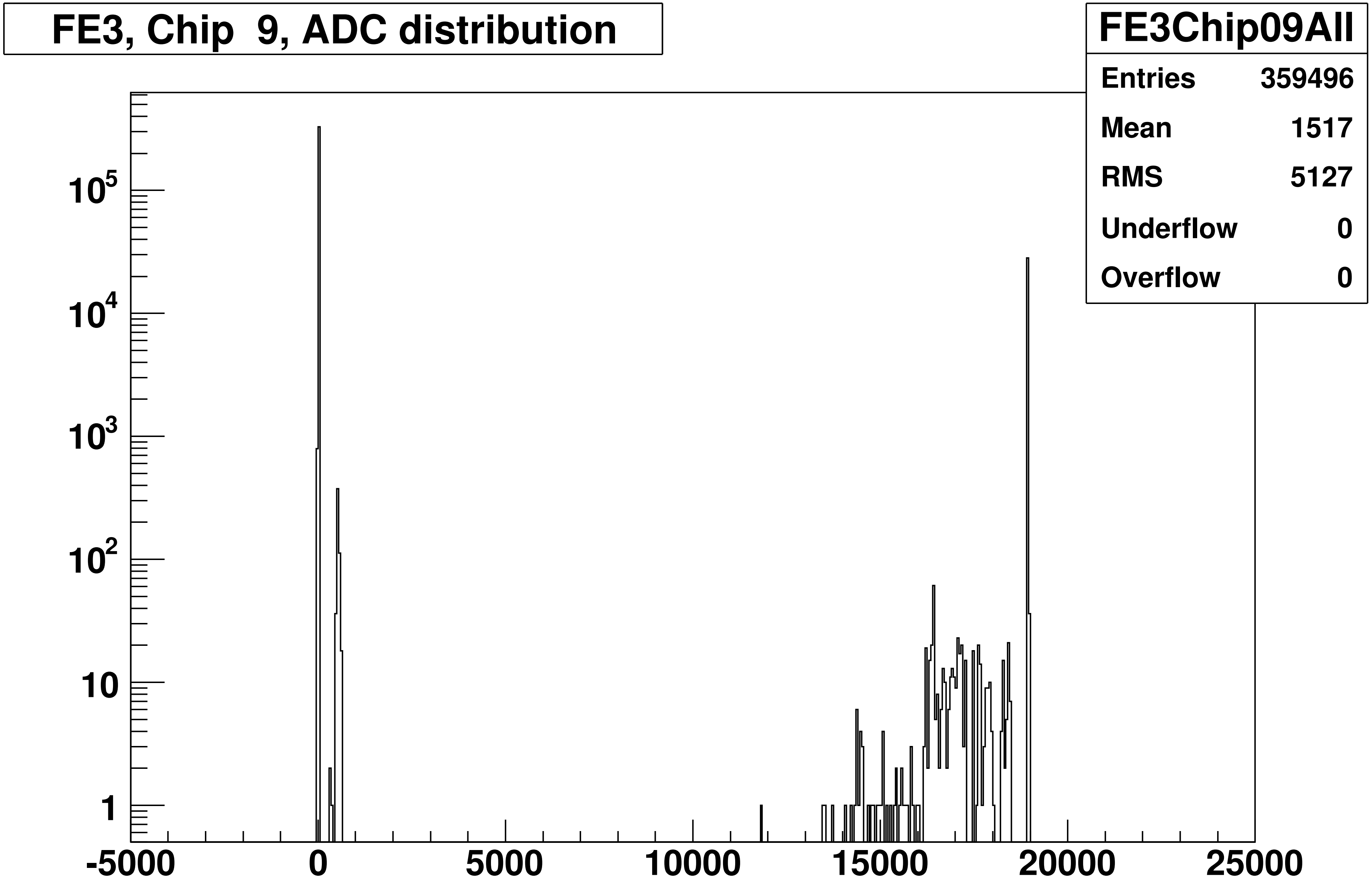
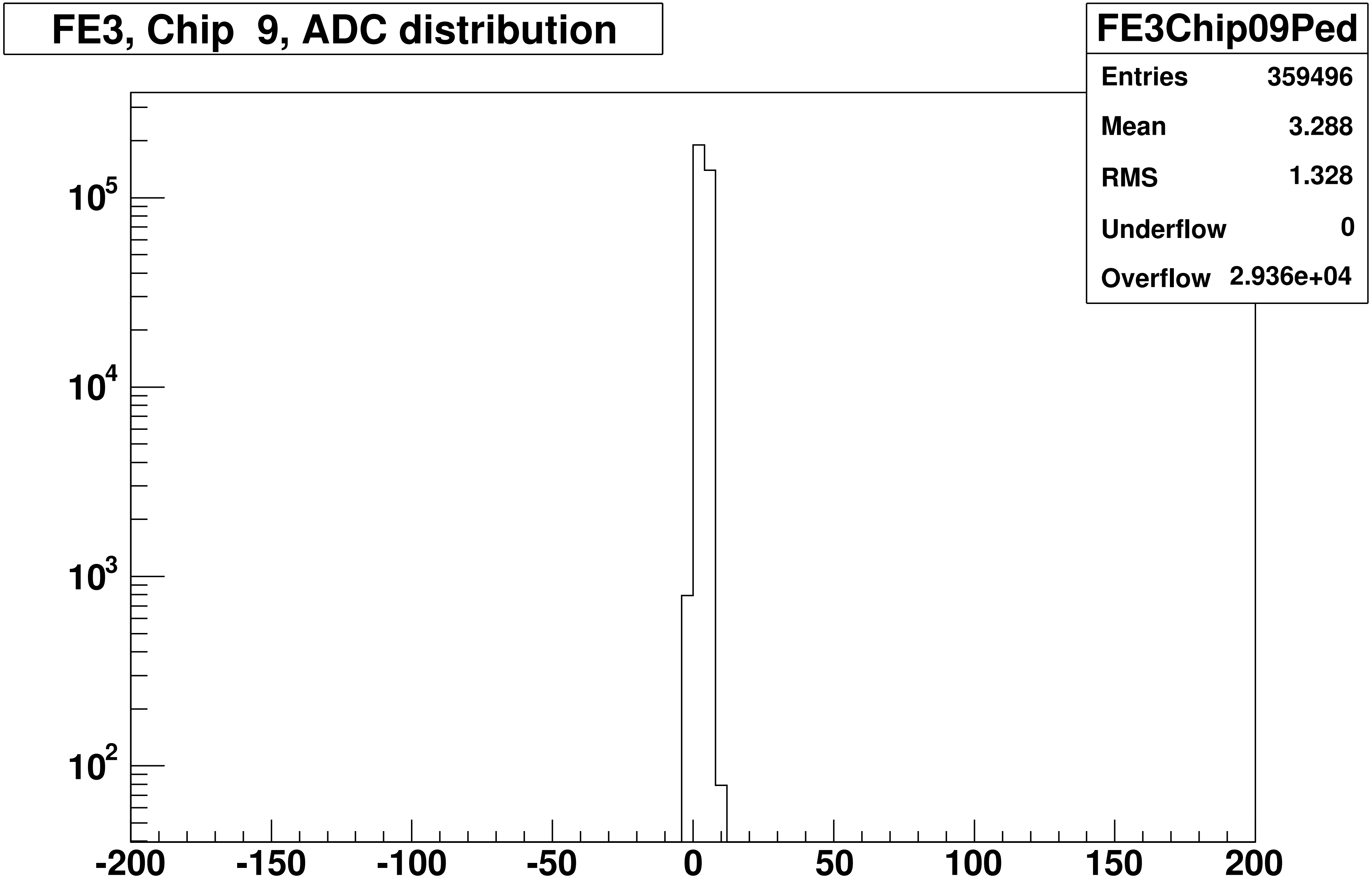
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE3, Chip 9, ADC distribution
FE3Chip09All
Entries 359496
Mean 1517
RMS 5127
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE3, Chip 9, ADC distribution
FE3Chip09Ped
Entries 359496
Mean 3.288
RMS 1.328
Underflow 0
Overflow 2.936e+04
10^5
10^4
10^3
10^2
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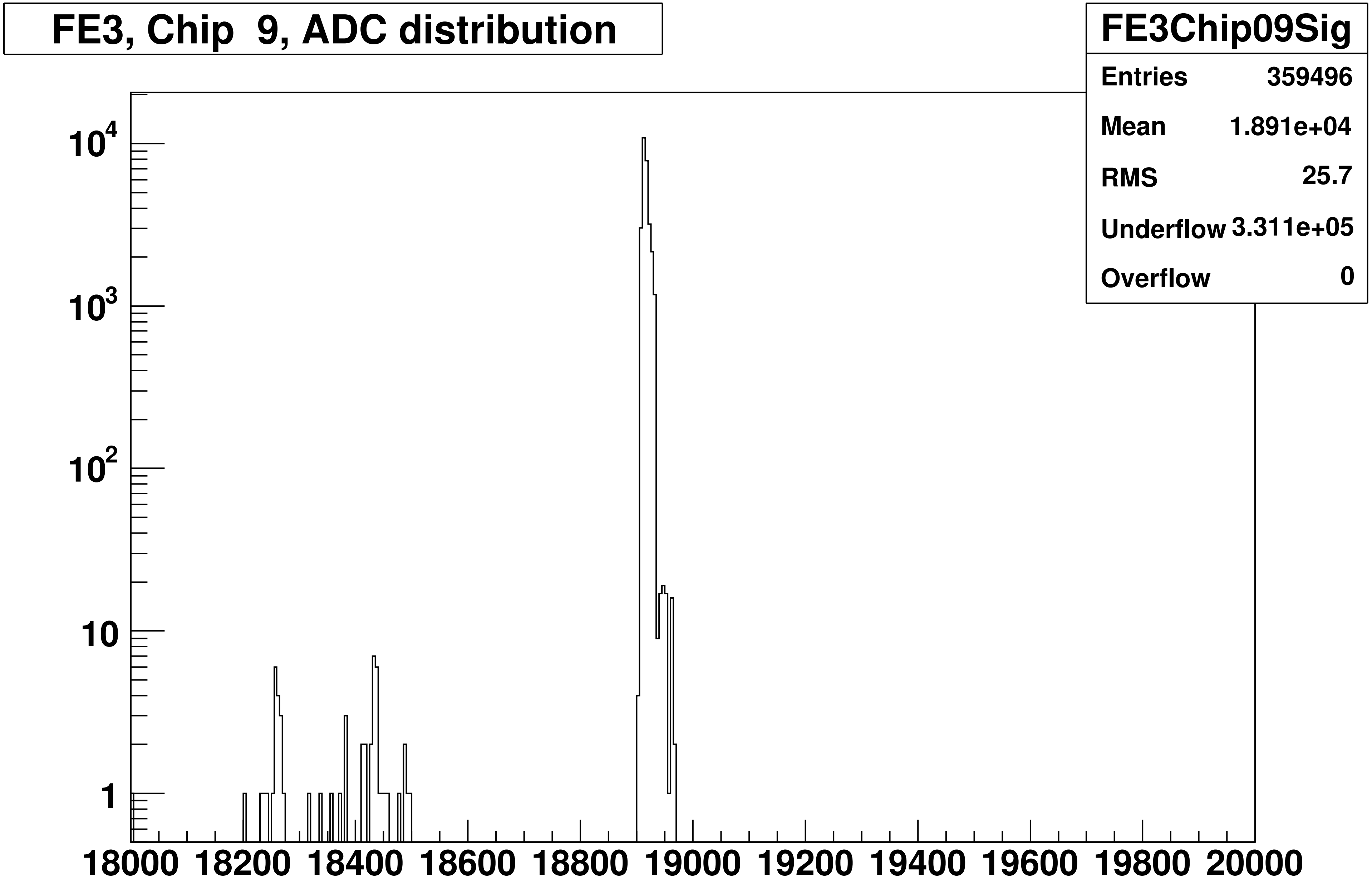
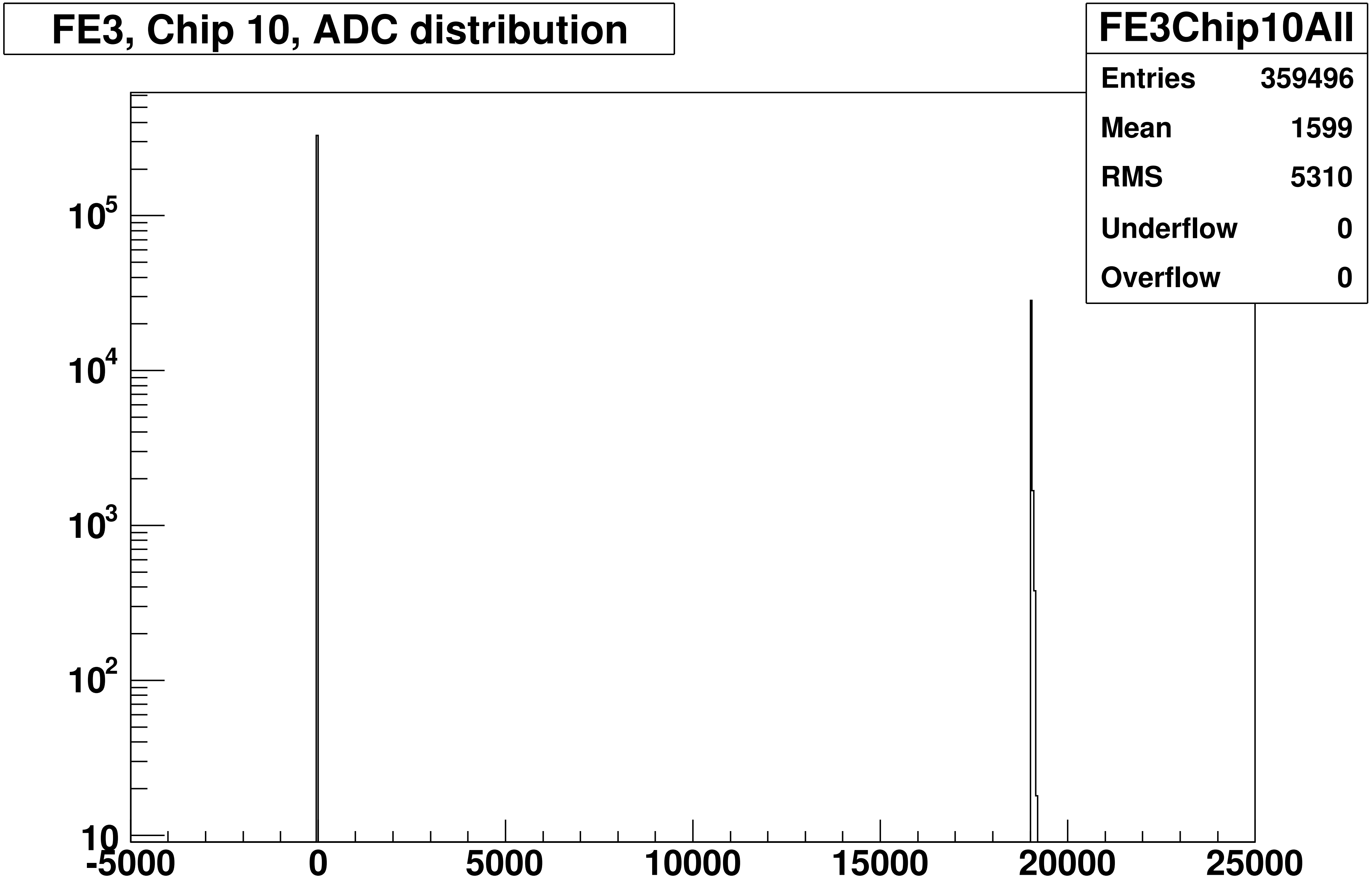
100
150
200



FE3, Chip 9, ADC distribution
FE3Chip09Sig
Entries 359496
Mean 1.891e+04
RMS 25.7
Underflow 3.311e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000



FE3, Chip 10, ADC distribution
FE3Chip10All
Entries 359496
Mean 1599
RMS 5310
Underflow 0
Overflow 0
10
10^2
10^3
10^4
10^5
-5000
0
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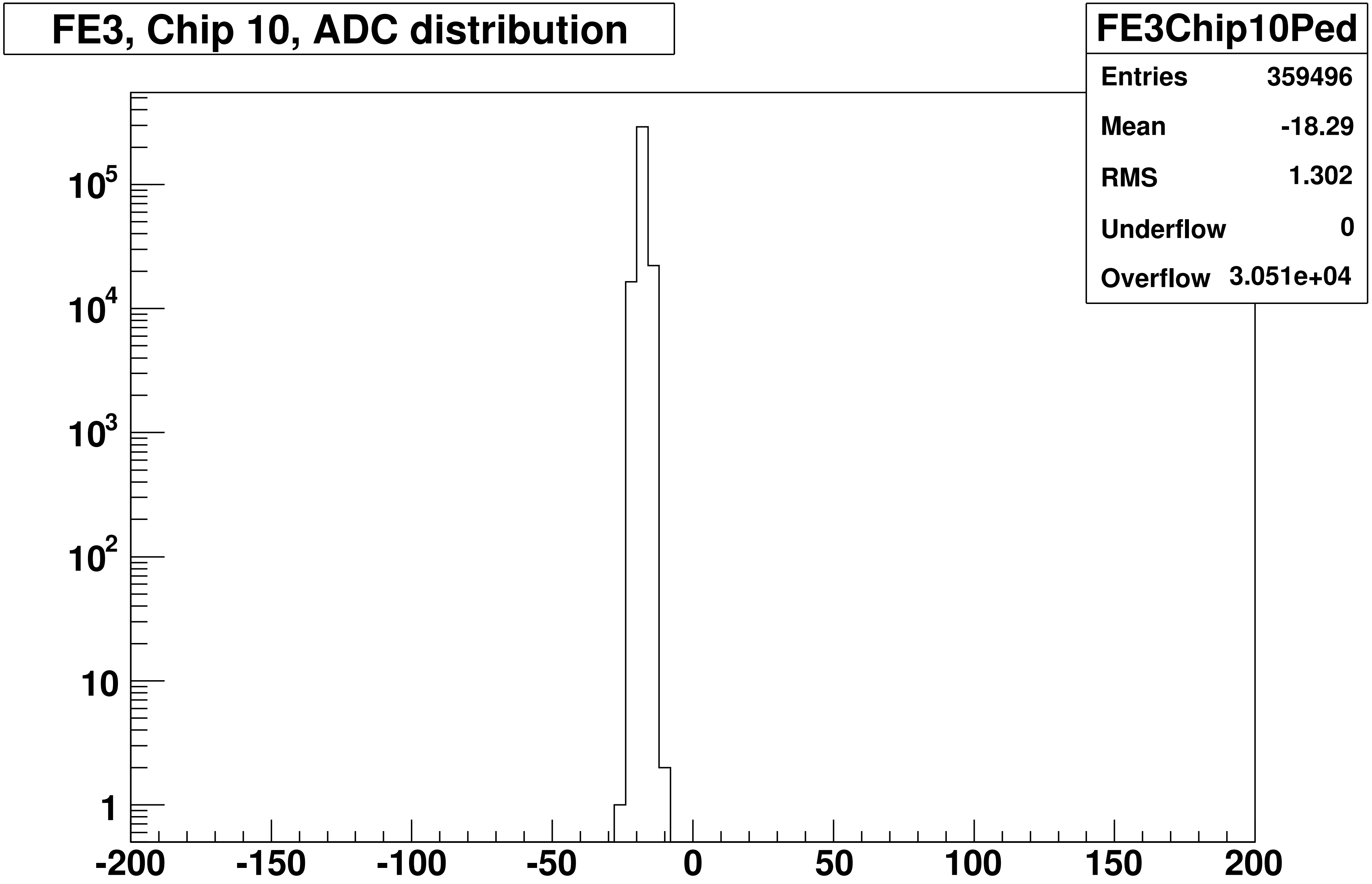
10000
15000
20000
25000


FE3, Chip 10, ADC distribution
FE3Chip10Ped
Entries 359496
Mean -18.29
RMS 1.302
Underflow 0
Overflow 3.051e+04
10^5
10^4
10^3
10^2
10
1
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-100
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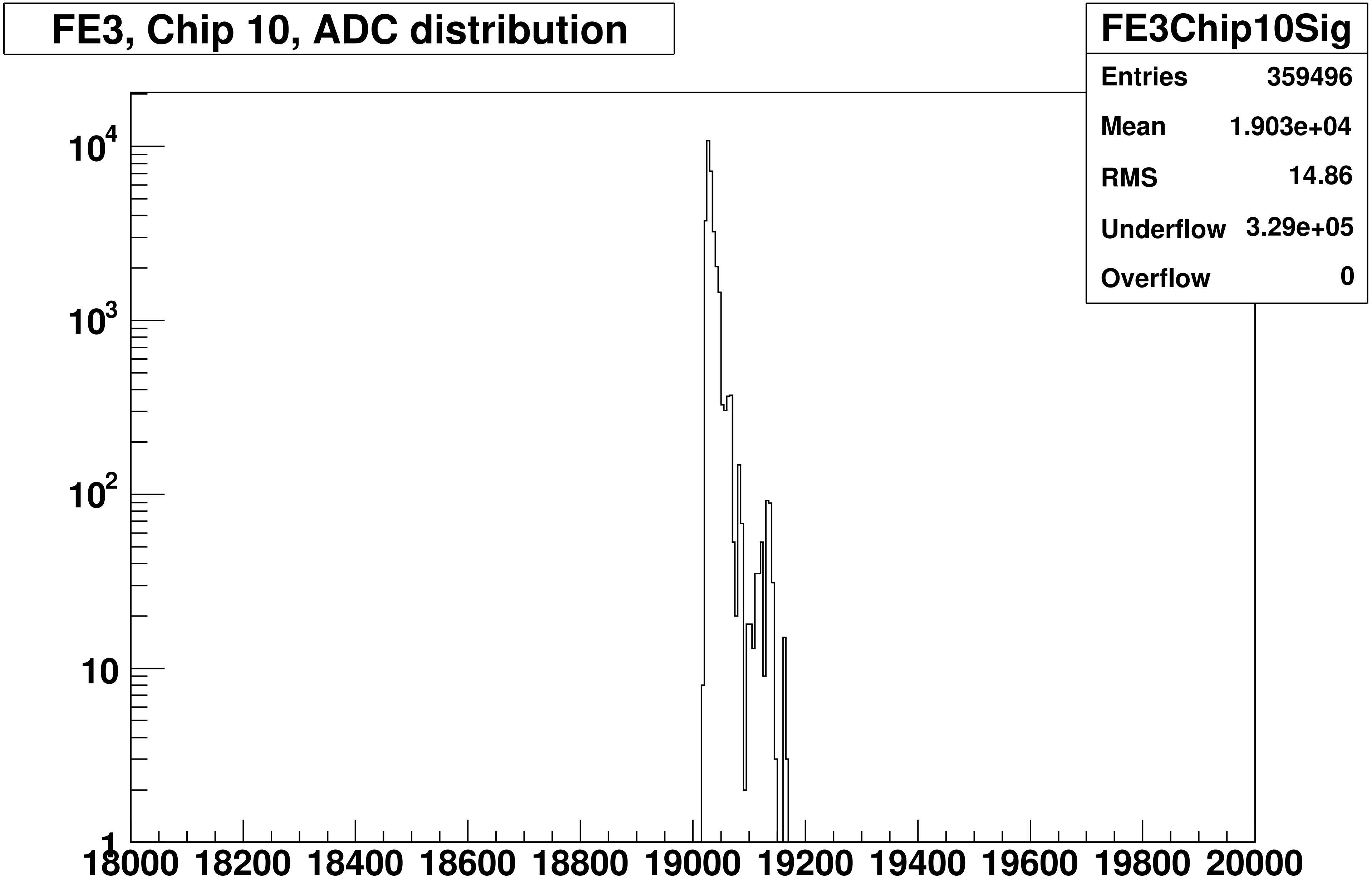
150
200


FE3, Chip 10, ADC distribution
FE3Chip10Sig
Entries 359496
Mean 1.903e+04
RMS 14.86
Underflow 3.29e+05
Overflow 0
10^4
10^3
10^2
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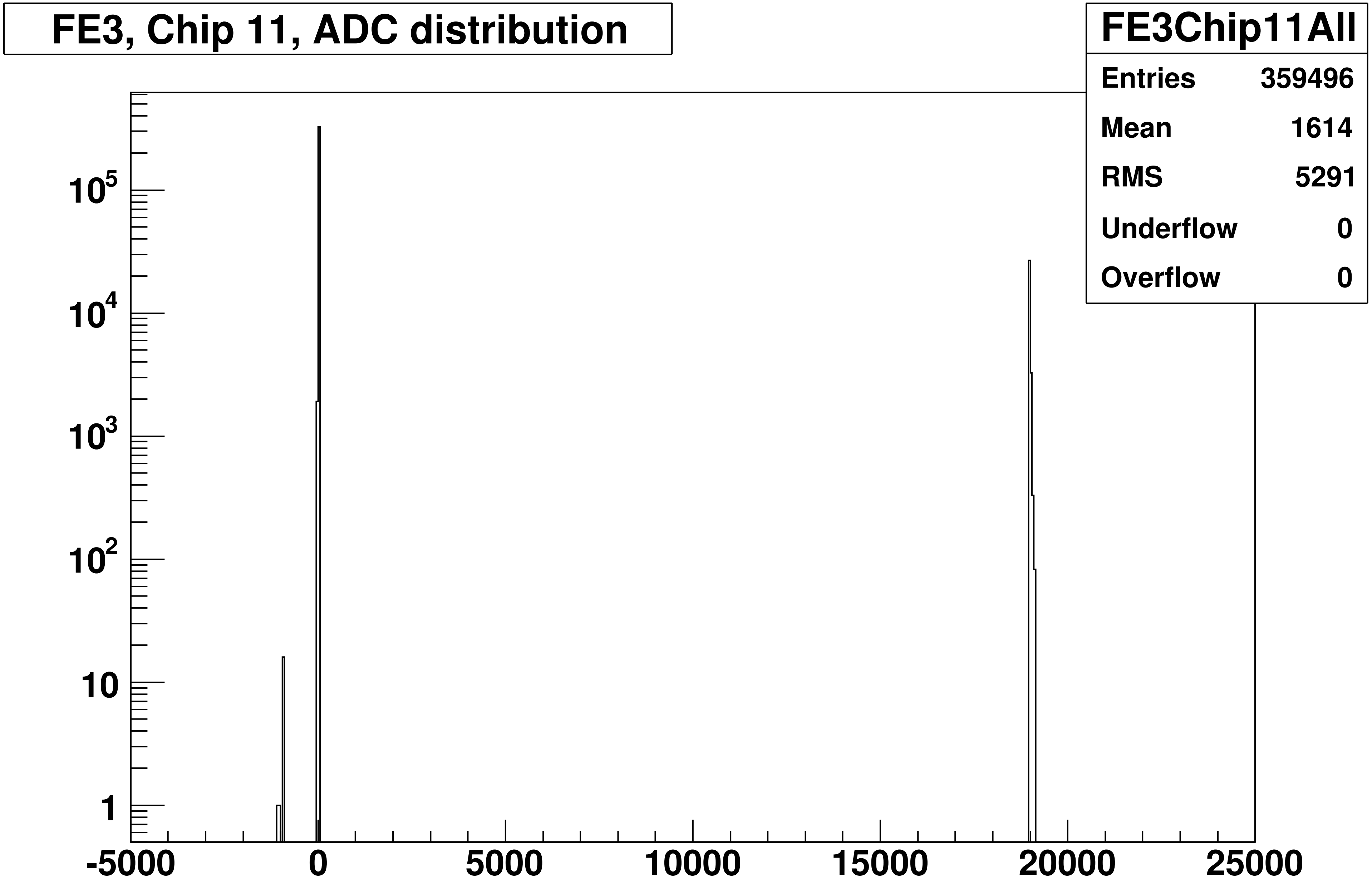
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE3, Chip 11, ADC distribution
FE3Chip11All
Entries 359496
Mean 1614
RMS 5291
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
1
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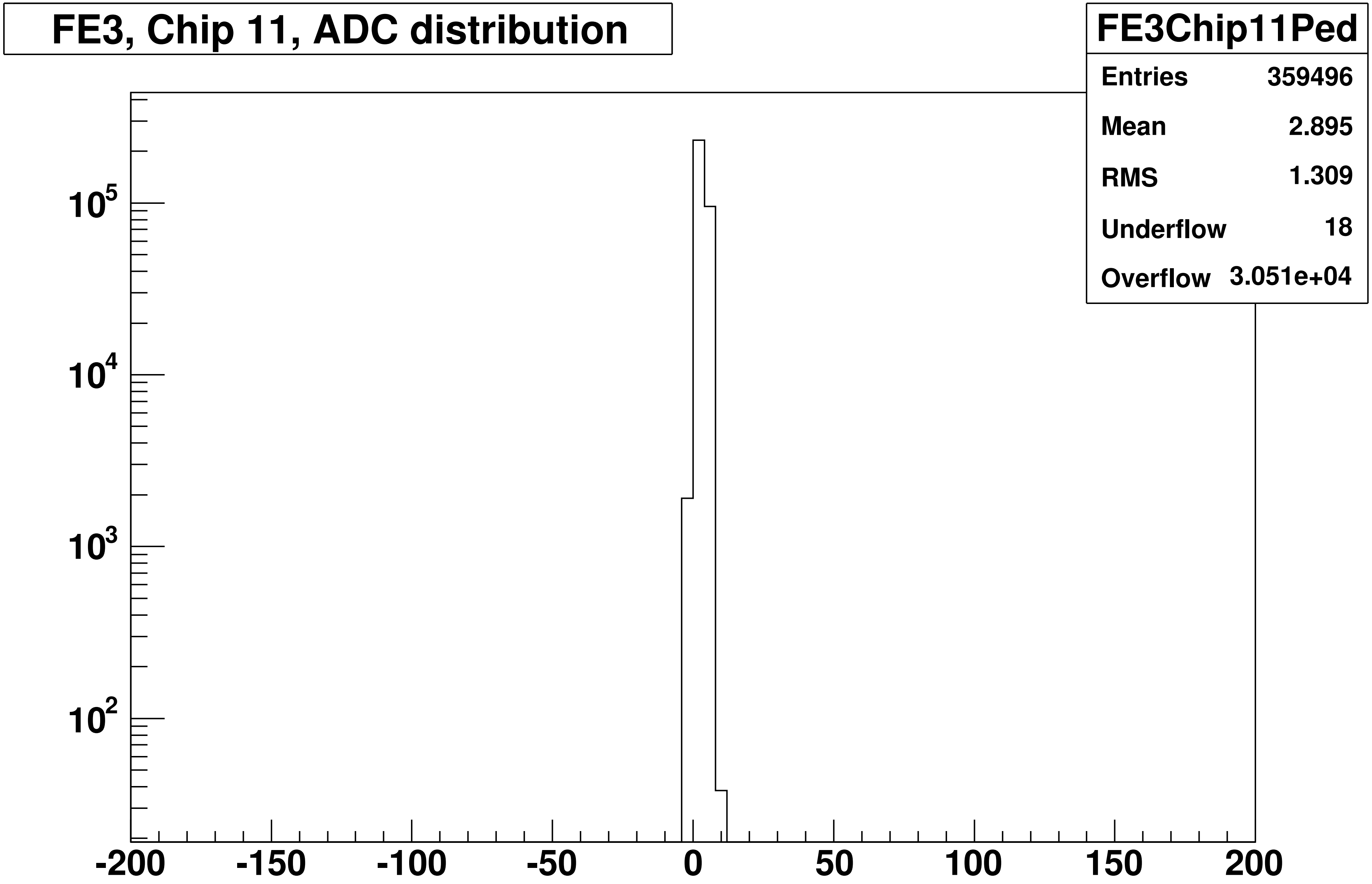
10000
15000
20000
25000


FE3, Chip 11, ADC distribution
FE3Chip11Ped
Entries 359496
Mean 2.895
RMS 1.309
Underflow 18
Overflow 3.051e+04
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10^3
10^2
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-100
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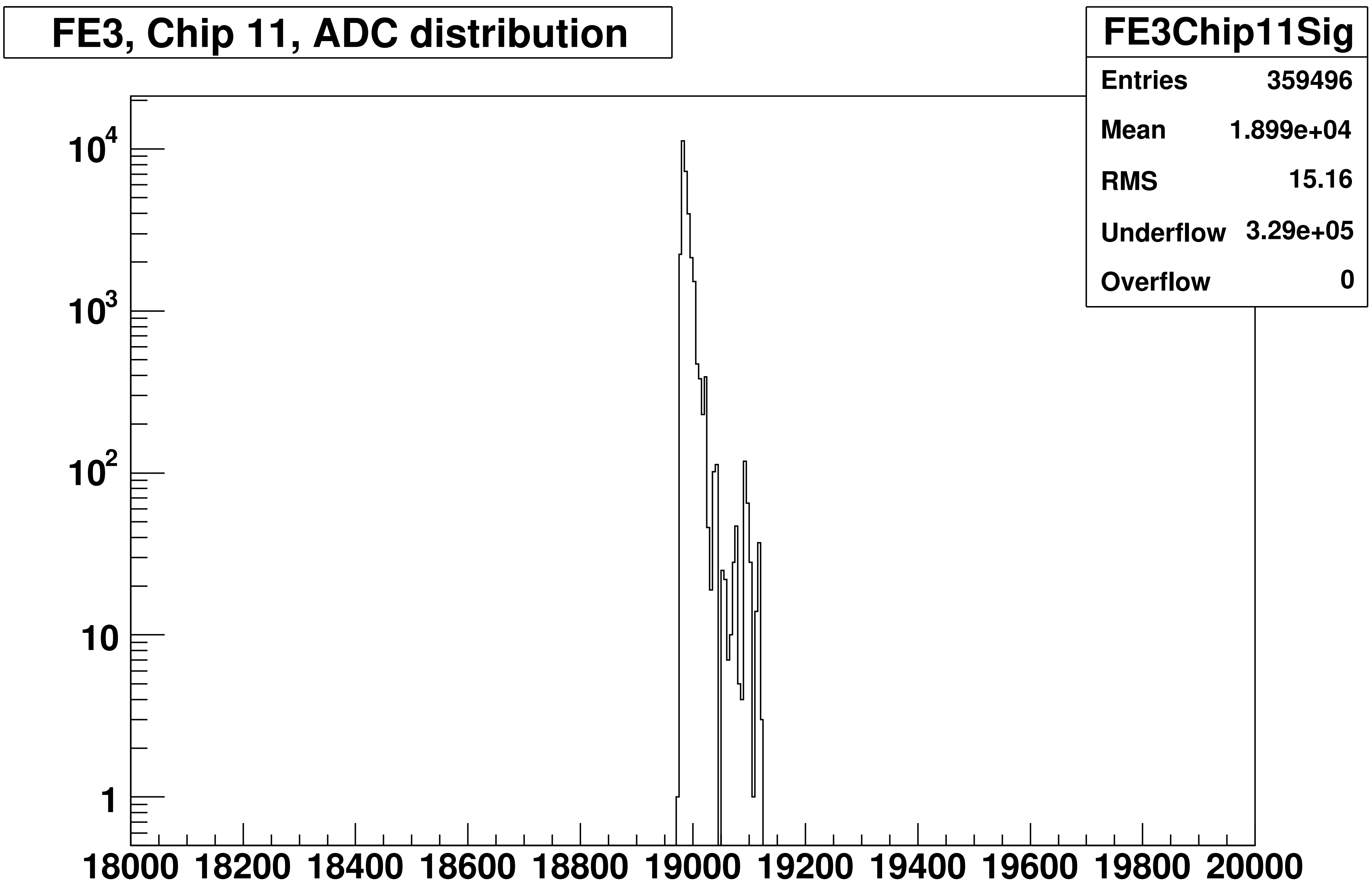
150
200


FE3, Chip 11, ADC distribution
FE3Chip11Sig
Entries 359496
Mean 1.899e+04
RMS 15.16
Underflow 3.29e+05
Overflow 0
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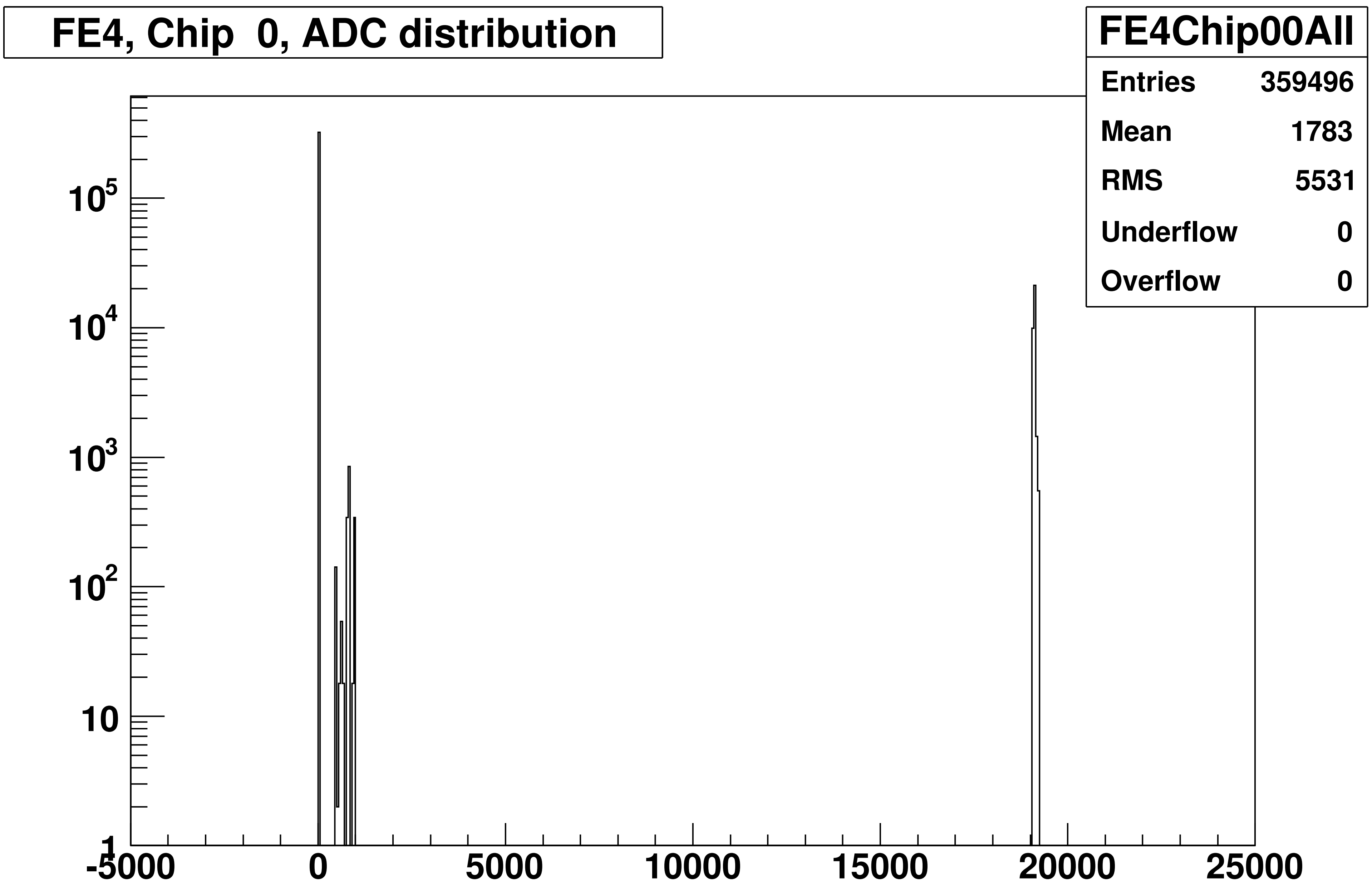
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE4, Chip 0, ADC distribution
FE4Chip00All
Entries 359496
Mean 1783
RMS 5531
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
1
-5000
0
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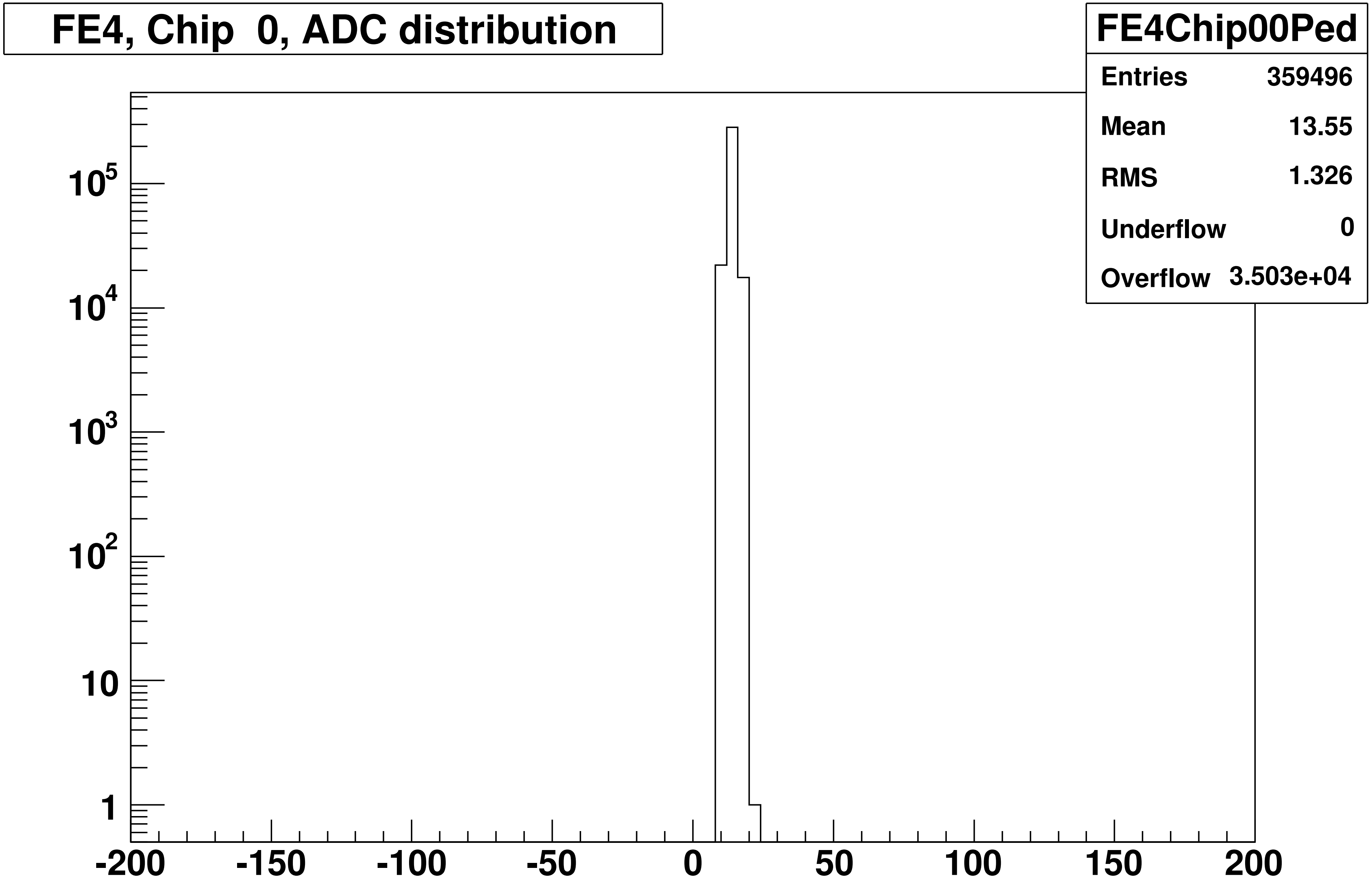
25000


FE4, Chip 0, ADC distribution
FE4Chip00Ped
Entries 359496
Mean 13.55
RMS 1.326
Underflow 0
Overflow 3.503e+04
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10^3
10^2
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150
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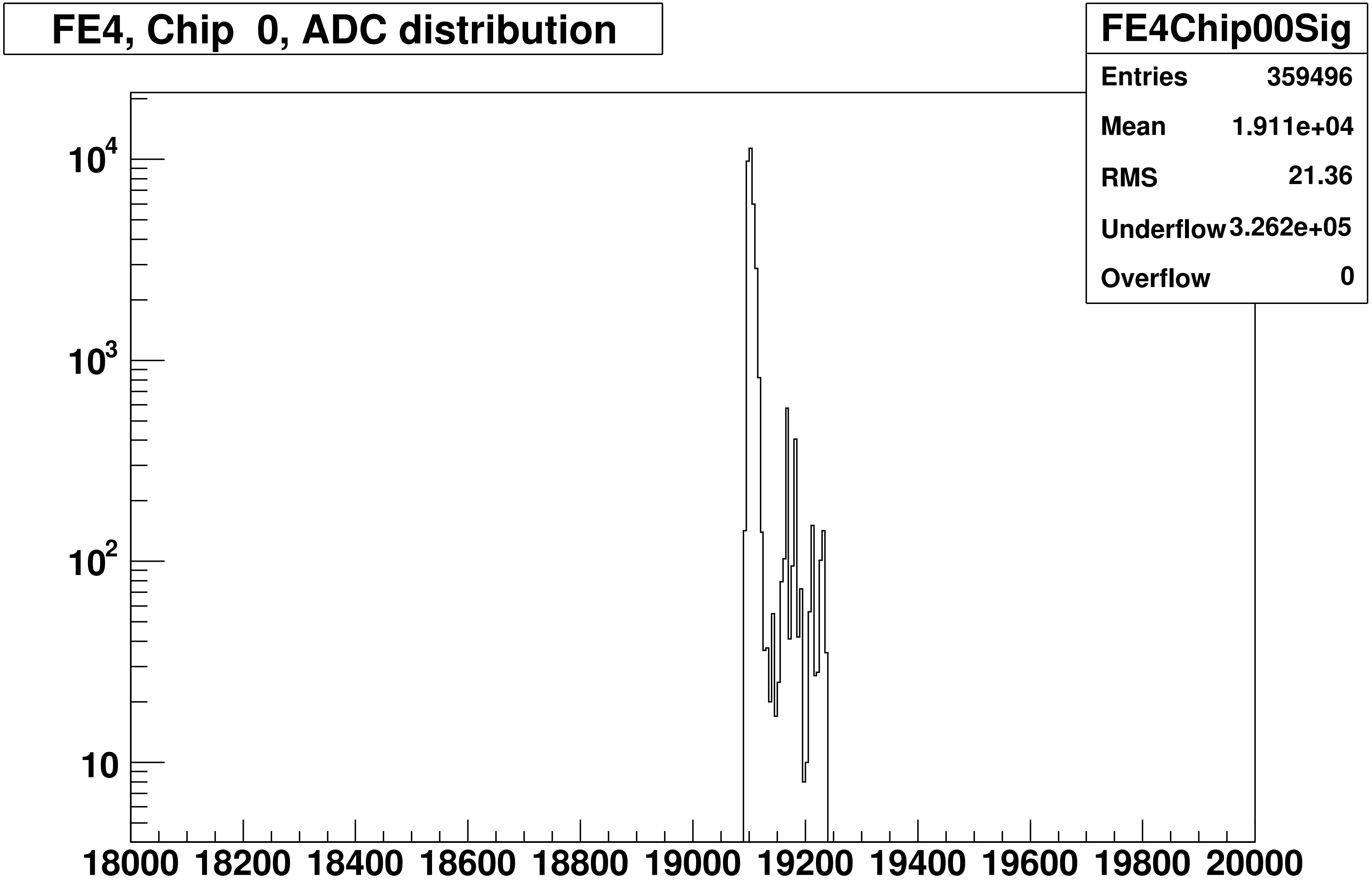

FE4, Chip 0, ADC distribution
FE4Chip00Sig
Entries 359496
Mean 1.911e+04
RMS 21.36
Underflow 3.262e+05
Overflow 0
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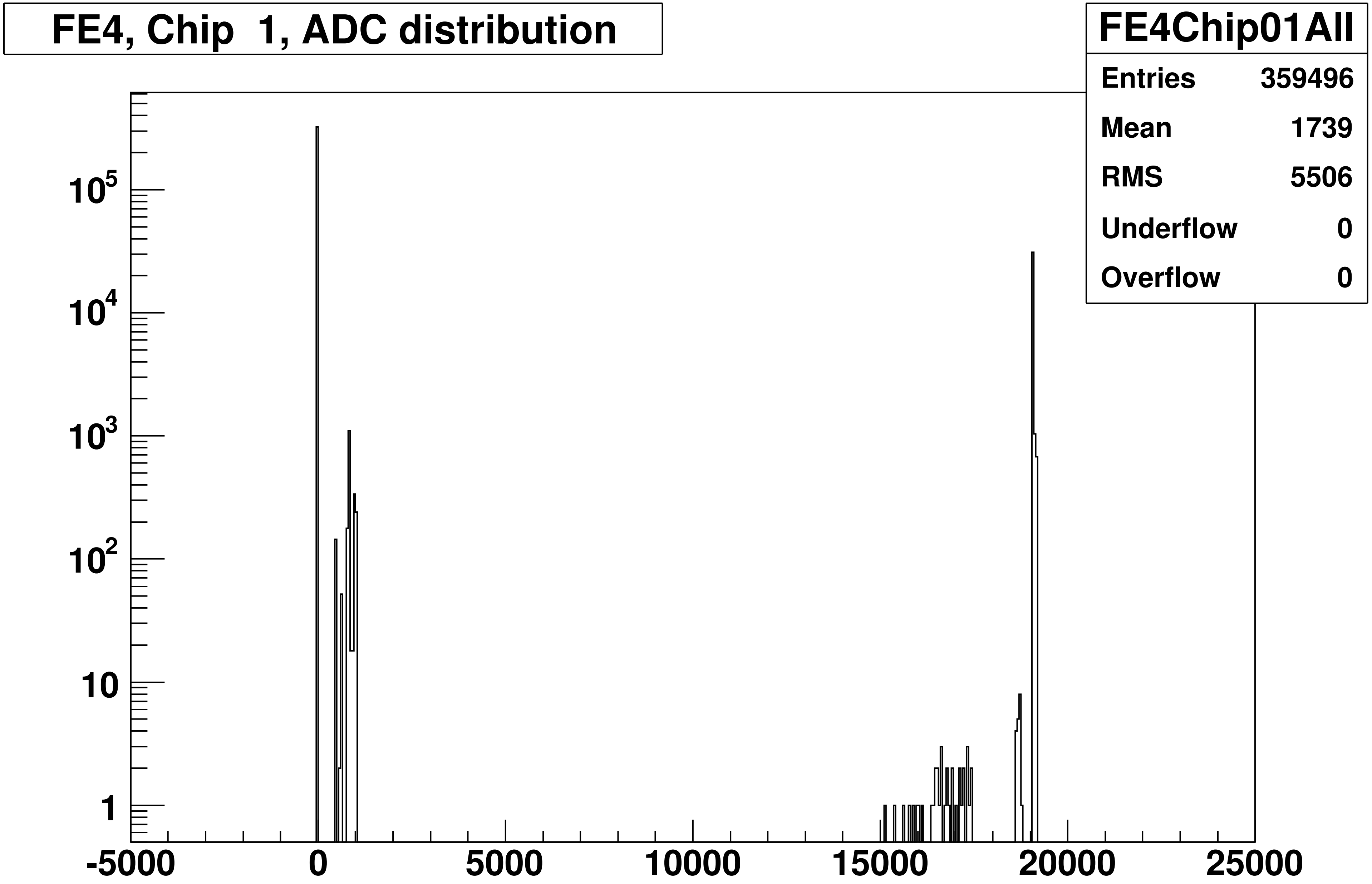
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE4, Chip 1, ADC distribution
FE4Chip01All
Entries 359496
Mean 1739
RMS 5506
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
1
-5000
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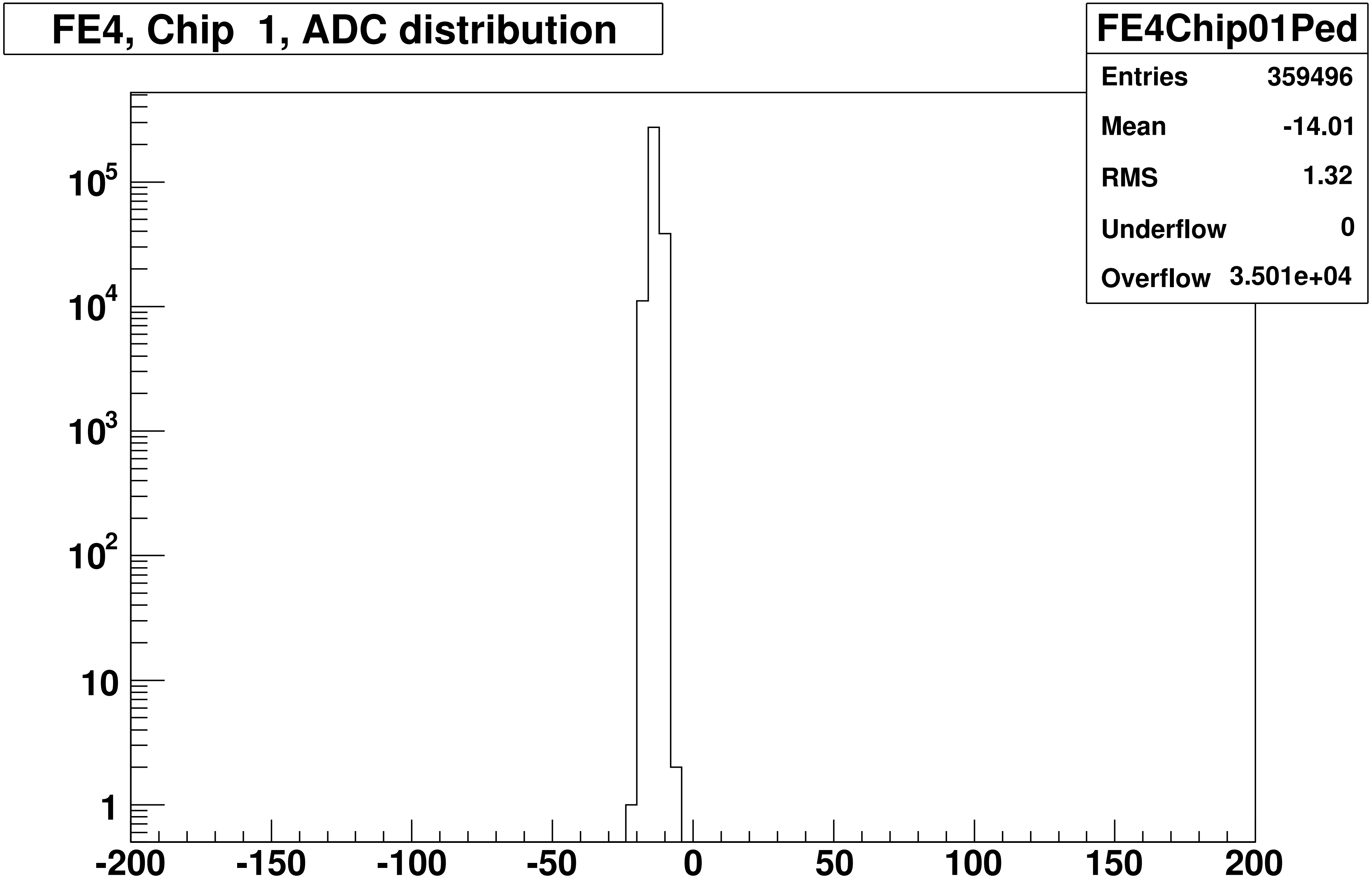
15000
20000
25000



FE4, Chip 1, ADC distribution
FE4Chip01Ped
Entries 359496
Mean -14.01
RMS 1.32
Underflow 0
Overflow 3.501e+04
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10^3
10^2
10
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-100
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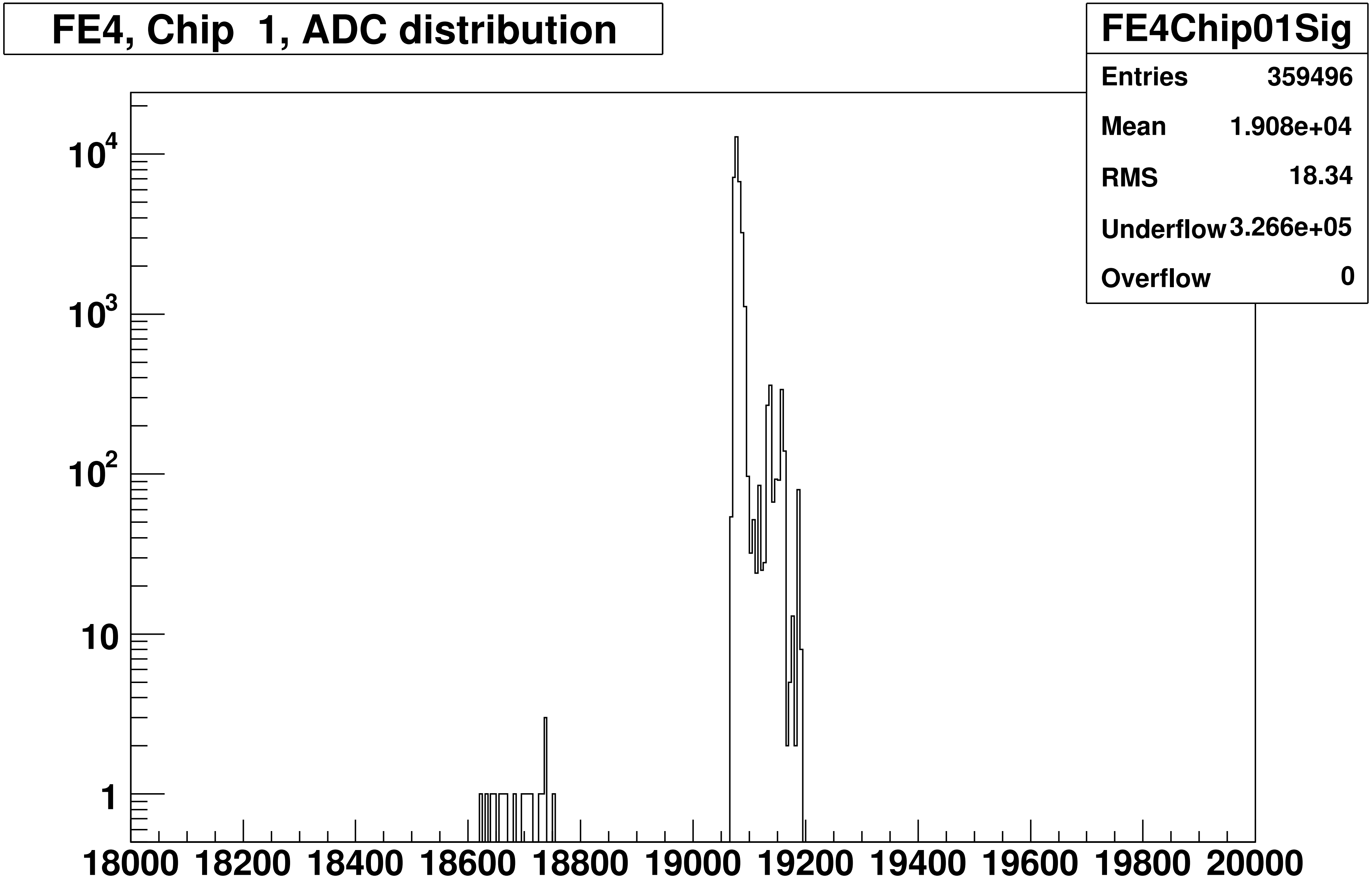
200


FE4, Chip 1, ADC distribution
FE4Chip01Sig
Entries 359496
Mean 1.908e+04
RMS 18.34
Underflow 3.266e+05
Overflow 0
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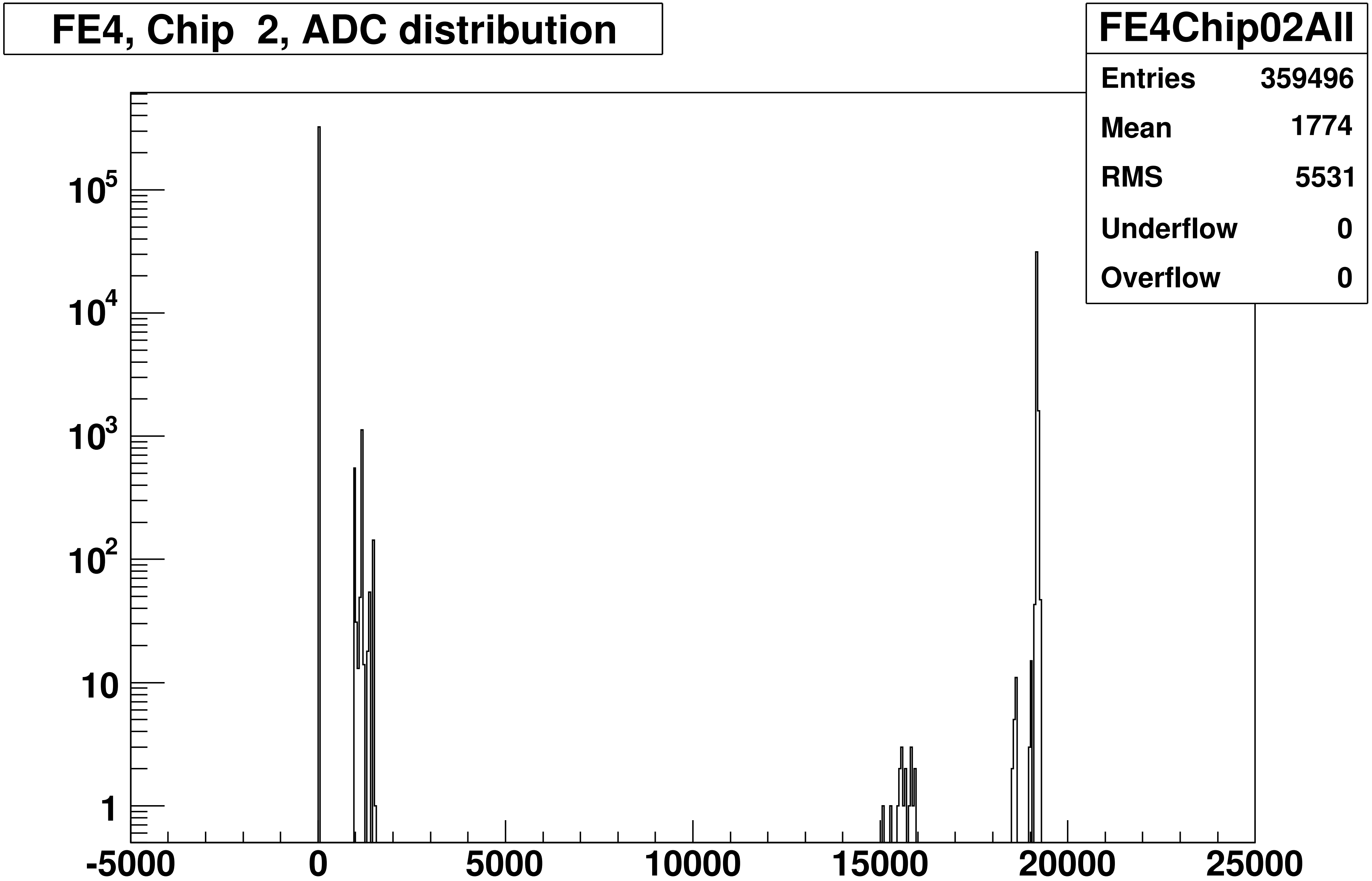
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE4, Chip 2, ADC distribution
FE4Chip02All
Entries 359496
Mean 1774
RMS 5531
Underflow 0
Overflow 0
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10^4
10^3
10^2
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1
-5000
0
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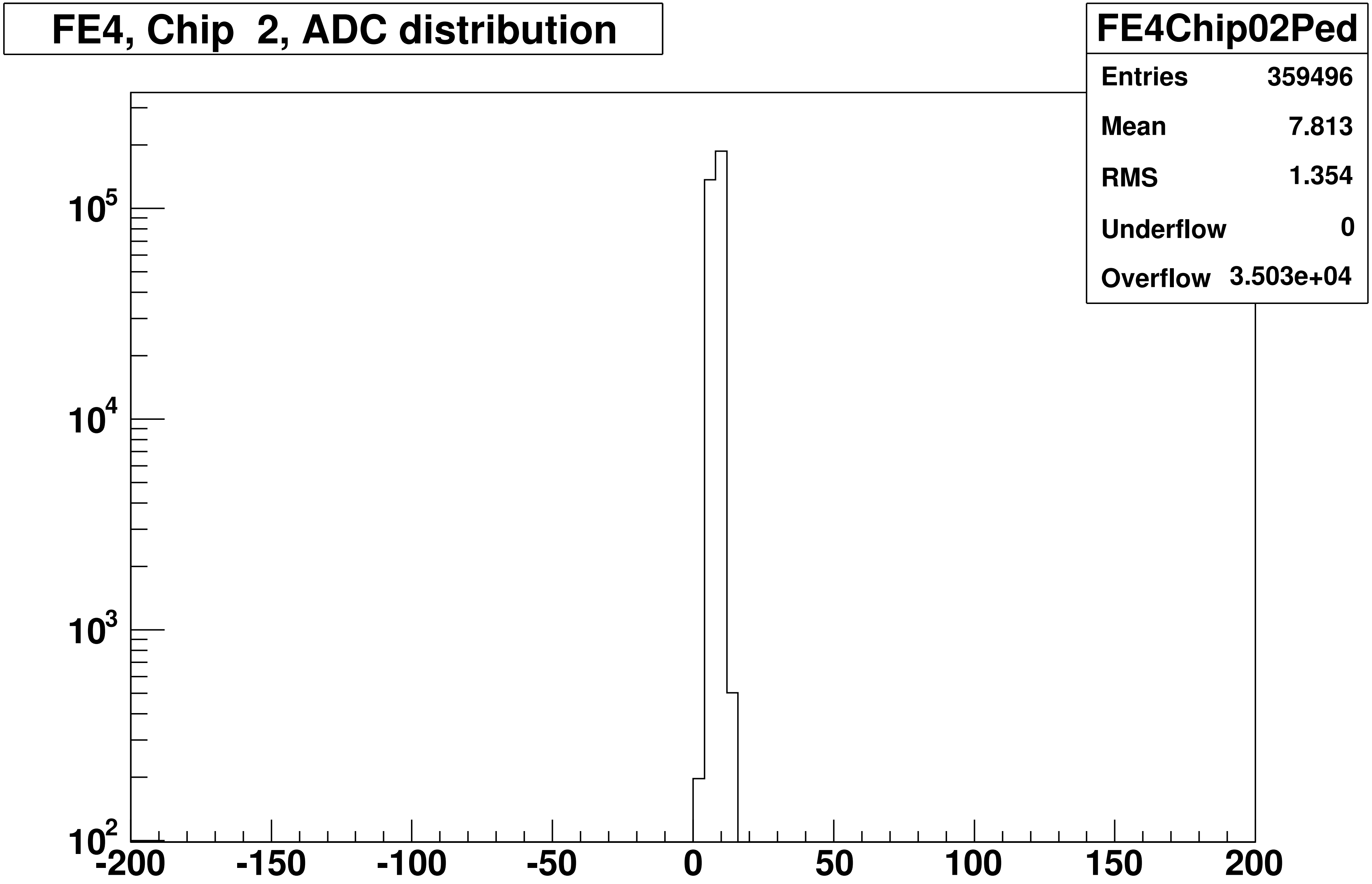
10000
15000
20000
25000


FE4, Chip 2, ADC distribution
FE4Chip02Ped
Entries 359496
Mean 7.813
RMS 1.354
Underflow 0
Overflow 3.503e+04
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10^3
10^2
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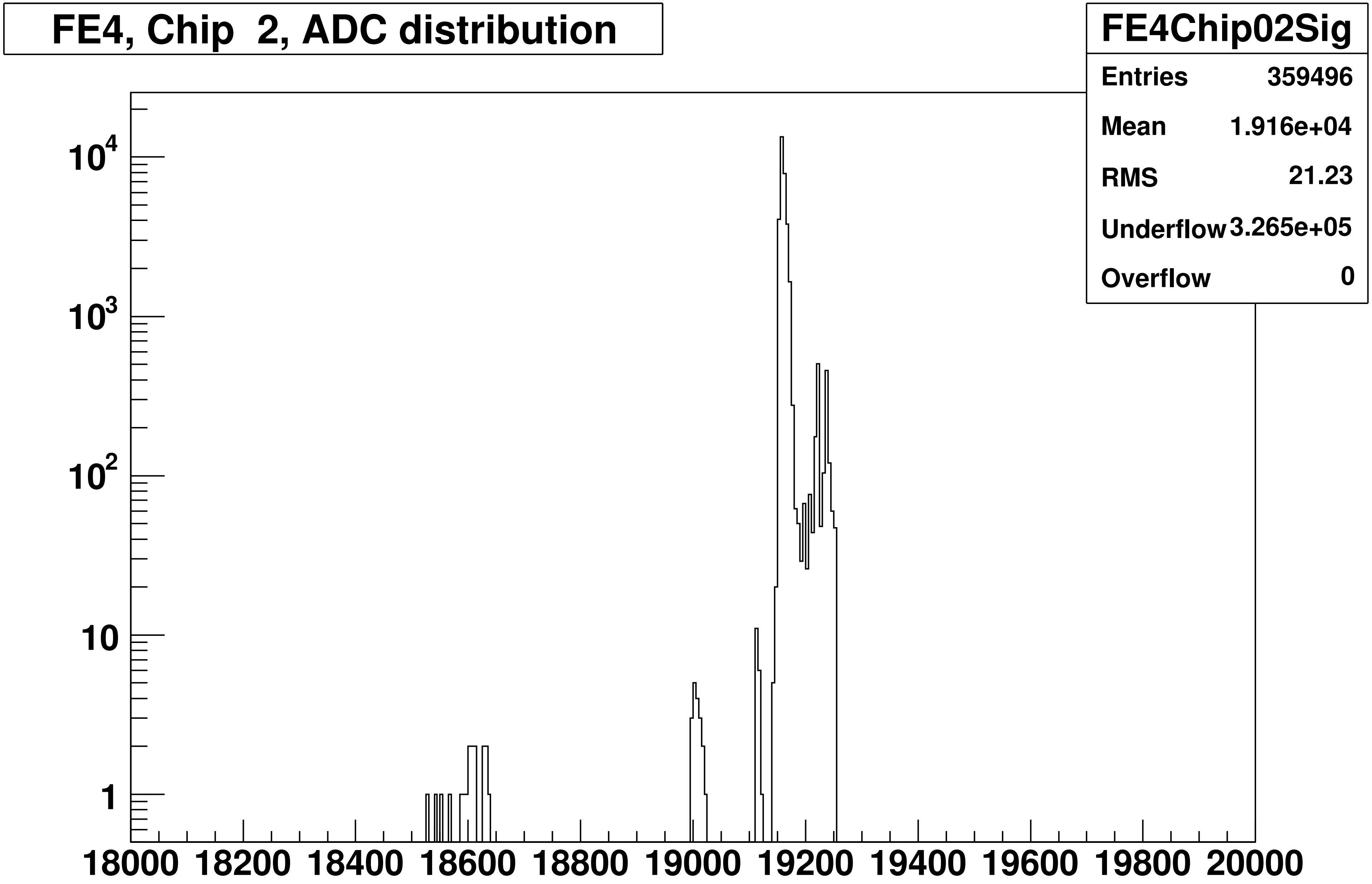
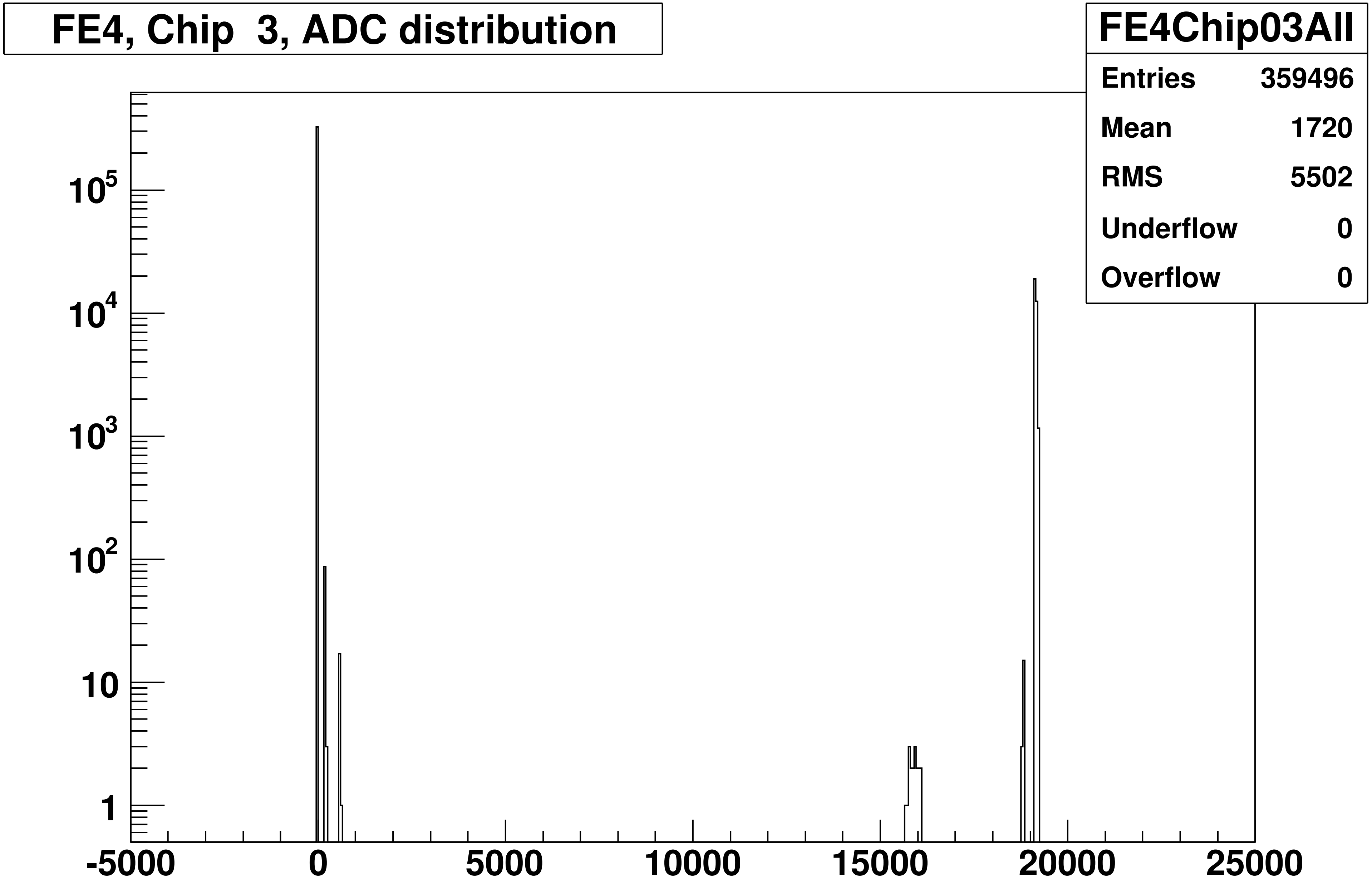
150
200



FE4, Chip 2, ADC distribution
FE4Chip02Sig
Entries 359496
Mean 1.916e+04
RMS 21.23
Underflow 3.265e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE4, Chip 3, ADC distribution
FE4Chip03All
Entries 359496
Mean 1720
RMS 5502
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
1
-5000
0
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10000
15000
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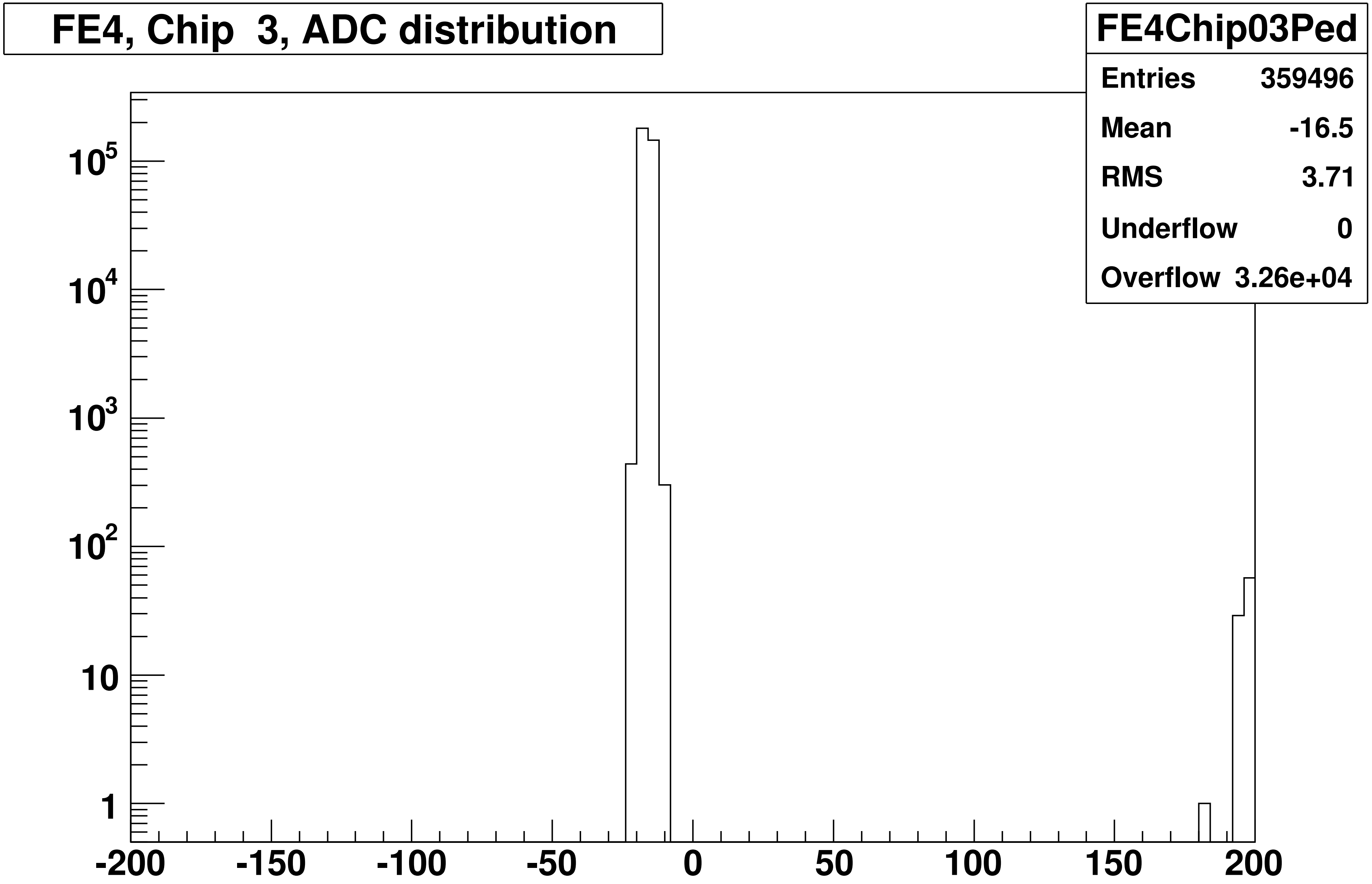
25000



FE4, Chip 3, ADC distribution
FE4Chip03Ped
Entries 359496
Mean -16.5
RMS 3.71
Underflow 0
Overflow 3.26e+04
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10^3
10^2
10
1
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-100
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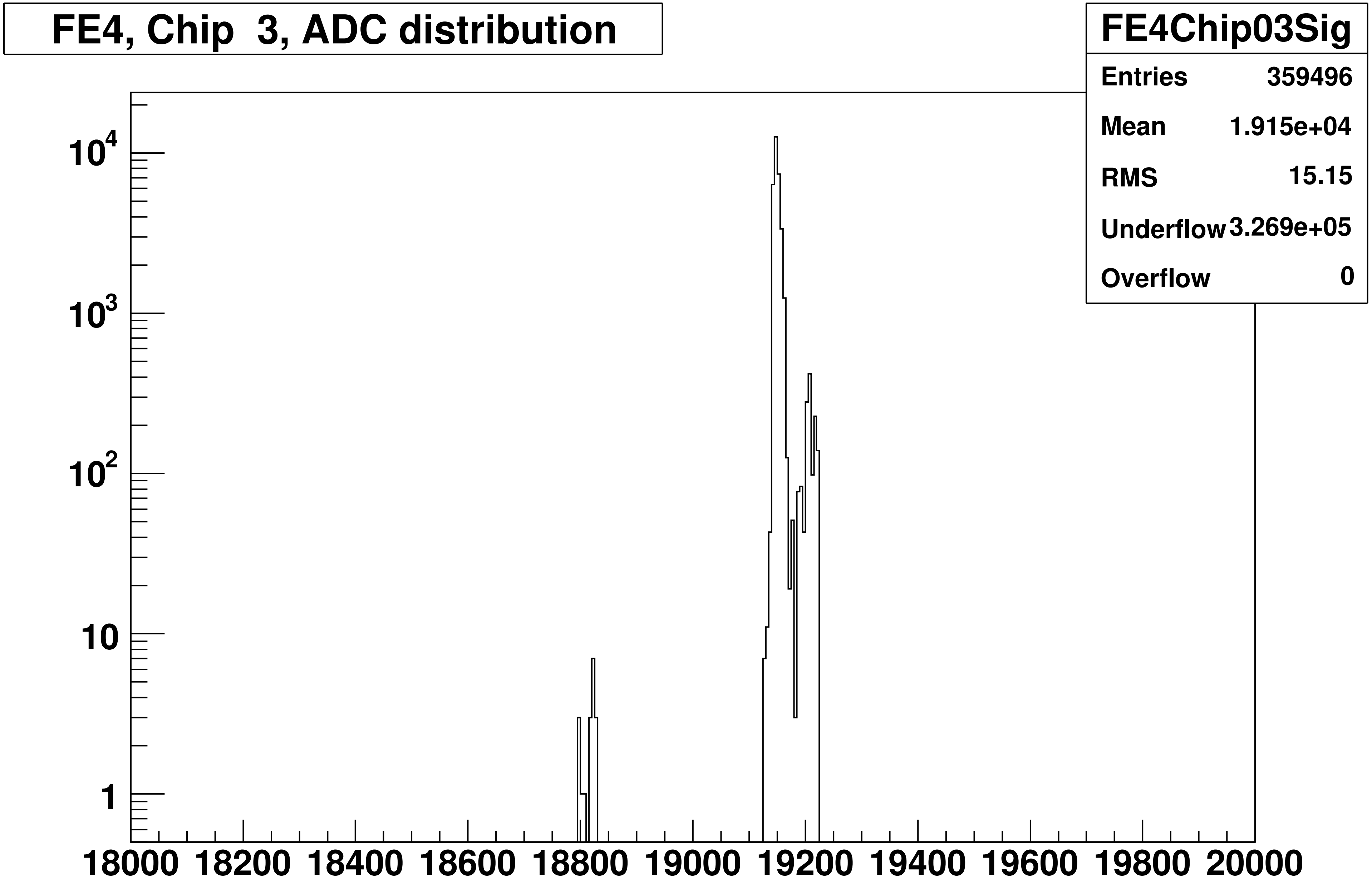
150
200


FE4, Chip 3, ADC distribution
FE4Chip03Sig
Entries 359496
Mean 1.915e+04
RMS 15.15
Underflow 3.269e+05
Overflow 0
10^4
10^3
10^2
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1
18000
18200
18400
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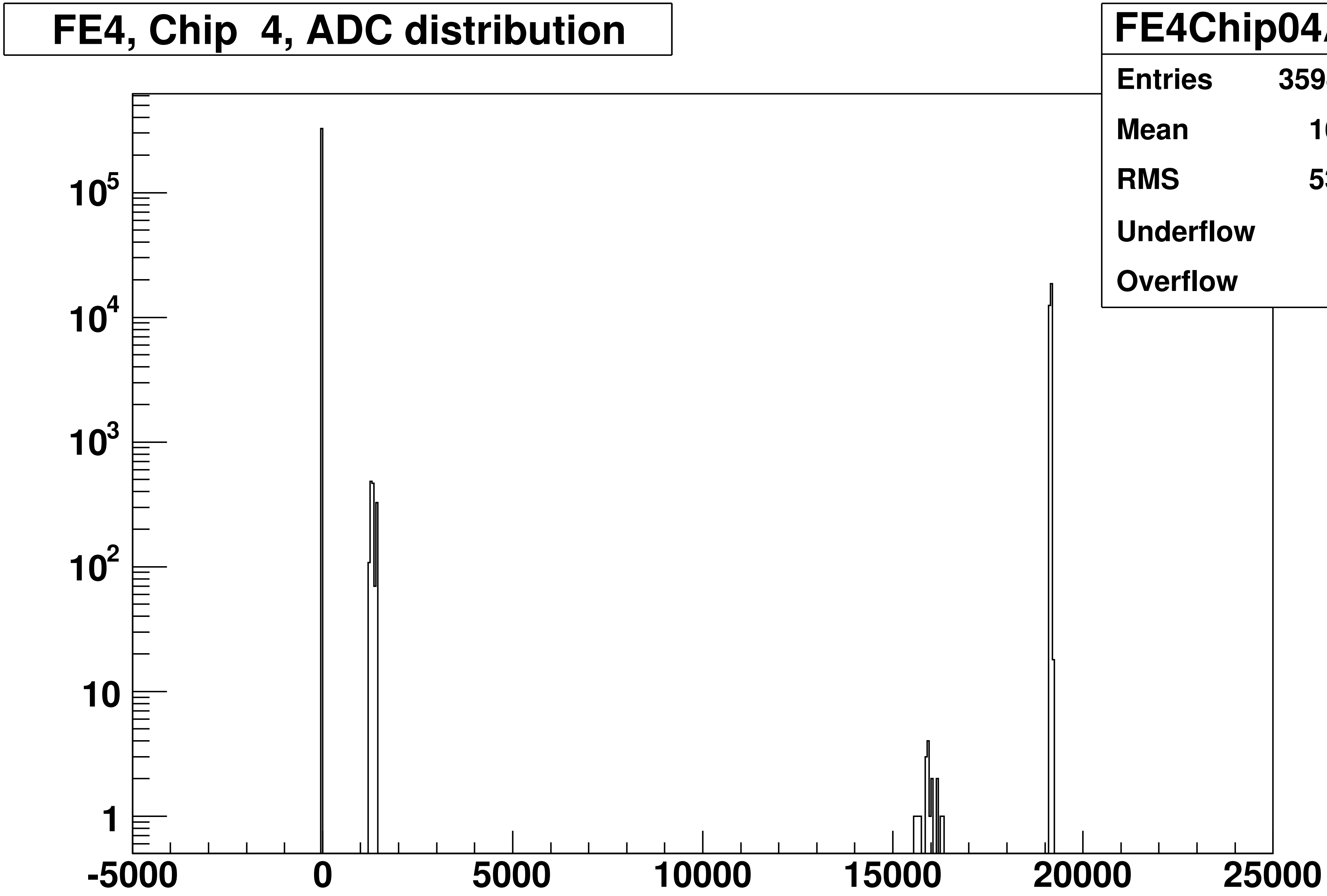
19800
20000



FE4, Chip 4, ADC distribution
FE4Chip04All
Entries 359496
Mean 1652
RMS 5388
Underflow 0
Overflow 0
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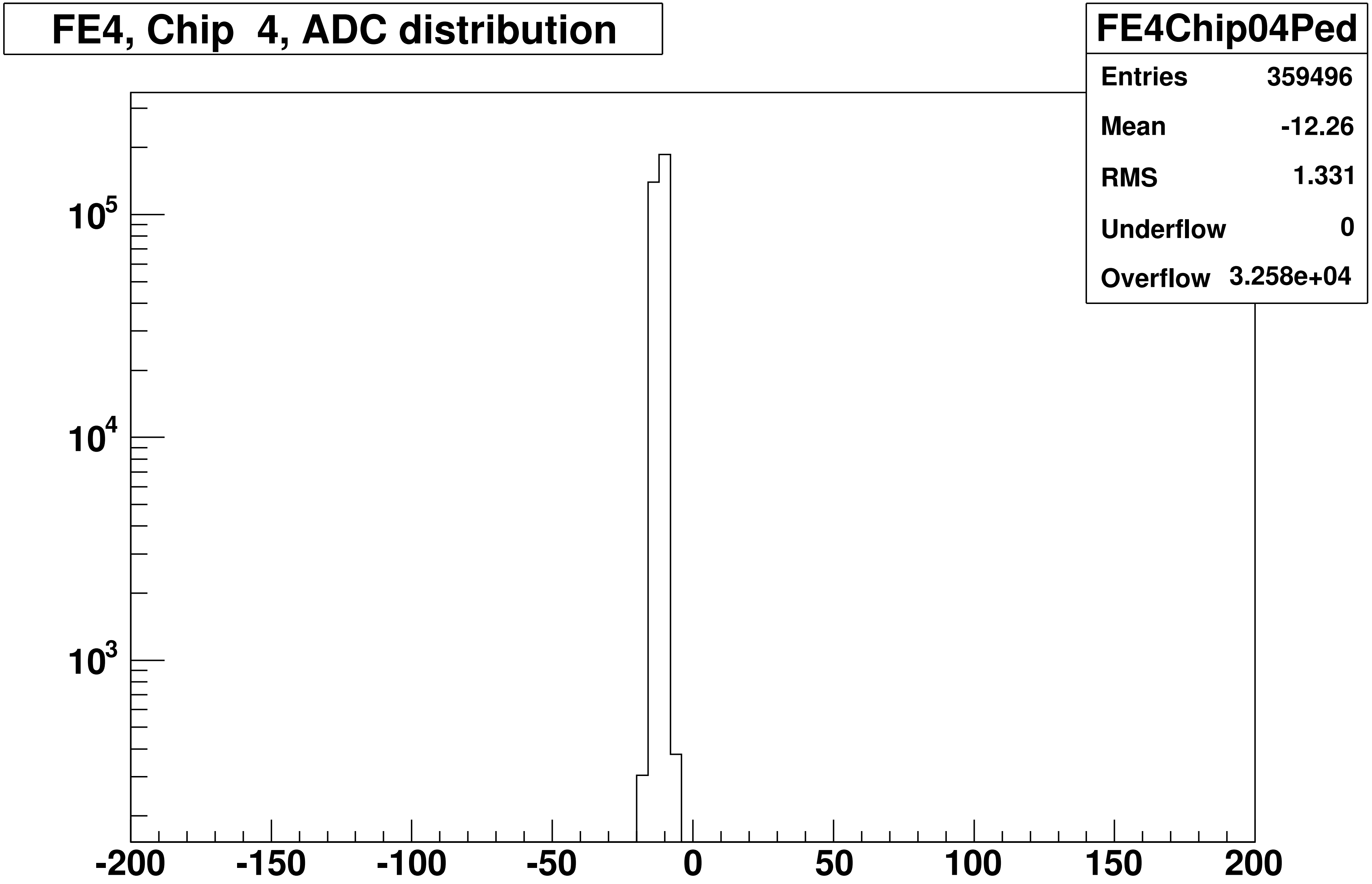
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE4, Chip 4, ADC distribution
FE4Chip04Ped
Entries 359496
Mean -12.26
RMS 1.331
Underflow 0
Overflow 3.258e+04
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10^4
10^3
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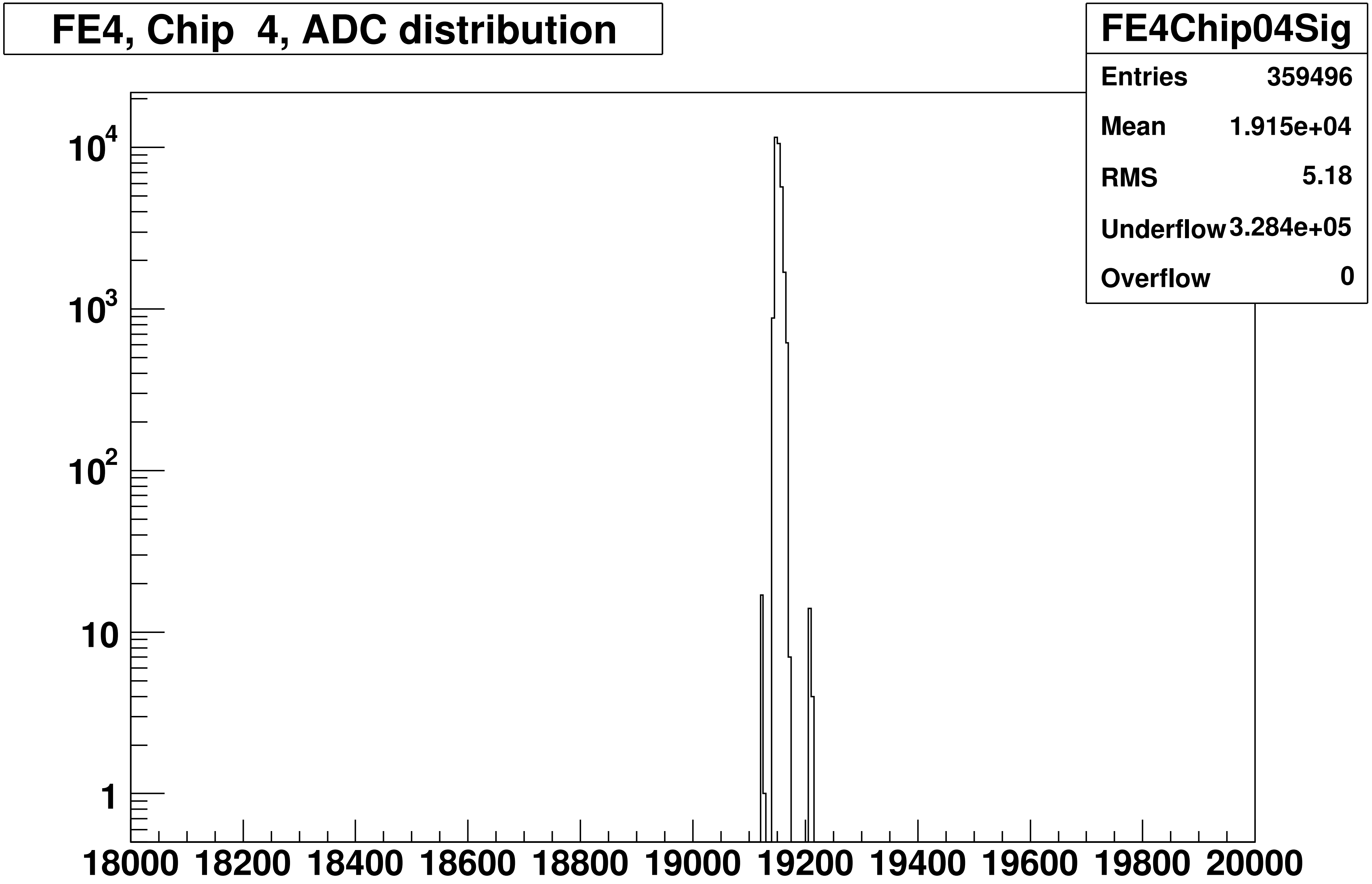

FE4, Chip 4, ADC distribution
FE4Chip04Sig
Entries 359496
Mean 1.915e+04
RMS 5.18
Underflow 3.284e+05
Overflow 0
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10^3
10^2
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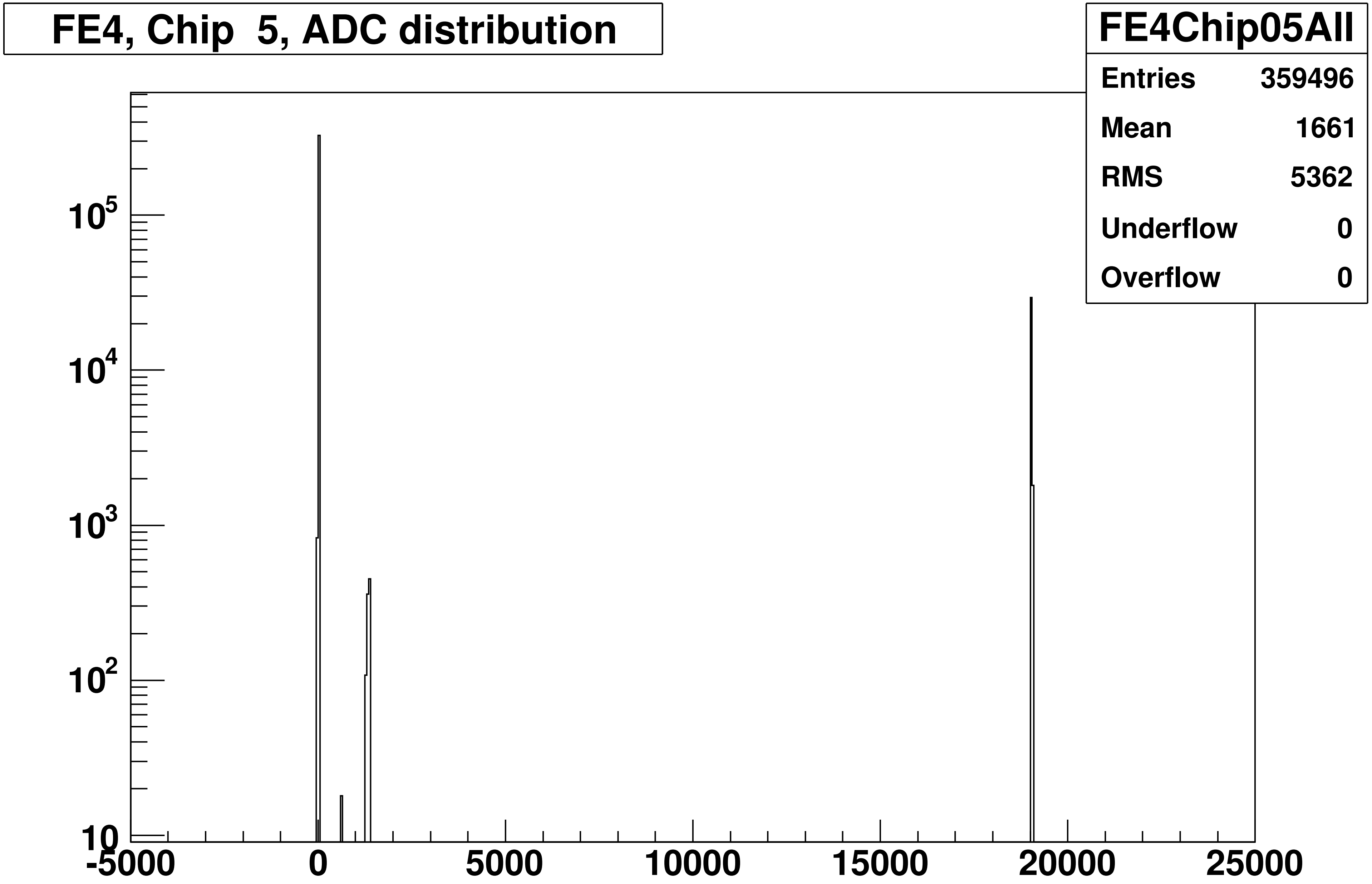
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE4, Chip 5, ADC distribution
FE4Chip05All
Entries 359496
Mean 1661
RMS 5362
Underflow 0
Overflow 0
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10^4
10^3
10^2
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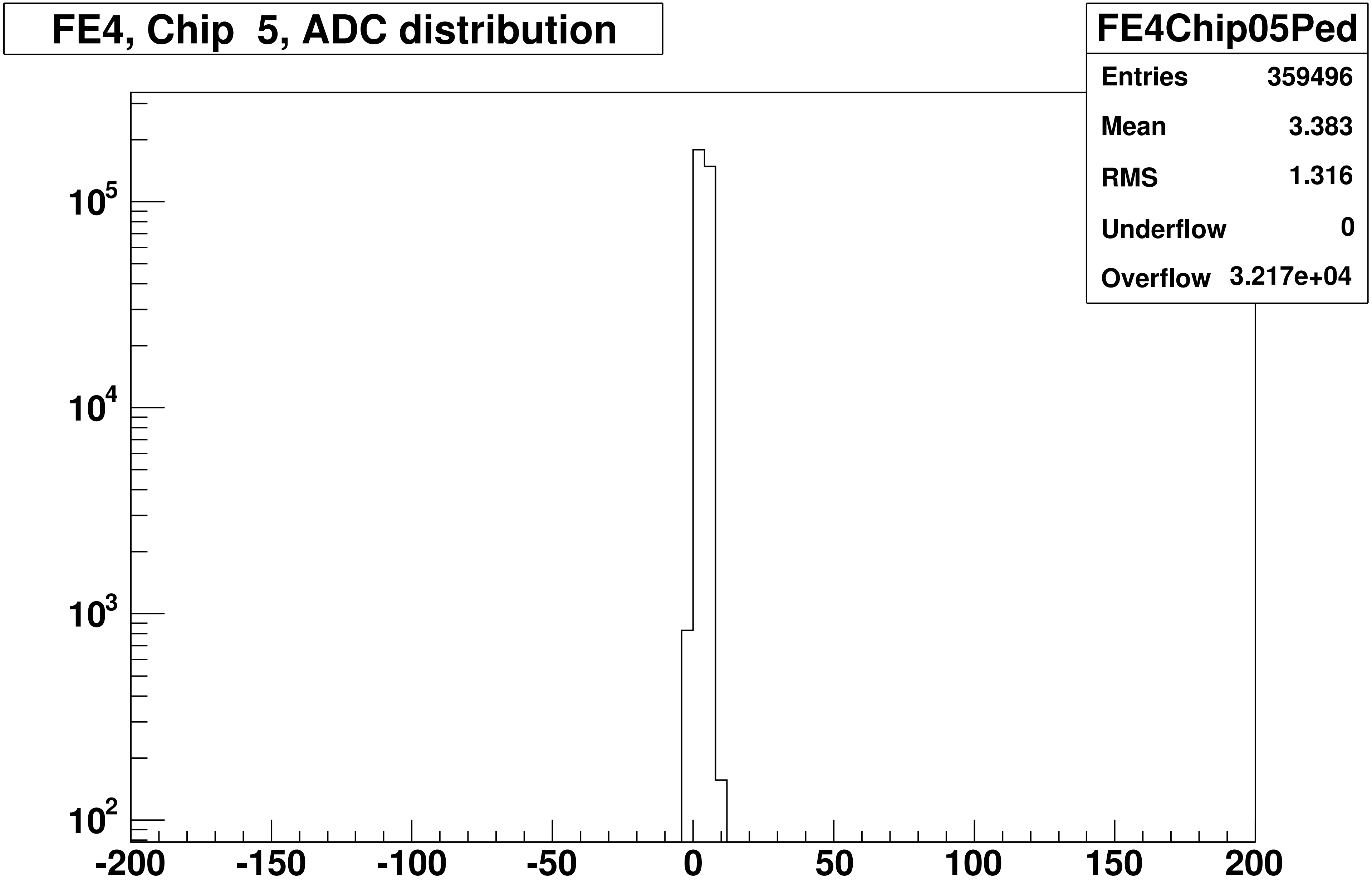
25000


FE4, Chip 5, ADC distribution
FE4Chip05Ped
Entries 359496
Mean 3.383
RMS 1.316
Underflow 0
Overflow 3.217e+04
10^5
10^4
10^3
10^2
-200
-150
-100
-50
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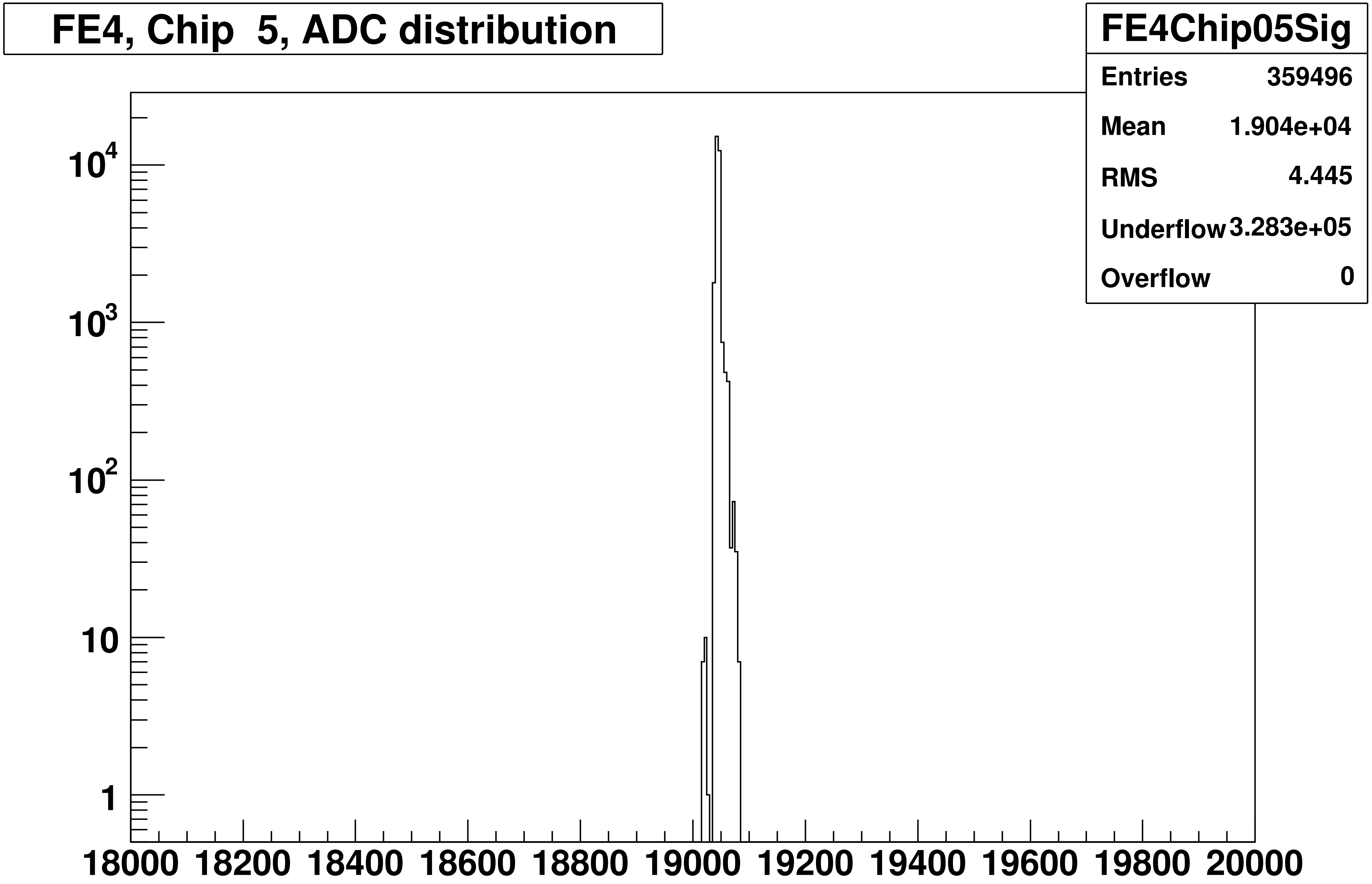
100
150
200


FE4, Chip 5, ADC distribution
FE4Chip05Sig
Entries 359496
Mean 1.904e+04
RMS 4.445
Underflow 3.283e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
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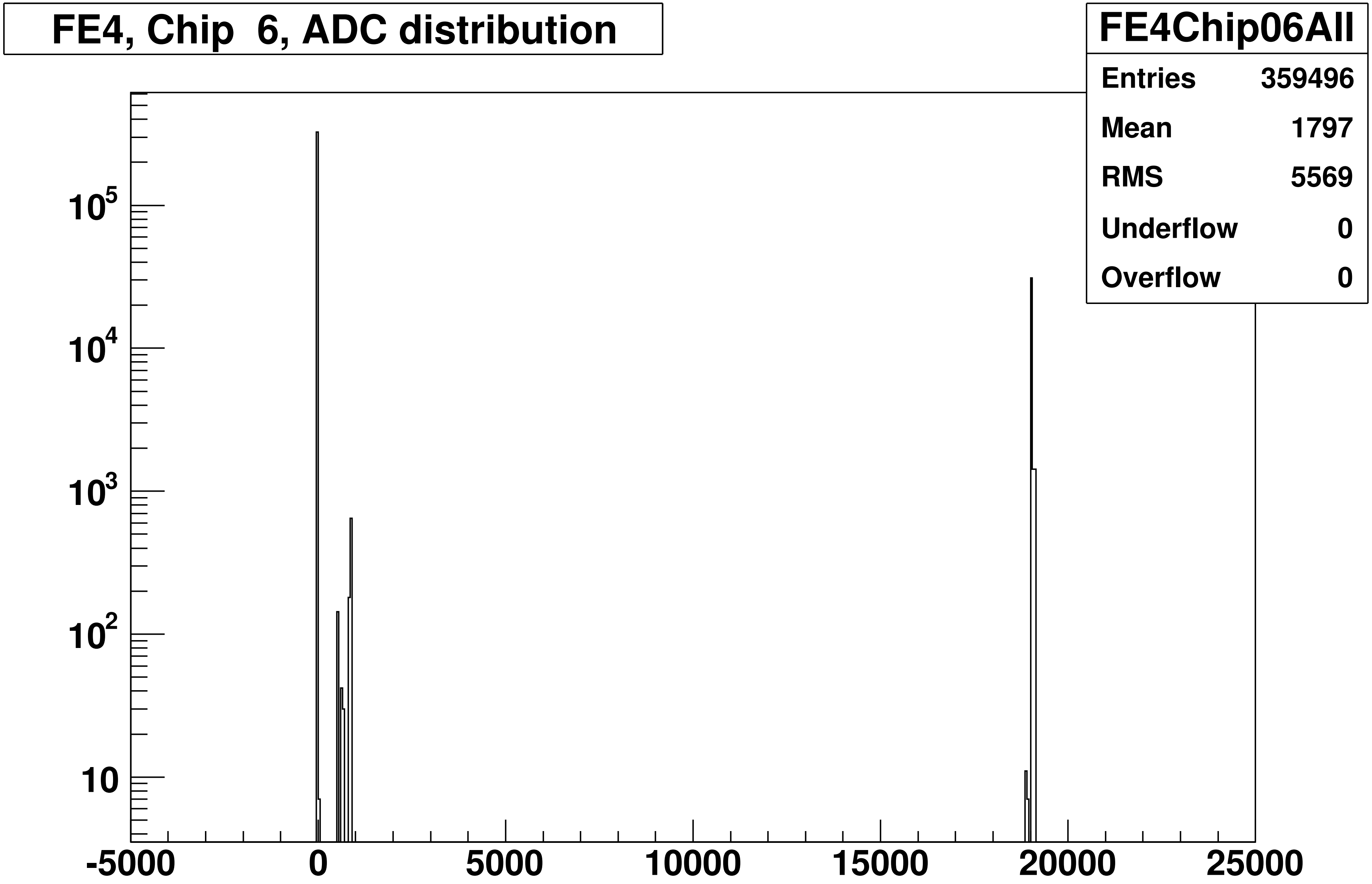
19600
19800
20000


FE4, Chip 6, ADC distribution
FE4Chip06All
Entries 359496
Mean 1797
RMS 5569
Underflow 0
Overflow 0
10
10^2
10^3
10^4
10^5
-5000
0
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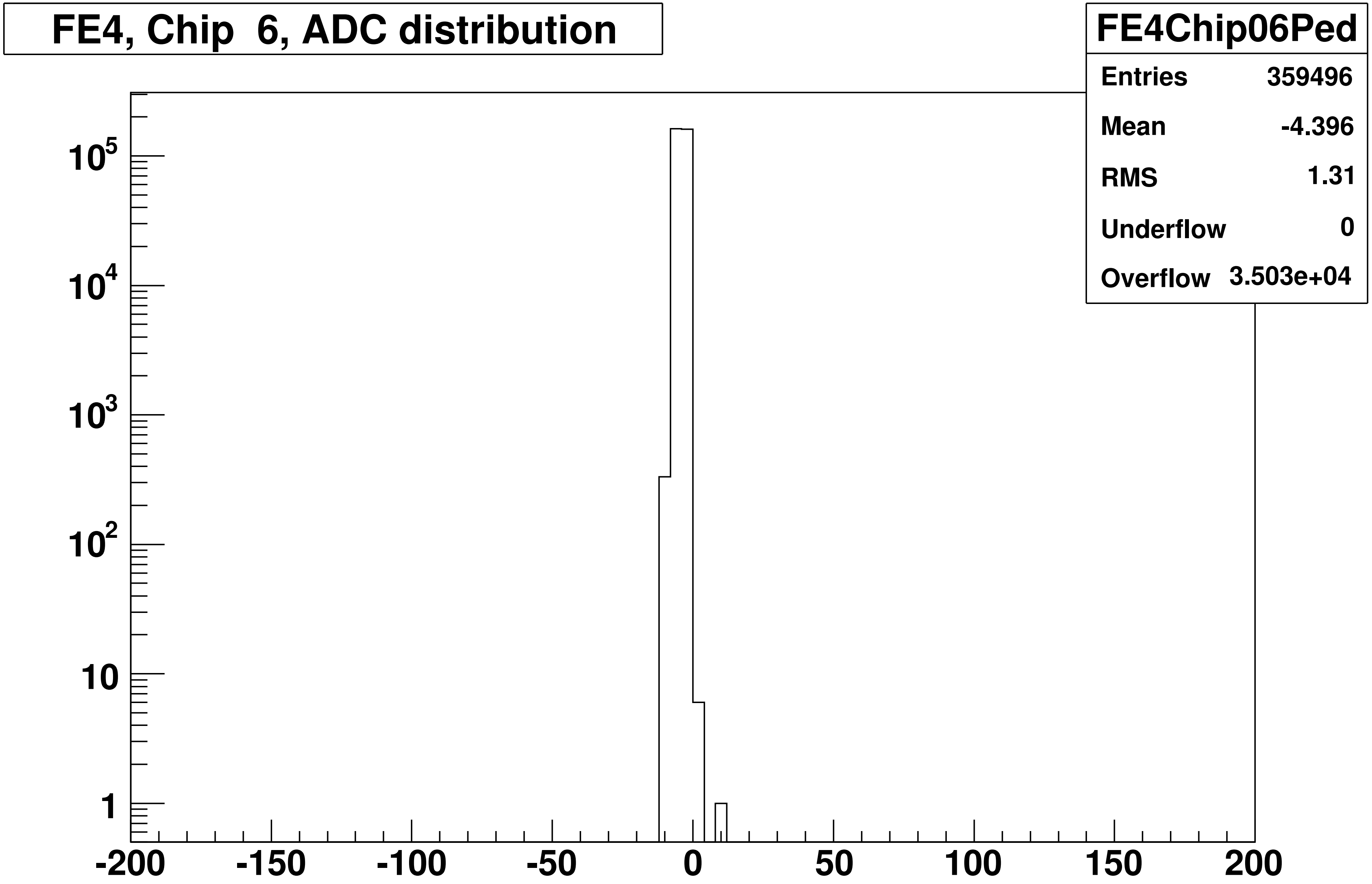
10000
15000
20000
25000



FE4, Chip 6, ADC distribution
FE4Chip06Ped
Entries 359496
Mean -4.396
RMS 1.31
Underflow 0
Overflow 3.503e+04
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10^4
10^3
10^2
10
1
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0
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100
150
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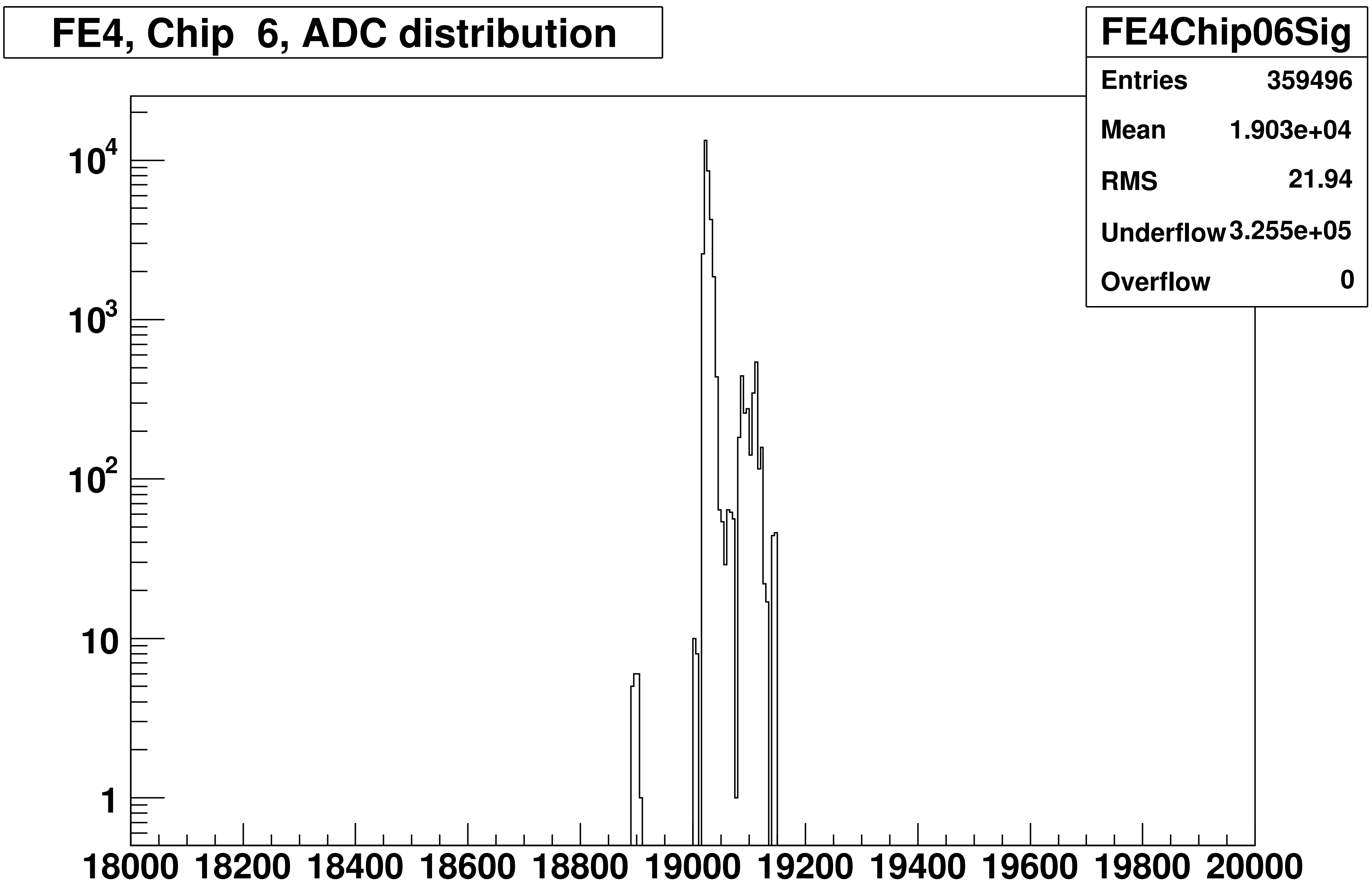
FE4, Chip 6, ADC distribution
FE4Chip06Sig
Entries 359496
Mean 1.903e+04
RMS 21.94
Underflow 3.255e+05
Overflow 0
10^4
10^3
10^2
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1
18000
18200
18400
18600
18800
19000
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19800
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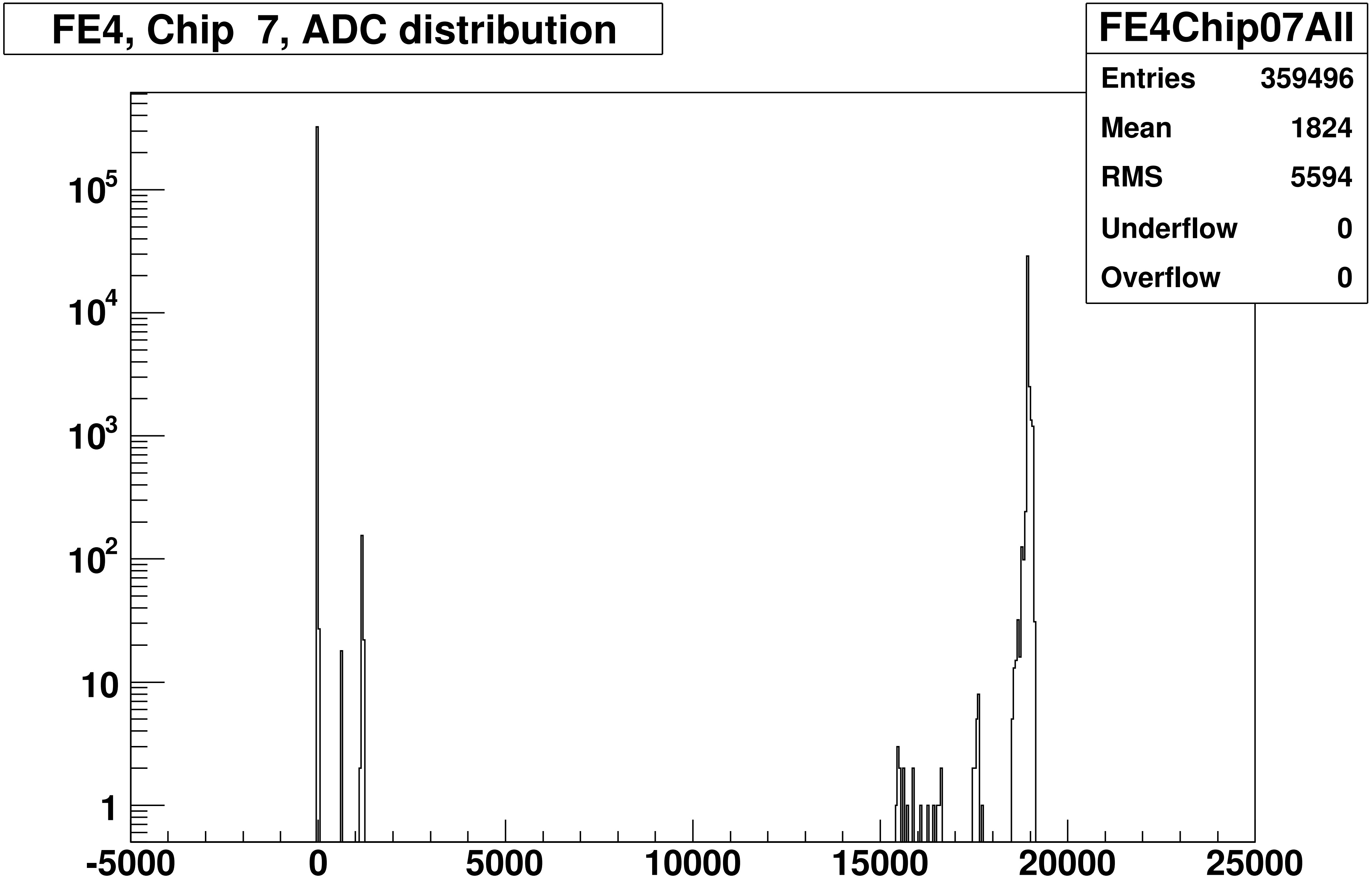
FE4, Chip 7, ADC distribution
FE4Chip07All
Entries 359496
Mean 1824
RMS 5594
Underflow 0
Overflow 0
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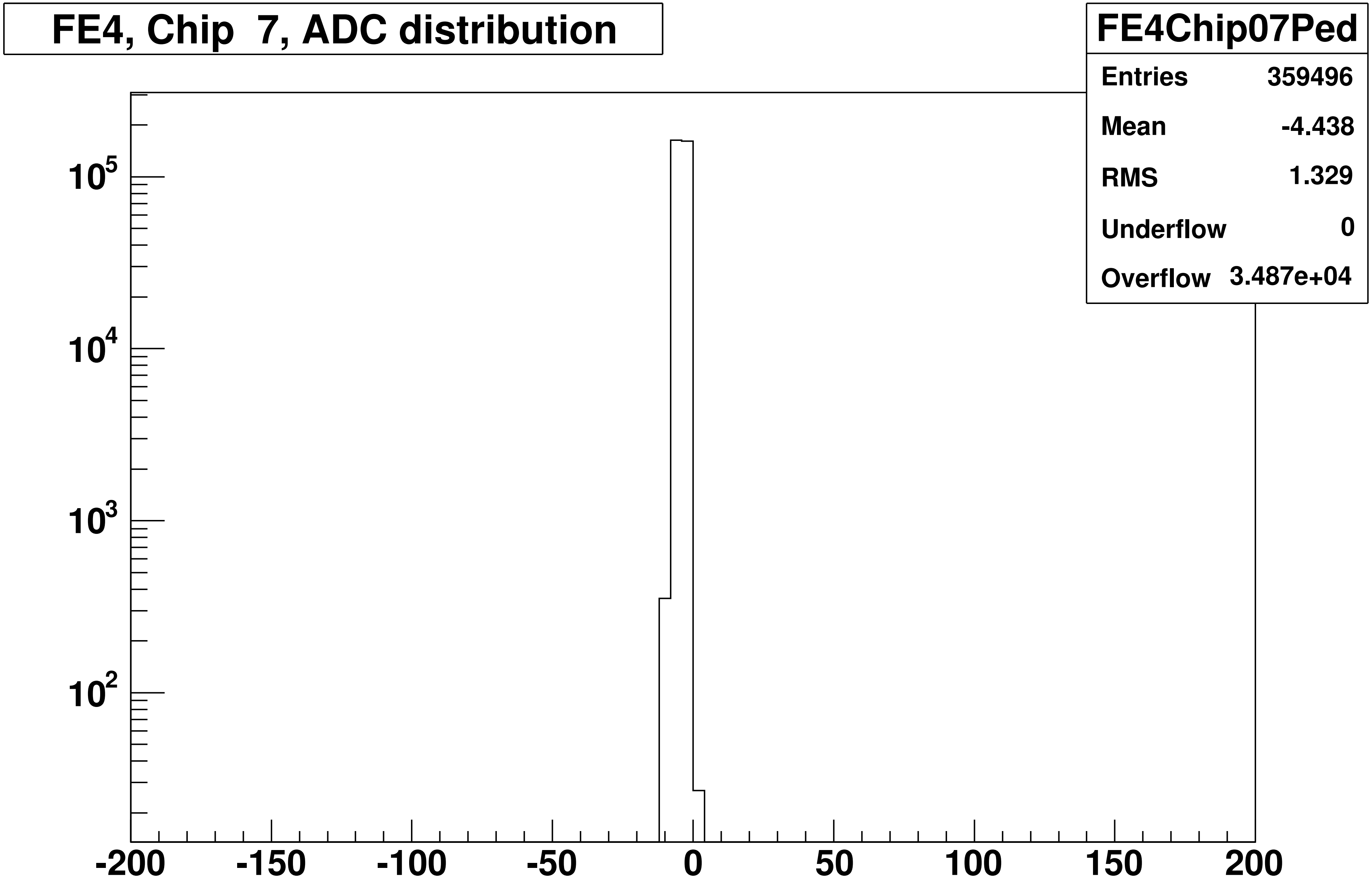
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE4, Chip 7, ADC distribution
FE4Chip07Ped
Entries 359496
Mean -4.438
RMS 1.329
Underflow 0
Overflow 3.487e+04
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10^3
10^2
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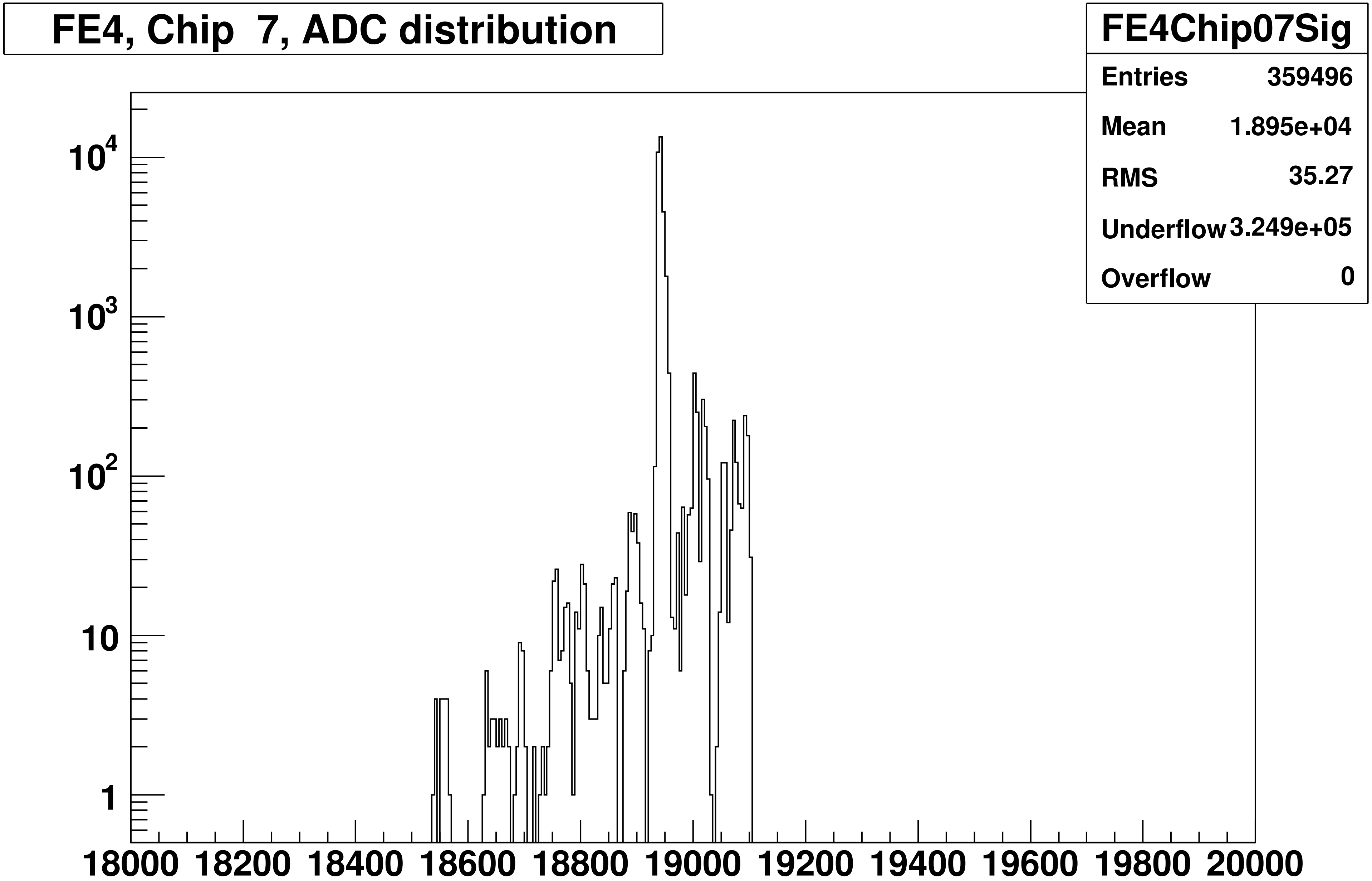
50
100
150
200



FE4, Chip 7, ADC distribution
FE4Chip07Sig
Entries 359496
Mean 1.895e+04
RMS 35.27
Underflow 3.249e+05
Overflow 0
10^4
10^3
10^2
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1
18000
18200
18400
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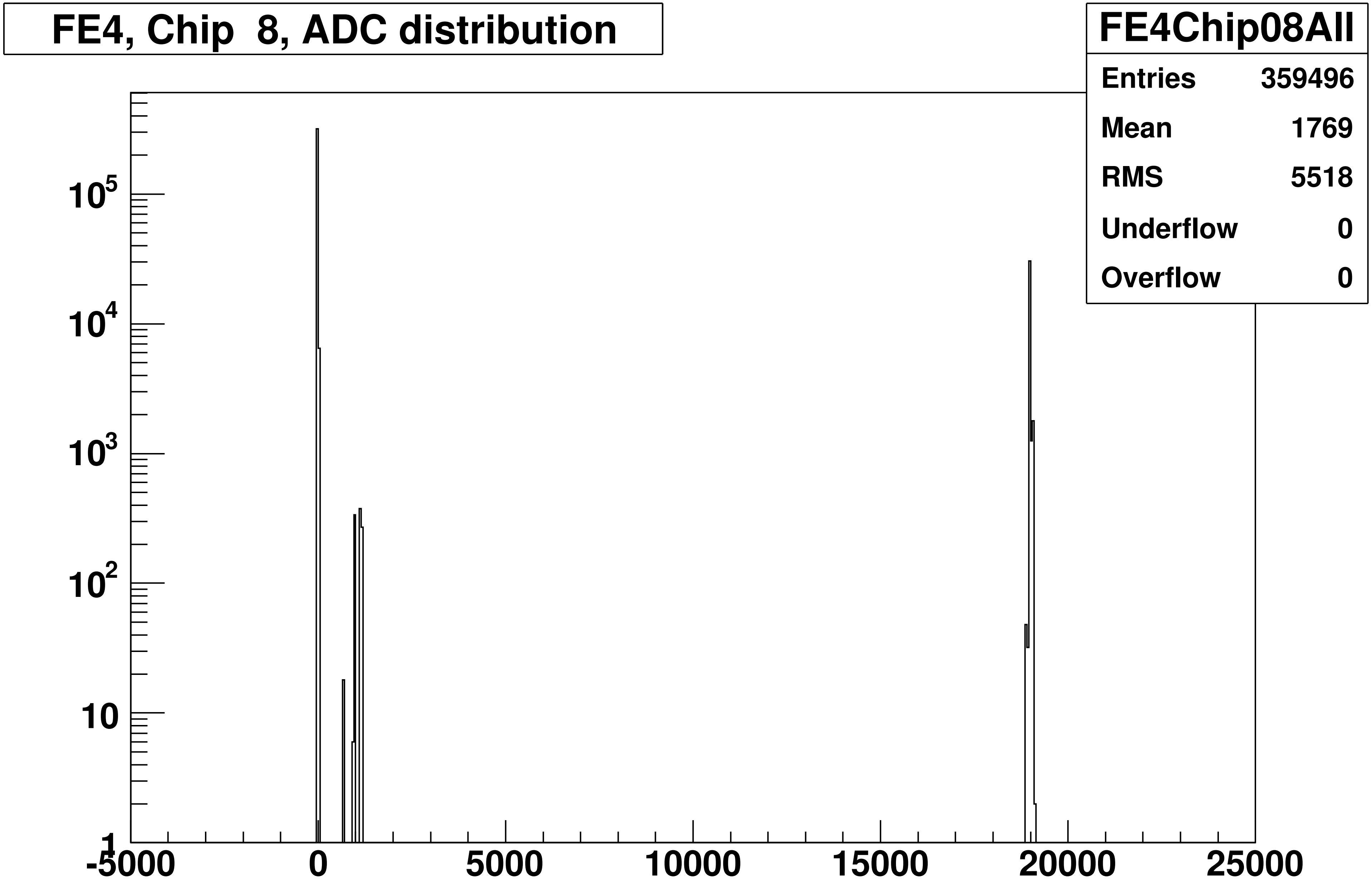

FE4, Chip 8, ADC distribution
FE4Chip08All
Entries 359496
Mean 1769
RMS 5518
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
1
-5000
0
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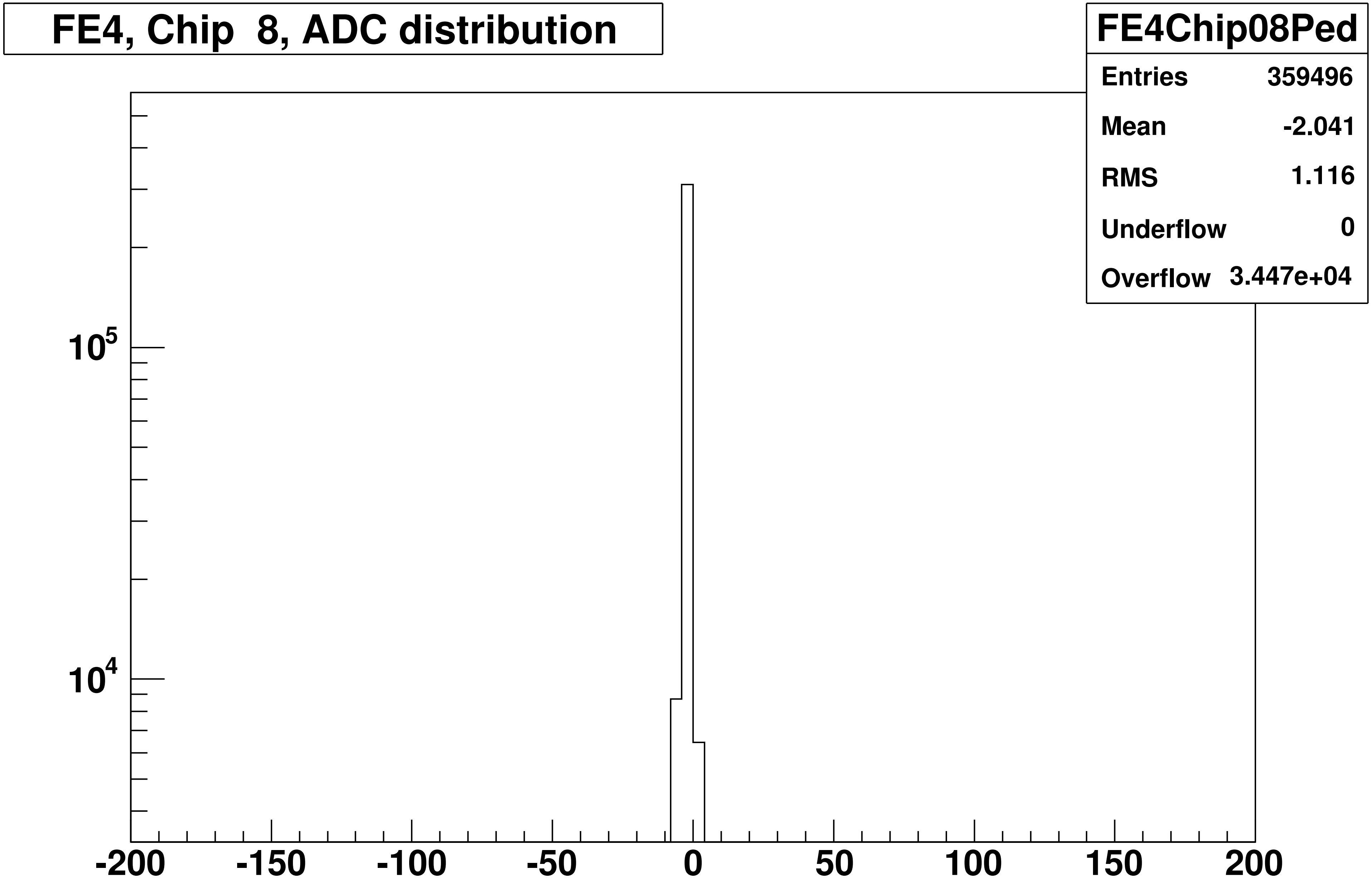
10000
15000
20000
25000


FE4, Chip 8, ADC distribution
FE4Chip08Ped
Entries 359496
Mean -2.041
RMS 1.116
Underflow 0
Overflow 3.447e+04
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10^4
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0
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100
150
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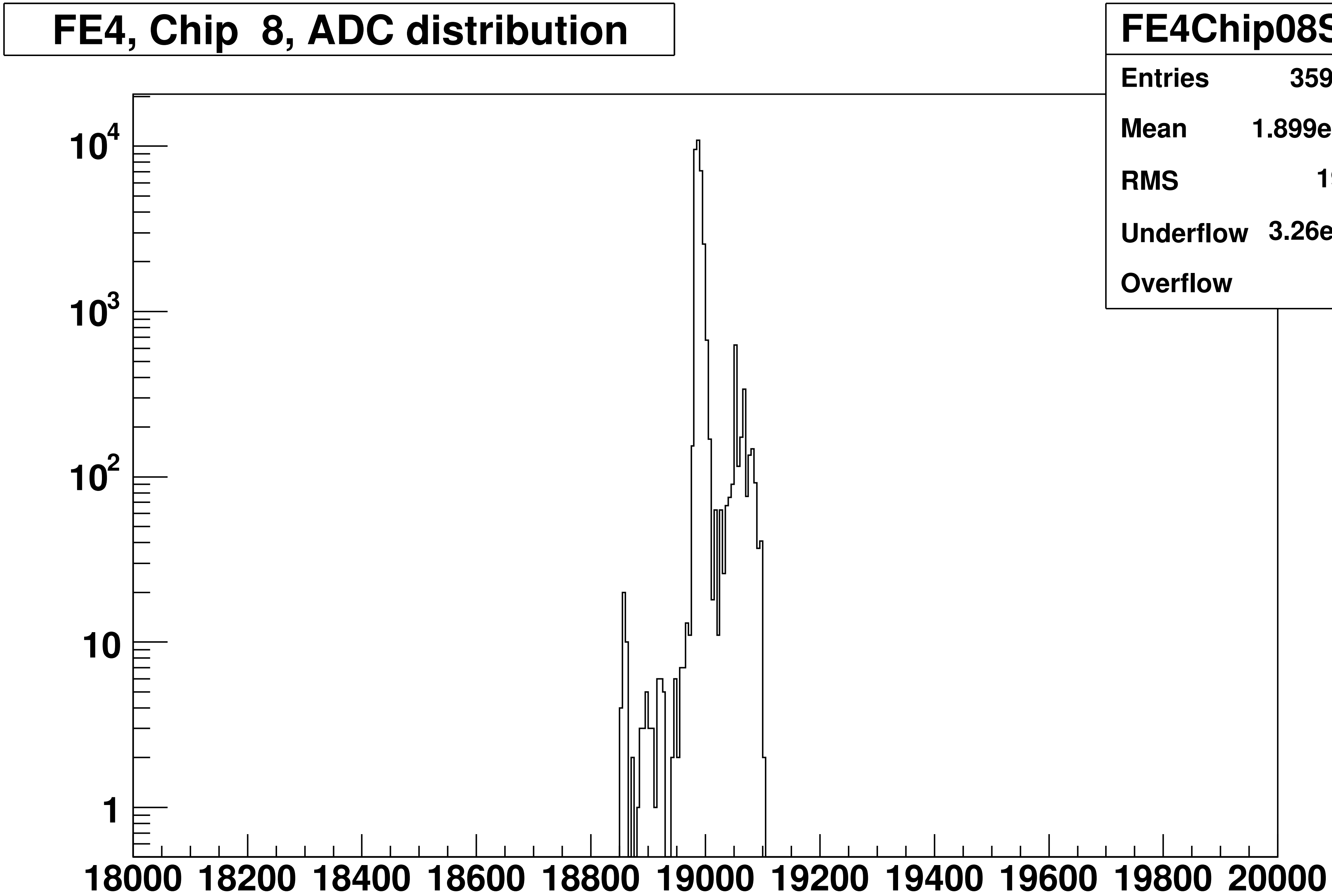

FE4, Chip 8, ADC distribution
FE4Chip08Sig
Entries 359496
Mean 1.899e+04
RMS 19.61
Underflow 3.26e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
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19000
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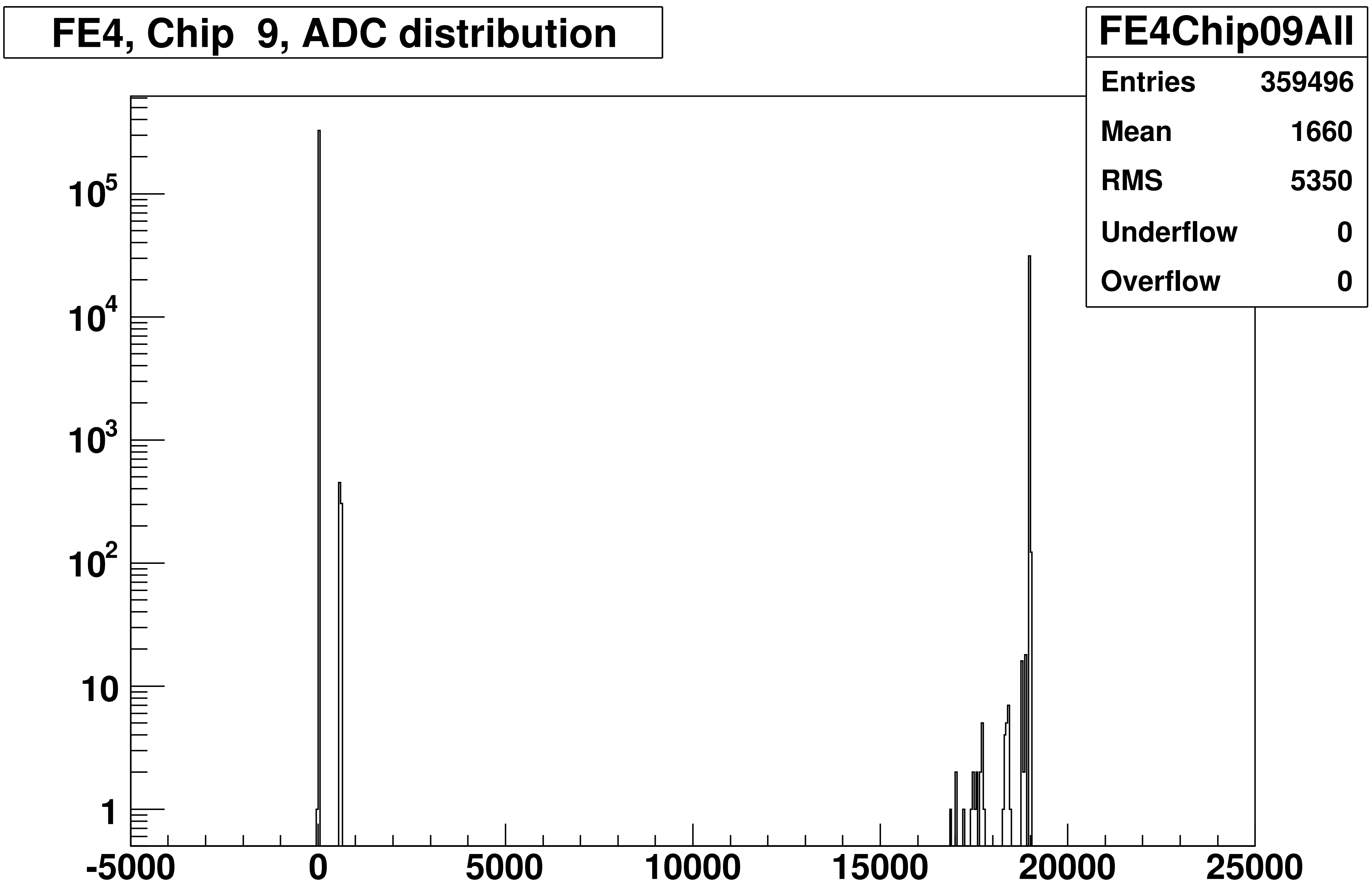
19600
19800
20000


FE4, Chip 9, ADC distribution
FE4Chip09All
Entries 359496
Mean 1660
RMS 5350
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
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-5000
0
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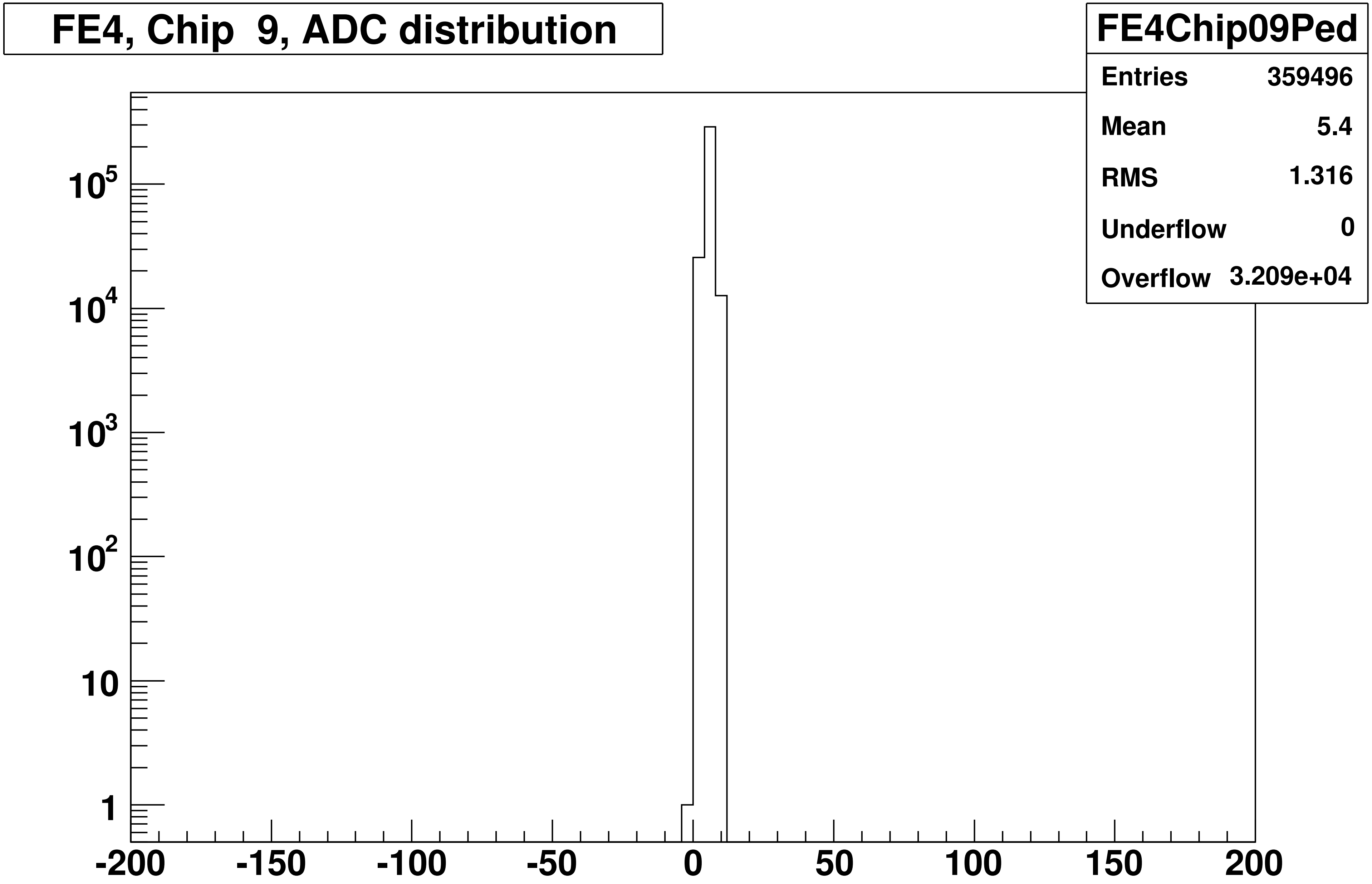
10000
15000
20000
25000



FE4, Chip 9, ADC distribution
FE4Chip09Ped
Entries 359496
Mean 5.4
RMS 1.316
Underflow 0
Overflow 3.209e+04
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10^4
10^3
10^2
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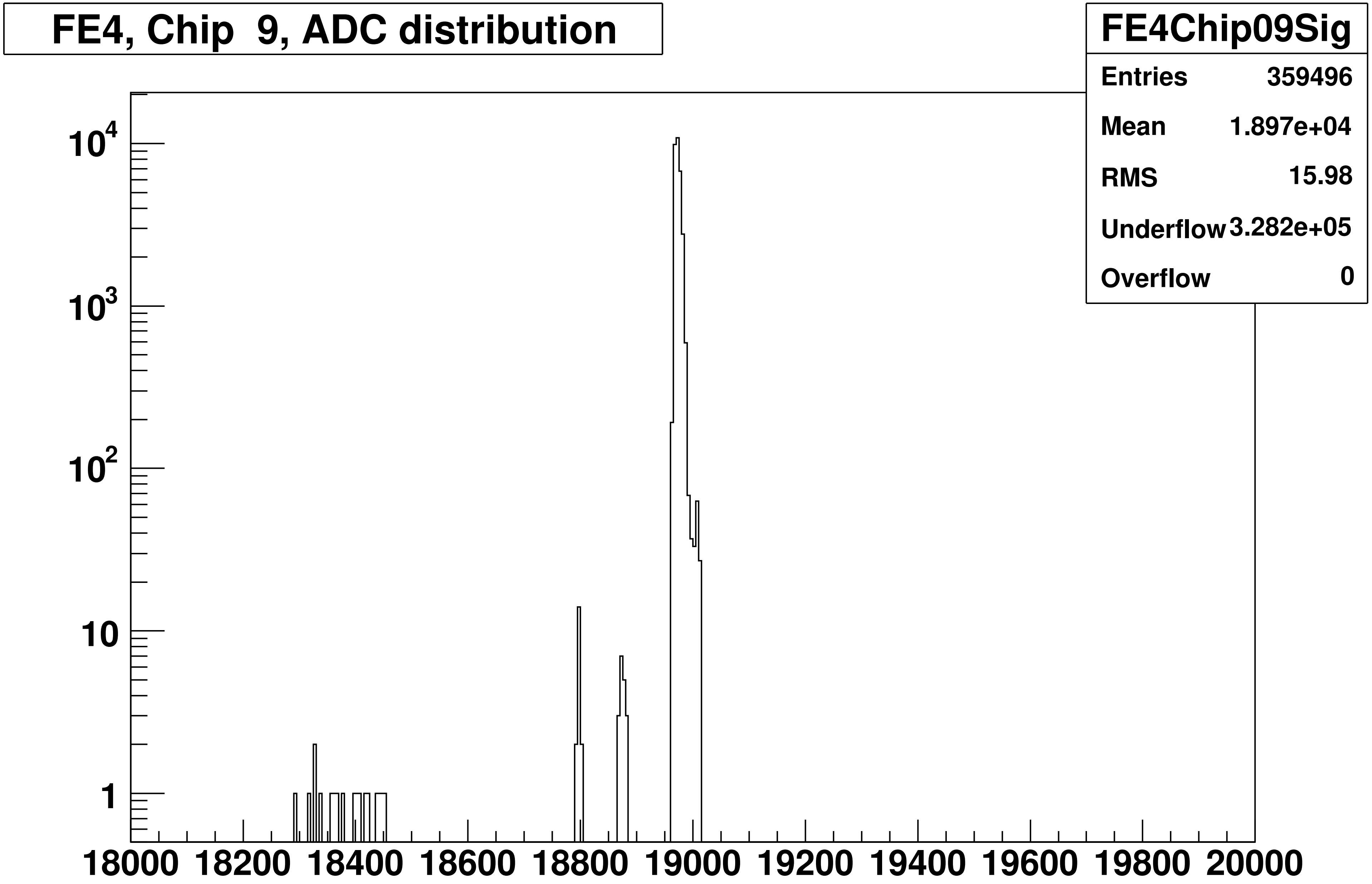
100
150
200


FE4, Chip 9, ADC distribution
FE4Chip09Sig
Entries 359496
Mean 1.897e+04
RMS 15.98
Underflow 3.282e+05
Overflow 0
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10^3
10^2
10
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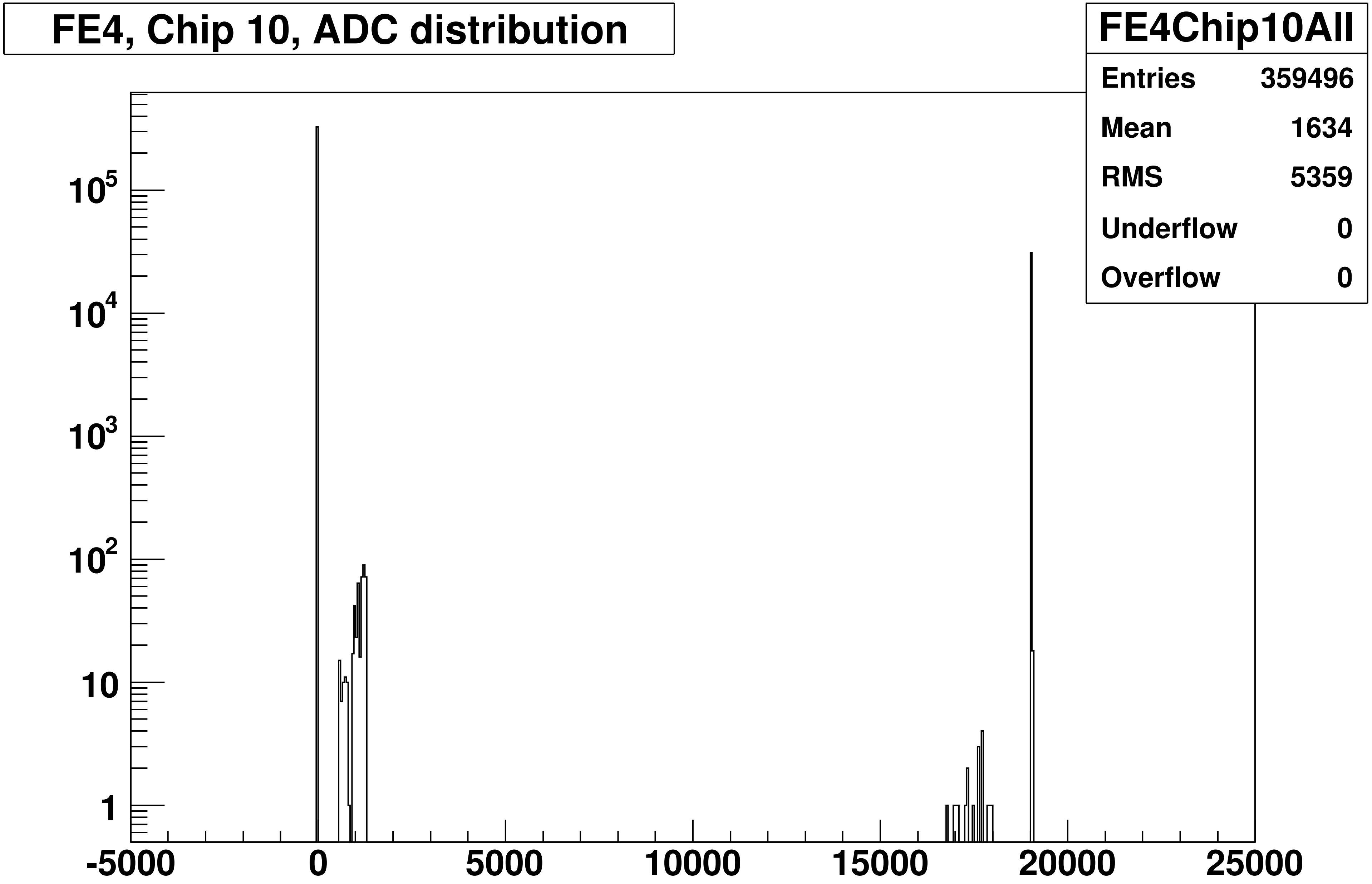
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE4, Chip 10, ADC distribution
FE4Chip10All
Entries 359496
Mean 1634
RMS 5359
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
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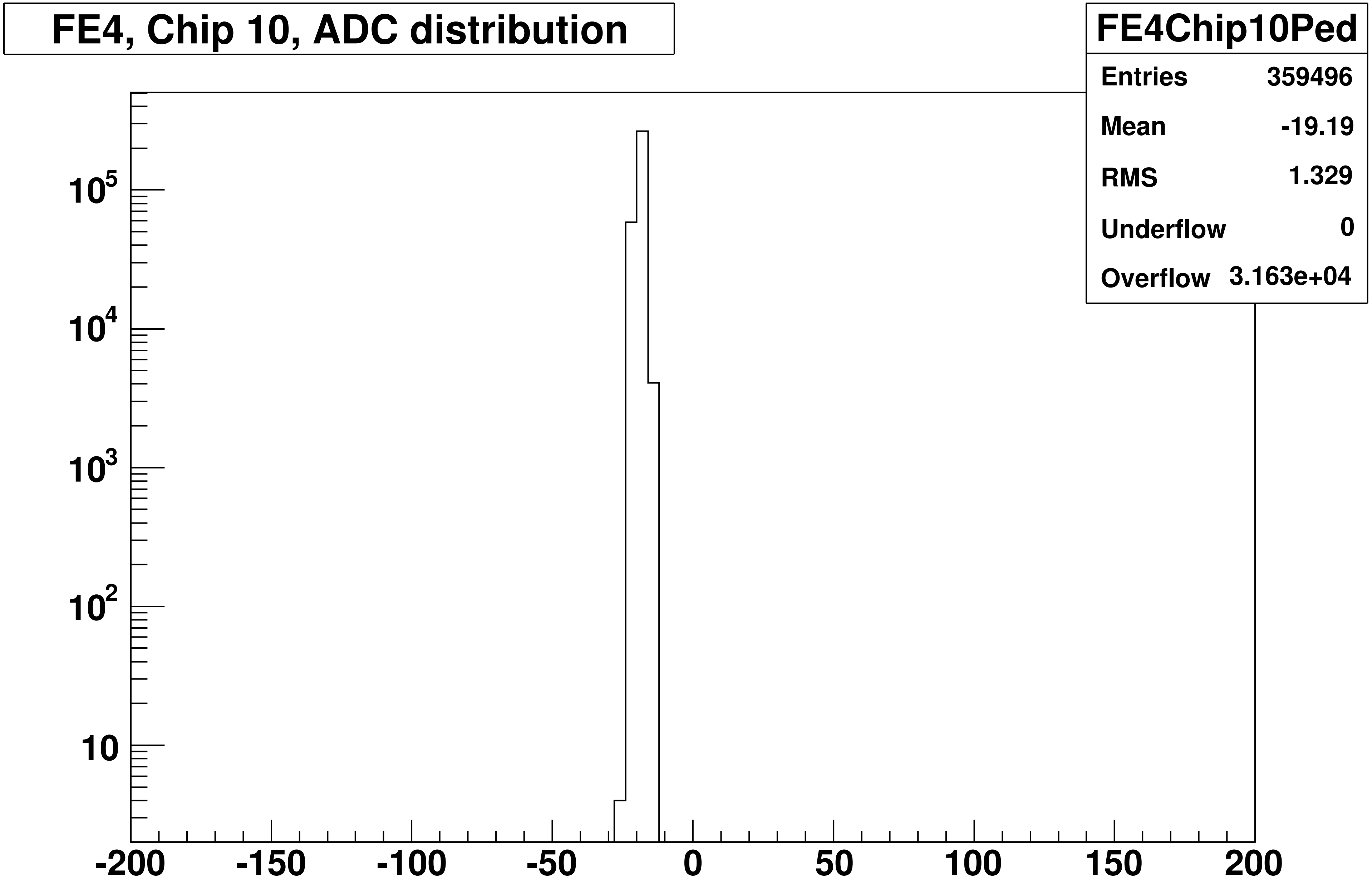
25000


FE4, Chip 10, ADC distribution
FE4Chip10Ped
Entries 359496
Mean -19.19
RMS 1.329
Underflow 0
Overflow 3.163e+04
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10^2
10^3
10^4
10^5
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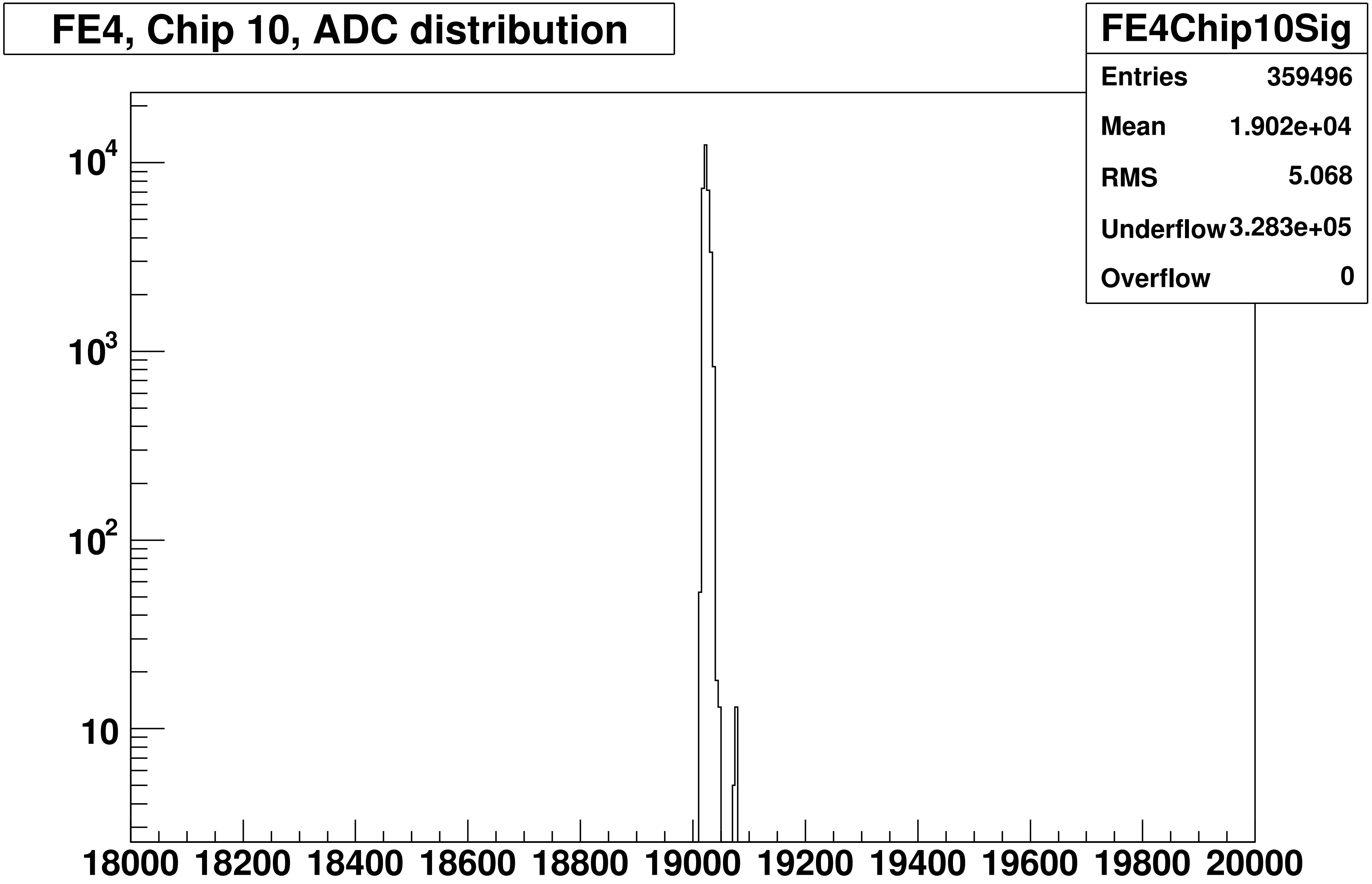
100
150
200


FE4, Chip 10, ADC distribution
FE4Chip10Sig
Entries 359496
Mean 1.902e+04
RMS 5.068
Underflow 3.283e+05
Overflow 0
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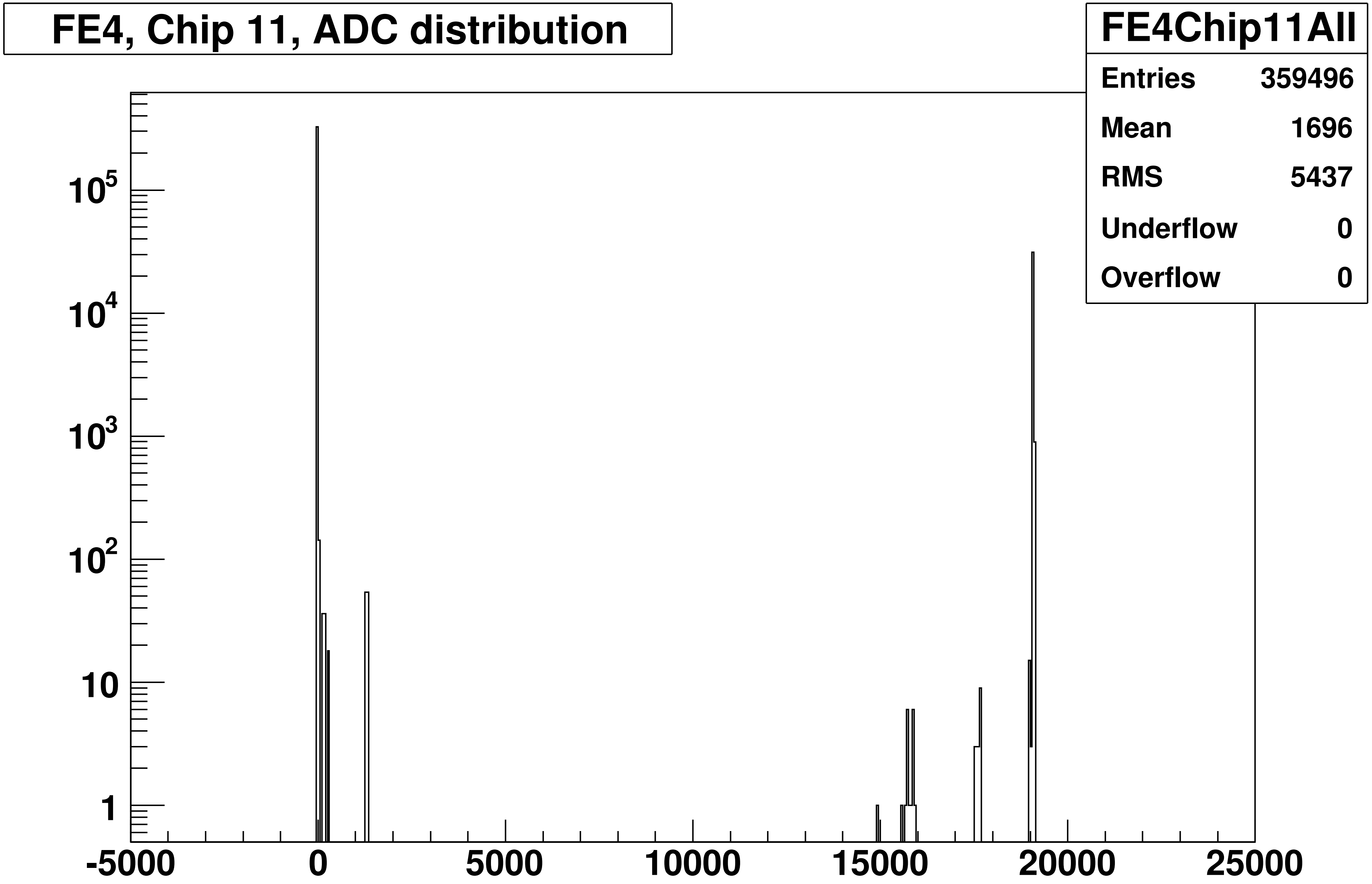
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE4, Chip 11, ADC distribution
FE4Chip11All
Entries 359496
Mean 1696
RMS 5437
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
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10000
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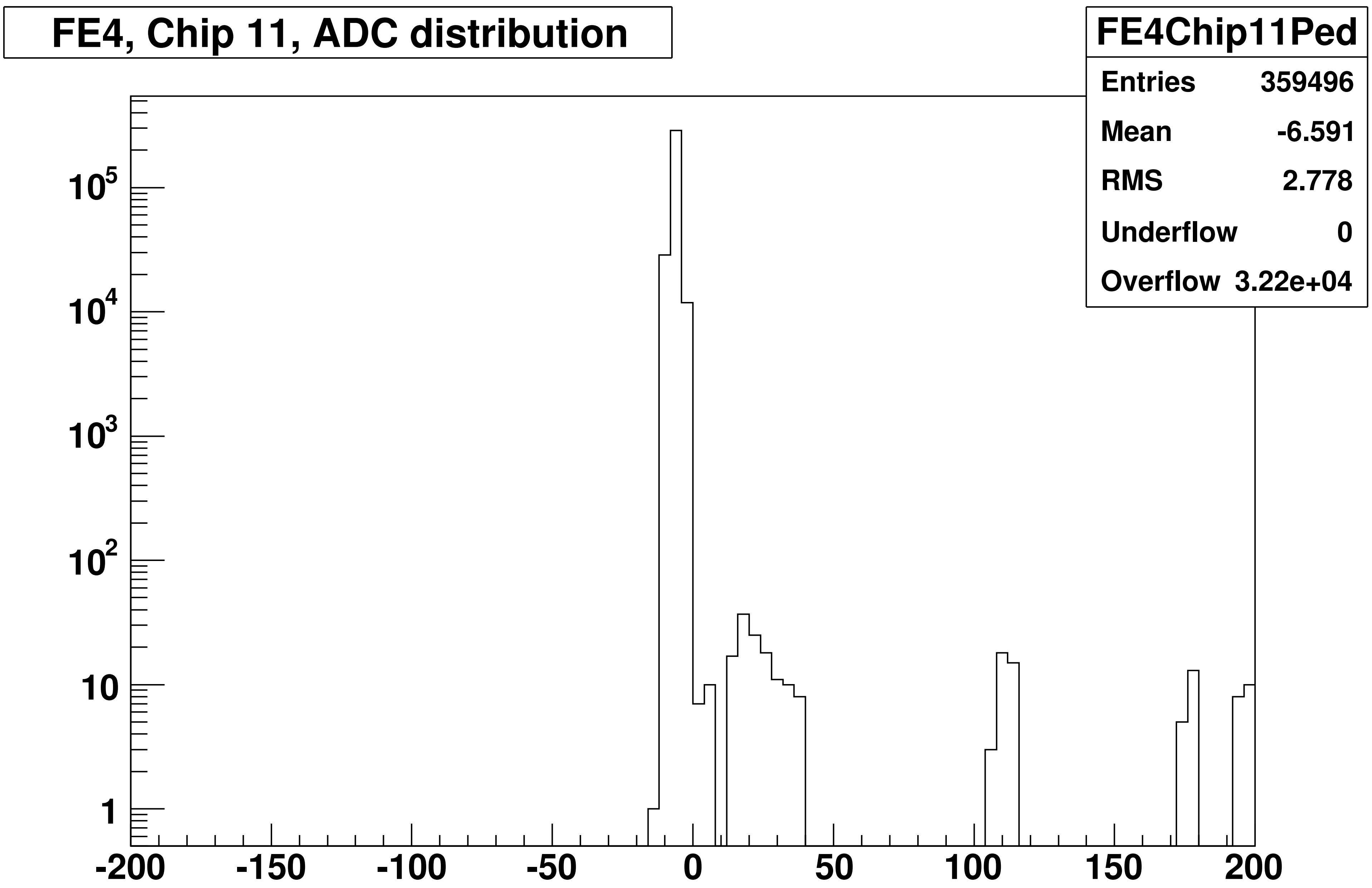
20000
25000



FE4, Chip 11, ADC distribution
FE4Chip11Ped
Entries 359496
Mean -6.591
RMS 2.778
Underflow 0
Overflow 3.22e+04
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10^4
10^3
10^2
10
1
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-150
-100
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150
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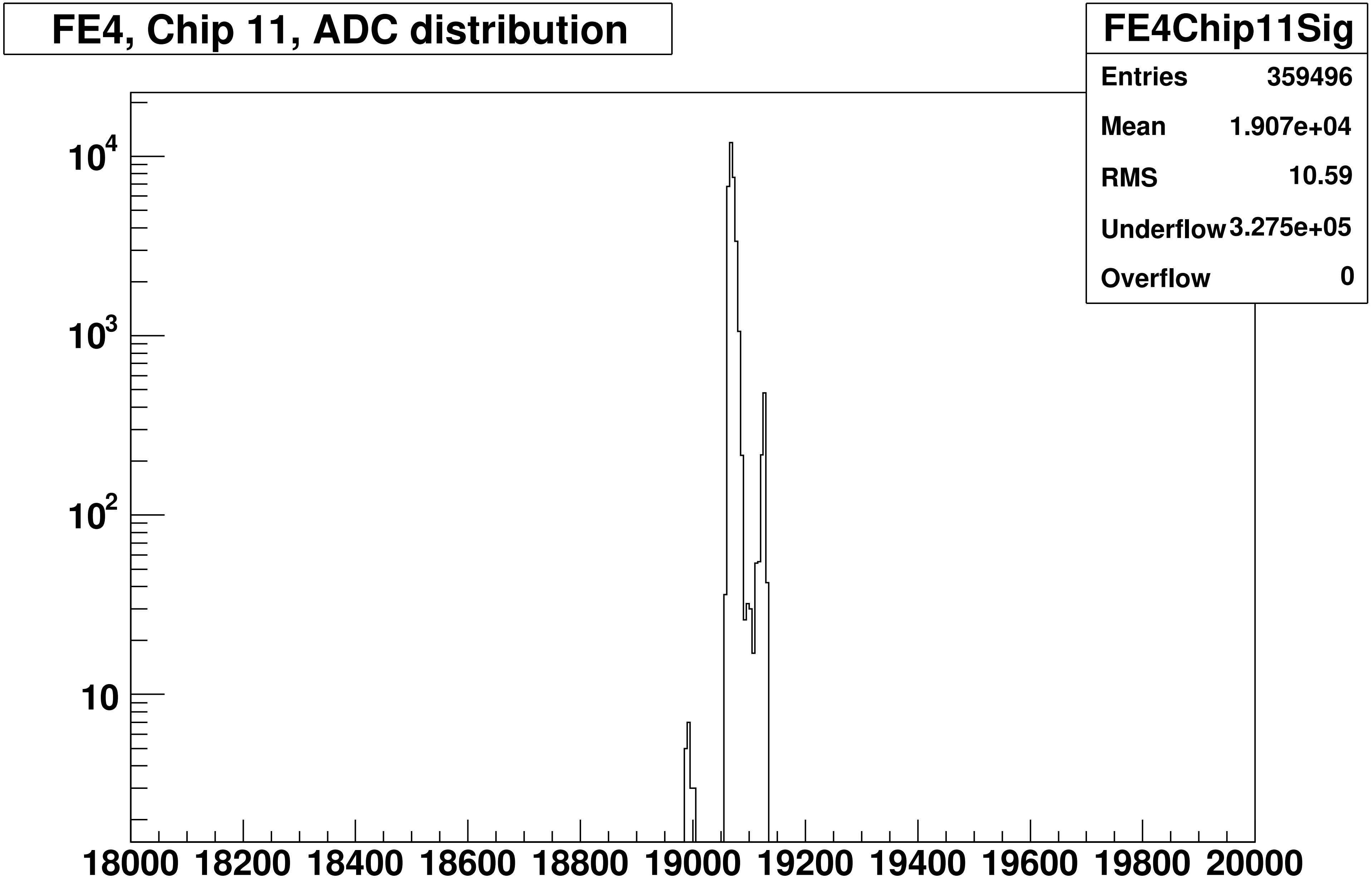
FE4, Chip 11, ADC distribution
FE4Chip11Sig
Entries 359496
Mean 1.907e+04
RMS 10.59
Underflow 3.275e+05
Overflow 0
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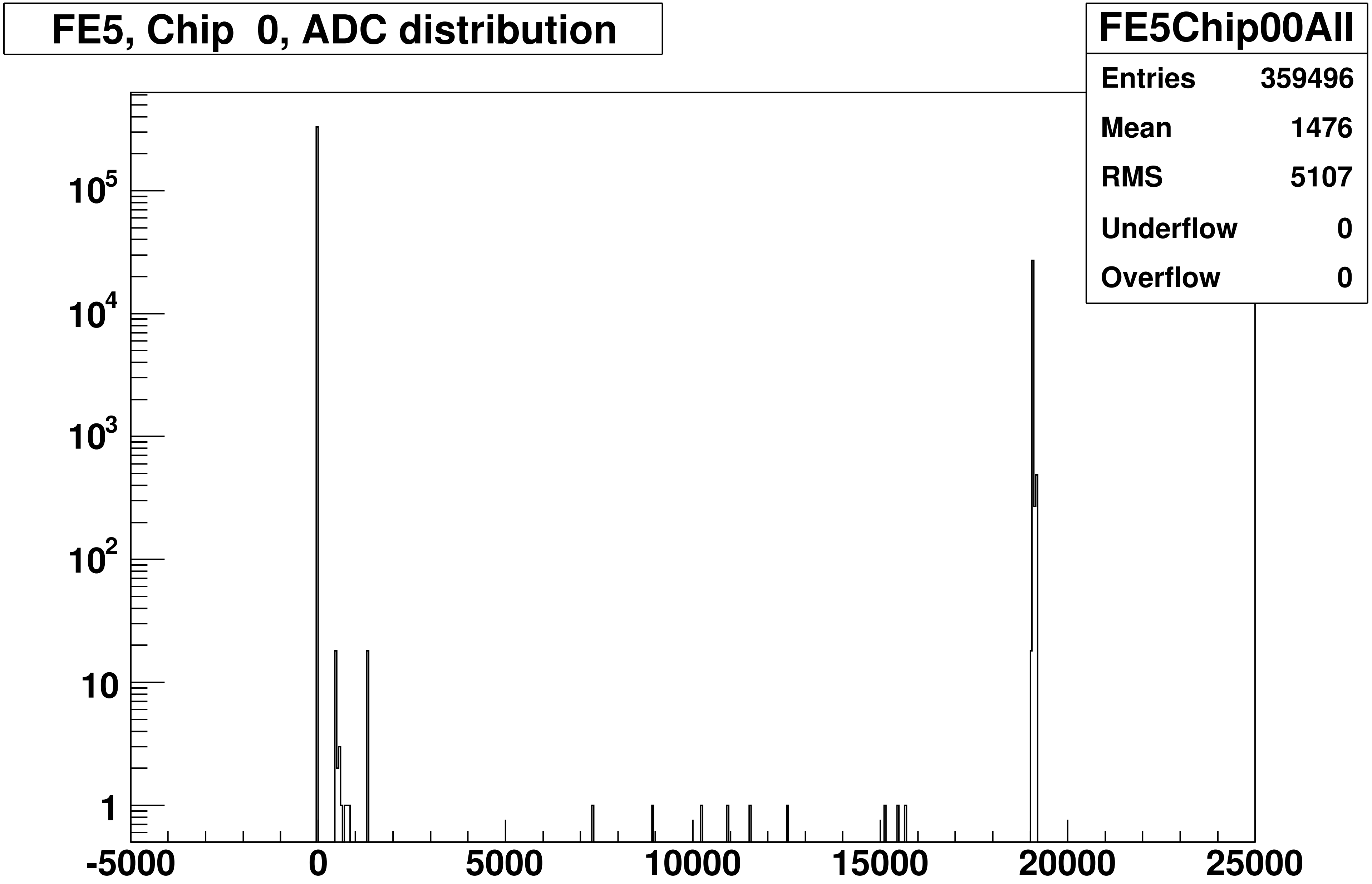
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE5, Chip 0, ADC distribution
FE5Chip00All
Entries 359496
Mean 1476
RMS 5107
Underflow 0
Overflow 0
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10^4
10^3
10^2
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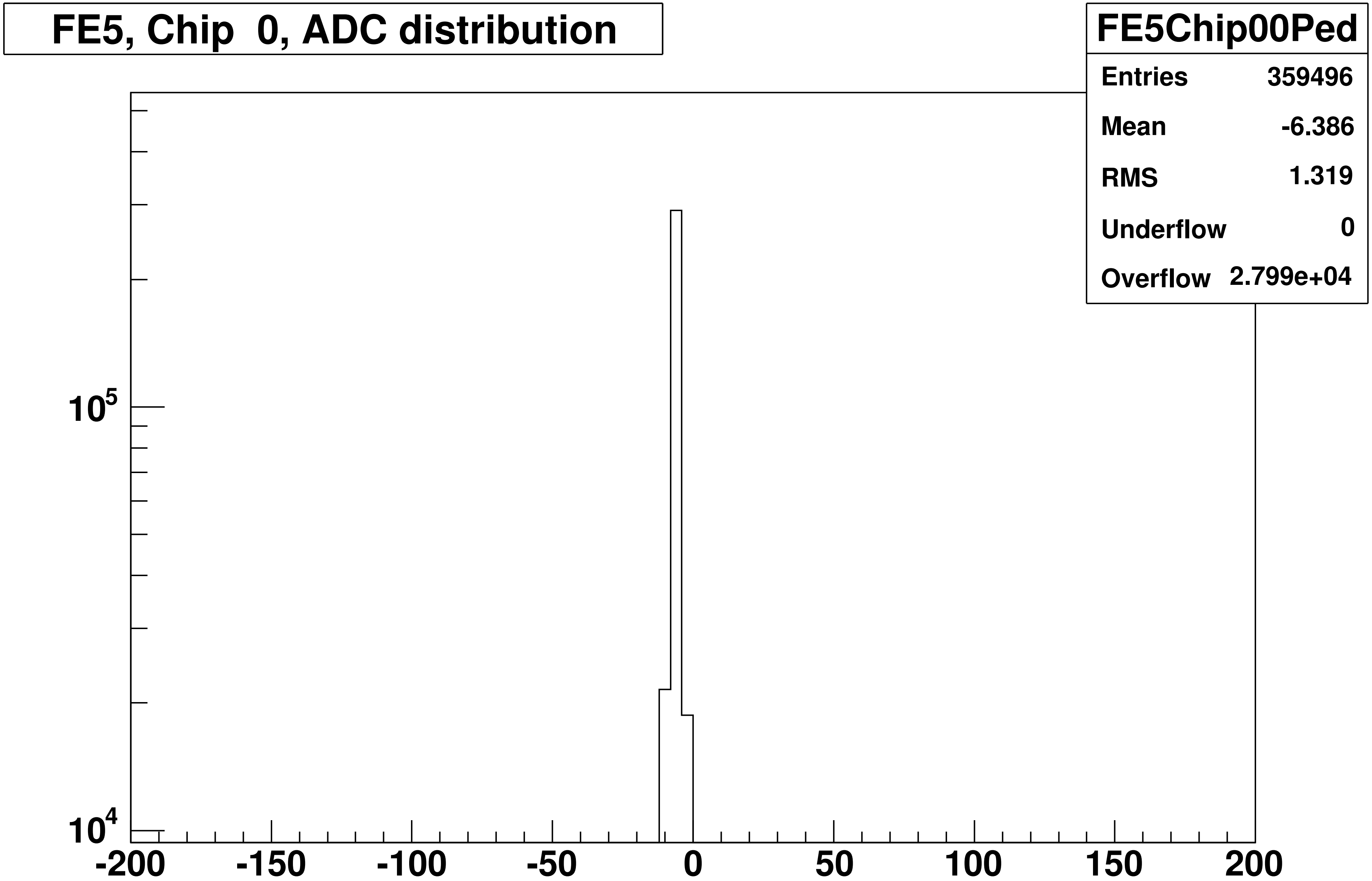
FE5, Chip 0, ADC distribution
FE5Chip00Ped
Entries 359496
Mean -6.386
RMS 1.319
Underflow 0
Overflow 2.799e+04
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10^4
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150
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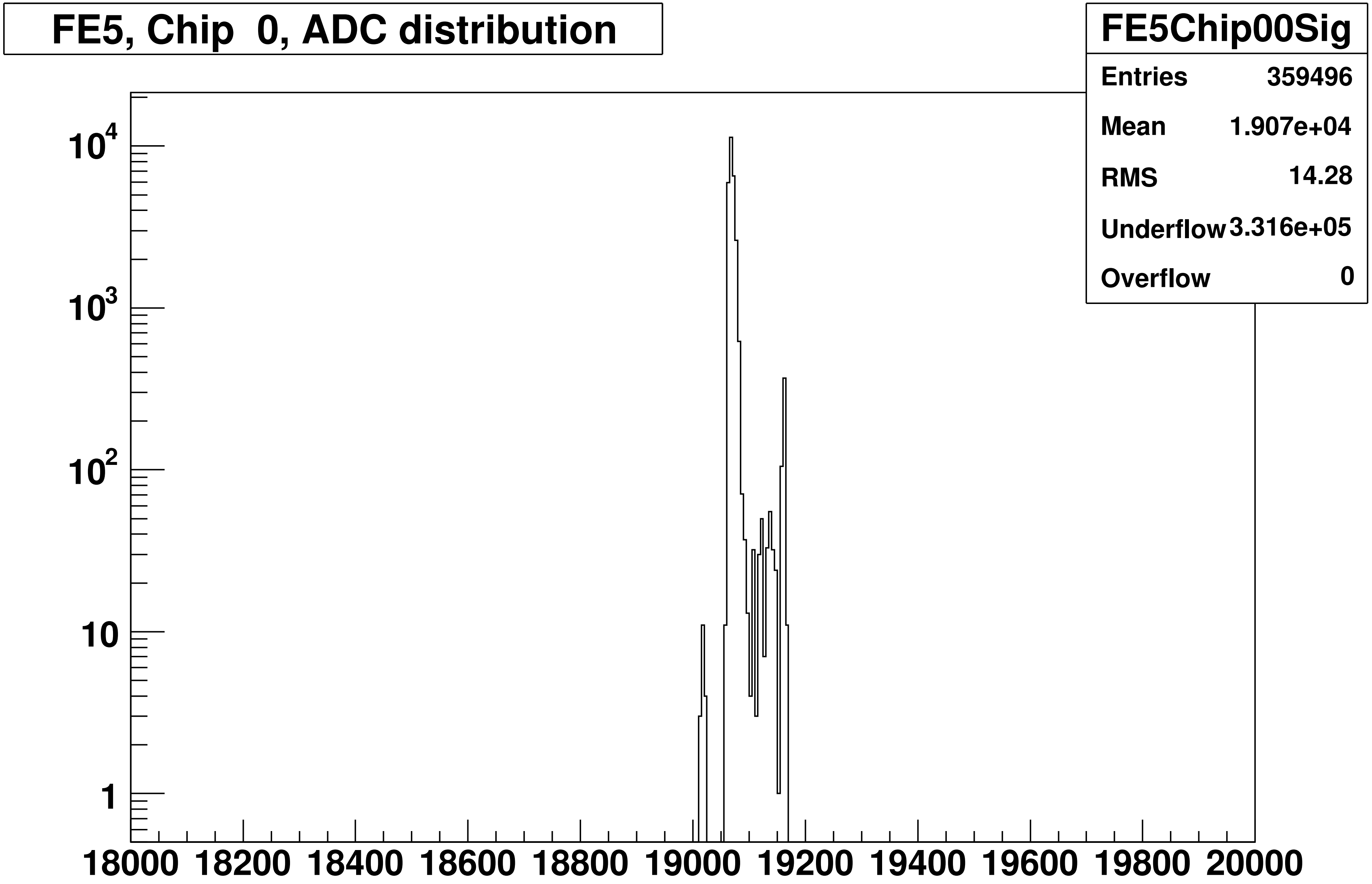

FE5, Chip 0, ADC distribution
FE5Chip00Sig
Entries 359496
Mean 1.907e+04
RMS 14.28
Underflow 3.316e+05
Overflow 0
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10^3
10^2
10
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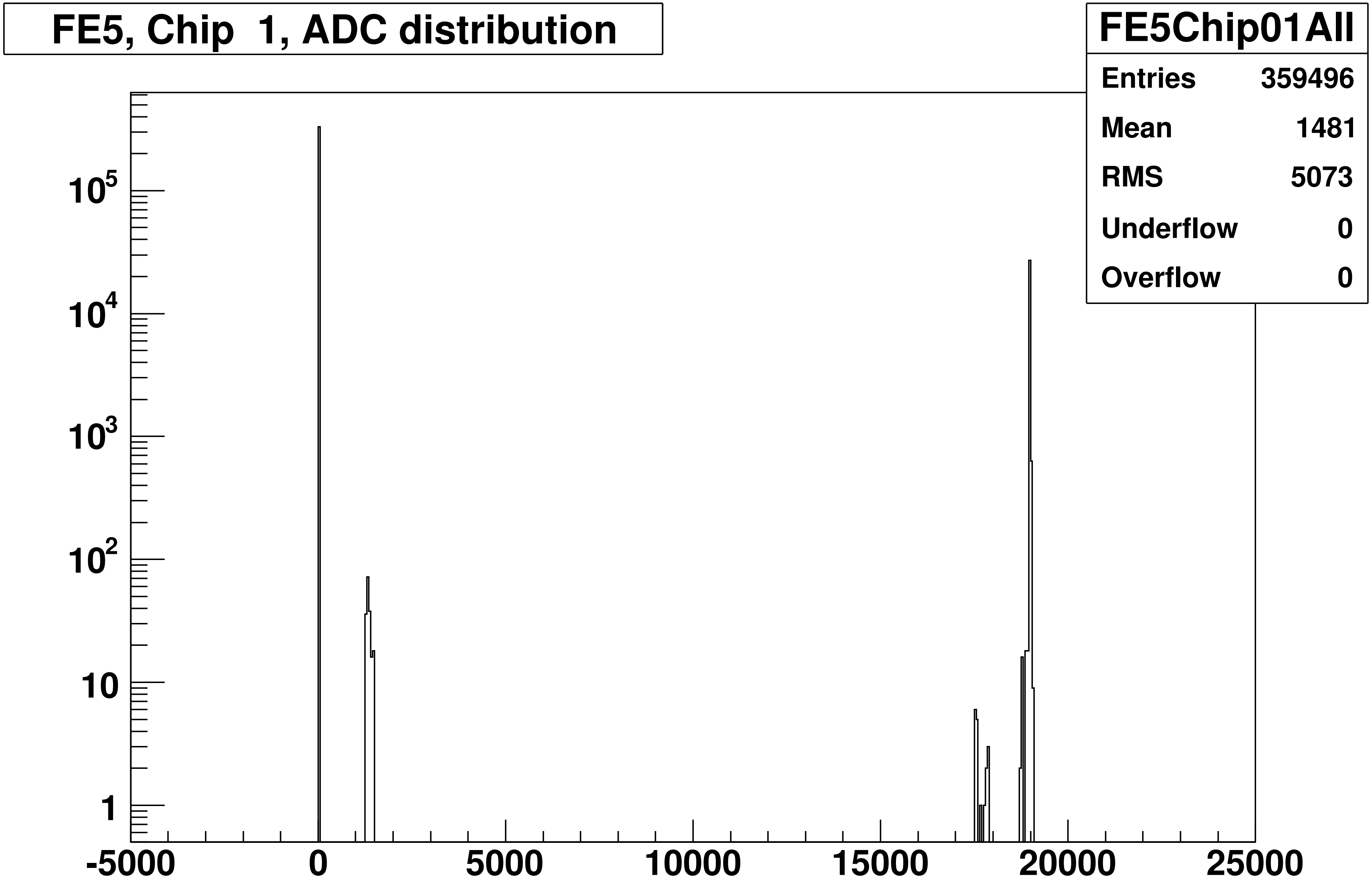
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE5, Chip 1, ADC distribution
FE5Chip01All
Entries 359496
Mean 1481
RMS 5073
Underflow 0
Overflow 0
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10^4
10^3
10^2
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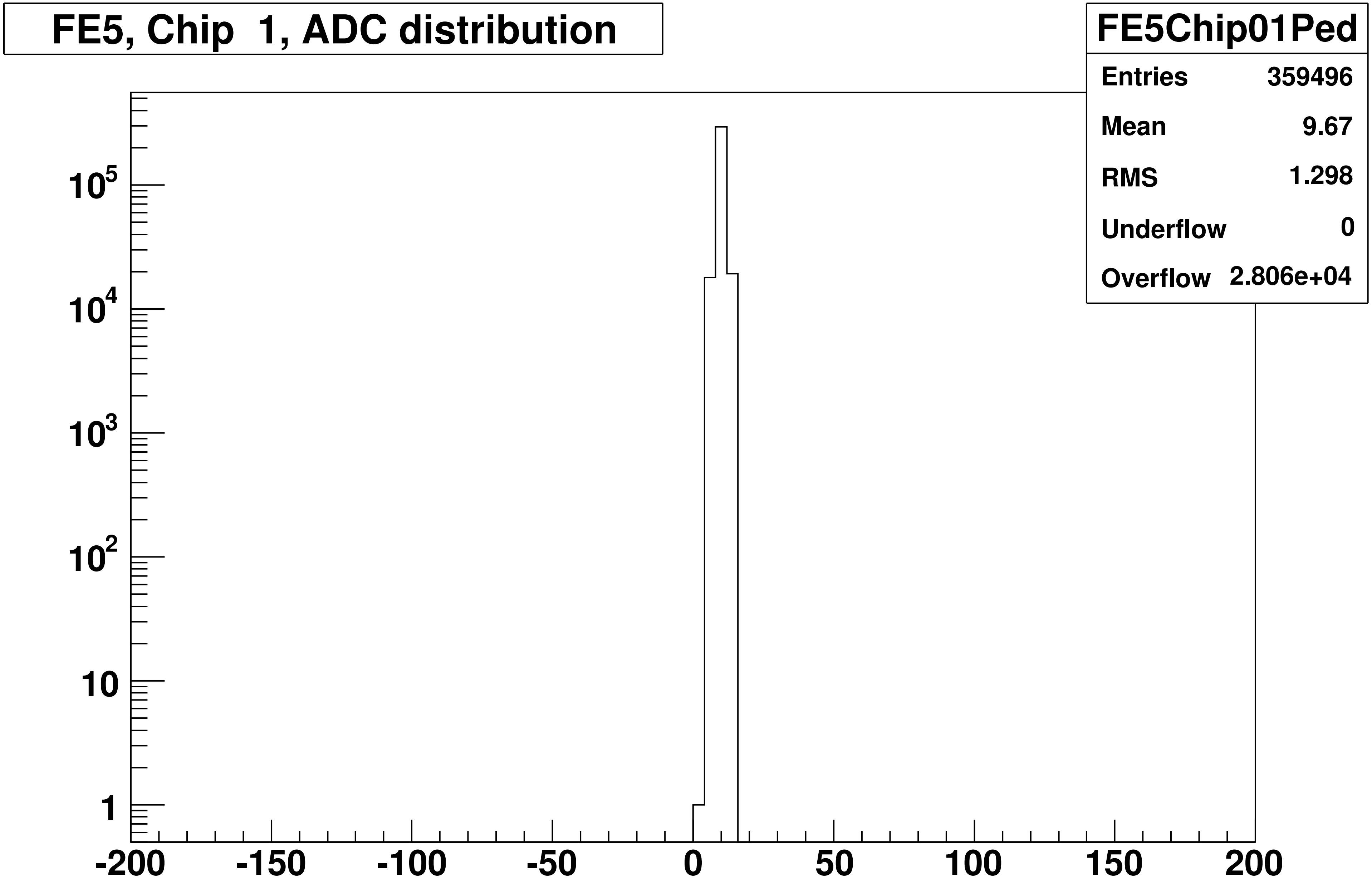

FE5, Chip 1, ADC distribution
FE5Chip01Ped
Entries 359496
Mean 9.67
RMS 1.298
Underflow 0
Overflow 2.806e+04
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10^3
10^2
10
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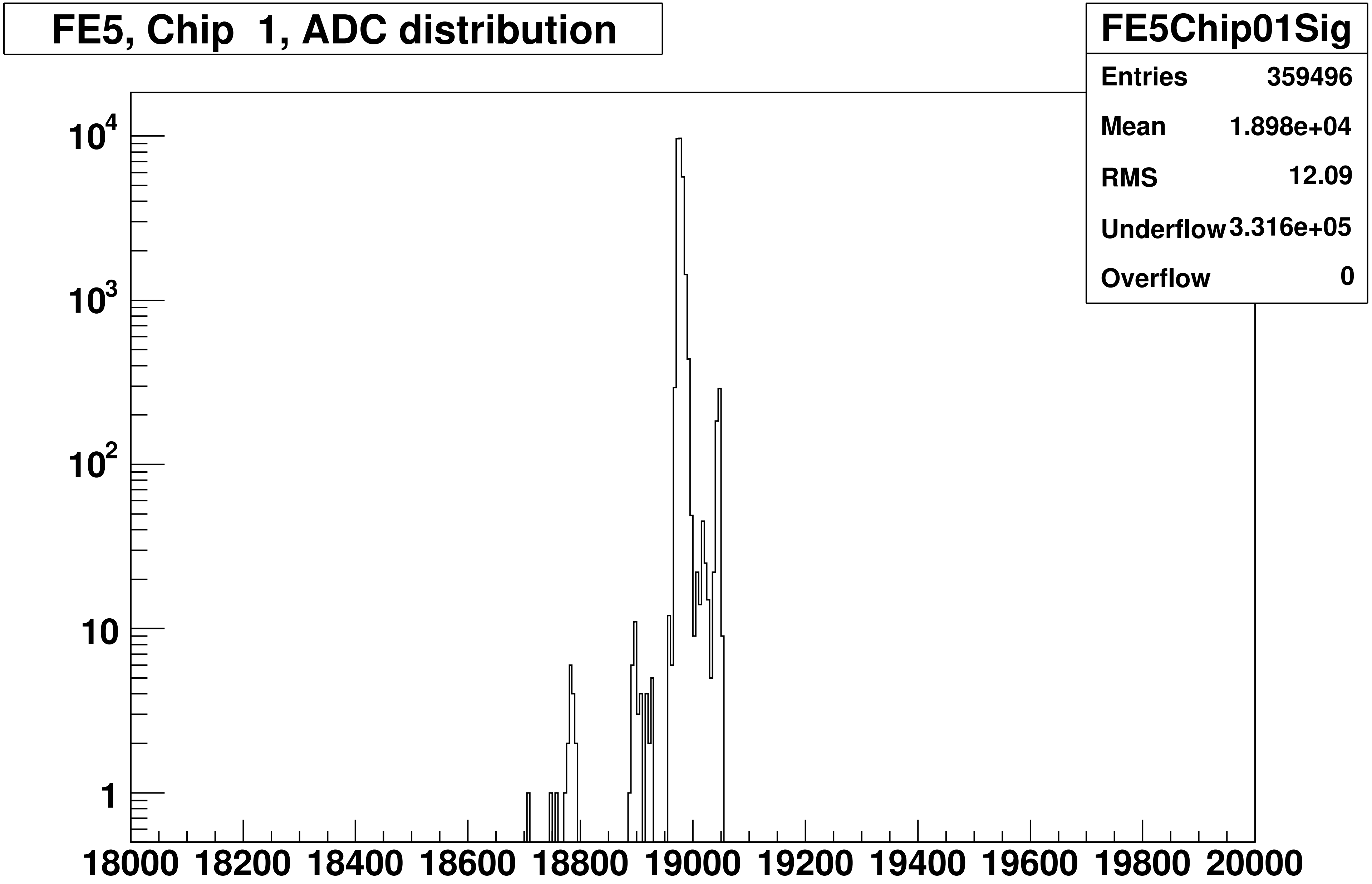

FE5, Chip 1, ADC distribution
FE5Chip01Sig
Entries 359496
Mean 1.898e+04
RMS 12.09
Underflow 3.316e+05
Overflow 0
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10^3
10^2
10
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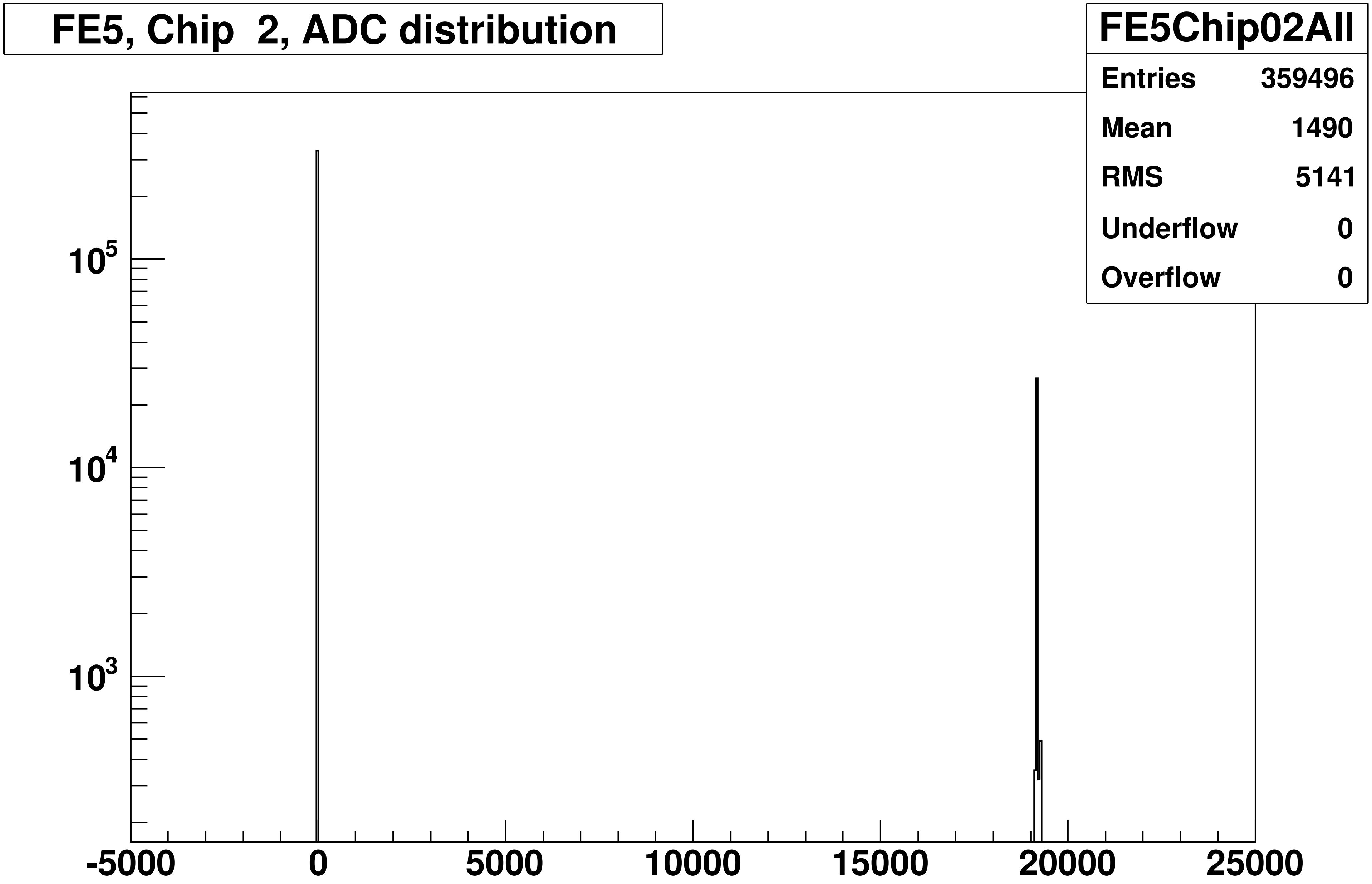
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE5, Chip 2, ADC distribution
FE5Chip02All
Entries 359496
Mean 1490
RMS 5141
Underflow 0
Overflow 0
10^5
10^4
10^3
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0
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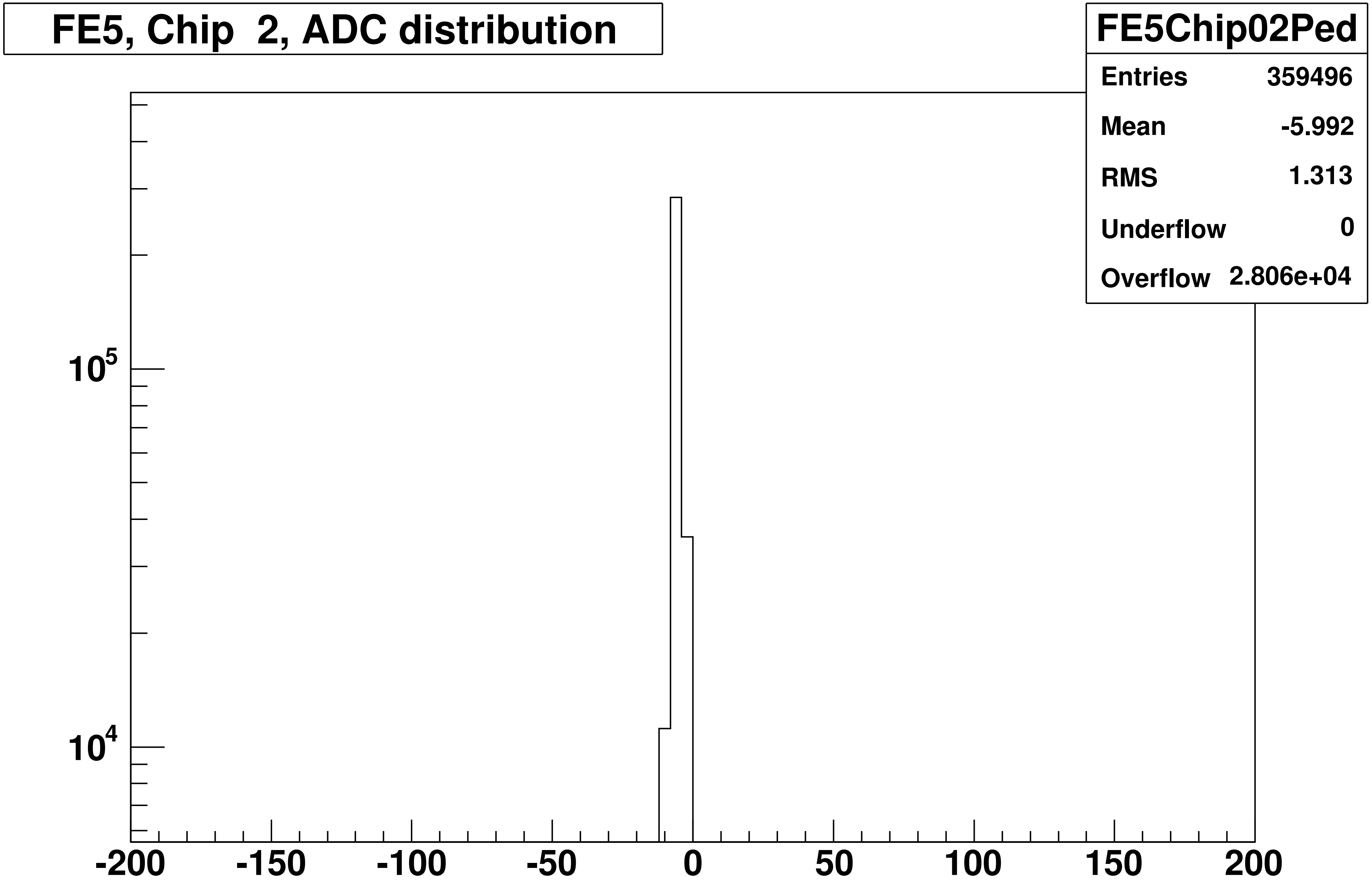
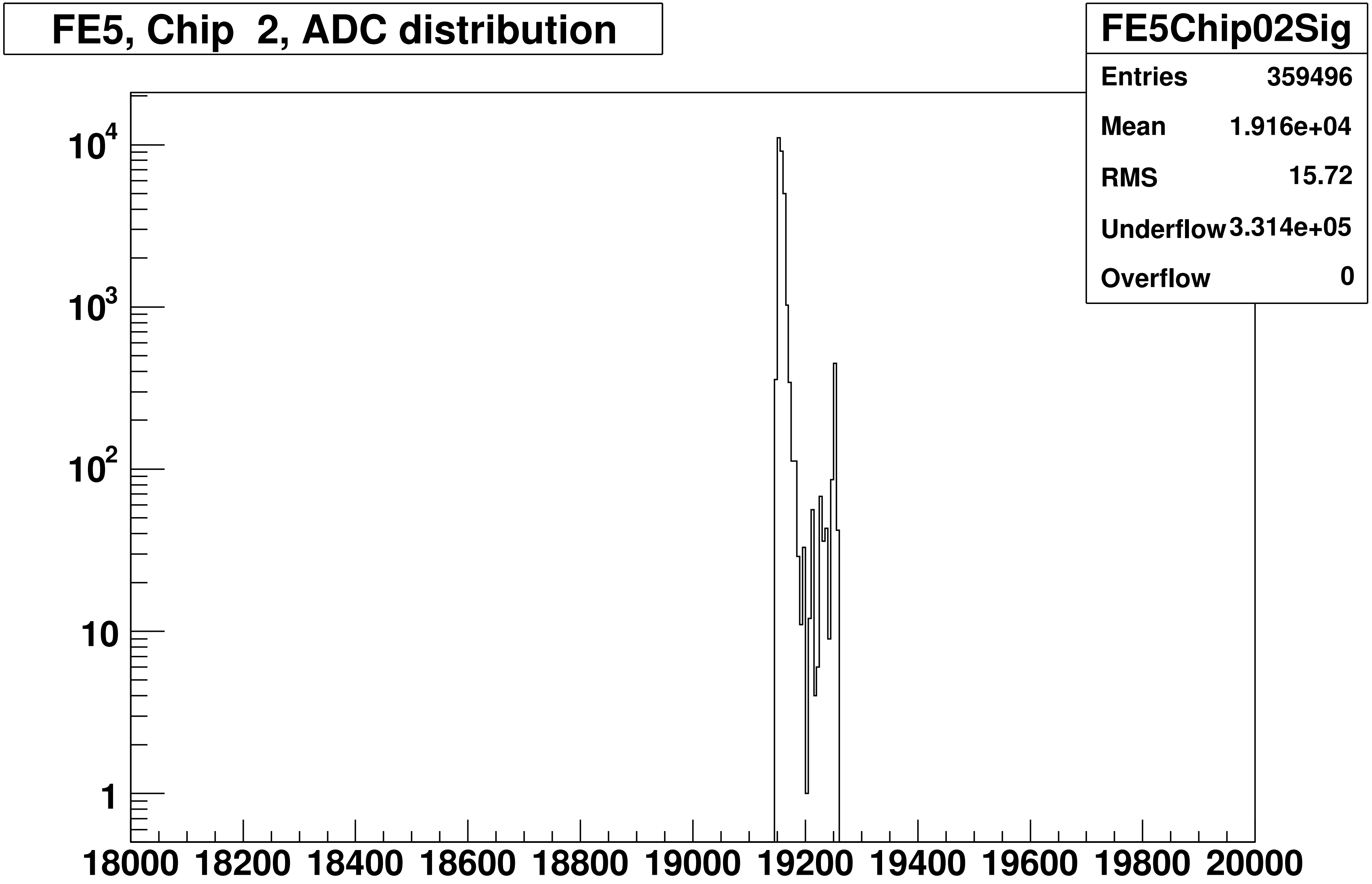
15000
20000
25000


FE5, Chip 2, ADC distribution
FE5Chip02Ped
Entries 359496
Mean -5.992
RMS 1.313
Underflow 0
Overflow 2.806e+04
10^5
10^4
-200
-150
-100
-50
0
50
100
150
200



FE5, Chip 2, ADC distribution
FE5Chip02Sig
Entries 359496
Mean 1.916e+04
RMS 15.72
Underflow 3.314e+05
Overflow 0
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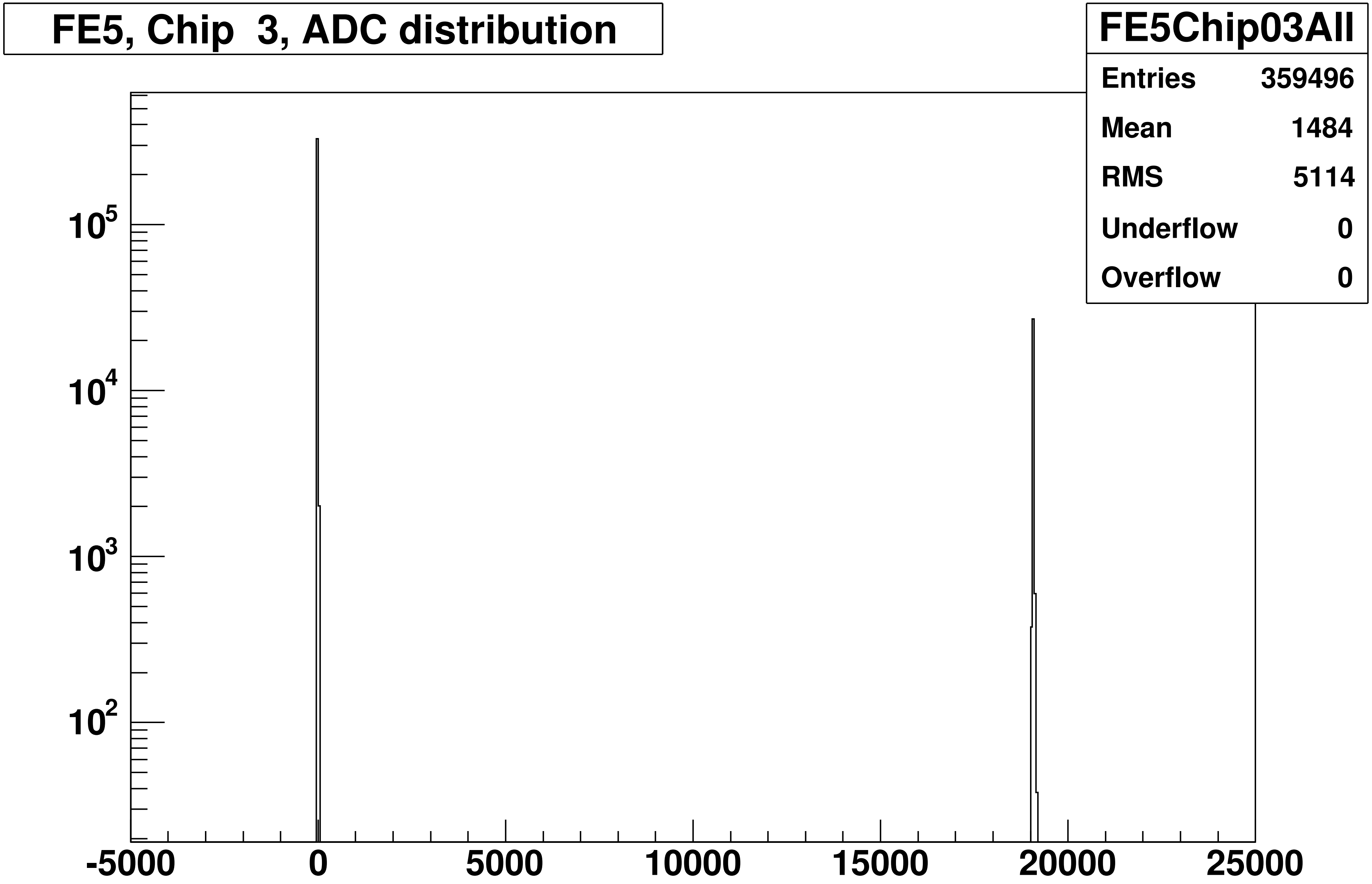
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE5, Chip 3, ADC distribution
FE5Chip03All
Entries 359496
Mean 1484
RMS 5114
Underflow 0
Overflow 0
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10^3
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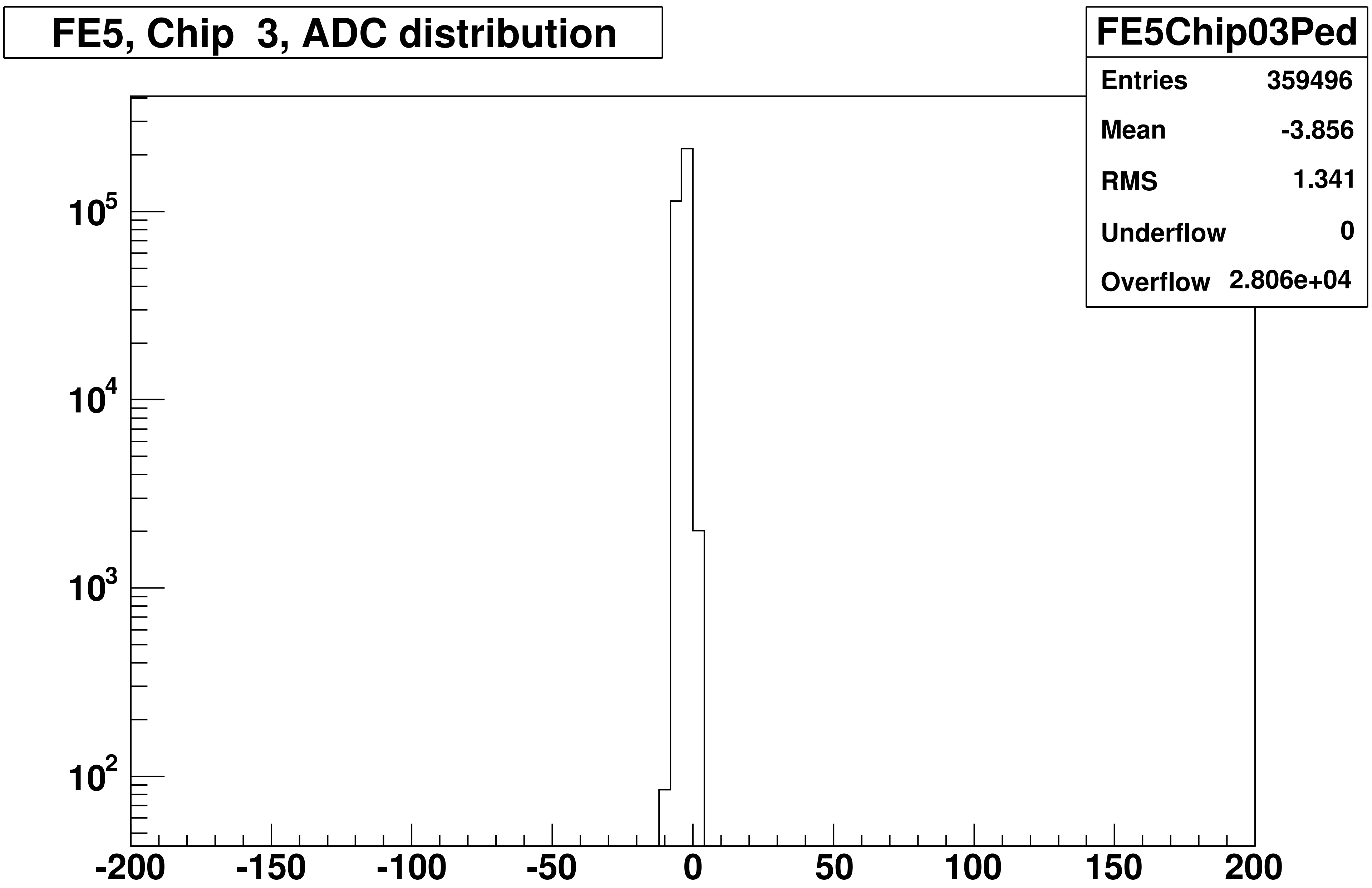
25000


FE5, Chip 3, ADC distribution
FE5Chip03Ped
Entries 359496
Mean -3.856
RMS 1.341
Underflow 0
Overflow 2.806e+04
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10^4
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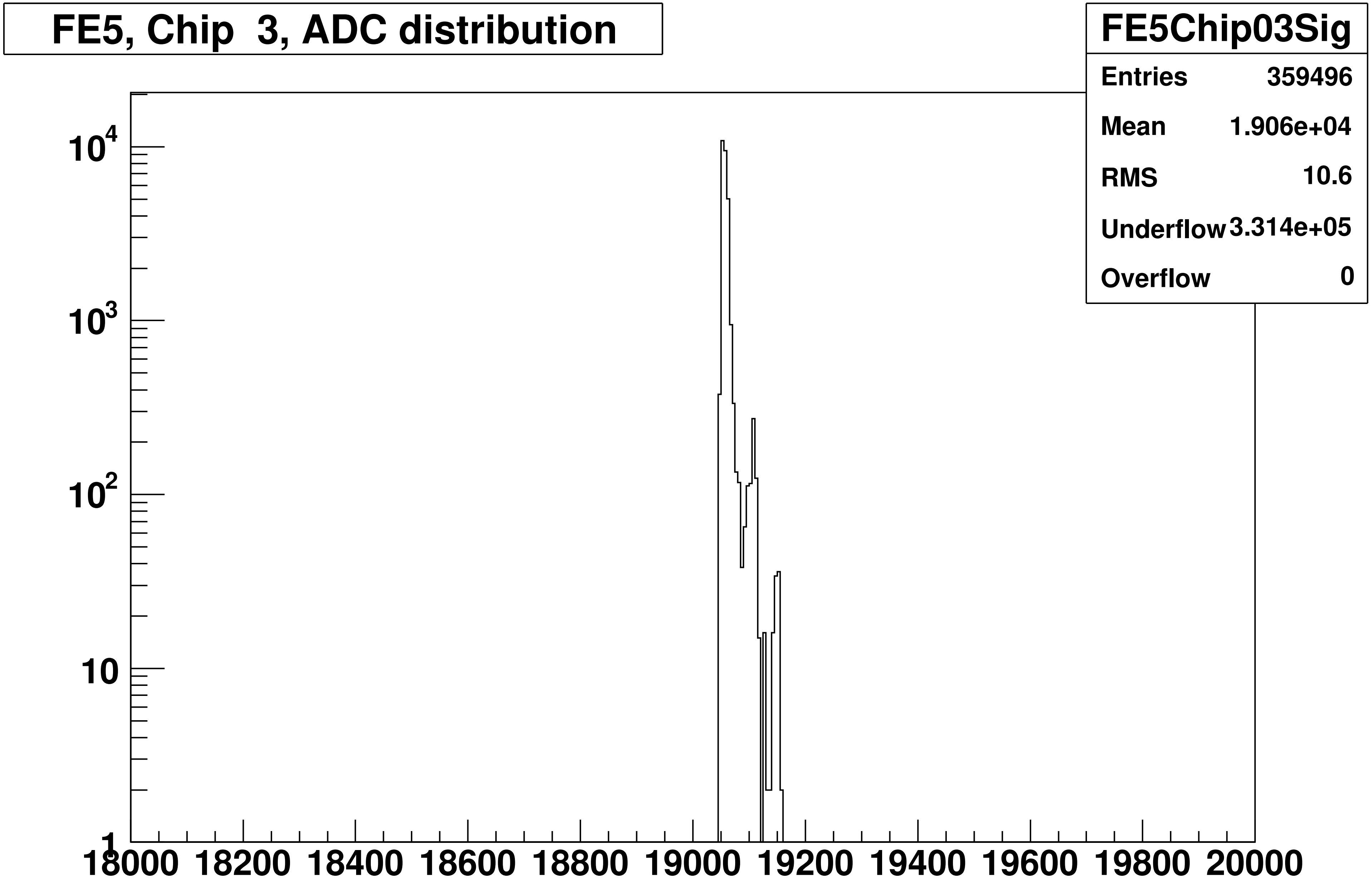
150
200


FE5, Chip 3, ADC distribution
FE5Chip03Sig
Entries 359496
Mean 1.906e+04
RMS 10.6
Underflow 3.314e+05
Overflow 0
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10^3
10^2
10
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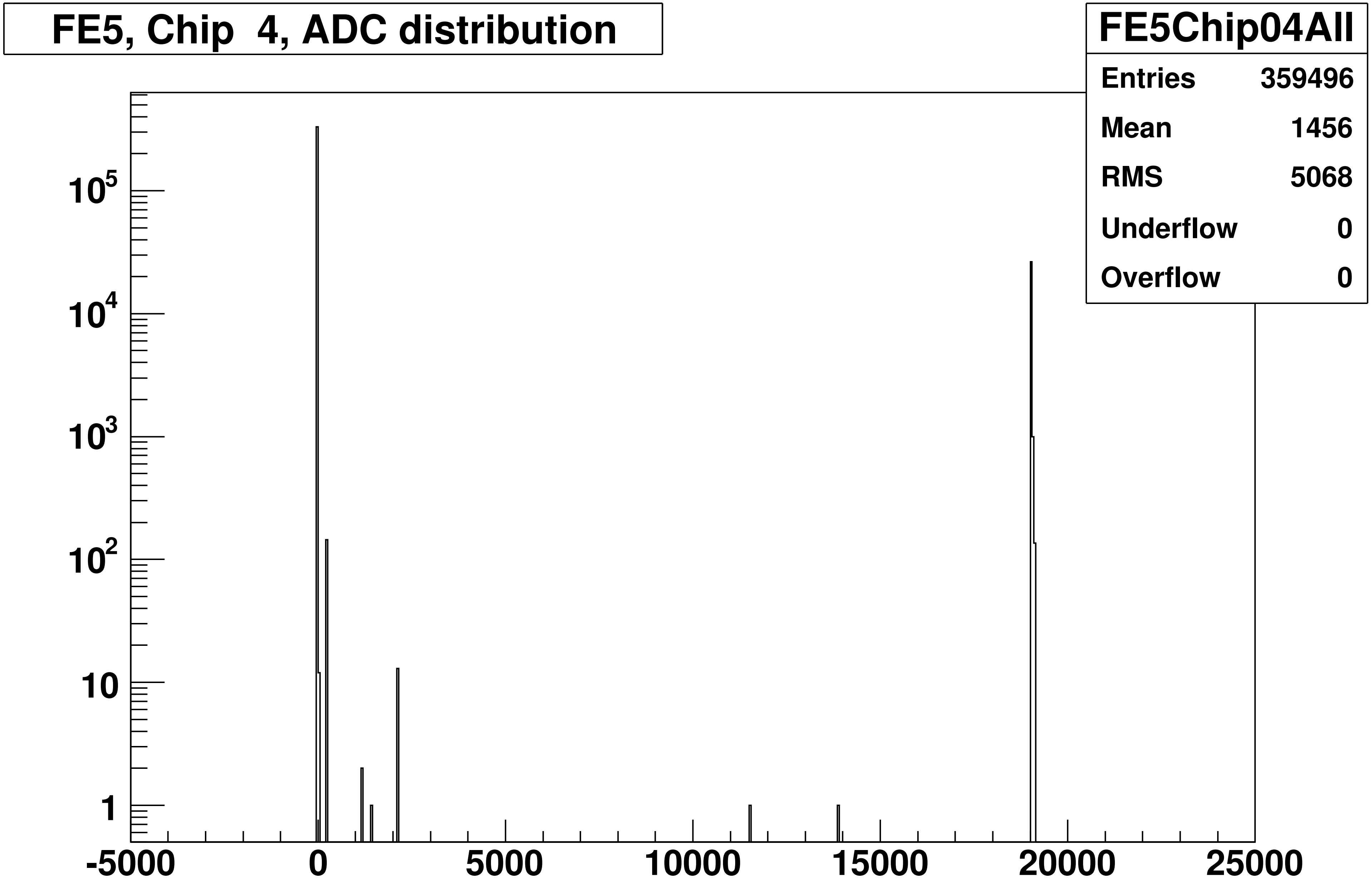
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE5, Chip 4, ADC distribution
FE5Chip04All
Entries 359496
Mean 1456
RMS 5068
Underflow 0
Overflow 0
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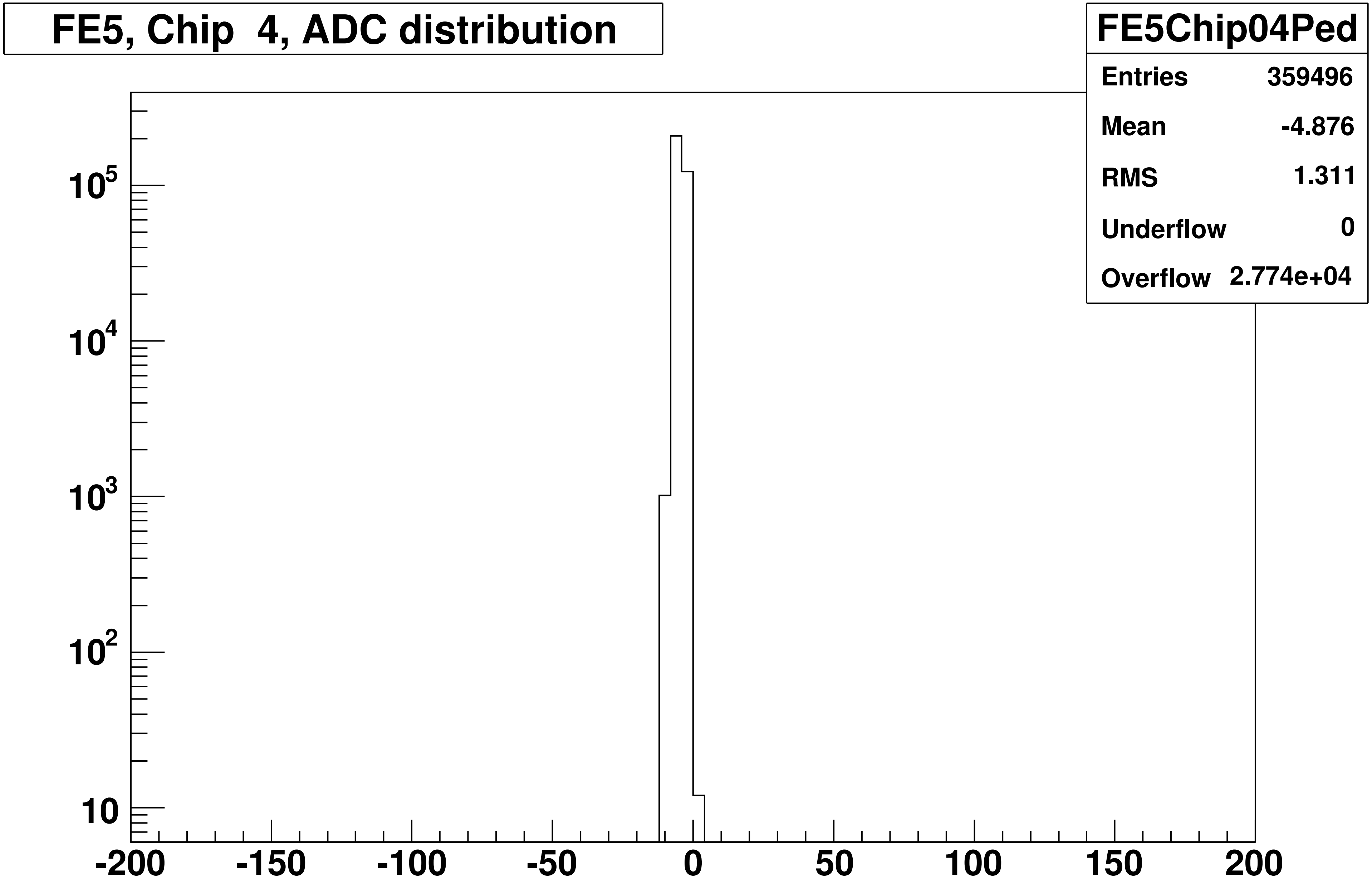
FE5, Chip 4, ADC distribution
FE5Chip04Ped
Entries 359496
Mean -4.876
RMS 1.311
Underflow 0
Overflow 2.774e+04
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10^3
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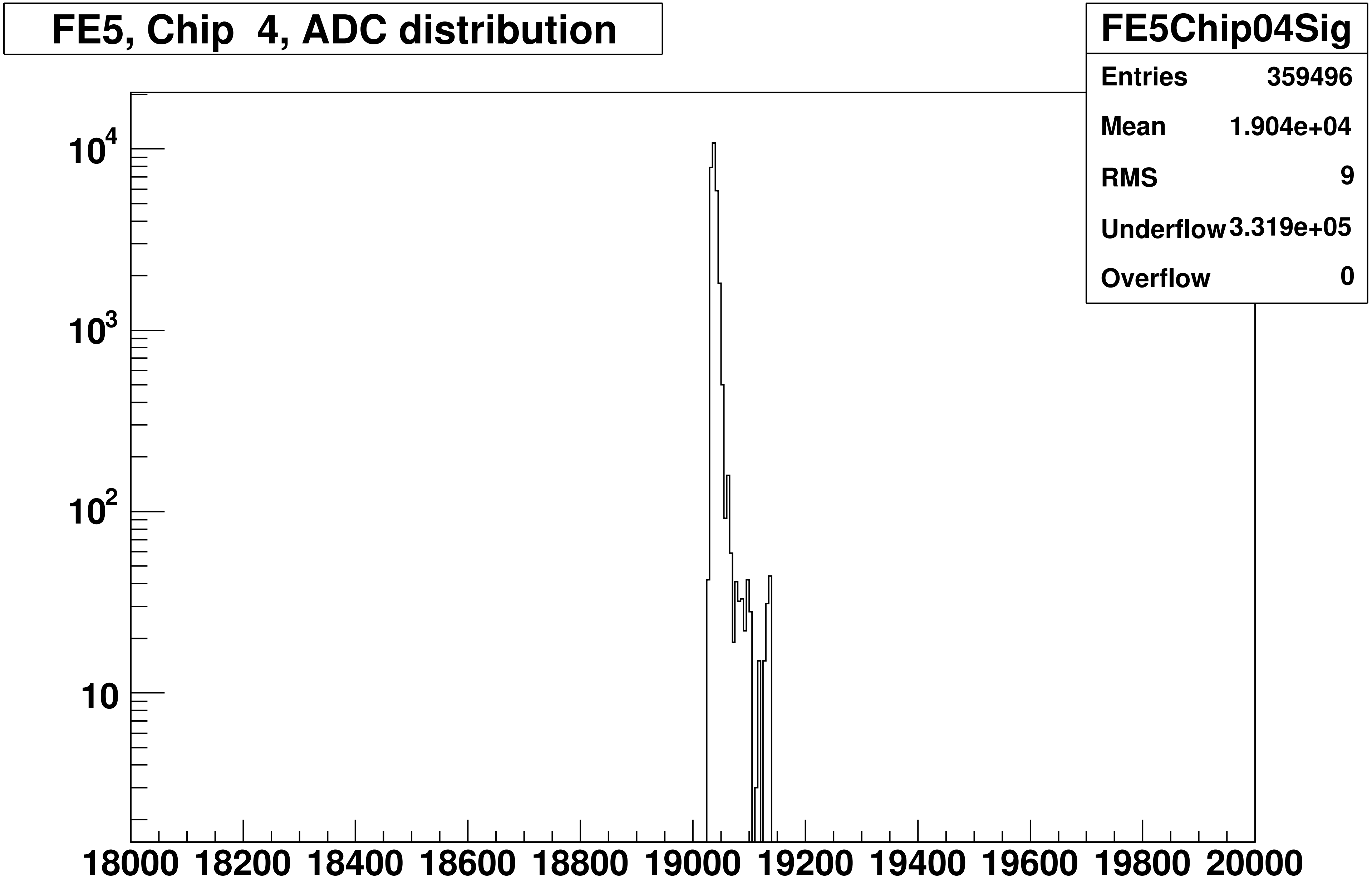
FE5, Chip 4, ADC distribution
FE5Chip04Sig
Entries 359496
Mean 1.904e+04
RMS 9
Underflow 3.319e+05
Overflow 0
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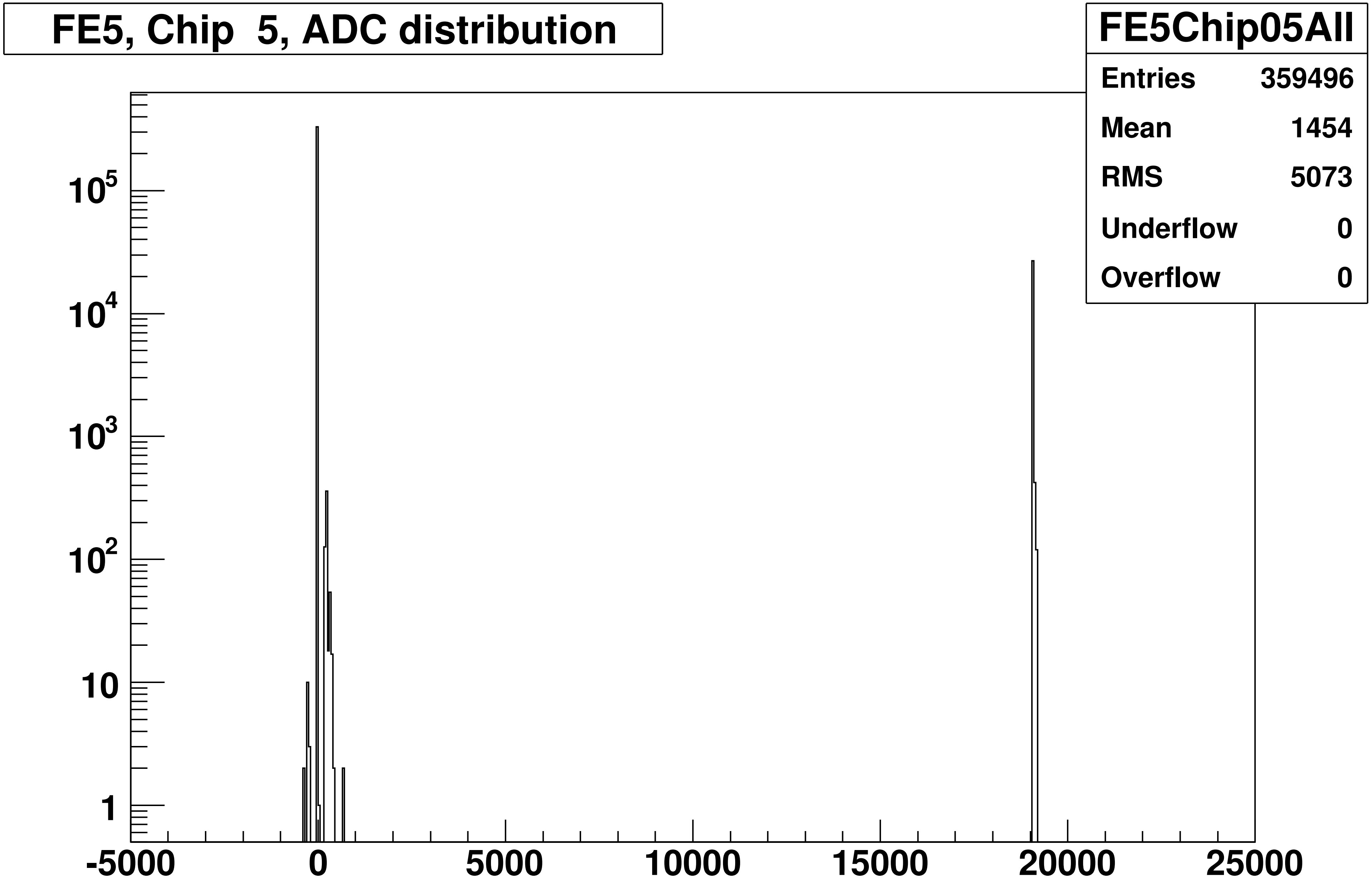
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE5, Chip 5, ADC distribution
FE5Chip05All
Entries 359496
Mean 1454
RMS 5073
Underflow 0
Overflow 0
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10^4
10^3
10^2
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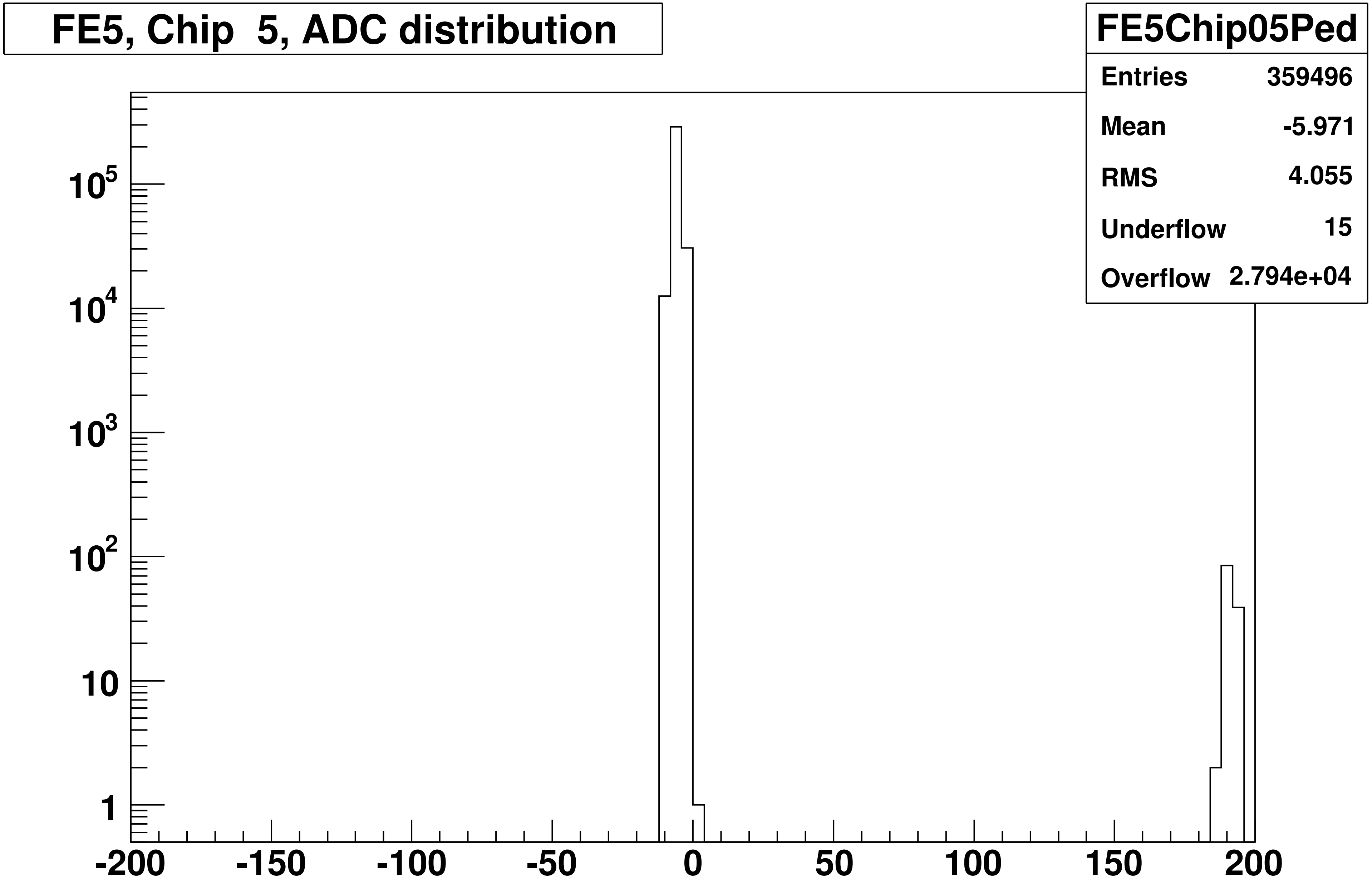
FE5, Chip 5, ADC distribution
FE5Chip05Ped
Entries 359496
Mean -5.971
RMS 4.055
Underflow 15
Overflow 2.794e+04
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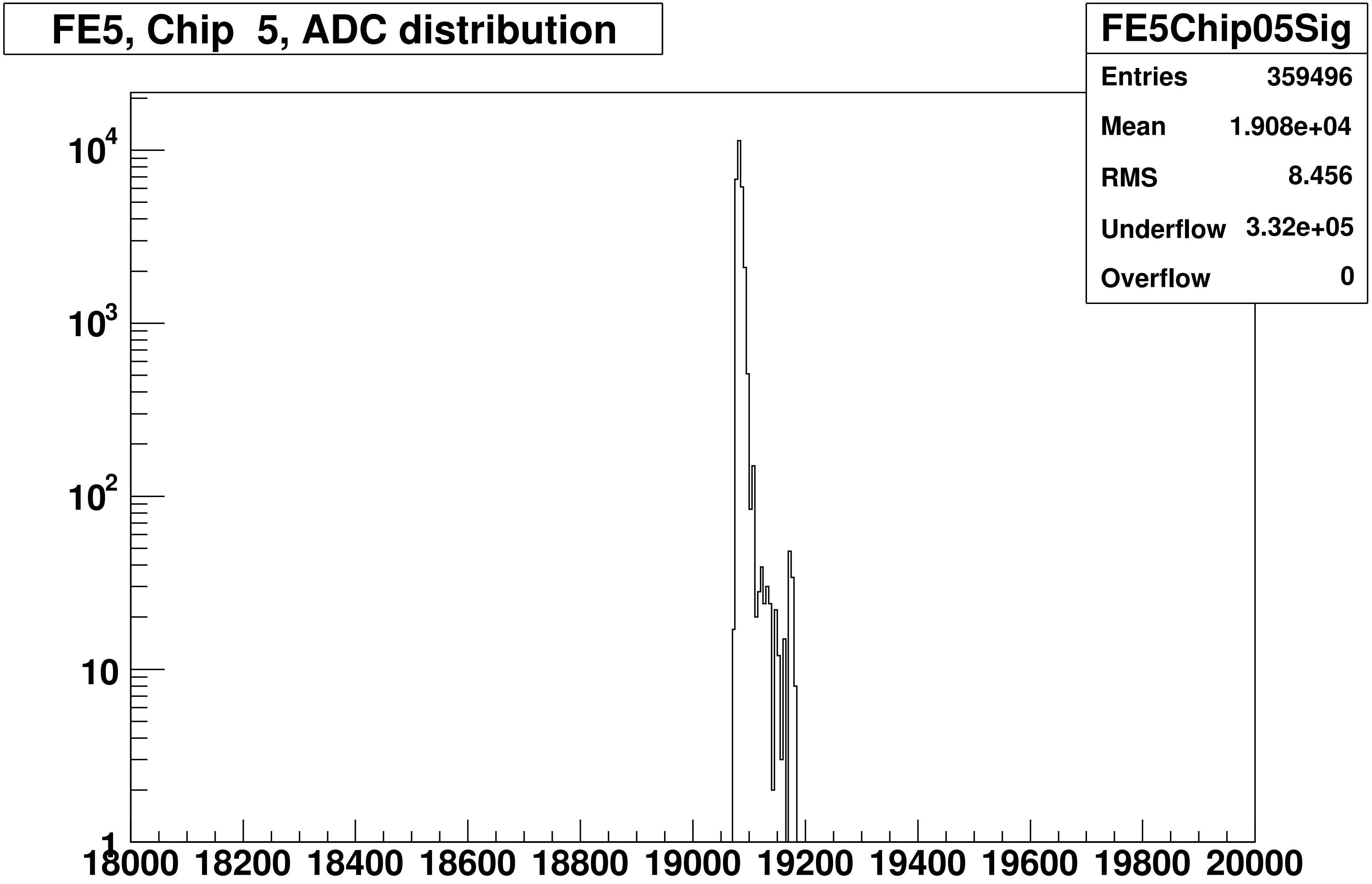
FE5, Chip 5, ADC distribution
FE5Chip05Sig
Entries 359496
Mean 1.908e+04
RMS 8.456
Underflow 3.32e+05
Overflow 0
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10^2
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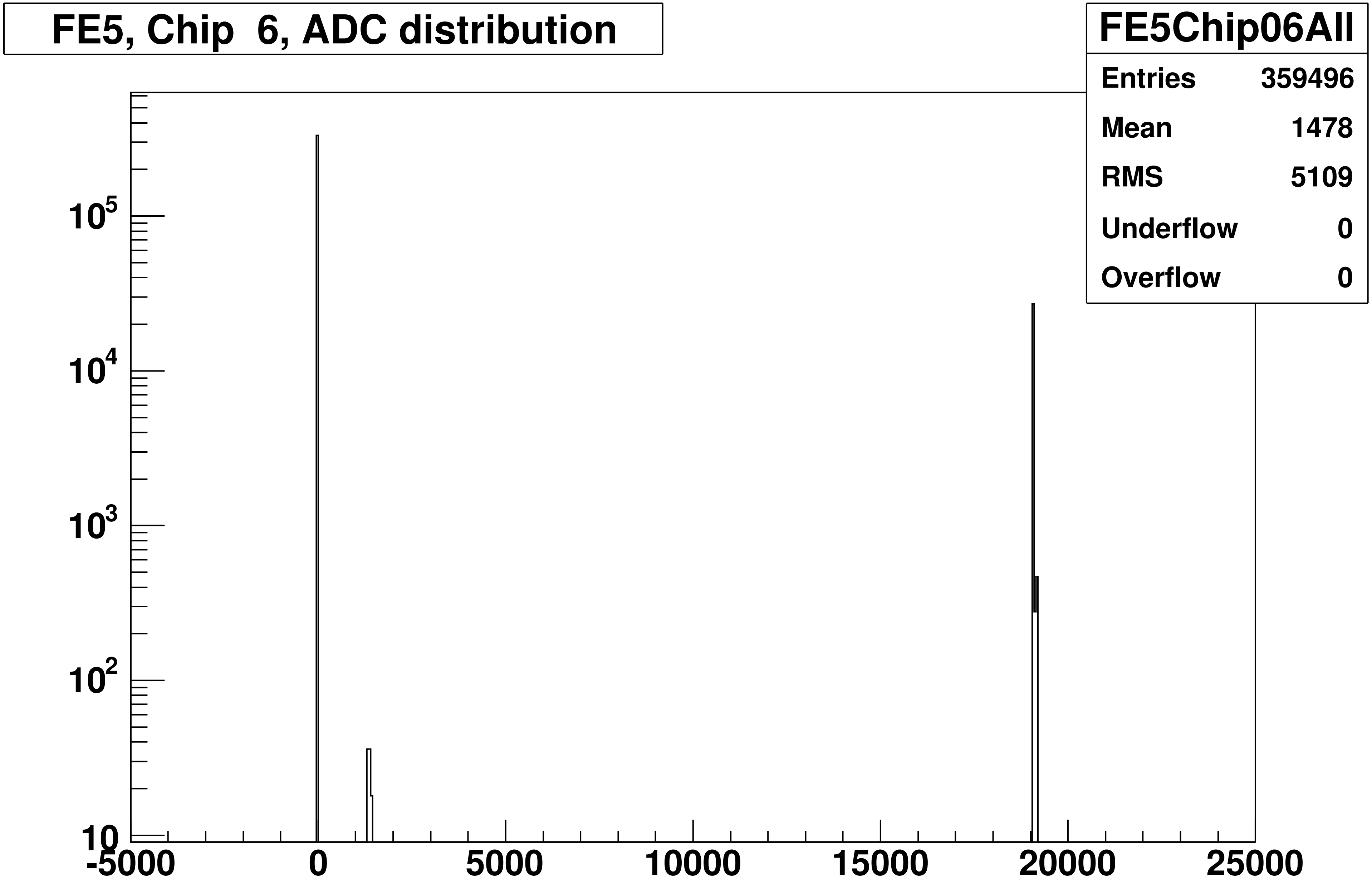
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE5, Chip 6, ADC distribution
FE5Chip06All
Entries 359496
Mean 1478
RMS 5109
Underflow 0
Overflow 0
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10^4
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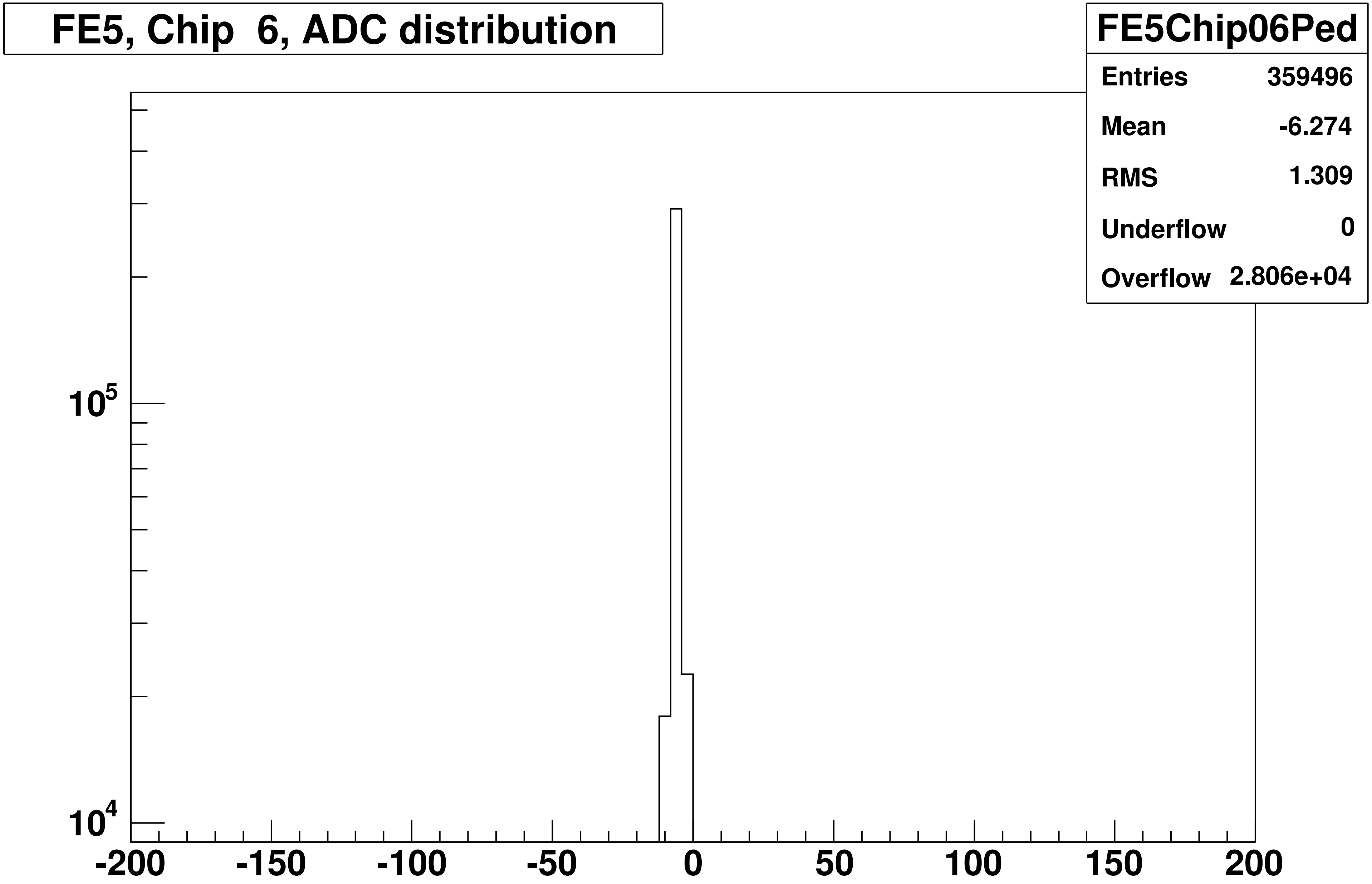
FE5, Chip 6, ADC distribution
FE5Chip06Ped
Entries 359496
Mean -6.274
RMS 1.309
Underflow 0
Overflow 2.806e+04
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150
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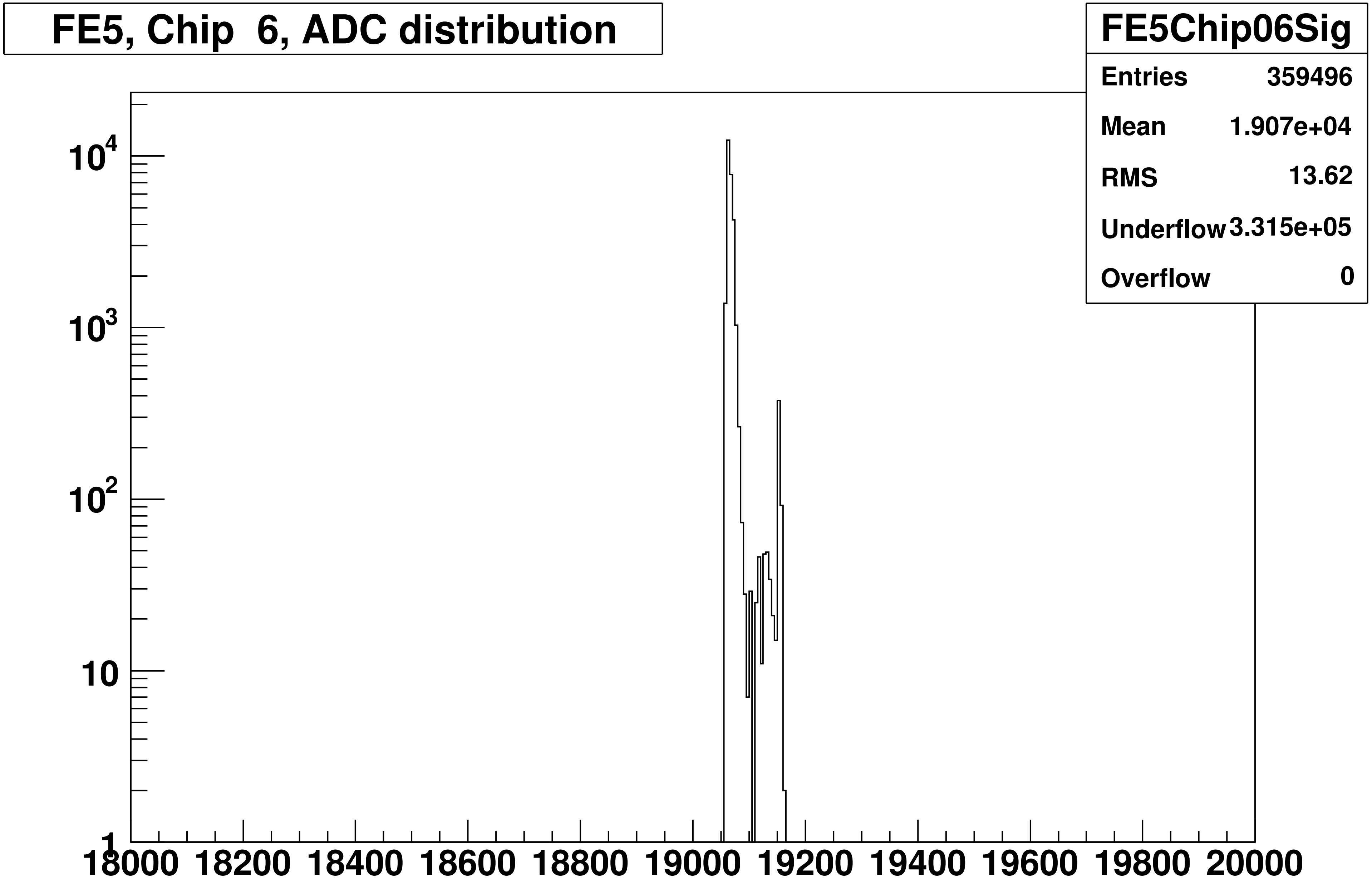

FE5, Chip 6, ADC distribution
FE5Chip06Sig
Entries 359496
Mean 1.907e+04
RMS 13.62
Underflow 3.315e+05
Overflow 0
10^4
10^3
10^2
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1
18000
18200
18400
18600
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19000
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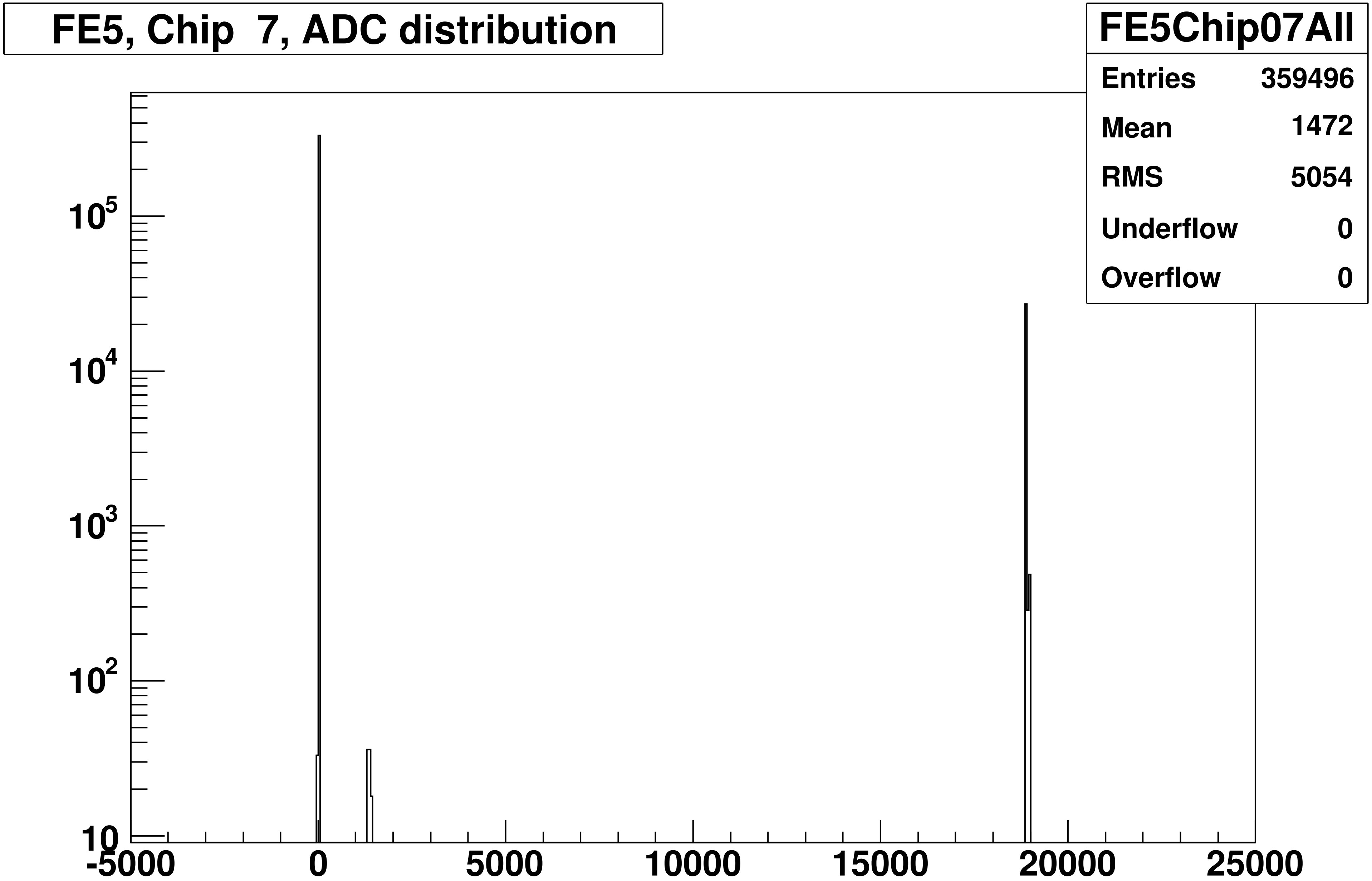
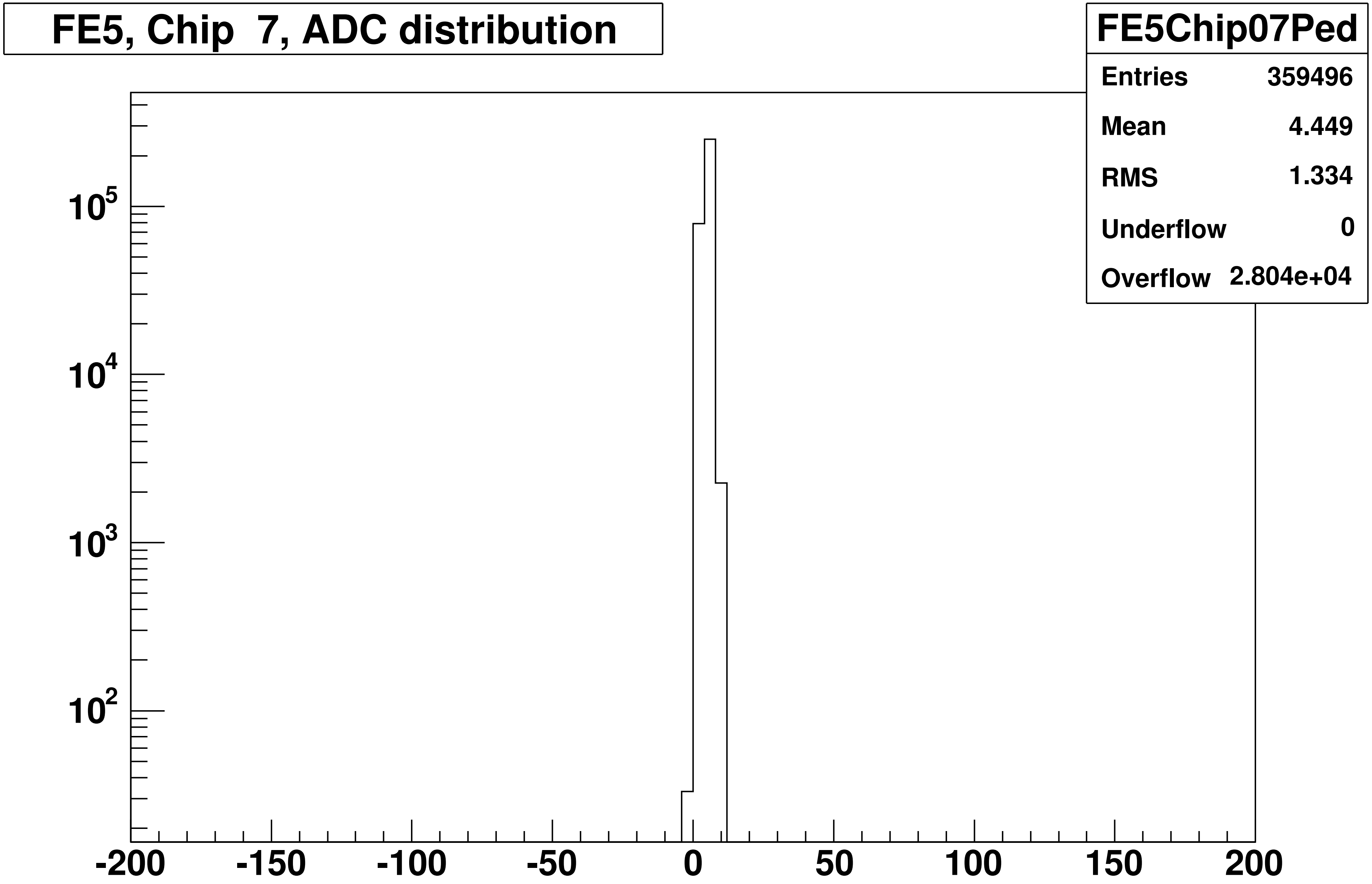
19800
20000


FE5, Chip 7, ADC distribution
FE5Chip07All
Entries 359496
Mean 1472
RMS 5054
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE5, Chip 7, ADC distribution
FE5Chip07Ped
Entries 359496
Mean 4.449
RMS 1.334
Underflow 0
Overflow 2.804e+04
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10^4
10^3
10^2
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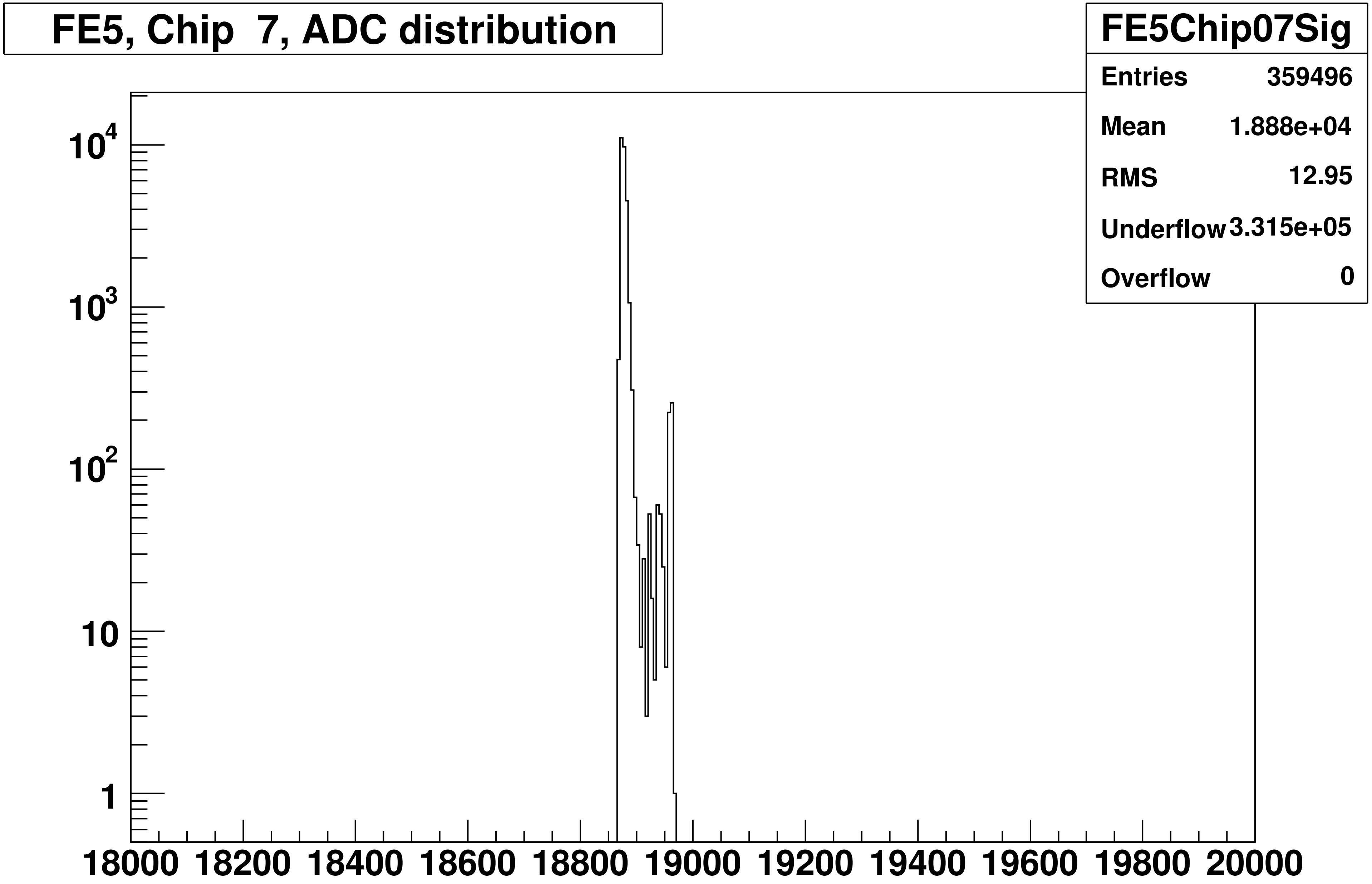
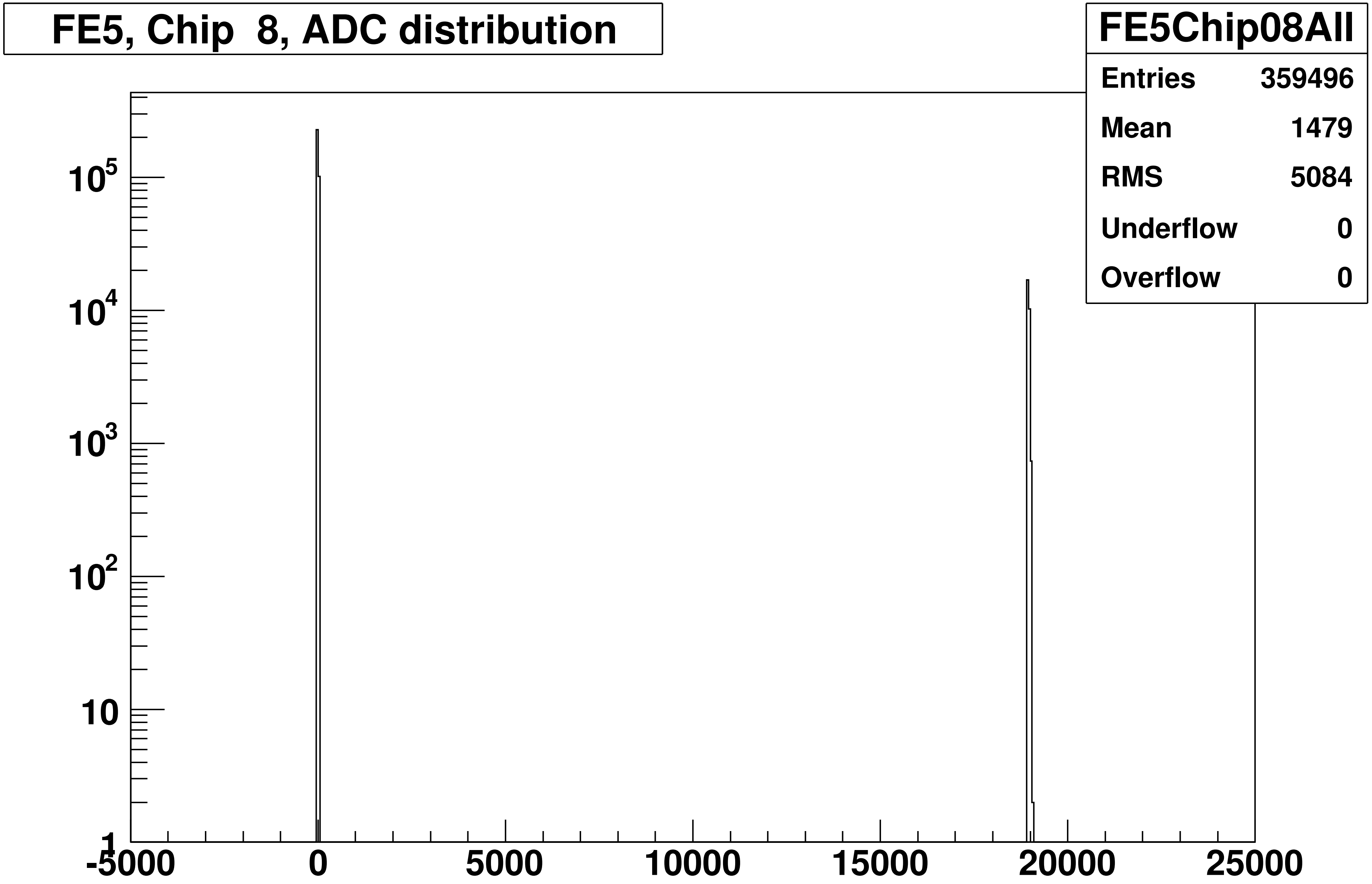
150
200


FE5, Chip 7, ADC distribution
FE5Chip07Sig
Entries 359496
Mean 1.888e+04
RMS 12.95
Underflow 3.315e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE5, Chip 8, ADC distribution
FE5Chip08All
Entries 359496
Mean 1479
RMS 5084
Underflow 0
Overflow 0
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10^4
10^3
10^2
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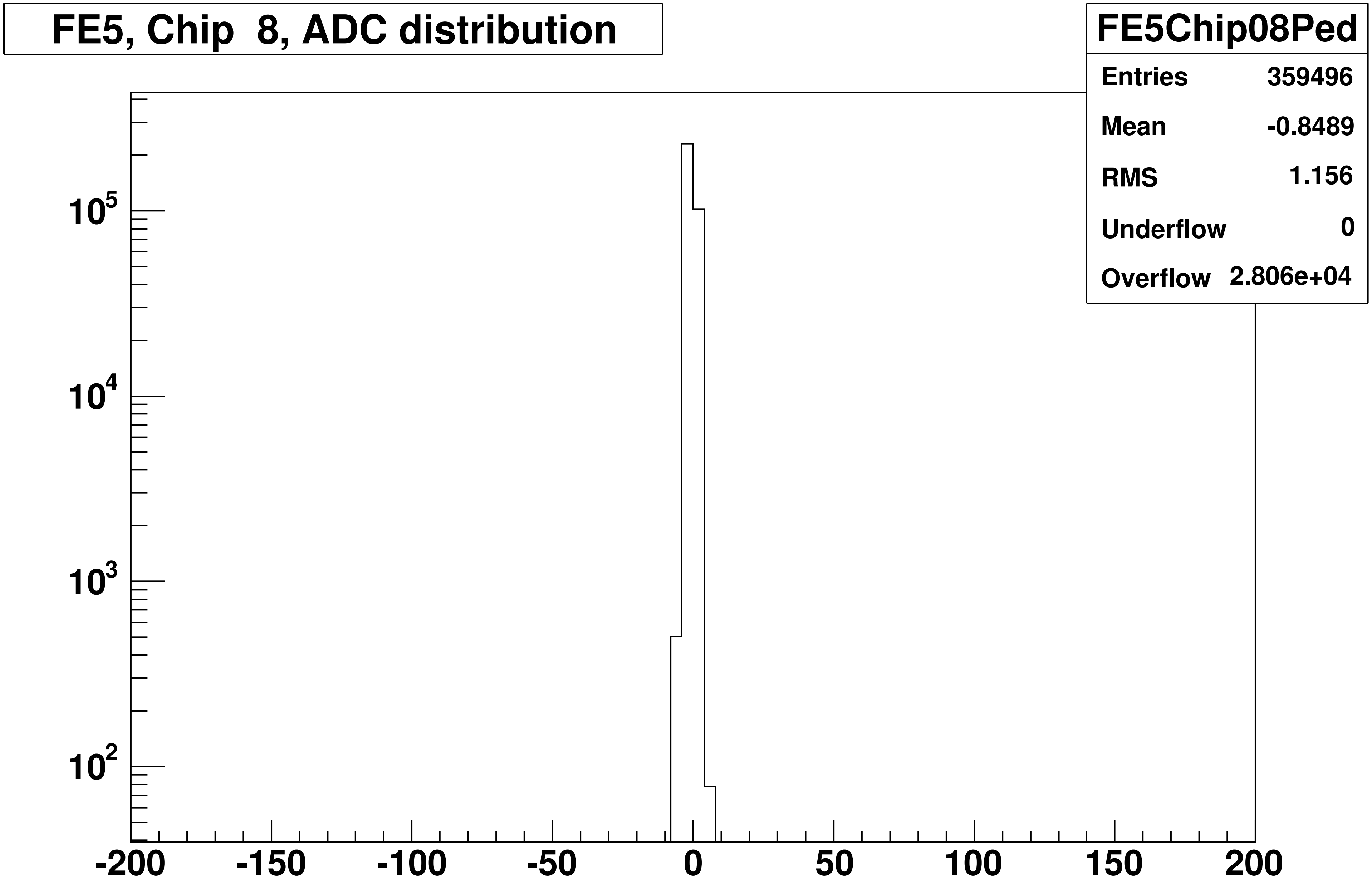
1
-5000
0
5000
10000
15000
20000
25000


FE5, Chip 8, ADC distribution
FE5Chip08Ped
Entries 359496
Mean -0.8489
RMS 1.156
Underflow 0
Overflow 2.806e+04
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10^4
10^3
10^2
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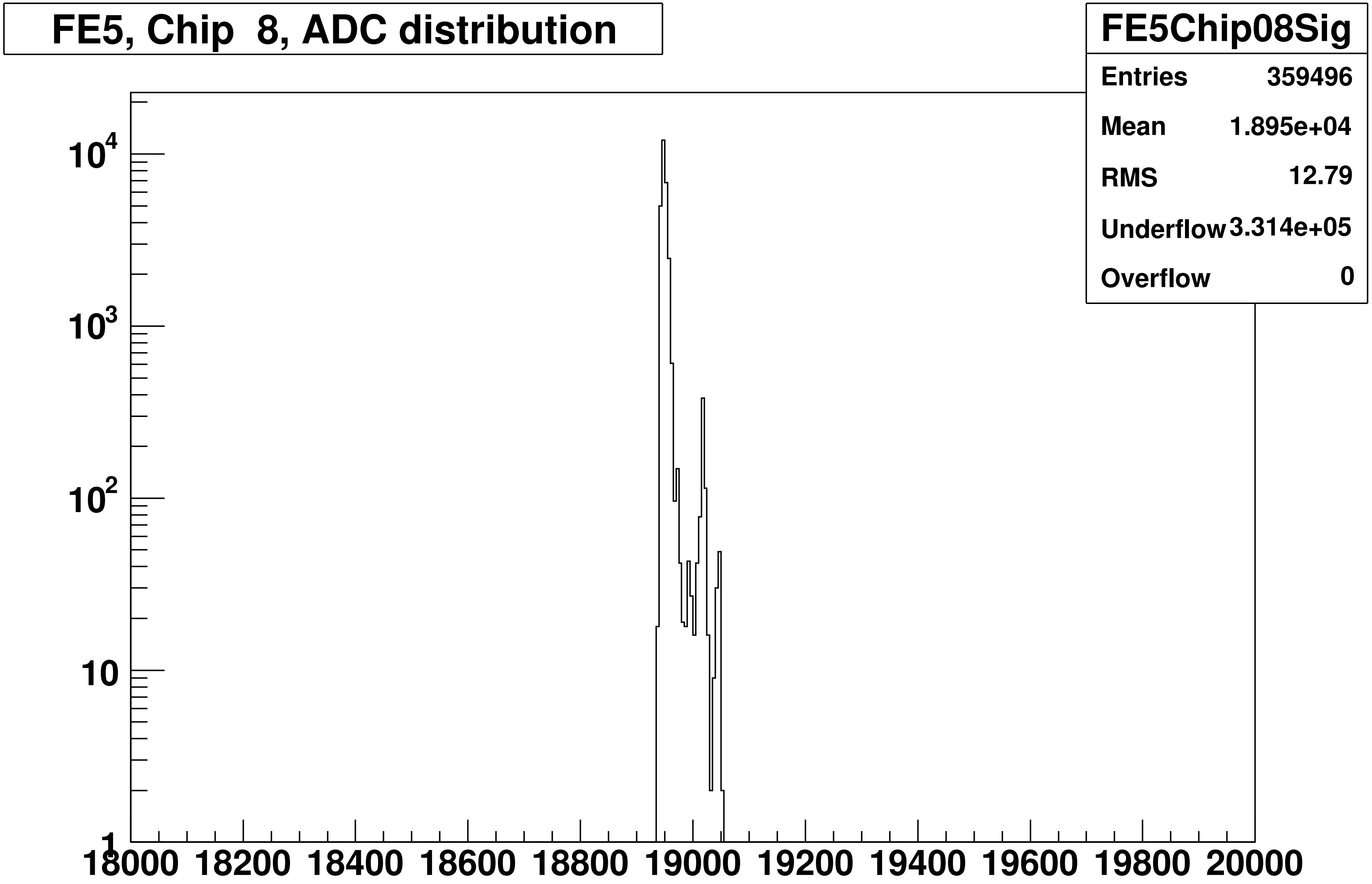
50
100
150
200


FE5, Chip 8, ADC distribution
FE5Chip08Sig
Entries 359496
Mean 1.895e+04
RMS 12.79
Underflow 3.314e+05
Overflow 0
10^4
10^3
10^2
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1
18000
18200
18400
18600
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19000
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19800
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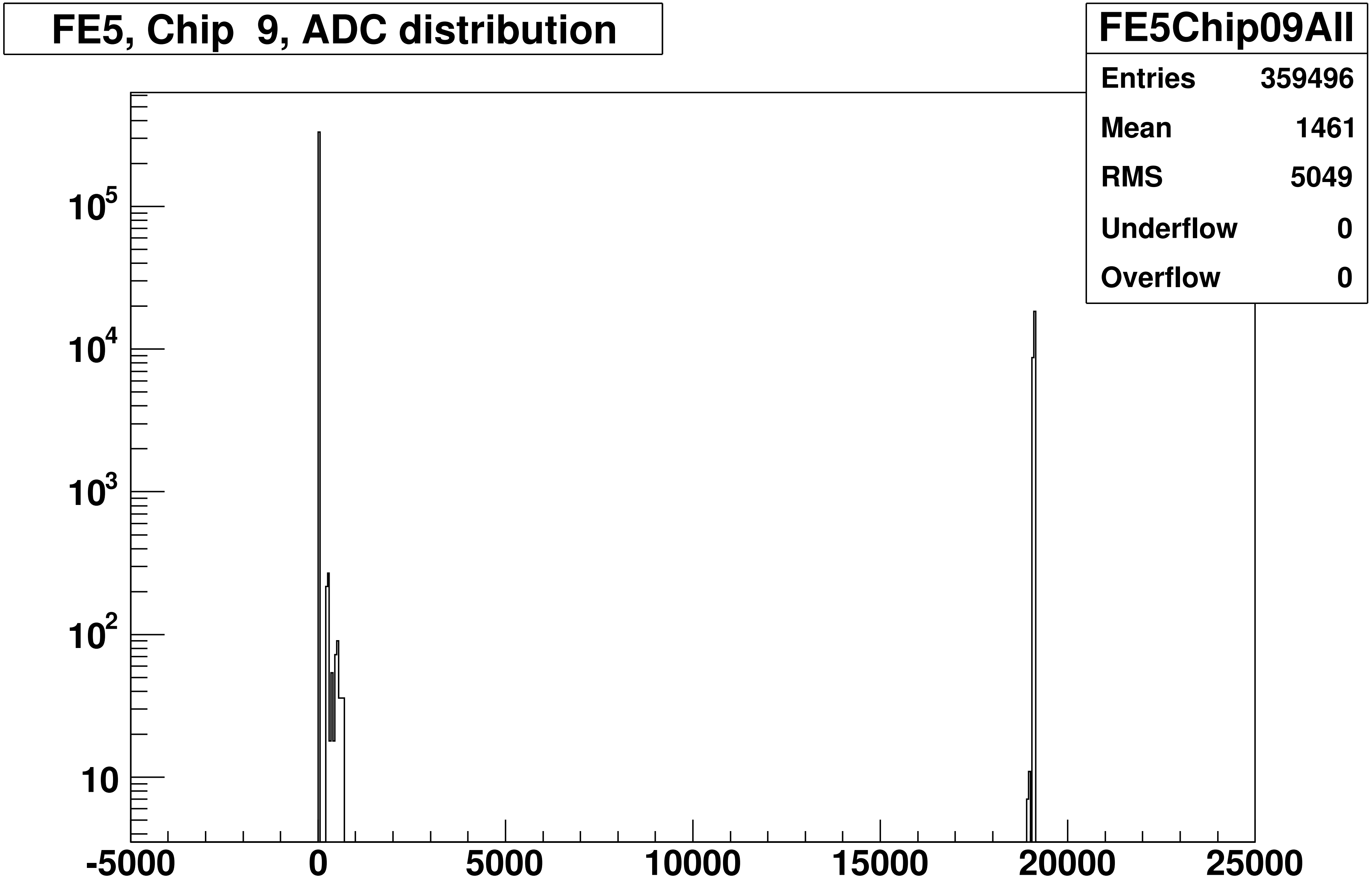
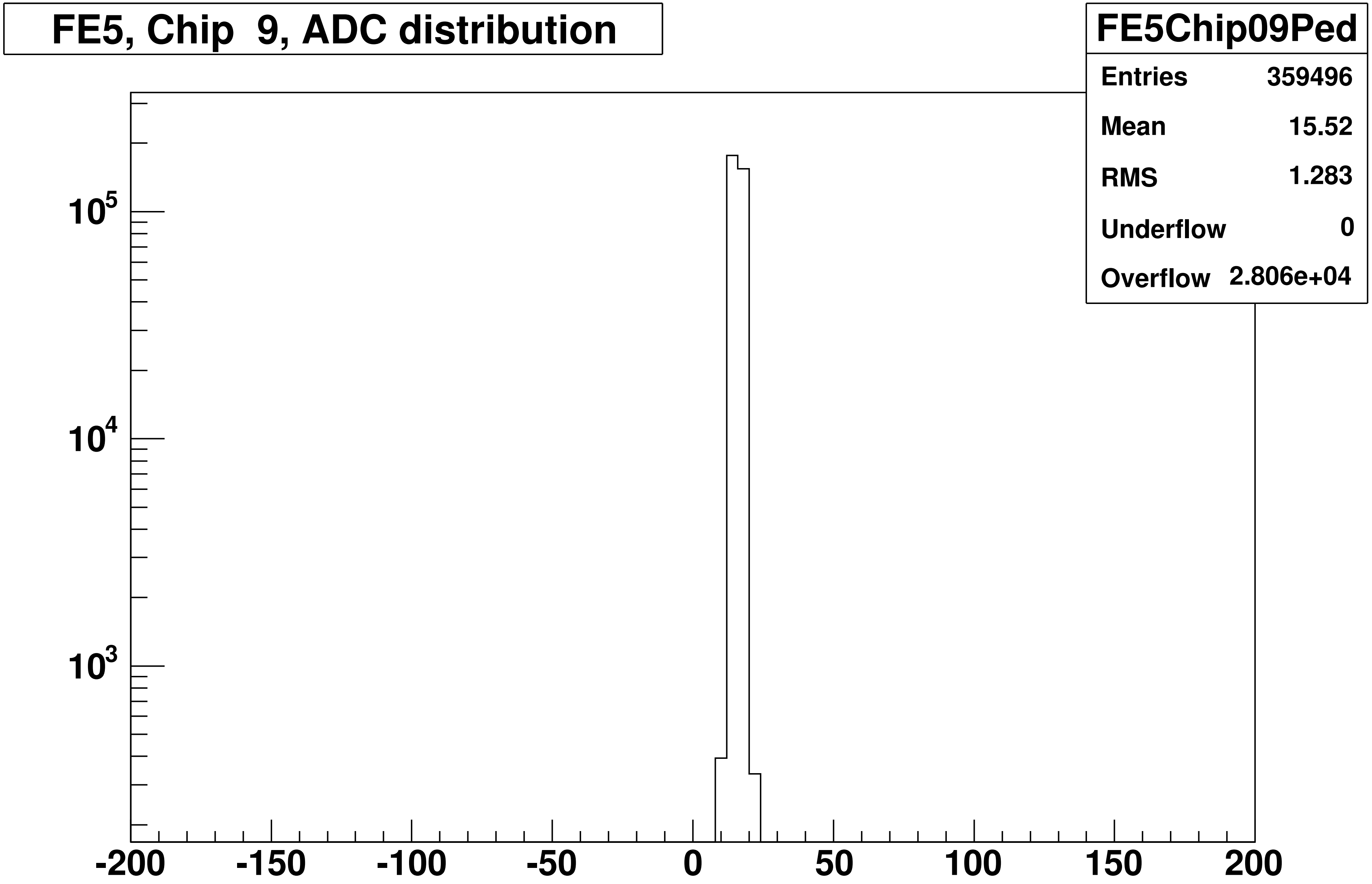


FE5, Chip 9, ADC distribution
FE5Chip09All
Entries 359496
Mean 1461
RMS 5049
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE5, Chip 9, ADC distribution
FE5Chip09Ped
Entries 359496
Mean 15.52
RMS 1.283
Underflow 0
Overflow 2.806e+04
10^5
10^4
10^3
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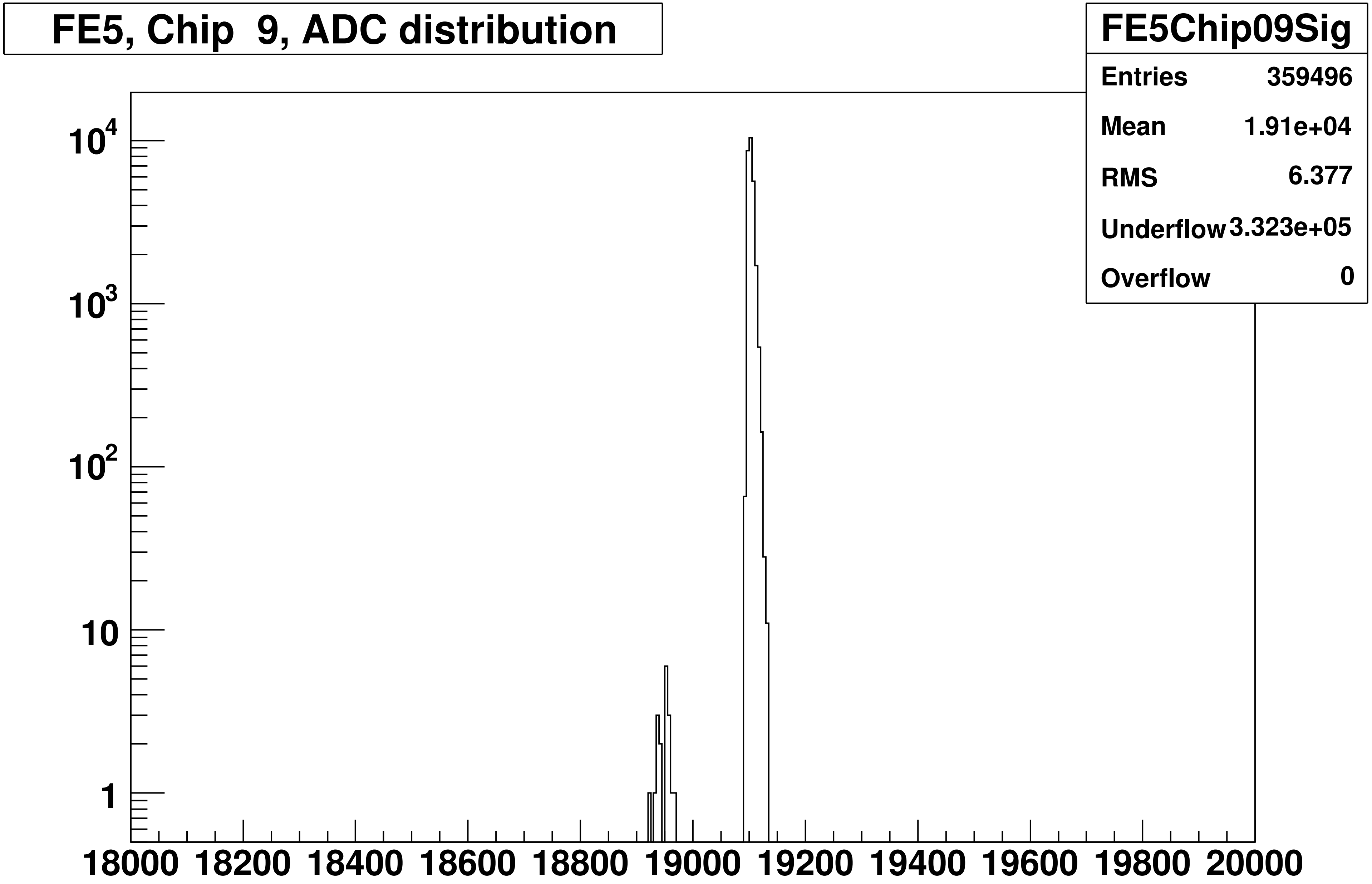
-150
-100
-50
0
50
100
150
200



FE5, Chip 9, ADC distribution
FE5Chip09Sig
Entries 359496
Mean 1.91e+04
RMS 6.377
Underflow 3.323e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
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19000
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19400
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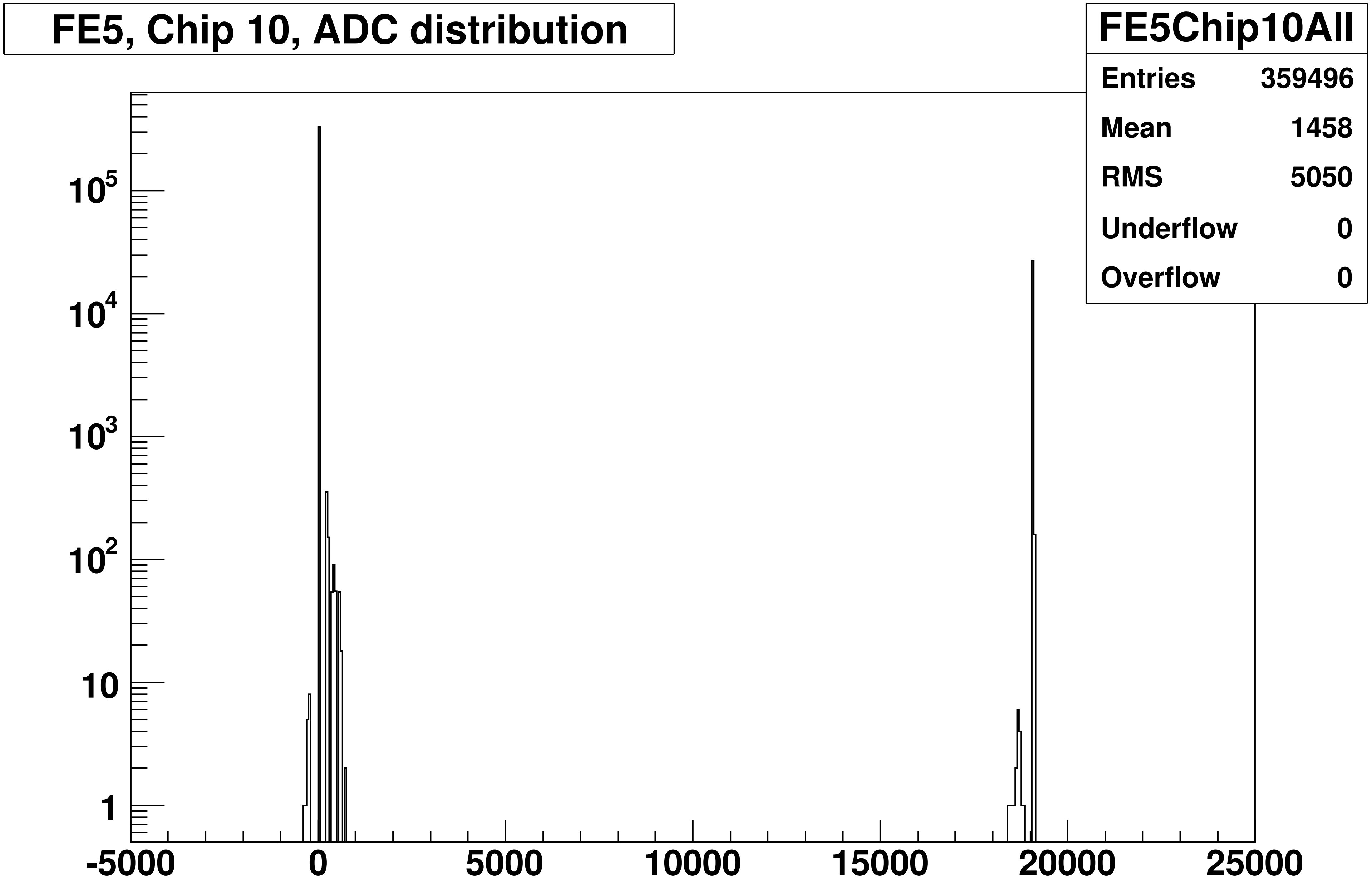
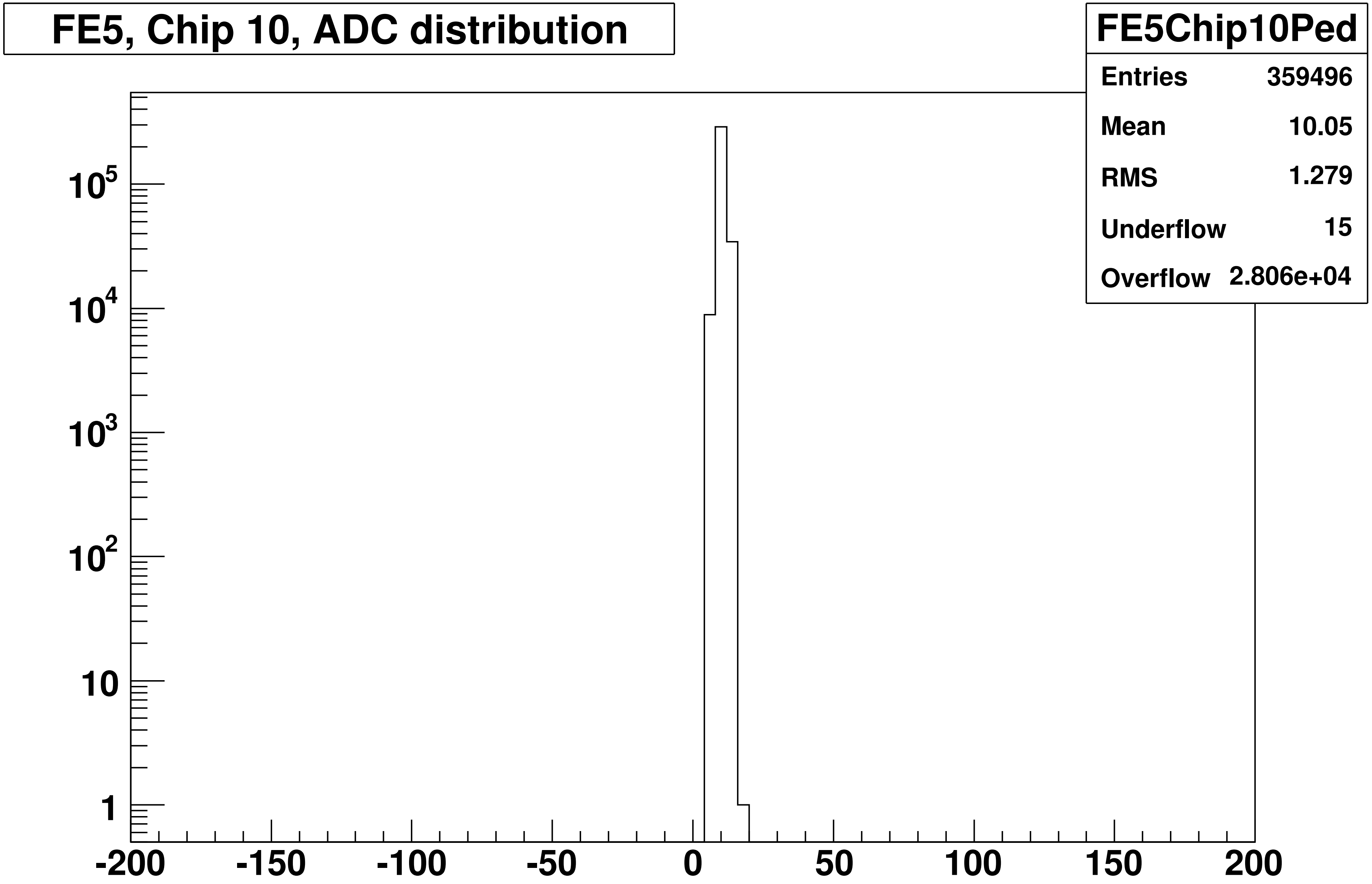

FE5, Chip 10, ADC distribution
FE5Chip10All
Entries 359496
Mean 1458
RMS 5050
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE5, Chip 10, ADC distribution
FE5Chip10Ped
Entries 359496
Mean 10.05
RMS 1.279
Underflow 15
Overflow 2.806e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
-50
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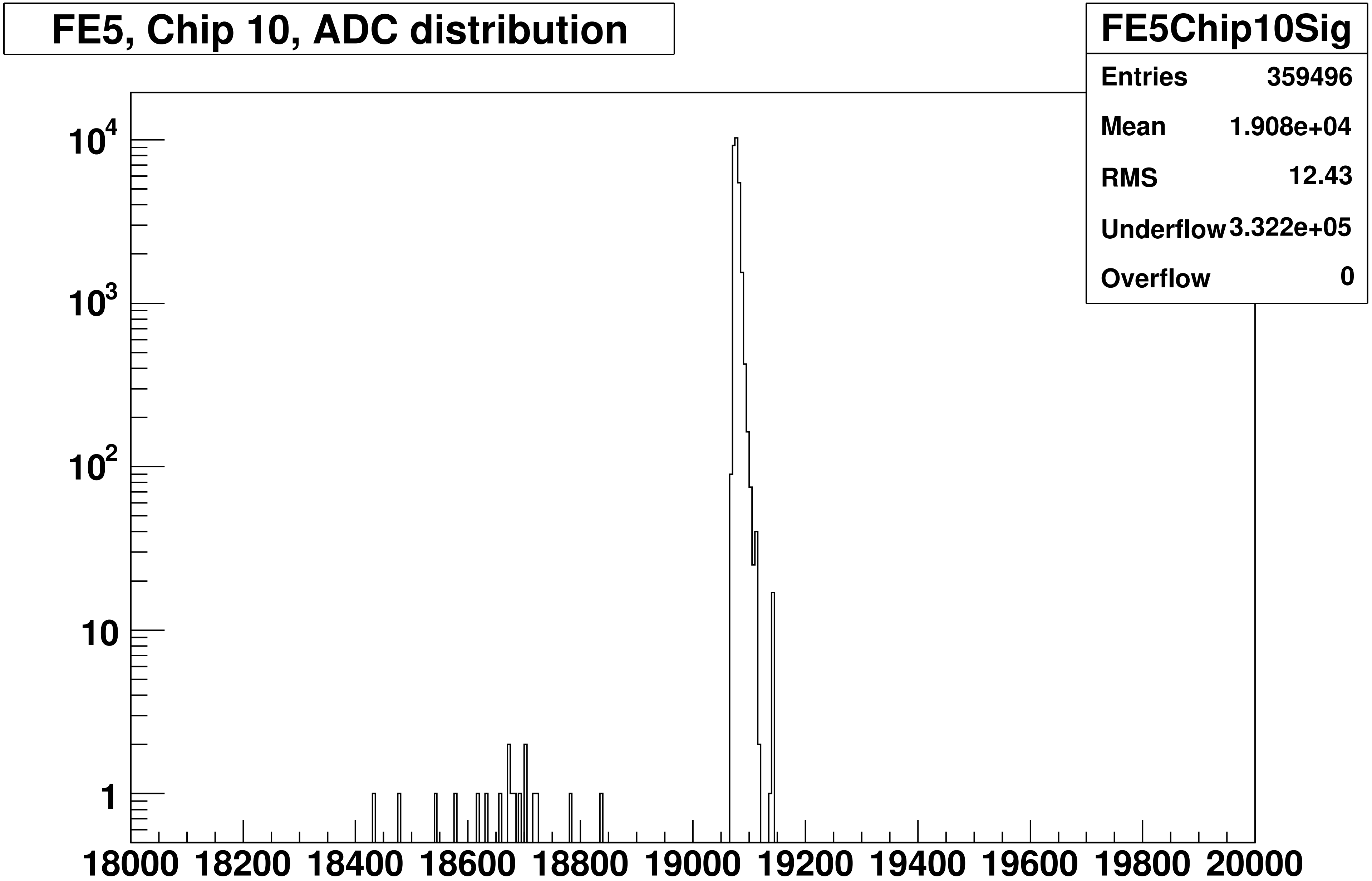
100
150
200


FE5, Chip 10, ADC distribution
FE5Chip10Sig
Entries 359496
Mean 1.908e+04
RMS 12.43
Underflow 3.322e+05
Overflow 0
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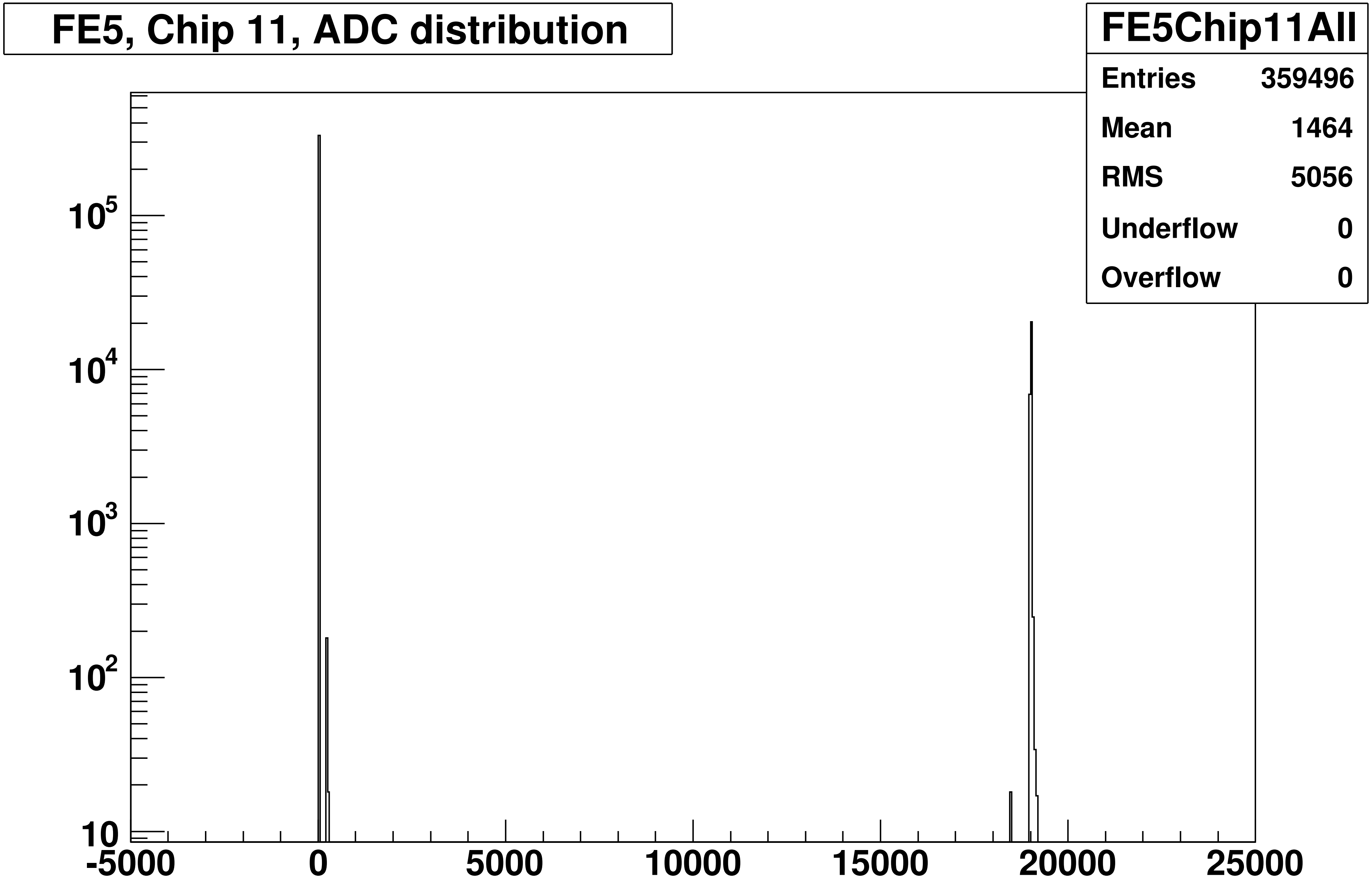
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE5, Chip 11, ADC distribution
FE5Chip11All
Entries 359496
Mean 1464
RMS 5056
Underflow 0
Overflow 0
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10^4
10^3
10^2
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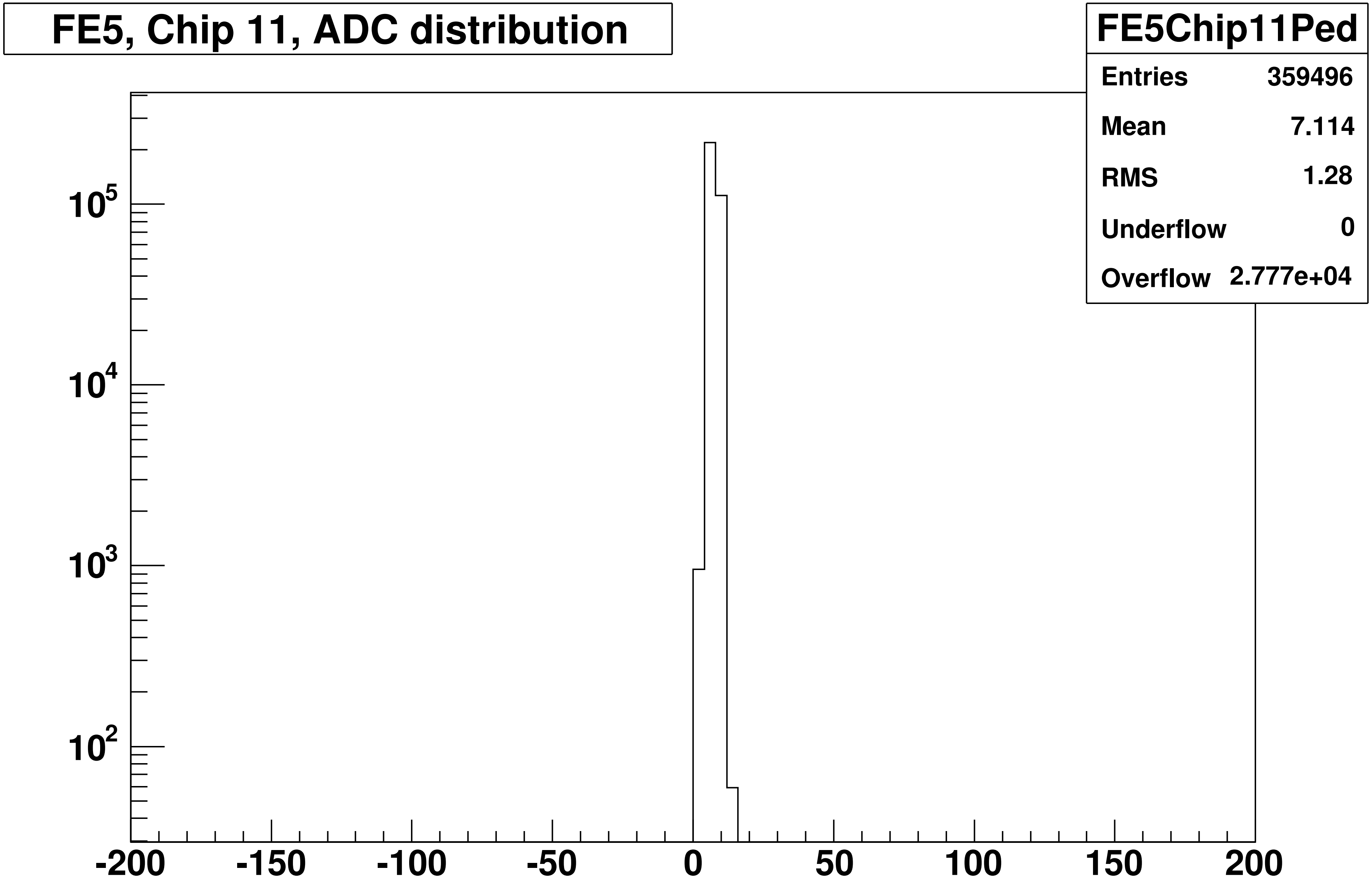
-5000
0
5000
10000
15000
20000
25000



FE5, Chip 11, ADC distribution
FE5Chip11Ped
Entries 359496
Mean 7.114
RMS 1.28
Underflow 0
Overflow 2.777e+04
10^5
10^4
10^3
10^2
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-100
-50
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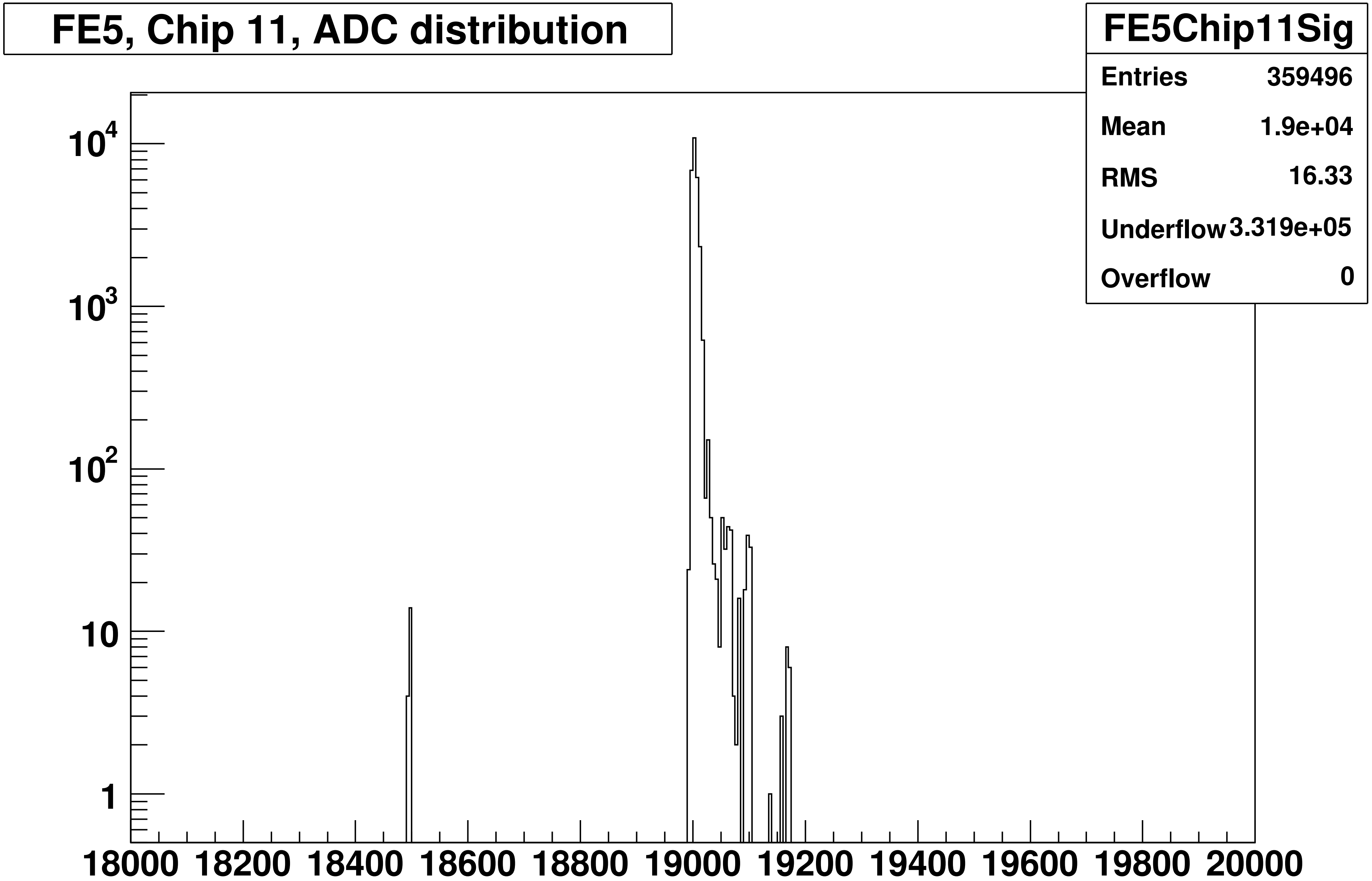
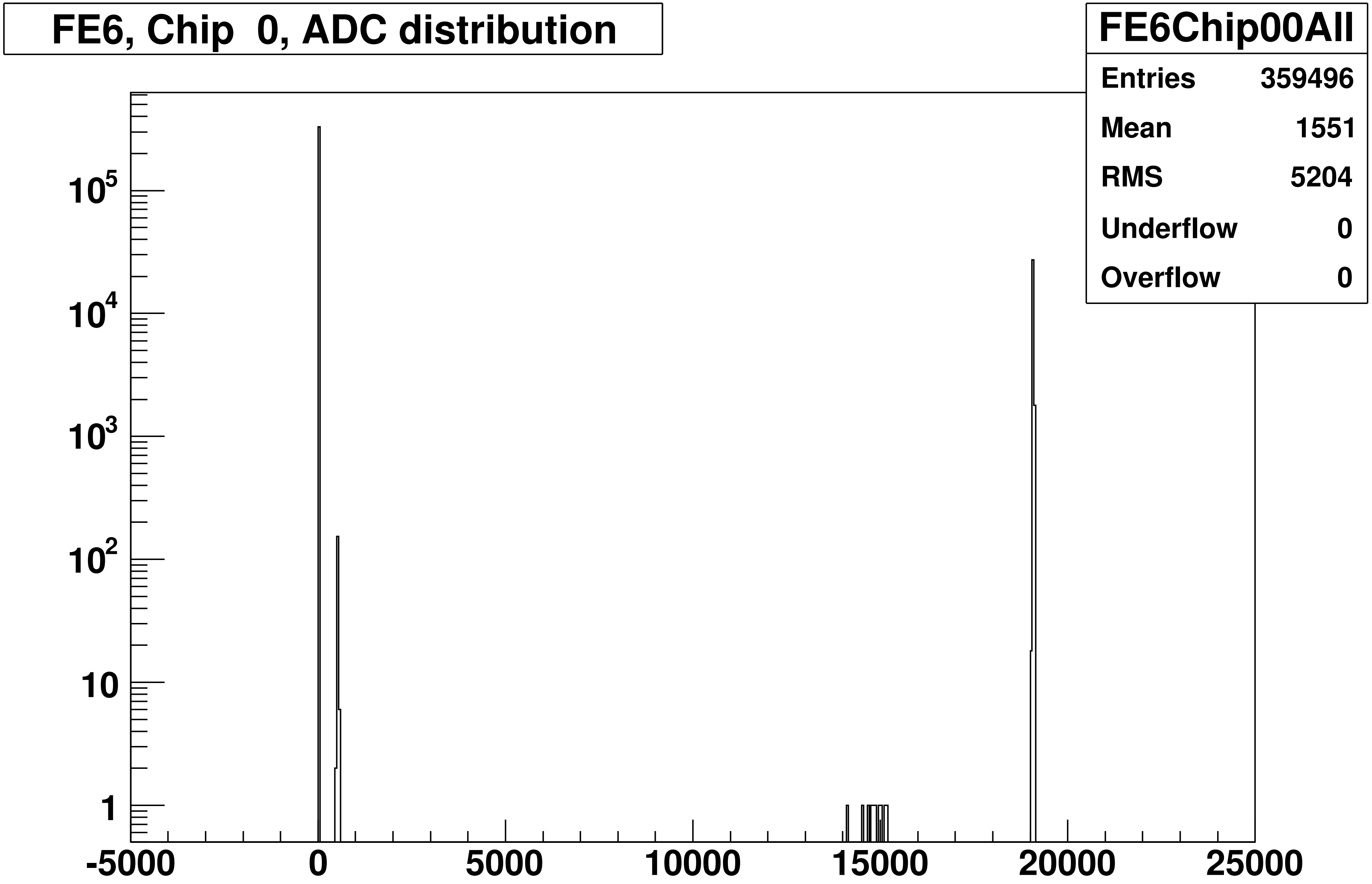
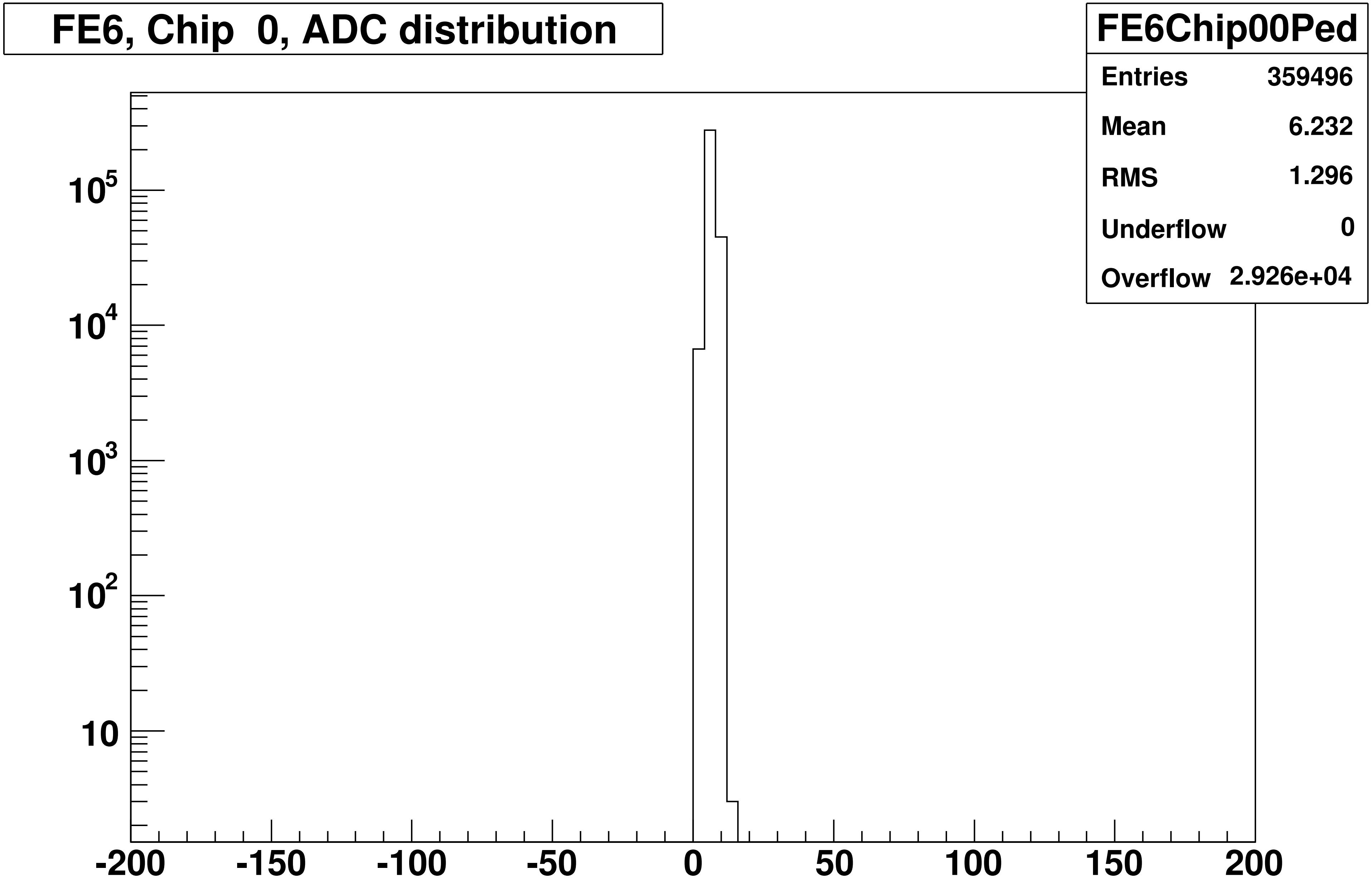
50
100
150
200

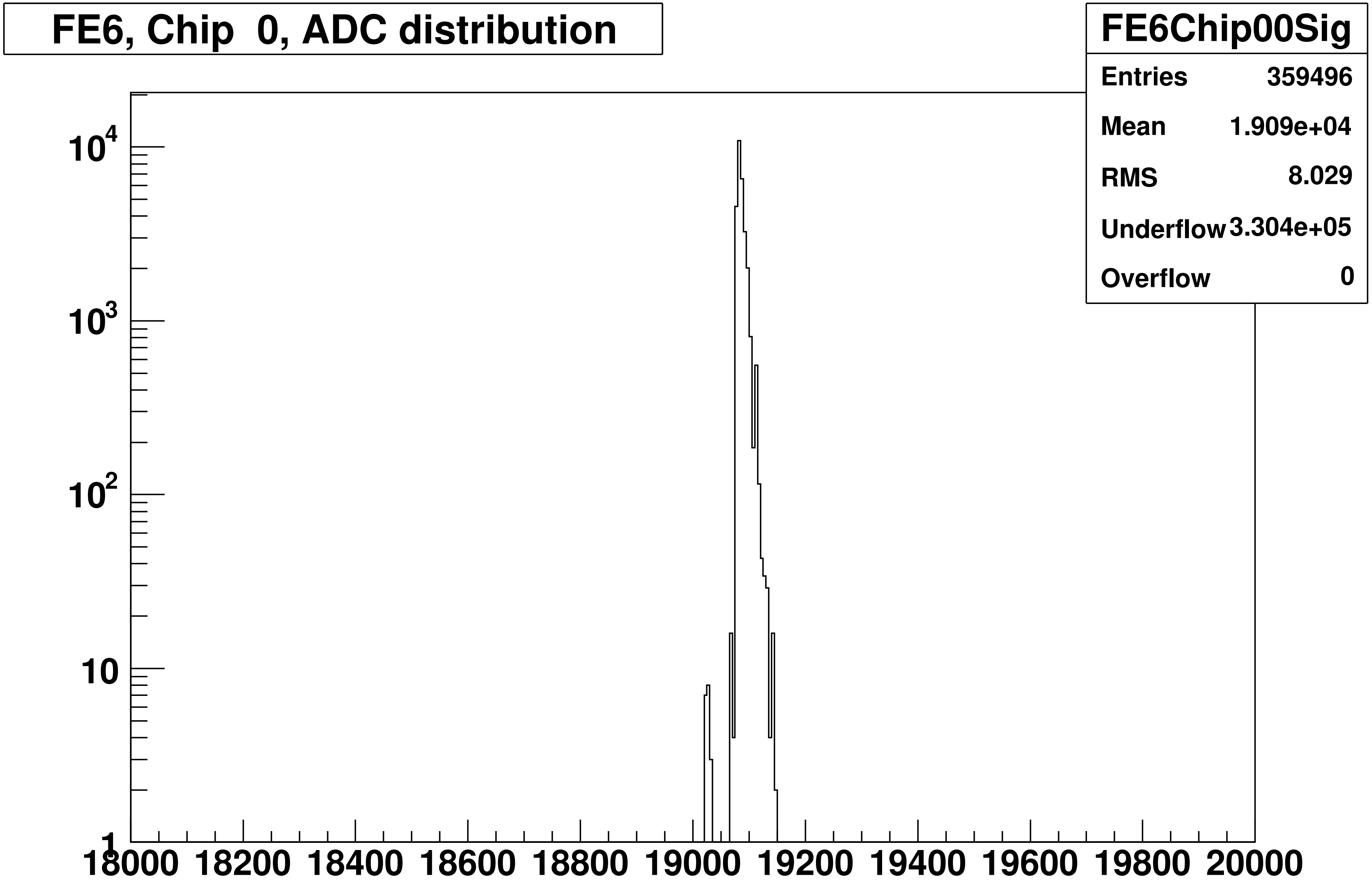

FE5, Chip 11, ADC distribution
FE5Chip11Sig
Entries 359496
Mean 1.9e+04
RMS 16.33
Underflow 3.319e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000



FE6, Chip 0, ADC distribution
FE6Chip00All
Entries 359496
Mean 1551
RMS 5204
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE6, Chip 0, ADC distribution
FE6Chip00Ped
Entries 359496
Mean 6.232
RMS 1.296
Underflow 0
Overflow 2.926e+04
10^5
10^4
10^3
10^2
10
-200
-150
-100
-50
0
50
100
150
200


FE6, Chip 0, ADC distribution
FE6Chip00Sig
Entries 359496
Mean 1.909e+04
RMS 8.029
Underflow 3.304e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
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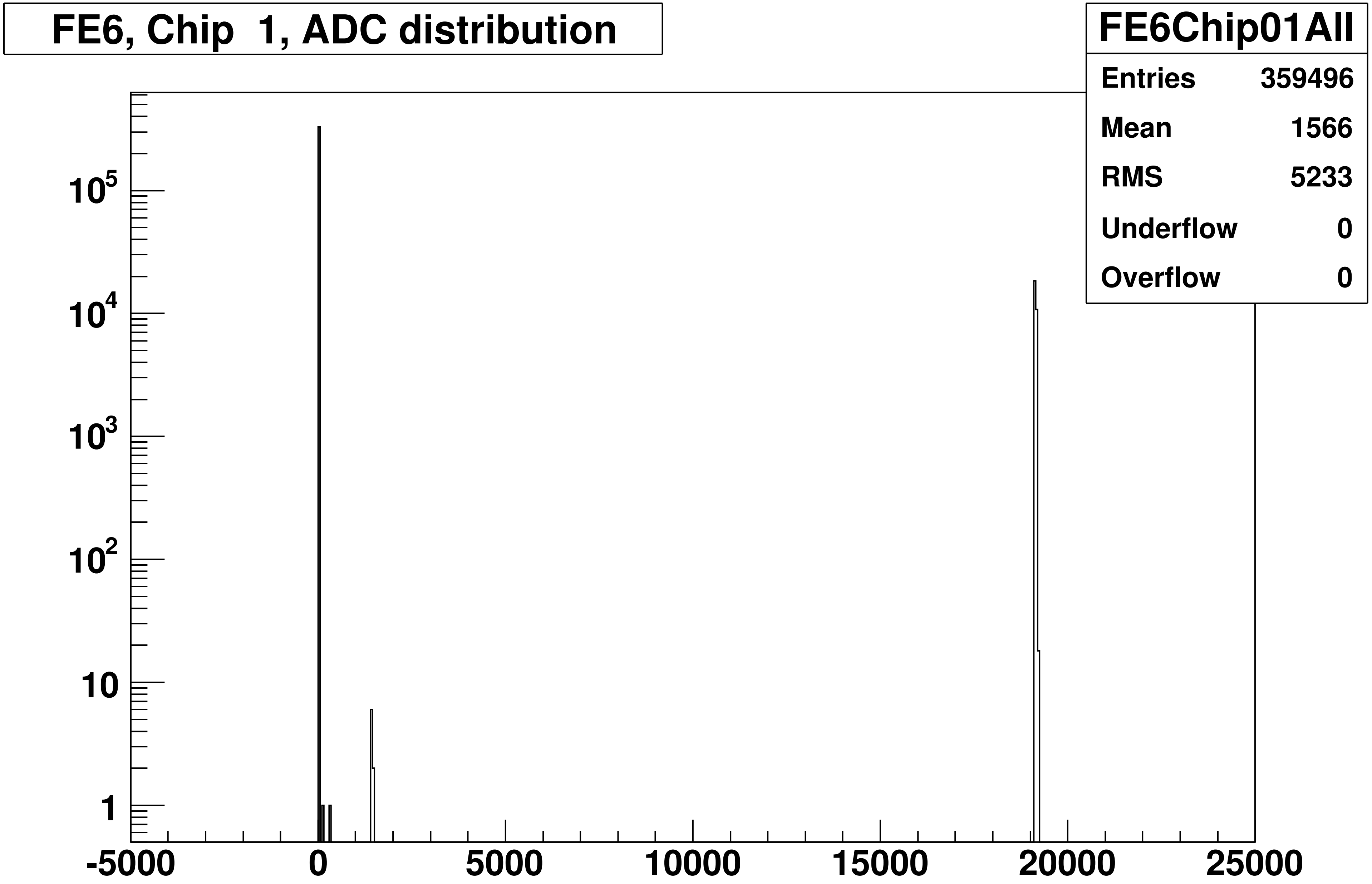
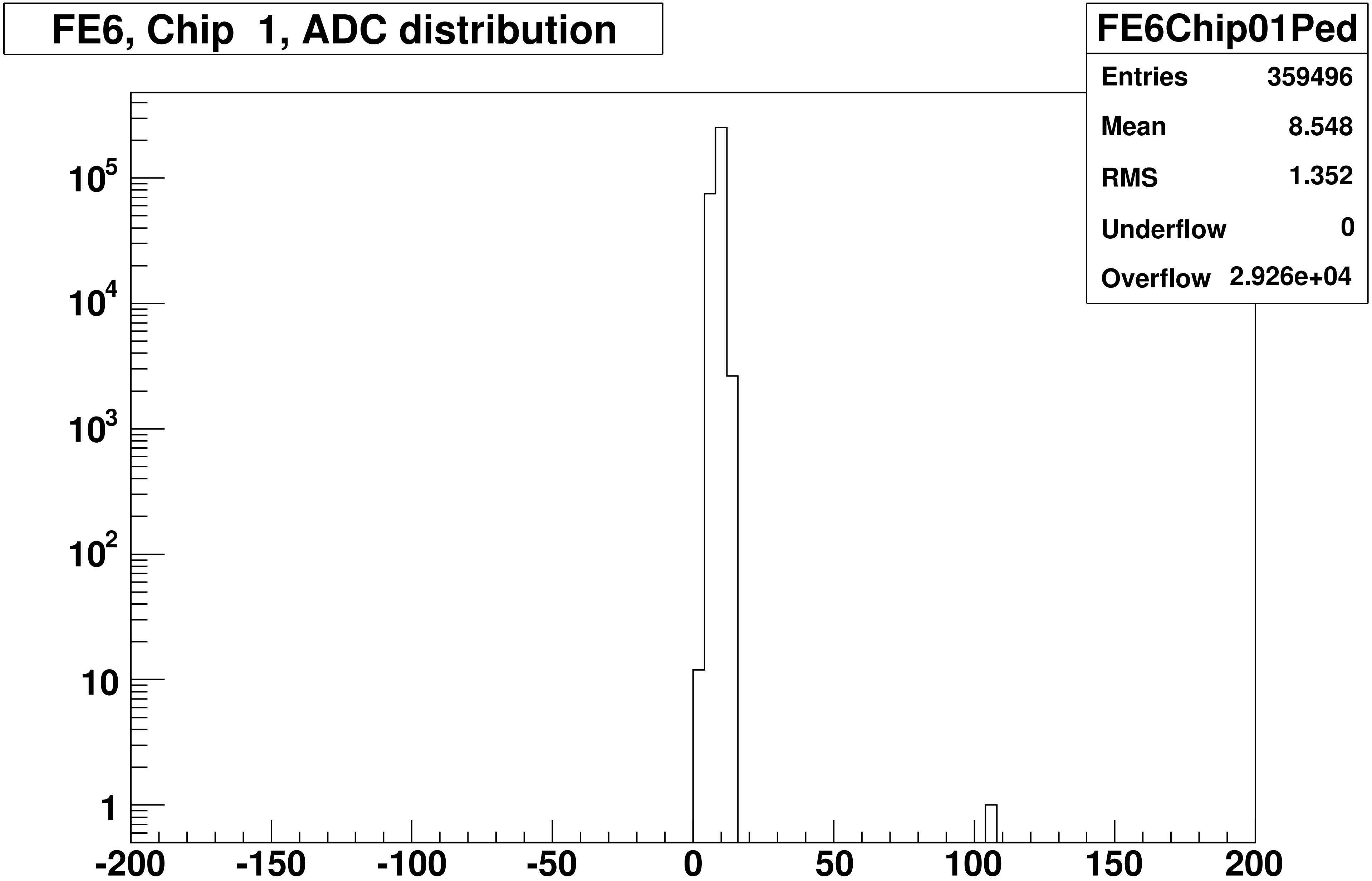
19400
19600
19800
20000


FE6, Chip 1, ADC distribution
FE6Chip01All
Entries 359496
Mean 1566
RMS 5233
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE6, Chip 1, ADC distribution
FE6Chip01Ped
Entries 359496
Mean 8.548
RMS 1.352
Underflow 0
Overflow 2.926e+04
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10^3
10^2
10
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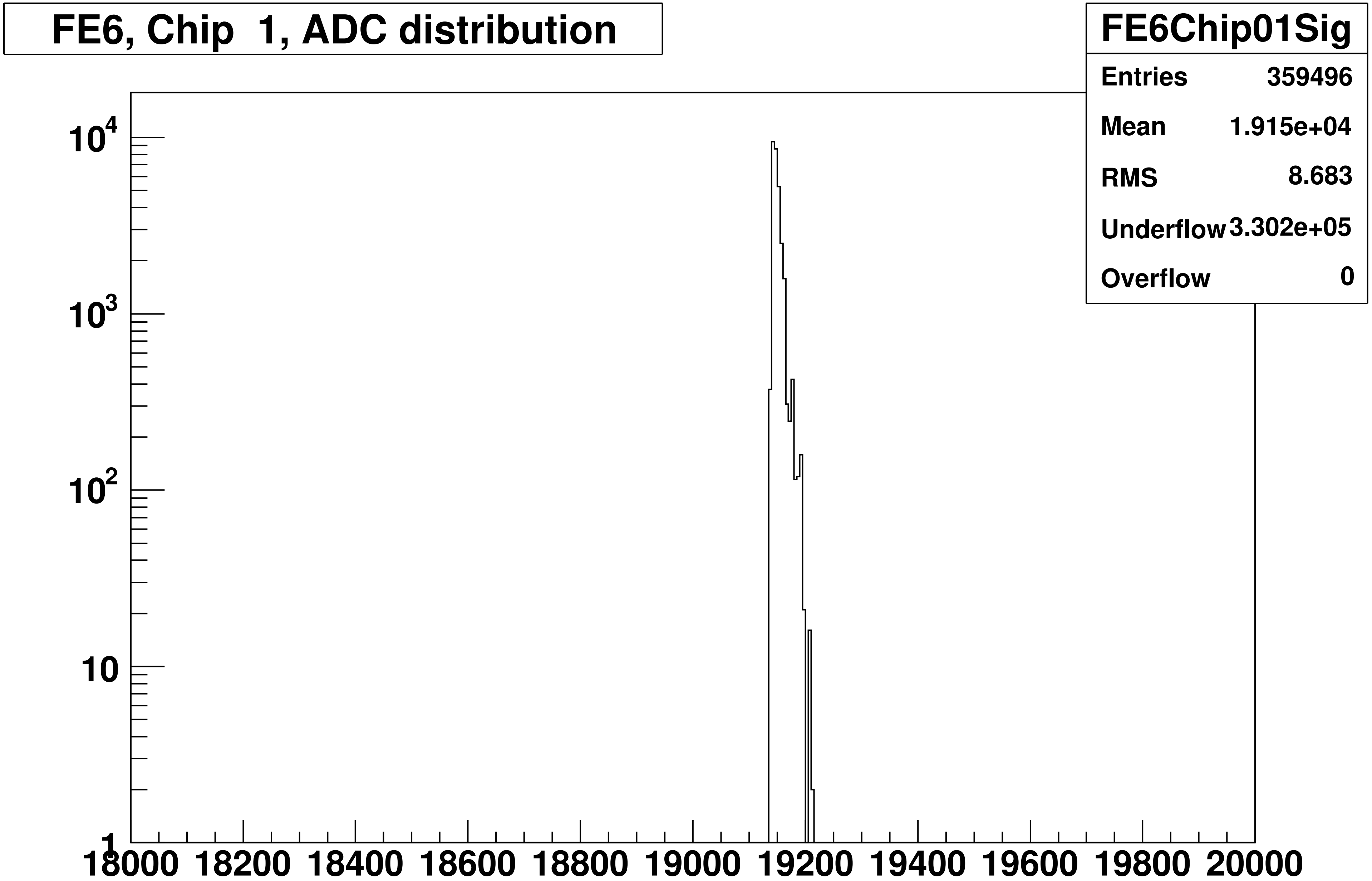
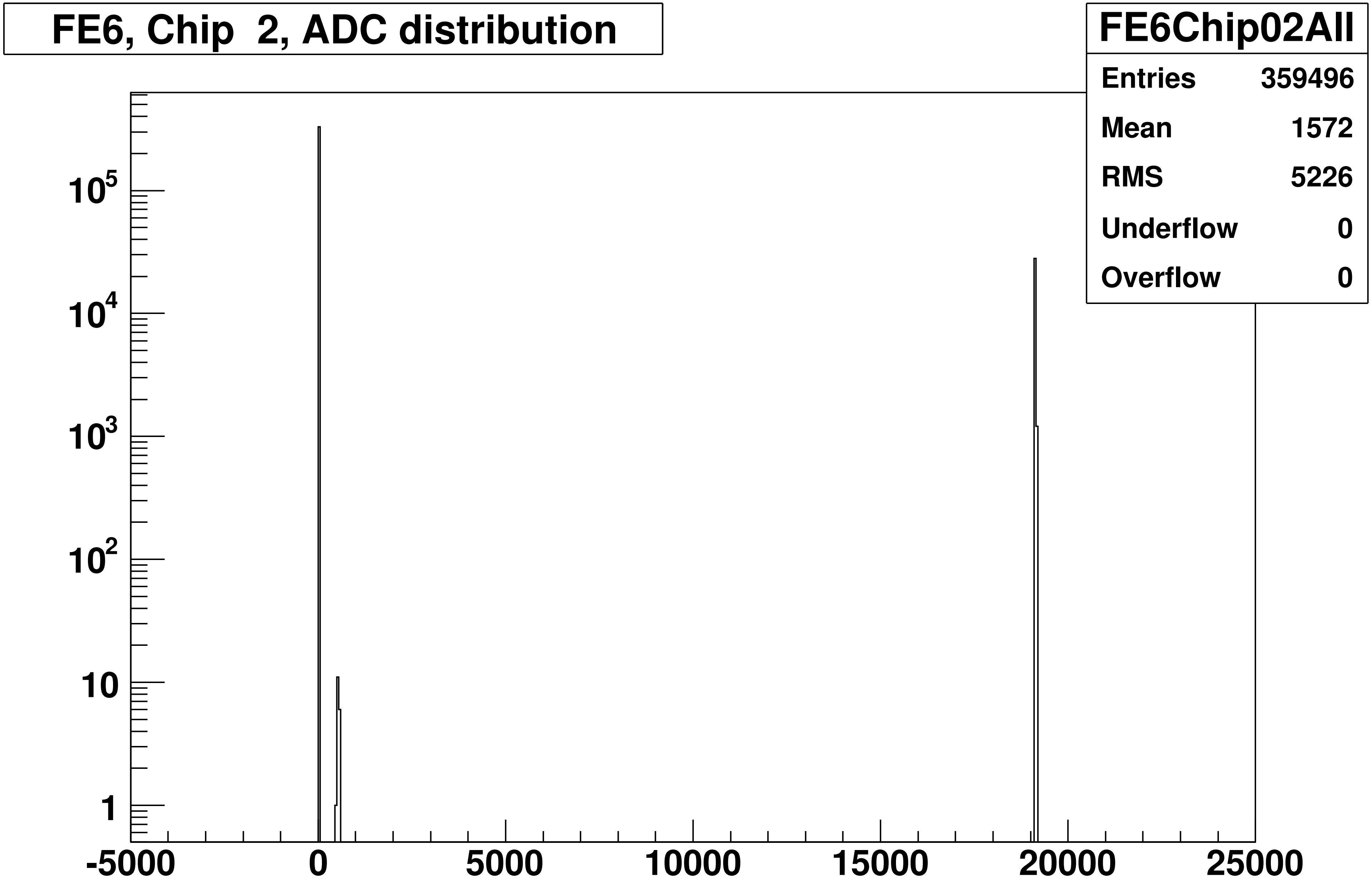
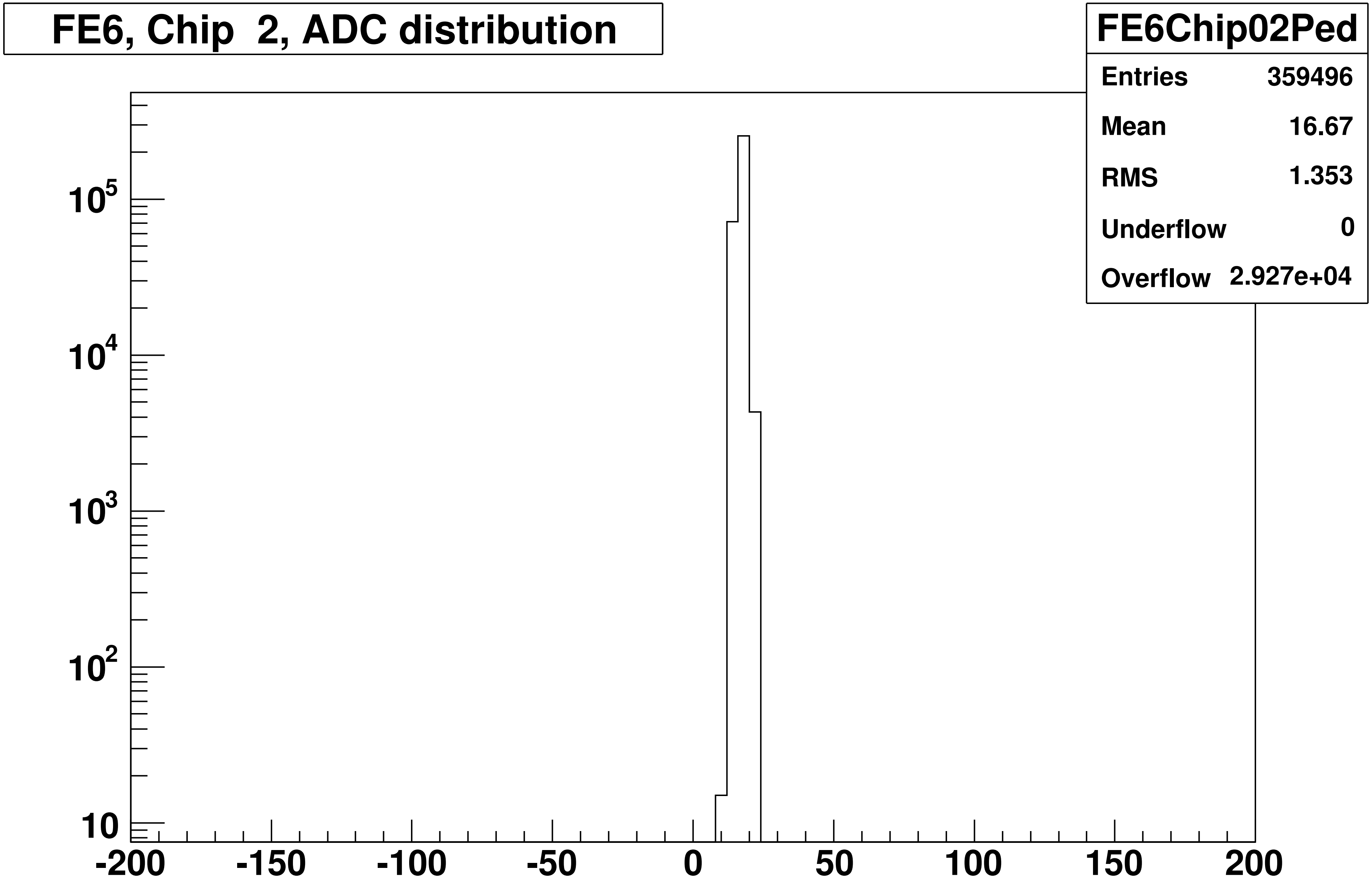
150
200



FE6, Chip 1, ADC distribution
FE6Chip01Sig
Entries 359496
Mean 1.915e+04
RMS 8.683
Underflow 3.302e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE6, Chip 2, ADC distribution
FE6Chip02All
Entries 359496
Mean 1572
RMS 5226
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE6, Chip 2, ADC distribution
FE6Chip02Ped
Entries 359496
Mean 16.67
RMS 1.353
Underflow 0
Overflow 2.927e+04
10^5
10^4
10^3
10^2
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-200
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-100
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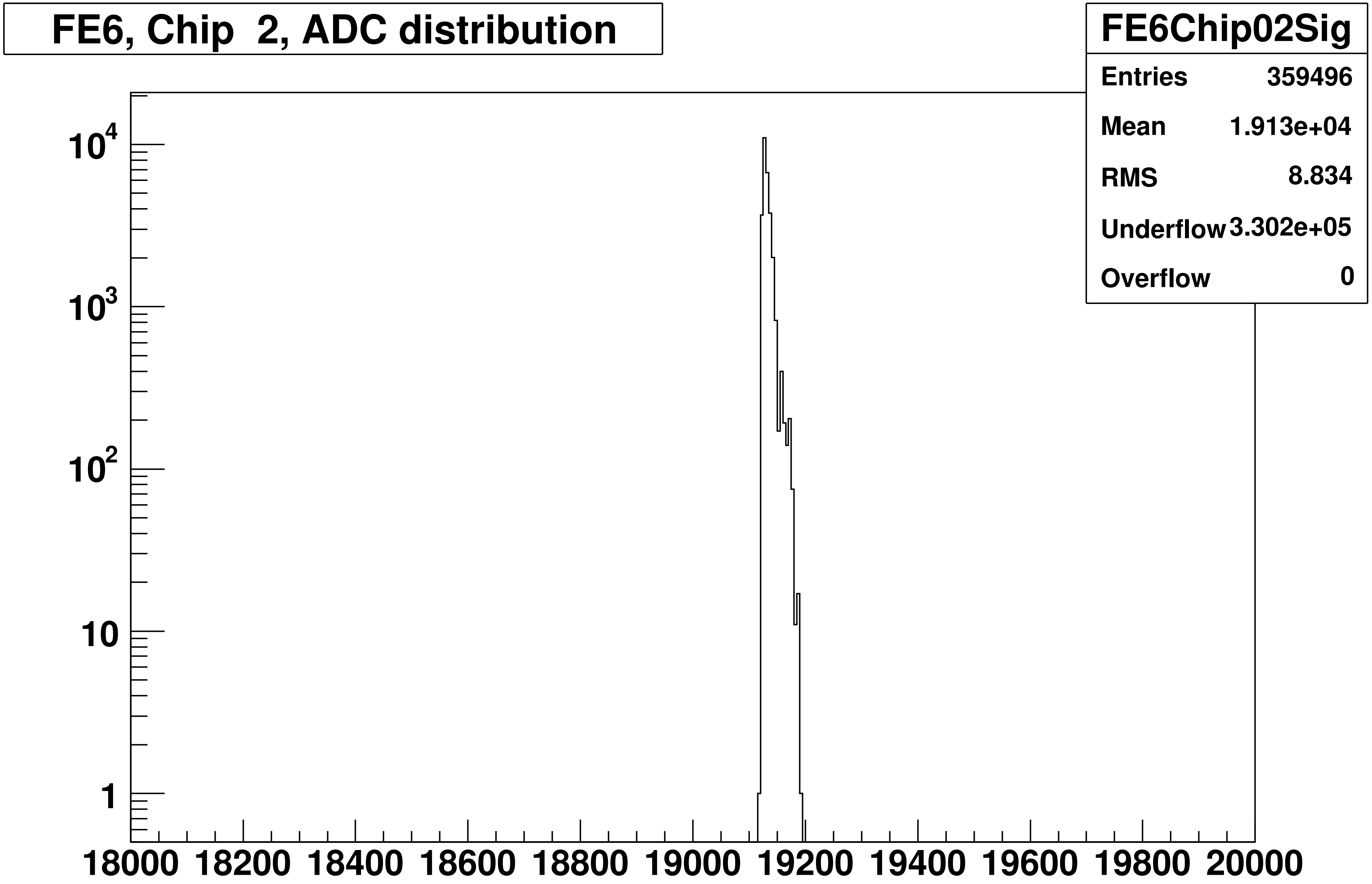
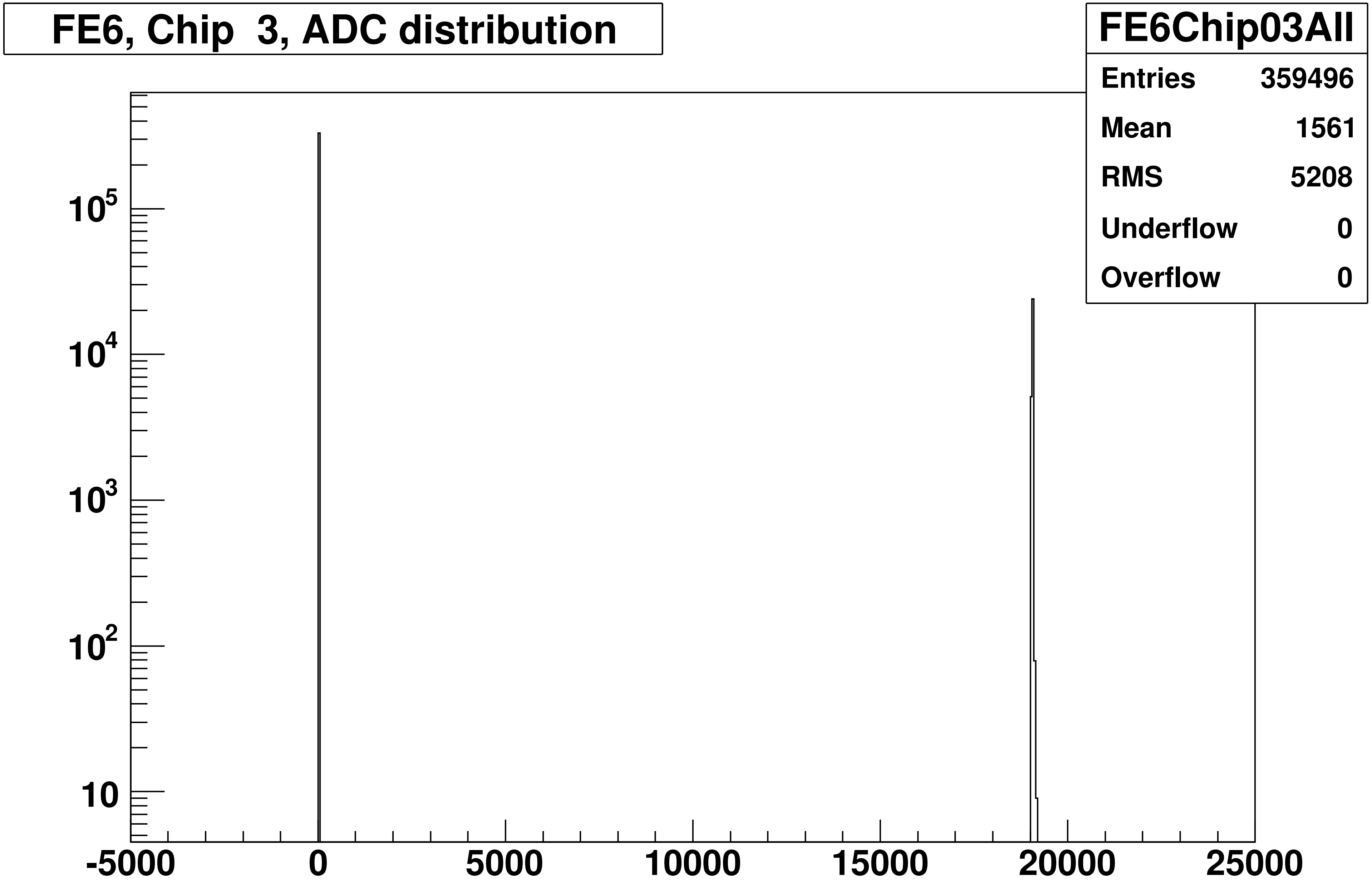
100
150
200



FE6, Chip 2, ADC distribution
FE6Chip02Sig
Entries 359496
Mean 1.913e+04
RMS 8.834
Underflow 3.302e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE6, Chip 3, ADC distribution
FE6Chip03All
Entries 359496
Mean 1561
RMS 5208
Underflow 0
Overflow 0
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10^4
10^3
10^2
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10000
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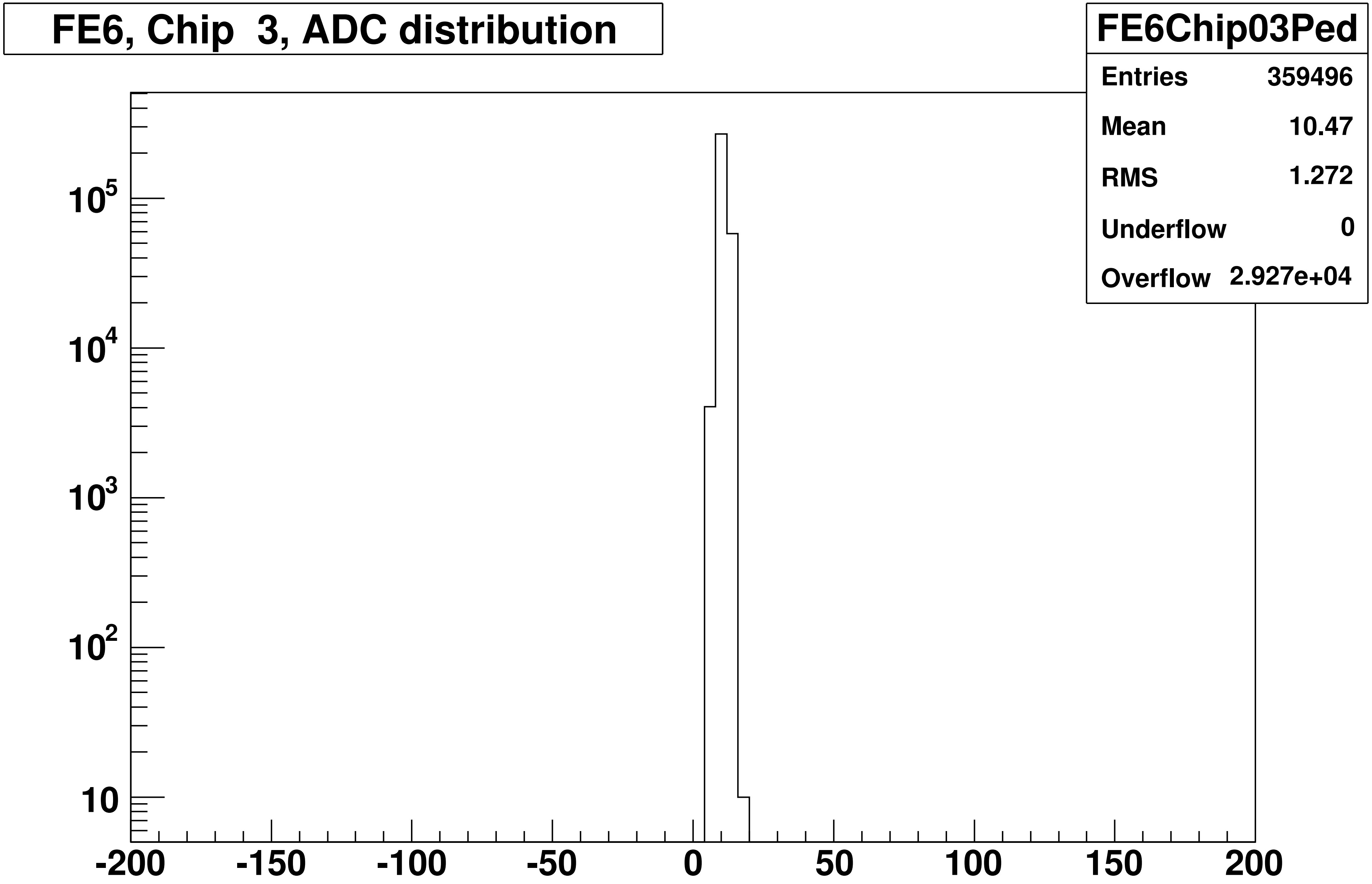
25000


FE6, Chip 3, ADC distribution
FE6Chip03Ped
Entries 359496
Mean 10.47
RMS 1.272
Underflow 0
Overflow 2.927e+04
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10^4
10^3
10^2
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150
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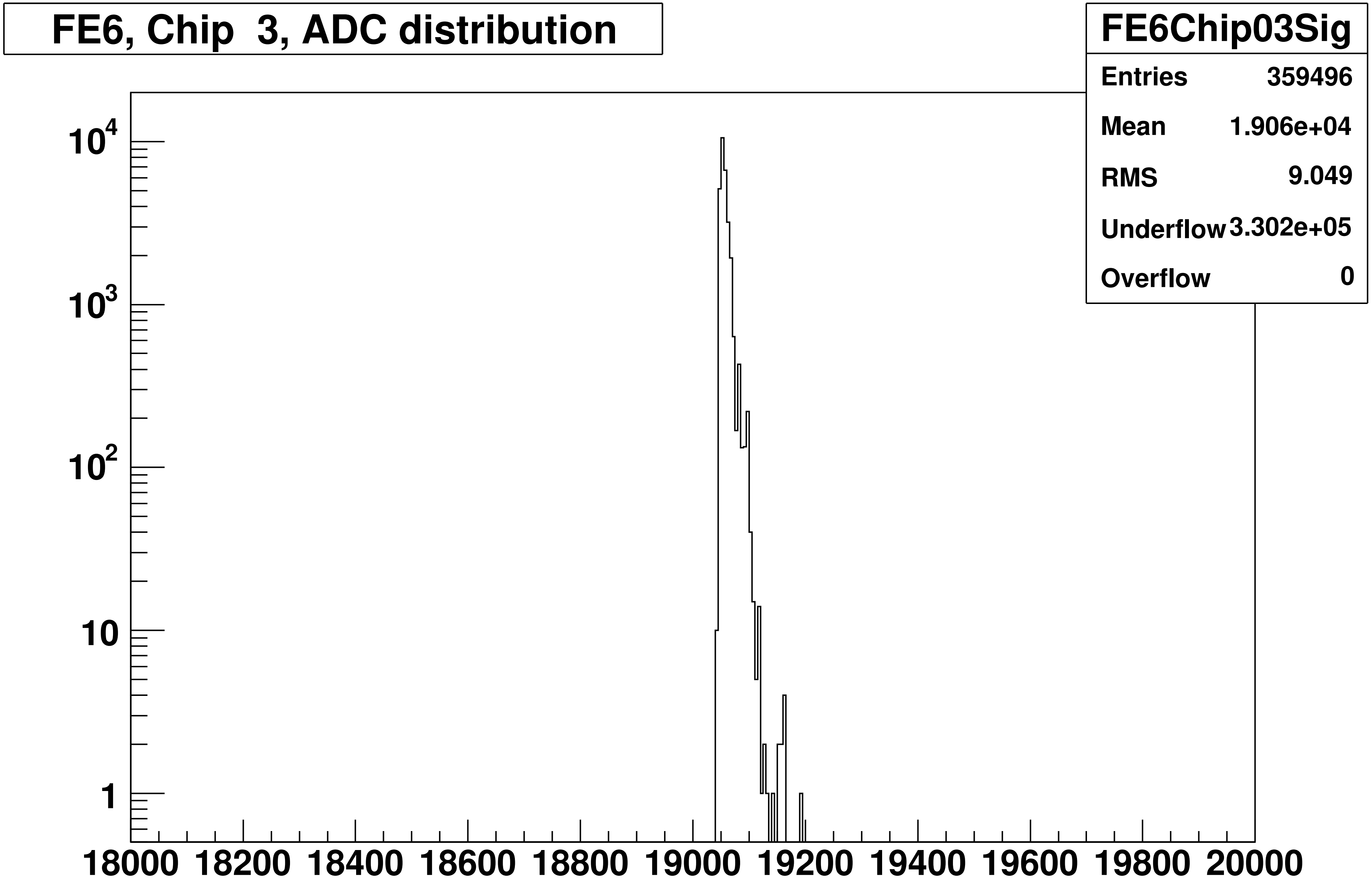
FE6, Chip 3, ADC distribution
FE6Chip03Sig
Entries 359496
Mean 1.906e+04
RMS 9.049
Underflow 3.302e+05
Overflow 0
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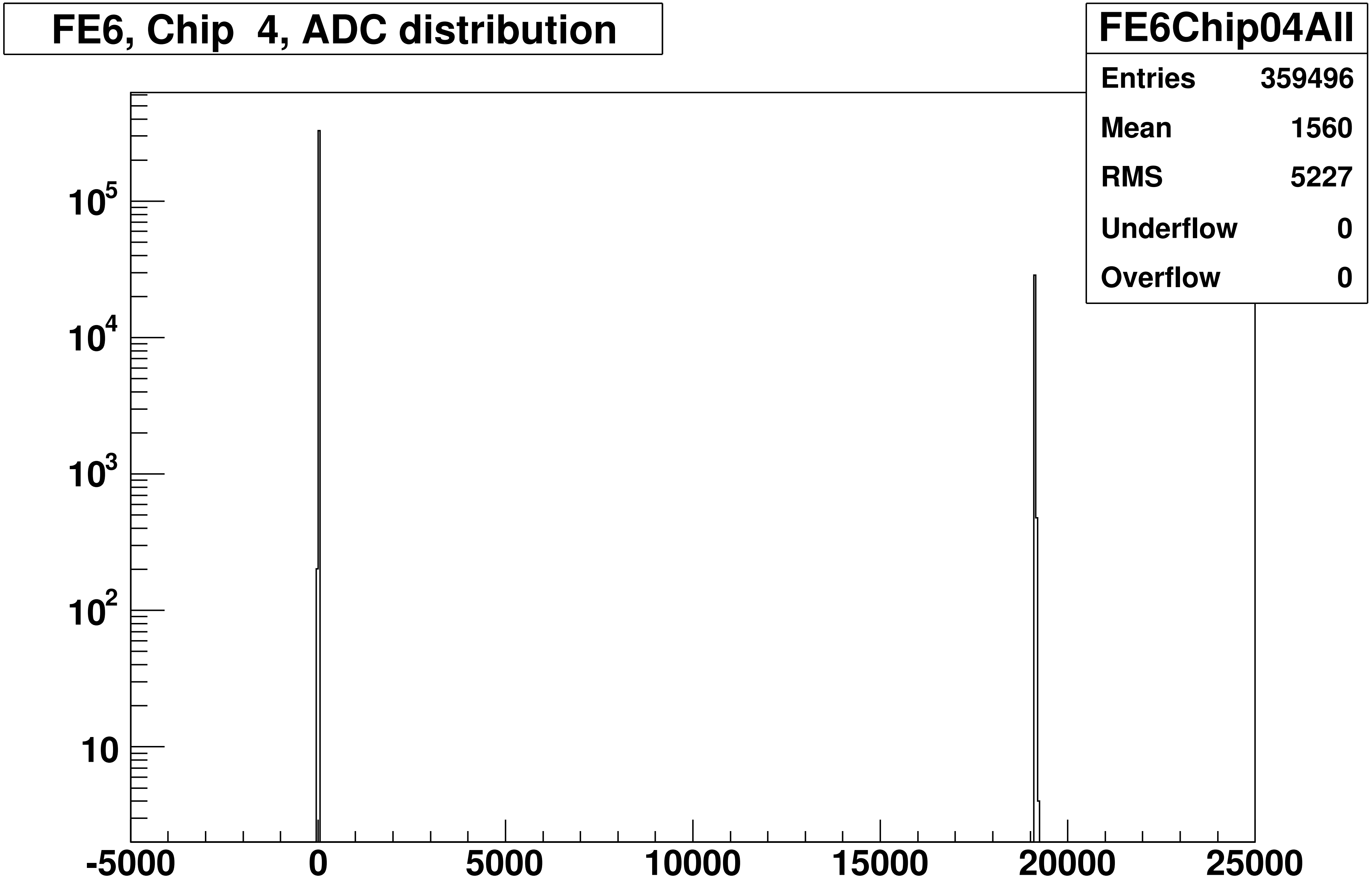
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE6, Chip 4, ADC distribution
FE6Chip04All
Entries 359496
Mean 1560
RMS 5227
Underflow 0
Overflow 0
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10^2
10^3
10^4
10^5
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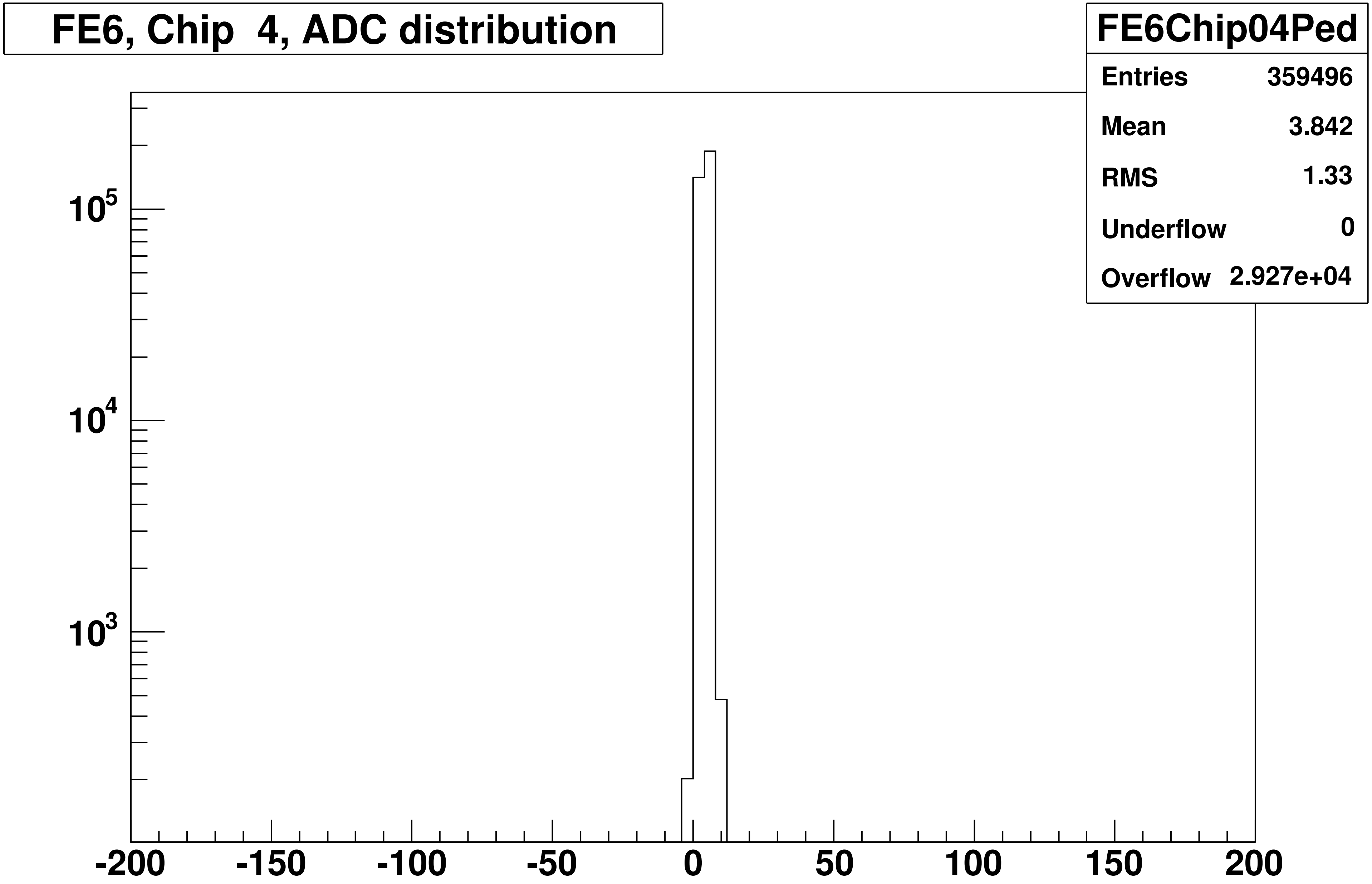
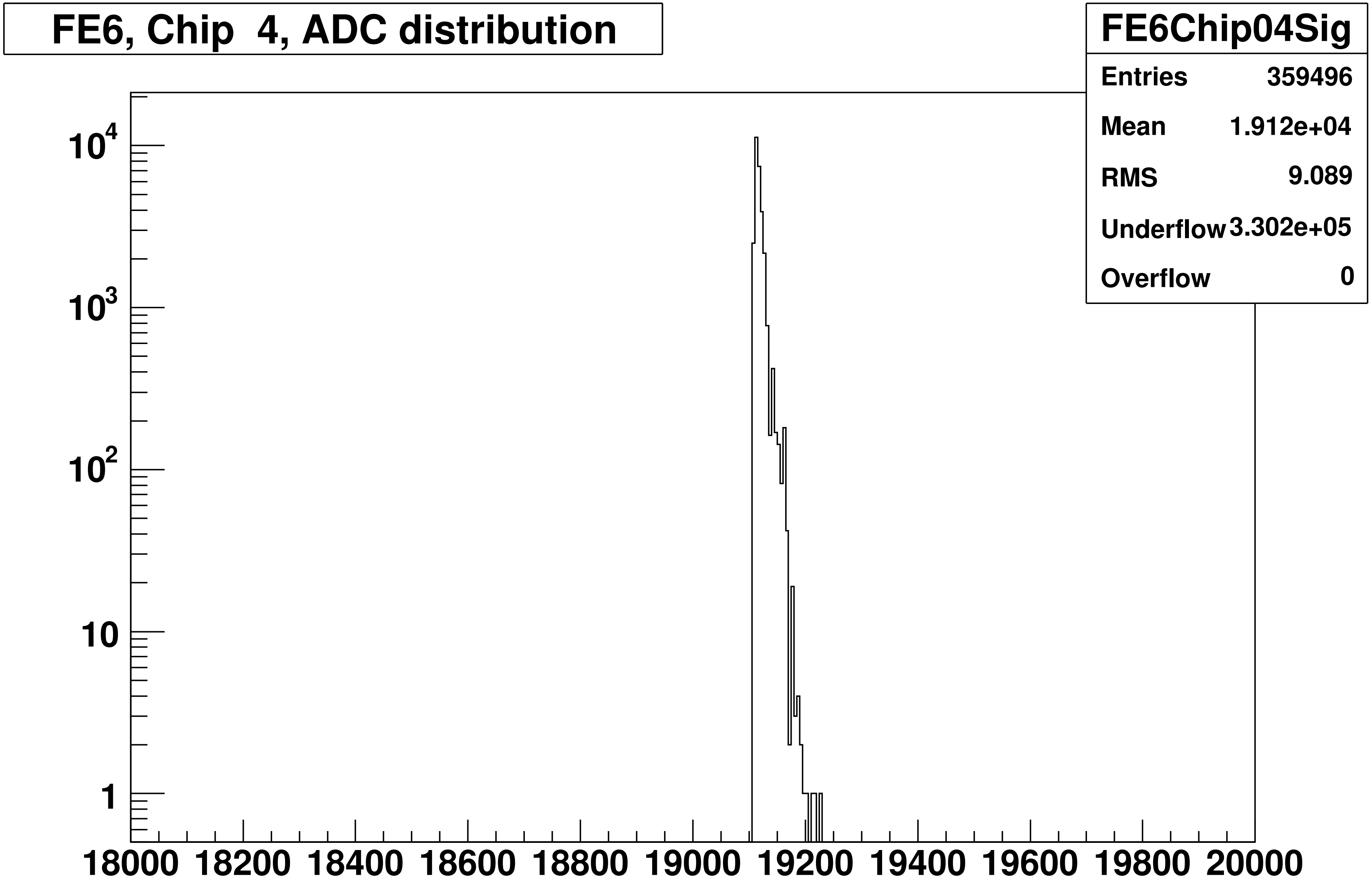
15000
20000
25000



FE6, Chip 4, ADC distribution
FE6Chip04Ped
Entries 359496
Mean 3.842
RMS 1.33
Underflow 0
Overflow 2.927e+04
10^5
10^4
10^3
-200
-150
-100
-50
0
50
100
150
200


FE6, Chip 4, ADC distribution
FE6Chip04Sig
Entries 359496
Mean 1.912e+04
RMS 9.089
Underflow 3.302e+05
Overflow 0
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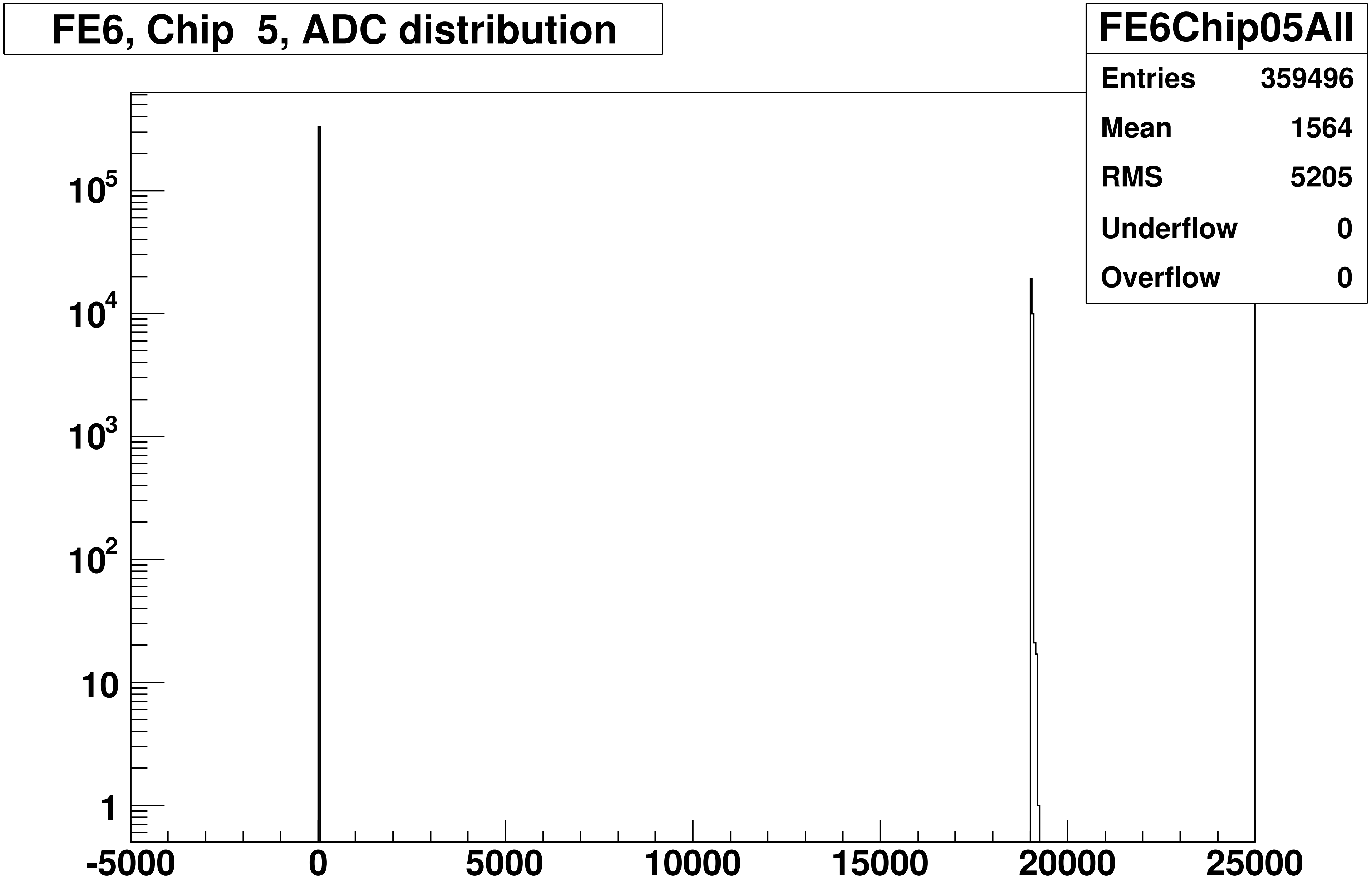
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE6, Chip 5, ADC distribution
FE6Chip05All
Entries 359496
Mean 1564
RMS 5205
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
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0
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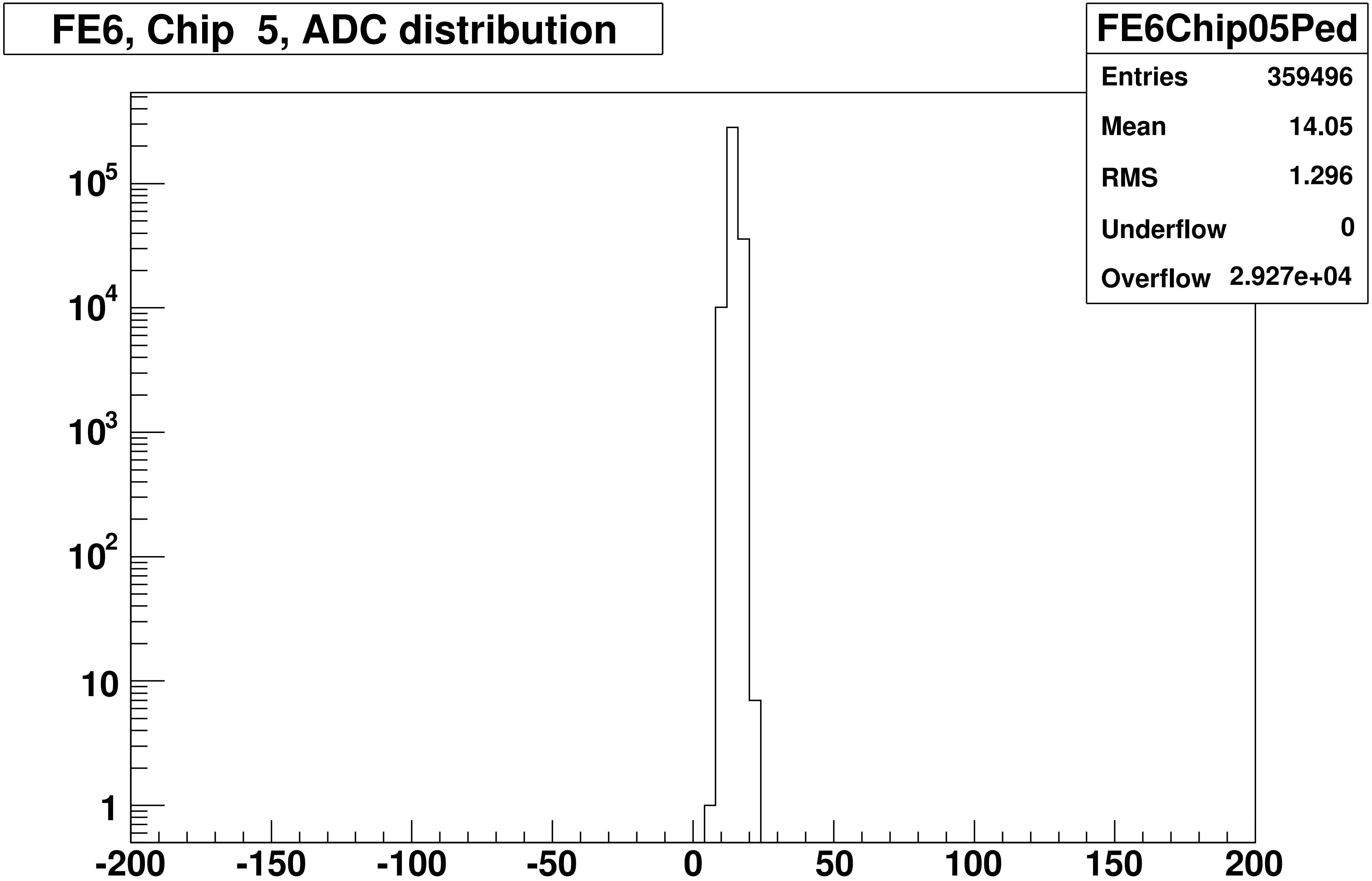
10000
15000
20000
25000


FE6, Chip 5, ADC distribution
FE6Chip05Ped
Entries 359496
Mean 14.05
RMS 1.296
Underflow 0
Overflow 2.927e+04
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10^4
10^3
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-100
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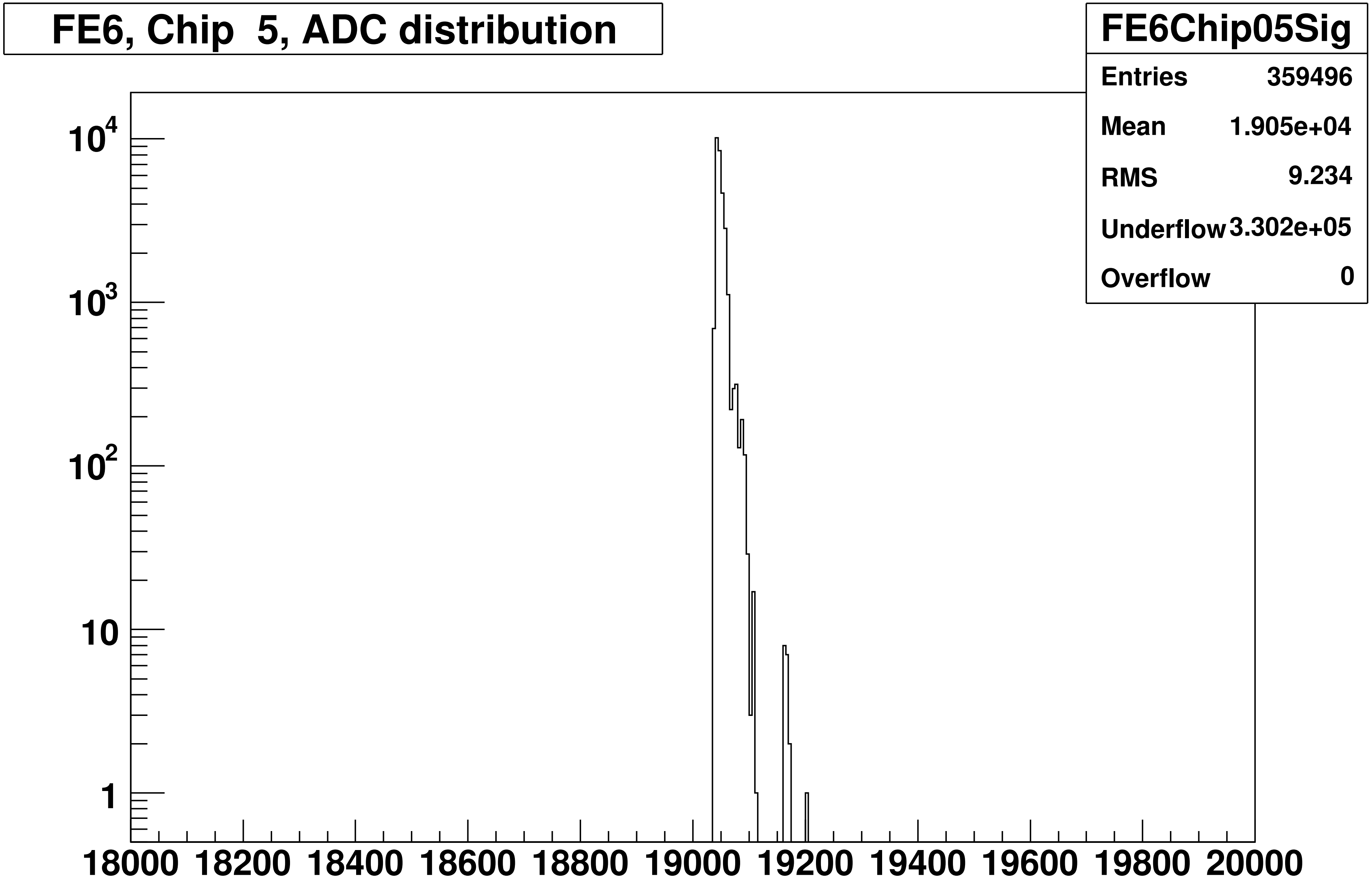
0
50
100
150
200


FE6, Chip 5, ADC distribution
FE6Chip05Sig
Entries 359496
Mean 1.905e+04
RMS 9.234
Underflow 3.302e+05
Overflow 0
10^4
10^3
10^2
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1
18000
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18400
18600
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19000
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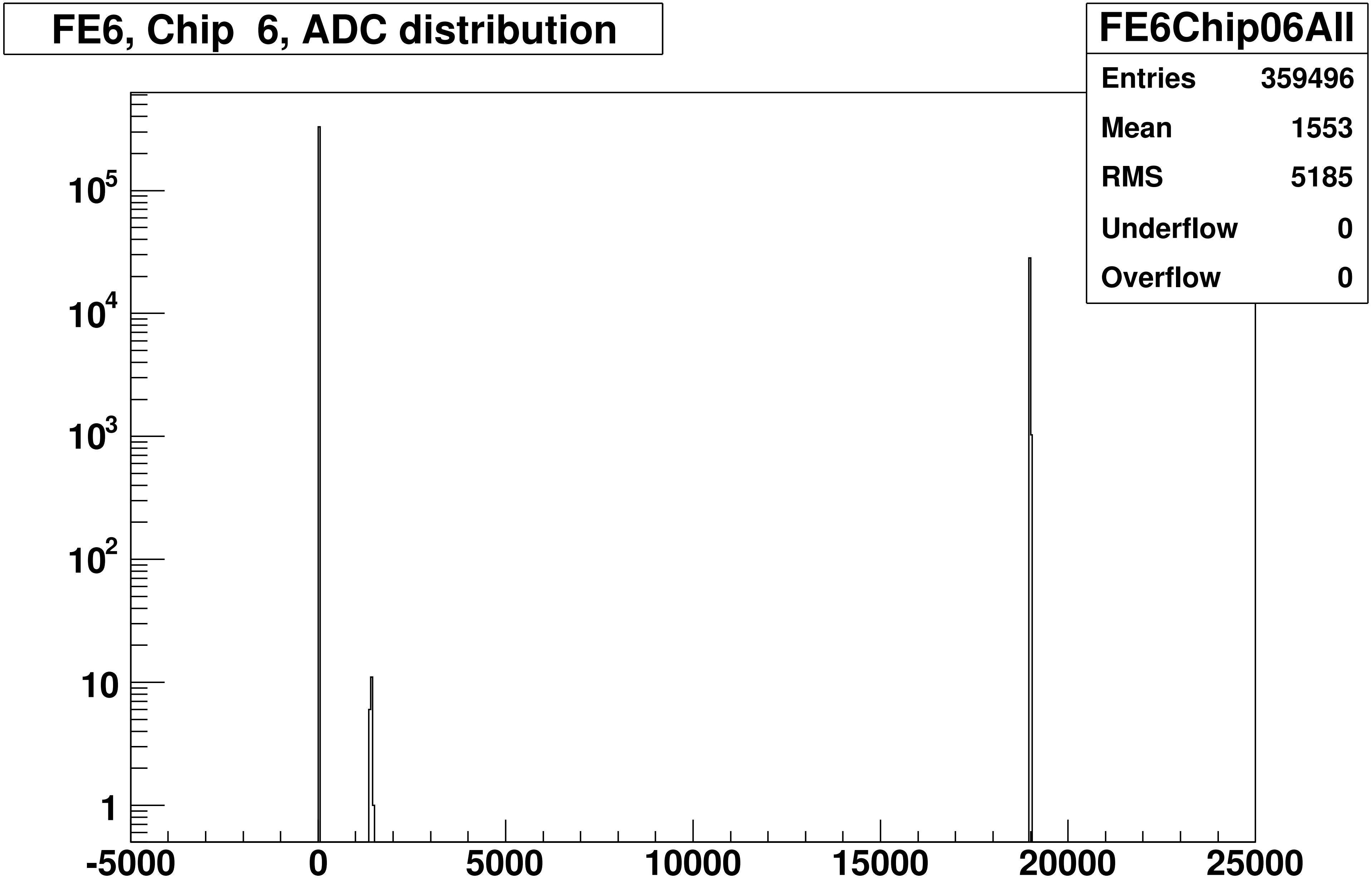
19600
19800
20000



FE6, Chip 6, ADC distribution
FE6Chip06All
Entries 359496
Mean 1553
RMS 5185
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
1
-5000
0
5000
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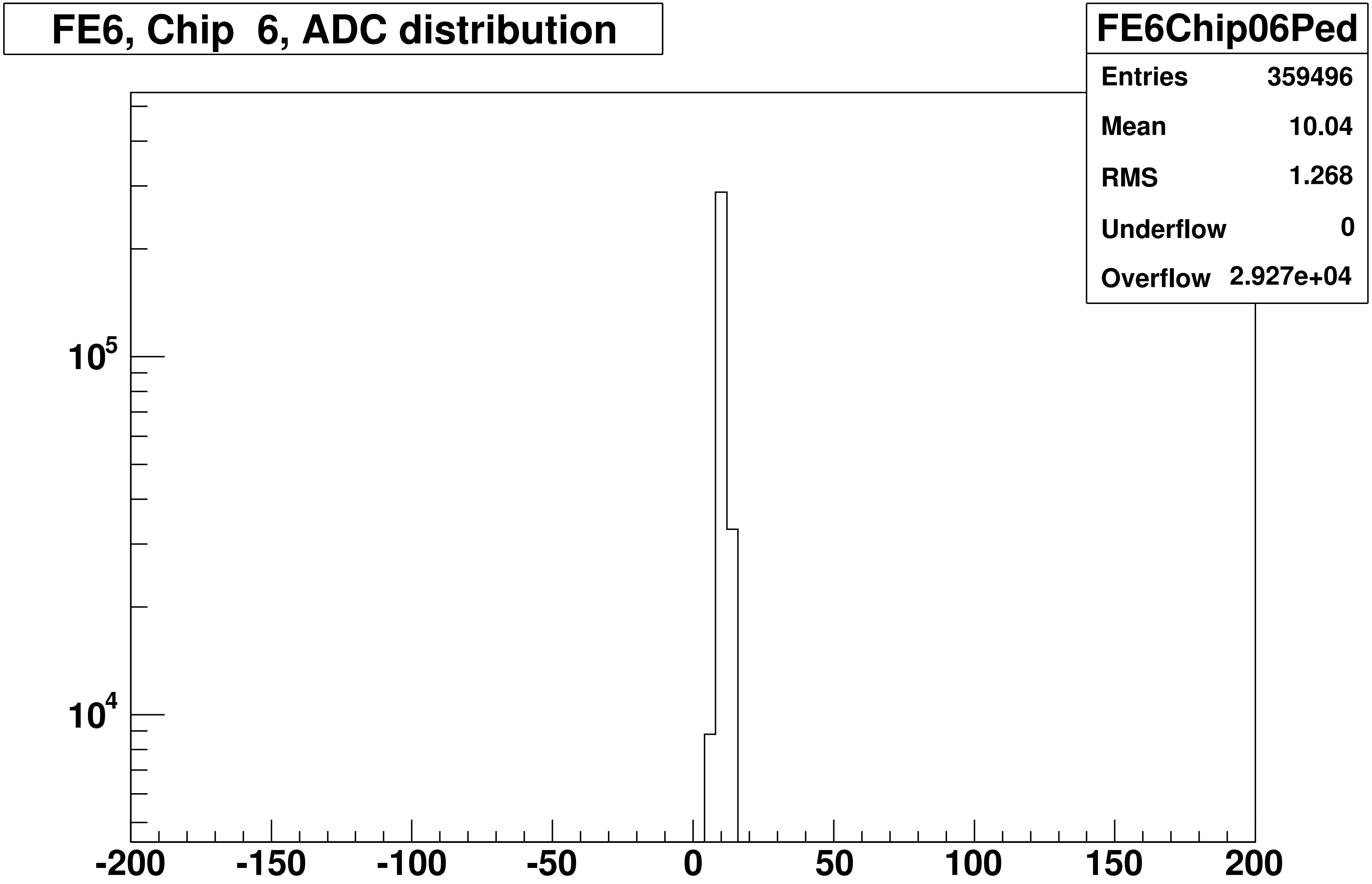
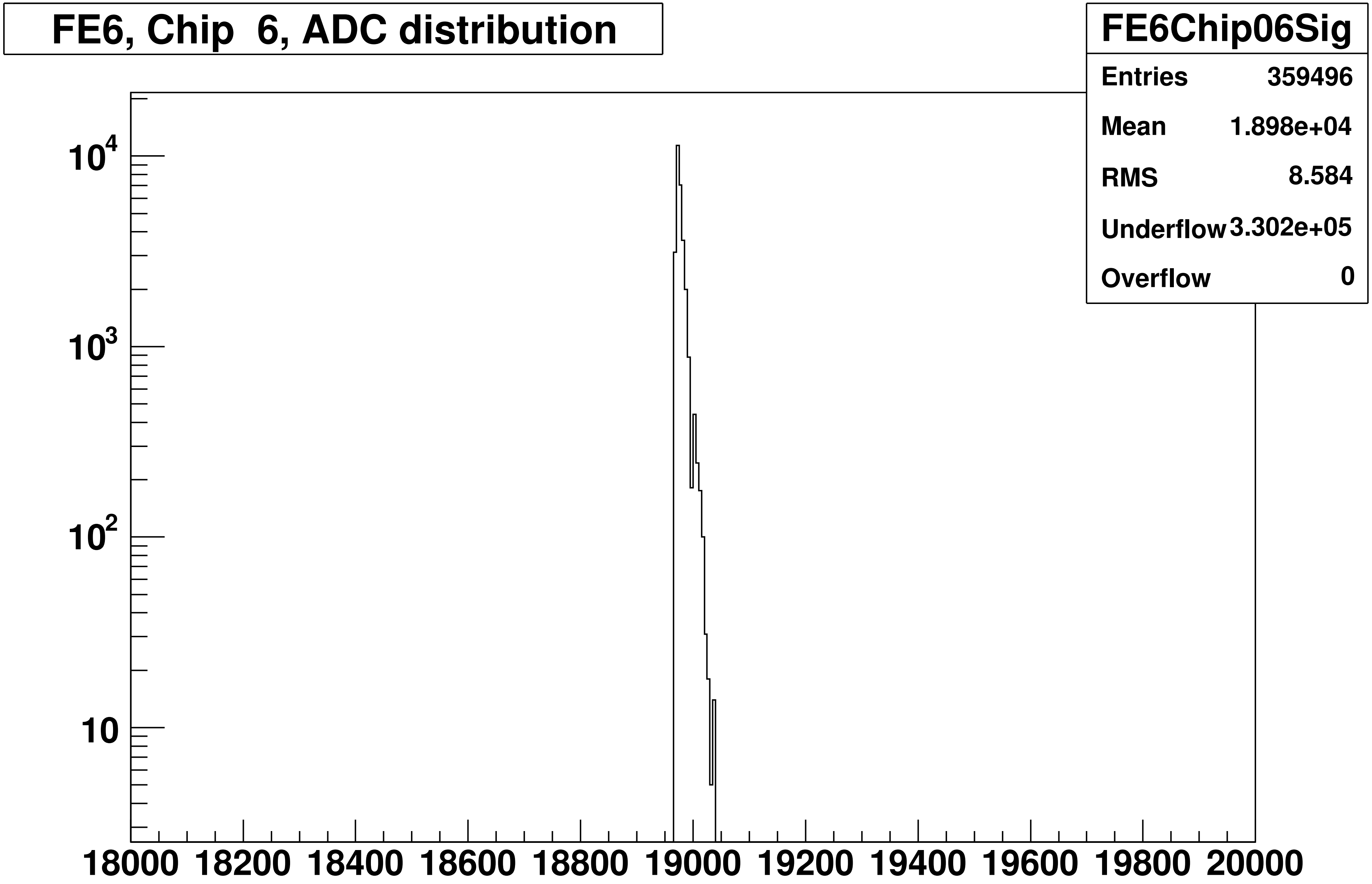
15000
20000
25000



FE6, Chip 6, ADC distribution
FE6Chip06Ped
Entries 359496
Mean 10.04
RMS 1.268
Underflow 0
Overflow 2.927e+04
10^5
10^4
-200
-150
-100
-50
0
50
100
150
200


FE6, Chip 6, ADC distribution
FE6Chip06Sig
Entries 359496
Mean 1.898e+04
RMS 8.584
Underflow 3.302e+05
Overflow 0
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10^3
10^2
10
18000
18200
18400
18600
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19000
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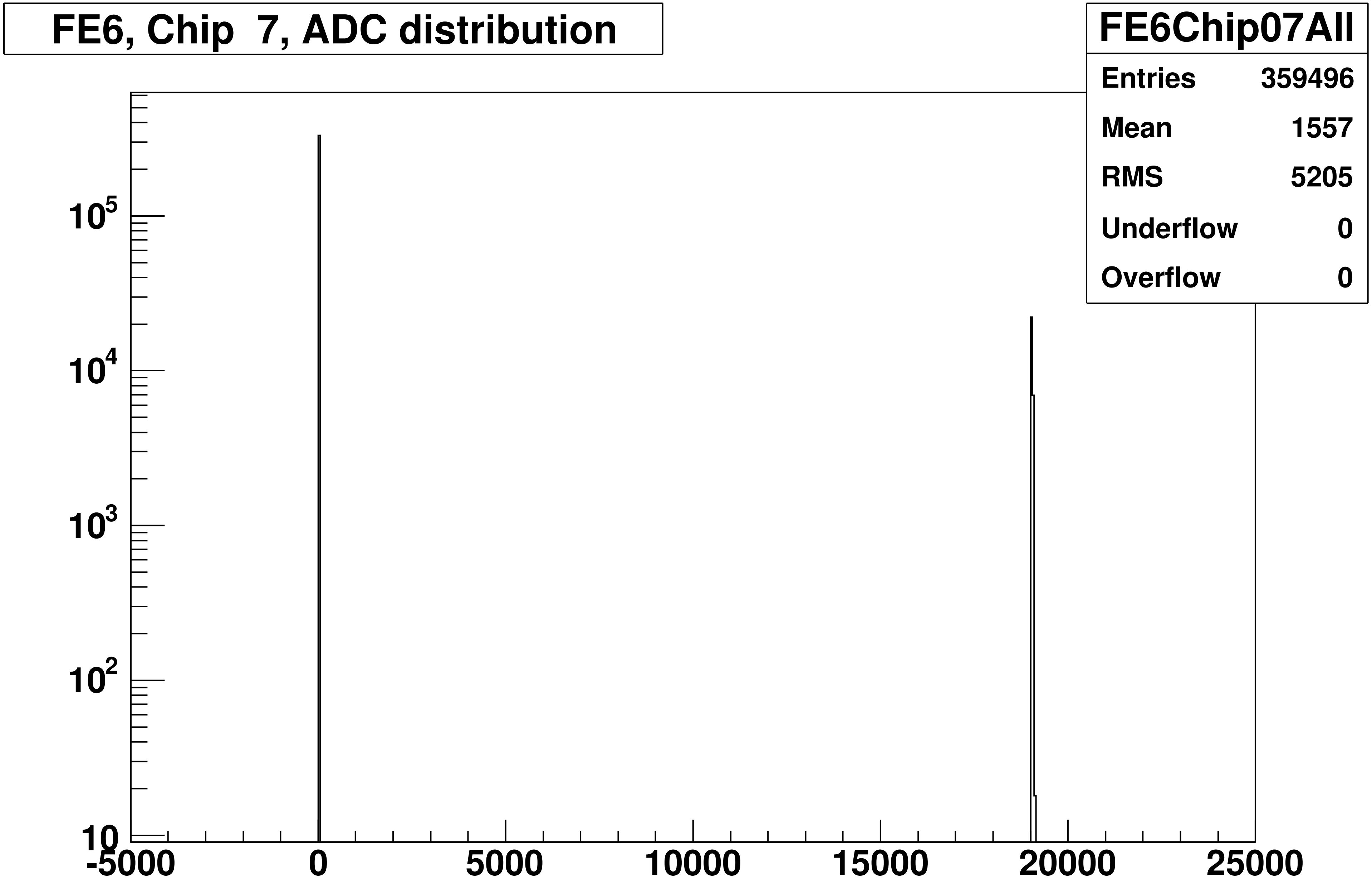
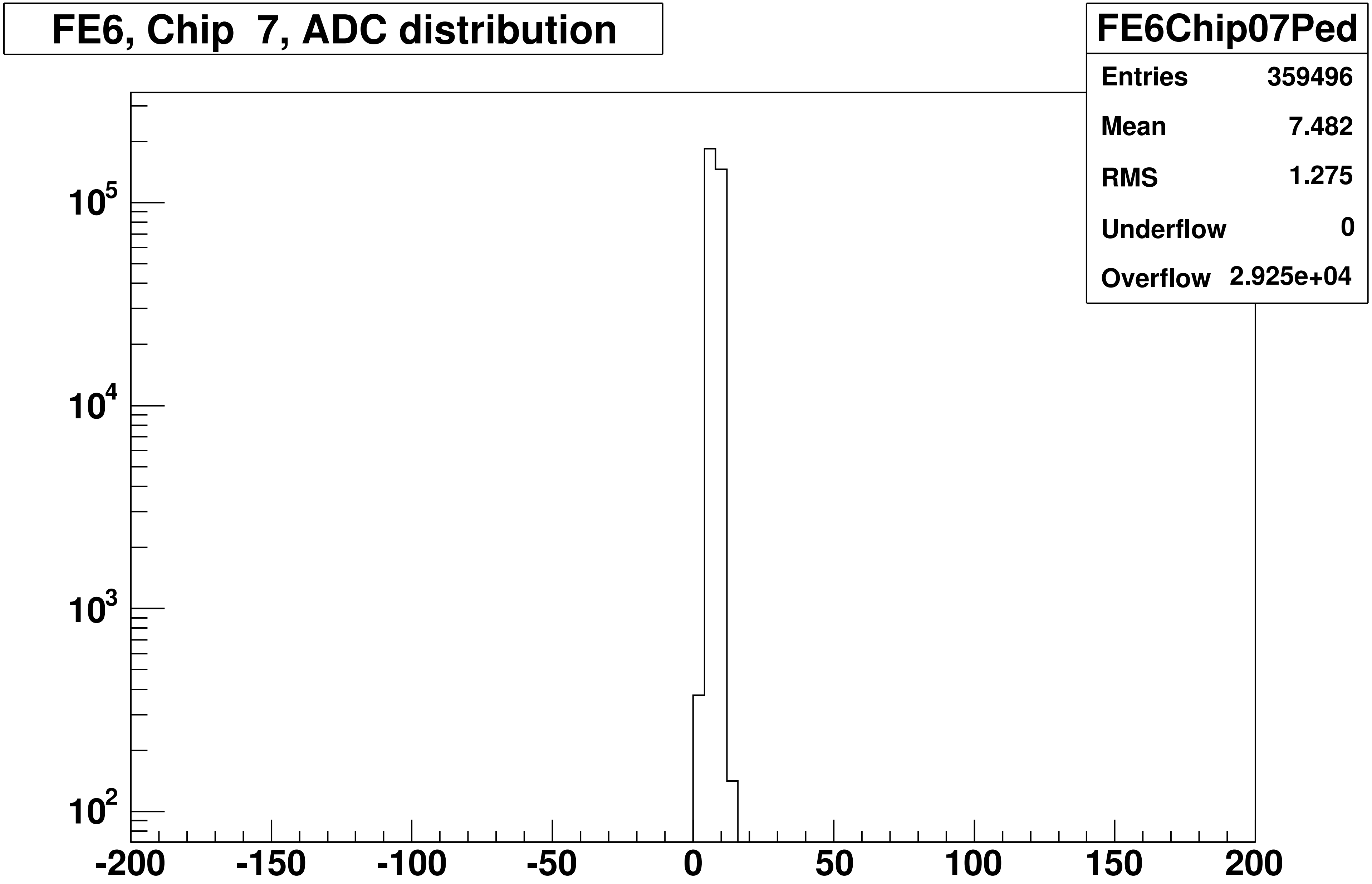
19600
19800
20000



FE6, Chip 7, ADC distribution
FE6Chip07All
Entries 359496
Mean 1557
RMS 5205
Underflow 0
Overflow 0
10
10^2
10^3
10^4
10^5
-5000
0
5000
10000
15000
20000
25000


FE6, Chip 7, ADC distribution
FE6Chip07Ped
Entries 359496
Mean 7.482
RMS 1.275
Underflow 0
Overflow 2.925e+04
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10^4
10^3
10^2
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-100
-50
0
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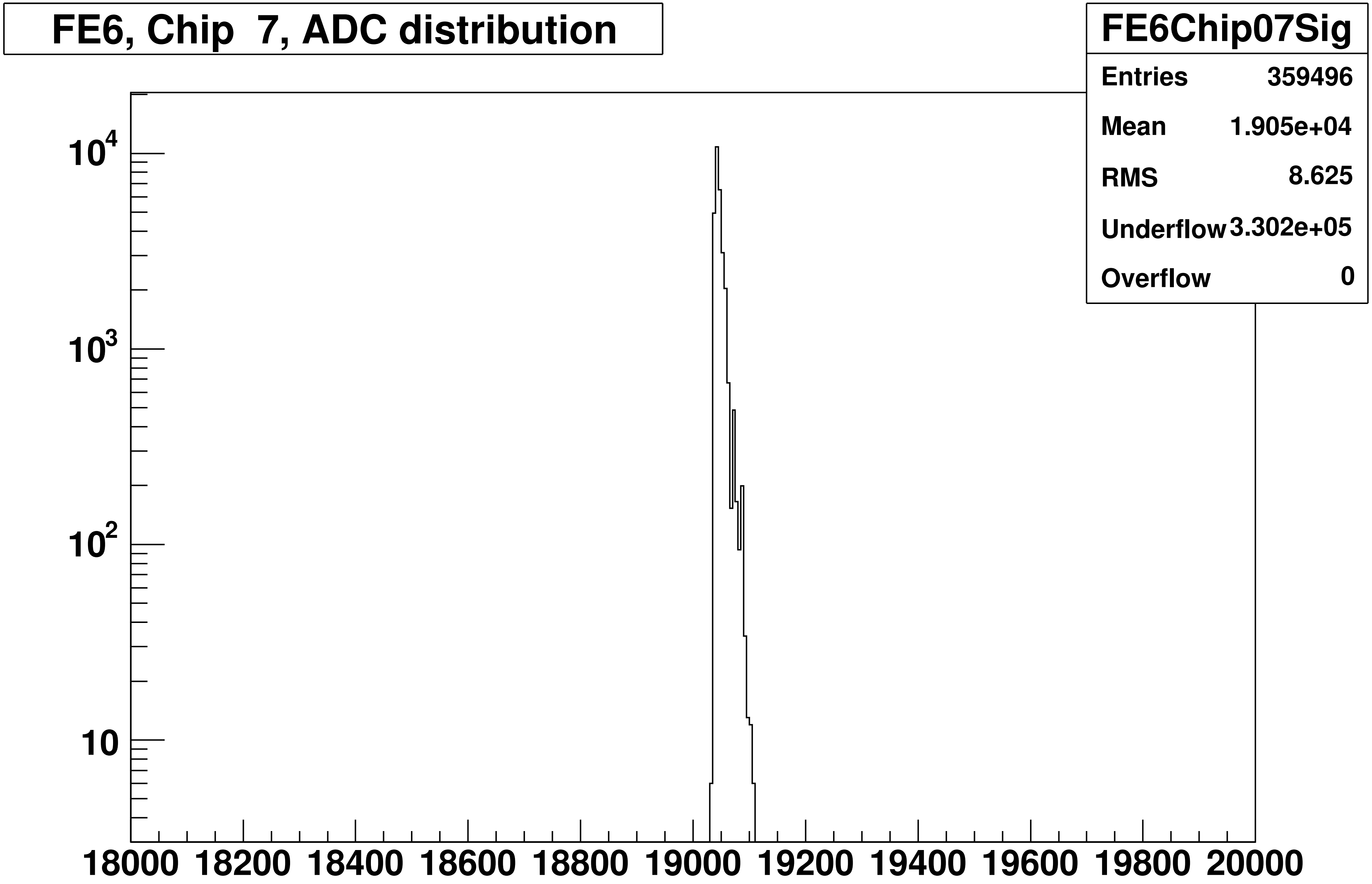
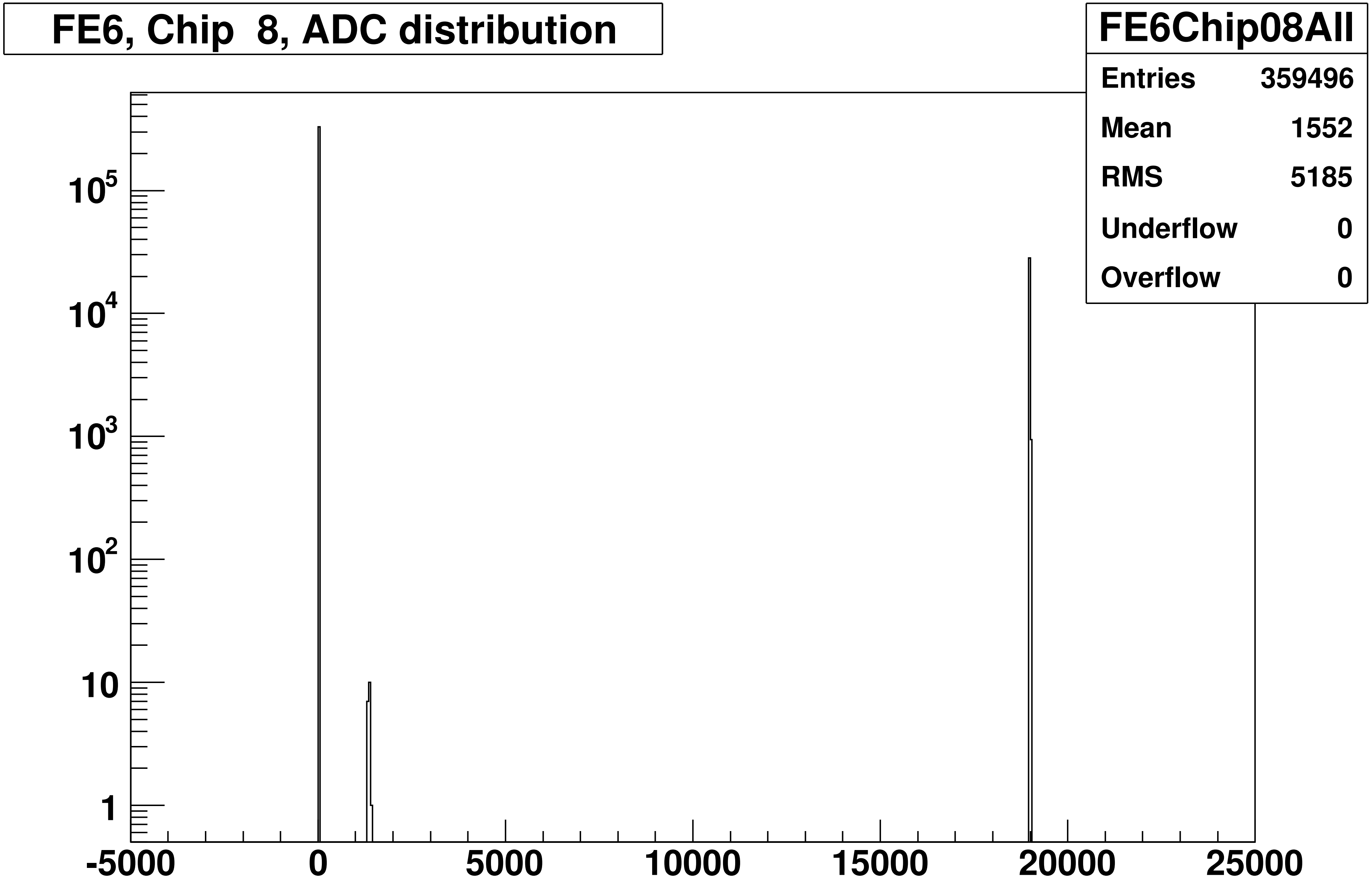
100
150
200


FE6, Chip 7, ADC distribution
FE6Chip07Sig
Entries 359496
Mean 1.905e+04
RMS 8.625
Underflow 3.302e+05
Overflow 0
10^4
10^3
10^2
10
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000


FE6, Chip 8, ADC distribution
FE6Chip08All
Entries 359496
Mean 1552
RMS 5185
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
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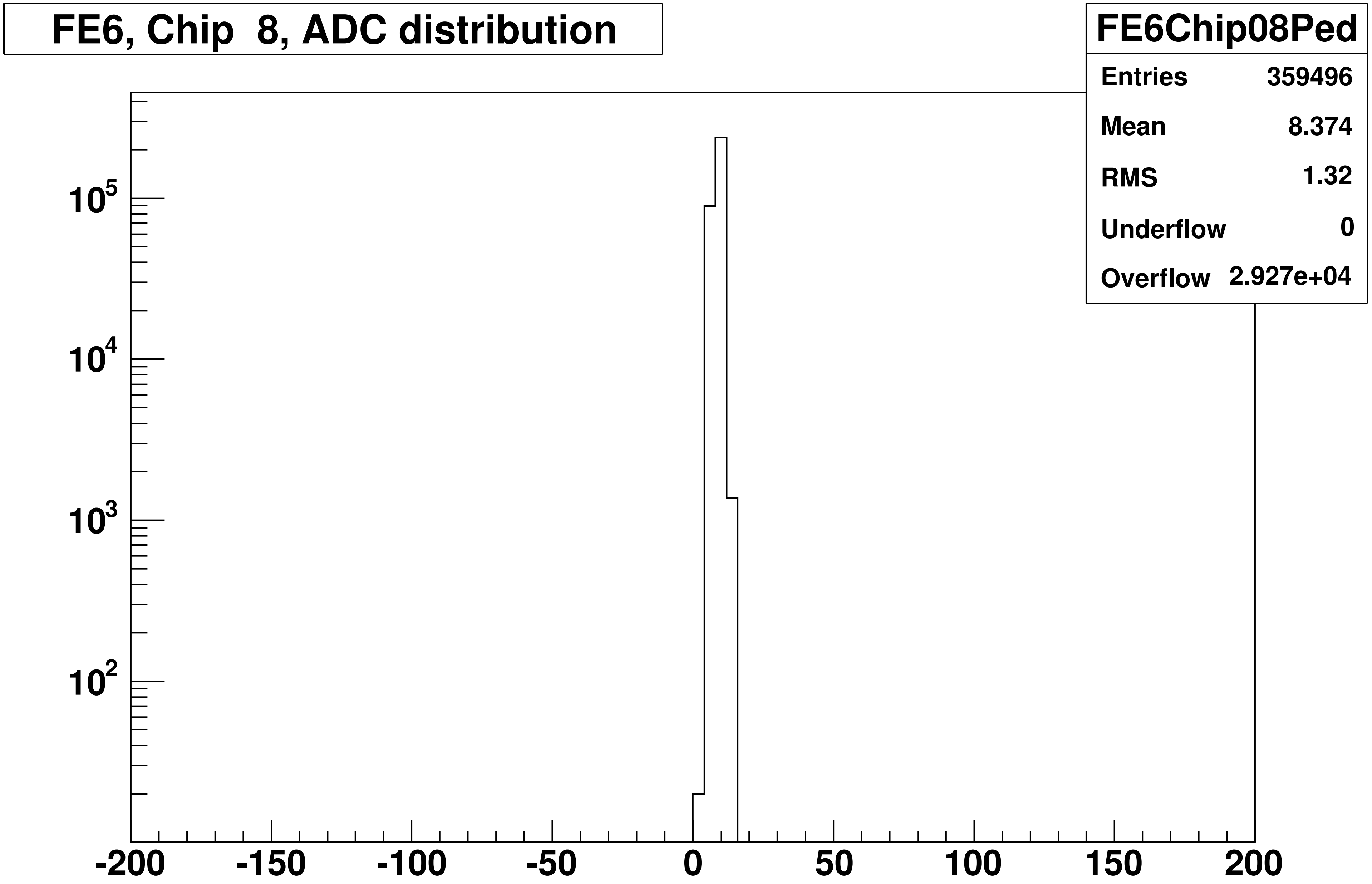
FE6, Chip 8, ADC distribution
FE6Chip08Ped
Entries 359496
Mean 8.374
RMS 1.32
Underflow 0
Overflow 2.927e+04
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10^4
10^3
10^2
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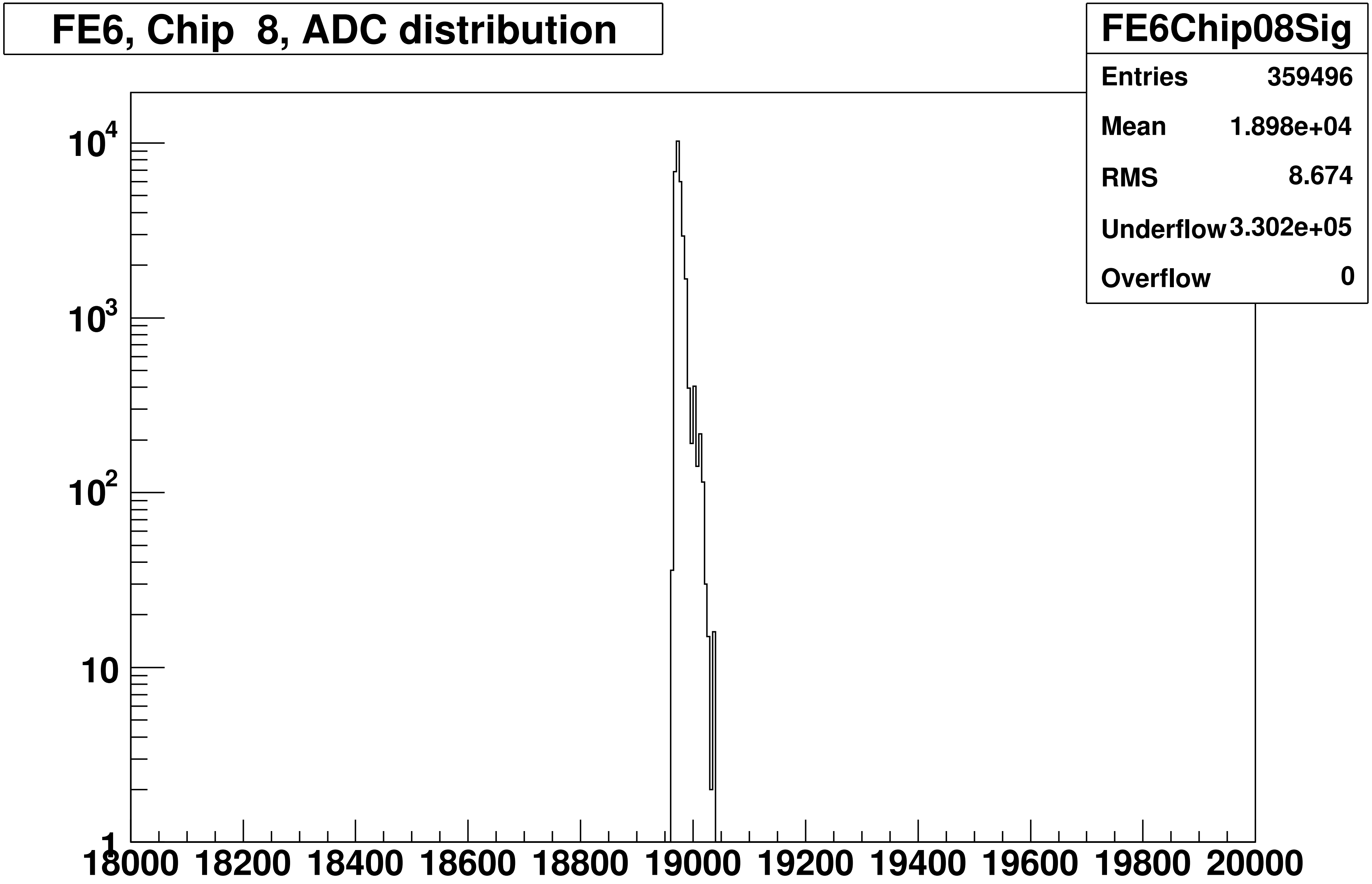
100
150
200


FE6, Chip 8, ADC distribution
FE6Chip08Sig
Entries 359496
Mean 1.898e+04
RMS 8.674
Underflow 3.302e+05
Overflow 0
10^4
10^3
10^2
10
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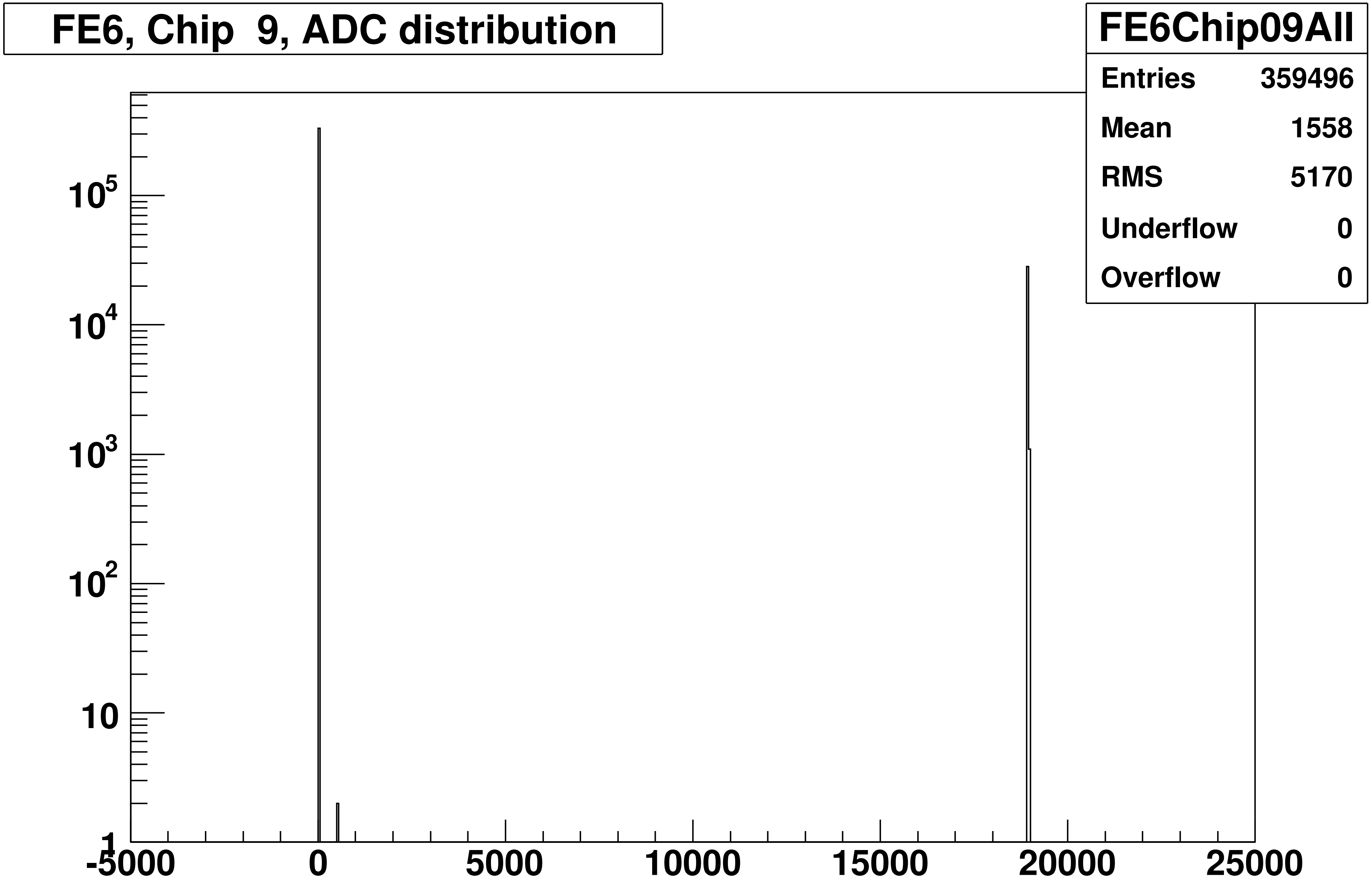
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE6, Chip 9, ADC distribution
FE6Chip09All
Entries 359496
Mean 1558
RMS 5170
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
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-5000
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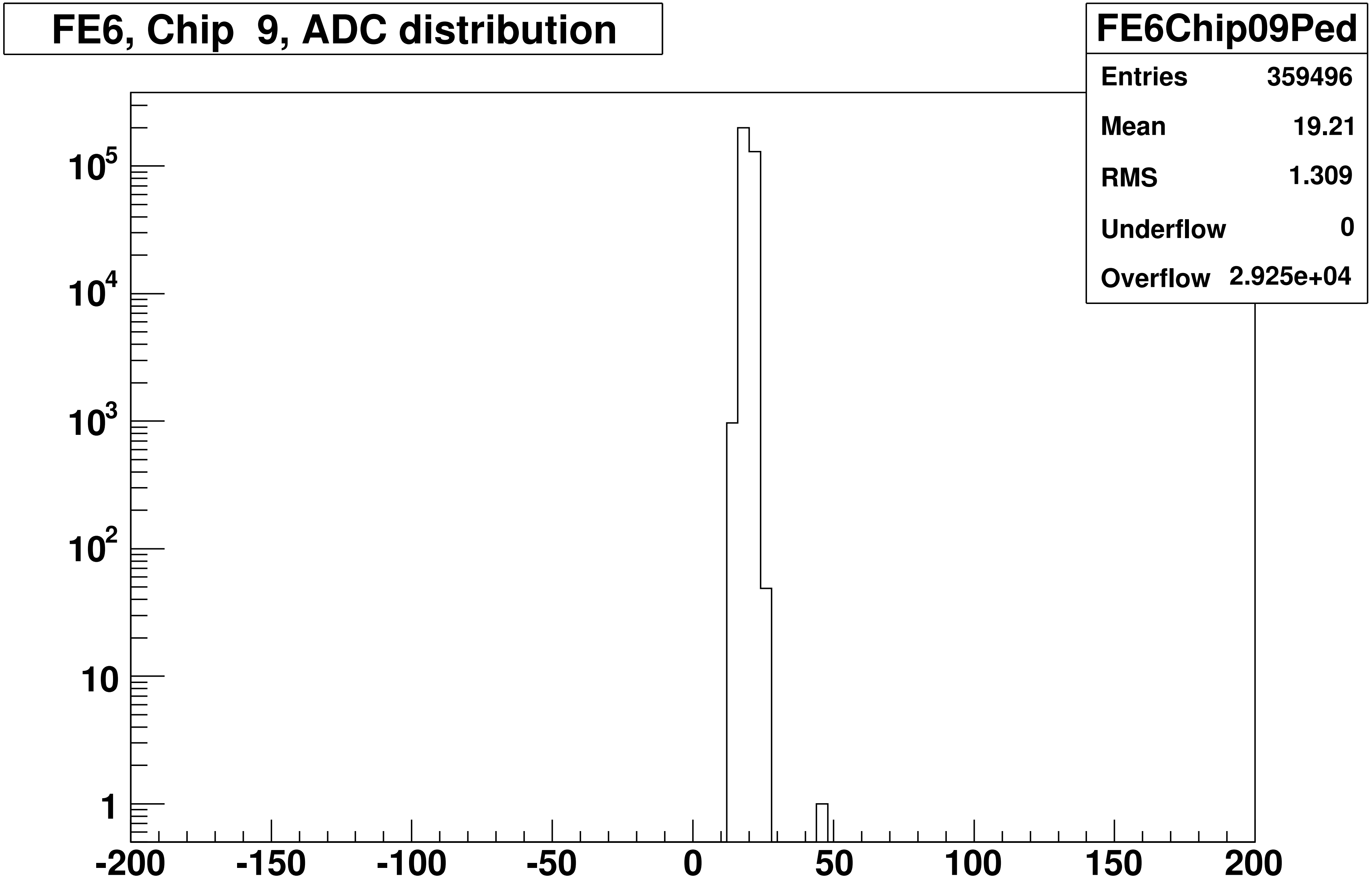
10000
15000
20000
25000



FE6, Chip 9, ADC distribution
FE6Chip09Ped
Entries 359496
Mean 19.21
RMS 1.309
Underflow 0
Overflow 2.925e+04
10^5
10^4
10^3
10^2
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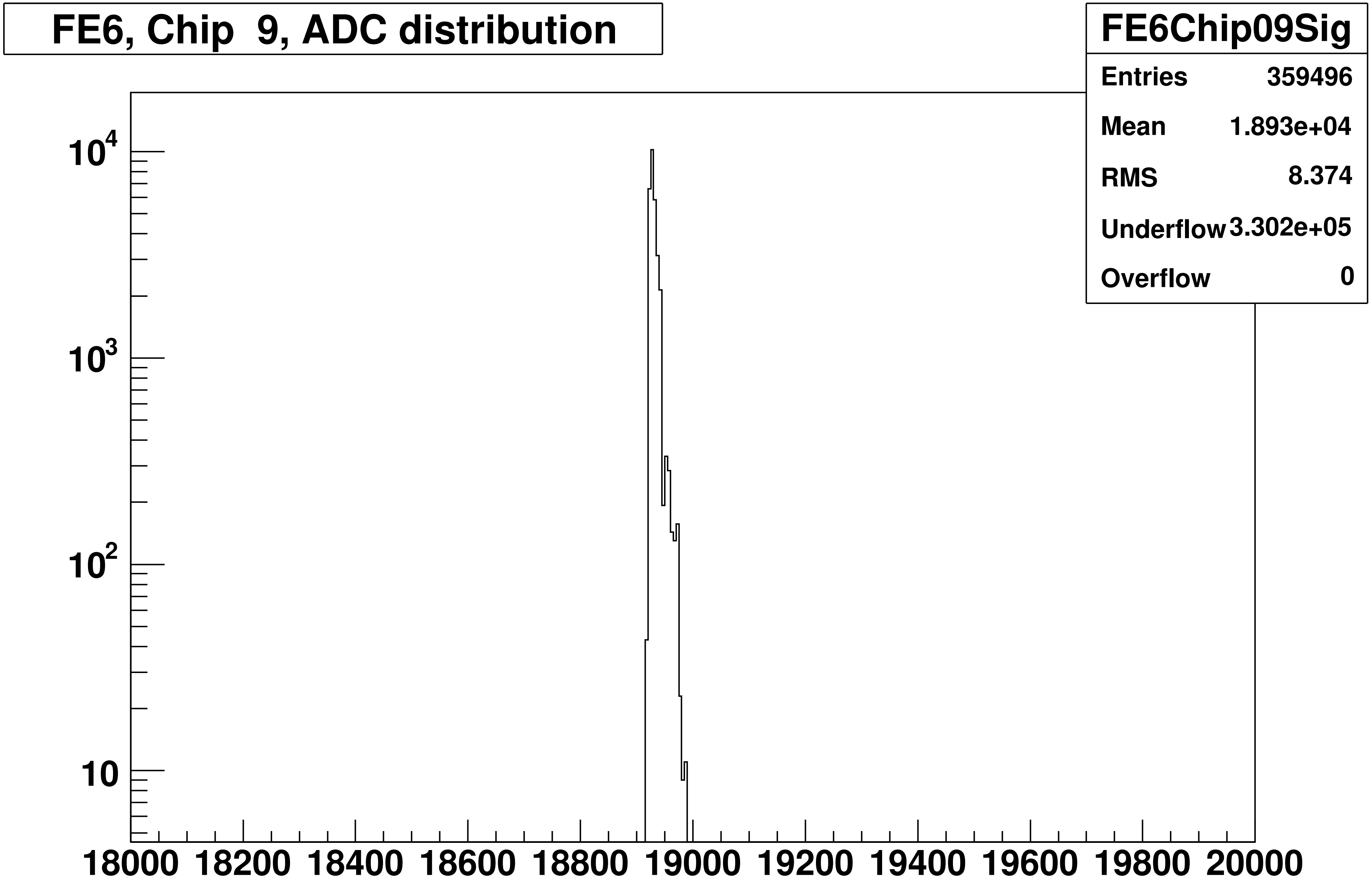
FE6, Chip 9, ADC distribution
FE6Chip09Sig
Entries 359496
Mean 1.893e+04
RMS 8.374
Underflow 3.302e+05
Overflow 0
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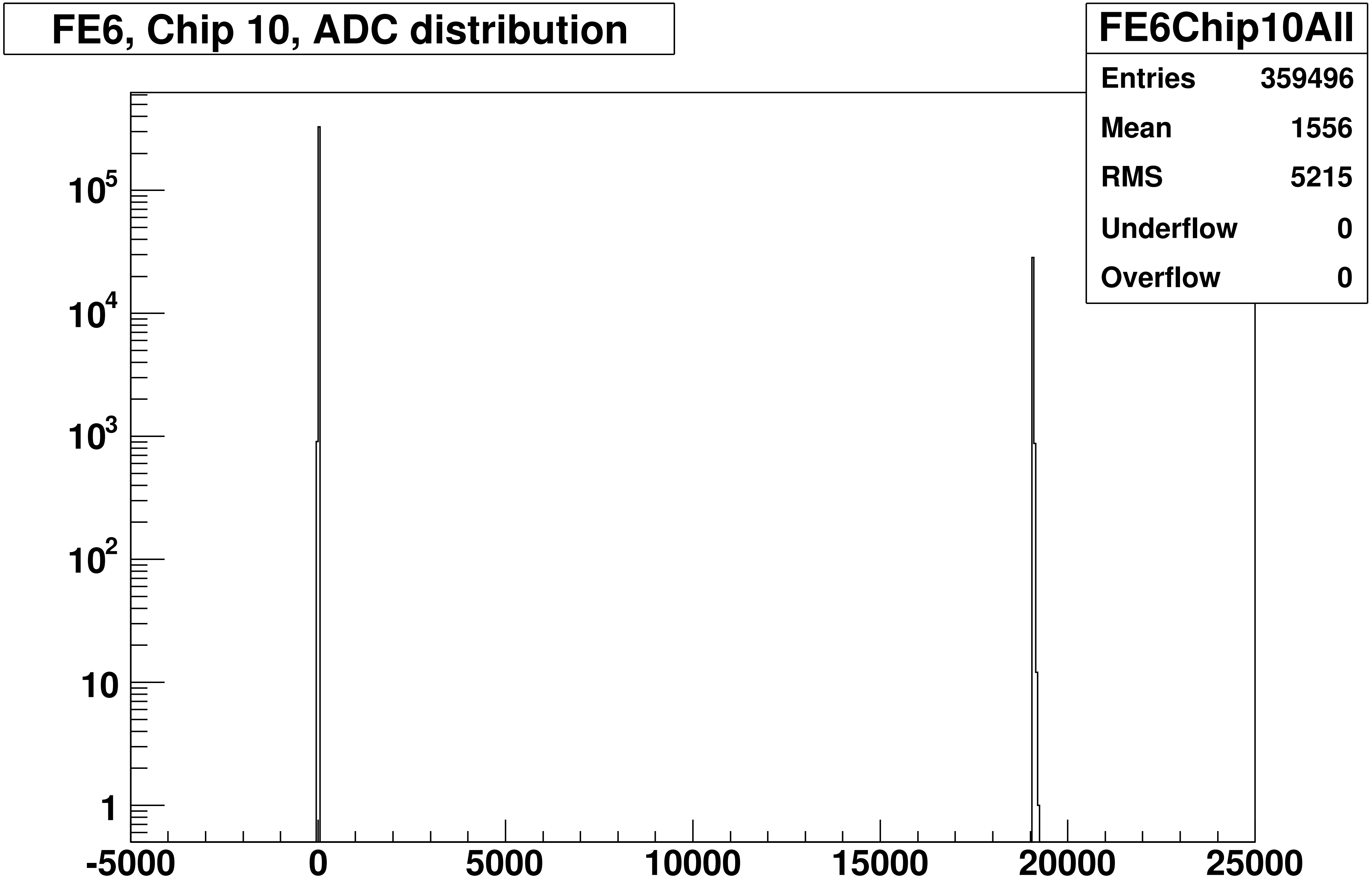
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE6, Chip 10, ADC distribution
FE6Chip10All
Entries 359496
Mean 1556
RMS 5215
Underflow 0
Overflow 0
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10^4
10^3
10^2
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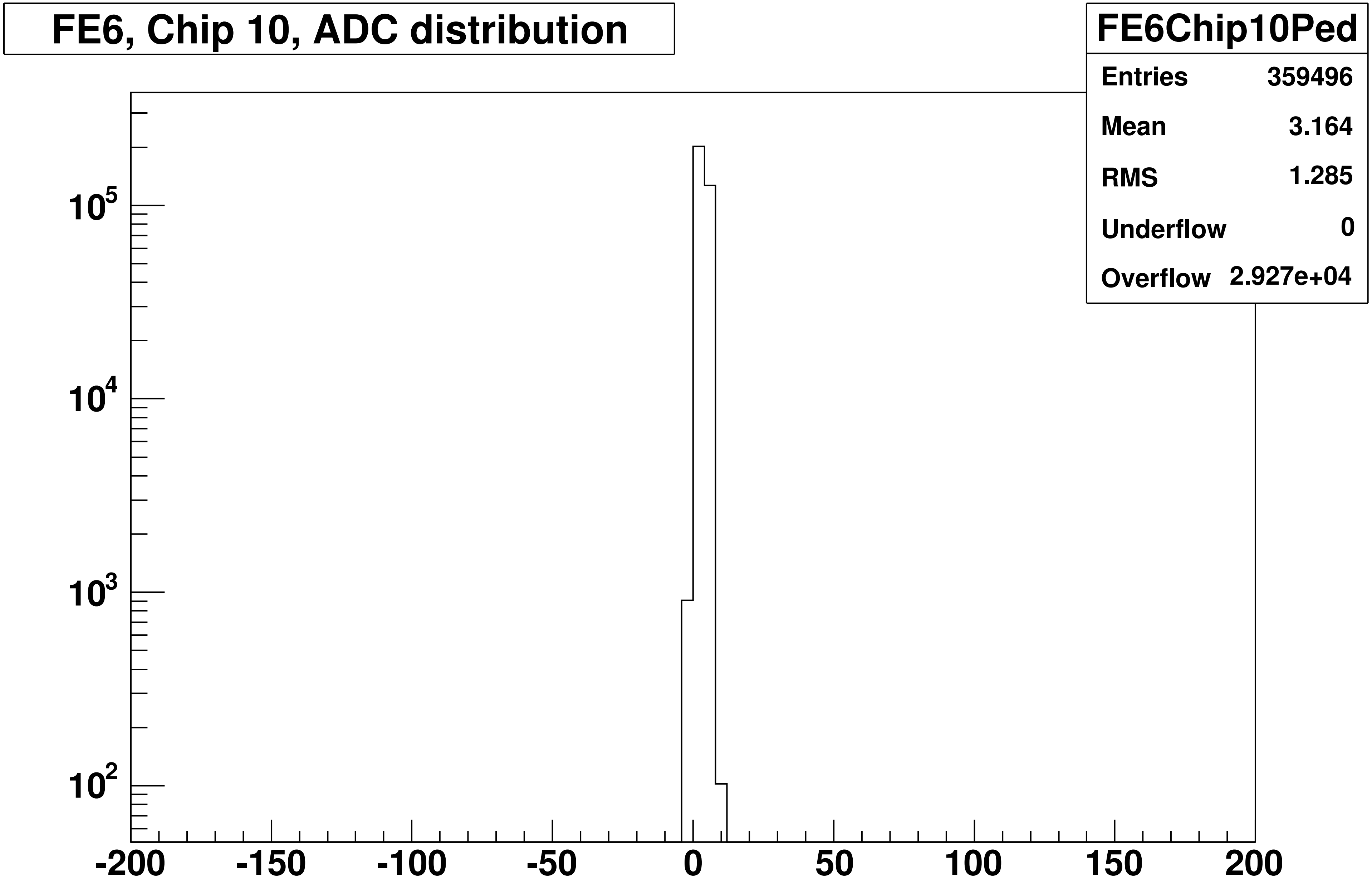
10000
15000
20000
25000


FE6, Chip 10, ADC distribution
FE6Chip10Ped
Entries 359496
Mean 3.164
RMS 1.285
Underflow 0
Overflow 2.927e+04
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10^4
10^3
10^2
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-100
-50
0
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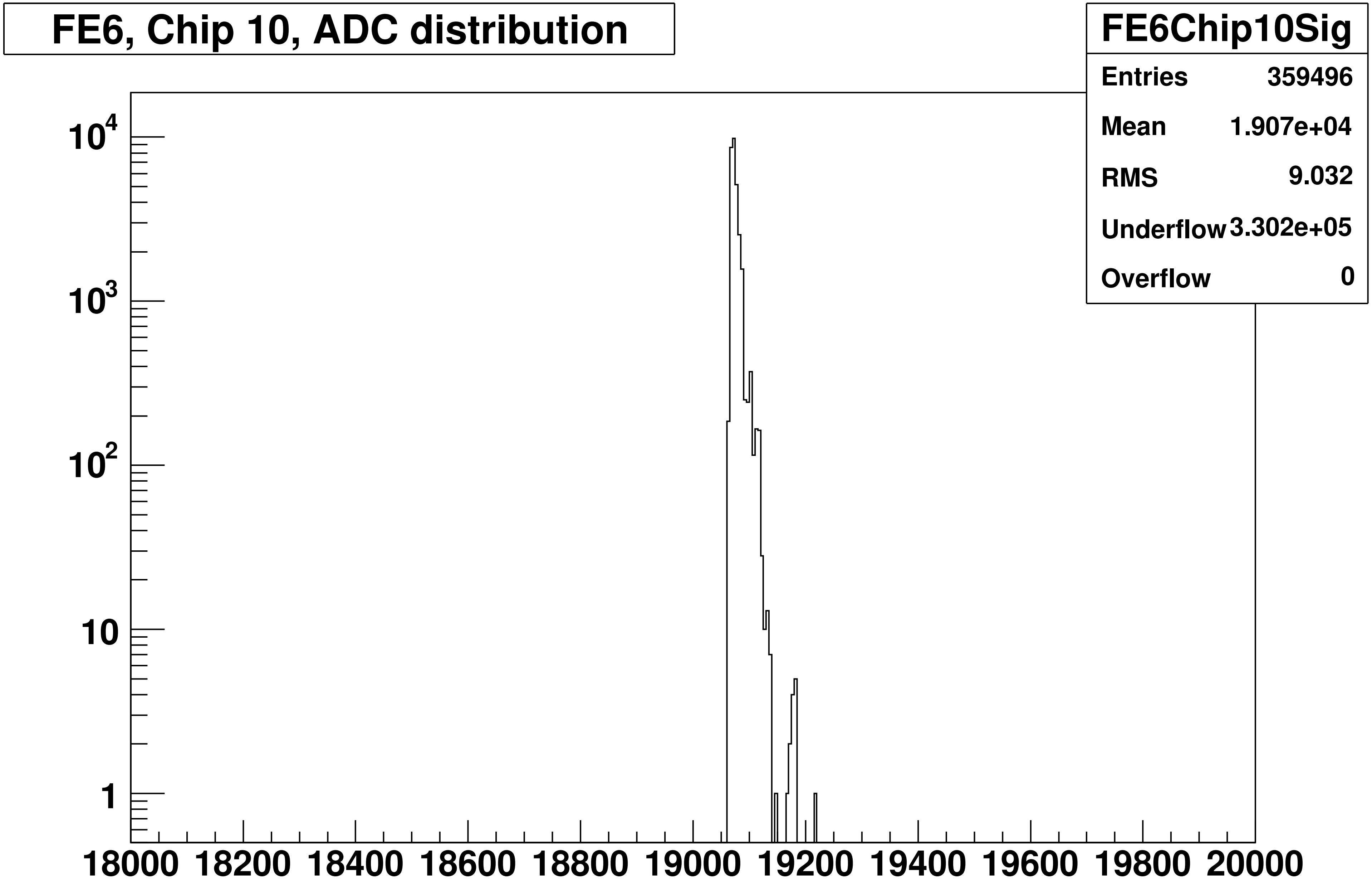
100
150
200



FE6, Chip 10, ADC distribution
FE6Chip10Sig
Entries 359496
Mean 1.907e+04
RMS 9.032
Underflow 3.302e+05
Overflow 0
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10^3
10^2
10
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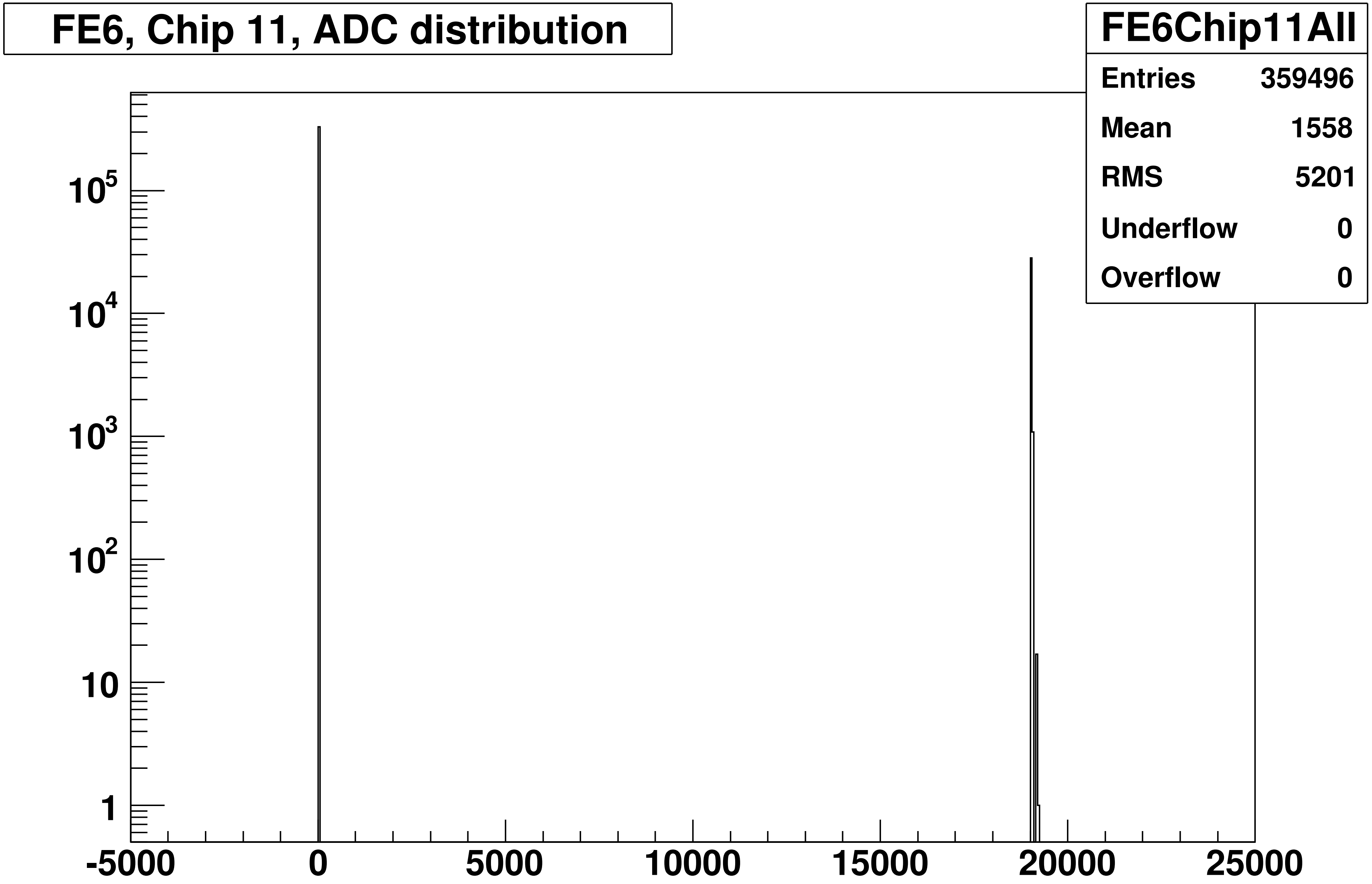
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE6, Chip 11, ADC distribution
FE6Chip11All
Entries 359496
Mean 1558
RMS 5201
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
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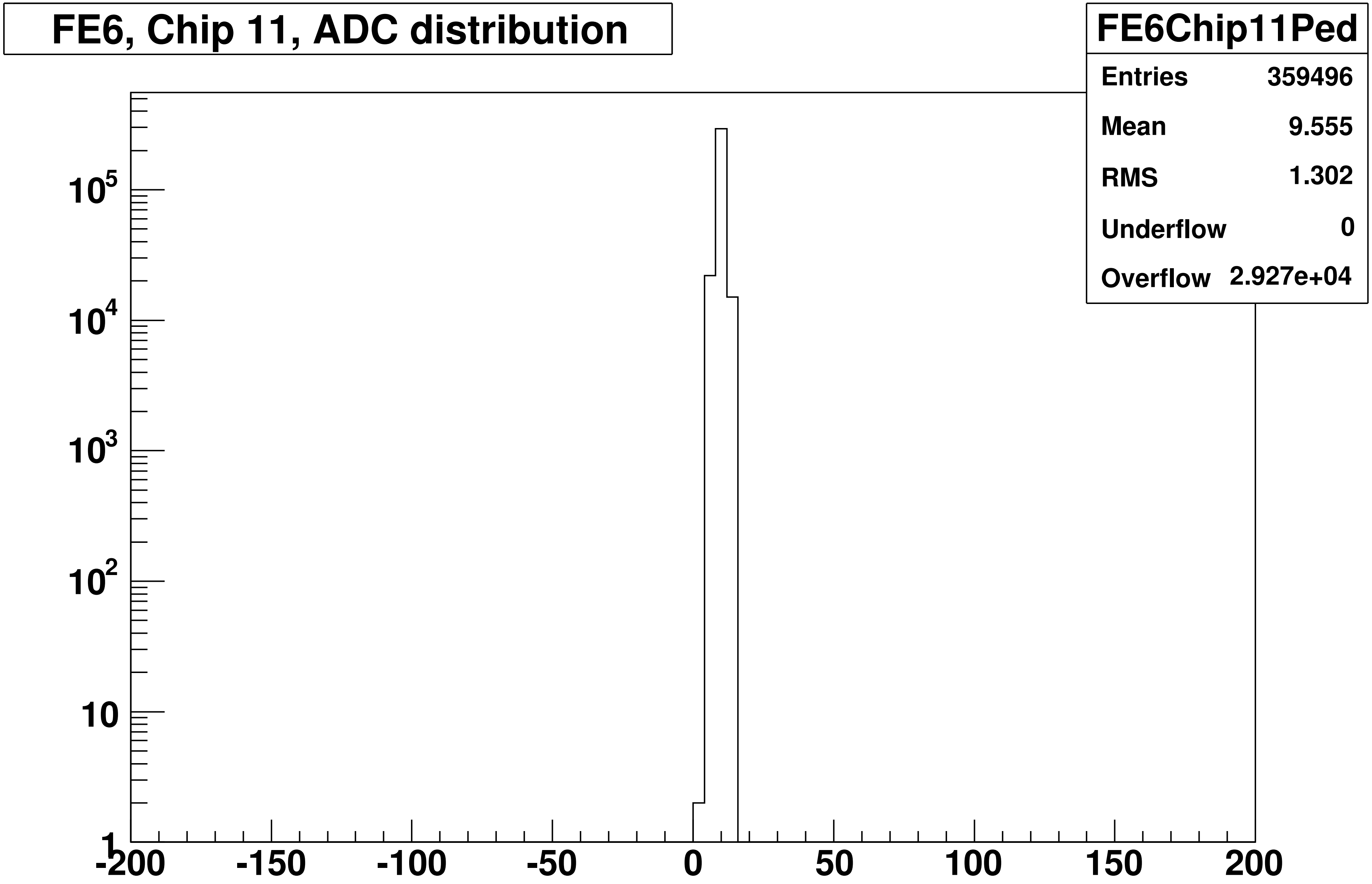
10000
15000
20000
25000


FE6, Chip 11, ADC distribution
FE6Chip11Ped
Entries 359496
Mean 9.555
RMS 1.302
Underflow 0
Overflow 2.927e+04
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10^4
10^3
10^2
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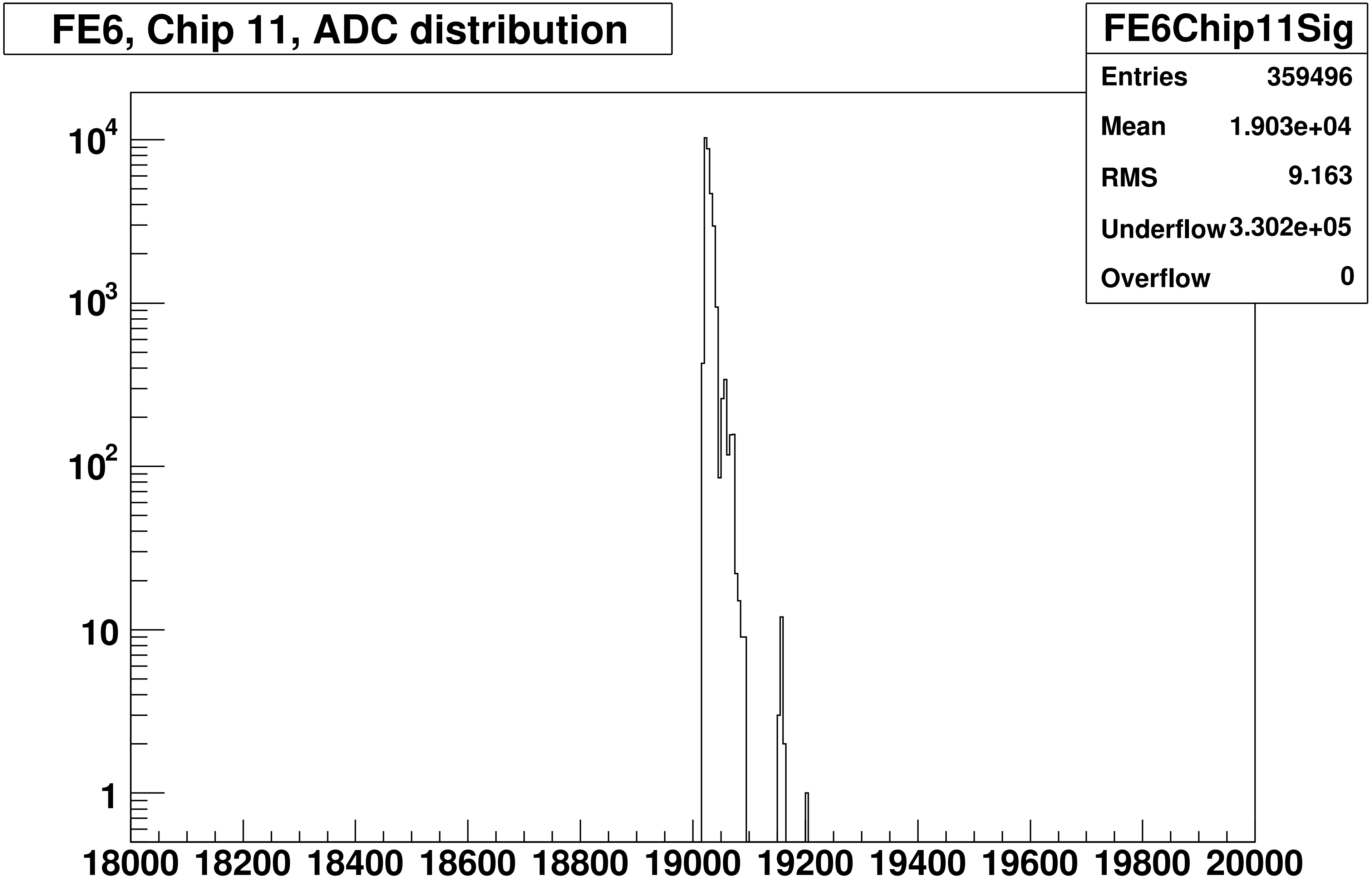
50
100
150
200


FE6, Chip 11, ADC distribution
FE6Chip11Sig
Entries 359496
Mean 1.903e+04
RMS 9.163
Underflow 3.302e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
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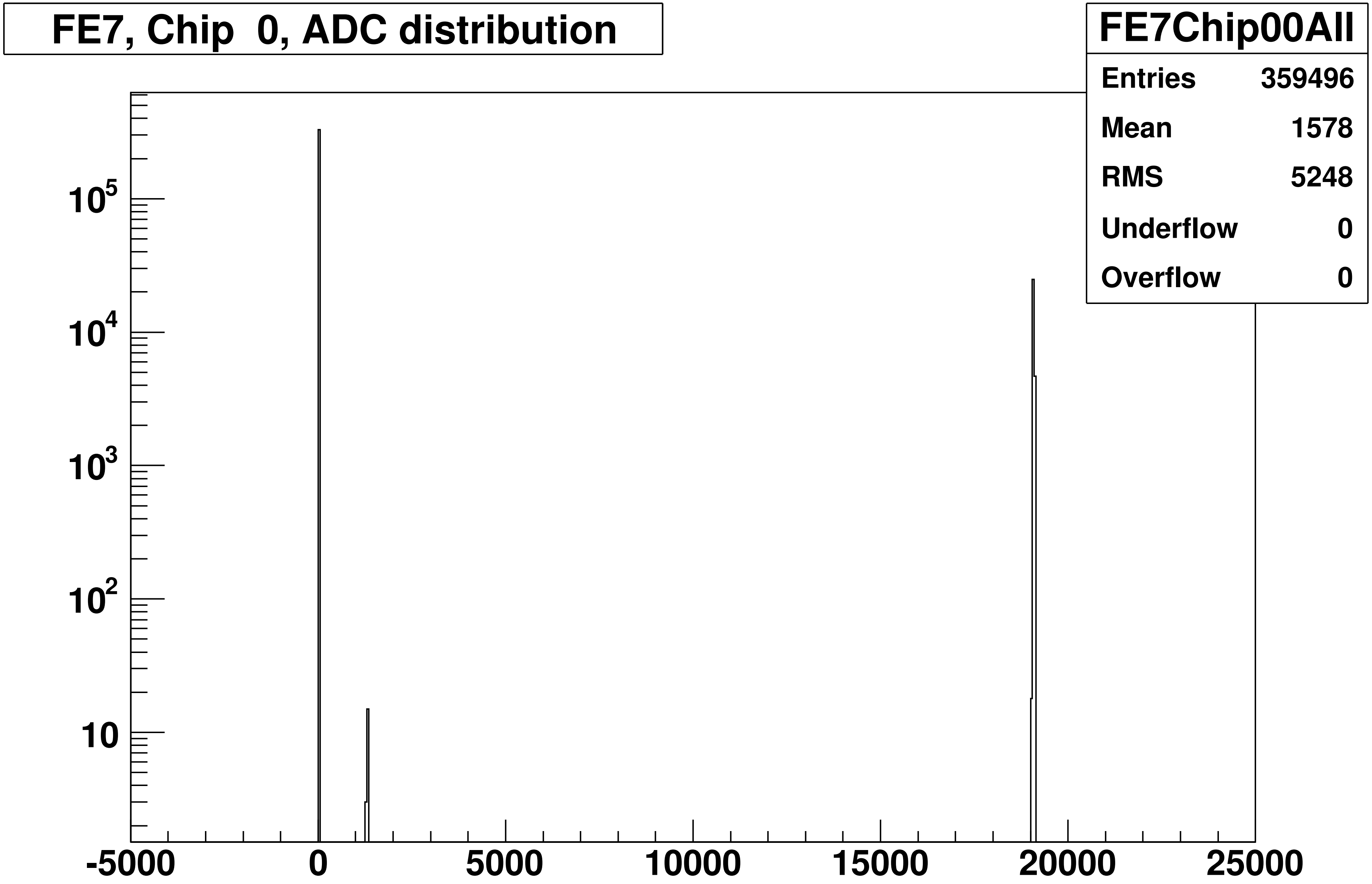
19600
19800
20000



FE7, Chip 0, ADC distribution
FE7Chip00All
Entries 359496
Mean 1578
RMS 5248
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
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-5000
0
5000
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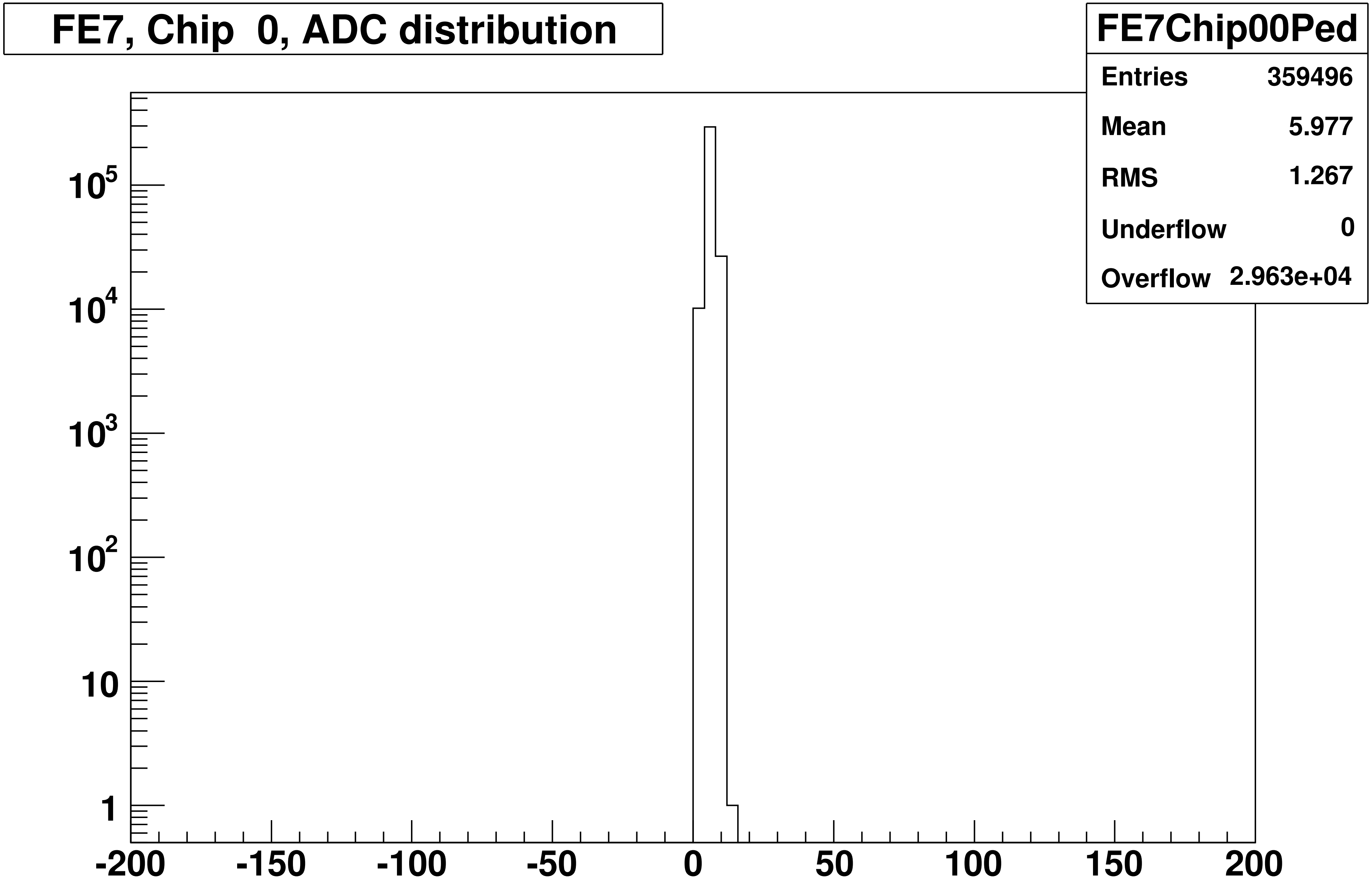
15000
20000
25000


FE7, Chip 0, ADC distribution
FE7Chip00Ped
Entries 359496
Mean 5.977
RMS 1.267
Underflow 0
Overflow 2.963e+04
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10^4
10^3
10^2
10
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150
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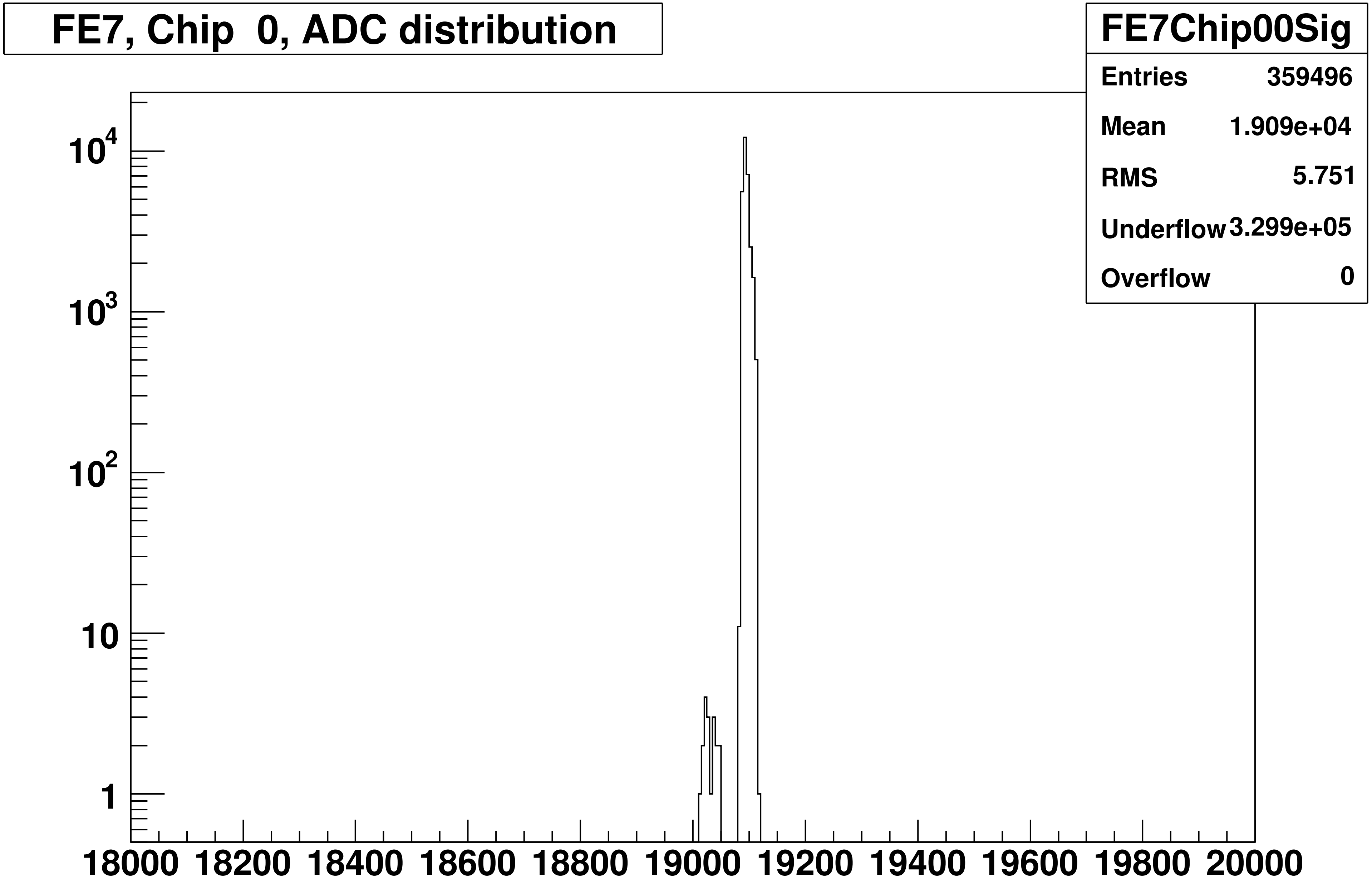
FE7, Chip 0, ADC distribution
FE7Chip00Sig
Entries 359496
Mean 1.909e+04
RMS 5.751
Underflow 3.299e+05
Overflow 0
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10^3
10^2
10
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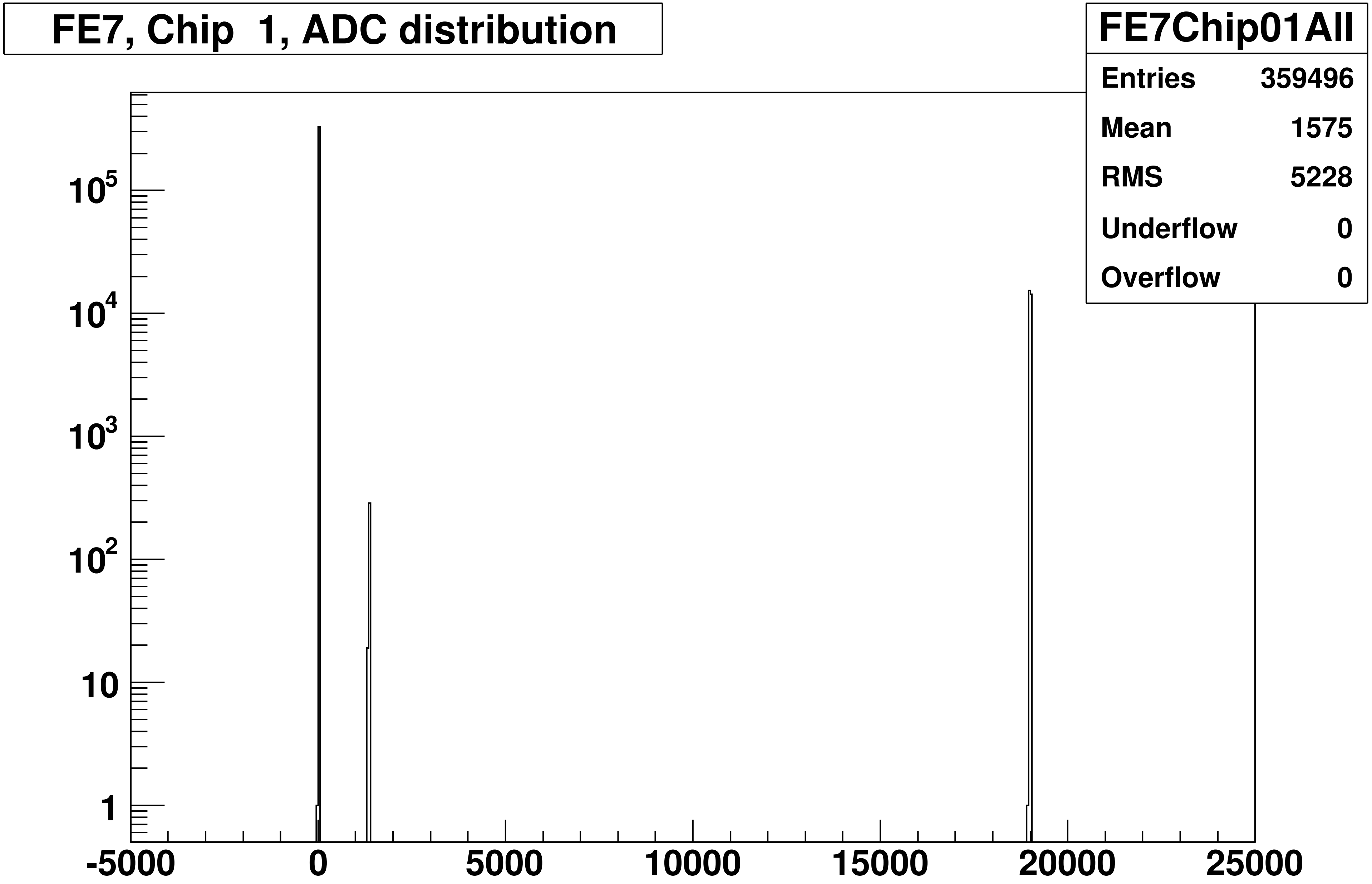
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE7, Chip 1, ADC distribution
FE7Chip01All
Entries 359496
Mean 1575
RMS 5228
Underflow 0
Overflow 0
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10^4
10^3
10^2
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-5000
0
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10000
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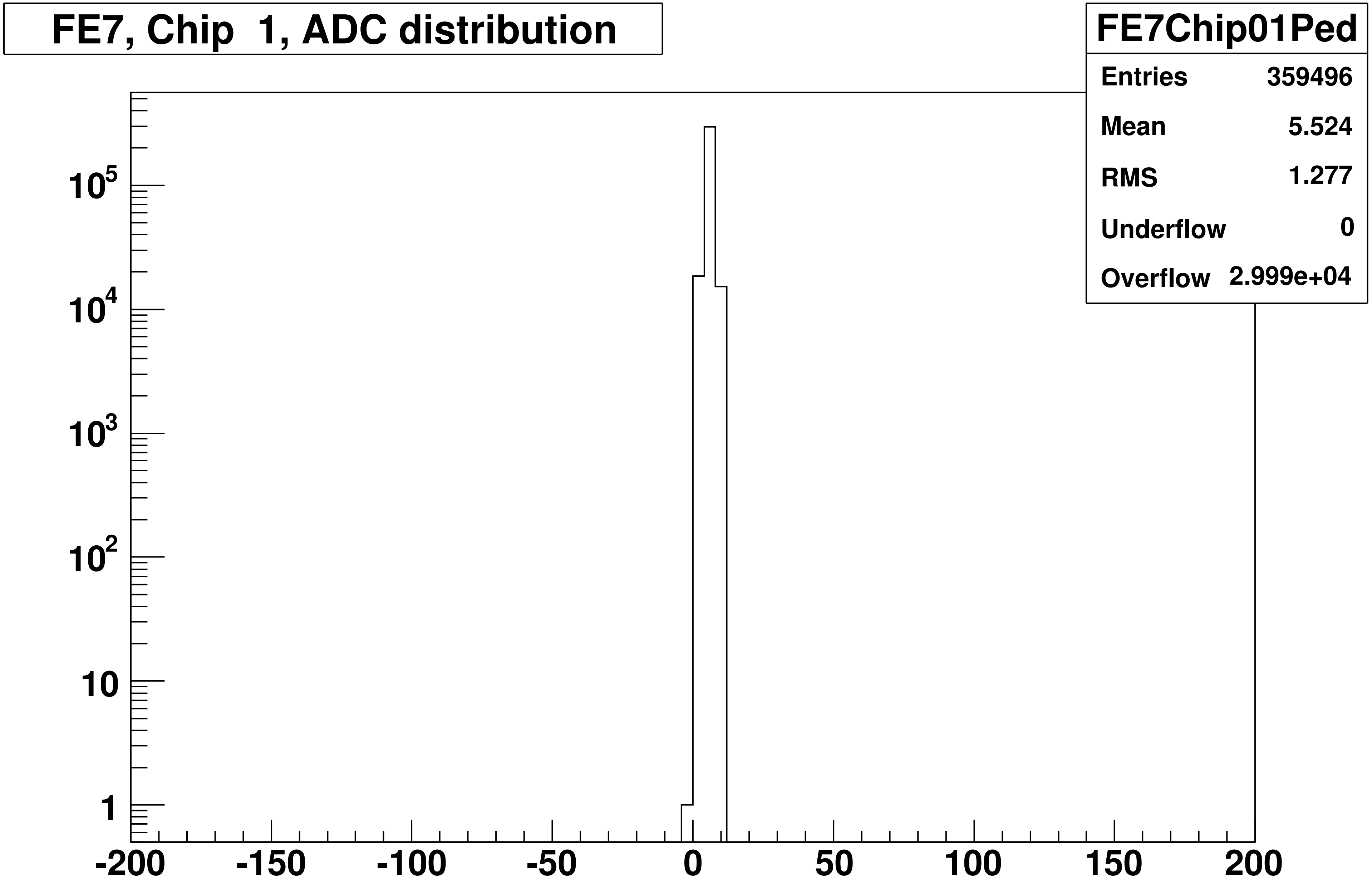
20000
25000


FE7, Chip 1, ADC distribution
FE7Chip01Ped
Entries 359496
Mean 5.524
RMS 1.277
Underflow 0
Overflow 2.999e+04
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10^4
10^3
10^2
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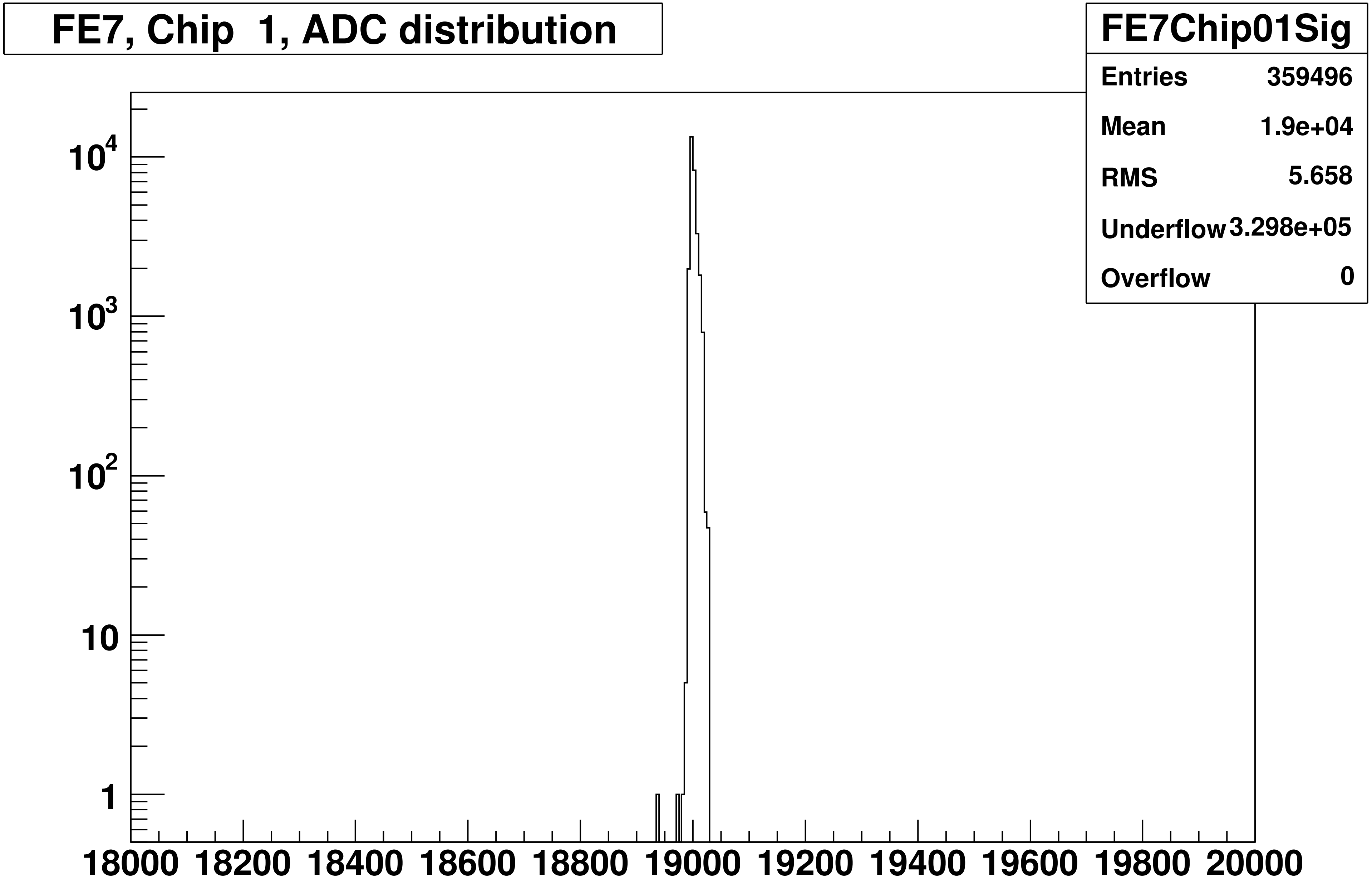
150
200


FE7, Chip 1, ADC distribution
FE7Chip01Sig
Entries 359496
Mean 1.9e+04
RMS 5.658
Underflow 3.298e+05
Overflow 0
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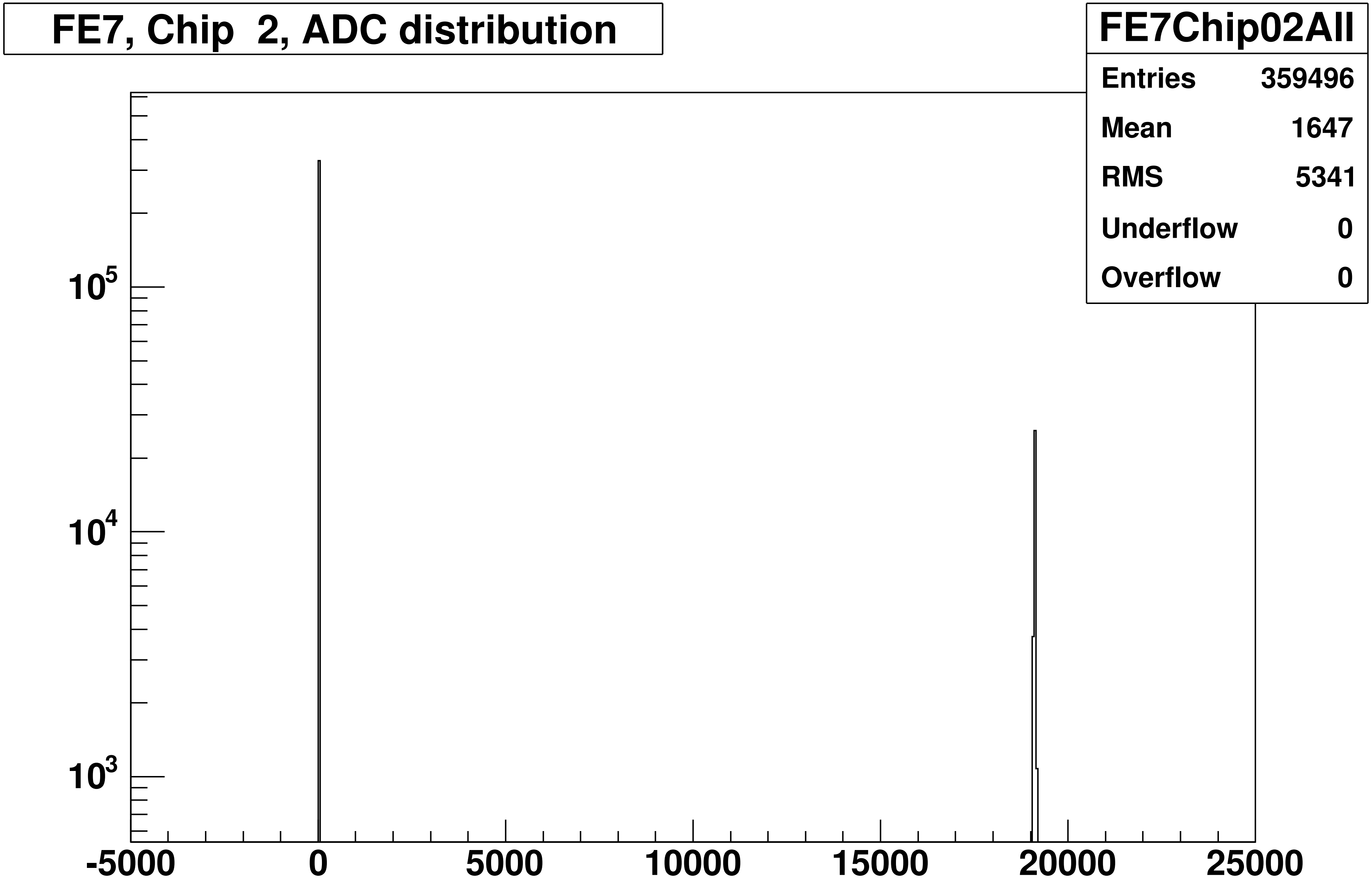
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE7, Chip 2, ADC distribution
FE7Chip02All
Entries 359496
Mean 1647
RMS 5341
Underflow 0
Overflow 0
10^5
10^4
10^3
-5000
0
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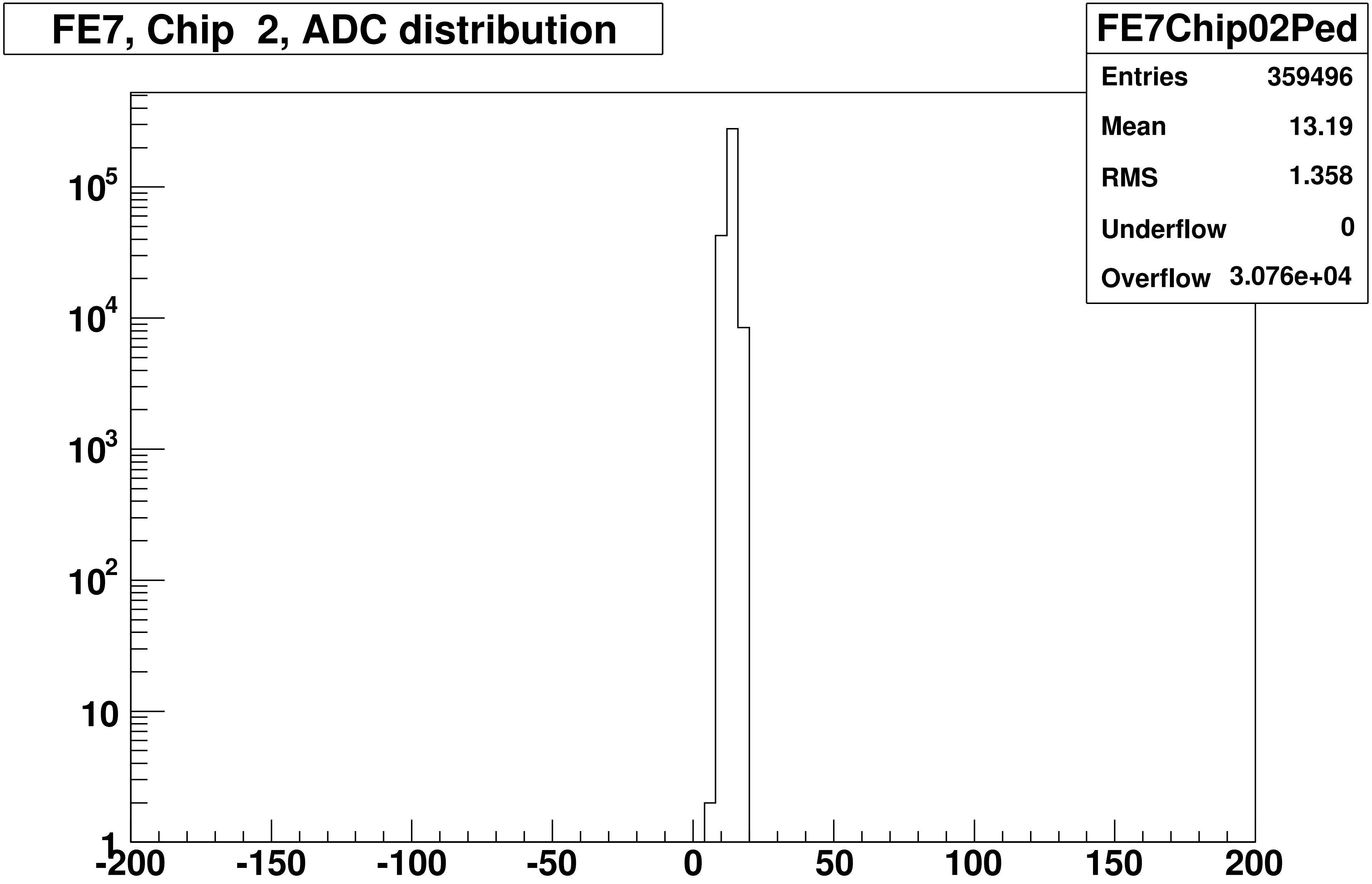
10000
15000
20000
25000


FE7, Chip 2, ADC distribution
FE7Chip02Ped
Entries 359496
Mean 13.19
RMS 1.358
Underflow 0
Overflow 3.076e+04
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10^4
10^3
10^2
10
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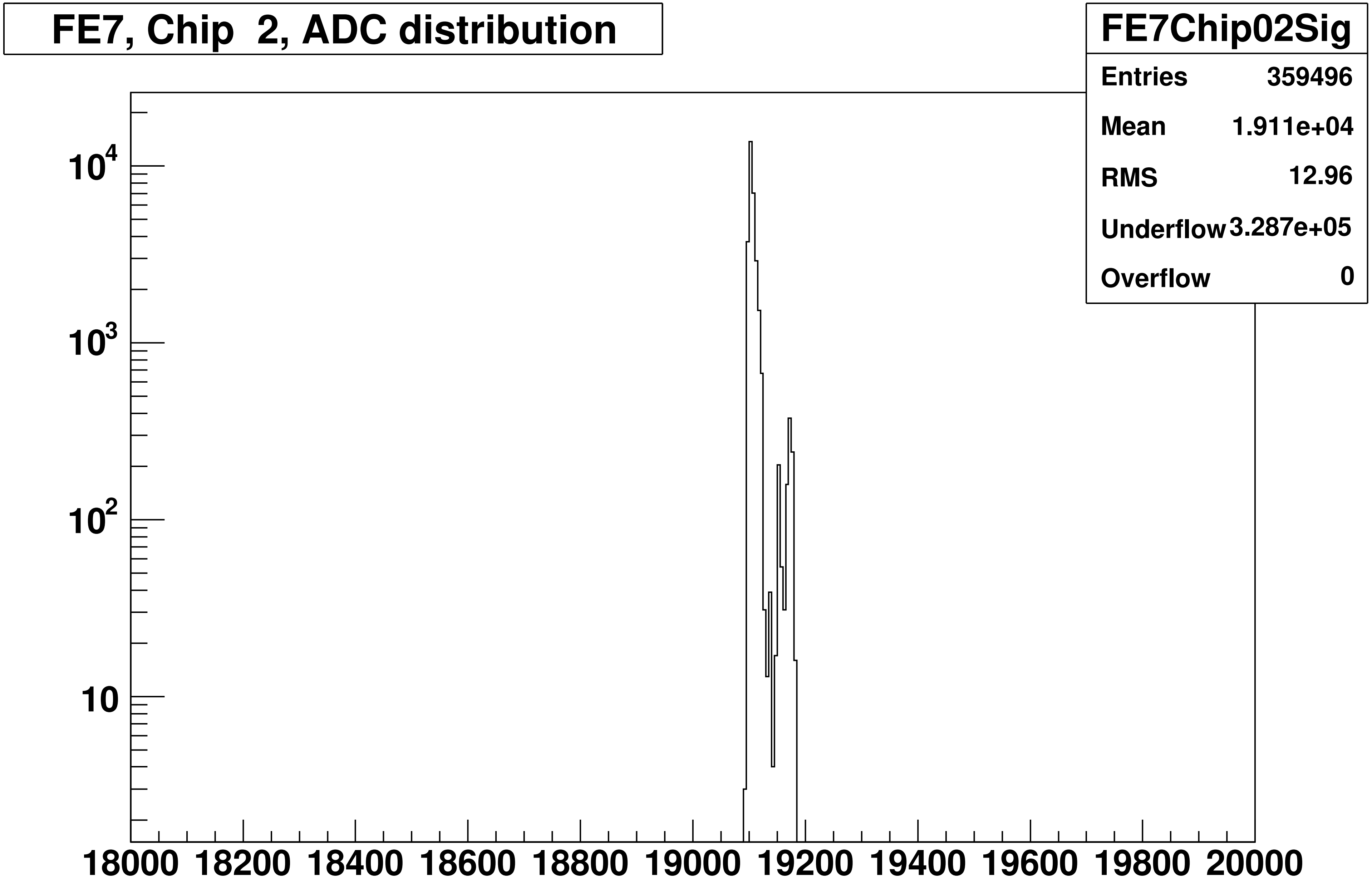
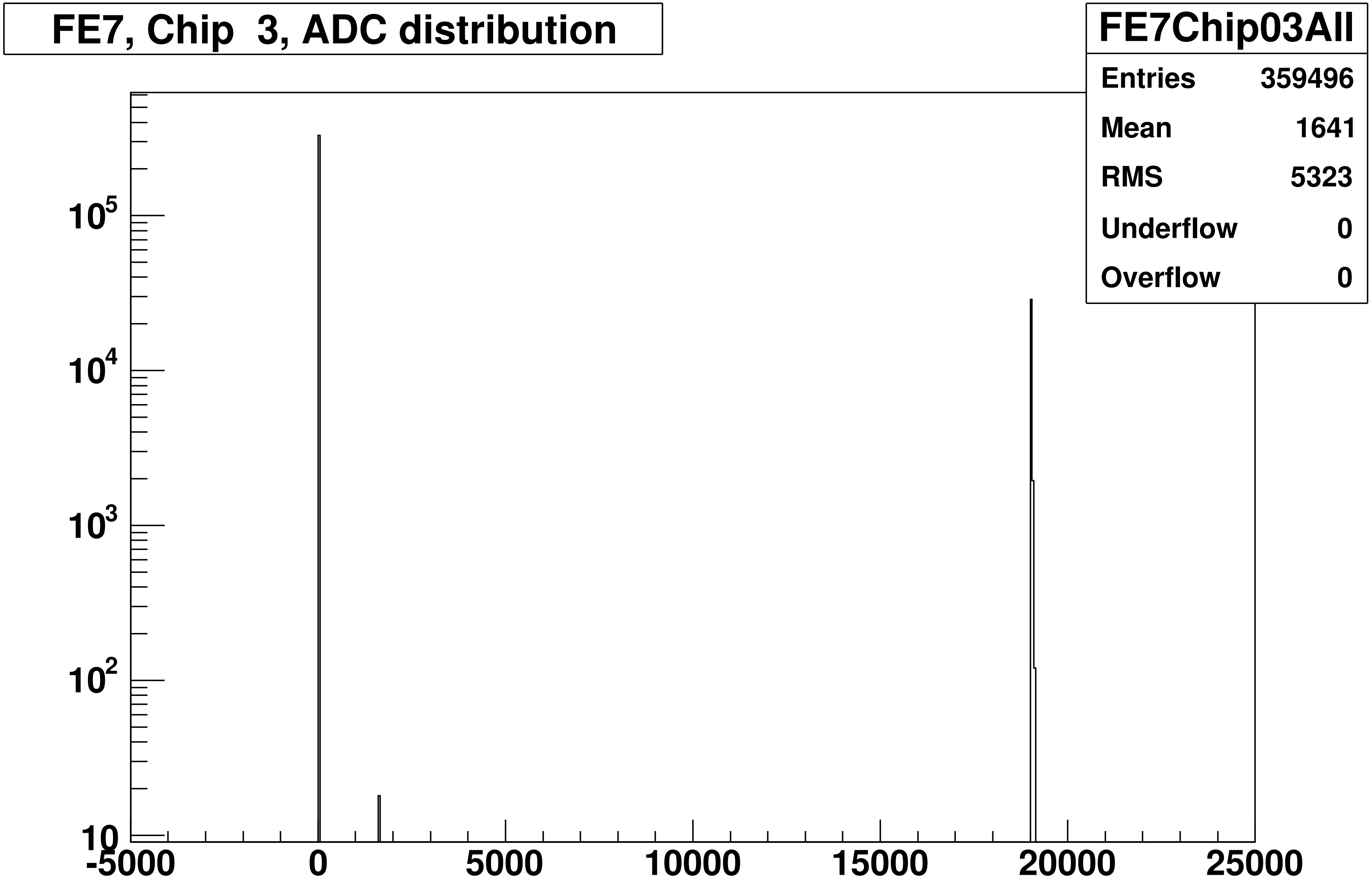

FE7, Chip 2, ADC distribution
FE7Chip02Sig
Entries 359496
Mean 1.911e+04
RMS 12.96
Underflow 3.287e+05
Overflow 0
10^4
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE7, Chip 3, ADC distribution
FE7Chip03All
Entries 359496
Mean 1641
RMS 5323
Underflow 0
Overflow 0
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10^4
10^3
10^2
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0
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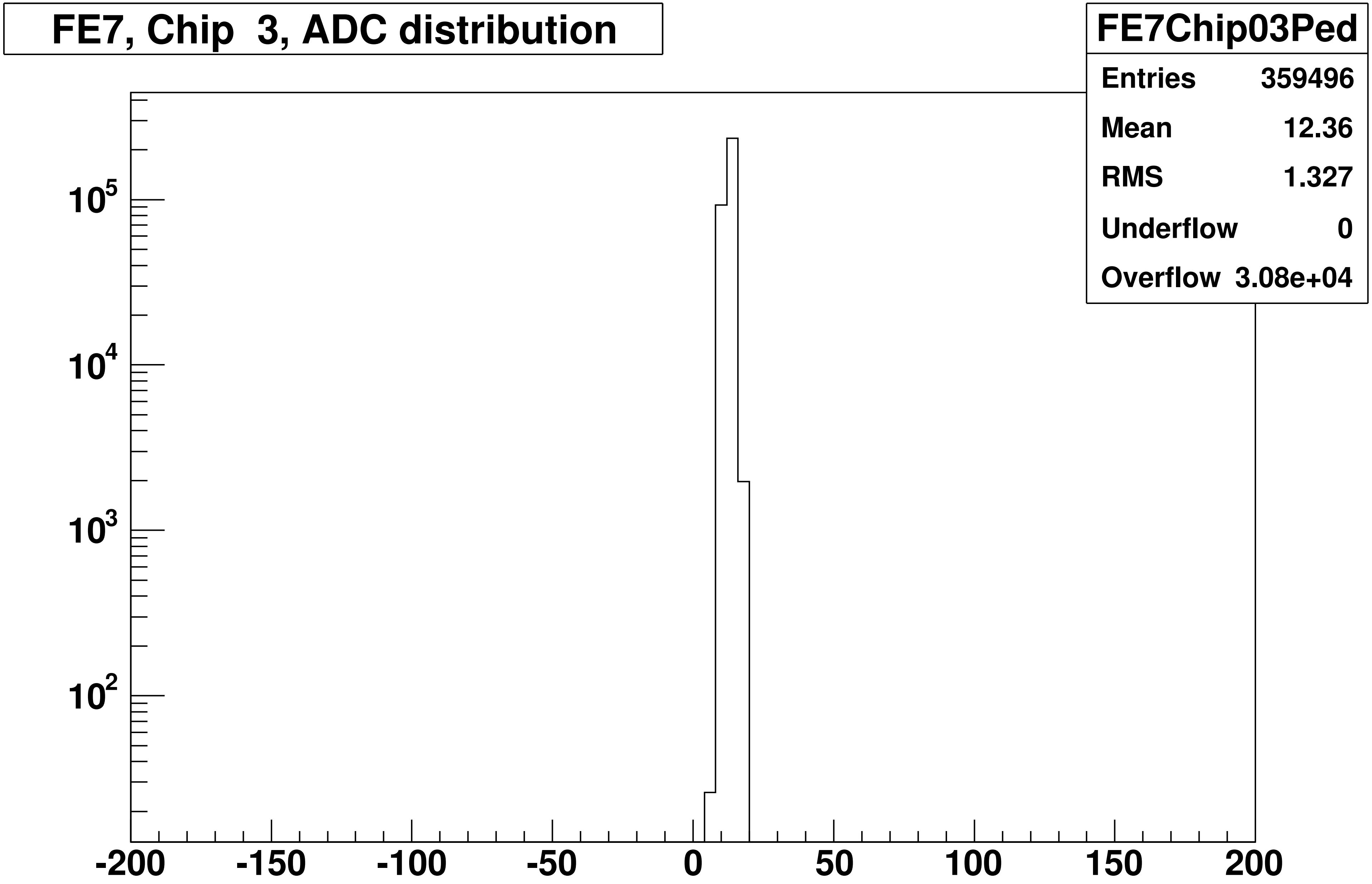
20000
25000



FE7, Chip 3, ADC distribution
FE7Chip03Ped
Entries 359496
Mean 12.36
RMS 1.327
Underflow 0
Overflow 3.08e+04
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10^4
10^3
10^2
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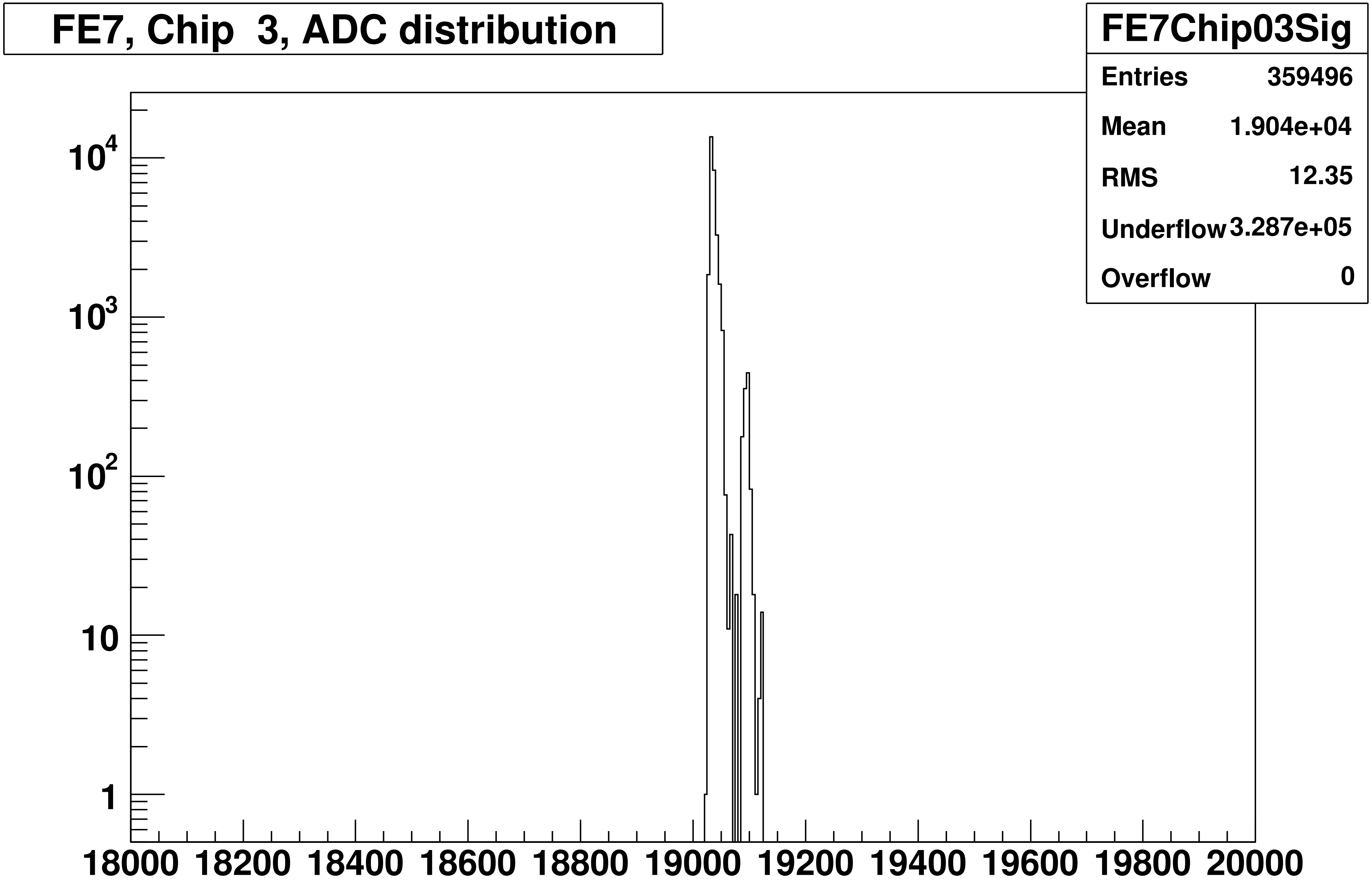
100
150
200


FE7, Chip 3, ADC distribution
FE7Chip03Sig
Entries 359496
Mean 1.904e+04
RMS 12.35
Underflow 3.287e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
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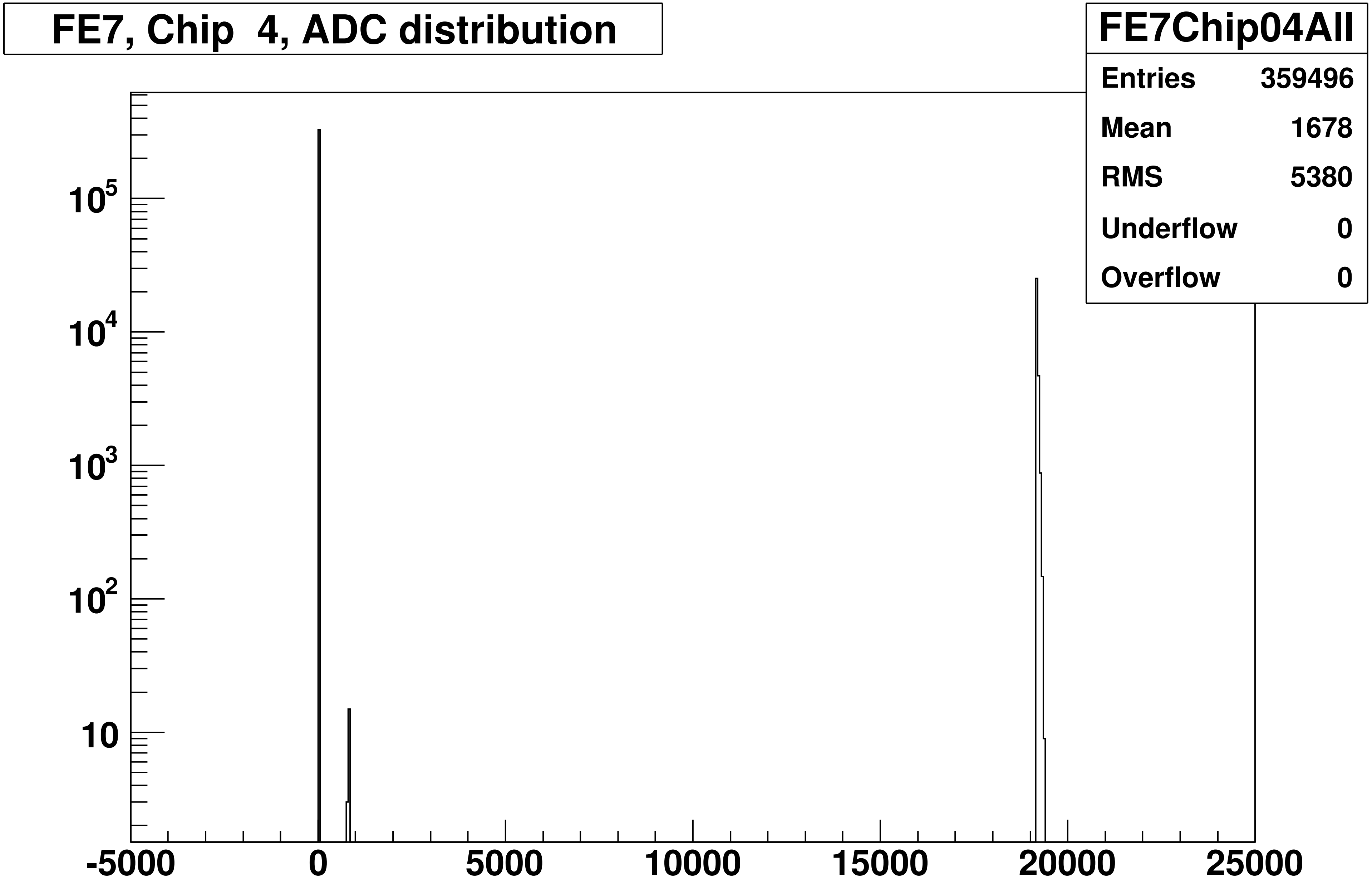
20000


FE7, Chip 4, ADC distribution
FE7Chip04All
Entries 359496
Mean 1678
RMS 5380
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
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-5000
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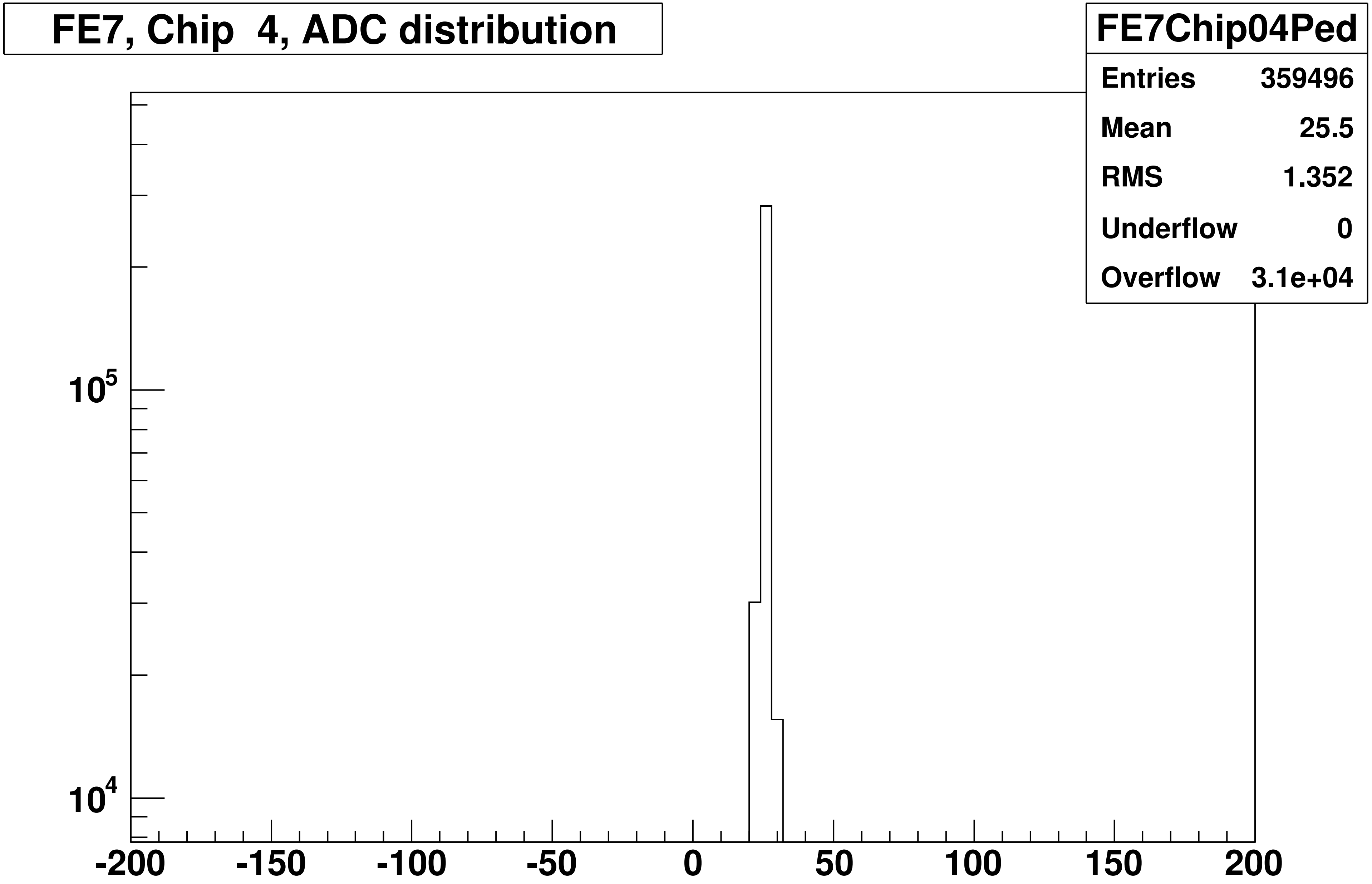
20000
25000


FE7, Chip 4, ADC distribution
FE7Chip04Ped
Entries 359496
Mean 25.5
RMS 1.352
Underflow 0
Overflow 3.1e+04
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10^4
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-100
-50
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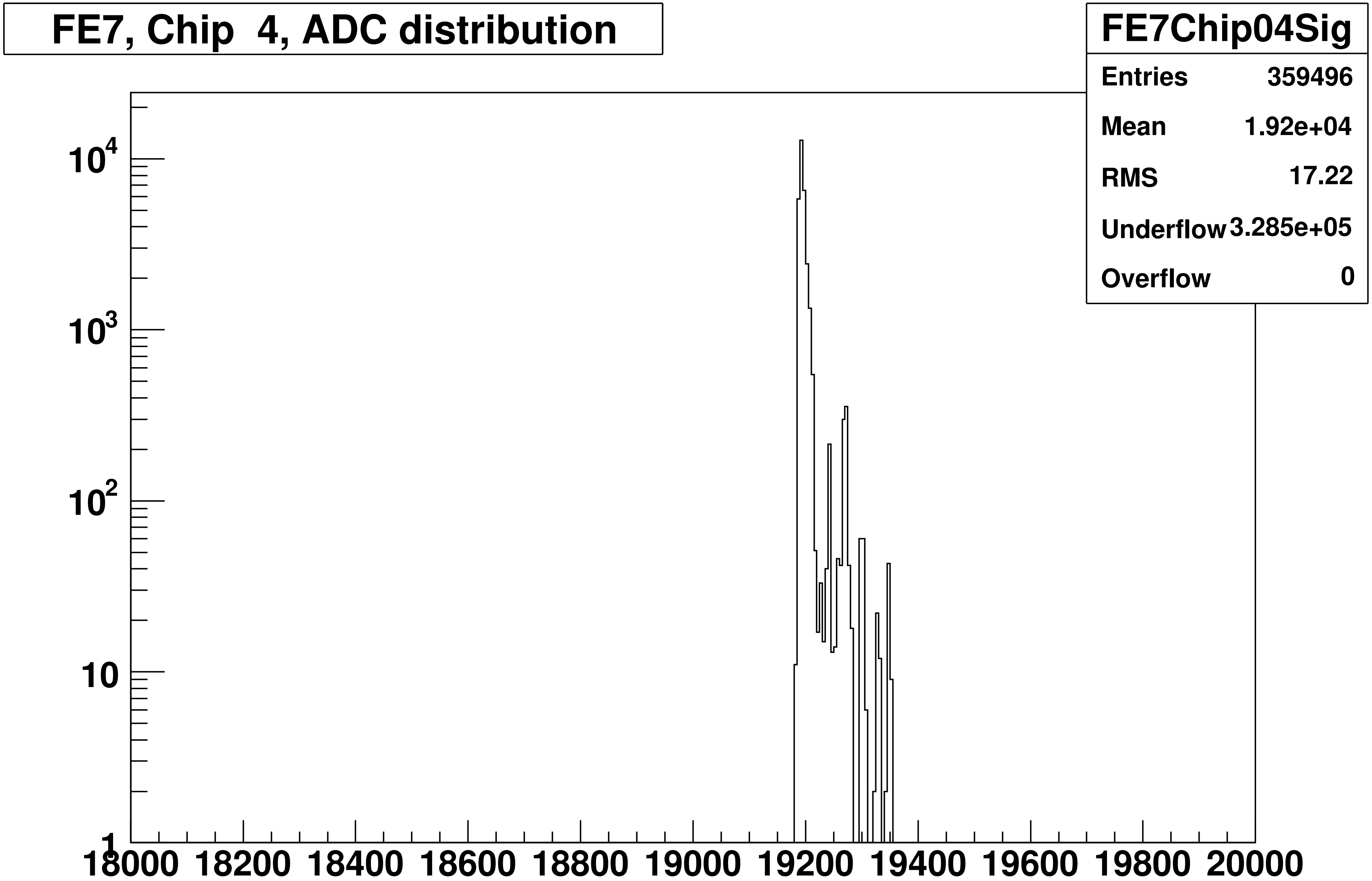
50
100
150
200



FE7, Chip 4, ADC distribution
FE7Chip04Sig
Entries 359496
Mean 1.92e+04
RMS 17.22
Underflow 3.285e+05
Overflow 0
10^4
10^3
10^2
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1
18000
18200
18400
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19000
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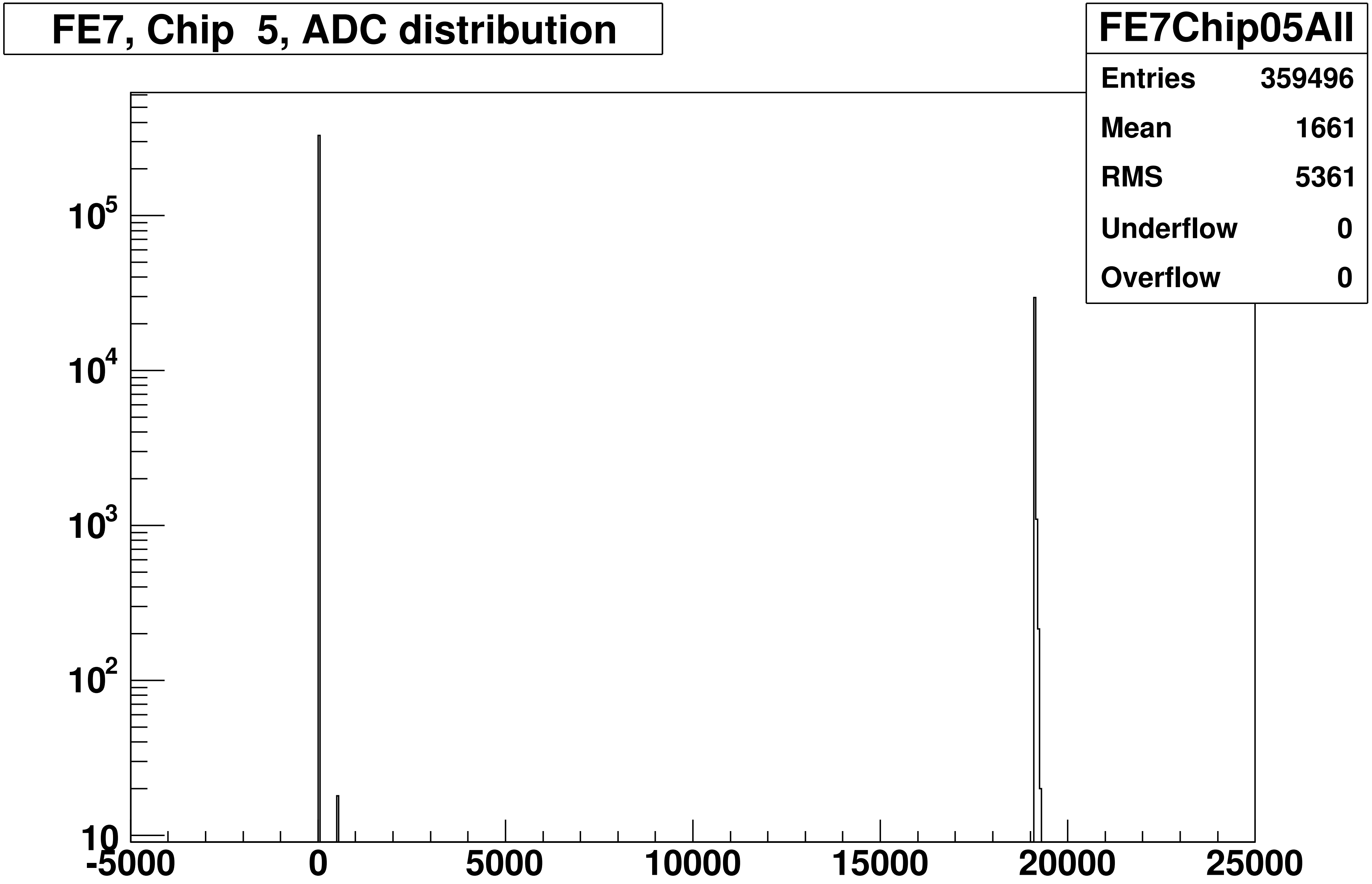
19600
19800
20000


FE7, Chip 5, ADC distribution
FE7Chip05All
Entries 359496
Mean 1661
RMS 5361
Underflow 0
Overflow 0
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10^2
10^3
10^4
10^5
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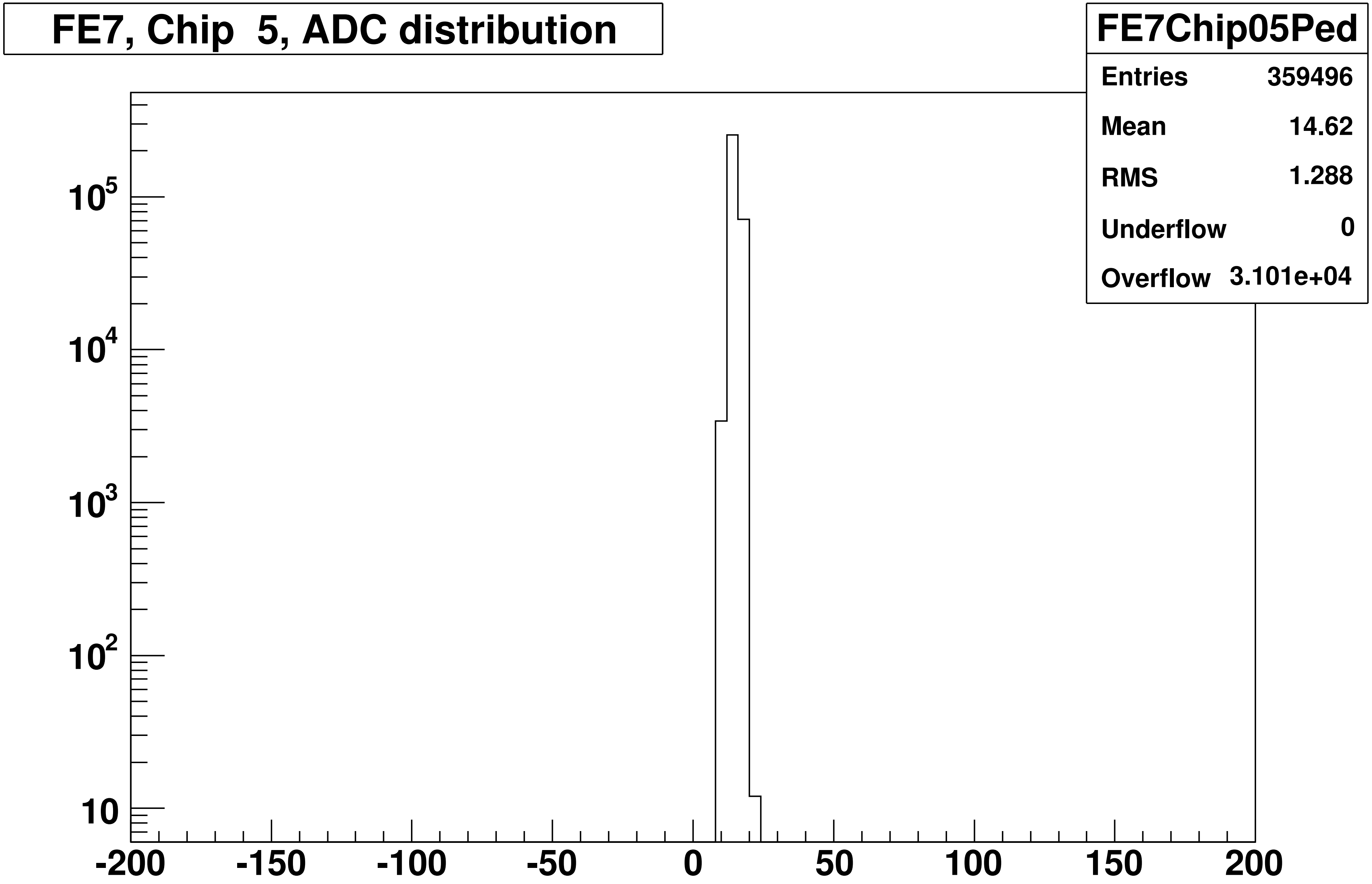
10000
15000
20000
25000


FE7, Chip 5, ADC distribution
FE7Chip05Ped
Entries 359496
Mean 14.62
RMS 1.288
Underflow 0
Overflow 3.101e+04
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10^4
10^3
10^2
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-200
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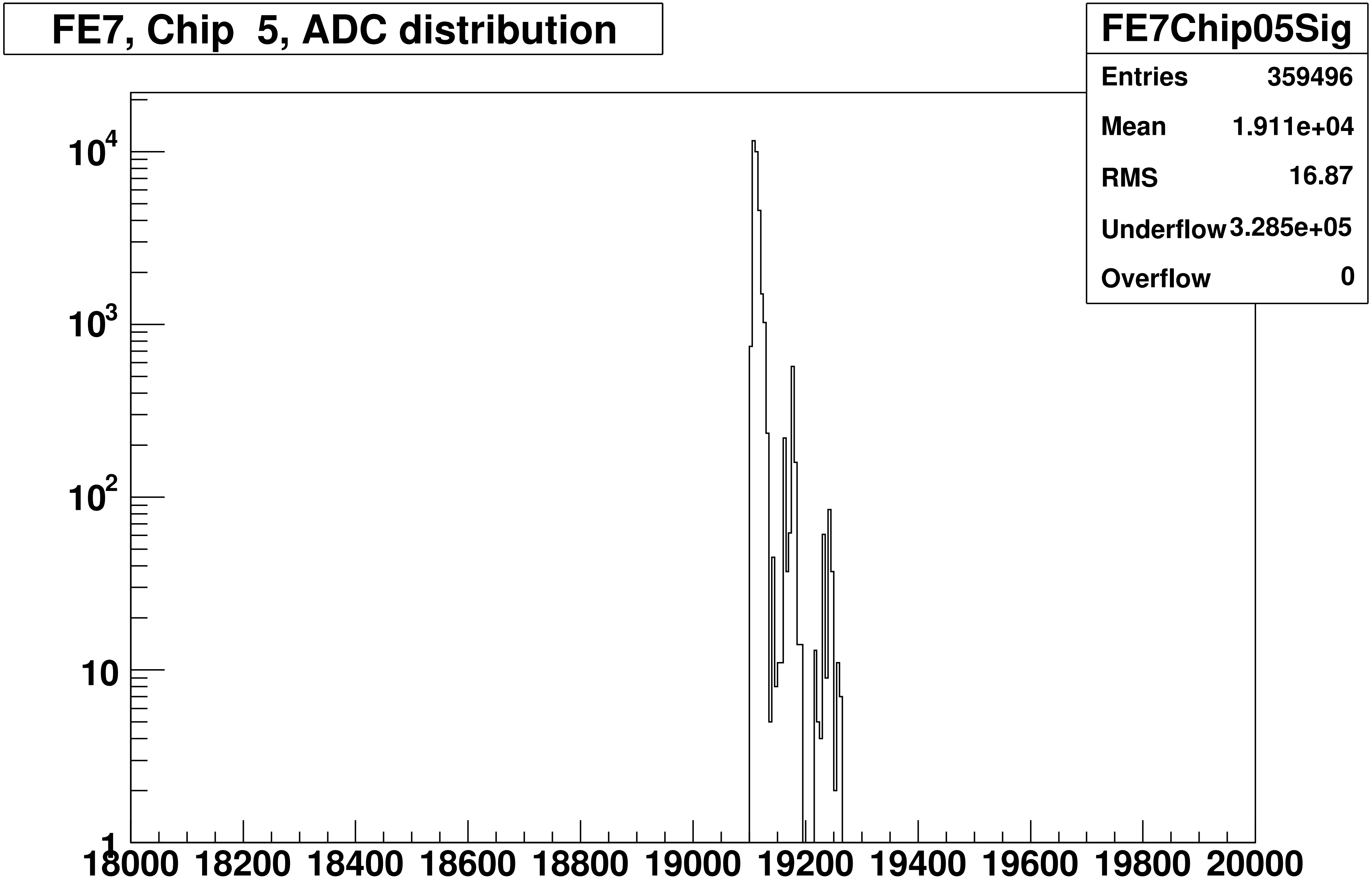
-100
-50
0
50
100
150
200


FE7, Chip 5, ADC distribution
FE7Chip05Sig
Entries 359496
Mean 1.911e+04
RMS 16.87
Underflow 3.285e+05
Overflow 0
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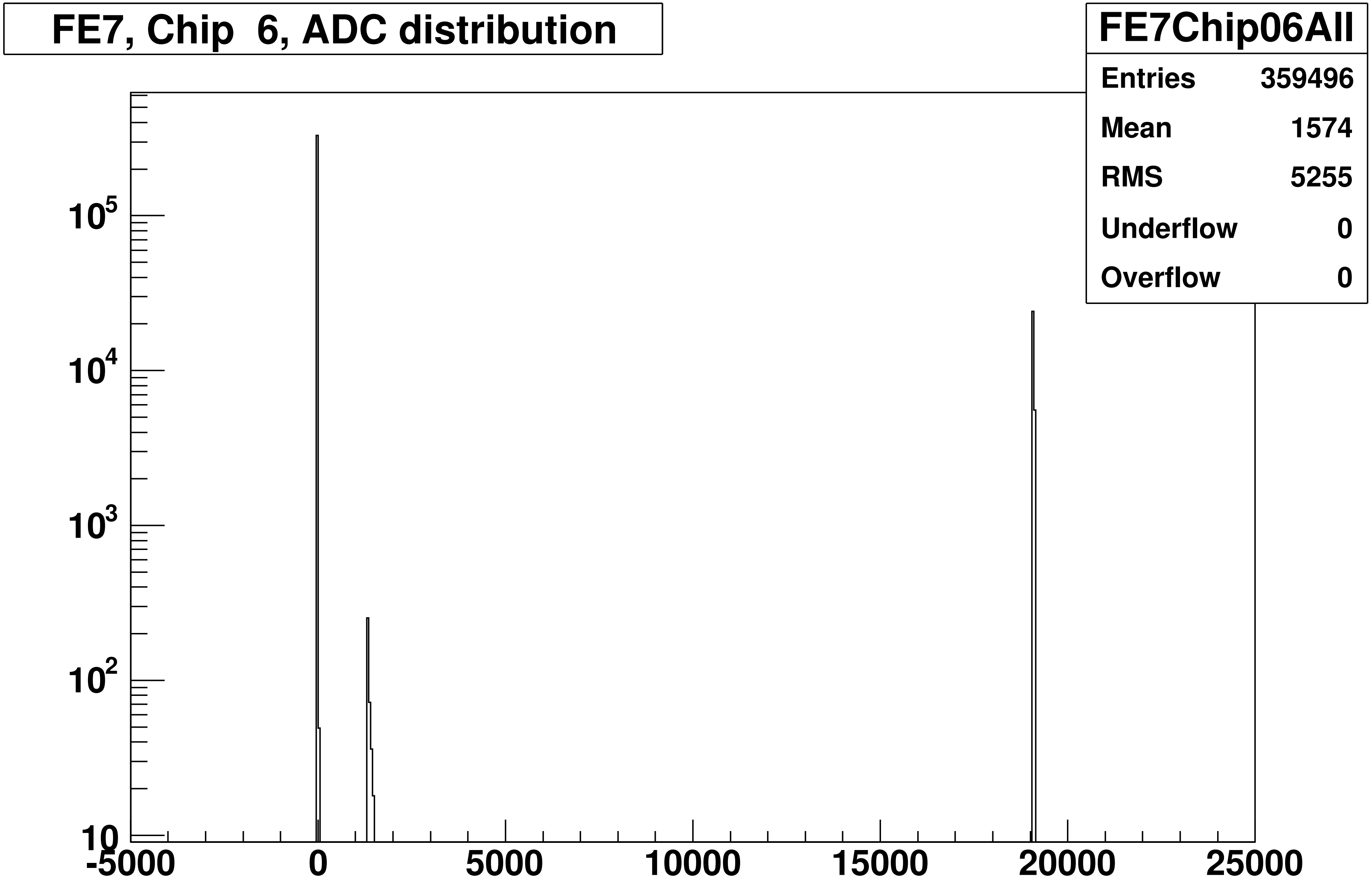
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE7, Chip 6, ADC distribution
FE7Chip06All
Entries 359496
Mean 1574
RMS 5255
Underflow 0
Overflow 0
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10^4
10^3
10^2
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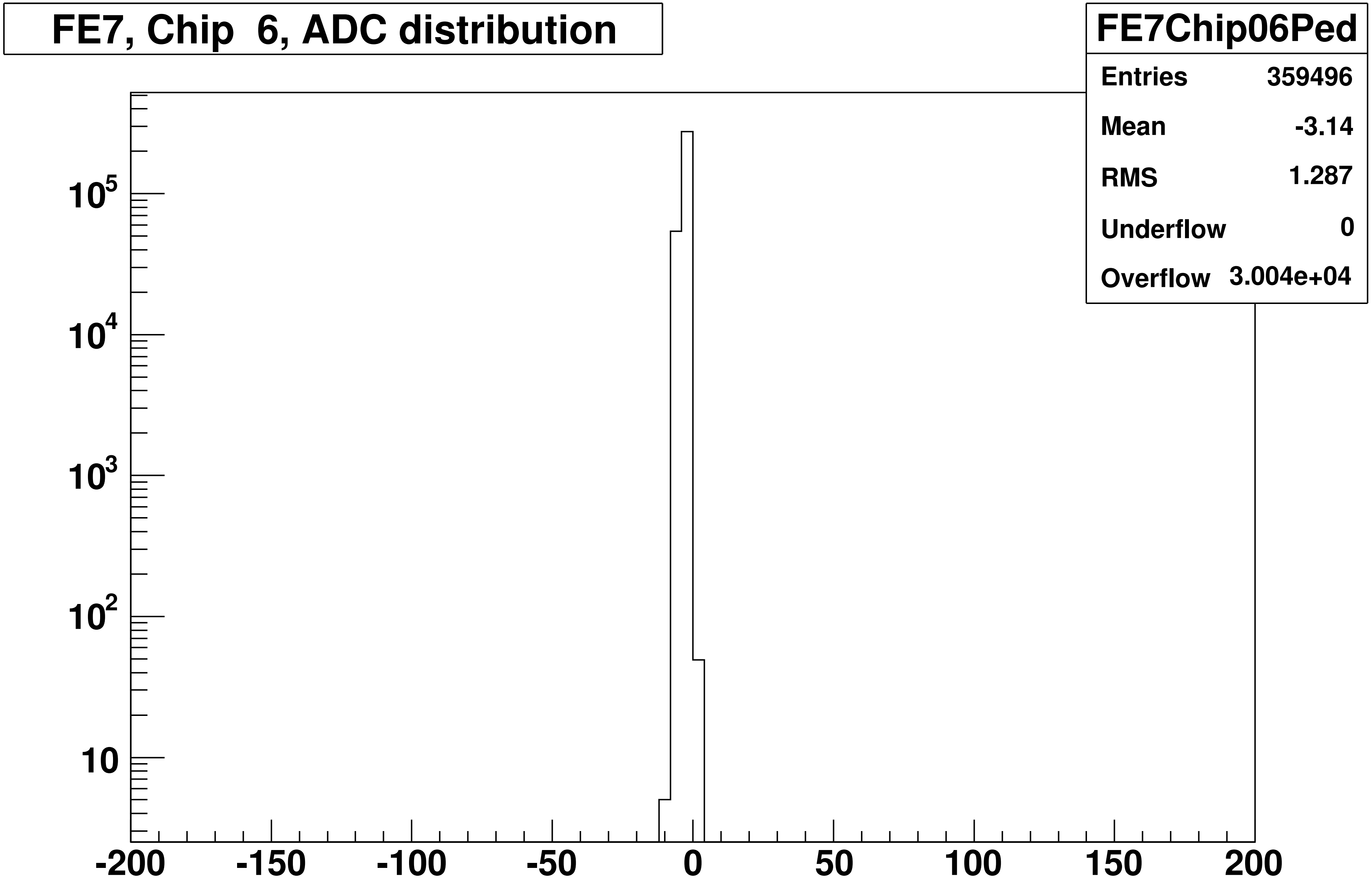
-5000
0
5000
10000
15000
20000
25000



FE7, Chip 6, ADC distribution
FE7Chip06Ped
Entries 359496
Mean -3.14
RMS 1.287
Underflow 0
Overflow 3.004e+04
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10^4
10^3
10^2
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-200
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-100
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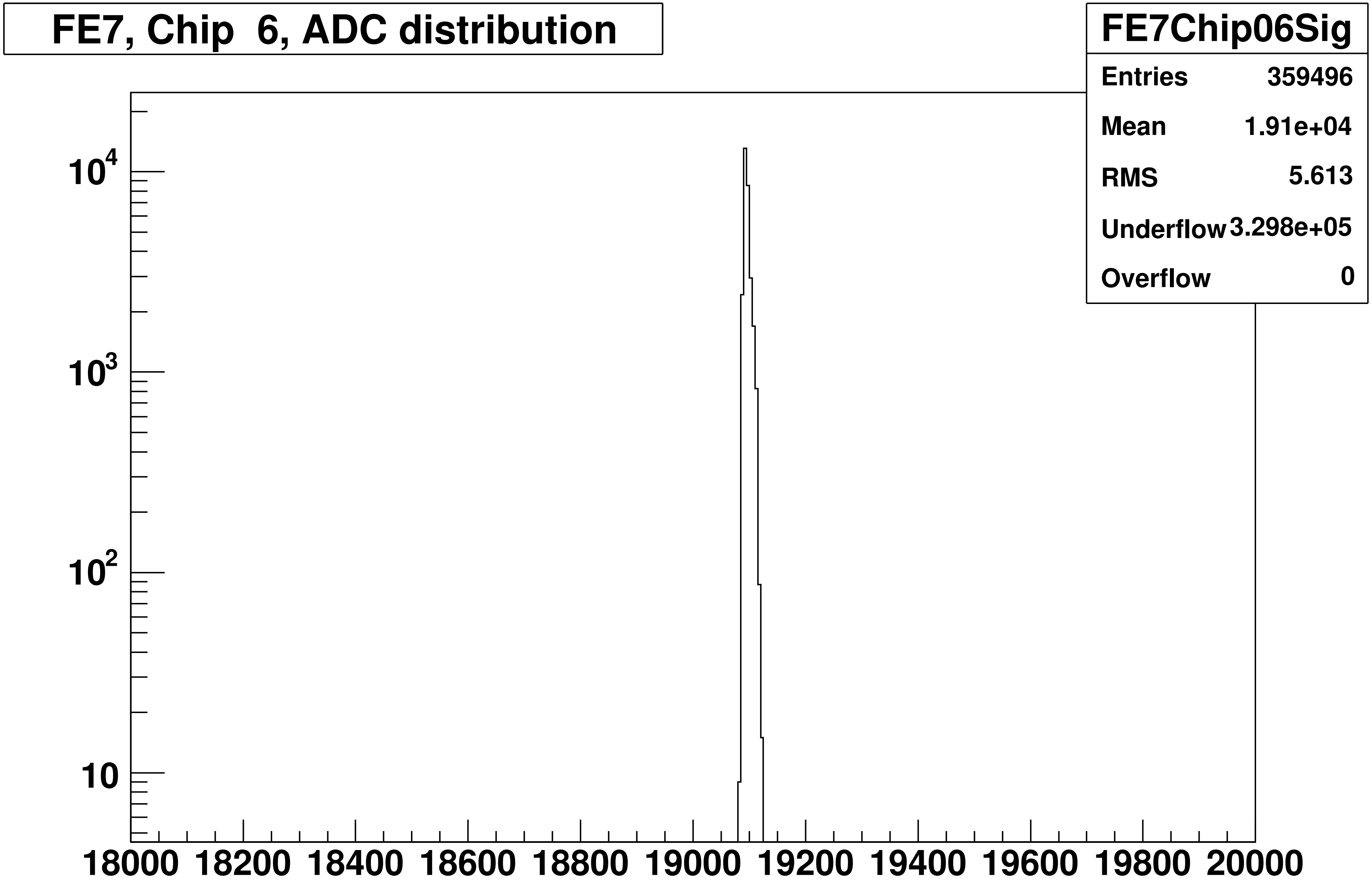
100
150
200


FE7, Chip 6, ADC distribution
FE7Chip06Sig
Entries 359496
Mean 1.91e+04
RMS 5.613
Underflow 3.298e+05
Overflow 0
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10^2
10^3
10^4
18000
18200
18400
18600
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19000
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19400
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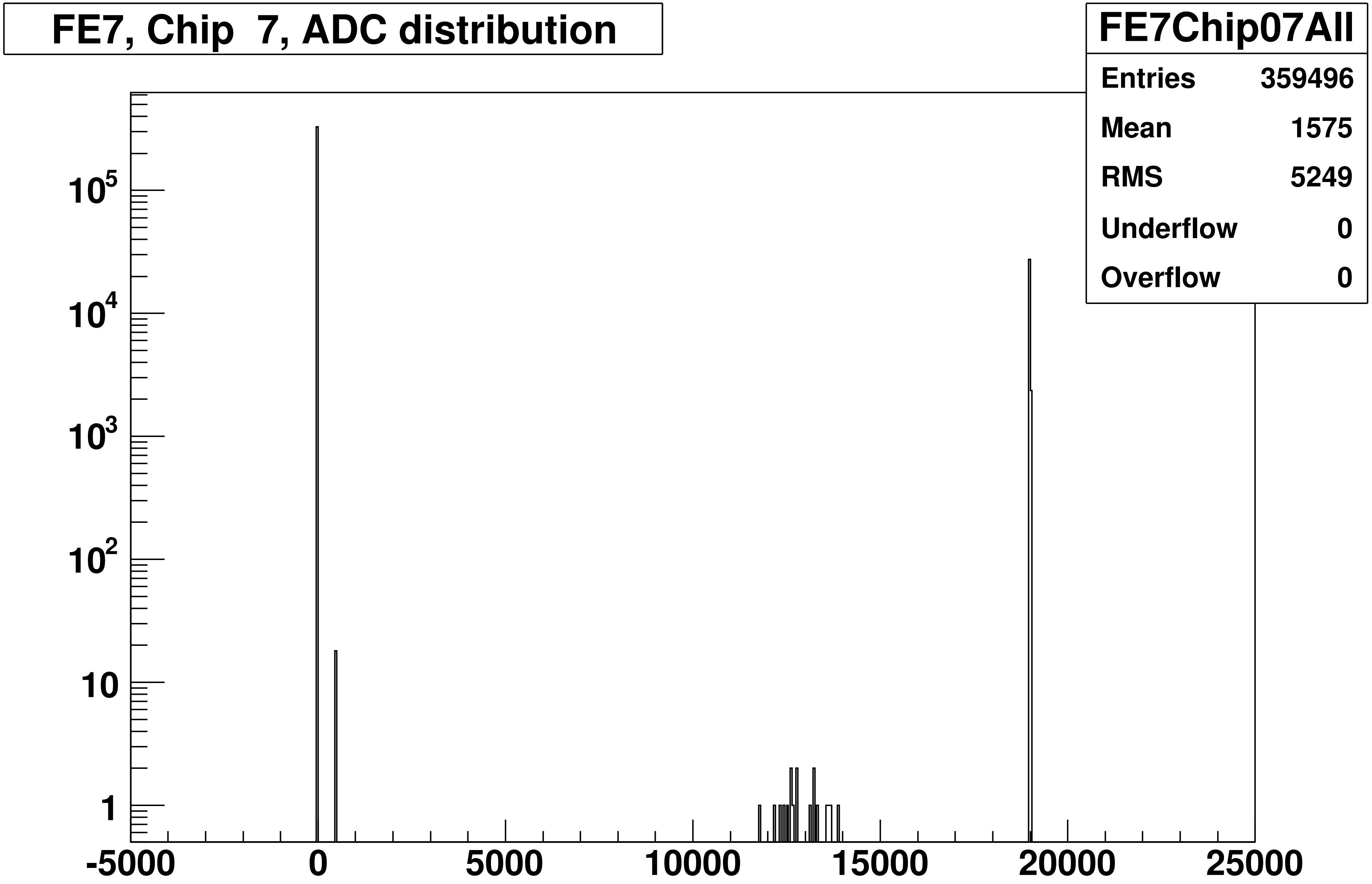
20000


FE7, Chip 7, ADC distribution
FE7Chip07All
Entries 359496
Mean 1575
RMS 5249
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
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-5000
0
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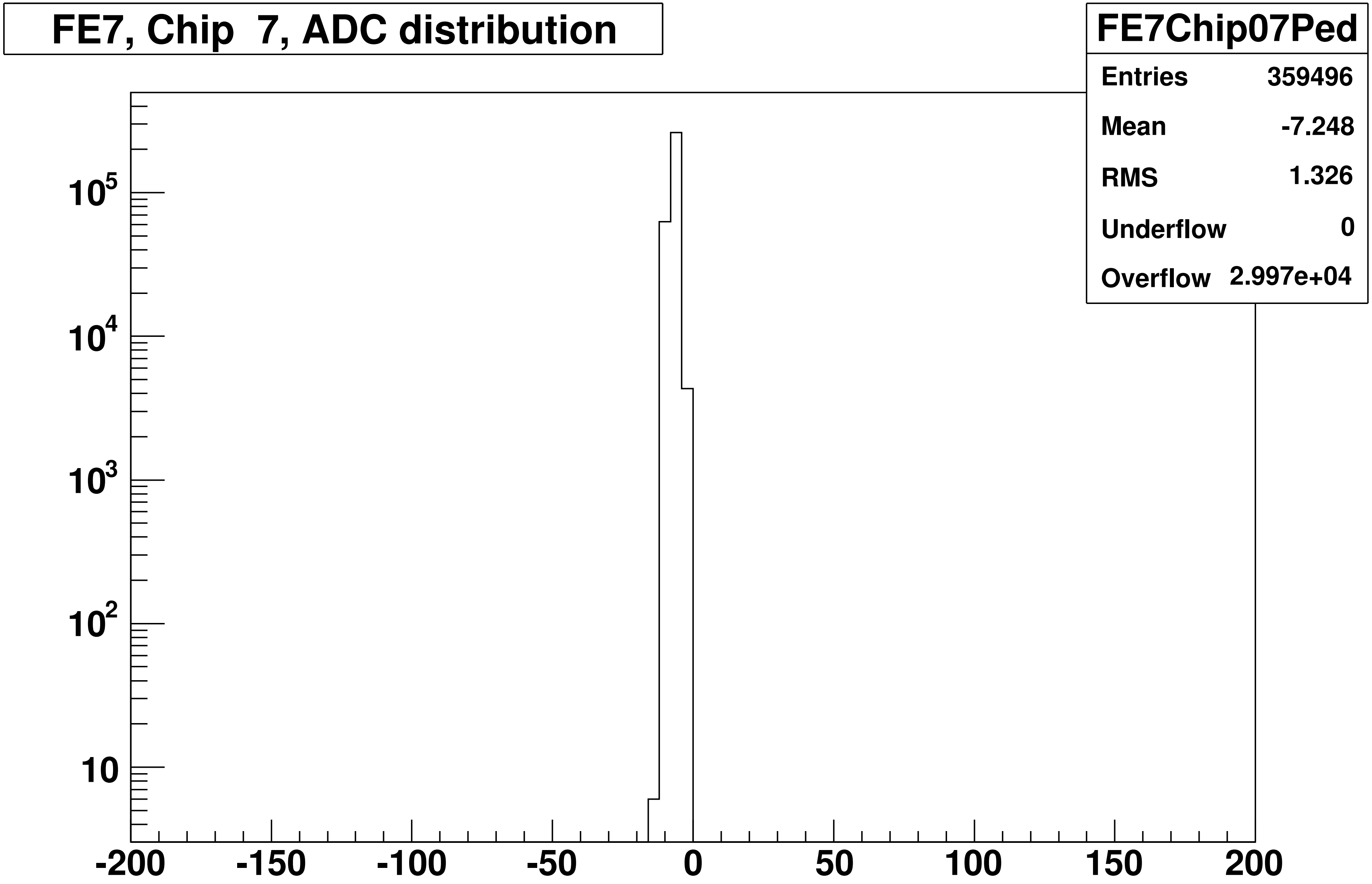
10000
15000
20000
25000



FE7, Chip 7, ADC distribution
FE7Chip07Ped
Entries 359496
Mean -7.248
RMS 1.326
Underflow 0
Overflow 2.997e+04
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10^4
10^3
10^2
10
-200
-150
-100
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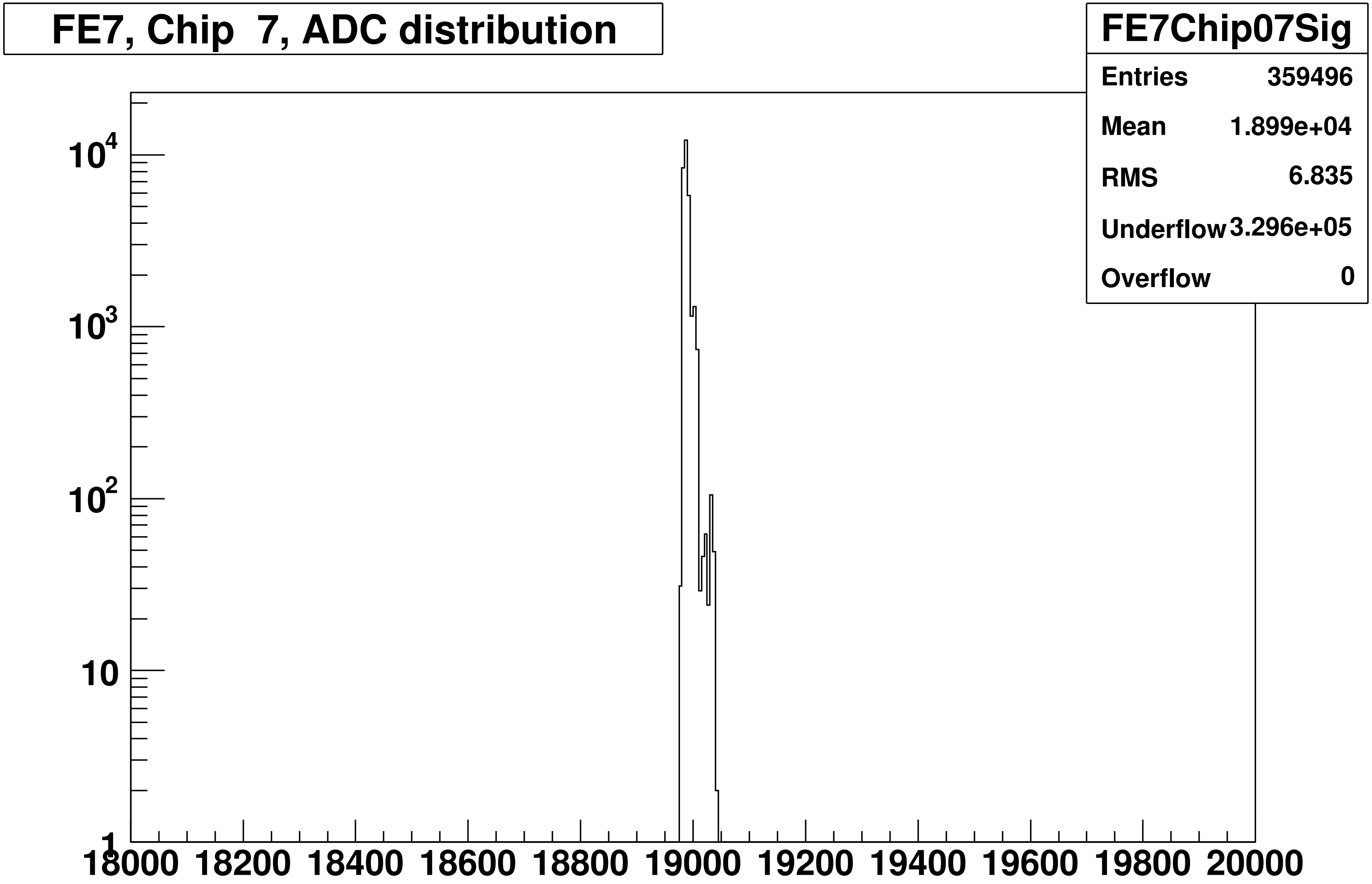
100
150
200


FE7, Chip 7, ADC distribution
FE7Chip07Sig
Entries 359496
Mean 1.899e+04
RMS 6.835
Underflow 3.296e+05
Overflow 0
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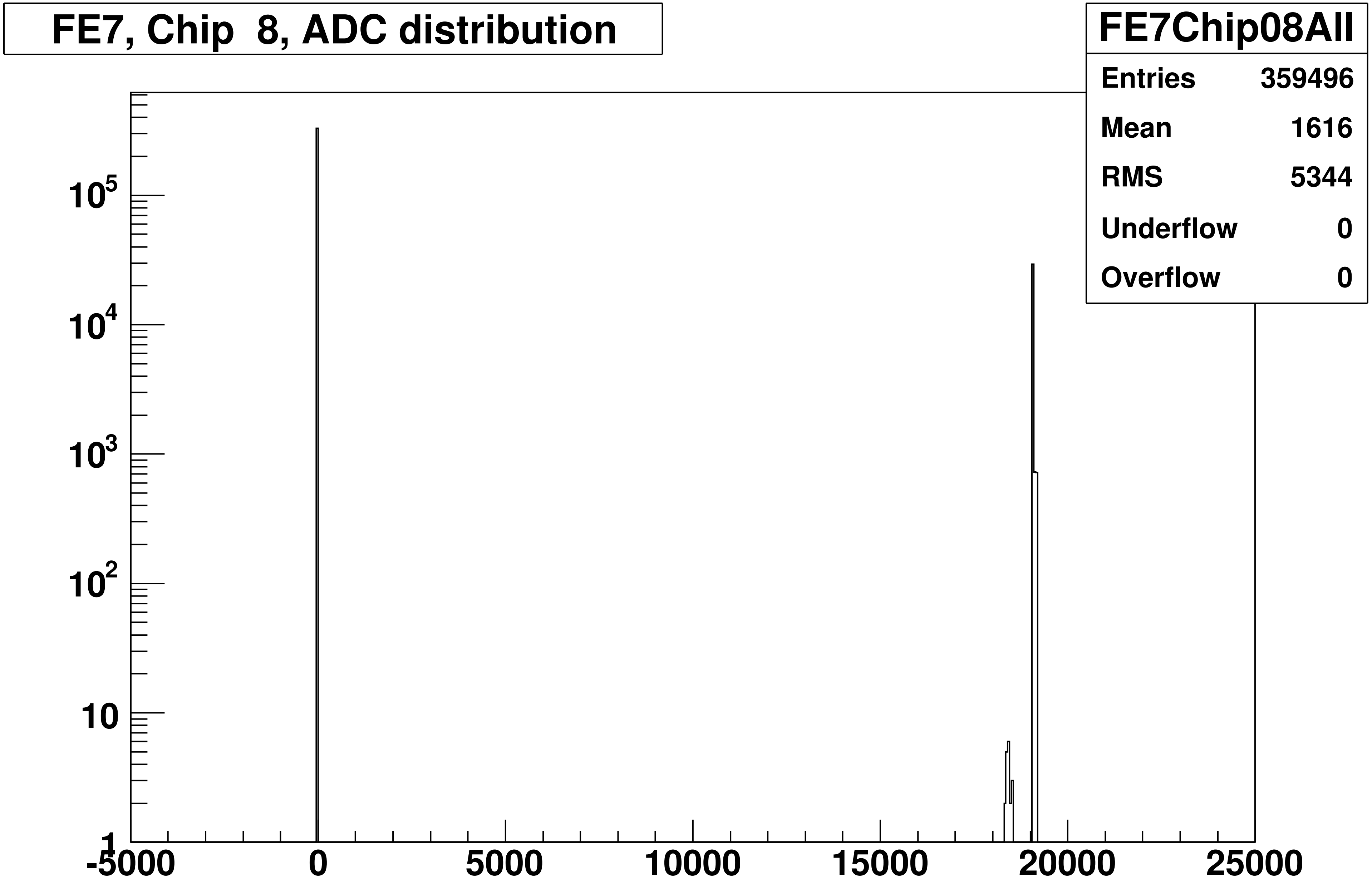
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE7, Chip 8, ADC distribution
FE7Chip08All
Entries 359496
Mean 1616
RMS 5344
Underflow 0
Overflow 0
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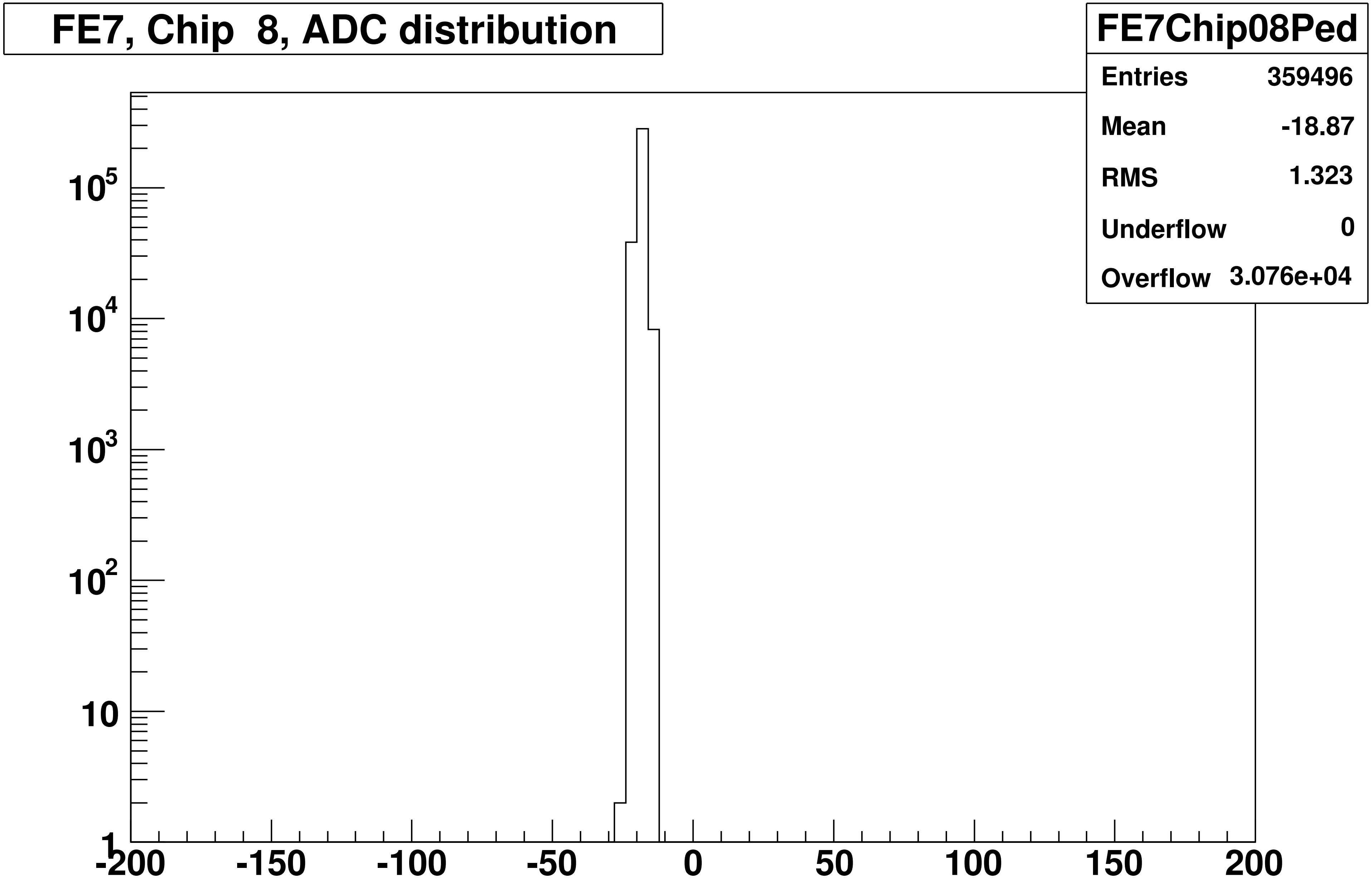
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE7, Chip 8, ADC distribution
FE7Chip08Ped
Entries 359496
Mean -18.87
RMS 1.323
Underflow 0
Overflow 3.076e+04
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10^4
10^3
10^2
10
1
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-100
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50
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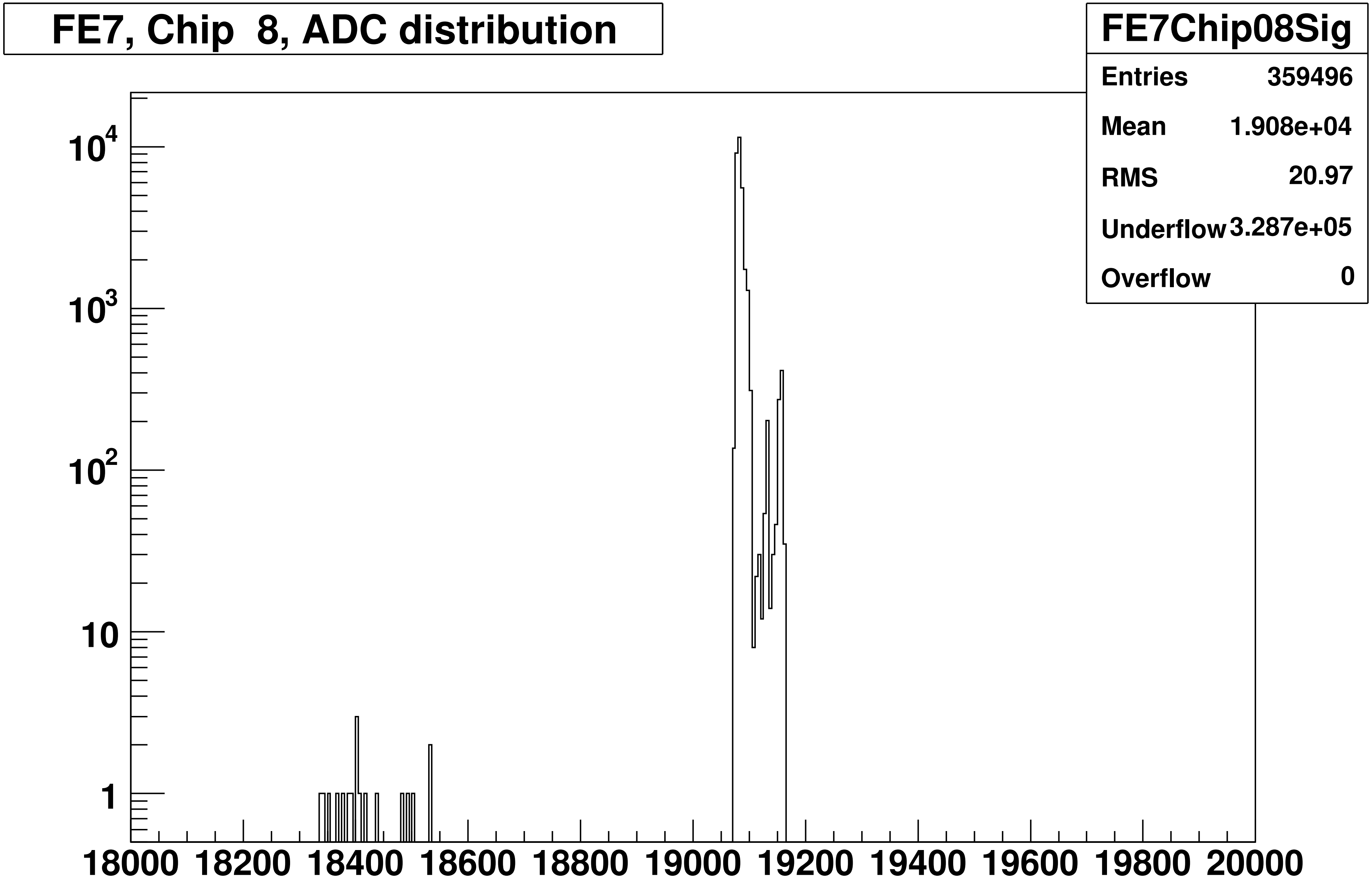
150
200


FE7, Chip 8, ADC distribution
FE7Chip08Sig
Entries 359496
Mean 1.908e+04
RMS 20.97
Underflow 3.287e+05
Overflow 0
10^4
10^3
10^2
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18000
18200
18400
18600
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19000
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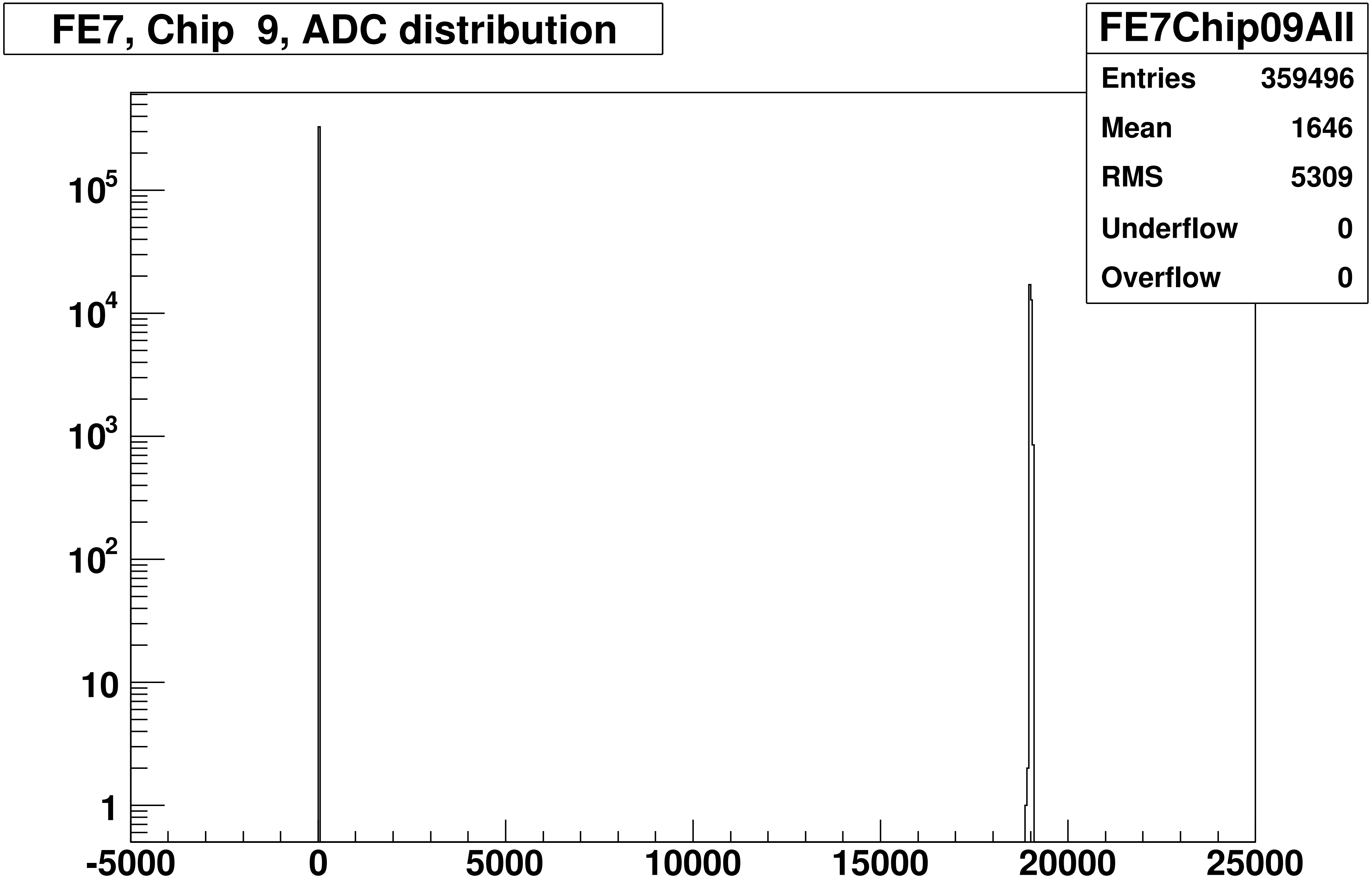
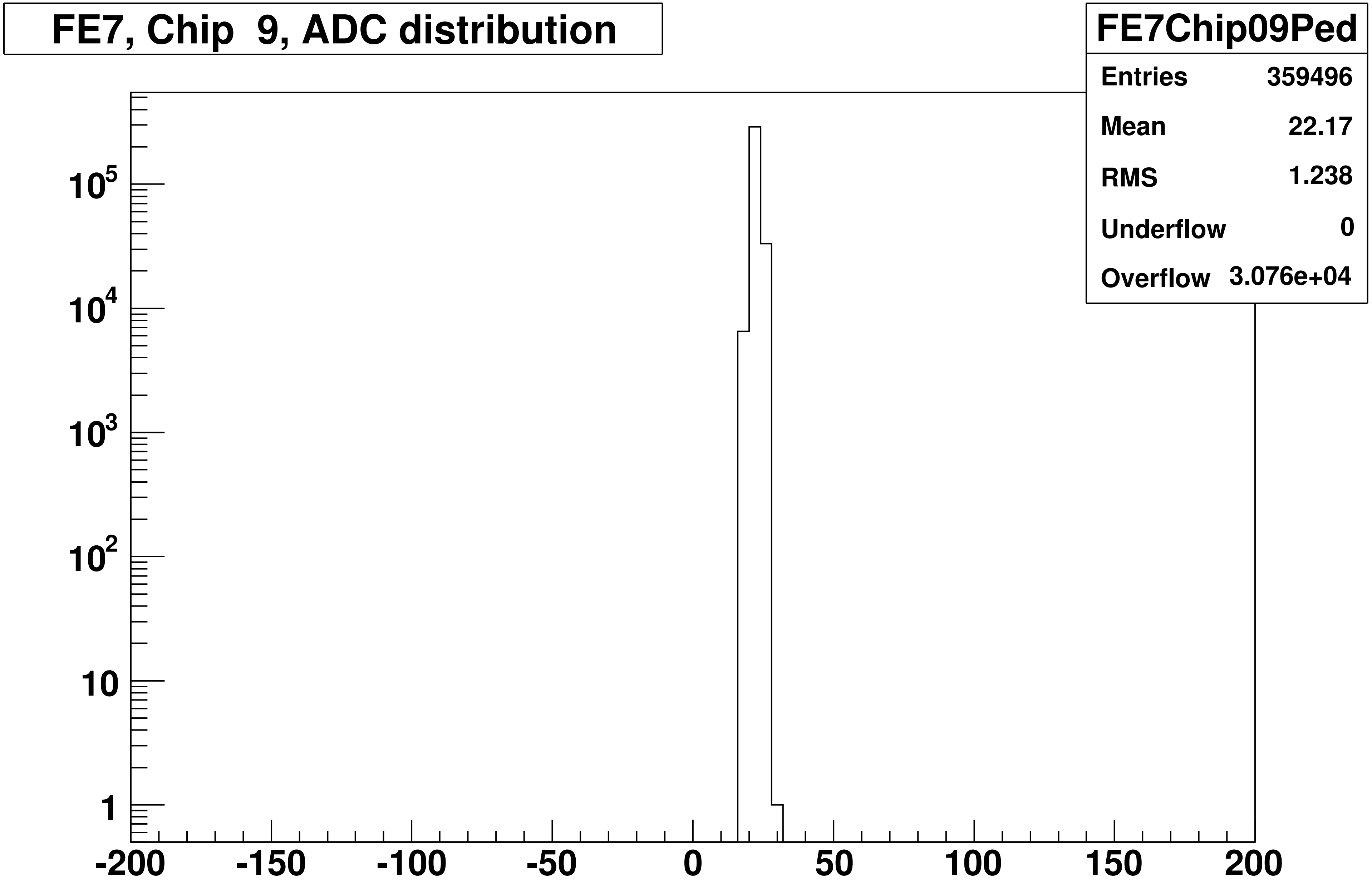
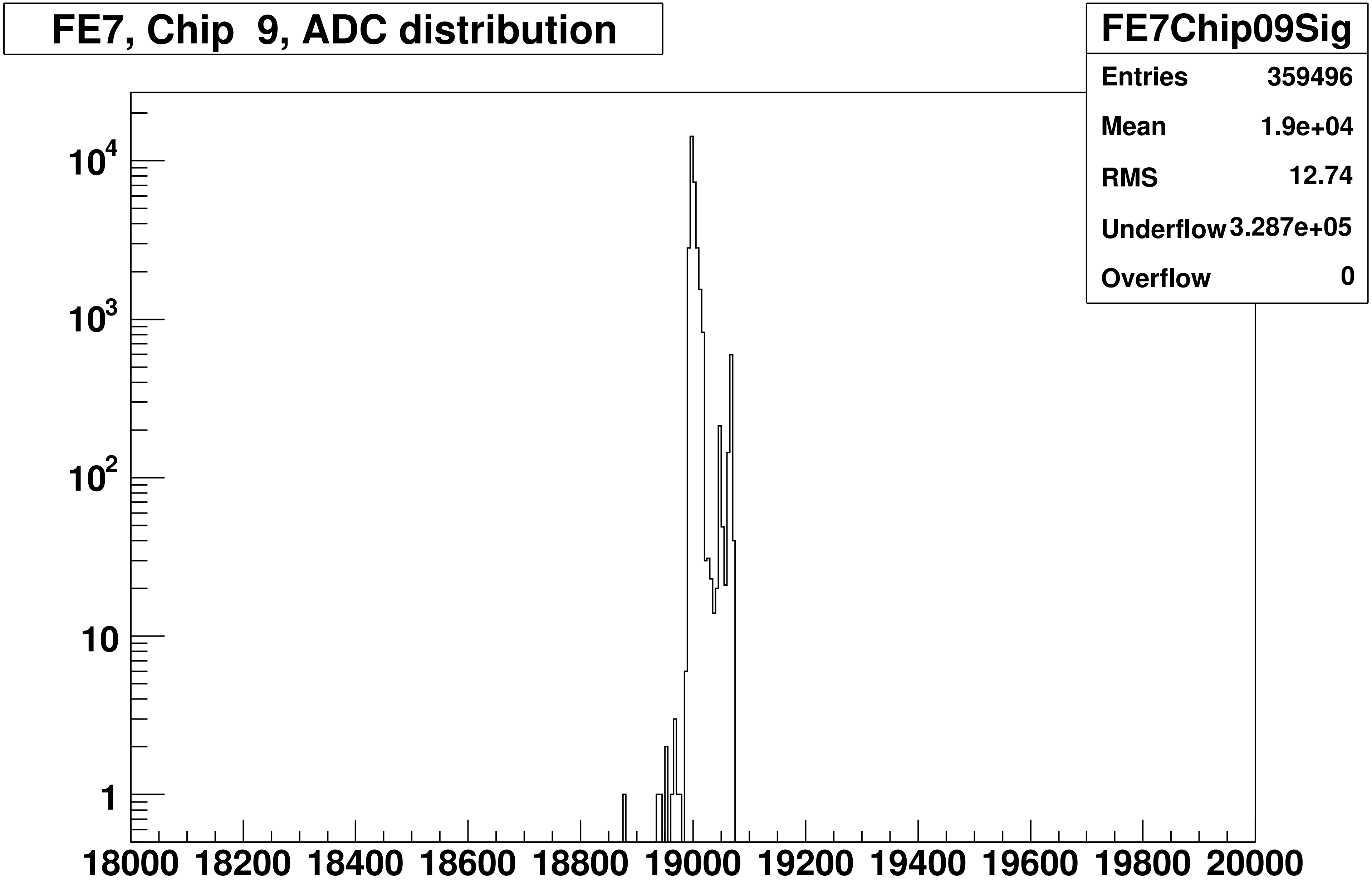
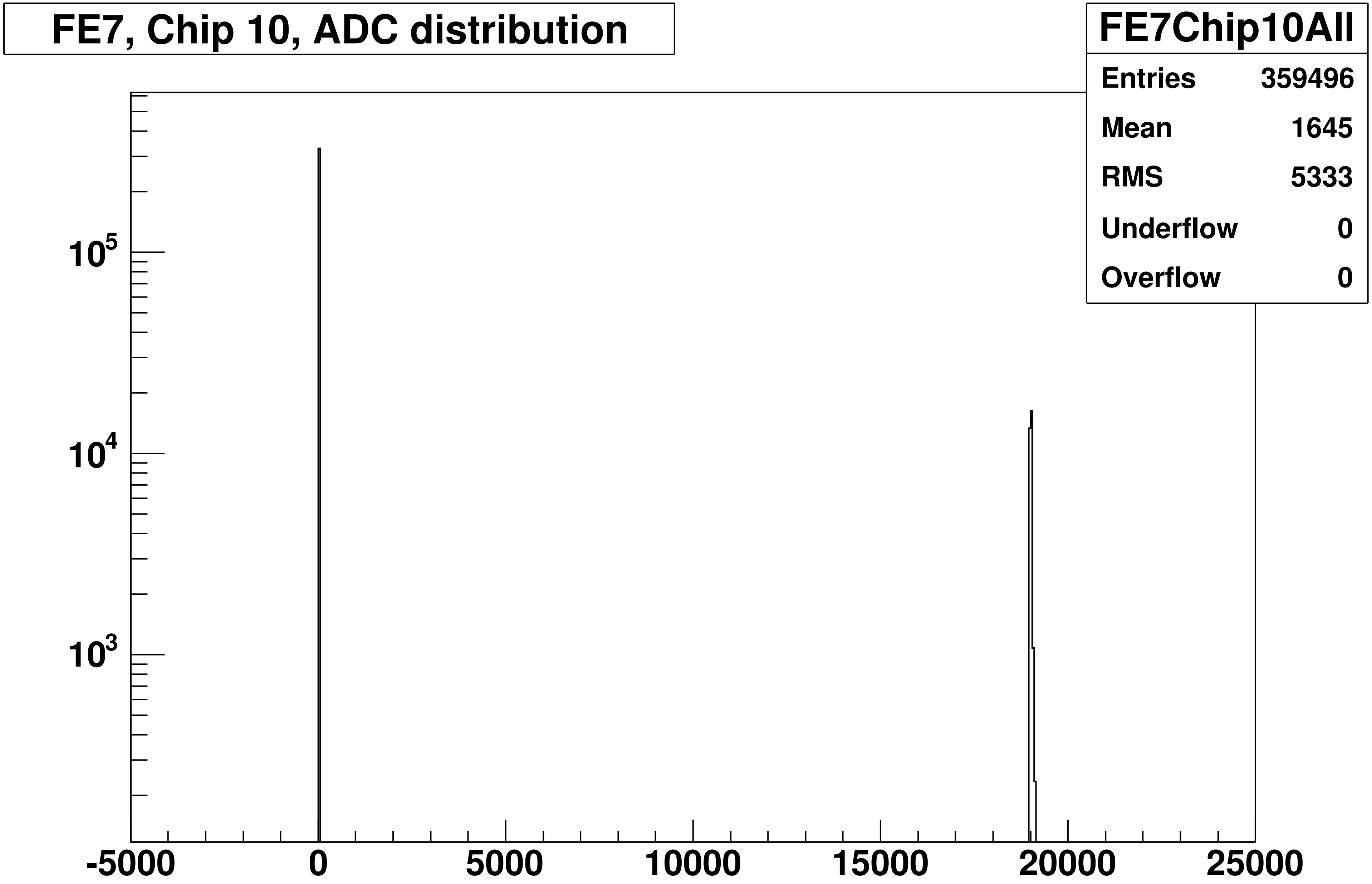
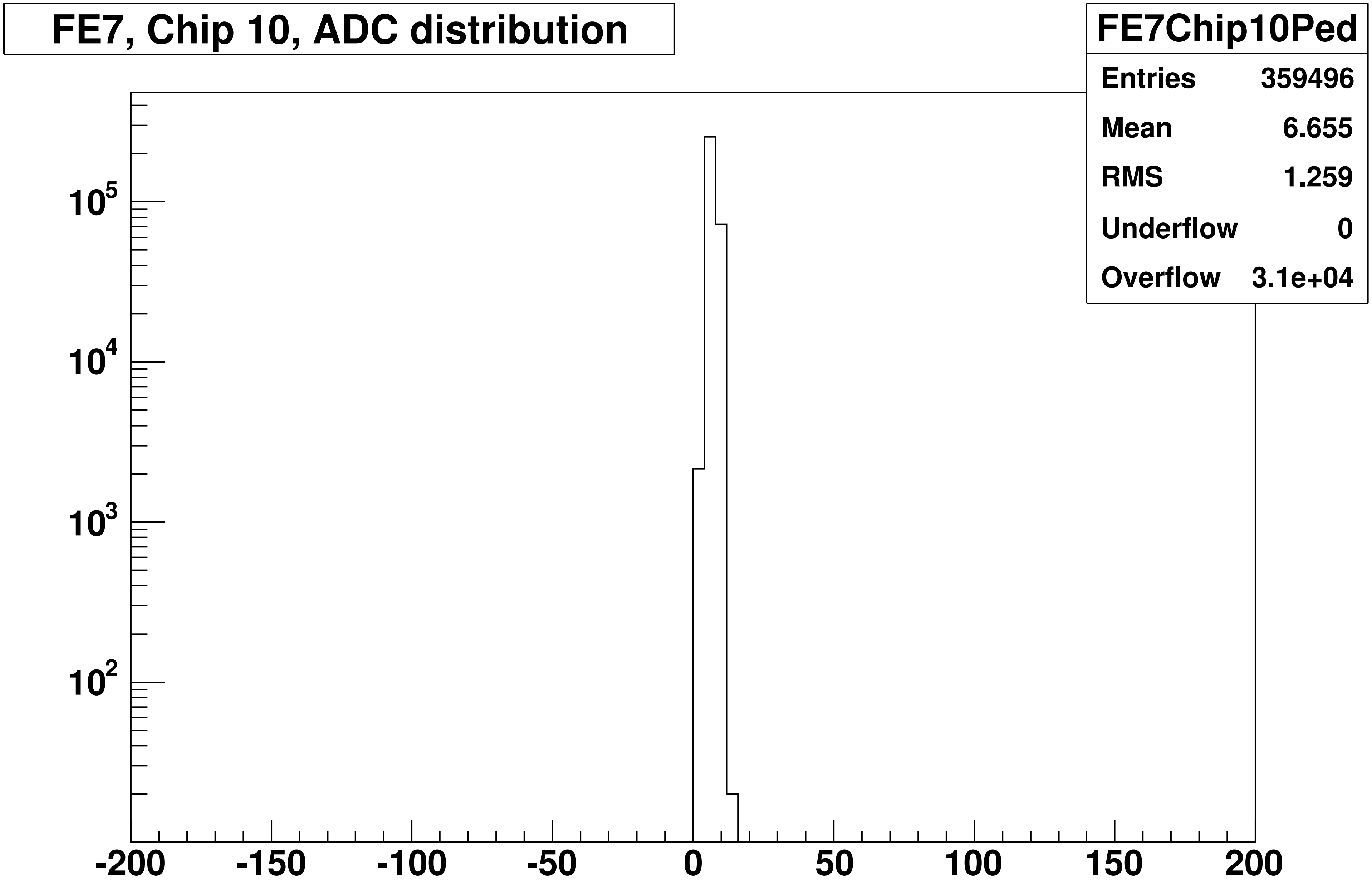
19800
20000


FE7, Chip 9, ADC distribution
FE7Chip09All
Entries 359496
Mean 1646
RMS 5309
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000

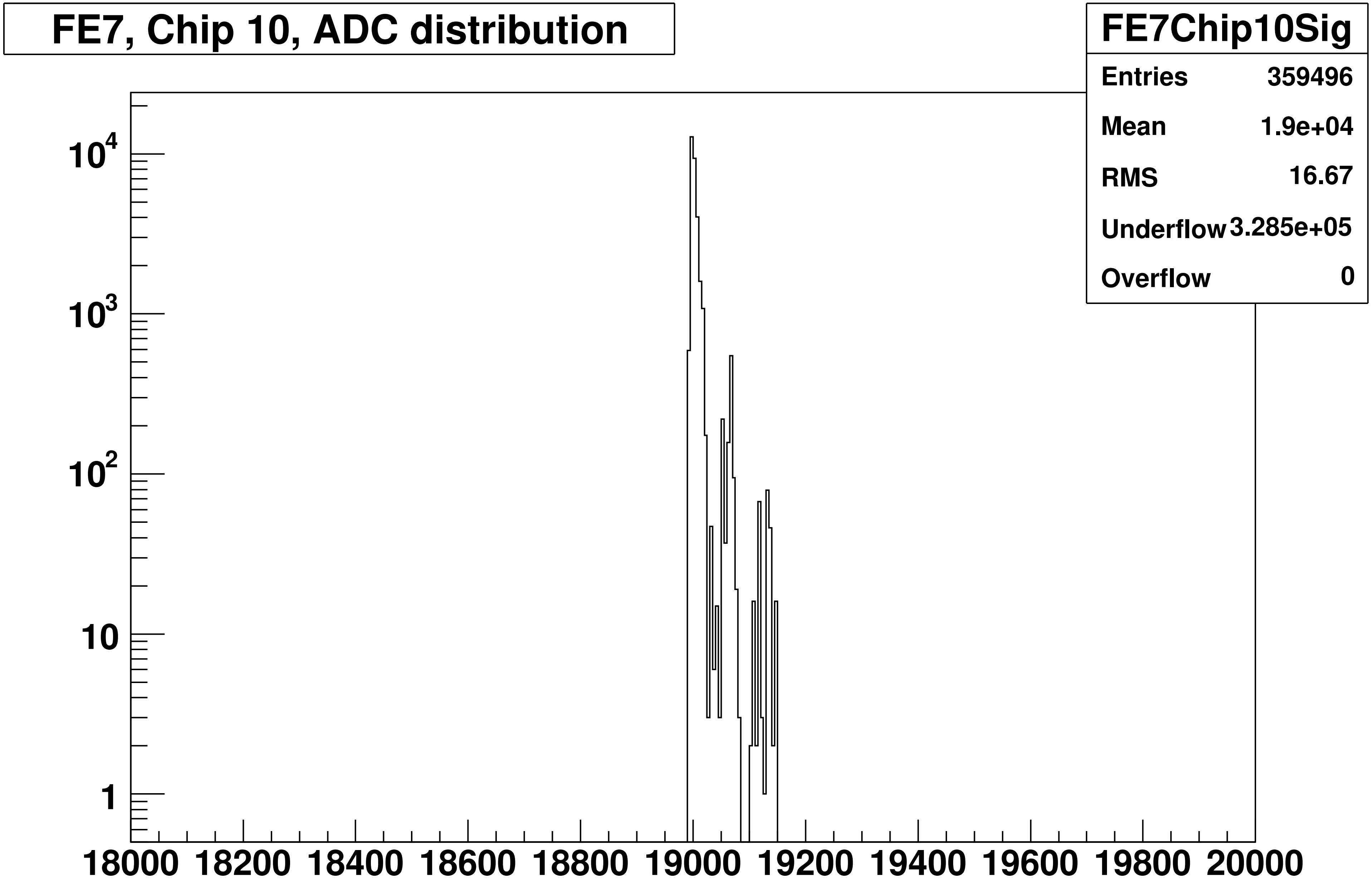

FE7, Chip 9, ADC distribution
FE7Chip09Ped
Entries 359496
Mean 22.17
RMS 1.238
Underflow 0
Overflow 3.076e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
200


FE7, Chip 9, ADC distribution
FE7Chip09Sig
Entries 359496
Mean 1.9e+04
RMS 12.74
Underflow 3.287e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000

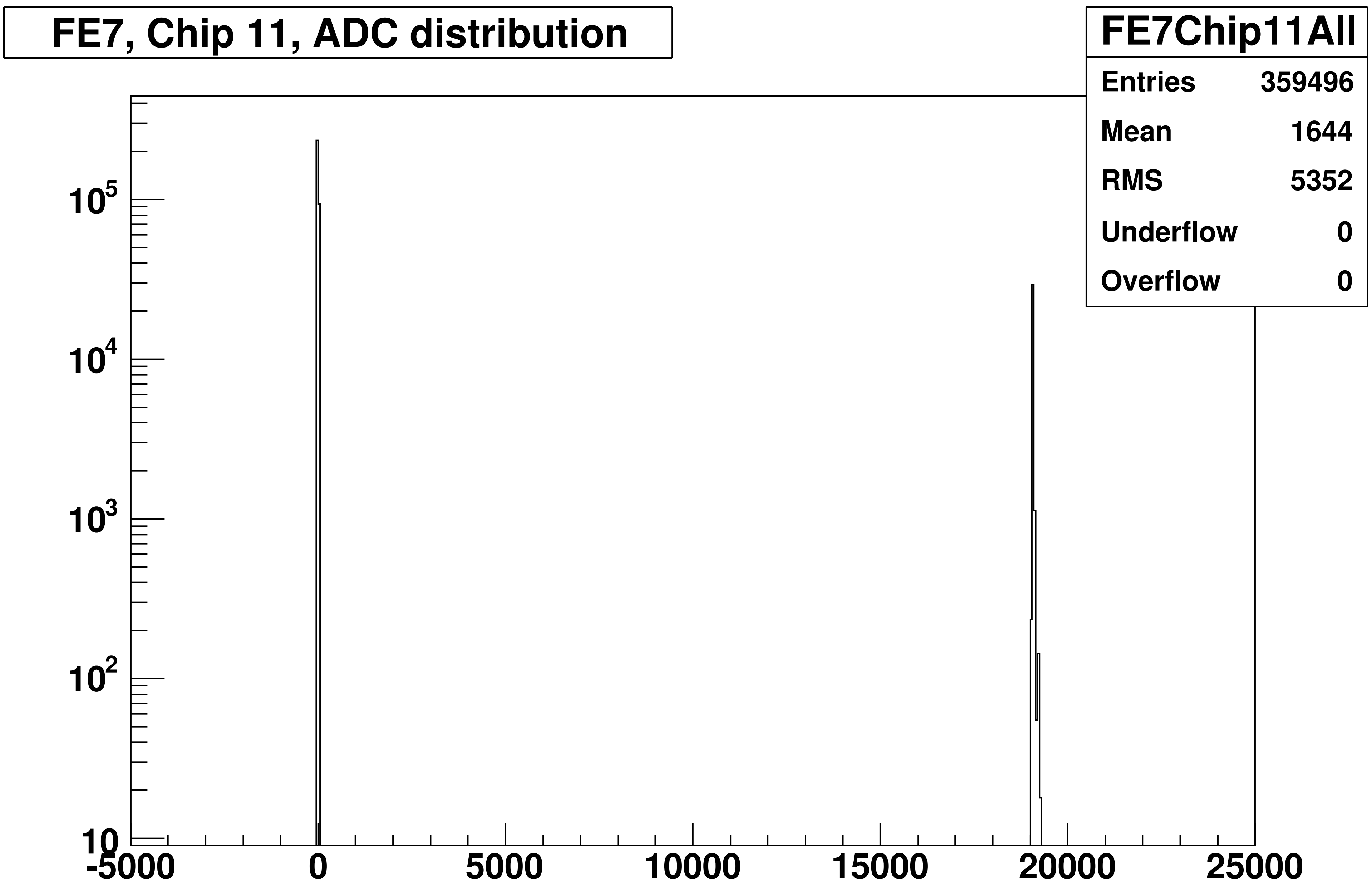

FE7, Chip 10, ADC distribution
FE7Chip10All
Entries 359496
Mean 1645
RMS 5333
Underflow 0
Overflow 0
10^5
10^4
10^3
-5000
0
5000
10000
15000
20000
25000

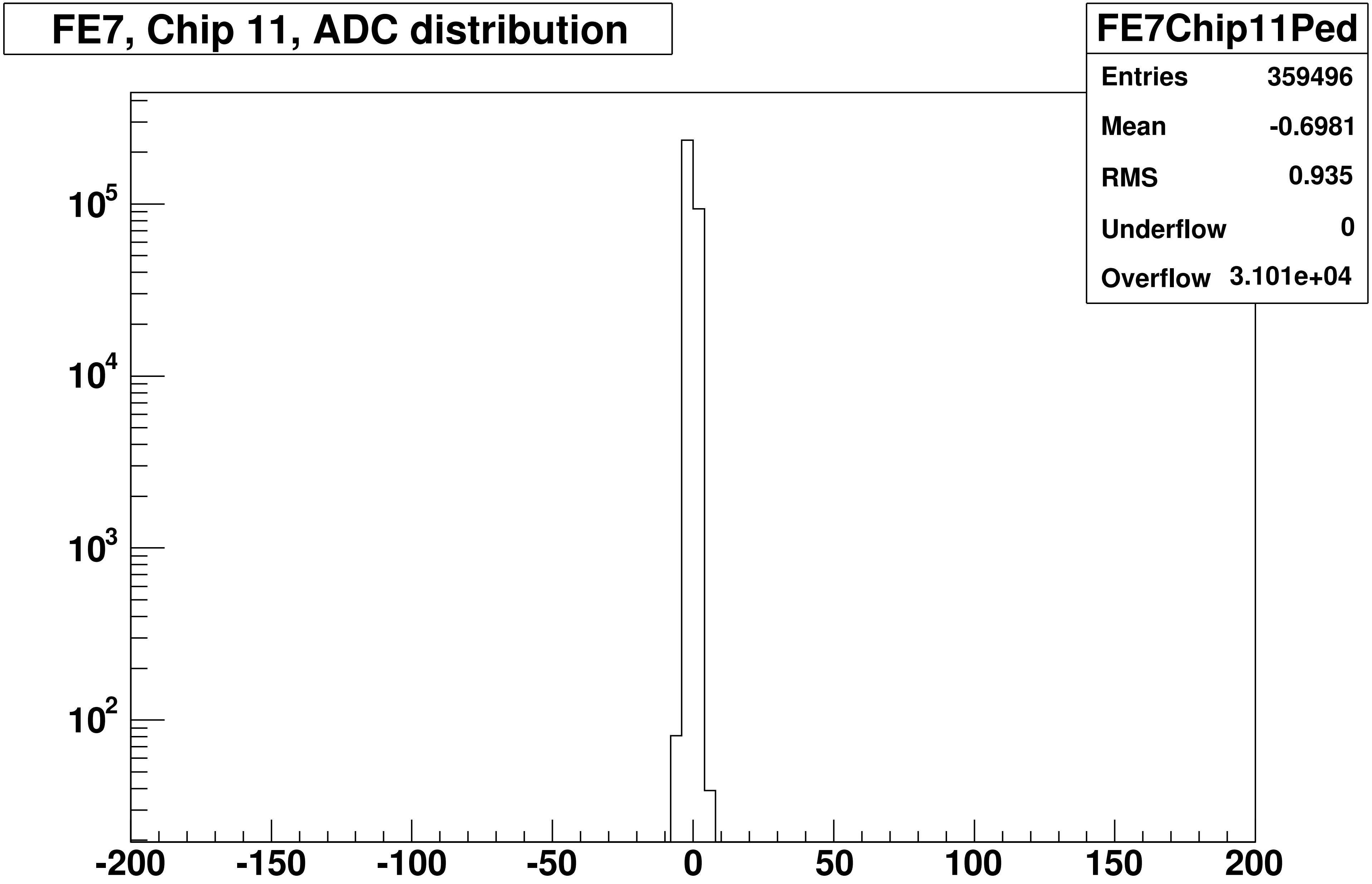


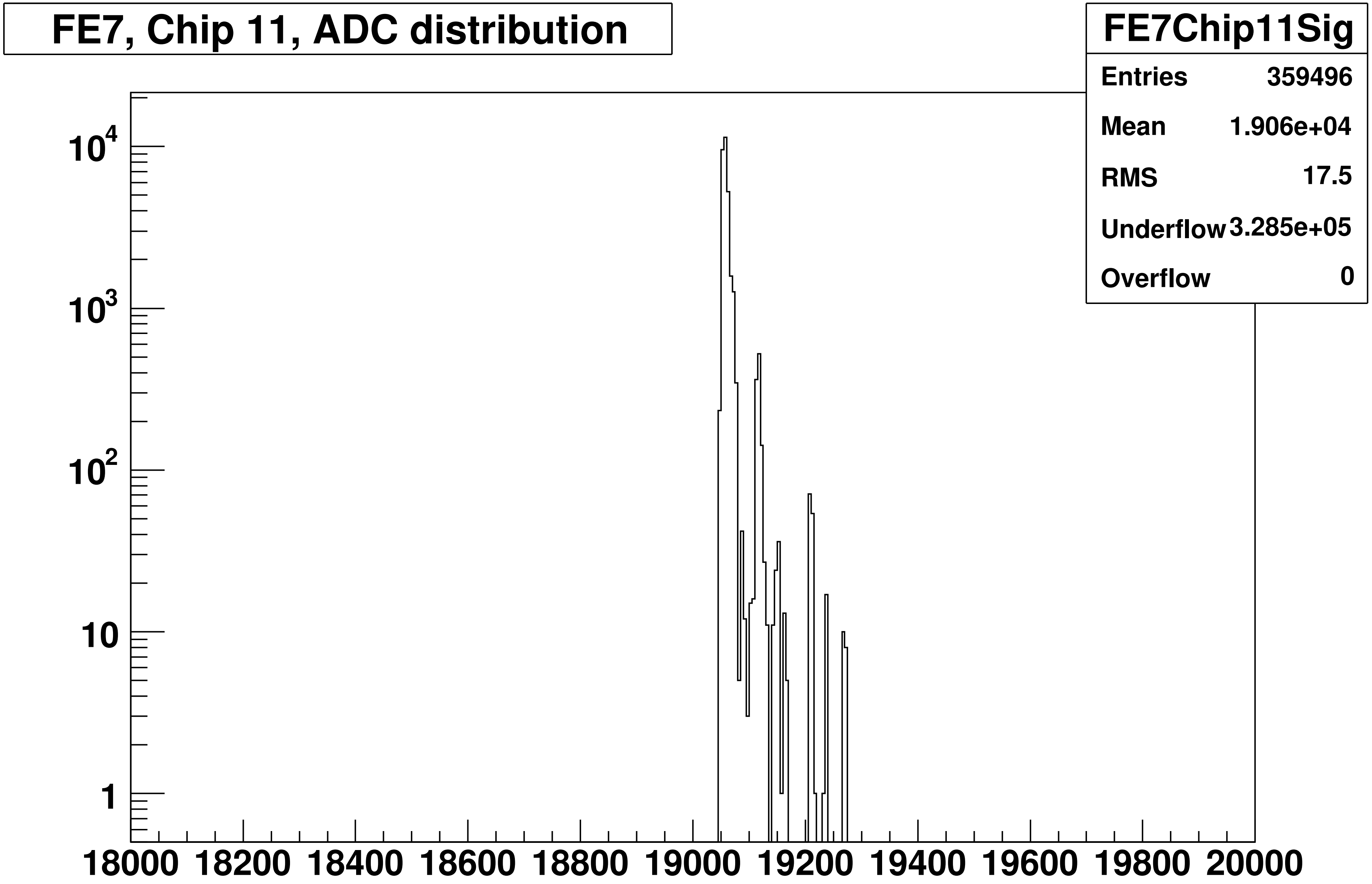
FE7, Chip 10, ADC distribution
FE7Chip10Ped
Entries 359496
Mean 6.655
RMS 1.259
Underflow 0
Overflow 3.1e+04
10^5
10^4
10^3
10^2
-200
-150
-100
-50
0
50
100
150
200

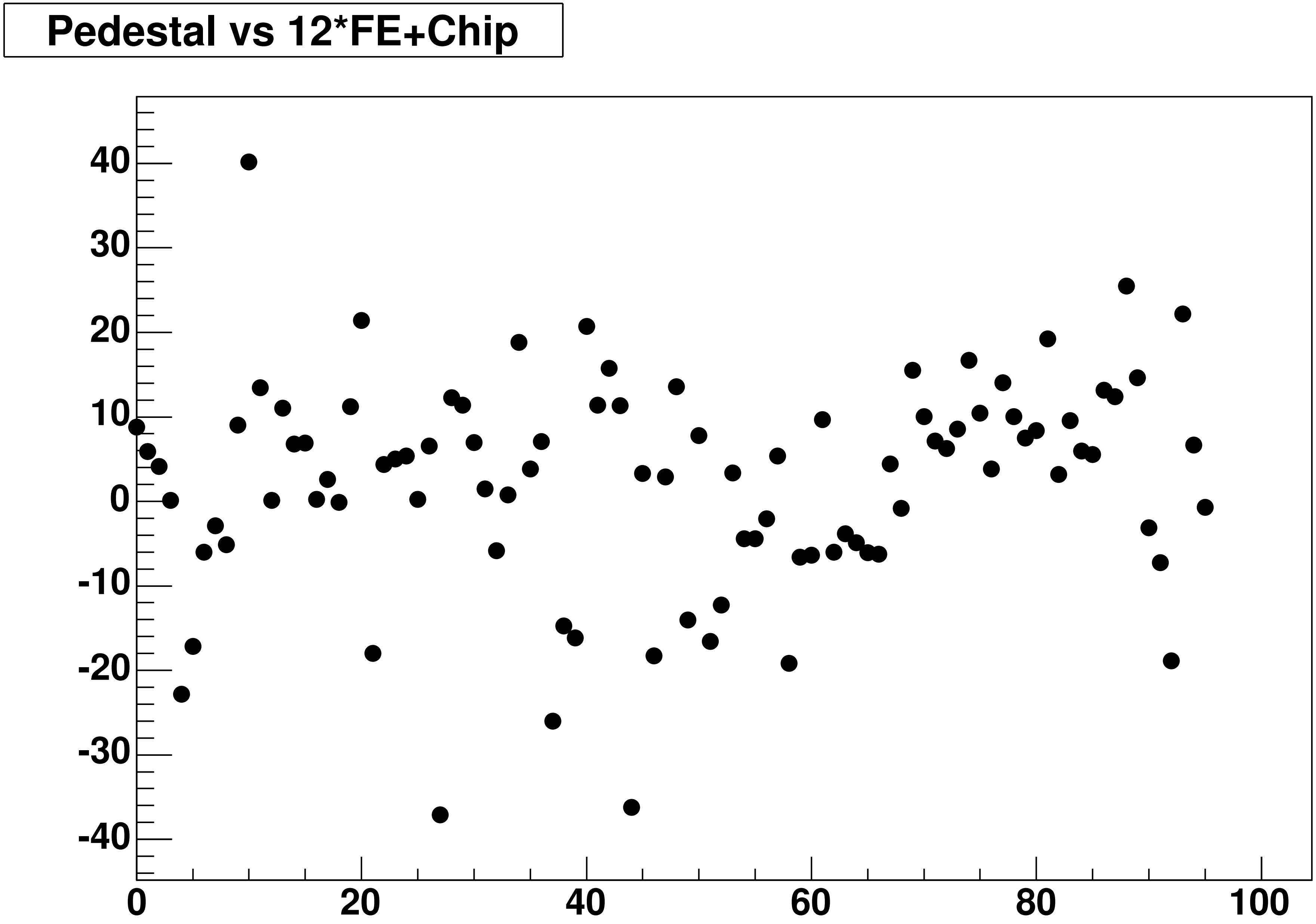


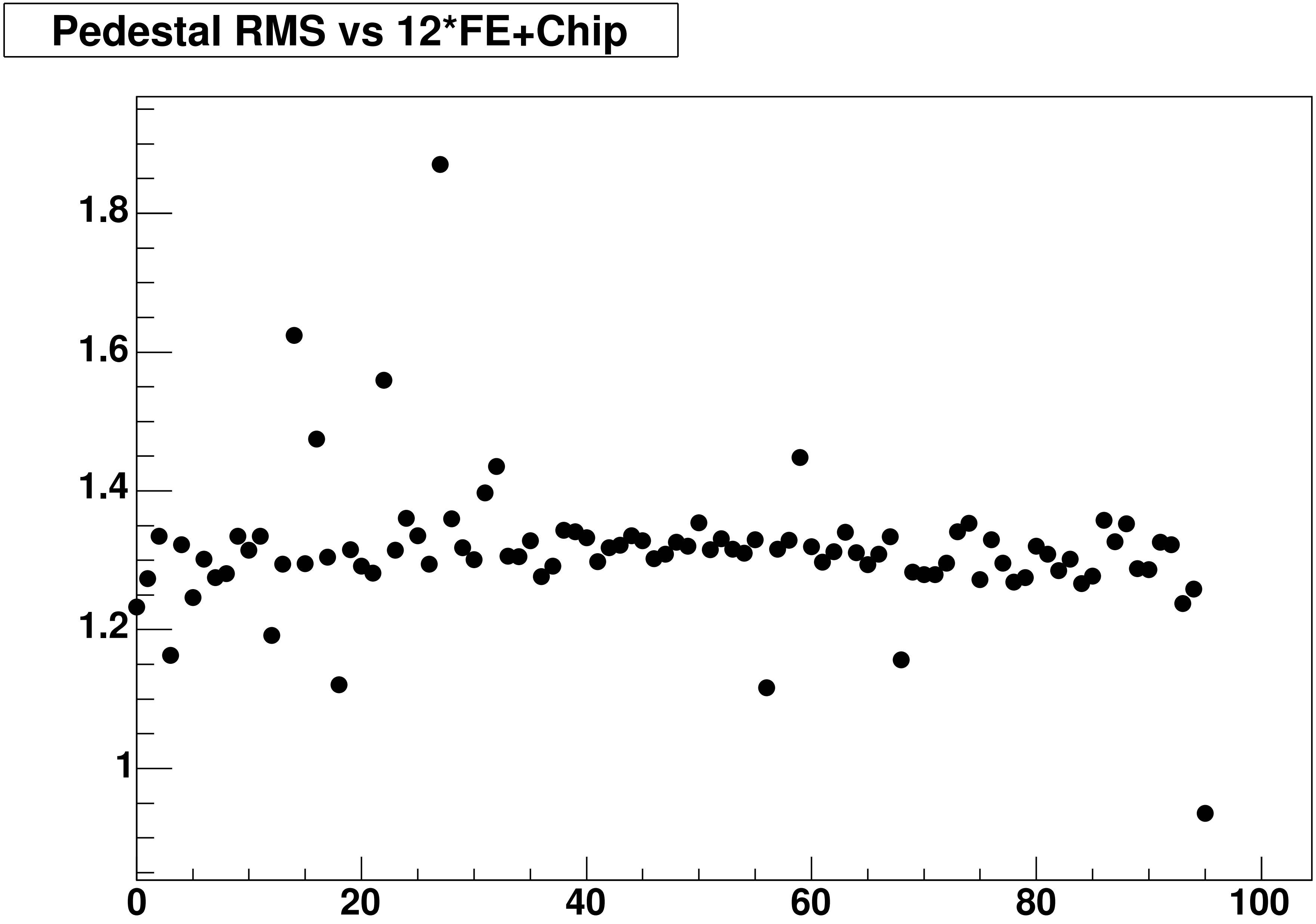
FE7, Chip 10, ADC distribution
FE7Chip10Sig
Entries 359496
Mean 1.9e+04
RMS 16.67
Underflow 3.285e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000

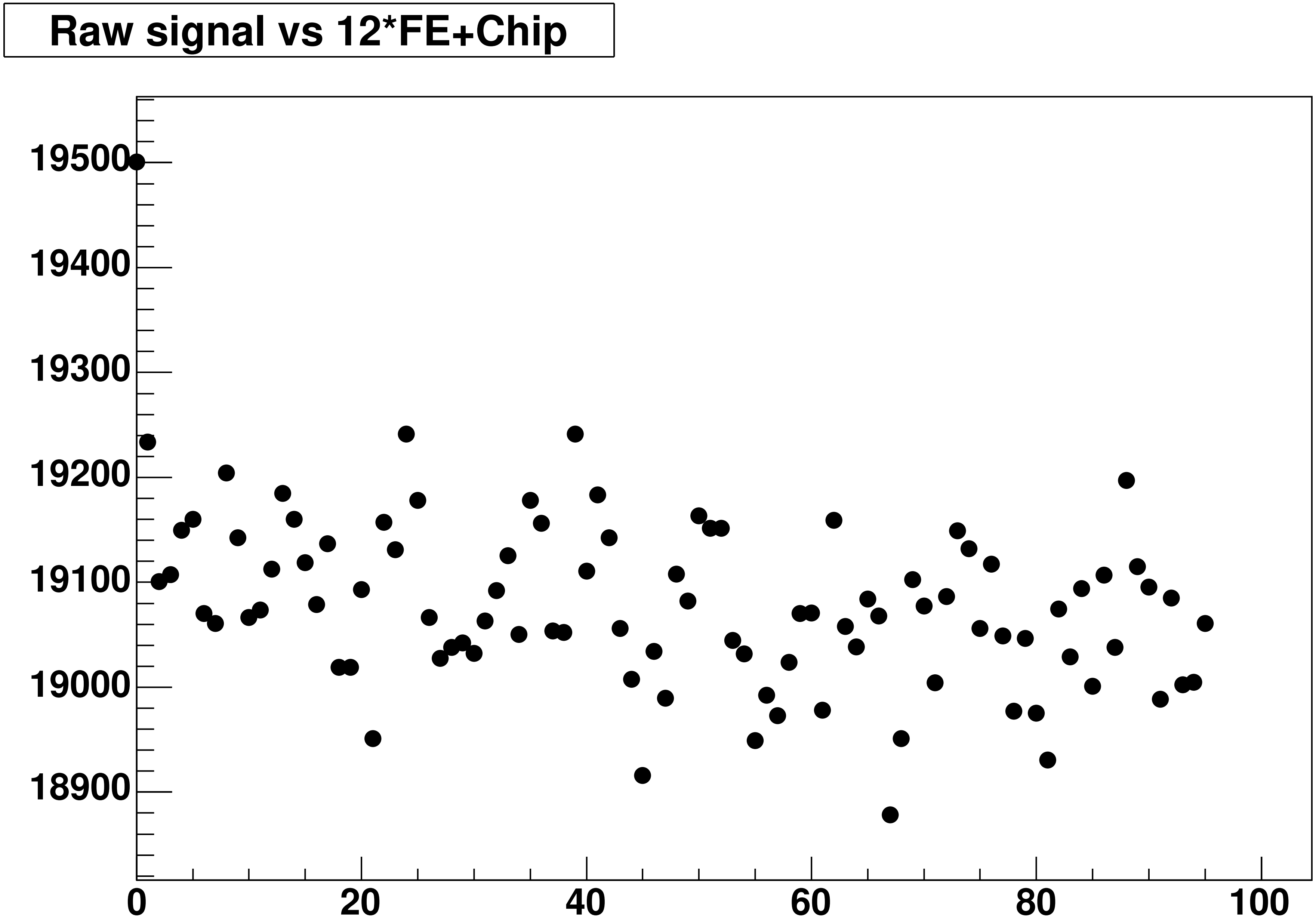

FE7, Chip 11, ADC distribution
FE7Chip11All
Entries 359496
Mean 1644
RMS 5352
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000

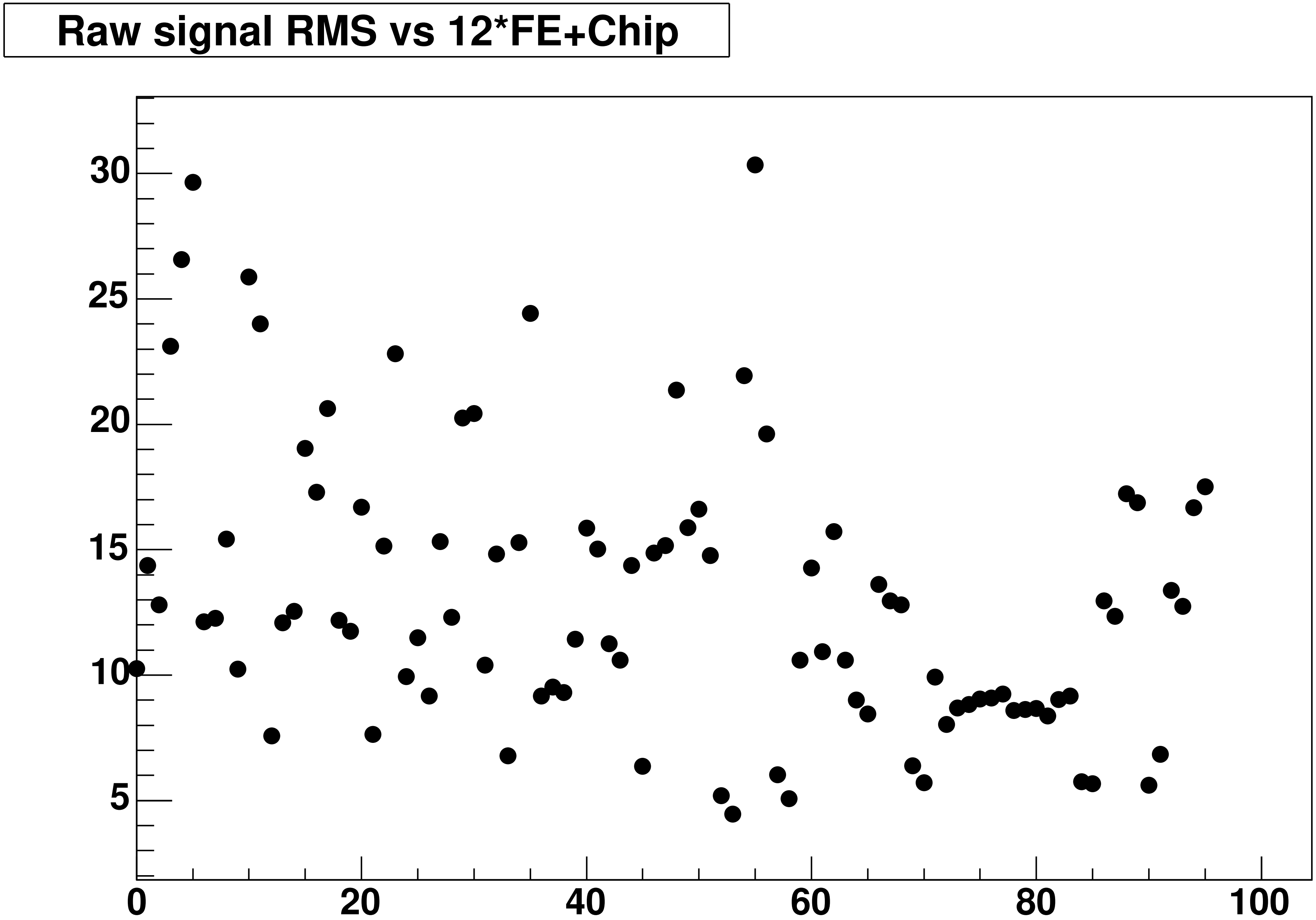

FE7, Chip 11, ADC distribution
FE7Chip11Ped
Entries 359496
Mean -0.6981
RMS 0.935
Underflow 0
Overflow 3.101e+04
10^5
10^4
10^3
10^2
-200
-150
-100
-50
0
50
100
150
200


FE7, Chip 11, ADC distribution
FE7Chip11Sig
Entries 359496
Mean 1.906e+04
RMS 17.5
Underflow 3.285e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000

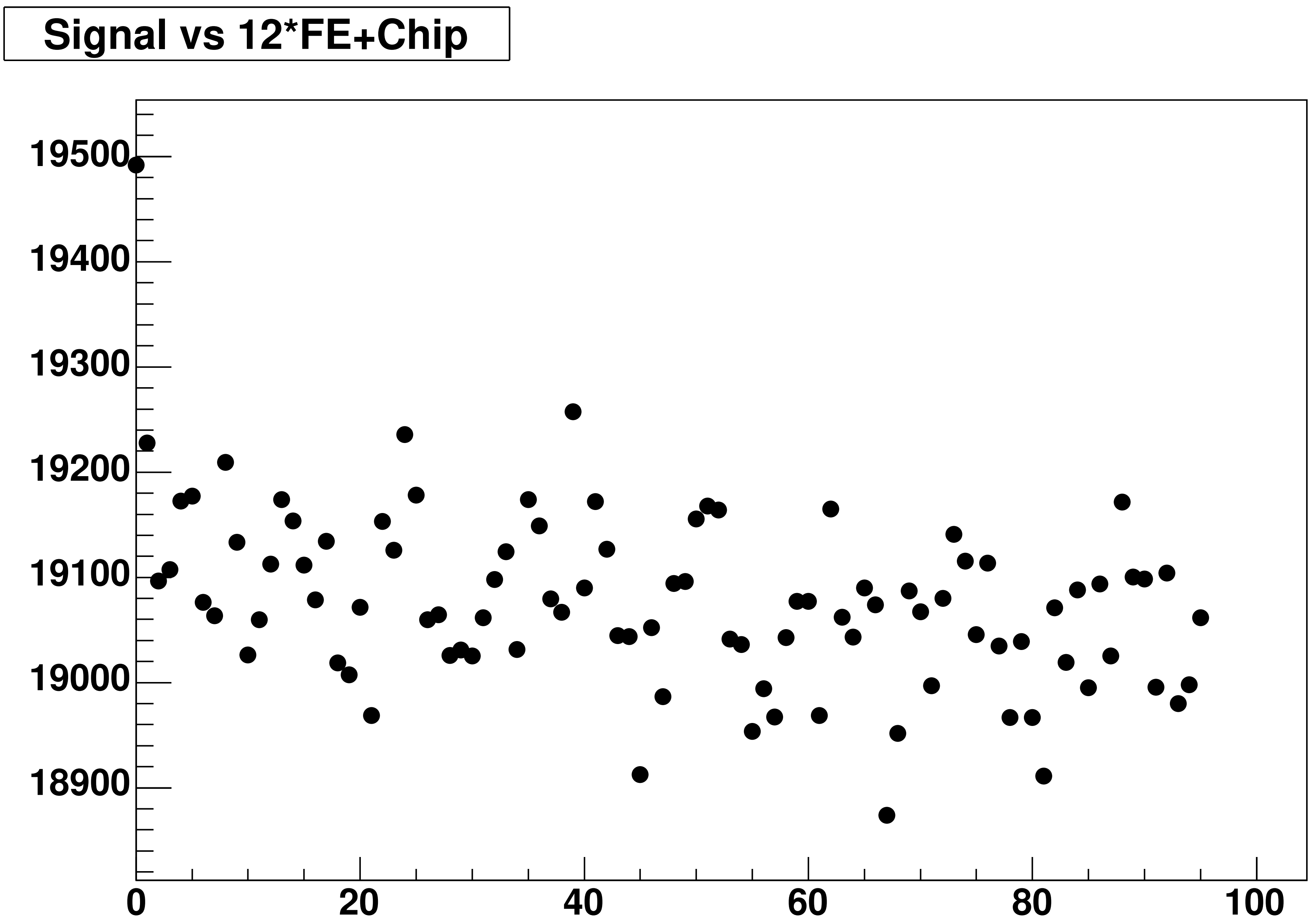

Pedestal vs 12*FE+Chip
40
30
20
10
0
-10
-20
-30
-40
0
20
40
60
80
100

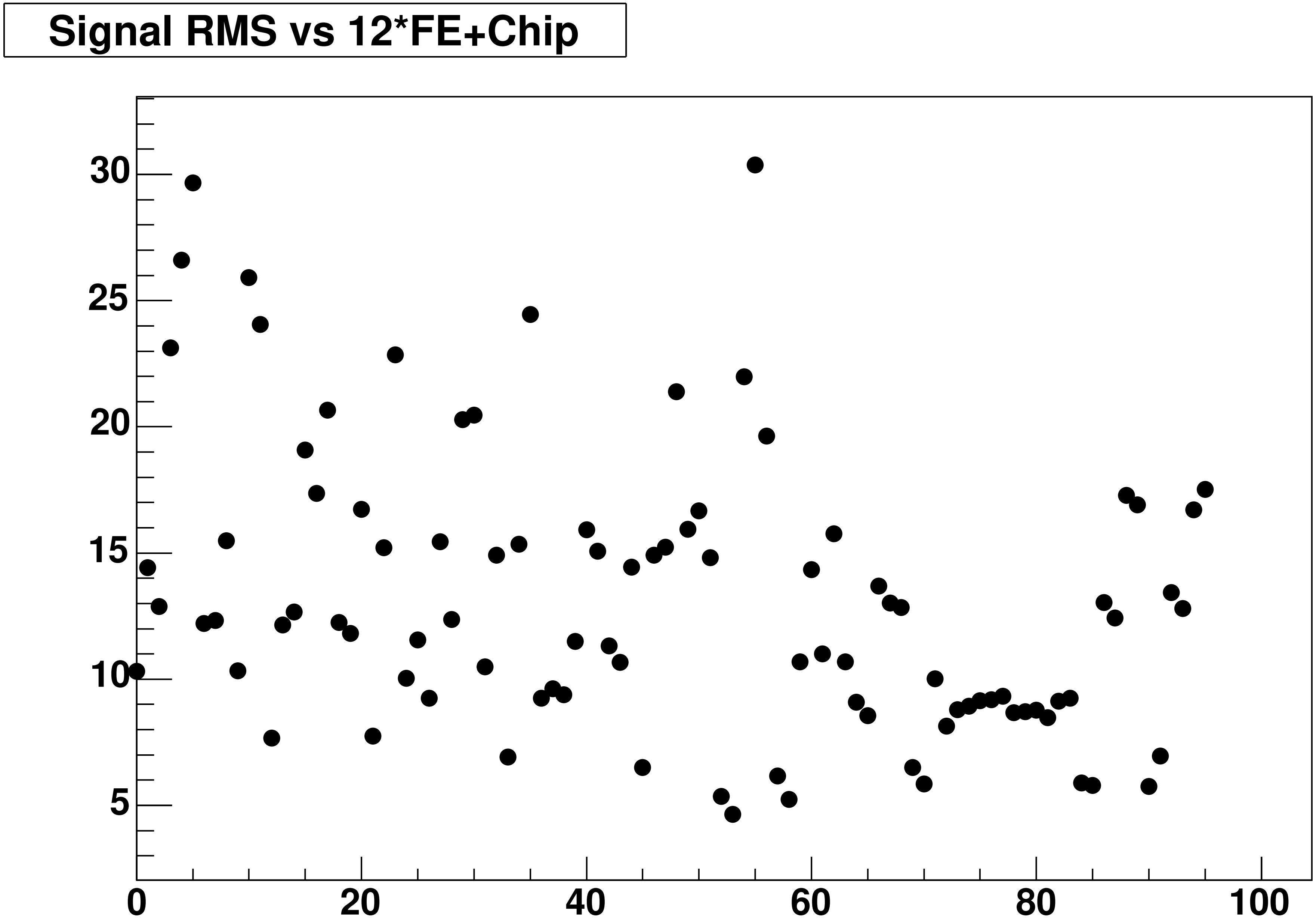

Pedestal RMS vs 12*FE+Chip
1.8
1.6
1.4
1.2
1
0
20
40
60
80
100


Raw signal vs 12*FE+Chip
19500
19400
19300
19200
19100
19000
18900
0
20
40
60
80
100



Raw signal RMS vs 12*FE+Chip
5
10
15
20
25
30
0
20
40
60
80
100


Signal vs 12*FE+Chip
19500
19400
19300
19200
19100
19000
18900
0
20
40
60
80
100


Signal RMS vs 12*FE+Chip
30
25
20
15
10
5
0
20
40
60
80
100