CALICE ECAL Readout Electronics: VFE PCB Interface Specification

June 15, 2004

1 Introduction

The CALICE electromagnetic calorimeter (ECAL) will consist of 30 layers of silicon diodes. Each layer comprises a 3×3 array of silicon diode wafers, each containing a 6×6 array of diodes. Each diode needs to be read out and so corresponds to a channel. Hence, each wafer contains 36 channels, each layer contains $36 \times 9 = 324$ channels and the whole prototype is $324 \times 30 = 9720$ channels.

The silicon wafers will be mounted onto very-front-end cards (VFE PCB). Each VFE PCB can hold up to 6 wafers in a 2×3 array. Each layer will therefore consist of one VFE PCB fully-populated with 6 wafers and one VFE PCB half-populated with 3 wafers in a 1×3 array. Because the VFE PCBs will be physically mounted with their orientation alternating in each layer between top and bottom side facing forwards, then the 3 wafers in the half-populated VFE PCB will be alternating between the two possible 1×3 arrays. Hence, there will be 3 different types of VFE PCB; fully-populated, left-hand half-populated and right-hand half-populated; these are shown in Fig. 1. There are 60 VFE PCB's in total, 30 fully-populated, 15 left half-populated and 15 right half-populated, with each layer containing one fully-populated and one half-populated VFE PCB.

The wafers will be read out using VFE FLC_PHY3 chips, each reading 18 channels. Hence, there will be six or twelve VFE chips per VFE PCB. The 18 channels are multiplexed onto a single output line per VFE chip. The mapping of channels to chips is shown in Fig. 2. The VFE chip will also accept a calibration signal which is used to inject a pulse at the chip input.

The interface to the readout elecronics is the connector on the VFE PCB which supplies the driving signals for the VFE PCB and takes the output signals. The power for the VFE PCB is supplied separately.

2 Signals

The readout electronics will have an independent ground from the VFE PCB's. Hence, all signals on the PCB connector which provide the interface to the readout electronics are differential. The connector shield will be grounded at the readout board end and will have a $100\,\Omega$ resistor to ground at the VFE PCB end.

Table 1 lists the numbers and types of signals to and from a fully-populated VFE PCB.
Notes:

1. All LVDS signals will have the standard $+1.2\,\mathrm{V}$ quiescent level.

2. The gain selection switches between gains of $\times 1$ (level high) and $\times 10$ (level low).

3. The LED control simply lights the VFE PCB LED when set high.

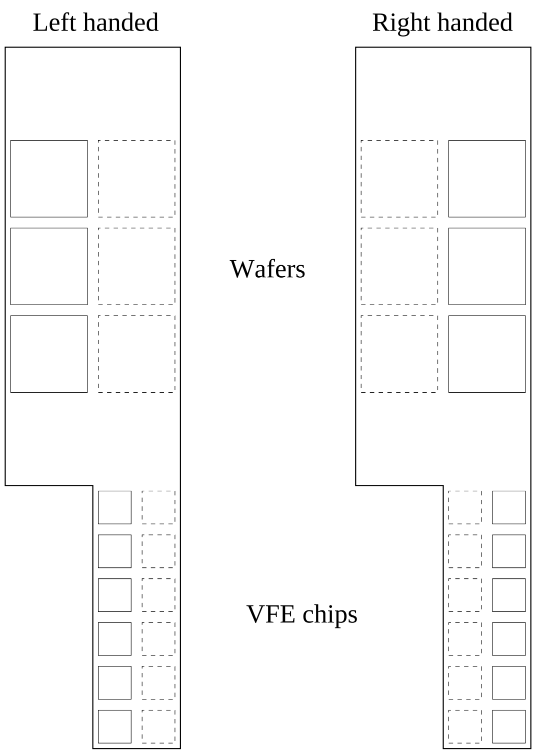

Figure 1: Left-handed and right-handed versions of the VFE PCB. The unmounted wafers and VFE chips are shown dashed. The fully populated version has all 6 wafers and 12 VFE chips mounted.

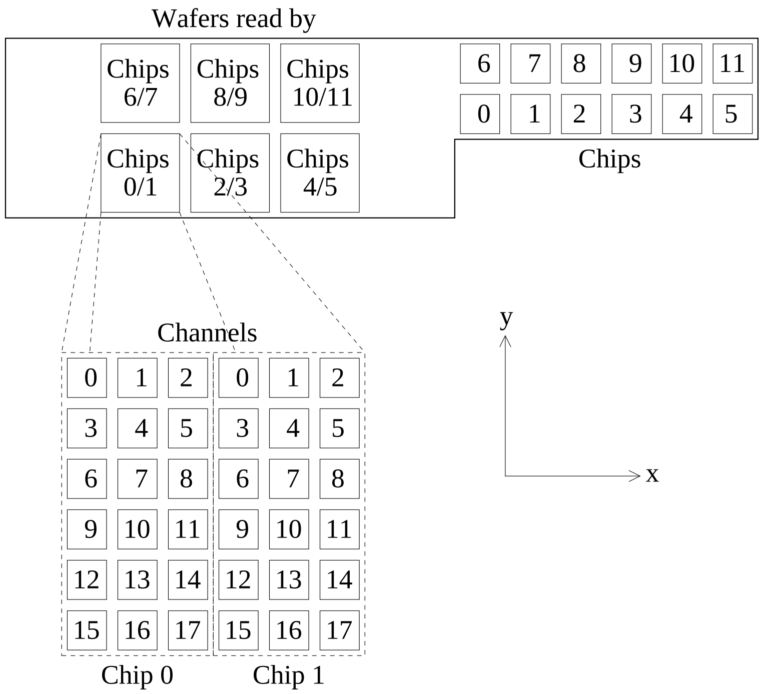

Figure 2: Chip and channel numbering for the VFE PCB. Within the PCB, the x and y locations are given (in integer arithmetic) by `x=3*(chip%6)+(chan%3)` and `y=6*(chip/6)-(chan/3)+5`.

Signal (Name)	I/O	Type	Specification	Number	Pins	Notes
Sample-and-hold (HOLD)	I	Digital	Bus LVDS	1	2	1
Shift register reset (RESET)	I	Digital	Bus LVDS	1	2	1
Shift register input (SRIN)	I	Digital	Bus LVDS	1	2	1
Shift register multiplex clock (CLOCK)	I	Digital	Bus LVDS	1	2	1
Gain selection (GAIN_SW)	I	Digital	Bus LVDS	1	2	1,2
LED control (ADDRESS)	I	Digital	Bus LVDS	1	2	1,3
Shift register output (SROUT)	O	Digital	(Bus?) LVDS	1	2	1,4
VFE PCB identification (TYPE0-3)	O	Digital	(Bus?) LVDS	4	8	1,5
Channel signal output (OUTPUT1-12)	O	Analogue	Diff. $0 - 2.5\,\mathrm{V}$	12	24	6,7
Calibration timing strobe (TCALIB1-2)	I	Digital	Bus LVDS	2	4	1,8
Calibration group selection (ENABLE1-6)	I	Digital	Bus LVDS	6	12	1,8
Calibration signal level (VCALIB)	I	Analogue	Diff. $0 - 2.5\,\mathrm{V}$	1	2	9
Total				32	64	

Table 1: Signals to ("I") and from ("O") the VFE PCB.

4. The shift register output signal is the AND of the outputs from the twelve VFE chips on the VFE PCB. For half-populated VFE PCBs, the six unused AND inputs will be pulled high.

5. The VFE PCB identification indicates the type of VFE PCB. For a fully populated board, the type bits are 1011 (MSB to LSB), for left-handed they are 1010, and for right-handed they are 1001.

6. The range of the channel signal output depends on the termination. The above $0 - 2.5\,\mathrm{V}$ range assumes $100\,\Omega$ termination within the readout electronics. The tolerance on this range is $\pm 0.1\,\mathrm{V}$ and the expected noise is $\sim 5\,\mathrm{mV}$.

7. The twelve channel signal outputs each correspond to the output of one VFE chip. OUTPUT1 corresponds to chip 0, etc. For half-populated VFE PCBs, only six of these channel signal outputs will be used.

8. The calibration group select value sets which group of channels to calibrate. The 18 channels per VFE chip are divided into six groups of three channels each. These six groups can be selected bitwise; the same group is tested simultaneously on all VFE chips. The two calibration timing strobe signals allow a selection of the two banks of VFE chips corresponding to half-populated boards.

9. The same calibration voltage is used for all VFE chips on the board. The calibration signal level dynamic range and precision must be at least at good as that for the channel signal output.

3 Timing

The time-dependent signals are shown in Fig. 3. The gain selection, calibration group select lines, calibration signal level lines and VFE PCB identification lines are constant during data capture and transfer.

The LED control line can be operated independently of any of the above and so can change at any time, as desired.

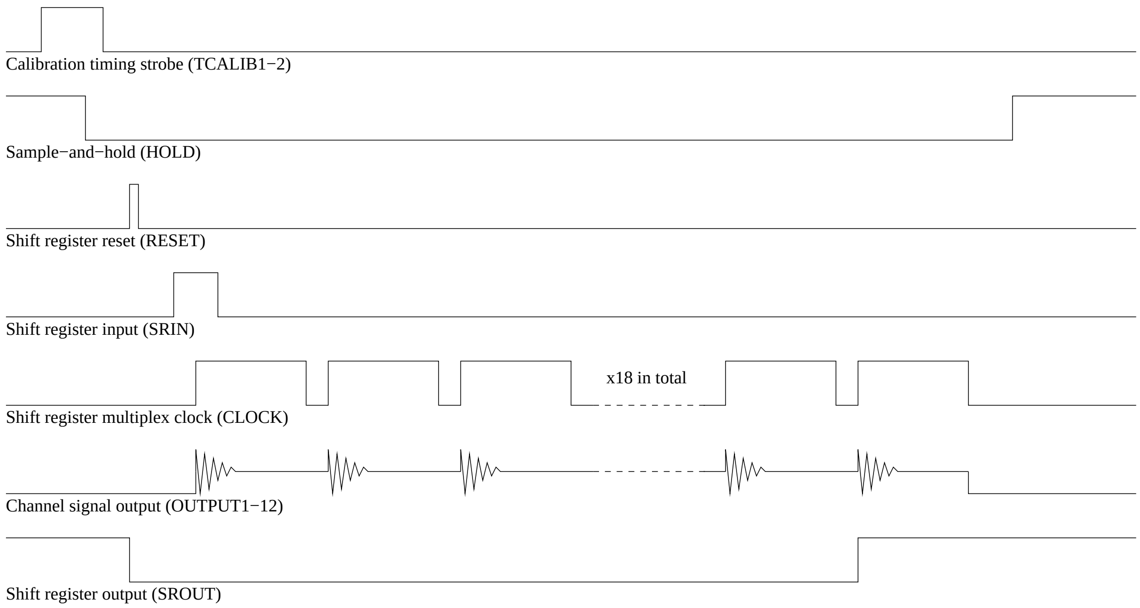

Figure 3: Time-dependent signals to and from the VFE PCB. The gain select, calibration group select, signal level and board identification signals are constant throughout this sequence and so are not shown.

The exact timing requirements of these signals are set by the VFE PCB but have not yet been specified.
Notes:

1. The calibration timing strobe is only present if calibrating. It must stay high until after the sample-and-hold goes low.
2. The timing between the start of the sequence (given by the rising edge of the trigger input) or, if calibrating, the rising edge of the calibration timing strobe, to the sample-and-hold must be accurately adjustable to $\leq$ 10ns.
3. The sample-and-hold must stay low until all channels have been multiplexed out.
4. The shift register input must overlap with the first shift register clock.
5. The shift register clock speed must be $\leq$ 5MHz.
6. The shift register output appears on the rising edge of the 18th multiplex clock. Unless extra clocks are sent, it stays on until the shift register is reset at the start of the next sequence.

4 Connectors and cables

The physical thickness of the VFE PCB and connector cannot exceed 8mm due to space contraints. The connector will be the same 68-pin mini-SCSI connector as will be used at the readout electronics end.

Each readout board will handle up to eight cables of fully-populated VFE PCBs, i.e. $8 \times 12 \times 18 = 1728$ channels. There will be 16 connectors per board in 8 pairs. Each pair can be used for one fully-populated VFE PCB cable or two half-populated VFE PCB cables, one left-handed and one right-handed.

The cable should be twisted pair and 3m long. There are no radiation-hard requirements but the cable should meet CERN/DESY specifications for safety.

Table 2 lists the signals on the VFE PCB connector for the three types of VFE PCB.

Connector	VFE PCB Signal		
Pair	Fully-populated	Left Half-populated	Right Half-populated
35,1	OUTPUT1+,−	OUTPUT1+,−	Unconnected????
36,2	OUTPUT7+,−	Unconnected????	OUTPUT7+,−
37,3	Unconnected	Unconnected	Unconnected
38,4	OUTPUT2+,−	OUTPUT2+,−	Unconnected????
39,5	OUTPUT8+,−	Unconnected????	OUTPUT8+,−
40,6	HOLD+,−	HOLD+,−	HOLD+,−
41,7	VCALIB+,−	VCALIB+,−	VCALIB+,−
42,8	SRIN+,−	SRIN+,−	SRIN+,−
43,9	RESET+,−	RESET+,−	RESET+,−
44,10	ENABLE1+,−	ENABLE1+,−	ENABLE1+,−
45,11	ENABLE2+,−	ENABLE2+,−	ENABLE2+,−
46,12	ENABLE3+,−	ENABLE3+,−	ENABLE3+,−
47,13	CLOCK+,−	CLOCK+,−	CLOCK+,−
48,14	OUTPUT3+,−	OUTPUT3+,−	Unconnected????
49,15	OUTPUT9+,−	Unconnected????	OUTPUT9+,−
50,16	ENABLE4+,−	ENABLE4+,−	ENABLE4+,−
51,17	ENABLE5+,−	ENABLE5+,−	ENABLE5+,−
52,18	ENABLE6+,−	ENABLE6+,−	ENABLE6+,−
53,19	Unconnected	Unconnected	Unconnected
54,20	OUTPUT4+,−	OUTPUT4+,−	Unconnected????
55,21	OUTPUT10+,−	Unconnected????	OUTPUT10+,−
56,22	SROUT+,−	SROUT+,−	SROUT+,−
57,23	ADDRESS+,−	ADDRESS+,−	ADDRESS+,−
58,24	GAIN_SW+,−	GAIN_SW+,−	GAIN_SW+,−
59,25	TCALIB1+,−	TCALIB1+,−	Unconnected????
60,26	TCALIB2+,−	Unconnected????	TCALIB2+,−
61,27	TYPE0+,−	TYPE0+,−	TYPE0+,−
62,28	TYPE1+,−	TYPE1+,−	TYPE1+,−
63,29	TYPE2+,−	TYPE2+,−	TYPE2+,−
64,30	OUTPUT5+,−	OUTPUT5+,−	Unconnected????
65,31	OUTPUT11+,−	Unconnected????	OUTPUT11+,−
66,32	TYPE3+,−	TYPE3+,−	TYPE3+,−
67,33	OUTPUT6+,−	OUTPUT6+,−	Unconnected????
68,34	OUTPUT12+,−	Unconnected????	OUTPUT12+,−

Table 2: Signals on VFE PCB connector.